

Compact, Standard-Performance TTL Delay Lines

*HTTL
8-pin DIP*

- 5 to 500 ns delays available.
- Five equal taps in 20% increments of total delay.
- Temperature coefficient ± 2 ns or $\pm 4\%$ (whichever is greater) at maximum delay, 0 to 70°C.
- Compatible with Schottky TTL, low-power Schottky TTL, FACT, AS, ALS and FAST logic circuits.
- Transfer-molded packaging for highest reliability.
- Designed for leading edge timing. Trailing edge timing available.
- Supply voltage + 5Vdc.
- Standard size (excluding leads) — 0.5" x 0.3" x 0.25" (L x W x H).
- 8-pin DIP.

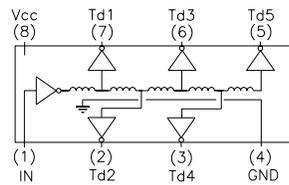
MODEL HTTLDL ACTIVE TTL DELAY LINES

PART NO.	TAP DELAYS (ns)					ALL TAPS (Max.)	
	T _{D1}	T _{D2}	T _{D3}	T _{D4}	T _{D5}	T _{RO}	T _{FD}
HTTLDL025	5.0	10.0	15.0	20.0	25.0	2.0	2.0
HTTLDL050	10.0	20.0	30.0	40.0	50.0	2.0	2.0
HTTLDL075	15.0	30.0	45.0	60.0	75.0	2.0	2.0
HTTLDL100	20.0	40.0	60.0	80.0	100.0	2.0	5.0
HTTLDL125	25.0	50.0	75.0	100.0	125.0	2.0	6.0
HTTLDL150	30.00	60.0	90.0	120.0	150.0	2.0	7.0
HTTLDL200	40.00	80.0	120.0	160.0	200.0	2.0	8.0
HTTLDL250	50.00	100.0	150.0	200.0	250.0	2.0	9.0
HTTLDL500	100.0	200.0	300.0	400.0	500.0	2.0	9.0

Delay Characteristics measured at $V_{CC} = 5.0V$, 25°C, no load.
 Delay Tolerance ± 2 ns or 5%, whichever is greater.
 Rise time measured @ 0.8V to 2.0V levels.
 For minimum input pulse width -- contact factory.

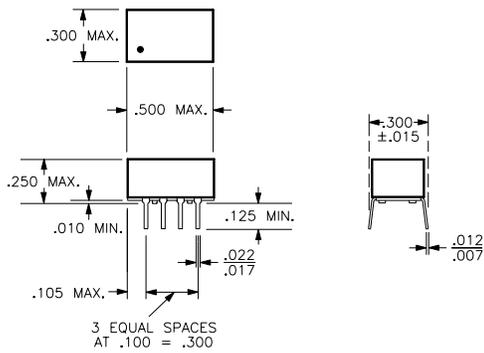


SCHEMATIC



HTTL
8-pin DIP

MECHANICAL OUTLINE



Notes

- Only the pins specified in the schematics are provided with each package.
- Pin numbers shown are for reference only and are not necessarily marked on unit.
- Lead material is electro tin plated (alloy 42) or solder dipped.
- All specifications are subject to change without notice.

HTTL-7