# RTL8169S-32/RTL8169S-64
# RTL8110S-32/RTL8110S-64

## INTEGRATED GIGABIT ETHERNET CONTROLLER

## DATASHEET

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This document is intended for use by the software engineer when programming for Realtek RTL8169S/RTL8110S-32 & RTL8169S/RTL8110S-64 controller chips. Information pertaining to the hardware design of products using these chips is contained in a separate document.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

## REVISION HISTORY

| Revision | Release Date | Summary |
|---|---|---|
| 1.0 | 2003/03/20 | First release. |
| 1.1 | 2003/04/12 | Revised pin name and pin assignments. |
| 1.2 | 2003/06/24 | Minor 233-pin TFBGA pin number corrections.<br>IEEE 802.3z changed to IEEE 802.3ab in General Description. |
| 1.3 | 2003/09/10 | Add the voltage variation to DC characteristics.<br>Add registers definition. |

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# 1. General Description

The Realtek RTL8169S/RTL8110S-32 and RTL8169S/RTL8110S-64 LOM Ethernet controllers combine a triple-speed IEEE 802.3 compliant media access controller (MAC) with a triple-speed Ethernet transceiver, 32(64*)-bit PCI bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, they offer high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The devices support the PCI v2.2 bus interface for host communications with power management and are compliant with the IEEE 802.3 specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. They also support an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space.

They also support the Advanced Configuration Power management Interface (ACPI)--power management for modern operating systems that are capable of Operating System directed Power Management (OSPM)--to achieve the most efficient power management possible.

In addition to the ACPI feature, the RTL8169S/RTL8110S-32 and RTL8169S/RTL8110S-64 support remote wake-up (including AMD Magic Packet, Re-LinkOk, and Microsoft® Wake-up frame) in both ACPI and APM (Advanced Power Management) environments. Also, the LWAKE pin provides four different output signals including active high, active low, positive pulse, and negative pulse. The versatility of the LWAKE pin provides motherboards with Wake-On-LAN (WOL) functionality. To support WOL from a deep power down state (e.g. D3cold, i.e. main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8169S/RTL8110S-32 and RTL8169S/RTL8110S-64.

The RTL8169S/RTL8110S is fully compliant with Microsoft® NDIS5 (IP, TCP, UDP) Checksum and Segmentation Task-offload features, and supports IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation as a server network card. Also, the devices boost their PCI performance by supporting PCI Memory Read Line & Memory Read Multiple when transmitting, and Memory Write and Invalidate when receiving. To better qualify as a server card, the RTL8169S/RTL8110S-32 and RTL8169S/RTL8110S-64 support the PCI Dual Address Cycle (DAC) command when the assigned buffers reside at a physical memory address higher than 4 Gigabytes.

* 233-PIN TFBGA package only.

# 2. Features

- Integrated 10/100/1000 transceiver
- Auto-Negotiation with Next page capability
- Supports PCI 2.2, 32-bit/64-bit (RTL8169S/RTL8110S-64 only), 33/66MHz
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Wake-on-LAN and remote wake-up support
- Microsoft® NDIS5 Checksum Offload (IP, TCP, UDP) and largesend offload support
- Supports Full Duplex flow control (IEEE 802.3x)
- Fully compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab
- Supports IEEE 802.1Q VLAN tagging
- Serial EEPROM
- 3.3V signaling, 5V PCI I/O tolerant
- Transmit/Receive FIFO (8K/64K) support
- Supports power down/link down power saving
- JTAG support
- 128-pin QFP/233-pin TFBGA package

# 3. System Applications

- Gigabit Ethernet on Motherboard – RTL8110S.
- Gigabit Ethernet Network Interface Cards/Workstation Cards – RTL8169S

# 4. Pin Assignments

## 4.1. RTL8169S-32 128-Pin QFP Pin Assignments

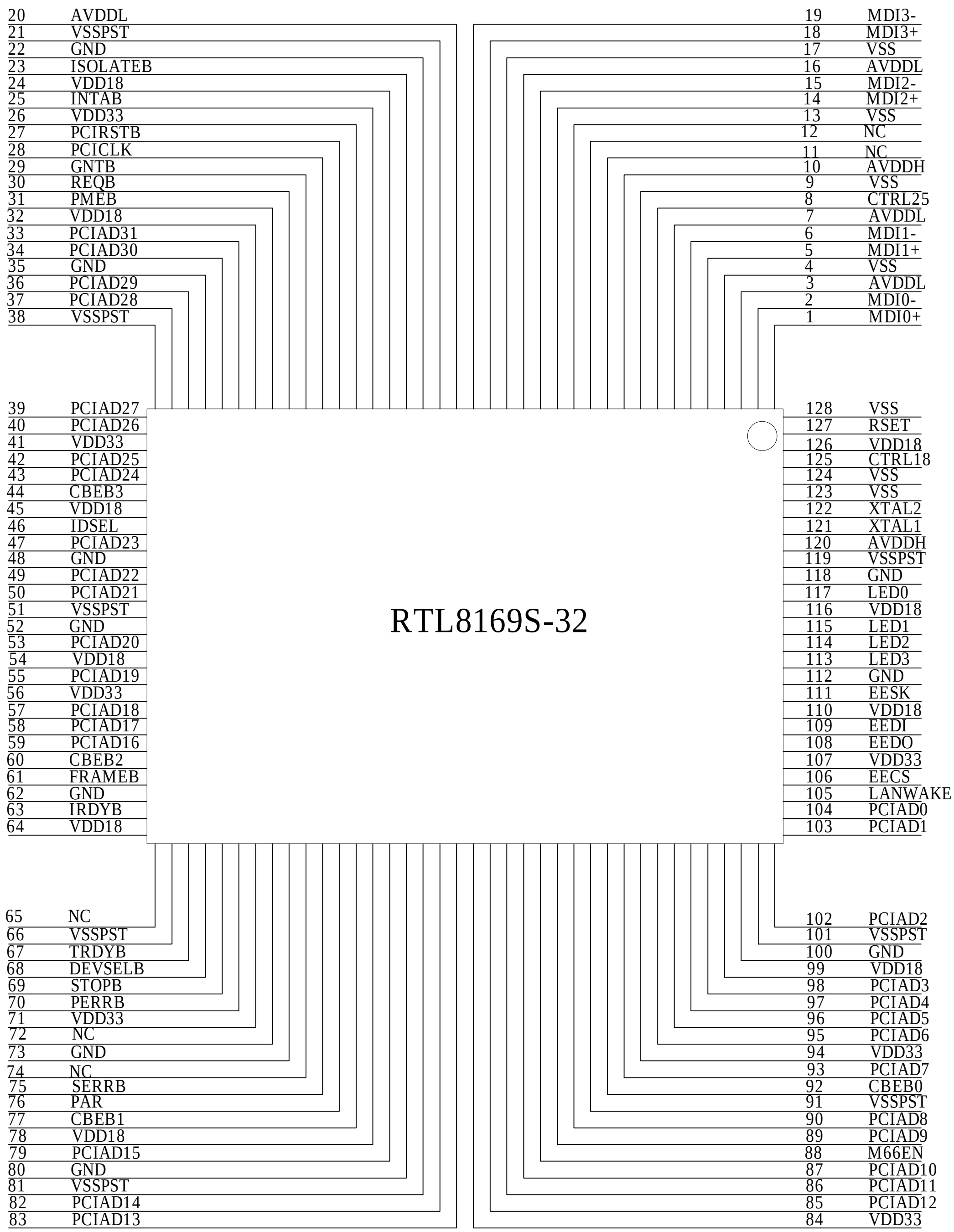



**Figure 1. RTL8169S-32 128-Pin QFP Pin Assignments**

## 4.2. RTL8169S-64 233-Pin TFBGA Pin Assignments

RTL8169S-64

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | NC | NC | NC | XTAL1 | XTAL2 | NC | NC | NC | NC | EESK | EEDO | LANWAKE | NC | AD3 | NC | AD6 |
| B | NC | NC | CTRL18 | NC | NC | NC | NC | NC | NC | VDD33 | EEDI | EECS | AD1 | NC | NC | AD5 | AD32 |
| C | NC | MDI0+ | AVDDL | VSS | VDD18 | AVDDH | VDD18 | VDD33 | VDD33 | LED0 | LED2 | AD0 | NC | AD2 | NC | AD7 | AD33 |
| D | MDI0- | MDI1+ | AVDDL | RSET | VSS | VSS | VSS | VDD18 | LED3 | LED1 | GND | GND | GND | GND | AD4 | CBEB0 | AD34 |
| E | MDI1- | AVDDH | VSS | CTRL25 | | | | | | | | | | GND | AD8 | AD35 | AD9 |
| F | MDI2+ | NC | NC | VSS | | | | | | | | | | VDD18 | VDD33 | AD36 | M66EN |
| G | MDI3+ | MDI2- | AVDDL | VSS | | | GND | GND | GND | GND | GND | | | GND | AD37 | AD10 | AD38 |
| H | VDD33 | MDI3- | AVDDL | VDD18 | | | GND | GND | GND | GND | GND | | | GND | VDD33 | AD11 | AD39 |
| J | ISOLATEB | VDD33 | VDD33 | GND | | | GND | GND | GND | GND | GND | | | GND | AD12 | AD40 | AD13 |
| K | NC | ACK64B | INTAB | GND | | | GND | GND | GND | GND | GND | | | VDD18 | VDD33 | AD14 | AD41 |
| L | NC | REQ64B | PCIRSTB | VDD18 | | | GND | GND | GND | GND | GND | | | GND | VDD33 | AD15 | CBEB1 |
| M | PCICLK | CBEB7 | CBEB6 | GND | | | | | | | | | | GND | AD42 | PAR | AD43 |
| N | CBEB5 | GNTB | NC | GND | | | | | | | | | | GND | SERRB | AD44 | NC |
| P | NC | REQB | PMEB | GND | GND | VDD18 | GND | GND | VDD18 | GND | GND | VDD18 | GND | GND | NC | AD45 | PERRB |
| R | CBEB4 | PAR64 | AD28 | AD62 | AD25 | CBEB3 | VDD33 | VDD33 | AD18 | VDD33 | VDD33 | AD50 | FRAMEB | IRDY | AD49 | TRDYB | AD46 |
| T | AD31 | AD30 | AD63 | AD27 | AD60 | AD59 | AD23 | AD22 | AD21 | AD20 | AD19 | AD17 | CBEB2 | AD51 | NC | DEVSELB | STOPB |
| U | NC | AD29 | AD26 | AD61 | AD24 | IDSEL | AD58 | AD57 | AD56 | NC | AD55 | AD54 | AD53 | AD16 | AD52 | AD48 | AD47 |

**Figure 2. RTL8169S-64 233-Pin TFBGA Pin Assignments**

## 4.3. RTL8110S-32 128-Pin QFP Pin Assignments

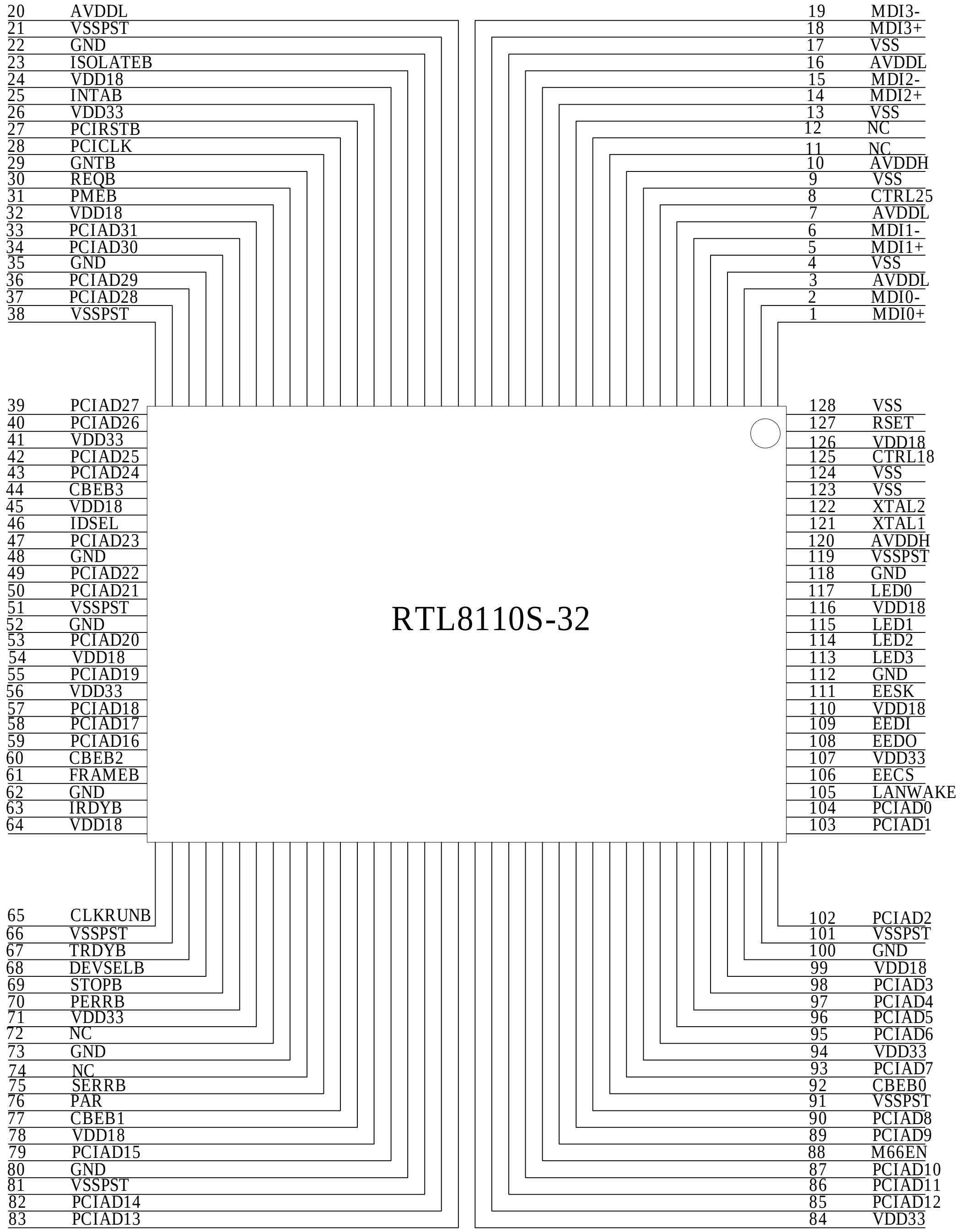



**Figure 3. RTL8110S-32 128-Pin QFP Pin Assignments**

## 4.4. RTL8110S-64 233-Pin TFBGA Pin Assignments

RTL8110S-64

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | NC | NC | NC | XTAL1 | XTAL2 | NC | NC | NC | NC | EESK | EEDO | LANWAKE | NC | AD3 | NC | AD6 |
| B | NC | NC | CTRL18 | NC | NC | NC | NC | NC | NC | VDD33 | EEDI | EECS | AD1 | NC | NC | AD5 | AD32 |
| C | NC | MDI0+ | AVDDL | VSS | VDD18 | AVDDH | VDD18 | VDD33 | VDD33 | LED0 | LED2 | AD0 | NC | AD2 | NC | AD7 | AD33 |
| D | MDI0- | MDI1+ | AVDDL | RSET | VSS | VSS | VSS | VDD18 | LED3 | LED1 | GND | GND | GND | GND | AD4 | CBEB0 | AD34 |
| E | MDI1- | AVDDH | VSS | CTRL25 | | | | | | | | | | GND | AD8 | AD35 | AD9 |
| F | MDI2+ | NC | NC | VSS | | | | | | | | | | VDD18 | VDD33 | AD36 | M66EN |
| G | MDI3+ | MDI2- | AVDDL | VSS | | | GND | GND | GND | GND | GND | | | GND | AD37 | AD10 | AD38 |
| H | VDD33 | MDI3- | AVDDL | VDD18 | | | GND | GND | GND | GND | GND | | | GND | VDD33 | AD11 | AD39 |
| J | ISOLATEB | VDD33 | VDD33 | GND | | | GND | GND | GND | GND | GND | | | GND | AD12 | AD40 | AD13 |
| K | NC | ACK64B | INTAB | GND | | | GND | GND | GND | GND | GND | | | VDD18 | VDD33 | AD14 | AD41 |
| L | NC | REQ64B | PCIRSTB | VDD18 | | | GND | GND | GND | GND | GND | | | GND | VDD33 | AD15 | CBEB1 |
| M | PCICLK | CBEB7 | CBEB6 | GND | | | | | | | | | | GND | AD42 | PAR | AD43 |
| N | CBEB5 | GNTB | NC | GND | | | | | | | | | | GND | SERRB | AD44 | NC |
| P | NC | REQB | PMEB | GND | GND | VDD18 | GND | GND | VDD18 | GND | GND | VDD18 | GND | GND | NC | AD45 | PERRB |
| R | CBEB4 | PAR64 | AD28 | AD62 | AD25 | CBEB3 | VDD33 | VDD33 | AD18 | VDD33 | VDD33 | AD50 | FRAMEB | IRDY | AD49 | TRDYB | AD46 |
| T | AD31 | AD30 | AD63 | AD27 | AD60 | AD59 | AD23 | AD22 | AD21 | AD20 | AD19 | AD17 | CBEB2 | AD51 | CLKRUNB | DEVSELB | STOPB |
| U | NC | AD29 | AD26 | AD61 | AD24 | IDSEL | AD58 | AD57 | AD56 | NC | AD55 | AD54 | AD53 | AD16 | AD52 | AD48 | AD47 |

**Figure 4. RTL8110S-64 233-Pin TFBGA Pin Assignments**

# 5. Pin Descriptions

The following signal type codes are used in the tables:
I: Input.
O: Output
T/S: Tri-State bi-directional input/output pin.
S/T/S: Sustained Tri-State.
O/D: Open Drain.

## 5.1. *Power Management/Isolation*

**Table 1. Power Management/Isolation**

<table>
<tr><th>Symbol</th><th>Type</th><th>Pin No (128QFP)</th><th>Pin No (233BGA)</th><th>Description</th></tr>
<tr><td>PMEB (PME#)</td><td>O/D</td><td>31</td><td>P3</td><td>Power Management Event: Open drain, active low.<br>Used to request a change in the current power management state and/or to indicate that a power management event has occurred.</td></tr>
<tr><td>ISOLATEB (ISOLATE#)</td><td>I</td><td>23</td><td>J1</td><td>Isolate Pin: Active low.<br>Used to isolate the RTL8169S/RTL8110S from the PCI bus. The RTL8169S/RTL8110S will not drive its PCI outputs (excluding PME#) and will not sample its PCI input (including PCIRSTB and PCICLK) as long as the Isolate pin is asserted.</td></tr>
<tr><td>LANWAKE</td><td>O</td><td>105</td><td>A13</td><td>LAN WAKE-UP Signal (When CardB_En=0, bit2 Config3):<br>This signal is used to inform the motherboard to execute the wake-up process. The motherboard must support Wake-On-LAN (WOL). There are 4 choices of output that may be asserted from the LANWAKE pin (active high, active low, positive pulse, and negative pulse). We can configure the LANWAKE output via two CONFIG bits: LWACT(Config1.4) and LWPTN(Config4.2).
<table>
<tr><td colspan="2" rowspan="2">LWAKE Output</td><td colspan="2">LWACT</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td rowspan="2">LWPTN</td><td>0</td><td>Active high</td><td>Active low</td></tr>
<tr><td>1</td><td>Positive pulse</td><td>Negative pulse</td></tr>
</table>
The default output is an active high signal. Once a PME event is received, the LANWAKE and PMEB assert at the same time when the LWPME (bit4, CONFIG4) is set to 0. If the LWPME is set to 1, the LANWAKE asserts only when the PMEB asserts and ISOLATEB is low.</td></tr>
</table>

## 5.2. PCI Interface

**Table 2. PCI Interface**

| Symbol | Type | Pin No. (128QFP) | Pin No. (233BGA) | Description |
|---|---|---|---|---|
| PCIADPIN63-32 | T/S | | T3, R4, U4, T5, T6, U7, U8, U9, U11, U12, U13, U15, T14, R12, R15, U16, U17, R17, P16, N16, M17, M15, K17, J16, H17, G17, G15, F16, E16, D17, C17, B17 | **AD63-32: High 32-bit PCI address and data multiplexed pins.** Address and Data are multiplexed on the same pins and provide 32 additional bits. During an address phase (when using the DAC command and when REQ64B is asserted), the upper 32-bits of a 64-bit address are transferred; otherwise, these bits are reserved but are stable and undetermined. During a data phase, an additional 32-bits of data are transferred when a 64-bit transaction has been negotiated by the assertion of REQ64B and ACK64B. |
| PCIADPIN31-0 | T/S | 33, 34, 36, 37, 39, 40, 42, 43, 47, 49, 50, 53, 55, 57, 58, 59, 79, 82, 83, 85, 86, 87, 89, 90, 93, 95, 96, 97, 98, 102, 103, 104 | T1, T2, U2, R3, T4, U3, R5, U5, T7, T8, T9, T10, T11, R9, T12, U14, L16, K16, J17, J15, H16, G16, E17, E15, C16, A17, B16, D15, A15, C14, B13, C12 | **AD31-0: Low 32-bit PCI address and data multiplexed pins.** The address phase is the first clock cycle in which FRAMEB is asserted. During the address phase, AD31-0 contains a physical address (32 bits). For I/O, this is a byte address, and for configuration and memory, it is a double-word address. The RTL8169S/RTL8110S supports both big-endian and little-endian byte ordering. Write data is stable and valid when IRDYB is asserted. Read data is stable and valid when TRDYB is asserted. Data I is transferred during those clocks where both IRDYB and TRDYB are asserted. |
| CBEBPIN7-4 | T/S | | M2, M3, N1, R1 | **PCI bus command and byte enables multiplexed pins.** During the address phase of a transaction, CBEBPIN7-4 define the bus command. During the data phase, CBEBPIN7-4 are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. CBEBPIN4 applies to byte 4, and CBEBPIN7 applies to byte 7. |
| CBEBPIN3-0 | T/S | 44, 60, 77, 92 | R6, T13, L17, D16 | **PCI bus command and byte enables multiplexed pins.** During the address phase of a transaction, CBEBPIN3-0 define the bus command. During the data phase, CBEBPIN3-0 are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. CBEBPIN0 applies to byte 0, and CBEBPIN3 applies to byte 3. |

| Symbol | Type | Pin No. (128QFP) | Pin No. (233BGA) | Description |
|---|---|---|---|---|
| PCICLK | I | 28 | M1 | **PCI clock:** This clock input provides timing for all PCI transactions and is input to the PCI device. Supports up to a 66MHz PCI clock. |
| CLKRUNB | I/O | 65 | T15 | **Clock Run:** This signal is used by the RTL8110S to request starting (or speeding up) of the PCICLK clock. CLKRUNB also indicates the clock status. For the RTL8110S, CLKRUNB is an open drain output as well as an input. The RTL8110S requests the central resource to start, speed up, or maintain the interface clock by the assertion of CLKRUNB. For the host system, it is an S/T/S signal. The host system (central resource) is responsible for maintaining CLKRUNB asserted, and for driving it high to the negated (deasserted) state.<br>For RTL8169S-32/64, this pin is NC pin. |
| DEVSELB | S/T/S | 68 | T16 | **Device Select:** As a bus master, the RTL8169S/RTL8110S samples this signal to insure that a PCI target recognizes the destination address for the data transfer. As a target, the RTL8169S/RTL8110S asserts this signal low when it recognizes its target address after FRAMEB is asserted. |
| FRAMEB | S/T/S | 61 | R13 | **Cycle Frame:** As a bus master, this pin indicates the beginning and duration of an access. FRAMEB is asserted low to indicate the start of a bus transaction. While FRAMEB is asserted, data transfer continues. When FRAMEB is de-asserted, the transaction is in the final data phase.<br>As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it. |
| GNTB | I | 29 | N2 | **Grant:** This signal is asserted low to indicate to the RTL8169S/RTL8110S that the central arbiter has granted the ownership of the bus to the RTL8169S/RTL8110S. This input is used when the device is acting as a bus master. |
| REQB | T/S | 30 | P2 | **Request:** The RTL8169S/RTL8110S will assert this signal low to request the ownership of the bus from the central arbiter. |
| IDSEL | I | 46 | U6 | **Initialization Device Select**: This pin allows the device to identify when configuration read/write transactions are intended for it. |
| INTAB | O/D | 25 | K3 | **Interrupt A:** Used to request an interrupt. It is asserted low when an interrupt condition occurs, as defined by the Interrupt Status, Interrupt Mask. |

| Symbol | Type | Pin No. (128QFP) | Pin No. (233BGA) | Description |
|---|---|---|---|---|
| IRDYB | S/T/S | 63 | R14 | **Initiator Ready**: This indicates the initiating agent's ability to complete the current data phase of the transaction.<br>As a bus master, this signal will be asserted low when the device is ready to complete the current data phase transaction. This signal is used in conjunction with the TRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low. As a target, this signal indicates that the master has put data on the bus. |
| TRDYB | S/T/S | 67 | R16 | **Target Ready:** This indicates the target agent's ability to complete the current phase of the transaction.<br>As a bus master, this signal indicates that the target is ready for the data during write operations and with the data during read operations. As a target, this signal will be asserted low when the (slave) device is ready to complete the current data phase transaction. This signal is used in conjunction with the IRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low. |
| PAR | T/S | 76 | M16 | **Parity:** This signal indicates even parity across PCIADPIN31-0 and CBEB3-0 including the PAR pin. PAR is stable and valid one clock after each address phase. For data phase, PAR is stable and valid one clock after either IRDYB is asserted on a write transaction or TRDYB is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. As a bus master, PAR is asserted during address and write data phases. As a target, PAR is asserted during read data phases. |
| M66EN | I | 88 | F17 | **66MHZ_ENABLE:** This pin indicates to the device whether the bus segment is operating at 66 or 33MHz. When this pin (active high) is asserted, the current PCI bus segment that the device resides on operates in 66-MHz mode. If this pin is de-asserted, the current PCI bus segment operates in 33-MHz mode. |
| PERRB | S/T/S | 70 | P17 | **Parity Error:** This pin is used to report data parity errors during all PCI transactions except a Special Cycle. PERRB is driven active (low) two clocks after a data parity error is detected by the device receiving data, and the minimum duration of PERRB is one clock for each data phase with parity error detected. |
| SERRB | O/D | 75 | N15 | **System Error:** If an address parity error is detected and Configuration Space Status register bit 15 (detected parity error) is enabled, the device asserts the SERRB pin low and bit 14 of the Status register in Configuration Space. |
| STOPB | S/T/S | 69 | T17 | **Stop:** Indicates that the current target is requesting the master to stop the current transaction. |

| Symbol | Type | Pin No. (128QFP) | Pin No. (233BGA) | Description |
|---|---|---|---|---|
| PCIRSTB | I | 27 | L3 | **Reset:** When PCIRSTB is asserted low, the device performs an internal system hardware reset. PCIRSTB must be held for a minimum period of 120 ns. |
| ACK64B | S/T/S | | K2 | **Acknowledge 64-bit Transfer:** When actively driven by a device that has positively decoded its address as the target of the current access, indicates the target is willing to transfer data using 64 bits. ACK64B has the same timing as DEVSELB. |
| REQ64B | S/T/S | | L2 | **Request 64-bit Transfer:** When asserted by the current bus master, indicates it desires to transfer data using 64 bits. REQ64B also has the same timing as FRAMEB. |
| PAR64 | T/S | | R2 | **Parity Upper DWORD** is an even parity bit that protects AD[64:32] and C/BE[7:4]. PAR64 must be valid one clock after each address phase on any transaction in which REQ64B is asserted. |

## *5.3. EEPROM*

**Table 3. EEPROM**

| Symbol | Type | Pin No (128QFP) | Pin No (233BGA) | Description |
|---|---|---|---|---|
| EESK | O | 111 | A11 | Serial data clock |
| EEDI/AUX | I | 109 | B11 | **EEDI:** Serial data input<br>**AUX:** Input pin to detect if Aux. Power exists or not on initial power-on.<br>This pin should be connected to EEPROM. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to aux. power via a resistor. If this pin is not pulled high to Aux. Power, the RTL8169S/RTL8110S assumes that no Aux. Power exists. |
| EEDO | O | 108 | A12 | Serial data output |
| EECS/BROMCSB | O | 106 | B12 | **EECS:** EEPROM chip select<br>**BROMCSB:** This is the chip select signal of the Boot PROM. |

## *5.4. Transceiver Interface*

**Table 4. Transceiver Interface**

| Symbol | Type | Pin No (128QFP) | Pin No (233BGA) | Description |
|---|---|---|---|---|
| MDI[0]+ | I/O | 1 | C2 | In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.<br>In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. |
| MDI[0]– | I/O | 2 | D1 | |

| Symbol | Type | Pin No (128QFP) | Pin No (233BGA) | Description |
|---|---|---|---|---|
| MDI[1]+ | I/O | 5 | D2 | In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.<br>In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. |
| MDI[1]– | I/O | 6 | E1 | |
| MDI[2]+ | I/O | 14 | F1 | In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair.<br>In MDI crossover mode, this pair acts as the BI_DD+/- pair. |
| MDI[2]– | I/O | 15 | G2 | |
| MDI[3]+ | I/O | 18 | G1 | In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair.<br>In MDI crossover mode, this pair acts as the BI_DC+/- pair. |
| MDI[3]– | I/O | 19 | H2 | |

## 5.5. *Clock*

**Table 5. Clock**

| Symbol | Type | Pin No (128QFP) | Pin No (233BGA) | Description |
|---|---|---|---|---|
| Xtal1 | I | 121 | A5 | Input of 25MHz clock reference. |
| Xtal2 | O | 122 | A6 | output of 25MHz clock reference. |

## 5.6. *Regulator & Reference*

**Table 6. Regulator & Reference**

| Symbol | Type | Pin No (128QFP) | Pin No (233BGA) | Description |
|---|---|---|---|---|
| CTRL25 | O | 8 | E4 | Regulator Control. Voltage control to external 2.5V regulator |
| CTRL18 | O | 125 | B3 | Regulator Control. Voltage control to external 1.8V regulator |
| RSET | I | 127 | D4 | Reference. External Resistor Reference. |

## 5.7. *LEDs*

**Table 7. LEDs**

<table>
<tr><th>Symbol</th><th>Type</th><th>Pin No (128QFP)</th><th>Pin No (233BGA)</th><th>Description</th></tr>
<tr><td>LED0</td><td>O</td><td>117</td><td>C10</td><td rowspan="3"><table><tr><th>LEDS 1-0</th><th>00</th><th>01</th><th>10</th><th>11</th></tr></table></td></tr>
<tr><td>LED1</td><td>O</td><td>115</td><td>D10</td></tr>
<tr><td>LED2</td><td>O</td><td>114</td><td>C11</td></tr>
</table>

<table>
<tr><td>LED3</td><td>O</td><td>113</td><td>D9</td><td>
<table>
<tr><td>LED0</td><td>Tx/Rx</td><td>ACT(Tx/Rx)</td><td>Tx</td><td>LINK10/ ACT</td></tr>
<tr><td>LED1</td><td>LINK 100</td><td>LINK10/100/ 1000</td><td>LINK10/100 /1000</td><td>LINK100/ ACT</td></tr>
<tr><td>LED2</td><td>LINK 10</td><td>FULL</td><td>Rx</td><td>FULL</td></tr>
<tr><td>LED3</td><td>LINK 1000</td><td>-</td><td>FULL</td><td>LINK1000/ ACT</td></tr>
</table>
</td></tr>
</table>

*Note 1: During power down mode, the LED signals are logic high.*

*Note 2: LEDS1-0's initial value comes from 93C46/93C56.*

## *5.8. Power & Ground*

**Table 8. Power & Ground**

| Symbol | Type | Pin No (128QFP) | Pin No (233BGA) | Description |
|---|---|---|---|---|
| VDD18 | Power | 24, 32, 45, 54, 64, 78, 99, 110, 116,126 | C5, C7, D8, F14, H4, K14, L4, P6, P9, P12 | Digital 1.8V power supply. |
| VDD33 | Power | 26, 41, 56, 71, 84, 94, 107 | B10, C8, C9, F15, H1, H15, J2, J3, K15, L15, R7, R8, R10, R11 | Digital 3.3V power supply. |
| GND/VSSPST | Power | 21, 22, 35, 38, 48, 51, 52, 62, 66, 73, 80, 81, 91, 100, 101, 112, 118, 119 | D11, D12, D13, D14, E14, G7, G8, G9, G10, G11, G14, H7, H8, H9, H10, H11, H14, J4, J7, J8, J9, J10, J11, J14, K4, K7, K8, K9, K10, K11, L7, L8, L9, L10, L11, L14, M4, M14, N4, N14, P4, P5, P7, P8, P10, P11, P13, P14 | Digital Ground |
| AVDDL | Power | 3, 7, 16, 20 | C3, D3, G3, H3 | Analog 2.5V power supply. |
| AVDDH | Power | 10, 120 | E2, C6 | Analog 3.3V power supply. |
| VSS | Power | 4, 9, 13, 17, 123, 124, 128 | F4, G4, C4, D5, D6, D7, E3 | Analog Ground |

## *5.9. NC (Not Connected) Pins*

**Table 9. NC (Not Connected) Pins**

| Symbol | Type | Pin No (128QFP) | Pin No (233BGA) | Description |
|---|---|---|---|---|
| NC | | 11, 12, 72, 74 | A1, A2, A3, A4, A7, A8, A9, A10, A14, A16, B1, B2, B4, B5, B6, B7, B8, B9, B14, B15, C1, C13, C15, F2, F3, K1, L1, N3, N17, P1, P15, U1, U10 | Not Connected. |

# 6. Register Descriptions

The RTL8169S/RTL8110S provides the following set of operational registers mapped into PCI memory space or I/O space.

**Table 10. MAC Registers**

| Offset | R/W | Tag | Description |
|---|---|---|---|
| 0000h | R/W | IDR0 | **ID Register 0:** The ID registers 0-5 are only permitted to write by 4-byte access. Read access can be byte, word, or double word access. The initial value is autoloaded from EEPROM EthernetID field. |
| 0001h | R/W | IDR1 | **ID Register 1** |
| 0002h | R/W | IDR2 | **ID Register 2** |
| 0003h | R/W | IDR3 | **ID Register 3** |
| 0004h | R/W | IDR4 | **ID Register 4** |
| 0005h | R/W | IDR5 | **ID Register 5** |
| 0006h-0007h | - | - | **Reserved** |
| 0008h | R/W | MAR0 | **Multicast Register 0:** The MAR registers 0-7 are only permitted to write by 4-bye access. Read access can be byte, word, or double word access. Driver is responsible for initializing these registers. |
| 0009h | R/W | MAR1 | **Multicast Register 1** |
| 000Ah | R/W | MAR2 | **Multicast Register 2** |
| 000Bh | R/W | MAR3 | **Multicast Register 3** |
| 000Ch | R/W | MAR4 | **Multicast Register 4** |

| | | | |
|---|---|---|---|
| 000Dh | R/W | MAR5 | **Multicast Register 5** |
| 000Eh | R/W | MAR6 | **Multicast Register 6** |
| 000Fh | R/W | MAR7 | **Multicast Register 7** |
| 0010h-0017h | R/W | DTCCR | **Dump Tally Counter Command Register** (64-byte alignment) |
| 0018h-001Fh | - | - | **Reserved** |
| 0020h-0027h | R/W | TNPDS | **Transmit Normal Priority Descriptors**: Start address (64-bit). (256-byte alignment) |
| 0028h-002Fh | R/W | THPDS | **Transmit High Priority Descriptors:** Start address (64-bit). (256-byte alignment) |
| 0030h-0036h | - | - | **Reserved** |
| 0037h | R/W | CR | **Command Register** |
| 0038h | W | TPPoll | **Transmit Priority Polling register** |
| 0039h-003Bh | - | - | **Reserved** |
| 003Ch-003Dh | R/W | IMR | **Interrupt Mask Register** |
| 003Eh-003Fh | R/W | ISR | **Interrupt Status Register** |
| 0040h-0043h | R/W | TCR | **Transmit (Tx) Configuration Register** |
| 0044h-0047h | R/W | RCR | **Receive (Rx) Configuration Register** |
| 0048h-004Bh | R/W | TCTR | **Timer CounT Register:** This register contains a 32-bit general-purpose timer. Writing any value to this 32-bit register will reset the original timer and begin the count from zero. |
| 004Ch-004Fh | R/W | MPC | **Missed Packet Counter:** This 24-bit counter indicates the number of packets discarded due to Rx FIFO overflow. After a s/w reset, MPC is cleared. Only the lower 3 bytes are valid.<br>When any value is written to MPC, it will be reset. |
| 0050h | R/W | 9346CR | **93C46 (93C56) Command Register** |
| 0051h | R/W | CONFIG0 | **Configuration Register 0** |
| 0052h | R/W | CONFIG1 | **Configuration Register 1** |
| 0053h | R/W | CONFIG2 | **Configuration Register 2** |
| 0054h | R/W | CONFIG3 | **Configuration Register 3** |
| 0055h | R/W | CONFIG4 | **Configuration Register 4** |
| 0056h | R/W | CONFIG5 | **Configuration Register 5** |
| 0057h | - | - | **Reserved** |
| 0058h-005Bh | R /W | TimerInt | **Timer Interrupt Register:** Once having written a nonzero value to this register, the Timeout bit of ISR register will be set whenever the |

| | | | |
|---|---|---|---|
| | | | TCTR reaches to this value. The Timeout bit will never be set as long as TimerInt register is zero. |
| 005Ch-005Fh | - | - | **Reserved** |
| 0060h-0063h | R/W | PHYAR | **PHY Access Register** |
| 0064h-0067h | R/W | TBICSR0 | **TBI Control and Status Register** |
| 0068h-0069h | R/W | TBI_ANAR | **TBI Auto-Negotiation Advertisement Register** |
| 006Ah-006Bh | R | TBI_LPAR | **TBI Auto-Negotiation Link Partner Ability Register** |
| 006Ch | R | PHYStatus | **PHY(GMII, MII, or TBI) Status Register** |
| 006Dh-0083h | - | - | **Reserved** |
| 0084h–008Bh | R/W | Wakeup0 | **Power Management wakeup frame0 (64bit)** |
| 008Ch–0093h | R/W | Wakeup1 | **Power Management wakeup frame1 (64bit)** |
| 0094h–009Bh | R/W | Wakeup2LD | **Power Management wakeup frame2 (128bit), low D-Word** |
| 009Ch–00A3h | R/W | Wakeup2HD | **Power Management wakeup frame2, high D-Word** |
| 00A4h–00ABh | R/W | Wakeup3LD | **Power Management wakeup frame3 (128bit), low D-Word** |
| 00ACh–00B3h | R/W | Wakeup3HD | **Power Management wakeup frame3, high D-Word** |
| 00B4h–00BBh | R/W | Wakeup4LD | **Power Management wakeup frame4 (128bit), low D-Word** |
| 00BCh–00C3h | R/W | Wakeup4HD | **Power Management wakeup frame4, high D-Word** |
| 00C4h-00C5h | R/W | CRC0 | **16-bit CRC of wakeup frame 0** |
| 00C6h-00C7h | R/W | CRC1 | **16-bit CRC of wakeup frame 1** |
| 00C8h-00C9h | R/W | CRC2 | **16-bit CRC of wakeup frame 2** |
| 00CAh-00CBh | R/W | CRC3 | **16-bit CRC of wakeup frame 3** |
| 00CCh-00CDh | R/W | CRC4 | **16-bit CRC of wakeup frame 4** |
| 00CEh-00D9h | - | - | **Reserved** |
| 00DAh-00DBh | R/W | RMS | **Rx packet Maximum Size** |
| 00DCh-00DFh | - | - | **Reserved** |
| 00E0h-00E1h | R/W | C+CR | **C+ Command Register** |
| 00E2h-00E3h | - | - | **Reserved** |
| 00E4h-00EBh | R/W | RDSAR | **Receive Descriptor Start Address Register (256-byte alignment)** |
| 00ECh | R/W | MTPS | **Max Transmit Packet Size Register** |
| 00EDh-00FFh | - | - | **Reserved** |

## 6.1. DTCCR: Dump Tally Counter Command

(Offset 0010h-0017h, R/W)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 63-6 | R/W | CntrAddr | Starting address of the 12 Tally Counters being dumped to. (64-byte alignment address, 64 bytes long) |

| Offset of starting address | Counter | Description |
|---|---|---|
| 0 | TxOk | 64-bit counter of Tx Ok packets. |
| 8 | RxOk | 64-bit counter of Rx Ok packets. |
| 16 | TxER | 64-bit packet counter of Tx errors including Tx abort, carrier lost, Tx underrun, and out of window collision. |
| 24 | RxEr | 32-bit packet counter of Rx errors including CRC error packets (should be larger than 8 bytes) and missed packets. |
| 28 | MissPkt | 16-bit counter of missed packets (CRC Ok) resulted from Rx FIFO full. |
| 30 | FAE | 16-bit counter of Frame Alignment Error packets (MII mode only) |
| 32 | Tx1Col | 32-bit counter of those Tx Ok packets with only 1 collision happened before Tx Ok. |
| 36 | TxMCol | 32-bit counter of those Tx Ok packets with more than 1, and less than 16 collisions happened before Tx Ok. |
| 40 | RxOkPhy | 64-bit counter of all Rx Ok packets with physical address matched destination ID. |
| 48 | RxOkBrd | 64-bit counter of all Rx Ok packets with broadcast destination ID. |

<table>
<tr><td></td><td></td><td></td><td><table>
<tr><td>56</td><td>RxOkMul</td><td>32-bit counter of all Rx Ok packets with multicast destination ID.</td></tr>
<tr><td>60</td><td>TxAbt</td><td>16-bit counter of Tx abort packets.</td></tr>
<tr><td>62</td><td>TxUndrn</td><td>16-bit counter of Tx underrun and discard packets (only possible on jumbo frames).</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>3</td><td>R/W</td><td>Cmd</td><td>Command: When set, the RTL8169S/RTL8110S begins dumping 13 Tally counters to the address specified above.<br>When this bit is reset by the RTL8169S/RTL8110S, the dumping has been completed.</td></tr>
<tr><td>2-0</td><td>-</td><td>-</td><td>Reserved</td></tr>
</table>

## *6.2. Command*

(Offset 0037h, R/W)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 7-5 | - | - | **Reserved** |
| 4 | R/W | RST | **Reset:** Setting this bit to 1 forces the RTL8169S/RTL8110S into a software reset state which disables the transmitter and receiver, reinitializes the FIFOs, and resets the system buffer pointer to the initial value (the start address of each descriptor group set in TNPDS, THPDS, and RDSAR registers). The values of IDR0-5, MAR0-7 and PCI configuration space will have no changes. This bit is 1 during the reset operation, and is cleared to 0 by the RTL8169S/RTL8110S when the reset operation is complete. |
| 3 | R/W | RE | **Receiver Enable** |
| 2 | R/W | TE | **Transmitter Enable** |
| 1-0 | - | - | **Reserved** |

## *6.3. TPPoll: Transmit Priority Polling*

(Offset 0038h, R/W)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 7 | W | HPQ | **High Priority Queue polling:** Writing a '1' to this bit will notify the RTL8169S/RTL8110S that there is a high priority packet(s) waiting to be transmitted. The RTL8169S/RTL8110S will clear this bit automatically after all high priority packets have been transmitted.<br>Writing a '0' to this bit has no effect. |
| 6 | W | NPQ | **Normal Priority Queue polling:** Writing a '1' to this bit will notify the RTL8169S/RTL8110S that there is a normal priority packet(s) waiting to be transmitted. The RTL8169S/RTL8110S will clear this bit automatically after all normal priority packets have been transmitted.<br>Writing a '0' to this bit has no effect. |
| 5-1 | - | - | **Reserved** |
| 0 | W | FSWInt | **Forced Software Interrupt:** Writing a '1' to this bit will trigger an interrupt, and the SWInt bit (bit8, ISR, offset3Eh-3Fh) will set.<br>The RTL8169S/RTL8110S will clear this bit automatically after the SWInt bit (bit8, ISR) is cleared.<br>Writing a '0' to this bit has no effect. |

## *6.4. Interrupt Mask*

(Offset 003Ch-003Dh, R/W)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 15 | R/W | SERR | **System Error Interrupt:**<br>1: Enable, 0: Disable. |

| | | | |
|---|---|---|---|
| 14 | R/W | TimeOut | **Time Out Interrupt:**<br>1: Enable, 0: Disable. |
| 13-9 | - | - | **Reserved** |
| 8 | R/W | SWInt | **Software Interrupt:**<br>1: Enable, 0: Disable. |
| 7 | R/W | TDU | **Tx Descriptor Unavailable Interrupt:**<br>1: Enable, 0: Disable. |
| 6 | R/W | FOVW | **Rx FIFO Overflow Interrupt:**<br>1: Enable, 0: Disable. |
| 5 | R/W | LinkChg | **Link Change Interrupt:**<br>1: Enable, 0: Disable. |
| 4 | R/W | RDU | **Rx Descriptor Unavailable Interrupt:**<br>1: Enable, 0: Disable. |
| 3 | R/W | TER | **Tx Error Interrupt:**<br>1: Enable, 0: Disable. |
| 2 | R/W | TOK | **Tx Ok:**<br>Transmit (Tx) OK: Indicates that a packet transmission is completed successfully.<br>1: Enable, 0: Disable. |
| 1 | R/W | RER | **Rx Error Interrupt:**<br>1: Enable, 0: Disable. |
| 0 | R/W | ROK | **Rx OK Interrupt:**<br>1: Enable, 0: Disable. |

## *6.5. Interrupt Status*

(Offset 003Eh-003Fh, R/W)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 15 | R/W | SERR | **System Error:** This bit is set to 1 when the RTL8169S/RTL8110S signals a system error on the PCI bus. |
| 14 | R/W | TimeOut | **Time Out:** This bit is set to 1 when the TCTR register reaches the value of the TimerInt register. |

| | | | |
|---|---|---|---|
| 13-9 | - | - | **Reserved** |
| 8 | R/W | SWInt | **Software Interrupt:** This bit is set to 1 whenever a '1' is written by software to FSWInt (bit0, offset D9h, TPPoll register). |
| 7 | R/W | TDU | **Tx Descriptor Unavailable:** When set, this bit indicates that the Tx descriptor is unavailable. |
| 6 | R/W | FOVW | **Rx FIFO Overflow:** This bit set to 1 is caused by RDU, poor PCI performance, or overloaded PCI traffic. |
| 5 | R/W | LinkChg | **Link Change:** This bit is set to 1 when link status is changed. |
| 4 | R/W | RDU | **Rx Descriptor Unavailable:** When set to 1, this bit indicates that the Rx descriptor is unavailable.<br>The MPC (Missed Packet Counter, offset 4Ch-4Fh) indicates the number of packets discarded after Rx FIFO overflowed. |
| 3 | R/W | TER | **Transmit (Tx) Error:** This bit set to 1 indicates that a packet transmission was aborted, due to excessive collisions, according to the TXRR's setting in the TCR register. |
| 2 | R/W | TOK | **Transmit (Tx) OK:** When set to 1, this bit indicates that a packet transmission has been completed successfully. |
| 1 | R/W | RER | **Receive (Rx) Error:** When set to 1, this bit indicates that a packet has either a CRC error or a frame alignment error (FAE). A Rx error packet of CRC error is determined according to the setting of RER8, AER, AR bits in RCR register (offset 44h-47h). |
| 0 | R/W | ROK | **Receive (Rx) OK:** In normal mode, this bit set to 1 indicates the successful completion of a packet reception. |

- Writing 1 to any bit in the ISR will reset that bit.

## *6.6. Transmit Configuration*

(Offset 0040h-0043h, R/W)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 31 | - | - | **Reserved** |
| 30-26 | R | HWVERID0 | **Hardware Version ID0:** |

<table>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th></th><th>Bit30</th><th>Bit29</th><th>Bit28</th><th>Bit27</th><th>Bit26</th><th>Bit23</th></tr>
<tr><td>RTL8169</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>RTL8169S/RTL8110S</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">Not (0,0)</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>Reserved</td><td colspan="6">All other combination</td></tr>
</table>
</td></tr>
<tr><td>25-24</td><td>R/W</td><td>IFG1, 0</td><td>InterFrameGap Time: This field allows adjustment of the interframe gap time to be longer than the standards of 9.6 us for 10Mbps, 960 ns for 100Mbps, and 96 ns for 1000Mbps. The time can be programmed from 9.6 us to 14.4 us (10Mbps), 960ns to 1440ns (100Mbps), and 96ns to 144ns (1000Mbps).<br><br>The setting of the inter frame gap is:
<table>
<tr><th colspan="3">IFG[2:0]</th><th>IFG@1000MHz (ns)</th><th>IFG@100MHz (ns)</th><th>IFG@10MHz (us)</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>96</td><td>960</td><td>9.6</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>96 + 8</td><td>960 + 8 * 10</td><td>9.6 + 8 * 0.1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>96 + 16</td><td>960 + 16 * 10</td><td>9.6 + 16 * 0.1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>96 + 24</td><td>960 + 24 * 10</td><td>9.6 + 24 * 0.1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>96 + 48</td><td>960 + 48 * 10</td><td>9.6 + 48 * 0.1</td></tr>
</table>
- Other values are reserved.</td></tr>
<tr><td>23</td><td>R</td><td>HWVERID1</td><td>Hardware Version ID1: Please refer to HWVERID0.</td></tr>
<tr><td>22-20</td><td></td><td>-</td><td>Reserved</td></tr>
<tr><td>19</td><td>R/W</td><td>IFG2</td><td>InterFrameGap2</td></tr>
</table>

| | | | |
|---|---|---|---|
| 18, 17 | R/W | LBK1, LBK0 | **Loopback test:** There will be no packets on the (G)MII or TBI interface in Digital loopback mode, provided the external phyceiver is also set in loopback mode. The digital loopback function is independent of the current link status.<br><br>For analog loopback tests, software must force the external phyceiver into loopback mode while the RTL8169S/RTL8110S operates normally.<br><br>00 : Normal operation<br>01 : MAC loopback mode<br>10 : Reserved<br>11 : Reserved |
| 16 | R/W | CRC | **Append CRC:** Setting this bit to 1 means that there is no CRC appended at the end of a packet. Setting to 0 means that there is a CRC appended at the end of a packet. |
| 15-11 | - | - | **Reserved** |
| 10-8 | R/W | MXDMA2, 1, 0 | **Max DMA Burst Size per Tx DMA Burst:** This field sets the maximum size of transmit DMA data bursts according to the following table:<br><br>000 = 16 bytes<br>001 = 32 bytes<br>010 = 64 bytes<br>011 = 128 bytes<br>100 = 256 bytes<br>101 = 512 bytes<br>110 = 1024 bytes<br>111 = Unlimited |
| 7-0 | - | - | **Reserved** |

« The TCR register can only be changed after having set TE (bit2, Command register, offset 0037h).

## *6.7. Receive Configuration*

(Offset 0044h-0047h, R/W)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 31-17 | - | - | **Reserved** |
| 16 | R/W | RER8 | When this bit is set to 1, the RTL8169S/RTL8110S will calculate CRC of any received packet with length larger than 8 bytes.<br>When this bit is cleared, the RTL8169S/RTL8110S only calculates CRC of any received packet with length larger than 64-byte. The power-on default is zero.<br>If AER or AR is set, the RTL8169S/RTL8110S always calculates CRC of any incoming packet with packet length larger than 8 bytes. The RER8 is “Don’t care” in this situation. |
| 15-13 | R/W | RXFTH2, 1, 0 | **Rx FIFO Threshold:** Specifies the Rx FIFO Threshold level. When the number of the received data bytes from a packet, which is being received into the RTL8169S/RTL8110S's Rx FIFO, has reached this level (or the FIFO contains a complete packet), the receive PCI bus master function will begin to transfer the data from the FIFO to the host memory. This field sets the threshold level according to the following table:<br>000 = Reserved<br>001 = Reserved<br>010 = 64 bytes<br>011 = 128 bytes<br>100 = 256 bytes<br>101 = 512 bytes<br>110 = 1024 bytes<br>111 = no Rx threshold. The RTL8169S/RTL8110S begins the transfer of data after having received a whole packet in the FIFO. |
| 12-11 | - | - | **Reserved** |
| 10-8 | R/W | MXDMA2, 1, 0 | **Max DMA Burst Size per Rx DMA Burst:** This field sets the maximum size of the receive DMA data bursts according to the |

| | | | |
|---|---|---|---|
| | | | following table:<br>000 = Reserved<br>001 = Reserved<br>010 = 64 bytes<br>011 = 128 bytes<br>100 = 256 bytes<br>101 = 512 bytes<br>110 = 1024 bytes<br>111 = Unlimited |
| 7 | - | - | **Reserved** |
| 6 | R | 9356SEL | This bit reflects what type of EEPROM is used.<br>1: The EEPROM used is 9356.<br>0: The EEPROM used is 9346. |
| 5 | R/W | AER | **Accept Error Packet:**<br>When set to 1, all packets with CRC error, alignment error, and/or collided fragments will be accepted.<br>When set to 0, all packets with CRC error, alignment error, and/or collided fragments will be rejected. |
| 4 | R/W | AR | **Accept Runt:** This bit set to 1 allows the receiver to accept packets that are smaller than 64 bytes. The packet must be at least 8 bytes long to be accepted as a runt. |
| 3 | R/W | AB | **Accept Broadcast Packets:** 1: Accept, 0: Reject |
| 2 | R/W | AM | **Accept Multicast Packets:** 1: Accept, 0: Reject |
| 1 | R/W | APM | **Accept Physical Match Packets:** 1: Accept, 0: Reject |
| 0 | R/W | AAP | **Accept All Packets with Destination Address:** 1: Accept, 0: Reject |

## *6.8. 9346CR: 93C46 (93C56) Command*

(Offset 0050h, R/W)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 7-6 | R/W | EEM1-0 | **Operating Mode:** These 2 bits select the RTL8169S/RTL8110S |

<table>
<tr><td></td><td></td><td></td><td>operating mode.
<table>
<tr><th>EEM1</th><th>EEM0</th><th>Operating Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal (RTL8169S/RTL8110S network/host communication mode)</td></tr>
<tr><td>0</td><td>1</td><td>Auto-load: Entering this mode will make the RTL8169S/RTL8110S load the contents of the 93C46 (93C56) as when the PCI RSTB signal is asserted. This auto-load operation will take about 2 ms. Upon completion, the RTL8169S/RTL8110S automatically returns to normal mode (EEM1 = EEM0 = 0) and all of the other registers are reset to default values.</td></tr>
<tr><td>1</td><td>0</td><td>93C46 (93C56) programming: In this mode, both network and host bus master operations are disabled. The 93C46 (93C56) can be directly accessed via bit3-0 which now reflect the states of EECS, EESK, EEDI, & EEDO pins respectively.</td></tr>
<tr><td>1</td><td>1</td><td>Config register write enable: Before writing to CONFIGx registers, the RTL8169S/RTL8110S must be placed in this mode. This will prevent RTL8169S/RTL8110S configurations from accidental change.</td></tr>
</table>
</td></tr>
<tr><td>4-5</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>3</td><td>R/W</td><td>EECS</td><td rowspan="4">These bits reflect the state of the EECS, EESK, EEDI & EEDO pins in auto-load or 93C46 (93C56) programming mode and are valid only when the Flash bit is cleared.<br>Note: EESK, EEDI and EEDO is valid after boot ROM complete.</td></tr>
<tr><td>2</td><td>R/W</td><td>EESK</td></tr>
<tr><td>1</td><td>R/W</td><td>EEDI</td></tr>
<tr><td>0</td><td>R</td><td>EEDO</td></tr>
</table>

## *6.9. CONFIG 0*

(Offset 0051h, R/W)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 7-3 | - | - | **Reserved** |
| 2-0 | R | BS2, BS1, BS0 | **Select Boot ROM Size** |

| BS2 | BS1 | BS0 | Description |
|---|---|---|---|
| 0 | 0 | 0 | No Boot ROM |
| 0 | 0 | 1 | 8K Boot ROM |
| 0 | 1 | 0 | 16K Boot ROM |
| 0 | 1 | 1 | 32K Boot ROM |
| 1 | 0 | 0 | 64K Boot ROM |
| 1 | 0 | 1 | 128K Boot ROM |
| 1 | 1 | 0 | unused |
| 1 | 1 | 1 | unused |

## *6.10. CONFIG 1*

(Offset 0052h, R/W)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 7-6 | R/W | LEDS1-0 | Refer to the LED PIN definition. These bits initial value com from 93C46/93C56. |
| 5 | R/W | DVRLOAD | **Driver Load:** Software maybe use this bit to make sure that the driver has been loaded. Writing 1 is 1. Writing 0 is 0. When the command register bits IOEN, MEMEN, BMEN of PCI configuration space are written, the RTL8169S/RTL8110S will clear this bit automatically. |

<table>
<tr><td>4</td><td>R/W</td><td>LWACT</td><td>LWAKE Active Mode: The LWACT bit and LWPTN bit in CONFIG4 register are used to program the LWAKE pin's output signal. According to the combination of these two bits, there may be 4 choices of LWAKE signal, i.e., active high, active low, positive (high) pulse, and negative (low) pulse. The output pulse width is about 150 ms. In CardBus application, the LWACT and LWPTN have no meaning.<br><br>The default value of each of these two bits is 0, i.e., the default output signal of LWAKE pin is an active high signal.<br>
<table>
<tr><th colspan="2" rowspan="2">LWAKE output</th><th colspan="2">LWACT</th></tr>
<tr><td>0</td><td>1</td></tr>
<tr><th rowspan="2">LWPTN</th><td>0</td><td>Active high*</td><td>Active low</td></tr>
<tr><td>1</td><td>Positive pulse</td><td>Negative pulse</td></tr>
</table>
* Default value.</td></tr>
<tr><td>3</td><td>R</td><td>MEMMAP</td><td>Memory Mapping: The operational registers are mapped into PCI memory space.</td></tr>
<tr><td>2</td><td>R</td><td>IOMAP</td><td>I/O Mapping: The operational registers are mapped into PCI I/O space.</td></tr>
<tr><td>1</td><td>R/W</td><td>VPD</td><td>Vital Product Data: Set to enable Vital Product Data. The VPD data is stored in 93C46 or 93C56 from within offset 40h-7Fh.</td></tr>
<tr><td>0</td><td>R/W</td><td>PMEn</td><td>Power Management Enable:<br>Writable only when 93C46CR register EEM1=EEM0=1<br><br>Let A denote the New_Cap bit (bit 4 of the Status Register) in the PCI Configuration space offset 06h.<br>Let B denote the Cap_Ptr register in the PCI Configuration space offset 34h.<br>Let C denote the Cap_ID (power management) register in the PCI Configuration space offset 0DCh.<br>Let D denote the power management registers in the PCI Configuration space offset from 0DDh to 0E1h.<br>Let E denote the Next_Ptr (power management) register in the PCI Configuration space offset 0DDh.<br><br>PMEn setting:<br>0: A=B=C=E=0, D is invalid<br>1: A=1, B=0DCh, C=01h, D is valid, E is valid and depends on whether VPD is enabled or not.</td></tr>
</table>

## *6.11. CONFIG 2*

(Offset 0053h, R)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 7-5 | - | - | **Reserved** |
| 4 | R | Aux_Status | **Auxiliary Power Present Status:**<br>1: The Aux. Power is present.<br>0: The Aux. Power is absent.<br>The value of this bit is fixed after each PCI reset. |
| 3 | R | PCIBusWidth | **PCI Bus Width:**<br>1: 64-bit slot<br>0: 32-bit slot |
| 2-0 | R | PCICLKF2-0 | **PCI clock frequency:**<br>PCICLKF2-0 = 000: 33 MHz<br>PCICLKF2-0 = 001: 66 MHz<br>Other values: Reserved |

PCI clock frequency:

| PCICLKF2-0 | MHz |
|---|---|
| 000 | 33 |
| 001 | 66 |
| Other values | Reserved |

## *6.12. CONFIG 3*

(Offset 0054h, R/W)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 7 | R | GNTSel | **Grant Select:** Select the Frame's asserted time after the Grant signal has been asserted. The Frame and Grant are the PCI signals.<br>1: delay one clock from GNT assertion.<br>0: No delay |
| 6 | - | - | **Reserved** |
| 5 | R/W | Magic | **Magic Packet:** This bit is valid when the PWEn bit of CONFIG1 register is set. The RTL8169S/RTL8110S will assert the PMEB signal to wakeup the operating system when the Magic Packet is received. |

| | | | |
|---|---|---|---|
| | | | Once the RTL8169S/RTL8110S has been enabled for Magic Packet wakeup and has been put into an adequate state, it scans all incoming packets addressed to the node for a specific data sequence, which indicates to the controller that this is a Magic Packet frame. A Magic Packet frame must also meet the basic requirements: Destination address + Source address + data + CRC<br>The destination address may be the node ID of the receiving station or a multicast address, which includes the broadcast address.<br>The specific sequence consists of 16 duplications of 6 byte ID registers, with no breaks or interrupts. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream, 6 bytes of FFh. The device will also accept a multicast address, as long as the 16 duplications of the IEEE address match the address of the ID registers.<br>If the Node ID is 11h 22h 33h 44h 55h 66h, then the format of the Magic frame looks like the following:<br>Destination address + source address + MISC + FF FF FF FF FF FF + MISC + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + MISC + CRC |
| 4 | R/W | LinkUp | **Link Up:** This bit is valid when the PWEn bit of the CONFIG1 register is set. The RTL8169S/RTL8110S, in an adequate power state, will assert the PMEB signal to wakeup the operating system when the cable connection is reestablished. |
| 3-1 | - | - | **Reserved** |
| 0 | R | FBtBEn | **Fast Back to Back Enable:** 1: Enable, 0: Disable. |

## *6.13. CONFIG 4*

(Offset 0055h, R/W)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 7-5 | - | - | **Reserved** |
| 4 | R/W | LWPME | **LANWAKE vs PMEB:**<br>Set to 1: The LWAKE can only be asserted when the PMEB is asserted and the ISOLATEB is low.<br>Set to 0: The LWAKE and PMEB are asserted at the same time.<br>In CardBus applications, this bit has no meaning. |
| 3 | - | - | **Reserved** |
| 2 | R/W | LWPTN | **LWAKE pattern:** Please refer to the LWACT bit in CONFIG1 register. |
| 1-0 | - | - | **Reserved** |

## *6.14. CONFIG 5*

(Offset 0056h, R/W)

This register, unlike other Config registers, is not protected by 93C46 Command register. I.e. there is no need to enable the Config register write prior to writing to Config5.

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 7 | - | - | **Reserved** |
| 6 | R/W | BWF | **Broadcast Wakeup Frame:**<br>1: Enable Broadcast Wakeup Frame with mask bytes of only DID field = FF FF FF FF FF FF.<br>0: Default value. Disable Broadcast Wakeup Frame with mask bytes of only DID field = FF FF FF FF FF FF.<br>The power-on default value of this bit is 0. |
| 5 | R/W | MWF | **Multicast Wakeup Frame:** |

| | | | |
|---|---|---|---|
| | | | 1: Enable Multicast Wakeup Frame with mask bytes of only DID field, which is a multicast address.<br>0: Default value. Disable Multicast Wakeup Frame with mask bytes of only DID field, which is a multicast address.<br>The power-on default value of this bit is 0. |
| 4 | R/W | UWF | **Unicast Wakeup Frame:**<br>1: Enable Unicast Wakeup Frame with mask bytes of only DID field, which is its own physical address.<br>0: Default value. Disable Unicast Wakeup Frame with mask bytes of only DID field, which is its own physical address.<br>The power-on default value of this bit is 0. |
| 3-2 | - | - | **Reserved** |
| 1 | R/W | LANWake | **LANWake Signal Enable/Disable:**<br>1: Enable LANWake signal.<br>0: Disable LANWake signal. |
| 0 | R/W | PME_STS | **PME_Status bit:** Always sticky/can be reset by PCI RST# and software.<br>1: The PME_Status bit can be reset by PCI reset or by software.<br>0: The PME_Status bit can only be reset by software. |

- The bit1 and bit0 are auto-loaded from EEPROM Config5 byte to the RTL8169S/RTL8110S Config5 register.

## *6.15. PHYAR: PHY Access*

(Offset 0060h-0063h, R/W)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 31 | R/W | Flag | **Flag bit, used as PCI VPD access method:**<br>1: Write data to MII register, and turn to 0 automatically whenever the RTL8169S/RTL8110S has completed writing to the specified MII register.<br>0: Read data from MII register, and turn to 1 automatically whenever the RTL8169S/RTL8110S has completed retrieving data from the specified MII register. |

| | | | |
|---|---|---|---|
| 30-21 | - | - | **Reserved** |
| 20-16 | R/W | RegAddr4-0 | **5-bit GMII/MII register address.** |
| 15-0 | R/W | Data15-0 | **16-bit GMII/MII register data.** |

## *6.16. PHYStatus: PHY(GMII or TBI) Status*

(Offset 006Ch, R)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 7 | - | - | Reserved |
| 6 | R | TxFlow | **Transmit Flow Control:** 1: Enabled, 0: Disabled. |
| 5 | R | RxFlow | **Receive Flow Control:** 1: Enabled, 0: Disabled. |
| 4 | R | 1000MF | Link speed is 1000Mbps and in full-duplex. (GMII mode only) |
| 3 | R | 100M | Link speed is 100Mbps. (GMII or MII mode only) |
| 2 | R | 10M | Link speed is 10Mbps. (GMII or MII mode only) |
| 1 | R | LinkSts | Link Status. 1: Link Ok, 0: No Link. |
| 0 | R | FullDup | **Full-Duplex Status:** 1: Full-duplex mode, 0: Half-duplex mode. |

- This register is updated in less than 300us continously.

## *6.17. RMS: Receive (Rx) Packet Maximum Size*

(Offset 00DAh-00DBh, R)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 15-14 | - | - | **Reserved** |
| 13-0 | R/W | RMS | **Rx packet Maximum Size:**<br>i. This register should be always set to a value other than 0, in order to receive packets.<br>ii. The maximum Rx packet size supported is $2^{14}$-1, i.e., 16K-1 bytes.<br>iii. If this register is set to a value larger than $2^{13}$-1 (8K-1), ex. $2^{14}$-1, a received packet larger than $2^{13}$-1 will set both RWT and |

| | | | |
|---|---|---|---|
| | | | RES bits in the corresponding Rx Status Descriptor. If the packet, which is larger than $2^{13}$-1, is received without CRC error, it is still a good packet, although both RWT and RES bits are set in the corresponding Rx Status Descriptor. |

## *6.18. C+CR: C+ Command*

### (Offset 00E0h-00E1h, R/W)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 15 | - | - | **Reserved. Initial value = 0. Do not change this bit.** |
| 14-10 | - | - | **Reserved** |
| 9 | R/W | ENDIAN | **Endian Mode:**<br>1: Big-endian mode.<br>0: Little-endian mode. |
| 8-7 | - | - | **Reserved** |
| 6 | R/W | RxVLAN | **Receive VLAN De-tagging Enable:** 1: Enable. 0: Disable. |
| 5 | R/W | RxChkSum | **Receive Checksum Offload Enable:** 1: Enable. 0: Disable. |
| 4 | R/W | DAC | **PCI Dual Address Cycle Enable:** When set, the RTL8169S/RTL8110S will perform Tx/Rx DMA using PCI Dual Address Cycle only when the High 32-bit buffer address is not equal to 0.<br>1: Enable, 0: Disable (initial value at power-up). |
| 3 | R/W | MulRW | **PCI Multiple Read/Write Enable**. 1: Enable. 0: Disable.<br>- If this bit is enabled, the setting of Max Tx/Rx DMA burst size is no longer valid. |
| 2-0 | - | - | **Reserved** |

- **This register is the key before configuring other registers and descriptors.**
- **This register is word access only, byte access to this register has no effect.**

## *6.19. RDSAR: Receive Descriptor Start Address*

(Offset 00E4h-00EBh, R/W)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 63-0 | R/W | RDSA | **Receive Descriptor Start Address**: 64-bit address, 256-byte alignment address.<br>Bit[31:0]: Offset E7h-E4h, low 32-bit address.<br>Bit[63:32]: Offset EBh-E8h, high 32-bit address. |

## *6.20. MTPS: Max Transmit Packet Size*

(Offset 00ECh, R/W)

| Bit | R/W | Symbol | Description |
|---|---|---|---|
| 7-6 | - | - | **Reserved** |
| 5-0 | R/W | MTPS | **Max Tx Packet Size:** Specifies the maximum packet size that the RTL8169S/RTL8110S is to transmit.<br>- These fields count from 000001 to 111111 in unit of 128 bytes (For RTL8169, the unit is 32 bytes).<br>- For regular LAN applications, i.e., the max packet size is either 1518 or 1522(VLAN) bytes, this field must be larger than the max packet size. Ex., 0x0C.<br>- 000000 is reserved. Do not set to this value in any situation. This is the default value after power-on, driver has to set value other than 0 for correct operation.<br>- To support Jumbo Frame without possible Tx underruns, this field is suggested to be larger than the maximum packet transmitted.<br>- The maximum Jumbo Frame (without possible Tx underruns) that the RTL8169S/RTL8110S is able to transmit is 7440 (7436 |

| | | | |
|---|---|---|---|
| | | | + 4-byte CRC) bytes, therefore, this field has to be set to values larger than that to transmit a Jumbo Frame packet of size up to 7440 bytes. Ex., 0x3B (7552) bytes.<br>- If the MTPS is set to a value larger than 0x3B, the maximum length of packets transmitted can not exceed 7440 (7436 + CRC) bytes.<br>- If the MTPS is set to a value less than 0x3B, ex. 0x1F, then, as long as the PCI performance is good enough such that there's no Tx underruns, the length of the transmitted packet might be larger than 7440 bytes. Drivers should have to take good care of this configuration to transmit packets larger than 7440 bytes on different PC platforms to prevent from Tx underruns. |

# 7. PHY Register Description

## 7.1. *PHY Register definitions:*

Register maps and address definitions are given in the following table:

**Table 11. PHY Registers**

| Offset | Access | Tag | Description |
|---|---|---|---|
| 0 | RW | BMCR | Basic mode control register |
| 1 | RO | BMSR | Basic mode status register |
| 2 | RO | PHYAD1 | PHY identifier register 1 |
| 3 | RO | PHYAD2 | PHY identifier register 2 |
| 4 | RW | ANAR | Auto-negotiation advertising register |
| 5 | RW | ANLPAR | Auto-negotiation link partner ability register |
| 6 | RW | ANER | Auto-negotiation expansion register |
| 7 | RW | ANNPTR | Auto-negotiation next page transmit register |
| 8 | RW | ANNRPR | Auto-negotiation next page receive register |
| 9 | RW | GBCR | 1000Base-T control register |
| 10 | RO | GBSR | 1000Base-T status register |
| 11-14 | RO | Reserved | |
| 15 | RO | GBESR | 1000Base-T extended status register |
| 25-31 | RO | Reserved | |

## 7.2. *PHY Register Table:*

### 7.2.1. BMCR (address 0x00)

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 15 | Reset | R/W | 0 | Reset:<br>1 = Initiate software Reset / Reset in Process.<br>0 = Normal operation.<br>This bit sets the status and control registers of the PHY to their default states. This bit, which is self-clearing, returns a value of one until the reset process is complete. Reset is finished once the Auto-Negotiation process has begun or the device has entered its forced mode. |

| | | | | |
|---|---|---|---|---|
| 14 | Loopback | R/W | 0 | Loopback:<br>1 = Loopback enabled.<br>0 = Normal operation.<br>The loopback function enables MII/GMII transmit data to be routed to the MII/GMII receive data path. |
| 13 | Speed[0] | R/W | 0 | Speed Select:<br>When Auto-Negotiation is disabled, bits 6 and 13 select device speed selection per table below:<br>Speed[1] Speed[0] Speed Enabled<br>1 1 = Reserved<br>1 0 = 1000 Mb/s<br>0 1 = 100 Mb/s<br>0 0 = 10 Mb/s |
| 12 | ANE | R/W | 1 | Auto-Negotiation Enable:<br>1 = Auto-Negotiation Enabled - bits 6, 8 and 13 of this register are ignored when this bit is set.<br>0 = Auto-Negotiation Disabled - bits 6, 8 and 13 determine the link speed and mode. |
| 11 | PWD | R/W | 0 | Power Down:<br>1 = Power down (only Management Interface and logic active.)<br>0 = Normal operation. |
| 10 | Isolate | R/W | 0 | Isolate:<br>1 = Isolates the Port from the MII with the exception of the serial management.<br>0 = Normal operation. |
| 9 | Restart_AN | R/W | 0 | Restart Auto-Negotiation:<br>1 = Restart Auto-Negotiation. Re-initiates the Auto-Negotiation process. If Auto-Negotiation is disabled (bit 12 = 0), this bit is ignored. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated, whereupon it will self-clear. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit.<br>0 = Normal operation. |
| 8 | Duplex | R/W | 1 | Duplex Mode:<br>1 = Full Duplex operation. Duplex selection is allowed only when Auto-Negotiation is disabled (bit 12 = 0). |

| | | | | |
|---|---|---|---|---|
| | | | | 0 = Half Duplex operation. |
| 7 | Reserved | R/W | 0 | |
| 6 | Speed[1] | R/W | 1 | Speed Select: See description for bit 13. |
| 5:0 | Reserved | RO | 000000 | Reserved by IEEE |

### 7.2.2. BMSR (address 0x01)

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 15 | 100Base-T4 | RO | 0 | 100BASE-T4 Capable:<br>1 = Device able to perform 100BASE-T4 mode.<br>0 = Device not able to perform 100BASE-T4 mode.<br>RTL8169S/RTL8110S does not support 100BASE-T4 mode and bit should always be read back as “0”. |
| 14 | 100Base-TX(full) | RO | 1 | 100BASE-TX Full Duplex Capable:<br>1 = Device able to perform 100BASE-TX in full duplex mode.<br>0 = Device unable to perform 100BASE-TX in full duplex mode. |
| 13 | 100Base-TX(half) | RO | 1 | 100BASE-TX Half Duplex Capable:<br>1 = Device able to perform 100BASE-TX in half duplex mode.<br>0 = Device unable to perform 100BASE-TX in half duplex mode. |
| 12 | 10Base-T(full) | RO | 1 | 10BASE-T Full Duplex Capable:<br>1 = Device able to perform 10BASE-T in full duplex mode.<br>0 = Device unable to perform 10BASE-T in full duplex mode. |
| 11 | 10Base-T(half) | RO | 1 | 10BASE-T Half Duplex Capable:<br>1 = Device able to perform 10BASE-T in half duplex mode.<br>0 = Device unable to perform 10BASE-T in half duplex mode. |
| 10 | 100Base-T2(full) | RO | 0 | 100BASE-T2 Full Duplex Capable:<br>1 = Device able to perform 100BASE-T2 Full Duplex mode.<br>0 = Device unable to perform 100BASE-T2 Full Duplex mode.<br>RTL8169S/RTL8110S does not support 100BASE-T2 mode and bit should always be read back as “0”. |
| 9 | 100Base-T2(half) | RO | 0 | 100BASE-T2 Half Duplex Capable:<br>1 = Device able to perform 100BASE-T2 Half Duplex mode.<br>0 = Device unable to perform 100BASE-T2 Full Duplex mode.<br>RTL8169S/RTL8110S does not support 100BASE-T2 mode and bit should always be read back as “0”. |

| | | | | |
|---|---|---|---|---|
| 8 | 1000Base-T Extended status | RO | 1 | 1000BASE-T Extended Status Register:<br>1 = Device supports Extended Status Register 0x0F (15).<br>0 = Device does not supports Extended Status Register 0x0F |
| 7 | Reserved | RO | 0 | Reserved |
| 6 | Preamble Suppression | RO | 1 | Preamble suppression Capable:<br>1 = Device is able to perform management transaction with preamble suppressed, 32-bits of preamble is needed only once after reset, invalid opcode or invalid turnaround. |
| 5 | Auto-Negotiation Complete | RO | 0 | Auto-Negotiation Complete:<br>1 = Auto-Negotiation process complete, and contents of registers 5, 6, 7, & 8 are valid.<br>0 = Auto-Negotiation process not complete. |
| 4 | Remote Fault | RO | 0 | Remote Fault:<br>1 = Remote Fault condition detected (cleared on read or by reset). Fault criteria: Far End Fault Indication or notification from<br>Link Partner of Remote Fault.<br>0 = No remote fault condition detected. |
| 3 | Auto-Negotiation Ability | RO | 1 | Auto Configuration Ability:<br>1 = Device is able to perform Auto-Negotiation.<br>0 = Device is not able to perform Auto-Negotiation. |
| 2 | Link Status | RO | 0 | 1 = Link is up<br>0 = Link is down<br>This bit indicates if link was lost since the last read. |
| 1 | Jabber detect | RO | 0 | 1 = Jabber condition detected<br>0 = Jabber condition not detected |
| 0 | Extended Capability | RO | 1 | 1 = Extended register capability is enabled<br>0 = Extended register capability is disabled |

### 7.2.3. PHY Identifier Register 1 (address 0x02)

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 15:0 | OUI_MSB | RO | 001C | Organization unique identifier |

### 7.2.4. PHY Identifier Register 2 (address 0x03)

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| 15:0 | OUI_LSB | RO | C910 | Organization unique identifier |

### 7.2.5. ANAR (address 0x04)

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 15 | NextPage | R/W | 0 | 1 = Advertise<br>0 = Not advertised |
| 14 | Resv | RO | 0 | |
| 13 | Remote fault | R/W | 0 | 1 = Set Remote Fault bit<br>0 = Do not set Remote Fault bit |
| 12 | Resv | R/W | 0 | |
| 11 | Asymmetric PAUSE | R/W | 0 | 1 = Asymmetric Pause<br>0 = No asymmetric Pause |
| 10 | PAUSE | R/W | 0 | 1 = MAC PAUSE implemented<br>0 = MAC PAUSE not implemented |
| 9 | 100Base-T4 | RO | 0 | 0 = Not capable of 100BASE-T4 |
| 8 | 100Base-TX(full) | R/W | 1 | 1 = Advertise<br>0 = Not advertised |
| 7 | 100Base-TX(half) | R/W | 1 | 1 = Advertise<br>0 = Not advertised |
| 6 | 10Base-T(full) | R/W | 1 | 1 = Advertise<br>0 = Not advertised |
| 5 | 10Base-T(half) | R/W | 1 | 1 = Advertise<br>0 = Not advertised |
| 4:0 | Selector field | RO | 00001 | For 802.3 |

### 7.2.6. ANLPAR (address 0x05)

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 15 | Next Page | RO | 0 | Received Code Word Bit 15 |
| 14 | ACK | RO | 0 | Received Code Word Bit 14 |
| 13 | Remote Fault | RO | 0 | Received Code Word Bit 13 |
| 12:5 | Technology Ability Field | RO | 0 | Received Code Word Bit 12:5 |
| 4:0 | Selector Field | RO | 0 | Received Code Word Bit 4:0 |

### 7.2.7. ANER (address 0x06)

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 15:5 | resv | RO | 0 | Resv |
| 4 | Parallel Detection Fault | RO | 0 | 1 = A fault has been detected via the Parallel Detection function<br>0 = A fault has not been detected via the Parallel Detection function |
| 3 | Link Partner Next Pageable | RO | 0 | 1 = Link Partner is Next Page capable<br>0 = Link Partner is not Next Page capable |
| 2 | Local Next Pageable | RO | 1 | 1 = Local Device is Next Page able |
| 1 | Page Received | RO | 0 | 1 = A New Page has been received<br>0 = A New Page has not been received |
| 0 | Link Partner Auto-Negotiation Able | RO | 0 | 1 = Link Partner is Auto-Negotiation capable<br>0 = Link Partner is not Auto-Negotiation capable |

### 7.2.8. ANNPTR (address 0x07)

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 15 | Next Page | R/W | 0 | Transmit Code Word Bit 15 |
| 14 | Resv | RO | 0 | Transmit Code Word Bit 14 |
| 13 | Message Page | R/W | 1 | Transmit Code Word Bit 13 |
| 12 | Acknowledge 2 | RO | 0 | Transmit Code Word Bit 12 |
| 11 | Toggle | RO | 0 | Transmit Code Word Bit 11 |
| 10:0 | Message/Unformatted Field | R/W | 0x001 | Transmit Code Word Bit 10:0 |

### 7.2.9. ANNPRR(address 0x08)

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 15 | Reserved | RO | 0 | Received Code Word Bit 15 |
| 14 | Acknowledge | RO | 0 | Received Code Word Bit 14 |
| 13 | Message Page | RO | 0 | Received Code Word Bit 13 |
| 12 | Acknowledge 2 | RO | 0 | Received Code Word Bit 12 |
| 11 | Toggle | RO | 0 | Received Code Word Bit 11 |

| | | | | |
|---|---|---|---|---|
| 10:0 | Message/Unformatted Field | RO | 0x00 | Received Code Word Bit 10:0 |

### 7.2.10. GBCR (address 0x09)

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 15:13 | Test Mode | R/W | 0 | 000 = Normal Mode<br>001 = Test Mode 1 - Transmit Jitter Test<br>010 = Test Mode 2 - Transmit Jitter Test (MASTER mode)<br>011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode)<br>100 = Test Mode 4 - Transmit Distortion Test<br>101, 110, 111 = Reserved |
| 12 | MASTER/SLAVE Manual Configuration Enable | R/W | 0 | 1 = Manual MASTER/SLAVE configuration<br>0 = Automatic MASTER/SLAVE |
| 11 | MASTER/SLAVE Configuration Value | R/W | 0 | 1 = Manual configure as MASTER<br>0 = Manual configure as SLAVE |
| 10 | Port Type | R/W | 0 | 1 = Prefer multi-port device (MASTER)<br>0 = Prefer single port device (SLAVE) |
| 9 | 1000BASE-T Full Duplex | R/W | 0 | 1 = Advertise<br>0 = Not advertised |
| 8 | 1000BASE-T Half Duplex | R/W | 0 | 1 = Advertise<br>0 = Not advertised |
| 7:0 | Resv | R/W | 0 | Reserved |

### 7.2.11. GBSR (address 0x0A)

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 15 | MASTER/SLAVE Configuration Fault | RO | 0 | 1 = MASTER/SLAVE configuration fault detected<br>0 = No MASTER/SLAVE configuration fault detected |
| 14 | MASTER/SLAVE Configuration Resolution | RO | 0 | 1 = Local PHY configuration resolved to MASTER<br>0 = Local PHY configuration resolved to SLAVE |
| 13 | Local Receiver Status | RO | 0 | 1 = Local Receiver OK<br>0 = Local Receiver Not OK |
| 12 | Remote Receiver Status | RO | 0 | 1 = Remote Receiver OK<br>0 = Remote Receiver Not OK |

| | | | | |
|---|---|---|---|---|
| 11 | Link Partner 1000BASE-T Full Duplex Capability | RO | 0 | 1 = Link Partner is capable of 1000BASET full duplex<br>0 = Link Partner is not capable of 1000BASE-T full duplex |
| 10 | Link Partner 1000BASE-T Half Duplex Capability | RO | 0 | 1 = Link Partner is capable of 1000BASET half duplex<br>0 = Link Partner is not capable of 1000BASE-T half duplex |
| 9:8 | Reserved | RO | 00 | Reserved |
| 7:0 | Idle Error Count | RO | 0x00 | MSB of Idle Error Counter |

### 7.2.12. GBESR (address 0x0F)

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 15 | 1000BASE-X FD | RO | 0 | 0 = not 1000BASE-X full duplex capable |
| 14 | 1000BASE-X HD | RO | 0 | 0 = not 1000BASE-X half duplex capable |
| 13 | 1000BASE-T FD | RO | 1 | 1 = 1000BASE-T full duplex capable |
| 12 | 1000BASE-T HD | RO | 1 | 1 = 1000BASE-T half duplex capable |
| 11:0 | Reserved | RO | 0 | Reserved |

# 8. EEPROM (93C46 or 93C56) Contents

The RTL8169S/RTL8110S requires the attachment of an external EEPROM. The 93C46 is a 1K-bit EEPROM (the 93C56 is a 2K-bit EEPROM). The EEPROM interface provides the ability for the RTL8169S/RTL8110S to read from and write data to an external serial EEPROM device. Values in the external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following internal power on reset or software EEPROM autoload command. The RTL8169S/RTL8110S will autoload values from the EEPROM to these fields in configuration space and I/O space. If the EEPROM is not present, the RTL8169S/RTL8110S initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using "bit-bang" accesses via the 9346CR Register, or using PCI VPD.

Although it is actually addressed by words, its contents are listed below by bytes for convenience. After the initial power on or auto-load command in 9346CR, the RTL8169S/RTL8110S performs a series of EEPROM read operations from the 93C46 (93C56) address 00h to 31h.

- It is suggested to obtain Realtek approval before changing the default settings of the EEPROM.

**Table 12. EEPROM Contents**

| Bytes | Contents | Description |
|---|---|---|
| 00h<br>01h | 29h<br>81h | These 2 bytes contain ID code words for the RTL8169S/RTL8110S. The RTL8169S/RTL8110S will load the contents of the EEPROM into the corresponding location if the ID word (8129h) is correct. Otherwise, the Vendor ID and Device ID of the PCI configuration space are "10ECh" and "8129h". |
| 02h-03h | VID | **PCI Vendor ID:** PCI configuration space offset 00h-01h. |
| 04h-05h | DID | **PCI Device ID:** PCI configuration space offset 02h-03h. |
| 06h-07h | SVID | **PCI Subsystem Vendor ID:** PCI configuration space offset 2Ch-2Dh. |
| 08h-09h | SMID | **PCI Subsystem ID:** PCI configuration space offset 2Eh-2Fh. |
| 0Ah | MNGNT | **PCI Minimum Grant Timer:** PCI configuration space offset 3Eh. |
| 0Bh | MXLAT | **PCI Maximum Latency Timer:** PCI configuration space offset 3Fh. Set by software to the number of PCI clocks that the RTL8169S/RTL8110S may hold the PCI bus. |
| 0Ch | CONFIGx | Reserved<br><table><tr><td>Bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr></table> |

| | | |
|---|---|---|
| 0Dh | CONFIG3 | **RTL8169S/RTL8110S Configuration register 3:** Operational register offset 59h. |
| 0Eh-13h | Ethernet ID | **Ethernet ID:** After auto-load command or hardware reset, the RTL8169S/RTL8110S loads Ethernet ID to IDR0-IDR5 of the RTL8169S/RTL8110S's I/O registers. |
| 14h | CONFIG0 | **RTL8169S/RTL8110S Configuration register 0:** Operational registers offset 51h. |
| 15h | CONFIG1 | **RTL8169S/RTL8110S Configuration register 1:** Operational registers offset 52h. |
| 16h-17h | PMC | **Reserved:** Do not change this field without Realtek approval.<br>Power Management Capabilities. PCI configuration space address 52h and 53h. |
| 18h | - | **Reserved** |
| 19h | CONFIG4 | **Reserved:** Do not change this field without Realtek approval.<br>RTL8169S/RTL8110S Configuration register 4, operational registers offset 5Ah. |
| 1Ah-1Eh | - | **Reserved** |
| 1Fh | CONFIG_5 | Do not change this field without Realtek approval.<br>Bit7-2: Reserved.<br>Bit1: LANWake signal Enable/Disable<br>Set to 1: Enable LANWake signal.<br>Set to 0: Disable LANWake signal.<br>Bit0: PME_Status bit property<br>Set to 1: The PME_Status bit can be reset by PCI reset or by software if D3cold_support_PME is 0. If D3cold_support_PME=1, the PME_Status bit is a sticky bit.<br>Set to 0: The PME_Status bit is always a sticky bit and can only be reset by software. |
| 20h-31h | - | **Reserved:** Do not change this field without Realtek approval. |
| 32h-33h | CheckSum | **Reserved:** Do not change this field without Realtek approval.<br>Checksum of the EEPROM content. |
| 34h-3Eh | - | **Reserved:** Do not change this field without Realtek approval. |
| 3Fh | PXE_Para | **Reserved:** Do not change this field without Realtek approval.<br>PXE ROM code parameter. |
| 40h-7Fh | VPD_Data | **VPD data field:** Offset 40h is the start address of the VPD data. |
| 80h-FFh | - | **Reserved:** Do not change this field without Realtek approval. (93C56 only). |

# *8.1. EEPROM Related Registers*

**Table 13. EEPROM Related Registers**

| Offset | Name | Type | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 00h-05h | IDR0 – IDR5 | R/W* | | | | | | | | |
| 51h | CONFIG0 | R | | - | - | - | - | BS2 | BS1 | BS0 |
| | | W* | - | - | - | - | - | - | - | - |
| 52h | CONFIG1 | R | LEDS1 | LEDS0 | DVRLOAD | LWACT | MEMMAP | IOMAP | VPD | PMEN |
| | | W* | LEDS1 | LEDS0 | DVRLOAD | LWACT | - | - | VPD | PMEN |
| 54h | CONFIG3 | R | GNTDel | - | Magic | LinkUp | - | - | - | FBtBEn |
| | | W* | - | - | Magic | LinkUp | - | - | - | - |
| 55h | CONFIG4 | R/W* | - | - | - | LWPME | - | LWPTN | - | - |
| 56h | CONFIG5 | R/W* | - | - | - | - | - | - | LANWake | PME_STS |

* The registers marked with type = 'W*' can be written only if bits EEM1=EEM0=1.

# *8.2. EEPROM Related Power Management Registers*

**Table 14. EEPROM Related Power Management Registers**

| Configuration Space offset | Name | Type | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|
| DEh | PMC | R | Aux_I_b1 | Aux_I_b0 | DSI | Reserved | PMECLK | Version | | |
| DFh | | R | $PME\_D3_{cold}$ | $PME\_D3_{hot}$ | PME_D2 | PME_D1 | PME_D0 | D2 | D1 | Aux_I_b2 |

# 9. PCI Configuration Space Registers

## *9.1. PCI Bus Interface*

The RTL8169S/RTL8110S implements the PCI bus interface as defined in the PCI Local Bus Specifications Rev. 2.2. When internal registers are being accessed, the RTL8169S/RTL8110S acts as a PCI target (slave mode). When accessing host memory for descriptor or packet data transfer, the RTL8169S/RTL8110S acts as a PCI bus master.

All of the required pins and functions are implemented in the RTL8169S/RTL8110S as well as the optional pin, INTAB for support of interrupt requests is implemented as well. The bus interface also supports 64-bit and 66MHz operation in addition to the more common 32-bit and 33-MHz capabilities. For more information, refer to the PCI Local Bus Specifications Rev. 2.2, December 18, 1998.

### 9.1.1. Byte Ordering

The RTL8169S/RTL8110S can be configured to order the bytes of data on the PCI AD bus to conform to little-endian or big-endian ordering through the use of the ENDIAN bit of the C+ Command Register. When the RTL8169S/RTL8110S is configured in big-endian mode, all the data in data phase of either memory or I/O transaction to or from RTL8169S/RTL8110S is in big-endian mode. All data in data phase of any PCI configuration transaction to RTL8169S/RTL8110S should be in little-endian mode, no matter the RTL8169S/RTL8110S is set to big-endian or little-endian mode.

When configured for little-endian (ENDIAN bit=0), the byte orientation for receive and transmit data and descriptors in system memory is as follows:

| 31 – 24 | 23 – 16 | 15 – 8 | 7 – 0 |
|---|---|---|---|
| **Byte 3** | **Byte 2** | **Byte 1** | **Byte 0** |
| C/BE[3] (MSB) | C/BE[2] | C/BE[1] | C/BE[0] (LSB) |

Little-Endian Byte Ordering

When configured for big-endian mode (ENDIAN bit=1), the byte orientation for receive and transmit data and descriptors in system memory is as follows:

| 31 – 24 | 23 – 16 | 15 – 8 | 7 – 0 |
|---|---|---|---|
| **Byte 0** | **Byte 1** | **Byte 2** | **Byte 3** |
| C/BE[3] (LSB) | C/BE[2] | C/BE[1] | C/BE[0] (MSB) |

Big-Endian Byte Ordering

### 9.1.2. Interrupt Control

Interrupts are performed by asynchronously asserting the INTAB pin. This pin is an open drain output. The source of the interrupt can be determined by reading the Interrupt Status Register (ISR). One or more bits in the ISR will be set, denoting all currently pending interrupts. Writing 1 to any bit in ISR register clears that bit. Masking of specific interrupts can be accomplished by using the Interrupt Mask Register (IMR). Assertion of INTAB can be prevented by clearing the Interrupt Enable bit in the Interrupt Mask Register. This allows the system to defer interrupt processing as needed.

### 9.1.3. Latency Timer

The PCI Latency Timer described in LTR defines the maximum number of bus clocks that the device will hold the bus. Once the device gains control of the bus and issues FRAMEB, the Latency Timer will begin counting down. The LTR register specifies, in units of PCI bus clocks, the value of the latency timer of the RTL8169S/RTL8110S. When the RTL8169S/RTL8110S asserts FRAMEB, it enables its latency timer to count. If the RTL8169S/RTL8110S deasserts FRAMEB prior to count expiration, the content of the latency timer is ignored. Otherwise, after the count expires, the RTL8169S/RTL8110S initiates transaction termination as soon as its GNTB is deasserted. Software is able to read or write to LTR, and the default value is 00H.

### 9.1.4. 64-Bit Data Operation

The RTL8169S/RTL8110S samples the REQ64B pin at PCI RSTB deasserted to determine if the bus is 64-bit capable.

### 9.1.5. 64-Bit Addressing

The RTL8169S/RTL8110S supports 64-bit addressing (Dual Address Cycle, DAC) as a bus master for transferring descriptor and packet data information. The DAC mode can be enabled or disabled through software. The RTL8169S/RTL8110S only supports 32-bit addressing as a target.

## *9.2. Bus Operation*

### 9.2.1. Target Read

A Target Read operation starts with the system generating FRAMEB, Address, and either an IO read (0010b) or Memory Read (0110b) command. If the 32-bit address on the address bus matches the IO address range specified in IOAR (for I/O reads) or the memory address range specified in MEM (for memory reads), the RTL8169S/RTL8110S will generate DEVSELB 2 clock cycles later (medium speed). The system must tri-state the Address bus, and convert the C/BE bus to byte enables, after the address cycle. On the 2nd cycle after the assertion of DEVSELB, all 32-bits of data and TRDYB will become valid. If IRDYB is asserted at that time, TRDYB will be forced HIGH on the next clock for 1 cycle, and then tri-stated.

If FRAMEB is asserted beyond the assertion of IRDYB, the RTL8169S/RTL8110S will still make data available as described above, but will also issue a Disconnect. That is, it will assert the STOPB signal with TRDYB. STOPB will remain asserted until FRAMEB is detected as deasserted.

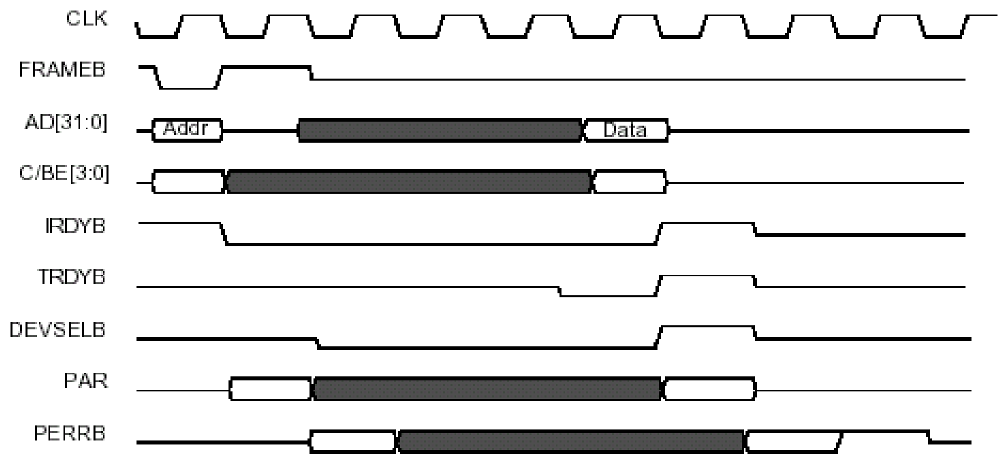



**Figure 5. Target Read Operation**

## 9.2.2. Target Write

A Target Write operation starts with the system generating FRAMEB, Address, and Command (0011b or 0111b). If the upper 24 bits on the address bus match IOAR (for I/O reads) or MEM (for memory reads), the RTL8169S/RTL8110S will generate DEVSELB 2 clock cycles later. On the 2nd cycle after the assertion of DEVSELB, the device will monitor the IRDYB signal. If IRDYB is asserted at that time, the RTL8169S/RTL8110S will assert TRDYB. On the next clock the 32-bit double word will be latched in, and TRDYB will be forced HIGH for 1 cycle and then tri-stated. Target write operations must be 32-bits wide.

If FRAMEB is asserted beyond the assertion of IRDYB, the RTL8169S/RTL8110S will still latch the first double word as described above, but will also issue a Disconnect. That is, it will assert the STOPB signal with TRDYB. STOPB will remain asserted until FRAMEB is detected as deasserted.

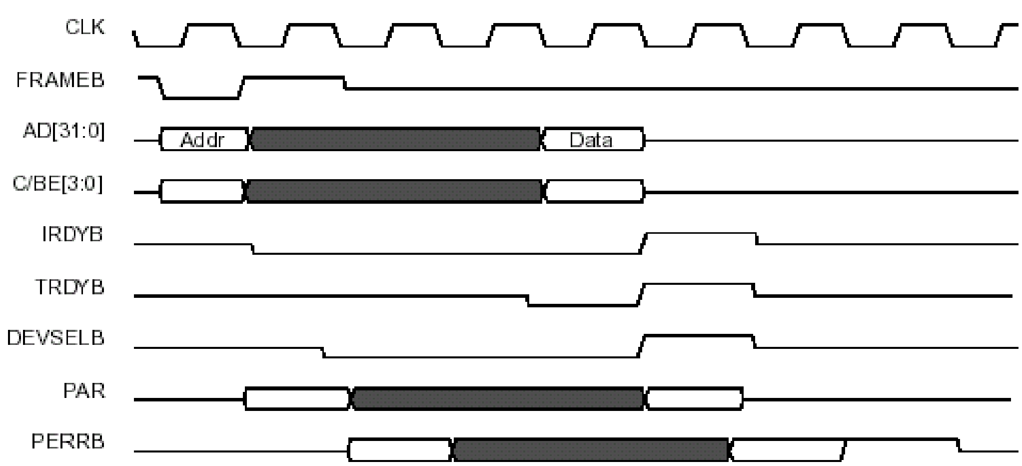



**Figure 6. Target Write Operation**

### 9.2.3. Master Read

A Master Read operation starts with the RTL8169S/RTL8110S asserting REQB. If GNTB is asserted within 2 clock cycles, FRAMEB, Address, and Command will be generated 2 clocks after REQB (Address and FRAMEB for 1 cycle only). If GNTB is asserted 3 cycles or later, FRAMEB, Address, and Command will be generated on the clock following GNTB.

The device will wait for 8 cycles for the assertion of DEVSELB. If DEVSELB is not asserted within 8 clocks, the device will issue a master abort by asserting FRAMEB HIGH for 1 cycle, and IRDYB will be forced HIGH on the following cycle. Both signals will become tri-state on the cycle following their deassertion.

On the clock edge after the generation of Address and Command, the address bus will become tri-state, and the C/BE bus will contain valid byte enables. On the clock edge after FRAMEB was asserted, IRDYB will be asserted (and FRAMEB will be deasserted if this is to be a single read operation). On the clock where both TRDYB and DEVSELB are detected as asserted, data will be latched in (and the byte enables will change if necessary). This will continue until the cycle following the deassertion of FRAMEB.

On the clock where the second to last read cycle occurs, FRAMEB will be forced HIGH (it will be tri-stated 1 cycle later). On the next clock edge that the device detects TRDYB asserted, it will force IRDYB HIGH. It, too, will be tri-stated 1 cycle later. This will conclude the read operation. The RTL8169S/RTL8110S will never force a wait state during a read operation.

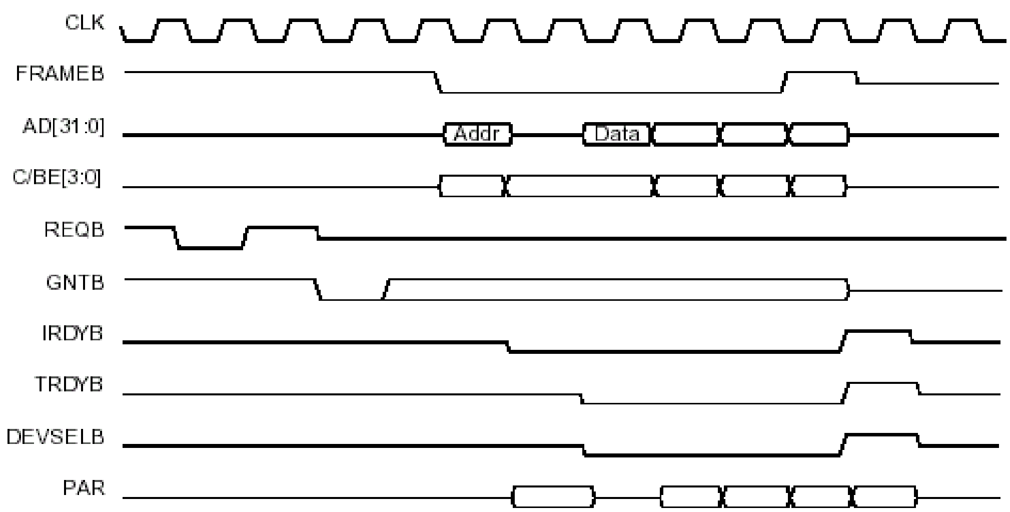



**Figure 7. Master Read Operation**

### 9.2.4. Master Write

A Master Write operation starts with the RTL8169S/RTL8110S asserting REQB. If GNTB is asserted within 2 clock cycles, FRAMEB, Address, and Command will be generated 2 clocks after REQB (Address and FRAMEB for 1 cycle only). If GNTB is asserted 3 cycles or later, FRAMEB, Address, and Command will be generated on the clock following GNTB.

The device will wait for 8 cycles for the assertion of DEVSELB. If DEVSELB is not asserted within 8 clocks, the device will issue a Master Abort by asserting FRAMEB HIGH for 1 cycle. IRDYB will be forced HIGH on the following cycle. Both signals will become tri-state on the cycle following their deassertion.

On the clock edge after the generation of Address and Command, the data bus will become valid, and the C/BE bus will contain valid byte enables. On the clock edge after FRAMEB was asserted, IRDYB will be asserted (and FRAMEB will be deasserted if this is to be a single read operation). On the clock where both TRDYB and DEVSELB are detected as asserted, valid data for the next cycle will become available (and the byte enables will change if necessary). This will continue until the cycle following the deassertion of FRAMEB.

On the clock where the second to last write cycle occurs, FRAMEB will be forced HIGH (it will be tri-stated 1 cycle later). On the next clock edge that the device detects TRDYB asserted, it will force IRDYB HIGH. It, too, will be tri-stated 1 cycle later. This will conclude the write operation. The RTL8169S/RTL8110S will never force a wait state during a write operation.

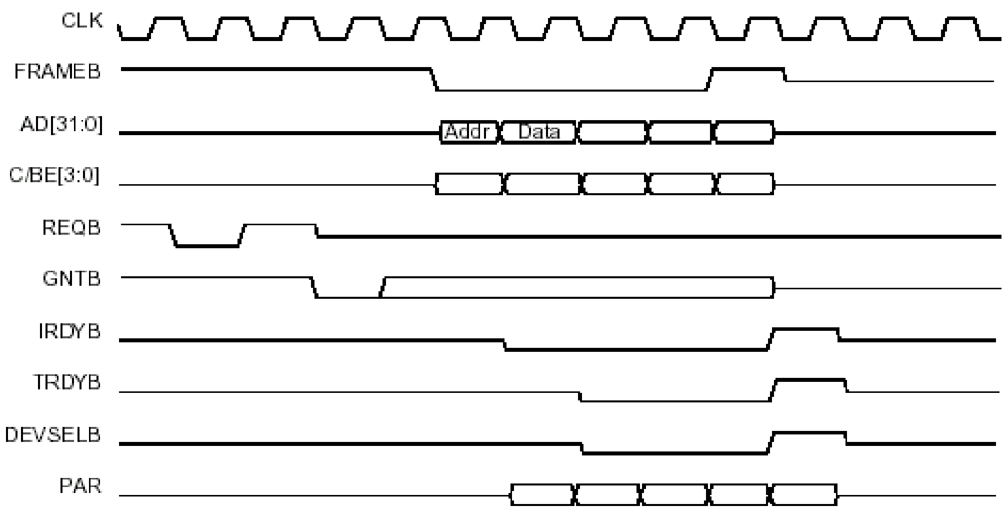



**Figure 8. Master Write Operation**

### 9.2.5. Configuration Access

Configuration register accesses are similar to target reads and writes in that they are single data word transfers and are initiated by the system. For the system to initiate a Configuration access, it must also generate IDSEL as well as the correct Command (1010b or 1011b) during the Address phase. The RTL8169S/RTL8110S will respond as it does during Target operations. Configuration reads must be 32-bits wide, but writes may access individual bytes.

# *9.3. Packet Buffering*

The RTL8169S/RTL8110S incorporates two independent FIFOs for transferring data to/from the system interface and from/to the network. The FIFOs, providing temporary storage of data freeing the host system from the real-time demands of the network.

The way in which the FIFOs are emptied and filled is controlled by the FIFO threshold values in the Max Transmit Packet Size and Receive Configuration registers. These values determine how full or empty the FIFOs must be before the device requests the bus. Once the RTL8169S/RTL8110S requests the bus, it will attempt to empty or fill the FIFOs as allowed by the respective MXDMA settings in the Transmit Configuration and Receive Configuration registers.

## 9.3.1. Transmit Buffer Manager

The buffer management scheme used on the RTL8169S/RTL8110S allows quick, simple and efficient use of the frame buffer memory. The buffer management scheme uses separate buffers and descriptors for packet information. This allows effective transfers of data to the transmit buffer manager by simply transferring the descriptor information to the transmit queue.

The Tx Buffer Manager DMAs packet data from system memory and places it in the 8KB transmit FIFO, and pulls data from the FIFO to send to the Tx MAC. Multiple packets may be present in the FIFO, allowing packets to be transmitted with minimum interframe gap. Additionally, once the RTL8169S/RTL8110S requests the bus, it will attempt to fill the FIFO as allowed by the MXDMA setting.

The Tx Buffer Manager process also supports priority queuing of transmit packets. It handles this by drawing from two separate descriptor lists to fill the internal FIFO. If packets are available in the high priority queues, they will be loaded into the FIFO before those of low priority.

## 9.3.2. Receive Buffer Manager

The Rx Buffer Manager uses the same buffer management scheme as used for transmits. The Rx Buffer Manager retrieves packet data from the Rx MAC and places it in the 64KB receive data FIFO, and pulls data from the FIFO for DMA to system memory. Similar to the transmit FIFO, the receive FIFO is controlled by the FIFO threshold value in RXFTH. This value determines the number of long words written into the FIFO from the MAC unit before a DMA request for system memory occurs. Once the RTL8169S/RTL8110S gets the bus, it will continue to transfer the long words from the FIFO until the data in the FIFO is less than one long word, or has reached the end of the packet, or the max DMA burst size is reached, as set in MXDMA.

## 9.3.3. Packet Recognition

The Rx packet filter and recognition logic allows software to control what packets are to be accepted, based on destination address and packet type. Address recognition logic includes support for broadcast, multicast hash, and unicast addresses. The packet recognition logic includes support for WOL, Pause, and programmable pattern recognition.

# 9.4. PCI Configuration Space Table

**Table 15. PCI Configuration Space Table**

| No. | Name | Type | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 00h | VID | R | VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 |
| 01h | | R | VID15 | VID14 | VID13 | VID12 | VID11 | VID10 | VID9 | VID8 |
| 02h | DID | R | DID7 | DID6 | DID5 | DID4 | DID3 | DID2 | DID1 | DID0 |
| 03h | | R | DID15 | DID14 | DID13 | DID12 | DID11 | DID10 | DID9 | DID8 |
| 04h | Command | R | 0 | PERRSP | 0 | MWIEN | 0 | BMEN | MEMEN | IOEN |
| | | W | - | PERRSP | - | MWIEN | - | BMEN | MEMEN | IOEN |
| 05h | | R | 0 | 0 | 0 | 0 | 0 | 0 | FBTBEN | SERREN |
| | | W | - | - | - | - | - | - | - | SERREN |
| 06h | Status | R | FBBC | 0 | 0 | NewCap | 0 | 0 | 0 | 0 |
| 07h | | R | DPERR | SSERR | RMABT | RTABT | STABT | DST1 | DST0 | DPD |
| | | W | DPERR | SSERR | RMABT | RTABT | STABT | - | - | DPD |
| 08h | Revision ID | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 09h | PIFR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Ah | SCR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Bh | BCR | R | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0Ch | CLS | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Dh | LTR | R | LTR7 | LTR6 | LTR5 | LTR4 | LTR3 | LTP2 | LTR1 | LTR0 |
| | | W | LTR7 | LTR6 | LTR5 | LTR4 | LTR3 | LTP2 | LTR1 | LTR0 |
| 0Eh | HTR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Fh | BIST | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10h | IOAR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IOIN |
| | | W | - | - | - | - | - | - | - | - |
| 11h | | R/W | IOAR15 | IOAR14 | IOAR13 | IOAR12 | IOAR11 | IOAR10 | IOAR9 | IOAR8 |
| 12h | | R/W | IOAR23 | IOAR22 | IOAR21 | IOAR20 | IOAR19 | IOAR18 | IOAR17 | IOAR16 |
| 13h | | R/W | IOAR31 | IOAR30 | IOAR29 | IOAR28 | IOAR27 | IOAR26 | IOAR25 | IOAR24 |
| 14h | MEMAR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MEMIN |
| | | W | - | - | - | - | - | - | - | - |
| 15h | | R/W | MEM15 | MEM14 | MEM13 | MEM12 | MEM11 | MEM10 | MEM9 | MEM8 |
| 16h | | R/W | MEM23 | MEM22 | MEM21 | MEM20 | MEM19 | MEM18 | MEM17 | MEM16 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 17h | | R/W | MEM31 | MEM30 | MEM29 | MEM28 | MEM27 | MEM26 | MEM25 | MEM24 |
| 18h-27h | RESERVED | | | | | | | | | |
| 28h-2Bh | RESERVED | | | | | | | | | |
| 2Ch | SVID | R | SVID7 | SVID6 | SVID5 | SVID4 | SVID3 | SVID2 | SVID1 | SVID0 |
| 2Dh | | R | SVID15 | SVID14 | SVID13 | SVID12 | SVID11 | SVID10 | SVID9 | SVID8 |
| 2Eh | SMID | R | SMID7 | SMID6 | SMID5 | SMID4 | SMID3 | SMID2 | SMID1 | SMID0 |
| 2Fh | | R | SMID15 | SMID14 | SMID13 | SMID12 | SMID11 | SMID10 | SMID9 | SMID8 |
| 30h | BMAR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BROMEN |
| | | W | - | - | - | - | - | - | - | BROMEN |
| 31h | | R | BMAR15 | BMAR14 | BMAR13 | BMAR12 | BMAR11 | 0 | 0 | 0 |
| | | W | BMAR15 | BMAR14 | BMAR13 | BMAR12 | BMAR11 | - | - | - |
| 32h | | R/W | BMAR23 | BMAR22 | BMAR21 | BMAR20 | BMAR19 | BMAR18 | BMAR17 | BMAR16 |
| 33h | | R/W | BMAR31 | BMAR30 | BMAR29 | BMAR28 | BMAR27 | BMAR26 | BMAR25 | BMAR24 |
| 34h | Cap_Ptr | R | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 35h-3Bh | RESERVED | | | | | | | | | |
| 3Ch | ILR | R/W | IRL7 | ILR6 | ILR5 | ILR4 | ILR3 | ILR2 | ILR1 | ILR0 |
| 3Dh | IPR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 3Eh | MNGNT | R | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 3Fh | MXLAT | R | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 40h–5Fh | RESERVED | | | | | | | | | |
| 60h | VPDID | R | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 61h | NextPtr | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 62h | Flag VPD Address | R/W | VPDADDR7 | VPDADDR6 | VPDADDR5 | VPDADDR4 | VPDADDR3 | VPDADDR2 | VPDADDR1 | VPDADDR0 |
| 63h | | R/W | Flag | VPDADDR14 | VPDADDR13 | VPDADDR12 | VPDADDR11 | VPDADDR10 | VPDADDR9 | VPDADDR8 |
| 64h | VPD Data | R/W | Data7 | Data6 | Data5 | Data4 | Data3 | Data2 | Data1 | Data0 |
| 65h | | R/W | Data15 | Data14 | Data13 | Data12 | Data11 | Data10 | Data9 | Data8 |
| 66h | | R/W | Data23 | Data22 | Data21 | Data20 | Data19 | Data18 | Data17 | Data16 |
| 67h | | R/W | Data31 | Data30 | Data29 | Data28 | Data27 | Data26 | Data25 | Data24 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 68h-DBh | RESERVED | | | | | | | | | |
| DCh | PMID | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| DDh | NextPtr | R | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| DEh | PMC | R | Aux_I_b1 | Aux_I_b0 | DSI | Reserved | PMECLK | Version | | |
| DFh | | R | PME_D3$_{cold}$ | PME_D3$_{hot}$ | PME_D2 | PME_D1 | PME_D0 | D2 | D1 | Aux_I_b2 |
| E0h | PMCSR | R | 0 | 0 | 0 | 0 | 0 | 0 | Power State | |
| | | W | - | - | - | - | - | - | Power State | |
| E1h | | R | PME_Status | - | - | - | - | - | - | PME_En |
| | | W | PME_Status | - | - | - | - | - | - | PME_En |
| E2h-FFh | RESERVED | | | | | | | | | |

« The above table is based on both VPD and Power Management are enabled.

## *9.5. PCI Configuration Space Functions*

The PCI configuration space is intended for configuration, initialization, and catastrophic error handling functions. The functions of the RTL8169S/RTL8110S's configuration space are described below.

**VID:** Vendor ID. This field will be set to a value corresponding to PCI Vendor ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 10ECh which is Realtek Semiconductor's PCI Vendor ID.

**DID:** Device ID. This field will be set to a value corresponding to PCI Device ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 8129h.

**Command:** The command register is a 16-bit register used to provide coarse control over a device's ability to generate and respond to PCI cycles.

**Table 16. Command Register in PCI Config Space**

| Bit | Symbol | Description |
|---|---|---|
| 15-10 | - | **Reserved** |
| 9 | FBTBEN | **Fast Back-To-Back Enable:** Config3<FBtBEn>=0:Read as 0. Write operation has no effect. The RTL8169S/RTL8110S will not generate Fast Back-to-back cycles. When Config3<FbtBEn>=1, This read/write bit controls whether or not a master can do fast back-to-back transactions to different devices. Initialization software will set the bit if all targets are fast back-to-back capable. A value of 1 means the master is allowed to generate fast back-to-back transaction to different |

| | | |
|---|---|---|
| | | agents. A value of 0 means fast back-to-back transactions are only allowed to the same agent. This bit's state after RST# is 0. |
| 8 | SERREN | **System Error Enable:** When set to 1, the RTL8169S/RTL8110S asserts the SERRB pin when it detects a parity error on the address phase (AD<31:0> and CBEB<3:0> ). |
| 7 | ADSTEP | **Address/Data Stepping:** Read as 0, and write operations have no effect. The RTL8169S/RTL8110S never performs address/data stepping. |
| 6 | PERRSP | **Parity Error Response:** When set to 1, the RTL8169S/RTL8110S will assert the PERRB pin on the detection of a data parity error when acting as the target, and will sample the PERRB pin as the master. When set to 0, any detected parity error is ignored and the RTL8169S/RTL8110S continues normal operation.<br>Parity checking is disabled after hardware reset (RSTB). |
| 5 | VGASNOOP | **VGA palette SNOOP:** Read as 0, write operations have no effect. |
| 4 | MWIEN | **Memory Write and Invalidate cycle Enable:** This is an enable bit for using the Memory Write and Invalidate command. When this bit is 1, the RTL8169S/RTL8110S as a master may generate the command. When this bit is 0, the RTL8169S/RTL8110S may generate Memory Write command instead. State after PCI RSTB is 0. |
| 3 | SCYCEN | **Special Cycle Enable:** Read as 0, write operations have no effect. The RTL8169S/RTL8110S ignores all special cycle operations. |
| 2 | BMEN | **Bus Master Enable:** When set to 1, the RTL8169S/RTL8110S is capable of acting as a PCI bus master. When set to 0, it is prohibited from acting as a bus master.<br>For normal operations, this bit must be set by the system BIOS. |
| 1 | MEMEN | **Memory Space Access:** When set to 1, the RTL8169S/RTL8110S responds to memory space accesses. When set to 0, the RTL8169S/RTL8110S ignores memory space accesses. |
| 0 | IOEN | **I/O Space Access:** When set to 1, the RTL8169S/RTL8110S responds to IO space accesses. When set to 0, the RTL8169S/RTL8110S ignores I/O space accesses. |

**Status:** The status register is a 16-bit register used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set.

**Table 17. Status Register in PCI Config Space**

| Bit | Symbol | Description |
|---|---|---|
| 15 | DPERR | **Detected Parity Error:** This bit, when set, indicates that the RTL8169S/RTL8110S has detected a parity error, even if parity error handling is disabled in command register PERRSP bit. |
| 14 | SSERR | **Signaled System Error:** This bit, when set, indicates that the RTL8169S/RTL8110S has asserted the system error pin, SERRB. Writing a 1 clears this bit to 0. |

| | | |
|---|---|---|
| 13 | RMABT | **Received Master Abort:** This bit, when set, indicates that the RTL8169S/RTL8110S has terminated a master transaction with master abort. Writing a 1 clears this bit to 0. |
| 12 | RTABT | **Received Target Abort:** This bit, when set, indicates that an RTL8169S/RTL8110S master transaction was terminated due to a target abort. Writing a 1 clears this bit to 0. |
| 11 | STABT | **Signaled Target Abort:** This bit is set to 1 whenever the RTL8169S/RTL8110S terminates a transaction with a target abort. Writing a 1 clears this bit to 0. |
| 10-9 | DST1-0 | **Device Select Timing:** These bits encode the timing of DEVSELB. They are set to 01b (medium), indicating the RTL8169S/RTL8110S will assert DEVSELB two clocks after FRAMEB is asserted. |
| 8 | DPD | **Data Parity error Detected:** This bit is set when the following conditions are met:<br>* The RTL8169S/RTL8110S asserts parity error (PERRB pin) or it senses the assertion of PERRB pin by another device.<br>* The RTL8169S/RTL8110S operates as a bus master for the operation that caused the error.<br>* The Command register PERRSP bit is set.<br>Writing a 1 clears this bit to 0. |
| 7 | FBBC | **Fast Back-To-Back Capable:** Config3<FbtBEn>=0, Read as 0, write operations have no effect. Config3<FbtBEn>=1, Read as 1. |
| 6 | UDF | **User Definable Features Supported:** Read as 0, and write operations have no effect. The RTL8169S/RTL8110S does not support UDF. |
| 5 | 66MHz | **66MHz Capable:** Read as 1, and write operations have no effect. The RTL8169S/RTL8110S supports 66MHz PCI clock. |
| 4 | NewCap | **New Capability:** Config3<PMEn>=0, Read as 0, and write operations have no effect. Config3<PMEn>=1, Read as 1. |
| 0-3 | - | **Reserved** |

**RID:** Revision ID Register

The Revision ID register is an 8-bit register that specifies the RTL8169S/RTL8110S controller revision number.

**PIFR:** Programming Interface Register

The programming interface register is an 8-bit register that identifies the programming interface of the RTL8169S/RTL8110S controller. The PCI specification reversion 2.1 doesn't define any other specific value for network devices. So PIFR = 00h.

**SCR:** Sub-Class Register

The Sub-class register is an 8-bit register that identifies the function of the RTL8169S/RTL8110S. SCR = 00h indicates that the RTL8169S/RTL8110S is an Ethernet controller.

**BCR:** Base-Class Register

The Base-class register is an 8-bit register that broadly classifies the function of the RTL8169S/RTL8110S. BCR = 02h indicates that the RTL8169S/RTL8110S is a network controller.

**CLS:** Cache Line Size

Specifies, in units of 32-bit words (double-words), the system cache line size. The RTL8169S/RTL8110S supports cache line size of 8, and 16 longwords (DWORDs). The RTL8169S/RTL8110S uses Cache Line Size for PCI commands that are cache oriented, such as memory-read-line, memory-read-multiple, and memory-write-and-invalidate.

**LTR:** Latency Timer Register

Specifies, in units of PCI bus clocks, the value of the latency timer of the RTL8169S/RTL8110S.

When the RTL8169S/RTL8110S asserts FRAMEB, it enables its latency timer to count. If the RTL8169S/RTL8110S deasserts FRAMEB prior to count expiration, the content of the latency timer is ignored. Otherwise, after the count expires, the RTL8169S/RTL8110S initiates transaction termination as soon as its GNTB is deasserted. Software is able to read or write, and the default value is 00h.

**HTR:** Header Type Register

Reads will return a 0, writes are ignored.

**BIST:** Built-in Self Test

Reads will return a 0, writes are ignored.

**IOAR:** This register specifies the BASE IO address which is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that it can be mapped into IO space.

**Table 18. IOAR Register in PCI Config Space**

| Bit | Symbol | Description |
|---|---|---|
| 31-8 | IOAR31-8 | **BASE IO Address:** This is set by software to the Base IO address for the operational register map. |
| 7-2 | IOSIZE | **Size Indication:** Read back as 0. This allows the PCI bridge to determine that the RTL8169S/RTL8110S requires 256 bytes of IO space. |
| 1 | - | **Reserved** |
| 0 | IOIN | **IO Space Indicator:** Read only. Set to 1 by the RTL8169S/RTL8110S to indicate that it is capable of being mapped into IO space. |

**MEMAR:** This register specifies the base memory address for memory accesses to the RTL8169S/RTL8110S operational registers. This register must be initialized prior to accessing any RTL8169S/RTL8110S's register with memory access.

**Table 19. MEMAR Register in PCI Config Space**

| Bit | Symbol | Description |
|---|---|---|
| 31-8 | MEM31-8 | **Base Memory Address:** This is set by software to the base address for the operational register map. |

| | | |
|---|---|---|
| 7-4 | MEMSIZE | **Memory Size:** These bits return 0, which indicates that the RTL8169S/RTL8110S requires 256 bytes of Memory Space. |
| 3 | MEMPF | **Memory Prefetchable:** Read only. Set to 0 by the RTL8169S/RTL8110S. |
| 2-1 | MEMLOC | **Memory Location Select:** Read only. Set to 0 by the RTL8169S/RTL8110S. This indicates that the base register is 32-bits wide and can be placed anywhere in the 32-bit memory space. |
| 0 | MEMIN | **Memory Space Indicator:** Read only. Set to 0 by the RTL8169S/RTL8110S to indicate that it is capable of being mapped into memory space. |

**SVID:** Subsystem Vendor ID. This field will be set to a value corresponding to PCI Subsystem Vendor ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 10ECh which is Realtek Semiconductor's PCI Subsystem Vendor ID.

**SMID:** Subsystem ID. This field will be set to value corresponding to PCI Subsystem ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 8129h.

**BMAR:** This register specifies the base memory address for memory accesses to the RTL8169S/RTL8110S operational registers. This register must be initialized prior to accessing any of the RTL8169S/RTL8110S's register with memory access.

**Table 20. BMAR Register in PCI Config Space**

| Bit | Symbol | Description |
|---|---|---|
| 31-18 | BMAR31-18 | **Boot ROM Base Address** |
| 17-11 | ROMSIZE | **Boot ROM Size:** These bits indicate how many Boot ROM spaces to be supported. The Relationship between Config 0 <BS2:0> and BMAR17-11 is as follows:<br>**BS2 BS1 BS0 Description**<br>0 0 0 No Boot ROM, BROMEN=0 (R)<br>0 0 1 8K Boot ROM, BROMEN (R/W), BMAR12-11 = 0 (R), BMAR17-13 (R/W)<br>0 1 0 16K Boot ROM, BROMEN (R/W), BMAR13-11 = 0 (R), BMAR17-14 (R/W)<br>0 1 1 32K Boot ROM, BROMEN (R/W), BMAR14-11 = 0 (R), BMAR17-15 (R/W)<br>1 0 0 64K Boot ROM, BROMEN (R/W), BMAR15-11 = 0 (R), BMAR17-16 (R/W)<br>1 0 1 128K Boot ROM, BROMEN(R/W), BMAR16-11=0 (R), BMAR17 (R/W)<br>1 1 0 unused<br>1 1 1 unused |
| 10-1 | - | **Reserved** (read back 0) |
| 0 | BROMEN | **Boot ROM Enable:** This is used by the PCI BIOS to enable accesses to Boot ROM. |

**ILR:** Interrupt Line Register

The Interrupt Line Register is an 8-bit register used to communicate with the routing of the interrupt. It is written by the POST software to set interrupt line for the RTL8169S/RTL8110S.

**IPR:** Interrupt Pin Register

The Interrupt Pin register is an 8-bit register indicating the interrupt pin used by the RTL8169S/RTL8110S. The RTL8169S/RTL8110S uses INTA interrupt pin. Read only. IPR = 01h.

**MNGNT:** Minimum Grant Timer: Read only

Specifies how long a burst period the RTL8169S/RTL8110S needs in units of 1/4 microsecond. This field will be set to a value from the external EEPROM. If there is no EEPROM, this field will default to a value of 20h.

**MXLAT:** Maximum Latency Timer: Read only

Specifies how often the RTL8169S/RTL8110S needs to gain access to the PCI bus in unit of 1/4 microsecond. This field will be set to a value from the external EEPROM. If there is no EEPROM, this field will default to a value of 20h.

## 9.6. *Default Value After Power-on (RSTB asserted)*

**Table 21. Power-on Default Value in PCI Configuration Space**

| No. | Name | Type | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 00h | VID | R | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 01h | | R | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 02h | DID | R | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 03h | | R | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 04h | Command | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | - | PERRSP | - | MWIEN | - | BMEN | MEMEN | IOEN |
| 05h | | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | - | - | - | - | - | - | - | SERREN |
| 06h | Status | R | 0 | 0 | 0 | NewCap | 0 | 0 | 0 | 0 |
| 07h | | R | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | W | DPERR | SSERR | RMABT | RTABT | STABT | - | - | DPD |
| 08h | Revision ID | R | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 09h | PIFR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Ah | SCR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Bh | BCR | R | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0Ch | CLS | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Dh | LTR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | LTR7 | LTR6 | LTR5 | LTR4 | LTR3 | LTP2 | LTR1 | LTR0 |
| 0Eh | HTR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0Fh | BIST | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10h | IOAR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 11h | | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 12h | | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 13h | | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 14h | MEMAR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15h | | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16h | | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 17h | | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 18h<br>\|<br>27h | - | RESERVED(ALL 0) | | | | | | | | |
| 28h | - | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 29h | | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2Ah | | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2Bh | | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2Ch | SVID | R | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 2Dh | | R | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 2Eh | SMID | R | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 2Fh | | R | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 30h | BMAR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | - | - | - | - | - | - | - | BROMEN |
| 31h | | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | BMAR15 | BMAR14 | BMAR13 | BMAR12 | BMAR11 | - | - | - |
| 32h | | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 33h | | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 34h | Cap-Ptr | R | Ptr7 | Ptr6 | Ptr5 | Ptr4 | Ptr3 | Ptr2 | Ptr1 | Ptr0 |
| 35h<br>\|<br>3Bh | - | RESERVED(ALL 0) | | | | | | | | |
| 3Ch | ILR | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3Dh | IPR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 3Eh | MNGNT | R | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 3Fh | MXLAT | R | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| 40h<br>\|<br>FFh | - | RESERVED(ALL 0) |

## 9.7. Power Management Function

The RTL8169S/RTL8110S is compliant with ACPI (Rev 1.0, 1.0b, 2.0), PCI Power Management (Rev 1.1), and Network Device Class Power Management Reference Specification (V1.0a), such as to support an OS-directed Power Management (OSPM) environment.

The RTL8169S/RTL8110S can monitor the network for a Wakeup Frame, a Magic Packet, or a Re-LinkOk, and notify the system via PME# when such a packet or event occurs. Then, the whole system can be restored to a normal state to process incoming jobs.

When the RTL8169S/RTL8110S is in power down mode (D1 ~ D3):

- The Rx state machine is stopped, and the RTL8169S/RTL8110S monitors the network for wakeup events such as a Magic Packet, Wakeup Frame, and/or Re-LinkOk, in order to wake up the system. When in power down mode, the RTL8169S/RTL8110S will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the Rx FIFO buffer.
- The FIFO status and packets that have already been received into the Rx FIFO before entering power down mode are held by the RTL8169S/RTL8110S.
- Transmission is stopped. PCI bus master mode is stopped. The Tx FIFO buffer is held.
- After restoration to a D0 state, the RTL8169S/RTL8110S transfers data that was not moved into the Tx FIFO buffer during power down mode. Packets that were not transmitted completely last time are re-transmitted.

The D3cold_support_PME bit (bit15, PMC register) and the Aux_I_b2:0 bits (bit8:6, PMC register) in PCI configuration space depend on the existence of Aux power (bit15, PMC) = 1.
If EEPROM D3cold_support_PME bit (bit15, PMC) = 0, the above 4 bits are all 0's.
Example:
**If EEPROM D3c_support_PME = 1:**

- If Aux. power exists, then PMC in PCI config space is the same as EEPROM PMC
  (if EEPROM PMC = C2 F7, then PCI PMC = C2 F7)
- If Aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0 's
  (if EEPROM PMC = C2 F7, the PCI PMC = 02 76)

In the above case, if wakeup support is desired when main power is off, it is suggested that the EEPROM PMC be set to C2 F7 (Realtek EEPROM default value).
**If EEPROM D3c_support_PME = 0:**

- If Aux. power exists, then PMC in PCI config space is the same as EEPROM PMC
  (if EEPROM PMC = C2 77, then PCI PMC = C2 77)

- If Aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's. (if EEPROM PMC = C2 77, then PCI PMC = 02 76)

In the above case, if wakeup support is not desired when main power is off, it is suggested that the EEPROM PMC be set to 02 76.

Link Wakeup occurs only when the following conditions are met:

- The LinkUp bit (CONFIG3#4) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the PME# can be asserted in the current power state.
- The Link status is re-established.

Magic Packet Wakeup occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8169S/RTL8110S, e.g. a broadcast, multicast, or unicast packet addressed to the current RTL8169S/RTL8110S adapter.
- The received Magic Packet does not contain a CRC error.
- The Magic bit (CONFIG3#5) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the PME# can be asserted in the current power state.
- The Magic Packet pattern matches, i.e. 6 * FFh + MISC (can be none) + 16 * DID(Destination ID) in any part of a valid (Fast) Ethernet packet.

A Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame is acceptable to the RTL8169S/RTL8110S, e.g. a broadcast, multicast, or unicast address to the current RTL8169S/RTL8110S adapter.
- The received Wakeup Frame does not contain a CRC error.
- The PMEn bit (CONFIG1#0) is set to 1.
- The 16-bit CRC* of the received Wakeup Frame matches with the 16-bit CRC* of the sample Wakeup Frame pattern given by the local machine's OS. Or, the RTL8169S/RTL8110S is configured to allow direct packet wakeup, e.g. a broadcast, multicast, or unicast network packet.

*16-bit CRC: The RTL8169S/RTL8110S supports two normal wakeup frames (covering 64 mask bytes from offset 0 to 63 of any incoming network packet) and three long wakeup frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet).

The PME# signal is asserted only when the following conditions are met:

1. The PMEn bit (bit0, CONFIG1) is set to 1.
2. The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
3. The RTL8169S/RTL8110S may assert PME# in the current power state or in isolation state, depending on the PME_Support (bit15-11) setting of the PMC register in PCI Configuration Space.
4. A Magic Packet, LinkUp, or Wakeup Frame been received.

5. Writing a 1 to the PME_Status (bit15) of the PMCSR register in the PCI Configuration Space clears this bit and causes the RTL8169S/RTL8110S to stop asserting a PME# (if enabled).

When the device is in power down mode, e.g. D1-D3, the IO, MEM, and Boot ROM spaces are all disabled. After a RST# assertion, the device's power state is restored to D0 automatically if the original power state was $D3_{cold}$. There is no hardware delay at the device's power state transition. When in ACPI mode, the device does not support PME (Power Management Enable) from D0 (this is the Realtek default setting of the PMC register auto loaded from EEPROM). The setting may be changed from the EEPROM, if required). The RTL8169S/RTL8110S also supports the legacy LAN WAKE-UP function. The LWAKE pin is used to notify legacy motherboards to execute the wake-up process whenever the device receives a wakeup event, such as Magic Packet.

The LWAKE signal is asserted according to the following settings:

1. LWPME bit (bit4, CONFIG4):

- LWAKE can only be asserted when the PMEB is asserted and the ISOLATEB is low.
- LWAKE is asserted whenever a wakeup event occurs.

2. Bit1 of DELAY byte (offset 1Fh, EEPROM):

- LWAKE signal is enabled.
- LWAKE signal is disabled.

## 9.8. Vital Product Data (VPD)

Bit 31 of the VPD is used to issue VPD read/write command and is also a flag used to indicate whether the transfer of data between the VPD data register and the 93C46/93C56 is completed or not.

1. Write VPD register: (write data to 93C46/93C56)
   Set the flag bit to 1 at the same time the VPD address is written to write VPD data to EEPROM. When the flag bit is reset to 0 by the RTL8169S/RTL8110S, the VPD data (4 bytes per VPD access) has been transferred from the VPD data register to EEPROM.
2. Read VPD register: (read data from 93C46/93C56)
   Reset the flag bit to 0 at the same time the VPD address is written to retrieve VPD data from EEPROM. When the flag bit is set to 1 by the RTL8169S/RTL8110S, the VPD data (4 bytes per VPD access) has been transferred from EEPROM to the VPD data register.

- Please refer to PCI Configuration Space Table in Section 8.1 and PCI 2.2 Specifications for further information.
- The VPD address does not have to be a DWORD-aligned address as defined in the PCI 2.2 Specifications, but the VPD data is always consecutive 4-byte data starting from the VPD address specified.
- Realtek reserves offset 40h to 7Fh in EEPROM mainly for VPD data to be stored.

- The VPD function of the RTL8169S/RTL8110S is designed to be able to access the full range of the 93C46 EEPROM (for 93C56, only the 1st half of the EEPROM content can be accessed via VPD).

# 10. Functional Description

## 10.1. Transmit & Receive Operations

The RTL8169S/RTL8110S supports a new descriptor-based buffer management that will significantly reduce host CPU utilization and is more suitable for server application. The new buffer management algorithm provides capabilities of Microsoft Large-Send offload, IP checksum offload, TCP checksum offload, UDP checksum offload, and IEEE802.1P, 802.1Q VLAN tagging. The RTL8169S/RTL8110S supports up to 1024 consecutive descriptors in memory for transmit and receive separately, which means there might be 3 descriptor rings, one is a high priority transmit descriptor ring, another is a normal priority transmit descriptor ring, and the other is a receive descriptor ring, each descriptor ring may consist of up to 1024 4-double-word consecutive descriptors. Each descriptor consists of 4 consecutive double words. The start address of each descriptor group should be 256-byte alignment. Software must pre-allocate enough buffers and configure all descriptor rings before transmitting and/or receiving packets. Descriptors can be chained to form a packet in both Tx and Rx.

Padding: The RTL8169S/RTL8110S will automatically pad any packets less than 64 bytes (including 4 bytes CRC) to 64-byte long (including 4-byte CRC) before transmitting that packet onto network medium. The padded data are all 0x00.

If a packet consists of 2 or more descriptors, then each of the descriptors in command mode should have the same configuration, except EOR, FS, LS bits.

### 10.1.1. Transmit

This portion implements the transmit portion of 802.3 Media Access Control. The Tx MAC retrieves packet data from the Tx Buffer Manager and sends it out through the transmit physical layer interface. Additionally, the Tx MAC provides MIB control information for transmit packets.

The Tx MAC has the capability to insert a 4-byte VLAN tag in the transmit packet. If Tx VLAN Tag insertion is enabled, the MAC will insert the 4 bytes, as specified in the VTAG register, following the source and destination addresses of the packet. The VLAN tag insertion can be enabled on a global or per-packet basis.

When operating in 1G mode, the RTL8169S/RTL8110S operates in full duplex mode only.

The Tx MAC supports task offloading of IP, TCP, and UDP checksum generation. It is capable of calculating the checksums and inserting them into the packet. The checksum calculation can be enabled on a global or per-packet basis.

The following information describes the structure of Tx descriptor, depending on different states in each Tx descriptor. The minimum Tx buffer should be at least of the size of 1 byte.

**Large-Send Task Offload Tx Descriptor Format (before transmitting, OWN=1, LGSEN=1, Tx command mode 0)**

### Table 22. Large-Send Task Offload Tx Command Descriptor

bit 31 30 29 28 27 26 16 15 14 13 8 7 6 5 4 3 2 1 0

<table>
<tr><td>OWN=1</td><td>EOR</td><td>FS</td><td>LS</td><td>LGSEN=1</td><td colspan="2">Large-Send MSS value (11 bits)</td><td colspan="4">Frame_Length</td><td>Offset 0</td></tr>
<tr><td colspan="5" rowspan="2">RSVD</td><td rowspan="2">TAGC</td><td rowspan="2">RSVD</td><td colspan="4">VLAN_TAG</td><td rowspan="2">Offset 4</td></tr>
<tr><td>VIDL</td><td>PRIO</td><td>CFI</td><td>VIDH</td></tr>
<tr><td colspan="11">TX_BUFFER_ADDRESS_LOW</td><td>Offset 8</td></tr>
<tr><td colspan="11">TX_BUFFER_ADDRESS_HIGH</td><td>Offset 12</td></tr>
</table>

| Offset# | Bit# | Symbol | Description |
|---|---|---|---|
| 0 | 31 | OWN | **Ownership:** This bit, when set, indicates that the descriptor is owned by THE NIC, and the data relative to this descriptor is ready to be transmitted. When cleared, it indicates that the descriptor is owned by host system. The NIC clears this bit when the relative buffer data is transmitted. In this case, OWN=1. |
| 0 | 30 | EOR | **End of Descriptor Ring:** This bit, when set, indicates that this is the last descriptor in descriptor ring. When the NIC's internal transmit pointer reaches here, the pointer will return to the first descriptor of the descriptor ring after transmitting the data relative to this descriptor. |
| 0 | 29 | FS | **First Segment Descriptor:** This bit, when set, indicates that this is the first descriptor of a Tx packet, and that this descriptor is pointing to the first segment of the packet. |
| 0 | 28 | LS | **Last Segment Descriptor:** This bit, when set, indicates that this is the last |

| | | | |
|---|---|---|---|
| | | | descriptor of a Tx packet, and that this descriptor is pointing to the last segment of the packet. |
| 0 | 27 | LGSEN | **Large Send:** A command bit; TCP/IP Large send operation enable. The driver sets this bit to ask the NIC to offload the Large send operation. In this case, LGSEN=1. |
| 0 | 26-16 | MSS | **Maximum Segmentation Size:** An 11-bit long command field, the driver passes Large-Send MSS to the NIC through this field. |
| 0 | 15-0 | Frame_Length | **Transmit Frame Length:** This field indicates the Tx frame length in TX buffer, in byte, to be transmitted. The maximum Large-Send frame length supported is $2^{16}$-1(64KB-1). |
| 4 | 31-18 | RSVD | **Reserved** |
| 4 | 17 | TAGC | **VLAN tag control bit:** 1: Enable. 0: Disable.<br>1: Add TAG. 0x8100 (Ethernet encoded tag protocol ID, indicating that this is a IEEE 802.1Q VLAN packet) is inserted after source address, and 2 bytes are inserted after tag protocol ID from VLAN_TAG field in transmit descriptor.<br>0: Packet remains unchanged when transmitting. I.e., the packet transmitted is the same as it was passed down by upper layer. |
| 4 | 16 | RSVD | **Reserved** |
| 4 | 15-0 | VLAN_TAG | The 2-byte VLAN_TAG contains information, from the upper layer, of user priority, canonical format indication, and VLAN ID. Please refer to IEEE 802.1Q for more VLAN tag information.<br>VIDH: The high 4 bits of a 12-bit VLAN ID.<br>VIDL: The low 8 bits of a 12-bit VLAN ID.<br>PRIO: 3-bit 8-level priority.<br>CFI: Canonical Format Indicator. |
| 8 | 31-0 | TxBuffL | **Low 32-bit address of transmit buffer** |
| 12 | 31-0 | TxBuffH | **High 32-bit address of transmit buffer** |

**Normal (including IP, TCP, UDP Checksum Task Offloads) Tx Descriptor Format (before transmitting, OWN=1, LGSEN=0, Tx command mode 1)**

### Table 23. Normal Tx Command Descriptor

bit 31 30 29 28 27 26 … 16 15 … 8 7 6 5 4 3 2 1 0

<table>
<tr><td>OWN=1</td><td>EOR</td><td>FS</td><td>LS</td><td>LGSEN=0</td><td>RSVD</td><td>RSVD</td><td>RSVD</td><td>RSVD</td><td>RSVD</td><td>RSVD</td><td>RSVD</td><td>RSVD</td><td>IPCS</td><td>UDPCS</td><td>TCPCS</td><td colspan="4">Frame_Length</td><td>Offset 0</td></tr>
<tr><td colspan="14" rowspan="2">RSVD</td><td rowspan="2">TAGC</td><td rowspan="2">RSVD</td><td colspan="4">VLAN_TAG</td><td rowspan="2">Offset 4</td></tr>
<tr><td>VIDL</td><td>PRIO</td><td>CFI</td><td>VIDH</td></tr>
<tr><td colspan="20">TX_BUFFER_ADDRESS_LOW</td><td>Offset 8</td></tr>
<tr><td colspan="20">TX_BUFFER_ADDRESS_HIGH</td><td>Offset 12</td></tr>
</table>

| Offset# | Bit# | Symbol | Description |
|---|---|---|---|
| 0 | 31 | OWN | **Ownership:** This bit, when set, indicates that the descriptor is owned by the NIC, and that the data relative to this descriptor is ready to be transmitted. When cleared, it indicates that the descriptor is owned by the host system. The NIC clears this bit when the relative buffer data is transmitted. In this case, OWN=1. |
| 0 | 30 | EOR | **End of descriptor Ring:** This bit, when set, indicates that this is the last descriptor in the descriptor ring. When the NIC's internal transmit pointer reaches here, the pointer will return to the first descriptor of the descriptor ring after transmitting the data relative to this descriptor. |
| 0 | 29 | FS | **First segment descriptor:** This bit, when set, indicates that this is the first descriptor of a Tx packet, and that this descriptor is pointing to the first |

| | | | |
|---|---|---|---|
| | | | segment of the packet. |
| 0 | 28 | LS | **Last segment descriptor:** This bit, when set, indicates that this is the last descriptor of a Tx packet, and that this descriptor is pointing to the last segment of the packet. |
| 0 | 27 | LGSEN | **Large Send:** A command bit; TCP/IP Large send operation enable. Driver sets this bit to ask NIC to offload Large send operation. In this case, LGSEN=0. |
| 0 | 26-19 | RSVD | **Reserved** |
| 0 | 18 | IPCS | **IP checksum offload:** A command bit. The driver sets this bit to ask the NIC to offload the IP checksum. |
| 0 | 17 | UDPCS | **UDP checksum offload:** A command bit. The driver sets this bit to ask the NIC to offload the UDP checksum. |
| 0 | 16 | TCPCS | **TCP checksum offload enable:** A command bit; The driver sets this bit to ask the NIC to offload the TCP checksum. |
| 0 | 15-0 | Frame_Length | **Transmit frame length:** This field indicates the length of the TX buffer, in bytes, to be transmitted |
| 4 | 31-18 | RSVD | **Reserved** |
| 4 | 17 | TAGC | **VLAN tag control bit:** 1: Enable. 0: Disable.<br>1: Add TAG. 0x8100 (Ethernet encoded tag protocol ID, indicating that this is an IEEE 802.1Q VLAN packet) is inserted after the source address, and 2 bytes are inserted after tag protocol ID from the VLAN_TAG field in transmit descriptor.<br>0: Packet remains unchanged when transmitting. I.e., the packet transmitted is the same as it was passed down by upper layer. |
| 4 | 16 | RSVD | **Reserved** |
| 4 | 15-0 | VLAN_TAG | **VLAN Tag:** The 2-byte VLAN_TAG contains information, from upper layer, of user priority, canonical format indicator, and VLAN ID. Please refer to IEEE 802.1Q for more VLAN tag information.<br>VIDH: The high 4 bits of a 12-bit VLAN ID.<br>VIDL: The low 8 bits of a 12-bit VLAN ID.<br>PRIO: 3-bit 8-level priority.<br>CFI: Canonical Format Indicator. |
| 8 | 31-0 | TxBuffL | **Low 32-bit address of transmit buffer** |
| 12 | 31-0 | TxBuffH | **High 32-bit address of transmit buffer** |

**Tx Status Descriptor (after transmitting, OWN=0, Tx status mode)**

After having transmitted, the Tx descriptor turns into a Tx status descriptor.

**Table 24. Tx Status Descriptor**

bit 31 30 29 28 27 26 16 15 8 7 6 5 4 3 2 1 0

<table>
<tr><td>OWN=0</td><td>EOR</td><td>FS</td><td>LS</td><td>RSVD</td><td>RSVD</td><td>RSVD</td><td>RSVD</td><td>RSVD</td><td>RSVD</td><td>RSVD</td><td>RSVD</td><td colspan="3">RSVD</td><td colspan="4">RSVD</td><td>Offset 0</td></tr>
<tr><td colspan="13" rowspan="2">RSVD</td><td rowspan="2">TAGC</td><td rowspan="2">RSVD</td><td colspan="4">VLAN_TAG</td><td rowspan="2">Offset 4</td></tr>
<tr><td>VIDL</td><td>PRIO</td><td>CFI</td><td>VIDH</td></tr>
<tr><td colspan="19">TX_BUFFER_ADDRESS_LOW</td><td>Offset 8</td></tr>
<tr><td colspan="19">TX_BUFFER_ADDRESS_HIGH</td><td>Offset 12</td></tr>
</table>

| Offset# | Bit# | Symbol | Description |
|---|---|---|---|
| 0 | 31 | OWN | **Ownership:** This bit, when set, indicates that the descriptor is owned by the NIC. When cleared, it indicates that the descriptor is owned by the host system. NIC clears this bit when the relative buffer data is already transmitted. In this case, OWN=0. |
| 0 | 30 | EOR | **End of Descriptor Ring:** When set, indicates that this is the last descriptor in descriptor ring. When NIC's internal transmit pointer reaches here, the pointer will return to the first descriptor of the descriptor ring after transmitting the data relative to this descriptor. |
| 0 | 29 | FS | **First Segment Descriptor:** This bit, when set, indicates that this is the first descriptor of a Tx packet, and that this descriptor is pointing to the first segment of the packet. |
| 0 | 28 | LS | **Last Segment Descriptor:** This bit, when set, indicates that this is the last descriptor of a Tx packet, and that this descriptor is pointing to the last |

| | | | |
|---|---|---|---|
| | | | segment of the packet. |
| 0 | 27-0 | RSVD | **Reserved** |
| 4 | 31-18 | RSVD | **Reserved** |
| 4 | 17 | TAGC | **VLAN Tag Control Bit:** 1: Enable. 0: Disable.<br>1: Add TAG. 0x8100 (Ethernet encoded tag protocol ID, indicating that this is an IEEE 802.1Q VLAN packet) is inserted after source address, and 2 bytes are inserted after tag protocol ID from VLAN_TAG field in transmit descriptor.<br>0: Packet remains unchanged when transmitting. I.e., the packet transmitted is the same as it was passed down by the upper layer. |
| 4 | 16 | RSVD | **Reserved** |
| 4 | 15-0 | VLAN_TAG | **VLAN Tag:** The 2-byte VLAN_TAG contains information, from the upper layer, of user priority, canonical format indicator, and VLAN ID. Please refer to IEEE 802.1Q for more VLAN tag information.<br>VIDH: The high 4 bits of a 12-bit VLAN ID.<br>VIDL: The low 8 bits of a 12-bit VLAN ID.<br>PRIO: 3-bit 8-level priority.<br>CFI: Canonical Format Indicator. |
| 8 | 31-0 | TxBuffL | **Low 32-bit address of transmit buffer** |
| 12 | 31-0 | TxBuffH | **High 32-bit address of transmit buffer** |

### 10.1.2. Receive

The receive portion implements the receive portion of 802.3 Media Access Control. The Rx MAC retrieves packet data from the receive portion and sends it to the Rx Buffer Manager. Additionally, the Rx MAC provides MIB control information and packet address data for the Rx Filter.

The Rx MAC can detect packets containing a 4-byte VLAN tag, and remove the VLAN tag from the received packet. If Rx VLAN Tag Removal is enabled, then the 4 bytes following the source and destination addresses will be stripped out. The VLAN status can be returned in the VLAN Tag field.

The Rx MAC supports IP checksum verification. It can validate IP checksums as well as TCP and UDP checksums. Packets can be discarded based on detecting checksum errors.

The following information describes what the Rx descriptor may look like, depending on different states in each Rx descriptor. Any Rx buffer pointed to by one of the Rx descriptors should be at least 8 bytes in length, and should be 8-byte alignment in memory. The length of each Rx buffer should be a multiple of 8 bytes.

**Rx Command Descriptor (OWN=1)**

The driver should pre-allocate Rx buffers and configure Rx descriptors before packet reception. The following describes what Rx descriptors may look like before packet reception.

**Table 25. Rx Command Descriptor**

<table>
<tr><td>bit</td><td colspan="2">31 30 29 28</td><td colspan="3">19 18 17 16 15 14 13 12</td><td colspan="3">8 7 6 5 4 3 2 1 0</td><td></td></tr>
<tr><td></td><td>OWN=1</td><td>EOR</td><td colspan="2">RSVD</td><td colspan="4">Buffer_Size</td><td>Offset 0</td></tr>
<tr><td rowspan="2"></td><td colspan="3" rowspan="2">RSVD</td><td rowspan="2">TAVA</td><td colspan="4">VLAN_TAG</td><td rowspan="2">Offset 4</td></tr>
<tr><td>VIDL</td><td>PRIO</td><td>CFI</td><td>VIDH</td></tr>
<tr><td></td><td colspan="8">RX_BUFFER_ADDRESS_LOW</td><td>Offset 8</td></tr>
<tr><td></td><td colspan="8">RX_BUFFER_ADDRESS_HIGH</td><td>Offset 12</td></tr>
</table>

| Offset# | Bit# | Symbol | Description |
|---|---|---|---|
| 0 | 31 | OWN | **Ownership:** This bit, when set, indicates that the descriptor is owned by the NIC, and is ready to receive a packet. The OWN bit is set by the driver after having pre-allocated the buffer at initialization, or the host has released the buffer to the driver. In this case, OWN=1. |
| 0 | 30 | EOR | **End of Rx descriptor Ring:** This bit, set to 1 indicates that this descriptor is the last descriptor of the Rx descriptor ring. Once the NIC's internal receive descriptor pointer reaches here, it will return to the first descriptor of the Rx descriptor ring after this descriptor is used by packet reception. |
| 0 | 29-14 | RSVD | **Reserved** |
| 0 | 13-0 | Buffer_Size | **Buffer Size:** This field indicate the receive buffer size in bytes. The Rx buffer size should not exceed $2^{13}$-1(8KB-1) and should be a multiple of 8. I.e., the maximum value of this field is 0x1FF8, and bit2-0 and bit13 should be always 0. |

| | | | |
|---|---|---|---|
| 4 | 31-17 | RSVD | **Reserved** |
| 4 | 16 | TAVA | **Tag Available:** This bit, when set, indicates that the received packet is an IEEE802.1Q VLAN TAG (0x8100) available packet. |
| 4 | 15-0 | VLAN_TAG | **VLAN Tag:** If the TAG of the packet is 0x8100, The RTL8169S/RTL8110S extracts four bytes from after source ID, sets the TAVA bit to 1, and moves the TAG value of this field in Rx descriptor.<br>VIDH: The high 4 bits of a 12-bit VLAN ID.<br>VIDL: The low 8 bits of a 12-bit VLAN ID.<br>PRIO: 3-bit 8-level priority.<br>CFI: Canonical Format Indicator. |
| 8 | 31-0 | RxBuffL | **Low 32-bit Address of Receive Buffer.** 8-byte alignment is required, i.e., the lowest 3 LSB bits should be 0. |
| 12 | 31-0 | RxBuffH | **High 32-bit Address of Receive Buffer** |

**Rx Status Descriptor (OWN=0)**

When packet is received, the Rx command descriptor turns to be a Rx status descriptor.

**Table 26. Rx Status Descriptor**

<table>
<tr><td>bit</td><td colspan="6">31 30 29 28 27 26</td><td colspan="12">16 15 14 13 12</td><td colspan="4">8 7 6 5 4 3 2 1 0</td><td></td></tr>
<tr><td></td><td>OWN=0</td><td>EOR</td><td>FS</td><td>LS</td><td>MAR</td><td>PAM</td><td>BAR</td><td>RSVD</td><td>RSVD</td><td>RWT</td><td>RES</td><td>RUNT</td><td>CRC</td><td>PID1</td><td>PID0</td><td>IPF</td><td>UDPF</td><td>TCPF</td><td colspan="4">Frame_Length</td><td>Offset 0</td></tr>
<tr><td></td><td colspan="15" rowspan="2">RSVD</td><td rowspan="2">TAVA</td><td colspan="6">VLAN_TAG</td><td rowspan="2">Offset 4</td></tr>
<tr><td colspan="3">VIDL</td><td>PRIO</td><td>CFI</td><td>VIDH</td></tr>
<tr><td></td><td colspan="22">RX_BUFFER_ADDRESS_LOW</td><td>Offset 8</td></tr>
<tr><td></td><td colspan="22">RX_BUFFER_ADDRESS_HIGH</td><td>Offset 12</td></tr>
</table>

| Offset# | Bit# | Symbol | Description |
|---|---|---|---|
| 0 | 31 | OWN | **Ownership:** This bit, when set, indicates that the descriptor is owned by the NIC. When cleared, it indicates that the descriptor is owned by the host system. The NIC clears this bit when the NIC has filled up this Rx buffer with a packet or part of a packet. In this case, OWN=0. |
| 0 | 30 | EOR | **End of Rx Descriptor Ring:** This bit, set to 1, indicates that this descriptor is the last descriptor of the Rx descriptor ring. Once the NIC's internal receive descriptor pointer reaches here, it will return to the first descriptor of the Rx descriptor ring after this descriptor is used by packet reception. |
| 0 | 29 | FS | **First Segment descriptor:** This bit, when set, indicates that this is the first descriptor of a received packet, and this descriptor is pointing to the first segment of the packet. |
| 0 | 28 | LS | **Last Segment Descriptor:** This bit, when set, indicates that this is the last descriptor of a received packet, and this descriptor is pointing to the last segment of the packet. |
| 0 | 27 | MAR | **Multicast Address Packet Received:** This bit, when set, indicates that a multicast packet has been received. |
| 0 | 26 | PAM | **Physical Address Matched:** This bit, when set, indicates that the destination address of this Rx packet matches the value in the RTL8169S/RTL8110S's ID registers. |
| 0 | 25 | BAR | **Broadcast Address Received:** This bit, when set, indicates that a broadcast packet has been received. BAR and MAR will not be set simultaneously. |
| 0 | 24 | RSVD | **Reserved, always a 0.** |
| 0 | 23 | RSVD | **Reserved, always a 1.** |
| 0 | 22 | RWT | **Receive Watchdog Timer Expired:** This bit is set whenever the received packet length exceeds 8192 bytes. |
| 0 | 21 | RES | **Receive Error Summary:** This bit, when set, indicates that at least one of the following errors has occurred: CRC, RUNT, RWT, FAE. This bit is valid only when LS (Last segment bit) is set |
| 0 | 20 | RUNT | **Runt Packet:** This bit, when set, indicates that the received packet length is smaller than 64 bytes. RUNT packets are able to be received only when RCR_AR is set. |
| 0 | 19 | CRC | **CRC Error:** This bit, when set, indicates that a CRC error has occurred on the received packet. A CRC packet is able to be received only when |

<table>
<tr><td></td><td></td><td></td><td>RCR_AER is set.</td></tr>
<tr><td>0</td><td>18, 17</td><td>PID1, PID0</td><td>Protocol ID1, Protocol ID0: These 2 bits indicate the protocol type of the packet received.
<table>
<tr><th></th><th>PID1</th><th>PID0</th></tr>
<tr><td>Non-IP</td><td>0</td><td>0</td></tr>
<tr><td>TCP/IP</td><td>0</td><td>1</td></tr>
<tr><td>UDP/IP</td><td>1</td><td>0</td></tr>
<tr><td>IP</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>0</td><td>16</td><td>IPF</td><td>IP Checksum Failure: 1: Failure, 0: No failure.</td></tr>
<tr><td>0</td><td>15</td><td>UDPF</td><td>UDP Checksum Failure: 1: Failure, 0: No failure.</td></tr>
<tr><td>0</td><td>14</td><td>TCPF</td><td>TCP Checksum Failure: 1: Failure, 0: No failure.</td></tr>
<tr><td>0</td><td>13-0</td><td>Frame_Length</td><td>When OWN=0 and LS =1, these bits indicate the received packet length including CRC, in bytes.</td></tr>
<tr><td>4</td><td>31-17</td><td>RSVD</td><td>Reserved</td></tr>
<tr><td>4</td><td>16</td><td>TAVA</td><td>Tag Available: When set, the received packet is an IEEE802.1Q VLAN TAG (0x8100) available packet.</td></tr>
<tr><td>4</td><td>15-0</td><td>VLAN_TAG</td><td>VLAN Tag: If the TAG of the packet is 0x8100, The RTL8169S/RTL8110S extracts four bytes from the after source ID, sets TAVA bit to 1, and moves the TAG value to this field in the Rx descriptor.<br>VIDH: The high 4 bits of a 12-bit VLAN ID.<br>VIDL: The low 8 bits of a 12-bit VLAN ID.<br>PRIO: 3-bit 8-level priority.<br>CFI: Canonical Format Indicator.</td></tr>
<tr><td>8</td><td>31-0</td><td>RxBuffL</td><td>Low 32-bit Address of Receive Buffer. 8-byte alignment is required.</td></tr>
<tr><td>12</td><td>31-0</td><td>RxBuffH</td><td>High 32-bit Address of Receive Buffer</td></tr>
</table>

## *10.2. Flow Control*

The RTL8169S/RTL8110S supports IEEE802.3X flow control, based on the result of N-Way, to improve performance in full-duplex mode. It detects and sends PAUSE packets to achieve the flow control task. Results from the N-Way process with the link partner determine if flow control is supported for the current connection.

### 10.2.1. Control Frame Transmission

When the RTL8169S/RTL8110S is running out of receive descriptors in full duplex mode, it sends a PAUSE packet (with pause_time=FFFFh) to inform the source station to stop transmission for the specified period of time. Once the receive descriptors are available again, the RTL8169S/RTL8110S sends another PAUSE packet (with pause_time=0000h) to wake up the source station to restart transmission.

### 10.2.2. Control Frame Reception

The RTL8169S/RTL8110S enters backoff state for the specified period of time when it receives a valid PAUSE packet (with pause_time=n) in full duplex mode. If the PAUSE packet is received while the RTL8169S/RTL8110S is transmitting, the RTL8169S/RTL8110S starts to backoff after the current transmission is completed. The RTL8169S/RTL8110S is free to transmit packets when it receives a valid PAUSE packet (with pause_time=0000h) or the backoff timer(=n*512 bit time) elapses.

The PAUSE operation cannot be used to inhibit transmission of MAC Control frames (e.g. a PAUSE packet). The N-way flow control capability can be disabled. Please refer to Section 7, EEPROM (93C46 or 93C56) Contents for further information.

## *10.3. Memory Functions*

### 10.3.1. Memory Read Line (MRL)

The Memory Read Line command reads more than a longword (DWORD) up to the cache line boundary in a prefetchable address space. The Memory Read Line command is semantically identical to the Memory Read command except that it additionally indicates that the master intends to fetch a complete cache line. This command is intended to be used with bulk sequential data transfers where the memory system and the requesting master might gain some performance advantages by reading up to a cache line boundary in response to the request rather than a single memory cycle. As with the Memory Read command, pre-fetched buffers must be invalidated before any synchronization events are passed through this access path.

The RTL8169S/RTL8110S performs MRL according to the following rules:

i. Read accesses that reach the cache line boundary use the Memory Read Line command (MRL) instead of the Memory Read command.
ii. Read accesses that do not reach the cache line boundary use the Memory Read (MR) command.
iii. The Memory Read Line (MRL) command operates in conjunction with the Memory Read Multiple command (MRM).
iv. The RTL8169S/RTL8110S will terminate the read transaction on the cache line boundary when it is out of resources on the transmit DMA. For example, when the transmit FIFO is almost full.

### 10.3.2. Memory Read Multiple (MRM)

The Memory Read Multiple command is semantically identical to the Memory Read command except that it additionally indicates that the master may intend to fetch more than one cache line before disconnecting. The memory controller should continue pipelining memory requests as long as FRAMEB is asserted. This command is intended to be used with bulk sequential data transfers where the memory system and the requesting master might gain some performance advantage by sequentially reading ahead one or more additional cache line(s) when a software transparent buffer is available for temporary storage.

The RTL8169S/RTL8110S performs MRM according to the following rules,

i. When the RTL8169S/RTL8110S reads full cache lines, it will use the Memory Read Multiple command.

ii. If the memory buffer is not cache-aligned, the RTL8169S/RTL8110S will use the Memory Read Line command to reach the cache line boundary first.

**Example:**

Assume the packet length = 1514 byte, cache line size = 16 longwords (DWORDs), and Tx buffer start address = 64m+4 (m > 0).

;Step1: Memory Read Line (MRL)
;Data: (0-3) => (4-7) => (8-11) =>……….. => (56-59) (byte offset of the Tx packet)
;From Address: <64m+4>, <64m+8>, ………, <64m+60> (reach cache line boundary)
;Step2. Memory Read Multiple (MRM)
;Data: (60-63) => (64-67) => (68-71) => ……………………….….. => (1454-1467)
;From Address: <64m+64>, <64m+68>, …………………., <64m+64+(16*4)*21+(16-1)*4>
;Step3. Memory Read(MR)
;Data: (1468-1471) => (1472-1475) => ……………………………, => (1510-1513)
;From Address:<64m+64+(16*4)*22>,<64m+64+(16*4)*22+4>,..,<64m+64+(16*4)*22+42>
Step1: Memory Read Multiple (MRM)
Data: (0-3) => (4-7) => (8-11) =>………….. => (1454-1467)
From Address: <64m+4>, <64m+8>, ………, <64m+64+(16*4)*21+(16-1)*4>
Step2. Memory Read(MRL)
Data: (1468-1471) => (1472-1475) => ……………………………, => (1510-1513)
From Address:<64m+64+(16*4)*22>,<64m+64+(16*4)*22+4>,..,<64m+64+(16*4)*22+42>

### 10.3.3. Memory Write and Invalidate (MWI)

The Memory Write and Invalidate command is semantically identical to the Memory Write command except that it additionally guarantees a minimum transfer of one complete cache line; i.e., the master intends to write all bytes within the addressed cache line in a single PCI transaction unless interrupted by the target. Note: All byte enables must be asserted during each data phase for this command. The master may allow the transaction to cross a cache line boundary only if it intends to transfer the entire next line also. This command requires implementation of a configuration register in the master indicating the cache line size and may only be used with Linear Burst Ordering. It allows a memory performance optimization by invalidating a "dirty" line in a write-back cache without requiring the actual write-back cycle, thus shortening access time. The RTL8169S/RTL8110S uses the MWI command while writing full cache lines, and the Memory Write command while writing partial cache lines.

The RTL8169S/RTL8110S issues MWI command, instead of MW command on Rx DMA when the following requirements are met:

i. The Cache Line Size written in offset 0Ch of the PCI configuration space is 8 or 16 longwords (DWORDs).
ii. The accessed address is cache line aligned.
iii. The RTL8169S/RTL8110S has at least 8/16 longwords (DWORDs) of data in its Rx FIFO.
iv. The MWI (bit 4) in the PCI Configuration Command register should be set to 1.

The RTL8169S/RTL8110S uses the Memory Write (MW) command instead of the MWI whenever there any one of the above listed requirements has failed. The RTL8169S/RTL8110S terminates the WMI cycle at the end of the cache line when a WMI cycle has started and at least one of the requirements are no longer held.

**Example:**

Assume Rx packet length = 1514 byte, cache line size = 16 DWORDs (longwords), and Rx buffer start address = 64m+4 (m > 0).

Step1: Memory Write (MW)

Data: (0-3) => (4-7) => (8-11) => ……….... => (56-59) (byte offset of the Rx packet)

To Address: <64m+4>, <64m+8>, …………., <64m+60> (reach cache line boundary)

Step2. Memory Write and Invalidate (MWI)

Data: (60-63) => (64-67) => (68-71) => …………………….…..... => (1454-1457)

To Address: <64m+64>, <64m+68>, ………………..….., <64m+64+(16*4)*21+(16-1)*4>

Step3. Memory Write(MW)

Data: (1458-1461) => (1462-1465) => ……………………..……... => (1512-1513)

To Address: <64m+64+(16*4)*22>, <64m+64+(16*4)*22+4>, , <64m+64+(16*4)*22+42>

## 10.3.4. Dual Address Cycle (DAC)

The Dual Address Cycle (DAC) command is used to transfer a 64-bit address to devices that support 64-bit addressing when the address is not in the low 4 GB address space. The RTL8169S/RTL8110S is capable of performing DAC, such that it is very competent as a network server card in a heavy-duty server with the possibility of allocating a memory buffer above a 4GB memory address space.

# *10.4. LED Functions*

The RTL8169S/RTL8110S supports 4 LED signals in 4 different configurable operation modes. The following sections describe the different LED actions.

## 10.4.1. Link Monitor

The Link Monitor senses the link integrity or if a station is down, such as LINK10, LINK100, LINK1000, LINK10/100/1000, LINK10/ACT, LINK100/ACT, or LINK1000/ACT. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high indicating that no network connection exists.

## 10.4.2. Rx LED

In 10/100/1000Mbps mode, blinking of the Rx LED indicates that receive activity is occurring.

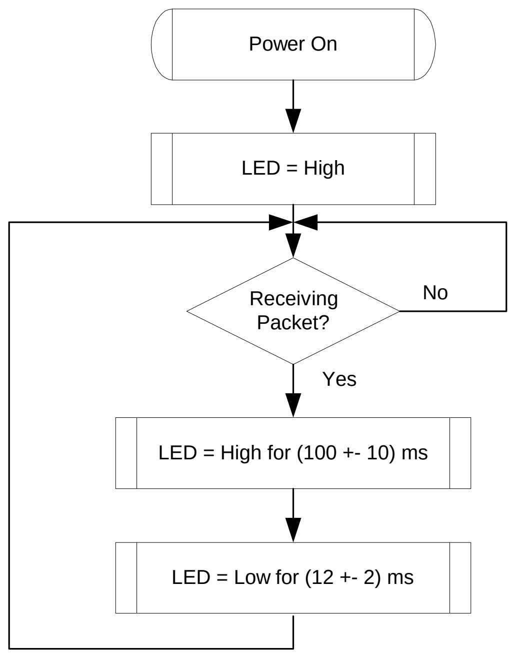



**Figure 9. Rx LED**

### 10.4.3. Tx LED

In 10/100/1000Mbps mode, blinking of the Tx LED indicates that transmit activity is occurring.

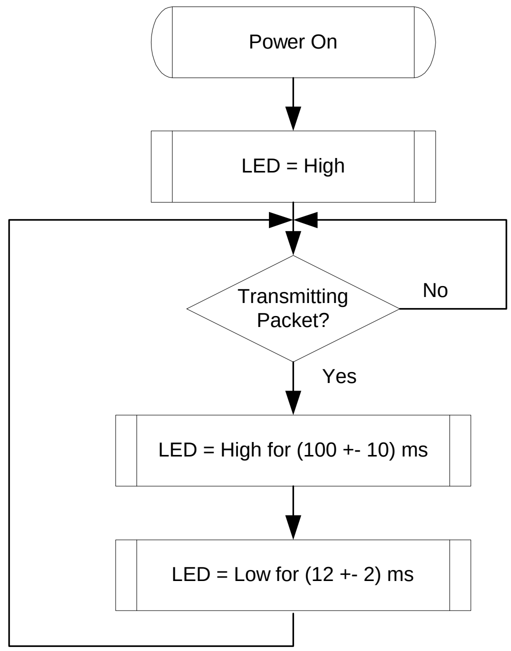



**Figure 10. Tx LED**

### 10.4.4. Tx/Rx LED

In 10/100/1000Mbps mode, blinking of the Tx/Rx LED indicates that both transmit and receive activity is occurring.

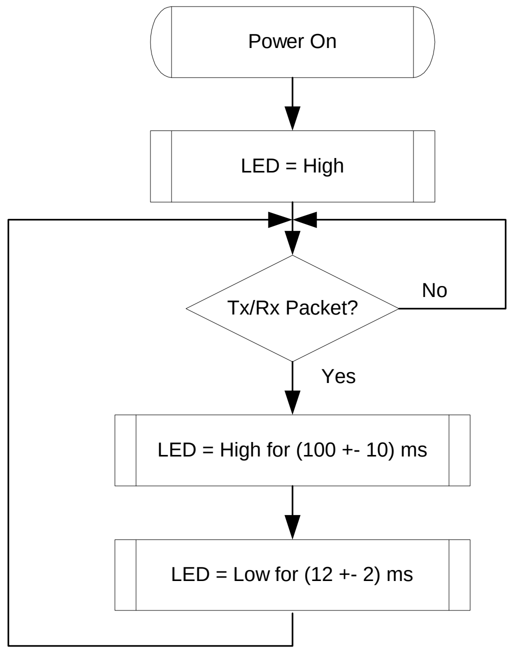



**Figure 11. Tx/Rx LED**

### 10.4.5. LINK/ACT LED

In 10/100/1000Mbps mode, blinking of the LINK/ACT LED indicates that the RTL8169S/RTL8110S is linked and operating properly. This LED high for extended periods, indicates that a link problem exists.

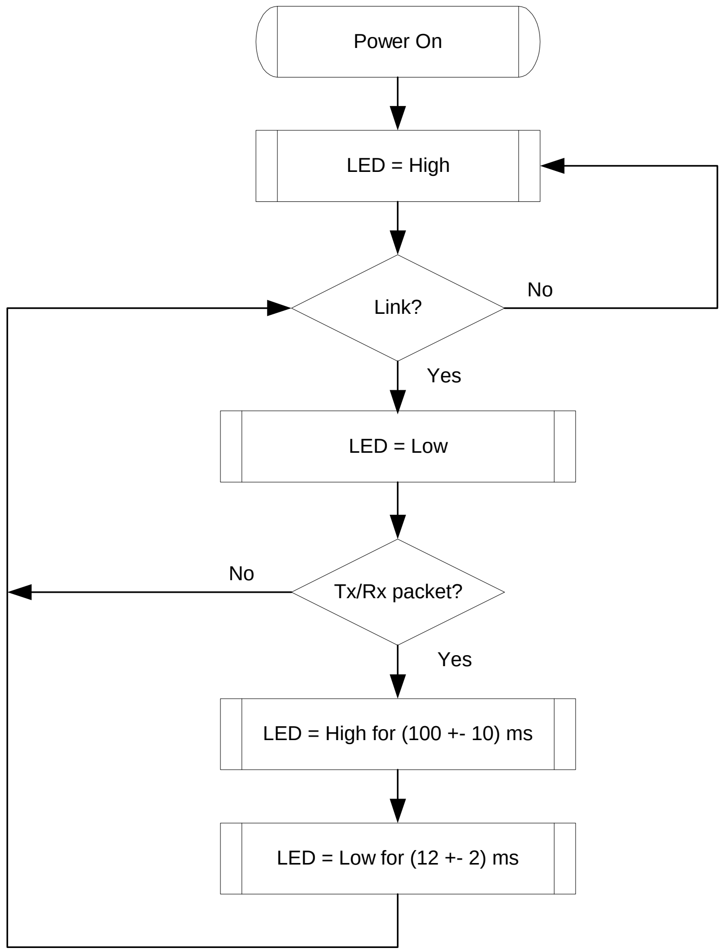



**Figure 12. LINK/ACT LED**

## *10.5. PHY Transceiver*

### 10.5.1. PHY Transmitter

In 10Mbps mode, the Tx MAC retrieves packet data from the Tx Buffer Manager and sends it out through the transmitting physical layer interface. The transmit 4-bit nibbles (TXD[3:0]) clocked at 2.5Mhz (TXC), are serialized into 10Mbps serial data. Then, the 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the DAC converter.

In 100Mbps mode, the transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25Mhz (TXC), are converted into 5B symbol code via 4B/5B coding technology, scrambling, and serializing before being converted to 125Mhz NRZ and NRZI signals. After that, the NRZI signal is passed to the MLT3 encoder, then to the DAC converter for transmission onto the media.

In 1000Mbps mode, the RTL8169S/RTL8110S's PCS layer receives data bytes from the MAC through the GMII interface and performs the generation of continuous code-groups through 4D-PAM5 coding technology. Then, those code groups are passed through waveform shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through DAC converter.

### 10.5.2. PHY Receiver

In MII (10Mbps) mode, the received differential signal is converted into a Manchester-encoded data stream. The stream is processed with a Manchester decoder, and is de-serialized into 4-bit wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz. In 100Mbps mode, the MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and then is presented to the MII interface in 4-bit wide nibbles at a clock speed of 25MHz.

In GMII mode, the input signal from the media first passes through the on-chip sophisticated hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. Afterwards, the received signal is processed with adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. Then, the 8-bit wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the receive MII/GMII interface and sends it to the Rx Buffer Manager.

## *10.6. Next Page*

If 1000Base-T mode is advertised, three additional Next Pages are automatically exchanged between the two link partners. Users can set Reg4.15 to 1 to exchange extra Next Pages via Reg7 and Reg8 as defined in IEEE 802.3ab.

## *10.7. EEPROM Interface*

The RTL8169S/RTL8110S requires the attachment of an external EEPROM. The 93C46 is a 1K-bit EEPROM (the 93C56 is a 2K-bit EEPROM). The EEPROM interface provides the ability for the RTL8169S/RTL8110S to read from and write data to an external serial EEPROM device.

Values in the external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following a power-on or software EEPROM auto load command. The RTL8169S/RTL8110S will auto-load values from the EEPROM. If the EEPROM is not present, the RTL8169S/RTL8110S initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using "bit-bang" accesses via the 9346CR Register, or using PCI VPD. The interface consists of EESK, EECS, EEDO, and EEDI.

**Table 27. EEPROM Interface**

| EEPROM | Description |
|---|---|
| EECS | 93C46 (93C56) chip select |
| EESK | EEPROM serial data clock |
| EEDI/Aux | Input data bus/Input pin to detect if Aux. Power exists or not on initial power-on. This pin should be connected to Boot PROM. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to aux. power via a resistor. If this pin is not pulled high to Aux. Power, the RTL8169S/RTL8110S assumes that no Aux. Power exists. |
| EEDO | Output data bus |

# 11. Characteristics

## 11.1. Absolute Maximum Ratings

**WARNING:** Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

**Table 28. Absolute Maximum Ratings**

| Description/Symbol | Minimum | Maximum | Unit |
|---|---|---|---|
| Supply Voltage (VDD33, AVDDH) | -0.5 | 4 | V |
| Supply Voltage (VDD25) | -0.5 | 3 | V |
| Supply Voltage (VDD18) | -0.5 | 2 | V |
| Input Voltage (DCinput) | -0.5 | VDD33 + 0.5 | V |
| Output Voltage (DCoutput) | -0.5 | VDD33 + 0.5 | V |
| Storage Temperature | -55 | +125 | °C |

## 11.2. Recommended Operating Conditions

**Table 29. Recommended Operating Conditions**

| Description | Pins | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Supply Voltage VDD | VDD33, AVDDH | 3.0 | 3.3 | 3.6 | V |
| | VDD25 | 2.325 | 2.5 | 2.675 | V |
| | VDD18 | 1.674 | 1.8 | 1.926 | V |
| Ambient Temperature $T_A$ | | 0 | | 70 | °C |
| Maximum Junction Temperature | | | | 125 | °C |

## 11.3. Crystal Requirements

**Table 30. Crystal Requirements**

| Symbol | Description/Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $F_{ref}$ | Parallel resonant crystal reference frequency, fundamental mode, AT-cut type. | | 25 | | MHz |
| $F_{ref}$ Stability | Parallel resonant crystal frequency stability, fundamental mode, AT-cut type. $T_a$=25℃. | -50 | | +50 | ppm |
| $F_{ref}$ Tolerance | Parallel resonant crystal frequency tolerance, fundamental mode, AT-cut type. $T_a$=-20℃~+70℃. | -30 | | +30 | ppm |
| $F_{ref}$ Duty Cycle | Reference clock input duty cycle | 40 | | 60 | % |
| $C_L$ | Load Capacitance | | | | pF |

| Symbol | Description/Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| ESR | Equivalent Series Resistance | | | | Ω |
| DL | Drive Level | | | 0.5 | mW |

## 11.4. Thermal Characteristics

**Table 31. Thermal Characteristics**

| Parameter | Minimum | Maximum | Units |
|---|---|---|---|
| Storage temperature | -55 | +125 | °C |
| Operating temperature | 0 | 70 | °C |

## 11.5. DC Characteristics

**Table 32. DC Characteristics**

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| VDD33 | 3.3V Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| VDD18 | 1.8V Supply Voltage | | 1.71 | 1.8 | 1.98 | V |
| VDD25 | 2.5V Supply Voltage | | 2.25 | 2.5 | 2.75 | V |
| $V_{oh}$ | Minimum High Level Output Voltage | $I_{oh}$ = -8mA | 0.9 * Vcc | | Vcc | V |
| $V_{ol}$ | Maximum Low Level Output Voltage | $I_{ol}$ = 8mA | | | 0.1 * Vcc | V |
| $V_{ih}$ | Minimum High Level Input Voltage | | 0.5 * Vcc | | Vcc+0.5 | V |
| $V_{il}$ | Maximum Low Level Input Voltage | | -0.5 | | 0.3 * Vcc | V |
| $I_{in}$ | Input Current | $V_{in}$ = $V_{cc}$ or GND | -1.0 | | 1.0 | uA |
| $I_{oz}$ | Tri-State Output Leakage Current | $V_{out}$ = $V_{cc}$ or GND | -10 | | 10 | uA |
| Icc33 | Average Operating Supply Current from 3.3V | | | | | mA |
| $I_{cc18}$ | Average Operating Supply Current from 1.8V | | | | | mA |

# *11.6. AC Characteristics*

## 11.6.1. Serial EEPROM Interface Timing

93C46(64*16)/93C56(128*16)

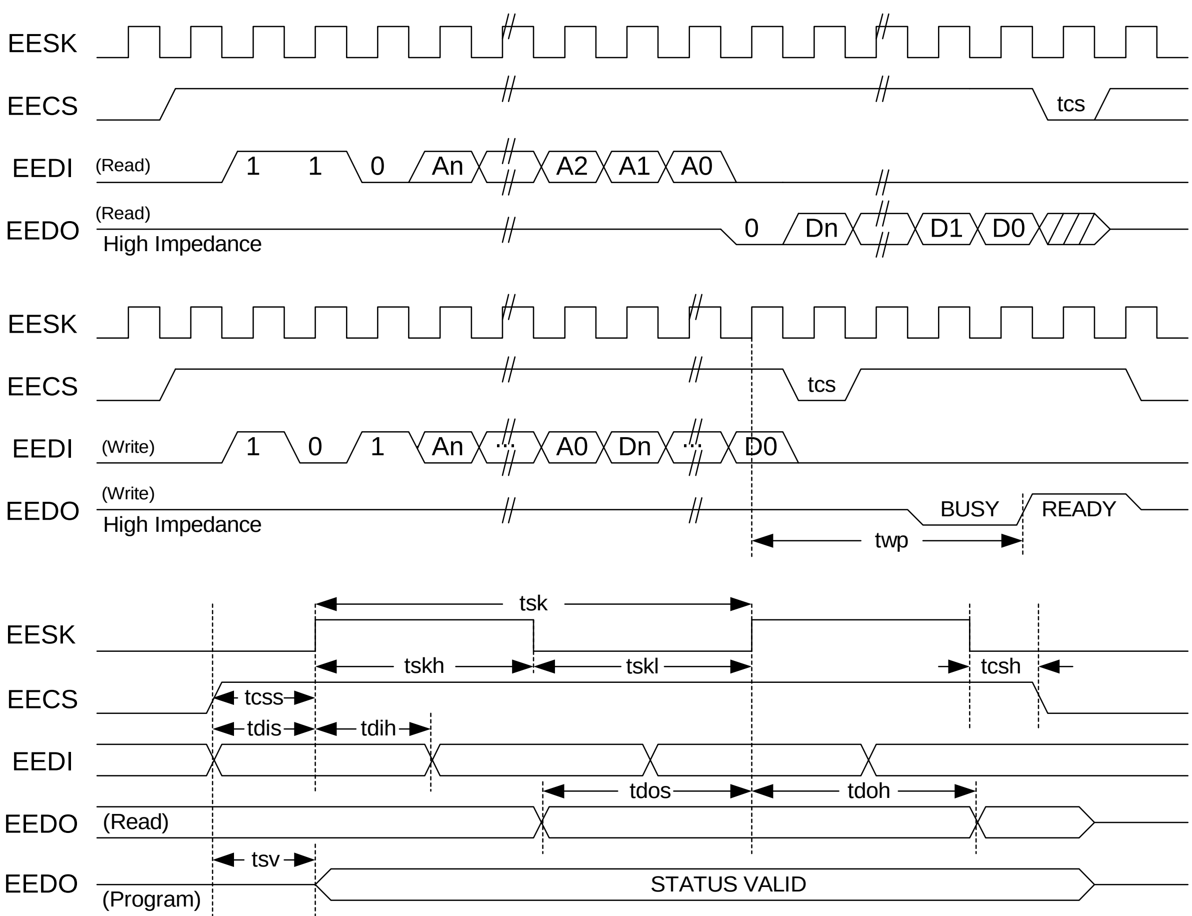



**Figure 13. Serial EEPROM Interface Timing**

**Table 33. EEPROM Access Timing Parameters**

| Symbol | Parameter | EEPROM Type | Min. | Max. | Unit |
|---|---|---|---|---|---|
| tcs | Minimum CS Low Time | 9346/9356 | 1000/250 | | ns |
| twp | Write Cycle Time | 9346/9356 | | 10/10 | ms |
| tsk | SK Clock Cycle Time | 9346/9356 | 4/1 | | us |
| tskh | SK High Time | 9346/9356 | 1000/500 | | ns |
| tskl | SK Low Time | 9346/9356 | 1000/250 | | ns |
| tcss | CS Setup Time | 9346/9356 | 200/50 | | ns |
| tcsh | CS Hold Time | 9346/9356 | 0/0 | | ns |

| Symbol | Parameter | EEPROM Type | Min. | Max. | Unit |
|---|---|---|---|---|---|
| tdis | DI Setup Time | 9346/9356 | 400/50 | | ns |
| tdih | DI Hold Time | 9346/9356 | 400/100 | | ns |
| tdos | DO Setup Time | 9346/9356 | 2000/500 | | ns |
| tdoh | DO Hold Time | 9346/9356 | | 2000/500 | ns |
| tsv | CS to Status Valid | 9346/9356 | | 1000/500 | ns |

# *11.7. PCI Bus Operation Timing*

## 11.7.1. PCI Bus Timing Parameters

**Table 34. PCI Bus Timing Parameters**

| | | 66MHz | | 33MHz | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Min** | **Symbol** | **Parameter** |
| T val | CLK to Signal Valid Delay-bused signals | 2 | 6 | 2 | 11 | ns |
| T val(ptp) | CLK to Signal Valid Delay-point to point | 2 | 6 | 2 | 12 | ns |
| T on | Float to Active Delay | 2 | | 2 | | ns |
| T off | Active to Float Delay | | 14 | | 28 | ns |
| T su | Input Setup Time to CLK-bused signals | 3 | | 7 | | ns |
| T su(ptp) | Input Setup Time to CLK-point to point | 5 | | 10 | | ns |
| T h | Input Hold Time from CLK | 0 | | 0 | | ns |
| T rst | Reset active time after power stable | 1 | | 1 | | ms |
| T rst-clk | Reset active time after CLK STABLE | 100 | | 100 | | us |
| T rst-off | Reset Active to Output Float delay | | 40 | | 40 | ns |
| Trrsu | REQB to REQ64B Setup Time | 10*Tcyc | | 10*Tcyc | | ns |
| Trrh | RSTB to REQ64B Hold Time | 0 | 50 | 0 | 50 | ns |
| T rhfa | RSTB High to First configuration Access | 2^25 | | 2^25 | | clocks |
| T rhff | RSTB High to First FRAMEB assertion | 5 | | 5 | | clocks |

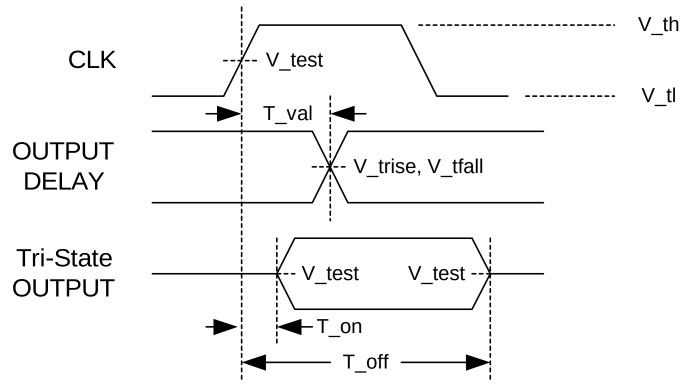



**Figure 14. Output Timing Measurement Conditions**

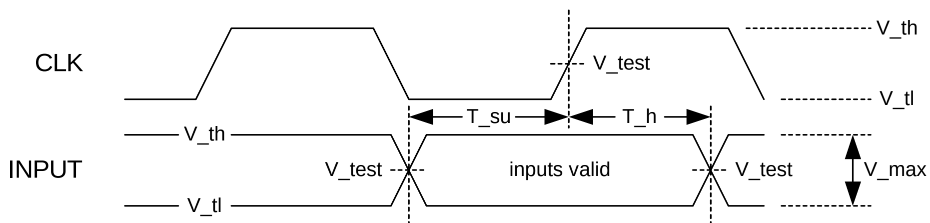



**Figure 15. Input Timing Measurement Conditions**

**Table 35. Measurement Condition Parameters**

| Symbol | Level | Units |
|---|---|---|
| **Vth** | 0.6Vcc | V |
| **Vtf** | 0.2Vcc | V |
| **Vtest** | 0.4Vcc | V |
| **Vtrise** | 0.285Vcc | V |
| **Vtfall** | 0.615Vcc | V |
| **Vmax** | 0.4Vcc | V |
| **Input Signal Edge Rate** | 1 | V/ns |

### 11.7.2. PCI Clock Specification

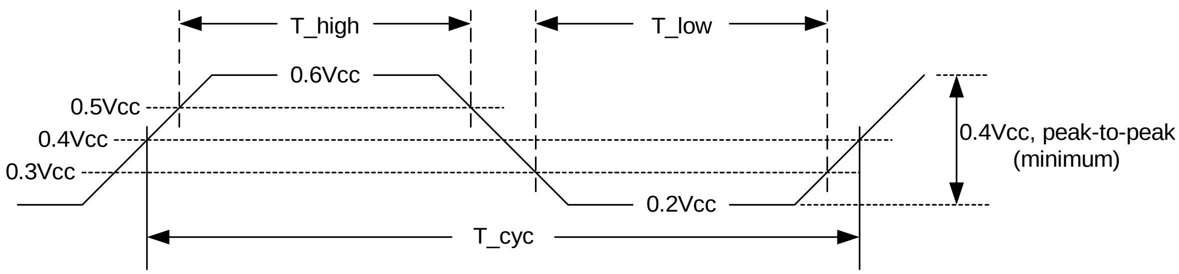



**Figure 16. 3.3V Clock Waveform**

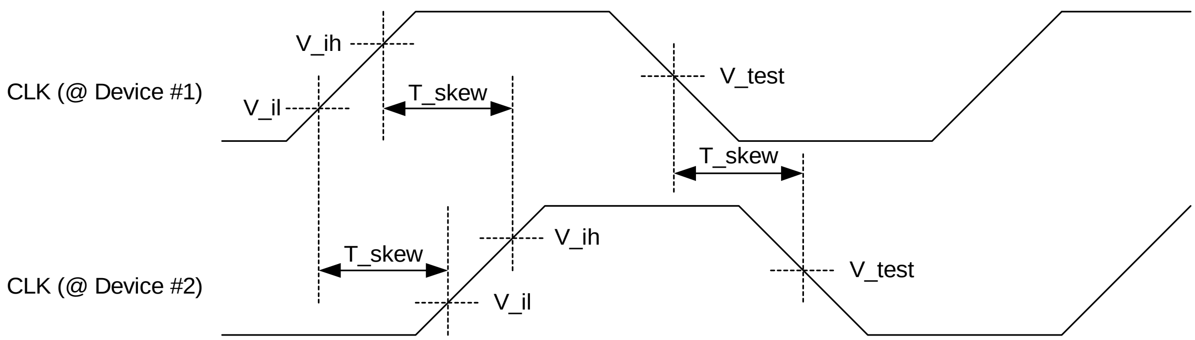



**Figure 17. Clock Skew Diagram**

**Table 36. Clock and Reset Specifications**

| | | 66MHz | | 33MHz | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Min** | **Symbol** | **Parameter** |
| Tcyc | CLK Cycle Time | 15 | 30 | 30 | ∞ | ns |
| Thigh | CLK High Time | 6 | | 11 | | ns |
| Tlow | CLK Low Time | 6 | | 11 | | ns |
| -- | CLK Slew Rate | 1.5 | 4 | 1 | 4 | V/ns |
| -- | RST# Slew Rate | 50 | - | 50 | - | mV/ns |
| Tskew | CLK Skew | | 1 | | 2 | ns |

## 11.7.3. PCI Transactions

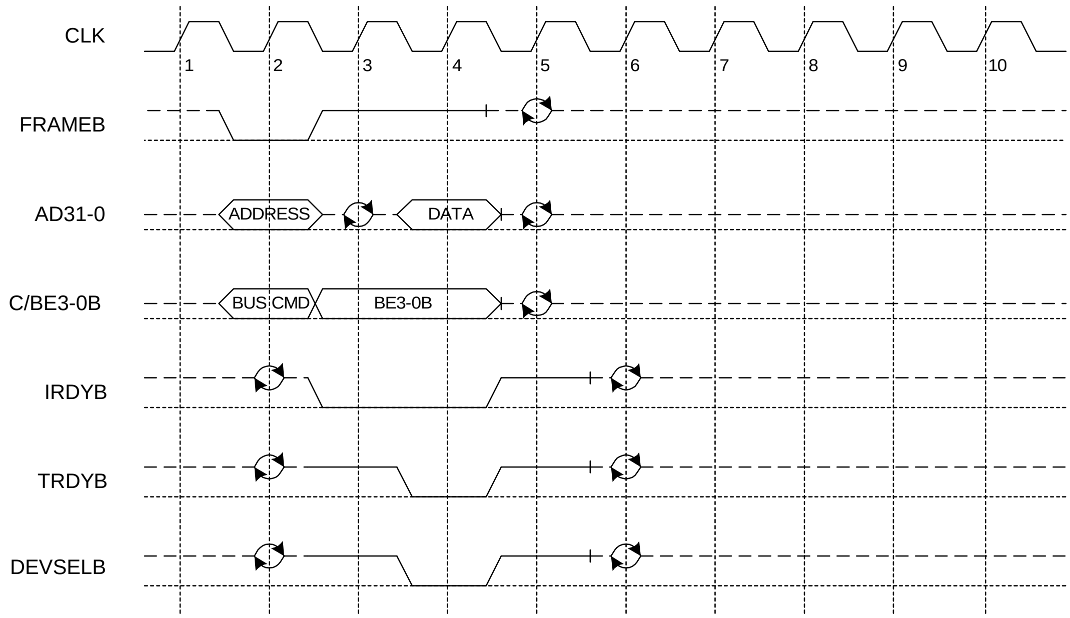



**Figure 18. I/O Read**

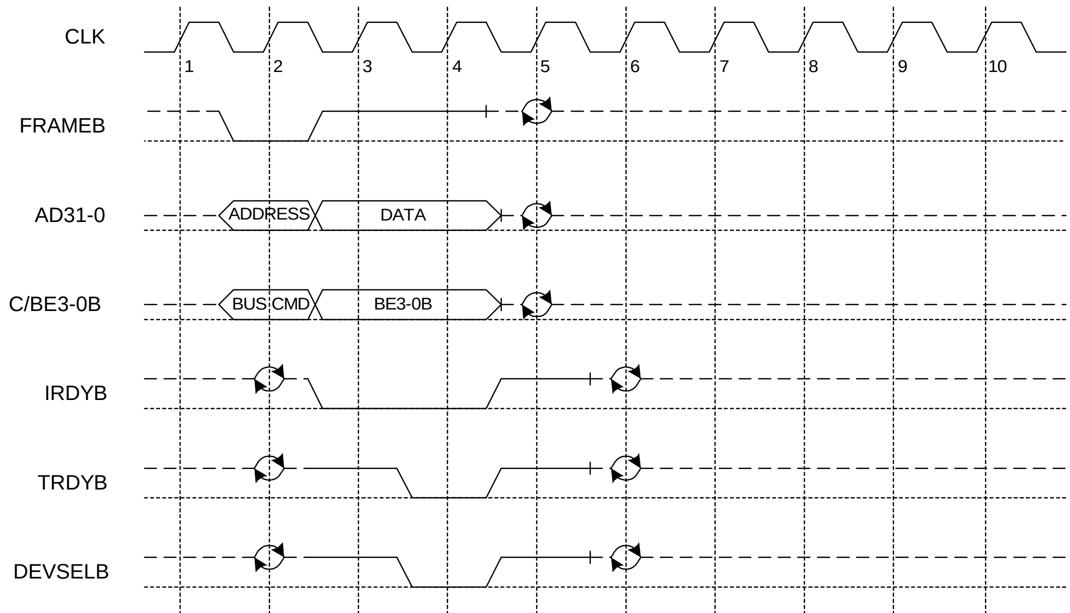



**Figure 19. I/O Write**

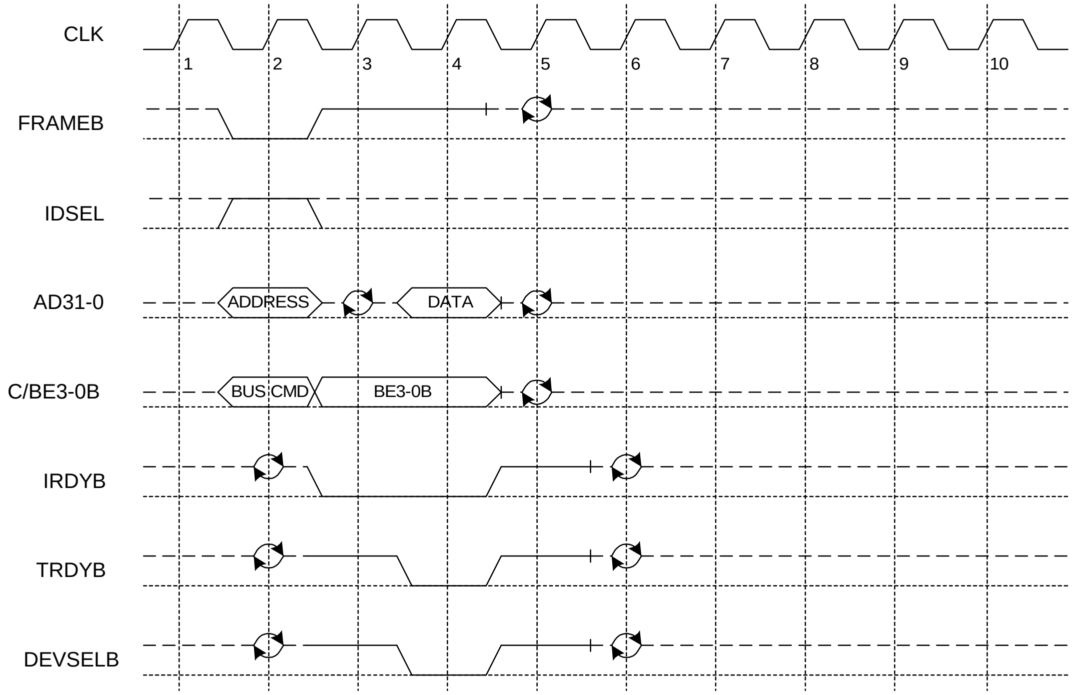



**Figure 20. Configuration Read**

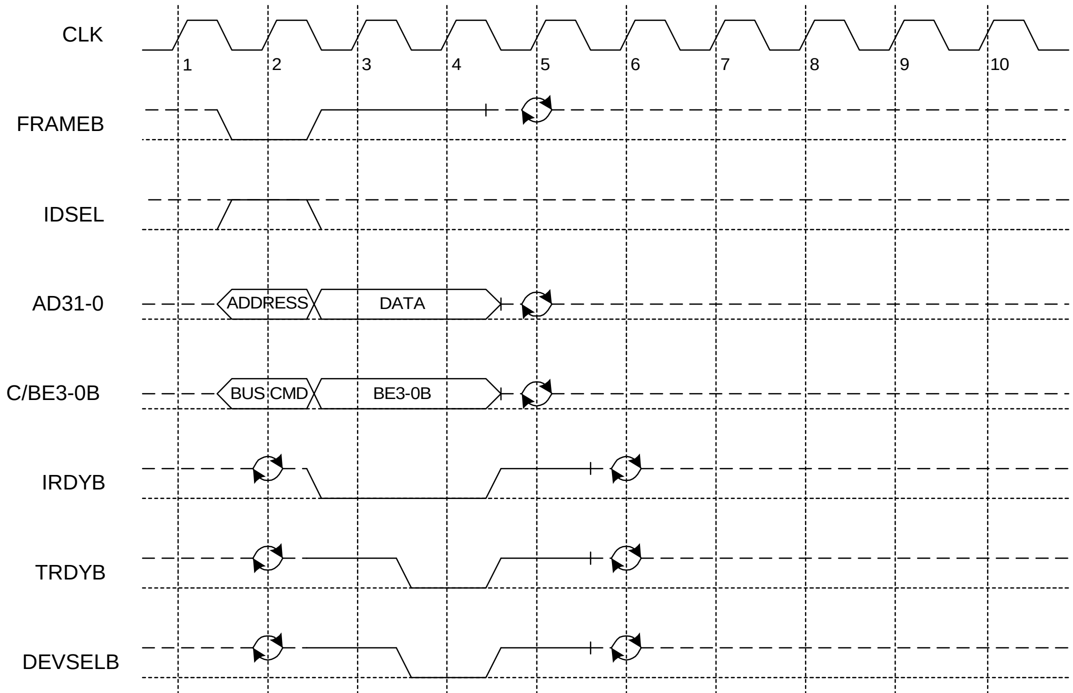



**Figure 21. Configuration Write**

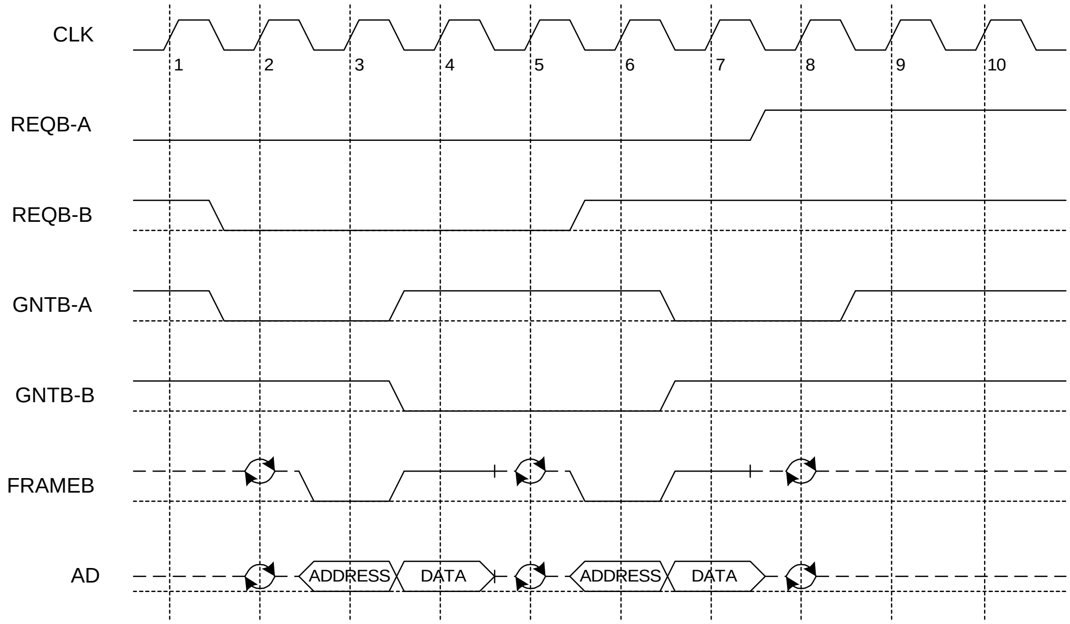



**Figure 22. Bus Arbitration**

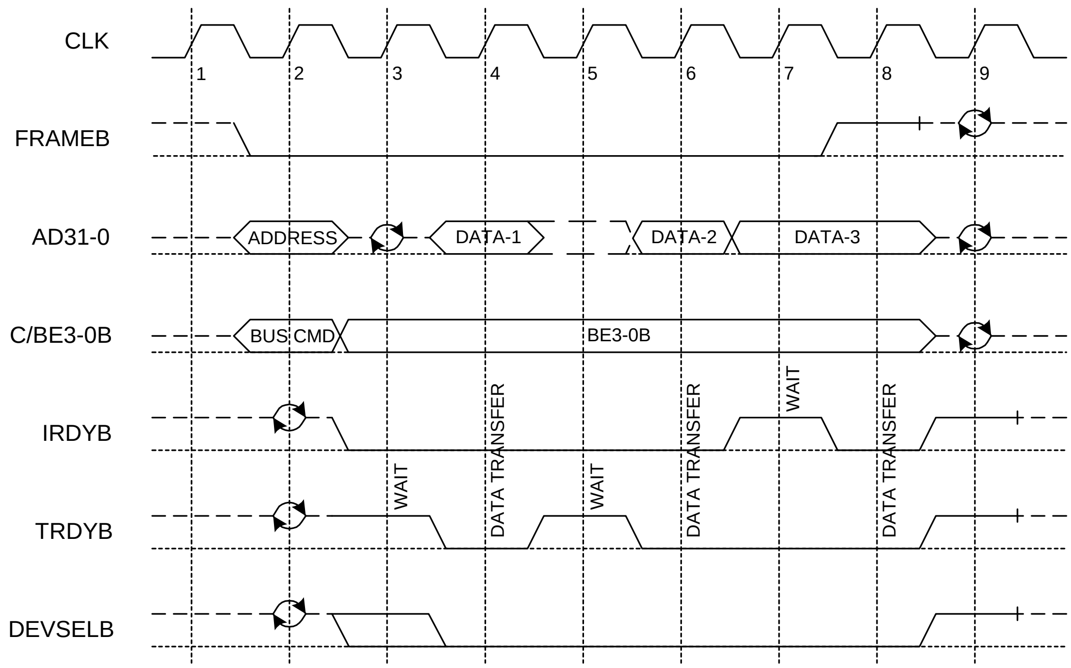



**Figure 23. Memory Read below 4GB (32-bit address, 32-bit data; 32-bit slot)**

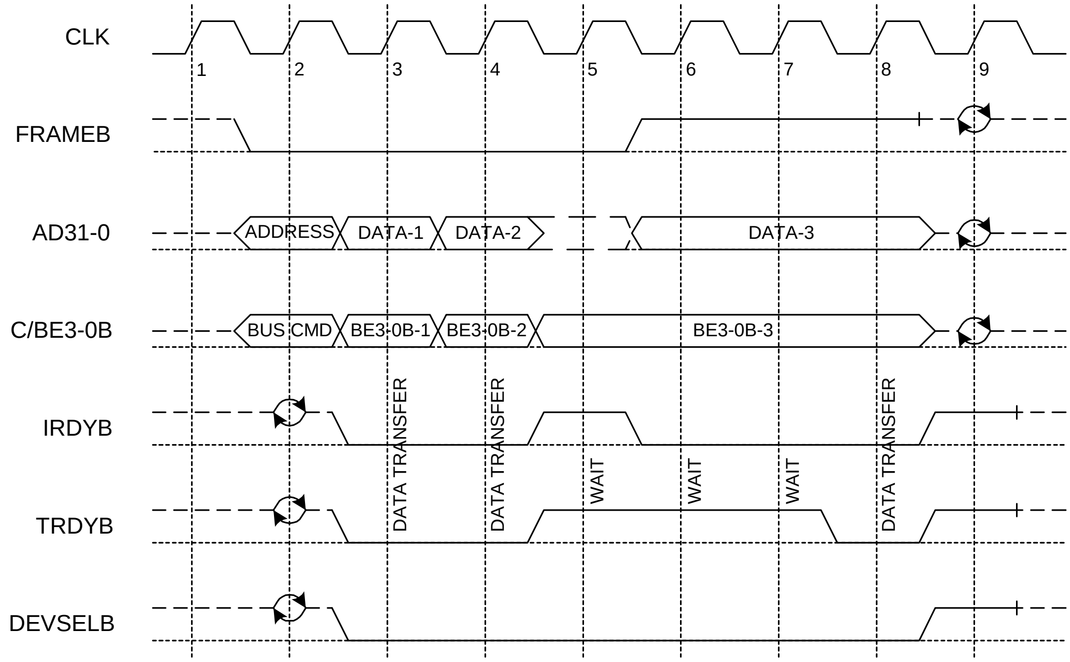



**Figure 24. Memory Write below 4GB (32-bit address, 32-bit data; 32-bit slot)**

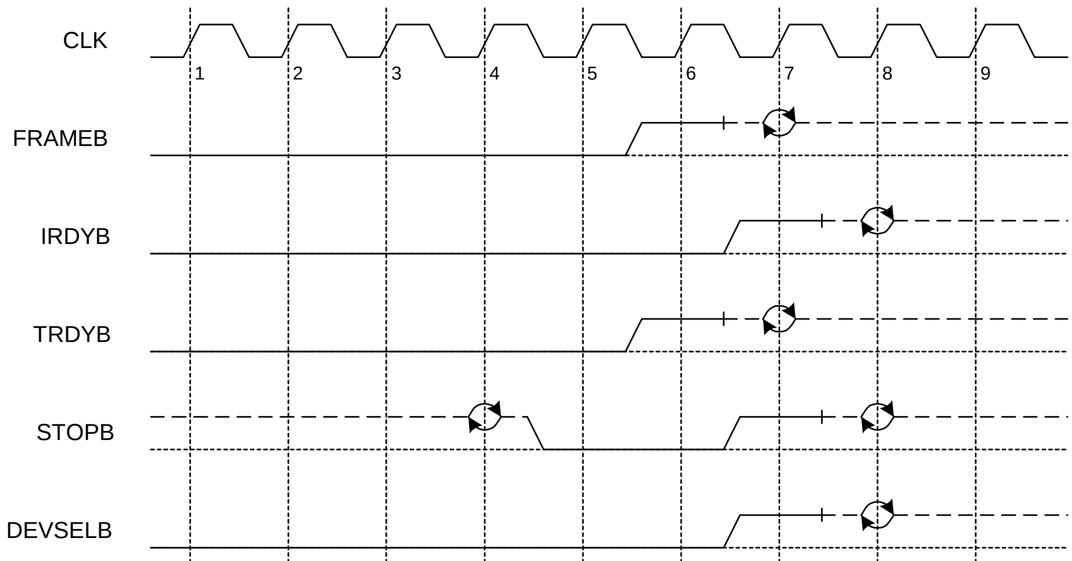



**Figure 25. Target Initiated Termination - Disconnect**

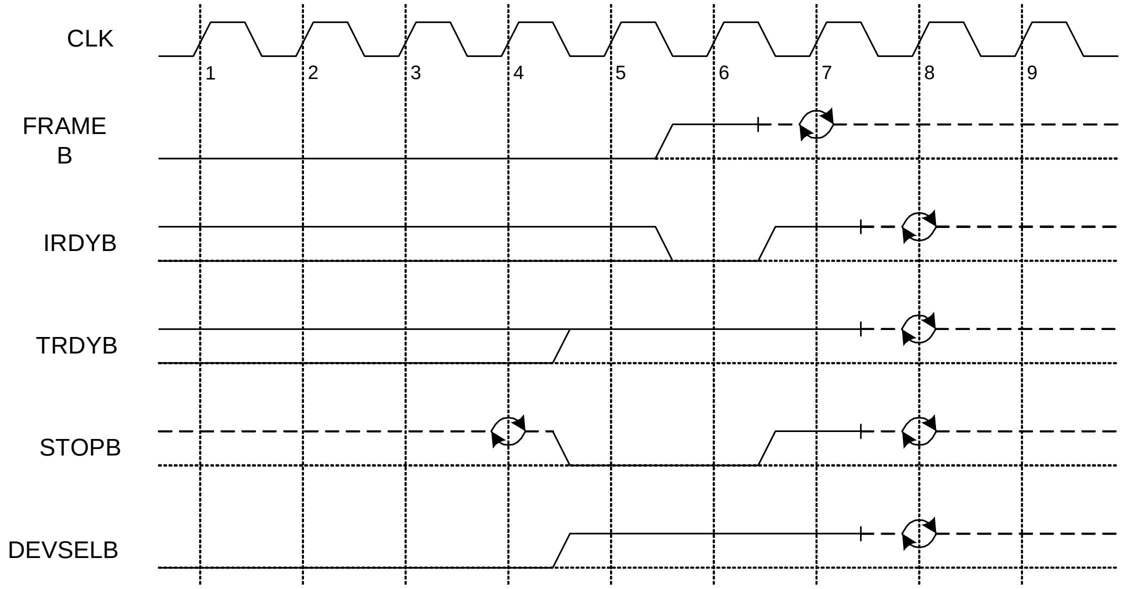



**Figure 26. Target Initiated Termination - Abort**

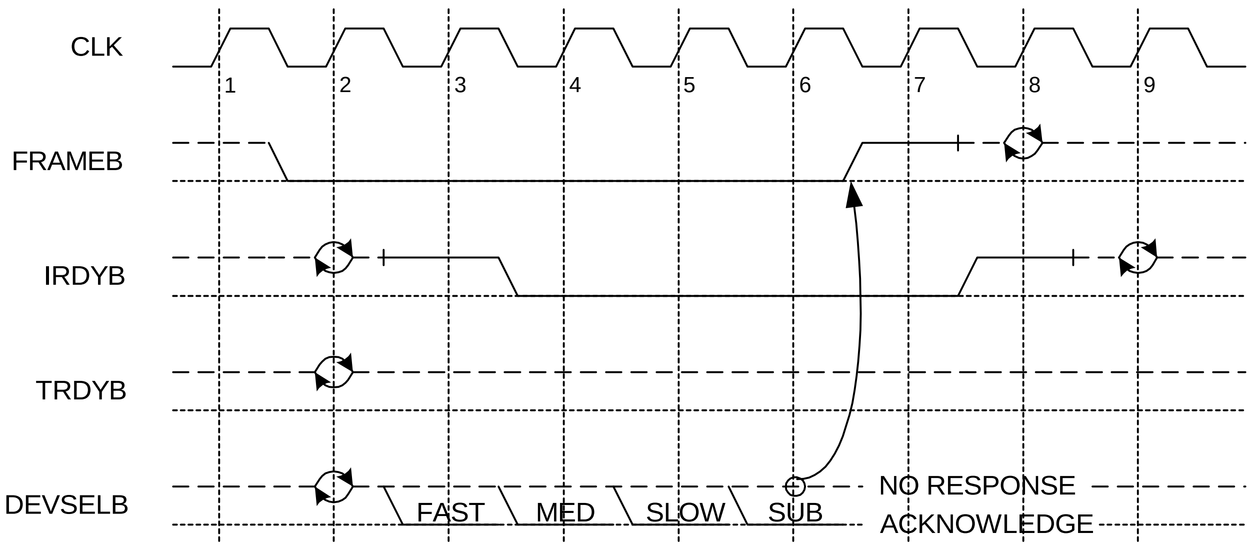



**Figure 27. Master Initiated Termination - Abort**

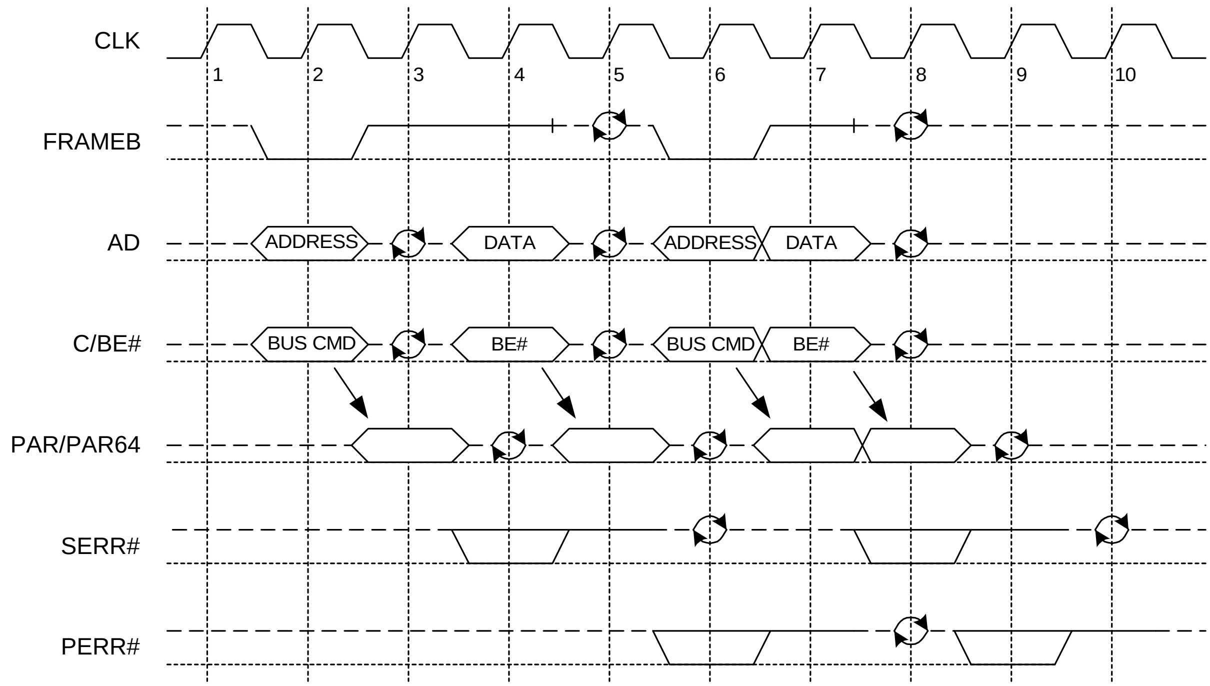



**Figure 28. Parity Operation – One Example**

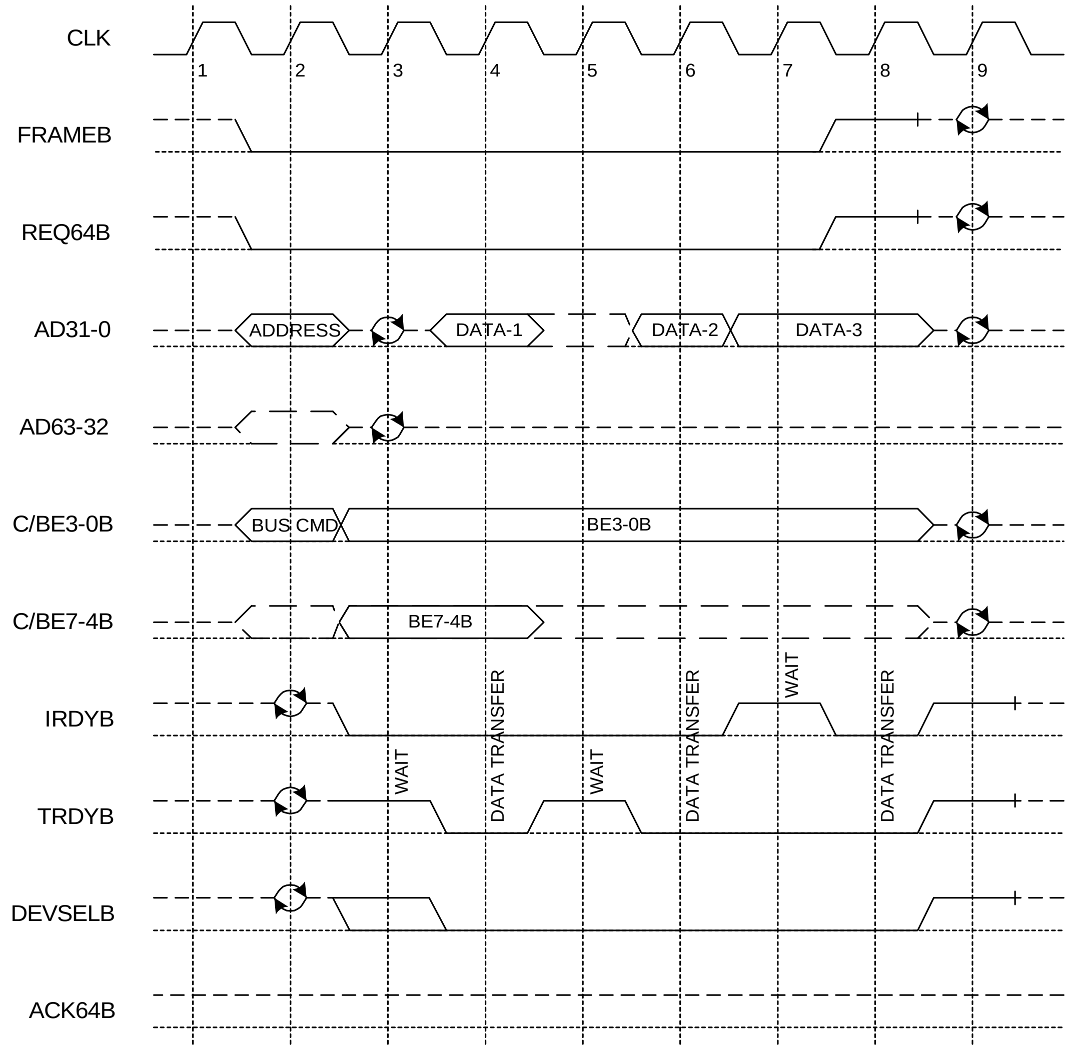



**Figure 29. Memory Read Below 4GB (32-bit address, 32-bit data transfer granted; 64-bit slot)**

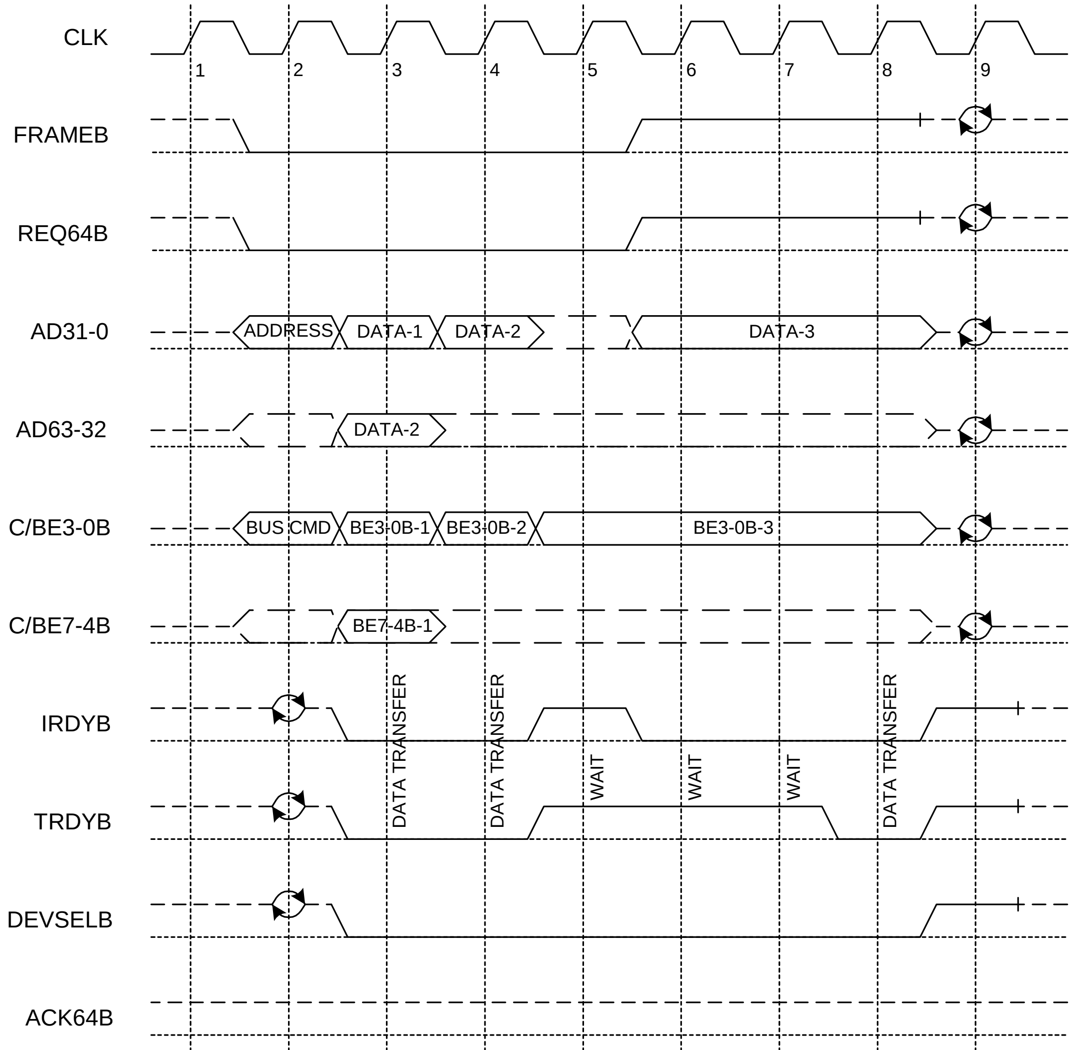



**Figure 30. Memory Write below 4GB (32-bit address, 32-bit data transfer granted; 64-bit slot)**

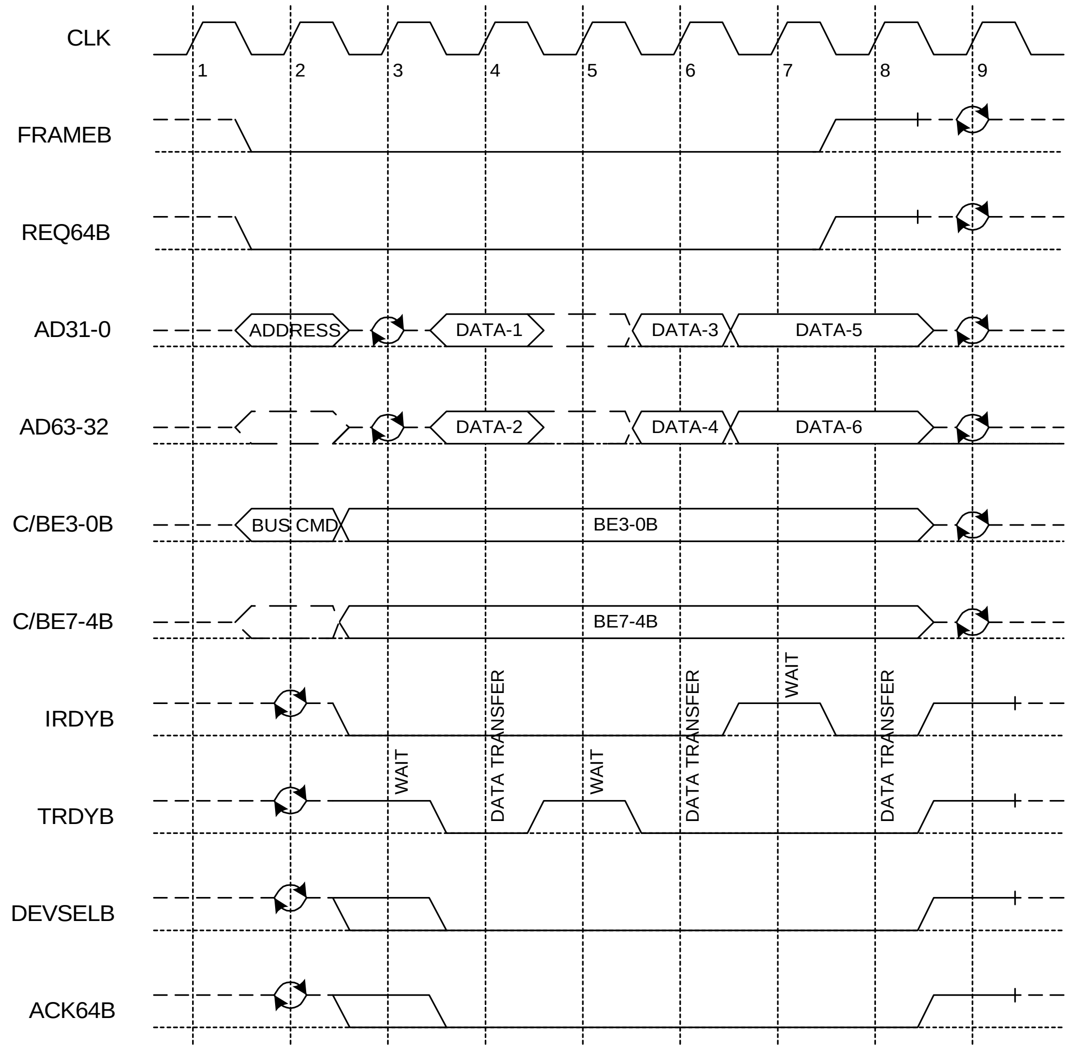



**Figure 31. Memory Read below 4GB (32-bit address, 64-bit data transfer granted; 64-bit slot)**

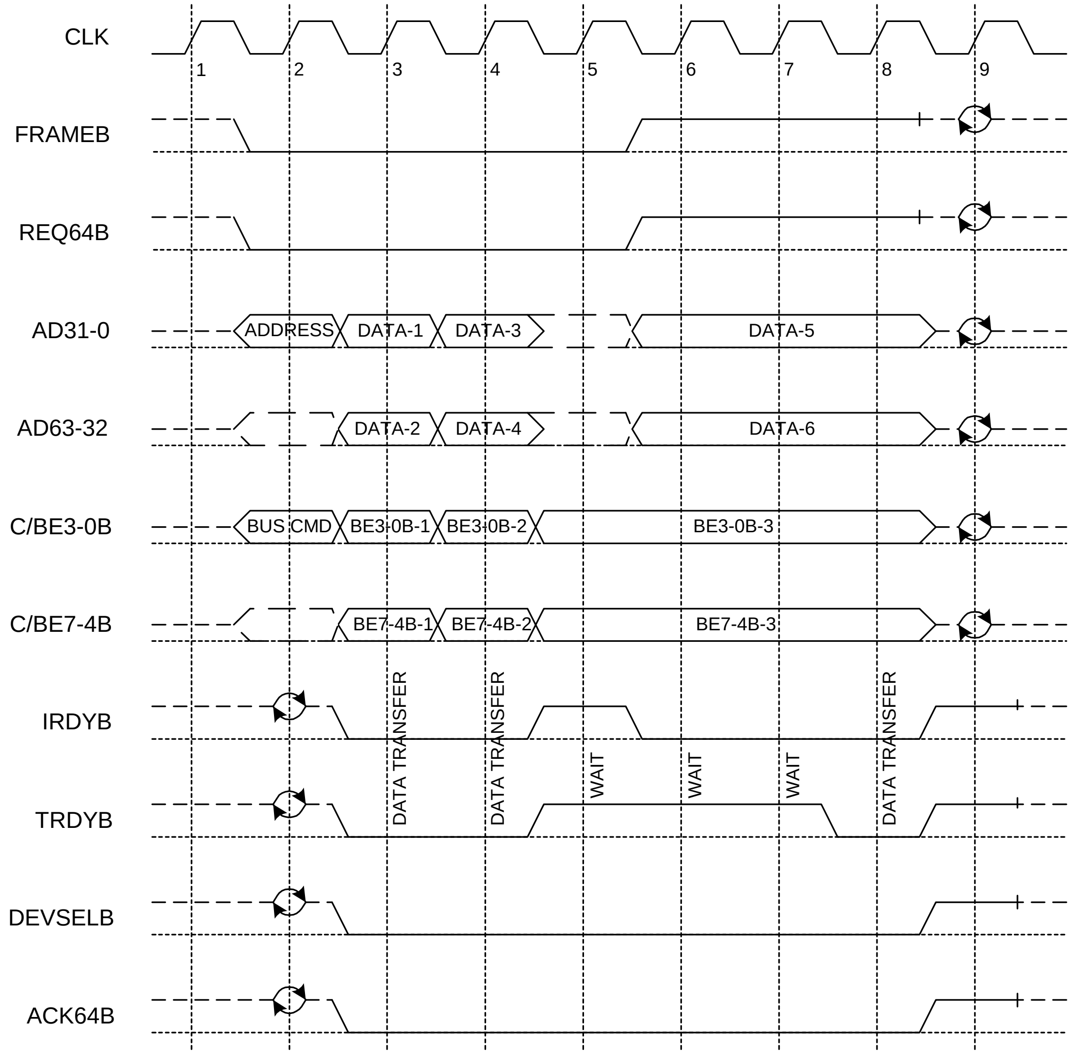



**Figure 32. Memory Write below 4GB (32-bit address, 64-bit data transfer granted; 64-bit slot)**

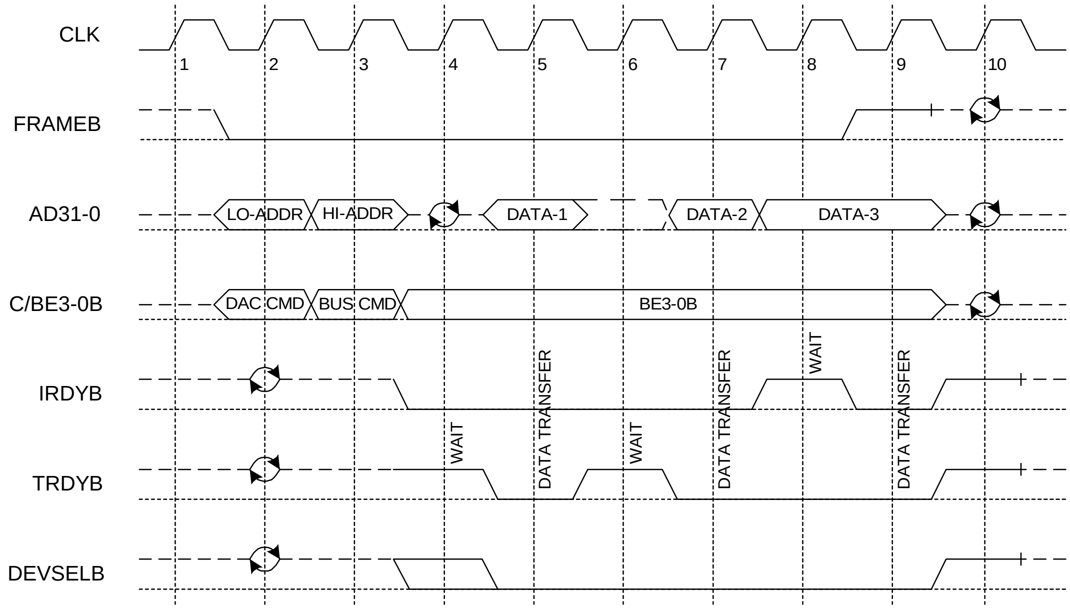



**Figure 33. Memory Read above 4GB (DAC, 64-bit address, 32-bit data; 32-bit slot)**

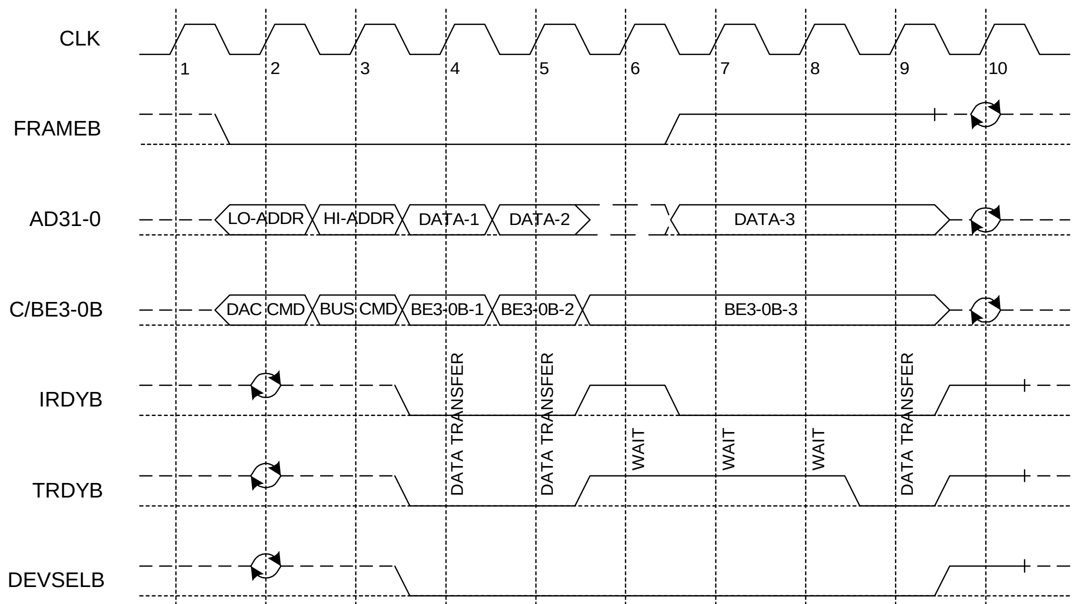



**Figure 34. Memory Write above 4GB (DAC, 64-bit address, 32-bit data; 32-bit slot)**

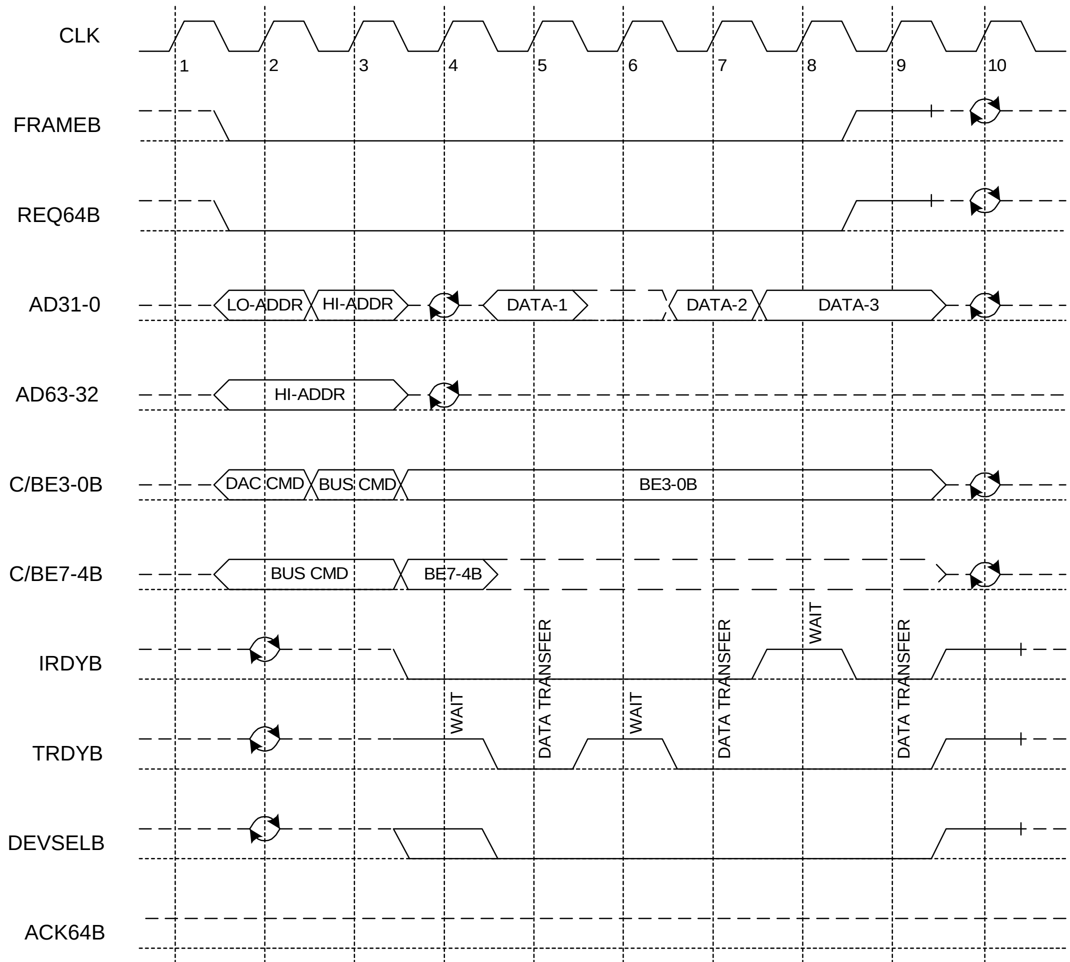



**Figure 35. Memory Read above 4GB (DAC, 64-bit address, 32-bit data transfer granted; 64-bit slot)**

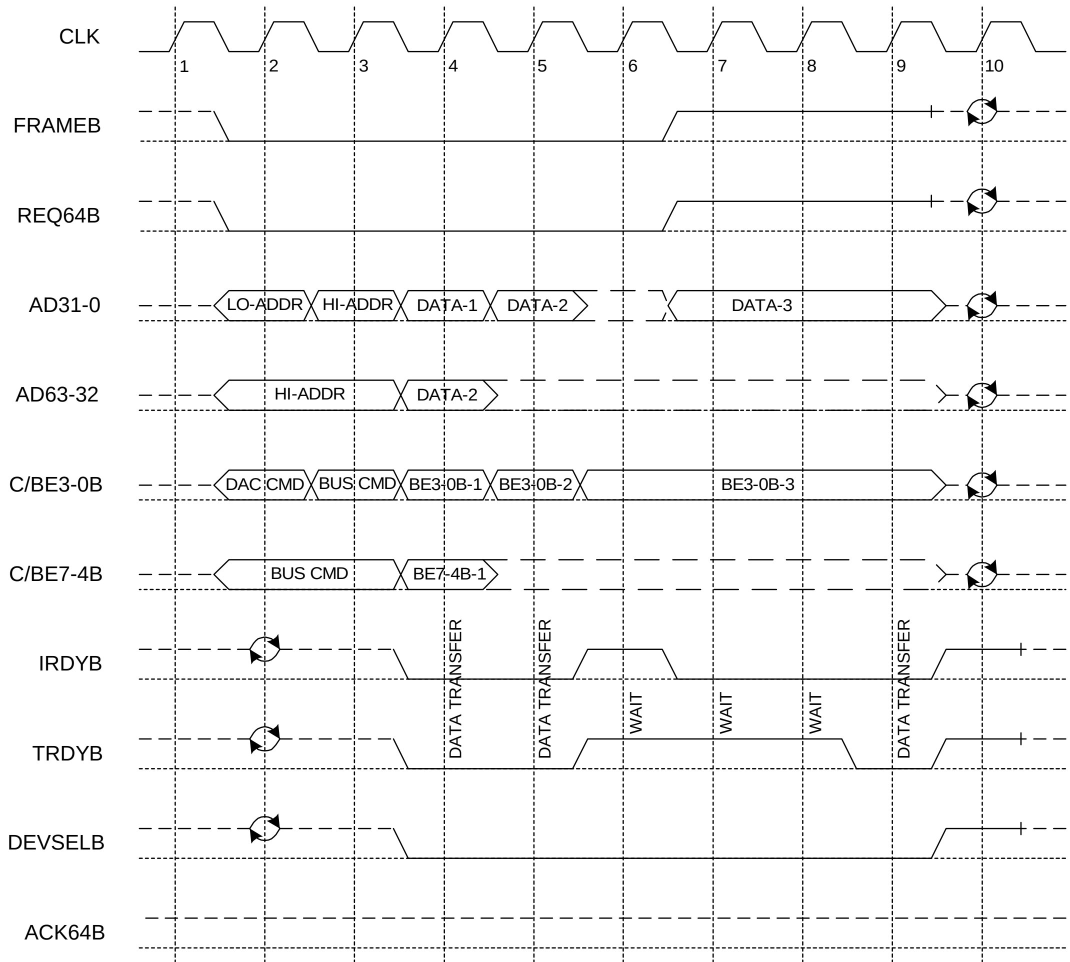



**Figure 36. Memory Write above 4GB (DAC, 64-bit address, 32-bit data transfer granted; 64-bit slot)**

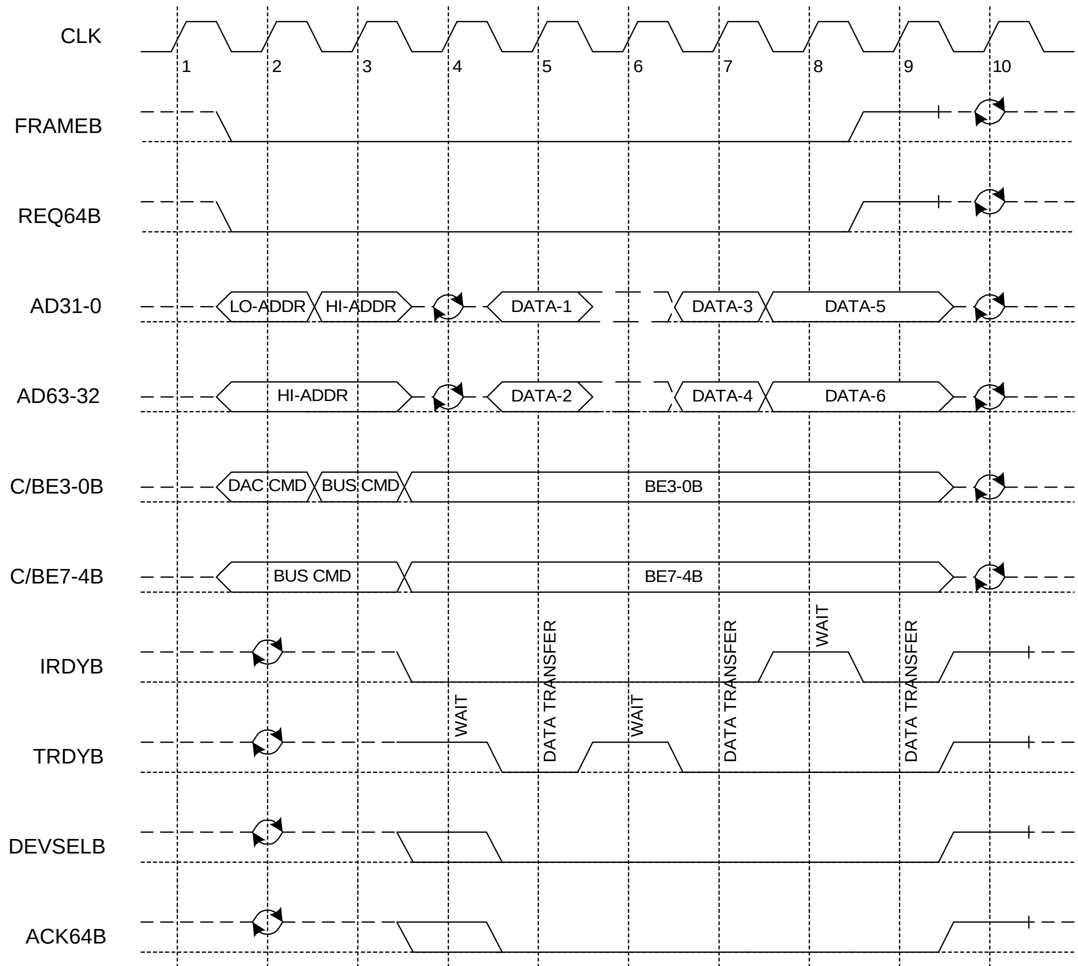



**Figure 37. Memory Read above 4GB (DAC, 64-bit address, 64-bit data transfer granted; 64-bit slot)**

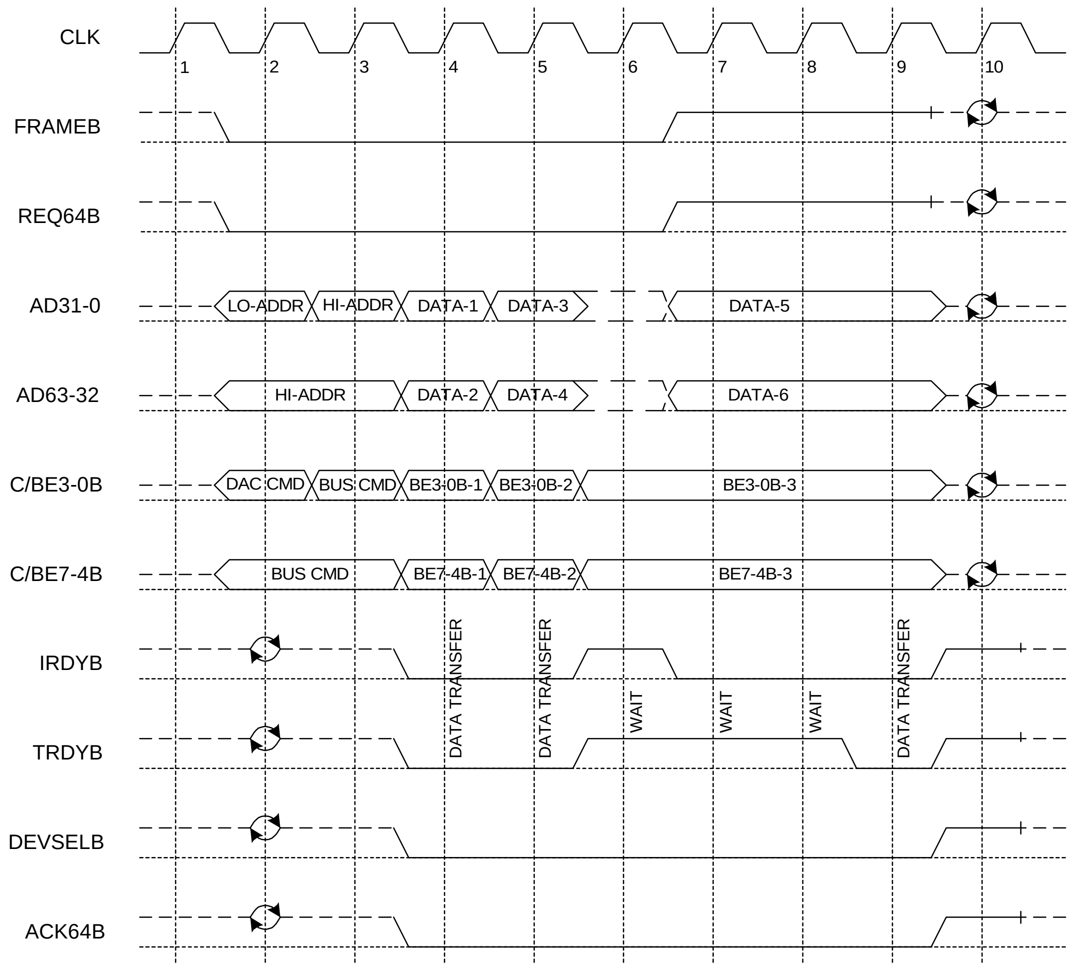
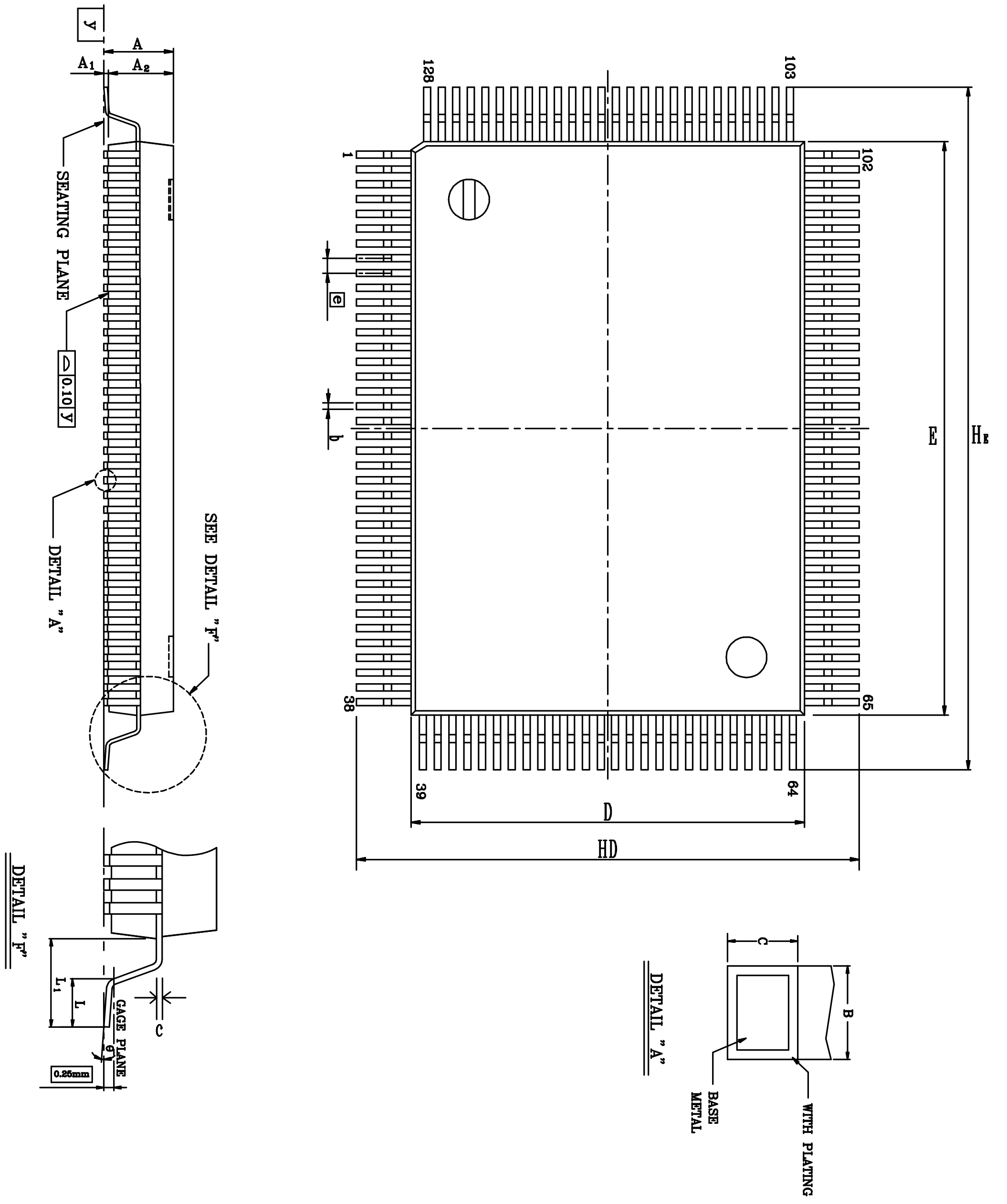



**Figure 38. Memory Write above 4GB (DAC, 64-bit address, 64-bit data transfer granted; 64-bit slot)**

# 12. Mechanical Dimensions

## 12.1. 128-Pin QFP Mechanical Dimensions




See the Mechanical Dimensions notes on the next page.

## 12.2. Notes for 128-Pin QFP Dimensions

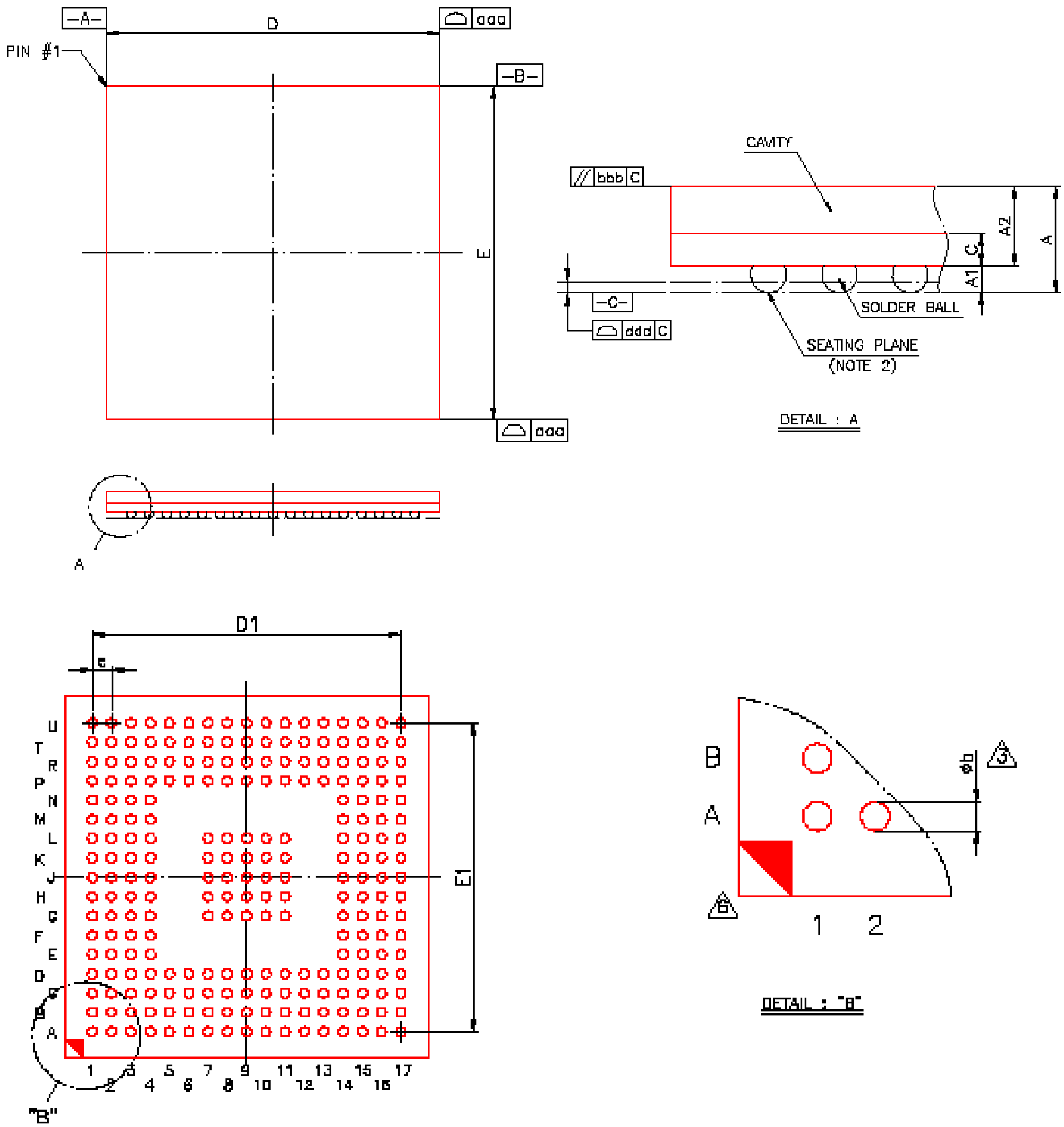
| Symbol | Dimensions in inches | | | Dimensions in mm | | |
|---|---|---|---|---|---|---|
| | Min | Typical | Max | Min | Typical | Max |
| **A** | - | - | 0.134 | - | - | 3.40 |
| **A1** | 0.004 | 0.010 | 0.036 | 0.10 | **0.25** | 0.91 |
| **A2** | 0.102 | 0.112 | 0.122 | 2.60 | **2.85** | 3.10 |
| **c** | 0.002 | 0.006 | 0.010 | 0.05 | **0.15** | 0.25 |
| **D** | 0.541 | 0.551 | 0.561 | 13.75 | **14.00** | 14.25 |
| **E** | 0.778 | 0.787 | 0.797 | 19.75 | **20.00** | 20.25 |
| e | 0.010 | 0.020 | 0.030 | 0.25 | **0.5** | 0.75 |
| **HD** | 0.665 | 0.677 | 0.689 | 16.90 | **17.20** | 17.50 |
| **HE** | 0.902 | 0.913 | 0.925 | 22.90 | **23.20** | 23.50 |
| **L** | 0.027 | 0.035 | 0.043 | 0.68 | **0.88** | 1.08 |
| **L1** | 0.053 | 0.063 | 0.073 | 1.35 | **1.60** | 1.85 |
| **y** | - | - | 0.004 | - | - | 0.10 |
| **θ** | 0° | - | 12° | 0° | - | 12° |

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar rotrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. Should be based on final visual inspection.

| TITLE: -CU L/F, FOOTPRINT 3.2 mm | | | |
|---|---|---|---|
| LEADFRAME MATERIAL: | | | |
| APPROVE | | DOC. NO. | |
| | | VERSION | |
| | | PAGE | |
| CHECK | | DWG NO. | Q128 - 1 |
| | | DATE | |
| REALTEK SEMICONDUCTOR CO., LTD | | | |

# 12.3. 233-PIN TFBGA Mechanical Dimensions




See the Mechanical Dimensions notes on the next page.

## 12.4. Notes for 233-Pin TFBGA Dimensions

| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | --- | --- | 1.30 | --- | --- | 0.051 |
| A1 | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| A2 | 0.84 | 0.89 | 0.94 | 0.033 | 0.035 | 0.037 |
| c | 0.32 | 0.36 | 0.40 | 0.013 | 0.014 | 0.016 |
| D | 14.90 | 15.00 | 15.10 | 0.587 | 0.591 | 0.594 |
| E | 14.90 | 15.00 | 15.10 | 0.587 | 0.591 | 0.594 |
| D1 | --- | 12.80 | --- | --- | 0.504 | --- |
| E1 | --- | 12.80 | --- | --- | 0.504 | --- |
| e | --- | 0.80 | --- | --- | 0.031 | --- |
| b | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| aaa | 0.10 | | | 0.004 | | |
| bbb | 0.10 | | | 0.004 | | |
| ddd | 0.12 | | | 0.005 | | |
| eee | 0.15 | | | 0.006 | | |
| fff | 0.08 | | | 0.003 | | |
| MD/ME | 17/17 | | | 17/17 | | |

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERANCE DOCUMENT : JEDEC MO-205
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

# 13. Ordering Information

**Table 37. Ordering Information**

| Part number | Package | Status |
|---|---|---|
| RTL8169S-32 | 128-pin QFP | |
| RTL8169S-64 | 233-pin TFBGA | |
| RTL8110S-32 | 128-pin QFP | |
| RTL8110S-64 | 233-pin TFBGA | |

# Appendix A. Driver programming note

## A-1 MAC registers configuration sequence

The "**C+ Command**" and "**Command**" registers are the key parameters before any other registers or descriptors are configured. It is necessary to configure the MAC registers as following Steps:

Step1. Configure C+ Command Register (Offset 00E0h-00E1h)
Step2. Configure Command Register (Offset 0037h)
Step3. Configure Other Registers

## A-2 Multicast Registers configuration

The way to configure the MAR registers is the same with the NE2000 driver.

## A-3 Checksum offload Tx Descriptor note

To transmit an Ethernet packet, the upper layer might split this packet to several transmit buffers. Each transmit buffer corresponds to a Tx descriptor. If it transmits a packet with the **Checksum Task Offload**, it is necessary to set the related checksum offload bits of all Tx descriptors with this packet.

## A-4 GMII registers configuration sequence during driver initialization

Configure the GMII registers as below during driver initialization:

1. OutPortUlong(offset0x60, 0x801f0001);
2. OutPortUlong(offset0x60, 0x80151000);
3. OutPortUlong(offset0x60, 0x801865c7);
4. OutPortUlong(offset0x60, 0x80040000);
5. OutPortUlong(offset0x60, 0x800300a1);
6. OutPortUlong(offset0x60, 0x80020008);
7. OutPortUlong(offset0x60, 0x80011020);
8. OutPortUlong(offset0x60, 0x80001000);
9. OutPortUlong(offset0x60, 0x80040800);

10. OutPortUlong(offset0x60, 0x80040000);
11. OutPortUlong(offset0x60, 0x80047000);
12. OutPortUlong(offset0x60, 0x8003ff41);
13. OutPortUlong(offset0x60, 0x8002de60);
14. OutPortUlong(offset0x60, 0x80010140);
15. OutPortUlong(offset0x60, 0x80000077);
16 OutPortUlong(offset0x60, 0x80047800);
17. OutPortUlong(offset0x60, 0x80047000);
18. OutPortUlong(offset0x60, 0x8004a000);
19. OutPortUlong(offset0x60, 0x8003df01);
20. OutPortUlong(offset0x60, 0x8002df20);
21. OutPortUlong(offset0x60, 0x8001ff95);
22. OutPortUlong(offset0x60, 0x8000fa00);
23. OutPortUlong(offset0x60, 0x8004a800);
24. OutPortUlong(offset0x60, 0x8004a000);
25. OutPortUlong(offset0x60, 0x8004b000);
26. OutPortUlong(offset0x60, 0x8003ff41);
27. OutPortUlong(offset0x60, 0x8002de20);
28. OutPortUlong(offset0x60, 0x80010140);
29. OutPortUlong(offset0x60, 0x800000bb);
30. OutPortUlong(offset0x60, 0x8004b800);
31. OutPortUlong(offset0x60, 0x8004b000);
32. OutPortUlong(offset0x60, 0x8004f000);
33. OutPortUlong(offset0x60, 0x8003df01);
34. OutPortUlong(offset0x60, 0x8002df20);
35. OutPortUlong(offset0x60, 0x8001ff95);
36. OutPortUlong(offset0x60, 0x8000bf00);
37. OutPortUlong(offset0x60, 0x8004f800);
38. OutPortUlong(offset0x60, 0x8004f000);
39. OutPortUlong(offset0x60, 0x80040000);
40. OutPortUlong(offset0x60, 0x801f0000);
41. OutPortUlong(offset0x60, 0x800b0000);

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