

## TECH BRIEF:

# MDP Improves Microprocessor Design

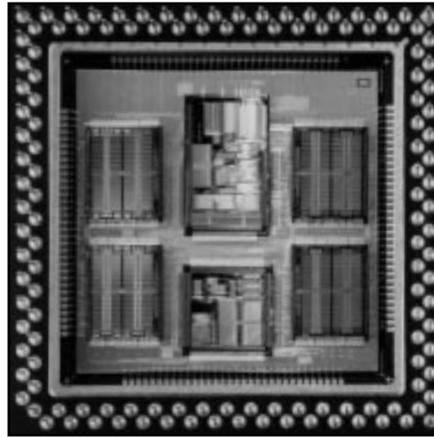
In the computer industry's never ending drive for more speed and performance, semiconductor manufacturers are under constant pressure to produce silicon with higher density and greater functionality while maintaining or lowering their cost structure. These conflicting goals can be met by utilizing multi-die packaging (MDP) technology as ROSS has demonstrated recently with their 90 MHz hyperSPARC.

MDP technology integrates multiple bare die into a single IC package. Instead of driving high-frequency signals from chip to chip across a PCB, these signals travel millimeters through a silicon substrate with only a fraction of the capacitive and inductive loads. This not only results in higher attainable clock speeds, but also a considerable reduction in power consumption.

Providing interconnect through a silicon substrate offers significant benefits over interconnect through a PCB, including higher clock frequencies, lower power consumption, less capacitive loading, and smaller board surface requirements. In addition, the reliability and speed of a chipset assembled in an MDP is greater than if implemented as discrete chips.

MDP technology successfully addresses fundamental limitations of

conventional packaging. Bare die are simply faster than packaged die, due in large part to the interconnection scheme. To suppliers of advanced microprocessor products such as ROSS Technology, the nanoseconds gained



RT629 hyperSPARC MDP

by MDPs in signal transmissions between chips are significant. Multi-die packaging makes systems and semiconductor designers' jobs easier, and it makes higher performance products possible without any modifications to existing die. MDPs are also more economical to manufacture because they utilize smaller die.

ROSS' hyperSPARC chipset is a full custom CMOS implementation of the SPARC RISC architecture. The components of the chipset include the RT620 Central Processing Unit (CPU), the RT625 Cache Controller, Memory Management, and Tag Unit (CMTU),

and the RT627 Cache Data Unit (CDU). Together, they compromise a six-chip CPU with 256 Kbytes of second-level cache and complete support for multi-processing systems. ROSS' MDP implementation is a 131-pin PGA package which mounts the six individual bare die into the cavity of the PGA package. The I/O signals are brought to the outside world using conventional wire-bonding.

It is clear to designers and manufacturers that the "chipset" approach to CPU design is the most economically attractive solution to meeting the challenges of price, performance, and space imposed by the computer industry. Rising costs drive semiconductor vendors away from huge, monolithic die; board area and performance requirements drive manufacturers from multiple discrete packages. The intersection is MDP.



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