Savage4 Graphics/Video Accelerator Family

Hardware Reference

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NOTATIONAL CONVENTIONS

The following notational conventions are used in this data book:

Signal names are shown in all uppercase letters. For example, XD.

A bar over a signal name indicates an active low signal. For example, $\overline{OE}$.

n-m indicates a bit field from bit n to bit m. For example, 7-0 specifies bits 7 through 0, inclusive.

n:m indicates a signal (pin) range from n to m. For example D[7:0] specifies data lines 7 through 0, inclusive

Use of a trailing letter H indicates a hexadecimal number. For example, 7AH is a hexadecimal number.

Use of a trailing letter b indicates a binary number. For example, 010b is a binary number.

When numerical modifiers such as K or M are used, they refer to binary rather than decimal form. Thus, for example, 1 KByte would be equivalent to 1024, not 1,000 bytes.

NOTICES

Additional information may be obtained from:

S3 Incorporated, Literature Department P.O. Box 58058, Santa Clara, CA 95052-8058.

Telephone: 408-588-8000, Fax: 408-980-5444

Changes Since the Previous Version (DB046-0.3, January 1999)

1. Section 2: Changed mold cap dimension to 29x29 mm max and cap height to 2.5 mm max (motherboard package)
2. Section 3: Added BISTON and DFTON pins with requirement to tie these to ground. Changed RSET resistor to 140 Ohms to conform to new VESA standard for full scale output voltage. Corrected drive current control descriptions for PCI/AGP. Added requirements for external oscillator connected to XIN.
3. Section 4: Extensively revised and expanded the electrical specifications.
4. Section 5: Removed panel and TV connections from strapping options (no need to strap)
5. Section 7: Corrected 1Mx32 SGRAM connection diagram. Corrected bit setting for 1Mx32 dual chip select 16MB configuration
6. Section 9: Modified analog power and ground connections for REGOUTA and REGINA pins.

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- 140M pixels/second trilinear fill rate
- Full AGP 4x/2x, including sideband addressing and execute mode
- S3 DX6 texture compression (S3TC)
- Flat panel desktop monitor support
- High quality DVD video playback

3D Rendering Features

- Single-pass multiple textures
- Hardware bump mapping
- Full scene anti-aliasing
- Anisotropic filtering
- 8-bit stencil buffer
- Single cycle trilinear filtering
- 32-bit true color rendering
- Specular lighting and diffuse shading
- Alpha blending modes
- MPEG-2 video textures
- Vertex and table fog
- 16- or 24-bit Z-buffering
- Sprite anti-aliasing, reflection mapping, texture morphing, shadows, procedural textures and atmospheric effects

Motion Video Architecture

- High quality up/down scaler
- Planar to packed format conversion
- Motion compensation for full speed DVD playback
- Hardware subpicture blending and highlights
- Multiple video windows for video conferencing
- Contrast, hue, saturation, brightness and gamma controls
- 60MHz VIP video port allows HDTV resolutions
- Digital port for NTSC/PAL TV encoders

High Speed Memory Bus

- 125/143 MHz memory interface
- 2 to 32 MB frame buffer
- 1Mx16 or 2Mx32 or 4Mx16 SDRAMs
- 256Kx32 or 512Kx32 or 1Mx32 SGRAMs
- SO-DIMM memory upgrade
- Block write support with SGRAM

2D Acceleration Features

- Highly optimized 128-bit graphics engine
- Full featured 2D engine for acceleration of BitBLT, rectangle fill, line draw, polygon fill, panning/scrolling and hardware cursor
- 8, 16, and 32 bpp mode acceleration

Flat Panel Desktop Monitor Support

- 24-bit digital interface for flat panel encoders
- Auto-expansion and centering for VGA text and graphics modes
- Support for all resolutions up to 1280x1024

Full Software Support

- Drivers for major operating systems and APIs: [Windows® 9x, Windows NT 4.0/5.0, Windows 3.x and OS/2® 2.1/3.0 (Warp™), Direct3D™ , DirectDraw™ and DirectShow™ , OpenGL™ ICD for Windows 9x and NT]
- Comprehensive SDK, utilities and ISV tools
- ISV and bundling programs

Additional Features

- 300MHz RAMDAC with gamma correction
- I^2C serial bus and flash ROM support
- ACPI and PCI power management
- Hardware and BIOS support for VESA timings and DDC monitor communications
- PCI 2.2 bus support including bus mastering
- 27x27mm PBGA with 336 balls for add-in card implementations
- 31x31mm PBGA with 353 ball for motherboard implementations
- 2.5V core with 3.3V/5V tolerant I/O

1.0 OVERVIEW

S3® adds the following graphics controllers to the Savage4™ product family.

Part Number	Part Name	Max AGP Support	Max Frame Buffer Size	MCLK/ECLK (MHz)*	Package Size	Pinout Optimized for:	CR92_4	CRB0_5	CR37_2
86C397	Savage4 PRO™ 143	4X	32MB	143/125	27x27mm	AIC/MB	1	1	1
86C397	Savage4 PRO	4X	32MB	125/110	27x27mm	AIC/MB	1	1	1
86C395	Savage4 GT™	2X	16MB	125/110	27x27mm	AIC/MB	1	0	1
86C394	Savage4 LT™	2x	8MB	110/110	27x27mm	AIC/MB	0	0	1
86C396	Savage4 PRO-M™ 143	4X	32MB	143/125	31x31mm	Motherboard	1	1	0
86C396	Savage4 PRO-M	4X	32MB	125/110	31x31mm	Motherboard	1	1	0

* MCLK = Memory clock; ECLK = Engine clock

This family brings high-performance 3D graphics to the mainstream PC by integrating 2D acceleration, DVD video acceleration and leading edge 3D performance into cost effective packages. The Savage4 family provides the ideal solutions for the high-performance consumer, corporate desktop user and entry level professional.

The industry's first AGP 4x solution, Savage4 combines AGP 4x with S3's DX6 texture compression (S3TC) to deliver unprecedented 3D performance and image quality for the mainstream desktop PC market. Supported by many of 1999's top

3D games such as Unreal Tournament and Quake III Arena, S3TC enables software developers to use up to 8x the amount of texture storage and AGP bus bandwidth.

1.1 HIGH-PERFORMANCE 3D ACCELERATOR

Featuring a new super-pipelined 128-bit engine, Savage4 utilizes a single cycle architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including single-pass multitexturing, full scene anti-aliasing, anisotropic filtering, an 8-bit stencil buffer and hardware bump mapping. Savage4 also offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering - enabling stunning image quality without performance loss. Savage4 further enhances image quality with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images.

Savage4's advanced triangle setup engine provides industry leading 3D performance for a realistic user experience in games and other interactive 3D applications. The 3D engine is designed for AGP texturing from system memory or the local frame buffer.

1.2 128-BIT 2D GRAPHICS ENGINE

Savage4's advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. Several enhancements have been made to the 2D architecture to maintain best of class performance and to provide acceleration in all color depths.

1.3 DVD PLAYBACK AND VIDEO CONFERENCING

Savage4 provides the ideal architecture for high quality MPEG-2 playback for interactive DVD applications and video conferencing. The video accelerator offloads the CPU by performing the planar to packed format conversion and motion compensation tasks. The enhanced scaling algorithm delivers incredible full-screen video playback. The multiple video windows and image mirroring provides the ideal solution for video conferencing. Finally, the 60 MHz VIP video port allows low cost connection to industry-standard MPEG-2 decoders and video digitizers for applications such as WebTV® and TV tuner designs.

1.4 FLAT PANEL DESKTOP MONITOR SUPPORT

Savage4 has the capability of displaying graphics on flat panel desktop monitors using a 24-bit digital interface to an external encoder. Savage4 also supports autoexpansion and centering of all VGA text and graphics modes so the entire flat panel display will be utilized. All resolutions are supported up to 1280x1024.

1.5 HIGH SCREEN RESOLUTION CRT SUPPORT

	Frame Buffer Size		
Resolutions Supported	**4 MB**	**8 MB**	**16/32 MB**
640x480x8/16/32	✔	✔	✔
800x600x8/16/32	✔	✔	✔
1024x768x8/16/32	✔	✔	✔
1280x1024x8/16	✔	✔	✔
1280x1024x32		✔	✔
1600x1200x8/16	✔	✔	✔
1600x1200x32		✔	✔
1920x1440x8	✔	✔	✔
1920x1440x16		✔	✔
1920x1440x32			✔

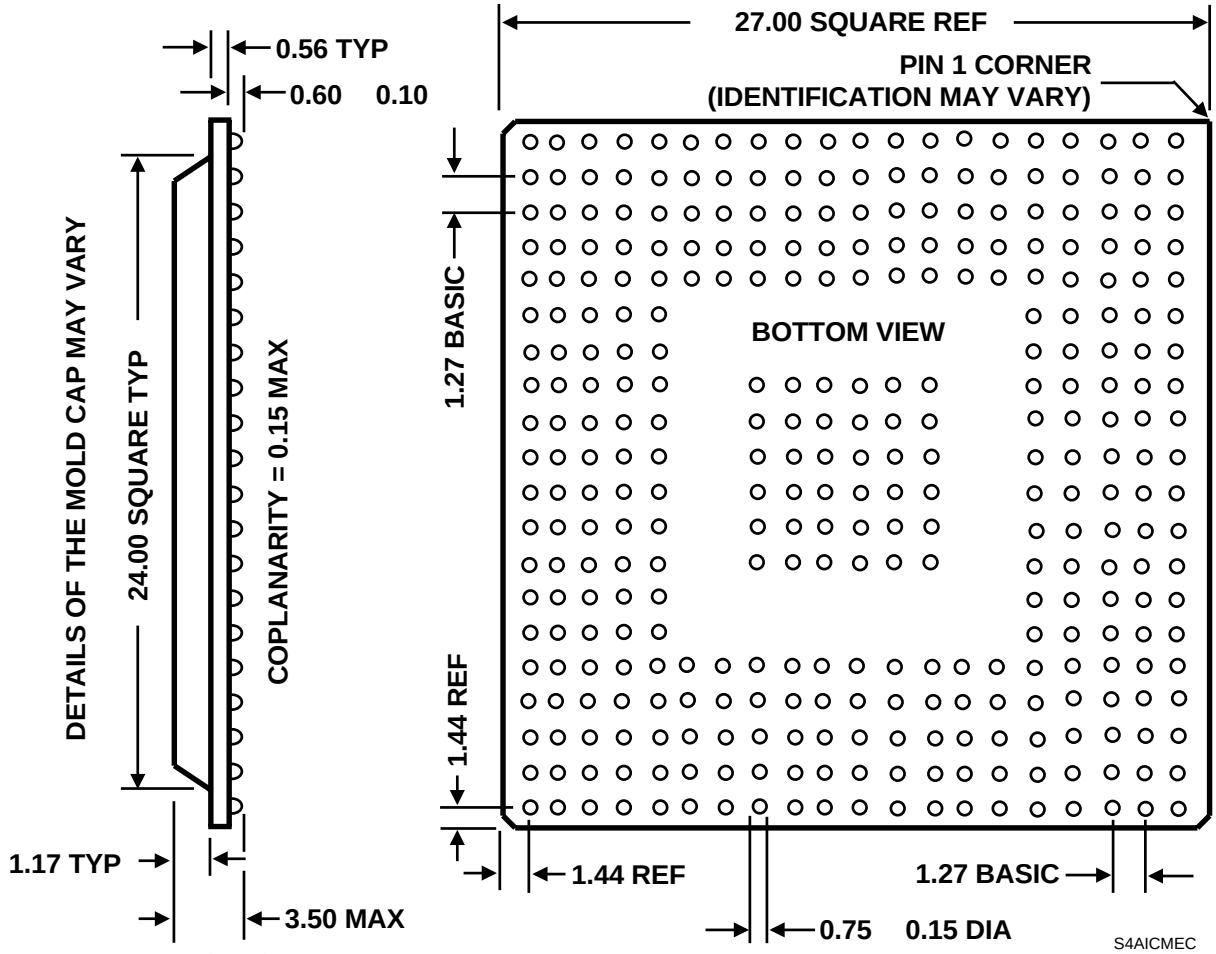
Section 2: Mechanical Data

2.1 THERMAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
Case Temperature (no heat sink)			110	°C
Case Temperature (heat sink)			95	°C

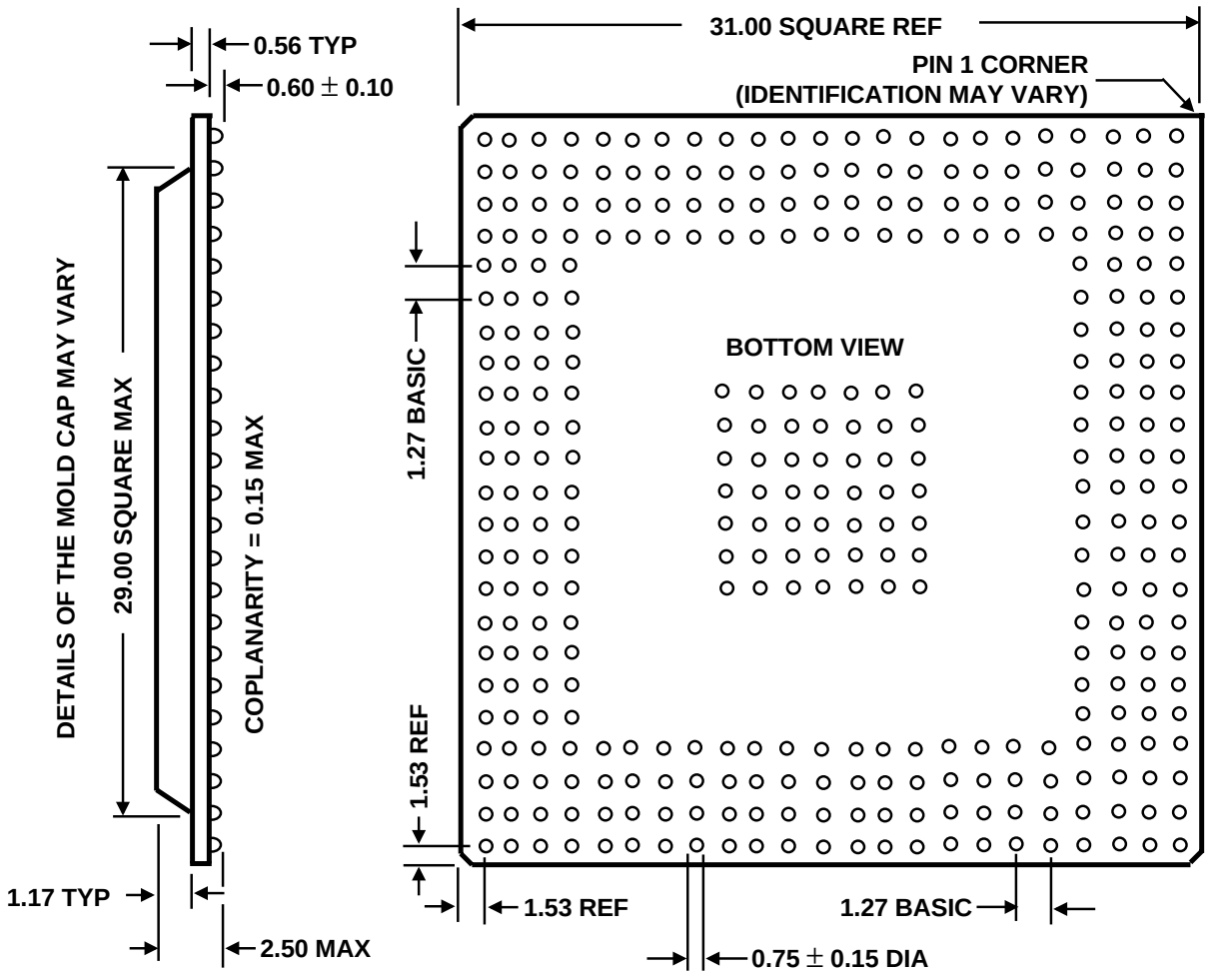
2.2 MECHANICAL DIMENSIONS

The mechanical dimensions for the add-in card and motherboard packages are given in Figures 2-1 and 2-2 respectively.



NOTES:
1. ALL DIMENSIONS IN MILLIMETERS
2. DIMENSIONS ARE IN COMPLIANCE WITH JEDEC REFERENCE MO-151
3. SUBSTRATE THICKNESS MAY VARY BY SUPPLIER

Figure 2-1. Add-in Card PBGA Mechanical Dimensions



NOTES:
1. ALL DIMENSIONS IN MILLIMETERS
2. DIMENSIONS ARE IN COMPLIANCE WITH JEDEC REFERENCE MO-151
3. SUBSTRATE THICKNESS MAY VARY BY SUPPLIER

Figure 2-2. Motherboard PBGA Mechanical Dimensions

Section 3: Pins

3.1 ADD-IN CARD PINOUT DIAGRAM

The add-in card pinout is shown in Figure 3-1.

A1 ROMEN FCE EPCS0	A2 FOE EPCS1	A3 PD32	A4 PD33	A5 PD47	A6 PD46	A7 PD48	A8 PD50	A9 SDCLKOUT	A10 PD63	A11 PD61	A12 PD58	A13 DQM5	A14 N/C	A15 CAS	A16 CS1	A17 MA7	A18 MA5	A19 MA3	A20 VSS
B1 VID0 LD0	B2 FWE EPSI	B3 PD34	B4 PD35	B5 VDDm	B6 PD45	B7 PD40	B8 PD51	B9 VDDm	B10 PD62	B11 PD60	B12 PD57	B13 VDDm	B14 DQM6	B15 RAS	B16 CS0	B17 VDDm	B18 MA4	B19 MA1	B20 MA2
C1 VID2 LD2	C2 VID1 LD1	C3 PD36	C4 PD37	C5 PD38	C6 PD44	C7 PD42	C8 PD49	C9 PD52	C10 PD54	C11 PD59	C12 PD56	C13 SDCLK1	C14 DQM4	C15 CS3	C16 DSF	C17 MA6	C18 MA9	C19 MA10	C20 MA0
D1 VID4 LD4	D2 HAD1 HREF	D3 VID3 LD3	D4 VSS	D5 PD39	D6 PD43	D7 PD41	D8 VSS	D9 PD53	D10 PD55	D11 SDCLK2	D12 DQM7	D13 VSS	D14 WE	D15 CS2	D16 MA8	D17 DQM0	D18 DQM2	D19 DQM3	D20 DQM1
E1 VID6 LD6	E2 HCTL VS	E3 VID5 LD5	E4 HAD0 ODDIN	E5 SPD1	E6 SPCLK1	E7 N/C	E8 SDCLKR2	E9 VSS	E10 N/C	E11 VDDCORE	E12 N/C	E13 VDDCORE	E14 N/C	E15 N/C	E16 N/C	E17 PD24	E18 PD25	E19 VDDm	E20 PD26
F1 VIPCLK	F2 PIXCLK LCLK	F3 VID7 LD7	F4 SPCLK2	F5 N/C											F16 N/C	F17 VSS	F18 PD27	F19 PD28	F20 PD29
G1 ROMD0 TVDAT0 PANELD0	G2 GOP0	G3 GPOUT	G4 SPD2	G5 N/C											G16 N/C	G17 PD23	G18 PD22	G19 PD30	G20 PD31
H1 ROMD4 TVDAT4 PANELD4	H2 ROMD3 TVDAT3 PANELD3	H3 ROMD2 TVDAT2 PANELD2	H4 ROMD1 TVDAT1 PANELD1	H5 VDDv			H8 VSS	H9 VSS	H10 VSS	H11 VSS	H12 VSS	H13 VSS			H16 VDDCORE	H17 PD21	H18 PD20	H19 PD19	H20 PD18
J1 TVCLKR PANELCLK	J2 ROMD7 TVDAT7 PANELD7	J3 ROMD6 TVDAT6 PANELD6	J4 ROMD5 TVDAT5 PANELD5	J5 VDDv			J8 VSS	J9 VSS	J10 VSS	J11 VSS	J12 VSS	J13 VSS			J16 VREFM	J17 PD8	J18 PD17	J19 VDDm	J20 PD16
K1 VSS	K2 TVCLK PANELDE	K3 ROMA1 TVHS PANELD9	K4 ROMA0 TVVS PANELD8	K5 BISTON (tie to VSS)			K8 VSS	K9 VSS	K10 VSS	K11 VSS	K12 VSS	K13 VSS			K16 SDCLKR1	K17 VSS	K18 PD9	K19 PD12	K20 PD13
L1 ROMA5 TVDAT9 PANELD13	L2 ROMA4 TVDAT8 PANELD12	L3 ROMA3 TVBLANK PANELD11 EPCLK DCLK	L4 ROMA2 PANELD10 EPSO OVERLAY	L5 VDDCORE			L8 VSS	L9 VSS	L10 VSS	L11 VSS	L12 VSS	L13 VSS			L16 VSS	L17 PD10	L18 PD11	L19 PD14	L20 PD15
M1 ROMA9 PANELD17	M2 ROMA8 PANELD16	M3 ROMA7 TVDAT11 PANELD15	M4 ROMA6 TVDAT10 PANELD14	M5 VSS			M8 VSS	M9 VSS	M10 VSS	M11 VSS	M12 VSS	M13 VSS			M16 DFTON (tie to VSS)	M17 PD7	M18 PD6	M19 PD3	M20 PD2
N1 ROMA13 PANELD21	N2 ROMA12 PANELD20	N3 ROMA11 PANELD19	N4 ROMA10 PANELD18	N5 PANELDET			N8 VSS	N9 VSS	N10 VSS	N11 VSS	N12 VSS	N13 VSS			N16 VDDCORE	N17 PD5	N18 PD4	N19 VDDm	N20 PD1
P1 PANELVS	P2 PANELHS	P3 ROMA15 PANELD23	P4 ROMA14 PANELD22	P5 N/C											P16 N/C	P17 VSS	P18 AD1	P19 AD0	P20 PD0
R1 AB	R2 AVSS	R3 REGINA	R4 REGOUTA	R5 VDDCORE											R16 N/C	R17 AD4	R18 AD3	R19 VDDq	R20 AD2
T1 RSET	T2 AR	T3 AG	T4 AVDD	T5 N/C	T6 N/C	T7 VDDd	T8 VSS	T9 VSS	T10 VREFB	T11 VDDqCOMP	T12 VDDCORE	T13 VDDCORE	T14 VDDd	T15 N/C	T16 N/C	T17 AD5	T18 AD7	T19 AD6	T20 AD_STB0
U1 CLKAVDD2	U2 CLKAVSS	U3 AVSS	U4 AVDD	U5 GNT	U6 RBF IDSEL	U7 SBA0	U8 VSS	U9 SBA5	U10 AD31	U11 VSS	U12 AD24	U13 AD23	U14 VSS	U15 AD18	U16 IRDY	U17 VSS	U18 AD8	U19 C/BE0	U20 AD_STB0
V1 CLKAVSS	V2 CLKAVDD1	V3 CLKAVSS	V4 SCLK	V5 ST0	V6 PIPE	V7 SBA1	V8 SB_STB	V9 SBA6	V10 AD30	V11 AD27	V12 AD_STB1	V13 AD_STB1	V14 AD19	V15 C/BE2	V16 FRAME	V17 STOP	V18 AD15	V19 AD10	V20 AD9
W1 XOUT	W2 CLKAVDD3	W3 HSYNC	W4 RESET	W5 ST1	W6 VDDq	W7 SBA2	W8 SB_STB	W9 VDDq	W10 AD29	W11 AD26	W12 VDDq	W13 AD21	W14 AD20	W15 VDDq	W16 DEVSEL	W17 PAR	W18 VDDq	W19 AD12	W20 AD11
Y1 XIN	Y2 VSYNC	Y3 INTA	Y4 REQ	Y5 ST2	Y6 N/C	Y7 SBA3	Y8 SBA4	Y9 SBA7	Y10 AD28	Y11 AD25	Y12 C/BE3	Y13 AD22	Y14 AD17	Y15 AD16	Y16 TRDY	Y17 C/BE1	Y18 AD14	Y19 AD13	Y20 VSS

Figure 3-1. Add-in Card Pinout (Top View)

Note: VDDx = 3.3V (except VDDq may be 1.5V); VDDCORE = 2.5V

3.2 PIN DESCRIPTIONS (ALL Savage4 FAMILY PARTS)

The following table provides a brief description of each pin. Where two output drive strengths are given, the value is programmable. The following abbreviations are used for pin types.

I - Input signal
O - Output signal
B - Bidirectional signal

Table 3-1. Pin Descriptions

Symbol	Type	Drive (mA)	Description
AGP BUS INTERFACE			
AD[31:0]	B	24/16/8/4	Multiplexed Address/Data Bus. A bus transaction (cycle) consists of an address phase followed by one or more data phases. 16 mA is the AGP default. Other drives can be selected via CR80_1-0.
$\overline{\text{C/BE[3:0]}}$	B	24/16/8/4	Bus Command/Data Byte Enables. These signals carry the bus command during the address phase and the byte enables during the data phase. 16 mA is the default drive. Other drives can be selected via CR80_1-0.
SCLK	I		AGP System Clock. This input drives the internal AGP PLL.
$\overline{\text{INTA}}$	O	24/16/8/4	Interrupt Request. If ROMD0 is strapped high at reset (clearing CR36_0 to 0), no interrupt will be requested during PCI configuration. 16 mA is the default drive. Other drives can be selected via CR80_1-0.
$\overline{\text{IRDY}}$	B	24/16/8/4	Initiator Ready. This signal is an input when an external bus master has control of the AGP Bus and an output for bus master AGP operation. 16 mA is the default drive. Other drives can be selected via CR80_1-0. Internally pulled up.
$\overline{\text{TRDY}}$	B	24/16/8/4	Target Ready. This signal is an output when an external bus master has control of the AGP Bus and an input for bus master AGP operation. 16 mA is the default drive. Other drives can be selected via CR80_1-0. Internally pulled up.
$\overline{\text{RESET}}$	I		System Reset. Asserting this signal forces the registers and state machines to a known state.
$\overline{\text{REQ}}$	O	24/16/8/4	Request. This signal is asserted to request control of the AGP Bus for bus master DMA operation. 16 mA is the default drive. Other drives can be selected via CR80_1-0.
$\overline{\text{GNT}}$	I		Grant. Assertion of this signal grants control of the AGP Bus for bus master DMA operation.
ST[2:0]	I		Status Bus. Tie to VSS for PCI configurations.
SBA[7:0]	O	8/16	Side Band Address Bus. 8 mA is the default drive. 16 mA is selected via CR80_2 = 1.
SB_STB	O	8/16	Side Band Address Strobe. 8 mA is the default drive. 16 mA is selected via CR80_2 = 1. Internally pulled up.
$\overline{\text{SB\_STB}}$	O	8/16	Differential Side Band Address Strobe. 8 mA is the default drive. 16 mA is selected via CR80_2 = 1. Internally pulled down.
AD_STB[1:0]	B	24/16/8/4	Strobes for AD Bus. 16 mA is the default drive. Other drives can be selected via CR80_1-0. Internally pulled up.
$\overline{\text{AD\_STB[1:0]}}$	B	24/16/8/4	Differential Strobes for AD Bus. 16 mA is the default drive. Other drives can be selected via CR80_1-0. Internally pulled down.
$\overline{\text{RBF}}$	O	24/16/8/4	Read Buffer Full. 16 mA is the default drive. Other drives can be selected via CR80_1-0.
$\overline{\text{PIPE}}$	O	24/16/8/4	Pipelined Request. 16 mA is the default drive. Other drives can be selected via CR80_1-0. Internally pulled up.
VDDqCOMP	I		VDDq Compensation. Connected to VDDq via a 237Ω or 243Ω resistor. Can be tied to VSS for 3.3V VDDq-only or PCI configurations.

Table 3-1. Pin Descriptions (continued)

Symbol	Type	Drive (mA)	Description
PCI BUS INTERFACE			
AD[31:0]	B	24/16/8/4	Multiplexed Address/Data Bus. 24 mA is the default drive. Other drives can be selected via CR80_1-0.
$\overline{\text{C/BE}}$[3:0]	B	24/16/8/4	Bus Command/Data Byte Enables. These signals carry the bus command during the address phase and the byte enables during the data phase. 24 mA is the default drive. Other drives can be selected via CR80_1-0.
SCLK	I		PCI System Clock.
$\overline{\text{INTA}}$	O	24/16/8/4	Interrupt Request. If ROMD0 is strapped high at reset (clearing CR36_0 to 0), no interrupt will be requested during PCI configuration. 24 mA is the default drive. Other drives can be selected via CR80_1-0.
$\overline{\text{IRDY}}$	B	24/16	Initiator Ready. This signal is an input when an external bus master has control of the PCI Bus and an output for bus master PCI operation. 24 mA is the default drive. Other drives can be selected via CR80_1-0. Internally pulled up.
$\overline{\text{TRDY}}$	B	24/16	Target Ready. This signal is an output when an external bus master has control of the PCI Bus and an input for bus master PCI operation. 24 mA is the default drive. Other drives can be selected via CR80_1-0. Internally pulled up.
$\overline{\text{DEVSEL}}$	B	24/16	Device Select. This signal is an output when an external bus master has control of the PCI Bus and an input for bus master PCI operation. 24 mA is the default drive. Other drives can be selected via CR80_1-0. Internally pulled up.
IDSEL	I		Initialization Device Select. This input is the chip select for PCI configuration register reads/writes.
$\overline{\text{RESET}}$	I		System Reset. Assertion forces the registers/state machines to a known state.
$\overline{\text{FRAME}}$	B	24/16	Cycle Frame. This signal is an input when an external bus master has control of the PCI Bus and an output for bus master PCI operation. 24 mA is the default drive. Other drives can be selected via CR80_1-0. Internally pulled up.
PAR	B	24/16	Parity. This signal is an output from the bus master during writes and an input to the bus master during reads. 24 mA is the default drive. Other drives can be selected via CR80_1-0.
$\overline{\text{STOP}}$	B	24/16	Stop. This signal is an input to the bus master from the target indicating a request to stop the current transaction. 24 mA is the default drive. Other drives can be selected via CR80_1-0. Internally pulled up.
$\overline{\text{REQ}}$	O	24/16	Request. Assertion requests control of the PCI Bus for bus master DMA operation. 24 mA is the default drive. Other drives can be selected via CR80_1-0.
$\overline{\text{GNT}}$	I		Grant. Assertion of this signal grants control of the PCI Bus for bus master DMA operation.
CLOCK CONTROL AND INPUT			
XIN	I		Reference Frequency Input. An external 14.318 MHz crystal is connected between XOUT and this pin. Alternately, an external oscillator can be connected.
XOUT	O		Crystal Output. This pin drives the crystal via an internal oscillator. If an external oscillator is connected to XIN, this pin can be left unconnected.

Table 3-1. Pin Descriptions (Continued)

Symbol	Type	Drive (mA)	Description
DISPLAY MEMORY INTERFACE			
MA[10:0]	O	16/8	Memory Address Bus. The video memory row and column addresses are multiplexed on these lines. See Section 7 of the Savage4 Hardware Reference for the required connections to various types of memory. MA8 always connects to the Auto Precharge pin on the memory. 16 mA is the default drive. 8 mA is selected via CR80_5 = 1. Internally pulled up.
PD[63:0]	B	16/8	Display Memory Pixel Data Bus Lines 63:0. 16 mA is the default drive. 8 mA is selected via CR80_4 = 1. Internally pulled up.
SDCLK1	O	24/16	Clock for lower half of memory (up to 4 chips). 24 mA is the default drive. 16 mA is selected via CR80_7 = 1. Internally pulled down.
SDCLK2	O	24/16	Clock for upper half of memory. 24 mA is the default drive. 16 mA is selected via CR80_7 = 1. Internally pulled down.
SDCLKR1	I		Return SDCLK. See SDCLKOUT. This delayed clock return is used to latch read data.
SDCLKR2	I		Return SDCLK. See SDCLKOUT. This delayed clock return is used to latch read data.
SDCLKOUT	O		Dummy Clock Output. This signal is looped back to the two SDCLKR inputs to control read data latching timing.
$\overline{RAS}$	O	16/8	Row Address Strobe. 16 mA is the default drive. 8 mA is selected via CR80_6 = 1. Internally pulled up.
$\overline{CAS}$	O	16/8	Column Address Strobe. 16 mA is the default drive. 8 mA is selected via CR80_6 = 1. Internally pulled up.
DQM[7:0]	O	16/8	Data Input/Output Masks. 16 mA is the default drive. 8 mA is selected via CR80_6 = 1. Internally pulled up.
$\overline{CS}$[3:0]	O	16/8	Chip Selects. The functions of these signals change depending on the memory type. See Section 7 of the Savage4 Hardware Reference. 16 mA is the default drive. 8 mA is selected via CR80_6 = 1. Internally pulled up.
$\overline{WE}$	O	16/8	Write Enable. Default drive is 16 mA. 8 mA is selected via CR80_6 = 1. Internally pulled up.
DSF	O	16/8	Special Function. (SGRAM) 16 mA is the default drive. 8 mA is selected via CR80_6 = 1. Internally pulled up.
CRT INTERFACE			
RSET			Reference Resistor. Tie to AVSS through an external 140Ω resistor to control the RAMDAC full-scale current value.
AR	O		Analog Red. Analog red output to the CRT monitor.
AB	O		Analog Blue. Analog blue output to the CRT monitor.
AG	O		Analog Green. Analog green output to the CRT monitor.
HSYNC	O		Horizontal Sync. Output to CRT.
VSYNC	O		Vertical Sync. Output to CRT.
TFT FLAT PANEL INTERFACE			
PANELD[23:0]	O	8/16	Panel Data. Internally pulled down during reset. 8 mA is the default (4 mA for Rev. A). 16 mA is selected via SR3D_6 = 1 (8 mA for Rev. A).
PANELVS	O		Panel VSYNC. Internally pulled down.
PANELHS	O		Panel HSYNC. Internally pulled down.
PANELCLK	O	8/16	Panel Clock. Internally pulled down. 8 mA is the default. 16 mA is selected via SR3D_6 = 1.
PANELDE	O		Panel Data Enable. Internally pulled down.
PANELDET	I		Panel Detect. If SR30_1 = 0, SR30_2 will read 1 if a flat panel is appropriately connected to ball N5. Must be tied to VSS is not used.

Table 3-1. Pin Descriptions (Continued)

Symbol	Type	Drive (mA)	Description
EXTERNAL TV ENCODER INTERFACE			
TVDAT[11:0]	O		TV Data. 24-bit RGB data is output on TVDAT[11:0] (two clock edges/pixel). Internally pulled down during reset.
TVCLK	I		TV Clock. Input clock from TV encoder. Internally pulled down.
TVCLKR	O		TV Return Clock. Output to TV encoder. Internally pulled down.
TVVS	O		TV VSYNC. Internally pulled down during reset.
TVHS	O		TV HSYNC. Internally pulled down during reset.
$\overline{\text{TVBLANK}}$	O		TV Blanking Signal. Internally pulled down during reset.
HDTV INTERFACE			
DCLK	O		Dot (pixel) Clock. The graphics dot clock is output on the DCLK pin when MM8188_30 = 1. This provides timing for an external high resolution TV decoder.
OVERLAY	O		Overlay. This is output on the OVERLAY pin when MM8188_30 = 1. This controls an analog MUX such that primary stream data is displayed when OVERLAY is low and high resolution RGB TV data is displayed when OVERLAY is high.
ROM INTERFACES			
$\overline{\text{ROMEN}}$	O	8	ROM Enable. This signal provides the chip enable and output enable inputs for non-programmable BIOS ROM reads. Internally pulled up.
ROMA[15:0]	O	8	ROM Address Bus. Internally pulled down during reset.
ROMD[7:0]	B	8	ROM Data Bus. Internally pulled down during reset.
$\overline{\text{FCE}}$	O	8	Flash Memory Chip Enable. Internally pulled up.
$\overline{\text{FOE}}$	O	8	Flash Memory Output Enable. Internally pulled down during reset.
$\overline{\text{FWE}}$	O	8	Flash Memory Write Enable. Internally pulled down during reset.
EPCLK	O	8	Serial EEPROM Clock. Internally pulled down during reset.
$\overline{\text{EPCS0}}$	O	8	Serial EEPROM Chip Select 0. For 1st 32K EEPROM. Internally pulled down during reset.
$\overline{\text{EPCS1}}$	O	8	Serial EEPROM Chip Select 1. For 2nd 32K EEPROM. Internally pulled down during reset.
EPSO	O	8	Serial EEPROM Data Out. Internally pulled down during reset.
EPSI	I		Serial EEPROM Data In. Internally pulled down during reset.
LOCAL PERIPHERAL BUS (LPB)			
LD[7:0]	I		LPB Data Bus. Video data input.
HREF	I		HSYNC.
VS	I		VSYNC.
LCLK	I		LPB Clock.
$\overline{\text{ODDIN}}$	I		ODD/EVEN field. Low = odd field input from the digitizer. High = even field input.
VIDEO INTERFACE PORT (VIP)			
VID[7:0]	B	8	VIP Data Bus.
HAD[1:0]	B	8	Host Address Data Bus.
HCTL	B	8	Host Control.
VIPCLK	O	16	VIP Clock.
PIXCLK	I		VIP Pixel Clock.

Table 3-1. Pin Descriptions (Continued)

Symbol	Type	Drive (mA)	Description
MISCELLANEOUS FUNCTIONS			
GOP0	O	8	General Output Port. The content of CR5C_0 is reflected on this pin. Internally pulled down during reset.
GPOUT	O	8	General Purpose Output. This pin reflects the state of SRD_0.
SPCLK[1:2]	B	8	Serial Port Clocks. These are the clocks for serial data transfer. SPCLK1 is typically used for I^2C communications. As an output, it is programmed via MMFF20_0 or CRA0_0. As an input, its status is read via MMFF20_2 or CRA0_2. In either case the serial port must be enabled by MMFF20_4 = 1 or CRA0_4 = 1. SPCLK2 is typically used for DDC monitor communications. As an output, it is programmed via CRAA_0. As an input, its status is read via CRAA_2. The port is enabled via CRAA_4 = 1.
SPD[1:2]	B	8	Serial Port Data. These are the data signals for serial data transfer. SPD1 is typically used for I^2C communications. As an output, it is programmed via MMFF20_1 or CRA0_1. As an input, its status is read via MMFF20_3 or CRA0_3. In either case the serial port must be enabled by MMFF20_4 = 1 or CRA0_4 = 1. SPD2 is typically used for DDC monitor communications. As on output, it is programmed via CRAA_1. As an input, its status is read via CRAA_3. The port is enabled via CRAA_4 = 1.
BISTON	I		This pin is used for S3 testing and must be tied to VSS on all board designs.
DFTON	I		This pin is used for S3 testing and must be tied to VSS on all board designs.
POWER AND GROUND			
VDDm	I		Digital power supply (3.3V) for memory interface
VDDq	I		Digital power supply for system bus interface. Normally 3.3V. 1.5V is optional for 2X AGP and mandatory for 4X AGP.
VDDv	I		Digital power supply (3.3V) for peripheral interface
VDDd	I		Second digital power supply for system bus interface. Always 3.3V even if VDDq is 1.5V.
VDDCORE	I		Core digital power supply (2.5V)
CLKAVDD[1:3]	I		Analog power supply for PLLs (2.5V) (1 = ECLK, 2 = MCLK, 3 = DCLK)
VSS	I		Digital ground
AVDD	I		Analog power supply (2.5V)
AVSS	I		Analog ground
CLKAVSS	I		Analog ground for PLLs
REGOUTA	O		Connect to 2.5V as shown in Section 9.8. SR1C_6 must be set to 1. This pin can be left unconnected for PCI configurations.
REGINA	I		Connect to 3.3V for future compatibility.
VREFM	I		Memory interface voltage reference. See Section 9.8 for the required connection.
VREFB	I		System bus interface voltage reference. See Section 9.8 for the required connection.

3.3 PIN LISTS (ADD-IN CARD PINOUT)

Table 3-2. Alphabetical Pin Listing (Add-in Card Pinout)

Name	Pins
AB	R1
AD_STB[1:0]	V12, U20
$\overline{\text{AD\_STB[1:0]}}$	V13, T20
AD[31:16]	U10, V10, W10, Y10, V11, W11, Y11, U12, U13, Y13, W13, W14, V14, U15, Y14, Y15
AD[15:0]	V18, Y18, Y19, W19, W20, V19, V20, U18, T18, T19, T17, R17, R18, R20, P18, P19
AG	T3
AR	T2
AVDD	T4, U4
AVSS	R2, U3
BISTON	k5
$\overline{\text{CAS}}$	A15
$\overline{\text{C/BE[3:0]}}$	Y12, V15, Y17, U19
CLKAVDD[1:3]	W2, V2, U1
CLKAVSS	U2, V1, V3
$\overline{\text{CS[3:0]}}$	C15, D15, A16, B16
DCLK	L3
$\overline{\text{DEVSEL}}$	W16
DFTON	m16
DQM[7:0]	D12, B14, A13, C14, D19, D18, D20, D17
DSF	C16
EPCLK	L3
$\overline{\text{EPCS[1:0]}}$	A2, A1
EPSI	B2
EPSO	L4
$\overline{\text{FCE}}$	A1
$\overline{\text{FOE}}$	A2
$\overline{\text{FRAME}}$	V16
$\overline{\text{FWE}}$	B2
$\overline{\text{GNT}}$	U5
GOP0	G2
GPOUT	G3
HAD[1:0]	D2, E4
HCTL	E2
HREF	D2
HSYNC	W3
IDSEL	U6
$\overline{\text{INTA}}$	Y3
$\overline{\text{IRDY}}$	U16
LCLK	F2
LD[7:0]	F3, E1, E3, D1, D3, C1, C2, B1
MA[10:0]	C19, C18, D16, A17, C17, A18, B18, A19, B20, B19, C20
N/C	A14, E7, E10, E12, E14, E15, E16, F5, F16, G5, G16, K5, P5, P16, R16, T5, T6, T15, T16, Y6
$\overline{\text{ODDIN}}$	E4
OVERLAY	L4
PANELCLK	J1
PANELD[23:0]	P3, P4, N1, N2, N3, N4, M1, M2, M3, M4, L1, L2, L3, L4, K3, K4, J2, J3, J4, H1, H2, H3, H4, G1
PANELDE	K2
PANELDET	N5
PANELHS	P2
PANELVS	P1
PAR	W17
PD[63:48]	A10, B10, A11, B11, C11, A12, B12, C12, D10, C10, D9, C9, B8, A8, C8, A7
PD[47:32]	A5, A6, B6, C6, D6, C7, D7, B7, D5, C5, C4, C3, B4, B3, A4, A3
PD[31:16]	G20, G19, F20, F19, F18, E20, E18, E17, G17, G18, H17, H18, H19, H20, J18, J20
PD[15:0]	L20, L19, K20, K19, L18, L17, K18, J17, M17, M18, N17, N18, M19, M20, N20, P20

Table 3-2. Alphabetical Pin Listing (Continued)

Name	Pins
$\overline{\text{PIPE}}$	V6
PIXCLK	F2
$\overline{\text{RAS}}$	B15
$\overline{\text{RBF}}$	U6
REGINA	R3
REGOUTA	R4
$\overline{\text{REQ}}$	Y4
$\overline{\text{RESET}}$	W4
ROMA[15:0]	P3, P4, N1, N2, N3, N4, M1, M2, M3, M4, L1, L2, L3, L4, K3, K4
ROMD[7:0]	J2, J3, J4, H1, H2, H3, H4, G1
$\overline{\text{ROMEN}}$	A1
RSET	T1
SB_STB	V8
$\overline{\text{SB\_STB}}$	W8
SBA[7:0]	Y9, V9, U9, Y8, Y7, W7, V7, U7
SCLK	V4
SDCLK[1:2]	C13, D11
SDCLKOUT	A9
SDCLKR[1:2]	K16, E8
SPCLK[1:2]	E6, F4
SPD[1:2]	E5, G4
ST[2:0]	Y5, W5, V5
$\overline{\text{STOP}}$	V17
$\overline{\text{TRDY}}$	Y16
$\overline{\text{TVBLANK}}$	L3
TVCLK	K2
TVCLKR	J1
TVDAT[11:0]	M3, M4, L1, L2, J2, J3, J4, H1, H2, H3, H4, G1
TVHS	K3
TVVS	K4
VDDCORE	E11, E13, H16, L5, N16, R5, T12, T13
VDDd	T7, T14
VDDm	B5, B9, B13, B17, E19, J19, N19
VDDq	R19, W6, W9, W12, W15, W18
VDDqCOMP	T11
VDDv	H5, J5
VID[7:0]	F3, E1, E3, D1, D3, C1, C2, B1
VIPCLK	F1
VREFB	T10
VREFM	J16
VS	E2
VSS	A20, D4, D8, D13, E9, F17, H8, H9, H10, H11, H12, H13, J8, J9, J10, J11, J12, J13, K1, K8, K9, K10, K11, K12,
	K13, K17, L8, L9, L10. L11, L12, L13, L16, M5, M8, M9, M10, M11, M12, M13, N8, N9, N10, N11, N12, N13,
	P17, T8, T9, U8, U11, U14, U17, Y20
VSYNC	Y2
$\overline{\text{WE}}$	D14
XIN	Y1
XOUT	W1

Table 3-3. Numerical Pin Listing (Add-in Card Pinout)

Name	Pins	Name	Pins
A1	ROMEN/FCE/EPCS0	C19	MA10
A2	FOE/EPCS1	C20	MA0
A3	PD32	D1	VID4/LD4
A4	PD33	D2	HREF/HAD1
A5	PD47	D3	VID3/LD3
A6	PD46	D4	VSS
A7	PD48	D5	PD39
A8	PD50	D6	PD43
A9	SDCLKOUT	D7	PD41
A10	PD63	D8	VSS
A11	PD61	D9	PD53
A12	PD58	D10	PD55
A13	DQM5	D11	SDCLK2
A14	N/C	D12	DQM7
A15	CAS	D13	VSS
A16	CS1	D14	WE
A17	MA7	D15	CS2
A18	MA5	D16	MA8
A19	MA3	D17	DQM0
A20	VSS	D18	DQM2
B1	VID0/LD0	D19	DQM3
B2	FWE/EPSI	D20	DQM1
B3	PD34	E1	VID6/LD6
B4	PD35	E2	HCTL/VS
B5	VDDm	E3	VID5/LD5
B6	PD45	E4	HAD0/ODDIN
B7	PD40	E5	SPD1
B8	PD51	E6	SPCLK1
B9	VDDm	E7	N/C
B10	PD62	E8	SDCLKR2
B11	PD60	E9	VSS
B12	PD57	E10	N/C
B13	VDDm	E11	VDDCORE
B14	DQM6	E12	N/C
B15	RAS	E13	VDDCORE
B16	CS0	E14	N/C
B17	VDDm	E15	N/C
B18	MA4	E16	N/C
B19	MA1	E17	PD24
B20	MA2	E18	PD25
C1	VID2/LD2	E19	VDDm
C2	VID1/LD1	E20	PD26
C3	PD36	F1	VIPCLK
C4	PD37	F2	PIXCLK/LCLK
C5	PD38	F3	VID7/LD7
C6	PD44	F4	SPCLK2
C7	PD42	F5	N/C
C8	PD49	F16	N/C
C9	PD52	F17	VSS
C10	PD54	F18	PD27
C11	PD59	F19	PD28
C12	PD56	F20	PD29
C13	SDCLK1	G1	ROMD0/TVDAT0/PANELD0/EPCK
C14	DQM4	G2	GOP0
C15	CS3	G3	GPOUT
C16	DSF	G4	SPD2
C17	MA6	G5	N/C
C18	MA9	G16	N/C

Table 3-3. Numerical Pin Listing (Continued)

Name	Pins	Name	Pins
G17	PD23	L9	VSS
G18	PD22	L10	VSS
G19	PD30	L11	VSS
G20	PD31	L12	VSS
H1	ROMD4/TVDAT4/PANELD4	L13	VSS
H2	ROMD3/TVDAT3/PANELD3	L16	VSS
H3	ROMD2/TVDAT2/PANELD2	L17	PD10
H4	ROMD1/TVDAT1/PANELD1/EPSO	L18	PD11
H5	VDDv	L19	PD14
H8	VSS	L20	PD15
H9	VSS	M1	ROMA9/PANELD17
H10	VSS	M2	ROMA8/PANELD16
H11	VSS	M3	ROMA7/TVDAT11/PANELD15
H12	VSS	M4	ROMA6/TVDAT10/PANELD14
H13	VSS	M5	VSS
H16	VDDCORE	M8	VSS
H17	PD21	M9	VSS
H18	PD20	M10	VSS
H19	PD19	M11	VSS
H20	PD18	M12	VSS
J1	TVCLKR/PANELCLK	M13	VSS
J2	ROMD7/TVDAT7/PANELD7	M16	DFTON (tie to VSS)
J3	ROMD6/TVDAT6/PANELD6	M17	PD7
J4	ROMD5/TVDAT5/PANELD5	M18	PD6
J5	VDDv	M19	PD3
J8	VSS	M20	PD2
J9	VSS	N1	ROMA13/PANELD21
J10	VSS	N2	ROMA12/PANELD20
J11	VSS	N3	ROMA11/PANELD19
J12	VSS	N4	ROMA10/PANELD18
J13	VSS	N5	PANELDET
J16	VREFM	N8	VSS
J17	PD8	N9	VSS
J18	PD17	N10	VSS
J19	VDDm	N11	VSS
J20	PD16	N12	VSS
K1	VSS	N13	VSS
K2	PANELDE/TVCLK	N16	VDDCORE
K3	ROMA1/TVHS/PANELD9	N17	PD5
K4	ROMA0/TVVS/PANELD8	N18	PD4
K5	BISTON (tie to VSS)	N19	VDDm
K8	VSS	N20	PD1
K9	VSS	P1	PANELVS
K10	VSS	P2	PANELHS
K11	VSS	P3	ROMA15/PANELD23
K12	VSS	P4	ROMA14/PANELD22
K13	VSS	P5	N/C
K16	SDCLKR1	P16	N/C
K17	VSS	P17	VSS
K18	PD9	P18	AD1
K19	PD12	P19	AD0
K20	PD13	P20	PD0
L1	ROMA5/TVDAT9/PANELD13	R1	AB
L2	ROMA4/TVDAT8/PANELD12	R2	AVSS
L3	ROMA3/$\overline{\text{TVBLANK}}$/PANELD11/EPCLK/DCLK	R3	REGINA
L4	ROMA2/PANELD10/EPSO/OVERLAY	R4	REGOUTA
L5	VDDCORE	R5	VDDCORE
L8	VSS	R16	N/C

Table 3-3. Numerical Pin Listing (Continued)

Name	Pins	Name	Pins
R17	AD4	V9	SBA6
R18	AD3	V10	AD30
R19	VDDq	V11	AD27
R20	AD2	V12	AD_STB1
T1	RSET	V13	$\overline{\text{AD\_STB1}}$
T2	AR	V14	AD19
T3	AG	V15	$\overline{\text{C/BE2}}$
T4	AVDD	V16	$\overline{\text{FRAME}}$
T5	N/C	V17	$\overline{\text{STOP}}$
T6	N/C	V18	AD15
T7	N/C	V19	AD10
T8	VSS	V20	AD9
T9	VSS	W1	XOUT
T10	VREFB	W2	CLKAVDD3
T11	VDDqCOMP	W3	HSYNC
T12	VDDCORE	W4	$\overline{\text{RESET}}$
T13	VDDCORE	W5	ST1
T14	N/C	W6	VDDq
T15	N/C	W7	SBA2
T16	N/C	W8	$\overline{\text{SB\_STB}}$
T17	AD5	W9	VDDq
T18	AD7	W10	AD29
T19	AD6	W11	AD26
T20	$\overline{\text{AD\_STB0}}$	W12	VDDq
U1	CLKAVDD2	W13	AD21
U2	CLKAVSS	W14	AD20
U3	AVSS	W15	VDDq
U4	AVDD	W16	$\overline{\text{DEVSEL}}$
U5	$\overline{\text{GNT}}$	W17	PAR
U6	$\overline{\text{RBF}}$/IDSEL	W18	VDDq
U7	SBA0	W19	AD12
U8	VSS	W20	AD11
U9	SBA5	Y1	XIN
U10	AD31	Y2	VSYNC
U11	VSS	Y3	$\overline{\text{INTA}}$
U12	AD24	Y4	$\overline{\text{REQ}}$
U13	AD23	Y5	ST2
U14	VSS	Y6	WBF
U15	AD18	Y7	SBA3
U16	$\overline{\text{IRDY}}$	Y8	SBA4
U17	VSS	Y9	SBA7
U18	AD8	Y10	AD28
U19	$\overline{\text{C/BE0}}$	Y11	AD25
U20	AD_STB0	Y12	$\overline{\text{C/BE3}}$
V1	CLKAVSS	Y13	AD22
V2	CLKAVDD1	Y14	AD17
V3	CLKAVSS	Y15	AD16
V4	SCLK	Y16	$\overline{\text{TRDY}}$
V5	ST0	Y17	$\overline{\text{C/BE1}}$
V6	$\overline{\text{PIPE}}$	Y18	AD14
V7	SBA1	Y19	AD13
V8	SB_STB	Y20	VSS

3.4 MOTHERBOARD PINOUT DIAGRAM

A1 N/C	A2 N/C	A3 N/C	A4 PD35	A5 PD39	A6 PD46	A7 PD43	A8 PD40	A9 N/C	A10 PD51	A11 PD53	A12 N/C	A13 PD54	A14 PD59	A15 PD57	A16 DQM7	A17 N/C	A18 DQM4	A19 CS3	A20 DSF	A21 MA6	A22 N/C	A23 VSS
B1 N/C	B2 N/C	B3 PD32	B4 PD34	B5 PD37	B6 VDDm	B7 PD45	B8 PD48	B9 PD41	B10 VDDm	B11 PD52	B12 PD63	B13 PD55	B14 SDCLK2	B15 VDDm	B16 DQM5	B17 DQM6	B18 RAS	B19 CS0	B20 VDDm	B21 MA3	B22 MA0	B23 N/C
C1 VID3 LD3	C2 VID2 LD2	C3 ROMEN FCE EPCS0	C4 FWE EPSI	C5 PD36	C6 PD47	C7 SPD1	C8 PD44	C9 PD42	C10 PD50	C11 SDCLKOUT	C12 PD62	C13 PD61	C14 PD58	C15 PD56	C16 SDCLK1	C17 CAS	C18 CS1	C19 MA7	C20 MA4	C21 MA1	C22 MA10	C23 N/C
D1 VID4 LD4	D2 HAD1 HREF	D3 VID1 LD1	D4 VSS	D5 FOE EPCS1	D6 PD33	D7 PD38	D8 SPCLK1	D9 VSS	D10 SDCLKR2	D11 PD49	D12 VDDCORE	D13 PD60	D14 VDDCORE	D15 VSS	D16 WE	D17 CS2	D18 MA8	D19 MA5	D20 MA2	D21 MA9	D22 DQM3	D23 N/C
E1 VID6 LD6	E2 VID5 LD5	E3 HAD0 ODDIN	E4 VID0 LD0																E20 DQM1	E21 DQM2	E22 PD26	E23 PD24
F1 VIPCLK	F2 PIXCLK LCLK	F3 SPCLK2	F4 HCTL VS																F20 DQM0	F21 PD25	F22 VDDm	F23 PD28
G1 GOP0	G2 GPOUT	G3 SPD2	G4 VID7 LD7																G20 VSS	G21 PD29	G22 PD27	G23 PD30
H1 ROMD3 TVDAT3 PANELD3	H2 ROMD2 TVDAT2 PANELD2	H3 ROMD0 TVDAT0 PANELD0	H4 VDDv																H20 VDDCORE	H21 PD31	H22 PD23	H23 PD19
J1 ROMD6 TVDAT6 PANELD6	J2 ROMD5 TVDAT5 PANELD5	J3 ROMD4 TVDAT4 PANELD4	J4 ROMD1 TVDAT1 PANELD1					J9 VSS	J10 VSS	J11 VSS	J12 VSS	J13 VSS	J14 VSS	J15 VSS					J20 PD22	J21 PD18	J22 PD20	J23 PD21
K1 ROMA0 TVVS PANELD8	K2 BISTON (tie to VSS)	K3 TVCLKR PANELCLK	K4 ROMD7 TVDAT7 PANELD7					K9 VSS	K10 VSS	K11 VSS	K12 VSS	K13 VSS	K14 VSS	K15 VSS					K20 SDCLKR1	K21 PD16	K22 VDDm	K23 PD17
L1 VSS	L2 ROMA2 PANELD10 EPSO OVERLAY	L3 TVCLK PANELDE	L4 ROMA1 TVHS PANELD9					L9 VSS	L10 VSS	L11 VSS	L12 VSS	L13 VSS	L14 VSS	L15 VSS					L20 VSS	L21 PD8	L22 VREFM	L23 PD13
M1 ROMA5 TVDAT9 PANELD13	M2 ROMA4 TVDAT8 PANELD12	M3 ROMA3 TVBLANK PANELD11 EPCLK DCLK	M4 VDDv					M9 VSS	M10 VSS	M11 VSS	M12 VSS	M13 VSS	M14 VSS	M15 VSS					M20 PD12	M21 PD9	M22 PD15	M23 PD14
N1 ROMA6 TVDAT10 PANELD14	N2 ROMA7 TVDAT11 PANELD15	N3 ROMA8 PANELD16	N4 VDDCORE					N9 VSS	N10 VSS	N11 VSS	N12 VSS	N13 VSS	N14 VSS	N15 VSS					N20 N/C	N21 PD11	N22 PD10	N23 PD2
P1 ROMA9 PANELD17	P2 ROMA10 PANELD18	P3 ROMA11 PANELD19	P4 ROMA13 PANELD21					P9 VSS	P10 VSS	P11 VSS	P12 VSS	P13 VSS	P14 VSS	P15 VSS					P20 DFTON (tie to VSS)	P21 PD7	P22 PD6	P23 PD3
R1 ROMA12 PANELD20	R2 ROMA14 PANELD22	R3 ROMA15 PANELD23	R4 PANELVS					R9 VSS	R10 VSS	R11 VSS	R12 VSS	R13 VDDCORE	R14 VDDCORE	R15 VSS					R20 PD5	R21 PD4	R22 VDDm	R23 PD1
T1 PANELHS	T2 PANELDET	T3 AVSS	T4 VDDCORE																T20 VDDCORE	T21 VSS	T22 N/C	T23 PD0
U1 N/C	U2 REGOUTA	U3 AVDD	U4 AVDD																U20 VDDd	U21 N/C	U22 N/C	U23 N/C
V1 REGINA	V2 CLKAVSS	V3 AB	V4 AVSS																V20 N/C	V21 N/C	V22 N/C	V23 N/C
W1 CLKAVDD2	W2 AG	W3 AD5	W4 AD_STB0																W20 N/C	W21 N/C	W22 VDDq	W23 N/C (Note 3)
Y1 AR	Y2 RSET	Y3 AD3	Y4 AD7	Y5 AD_STB0	Y6 AD8	Y7 AD11	Y8 VSS	Y9 C/BE1	Y10 N/C	Y11 VSS	Y12 AD17	Y13 VDDqCOMP	Y14 VSS	Y15 AD29	Y16 VDDd	Y17 VSS	Y18 SB_STB	Y19 N/C	Y20 VSS	Y21 PIPE	Y22 INTA	Y23 VREFB
AA1 CLKAVSS	AA2 CLKAVDD1	AA3 CLKAVDD3	AA4 VDDq	AA5 AD6	AA6 AD12	AA7 AD14	AA8 AD13	AA9 STOP	AA10 IRDY	AA11 C/BE2	AA12 AD21	AA13 C/BE3	AA14 AD23	AA15 AD24	AA16 AD31	AA17 SBA6	AA18 SBA5	AA19 SB_STB	AA20 RBF IDSEL	AA21 GNT	AA22 REQ	AA23 SCLK
AB1 XOUT	AB2 CLKAVSS	AB3 HSYNC	AB4 AD1	AB5 C/BE0	AB6 VDDq	AB7 AD10	AB8 AD15	AB9 VDDq	AB10 AD18	AB11 DEVSEL	AB12 VDDq	AB13 AD25	AB14 AD_STB1	AB15 VDDq	AB16 AD30	AB17 SBA4	AB18 VDDq	AB19 SBA1	AB20 ST2	AB21 VDDq	AB22 ST0	AB23 RESET
AC1 XIN	AC2 VSYNC	AC3 AD4	AC4 AD0	AC5 AD2	AC6 AD9	AC7 PAR	AC8 FRAME	AC9 TRDY	AC10 AD16	AC11 AD20	AC12 AD19	AC13 AD22	AC14 AD_STB1	AC15 AD27	AC16 AD26	AC17 AD28	AC18 SBA0	AC19 SBA2	AC20 SBA3	AC21 SBA7	AC22 N/C	AC23 ST1

Figure 3-2. Motherboard Pinout (Top View)

Note

1 VDDx = 3.3V (except VDDq may be 1.5V); VDDCORE = 2.5V

2. The BIOS ROM interface signals shown are not required for a motherboard implementation and are not supported. However, most of the ROM pins are included in the NAND tree scan and need to be brought out on the board to allow a complete scan test. See Section 5.

3. For compatibility with a future S3 chip, pin W23 should be connected to the $\overline{\text{WBF}}$ pin on the chip set.

3.5 PIN LISTS (MOTHERBOARD CARD PINOUT)

Table 3-4. Alphabetical Pin Listing (Motherboard Card Pinout)

Name	Pins
AB	V3
AD_STB[1:0]	AB14, Y5
$\overline{\text{AD\_STB}}$[1:0]	AC14, W4
AD[31:16]	AA16, AB16, Y15, AC17, AC15, AC16, AB13, AA15, AA14, AC13, AA12, AC11, AC12, AB10, Y12, AC10
AD[15:0]	AB8, AA7, AA8, AA6, Y7, AB7, AC6, Y6, Y4, AA5, W3, AC3, Y3, AC5, AB4, AC4
AG	W2
AR	Y1
AVDD	U3, U4
AVSS	T3, V4
BISTON	K2
$\overline{\text{CAS}}$	C17
$\overline{\text{C/BE}}$[3:0]	AA13, AA11, Y9, AB5
CLKAVDD[1:3]	AA2, W1, AA3
CLKAVSS	V2, AA1, AB2
$\overline{\text{CS}}$[3:0]	A19, D17, C18, B19
DCLK	M3
$\overline{\text{DEVSEL}}$	AB11
DFTON	P20
DQM[7:0]	A16, B17, B16, A18, D22, E21, E20, F20
DSF	A20
EPCLK	M3
$\overline{\text{EPCS}}$[1:0]	D5, C3
EPSI	C4
EPSO	L2
$\overline{\text{FCE}}$	C3
$\overline{\text{FOE}}$	D5
$\overline{\text{FRAME}}$	AC8
$\overline{\text{FWE}}$	C4
$\overline{\text{GNT}}$	AA21
GOP0	G1
GPOUT	G2
HAD[1:0]	D2, E3
HCTL	F4
HREF	D2
HSYNC	AB3
IDSEL	AA20
$\overline{\text{INTA}}$	Y22
$\overline{\text{IRDY}}$	AA10
LCLK	F2
LD[7:0]	G4, E1, E2, D1, C1, C2, D3, E4
MA[10:0]	C22, D21, D18, C19, A21, D19, C20, B21, D20, C21, B22
N/C	A1, A2, A3, A9, A12, A17, A22, B1, B2, B23, C23, D23, N20, T22, U1, U21, U22, U23, V20, V21, V22,
	V23, W20, W21, W23, Y10, Y19, AC22
$\overline{\text{ODDIN}}$	E3
OVERLAY	L2
PANELCLK	K3
PANELD[23:0]	R3, R2, P4, R1, P3, P2, P1, N3, N2, N1, M1, M2, M3, L2, L4, K1, K4, J1, J2, J3, H1, H2, J4, H3
PANELDE	L3
PANELDET	T2
PANELHS	T1
PANELVS	R4
PAR	AC7
PD[63:48]	B12, C12, C13, D13, A14, C14, A15, C15, B13, A13, A11, B11, A10, C10, D11, B8
PD[47:32]	C6, A6, B7, C8, A7, C9, B9, A8, A5, D7, B5, C5, A4, B4, D6, B3
PD[31:16]	H21, G23, G21, F23, G22, E22, F21, E23, H22, J20, J23, J22, H23, J21, K23, K21

Table 3-4. Alphabetical Pin Listing (Motherboard Pinout) Continued

Name	Pins
PD[15:0]	M22, M23, L23, M20, N21, N22, M21, L21, P21, P22, R20, R21, P23, N23, R23, T23
$\overline{\text{PIPE}}$	Y21
PIXCLK	F2
$\overline{\text{RAS}}$	B18
$\overline{\text{RBF}}$	AA20
REGINA	V1
REGOUTA	U2
$\overline{\text{REQ}}$	AA22
$\overline{\text{RESET}}$	AB23
ROMA[15:0]	R3, R2, P4, R1, P3, P2, P1, N3, N2, N1, M1, M2, M3, L2, L4, K1
ROMD[7:0]	K4, J1, J2, J3, H1, H2, J4, H3
$\overline{\text{ROMEN}}$	C3
RSET	Y2
SB_STB	Y18
$\overline{\text{SB\_STB}}$	AA19
SBA[7:0]	AC21, AA17, AA18, AB17, AC20, AC19, AB19, AC18
SCLK	AA23
SDCLK[1:2]	C16, B14
SDCLKOUT	C11
SDCLKR[1:2]	K20, D10
SPCLK[1:2]	D8, F3
SPD[1:2]	C7, G3
ST[2:0]	AB20, AC23, AB22
$\overline{\text{STOP}}$	AA9
$\overline{\text{TRDY}}$	AC9
$\overline{\text{TVBLANK}}$	M3
TVCLK	L3
TVCLKR	K3
TVDAT[11:0]	N2, N1, M1, M2, K4, J1, J2, J3, H1, H2, J4, H3
TVHS	L4
TVVS	K1
VDDCORE	D12, D14, H20, N4, R13, R14, T4, T20
VDDd	U20, Y16
VDDm	B6, B10, B15, B20, F22, K22, R22
VDDq	W22, AA4, AB6, AB9, AB12, AB15, AB18, AB21
VDDqCOMP	Y13
VDDv	H4, M4
VID[7:0]	G4, E1, E2, D1, C1, C2, D3, E4
VIPCLK	F1
VREFB	Y23
VREFM	L22
VS	F4
VSS	A23, D4, D9, D15, G20, J9, J10, J11, J12, J13, J14, J15, K9, K10, K11, K12, K13, K14, K15, L1, L9, L10,
	L11, L12, L13, L14, L15, L20, M9, M10, M11, M12, M13, M14, M15, N9, N10, N11, N12, N13, N14, N15,
	P9, P10, P11, P12, P13, P14, P15, R9, R10, R11, R12, R15, T21, Y8, Y11, Y14, Y17, Y20
VSYNC	AC2
$\overline{\text{WE}}$	D16
XIN	AC1
XOUT	AB1

Table 3-5 Numerical Pin Listing (Motherboard Pinout)

Pin #	Name	Pin #	Name
A1	N/C	C13	PD61
A2	N/C	C14	PD58
A3	N/C	C15	PD56
A4	PD35	C16	SDCLK1
A5	PD39	C17	$\overline{CAS}$
A6	PD46	C18	$\overline{CS1}$
A7	PD43	C19	MA7
A8	PD40	C20	MA4
A9	N/C	C21	MA1
A10	PD51	C22	MA10
A11	PD53	C23	N/C
A12	N/C	D1	VID4/LD4
A13	PD54	D2	HAD1/HREF
A14	PD59	D3	VID1/LD1
A15	PD57	D4	VSS
A16	DQM7	D5	$\overline{FOE}$/$\overline{EPCS1}$
A17	N/C	D6	PD33
A18	DQM4	D7	PD38
A19	$\overline{CS3}$	D8	SPCLK1
A20	DSF	D9	VSS
A21	MA6	D10	SDCLKR2
A22	N/C	D11	PD49
A23	VSS	D12	VDDCORE
B1	N/C	D13	PD60
B2	N/C	D14	VDDCORE
B3	PD32	D15	VSS
B4	PD34	D16	$\overline{WE}$
B5	PD37	D17	$\overline{CS2}$
B6	VDDm	D18	MA8
B7	PD45	D19	MA5
B8	PD48	D20	MA2
B9	PD41	D21	MA9
B10	VDDm	D22	DQM3
B11	PD52	D23	N/C
B12	PD63	E1	VID6/LD6
B13	PD55	E2	VID5/LD5
B14	SDCLK2	E3	HAD0/$\overline{ODDIN}$
B15	VDDm	E4	VID0/LD0
B16	DQM5	E20	DQM1
B17	DQM6	E21	DQM2
B18	$\overline{RAS}$	E22	PD26
B19	$\overline{CS0}$	E23	PD24
B20	VDDm	F1	VIPCLK
B21	MA3	F2	PIXCLK/LCLK
B22	MA0	F3	SPCLK2
B23	N/C	F4	HCTL/VS
C1	VID3/LD3	F20	DQM0
C2	VID2/LD2	F21	PD25
C3	$\overline{ROMEN}$/$\overline{FCE}$/$\overline{EPCS0}$	F22	VDDm
C4	$\overline{FWE}$/EPSI	F23	PD28
C5	PD36	G1	GOP0
C6	PD47	G2	GPOUT
C7	SPD1	G3	SPD2
C8	PD44	G4	VID7/LD7
C9	PD42	G20	VSS
C10	PD50	G21	PD29
C11	SDCLKOUT	G22	PD27
C12	PD62	G23	PD30

Table 3-5. Numerical Pin Listing (Motherboard Pinout) Continued

Pin #	Name	Pin #	Name
H1	ROMD3/TVDAT3/PANELD3	M10	VSS
H2	ROMD2/TVDAT2/PANELD2	M11	VSS
H3	ROMD0/TVDAT0/PANELD0	M12	VSS
H4	VDDv	M13	VSS
H20	VDDCORE	M14	VSS
H21	PD31	M15	VSS
H22	PD23	M20	PD12
H23	PD19	M21	PD9
J1	ROMD6/TVDAT6/PANELD6	M22	PD15
J2	ROMD5/TVDAT5/PANELD5	M23	PD14
J3	ROMD4/TVDAT4/PANELD4	N1	ROMA6/TVDAT10/PANELD14
J4	ROMD1/TVDAT1/PANELD1	N2	ROMA7/TVDAT11/PANELD15
J9	VSS	N3	ROMA8/PANELD16
J10	VSS	N4	VDDCORE
J11	VSS	N9	VSS
J12	VSS	N10	VSS
J13	VSS	N11	VSS
J14	VSS	N12	VSS
J15	VSS	N13	VSS
J20	PD22	N14	VSS
J21	PD18	N15	VSS
J22	PD20	N20	N/C
J23	PD21	N21	PD11
K1	ROMA0/TVVS/PANELD8	N22	PD10
K2	BISTON (tie to VSS)	N23	PD2
K3	TVCLKR/PANELCLK	P1	ROMA9/PANELD17
K4	ROMD7/TVDAT7/PANELD7	P2	ROMA10/PANELD18
K9	VSS	P3	ROMA11/PANELD19
K10	VSS	P4	ROMA13/PANELD21
K11	VSS	P9	VSS
K12	VSS	P10	VSS
K13	VSS	P11	VSS
K14	VSS	P12	VSS
K15	VSS	P13	VSS
K20	SDCLKR1	P14	VSS
K21	PD16	P15	VSS
K22	VDDm	P20	DFTON (tie to VSS)
K23	PD17	P21	PD7
L1	VSS	P22	PD6
L2	ROMA2/PANELD10/EPSO/OVERLAY	P23	PD3
L3	TVCLK/PANELDE	R1	ROMA12/PANELD20
L4	ROMA1/TVHS/PANELD9	R2	ROMA14/PANELD22
L9	VSS	R3	ROMA15/PANELD23
L10	VSS	R4	PANELVS
L11	VSS	R9	VSS
L12	VSS	R10	VSS
L13	VSS	R11	VSS
L14	VSS	R12	VSS
L15	VSS	R13	VDDCORE
L20	VSS	R14	VDDCORE
L21	PD8	R15	VSS
L22	VREFM	R20	PD5
L23	PD13	R21	PD4
M1	ROMA5/TVDAT9/PANELD13	R22	VDDm
M2	ROMA4/TVDAT8/PANELD12	R23	PD1
M3	ROMA3/PANELD11/$\overline{\text{TVBLANK}}$/EPCLK/DCLK	T1	PANELHS
M4	VDDv	T2	PANELDET
M9	VSS	T3	AVSS

Table 3-5. Numerical Pin Listing (Motherboard Pinout) Continued

Pin #	Name	Pin #	Name
T4	VDDCORE	AA7	AD14
T20	VDDCORE	AA8	AD13
T21	VSS	AA9	STOP
T22	N/C	AA10	IRDY
T23	PD0	AA11	C/BE2
U1	N/C	AA12	AD21
U2	REGOUTA	AA13	C/BE3
U3	AVDD	AA14	AD23
U4	AVDD	AA15	AD24
U20	VDDd	AA16	AD31
U21	N/C	AA17	SBA6
U22	N/C	AA18	SBA5
U23	N/C	AA19	SB_STB
V1	REGINA	AA20	RBF/IDSEL
V2	CLKAVSS	AA21	GNT
V3	AB	AA22	REQ
V4	AVSS	AA23	SCLK
V20	N/C	AB1	XOUT
V21	N/C	AB2	CLKAVSS
V22	N/C	AB3	HSYNC
V23	N/C	AB4	AD1
W1	CLKAVDD2	AB5	C/BE0
W2	AG	AB6	VDDq
W3	AD5	AB7	AD10
W4	AD_STB0	AB8	AD15
W20	N/C	AB9	VDDq
W21	N/C	AB10	AD18
W22	VDDq	AB11	DEVSEL
W23	N/C (connect to AGP WBF for future compatibility)	AB12	VDDq
Y1	AR	AB13	AD25
Y2	RSET	AB14	AD_STB1
Y3	AD3	AB15	VDDq
Y4	AD7	AB16	AD30
Y5	AD_STB0	AB17	SBA4
Y6	AD8	AB18	VDDq
Y7	AD11	AB19	SBA1
Y8	VSS	AB20	ST2
Y9	C/BE1	AB21	VDDq
Y10	N/C	AB22	ST0
Y11	VSS	AB23	RESET
Y12	AD17	AC1	XIN
Y13	VDDqCOMP	AC2	VSYNC
Y14	VSS	AC3	AD4
Y15	AD29	AC4	AD0
Y16	VDDd	AC5	AD2
Y17	VSS	AC6	AD9
Y18	SB_STB	AC7	PAR
Y19	N/C	AC8	FRAME
Y20	VSS	AC9	TRDY
Y21	PIPE	AC10	AD16
Y22	INTA	AC11	AD20
Y23	VREFB	AC12	AD19
AA1	CLKAVSS	AC13	AD22
AA2	CLKAVDD1	AC14	AD_STB1
AA3	CLKAVDD3	AC15	AD27
AA4	VDDq	AC16	AD26
AA5	AD6	AC17	AD28
AA6	AD12	AC18	SBA0

Table 3-5. Numerical Pin Listing (Motherboard Pinout) Continued

Pin #	Name
AC19	SBA2
AC20	SBA3
AC21	SBA7
AC22	N/C
AC23	ST1

Section 4: Electrical Data

4.1 MAXIMUM RATINGS

Table 4-1. Absolute Maximum Ratings

Storage temperature	-40° C to 125° C
DC Supply Voltage	VDD + 10%
I/O Pin Voltage with respect to V_{SS}	-0.5V to V_{DD}+0.5V

Warning: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

4.2 DC SPECIFICATIONS

Table 4-2. Digital DC Specifications

In this table, VDDx can be VDDm, VDDv and VDDq @ 3.3V and VDDq at 1.5V)

Symbol	Parameter	Min	Max	Unit
V_{IL}	Input Low Voltage	-0.5	0.3 VDDx	V
V_{IH}	Input High Voltage	0.5 VDDx	VDDx + 0.5	V
V_{OL1}	Output Low Voltage		0.15 VDDx	V
V_{OH1}	Output High Voltage	0.65 VDDx		V
V_{OL2}	Output Low Voltage (I_{OUT} = -500 µA)		0.1 VDDx	V
V_{OH2}	Output High Voltage (I_{OUT} = 1500 µA)	0.9 VDDx		V
I_{OL}	Output Low Current @ V_{OL} max	(Note 1)		mA
I_{OH}	Output High Current @ V_{OH} min	(Note 2)		mA
I_{IL}	Input Leakage Current		±10	µA
C_{IN}	Input Capacitance		8	pF
C_{OUT}	Output Capacitance		8	pF

Notes

1. Drive strengths are given for each output in Table 3-1.
2. This value is -1 the drive level listed for each output in Table 3-1.

Table 4-3. Power Supply Current

Symbol	Parameter	Min	Max	Unit
I_{CC}	Power Supply Current (1.575V max)		20 (Notes 1, 2)	mA
I_{CC}	Power Supply Current (2.63V max)		1.2 (Notes 1, 3)	A
I_{CC}	Power Supply Current (3.47V max)		20 (Notes 1, 4))	mA

Notes

1. I_{CC} measured for a resolution of 1280x1024x16 at 75 Hz refresh. The 2D, 3D and Streams Processor functions were active. Ambient temperature was 20° C. MCLK = 143 MHz; ECLK = 100 MHz.
2. System bus interface current if VDDq = nominal 1.5V
3. Core logic current
4. I/O logic current (except for system bus I/O if VDDq = 3.3V)

Table 4-4. RAMDAC/Clock Synthesizer DC Specifications

Symbol	Parameter	Min	Typical	Max	Unit
AVDD	DAC supply voltage	2.425	2.5	2.625	V
AVDD (CLOCK)	PLL supply voltage	2.425	2.5	2.625	V
V_{OUT}	DAC full scale voltage (Note 1)	630	700	730	mV
|DNL|	Differential non-linearity (absolute value)		0.25 (Note 2)	1	LSB
|INL|	Integral non-linearity (absolute value)		0.25 (Note 2)	1	LSB

Notes

1. Condition for V_{OUT} is a 75 Ω doubly terminated load and RSET = 140 Ω. V_{OUT} varies inversely with RSET. It can also be adjusted by small increments via SR27_2-0. The output varies inversely with the value in this field. The output can also be raised by 7.6% at all levels by enabling the DAC pedestal (SR27_3 = 1).
2. The typical value is a typical maximum deviation.

4.3 AC SPECIFICATIONS

4.3.1 RAMDAC AC Specifications

Table 4-5. RAMDAC AC Specifications

Load: 75Ω doubly terminated with 80 pF load

Parameter	Typical	Max	Unit	Notes
DAC Output Rise/Fall Time	1		ns	1
DAC-to-DAC Output Skew	0		ns	2

Notes

1. Measured from 10% to 90% full scale
2. With DAC outputs equally loaded

4.3.2 Clock Timing

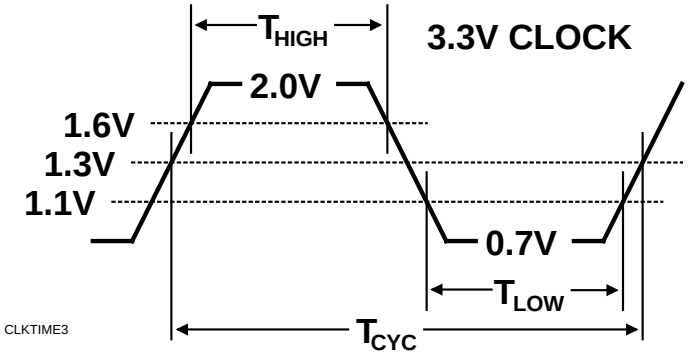


Figure 4-1. Clock Waveform Timing

Table 4-6. Clock Waveform Timing

Symbol	Parameter	Min	Max	Units	Notes
T_{CYC}	LCLK Cycle Time	25	200	ns	
	PIXCLK Cycle Time	16.7	50	ns	
	VIPCLK Cycle Time	16.7	125	ns	
	DCLK Cycle Time (VGA Mode)	25	50	ns	
	DCLK Cycle Time (Enhanced Mode)	7.4	50	ns	1
	SDCLK Cycle Time (125 MHz)	8	25	ns	
	SDCLK Cycle Time (143 MHz)	7	25	ns	
$T_{HIGH,LOW}$	LCLK High/Low Time	12	80	ns	
	PIXCLK High/Low Time	7	80	ns	
	VIPCLK High/Low Time	7	80	ns	
	SDCLK High/Low Time (125 MHz)	3.0	11	ns	
	SDCLK High/Low Time (143 MHz)	2.5	11	ns	
	Slew Rate (all clocks)	0.5	3.0	V/ns	2

Notes

1. The maximum DCLK with single clocking is 135 MHz. The maximum DCLK rate with clock doubling is 270 MHz, with two 8-bit pixels clocked into the RAMDAC each clock at 135 MHz.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.

4.3.3 Input/Output Timing

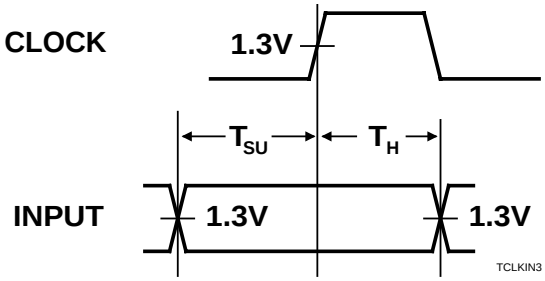


Figure 4-2. Input Timing

Table 4-7. SCLK-Referenced Input Timing (Non-AGP)

Symbol			
PCI Bus			
T_{SU}	All inputs setup	7	ns
T_H	All inputs hold	1	ns
ROM Interface			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	ROMD[7:0] setup	5	ns
T_H	ROMD[7:0] hold	2	ns

Table 4-8. LCLK-Referenced Input Timing

Digitizer Interface (Video 8)			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	LD[7:0], $\overline{ODD}$ setup	6	ns
T_H	LD[7:0], $\overline{ODD}$ hold	8	ns
T_{SU}	HREF, VS setup	6	ns
T_H	HREF, VS hold	7	ns

Table 4-9. PIXCLK-Referenced Input Timing

VIP Interface			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	VID[7:0] setup	5	ns
T_H	VID[7:0] hold	0	ns

Table 4-10. VIPCLK-Referenced Input Timing

VIP Interface			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	HAD[1:0], HCTL setup	5	ns
T_H	HAD[1:0], HCTL hold	0	ns

Table 4-11. SDCLKRx-Referenced Input Timing

Symbol	**Parameter**	**Min**	**Units**
T_{SU}	PD[63:0] setup	0.5	ns
T_H	PD[63:0] hold	2.5	ns

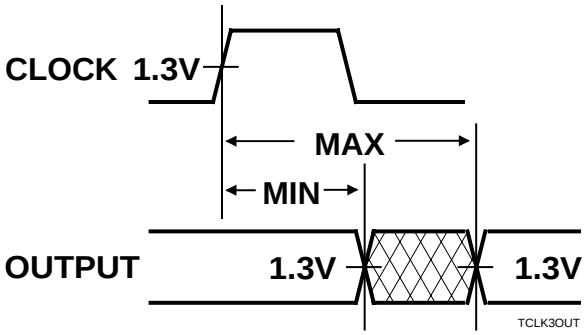


Figure 4-3. Output Timing

The minimum delay is the minimum time after the clock edge that the valid signal state from the previous cycle will begin transition to the next state (become invalid). The maximum delay is the maximum time after the clock edge that the signal is valid for the next cycle.

Table 4-12. SCLK-Referenced Output Timing (Non-AGP)

PCI Bus					
Parameter	**Min**	**Max**	**Units**	**Load (pF)**	**Notes**
All PCI signals delay	2	11	ns	50	1, 2
ROM Interface					
Parameter	**Min**	**Max**	**Units**	**Load(pF)**	**Notes**
ROMA[15:0], ROMD[7:0] valid delay	4	13	ns	30	
$\overline{FOE}$, $\overline{FWE}$, $\overline{FCE}$ delay	4	13	ns	30	

Notes

1. Delays for PCI signals are based on the 33 MHz PCI 2.2 specification.
2. Medium $\overline{DEVSEL}$ timing used

Table 4-13. VIPCLK-Referenced Output Timing

VIP Interface					
Parameter	**Min**	**Max**	**Units**	**Load (pF)**	**Notes**
HAD[1:0], HCTL delay	TBD	TBD	ns	50	

Table 4-14. SDCLKx-Referenced Output Timing

All values TBD.

Parameter	**Min**	**Max**	**Units**	**Load (pF)**	**Notes**
PD[63:0] valid delay			ns		
MA[10:0] valid delay			ns		
DQM[7:0] active, inactive delay			ns		
$\overline{RAS}$ active, inactive delay			ns		
$\overline{CAS}$ active, inactive delay			ns		
$\overline{CS}$[3:0] active, inactive delay			ns		
$\overline{WE}$ active, inactive delay			ns		

Table 4-15. TVCLKR-Referenced Output Timing

Parameter	Min	Max	Units	Load (pF)	Notes
TVDAT[11:0], TVVS, TVHS, $\overline{\text{TVBLANK}}$ delay	TBD	TBD	ns		TVCLKR is the return of the TVCLK signal from the encoder. TVCLK can be skewed via SR35_3-0 to guarantee that the outputs to the encoder meet the required setup and hold times.

Table 4-16. PANELCLK-Referenced Output Timing

All values TBD. Timings are all relative to the falling edge of PANELCLK.

Parameter	Min	Max	Units	Load (pF)	Notes
PANELD[23:0] delay			ns		
PANELVS, PANELHS, PANELDE delay			ns		

4.4 AGP AC TIMING

The AGP clock is always 66 MHz and can be either 1.5V or 3.3V (VDDq). The specifications for this clock (SCLK) are given in Tables 4-17 and 4-18.

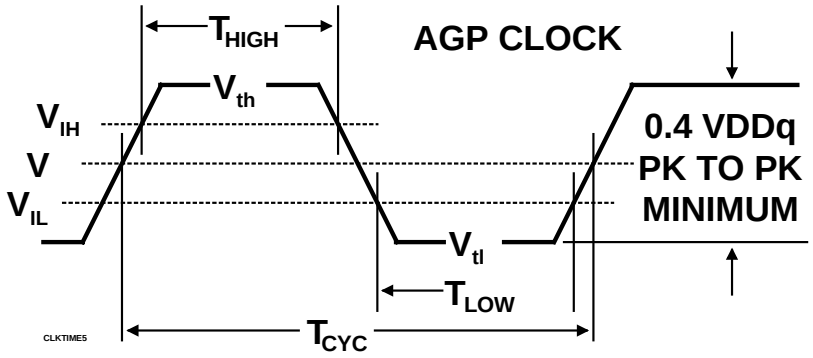


Figure 4-4. PCI/AGP Clock Specification

Table 4-17. SCLK Electrical Characteristics

Symbol	3.3V Signaling Levels	1.5V Signaling Levels	Units
Vth	0.6VDDq	0.7VDDq	V
Vtl	0.2VDDq	0.3VDDq	V
V	0.4VDDq	0.5VDDq	V

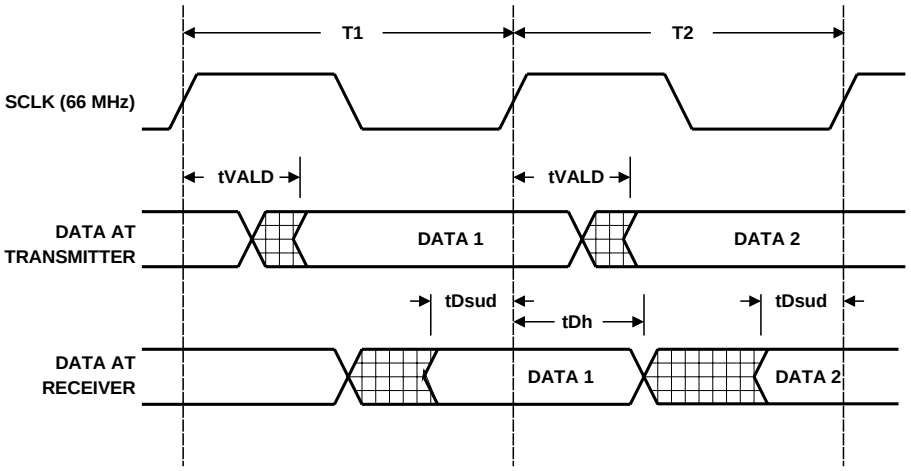


Figure 4-5. AGP 1x AC Timing

Table 4-18. AGP 1x AC Timing

Symbol	Parameter	Min	Max	Units	Notes
AGP Clock (SCLK)					
tCYC	SCLK cycle time	15	30	ns	
tHIGH	SCLK high time	6		ns	
tLOW	SCLK low time	6		ns	
	SCLK slew rate	1.5	4	V/ns	
Transmitter Output Signals					
tVALC	SCLK rising to control signal valid delay	1	5.5	ns	
tVALD	SCLK rising to data valid delay	1	6	ns	
	Output slew rate	1.5	4	V/ns	
Receiver Input Signals					
tCsu	Control signals setup time to SCLK rising	6		ns	
tCh	Control signals hold time from SCLK rising	0		ns	
tDsu	Data setup to SCLK rising	5.5		ns	
tDh	Data hold time from SCLK rising	0		ns	
$\overline{\text{RESET}}$ Signal					
	$\overline{\text{RESET}}$ active time after stable power	1		ms	
	$\overline{\text{RESET}}$ active time after SCLK stable	100		µs	
	$\overline{\text{RESET}}$ slew rate	50		mV/ns	

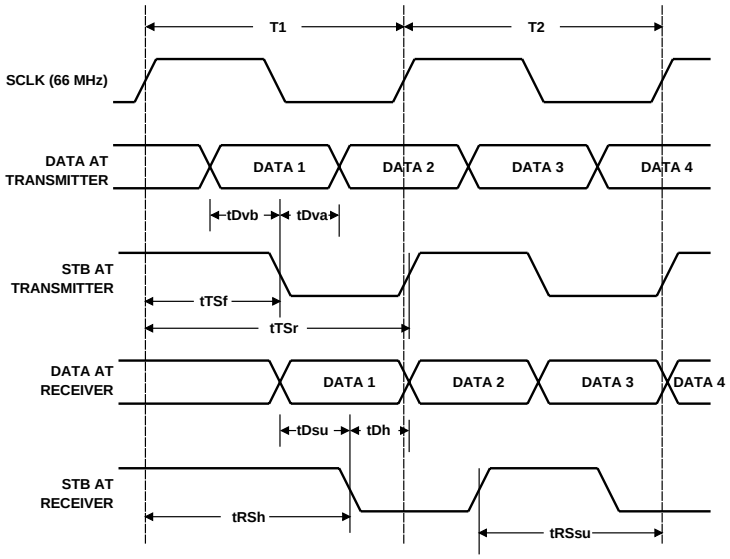


Figure 4-6. AGP 2x Timing

Table 4-19. AGP 2x AC Timing

This table applies to AD[31:0], $\overline{\text{C/BE}}$[3:0] and SBA[7:0]. For all other signals, see AGP 1x timing.

Symbol	Parameter	Min	Max	Units	Notes
Transmitter Output Signals					
tTSf	SCLK rising to transmit strobe falling	2	12	ns	
tTSr	SCLK rising to transmit strobe rising		20	ns	
	Strobe high/low	5		ns	
tDVb	Data valid before strobe falling	1.7		ns	
tDVa	Data valid after strobe falling	1.9		ns	
Receiver Input Signals					
tRSsu	Receive strobe setup time to SCLK rising	6		ns	
tRSh	Receive strobe hold time from SCLK rising	1		ns	
tDsu	Data to strobe setup time	1		ns	
tDh	Data to strobe hold time	1		ns	

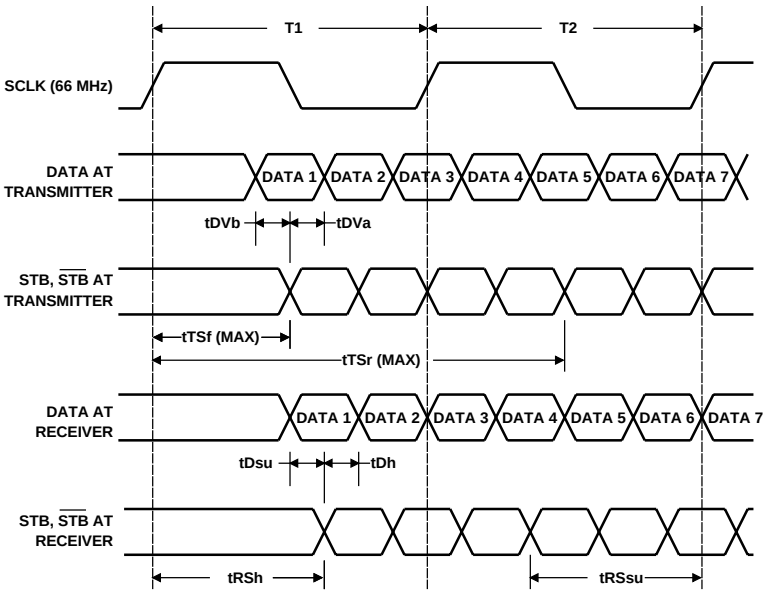


Figure 4-7. AGP 4x Timing

Table 4-20. AGP 4x AC Timing

This table applies to AD[31:0], $\overline{\text{C/BE}}$[3:0] and SBA[7:0]. For all other signals, see AGP 1x timing.

Symbol	Parameter	Min	Max	Units	Notes
Transmitter Output Signals					
tTSf	SCLK rising to first transmit strobe transition	1.9	8	ns	
tTSr	SCLK rising to fourth transmit strobe transition		20	ns	
tDVb	Data valid before strobe	-0.95		ns	
tDVa	Data valid after strobe	1.15		ns	
Receiver Input Signals					
tRSsu	Receive strobe setup time to SCLK rising	6		ns	
tRSh	Receive strobe hold time from SCLK rising	0.5		ns	
tDsu	Data to strobe setup time	0.4		ns	
tDh	Data to strobe hold time	0.7		ns	

4.5 ODD/EVEN FIELD DETECT TIMING

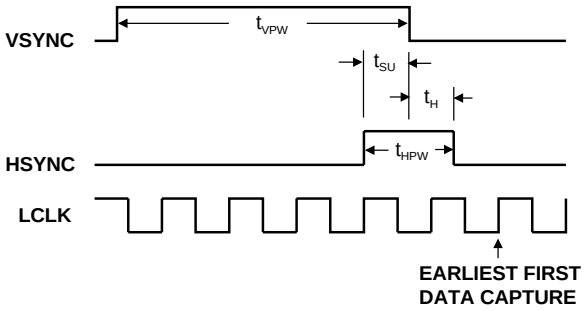


Figure 4-8. Odd/Even Field Detection Timing

Table 4-21. Odd/Even Field Detection Timing

Symbol	Parameter	Min	Max
T_{SU}	HSYNC high to VSYNC falling edge	5 ns	
T_H	HSYNC high after VSYNC falling edge	5 ns	
T_{HPW}	HSYNC pulse width	1 LCLK	6 µs
T_{VPW}	VSYNC pulse width	1 LCLK	528 µs

4.6 POWER-ON STRAPPING TIMING

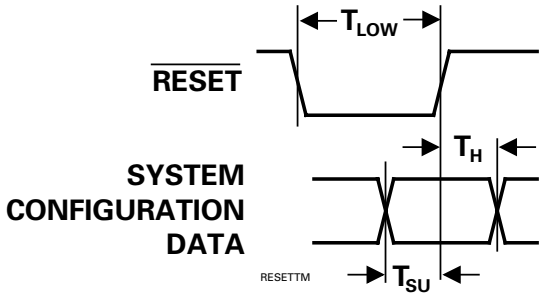


Figure 4-9. Reset Timing

Table 4-22. Reset Timing

Symbol	Parameter	Min	Units
T_{LOW}	$\overline{\text{RESET}}$ active pulse width	1000	ns
T_{SU}	Strapping pins setup to $\overline{\text{RESET}}$ inactive	20	ns
T_H	Strapping pins hold from $\overline{\text{RESET}}$ inactive	10	ns

Section 5: Reset and Testing

The $\overline{\text{RESET}}$ signal resets the internal state machines and places all registers in their power-on default states.

5.1 CONFIGURATION STRAPPING

Certain Savage4 functions have options that must be selected and fixed at reset (before the register bits controlling these functions can be programmed by software). This is accomplished via power-on configuration strapping.

The strapping pins are pulled low internally and can be individually pulled high through 10 KΩ resistors. These pull-ups and pull-downs do not affect normal operation of the pins, but they do force the pins to a definite state during reset. At the rising edge of the reset signal, this state is sampled, the result is inverted and the data loaded into the CR36, CR37 and CRB0 registers. The data is used for system configuration. The definitions of the strapping bits at the rising edge of the reset signal are shown in Table 5-1.

Important Note: As described above, the signal levels on the strapping pins are inverted before being latched in the various strapping bit registers. Since the strapping pins all have internal pull-downs, the default values for each of the strapping bits is 1. The value latched at reset can be changed to 0 by adding an external pull-up to the appropriate pin. After reset, the strapping bits are written and read normally, i.e., there is no inversion of the register values.

Table 5-1. Definition of Strapping Bits at the Rising Edge of the Reset Signal

Note: The CR Bit Values in this table are the latched values as software would read or write them. See explanation on the previous page.

In all cases below, a CR bit value of 1 is the default (no external strapping resistor). (AIC = Add-in Card; MB = Motherboard)

Pin Name	Pin # (AIC) Pin # (MB)	CR Bit(s) Value	Description
ROMD0	G1	CR36_0	**PCI Interrupt**
	H3	0	Disable $\overline{\text{INTA}}$ claim (00H in PCI3D)
		1	Enable $\overline{\text{INTA}}$ claim (01H in PCI3D)
ROMD3	H2	CR36_3	**BIOS Type**
	Not used	0	Flash BIOS ROM
		1	Non-flash BIOS ROM
ROMD4	H1	CR36_4	**I/O Disable**
	J3	0	Disable I/O access. PCI04_0 ignored.
		1	Enable I/O access via PCI04_0 = 1.
ROMD6	J3	CR37_1	**NAND Tree Test**
	N1	0	Enable NAND tree testing
		1	Normal Operation
ROMD7	J2	CR37_2	**Subsystem ID Source**
	K4	0	Read subsystem ID information from CR81-CR84
		1	Read subsystem ID information from the ROM BIOS
ROMA2	L4	CR37_5	**AGP IDSEL**
	L2	0	IDSEL connected internally to AD16 (AGP bus only - add-in card)
		1	IDSEL connected internally to AD17 (AGP bus only - motherboard)
ROMA3	L3	CR37_6	**Bus Select**
	M3	0	PCI Bus (Bus drive current = 16 mA -CR80_1-0 = 00)
		1	AGP Bus (Bus drive current = 8 mA - CR80_1-0 = 01)
ROMA4	L2	CR37_7	**AGP Signals Clock Source**
	M2	0	AGP signals driven by external SCLK
		1	AGP signals driven by internally generated clock
ROMA7	M3	CRB0_2	**EPROM Type**
	Not used	0	Serial SPI EEPROM
		1	Parallel EPROM
ROMA10	N4	CRB0_5	**Savage4 Chip Type**
	P2	0	Savage4 GT or Savage4 LT installed
		1	Savage4 Pro or Savage4 Pro-M installed
ROMA11	N3	CRB0_6	**PCI Signals Clock Source**
	P3	0	PCI signals driven by internal AGP 1x clock
		1	PCI signals driven by input on SCLK pin
ROMA12	N2	CRB0_7	**PCI Base Address Mapping**
	R1	0	Address Mapping 1 (varies by chip revision)
		1	Address Mapping 0 (PCI10, 14) (16M assigned to PCI10; 128M assigned to PCI14)

5.2 NAND TREE SCAN

NAND tree scanning is enabled when ROMD6 is pulled high at reset. Most digital pins become inputs except as noted below.

The tester drives high logic to all digital input pins. It then sequentially drives and holds each input low and records the state of the FWE pin. If all pin connections are good, the output will be a perfect square wave. If this pattern is broken, the location of the incorrect signal level in the sequence identifies the bad connection. Note that some designs may not use all the pins in the NAND tree (such as if TV out is not implemented). These pins must still all be brought out to the tester if the output is to be a perfect square wave.

The following pins are not tested:

RESET
FWE
XIN
XOUT
RSET
AR
AB
AG
VREFB
VREFM
REGINA
REGOUTA
GPOUT
GOP0
SB_STB
SB_STB
AD_STB[1:0]
AD_STB[1:0]
SDCLKR[1:2]
ROMEN
All analog and digital powers and grounds
All test pins

The connections must be tested in the signal order given in Table 5-2(add-in card part) or Table 5-3 (motherboard part). The first column is tested first, the second column next, etc.

Table 5-2. NAND-tree Scan Order (Add-in Card Pinout)

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
B1	VID0	V7	SBA1	M19	PD3	C12	PD56
C2	VID1	W7	SBA2	M20	PD2	B12	PD57
C1	VID2	Y7	SBA3	L17	PD10	A12	PD58
D3	VID3	Y8	SBA4	L18	PD11	D11	SDCLK2
D2	HAD1	U9	SBA5	L19	PD14	C11	PD59
D1	VID4	V9	SBA6	L20	PD15	B11	PD60
E4	HAD0	Y9	SBA7	K18	PD9	A11	PD61
E3	VID5	U10	AD31	K19	PD12	D10	PD55
E1	VID6	V10	AD30	K20	PD13	C10	PD54
F4	SPCLK2	W10	AD29	J17	PD8	B10	PD62
F3	VID7	Y10	AD28	J18	PD17	A10	PD63
F2	PIXCLK	V11	AD27	J20	PD16	D9	PD53
F1	VIPCLK	W11	AD26	H17	PD21	C9	PD52
E5	SPD2	Y11	AD25	H18	PD20	A9	SDCLKOUT
G1	ROMD0	U12	AD24	H19	PD19	C8	PD49
H4	ROMD1	U13	AD23	H20	PD18	B8	PD51
H3	ROMD2	Y12	$\overline{C/BE3}$	G17	PD23	A8	PD50
H2	ROMD3	W13	AD21	G18	PD22	D7	PD41
H1	ROMD4	Y13	AD22	G19	PD30	C7	PD42
J4	ROMD5	V14	AD19	G20	PD31	B7	PD40
J3	ROMD6	W14	AD20	F18	PD27	A7	PD48
J2	ROMD7	Y14	AD17	F19	PD28	E6	SPCLK1
J1	TVCLKR	U15	AD18	F20	PD29	D6	PD43
K4	ROMA0	V15	$\overline{C/BE2}$	E17	PD24	C6	PD44
K3	ROMA1	Y15	AD16	E18	PD25	B6	PD45
K2	TVCLK	U16	$\overline{IRDY}$	E20	PD26	A6	PD46
L4	ROMA2	V16	$\overline{FRAME}$	D17	DQM0	E5	SPD1
L3	ROMA3	W16	$\overline{DEVSEL}$	D18	DQM2	D5	PD39
L2	ROMA4	Y16	$\overline{TRDY}$	D19	DQM3	C5	PD38
L1	ROMA5	V17	$\overline{STOP}$	D20	DQM1	C4	PD37
M4	ROMA6	W17	PAR	C18	MA9	B4	PD35
M3	ROMA7	Y17	$\overline{C/BE1}$	C19	MA10	A4	PD33
M2	ROMA8	V18	AD15	C20	MA0	C3	PD36
M1	ROMA9	Y18	AD14	B19	MA1	B3	PD34
N4	ROMA10	W19	AD12	B20	MA2	A3	PD32
N3	ROMA11	Y19	AD13	A19	MA3	A2	$\overline{FOE}$
N2	ROMA12	W20	AD11	B18	MA4		
N1	ROMA13	V19	AD10	A18	MA5		
P4	ROMA14	V20	AD9	C17	MA6		
P3	ROMA15	U18	AD8	A17	MA7		
P2	PANELHS	U19	$\overline{C/BE0}$	D16	MA8		
P1	PANELVS	T17	AD5	C16	DSF		
N5	PANELDET	T18	AD7	B16	$\overline{CS0}$		
Y2	VSYNC	T19	AD6	A16	$\overline{CS1}$		
W3	HSYNC	R17	AD4	D15	$\overline{CS2}$		
Y3	$\overline{INTA}$	R20	AD2	C15	$\overline{CS3}$		
Y4	$\overline{REQ}$	P18	AD1	B15	$\overline{RAS}$		
U5	$\overline{GNT}$	P19	AD0	A15	$\overline{CAS}$		
V5	ST0	P20	PD0	D14	$\overline{WE}$		
W5	ST1	N17	PD5	C14	DQM4		
Y5	ST2	N18	PD4	B14	DQM6		
U6	$\overline{RBF}$	N20	PD1	C13	SDCLK1		
V6	$\overline{PIPE}$	M17	PD7	A13	DQM5		
U7	SBA0	M18	PD6	D12	DQM7		

Table 5-3. NAND-tree Scan Order (Motherboard Pinout)

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
E4	VID0	AB19	SBA1	P23	PD3	C15	PD56
D3	VID1	AC19	SBA2	N23	PD2	A15	PD57
C2	VID2	AC20	SBA3	N22	PD10	C14	PD58
C1	VID3	AB17	SBA4	N21	PD11	B14	SDCLK2
D2	HAD1	AA18	SBA5	M23	PD14	A14	PD59
D1	VID4	AA17	SBA6	M22	PD15	D13	PD60
E3	HAD0	AC21	SBA7	M21	PD9	C13	PD61
E2	VID5	AA16	AD31	M20	PD12	B13	PD55
E1	VID6	AB16	AD30	L23	PD13	A13	PD54
F3	SPCLK2	Y15	AD29	L21	PD8	C12	PD62
G4	VID7	AC17	AD28	K23	PD17	B12	PD63
F2	PIXCLK	AC15	AD27	K21	PD16	A11	PD53
F1	VIPCLK	AC16	AD26	J23	PD21	B11	PD52
G3	SPD2	AB13	AD25	J22	PD20	C11	SDCLKOUT
H3	ROMD0	AA15	AD24	H23	PD19	D11	PD49
J4	ROMD1	AA14	AD23	J21	PD18	A10	PD51
H2	ROMD2	AA13	$\overline{C/BE3}$	H22	PD23	C10	PD50
H1	ROMD3	AA12	AD21	J20	PD22	B9	PD41
J3	ROMD4	AC13	AD22	G23	PD30	C9	PD42
J2	ROMD5	AC12	AD19	H21	PD31	A8	PD40
J1	ROMD6	AC11	AD20	G22	PD27	B8	PD48
K4	ROMD7	Y12	AD17	F23	PD28	D8	SPCLK1
K3	TVCLKR	AB10	AD18	G21	PD29	A7	PD43
K1	ROMA0	AA11	$\overline{C/BE2}$	E23	PD24	C8	PD44
L4	ROMA1	AC10	AD16	F21	PD25	B7	PD45
L3	TVCLK	AA10	$\overline{IRDY}$	E22	PD26	A6	PD46
L2	ROMA2	AC8	$\overline{FRAME}$	F20	DQM0	C7	SPD1
M3	ROMA3	AB11	$\overline{DEVSEL}$	E21	DQM2	A5	PD39
M2	ROMA4	AC9	$\overline{TRDY}$	D22	DQM3	D7	PD38
M1	ROMA5	AA9	$\overline{STOP}$	E20	DQM1	B5	PD37
N1	ROMA6	AC7	PAR	D21	MA9	A4	PD35
N2	ROMA7	Y9	$\overline{C/BE1}$	C22	MA10	D6	PD33
N3	ROMA8	AB8	AD15	B22	MA0	C5	PD36
P1	ROMA9	AA7	AD14	C21	MA1	B4	PD34
P2	ROMA10	AA6	AD12	D20	MA2	B3	PD32
P3	ROMA11	AA8	AD13	B21	MA3	D5	$\overline{FOE}$
R1	ROMA12	Y7	AD11	C20	MA4		
P4	ROMA13	AB7	AD10	D19	MA5		
R2	ROMA14	AC6	AD9	A21	MA6		
R3	ROMA15	Y6	AD8	C19	MA7		
T1	PANELHS	AB5	$\overline{C/BE0}$	D18	MA8		
R4	PANELVS	W3	AD5	A20	DSF		
T2	PANELDET	Y4	AD7	B19	$\overline{CS0}$		
AC2	VSYNC	AA5	AD6	C18	$\overline{CS1}$		
AB3	HSYNC	AC3	AD4	D17	$\overline{CS2}$		
Y22	$\overline{INTA}$	AC5	AD2	A19	$\overline{CS3}$		
AA22	$\overline{REQ}$	AB4	AD1	B18	$\overline{RAS}$		
AA21	$\overline{GNT}$	AC4	AD0	C17	$\overline{CAS}$		
AB22	ST0	T23	PD0	D16	$\overline{WE}$		
AC23	ST1	R20	PD5	A18	DQM4		
AB20	ST2	R21	PD4	B17	DQM6		
AA20	$\overline{RBF}$	R23	PD1	C16	SDCLK1		
Y21	$\overline{PIPE}$	P21	PD7	B16	DQM5		
AC18	SBA0	P22	PD6	A16	DQM7		

Section 6: PCI/AGP Bus Interfaces

Savage4 supports either PCI or AGP bus operation. Savage4 Pro and Savage4 MT (all speeds) support 1X, 2X and 4X AGP operation. Savage4 GT and Savage4 LT support 1X and 2X AGP operation.

6.1 PCI BUS INTERFACE

The pinout and other specifications for the Savage4 conform with Revision 2.2 of the the PCI specification. No glue logic is required. The ROMA3 pin must be pulled high externally with a 10K resistor. This causes a 0 to be latched in CR37_6 at reset and configure Savage4 for PCI bus operation.

6.1.1 PCI Configuration

The Vendor ID register (Index 00H) in the PCI Configuration space is hardwired to 5333H to specify S3 Incorporated as the vendor. The Device ID register is hardwired to 8A22H.

Bits 10-9 of the Status register (Index 06H) are hardwired to 01b to specify medium $\overline{\text{DEVSEL}}$ timing. The Class Code register (Index 08H) is hardwired to 30000xxH to specify that the Savage4 is a VGA compatible device.

There are two MMIO address mappings, as determined by the state of CRB0_7. By default, CRB0_7 = 1, which selects Mapping 0. This uses the PCI base addresses specified by PCI10 and PCI14. 16 MBytes of address space is claimed by PCI10 and 128 MBytes of address space is claimed by PCI14. If the ROMA12 pin is strapped high at reset, a 0 is latched in CRB0_7 and selects Mapping 1. This uses base addresses PCI10 (same as Mapping 0), PCI14 (redefined from Mapping 0 to claim 16 MBytes) and adds PCI18, PCI1C, PCI20 and PCI24, each claiming 16 MBytes. Thus, Mapping 1 allows the address space claimed to be broken up into smaller blocks, as required by some operating systems. The Base Address 0 register (Index 10H) defaults to address 7000 0000H. This is the relocatable base address for memory-mapped I/O register accessing.

PCI04_4 is hardwired to 1 to indicate a capabilities list is available. PCI34_7-0 point to the PCI power management registers starting at offset DC. The basic power states (D0-D3) are supported as explained by the *PCI Bus Power Management Interface Specification, Revision 1.0*.

6.1.2 PCI Subsystem ID

The Subsystem ID and Subsystem Vendor ID are located in a 32-bit read only register at PCI Configuration Space Index 2C. These registers reflect the content of 4 read/write CR registers as follows:

Register	CR Space	PCI Configuration Space
Subsystem Vendor ID Low Byte	CR81	Index 2CH
Subsystem Vendor ID High Byte	CR82	Index 2DH
Subsystem ID Low Byte	CR83	Index 2EH
Subsystem ID High Byte	CR84	Index 2FH

These registers allow identification of particular vendors using the same graphics chip. The following design allows the subsystem identification to be handled by software (no hardwiring).

For add-in card cases, the system BIOS will typically attempt to read the subsystem ID information before the video BIOS is run. When this occurs, Savage4 will check a read/write Subsystem ID Source bit (CR37_2), which defaults to 1 on power-up. This bit is defined as follows:

CR37_2 - Subsystem ID Source

0 = Read subsystem ID information from chip registers
1 = Read subsystem ID information from BIOS

On power-up, with this bit set to 1, the following occurs:

1. The PCI bus is claimed and held by the Savage4 when an attempt to read the subsystem ID occurs.
2. Video ROM BIOS locations C0040-C0043 are read, depending on which $\overline{BE[0:3]}$ lines are enabled. For example, if only $\overline{BE0}$ is enabled, then the byte at C0040 will be read. The information in C0040-C0043 is editable using S3's Video BIOS edit utility, and thus can be tailored by each vendor. The ROM information is automatically copied into the ID registers (CR81-CR84 and the mirrored PCI2C-PCI2F).
3. The PCI bus is released.
4. (Some time later) The video BIOS is run. It resets CR37_2 to 0. Until this step is taken, all subsystem register accesses will generate the sequence listed in steps 1-3 above.

From this point on until the next hard re-boot, all subsystem register accesses will be directed to the PCI subsystem registers. A soft reset (e.g., CTL-ALT-DEL) does not change the state of CR37_2 and thus does not affect the subsystem ID read process.

Motherboard designs incorporate the video BIOS and system BIOS in the same ROM, so care must be taken that the Savage4 does not generate a video ROM access cycle. To accomplish this, ROMD7 is pulled high at reset with an external 10K resistor to latch a 0 in CR37_2. The system BIOS must then load the subsystem ID information in the Savage4 before any ID scanning takes place. To do this, it must turn on the Savage4, enable I/O accesses in the PCI configuration space, unlock the CR registers, program the subsystem ID information in the registers described above, then turn off the Savage4.

6.2 AGP BUS INTERFACE

Savage4 conforms with the requirements of Revision 2.0 of the AGP master interface specification. No glue logic is required. AGP operation is enabled by default (CR37_6 = 1). Major functions supported include:

- $\overline{PIPE}$ and 1x/2x/4x side band addressing
- Data received at 1x/2x/4x clock rate
- Fast back to back data transfers
- Early grant
- Flow control of $\overline{RBF}$ and throttling
- Up to 32 outstanding AGP requests
- Master read for 3D textures in system memory
- Command split function

For the most part, AGP configuration is identical to PCI configuration. PCI04_4 is hardwired to 1 to indicate that Savage4 implements a list of capabilities. PCI34_7-0 point to the location of this list, which is at offset 80H. PCI80, PCI84 and PCI88 implement the register bits required by the AGP specification. PCI88_2-0 select the data rate. Savage4 GT devices (86C395) and Savage4 LT devices (86C34) do not support 4x clocking. This is indicated by implementing an external pull-up resistor on the ROMA10 pin. This latches a 0 in CRB0_5 at reset, which in turn clears PCI84_2 to 0 to indicate no 4x support. PCI88_8 = 1 enables AGP bus master operations. PCI88_9 =1 enables sideband addressing. This should only be done if the design supports this function. This is indicated by PCI84_9 (1 = sideband addressing supported). The state of PCI84_9 is determined by the state of CR70_7.

CR37_5 latches the state of the ROMA2 pin at reset to select whether IDSEL will be connected to AD16 (CR37_5 = 0, external pull-up) or to AD17 (CR37_5 = 1, default). Connecting to AD16 is appropriate for add-in cards; connecting to AD17 is appropriate for motherboard implementations. The AGP 2x or 4x interface can operated at either 1.5V VDDq or 3.3V VDDq. 1.5V is required for 4x clocking. If 1.5V VDDq is used, the VDDqCOMP pin must be tied to VDDq via a 240Ω 1% resistor.

6.3 INTERRUPT GENERATION

Whatever the mode of operation (VGA or Enhanced), bit 4 of CR32 must be set to 1 to enable interrupt generation. When an enabled interrupt is generated, $\overline{INTA}$ is pulled low unless CR36_0 = 0 (ROMD0 pulled high at reset), for which case no PCI interrupt line is claimed during PCI configuration.

When Savage4 is being operated in VGA mode (CR66_0 = 0), only a vertical retrace can generate an interrupt. This is enabled when CR11_5 = 0 and CR11_4 = 1. When an interrupt occurs, it is cleared by writing a 0 to CR11_4. The interrupt must then be re-enabled by writing a 1 to the same bit. Note that the BIOS clears both bit 4 and bit 5 of CR11 to 0 during power-on, a mode set or a reset. Thus, interrupt generation is disabled until bit 4 is set to 1.

In Enhanced mode (CR66_0 = 1 or 3D operation), interrupts can be generated by a vertical retrace, command or bus FIFO overflow, command or bus FIFO empty or by a BCI command. These interrupts are enabled and cleared and their status reported via MM8504. LPB and serial port interrupts are controlled via MMFF08. If interrupts are used, they should be cleared before they are enabled.

Multiple interrupts can be enabled at the same time in Enhanced mode. The interrupt pin will remain asserted until all interrupt status bits are cleared.

Section 7: Display Memory

Savage4 supports SDRAM/SGRAM for its video frame buffer. This section describes the various configurations supported, the functional timing for memory accesses and the operation of various register bits that affect memory timing and operation.

Supported SDRAM/SGRAM commands are:

- Set Mode Register
- Set Special Register (SGRAM only)
- Read
- Write
- Block Write (SGRAM only)
- Precharge, Precharge all Banks
- $\overline{CAS}$ before $\overline{RAS}$ Refresh

The maximum frame buffer size supported by each of the Savage4 family parts is shown in Table 7-1.

Table 7-1. Maximum Frame Buffer Size by Part

Part Name	Maximum Supported Frame Buffer Size
Savage4 Pro, Savage4 Pro-M (all speeds)	32 MBytes
Savage4 GT	16 MBytes
Savage4 LT	8 MBytes

The supported configurations (subject to the limits shown in Table 7-1) are shown in Table 7-2.

Table 7-2. Supported Memory Configurations

Memory Configuration					Register Settings		
Type	Pieces	FB Size (MB)	Banks	Interface	CR36_7-5	CR68_7-6	CR92_6
1Mx16 SDRAM	2	4	2	32-bit	001	01	0
	4	8	2	64-bit	010	01	0
	8	16	2	64-bit	100	01	0
2Mx32 SDRAM	1	8	4	32-bit	001	01	1
	2	16	4	64-bit	100	01	1
	4	32	4	64-bit	111	00	1
4Mx16 SDRAM	4	32	4	64-bit	101	01	0
256Kx32 SGRAM	2	2	2	64-bit	000	11	0
	4	4	2	64-bit	001	11	0
	8	8	2	64-bit	010	11	0
512Kx32 SGRAM	1	2	2	32-bit	000	10	0
	2	4	2	64-bit	001	10	0
	4	8	2	64-bit	010	10	0
	6	12	2	64-bit	011	10	0
	8	16	2	64-bit	100	10	0
1Mx32 SGRAM	1	4	2	32-bit	001	01	0
	2	8	2	64-bit	010	01	0
	4	16	2	64-bit	100	01	0
1Mx32 SGRAM	2	8	2	64-bit	010	10	0
(dual chip select)	4	16	2	64-bit	100	10	0

7.1 SDRAM/SGRAM CONFIGURATIONS

The 1Mx16 SDRAM configurations are shown in Figure 7-1. As is the case for all the configurations described below, the first pin names shown are those for the memory chip. The second name shown (in parentheses) is the Savage4 pin name. Only one name is shown where the names are identical.

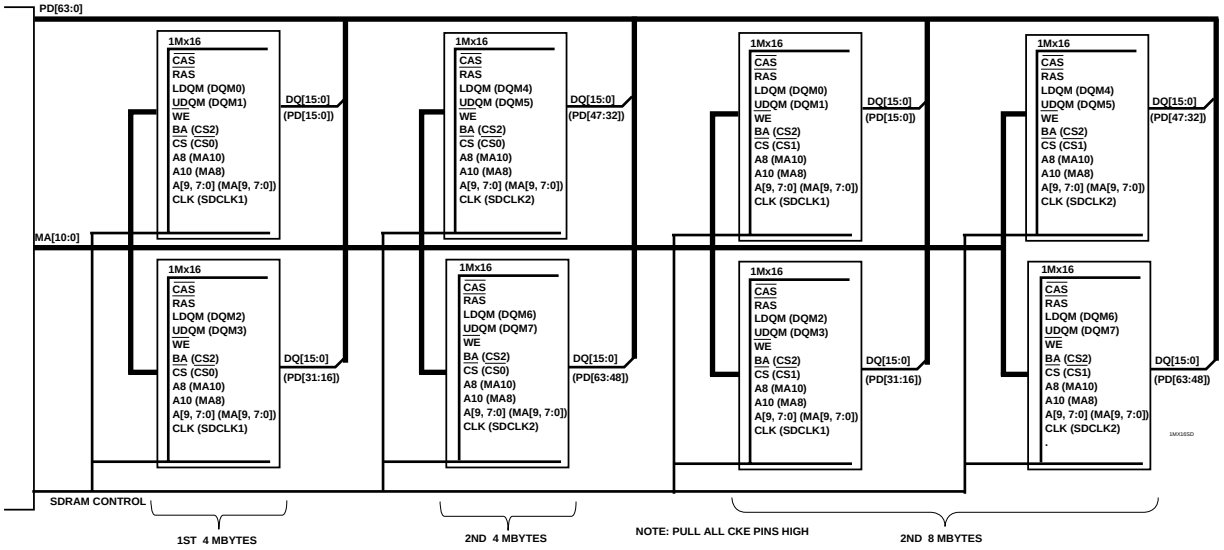


Figure 7-1. 1Mx16 SDRAM Configurations

The 2Mx32 4-bank SDRAM configurations are shown in Figure 7-2.

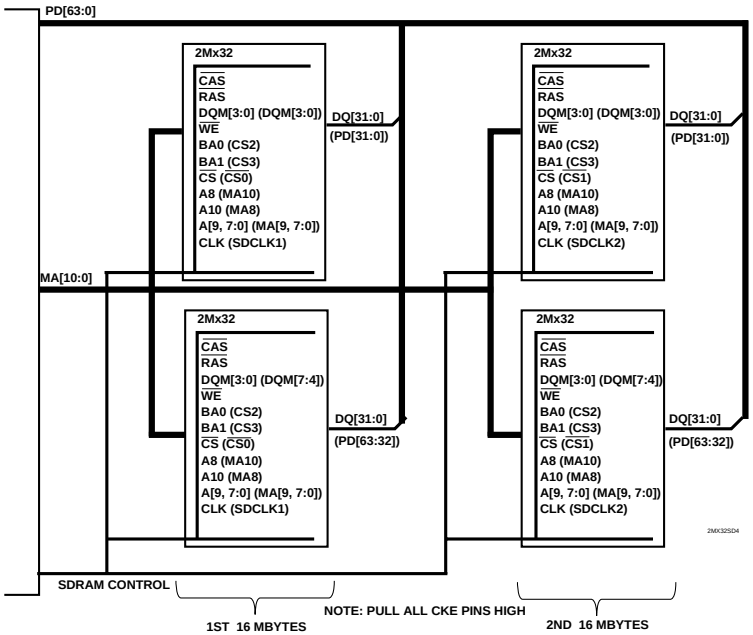


Figure 7-2. 2Mx32 4-Bank SDRAM Configurations

The single supported 32-MByte configuration for 4Mx16 4-bank SDRAMs is shown in Figure 7-3.

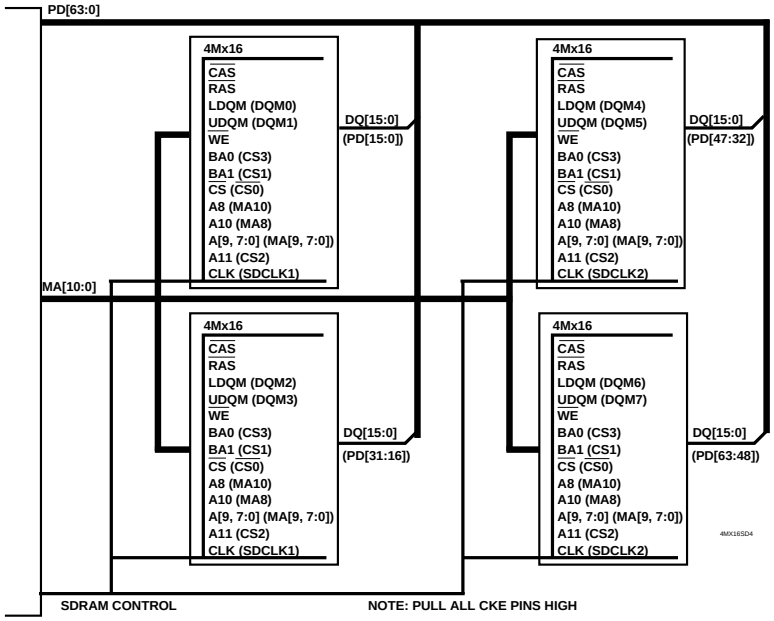


Figure 7-3. 4Mx16 4-Bank SDRAM Configuration

The 256Kx32 2-bank SGRAM configurations are shown in Figure 7-4. Some manufacturers may call pin 29 BS (instead of BA), but this pin connects to the Savage4 MA9 pin for all manufacturers.

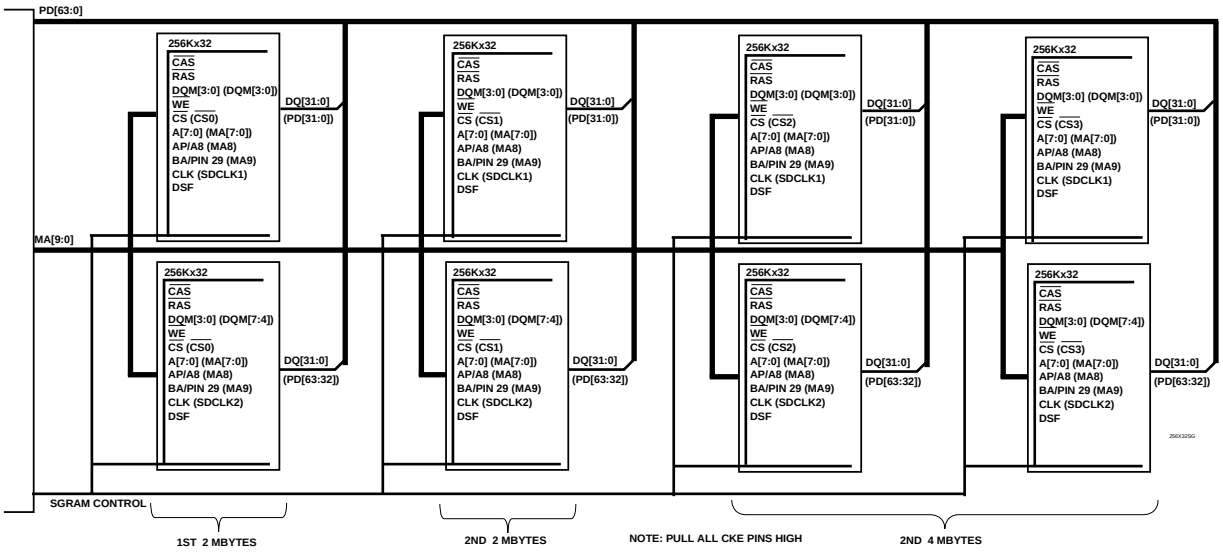


Figure 7-4. 256Kx32 SGRAM Configurations

The 512Kx32 2-bank SGRAM configurations are shown in Figure 7-5. Some manufacturers may call pin 29 BS (instead of BA), but this pin connects to the Savage4 MA9 pin for all manufacturers. Similarly, the name for pin 30 varies by manufacturer, but this pin connects to the Savage4 MA10 pin for all manufacturers.

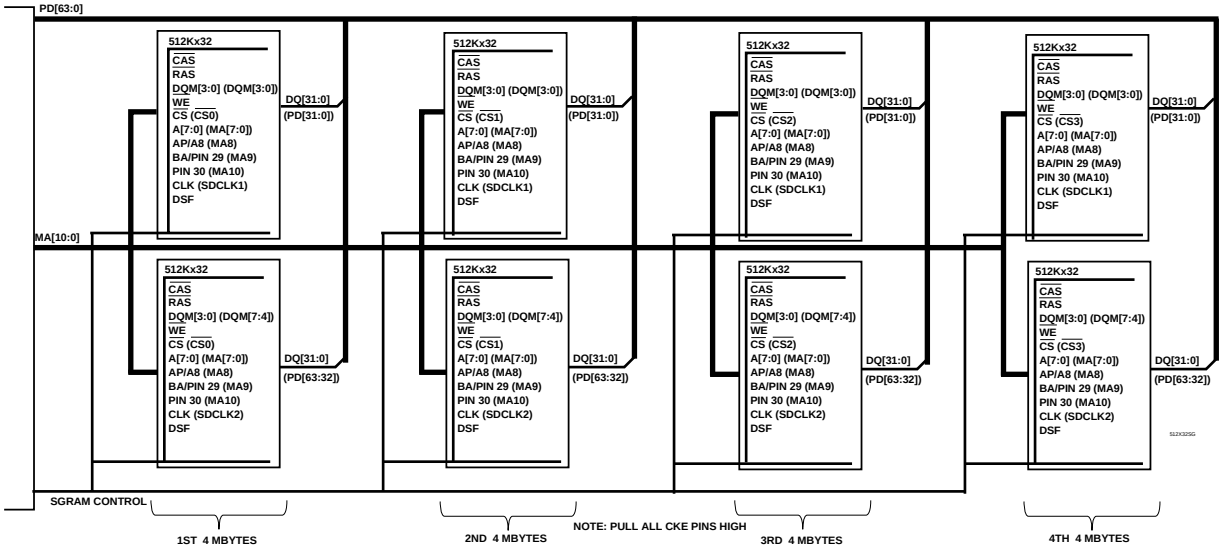


Figure 7-5. 512Kx32 SGRAM Configurations

The 1Mx32 SGRAM configurations are shown in Figure 7-6.

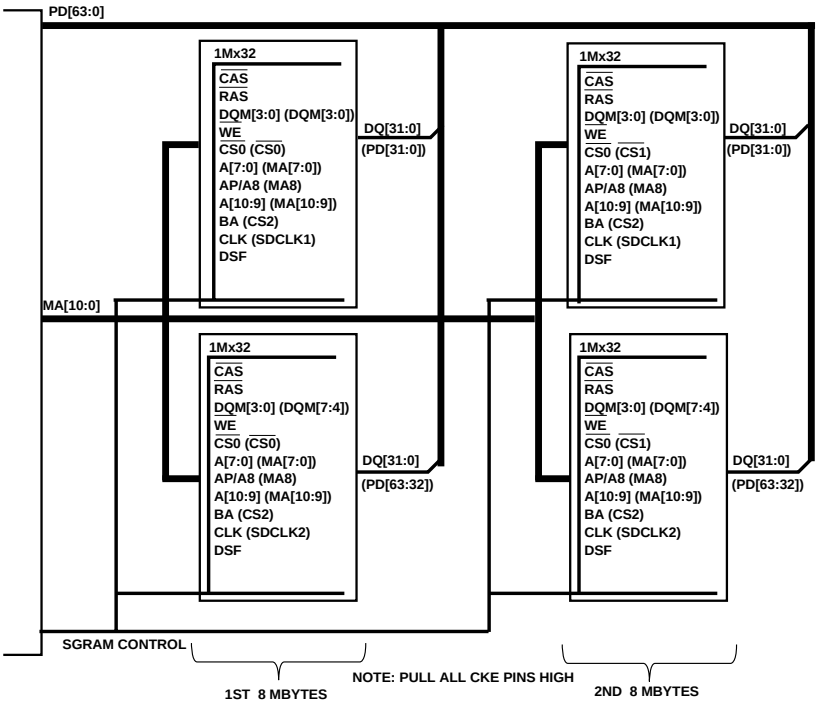


Figure 7-6. 1Mx32 SGRAM Configurations

The 1Mx32 dual chip select SGRAM configurations are shown in Figure 7-7.

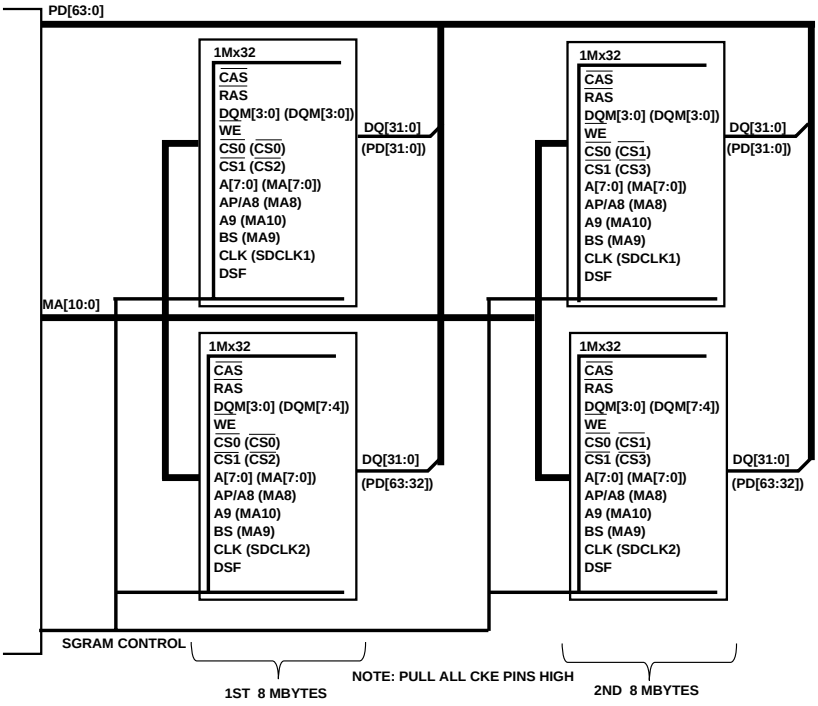


Figure 7-7. 1Mx32 Dual CS SGRAM Configurations

7.2 SDRAM/SGRAM MODE SET

DRAMs/SGRAMs require that their operating mode be programmed after reset. The $\overline{CAS}$ latency is programmed in CR6F_6-5. This setting is written to the SDRAM/SGRAM by a mode set cycle generated when CR88_5 is set to 1.

7.3 SDRAM/SGRAM REFRESH

Savage4 supports the standard $\overline{CAS}$ before $\overline{RAS}$ refresh method. The functional timing for this can be found in any SDRAM/SGRAM data book. The time from the last auto refresh cycle to the next activate command is programmable via CR68_1-0. CR3A_1-0 provide options for the refresh frequency. CR87_5-4 provide an option to adjust the refresh counter for various memory clock rates. However, this adjustment is usually not necessary.

7.4 SDRAM/SGRAM CLOCKING

Savage4 provides two output clocks (SDCLK1 and SDCLK2) for driving the synchronous memory chips. In general, SDCLK1 should connect to the lower half of the memory configuration and SDCLK2 to the upper half. This is particularly required for 8-chip configurations. For 4-chip or fewer configurations, using only SDCLK 1 is acceptable, with SDCLK2 becoming a no connect.

7.5 SDRAM/SGRAM READ DATA LATCHING

Latching of read data is based on the inputs to the SDCLKR1 and SDCLKR2 pins. These signals are a loopback of the SDCLKOUT output. The two branches of the SDCLKOUT signal (to SDCLKR1 and SDCLKR2) should be made equal in length on the PCBA. A design-specific capacitance is attached to the SDCLKOUT trace (before the branch) to adjust for the capacitive delay related to the memory chips. See S3 reference designs for details. The timing of the SDCLKR inputs can also be adjusted via SR1D.

7.6 SDRAM/SGRAM FUNCTIONAL TIMING

This section provides functional timing for SDRAM/SGRAM read and write cycles and describes how certain timing parameters can be adjusted via register programming.

Figure 7-8 shows the functional timing for an SDRAM/SGRAM read cycle. COMMAND is made up by a standard combination of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$. Please refer to SDRAM/SGRAM data sheets for the truth table. Illustrated in the figure is a sequence of 3 reads of burst length 1. Before any READ or WRITE commands can be issued to a bank within the SDRAM/SGRAM, a row in that bank must be "opened". This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated. A read is then initiated with a READ command, as illustrated. Illustrated in Figure 7-8 is the relative timing of the feedback clock, SDCLKRx, with the data at the PD inputs.

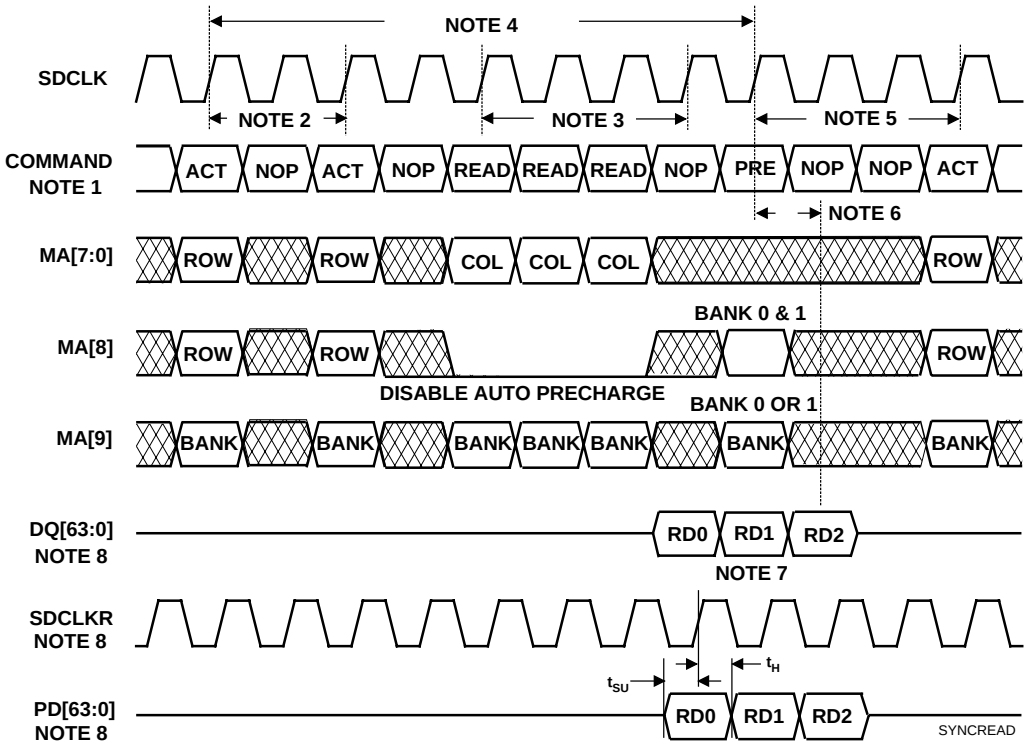


Figure 7-8. Memory Read Cycle - CAS Latency 3

Notes:

1. SGRAM/SDRAM data sheets provide the command truth tables.
2. Consecutive bank activation t_{ACT} timing is programmed via CR6F_3.
3. $\overline{CAS}$ latency (t_{CL}) is 3 in this example.
4. Minimum $\overline{RAS}$ active to the next $\overline{RAS}$ precharge time (t_{RAS}) is programmable via CR68_3.
5. $\overline{RAS}$ precharge time (t_{RP})is programmable via CR68_5-4.
6. The last data out to row precharge delay is programmable via CR6F_4. This is only effective if the minimum t_{RAS} time restriction is met.
7. Burst length is fixed at 1.
8. DQ is data at the SGRAM/SDRAM output pins. PD is data at the Savage4 input pins. SDCLKRx is used to latch the read data.

Figure 7-9 shows the functional timing for a sequence of 4 SDRAM/SGRAM write cycles (burst = 1). The first WRITE command is issued t_{RCD} clock cycles after the ACTIVE command. The bank and row addresses are asserted during ACTIVE. The column and bank addresses are provided with each WRITE command. Valid data is output coincident with each WRITE command.

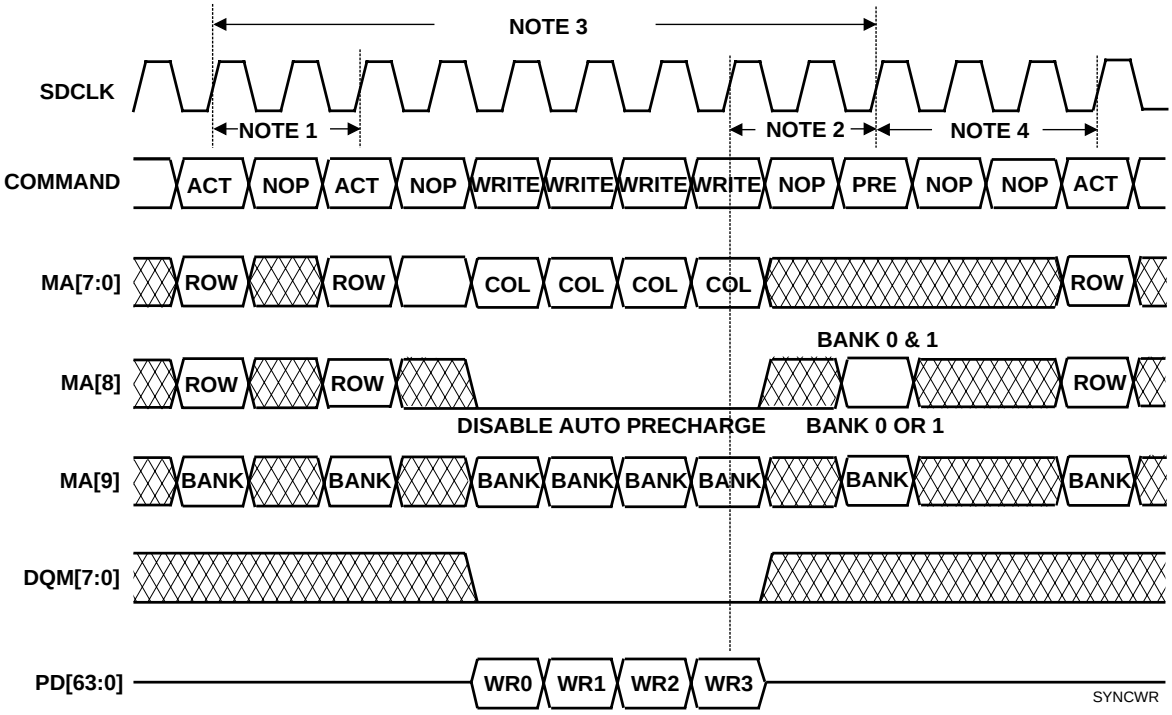


Figure 7-9. Memory Write Cycle

Notes:

1. Consecutive bank activation timing is programmed via CR6F_3.
2. Last data in to row precharge delay is programmable via CR68_2.
3. Minimum $\overline{RAS}$ active to the next $\overline{RAS}$ precharge time (t_{RAS}) is programmable via CR68_3.
4. $\overline{RAS}$ precharge time (t_{RP})is programmable via CR68_5-4.

Section 8: Local Peripheral Bus/VIP

The Local Peripheral Bus (LPB) is enabled when bit 0 of MMFF00 is set to 1. The LPB function provides the following:

- 8-bit Video Interface Port (VIP)
- 8-bit interface to industry standard video digitizers

8.1 VIP INTERFACE

The VIP interface is compliant with the *Video Interface Port VIP Specification*, Version 1.1. Only a single slave device can be active at one time (no concurrency). VIP mode is selected by setting MMFF00_3-1 to 110b and provides a glueless interface to VIP-compliant devices. The VIP signals are listed in Table 8-1. See the VIP specification for other interface and timing information.

Table 8-1. VIP Signals

VIP Signal	Pin(s)
VID[7:0]	F3, E1, E3, D1, D3, C1, C2, B1
PIXCLK	F2
VIPCLK	F1
HCTL	E2
HAD[1:0]	D2, E4

The Savage4 VIP implementation supports live video (MMFF14_15-14 = 01b) or MPEG (MMFF14_15-14 = 00b) decoders. Incoming video data transfer uses the standard VIP protocol.

A two-way interface is provided for read/write of the VIP device registers and FIFOs. The type of transaction is programmed in MMFF14_13-12 as follows:

00 = Register write
01 = FIFO write
10 = Register read
11 = FIFO read

Register read/writes are performed by programming the register address in MMFF14_11-0 and then writing to MMFF18 to trigger the transaction. The data written for a read is ignored. Read/write bursts of from 1 to 4 bytes are specified via MMFF14_23-22, assuming the VIP device supports bursting. For example, if a burst write of 4 is specified, the four bytes are written to MMFF18. This will generate four consecutive 8-bit writes to the VIP device register space (bits 7-0 first, bits 15-8 next, etc.). Similarly, the first byte of a burst read appears in bits 7-0, the second in bits 15-8, etc.

The only FIFO read transactions supported are for Ports 0 and 1 status. These are done as for register reads, with the address specified in MMFF14_11-8 and the results latched in MMFF18 after a write of anything to that register.

The LPB has an 8x32 output FIFO that is used for transferring compressed video data to a VIP decoder (FIFO write). Software checks the status (MMFFO4_3-0), and writes some number of DWords into the output FIFO via writes to the 16 DWord address range from FF40 to FF5F. Writes to anywhere in this range are directed to the output FIFO. As soon as this FIFO has one entry, it will start trying to burst this data to the VIP device FIFO specified by MMFF14_11-8. The size of the burst is specified in MMFF14_21-20 (4, 8, 12 or 16 bytes).

VIPCLK can be SCLK or SCLK/2 (MMFFA0_10 = 1). The latter is used for AGP (SCLK = 66 MHz) operation.

8.2 LPB VIDEO DIGITIZER INTERFACE

When MMFF00_3-1 = 010b, the following video digitizer interface is enabled. All signals are inputs from the digitizer.

Table 8-2. LPB Video 8 Mode Signals

LPB Signal	Pin(s)	Description
LD[7:0]	F3, E1, E3, D1, D3, C1, C2, B1	Video data bus
LCLK	F2	Pixel clock
$\overline{\text{ODDIN}}$	E4	Odd field indicator (low = odd)
VS	E2	Vertical sync
HREF	D2	Horizontal reference or sync

A serial I^2C interface is provided to program the digitizer. This interface is described in Section 9. This interface can also be used with devices that implement the VIP video port but not the host port.

The video data input protocol is shown in Figure 8-1. In this figure, both VSYNC (VS) and HSYNC (HREF) have active high polarity. The vertical offset (MMFF28_24-16) is 1, meaning the first line is skipped. The horizontal offset HO (MMFF28_11-0) is 1, meaning that the first data starts one clock after the second HREF goes low. HREF goes high again some time after the last byte of the line, whose position is specified by the line width (LW) programmed in MMFF24_11-0. The widths of the VS and HREF pulses shown may vary.

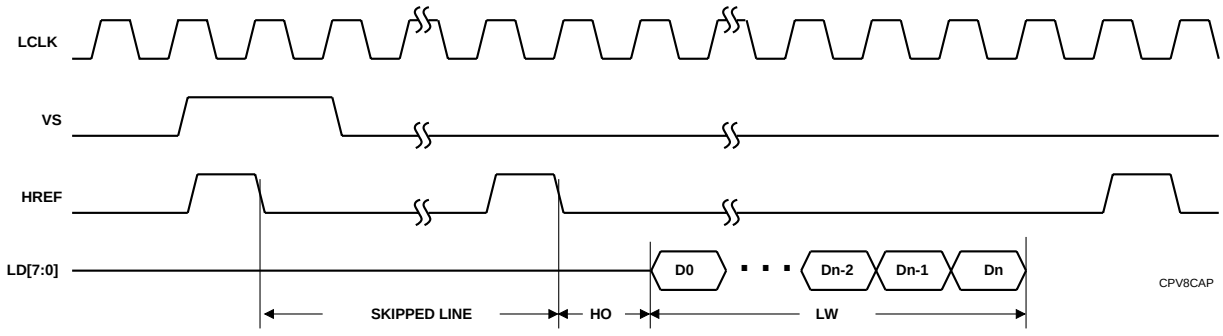


Figure 8-1. Video 8 Mode Input

Odd/even field detection is based on the following protocol:

Each time the vertical sync input (VS) transitions from high to low, the state of the horizontal sync input (HREF) is latched. A logic 0 for HREF indicates the even field is being sent. A logic 1 indicates the odd field is being sent. This is shown in Figure 8-2.

This value is EXCLUSIVE-ORed with the value of MMFF00_29 to allow polarity inversion, and the result (status) is latched in MMFF00_28.

For video input devices that do not provide sync signals in conformance with this protocol, alternate signals must be provided that meet the timing requirements given in the AC Specifications in Section 4.

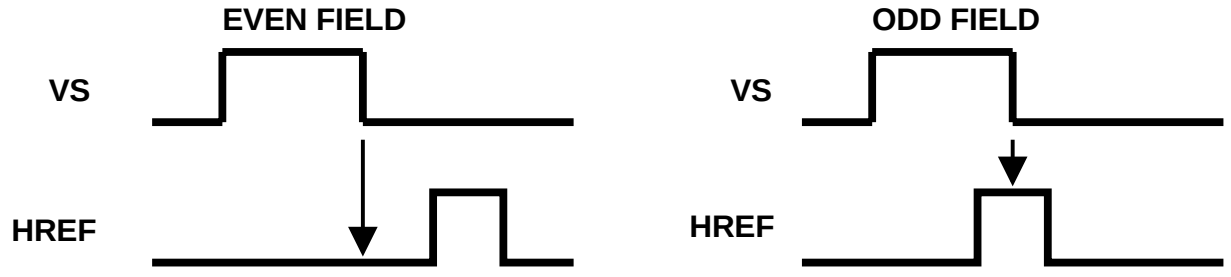


Figure 8-2. Odd/Even Field Detection

Section 9: Other Interfaces

This section explains the video BIOS ROM interfaces, the General Output Ports and the serial, CRT, flat panel, TV and HDTV interfaces. Power filtering is also described.

9.1 VIDEO BIOS ROM INTERFACE

The video BIOS ROM contains power-on initialization, mode setup, and video data read/write routines. The video BIOS can be part of the system ROM or it can be implemented separately. This section describes a separate implementation (add-in card). Three separate ROM interfaces are provided; parallel non-programmable, parallel programmable and serial. These are not supported for the Savage4 MT part, as they are not required for a motherboard implementation.

Figure 9-1 shows the implementation for a non-programmable 64K ROM. No hardware strapping is required to support this interface. The same implementation would apply to a 32K ROM except that A15 would not be used. A BIOS read causes Savage4 to output the address to the ROM. Next, $\overline{\text{ROMEN}}$ is asserted to cause the ROM to return data, which is then passed to the PCI bus and $\overline{\text{TRDY}}$ is asserted.

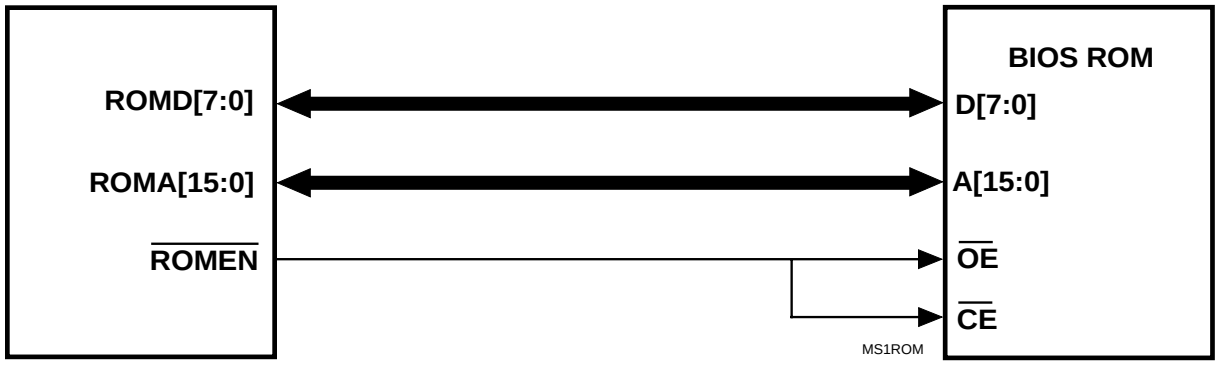


Figure 9-1. Non-Programmable BIOS ROM Interface

Savage4 also supports 16- and 32-bit ROM reads, as defined by the states of the byte enables. For a 16-bit read, Savage4 automatically increments the lower address once and generates the second byte of read data. For a 32-bit read, Savage4 automatically increments the lower address three times and generates the remaining three bytes of read data. In both cases, $\overline{\text{TRDY}}$ is delayed until all the required data is available on the AD bus.

Savage4 also supports flash (programmable) ROMs (FlashROM) in sizes up to 64 KBytes. The interface is shown in Figure 9-2. The ROMD3 pin can be strapped to VDD via 10K resistor to enable this interface, but this is not required. Instead, software can detect the presence of a flash device and only clear CR36_3 to 0 when writing to the memory is required. This prevents the ROM $\overline{\text{FWE}}$ signal from toggling inadvertently and causing an unwanted write cycle. Programming the FlashROM is done by programming the FlashROM address into CRA1 (low byte), CRA2 and CRA3 (high byte). Data is then written to CRA4.

The serial EEPROM interface is shown in Figure 9-3. The ROMA7 pin must be strapped to VDD via a 10K resistor to enable this interface. Either a 32K ROM (one chip) and 64K ROM (two chips) is supported as shown in the figure. CRB3_0 = 1 enables writing to the lower 32K ROM. CRB2 is then written to initiate a ROM read or write cycle. CRB3_0 should then be cleared to 0 to disable the ROM write capability. CRB5_0 = 1 enables writing to the upper 32K ROM. CRB4 is then written to initiate a ROM read or write cycle. CRB5_0 should then be cleared to 0 to disable the ROM write capability. The read/write protocols are specified by the individual ROM vendors.

PCI/AGP systems support a relocatable 64-KByte video BIOS address range via the BIOS ROM Base Address configuration register (Index 30H). Bit 0 of the BIOS ROM Base Address register (Index 30H) is cleared to 0 to disable BIOS accesses. At system boot time, the ROM is read and shadowed to system memory. The system BIOS always reads starting from the base address specified in PCI30. Savage4 directs the read to the correct ROM location.

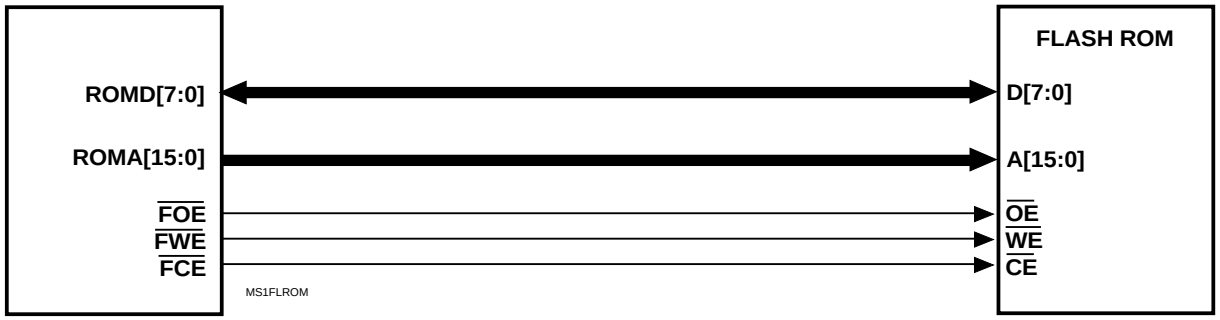


Figure 9-2. Programmable BIOS ROM Interface

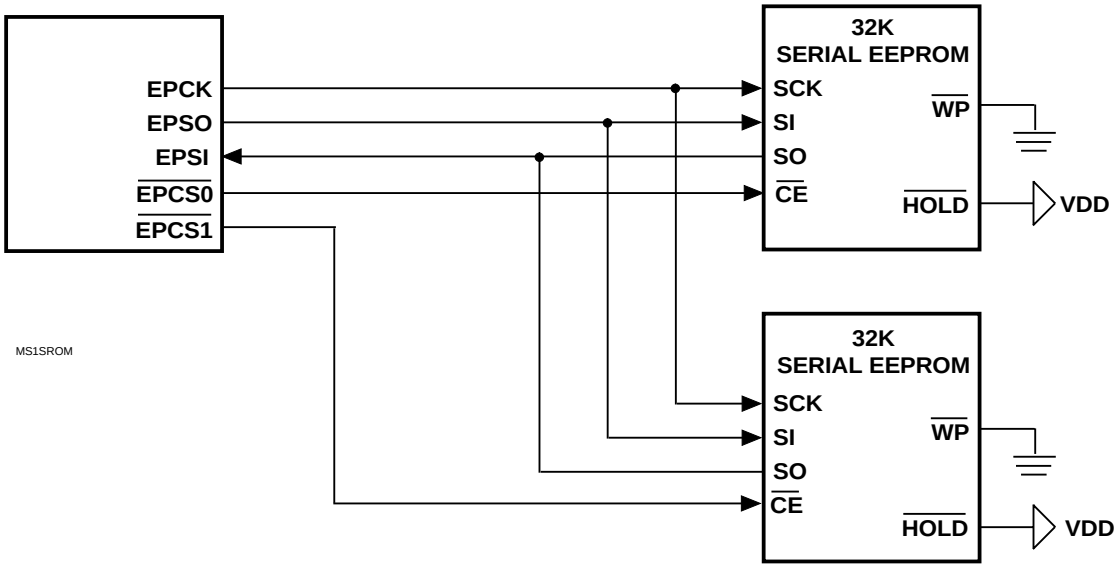


Figure 9-3. Serial BIOS EPROM Interface

9.2 GENERAL OUTPUT PORT

Savage4 provides two 1-bit general output ports. The GOP0 pin relects the state of CR5C_0. The GPOUT pin reflects the state of SRD_0.

9.3 I^2C SERIAL COMMUNICATIONS PORT

One serial communications port is implemented in a register that can be accessed either via MMFF20 or CRA0. Bit 4 is set to 1 to enable the interface. The clock is written to bit 0 (= 0) and data to bit 1 (= 0), driving the SPCLK1 and SPD1 pins low respectively. The state of the SPCLK1 pin can be read via bit 2 and the state of the SPD1 pin can be read via bit 3. The SPCLK1 and SPD1 pins are tri-stated when their corresponding control bits are reset to 0, allowing other devices to drive the serial bus.

This serial port is typically used for I^2C interfacing. When SPCLK1 and SPD1 are tri-stated, Savage4 can detect an I^2C start condition (SPD1 driven low while SPCLK1 is not driven low). This condition is generated by another I^2C master that wants control of the I^2C bus. If bit 19 of MMFF08 is set to 1, detection of a start condition generates an interrupt and sets bit 3 of

MMFF08 to 1. If bit 24 of MMFF08 is set to 1, Savage4 drives SPCLK1 low to generate I^2C wait states until the Host can clear the interrupt and service the I^2C bus.

9.4 CRT INTERFACE

Savage4 provides the following CRT interface signals:

- AR (analog red)
- AG (analog green)
- AB (analog blue
- HSYNC (horizontal sync)
- VSYNC (vertical sync)

In addition, DDC2 monitor communications can be implemented via the serial communications port controlled by CRAA_4-0. These bits control two-way communications over the SPCLK2 (clock) and SPD2 (data) lines. The operation is the same as described for the I^2C port in the previous section except that interrupts and wait states are not supported.

9.5 EXTERNAL TV ENCODER INTERFACE

Figure 9-4 shows the interface to an external Rockwell® Bt868/869 TV encoder (or compatible device). The TV outputs are generated whenever the clock input from the decoder is present on the TVCLK pin and CRB0_4 = 0. The latter can be accomplished via programming or by attaching a 10K pull-up resistor to the ROMA9 pin. The encoder is controlled via the I^2C interface. TV monitor detection is also done via this interface. The TV encoder interface and the flat panel interface are multiplexed on common pins, so only one of these can be implemented for a given design.

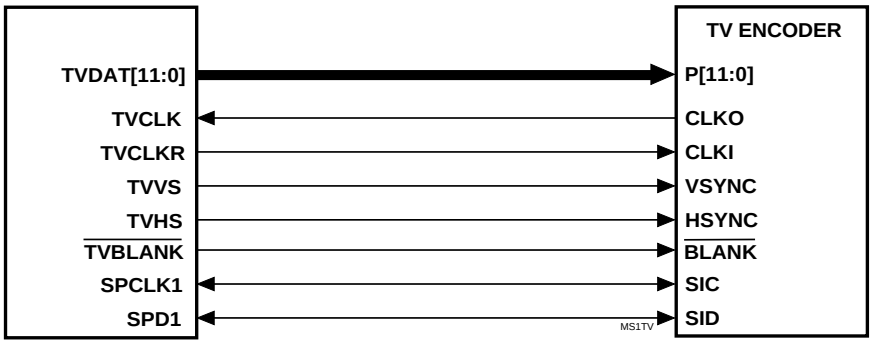


Figure 9-4. External TV Encoder Interface

Savage4 supports three output formats as shown in Table 9-1. As shown in Figure 9-4, P[11:0] on the encoder connect to TVDAT[11:0] on Savage4. The CLKI pin on the encoder connects to TVCLKR pin on Savage4.

Table 9-1 External TV Encoder Output Data Formats

	SR35_5-4 = 00		SR35_5-4 = 01		SR35_5-4 = 10	
Pin	CKLI Rising	CLKI Falling	CLKI Rising	CLKI Falling	CLKI Rising	CLKI Falling
P11	G4	R7	B7	G3	R7	G3
P10	G3	R6	B6	G2	R6	G2
P9	G2	R5	B5	G1	R5	G1
P8	B7	R4	B4	G0	R4	G0
P7	B6	R3	B3	R7	R3	B7
P6	B5	G7	B2	R6	R2	B6
P5	B4	G6	B1	R5	R1	B5
P4	B3	G5	B0	R4	R0	B4
P3	G0	R2	G7	R3	G7	B3
P2	B2	R1	G6	R2	G6	B2
P1	B1	R0	G5	R1	G5	B1
P0	B0	G1	G4	R0	G4	B0

9.6 TFT FLAT PANEL TMDS INTERFACE

Figure 9-5 shows the hardware connections to a receiver conforming to VESA® TMDS™ standard. This interface allows Savage4 to drive a TFT flat panel over considerable distance and is active when SR31_4 = 1 and CRB0_3 = 0. The latter can be accomplished via programming or by attaching a 10K pull-up resistor to the ROMA8 pin. Panel power sequencing is controlled by the receiver components.

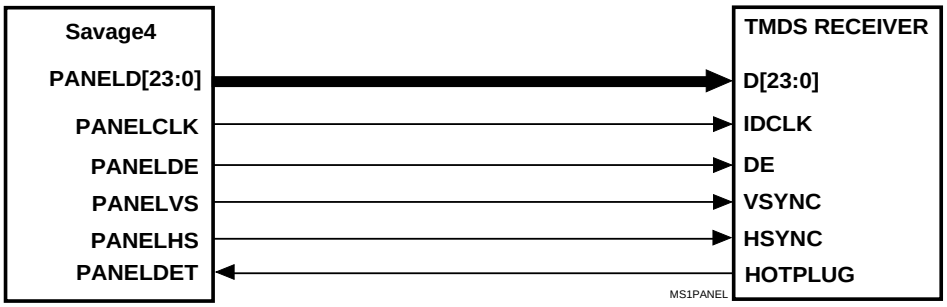


Figure 9-5. TMDS Interface

Savage4 provides the following panel detection capability. If SR30_1 = 0 and the PANELDET pin is properly connected to a voltage source indicating the presence/absence of a panel, SR30_1 will reflect the high/low state of this input. A read of 1 indicates that a powered-up panel is connected.

For proper flat panel output with a standard VGA primary screen and the Streams Processor active, the following special register settings are required:

CR3A_4 = 1
CR67_3-2 = 01b (Steams Processor secondary and VGA primary)
CR67_7-4 = desired bits/pixel mode
CR90_3 = 1 (CR0 must be programmed before this is set to 1. Setting this bit is not required for 8 bits/pixel modes)
CR90_6 = 1 (this bit must also be set to 1 for 8 bits/pixel modes)
MM8180 = 00000000H

These settings are required for correct automatic centering and expansion with Streams Processor operation.

9.7 HIGH DEFINITION TV OVERLAY

Figure 9-6 shows the hardware connections allowing RGB output from a high definition TV decoder to be overlaid on the graphics primary stream. The DCLK and OVERLAY outputs are enabled by setting MM8188_30 = 1. Note that these outpus are multiplexed with TV or flat panel functions, so these should be disabled when the HDTV function is enabled.

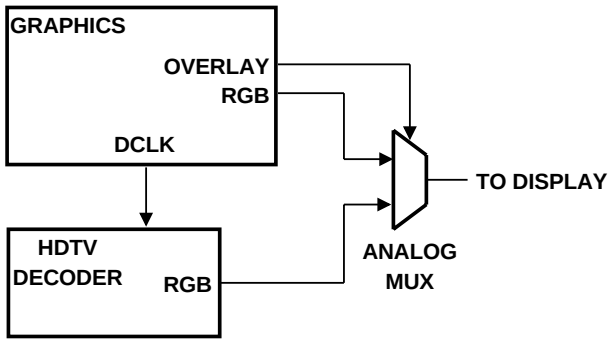


Figure 9-6. HDTV Interface

9.8 POWER AND GROUND INTERFACES

Extensive filtering is required on the power pins to ensure stable operation. In general, each bypass capacitor should be place as close to the power pin it filters as possible and the capacitor should be between the pin and the power source. The numbers and sizes of capacitors is dependent on many factors, including capacitive loadings and board layout. S3 reference designs provide examples and guidelines for these issues.

Figure 9-7 shows the recommended power connections for the analog pins. The circuitry shown in Figure 9-8 for REGINA and REGOUTA can be eliminated for PCI configurations. For this case, the pins are left unconnected.

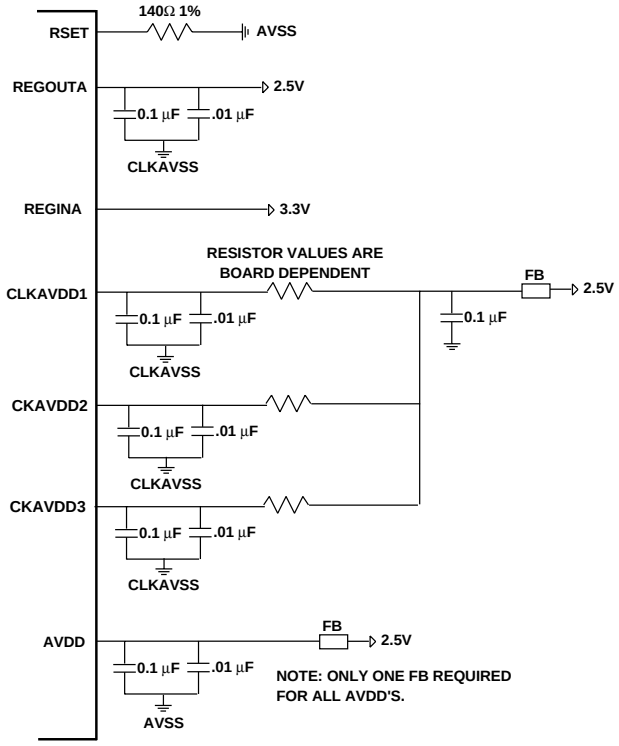


Figure 9-7. Analog Block Power and Ground Connections

Figure 9-8 shows the voltage reference interfaces. The acceptable resistor values for the VREFB interface for 3.3V VDDq are shown in Table 9-2. This table is taken from the *A.G.P. Platform Design Guide (Rev. 1.1)*. If VDDq is 1.5V, Savage4 receives its VREFB input from pin B66 of the AGP connector. The circuit shown on the right of Figure 9-8 must be connected to AGP connector pin A66 to generate the correct referenced voltage.

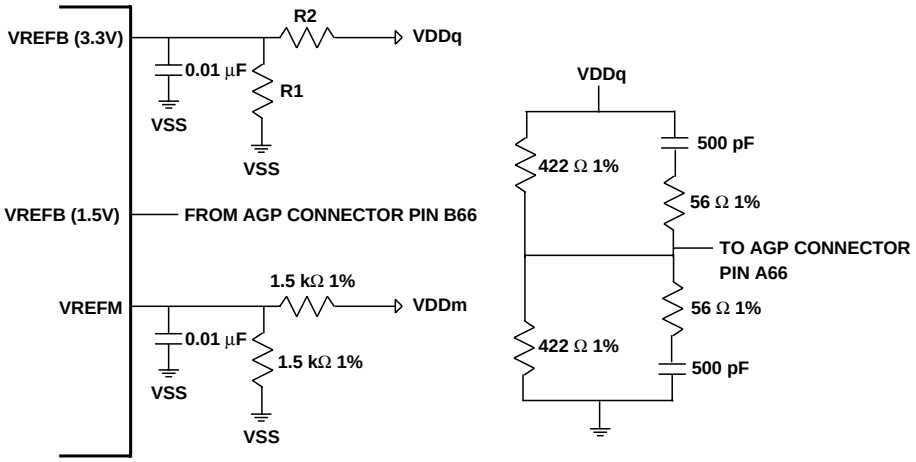


Figure 9-8. VREFx Connections

Table 9-2. VREFB Resistor Values (3.3V)

R1 (KOhm)	R2 (KOhm)	Tolerance (%)
1.00	1.50	1
1.10	1.65	1
1.40	2.10	1
1.58	2.37	1
1.62	2.43	1
1.74	2.61	1
1.78	2.67	1
1.96	2.94	1
2.32 (max)	3.48 (max)	1
0.10	0.15	2
0.12	0.18	2
0.16	0.24	2
0.18 (max)	0.27 (max)	2

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