

**LC895199K****SANYO****ATAPI / IDE-Interface CD-ROM Error Correction IC****Preliminary****Functions**

- CD-ROM ECC function, Subcode read function, ATAPI (IDE) I/F (register block, etc.), CAV audio function

**Features**

- Built-in ATAPI (IDE) I/F
- 32x speed supported  
using EDO-DRAM ( $\times 16$ , 50 ns)  
16.6 Mbytes/s (with IORDY)  
Operating frequency: 33.8688 MHz
- 32x speed supported  
using EDO-DRAM ( $\times 16$ , 45 ns)  
16.6 Mbytes/s (without IORDY)  
Operating frequency: 33.8688 MHz
- 24x speed supported  
using EDO-DRAM ( $\times 16$ , 50 ns)  
16.6 Mbytes/s (without IORDY)  
Operating frequency: 33.8688 MHz
- 1 Mbit to 4 Mbits of buffer RAM connectable in case of DRAM
- CD main channel, C2 flag, and subcode areas in buffer RAM can be freely set by user
- Built-in batch transfer function (function for sending CD main channel, C2 flag, subcode, etc. at one time)
- Built-in multi block transfer function (function for sending several blocks at one time)
- Built-in CAV audio function
- Built-in intelligent functions (auto buffering, auto decoding, CD-R support, etc.)
- Built-in subcode P to W buffering function (NO-ECC) and CD-TEXT support
- Ultra DMA, MODE2, MODE1, MODE0 support

**Specifications****Absolute Maximum Ratings at  $V_{SS} = 0$  V**

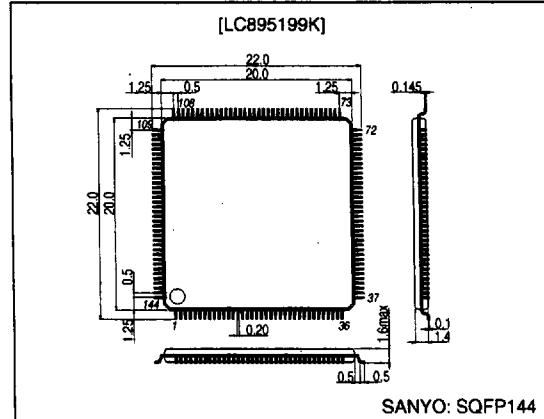
Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\ max}$	$T_a = 25^\circ C$	-0.3 to +7.0	V
Input/output voltage	$V_{I/O}$	$T_a = 25^\circ C$	-0.3 to $V_{DD} + 0.3$	V
Allowable power dissipation	$P_d\ max$	$T_a \leq 70^\circ C$	550	mW
Operating temperature	$T_{opr}$		-30 to +70	°C
Storage temperature	$T_{stg}$		-55 to +125	°C
Soldering temperature (pin part only)		10 s	235	°C
Input/output power	$I_i, I_o$		$\pm 20$	mA

Note: \* Per 1 input/output reference cell

**Package Dimensions**

unit: mm

3214-SQFP144



**Allowable Operating Range at  $T_a = -30$  to  $+70^\circ\text{C}$ ,  $V_{SS} = 0 \text{ V}$** **IO cell 5.0 V supply voltage**

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}$		4.5	5.0	5.5	V
Input voltage range	$V_{IN}$		0		$V_{DD}$	V

**Internal cell 3.3 V supply voltage**

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}$		3.0	3.3	3.6	V
Input voltage range	$V_{IN}$		0		$V_{DD}$	V

**DC Characteristics at  $T_a = -30$  to  $+70^\circ\text{C}$ ,  $V_{SS} = 0 \text{ V}$ ,  $V_{DD} = 4.5$  to  $5.5 \text{ V}$** 

Parameter	Symbol	Conditions	Ratings			Unit	Applicable pins *1
			min	typ	max		
High-level input voltage	$V_{IH}$	TTL levels	2.2	—	—	V	(1)
Low-level input voltage	$V_{IL}$		—	—	0.8	V	
High-level input voltage	$V_{IH}$	TTL levels with pull-down resistor	2.2	—	—	V	(10)
Low-level input voltage	$V_{IL}$		—	—	0.8	V	
High-level input voltage	$V_{IH}$	TTL levels Schmitt	2.4	—	—	V	(2), (3), (11)
Low-level input voltage	$V_{IL}$		—	—	0.8	V	
High-level output voltage	$V_{OH}$	$I_{OH1} = -4 \text{ mA}$	$V_{DD} - 2.1$	—	—	V	(4)
Low-level output voltage	$V_{OL}$	$I_{OL1} = 4 \text{ mA}$	—	—	0.4	V	
High-level output voltage	$V_{OH}$	$I_{OH1} = -8 \text{ mA}$	$V_{DD} - 2.1$	—	—	V	(10), (12)
Low-level output voltage	$V_{OL}$	$I_{OL1} = 8 \text{ mA}$	—	—	0.4	V	
High-level output voltage	$V_{OH}$	$I_{OH1} = -12 \text{ mA}$	$V_{DD} - 2.1$	—	—	V	(5)
Low-level output voltage	$V_{OL}$	$I_{OL1} = 12 \text{ mA}$	—	—	0.4	V	
High-level output voltage	$V_{OH}$	$I_{OH1} = -12 \text{ mA}$	$V_{DD} - 2.1$	—	—	V	(5)
Low-level output voltage	$V_{OL}$	$I_{OL1} = 12 \text{ mA}$	—	—	0.4	V	
High-level output voltage	$V_{OH}$	$I_{OH1} = -4 \text{ mA}$	$V_{DD} - 2.1$	—	—	V	(8), (11)
Low-level output voltage	$V_{OL}$	$I_{OL1} = 24 \text{ mA}$	—	—	0.4	V	
Low-level output voltage	$V_{OL}$	$I_{OL1} = 24 \text{ mA}$	—	—	0.4	V	(9)
Low-level output voltage	$V_{OL}$	$I_{OL1} = 8 \text{ mA}$	—	—	0.4	V	(6), (7)
Input leak current	$I_{IL}$	$V_I = V_{SS}, V_{DD}$	-10		+10	$\mu\text{A}$	(1), (2), (3), (11)
Output leak current	$I_{OZ}$	During high-impedance output	-10		+10	$\mu\text{A}$	(6), (8), (9), (11)
Pull-up resistance	$R_{UP}$		40	80	160	$\text{k}\Omega$	(10)
Pull-up resistance	$R_{UP}$		20	40	80	$\text{k}\Omega$	(7), ZDMACK *2

Note: \*1 The applicable pin sets are as follows.

\*2 When ZDMACK is reset, internal pull-up resistor is OFF.

When Config-Reg-R46 (PULON)-bit 0 (ZDMACK) = 1, pull-up resistor becomes ON.

**INPUT**

- (1) ATPINSEL, CSCTRL, SUA0 to 6, BCK, C2PO, LRCK, SDATA, SBSO, SCOR, WFCK, TEST0 to 1
- (2) ZRESET, ZCS, ZRD, ZWR, CSEL
- (3) DA0 to 2, ZCS1FX, ZCS3FX, ZDIOR, ZDLOW, ZDMACK, ZHRST

**OUTPUT**

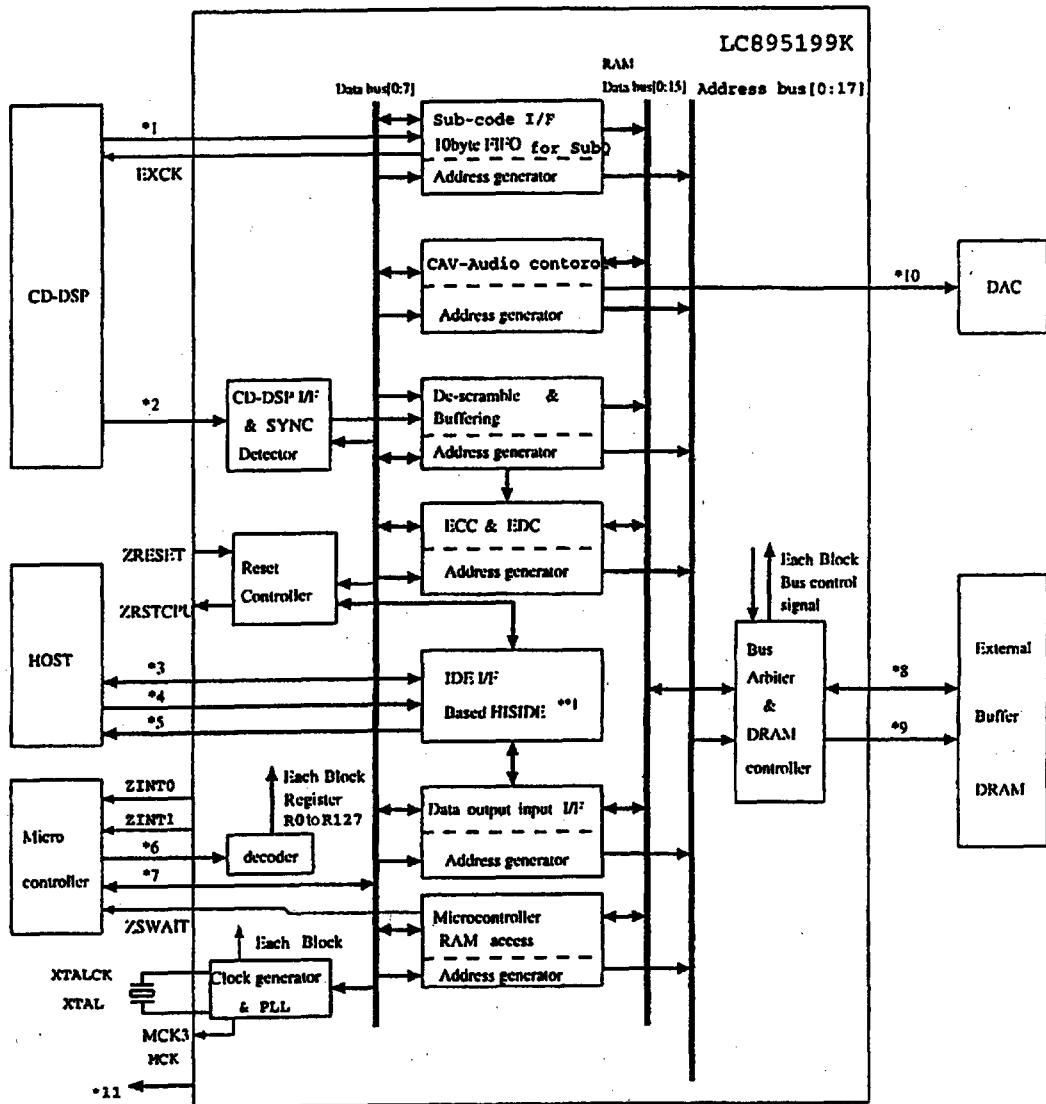
- (4) RA0 to 8, ZRAS0, ZCAS0 to 1, ZUWE, ZLWE, ZOE
- (5) MCK, MCK3
- (6) ZRSTCPU
- (7) ZINT, ZINT1, ZSWAIT
- (8) DMARQ, HINTRQ
- (9) IORDY, ZIODES16

**INOUT**

- (10) D0 to 7, IO0 to 15, HDB0 to 7
- (11) DD0 to 15, ZDASP, ZPDIG
- (12) EXCK

Note: Pins XTAL and XTALCK are not included in the DC characteristics.

## Block Diagram



- \*1 WFCK, SBSO, SCOR
- \*2 BCK, SDATA, LRCK, C2PO
- \*3 DDO to DD15, ZDASP, ZPDIAG
- \*4 ZCS1FX, ZCS3FX, DAO to 2, ZDIO, ZDLOW, ZDMACK, CSEL
- \*5 DMARQ, HINTRQ, ZI0CS16, IORDY, ZHRST
- \*6 ZRD, ZWR, SUA0 to 6, ZCS, CSCTRL
- \*7 D0 to D7
- \*8 IO0 to IO15
- \*9 RA0 to RA8, ZRAS0, ZCAS0, ZCAS1, ZOE, ZUWE, ZLWE
- \*10 DBCK, DLRCK, DSDATA
- \*11 IOP0 to IOP7
- \*\*1 HISIDE(WD25C32) is made by WESTERN DIGITAL