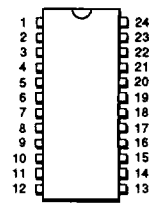
SIERRA SEMICONDUCTOR

SC11328
Programmable Frequency Synthesizer (PFS)

FEATURES

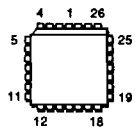
- ☐ Output frequencies up to a maximum of 100 MHz.
- ☐ High resolution frequency synthesis.
- ☐ Digitally programmable high resolution phase locked frequency.
- ☐ Dynamically programmable frequency.
- ☐ Internal mask programmable ROM for fixed frequency configuration
- ☐ Microprocessor compatible serial digital interface.
- ☐ 24-pin DIP or 28-pin PLCC.
- ☐ Pin compatible with SC22318 E^2 device

24-PIN DIP PACKAGE



SC11328CN

28-PIN PLCC PACKAGE

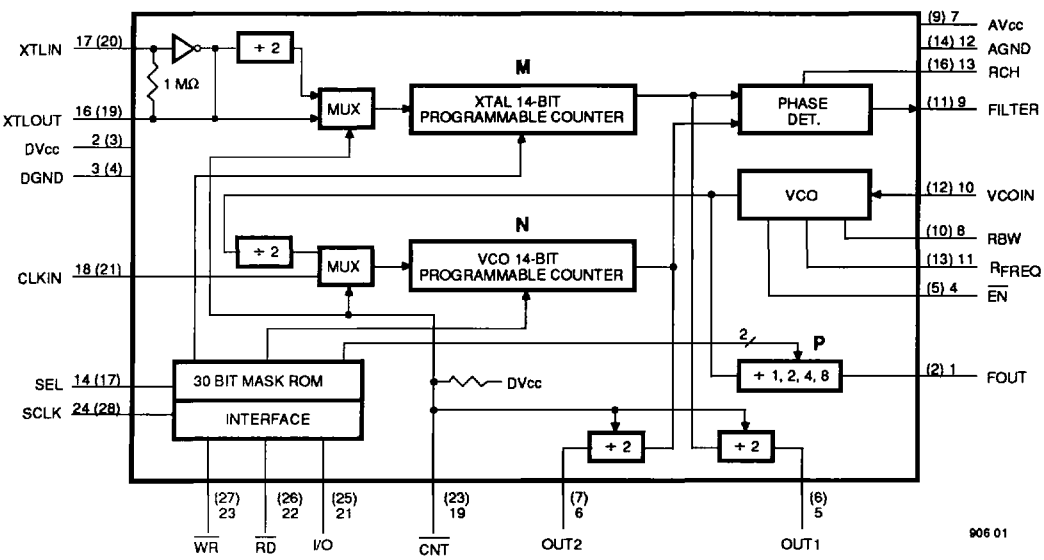


SC11328CV

GENERAL DESCRIPTION

The SC11328 is a CMOS Frequency Synthesizer. This part utilizes two 14-bit programmable Counters, an on chip oscillator (which requires an external crystal), a voltage-controlled oscillator and a phase detector to generate a 1 MHz to 100 MHz clock. The SC11328 is digitally programmed through a serial interface to provide clock frequencies with an accuracy of 14-bits. The device can be implemented in a fixed configuration with the counter divide ratio stored in a mask programmable on-chip ROM. In a microprocessor based system, it can be dynamically programmed to the application requirement. The part can also be operated as two independently programmable 14-bit dividers. The SC11328 is available in both 24-pin DIP and 28-pin PLCC packages.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES ARE DIP PACKAGE PINOUTS. NUMBERS IN ( ) ARE PLCC PINS.

Figure 1.

PIN DESCRIPTION

PIN NO. DIP	PIN NO. PLCC	PIN NAME	FUNCTION
1	2	FOUT	Voltage controlled oscillator output.
2	3	DVcc	Digital power supply.
3	4	DGND	Digital ground.
4	5	$\overline{EN}$	VCO enable pin (Active low).
5	6	OUT1	Output of divider "M".
6	7	OUT2	Output of divider "N".
7	9	AVcc	Analog power supply.
8	10	R_{BW}	Resistor to set VCO bandwidth (driven by VCOIN).
9	11	FILTER	Phase locked loop filter.
10	12	VCOIN	Input of VCO.
11	13	R_{FREQ}	Resistor to set VCO free running frequency (R_{FREQ}).
12	14	AGND	Analog ground.
13	16	RCH	Resistor to set the charge pump current (1.25 V).
14	17	SEL	Mode select pin. For SEL = High, source of divide ratios is mask programmable ROM. For SEL = Low, source of divide ratios is internal registers.
15	—	—	Not used.
16	19	XTLOUT	Crystal oscillator output pin. XTLOUT and XTLIN connect to a crystal to generate a crystal locked clock for the chip. If a suitable clock is already available in the system the XTLIN pin can be driven.
17	20	XTLIN	Crystal oscillator input pin.
18	21	CLKIN	Input to divider "N".
19	23	$\overline{CNT}$	Straight divider select pin. When $\overline{CNT}$ = low, PLL mode is disabled and straight divider mode is enabled.
20	—	—	Not used.
21	25	I/O	Serial interface input/output.
22	26	$\overline{RD}$	Serial interface read signal. During low period of this signal the data in the internal shift register is shifted out through the I/O pin.
23	27	$\overline{WR}$	Serial interface write signal. During low period of this signal the data is shifted in the internal shift register from the I/O pin.
24	28	SCLK	Serial interface clock signal.

FUNCTIONAL DESCRIPTION

Chip Architecture

The block diagram of the SC11328 is shown on Page 1 Fig. 1. It consists of two programmable 14-bit dividers, a crystal oscillator, a Phase-Locked Loop (PLL) system, a serial microprocessor interface, a metal mask programmable ROM, and a Post-scaler 2 bit divider. The two 14-bit programmable counters divide the outputs of the oscillator and VCO by "M" and "N" respectively, where "M" and "N" are two integer numbers in the range of 1 to 16,383. The divided outputs are phase-locked to each other by the PLL circuit. The output of the VCO is then divided by the post-scaler modulo "P", where "P" can have a value of 1, 2, 4 or 8. For operation in the range between 1 and 10 MHz the post scaler is required. Above 10 MHz, the post scaler can be used to improve the jitter performance. The output frequency, F_{OUT}, can be calculated as follows:

$$F_{OUT} = F_{VCO}/P = [N/(M \times P)] \times F_{OSC}$$

F_{VCO} = VCO Frequency

F_{OSC} = Oscillation frequency

M, N range from 1 to 16,383 and P = 1, 2, 4 or 8.

The M and N counters need 16 bits for programming (two bits of address and 14 bits of data), and the P-scaler needs 2 bits. These bits can be loaded into the temporary registers that can be addressed through the four-pin serial interface. The M, N and P values stored in the metal mask programmable ROM may be selected instead of using the serial interface.

Circuit Description

Phase-Locked Loop (PLL) Circuit

The PLL circuit consists of a voltage controlled oscillator (VCO), a phase detector circuit, a charge-pump and an external loop-filter. The VCO center frequency and bandwidth are determined by the two external resistors R_{FREQ} and R_{BW}, respectively. V_{VCOIN} represents the VCO input voltage from the loop-filter.

Choosing suitable R_{FREQ} and R_{BW} (bandwidth) values can be accomplished using several different iterative methods. Below are several defining equations and one method for choosing R_{FREQ} and R_{BW}. Note that F_{VCO} is the input frequency of the post-scaler. In general, F_{VCOMIN} should be greater than 10 MHz, F_{VCOMAX} should be less than 100 MHz and F_{VCOMAX}/F_{VCOMIN} should not exceed EQ. 3, which can range typicallyfrom 1 to 3.

The PLL incorporates phase/frequency detector (PFD) logic. A charge pump is used to convert the logic states of the PFD into analog signals suitable for controlling the VCO. The charge pump current is

DEFINING EQUATIONS:

EQ. 1

$$I_{BIAS} = \frac{V_{VCOIN}}{R_{BW}} + \frac{2.2V}{R_{FREQ}}$$

V_{VCOIN} typically can range from 1V to 3V; 2V is nominal.

EQ. 2

$$F_{VCO} = \frac{1000}{\frac{4400}{I_{BIAS}} + 3}$$

EQ. 3

$$\frac{F_{VCOMAX}}{F_{VCOMIN}} = \frac{V_{VCOMAX} + 2.2\,\frac{R_{BW}}{R_{FREQ}}}{V_{VCOMIN} + 2.2\,\frac{R_{BW}}{R_{FREQ}}}$$

Outlined below is a method for calculating R_{FREQ} and R_{BW} using EQ. 1 and EQ. 2.

Step 1. Choose the desired F_{VCOMIN} and F_{VCOMAX}.

Step 2. Calculate $I_{BIASMIN}$ and $I_{BIASMAX}$ using EQ. 4 and EQ.5.

EQ. 4

$$I_{BIASMIN} = \frac{4400}{\frac{1000}{F_{VCOMIN}} - 3}$$

EQ. 5

$$I_{BIASMAX} = \frac{4400}{\frac{1000}{F_{VCOMAX}} - 3}$$

Step 3. Calculate R_{BW} by using EQ. 6 and subtracting $I_{BIASMAX}$ from $I_{BIASMIN}$.

EQ. 6

$$R_{BW} = \frac{V_{COMAX} - V_{COMIN}}{I_{BIASMAX} - I_{BIASMIN}} = \frac{3V - 1V}{\Delta I_{BIAS}}$$

Step 4. Calculate R_{FREQ} using EQ. 7.

EQ. 7

$$R_{FREQ} = \frac{2.2V}{I_{BIASMAX} - \frac{3V}{R_{BW}}}$$

R_{BW} in MΩ, I_{BIAS} in μA

Step 5. If either R_{FREQ} or R_{BW} is negative, then choose a smaller ΔF_{VCO} and repeat steps 1 through 4.

determined by the external resistor RCH, and its value is given by:

ICH = 1.25V/RCH; RCH ~1.6 KΩ

A filter is added after the charge-pump to smooth the VCO control voltage. Figure 2 shows the complete PLL circuit. The states of the PFD are determined by the edges of the input wave-form. If the R-input (reference) phase leads the V-input (VCO) phase, then an edge of the R input sets the U (up) terminal true. The next V edge resets the U terminal false. Conversely, if V leads R, a V edge sets D (down) true and the next R edge resets D false. Both U and D can be false simultaneously, or either one alone can be true, but both can never be true simultaneously. Therefore a PFD has three allowable states at its output terminals, up (U), down (D) and neutral(N).

A typical circuit for the charge-pump and two possible loop-filters are shown in Figure 3. The loop filter consisting of the simple resistor capacitor combination has the disadvantage of having some granularity effect. Upon each cycle of the PFD, the pumping current Ip is driven into the filter impedance which responds with an instataneous voltage jump of delta (Vc) = ICH*R2.

At the end of the charging interval, the pump current switches off and a voltage jump of equal magnitude occurs in the opposite direction. The frequency of the VCO follows the voltage steps so there will be frequency excursion. The second loop filter has an additional capacitor C3 is parallel with the R2-C2 impedance. Because of this capacitor, the VCO control voltage has a continuous ramp-like, exponential function for each pump pulse, instead of the rectangular jump that is present in the filter without the additional capacitor.

Mask Programmable ROM

For fixed frequency configuration, the M, N and P divide ratios can be stored in an on-chip ROM with a custom metal mask. To access the counter divide ratios in the ROM, the SEL pin should be tied high. Contact Sierra Semiconductor for generation of a custom metal mask for ROM storage.

Serial Interface

Each counter needs 16 bits for programming, out of which 2 bits are for the destination's address and 14 are for data bits (see Table 1 and 2). The programming bits are loaded into the chip through the serial interface and are stored in the registers in Figure 4.

The divider programming data is stored in the internal temporary register through a four pin serial interface. When $\overline{WR}$ goes low, sixteen bits of data are shifted serially into the chip through the I/O pin.The sixteen bits constitute fourteen bits of programming data and two bits of destination address. The data is sampled on the rising edge of the shift clock (SCLK). When $\overline{WR}$ goes high, the contents of the memory location selected by the two bit destination address is updated by the fourteen bit data. For proper

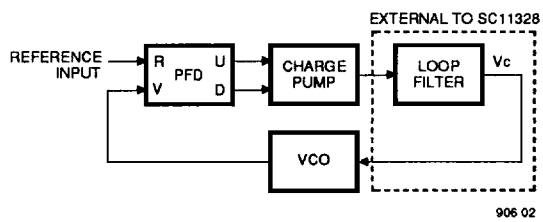


Figure 2. PLL with Three-State Phase Detector and Charge Pump

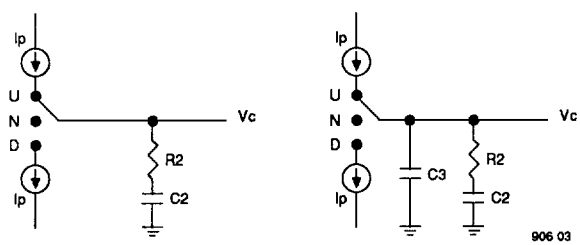


Figure 3. Charge Pumps and Loop Filters

A1	A0	DESTINATION
0	0	P (D0–D1)
0	1	N (D0-D13)
1	0	M (D0–D13)
1	1	Reserved

Table 1.

Note: When writing to the P Register D2 to D13 = 0, see Table 2 for D0, D1 values.

D1	D0	DATA
0	0	÷1
0	1	÷2
1	0	÷4
1	1	÷8

Table 2.

Note: This table is for use with the P Register only.

D13	...	D3	D2	D1	D0	DATA
0		0	0	0	0	+1
0		0	0	0	1	+1
0		0	0	1	0	+2
0		0	1	0	0	+4
						⋮
1		0	0	0	0	+8192
	...					⋮
1		1	1	1	1	+16383

Table 3.

Note: This table is for use with the M and N register.

operation of the interface, there has to be exactly sixteen SCLK pulses within the $\overline{WR}$ high-to low and low to high transition period. After WR goes high, an additional 10 SCLK pulses are required to load the new data. Also, the first Write after a Power Up requires 10 SCLK pulses before WR goes low. After the 10 SCLK pulses, the user can read the data into the temporary register. Every read of a selected location should be preceded by a write into the same location. To read the data out, The $\overline{RD}$ signal should be pulled low. After sixteen clock pulses all the data inside the shift register will be clocked out of the I/O pin. The data appears at the output, on the rising edge of the shift clock (SCLK).

To avoid conflicts, the falling edge of the $\overline{RD}$ signal should be at least ten SCLK periods away from the rising edge of $\overline{WR}$.

The same rule applies to consecutive write cycles. The serial interface timing diagram is shown in Figure 6 and Figure 7.

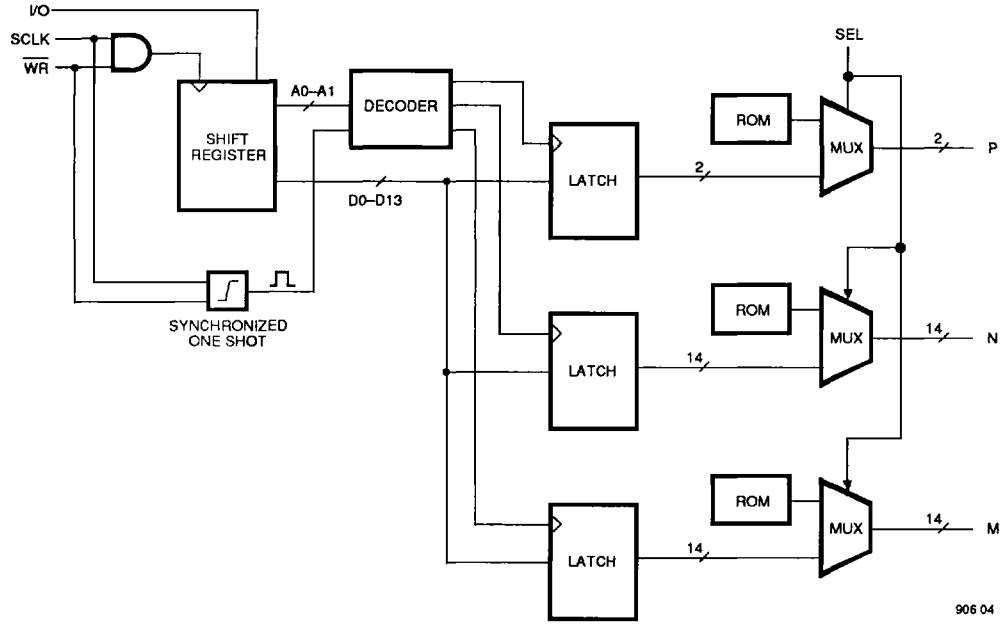


Figure 4. Storage Unit For Programming of Dividers

CRYSTAL CONNECTION

Figure 5 shows a typical crystal implementation. The capacitors C1 and C2 have a range of 20pF to 5 pF. Depending on the frequency of the crystal, it is recommended to use maximum 20 pF for frequencies lower than 10 MHz, and for frequencies above 10 MHz capacitor values between 10pF and 5 pF are recommended.

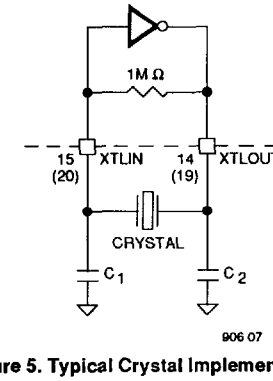


Figure 5. Typical Crystal Implementation

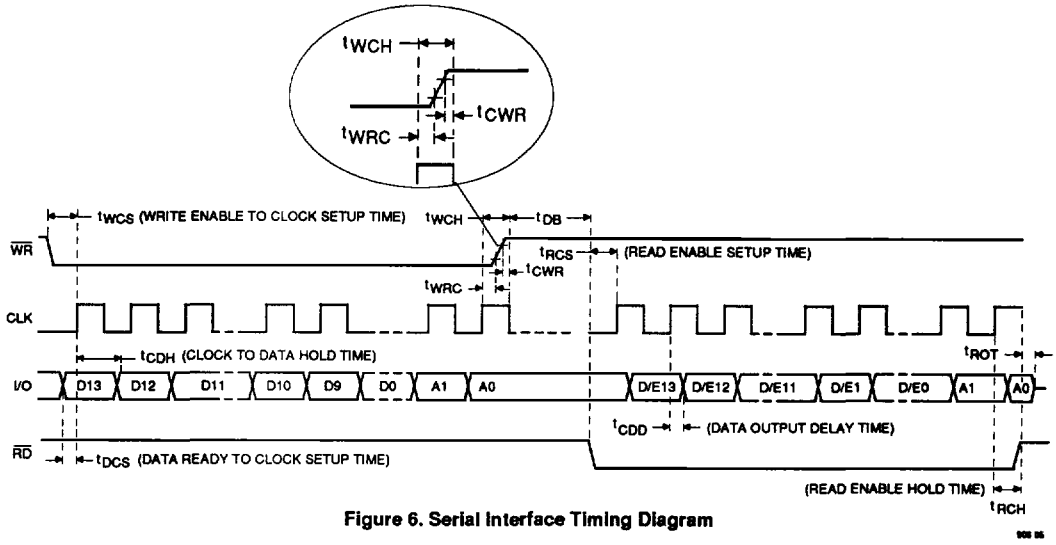


Figure 6. Serial Interface Timing Diagram

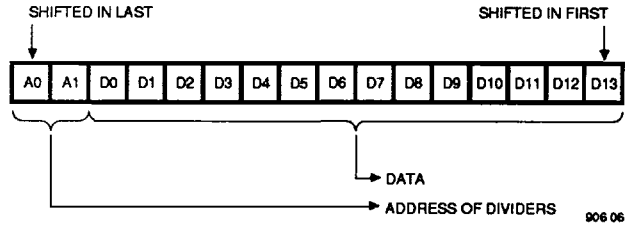


Figure 7. Address/Data Allocations for the Input Bits

SERIAL INPUT TIMING

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{WCS}	Write Enable to Clock Set Up Time	50			ns
t_{DCS}	Data Ready to Clock Set-Up Time	50			ns
t_{CDH}	Clock to Data Hold Time	50			ns
t_{CWR}	Clock to Write Enable Rising Edge	40			ns
t_{WRC}	Write Enable Rising Edge to Clock	40			ns
t_{WCH}	Clock to Write Enable Hold Time	50			ns
t_{DB}	The number of SCLK periods after Power Up, before the first Write Cycle and after aech Write Cycle	10			SCLK Periods
t_{RCS}	Read Enable to Clock Set-up Time	50			ns
t_{CDD}	Clock to Data Output Delay Time			75	ns
t_{RCH}	Clock to Read Enable Hold Time	75			ns
SCLK	Clock Frequency			5	MHz
t_{ROT}	Read Enable High to Output Tristate			50	ns

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2 and 3)

Supply Voltage, Vcc–GND	6 V
DC Input Voltage	GND–0.5 to Vcc +0.5 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 sec.)	300°C

OPERATING CONDITIONS

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNITS
Ta	Ambient Temperature		0		70	°C
Vcc	Positive Supply Voltage		4.5	5.0	5.5	V
GND	Ground			0		V
XTLIN, XTLOUT	Crystal Frequency			20	30	MHz
Tr,Tf	Input Rise or Fall Time				50	ns

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package –12mW/°C from 65–85°C

DC ELECTRICAL CHARACTERISTICS (Ta = 0 TO 70°C, DVcc = 5V ±10%, AVcc = 5V ±10%)

PARAM.	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNITS
Icc	Quiescent Current			30		mA
Vih	High Level Input Voltage, All Inputs		2.2			V
Vil	Low Level Input Voltage, All Inputs				.8	V
Voh	High Level Output, All Outputs Except XTLOUT (Ioh = 0.5 mA) (Ioh = 100 µA)		 2.4 4.5			 V V
Vol	Low Level Output, All Outputs Except XTLOUT (Iol = 1.6 mA) (Iol = 100 µA)				 0.6 0.2	 V V
Voh	High Level Output XTLOUT (Ioh = 20 µA)		 4			 V
Vol	Low Level Output XTLOUT (Iol = 20 µA)				 0.2	 V