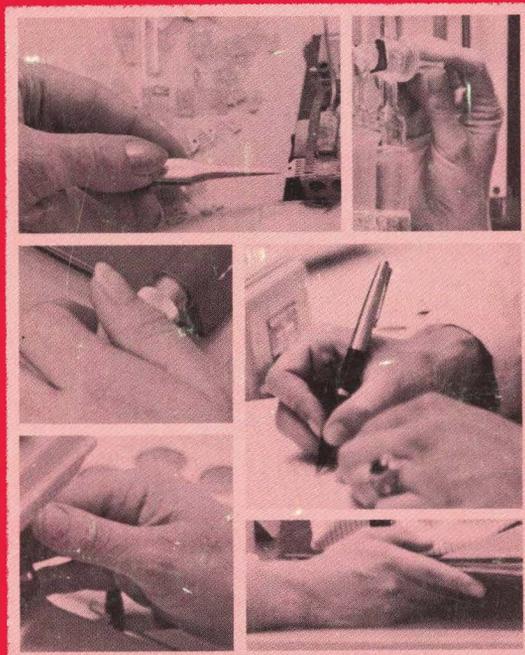


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SEPTEMBER 1969



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SECTION 1
INTRODUCTION TO DIGITAL LOGIC



APPLICATIONS MEMO

GUIDELINES FOR SELECTING A DIGITAL INTEGRATED CIRCUIT FAMILY

This memo discusses some guidelines for selecting a digital integrated circuit logic family. The discussion will include speed requirements, power consumption, noise margins and immunity, fan-out, some circuit characteristics, binaries, interfamily compatibility, and, in general, how these factors relate to cost.

The speed power trade-offs is an eternal problem. The speed power relationship is graphically illustrated in Figure 1 and indicates, in general, that higher speed circuits consume more power. If you need very high speed or very low power, the circuit selection is quite simple; there is a limited number of very low power or very high speed circuits available. Because the bulk of the circuits in use today are in the medium to high speed range, this discussion will be confined to these kinds of circuits. Specifically, as referenced to Figure 1, we will talk about those circuits with delays between 5ns and 35ns, power consumptions between 5mW and 25mW. An inter-

esting thing to note is the reasonable straight line formed by the TTL devices (400, 8400, SUHL I, 5400, 8800, SUHL II) which indicates that a speed/power trade-off in TTL exists. TTL employs a very low output impedance which provides a fast rise time that contributes to a relatively small portion of the overall switching time. Therefore, additional power consumed in the circuit to reduce internal delay is effective in reducing overall delays. In DTL a very large portion of the switching delay is slow rise time due to a high impedance output which is significantly affected by load capacitance. Therefore, one may put more power into the DTL circuit to reduce the inherent or internal circuit delay without appreciably affecting the overall switching time. The plot of pair delay versus capacitance shown in Figure 2 illustrates the effect of load capacitance on different output structure switching times. The low output impedance circuits TTL, Utilogic (active pull-ups), and RTL (small resistor pull-up) are relatively unaffected by load capacitance. The high output impedance (2 to 6K) DTL circuits are significantly affected by load capacitance.

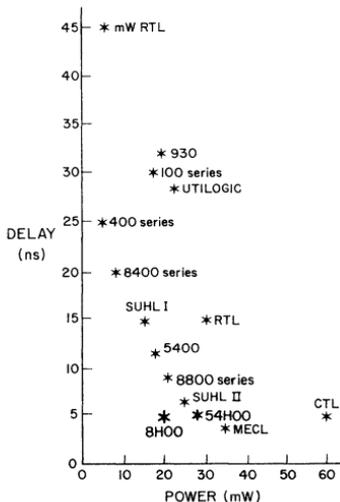


Figure 1 Switching Speed vs Power Consumption

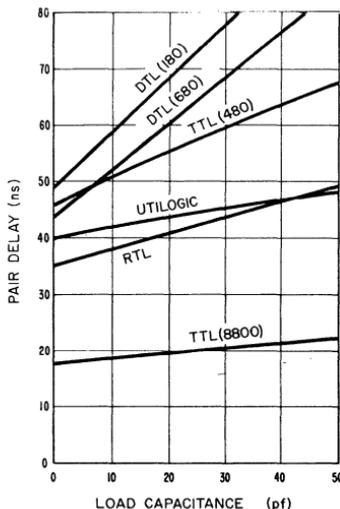


Figure 2 Switching Speed vs Load Capacitance

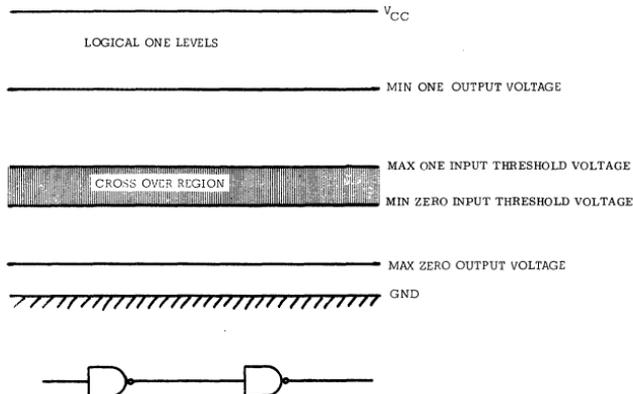


Figure 3 DC Noise Margin

Noise margins and immunity are important considerations for selecting a digital integrated circuit family. A qualitative representation of DC noise margin is shown graphically on Figure 3. The minimum logical ZERO level (assuming positive logic) DC noise margin is the difference between the minimum ZERO input threshold voltage and the maximum ZERO output voltage. The minimum logical ONE level DC noise margin is the difference between the minimum ONE output voltage and the maximum ONE input threshold voltage. The cross-over region has a finite width since a gate does not have infinite gain and the threshold voltage is an inverse function of temperature. The maximum ZERO level and the minimum ONE level should be determined under maximum fan-out loading.

AC noise margin is not so easily determined as is DC noise margin. AC noise margin is a function of both amplitude and duration, i. e., very narrow pulses will require larger amplitudes at a circuit input to affect its output. A measurement of AC noise margin (ZERO level) is shown on Figure 4 for various logic circuit types. Any combination of noise pulse width and amplitude that lies on or above a given curve will cause an incorrect output state. Notice that the medium speed 100 series DTL will reject wider pulses than the high speed 8800 series TTL (at a given pulse amplitude), i. e., narrow noise pulses will tend to affect the circuits as a direct function of the circuit speed. The noise pulse amplitude approaches the DC noise margin

for "wide" pulse widths (greater than 25ns or 30ns). The numerical values shown on the graph are typical values.

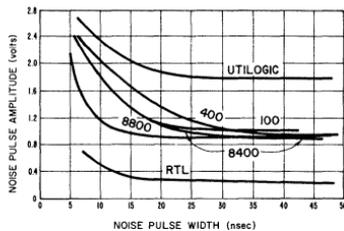


Figure 4 AC Noise Margin

AC noise immunity is a measure of the ability of a circuit to reject noise from other signal lines, external noise sources, and transients on the power distribution lines to the circuits. An accurate measurement of AC noise immunity is not easily obtained. Generally, cross-coupling of signals and external noise susceptibility will depend on the impedance of a circuit for a given logic state. Noise may be cross-coupled as shown in Figure 5. Two signal lines that are close together will have a certain amount of stray capacitance between them. The waveform shows the effect of the capacitance between the lines. Assume that the output of gate A is high and that gate B is switching at some frequency. The stray

capacitance will be discharged when gate B is logical ONE (since both sides of the capacitance are at the same level, logical ONE). When the output of gate B is switched to ZERO, the output of gate A, which is the input to gate C, will be momentarily lowered since the voltage across a capacitor cannot change instantaneously. The amount of change and duration of the disturbance at the input to gate C will be determined by the fall time of gate B, stray capacitance, and the output impedance of gate A in parallel with the input impedance to gate C. If the input to gate C is below threshold long enough (depending on the speed of gates C and D), the memory latch consisting of gates C and D will be set to the incorrect state. Thus, circuits with high impedance outputs are more susceptible to cross-coupling and external noise sources than circuits with low impedance outputs. The ZERO level logic state impedance is usually (DTL, Utilogic, TTL, RTL) that of a saturated transistor, hence it is not very susceptible to this type of noise. The ONE level logic state impedance may be a resistor or an active structure so that ONE level impedances vary with the logic circuit types. The active pull-up structure is usually a much lower output impedance than the resistor pull-up. TTL and Utilogic circuits employ active pull-up structures, DTL and RTL employ resistor pull-up except for DTL line drivers which employ active pull-up.

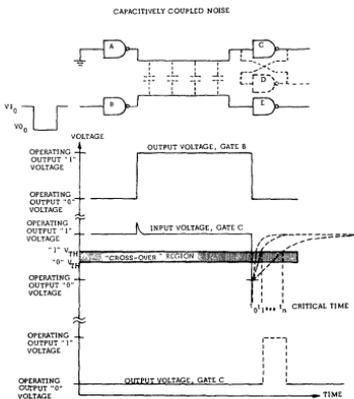


Figure 5 Cross Coupled Noise

System fabrication techniques will depend on the type of logic circuit being used. DTL and Utilogic do not require special fabrication

techniques because of slower operating speeds and high noise margins. TTL, RTL and CML (Current Mode Logic) may require special fabrication techniques such as ground planes, short lead lengths, and better power supply distribution due to high speed and low noise margins (RTL, CML). The effect of fabrication techniques may be seen in Figure 6. Waveform (a) was generated by high speed TTL, (b) low power TTL, and (c) DTL. Each circuit type was connected as a ring oscillator on a breadboard without a ground plane, and the circuits were interconnected with leads several inches in length. The high speed TTL exhibits ringing on the waveform while the low power TTL and DTL are not affected by the

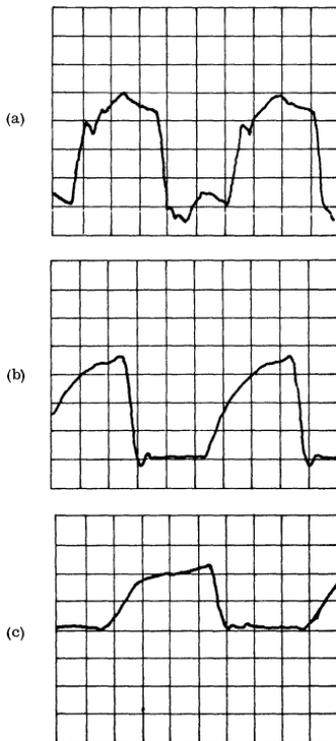


Figure 6 TTL, Low Power TTL, DTL Waveforms

set-up. The high speed TTL waveforms may be improved as shown in Figure 7 (b), 7 (a) is same as 6 (a). The improvement was obtained by using a ground plane, wide power distribution lines, and short interconnecting leads. These special techniques will result in an increase in overall system cost, hence if high speed is not required the slower high noise margin circuits should be considered.

Up to now this discussion has been about general considerations. Specific gate circuits and binary elements will now be discussed. The specific gate circuit types are DTL and TTL. A basic DTL circuit schematic is shown in Figure 8. If any diode input is logical ZERO (near ground), current will be diverted from the transistors and they will be turned off, resulting in a logical ONE (near V_{CC}) output. When all diode inputs are logical ONE the transistors will turn on resulting in a logical ZERO at the output. This gate implements the basic NAND logic function for positive logic. The fan-in of the DTL gate is easily expanded by simply adding diodes to the node point. Outputs may be connected together to perform collector logic as shown in Figure 9. Collector logic provides a free level of logic which reduces parts count and propagation delay for some applications. The resistor pull-up will result in relatively long turn-off times when driving capacitive loads as was mentioned earlier in this discussion. Internal isolation diodes are shown on the circuit schematic and care should be taken to limit current if these diodes become forward biased at interface points. The logic input diodes are collector base junctions which have fairly high breakdown voltages.

A basic TTL gate circuit schematic is shown in Figure 10. Any input that is logical ZERO will divert current from the pull-down transistor and provide base current to the pull-up transistors resulting in a logical ONE at the output. When all inputs are logical ONE, the pull-down transistor will be turned on and the pull-up transistors will be turned off resulting in a logical ZERO output. This gate also implements the basic NAND logic function for positive logic. The fan-in of the multiple emitter input is not easily expanded, hence most TTL gates do not have an expansion capability. The active pull-up output structure does not allow collector logic because large currents would result if one or more outputs were logical ONE and one or more outputs were logical ZERO simultaneously. The active pull-up structure allows the TTL gate to have relatively fast turn-off times even when driving capacitive loads. During each switching transition the pull-up and pull-down transistors are on simultaneously for a short period of time. This

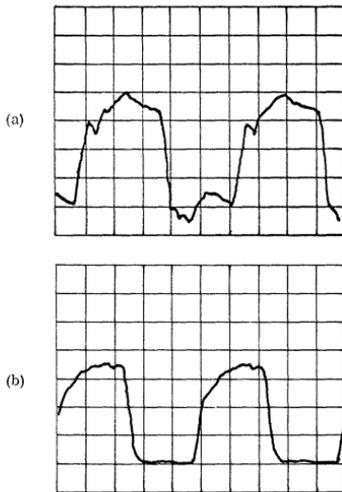


Figure 7 TTL Waveforms

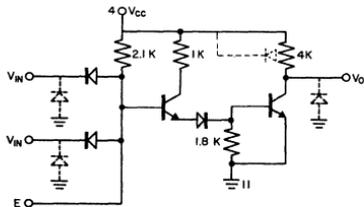


Figure 8 DTL Gate Schematic

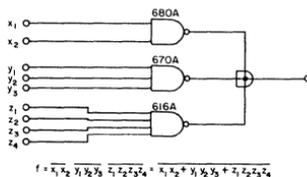


Figure 9 Collector Logic

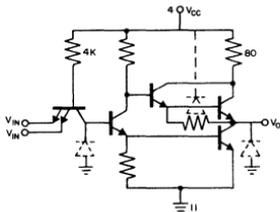


Figure 10 TTL Gate Schematic

"overlapping" causes the current spiking associated with high speed TTL circuits. An example of current spiking is shown in Figure 11 for a developmental high speed TTL gate. Current spiking will generate noise on the power supply distribution busses and also result in increased power consumption at high frequencies. Unused inputs on the multiple emitter transistor should be treated with care. When an unused input is left open, the noise immunity may be degraded and stray capacitance to ground may affect the switching speed of the element under certain conditions. Unused inputs tied to a driven input yields the best circuit speed, however, the additional logical ONE input leakage current required may significantly reduce the ONE level noise margin. The unused inputs may be tied to V_{CC} which will yield good noise immunity and speed, but may result in an input latchup problem. A voltage transient on the power supply V_{CC} line or ringing on a ZERO level input may momentarily increase the input voltage difference above the emitter breakdown voltage. Latchup will occur if the steady state latch voltage is less than the power supply voltage. Delatching of the circuit will require switching the ZERO level input to a ONE level or a reduction of the power supply voltage. The input breakdown characteristics for the TTL gate described earlier is shown in Figure 12. This gate was designed to have a steady state latch voltage in excess of the maximum operating V_{CC} (5.5V) to allow connection of unused inputs to V_{CC} .

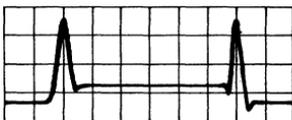


Figure 11 TTL Current Spiking

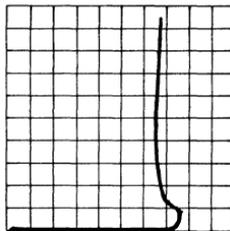


Figure 12 TTL Input Latchup

An important part of any digital logic family is the binary element. A simple bistable memory element may be implemented with gates as shown in Figure 13. This memory element is quite useful for parallel entry storage registers, however, it will not function in applications requiring synchronous clocking. The problem exists because the state on the R-S inputs will be transferred to the output soon after the control line becomes a logical ONE, and any change of state on the R-S inputs will be transferred to the output as long as the control input is logical ONE. Shift registers implemented with this type of binary will all be in the same state after the first clock pulse since the information to the input binary will propagate through the entire register (assuming the clock pulse is as wide as the register propagation delay). Counter circuits cannot be implemented with this type of binary for the same basic reasons. Various methods for solving this problem include master slave and AC clock coupling techniques.

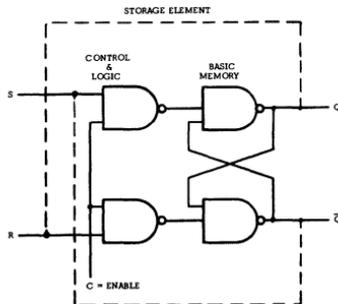


Figure 13 Basic Memory Element

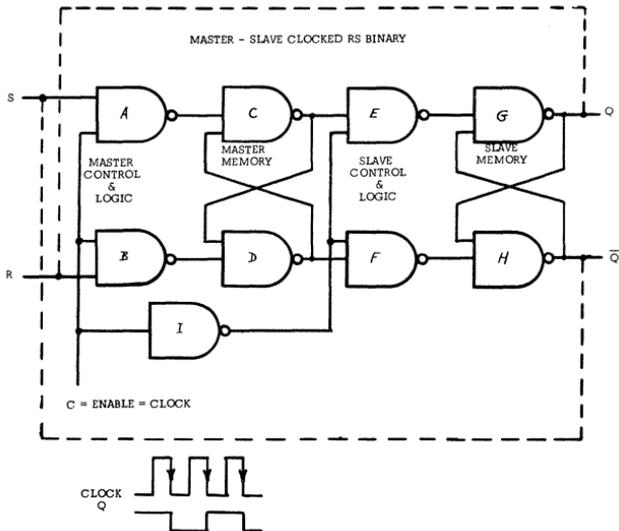


Figure 14 Master Slave Binary

A basic master slave binary is shown in Figure 14 and consists primarily of two simple memory elements. The master memory consists of gates C and D with control gates A and B, the slave memory consists of gates G and H with control gates E and F. An inverting element (I) is used to provide the complement of the clock (control) input to the slave control gates. When the clock input is logical ZERO, the state of the master memory is transferred into the slave memory via control gates E and F since the output inverter I is logical ONE. The inputs to the master memory are disabled at this time by control gates A and B. Changing the clock pulse to logical ONE will transfer the information on the R-S lines into the master memory, the output of inverter I will now be logical ZERO, disconnecting the master memory from the slave memory (by gates E and F) so long as the clock input remains logical ONE. Returning the clock input to logical ZERO will transfer the state of the master memory to the slave memory and disable the inputs to the master memory. Notice that the output of the binary cannot begin to change until the trailing edge of the clock occurs and at that time the R-S inputs will be locked out. It is

important that the voltage level at which the inverter switches is significantly lower than the voltage level which allows information from the R-S lines to enter the master memory to insure good noise immunity.

The AC clocking technique employs a basic memory element and a clock steering network as shown in Figure 15. The data inputs, R_C and S_C , are enabled with logical ZERO levels. A logical ZERO on a data input allows the associated capacitor to charge to the clock voltage level (logical ONE). A logical ONE on a data input allows the clock input (when logical ONE) to only discharge the capacitor. A transition on the clock line from a logical ONE to ZERO will turn off the gate associated with the charged capacitor. The output of this gate (which is now logical ONE) is applied to the input of the second gate. The logical ONE on the input to the second gate will cause its output to be logical ZERO which is connected back to the first gate to maintain its output at logical ONE providing a stable memory condition. The steering network is another method to implement trailing edge triggering, i. e., the output does not begin to change until the end of the clock pulse.

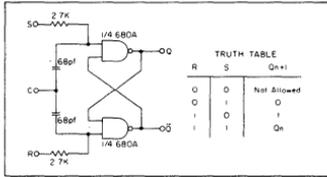


Figure 15 AC Binary

In system usage, master slave type binaries may have better clock line noise immunity, but will consume more power due to the larger number of gates. AC coupled binaries tend to require less chip area even though the capacitors are relatively large. Dual AC coupled binaries on a single chip are available as standard parts.

The binary elements just discussed are the R-S (Reset-Set) type. Other types of binaries available in integrated circuits are the J-K and D. Truth tables for R-S, J-K, D and T type binary elements are shown in Figure 16. The R-S binary truth table is for AC coupled elements which have inverting inputs. The J-K truth table is essentially the same as the R-S except for the condition when both inputs are activated simultaneously. This condition will complement the J-K at clock time, but is not allowed for the R-S. The D (Delay) binary element delays the input by one clock time. The truth table for the T binary element is the same as the first and last entry of the J-K, hence the T function is easily implemented with the J-K binary by connecting the J-K lines together.

Most applications may be accomplished with any of the binary elements, however, the efficiency of implementation may differ. Implementation of shift registers with the various binaries is shown in Figure 17. The number of elements is equal in all cases, however, the interconnections are simpler for the D type binary. Binary ripple counter implementation is shown in Figure 18. Again the number of elements is the same. A synchronous counter design is shown in Figure 19. The T type binary is most efficient for this application; however, the J-K type binary easily implements the T function as was mentioned earlier. The inverting inputs of the R-S binaries may be used to an advantage with NAND logic if an AND, or AND-OR, function is required on an input as is shown in Figure 20.

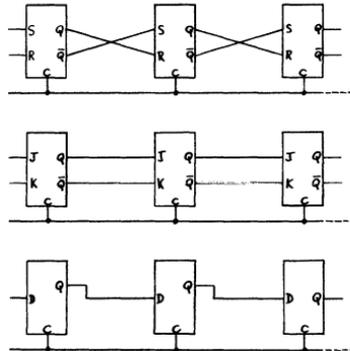


Figure 17 Shift Registers

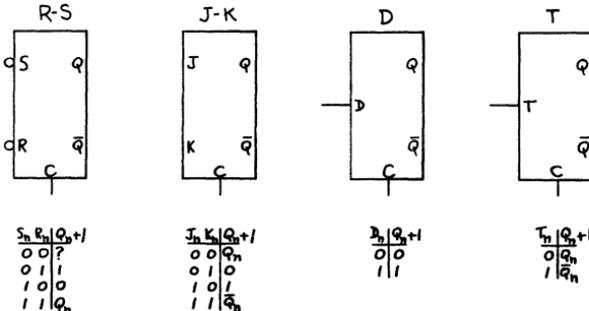


Figure 16 Binary Truth Tables

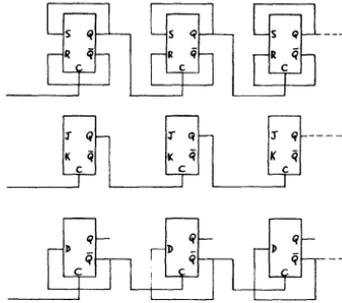


Figure 18 Ripple Counters

BINARY SYNCHRONOUS COUNTERS

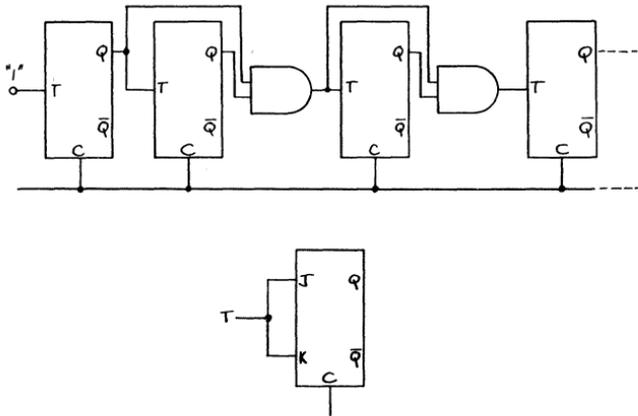


Figure 19 Synchronous Counters

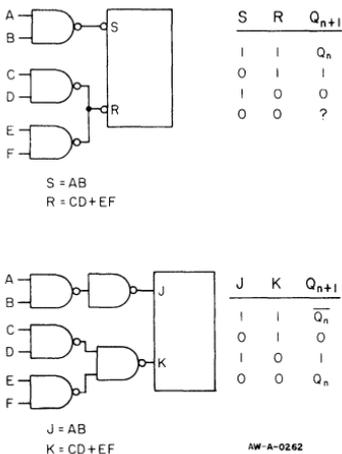


Figure 20 Inverting Binary Input Applications

Current sinking logic circuits such as DTL, low power TTL, and high speed TTL are basically compatible. An overall system design may be optimized by selecting devices from the various logic types most suitable to subsystem requirements with respect to speed, power, can count, etc. A designer may generate a set of rules from data sheets which allows interfacing of the various circuit types. However, difficulty arises when the various circuit types are characterized at different power supply voltages. Some manufacturers of digital integrated circuits are presently offering compatibly characterized logic families that incorporate elements of more than one circuit type. Examples of these compatible logic families are: Signetic's 8000 DCL (Designers' Choice Logic) which includes low power DTL/TTL, medium speed TTL, high speed TTL, interface devices, and MSI arrays.

The most important factors for selecting a digital logic family have now been discussed. These factors are tabulated in the relative comparison table of Figure 21. RTL is a

simple circuit which yields very low cost and medium speed, but sacrifices noise margins and fan-outs while consuming considerable power. DTL is a more complex low price circuit for medium speed systems which yields high noise margins with good fan-outs at low power. Utilogic was designed for optimum noise margins and high fan-outs in the medium speed range. Low power TTL provides medium speed operation with good noise margins and fan-outs at very low power consumption. TTL circuits provide high noise margins and fan-outs at high speeds. CML provides very high speed at very low noise margins and is used primarily in very high speed applications.

The cost to implement row on the chart is based on logic flexibility, parts cost and fabrication costs. RTL parts cost is very low, but the limited fan-out and high fabrication cost result in an overall medium to high cost system. DTL parts cost is low, logic flexibility is good, and fabrication cost is low resulting in low overall system cost. Utilogic parts cost is high, but very good logic flexibility and low fabrication costs result in a low overall system cost. Low power TTL parts cost is low, logic flexibility is fair to good, and fabrication cost is low resulting in an overall low system cost. TTL price is low, logic flexibility is somewhat limited, and fabrication costs are high resulting in a high overall system cost. CML parts price is high, flexibility is good, but fabrication costs are very high resulting in a very high overall system cost.

The factors discussed here should be related to a given system requirement to determine the digital logic family most suitable.

AW-A-0260

	DTL	UTILOGIC	TTL	TTL (low power)	RTL	CML
FAN OUT	GOOD	HIGH	HIGH	GOOD	LOW	HIGH
NOISE MARGINS	HIGH	EXCELLENT	HIGH	HIGH	LOW	VERY LOW
NOISE GENERATED	LOW	LOW	HIGH	LOW	LOW	VERY LOW
SPEED	MEDIUM	MEDIUM	HIGH TO VERY HIGH	MEDIUM	MEDIUM	VERY HIGH
POWER	LOW	MEDIUM	HIGH	VERY LOW	MEDIUM	VERY HIGH
COST TO IMPLEMENT	LOW	LOW	HIGH	LOW	HIGH	VERY HIGH

Figure 21 Relative Comparison Table



APPLICATIONS MEMO

NOISE IMMUNITY

Who, What, When, Where and Why

Many people have searched for a superior logic family which satisfies these questions. There are two specific areas of concern. These are the basic DC or common mode conditions and the dynamic or transient conditions. Either of these might permit propagation of an undesirable function through a logic system.

The common mode problems generally exist at interface locations and can be worsened with improperly designed ground systems which result in common mode transients. Though the DC problems are complex and of significant importance, they are well understood and generally limit conditions can be accounted for within the data sheet guarantees.

The common mode problems may be engineered to insignificance but the problems of engineering the physical problems of a dynamic solution are quite often impractical for logic systems. Let's consider what happens when gates are subjected to dynamic noise conditions. This by far is the most significant term for satisfactory system operation. Consider a gate connected as in Figure I, and an input frequency applied. A questionable output condition will exist for this circuit if the circuit coupling capacitance is sufficiently large.

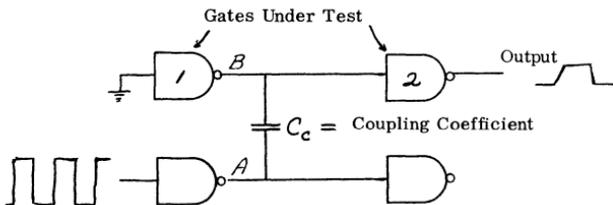


Figure I

The gate in question has a finite dynamic characteristic (T_{pd}). This is typically shown in Figure II. The transient induced will have a specific time constant. If the time below V_{th} for this transient is less than the gate propagation delay of the circuit, no output response will be seen. If the induced transient (τ_2) is greater than that of T_{pd} , then the gate will pass the signal along the logic network with a pulse width of τ_2 . The equation which must be satisfied can generally be described by the following:

$$\tau = R_0 C = k \left(\frac{V_{01}}{V_{th}} \right) T_{pd}$$

Where: R_o = Gate output "1" level impedance for gate No.1
 T_{pd} = Gate propagation delay of gate No. 2
 V_{th} = Voltage threshold of gate No. 2
 V_{01} = Voltage output of gate No. 1

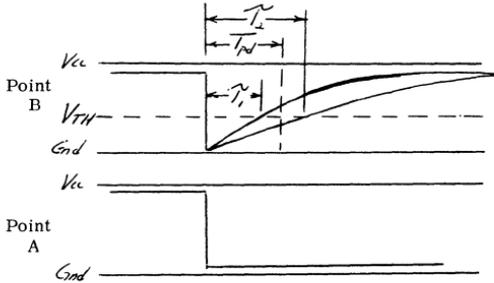


Figure II

A comparison of all gates may be made using the following equations:

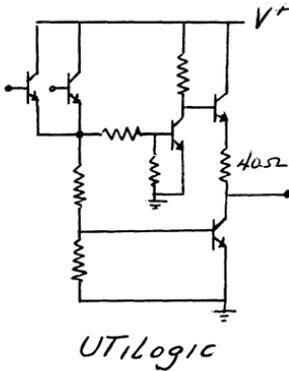
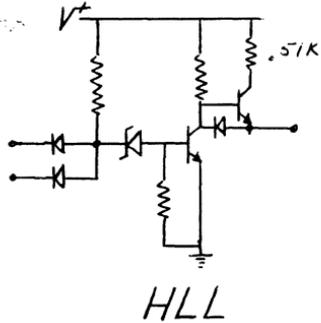
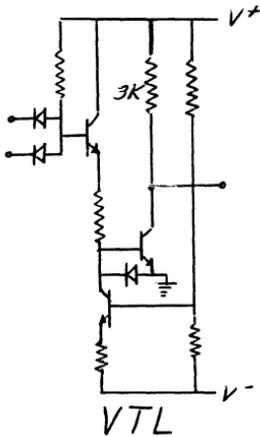
$$C = \left(\frac{V_{01}}{V_{th}} \right) \left(\frac{T_{pd}}{R_o} \right)$$

The larger the value of the coupling coefficient (C) the less noise susceptible a particular gate will be. The equation above indicates the following additional characteristics:

1. It can be seen that the lower the output impedance of the device the better the overall characteristics of the system.
2. It can also be seen that the larger the propagation delay the better the noise rejection for the system.
3. The ratio of gate supply voltage to threshold voltage is an important term. To improve dynamic coupling between gates the ratio of V_{01} gate output voltage to threshold voltage must be increased. Thus it is of little value in the dynamic analysis to have high level thresholds with high supply voltage if the ratio is not improved.

Some gates utilize high levels to decrease their noise susceptibility but have achieved no improvement in their dynamic noise coupling characteristic.

Some comparative examples of noise susceptibility are shown using the coupling coefficient equation for several high threshold gates and also the Utilogic gate. The gate schematic, the calculated coupling coefficient and per unit comparison of each gate are compared to the Utilogic gate.



Gate	C	Per Unit Comparison
Utilogic	1150×10^{-12}	1
HLL	237×10^{-12}	1/4.8
VTL	27.3×10^{-12}	1/42

This shows that the Utilogic gate is approximately 5 times better than HLL and 40 times better than VTL.



APPLICATIONS MEMO

GLOSSARY OF LOGIC TERMS

A

Abbreviations for Logic Forms:

CML:	Current - Mode - Logic
CTL:	Complementary - Transistor - Logic
DCL:	Designer's Choice Logic (SIGNETICS trademark)
DCTL:	Direct - Coupled - Transistor - Logic
DTL:	Diode - Transistor - Logic
ECL:	Emitter - Coupled - Logic
RCTL:	Resistor - Capacitor - Transistor - Logic
RTL:	Resistor - Transistor - Logic
TTL (T ² L):	Transistor - Transistor - Logic
UTILOGIC:	Trademark for SIGNETICS-developed Industrial logic form.

Accumulator - A register in an arithmetic unit for performance of arithmetical and logic functions such as addition and shifting.

Adder - Full Adder: A device for performing the sum with carry of two binary digits and carry of a previous operation.

- Half Adder: A device for performing the addition and carry of two binary digits without a facility to include a previous carry.

Alphanumeric - A combination of alphabetic characters and digital numbers.

AND - Logic implication generating a ONE output when all inputs are ONE. It is sufficient, if any input is ZERO to generate a ZERO. Example:

logic equation

$$A \cdot B \cdot C = D$$

Truth Table

logic symbol



A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

If A or B or C or all are ZERO, then D cannot be ONE (TRUE):

$$\bar{A} + \bar{B} + \bar{C} = \bar{D}$$

Astable Multivibrator – An oscillator generally with complementary outputs; no trigger is necessary.

Asynchronous Operation – Generally an operation that is started by a completion signal from a previous operation. It then proceeds at the maximum speed of the circuits until finished and generates its own completion signal.

B

Bar – Used to symbolize the inverse, or complement, of a function.

Example: Inversion of A is " \bar{A} ", read "A bar" or "A not".

Binary - Coded - Decimal: Code that covers the number 1, 2, 3, 4, 5, 6, 7, 8, 9, and 0 in binary notation using 4 binary digits. Examples:

Count Sequence for 8-4-2-1 BCD Code

2-4-2-1 Code

0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0
2	0	0	1	0	0	0	1
3	0	0	1	1	0	0	1
4	0	1	0	0	1	0	1
5	0	1	0	1	1	0	1
6	0	1	1	0	1	1	0
7	0	1	1	1	1	1	0
8	1	0	0	0	1	1	1
9	1	0	0	1	1	1	1
0	0	0	0	0	0	0	0

BCD – Originally an abbreviation for Binary - Coded - Decimal. Common practice is to call 8-4-2-1 BCD; all other codes, as 2-4-2-1, are called out.

Binary Number – Each digit of a binary number has only one of two possible states, which usually are called 0 and 1; each digit represents a number with the radix 2.

Example: 1 0 1 1 1 (binary)

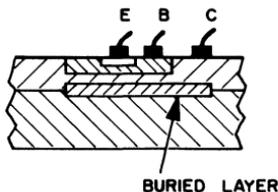
$$= 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 \quad (\text{radix } 2)$$
$$= 16 + 0 + 4 + 2 + 1 = 23$$

Bistable Multivibrator - a Flip-Flop, or Binary – A circuit with two stable states.

Bit – Binary Digit: The smallest part of information in a binary notation system. A bit is either a ONE or a ZERO.

Boolean Algebra – Algebraic rules in manipulating logic equations.

Buried Layer – A layer of heavily doped material (high conductivity) under the collector region, generally applied to reduce the collector saturation resistance. This layer is diffused on the wafer before the epitaxial growth.



Buffer – Usually an isolation stage between input and output of a digital circuit. Most of the Signetics flip-flops employ output buffering

- An intermediate storage device in a computer.
- Term sometimes used for a line driving element with high capacity loading capability and/or high fan-out.

Buss (Line) — A common connection line for distribution of ground, power supply or signals.

Byte — An 8-bit grouping of bits. May contain two 4-bit characters or some other combinations of bit sub-grouping to facilitate information handling.

C

Carry — In the addition of two binary digits, a carry is generated when the sum exceeds the radix 2.

Example:

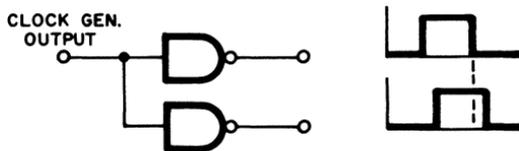
0 plus 0	= 0
1 plus 0	= 1
0 plus 1	= 1
1 plus 1	= 0 with a carry of "1" to the next higher digit.

Character — A 4-bit decimal or 6-bit alpha-numeric code.

Clear — Setting a number of memory elements or binaries to the ZERO state. Same as Reset.

Clock — Basic timing device in a system, usually providing a continuous chain of timing pulses (clock pulses).

Clock Skew — A phase shift in a single clock distribution system. Can be introduced by different delays in clock driving elements and/or by distribution paths. Excessive skew will cause malfunction.



Clock Stagger — A term generally applied to the time separation between clock pulses in a multi-phase clock system. It may be applied to the voltage separation of the clock thresholds in a flip flop such as the common DC-clock Master-Slave devices.

Coder — A device for converting data from one notation system to another.

Collector Logic — See Wired AND

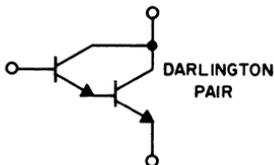
Comparator — Digitally, an arrangement of gates that checks two signals or numbers for equality and usually indicates "equality," "less than," "greater than". The most common types indicate "equality" only. An analog comparator compares two input levels and indicates "less than" or "greater than."

Complement — The logical inversion of a Boolean function; see DeMorgan's theorem. Used to express negative numbers to facilitate subtraction.

Core Memory — Storage device consisting of ferromagnetic cores with provisions to enter data and to read data. A ferromagnetic core has two stable states which are used to store a binary digit.

D

Darlington - Pair — Two transistors connected together according to figure below to obtain higher gain and higher input impedance.



Debugging — Act of checking system operation to identify malfunctions.

De Morgan's Theorem — The theorem states that the inversion of a series of AND implications is equal to the same series of inverted OR implications, or the inversion of a series of OR implications is equal the same series of inverted AND implications.

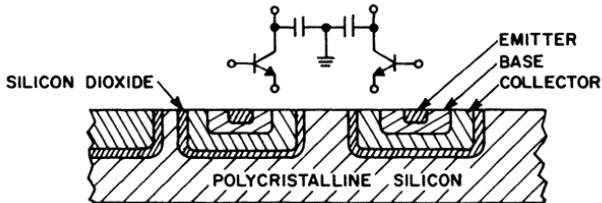
$$\overline{A \cdot B \cdot D} = \bar{A} + \bar{B} + \bar{C} \quad \overline{A + B + C} = \bar{A} \cdot \bar{B} \cdot \bar{C}$$

Die (Dice) or Chip — Tiny silicon block containing one or more circuit components (such as transistors, diodes, resistors, capacitors). A die may contain several circuit functions (e.g., Quadruple Gate).

Die Attach — Process of attaching by alloying the tiny silicon blocks to the mechanical support.

Die Sort — An electrical evaluation of the dice while in wafer form.

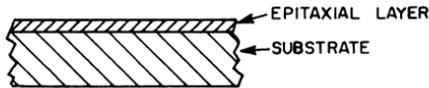
Dielectric Isolation — A process in which the individual components are separated through dielectric isolating layers (usually silicon dioxide).



Double Diffusion — See Isolation Diffusion.

E

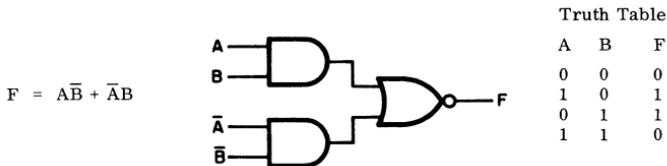
Epitaxial Growth — Depositing process of single crystal p or n - material or intrinsic silicon on a substrate.



Excess Three Code — A self-complementing BCD-Code. Any 8-4-2-1 BCD Code number might easily be transformed to an excess three number by adding a binary 3 (0011) to each number. If all zeros in a number are changed to ones and all ones to zeros, the nines complement of the number is obtained.

Excess Three Code	0	0011	5	1000
	1	0100	6	1001
	2	0101	7	1010
	3	0110	8	1011
	4	0111	9	1100

Exclusive - OR ($A \oplus B$) — (1) The function, either one, but not both, or A not equal B. (2) A name frequently given to the AND-NOR circuit (for example, 8840) since they are ideally suited for forming the function.



F

False — Statement for a ZERO in the Boolean Algebra.

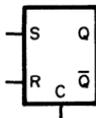
Fan In — Total number of inputs of a particular gate or function.

Fan Out — The number of loads connected to the output of a gate or function.

Flip-Flop — A circuit with two and only two stable states.

RS Flip-Flop — (see also Latch) Binary with set and reset inputs and the restriction that both inputs cannot be energized (0 for example shown in Truth Table) simultaneously because the resultant state will be indeterminate.

Q_{n+1} : Output state of the flip-flop one clock pulse (or one time increment) after the input combination appears.

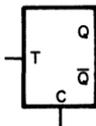


Truth Table
SE125, SE424

S	R	Q_{n+1}
1	1	Q
0	1	1
1	0	0
0	0	?

"0" enables inputs

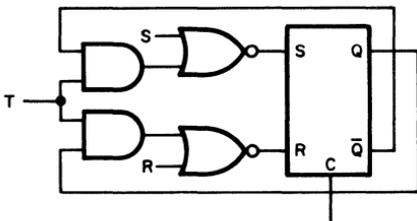
T Flip-Flop — Binary with a synchronous T-input; if T-input is high, flip-flop will toggle synchronously.



Truth Table

T^n	Q_{n+1}
0	Q^n
1	\bar{Q}^n

RST Flip-Flop — Binary with the feature of an RS and a T Flip-Flop.



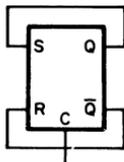
RST Derivation from RS

Truth Table

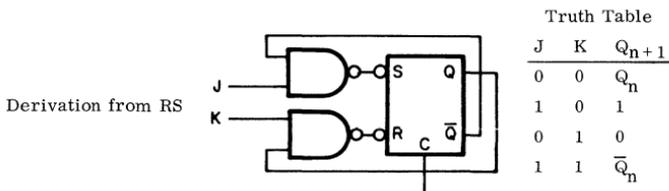
R^n	S^n	T^n	Q_{n+1}
0	0	0	Q^n
0	0	1	\bar{Q}^n
0	1	0	1
1	0	0	0
0	1	1	?
1	0	1	?
1	1	0	?
1	1	1	?

? = indeterminate

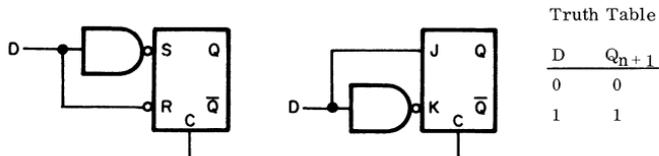
RS/T Flip-Flop — An RS Flip-Flop which may be connected to operate in toggling mode. The Signetics SE124 and SE424 are of this type.



J-K Flip-Flop — Binary with synchronous set and reset inputs; all input combinations permitted. Note that first three entries for J-K and RS are the same.



D Flip-Flop — Delay binary, the output shows the input signal at the next clock pulse (one clock pulse delayed).



Derivation from RS

Derivation from J-K

G

Gray Code — A binary code which is useful in input/output mechanisms (for example, shaft position encoders) because each number differs from the preceding one in one one digit.

Example: 0000
 0001
 0011
 0010
 0110
 0100
 0111
 0101, etc.

H

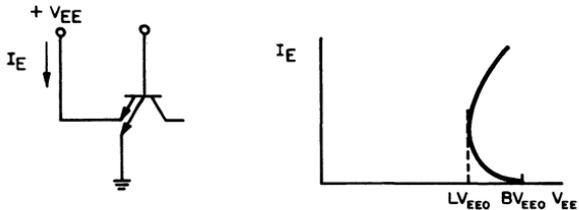
Holding Time — The period of time that the input states must remain after activation of the clock input.

Hybrid — A mating of two or more technologies or techniques, e.g.,

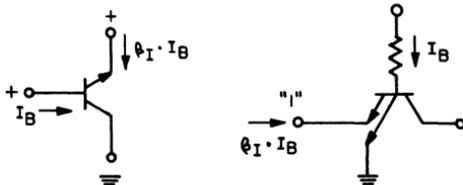
- (1) A class of integrated circuits where two or more silicon chips are interconnected within the package.
- (2) A combination of the monolithic and thin film methods of manufacture.

I

Input Latch (LV_{EEO}) — Minimum voltage between two emitters (multiple emitter) after breakdown.



Inverse BETA — Resulting gain of a transistor when the emitter and collector loads are physically reversed in a circuit's operation.



Inverter — A device or circuit to complement a Boolean Function (complement).

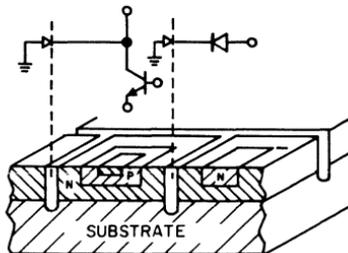


Buffer-Inverter



AND Gate + Inverter

Isolation Diffusion — Technique to separate the individual components within the monolithic silicon n-structure. P-diffused isolation zones form the p-n junctions which act as reverse biased diodes.



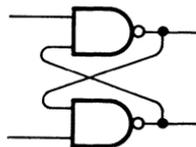
The transistors are double diffused; which means that the transistors are processed after the isolation diffusion by two diffusion steps.

Isolation Diode — p - n junctions, which surround all components, and act as biased diodes

L

Latch — Usually a feedback loop in a symmetrical digital circuit (such as a flip-flop) for retaining a state.

- A very simple RS flip-flop derived from two inverting gates:



Logic Depth/Logic Levels — Generally the number of driven gates in a synchronous system between an output of a memory element binary and the enabling input of the next memory element binary. The maximum allowable logic depth is determined through the switching delays of the gates and the input/output delays of the memory element binaries

Logic Levels — One of two possible states, ZERO or ONE.

Definition: for positive logic:	"UP" level = 1 TRUE
	"DOWN" level = 0 FALSE
for negative logic:	"DOWN" level = 1 TRUE
	"UP" level = 0 FALSE

LSB — Least Significant Bit—The lowest weighted digit of a binary number.

M

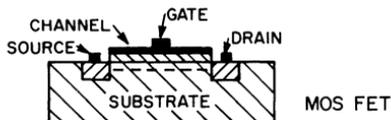
Master-Slave — A binary element containing two independent storage stages with a definite separation of the clock function to enter information to the master and to transfer it to the slave.

Signetics' SU and LU320, SP620 and SE125J are Master-Slave flip-flops.

Monolithic — Elements or circuits formed within a single semiconductor substrate.

Monostable Multivibrator: One-Shot — A circuit with one stable state, and one quasi-stable state. When triggered, the monostable changes its state and falls back to the stable state after a certain time determined by its RC time constant.

MOS — Metal Oxide Semiconductor — A field effect transistor whose gate is isolated from its channel through an oxide film. Also a capacitor formed by using similar techniques; semiconductor material forms one plate, metal (Al) the other plate, with oxide forming the dielectric.



Multiplex — Commutate: Sequentially connect a central unit or system to one of several channels.

MSB — Most Significant Bit — The highest weighted digit of a binary number.

N

NAND — Logic implication that produces the inverted AND function.

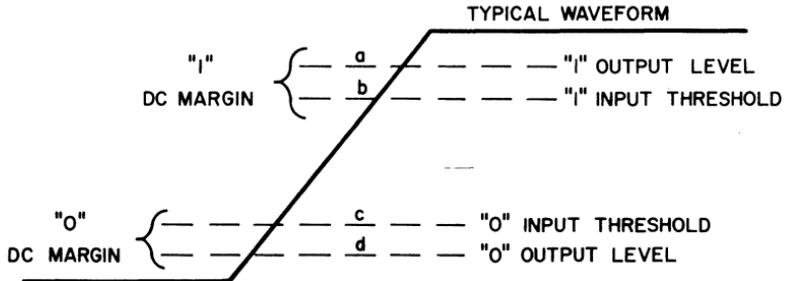
$$F = \overline{A \cdot B}$$



Truth Table

A	B	F
0	0	1
1	0	1
0	1	1
1	1	0

Noise Margin (DCM) — The DC difference between the levels required at an input and available at an output. For example, in the figure below; "1" DCM = a - b
"0" DCM = c - d



NOR — Logic implication that produces the inverted OR function.

$$F = \overline{A + B}$$



Truth Table

A	B	F
0	0	1
1	0	0
0	1	0
1	1	0

O

Octal Numbers — Octal Notation — A system using numbers with the radix 8.

One Shot — See Monostable.

OR (Inclusive) — Logic implication that produce at the output a ONE if at least one input is ONE.

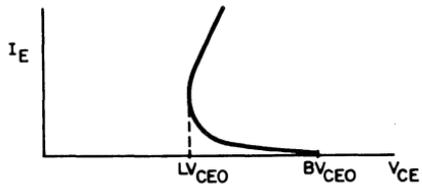
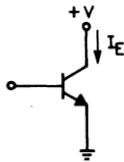
$$A + B = F$$



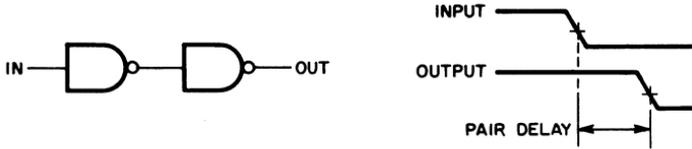
Truth Table

A	B	F
0	0	0
1	0	1
0	1	1
1	1	1

Output Latch (LV_{CEO}) — Minimum voltage after breakdown of collector-emitter.



Pair Delay — Propagation delay over two inverting stages.



Parallel Mode — The operation is performed for all binary digits simultaneously.

For example, in a register, read-in and read-out occur simultaneously for all digits contained in the register. Usually parallel mode requires more equipment than series mode, but speeds up the operation.

Parity Check — A simple kind of error-detecting scheme that requires an additional parity bit for each set of binary data. The binary set is always brought to an even (or odd) number of one digits with the parity bit before transfer operations and storage. The parity is tested after data transfers and storage readouts to check for errors that may have occurred during these operations.

Propagation Delay (t_{pd}) — Average propagation time per stage.

$$t_{pd} = \frac{1/\text{frequency}}{2 \times \text{no. stages}}$$



Pull-Down Resistor — Generally a resistor connected to ground or a negative voltage, for example, from the base of a transistor to a negative voltage.

Pull-Up Resistor — Generally a resistor connected to the positive supply voltage. For example, from V_{CC} to the output collector (such as in SE180).

Pull-Up (Active) — A transistor replaces the pull up resistor to effect low output impedance without high power consumption.

R

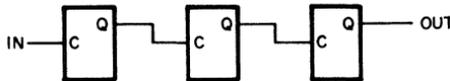
- Race — The condition that exists whenever a signal propagates through two or more memory elements during one clock period.
- A condition that occurs whenever changing the state of a system requires changing two or more state variables. If the final state is dependent upon which variable changes first, the condition is a critical race.

Register — A storage device for binary data generally used to store numbers for arithmetic operations or their result.

Reset — Changing the state of a binary from ONE to ZERO condition.

Ring Counter — A feedback shift register with only one stage in the ONE condition at any time. The shift register's output is fed back to the input to keep this single binary digit circulating. (See also Twisted Ring Counter)

Ripple Counter — An asynchronously controlled counter; the clock is derived from an output of a previous stage.



S

Scratch Pad Memory — Fast memory unit to store temporary data between operations in computers.

Serial Mode — The operation is performed bit by bit, generally beginning with the least significant bit. Read-in and read-out occurs bit after bit by shifting the binary data through the register.

Set — Changing the state of a binary from ZERO to ONE condition.

Set-Up Time — The periods of time that logic levels must be presented at a binary's logic inputs before the clock input may be activated.

Shift — Transfer data from one memory cell to another.

Shift Register — A storage device with the ability to shift the content in one or the other direction.

Single-Rank Binary — A flip-flop which requires not more than one full clock pulse of a single clock system to transfer the logic from a synchronous input to the binary's output. Contains only one memory stage.

Sink Load — A load with a current flow out of its input. A sink load must be driven by a current sink.

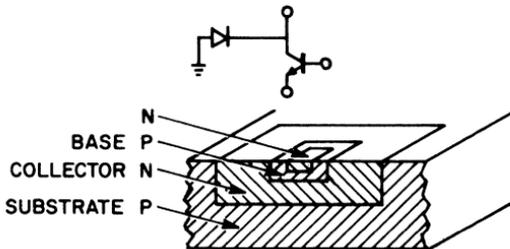
Source Load — A load with current flow into its input. A source load must be driven by a current source.

Standard Unit Load — Within each SIGNETICS Series, there is a standard load defined. Maximum fan-out is determined with this standard load or an equivalent circuit.

Synchronous Operation — Operation controlled by a clock pulse.

T

Triple Diffused — The transistors are fabricated within the monolithic substrate by three diffusion steps.

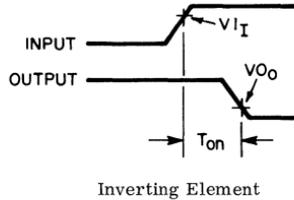


EXAMPLE: TRANSISTOR-DIODE

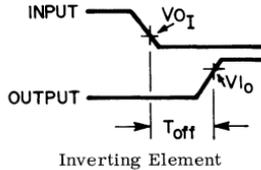
t_{hold} — (See Holding Time.)

t_{pd} — (See Propagation Delay)

T_{on} (Turn On Time) — Switching time delay of a driven digital element measured between input and output at specified voltage levels, usually the switching threshold voltages, e.g.:



T_{off} (Turn Off Time) — Switching time delay of a driven digital element measured between input and output as specified voltage levels, usually the switching threshold voltages.



True — True condition, the statement for a ONE in the Boolean Algebra.

Truth Table — A tabular list with all possible input logic combinations and the resulting output logic for all these combinations.

Example: $F = A \cdot \bar{B}$

Truth Table

A	B	F
0	0	0
1	0	1
0	1	0
1	1	0

Twisted Ring Counter — A feedback shift register with $2N$ states for N stages. The input to the first stage is the complement of the last stage.

U

Up-Down Counter (Reversible Counter) — Counter counting in ascending or descending order depending upon the logic at the up-down inputs.

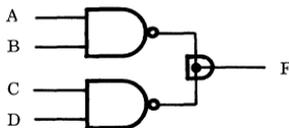
W

Wafer — Semiconductor slice of about 1-1/4 inch diameter, will generally produce several hundred dice.

Wired AND/Dot AND Collector Logic — An AND function formed by wiring two or more outputs together. An AND will result from the connection of npn collectors as in conventional DTL or RTL logic. Equal to Wired-OR if notation is negative logic (low level = 1).

Example:

$$f = (\overline{AB}) \cdot (\overline{CD})$$



Wired OR/Dot OR — An OR function formed by wiring two or more outputs employing active pull up and passive pull down together. Frequently applied to Wired AND since its function, $f = \overline{AB} \cdot \overline{CD}$, can be written $f = \overline{AB + CD}$.

Word — A term for the largest grouping of bits, characters, or bytes.



SECTION 2
DIGITAL CONSIDERATIONS BY FAMILY



APPLICATIONS MEMO

APPLICATION OF ELEMENTS
IN
SIGNETICS
DCL (DESIGNER'S CHOICE LOGIC) 8000 SERIES

SIGNETICS DCL (Designer's Choice Logic) 8000 Series is a family of integrated circuits offering high speed elements and arrays, as well as low power elements, all specified compatibly, to provide the designer with a wide variety of speed/power options.

The series is divided into three main groups: the 8800 group being the high speed elements, the 8200 group arrays, and the 8400 group the low power elements. A smaller group, designated 8H00, consists of very high speed gates.

Elements cover either the full military temperature range, -55°C to $+125^{\circ}\text{C}$ (designated by the prefix "S"; for example, S8470J), or the 0°C to $+70^{\circ}\text{C}$ range (designated by an "N" prefix). The N8000 elements are intended for the less stringent military environments (ground support and prototypes) and for industrial applications.

All elements are available in the 14-lead flat package (TO-88, designated by a "J" suffix; for example, S8470J), and the 14-lead dual-in-line package (TO-116, designated by an A suffix).

For complete specifications on any of the elements mentioned in this Application Memo, see the DCL handbook and the additional 8000-series data sheets.

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SECTION 1

DESCRIPTION OF THE ELEMENTS

8400 LOW POWER GROUP

The Signetics 8400 group of logic elements is a compatible set in which the more desirable characteristics of both DTL and TTL have been utilized, with emphasis on low power consumption. The group makes low can counts possible because of the variety of elements (including a dual binary) and the high fan-out of each element.

General Usage Rules

It is recommended that the unused inputs for all the 8000 Gates be connected to the driven inputs. Tying unused inputs to driven inputs provides the best speed since the shunt capacitances of the input actually tend to improve the switching time. It also facilitates board layout since shorting of adjacent pins is all that is necessary. The logical "1" current will be increased by $25\mu\text{A}$ for each driven input which is connected to an unused input. This results in a slight decrease in output levels (less than 15 mv for 8400 and 4 mv for 8800.)

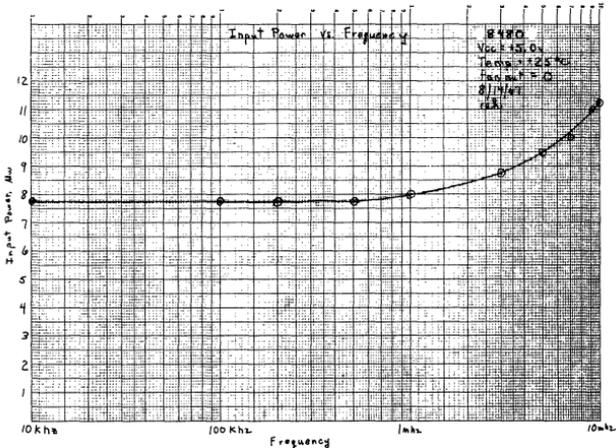
Unused inputs may also be left open or they may be tied to V_{CC} . Connecting the unused inputs to V_{CC} gives the best noise immunity and improves speed (slightly) over the open input case. With all TTL devices other than Signetics 8800 devices, an input latch-back breakdown can occur at voltages above the 5 volt normal operating supply. If the 8400 Gates are connected to V_{CC} then the connection should be made through a 5K ohm resistor.

The standard DC load of the 8000 elements is considered to be the input of the 8480 quad two-input NAND gate. The standard AC load is considered to be the clock input of the 8424 binary. The capacitance associated with the standard AC load is 50 pf.

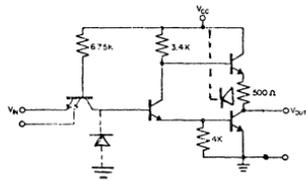
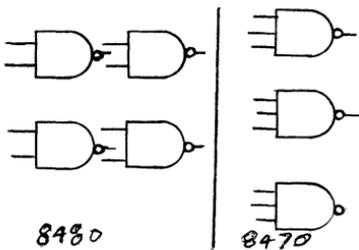
There are three types of output structure within the 8400 group. The first type has an active transistor pull-up, utilizing a 500 ohm series current-limiting resistor. Included in this type are all the 8400 elements except the 8455, 8515, 8417, 8471, and 8481. The active output structure is key to the reason why 8400 elements are able to achieve DTL performance at lower than normal DTL power levels. The effective output impedance of less than 600 ohms results in rise times which are much faster than in DTL (2K to 6K output impedance). However, when the gate is in the "0" state, the current drain is less than would result if a passive 600 ohm load resistor were used. Collector logic is not permitted due to the active pull-up outputs. However, the gates will not be damaged if their outputs are momentarily shorted to ground.

The second type also has an active transistor pull-up, but with a diode by-pass around a 200 ohm resistor. The 8455 is the only one of this type. This structure results in higher-fan-out, the sharp rise times into heavy capacitive loads, such as the 8424 clock input.

A curve of power vs. frequency for the 8480 is shown below. Note that the curve is almost flat, which means that virtually the same power is available for all frequencies. This characteristic was achieved through the special design of the output circuit.



The third type of output has bare collectors. In this type are the 8415, 8417, 8471 and 8481. The bare collectors permit the elements to be paralleled with other bare collector elements, or, in other words, they permit collector logic operation. The 8417 has an unconnected 4.4K ohm pull-up resistor.



NOTE: 1/4 of 8480 shown. Component values are typical.

8470 Triple Three-Input NAND Gate and 8480 Quadruple Two-Input NAND Gate

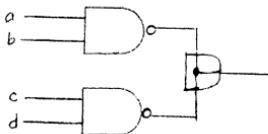
The 8470 and the 8480 incorporate the basic circuit configuration of the 8400 series. This configuration is the one usually associated with TTL families. A very efficient design has produced medium speed operation at low power levels. The design departs from traditional TTL design in that it employs a 500 ohm current-limiting resistor in the output structure.

Noise margins of the TTL elements in the 8400 series are comparable to margins in familiar DTL circuitry. On a DC basis, the input multiple-emitter transistor behaves very similarly to the diode array which would normally be employed in a DTL gate. The emitter inputs behave as conventional input diodes and the collector-base junction serves as the normal level-raising diode employed in DTL. The departure from DTL operation appears when the gate input is driven to zero level. During this transient period, the input transistor behaves as a transistor in grounded base mode and pulls current from the inboard, or phase splitting, transistor. The effect of this is to improve switching time by sweeping out the stored charge in the inboard transistor.

8471 Triple Three-Input NAND Gate and 8481 Quad Two-Input NAND Gate

The 8471 and the 8481 incorporate the same circuit configuration as the 8470/8480, except the output structure has bare collectors, which permits collector, or Wired-AND, logic.

"Wired-AND" is the nomenclature used by Signetics to indicate the collector logic function formed by connecting two or more passive pull-up outputs as shown.



The function formed is $\overline{ab} \cdot \overline{cd} = \overline{ab + cd}$. Because this function generator is the equivalent of the AND-NOR gate, it is frequently known as Wired-OR.

$$m = \frac{I_S - n I_{I_1}}{I_{I_0}}$$

where:

m = the number of outputs you want to connect together

I_S = the source current available to supply leakage currents

$$I_S = \frac{V_{CC} - V_{I_0}}{R_L}$$

V_{I_0} = output "1" voltage

R_L = the load resistor taken at its maximum value for computing source current

n = net fan-out in terms of standard loads

I_{I_1} = input "1" current

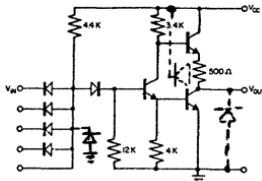
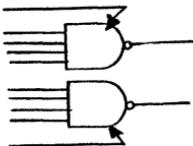
I_{I_0} = output "1" current

Since the 8417 includes a built-in optional pull-up resistor, it eliminates the need for discrete resistors in many cases. If discrete resistors are used, a tolerance of $\pm 2\%$ will be more efficient in terms of leakage driving capability and sink fan-out load. The table below shows some typical values of n , m , and R_L . R_L is given in multiples of 4.4K ohms (the value of the 8417 optional pull-up resistor)(see schematic of 8417). Thus, in the case of an n of 1, and an m of 36, a total of 4 of these resistors would have to be connected to the output. If there were no 8417's in the combination, then the equivalent resistance of four 4.4K ohm resistors in parallel (or 1.1K) would have to be connected between the output and V_{CC} . Thus, R_L can be read as "number of 4.4K resistors in parallel between the output and V_{CC} ." The $n = 3$ row shows that a 5.6k ohm resistor has to be paralleled with the two 4.6K's.

n	m	R_L
1	8	1
1	17	2
1	36	4
2	26	3
3	25	2 + 5.6K ohms
4	14	2
5	4	1
6	3	5.6K

8416 Dual Four-Input Expandable NAND Gate

The 8416 is a dual four-input DTL NAND gate with input structure utilizing four parallel diodes and a node to allow expansion by attaching diodes or diode arrays. The limitation of input expansion is described under 8731 quad two-input expander. The output structure employs active pull-up and pull-down (same as the 8480), thus providing low impedance driving source.

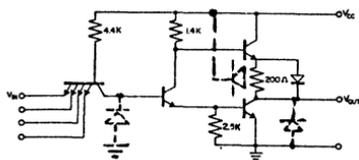
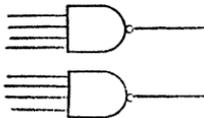


NOTE: 1/4 of 8416 shown. Component values are typical.

8455 Dual Four-Input Buffer/Driver

The 8455 is a dual four-input power NAND gate intended for driving the clock lines of the 8424 and other high capacitance loads. The output structure of the 8455 incorporates parallel resistor-diode combinations for optimum characteristics. The diode gives low output impedance characteristics under heavy loads to yield fast rise times into high capacitances; the resistor pulls the output level to high "1" levels at light load or at the end of the switching transient.

In general, the circuit performance of the 8455J is the same as the 8480J but it utilizes lower resistor values to achieve its greater current handling capabilities.

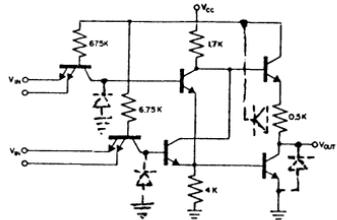
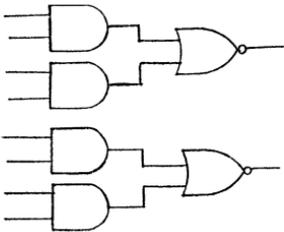


NOTE: 1/4 of 8455 shown. Component values are typical.

8440 AND-NOR Gate

The 8440 is a dual two-input AND-NOR gate which is ideally suited to implementing Exclusive-OR, digital comparators, and general AND-OR control logic functions to the input of the 8424. (See discussion under 8424.)

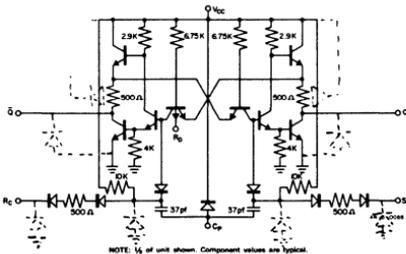
The 8440 circuit is a derivation of the 8480 circuit and, therefore, has essentially the same circuit performance figures.



NOTE: 1/5 of 8440s shown. Component values are typical

8424 Dual RS/T Binary Element

The 8424 normally operates as a triggered RS binary and will operate in the "T" mode by connecting output Q to input S_C and output Q̄ to input R_C. The 8424 is well suited for general logic applications. In counters and shift registers, it will typically operate to frequencies of 12MHz.



NOTE: 1/5 of unit shown. Component values are typical.

TRUTH TABLE

R _{Cn}	S _{Cn}	Q _{n+1}
1	0	1
0	1	0
1	1	Q
0	0	?

$$R_D = 0 \Rightarrow Q = 0$$

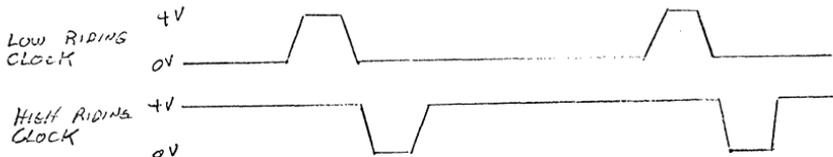
n is time prior to clock
n+1 is time following clock

A protective diode is included at the clock pulse input to limit positive excursions of the clock line to about 0.5 volts above the power supply and negative excursions to about -30 volts. The current in this diode should be limited to 1 mA on negative excursions and 10 mA on positive excursions.

The binary R_C and S_C inputs are two-thirds of a standard DC load, however, during the transient period when the clock is rising, additional transients flow out of the enabling input which is down. Therefore, the binary R_C and S_C inputs should be considered 1.5 loads to allow for this transient current. The direct reset input, R_D , represents one standard DC load. When not used, the R_D input must be terminated in a manner similar to that used for the gate family described earlier. The R_D input may be connected to the Q output if this is more convenient. This connection must be considered a loss of 1 for the "1" level fan-out for this element, and negates the output isolation. (See below.) The clock input of the binary is one AC load.

The recommended clock pulse waveform is a normally low-riding, positive-going pulse at least 2.5 volts in amplitude, 100 nanoseconds wide, with a fall time of less than 75 nanoseconds.

Logic levels to R_C and S_C inputs should be settled at their final values before the clock pulse rises and must remain stable all the while that the clock pulse is high. The condition that both inputs are simultaneously low at the time of the clock fall must be prevented to prevent ambiguous states.



If high-riding clock pulses are used, two factors must be considered. First, the clock source impedance must be low enough to supply the charging current required on "1" and "0" transitions at the logic (S_C/R_C) inputs without allowing significant voltage changes. The second area of concern associated with high-riding clock pulses is set-up time which will be on the order of 1.5 microseconds for "0" to "1" logic transitions. In other words, if the clock line is normally high, the logic lines should be stable for at least 1.5 microseconds before the fall of the clock pulse.

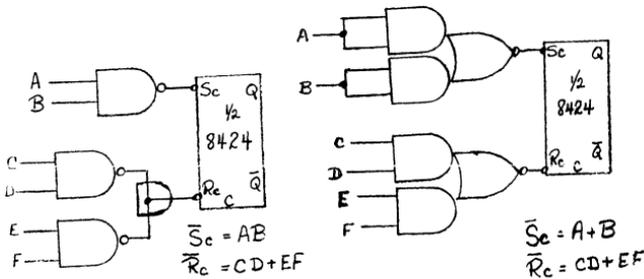
If the S_C input is low and the clock falls while the R_D line is low, a positive going spike of approximately 120 nanoseconds and 2.6 volts will exist on the Q output; no transient will exist on the \bar{Q} output.

In response to the synchronous R_C/S_C inputs, the flip-flop changes state on the falling edge of the clock pulse. The flip-flop will respond asynchronously to "0" levels at the direct preset input (R_D).

The 500 ohm series output resistors serve as current limiting resistors and also as memory-output isolation elements. The design of the 8424 is such outputs may be grounded without affecting the state of the memory section. This means that noise cannot disturb the stored state and that latch time is not affected by load.

Because the 8424 logic inputs (S_C and R_C) respond to low level inputs (that is, the 8424 performs as if the inputs incorporated inverters), it is especially suited to use with NAND and AND-NOR logic elements. The functions most frequently implemented at flip-flop inputs in logic systems are of AND and AND-OR form. Implementation of these functions requires an inverter if the flip-flop has 'non-inverting' inputs. Because the 8424 has inverting inputs, the AND function is available at NAND outputs; AND-OR functions are directly available at AND-NOR gates or at the output of NANDs ANDed with collector logic (NAND-AND is equivalent to AND-NOR).

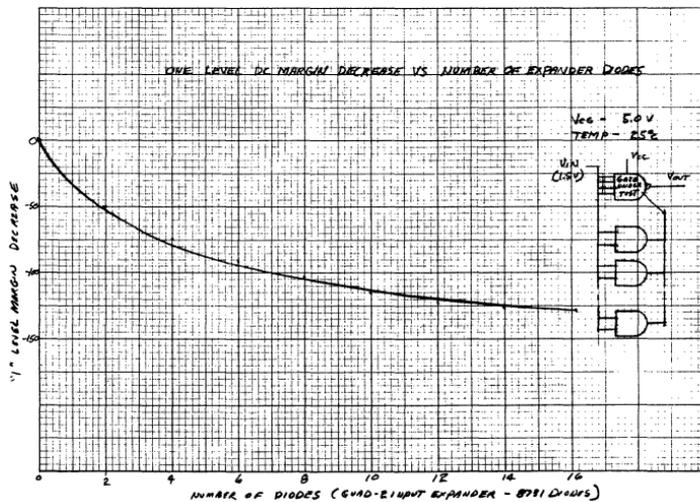
In high speed systems, the user will use the J* and K* inputs of the 8825 to implement AND and AND-OR functions. OR functions are most efficiently implemented by using non-inverting inputs with NAND gates.

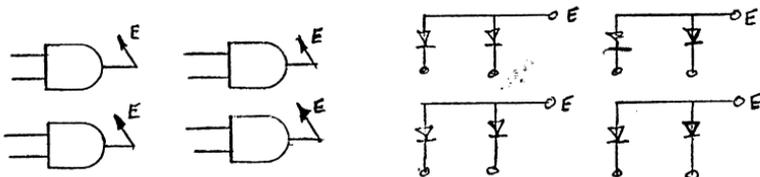


8731 Quad Two-Input DTL Expander

The 8731 input expander is a diode array for expanding the inputs on the 8416 and 8417. Input expansion influences both DC margins and switching times. Therefore, maximum fan-ins may be set by switching times in one case, DC margins in another. Turn-on delays for the expander will increase by about 3 nanoseconds per picofarad of capacitance on the expansion input since the input resistor of the gate must change this additional capacitance before the gate may be switched. This capacitance will be discharged through the input diode and low output impedance of the driving gate; therefore, turn-off time is not appreciably influenced.

From a noise margin consideration, the fan-in will be determined by the leakage currents of the input diode array. These currents will decrease the '1' margin as seen in the figure on the next page.





8800 HIGH SPEED GROUP

Main Features

The 8800 group is a family of high level TTL integrated circuits consisting of NAND gates, a power gate or driver, AND-NOR gates matching input expander, J-K flip-flops, dual D flip-flop and dual J-K flip-flops.

All gates are of the classical TTL design, utilizing multiple-emitter input transistors. Active pull-up output is used to maintain high speeds even under heavy capacitive loads and to enhance noise margins.

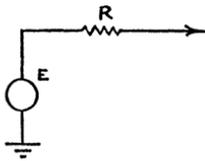
General Usage Rules

Unused inputs in the 8800 group should be handled the same as the 8400 Group. (See discussion under 8400 Group: "General Usage Rules.")

The low impedance active pull-up output structure results in fast turn-off even when driving capacitive loads. Collector logic is not permitted. However, units will not be damaged if their outputs are momentarily shorted to ground.

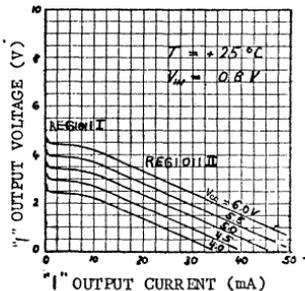
The high level (logical "1") output impedance of a typical 8800 series gate may be determined from the slope of the "1" OUTPUT VOLTAGE vs. "1" OUTPUT CURRENT curves below. The output impedance (slope) is dependent upon the output current, that is, there are two regions of constant slope. The output impedance is essentially that of an emitter follower in the lower current region. In the higher current region the output impedance is primarily that of the collector resistor (80 ohms). The equivalent voltage source may be determined from the "Y" intercept of the curves for a given power supply voltage (V_{CC}). A high level equivalent output circuit for a typical case is shown below.

The equivalent circuit values for other temperatures (-55°C , $+125^{\circ}\text{C}$) may be determined from the appropriate curves in the curve section of the data sheets. The equivalent circuit for the 8855 power gate may be obtained in the same manner using the 8855 curves in the curve section of the data sheet.



$$R = \frac{\Delta V}{\Delta I}$$

$E = \text{"Y" intercept}$
 $R \cong 25\Omega, \text{ Region I}$
 $E \cong 3.5V$
 $R \cong 80\Omega, \text{ Region II}$
 $E \cong 4.0V$
 $V_{CC} = 5.0V$

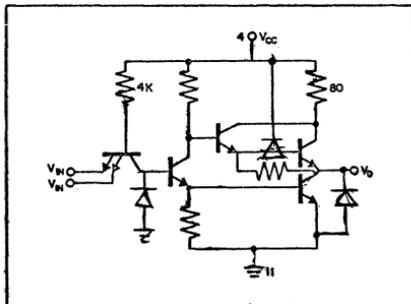
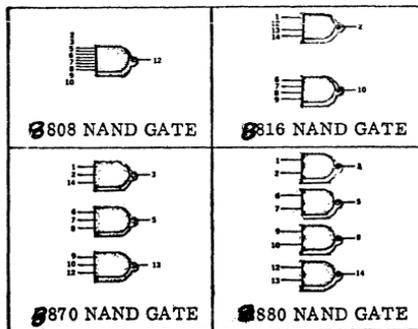


At interfaces where non-operating (V_{CC} off) gates may be connected to an operating system, due regard must be given the isolation diode associated with the resistor at the output of the gates. Power supply outputs frequently become a low impedance to ground when the input power is removed. In this case, gate outputs will be clamped positive with respect to ground. The output collector isolation diode will clamp the output negative with respect to ground.

Note that no resistor is tied directly to the output of the 8855.

8808, 8816, 8870, and 8880 NAND Gates

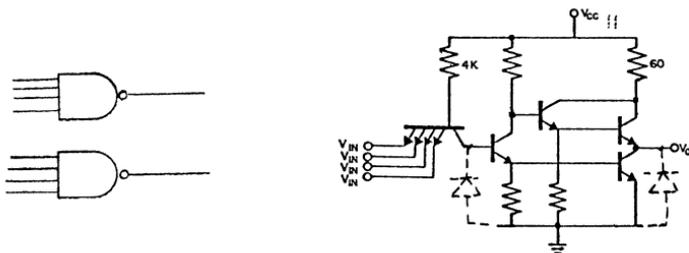
All of these gates perform the basic NAND logic function. The various configurations in this group differ only in the number of inputs per gate and the number of gates per package.



8808, 8816, SE870, 8880 BASIC NAND GATE

8855 Power NAND Gate

The 8855 is a dual four-input NAND gate intended for driving clock lines or other high capacitance loads. Its design is similar to that of the basic 8800 NAND gates described above. It features lower output impedance at both the "1" and "0" levels to allow high fan-out. Large geometry transistors are used in the output to provide higher current capability at low saturation voltage levels.



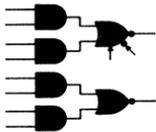
8840 Dual AND-OR-INVERT TTL Gate and 8848 AND-OR-INVERT TTL Gate

The 8840 is a dual 2 wide 2-input (2x2) AND-OR-INVERT gate with one-half of the element expandable. The 8848 is a 4 wide 2, 2, 2, 3 input AND-OR-INVERT expandable element. The 8840/8848 represent only one level of propagation delay every though the logic implies two levels of delay. The 8840 readily implements the Exclusive-OR logic function or may be used as a dual two-input NOR gate by simply using one input per AND gate. (See next page for schematic.)

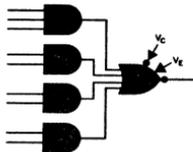
Each 8806 expander has basically the same logical effect as the built-in AND gates of the 8840/8848. The difference is the number of inputs per AND function (two inputs for 8840/8848 AND's and four inputs for the 8806 AND's). The 8840/8848 may be expanded with either the 8806 or with one other 8840 or 8848. Fan-in expansion will decrease the "0" input threshold voltage in accordance with the curves in figure on page 1-15.

If the user wishes to form AND-NOR functions which require expansion of the 8840 or 8848, it may be as effective to use the 8417, 8471 and/or 8481 elements in collector logic.

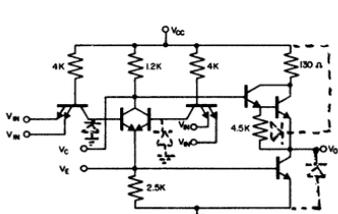
Extreme care should be exercised when laying out the lines for the 8840/8848 to connect expansion points to minimize capacitance and to minimize the possibility of noise pick-up, because the base of the output transistor is directly exposed.



8840

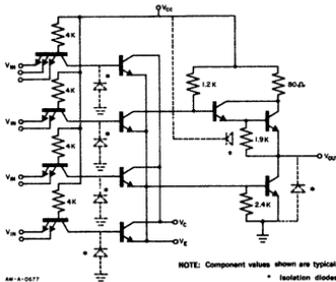


8848



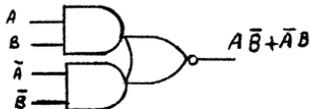
NOTE: 1/2 of unit shown. Component values are typical.

AR-4-0325



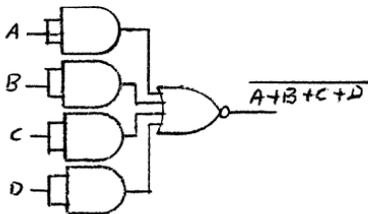
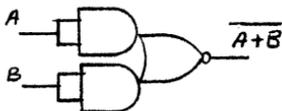
NOTE: Component values shown are typical.
* Isolation diodes

AR-4-0477

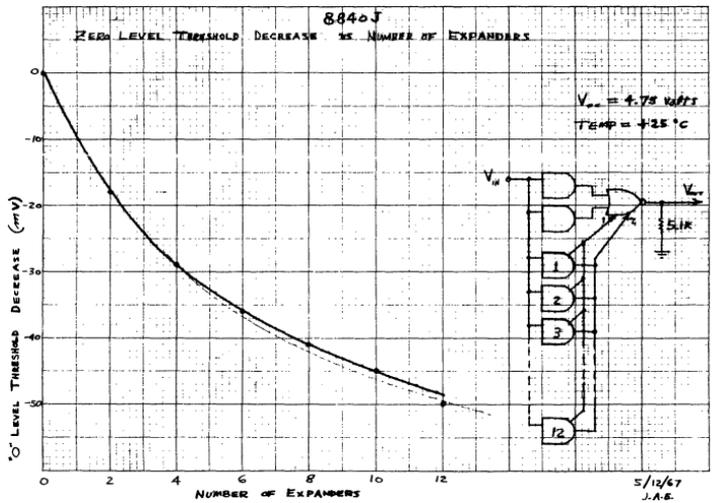


A	B	$A\bar{B} + \bar{A}B$
0	0	0
1	0	1
0	1	1
1	1	0

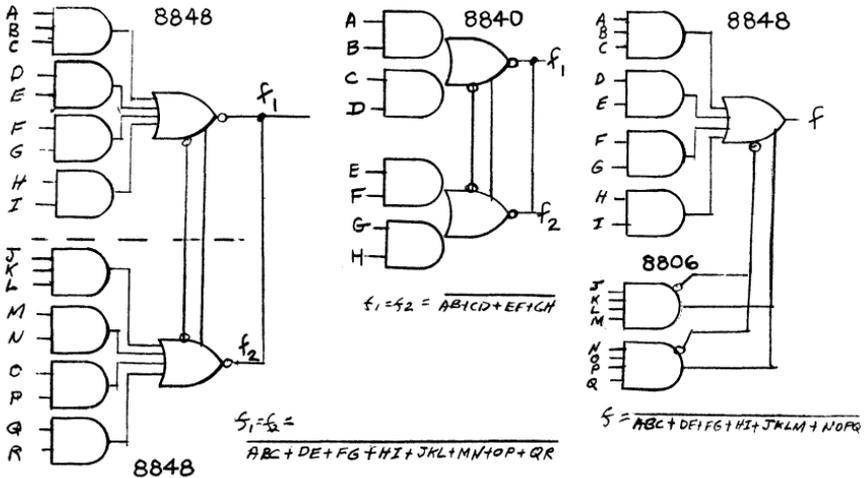
EXCLUSIVE-OR LOGIC



NOR LOGIC

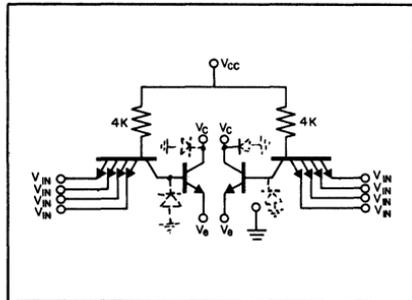


Considering the capacitance pick-up and the current gain of the elements, it is recommended that only one additional 8840 or 8848 be connected to another 8840 or 8848, although several 8806 elements can be connected to the 8840/8848.



8806 Dual Four-Input Expander

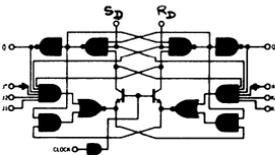
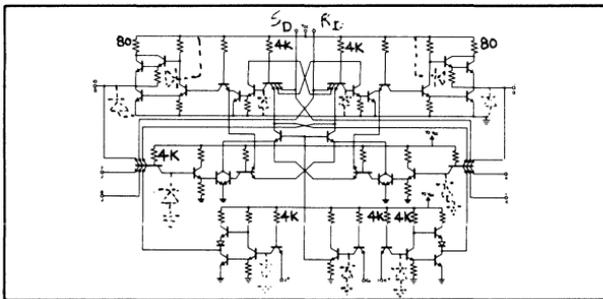
The 8806 is a dual four-input expander for one-half of the 8840 or the 8848. The V_C (collector) outputs of the 8806 connect to the V_C inputs of the 8840/8848. The V_E (emitter) outputs of the 8806 connect to the V_E input of the 8840/8848. For additional information, see discussion on 8840/8848 AND-OR-INVERT gates. The unused input rules of the basic NAND gates are applicable to the expander.



8825 J-K Binary Element

The 8825 is a single DC clocked flip-flop with multiple J, K inputs. Asynchronous S_D (set) and R_D (reset) lines are also provided.

The 8825 responds to the leading (positive going) edge of the clock input. Logical lock-out of the logic inputs prevents more than one transition of the flip-flop per clock pulse. The recommended clock pulse waveform is a positive going pulse at least 15 nanoseconds wide at the 2 volt level with rise and fall times of less than 150 nanoseconds.



TRUTH TABLE

J	K	Q_{n+1}	P_J	P_K	Q
0	0	Q_n	0	0	†
1	0	1	1	0	0
0	1	0	0	1	1
1	1	\bar{Q}_n	1	1	Q

$$J = J_1 J_2 J^*$$

$$K = K_1 K_2 K^*$$

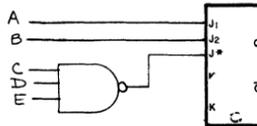
†Both outputs in 0 state

Logic levels to the J and K inputs should be stabilized at a logical "1" or "0" level 10 nanoseconds before the clock pulse rises and should remain stable for 10 nanoseconds after the rise of the clock pulse. Unused J and K input should be handled the same as the 8400 Group. (See discussion under 8400 Group, "General Usage Rules.")

Logic levels to the J* and K* inputs should be stabilized to the logical "1" or "0" level 25 nanoseconds before the clock pulse and should remain stable for 10 nanoseconds after the rise of the clock pulse. Unused J* and K* inputs must be tied to ground.

A logical "0" on the S_D line sets the Q output to logical "1". A logical "0" on the R_D line resets the Q output to logical "0". When the S_D and R_D lines are not activated, they must be at a logic "1" level, tied to V_{CC}, or open. To effect proper presetting action, the clock input must be low when activating S_D and R_D. If the clock is high, (logical "1") when activating S_D or R_D, both outputs may go to logical "0" simultaneously; when deactivation of S_D or R_D occurs, the flip-flop will return to the state it was in prior to activating S_D or R_D.

Gated J-K inputs reduce system can count for many applications. Utilization examples of the gated inputs are given in Section 3. The inverting inputs may be used as expander nodes with the basic NAND gates of the 8000 series, that is, connecting a NAND gate to an inverting input expands the number of AND terms at the input (J or K) (see below). If the input to J* is an 8840 with inputs CD and EF, then $J = AB(CD + EF)$. The figure below illustrates expansion with the 8870 NAND gate. Here $J = AB(CDE) = ABCDE$.



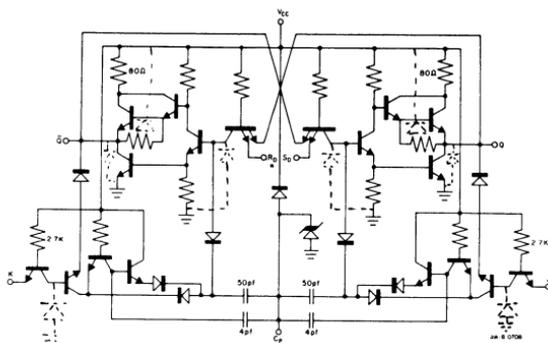
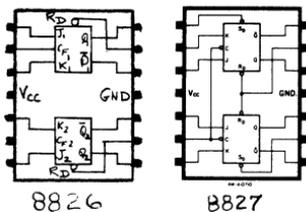
$$J = J_1 J_2 J^* = ABCDE$$

The outputs are fully buffered, therefore loading will have no effect on the state of the flip-flop.

8826, 8827 Dual J-K Binary Elements

The 8826/8827 contains two high-speed AC clocked J-K flip-flops. The 8826 features separate Clock and Reset lines for each flip-flop. The 8827 features common Clocks, common Reset and separate Set lines for each flip-flop.

The 8826/8827 responds to the trailing (negative-going) edge of the clock input. The recommended clock pulse waveform is a positive-going pulse that is at least 10 nanoseconds wide at the 2.4 volt level and has a fall time of less than 50 nanoseconds. Logic levels to the J and K inputs should be stabilized at a logical "1" or "0" level before the clock pulse rises and must remain stable until the clock pulse falls. The positive clock pulse width must be limited to 1.0μsecond maximum if the J and/or K input are a logical "0". There is no restriction on the maximum pulse width of an 8826 which is being used as a ripple counter since J and K inputs are both at a logical "1" level.



*Common to both flip-flops (8826 and 8827)
NOTE: 1/2 of unit shown. Component values are typical.

TRUTH TABLE		
J	K	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	\bar{Q}_n
$R_D = 0$	$Q = 0$	
$S_D = 0$	$Q = 1$	

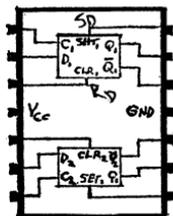
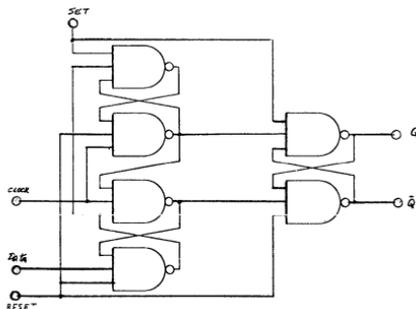
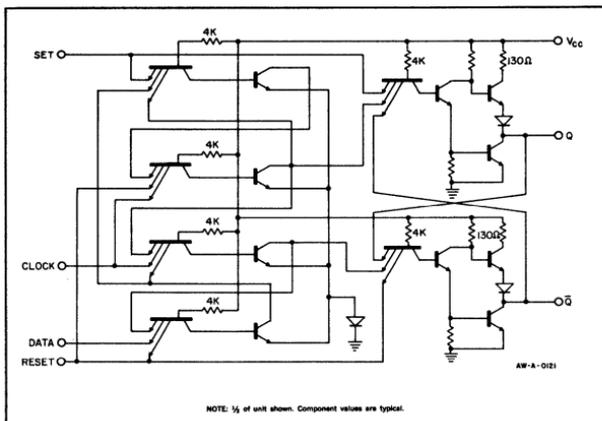
A logical "0" on the R_D (Reset) of an 8826/8827 line resets the Q output to a logical "0". The R_D line may be activated when the clock line is in either the logical "1" or the "0" state. If the clock input makes a logical "1" to "0" transition when R_D is a logical "0" and J is a logical "1", a positive-going spike approximately 150 nanoseconds wide will appear at the Q output; no transient will exist on the \bar{Q} output. For the 8827, the S_D (Set) line sets the Q output to a logical "1". The S_D line should be treated the same as the R_D line. A positive-going spike will appear on the \bar{Q} when S_D is a logical "0" and K is a logical "1" with a clock input "1" to "0" transition. Unused R_D inputs may be tied to Q and S_D to \bar{Q} , or may be connected to V_{CC} .

8828 Dual D Binary Element

The 8828 contains two DC clocked D (delay) flip-flops with separate Clock Clear and Set inputs for each flip-flop.

The logic state that is present at the D input is transferred to the Q output when the clock line is activated. The 8828 responds to the leading (positive-going) edge of the clock input pulse. Logic levels to the D input must be stabilized at a logical "1" or "0" level 20 nanoseconds before the clock pulse rises. The D input is locked out approximately one gate delay after the clock pulse exceeds the clock input threshold, hence, the D input must remain stable for 10 ns after the clock pulse rises.

A logical "0" on the Set line sets the Q output to a logical "1" and a logical "0" on the Reset line sets the Q output to a logical "0" regardless of the states of the D and clock inputs. When the Set and Reset lines are not activated, they must be at a logical "1" level, e.g., tied to V_{CC} , or Reset may be connected to Q and Set to \bar{Q} .



D	Q _{n+1}	Set	Clear	Q
0	0	0	0	†
1	1	0	1	1
		1	0	0
		1	1	Q

† Both outputs in "1" state

HIGH SPEED ARRAYS

The Signetics high speed array group includes the 8280, Decade Counter/Storage Register and 8281, Binary Counter/Storage Register. These elements were designed as subsystems to provide both counting and storage functions. Equivalent circuit logic diagrams are shown for these in Figures 1-1 and 1-2.

The 8280 is arranged so that it may be used in the familiar BCD mode (8421) or in the Bi-Quinary mode (5-4-2-1) to obtain the square wave output required by frequency synthesizers and similar applications. This flexibility is a result of separated divide-by-two and divide-by-five functions; the manner in which these functions are interconnected by the designer determines the mode of operation.

The 8281 contains separated one-stage and three-stage binary counters which may be cascaded to obtain a four-stage binary counter. Since outputs of each stage are available, the three-stage counter may be utilized as a two-stage counter (output, etc.) if this is the function desired. Both devices feature strobed single-ended parallel-entry capability with a separate Reset which is common to all four bits.

General Performance Characteristics

A partial circuit showing one binary bit, the strobe, and preset input circuits can be found in Figure 1-3.

All binary outputs utilize active pull-up output structures. Collector logic is not permitted because the active pull-up outputs cannot be paralleled and maintain proper logic "0" or "1" states. However, units will not be damaged if their outputs are momentarily shorted to ground.

To implement the count function, the individual flip-flops were made to exhibit J-K characteristics with a charge-storage clocking scheme. Change of state is effected on the negative transition edge of the clock pulse. The clock pulse amplitude must be at least 2 volts for at least 25 nanoseconds; fall time must be 50 nanoseconds or less.

The counters were designed to exhibit an optimum speed-power characteristic when operating in the BCD mode or (Mod. 2 followed by Mod. 5) for the decade and binary elements. The maximum allowable input pulse repetition rates to the Clock 1 input are greater than those allowable at the Clock 2 input. An input clock signal whose frequency is as great as 35 MHz can be accepted at C_1 for frequency division design applications. Similarly, a 20 MHz clock signal applied to C_2 will result in proper frequency division. It should be remembered that satisfactory operation of the counters require the negative transition be equal to or less than 50 nanoseconds. This requirement is resultant from the fact that the binaries use a stored charge principle and are therefore transition dependent.

The parallel entry inputs are single-ended in form and accomplished a logical "1" or "0" entry dependent upon the input logic state for the bit in question when the strobe gate is enabled. Change of counter state to that applied to the D inputs is accomplished by conditioning the Strobe input to the "0" level. The Strobe is direct coupled and therefore is not sensitive to rise or fall times. The Strobe input when at the logic "0" state can also be used as a count inhibit command in that its control will be dominant over the C_1 or C_2 clock inputs. It can be seen in the schematic (Figure 1-3) that when the Strobe is in the logic "0" state, Q_5 will be turned on if the preset input is in the logical "0" state or Q_4 will be turned off if the preset

8280 DECADE COUNTER

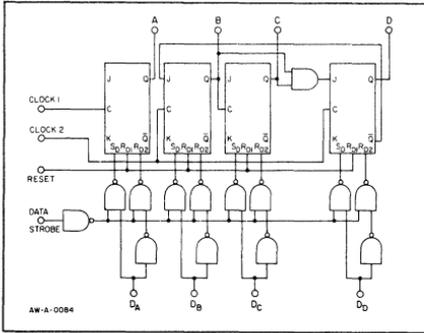


Fig. 1-1

8281 BINARY COUNTER

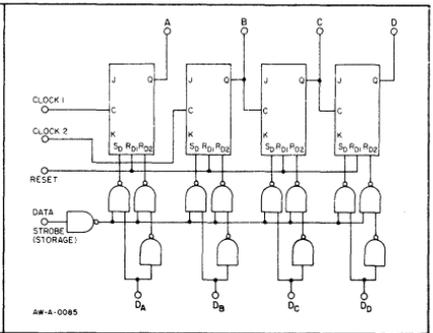


Fig. 1-2

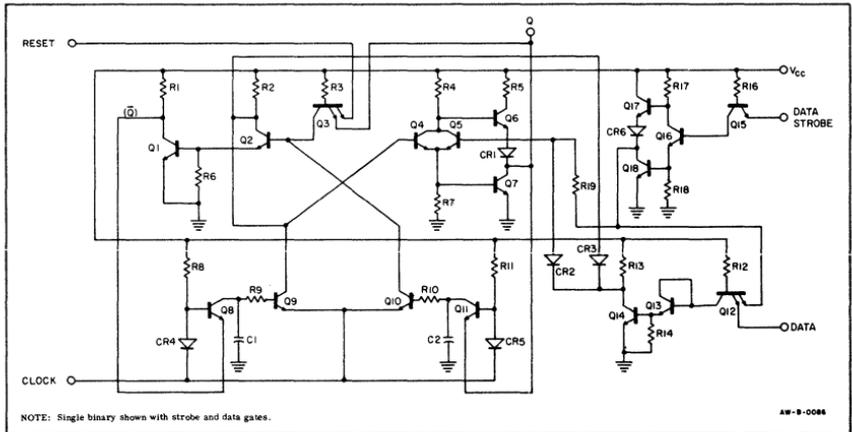


Fig. 1-3

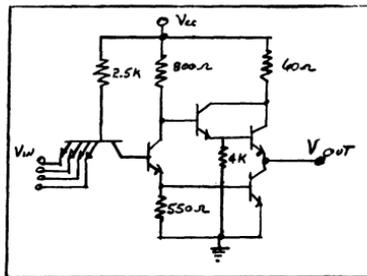
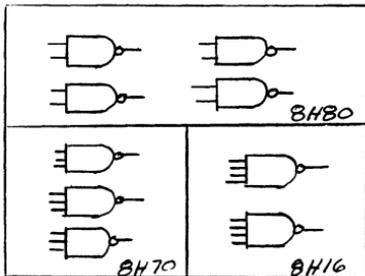
input is in the logical "1" state. These two direct strobe inputs cause the binary to acquire the appropriate logic "0" or "1" of the preset data. Strobe also dominates over Reset.

If the clocking signal is in the logic "1" state and a negative transition occurs during the Strobe interval, the Strobe interval must remain for at least 250 nanoseconds after the clocking transition to ensure that the parallel entered data is retained. The Strobe interval necessary to accomplish parallel entry of data under any condition is 250 nanoseconds. If a shorter Strobe interval is desired for faster operation of the counters, the Strobe signal should change to the "0" state for 50 nanoseconds after all "clocking signals." The term "clocking signal" may be the output of one binary bit clocking the next binary bit as in a ripple counter. See examples in Section 3, Special 8280/8281 Counter Applications.

ULTRA HIGH SPEED GROUP

The ultra high speed group is a family of high speed gates consisting of quad two-, triple three- and dual four-input NAND gates. The circuit solution is that of TTL.

- 8H16 Dual Four-Input NAND Gate,
- 8H70 Triple Three-Input NAND Gate,
- 8H80 Quad Two-Input NAND Gate



8H00 Description

The general characteristics of both the input and outputs of the ultra high speed gates are similar to those described before in both the 8400 gate and the 8800 gate types. The variation of input characteristics are that the input "0" loading should be considered 3 unit loads, the input "1" loading should be considered 2 unit loads. The output "0" and output "1" fan-outs are equal to 30.

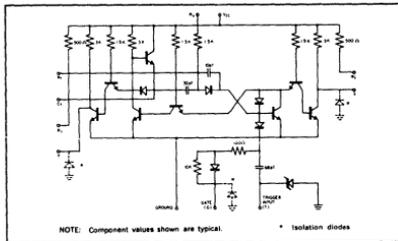
The same rules for terminating unused gate inputs apply to this family as have been discussed in the 8800 and 8400 gates. A speed improvement can be obtained if inputs are connected to driven inputs (see discussion under 8400 group: "General Usage Rules"). It should be remembered that paralleling inputs does accumulatively add to the "1" level fan-out.

This gate family is intended to interface completely with the other gates and elements within the 8000 family. They are intended for usage where 5 to 6 ns propagation delays are required.

8162 MONOSTABLE MULTIVIBRATOR

The 8162 is a general purpose one-shot with complementary outputs and optional 500 ohm load resistors.

A 1-5K ohm timing resistor is brought out for external connection to achieve maximum flexibility. The monostable provides high duty cycle (75%) and provides complete isolation of the timing stage and the output stage resulting in good fall time even with wide pulse widths.



The monostable's clock can be driven by any of 8000 Series element as long as the input rate is considered to be 2 AC fan-in loads or 100 picofarad. The clock pulse width should be at least 50 ns wide and fall time less than 75 ns.

The gate input, an enabling input for the clock line, is enabled when the gate input is low. With V_{CC} of the 8162 equal to or greater than 5.0V, as 8000 Series is specified, the gate input is inoperative and must be tied to ground.

The monstable provides complementary outputs with passive 3K pull-up resistors. This allows collector logic with the 8400 bare collector gates (see 8471, 8481, and/or 8415, 8417 gate discussion).

An optional 500 ohm pull-up resistor is provided at each output to be used where line capacitance is heavy and rise times must be maintained.

The 8162 element design employs a 30 picofarad timing resistor and 1.5K ohm optional timing resistor. The output pulse width may be increased by connecting capacitance between C_t and R_t terminal. External resistors are connected between R_t and V_{CC} .

The time constants can be calculated with the following equations:

A with internal resistor (only)

B with paralleled external and internal resistors

$$t \approx \frac{(C_x + C_{int}) R_x (10^3)}{1.5K + R_x}$$

where:

$$R_x > 1K$$

C_x connected between C_t and R_t

R_x connected between R_t and V_{CC}

R_t connected to V_{CC}

$$t \approx (C_x + C_{int}) (10^3)$$

where:

C_x connected between C_t and R_t

R_t connected to V_{CC}

C with no internal resistor (R_t)

$$t = \frac{(C_x + C_{int}) R_x (10^3)}{1.5K}$$

where:

$$R_x > 0.5K, \text{ But } < 4.7K$$

C_x connected between C_t and R_t

R_x connected between R_t and V_{CC}

R_t terminal unconnected

Maximum Duty Cycle 75%

- t = pulse duration in seconds
 C_x = external capacitor in farads
 R_x = external resistor in ohms
 C_{int} = Typical 30 pf

Pulse width tolerance using the internal resistor is approximately $\pm 25\%$ (unit to unit variations). Using external timing resistors a tolerance of less than 10% may be obtained.

SECTION 2

TYPICAL ELEMENT APPLICATIONS

DC DISTRIBUTION TECHNIQUES FOR INTEGRATED CIRCUITS

The distribution of power supply voltages and grounds in any system is about as much art as it is science. This is as true of integrated circuit systems as it is of more conventional systems. However, some of the problems are even more severe in an integrated system. Generally, space and weight are at a premium, so we are not free to use arbitrarily large busses. The circuits are much more densely packed so that at any given point there generally can be larger current densities. Integrated circuits usually have rather fast rise and fall times, which can generate large voltage spikes.

Even though DC and ground distribution are an art, some general rules can be given which, properly applied, can eliminate most of the problems.

To illustrate the magnitude of the problem, consider the fact that No. 22 solid copper wire has an inductance of about 35 nanohenry/inch. This may not sound like very much until one considers gates supplied by this bus which may be switching 100 mA in 1.0ns. Currents and rise times in this order of magnitude can generate noise spikes of 3.50V/inch on that bus. Just by changing this No. 22 wire to a 20 mil wide printed conductor buried in a multilayer printed circuit board with a ground plane 5 mils away, we can reduce the inductance and, hence, the noise voltage, by an order of magnitude.

As a general rule, DC distribution and ground lines should have as large a cross-section as is reasonable. Wide flat busses close together are much more effective than round wires for the same amount of copper. One point in the system should be defined as "the system ground-point." Generally, the common ground point of the power supplies is most convenient and most effective. Each major component of the system should be connected to this ground point by a separate wire. The DC ground line should be separate from the ground line which ties shields, chassis, etc. together. Inside each major component ground wires should again fan out from the incoming ground line as much as is practicable. Another possibility is to run a single large ground bus through the major component and connect each subassembly to it with smaller wires. Whichever approach is chosen, the DC ground wires should be insulated from the chassis. Metal chassis should never be used for ground distribution because of the possibility of setting up circulating currents in the chassis and thus producing excessive noise. One should definitely avoid stringing all subassemblies down one wire like beads on a string. These same general principles should be applied to each successive subassembly right down to the printed circuit card. In effect, the ground system branches out like the branches of a tree with a few devices strung along each twig at the last branching level. Chassis grounds should have a similar but separate system returning to the same defined ground point.

The DC voltage distribution lines should be handled in essentially the same fashion as the DC ground system. Where possible, running the voltage supply and ground throughwise, flat busses kept very close together will not only reduce inductances but also increases the capacitance between the lines and minimizes the voltage differences which can be induced between the two by external disturbances.

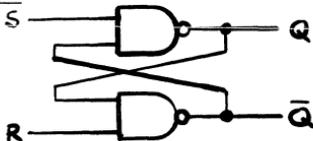
Devices which switch large currents in short times should be placed as close as possible to the next larger branch of the ground system, so as to minimize the inductance between those devices and the defined system ground. If several heavy current switches are close together on the same branch, a bypass capacitor of 5 to 10 microfarads should be connected close to those devices. This should be a tantalum capacitor, since its frequency response is much better than that of an ordinary aluminum electrolytic.

In cases where signals are distributed by coaxial cables, one should be careful that the cable does not interfere with the planned ground system. Grounding both ends of the cable shield can introduce unintentional ground loops which can generate large amounts of noise on the ground lines. Ground loops from this source can be eliminated by grounding only one end of the shield, usually the signal source end, and keeping the rest of the shield carefully insulated from both DC ground and chassis ground.

REVIEW OF FLIP-FLOP TYPES

The following is a review of the various flip-flop types. Note that the RS/T, the J-K, and the D are available in the 8000 series.

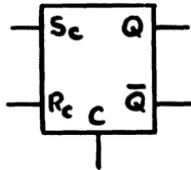
RS - LATCH



S	R	Q
0	0	$Q = \bar{Q} = 1$
1	0	0
0	1	1
1	1	No Change

The latch is the simplest flip-flop and is generally used where memory is the only requirement. The operation of the RS is asynchronous, i.e., no clock pulse is required.

RS/T (For Example, 8424)

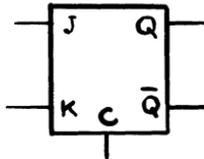


S_c	R_c	Q_{n+1}
0	0	?
1	0	0
0	1	1
1	1	Q_n

The RS/T is essentially a latch to which appropriate delay, steering, and trigger circuits have been added to allow synchronous (clock controlled) operation. The terminology RS/T was coined by Signetics to indicate a flip-flop which is a (clocked) RS, but may be made to operate as a T through external connections. The term RST had been used to fill this function; however, this use conflicts with the definition previously made by Phister.¹

The truth table shows that "0" input levels cause activation. This is not necessarily a characteristic of an RS/T; it is a characteristic of the Signetics 8424.

J-K (For Example, 8825, 8826, 8827, 8829)



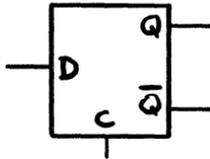
J	K	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	\bar{Q}_n

J-K flip-flops are becoming increasingly popular and are incorporating an increasing number of variations, e.g., J-K's are available with multiple J-K inputs and the inverting J-K (J^* , K^*) inputs as with the 8825.

Comparison of the truth tables for the RS/T and the J-K shows that three of the four possible input states are the same. In the fourth state, both inputs are energized causing an ambiguous condition for the RS/T but a defined condition for the J-K; the J-K will complement.

¹Phister, Montgomery A., "Logical Design of Digital Computers" Wiley.

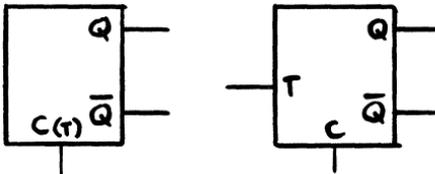
D (For Example, 8828)



D	Q_{n+1}
0	0
1	1

The D flip-flop is commonly known as the delay flip-flop. The logic state presented to the D input will appear at the Q output after the occurrence of the clocking transition.

T



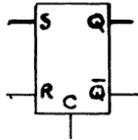
T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

The T flip-flop is known as the toggle; two common configurations exist. One has a T input and a clock input. The other has only a clock input; the internal structure causes the condition $T = 1$ continuously.

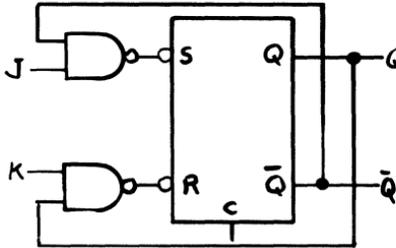
Relationship of Flip-Flop Types

The flip-flops are related as shown on the following two pages. The J-K, D, and T can be derived from the basic RS/T; the T and D from the J-K; and the T from the D. (For example, adding a NAND gate to the S input of the RS/T, and then tying the NAND gate input to the R input, results in a D flip-flop.) Truth tables of the circuits shown will be found to be the same as those of the equivalent flip-flops.

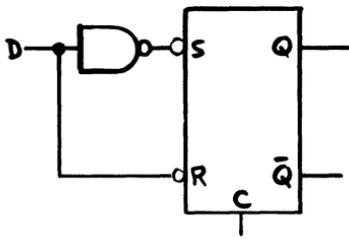
From RS/T:



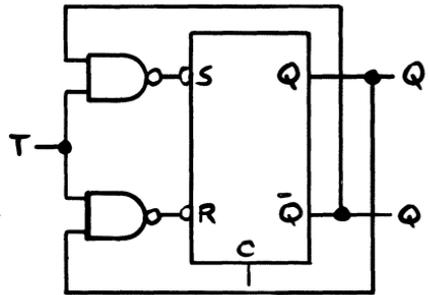
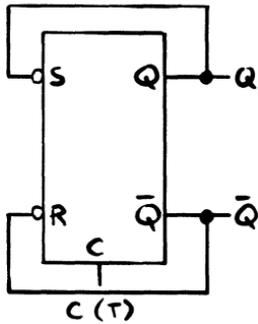
To J-K:



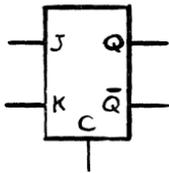
To D:



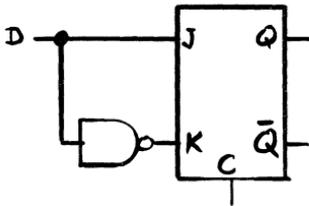
To T:



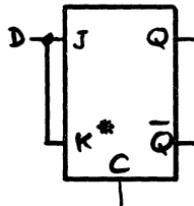
From J-K:



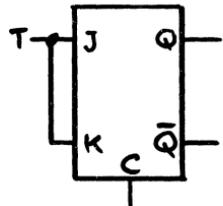
To D



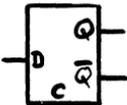
To D



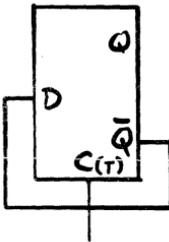
To T



from a D:

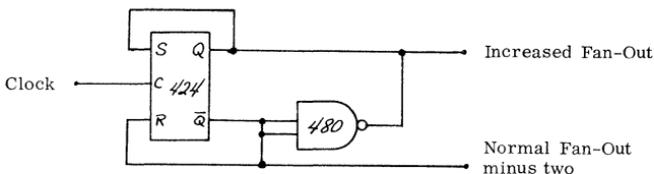


to a T



INCREASING THE FAN-OUT OF AN 8424 ELEMENT

If the fan-out of a binary element is to sink or source more than the specified rated output load, the addition of a single gate (8480) with the 8424 can result in an output drive capability of twice that of the 8424 for the output selected. The binary and gate interconnections are shown below. This circuit shows an improved fan-out configuration for a binary element connected as a ripple counter.



After an examination of the 8424 element circuit, it can be seen that this inter-element connection can be accomplished and improve the operational output characteristics, since the binary cross-coupling for the 8424 element is uniquely accomplished at an internal point rather than the output location (Q) as in some other binaries. This internal coupling allows the binary to maintain control of the gate and ensure proper binary action in either ripple counters, shift registers or any other RS/T operating mode.

To this point we have considered only the changes in DC fan-out characteristics for the circuit. Let us now consider smaller applications requiring higher AC fan-out and higher clock rates when driving larger loads. This same circuit can be used for both.

A typical element connected in a toggle mode and loaded with a 500 pf load was limited to 4 MHz when connected normally but operated at 6 MHz when the 8480 gate was added. It should be noted that this capacitive load exceeds the guarantees for the 8424 limit device but was used to show how such loads can be driven with this circuit interconnection. The above data shows how this simple circuit change can improve the least significant binary of a ripple counter. The resultant change is an increase in the maximum counting rate for the binary under load.

The AC fan-out of an 8424 binary can also be enhanced. This connection provides the sum of both the binary and gate output capabilities for AC fan-out from the Q output terminal. Note that the added gate could be an 8455 element rather than the 8480 element if AC or DC fan-outs from the Q output must be enhanced greatly.

One point which should be realized is that which is good for one output is not good for both. If both outputs are connected in a manner such as described for one, an effective RS latch between the gates is created and operation is uncertain.

This circuit variation shows how one can take advantage of the low power dual binary and accomplish what would otherwise require higher power type devices.

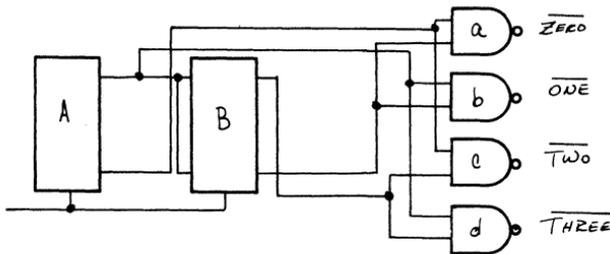
USE OF LOAD SHARING TO REDUCE FAN-OUT REQUIREMENTS

A problem, especially apparent in the design of decoding logic, is that of insufficient fan-out. The designer usually solves the problem by employing high fan-out elements or some form of fan-out augmentation.

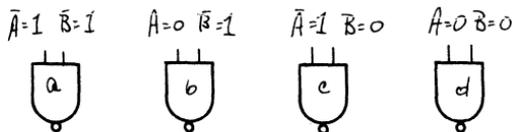
The need for additional fan-out may be frequently obviated by taking advantage of load sharing which can generally be employed when, BUT ONLY WHEN, the input states to the logic are predictable — as in a decoder.

What is meant by "load sharing?" We will assume (and justify later) that the input current of a gate will divide equally between all of the inputs that are low. For example, if two inputs of a gate are low (DTL, TTL) one-half of the input load current will flow out of each input; if four inputs are low, one-fourth load will flow from each input; etc.

Consider the simple four gate network to decode the four states of a binary counter.



When the counter is in state "0", the condition below exists:



Gate "a" presents no load since both inputs are high. \bar{B} is high so the total input current of gate "b" must be sunk by A, i.e., A sees one load due to "b". Likewise, gate "c" presents one load to B, but none to A.

Both inputs to the gate "d" are low. This allows us to introduce load sharing. Since two driving lines are available to sink the current, we allow one-half load to each of them.

Thus, we arrive at the conclusion that, for this condition at least, lines A and B each must drive 1.5 loads rather than the 2 loads which would normally be assigned. It is proper that the sum of the loads "seen" by the driving elements be one less than the total number of gates driven since in a decoder one gate will always have both inputs high so will present no sink load to the driver.

If the other three states of the counter were examined, one would see that for each state, two drivers (flip-flop output) with "0" outputs "see" 1.5 loads while the other two see no load.

In like manner, one can show that for any complete (i.e., all states decoded) binary decoder, each input must drive $\frac{2^N-1}{N}$ loads. Where N is the number of variables (bits to be decoded). The advantage of utilizing load sharing becomes very apparent as the number of variables increases. For example, at 6 stages (64 states) the loading on each input line is 10.5 if load sharing is utilized, but 32 if it is not.

Load sharing is most easily applied when the decoding includes all of the possible states of the input variables, but, with care, may be applied to other PREDIC-TABLE cases. Consider the BCD sequence below:

	A	B	C	D	
0	0	0	0	0	
1	1	0	0	0	
2	0	1	0	0	
3	1	1	0	0	
4	0	0	1	0	
5	1	0	1	0	
6	0	1	1	0	
7	1	1	1	0	
8	0	0	0	1	
9	1	0	0	1	

States not included in the decoding

Loads for this decoding may be determined quite readily by treating the decoder as two decoders.

DECODER 1			
A	B	C	
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

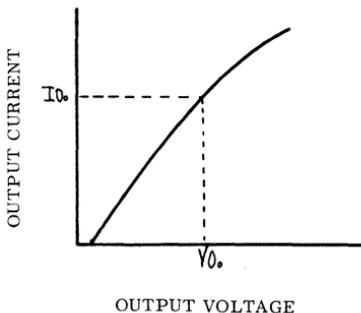
DECODER 2		
	A	D
8	0	1
9	1	1

Since Decoder 1 is a complete decoder, each input must drive 2-1/3 loads. In Decoder 2, A and \bar{A} must be able to drive a full load; D must be able to drive

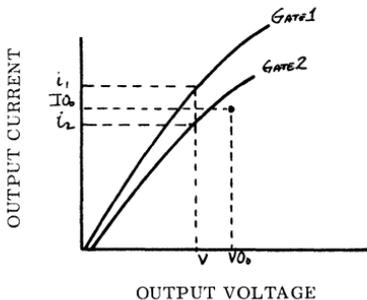
1.5 loads. Thus the total load is $3\frac{1}{3}$ loads on A and \bar{A} , $2\frac{1}{3}$ on B, \bar{B} , C, \bar{C} , and $1\frac{1}{2}$ loads on D. Likewise, the load on D is $1\frac{1}{2}$ loads; when D is low, (decoding for 0 and 1) B and C may both be high, but either A or \bar{A} must be low to aid D.

Note that load sharing can only be employed where inputs can be commoned (connected together) without changing the loading as in the "0" input current of a DTL gate. The "1" input current of DTL, TTL or RTL thus cannot be considered for load sharing.

What assurance do we have that the loads will divide as assumed? They probably will not unless the drivers are worst case elements, which is really the only condition of concern.



Consider that a 2-input gate is being driven by 2 gates, each of which exhibits an output characteristic as above. If each if fully loaded, the output voltage of each will be V_{00} , the guaranteed output voltage.



The usual case will be as above. At rated circuit (I_{00}) either gate will have an output voltage which is less than V_{00} . Gate 1 is assumed to be "better" than Gate 2.

The gates will be operating at a voltage near v where the sum of the currents, i_1 and i_2 is $2 I_{O_0}$. Gate 1 is carrying more than its share of the load, but by doing so, allows the output voltage of Gate 2 to decrease. Should any disturbance tend to make gate outputs be at appreciably different voltage levels, the currents would readjust to establish a new equilibrium condition.

ASYNCHRONOUS DATA REGISTERS

A problem frequently encountered in computer peripherals (and similar devices) is that of synchronizing input information with the internal functions of the peripheral.

The following discusses several solutions to the problem.

The circuit of Figure 2-1 is used when the problem is to detect whether or not input data was present during the sampling interval. As soon as Data goes to "1", the flip-flop will go to "1" and will remain "1" until the next Reset pulse.

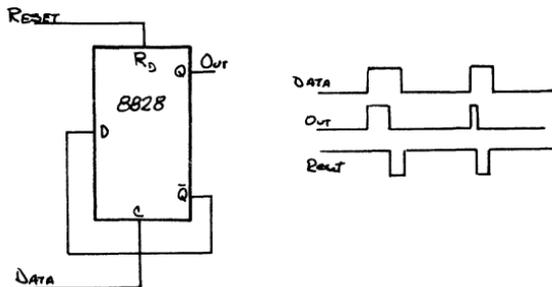


Figure 2-1

The circuit of Figure 2-2 is used when one wishes to sample an asynchronous input with a synchronous sample or clock pulse. The flip-flops will take the state of the data at the rise of the clock pulse. Changes in Data while the clock is high will have no effect.

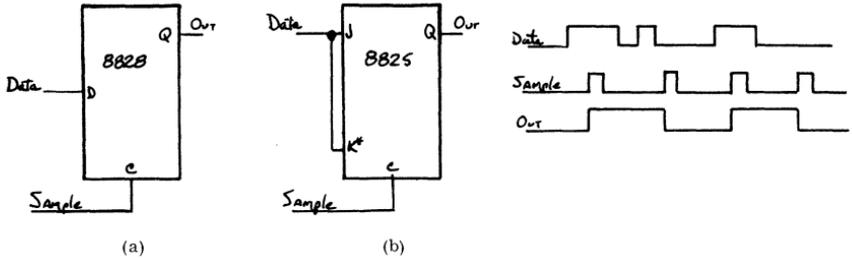


Figure 2-2

The circuit of Figure 2-3 is essentially the same as that of Figure 2-2 with the exception that the sampling will occur at the falling (negative going) edge of the clock pulse. If Data changes while clock is high, the output may be somewhat ambiguous if the change is within 75 nsec of the fall of the clock pulse. Generally this kind of sampling accuracy is acceptable.

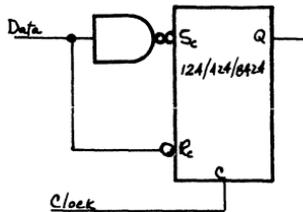


Figure 2-3

If the requirement is to convert RZ input information to NRZ information, the circuits of Figures 2-4, 2-5, 2-6 and 2-7 may be used. The waveforms are as in Figure 2-8.

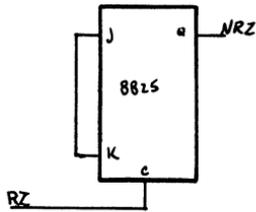


Figure 2-4

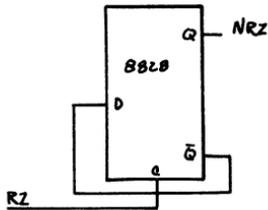


Figure 2-5

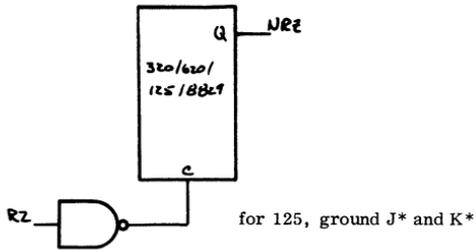


Figure 2-6

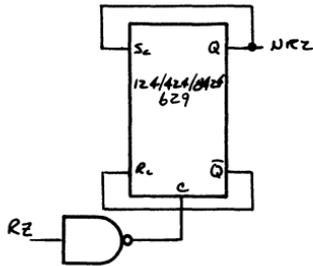


Figure 2-7

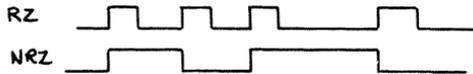


Figure 2-8

SOLVING HIGH FAN-OUT LOADING PROBLEMS

Most large synchronous systems require high fan-out drivers to clock the synchronous inputs of the system. The following will show how this condition can be satisfied with standard product.

The high fan-out solution is quite simple. Simply parallel sufficient gates so the sum of the individual gate fan-outs satisfy the load requirements. The term parallel means that not only the gate outputs are connected together but also the inputs. You will see (as in Figure 2-9) that in doing this the loading problem, if it exists, is moved back one gate location. This generally does not generate additional problems.

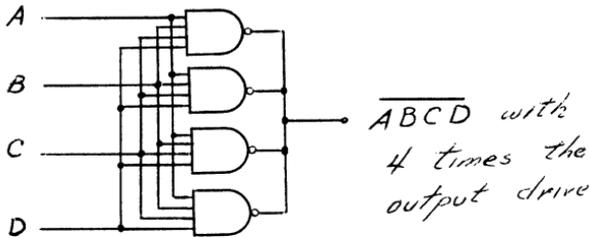


Figure 2-9

The only restrictions which should be established for these applications are as follows:

1. All gates should be of the same type and if possible should be within the same package.
2. Power supply decoupling should be exaggerated and applied close to the gates involved. This is especially important where gates with low impedance outputs are involved.

Let us now justify this solution by analyzing the application such as that of Figure 2-10.

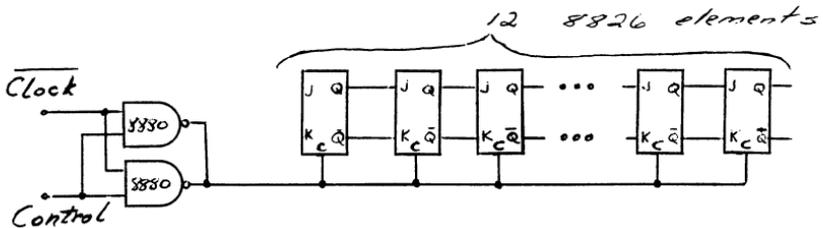


Figure 2-10

The steady state conditions for this solution are not difficult to justify since each gate will acquire a share of the available load. The gate with high sinking or sourcing capability will sink or source the most and the remainder taking a proportionate share. These steady state conditions have also been discussed in the previous subsection, "Use of Load Sharing to Reduce Fan-Out Requirements."

In describing the transient characteristics of elements connected in such a manner we must also agree that the dynamic load will divide proportionately to the ability of each gate to take such a load. This will then justify the solution while the gate outputs are in the active region.

There is now only one additional interval which must be described. The time interval where one gate is trying to switch and another has not yet begun to switch. Assume that we have two gates, one gate being a limit gate on the fast side and the other a limit gate on the slow side. Outputs of these gates have been shown in Figure 2-11. The slower gate has much longer storage or delay time than the faster gate.

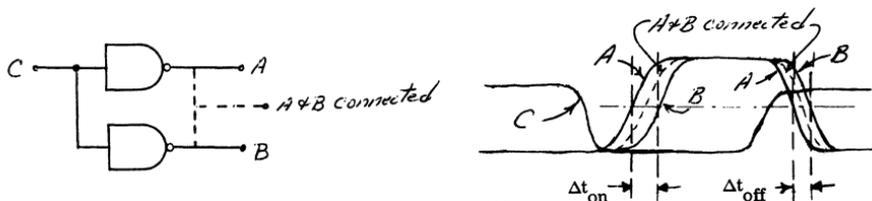


Figure 2-11

where: Δt_{on} is the incremental difference in the turn-on time
 Δt_{off} is the incremental difference in the turn-off time.

What happens when these gates have their outputs connected? You may recall from discrete transistor design that the storage time of a saturated transistor may be reduced by injecting large collector load currents into the saturated transistor operating in the storage time region. The surplus base charge is exhausted and the transistor is pulled out of saturation faster than would have occurred with a smaller collector load current. This is exactly what occurs when a fast gate drives into a slower gate. The faster gate provides the increased load to cause the second gate to recover more quickly. The net result of this is a mean characteristic gate of all gates connected in parallel. The dotted curve shows the gate output characteristic under this interconnection environment. This explanation shows what happens when two limit case gates are connected together. As many as 10 gates have been connected in this manner with the result being the characteristic of a mean gate.

Earlier in this subsection, we suggested that gates within the same package be paralleled if possible. This is because gates within the same package are quite similar in characteristics and would therefore minimize the differential delay between the gates.

The important thing to remember is that supply decoupling is quite important when large numbers of gates are connected in parallel. A value of $0.1\mu\text{fd}$ per gate is a good minimum value for the capacitor (between V_{CC} and Ground) being considered for these applications. There was a special reason for showing the circuit of Figure 2-10 for analysis. You can see the two 8880 gates connected in parallel will provide more clock driving capability than will one 8855 gate. Each solution would require half a package but generally the remaining 8880 gates can be more easily utilized in the remainder of the system design.

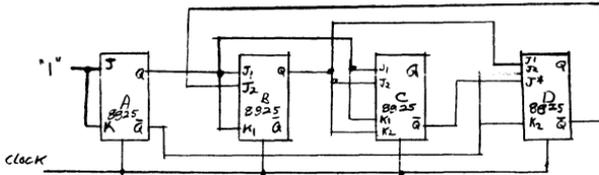
SECTION 3

TYPICAL SUBSYSTEM APPLICATIONS

COUNTERS

Synchronous BCD Decade Up Counter

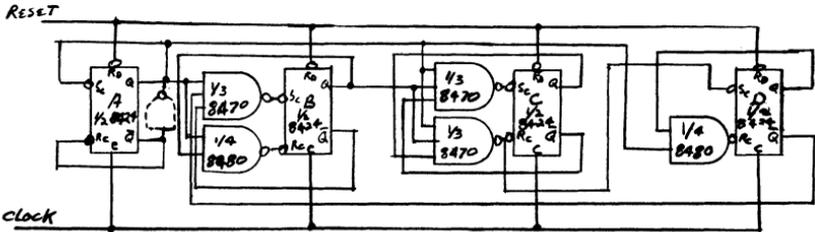
This design utilizes the built-in AND gates of the 8825.



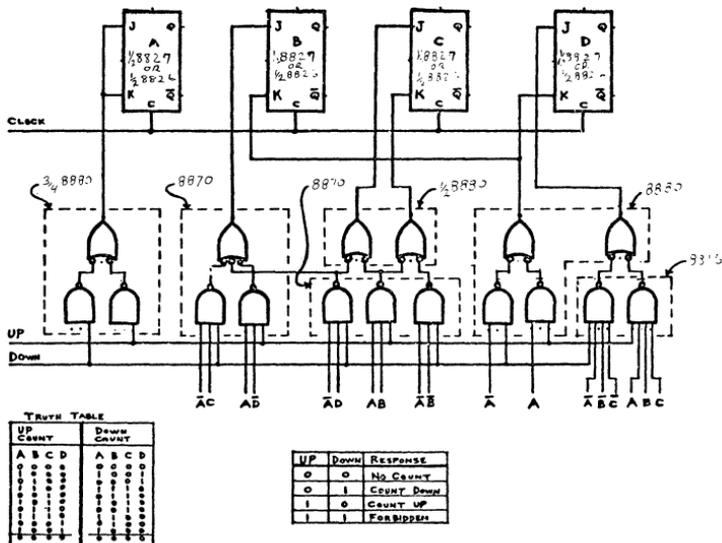
A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1
0	0	0	0

Another Synchronous BCD Decade Up Counter

This design utilizes a dual low-power flip-flop (8424) to realize a slower, but lower power consumption counter. To increase fan-out capability of the QA output, an 8480 can be connected as shown (by dotted gate). The fan-out will then be doubled.



Synchronous BCD Decade Up-Down Counter



BCD (8-4-2-1) Counter and Bi-Quinary Counter

Figure A, below, shows the 8280 connected as a BCD (8-4-2-1) counter. Typical input rates are above 35 MHz. The required external connection from A output to C₂ input uses adjacent pins to facilitate printed circuit board fabrication. The Bi-Quinary mode counter (- 5 followed by - 2) interconnection requirements for the 8280 are shown in Figure B. This mode is useful since the output of stage A is a square wave (typical input counting rates: 25 MHz). The 8280 counter is presettable to any state via the parallel entry gates which are enabled with the strobe.

The counting portion (exclude preset) of the 8280 can be implemented using two 8826's (dual J-K flip-flops), but two NAND gates or one NOR gate are required at the J input of the fourth flip-flop (D_j).

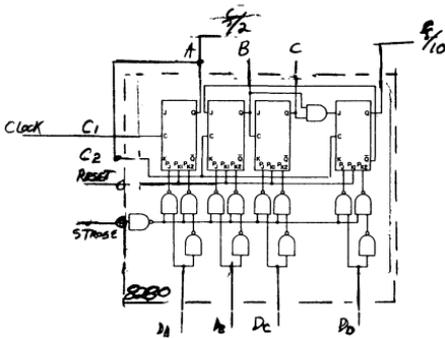


FIGURE A BCD COUNTER

A	B	C	D
0	0	0	0
0	0	0	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

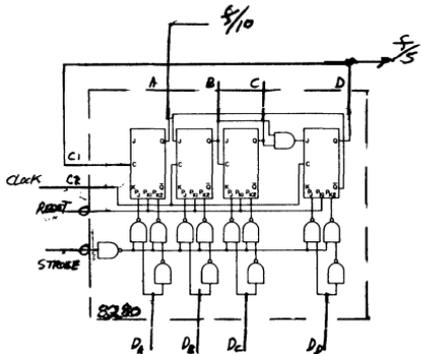
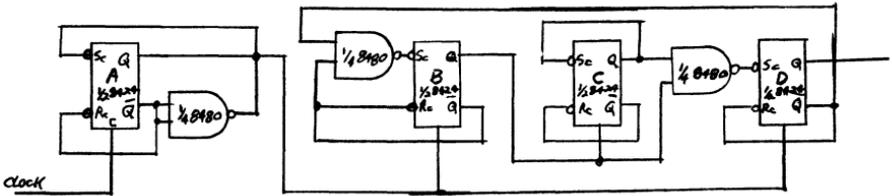


FIGURE B B1-QUINARY COUNTER

A	B	C	D
0	0	0	0
0	0	0	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Asynchronous BCD Decade Up Counter (1-2-4-8)(Low Power)

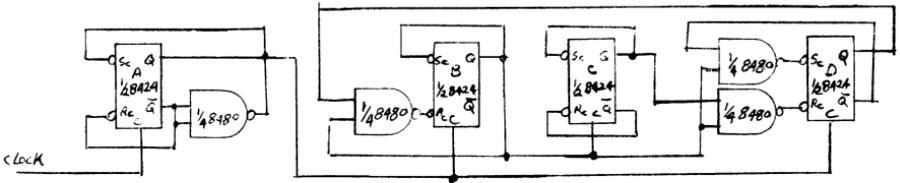
8400 Elements can be used for low-power BCD decade counters. This counter incorporates an 8424 dual RS/T flip-flop.



A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1

Asynchronous 1-2-4-2 Decade Counter

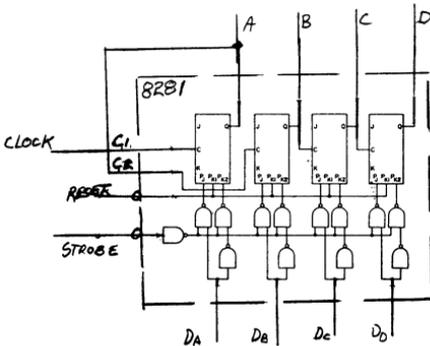
This counter provides the 1-2-4-2 count sequence utilizing the 8424 dual RS/T flip-flop.



A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	1
0	0	0	0

Binary Counter (8281)

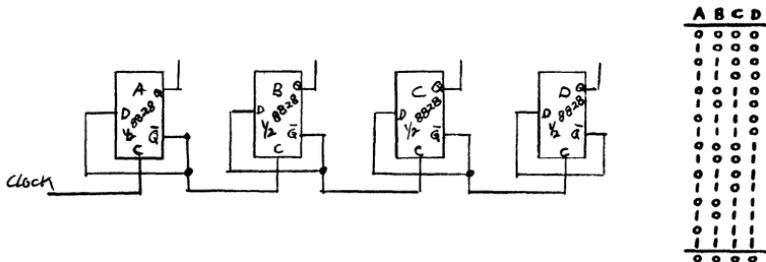
The Binary Counter interconnection requirement using the 8281 is shown below. Input clock signals applied to C_1 of 35 MHz can be accepted. Clock rates of 25 MHz can be accepted by the C_2 input. The 8281 is presetable to any state.



A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	1

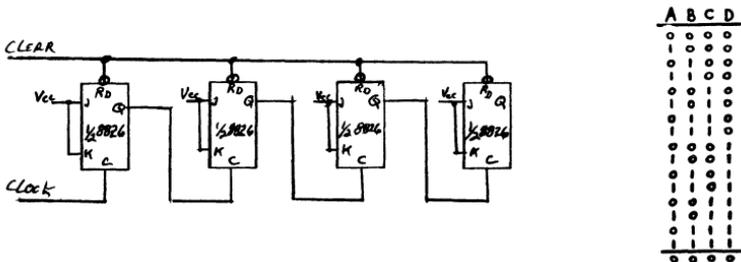
Asynchronous Divide by 16 Up Counter (8828)

The 8828 is a leading edge triggered flip-flop, therefore the clock input must be driven by the \bar{Q} output of the previous stage to perform the up count. If a down counter is required, the clock input must be driven by the Q output of the previous stage. Use this implementation in leading edge triggered systems. Speeds expected are 25 MHz.



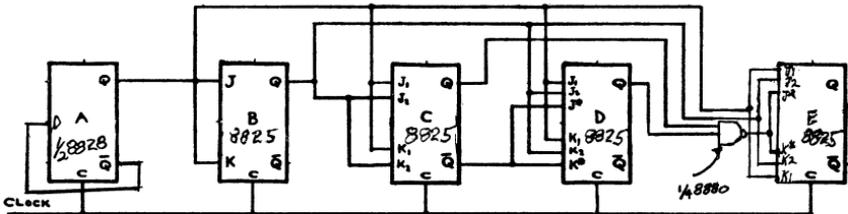
Another Asynchronous Divide by 16 Up Counter

The 8826 is a trailing edge trigger flip-flop, therefore the clock input must be driven by the Q output of the previous stage to perform the up count. If a down counter is required, the clock input must be driven by the \bar{Q} output of the previous stage. Speed expected 30 MHz.



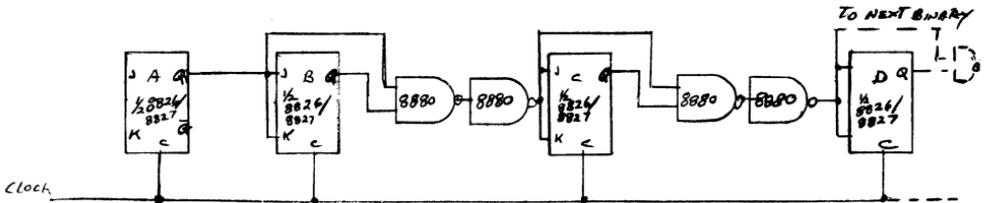
Synchronous Divide by 32 Up Counter

Four stages of a synchronous binary counter may be implemented without any external gates with the 8825 flip-flop. The first binary (A) is implemented with the 8828 dual D flip-flop as a part savings.



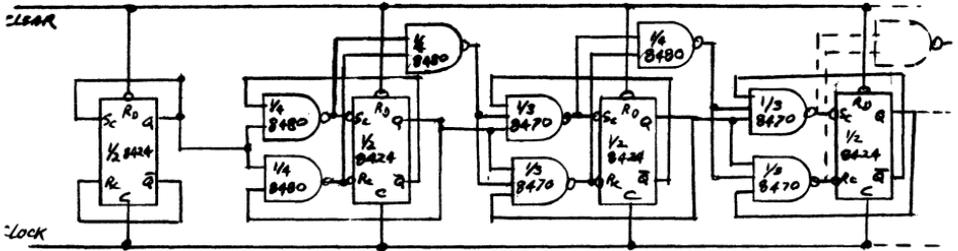
Synchronous Up Counter

The dual J-K flip-flop and the quad two-input gates are utilized for the up counter. The counter can be expanded by adding quad two-input gates and binaries. The speed will be limited by the number of gate propagation delays. Typical operation for four stages will be 14 MHz.



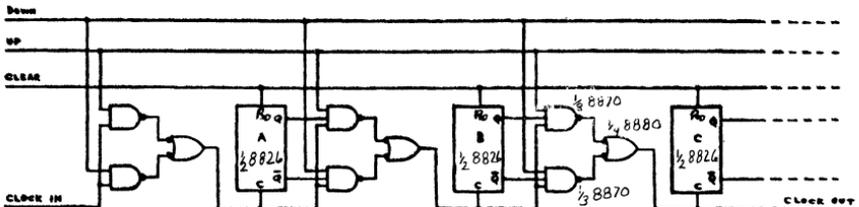
Synchronous Binary Counter

The dual RS/T binary and quad two-input and triple three-input low power gates are used to show the connection for a synchronous binary counter. The speed will be limited by the number of gate propagation delays. The speed for four stages will be approximately 6 MHz.



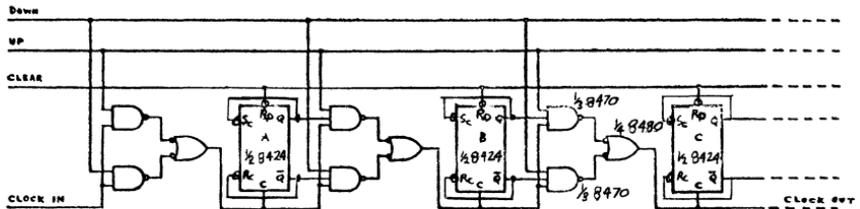
Binary Up-Down Counter

This counter is a modified ripple type counter which can be switched from up to down, or down to up, without causing incorrect counts. Whenever the clock line is logical ZERO all flip-flop clock inputs are unconditionally logical ZERO. The gating structure for each flip-flop is the same, hence it is very simple to add stages to the counter.



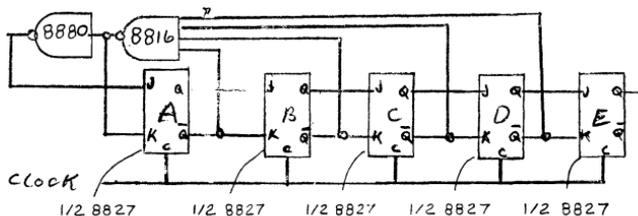
Another Binary Up-Down Counter

This counter is the same as the binary up-down counter above except there will be less power dissipation with this design since the 8400 elements are incorporated.



5- and 6-Bit Ring Counters, Self-Starting and Correcting

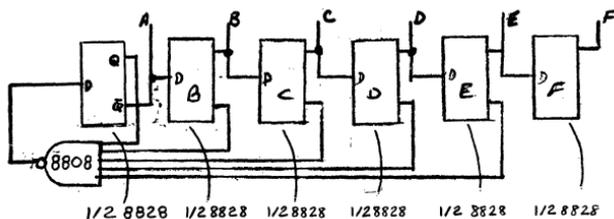
These ring counters feature low package count, high speed operation, and self-starting and correcting. Self-starting and correcting is accomplished by the gating structure in the feedback loop. The gates enter "0"s into the A binary until all inputs to the gate are "1"s. At that time all binaries are in the "0" state except the binary that is not connected in the feedback loop. The next clock pulse loads a "1" into the A binary which is the first state in the truth table.



TRUTH TABLE

A	B	C	D	E
1	0	0	0	0
1	0	0	0	0
0	1	0	0	0
0	0	1	0	0
0	0	0	1	0
0	0	0	0	1
1	0	0	0	0

5-Bit Ring Counter Using 8826 or 8827 Flip-Flops



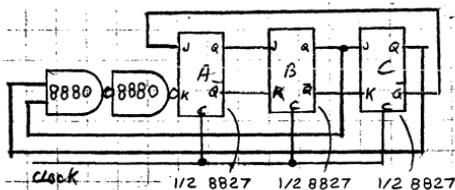
TRUTH TABLE

A	B	C	D	E	F
1	0	0	0	0	0
0	1	0	0	0	0
0	0	1	0	0	0
0	0	0	1	0	0
0	0	0	0	1	0
0	0	0	0	0	1
1	0	0	0	0	0

6-Bit Ring Counter Using 8828 Flip-Flop

3-, 4-, and 5-Bit Twisted Ring Counters, Self-Starting and Correcting

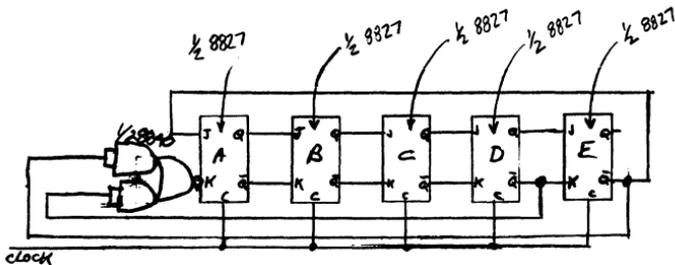
These twisted ring counters will correct themselves from stable sub-loop conditions which exist in the unused states by comparing the last and next-to-last binaries, thus controlling the input to the first binary.



TRUTH TABLE

A	B	C	UNUSED STATE
0	0	0	0 1 0
1	0	0	1 0 1
1	1	0	
1	1	1	
0	1	1	
0	0	1	

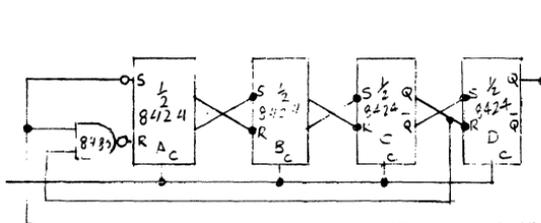
3-Bit Twisted Ring Counter



A	B	C	D	E
0	0	0	0	0
1	1	1	1	1
1	1	1	0	0
1	1	0	0	0
1	0	0	0	0
0	0	0	0	0
0	0	1	1	1
0	0	1	1	0
0	1	1	0	0
0	1	0	0	0
1	0	0	0	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
0	1	0	0	0

UNUSED TRAN
(TOTAL 22)

5-Bit Twisted Ring Counter



TRUTH TABLE

A	B	C	D
0	0	0	0
1	1	1	1
1	1	0	0
1	0	0	0
1	0	1	1
0	0	1	1
0	1	1	0
0	1	0	0

UNUSED STATE

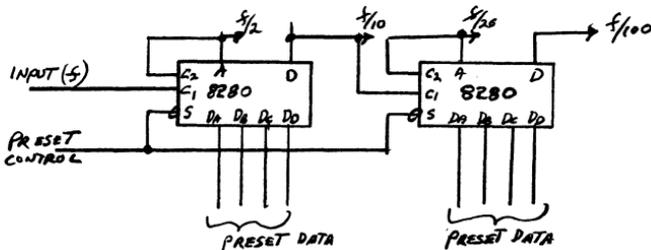
A	B	C	D
0	1	0	0
0	0	1	0
0	1	1	0
0	1	0	1
0	1	0	1
1	0	1	1
1	0	0	1

4-Bit Twisted Ring Counter

Special 8280/8281 Counter Applications

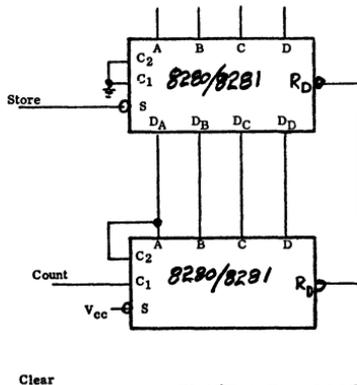
Counters in Cascade

The cascade configuration is applicable for either the 8280 (BCD mode shown) or the 8281. Some applications require a counter which counts a foreshortened sequence on the first cycle, but on subsequent cycles counts the full sequence. The 8280 and 8281 are well suited to these applications simply by presetting the starting count and allowing the normal modulus feedback to occur for modulus counting.



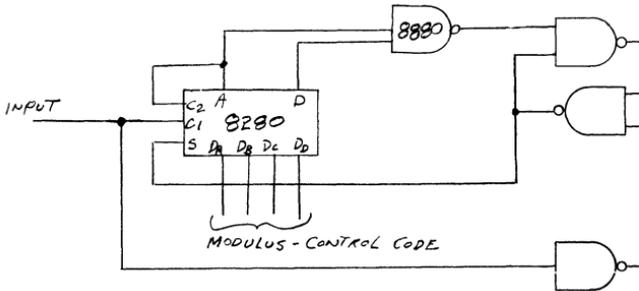
Count and Store

The count and store operation as illustrated below shows the suitability of the 8280 or 8281 as independent counters or storage elements. The parallel transfer to the storage element can be made synchronous with clock and accomplish a parallel transfer during the normal counting interval of the counter. This technique is sometimes used to obtain time differences since the count stored can later be subtracted from the final count of the counter.



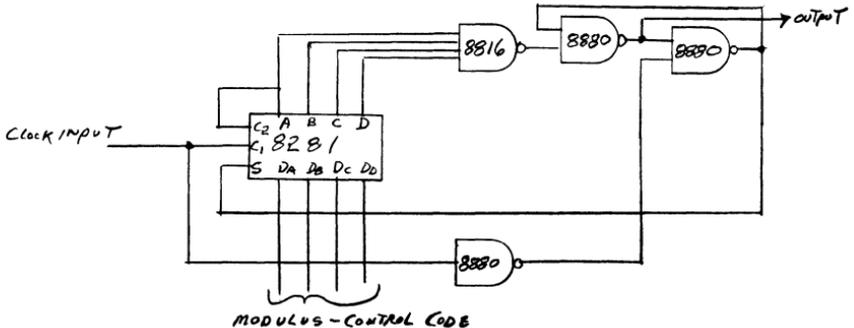
Single Stage Variable Modulus Counter (8280)

This counter sequences in its normal manner until the last state of the normal sequence is reached (1001). This state is detected by the gate, and the counter is parallel loaded with the modulus-control code presented. At the fall of the clock pulse, the counter resumes its normal sequence. The counter modulus N is 9 through 2 for preset of $10-(N+1)$, which is required because two counter states occur during one clock pulse interval. Typical counting rate of 4 MHz can be achieved.



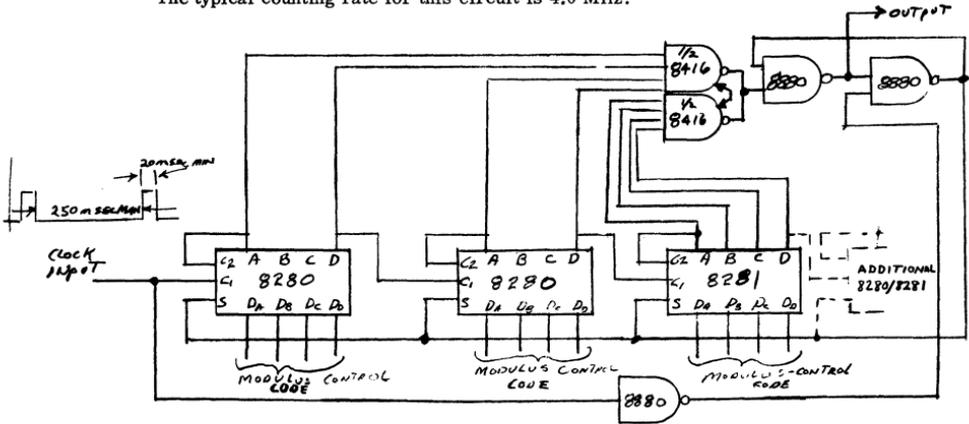
Single Stage Variable Modulus Counter (8281)

This counter sequence operates basically the same as the 8280 except it provides a modulus of 15 through 1. The latch circuit is necessary to ensure adequate strobe interval, which requires a 250 nanosecond width. Modulus N preset is $16-(N+1)$. Typical counting rate of 4.0 MHz can be achieved.



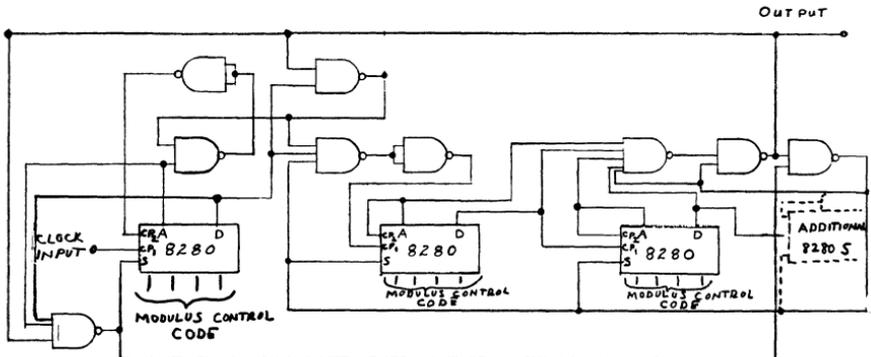
Cascaded Variable Modulus Counter (8280/8281)

This counter accomplishes multi-element storing of preset data by detecting the desired maximum count and enabling the strobe in a synchronous manner. The typical counting rate for this circuit is 4.0 MHz.



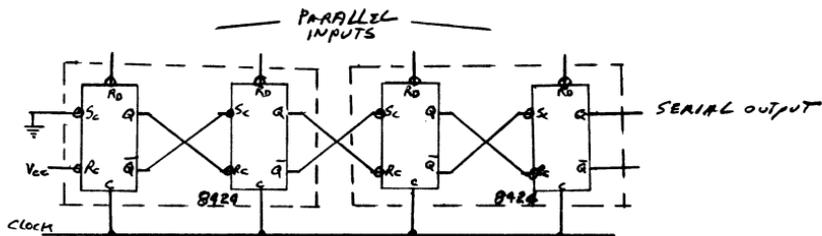
High Speed Variable Modulus Counter

High speed 12 to 15 MHz variable modulus counter can be achieved using the 8280's and 8400 (High Speed Gates). All decades except the least significant decade or the first decade will count in the same manner as the modulus counter above. Its strobe will be independent of the first decade. The strobe interval of the first decade can be 50ns since the "1" to "0" clocking transition is controlled with NAND gates. When this strobe occurs, it will also reset the latch (for strobing) of the other decades.

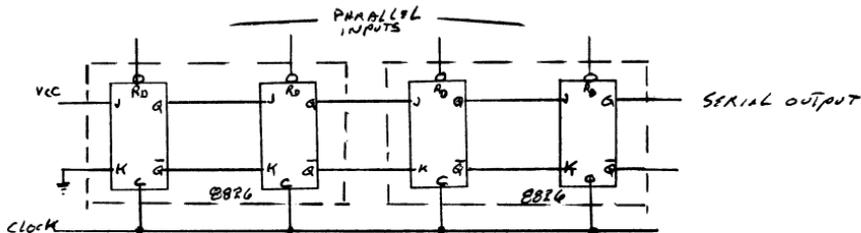


SHIFT REGISTERS

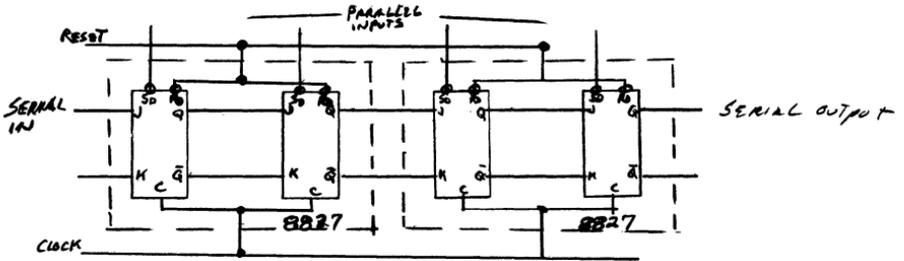
The shift registers below are connected using dual flip-flops; all except the 8828 are falling edge triggered. The 8827 and 8828 provide both asynchronous inputs (desirable for parallel transfer). The 8424 and 8826 can be parallel loaded by filling the register with "1"s. Each word is shifted out, then the R_D inputs can be used to insert "0"s at the proper locations.



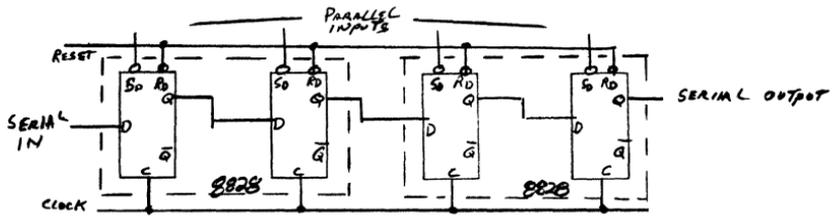
Parallel Transfer - Serial Output Shift Register



Parallel Transfer - Serial Output Shift Register



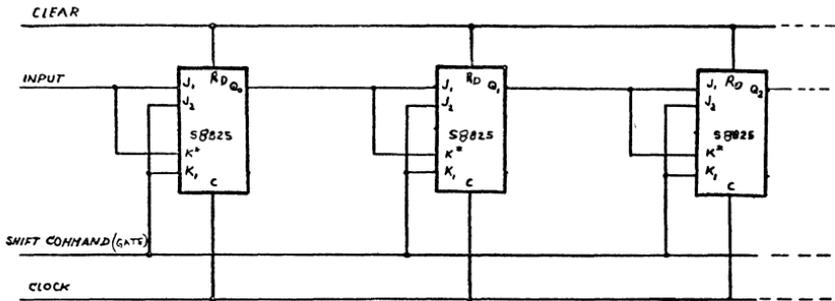
Serial - Parallel Entry Shift Register



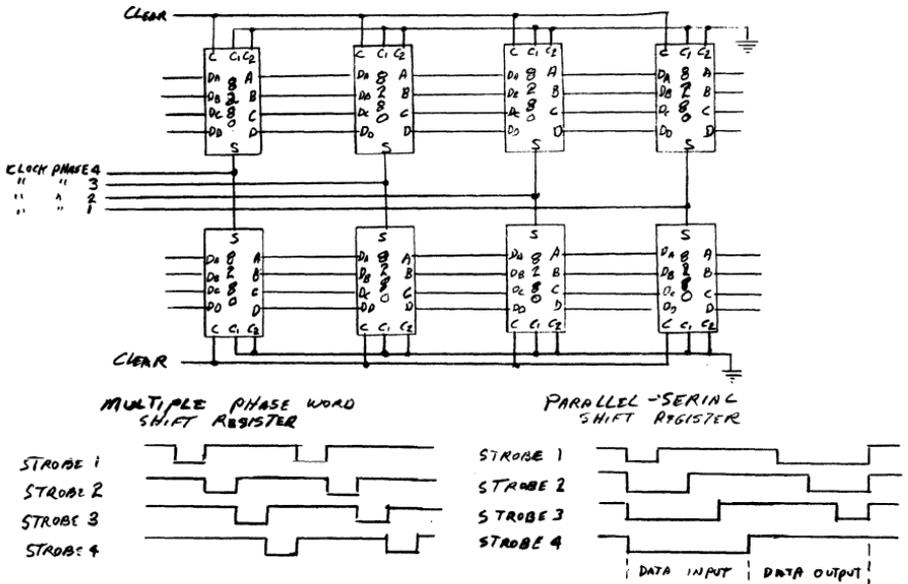
Serial - Parallel Entry Shift Register

Gated Shift Register

The gated shift register is a simple shift right register with a shift command control line. When the shift command is logical "0", the contents of the register will be unchanged by clock line pulses. When the shift command is logical "1", the contents of the register will be shifted one bit to the right for each clock pulse.



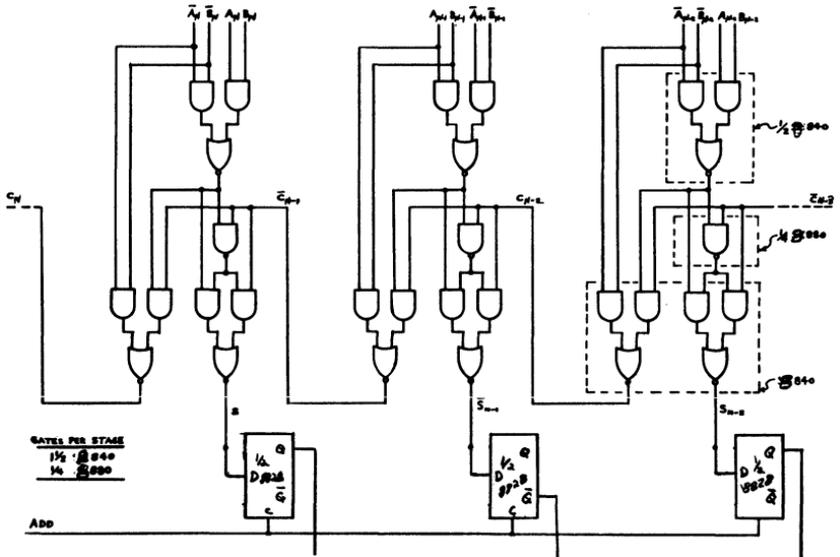
The following circuit shows how (using 8280/8281) to obtain shift register characteristics of N elements in length by using an N phase clock strobe system. The N elements would be capable of storing 4N bits which could be organized in 4 bit groups. This can be useful for systems requiring relatively small, parallel output temporary memory storage.



ADDERS, COMPARATORS, AND DECODERS

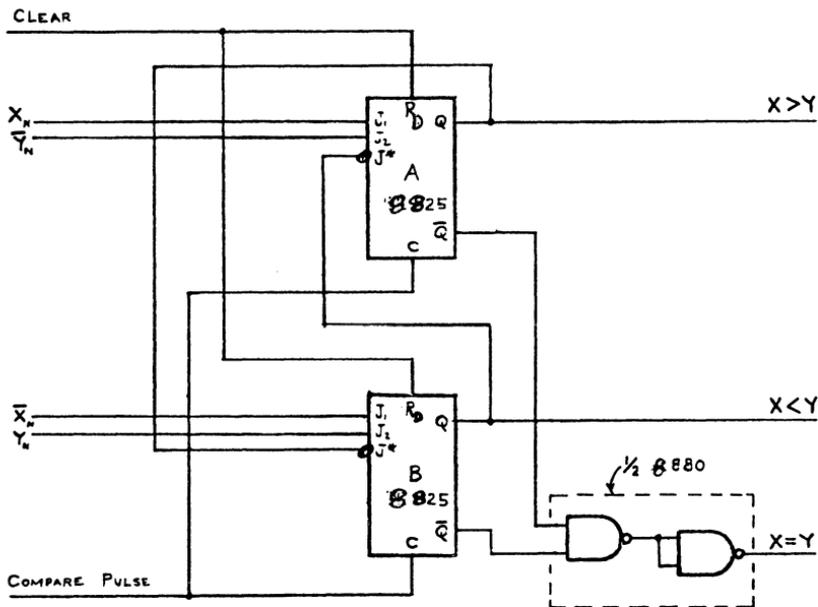
Parallel Binary Addition

The carry propagation delay is minimized by alternating between CARRY and CARRY in the carry propagation delay path. It is necessary to alternate the polarity of inputs A and B from stage to stage to do this. The carry propagation delay is determined by the 8840. The 8840 delay is equivalent to one level of logic; therefore, the carry propagation per stage is only one gate delay. Alternating the Q and \bar{Q} of the 8828 flip-flop eliminates the need for inverting SUM outputs.

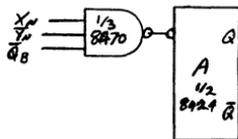


Serial Comparator

This serial comparator utilizes the gated inputs of the 8825 to minimize package count. A clear pulse must be provided before comparison begins. The serial comparison must begin with the most significant bits of binary words X and Y. The appropriate output (less than, equal to, greater than) will be a logical "1", and the other two outputs will be a logical "0" upon completion of the comparison. A clear pulse must be provided prior to comparison.



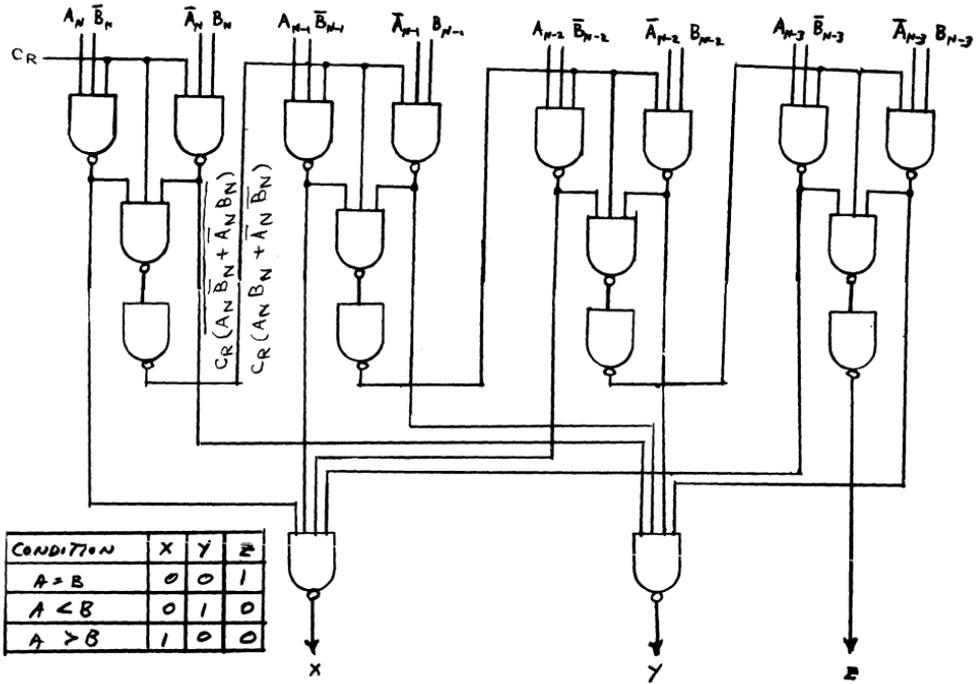
This serial comparator can be implemented using the 8424 with an 8470 as the input control gate. There is a reduction in power consumption and slight reduction in part count.



NOTE: Using the 8825, the J* input is Q_B but for 8470/8424 the complement is the input \bar{Q}_B .

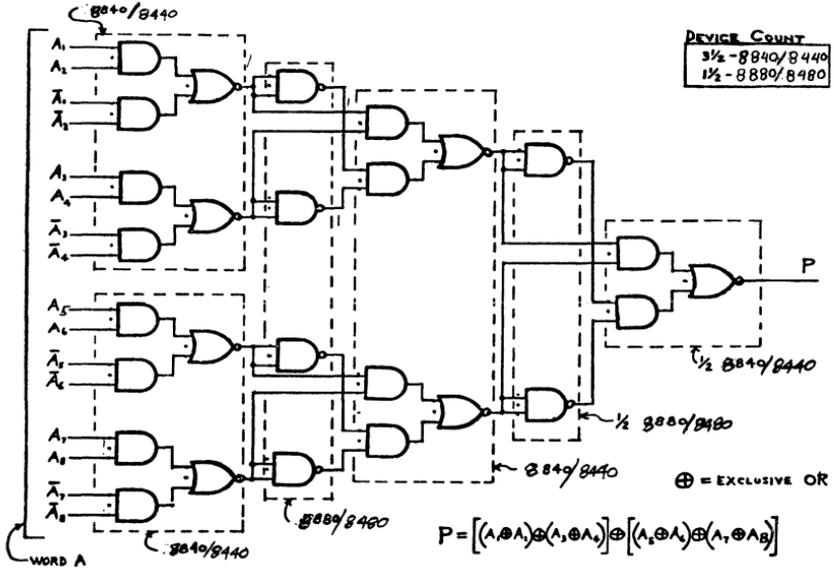
Parallel Comparator

The parallel comparator is most useful in high speed systems. All bits are compared simultaneously and the speed is limited only by two propagation delays per stage. The appropriate output (less than, equal to, greater than) will be a logical "1", and the other two outputs will be a logical "0" upon completion of the comparison.



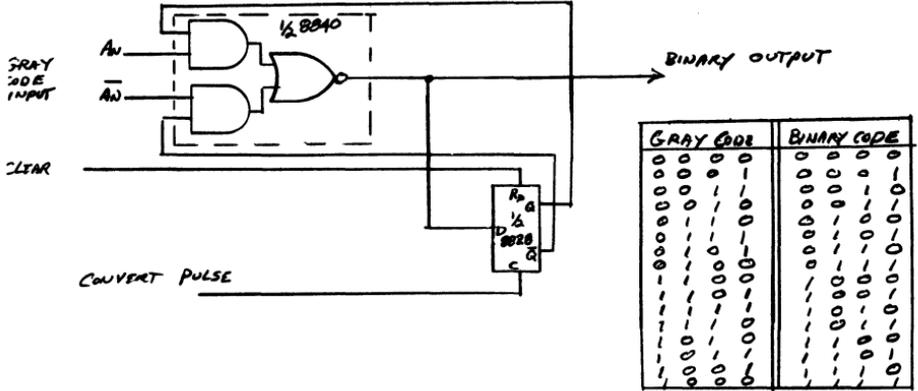
8-Bit Parallel Parity Generator-Tester

The output (P) will be a logic "0" when word A contains an even number of logical "1"s, and a logical "1" when word A contains an odd number of logical "1"s.

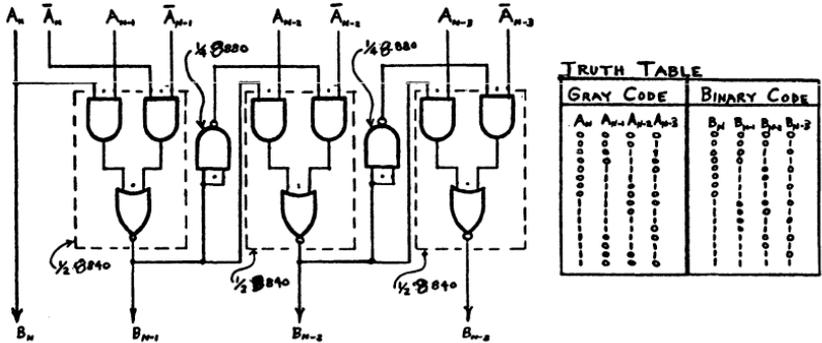


Gray to Binary Conversion, Serial

The serial gray to binary conversion must begin with the most significant bit. Also a clear pulse must be provided prior to the first serial bit.

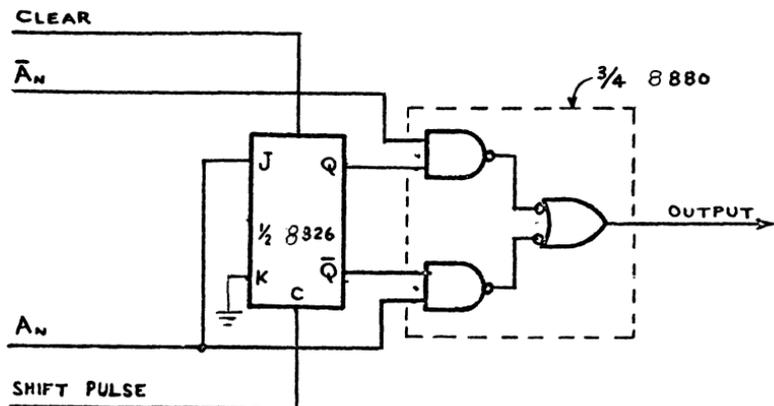


Parallel Gray to Binary Conversion



Serial Two's Complementer

A clear pulse must be provided before complementing begins. The serial two's complementer must begin with the least significant bit of the binary number.





APPLICATIONS MEMO

T²L "1" LEVEL INPUT CHARACTERISTICS

The system designer quite often is interested in what are the true input characteristics of our T²L elements. The unique characteristics of these parts have been summarized below:

1. The "1" input current is related to inverse β of the input transistor.
2. The input leakage is highest when one of the inputs is connected to ground while another input is connected to a logic "1" input state. The addition of a second input connected to ground does not change the input current established by that of the first ground connected emitter.
3. The successive addition of emitters connected to a logic "1" state produces a linear addition of input leakage currents.
4. The input leakage current variation as a function of temperature approximates the variation of inverse β as a function of temperature.

The input characteristic is that of a transistor whose input is the emitter junction. This transistor is always in a forward-biased mode. The forward-biased modes are either that of a forward-biased transistor in the normal mode as when the emitter is connected to ground, or a forward-biased transistor in the inverted mode as when the emitters are connected to a logical "1" input. The term inverted mode is used to describe a transistor operating in a mode where the base collector junction is the forward-biased region; and the emitter acts as the conventional collector junction. In this operation mode the transistor equations are still rigorous; however, the numbers have been modified due to the inverted characteristics. The circuit is also even further modified by forcing the transistor to be a very inefficient transistor when operated in the inverted mode. Figure I, shown below indicated this equivalent internal characteristic.

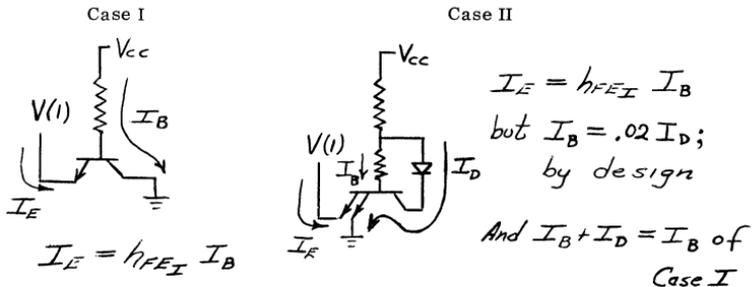


Figure I

We can see that the Case II technique results in an effective reduction in inverse β by 50 thus causing an input current reduction by a factor of 50. The Case II technique is utilized in the 8800 and 8H00 elements.

The point of all of this discussion is that the input characteristics differ significantly from the input characteristics of the conventional DTL input structure. As an example: The input leakage of the DTL gate will follow the input leakage equation for conventional diode. The leakage at 125° C will be approximately 100 times the leakage at 25° C. For the T²L logic input, the input current approximately doubles from 25° C to 125° C, (Figure II). This change in the T²L input current is not basically due to the leakage phenomena, but is fundamentally due to a change in effective inverted current gain. The equations for input leakage are shown in Figure I.

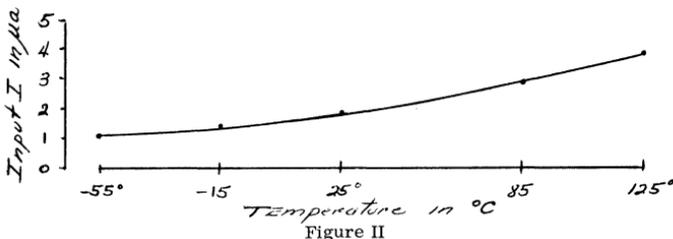


Figure II

Several other significant characteristics can be observed with T²L input structures. One being the fact that the current flowing thru a single emitter with all inputs to a gate in logic "1" state is less than if one of the many inputs were connected to ground. The change in input current is very nearly directly proportional to the change in current flowing in the forward-biased collector junction. Additional inputs that may be grounded do not change the magnitude of input current from that of the first ground connected input emitter.

Let us now consider the condition where multiple inputs are connected to a logic "1" input. This may occur quite often when one used the recommended paralleling of unused inputs to a driven gate connection. One finds that as inputs are connected successively the current addition is a linear and algebraic sum; therefore, if one were to connect all the inputs of a dual four input gate together so that the gate is used purely as an inverter the logic "1" load would be 4 times that of a conventional gate. The logic "0" load, however, would still be the 1 input "0" load. You can see then that it is very important that the "1" fan-out of a gate have significantly more fan-out capability than logic "0" output capability. Again this is especially true if one reviews Application Memo #57 dealing with load sharing.



L. Brock

APPLICATIONS MEMO

100/400J COMPATABILITY

The ability to interface 100J series DTL elements with 400J DTL performance low power elements is desirable in certain low power system applications. To optimize system performance, design engineers will often use both 100 and 400 series devices in the same system. The purpose of this memo is to provide an easy reference for determining 100/400 interface requirements for SE and NE products in the J, 14-lead flat package.

When interfacing different digital logic series elements such as the SE180J DTL device and the SE480J TTL device, consideration must be given to required DC noise margins, DC Fan-Out/Fan-In and AC loading. The 180 gate and the 480 gate are shown in Figure 1 (a) and (b) respectively. The 180 is DTL in structure with switching delays of 20 ns and power consumption of 10 mW per gate typically. The 480 is a TTL circuit with a 500 Ω resistor in the emitter of the active pull-up transistor. This resistor raises the typically low TTL output impedance producing DTL switching delays while maintaining a low power consumption of about 3 to 4 mW per gate. Typically, the 400 gates have slightly faster switching speeds and consume about one-third the power of the 100 gates, as shown in Figures 2 and 3.

The Guaranteed Worst Case* DC Parameters, shown in Table I, enables the designer to determine worst case loading parameters (both fan-in and fan-out) as well as worst case DC noise margin for any combination of 100 and 400 gates. Table II uses the basic information in Table I to generate the Guaranteed Worst Case Fan-Out Capability of any 100 or 400 series output structure driving a specific number of 100 or 400 series input structures; e.g., a SE455J gate can drive six SE180J gates.

The designer building a system using the 100 series elements might have critical areas within his system which require decreasing the power consumption. By using Tables I and II, the designer now has the tools with which he can interface the 100 series elements with the lower power 400 series elements.

*Guaranteed Worst Case for any parameter refers to the worst case V_{CC} , temperature and loading conditions for measuring minimum and/or maximum limits as guaranteed by the data sheet.

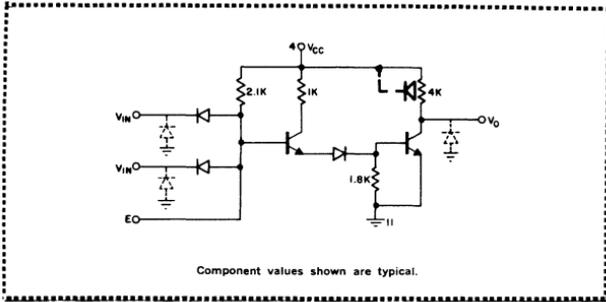


Fig. 1 (a). The 180 Gate Structure

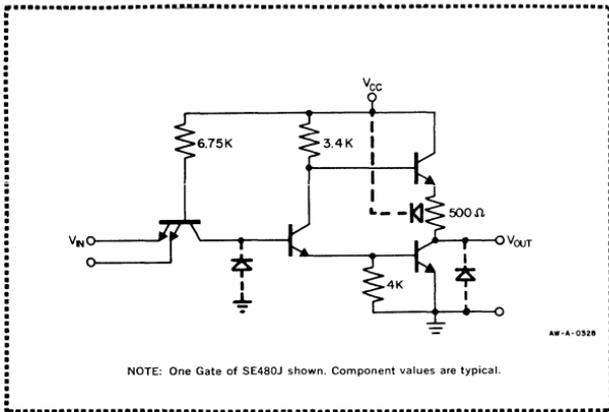


Fig. 1 (b). The 480 Gate Structure

FIGURE 2. A typical t_{on} and t_{off} vs. Load Capacitance for the SE180J and SE480J

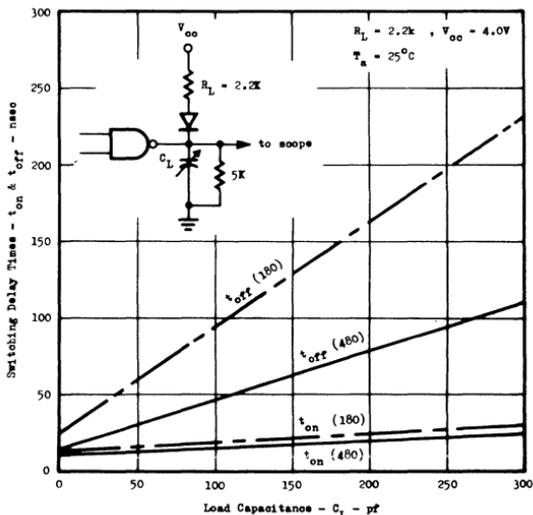


FIGURE 3. A Typical Consumption vs V_{oo} for the SE180J and SE480J $T_a = +25^\circ C$ unloaded per gate.

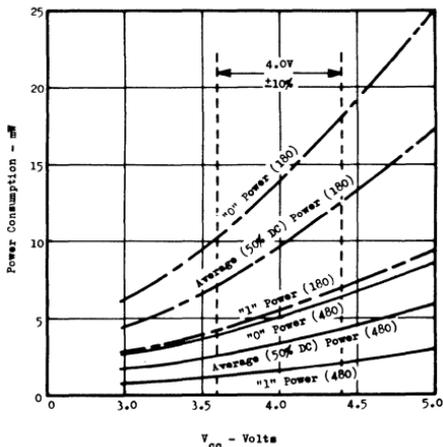


TABLE I 100/400 SERIES GUARANTEED WORST CASE DC PARAMETERS

	V_{O_o}	V_{O_i}	V_{1_o}	V_{1_i}	I_{O_o}	I_{O_i}	I_{1_o}	I_{1_i}
111, 112 ⁽¹⁾ 155, 156	0.45V	0.8V	3.2V 3.1V	2.3V	34.2 mA	-1.8 mA	-190 μ A	10 μ A
116, 170, 180 720, 721, 727, 730	0.45V	0.8V	3.1V	2.3V	10.9 mA	-1.8 mA	-60 μ A	10 μ A
124, 729 R _D , S _D R _C , S _C (2)	0.45V	0.55V 0.60V	3.1V	2.0V 2.0V	12.6 mA	-1.8 mA -1.3 mA	-70 μ A	10 μ A 10 μ A
125 J, K J*, K* P _J , P _K Clock	0.45V	0.8V	3.0V	2.2V	16 mA	-1.15 mA -0.9 mA -3.6 mA -4.5 mA	-80 μ A	10 μ A 10 μ A 20 μ A 25 μ A
161, 162 G	0.45V	1.0V	3.1V	3.1V	7.2 mA	-100 μ A	-40 μ A	125 μ A
415 ⁽¹⁾ , 417 ⁽¹⁾	0.30V	0.8V	2.3V ⁽¹⁾	2.1V	4.5 mA	-0.93 mA	-180 μ A ⁽¹⁾	10 μ A
416	0.30V	0.8V	2.3V	2.1V	3.7 mA	-0.93 mA	-180 μ A	10 μ A
470, 471 ⁽¹⁾ , 480, 481 ⁽¹⁾ , 490	0.30V	0.70V	2.3V	1.9V	3.7 mA	-0.62 mA	-180 μ A	20 μ A
440	0.30V	0.70V	2.3V	1.9V	3.7 mA	-0.62 mA	-180 μ A	20 μ A
455	0.30V	0.70V	2.3V	1.9V	12 mA	-0.96 mA	-500 μ A	20 μ A
424 R _D R _C ; S _C (2)	0.30V	0.70V 0.45V (2)	2.3V	1.9V 2.3V (2)	3.7 mA	-0.62 mA -0.42 mA	-180 μ A	20 μ A 10 μ A
425 R _D S _D R _C , S _C (2)	0.30V	0.70V 0.70V 0.45V (2)	2.3V	1.9V 1.9V 2.3V (2)	3.7 mA	-1.24 mA -0.62 mA -0.42 mA	-180 μ A	40 μ A 20 μ A 10 μ A

1. Rare collector devices with $R_L = 4.4K \Omega$ connected externally to $V_{CC} = 3.6V$.
2. Taking into consideration the loading conditions when the clock is high and, R_C and S_C change states. The clock R_C and S_C lines must be driven from the same type of gate; either 100 or 400 series gate but not both. V_{O_i} & V_{1_i} are not guaranteed numbers.



APPLICATIONS MEMO

"DEAR AUNT ABBE"

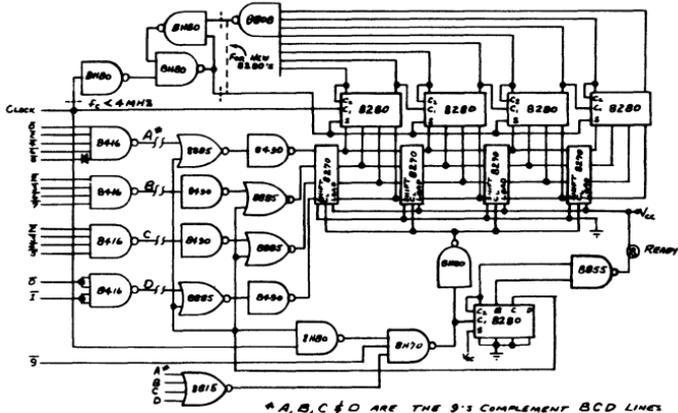
- Subjects:
1. Why "Dear Aunt Abbe" ?
 2. 8280 Application
 3. 8000 Series at -5V
 4. 8T18 Voltage Translator
 5. 8T80 Voltage Translator
 6. J-K Binary Inhibit

Q. What's the purpose of this Application Memo?

A. Finally, the Application Engineers have the basic framework with which information and new applications of a low priority nature can be distributed to the troops. Previously, unless applications were major enough to warrant a full fledged Application Memo or Note, the Application Engineer, through no fault of his own, just filed all low priority applications into his "Bag of Tricks." This Memo will serve as a "pressure release valve" for these minor applications and will be updated frequently.

Q. Is it possible to remotely program a multiple decade Variable Modulus Counter using a minimum number of interconnections?

A. Yes. The problem can be solved with the use of only five interconnections and a ground — four lines of 9's complement BCD and a 9 line plus ground — shown in Figure 1.



- Q. Can the 8000 series be operated with V_{CC} connected to ground and the ground terminal connected to a $-5V$ supply?
- A. No problem! Just be careful with test equipment grounds. Don't ground the $-5V \pm 5\%$ supply!
- Q. Is there a positive to negative voltage translator available with the 8000 series?
- A. The 8T18 high-to-low voltage interface elements work perfectly in this application if the following connections are made: ground to a $-5V \pm 5\%$ supply, V_{CC1} to ground and V_{CC2} to a $+15V \pm 5\%$ supply for $-55^{\circ}C$ to $+125^{\circ}C$ operation or V_{CC2} to a $+5V \pm 5\%$ supply for $-25^{\circ}C$ to $+125^{\circ}C$ operation. See Figure 2a.

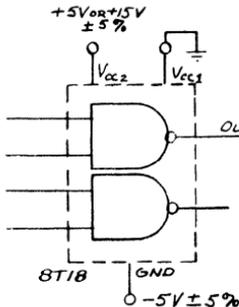


FIGURE 2a.

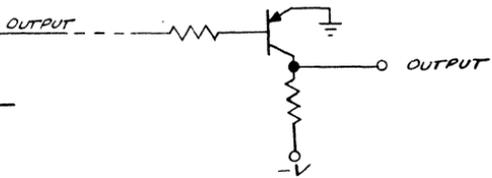


FIGURE 2b.

If the $-5V \pm 5\%$ power supplies are used, the designer has the capability of going from $+5V$ supply digital systems such as TTL or DTL to $-5V$ supply systems. An external PNP can be added to the output permitting large voltage swings, Figure 2b.

- Q. Does Signetics have a negative to positive voltage logic translator?
- A. The 8T80 and 8T90 can be used to translate from negative to positive voltage logic systems as shown in Figure 3.

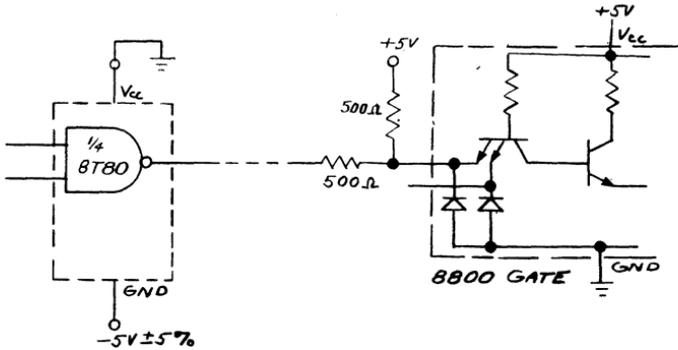
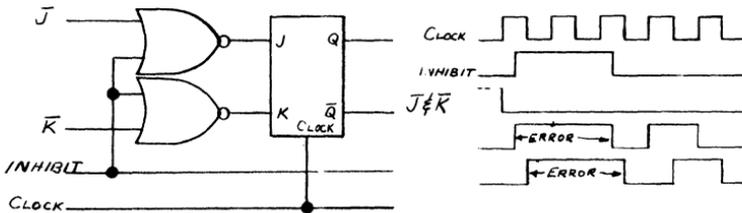


FIGURE 3

The inputs to the 8800 gates have diffused clamping diodes on them to limit negative input excursions.

- Q. When using the J and K inputs of the 8821, 8822, and 8824 or the 321 and 322 to inhibit normal operation as shown in Figure 4a, what problems, if any, will there be?

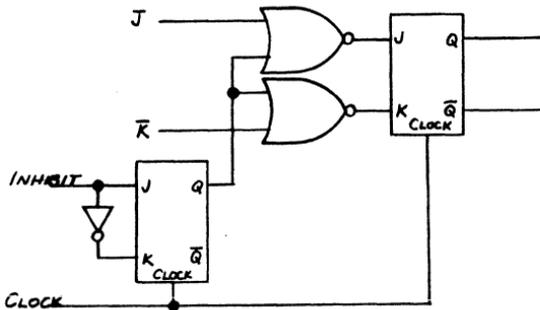
FIGURE 4A



- A. There is definitely the possibility of problems. If the asynchronous inhibit is actuated while the clock line is high, the master can be toggled due to either a threshold differential between the J and K inputs or a speed differential between gates #1 and #2.

Solution: Make the inhibit signal synchronous with the clock signal, as shown in Figure 4b.

FIGURE 4B





APPLICATIONS MEMO

"DEAR AUNT ABBE"

on

Kelvin connectors

Utilogic II fan-out, noise margins

Schmitt trigger using Utilogic II OR gate

Ripple counter using Utilogic II Binary

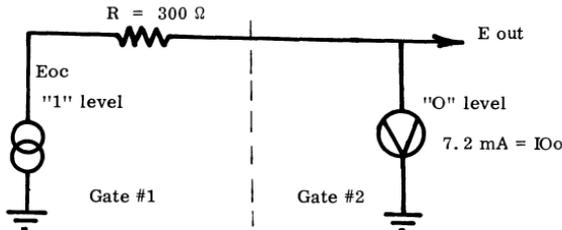
516 Operational Amplifier

SP600 collector logic

- Q. Signetics tester literature has made reference to Kelvin Connectors. What are they?
- A. The Kelvin (Lord) Connector is one designed to allow precision remote sensing. As applied to an integrated circuit tester, the Kelvin Connector provides two connector contacts for each pin on the IC. The test condition, e.g. $I_{Oo} = 30 \text{ mA}$ is applied to one contact; the sensor is connected through the other. Voltage drops due to the large current will cause measurement errors if the sensing is done at the source of the applied condition; however, by sensing at the pin of the IC, the sensor is not affected.
- A further advantage is gained by using two contacts - by checking for continuity between the contacts, it is possible to ensure that the connector is effecting good electrical contact with the IC.
- Q. I need a high fan out driver for a Utilogic system. Which device do you recommend?
- A. The 855 will have fan out of 30 to 320 clock inputs. To facilitate this use, the NE855K is grouped with LU3XXK on the price list. Note: The 855 is not suitable for driving Utilogic source loads.
- Q. Please explain the collector logic usage rules for SP600A.
- A. Each collector tied to another contributes a nominal load of 1/2 fan-out; however, resistor tolerances require that 3/4 load be allowed. The fan out of the gate is 8; therefore, 7 loads may be used by collector connection (the useful fan out will then be 1). This allows 9 collectors to be driven from each output, or that 10 outputs may be connected together.

- Q. I have designed a 516 amplifier using the technique described in Application Memo #71, page 4. It has a low level oscillation. I have good power supply by-passing and have taken great care with my circuit layout. What is wrong?
- A. Occasionally a production run of 516's will have devices with exceptionally high gain. Devices have been seen with open loop gains of 90 dB. When this occurs, the corner frequencies will be lower and the second corner frequency may be as low as 1 MHz. An amplifier design, using the techniques of Application Memo #71, should allow for this lower corner frequency in worst case type conditions.
- Q. Is the 1.2 volt typical noise threshold figure on SU 320 Data Sheet actually a noise margin figure?
- A. The noise threshold figure represents an indication of the maximum amount of external noise that can be introduced at a circuit ground without upsetting its operation. It can be related to the noise margin by knowing the test parameters. In the case of the SU 320, the 1.2 volt typical threshold point is arrived at by feeding 500 ns. pulses of increasing amplitude to the ground (pin 1) of a SU 320 under test through a $\frac{30\Omega}{50\Omega}$ resistor divider network.
- The threshold is reached for 1.2 volt input pulses which correspond to $1.2 \text{ V} \frac{30\Omega}{50\Omega} = 720 \text{ mV}$ actual noise pulse amplitude at circuit ground. This is the amount of noise that can be added to the $V_{CE}(\text{SAT})$ voltage at logic 'O' of circuit under test to make its output reach the input threshold of the load circuit. That amount of noise is called 'O' level noise margin. The figure can be checked from existing test curves which indicate that the SU 320 'O' level typical noise margin is 800 mV at -20°C , 700 mV at $+25^\circ \text{C}$ and 500 mV at $+80^\circ \text{C}$. From the same graph, '1' level typical noise margin would be 300 mV at -20°C , 500 mV at $+25^\circ \text{C}$ and 750 mV at $+80^\circ \text{C}$.
- Q. What do I do with pins 3 and 9 on the 516?
- A. These pins will be found most useful when it is necessary to minimize high frequency output stage crossover distortion. A 200k ohm resistor, connected between pins 9 and 10 and/or 2 and 3, will reduce crossover distortion appreciably. If not being used, these pins should be left open.
- Q. Can I operate the 516 on ± 12 Volt power supplies?
- A. Yes, the 516 may be operated on power supplies as low as ± 6 Volts, although at reduced output voltage swing and reduced open loop gain.
- Q. Do I have to operate the 516 from symmetrical power supplies?
- A. No, they may be operated from non-symmetrical supplies or a single power supply as long as the input common mode range is not exceeded.

- Q. 400-Series and 8400-Series gates with active pull-up cannot be used in collector logic configurations. Is this because the currents incurred would damage the device?
- A. No, the current levels which would be incurred with 8400 devices are not high enough to cause device damage. Actually, the output may be shorted to ground without damage. The restriction is because the output states may be ambiguous.



The figure above, shows the worst-case model for an 8480 in collector logic configuration (at +5.0 volts).

The numbers are obtained as follows:

E_{oc} is taken as the "1" output voltage.

$$R = \frac{E_{oc}}{\text{Output short circuit current}} = \frac{3.6}{12} = 300 \Omega$$

$I_o = \text{"0" Output current} = 7.2 \text{ mA}$.

7.2 mA conducted through the 300 impedance causes a drop of

$$7.2 (.3) = 2.16 \approx 2.2 \text{ volts.}$$

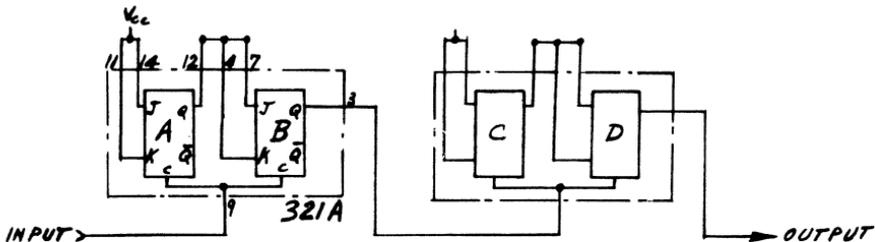
$$E_{\text{out}} = E_{oc} - 2.2 = 3.6 - 2.2 = 1.4 \text{ volts.}$$

Since 1.4 volts is neither a "0" or a "1", the output level is undefined; therefore, the configuration cannot be used.

- Q. I have compensated a 516 amplifier in accordance with Figure 3 of Application Memo #71, and it oscillates. What is wrong?
- A. Some 516's with date codes of late 1967 and 1968, show increased open loop gains (5 db) over earlier runs and will require a modification in the frequency compensation. The $0.05 \mu\text{F}$ capacitor may be changed to $0.1 \mu\text{F}$ or a 10 ohm resistor may be placed in series with the $0.05 \mu\text{F}$ capacitor. To ensure satisfactory 516 operation for all new designs using the circuit of Figure 3 of Application Memo #71, a compensating network of 5.1 ohm resistor and a $0.1 \mu\text{F}$ capacitor, connected in series between pins 4 and 8; is recommended.

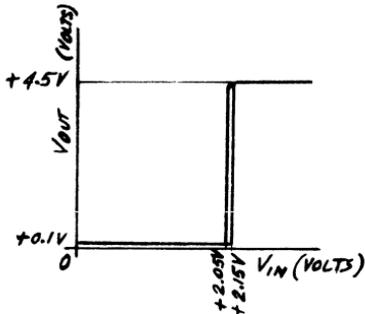
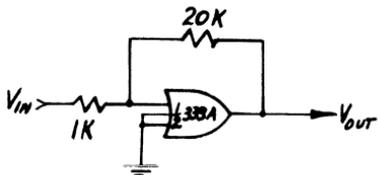
Q. Can I use the new 321 Dual J/K flip-flop in ripple counters?

A. No problem. Connect the circuits as shown below to obtain perfect binary operation in the ripple mode.



Q. Do you know of a good way to make a simple, low hysteresis, low cost and easy to implement Schmitt trigger circuit?

A. Such a circuit can be built with a Utilogic II "OR" gate and two discrete resistors as shown below. The typical response curve is for $V_{cc} = +5.0$ volt, $+25^\circ$ C temperature, unloaded output operating conditions.





APPLICATIONS MEMO

EXPANDED UTILIGIC II LINE

1. CIRCUITS DESCRIPTION

Several new circuits representing the "OR" and "NAND" logic functions have been added to the Utilogic II line to enhance its flexibility.

These new circuits consist of dual 4-input expandable, triple 3-input and quad 2-input gates in each of the "OR" and "NAND" logic functions, plus a triple 2-input expandable "OR" gate, a diode expander and a hex inverter.

All the new circuits are available in 14-pin dual-in-line silicone package in the SP (0°C to +75°C) and LU (+10°C to +55°C) operating temperature ranges conforming with the original Utilogic II product line.

The expanded Utilogic II line now consists of the following:

TABLE 1. Utilogic II Circuit Line

LOGIC FUNCTION	CIRCUIT	DESCRIPTION	PIN CONNECTIONS	NOTES
Transistor Expander	300A	Dual 3-Input Transistor Expander		
Diode Expander	301A	Quad 2-Input Diode Expander		New Circuit
AND	305A	Single 6-Input AND Gate		

LOGIC FUNCTION	CIRCUIT	DESCRIPTION	PIN CONNECTIONS	NOTES
AND	306A	Dual 3-Input AND Gate		
NOR	314A	Single 7-Input NOR Gate		
	317A	Dual 4-Input Expandable NOR Gate		Expands with Type 300A Expander
	370A	Triple 3-Input NOR Gate		
	380A	Quad 2-Input NOR Gate		
OR	333A	Dual 3-Input Expandable OR Gate		Expands with Type 300A Expander

LOGIC FUNCTION	CIRCUIT	DESCRIPTION	PIN CONNECTIONS	NOTES
OR	334A	Dual 4-Input Expandable OR Gate		New Circuits Expands with Type 300A Expander
	374A	Triple 3-Input OR Gate		New Circuit
	375A	Triple 2-Input Expandable OR Gate		New Circuit Expands with Type 300A Expander
	384A	Quad 2-Input OR Gate		New Circuit
NAND	337A	Dual 4-Input Expandable NAND Gate		New Circuit Expands with Type 301A Expander
	377A	Triple 3-Input NAND Gate		New Circuit

LOGIC FUNCTION	CIRCUIT	DESCRIPTION	PIN CONNECTIONS	NOTES
NAND	387A	Quad 2-Input NAND Gate		New Circuit
Buffer/ Driver	356A	Dual 4-Input Expandable NAND Buffer/ Driver		Expands with Type 301A Expander
J-K Binary	321A	Dual J-K Binary Common Clock and Reset		
	322B	Dual J-K Binary Separate Clock and Reset		

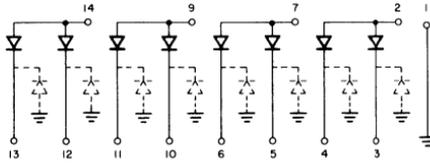


Figure 1. Schematic Diode Expander 301A

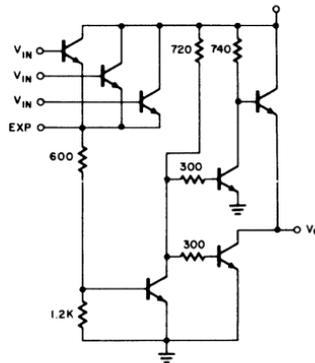


Figure 2. Schematic - Typical OR Gates 334A, 374A, 375A, 384A

NOTE: 3-Input Expandable Gate 333A shown. Number of inputs is the only difference between all gates of this group.

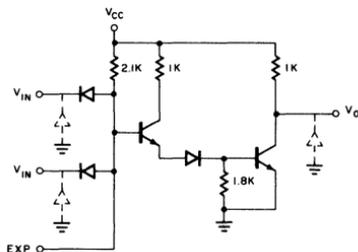


Figure 3. Schematic - Typical NAND Gates 337A, 377A, 387A

NOTE: 2-Input expandable gate shown. Number of inputs is the only difference between all gates of this group.

2. ADDED BENEFITS OF EXPANDED LINE

The inclusion of a complete choice of multicircuit packages in each logic function group of the Utilogic II line allows total utilization of all of its built-in advantages, namely:

- a. Lowest possible number of circuit packages required for any given logic design. This is achieved by a judicious intermix of NAND, NOR, and OR functions in the proper multicircuit package.
- b. Collector logic (wired-AND) capability with all NAND type gates. This further contributes to simplification of logic implementation and to reduction of circuit package count.
- c. Retention of Utilogic's traditionally high noise rejection while still enabling simple implementation of any logic problem.
- d. Full interface capability with complex functions of the DCL family (8200 series) such as shift registers, counters, decoders, etc., making Utilogic II a truly universal line of logic elements.

3. TYPICAL APPLICATIONS

The following applications represent typical logic functions implemented with Utilogic II circuits. The simplification and circuit count reduction achieved can easily be assessed by a simple comparison of the most complex functions with their NAND equivalent.

The digital comparator in Figure 4 generates the complement of an exclusive OR circuit. It is used in implementing the full adder (Figure 5) logic functions. The 3-bit parallel comparator shown on Figure 6 is a NOR/OR implementation while Figure 7 represents a typical case of Utilogic II/8200 interfacing in the design of a shift left/shift right register with parallel entry. Finally, an up-down synchronous decade counter made entirely from Utilogic II circuits is shown on Figure 8.

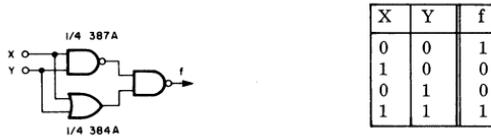
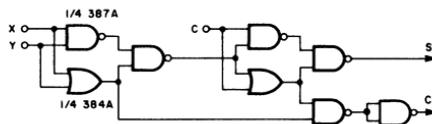


Figure 4. Digital Comparator

NOTE: This circuit can be made to generate the Exclusive-OR function by inverting the output f.

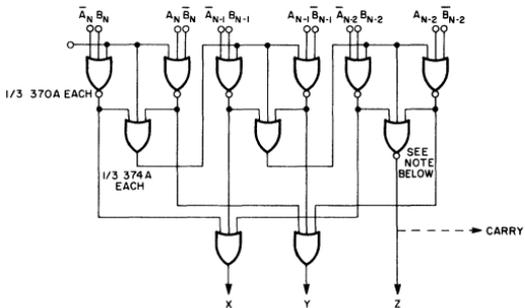


X	Y	C	S	C'
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

$$S = C(XY + \bar{X}\bar{Y}) + C(XY + \bar{X}\bar{Y})$$

$$C' = XY + C(X\bar{Y} + \bar{X}Y)$$

Figure 5. Full Adder

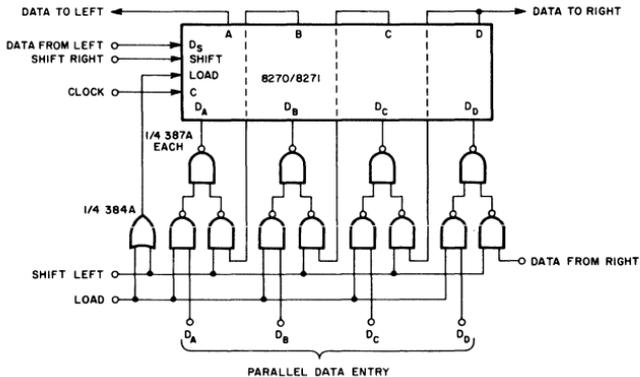


CONDITION	X	Y	Z
A > B	1	0	0
A = B	0	0	1
A < B	0	1	0

NOTE:

The NOR gate and Z line appear only at the least significant bit of the binary numbers being compared. To expand the number of kits being compared, replace the NOR gate with an OR gate to generate the carry term indicated. Move the NOR gate and Z line to the position representing the least significant kit.

Figure 6. Parallel Binary Comparator

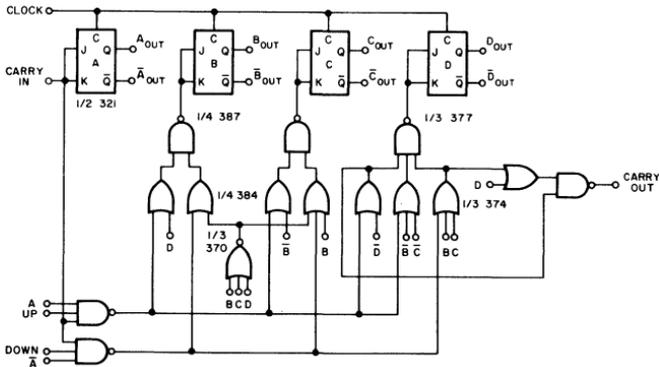


LOAD	SHIFT RIGHT	SHIFT LEFT	FUNCTION
0	0	0	Store
1	0	0	Parallel Load
0	1	0	Shift Right
0	0	1	Shift Left

PACKAGES COUNT
COMPARISON:

UTILOGIC II - $4\frac{1}{4}$ packs
DTL (600) - $4\frac{7}{12}$ packs

Figure 7. Shift Left/Shift Right Register with Parallel Data Entry



Up	Down	Function
0	0	No Count
0	1	Count Down
1	0	Count Up
1	1	Not Allowed

QUANTITY OF CKT. TYPES	CIRCUIT TYPE	TOTAL PK'GS
4	1/2 321A Flip-Flop	2
5	1/4 384A 2-Input OR	1-1/4
3	1/3 374A 3-Input OR	1
1	1/3 370A 3-Input NOR	1/3
3	1/4 387A 2-Input NAND	3/4
3	1/3 377A 3-Input NAND	<u>1</u>
	TOTAL	6-1/3

Figure 8. Up/Down Synchronous Decade Counter



APPLICATIONS MEMO

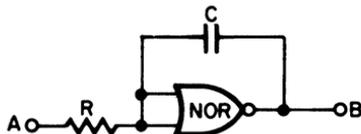
UTILOGIC NOR and OR GATE APPLICATIONS

- Integrators
- One-Shots
- Schmitt Triggers
- Linear Amplifier
- Oscillators
- Line Driver/Receiver

The NOR and OR gates in the Utilogic 300 Series* are extremely versatile devices. With an input impedance (Z_{in}) greater than 20,000 ohms and an output impedance (Z_{out}) less than 100 ohms, the circuit designer can use the Utilogic gates in a variety of applications. Shown below are a few of the unique applications.

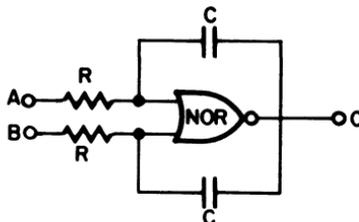
CIRCUIT 1 - The Linear Integrator

Figure 1a



$$B = - \int_0^t A dt$$

Figure 1b



$$C = - \int_0^t \frac{(A + B)}{2} dt$$

The Utilogic NOR gates make good linear integrators. A typical open loop gain of 25 dB can be expected at room temperature.

Figures 1a and 1b show two applications of the NOR gate being used in an integrating configuration. Figure 1a can be used for any system application which may require inexpensive linear integrators (i.e., there are four 2-input NOR gates in a 380 package). Both Figures 1a and 1b make excellent noise discriminators for digital systems.

* NOR's: 314, 317, 370, 380; OR's: 333, 334, 374, 375, 384.

CIRCUIT 2 - The Schmitt Trigger

Figure 2a

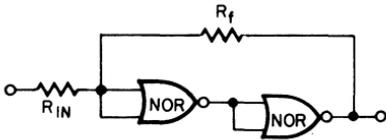
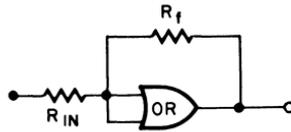


Figure 2b

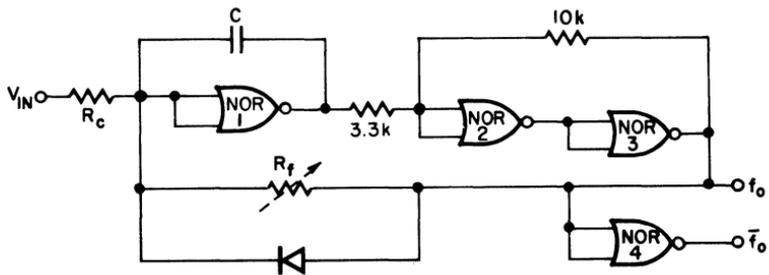


Figures 2a and 2b show Schmitt trigger implementations. The circuit in Figure 2a requires two 2-input NOR gates (two Schmitt triggers per package). Up to four Schmitt triggers per package can be realized using the 2-input OR gate implementation shown in Figure 2b. These Schmitt triggers have a variable hysteresis voltage which is approximately equal to:

$$V_{HYST.} \cong -3.7 \frac{R_{IN}}{R_f} \text{ Volts, } R_{IN} \leq 10K\Omega$$

CIRCUIT 3 - Oscillators

Figure 3a - Voltage Controlled Oscillator



Combining the linear integrator from Figure 1a and the Schmitt trigger from Figure 2a, produces the Voltage Controlled Oscillator shown in Figure 3a. There are three modes of operation:

- Mode 1. V_{IN} open or $R_c = \infty$, $f_0 \cong \frac{1}{1.2RC}$, $R \leq 10K\Omega$
C must be non-polarized.
- Mode 2. V_{IN} connected to a voltage supply and $R_c \leq 10K$. As V_{IN} decreases from the threshold region of Gate No.1 towards a negative voltage, f_0 increases; a 12:1 range of f_0 can be achieved.
- Mode 3. V_{IN} open or $R_c = \infty$, f_0 may be varied over a 1000:1 range by varying R_f . A variable resistor or a voltage controlled resistor (MOS FET) may be used in this application.

The oscillator operates best for a $V_{IN} < 0V$. The diode across R_f produces a positive-going pulse at f_0 . This VCO can be made with one 380 NOR package. It is self-starting and has an $f_0 \text{ MAX} \cong 5 \text{ MHz}$.

Figure 3b - Voltage Controlled Oscillator

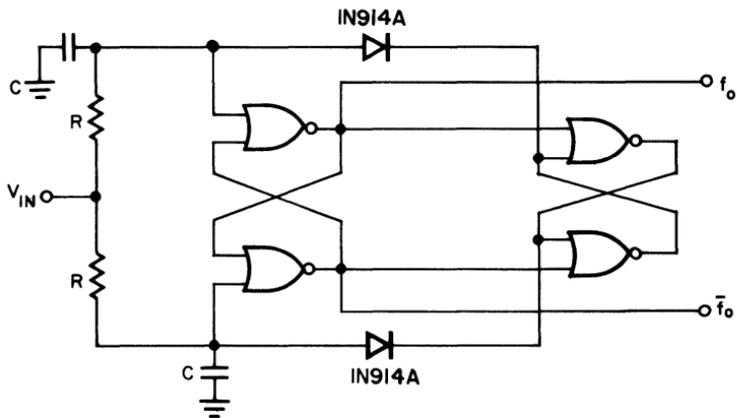


Figure 3b shows a self-starting VCO using a single Utilogic Quad 2-Input NOR package.

Performance data:

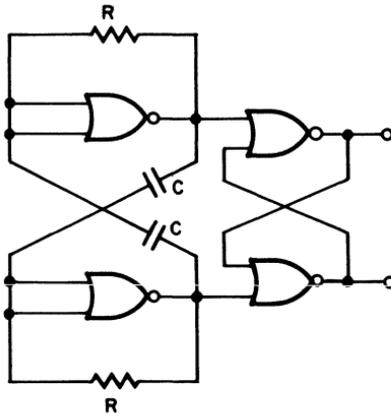
$$f_0 \cong \frac{1}{\tau}, \quad \tau = RC \text{ at } V_{IN} = V_{CC} = 5V \pm 5\%$$

$$\text{If: } V_{IN} = +2.5V \text{ to } +25V; R \leq 10K\Omega$$

Then: $f_0' = 1 f_0$ to $100 f_0$ or 100:1 range (f_0' = VCO frequency)

$$f_{0 \text{ MAX}} \cong 5\text{MHz}$$

Figure 3c - Self-Starting Multivibrator



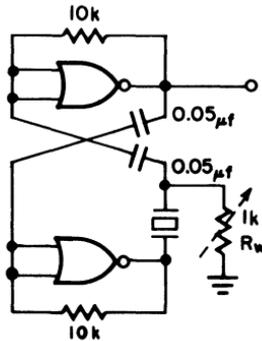
Performance data:

$$f_0 \cong \frac{1}{2\tau}, \quad \tau = RC, \quad R \leq 10K\Omega$$

$$f_{0 \text{ MAX}} \cong 5\text{MHz}$$

C must be non-polarized

Figure 3d - Crystal Controlled Oscillator

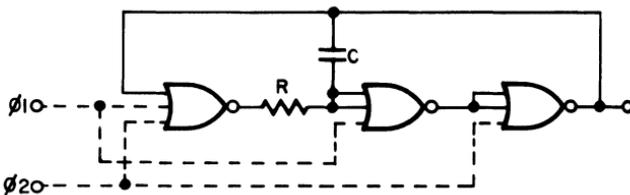


Performance data:

Crystal $f_0 = 100 \text{ kHz to } 2 \text{ MHz}$

R_W controls the amount of positive feedback permitting both sinusoidal and square-wave operation.

Figure 3e - RC Oscillator - with Synchronizing Inputs



Performance data:

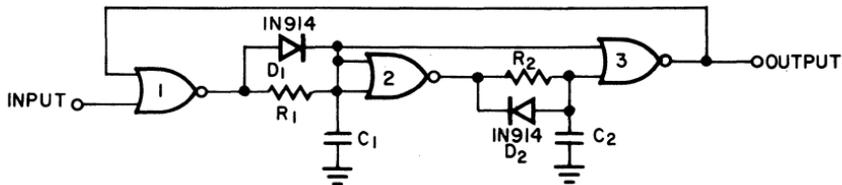
$$f_0 \cong \frac{1}{2\tau}; \quad \tau = RC$$

$$f_0 \text{ MAX} \cong 5 \text{ MHz}$$

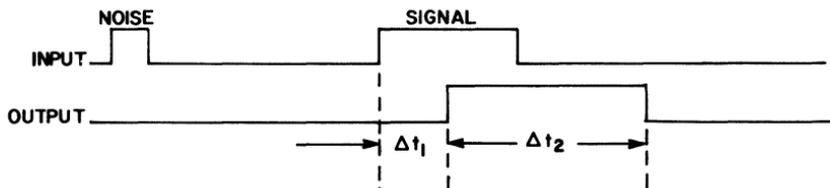
$\phi 1$ and $\phi 2$ must be 180° out-of-phase at a frequency greater than f_0 and have a pulse width of less than $1\mu\text{sec}$.

CIRCUIT 4 - One-Shots

Figure 4a - Noise-Discriminator One-Shot



Output vs. Input Information



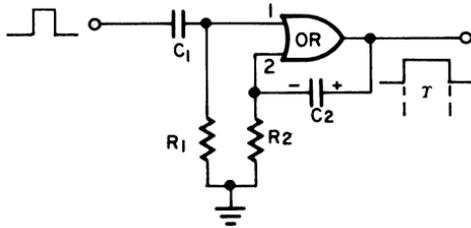
This one-shot circuit discriminates between noise lasting less than the time Δt_1 and an input signal having a duration greater than Δt_1 . An input of Δt_1 or longer produces an output pulse duration of Δt_2 . The output of Gate 3 is fed back into the input of Gate 1 which guarantees an output pulse of Δt_2 in duration if the input goes to a logic "0" during the output signal.

$$\Delta t_1 \cong 1.1 R_1 C_1$$

$$\Delta t_2 \cong 1.1 R_2 C_2$$

The diodes (D_1 and D_2) minimize the recovery time.

Figure 4b - OR Gate One-Shot



Performance data:

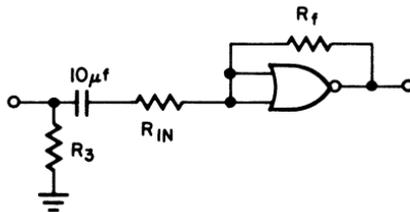
$$\tau \cong R_2 C_2, R_1 C_1 < R_2 C_2$$

The input pulse is differentiated by the $R_1 C_1$ network at input 1 which causes the output to rise nearly 4 volts. Input 2 also rises 4 volts locking the output in a "1" logic state until the voltage at input 2 discharges through $R_2 C_2$ down to the threshold region where positive feedback restores the output to a "0" state. The 384 Quad 2-Input OR Gate permits the fabrication of four one-shots using only one package. If C_1 and R_1 are deleted and the input signal is fed directly into input 1, the output pulse will have two modes:

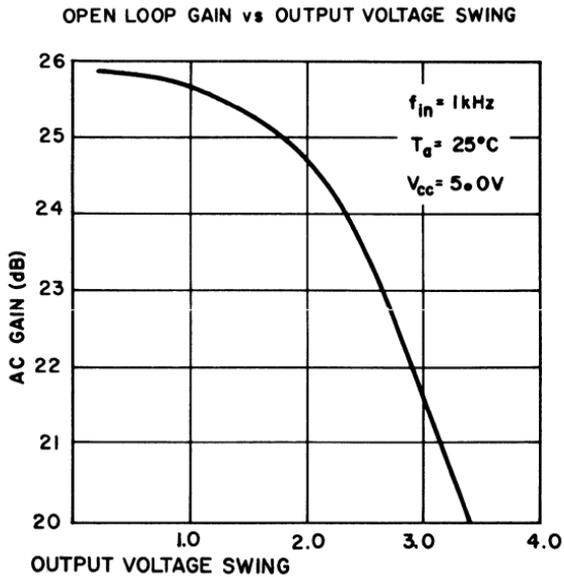
- Mode 1. If: input pulse $< \tau$
Then: output pulse = τ
- Mode 2. If: input pulse $> \tau$
Then: output pulse = input pulse

The circuit can be used to overcome contact bounce problems associated with mechanical to electronic interfaces and signal conditioning for short pulse inputs. The same circuit can also be built with two NOR gates.

CIRCUIT 5 - Linear Amplifier

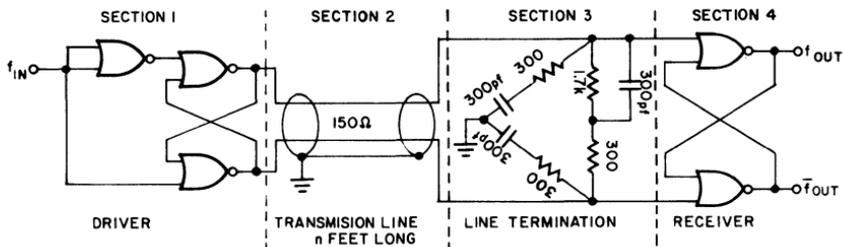


The gain of the amplifier is $G \cong \frac{A_0 R_f}{(A_0 + 1) R_{IN} + R_f}$. The open-loop gain is shown below as a function of output voltage swing:



The open-loop-3dB cut-off frequency is approximately 5 MHz

CIRCUIT 6 - Transmission Line Driver and Receiver



There are four basic sections of this system:

- Section 1 The Driver is a D-type latch producing complemented outputs using 380 NOR Gates.
- Section 2 A shielded twisted - pair n-feet in length.
- Section 3 The 150 ohm Line Termination - Delta configuration. The 1.7K resistor in parallel with 300pF and in series with 300 ohms between the inputs of the receiver provide an AC line termination as well as a DC load (2K ohms).
- Section 4 The receiver is a 380 NOR Gate Latch.

This technique has been used to transmit and receive data up to 1500 feet on multiple conductor telephone cable.

SECTION 3
DECODING AND STEERING



APPLICATIONS MEMO

J. Eccher

BINARY TO BCD CONVERTER

Conversion from binary to BCD is required whenever it is necessary to display binary numbers in decimal or to interface with equipment requiring binary coded decimal (BCD) information. A simple binary to BCD conversion technique is described in Reference 1. The method employed in this article requires only one operation per bit as suggested in the summary of Reference 1. Integrated circuits are ideally suited for implementing the converter to yield low parts count and high speed operation.

The converter system consists of three basic subsystems as shown in Figure 1. A parallel input serial output register, a clock pulse generator, and the binary to BCD conversion logic.

The parallel to serial register, Figure 2, consists primarily of dual D binaries connected as a shift register and gates to allow parallel entry. Also included is the option to convert Gray coded numbers to BCD. The Gray coded number is converted to binary in a serial operation as the data is being shifted to BCD conversion logic.

The clock pulse generator, Figure 3, applies the correct number of clock pulses to the shift register and conversion logic on command of a convert signal. The number of pulses generated depends upon the length of the binary number, e.g., in the converter described in this article 12 pulses are required to convert a 12 bit binary number.

The converter logic, Figure 4 (one decade shown), implements the rules described on page 315 of Reference 1. The rules are tabulated in Table 1 for any decade, S_5 is the least significant bit of the next higher decade, S_0 is the output of the parallel to serial register or the output of the next lower order decade converter logic.

TABLE I

S_4	S_3	S_2	S_1	S_5	S_4	S_3	S_2	S_1
0	0	0	0	0	0	0	0	S_0
0	0	0	1	0	0	0	1	S_0
0	0	1	0	0	0	1	0	S_0
0	0	1	1	0	0	1	1	S_0
0	1	0	0	0	1	0	0	S_0
0	1	0	1	1	0	0	0	S_0
0	1	1	0	1	0	0	1	S_0
0	1	1	1	1	0	1	0	S_0
1	0	0	0	1	0	1	1	S_0
1	0	0	1	1	1	0	0	S_0

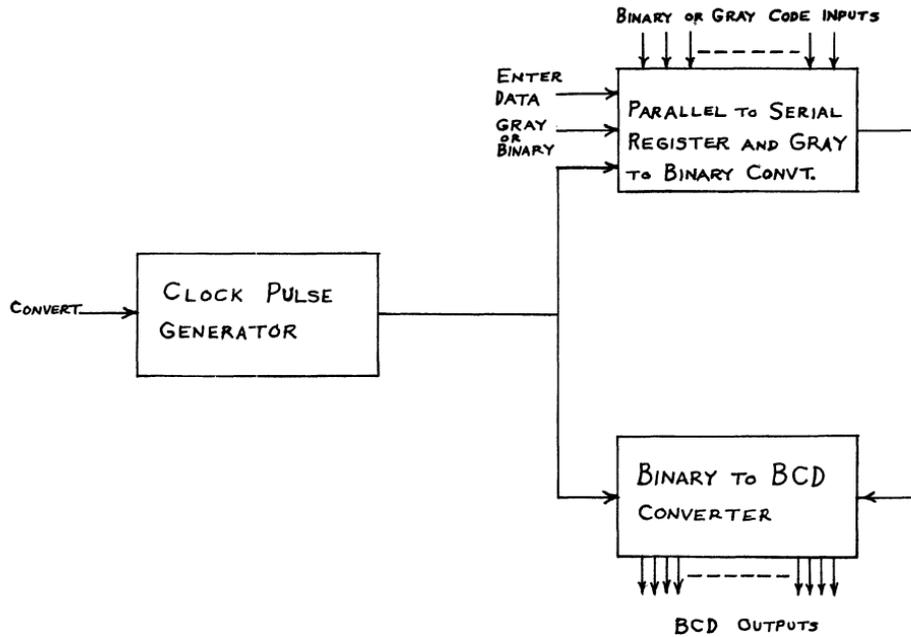


Figure 1. Converter System

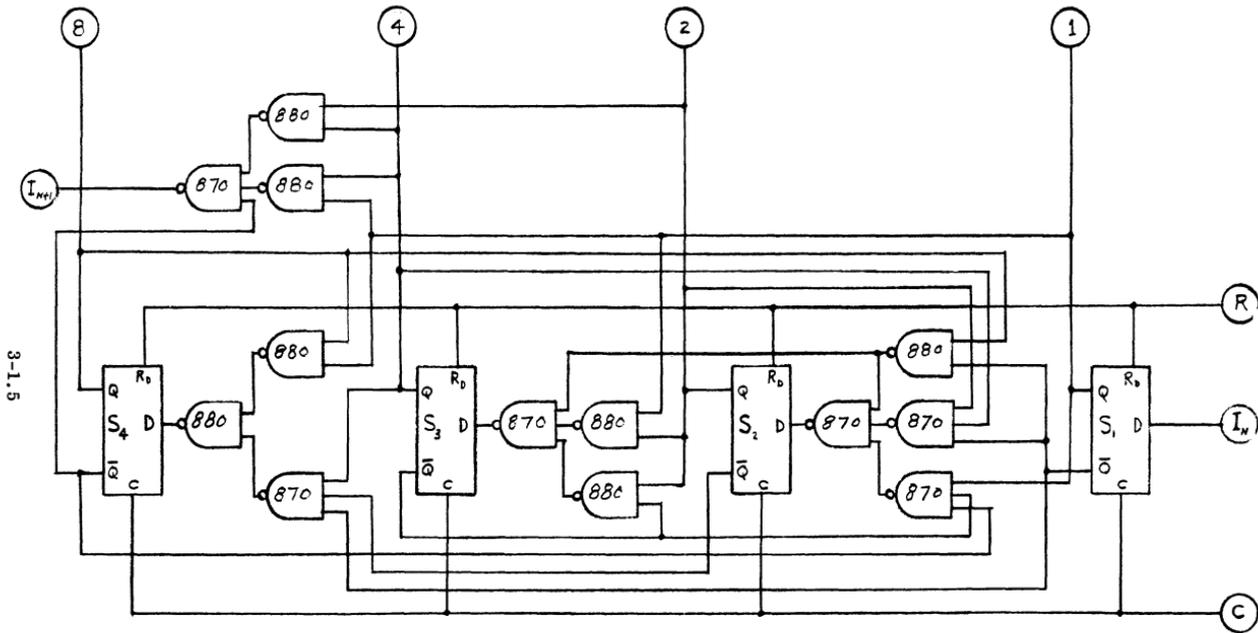


Figure 4. Binary to BCD Converter

At time N, the content of the decade (S_4, S_3, S_2, S_1) is tested. If the number is 4 or less it is simply shifted one bit to the left; if the number is 5 or greater a 3 is added to the number and the result is shifted one bit to the left. The contents of the decade plus the contents of the least significant bit of the next higher decade (S_5) is also shown in Table 1 at time N + 1. Design of the conversion logic is carried out using the techniques described in Reference 2.

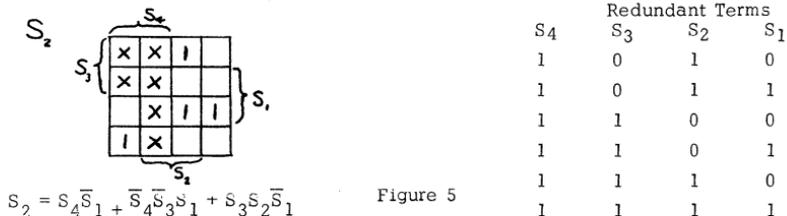


Figure 5

The design technique requires plotting all 1's that occur in a column (S_5, S_4, S_3, S_2) at time N + 1 on a veitch diagram. The veitch diagram for S_2 is shown in Figure 5; also included are the redundant terms (the states that do not occur) which are plotted as x's.

The resultant equation for the input logic to the S_2 binary is obtained by combining the 1's and the x's of the veitch diagram to obtain the simplest equation using rules given in Reference 2. The input equations for $S_3, S_4,$ and S_5 are obtained using the same techniques and the results are shown in Figure 6.

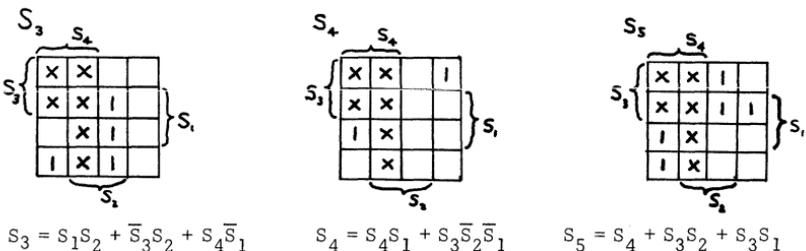


Figure 6

Conversion of a parallel binary number is carried out in the following sequence. The binary number is entered into the shift register on command of an enter signal. The entry signal activates the one shot multivibrator formed by gates 1, 2, 3 and 4 which enables the parallel entry gates. Gate 5 provides a clear signal preceding the one shot multivibrator pulse.

A convert signal enables the clock pulse generator to provide the correct number of pulses to the shift register and conversion logic. The latch consisting of gates 6 and 7 provides a reset pulse to the converter binaries; the gray to binary converter binary, and the counter associated with the clock pulse generator as well as setting the 629 binary to a ONE. The 629 binary enables the oscillator consisting of gates 8, 9, and 10 to free run. The output of the oscillator provides clock pulses until the Modulus 12 counter overflows which resets the 629 binary and stops the oscillator.

Data is shifted from the parallel entry register into the conversion storage register by the clock pulse generator. At each clock time the contents of the conversion register is controlled by the logic to meet the requirements of Table 1. At the end of the clock pulse train the BCD equivalent of the binary number is stored in the conversion register.

A gray coded number may be converted by setting switch S to the ground position which enables the serial gray to binary converter. The gray coded number is serially converted to binary and then applied to the binary to BCD converter.

The speed of conversion is determined by the frequency of the clock pulse oscillator and the length of the binary word. One clock time is required per binary bit, e.g., a 12 bit binary word will require 12 clock pulses. The maximum clock frequency is determined by the operating speed of the logic elements.

Integrated circuit implementation of this binary to BCD converter yields a low parts count, i.e., each decade requires only 6 packages, 2 quad gate packages, 2 triple gate packages, and 2 dual binary packages. The parallel to serial register is not required when the data is available in a serial form with the most significant bit appearing first. The clock pulse generator may be provided from another source such as digital computer eliminating the need for a separate pulse generator.

REFERENCES

- [1] John F. Couleur, "BIDEC - A Binary-to-Decimal or Decimal-to-Binary Converter." IRE Transactions on Electronic Computers, pp. 313-316, December 1958.
- [2] Montgomery Phister, Jr., Logical Design of Digital Computers. New York: Wiley 1958



APPLICATIONS MEMO

S/N 8250/8251 OCTAL/DECADE DECODERS

1. GENERAL DESCRIPTION

The Decade Decoder, S/N 8251, accepts a four bit input code and activates one of the ten mutually exclusive outputs.

The Octal Decoder, S/N 8250, decodes an octal number (3 bit), applied to the input pins and one of the eight outputs will be activated, representing the decoded number. The 8250/8251 are available in different configurations:

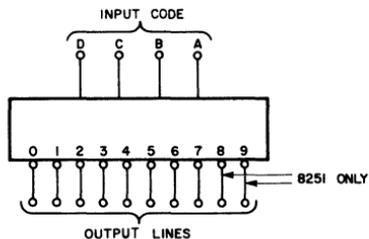
Octal Decoder

- a) S8250J - 14 pin flat pack, -55° C to +125° C
- b) N8250J - 14 pin flat pack, 0° C to +75° C.
- c) S8250A - 14 pin Dual-in-line, -55° C to + 125° C
- d) N8250A - 14 pin Dual-in-line, 0° C to +75° C

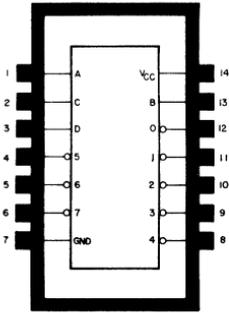
Decade Decoder

- a) S8251B - 16 pin Dual-in-line, -55° C to + 125° C
- b) N8251B - 16 pin Dual-in-line, 0° C to +75° C

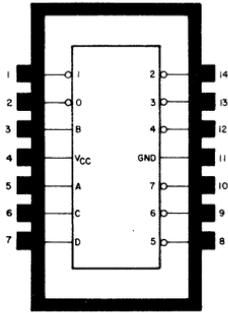
The Octal/Decade Decoders are very flexible devices for decoding and logic conversion applications.



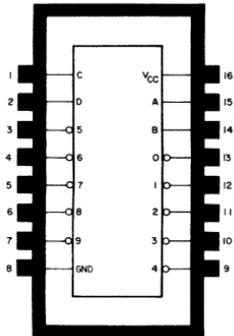
PIN CONFIGURATIONS



58250A
N8250A

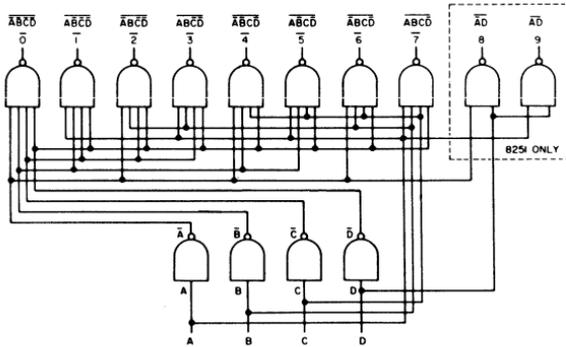


58250J
N8250J



58251B
N8251B

LOGIC DIAGRAM



2. SOME DECODER APPLICATIONS

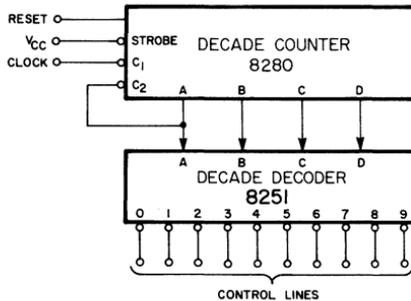
2.1 Decade Decoder (8251)

Let us assume that 10 different, sequential operations must be controlled. In this case, 10 control lines must be available and one of the 10 lines is activated for each state. Assuming the ten different states are characterized by its binary number, the following truth table results:

STATE	INPUTS D C B A	OUTPUTS									
		$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$	$\bar{8}$	$\bar{9}$
0	0 0 0 0	0	1	1	1	1	1	1	1	1	1
1	0 0 0 1	1	0	1	1	1	1	1	1	1	1
2	0 0 1 0	1	1	0	1	1	1	1	1	1	1
3	0 0 1 1	1	1	1	0	1	1	1	1	1	1
4	0 1 0 0	1	1	1	1	0	1	1	1	1	1
5	0 1 0 1	1	1	1	1	1	0	1	1	1	1
6	0 1 1 0	1	1	1	1	1	1	0	1	1	1
7	0 1 1 1	1	1	1	1	1	1	1	0	1	1
8	1 0 0 0	1	1	1	1	1	1	1	1	0	1
9	1 0 0 1	1	1	1	1	1	1	1	1	1	0

The 8251 Decade Decoder provides this function. As can be seen from the truth table, all non-activated outputs are high and the output number corresponding to the binary input number is low.

The Decade Decoder may be used conveniently in conjunction with the Decade Counter (8280). The change of the different states is controlled by the clock-signal.

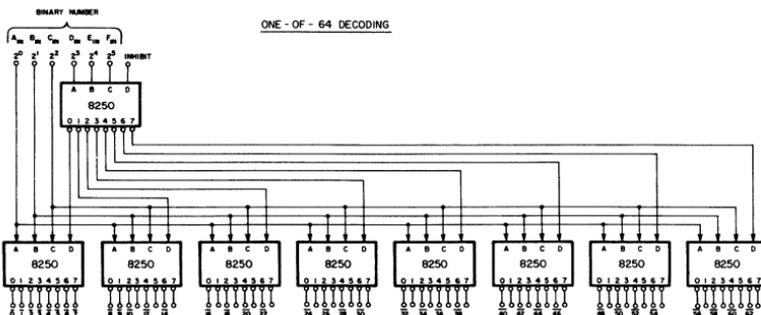


2.2 Octal Decoder (8250)

The Octal Decoder decodes the binary numbers 0 to 7 which are applied to the pins (CBA). The D-input provides gating of the input. When D is high, decoding is inhibited - when D is low, decoding occurs. The truth table of an Octal Decoder is given below.

STATE	D INPUT	INPUT C B A	OUTPUTS							
			0	1	2	3	4	5	6	7
0	0	0 0 0	0	1	1	1	1	1	1	1
1	0	0 0 1	1	0	1	1	1	1	1	1
2	0	0 1 0	1	1	0	1	1	1	1	1
3	0	0 1 1	1	1	1	0	1	1	1	1
4	0	1 0 0	1	1	1	1	0	1	1	1
5	0	1 0 1	1	1	1	1	1	0	1	1
6	0	1 1 0	1	1	1	1	1	1	0	1
7	0	1 1 1	1	1	1	1	1	1	1	0
8	1	0 0 0	1	1	1	1	1	1	1	1
9	1	0 0 1	1	1	1	1	1	1	1	1
10	1	0 1 0	1	1	1	1	1	1	1	1
11	1	0 1 1	1	1	1	1	1	1	1	1
12	1	1 0 0	1	1	1	1	1	1	1	1
13	1	1 0 1	1	1	1	1	1	1	1	1
14	1	1 1 0	1	1	1	1	1	1	1	1
15	1	1 1 1	1	1	1	1	1	1	1	1

The Octal Decoder can be extended to 64 control lines. The next example shows a "One-of-64 Decoding".



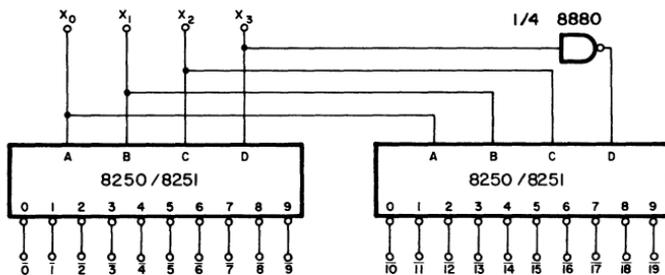
Load Chart for One-of-N Decoding

N	A _{in}	B _{in}	C _{in}	D _{in}	E _{in}	F _{in}
16	5.25	5.25	5.25	4	-	-
24	6.50	6.50	6.50	4	4	-
32	7.75	7.75	7.75	4	4	-
40	9.00	9.00	9.00	4	4	4
48	10.25	10.25	10.25	4	4	4
56	11.50	11.50	11.50	4	4	4
64	12.75	12.75	12.75	4	4	4

Note that the decoder device with inputs D_{in}, E_{in}, F_{in} controls the other eight octal decoders by the D-inputs. The decoding process may be stopped by the Inhibit line.

2.3 Arbitrary 4-Bit Decoding

Using two Decoders every 4-bit code may be decoded.



As an example we apply the excess-3 code to the pins (X_3, X_2, X_1, X_0) and examine the generated outputs.

Decimal Quantity	Excess -3 Code $X_3 X_2 X_1 X_0$	Activated Outputs (Not true levels)	Useful Outputs (Not true levels)
0	0 0 1 1	3 19	3 -
1	0 1 0 0	4 18	4 -
2	0 1 0 1	5 19	5 -
3	0 1 1 0	6 18	6 -
4	0 1 1 1	7 19	7 -
5	1 0 0 0	8 10	- 10
6	1 0 0 1	9 11	- 11
7	1 0 1 0	8 12	- 12
8	1 0 1 1	9 13	- 13
9	1 1 0 0	8 14	- 14

The well-defined outputs are listed at the right most column.

In the next table other codes will be shown with their corresponding outputs.

Decimal Quantity	Well-Defined Outputs (Not true levels)		
	Binary Coded Decimal	Aiken Code 2*4 2 1	4 2* 2 1
0	0	0	0
1	1	1	1
2	2	2	2
3	3	3	5
4	4	4	6
5	5	13	11
6	6	14	12
7	7	15	15
8	8 10	16	16
9	9 11	17	17

2.4 Code Conversion

The Decade Decoders are also useful in code conversion applications. As an example let us convert the Gray Code into the BCD Code. First we apply the Gray Code to the pins of two Decade Decoders. The activated outputs are listed in the following table.

Decimal Quantity	Gray Reflected Code $X_3 X_2 X_1 X_0$	Decoder Outputs	Binary Coded Decimal				
			Z_5	Z_4	Z_3	Z_2	Z_1
0	0 0 0 0	$\overline{0}$	0 0 0 0	0 0 0 0	0		
1	0 0 0 1	$\overline{1}$	0 0 0 0	0 0 0 1	1		
2	0 0 1 1	$\overline{3}$	0 0 0 0	0 0 1 0	0		
3	0 0 1 0	$\overline{2}$	0 0 0 0	0 0 1 1	1		
4	0 1 1 0	$\overline{6}$	0 0 0 0	0 1 0 0	0		
5	0 1 1 1	$\overline{7}$	0 0 0 0	0 1 0 1	1		
6	0 1 0 1	$\overline{5}$	0 0 0 0	0 1 1 0	0		
7	0 1 0 0	$\overline{4}$	0 0 0 0	0 1 1 1	1		
8	1 1 0 0	$\overline{14}$	0 0 0 0	1 0 0 0	0		
9	1 1 0 1	$\overline{15}$	0 0 0 0	1 0 0 1	1		
10	1 1 1 1	$\overline{17}$	0 0 0 1	0 0 0 0	0		
11	1 1 1 0	$\overline{16}$	0 0 0 1	0 0 0 1	1		
12	1 0 1 0	$\overline{12}$	0 0 0 1	0 0 1 0	0		
13	1 0 1 1	$\overline{13}$	0 0 0 1	0 0 1 1	1		
14	1 0 0 1	$\overline{11}$	0 0 0 1	0 1 0 0	0		
15	1 0 0 0	$\overline{10}$	0 0 0 1	0 1 0 1	1		

Now the Decoder outputs will be used to form the BCD Code.

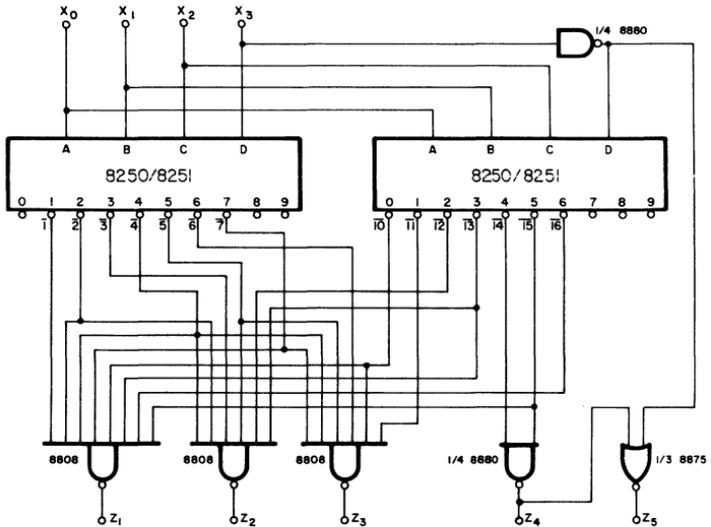
$$Z_4 = 14 + 15$$

$$Z_3 = 6 + 7 + 5 + 4 + 11 + 10$$

$$Z_2 = 3 + 2 + 5 + 4 + 12 + 13$$

$$Z_1 = 1 + 2 + 7 + 4 + 15 + 16 + 13 + 10$$

$$Z_5 = \overline{X_3} + Z_4$$



This configuration provides significant package count savings as shown in the table below.

Package Count with Decoders		Package Count with Standard Gates	
8250	2	8816	4
8808	3	8808	1
8880	1/2	8880	2 3/4
8885	1/4	8870	2/3
		8875	1/3
<hr/>		<hr/>	
Total	5 3/4	Total	8 3/4

- 8250 Octal Decoder
- 8808 Single 8 input NAND
- 8816 Dual 4 input NAND
- 8870 Triple 3 input NAND
- 8875 Triple 3 input NOR
- 8880 Quad 2 input NAND
- 8885 Quad 2 input NOR



APPLICATIONS MEMO

8-INPUT DIGITAL MULTIPLEXERS 8230, 8231, 8232

INTRODUCTION

The 8230, 8231 and 8232 are 8-bit digital multiplexers having internal select decoding and an output inhibit control line. These devices are designed using standard T^2L input and output structures (the 8231 is an open collector version): thus, they are compatible with DTL as well as T^2L . The 8230 is pin for pin interchangeable with the 9312. The 8231 has the same pins and logic configuration as the 8230, but with open collector output transistors.

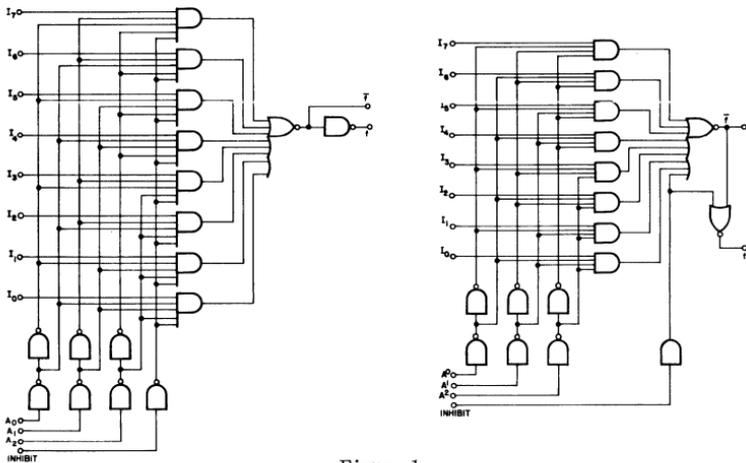


Figure 1

DESCRIPTIONS

The 8230 is available in 16-pin flat and dual in-line packages in both 0°C to $+75^{\circ}\text{C}$ and -55°C to $+125^{\circ}\text{C}$ temperature ranges. Eight multiplex input pins, three select decoding inputs, an output inhibit, f and \bar{f} outputs and V_{CC} and ground are provided.

The output inhibit control performs the function described in the truth table in Figure 1. As can be seen, the difference between the 8230/31 and 8232 is that the 8230/31 "inhibit" forces $f = "0"$ and $\bar{f} = "1"$, while on the 8232, "inhibit" forces f and $\bar{f} = "0"$.

The device accepts eight different inputs and gates one-of-eight to the output, depending on the three binary bits that form the input code.

Some applications for the 8-bit multiplexer are as follows:

- A. Methods for expansion
- B. Constructing a bipolar scratch pad memory from 8221 (32-bit memory, 8 words x 64 bits) (see Figure 5)
- C. Variable frequency counter (see Figure 6)
- D. Implementation of any four variable Boolean functions (see Figures 7 and 8)

EXPANSION OF THE 8230, 8231, 8232

Sixteen-line to one-line multiplexers are shown in Figures 2A and 2B (data inputs to the multiplexers are not shown). The basic idea is to simultaneously address the same input code line in both multiplexers and enable the output of only one. The 2^3 and $\overline{2^3}$ inputs act as the $\overline{\text{enable}}$ /inhibit control so that only one of the multiplexers is allowed to transmit information at a time. Remember, if the inhibit input is a "1", then the "f" output of the 8230/31/32 is forced to a "0". Therefore, in Figure 2A, one input to the 8885 (NOR gate) is always a logic "0", allowing the other multiplexer to be selected. An advantage of the 8231 (open collector) is that the outputs may be tied common and only an external pull-up resistor is necessary. (The " \overline{f} " outputs are used, as illustrated in Figure 2B, since the $\overline{\text{enable}}$ /inhibit line forces \overline{f} to logic "1".

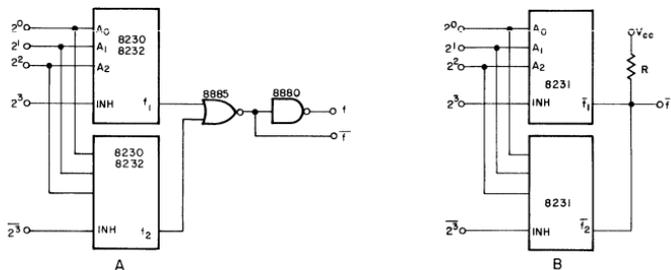


Figure 2

Figures 3 and 4 show further expansion using the same technique as in the example of Figure 2. The same address coding techniques may be used to expand the number of data inputs of the 8231. The \bar{f} outputs are tied in common and an external pull-up resistor replaces the NOR and NAND output gating.

Figure 5 is an example of a scratch pad memory of 64 words, each 16 bits in length. The memory is implemented using the 8221 (scratch pad 8 words, 4 bits/word) and the 8230. Only the addressing and Readout functions are shown, for clarity.

The addressing technique is to allow four 8221's to be addressed simultaneously and have the information transmitted to the Bit Lines numbered 1 through 16.

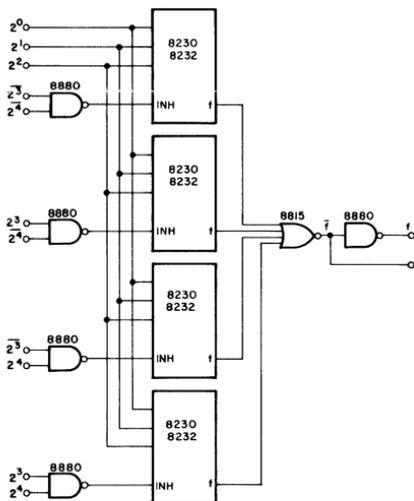


Figure 3

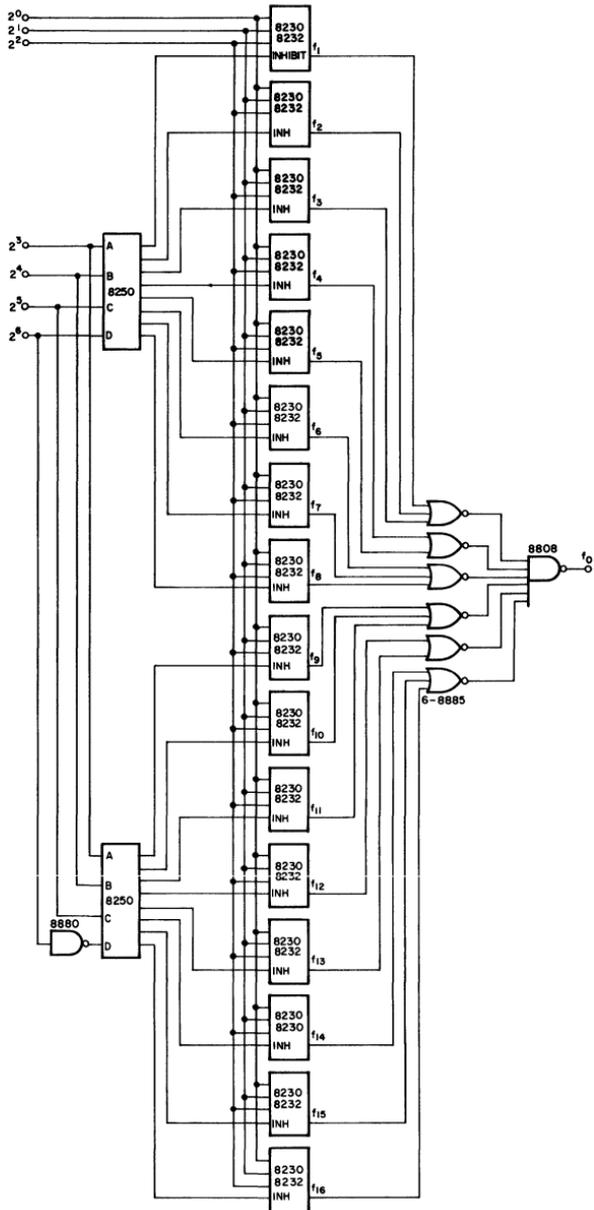


Figure 4

Address selection is performed as follows:

1. Address all 8221's simultaneously, thereby attempting to read 4 bits from each memory.
2. Address all 8230's simultaneously, thereby selecting the same input in all 16 multiplexers.
3. Referring to Figure 5B, the result is that 4 bits are read out from each of 4 individual memories, thus generating a 16-bit word.

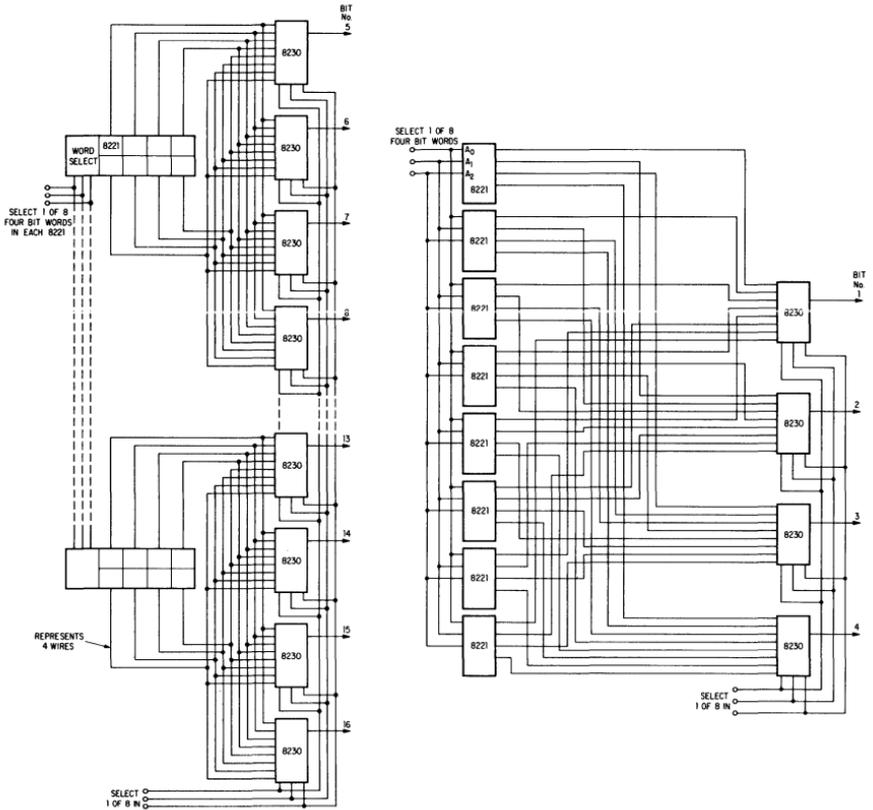
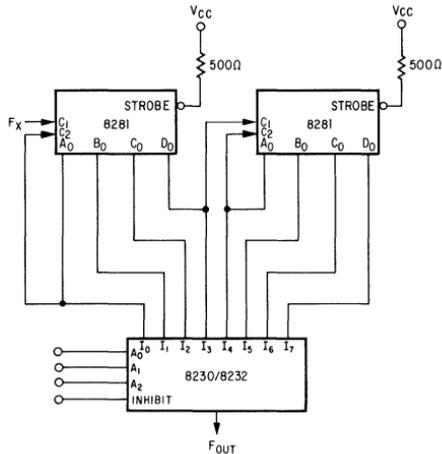


Figure 5

Figure 6 represents a simple frequency selector. Two 8281's (divide-by-16 binary counters) are connected in series. All 8 outputs are fed to the multiplexer. By selective addressing, as shown in Table 1, the various quantized frequencies are selected.



INHIBIT	A ₂	A ₁	A ₀	F _{OUT}
0	0	0	0	F _X /2
0	0	0	1	F _X /4
0	0	1	0	F _X /8
0	0	1	1	F _X /16
0	1	0	0	F _X /32
0	1	0	1	F _X /64
0	1	1	0	F _X /128
0	1	1	1	F _X /256
1	X	X	X	0

Figure 6

BOOLEAN FUNCTION GENERATOR

The 8230/32 may be used as a Boolean function generator that will produce any four variable Boolean functions.

Figure 7 illustrates how to implement the function generator using an 8271 4-bit shift register, and the 8230 or 8232.

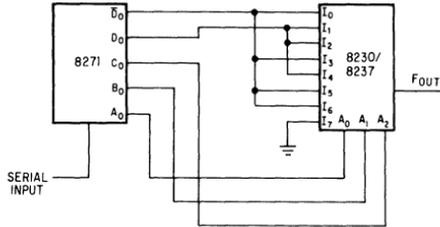


Figure 7

Example: the function that was chosen is:

$$f_{\text{out}} = \overline{A}\overline{B}\overline{C}D + A\overline{B}\overline{C}D + \overline{A}B\overline{C}D + \overline{A}B\overline{C}\overline{D} + A\overline{B}C\overline{D} + A\overline{B}C\overline{D} + \overline{A}B\overline{C}\overline{D} \quad (\text{Eq. 1})$$

This function was arbitrarily chosen and is non-reducible. To implement Eq. 1, Karnaugh maps are used to tell what logic states should be provided to the data inputs and input code lines.

Three of the variables are always applied to the code select pins (A_0 , A_1 , A_2). The fourth variable is connected to the appropriate data inputs (I_0 through I_7), depending on the Karnaugh maps.

Karnaugh Map No. 1 (Figure 8) is the 4-variable Boolean function that is implemented. Karnaugh Map No. 2 (Figure 8) describes the logic requirements at the data inputs.

Procedure

From Maps 1 and 2, the I_0 through I_7 connections can be determined. The content of the 2 squares (in Karnaugh Map No. 1) associated with an input on Karnaugh Map No. 2 determines which connection is made to that data input.

1. If both squares (Map No. 1) contain "0", ground the input.
2. If both squares (Map No. 1) contain "1"'s , connect the input to V_{cc} .
3. If the squares contain "1" and "0" (Map No. 1), and the "1" occurs in the square associated with the True form of the 4th variable, then connect the True output to the input specified by Map No. 2.
4. If the squares contain "1" and "0" (Map No. 1), and the "1" occurs in the square associated with the Complement form of the 4th variable, connect the Complement to the input specified by Map No. 2.

MAP 1

AB CD	00	01	11	10
00	1	0	1	0
01	0	1	0	1
11	1	0	0	0
10	0	1	0	1

MAP 2

AB CD	00	01	11	10
00	I_0	I_2	I_6	I_4
01				
11	I_1	I_3	I_7	I_5
10				

AB CD	00	01	11	10
00	1			
01	0			
11				
10				

$I_0 = \bar{D}$
MAP 1-A

AB CD	00	01	11	10
00				0
01				1
11				
10				

$I_4 = D$
MAP 1-E

AB CD	00	01	11	10
00				
01				
11	1			
10	0			

$I_1 = D$
MAP 1-B

AB CD	00	01	11	10
00				
01				
11				0
10				1

$I_5 = \bar{D}$
MAP 1-F

AB CD	00	01	11	10
00		0		
01		1		
11				
10				

$I_2 = \bar{D}$
MAP 1-C

AB CD	00	01	11	10
00			1	
01			0	
11				
10				

$I_6 = \bar{D}$
MAP 1-G

AB CD	00	01	11	10
00				
01				
11		0		
10		1		

$I_3 = \bar{D}$
MAP 1-D

AB CD	00	01	11	10
00				
01				
11			0	
10			0	

$I_7 = 0$ (GROUND)
MAP 1-H

Figure 8



APPLICATIONS MEMO

MSI GATING ARRAYS

- 8241** Quad Exclusive-OR Element
- 8242** 4-Bit Digital Comparator
- 8266/67** 2-Input, 4-Bit Digital Multiplexer

INTRODUCTION

Signetics DCL (8000 series) offers four MSI gating circuits which enable the system designer to implement the following common subsystem functions:

- COMPARATORS
- PARITY GENERATORS
- PARITY CHECKS
- COMPLEMENTORS
- ADDER-SUBTRACTORS
- MULTIPLEXERS

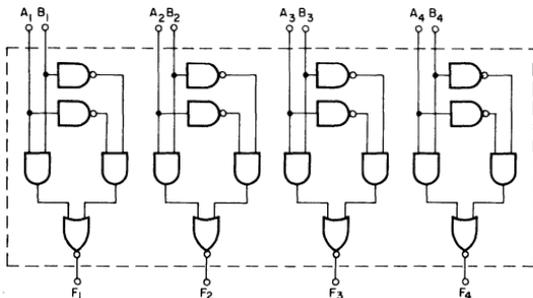
All four MSI circuits are designed with classic TTL techniques and represent an equivalent complexity of approximately 20 single gates.

DEVICE DESCRIPTION: 8241

The 8241 is a quad EXCLUSIVE-OR gate used in a variety of digital comparator and adder systems. The logic diagram is shown in Figure 1 along with its logic symbol and truth table.

Figure 1, 8241 Quad Exclusive-OR.

LOGIC DIAGRAM



TRUTH TABLE

A	B	f
0	0	0
0	1	1
1	0	1
1	1	0

Both Military (-55°C to +125°C) and Industrial (0°C to +75°C) temperature range devices are available in 14 pin dual-in-line and flat package configurations.

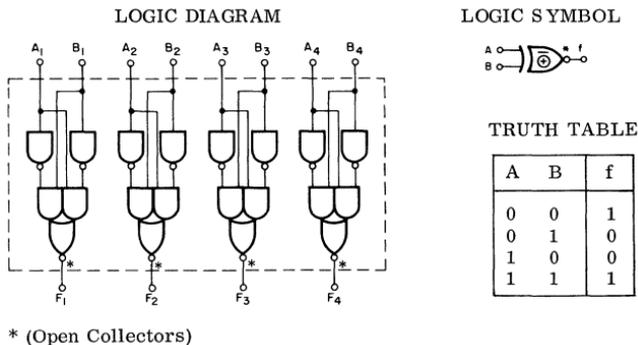
Conservative design practices require that the user decouple the 8241 by placing a .01µf capacitor between the V_{CC} and ground terminals of the device. Decoupling capacitors should be non-inductive.

DEVICE DESCRIPTION: 8242

The 8242 is a quad EQUALITY COMPARATOR or COINCIDENCE gate. Input bits A_nB_n are compared for equality. If A_n = B_n, the corresponding output F_n will be a logical "1". If A_n ≠ B_n, output F_n will be a logical "0".

The logic diagram, symbol and truth table for the 8242 are shown in Figure 2.

Figure 2. 8242 Quad Equality Gate



Both Military (-55°C to +125°C) and Industrial (0°C to +75°C) temperature range devices are available in 14 pin dual-in-line and flat package configurations.

Although TTL circuit design techniques are used in the 8242, the outputs feature open collector switching transistors. This feature allows the designer to select a variety of comparator lengths by tying the outputs F₁, F₂,... F_n together and selecting an external pull-up resistor in accordance with his specific requirements.

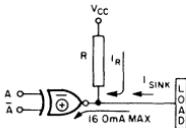
When selecting a pull-up resistor the following guidelines are suggested:

1. Determine the maximum current that the 8242 must sink from the load when the 8242 is in the "0" output state.



8242 Output = "0"

2. Subtract the required sink current from 16.0mA, the total sink capability of the 8242. This determines the amount of current which may be allowed to flow through the external pull-up resistor.

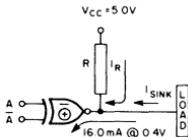


8242 output = "0"

$$I_R + I_{SINK} \leq 16.0\text{mA}$$

$$\text{max. } I_R \leq 16.0\text{mA} - I_{SINK}$$

3. Assume $V_{CC} = 5.0\text{V}$ and output "0" level = 0.4V max., then calculate the minimum value of the pull-up resistor required to satisfy $I_R + I_{SINK} \leq 16.0\text{mA}$.



8242 Output = "0"

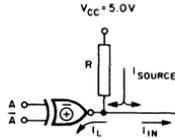
$$\text{min. } R \geq \frac{V_{CC} - V_{out} \text{ "0" }}{16.0\text{mA} - I_{SINK}}$$

$$\geq \frac{V_{CC} - V_{out} \text{ "0" }}{I_R}$$

$$\geq \frac{5.0\text{V} - 0.4\text{V}}{I_R}$$

$$\text{min. } R \geq \frac{4.6\text{V}}{I_R}$$

4. Check to ensure that the pull-up resistor selected is consistent with the "1" output voltage and "1" output current required.



8242 Output = "1"

$$I_L = 50\mu\text{A max.}$$

$$I_{\text{SOURCE}} = I_L + I_{\text{in}}$$

$$\text{"1" Output Voltage} = V_{\text{CC}} - (I_{\text{SOURCE}} \times R)$$

$$\text{max. } I_{\text{SOURCE}} \times R = V_{\text{CC}} - \text{"1" Output Voltage}$$

$$= 5.0\text{V} - 2.8\text{V}$$

$$\text{max. } I_{\text{SOURCE}} \times R \leq 2.2\text{V}$$

$$\text{max. } R \leq \frac{2.2\text{V}}{I_{\text{SOURCE}}}$$

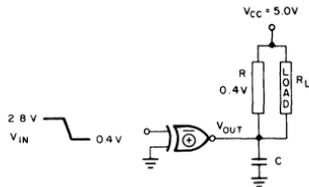
To ensure that normal "1" level noise margins are maintained, the "1" output voltage should be maintained at 2.8V or above for $V_{\text{CC}} = 5.0\text{V}$.

Under light fan-out conditions, a relatively large resistor ($\approx 4\text{K}$ to 10K) may be considered by the designer. Two considerations must be weighed in selecting a large value pull-up resistor.

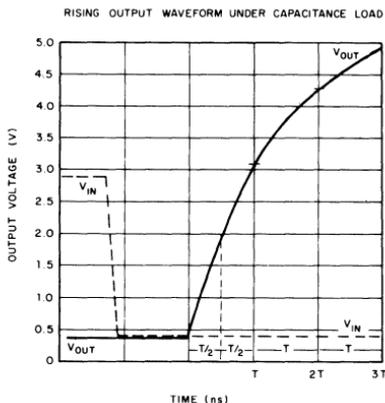
First, rise time into a capacitance load at the output will be directly related to the value of pull-up resistor used. An approximation of the time required for the rising output voltage to reach a defined "1" level (2.0V) is $\tau/2$, or $1/2 R_{\text{EQ}} C$.

$$\tau = R_{\text{EQ}} C$$

$$R_{\text{EQ}} = \frac{R \times R_L}{R + R_L}$$



The voltage level attained in time $\tau \approx 0.63 \times V_{CC} = 3.15V$, well above minimum "1" logic input threshold voltage.



The second consideration which should be given to use of a large value pull-up resistor is the resulting susceptibility to capacitively coupled noise along printed circuit runs or wire interconnects. Since the magnitude of coupled noise is related to the equivalent impedance between the output of the 8242 and its load, care should be taken in the physical layout to isolate the output of an 8242 where a large value pull-up resistor has been chosen. In general, a pull-up resistor of $1K\Omega$ or less is recommended where "0" DC fan-out is less than 10.0mA and power supply drain current is not critical.

There is no current spike associated with the output transition in the 8242 since the active pull-up of classic TTL designs has been removed. It is not necessary to capacitively decouple the 8242.

DEVICE DESCRIPTION: 8266

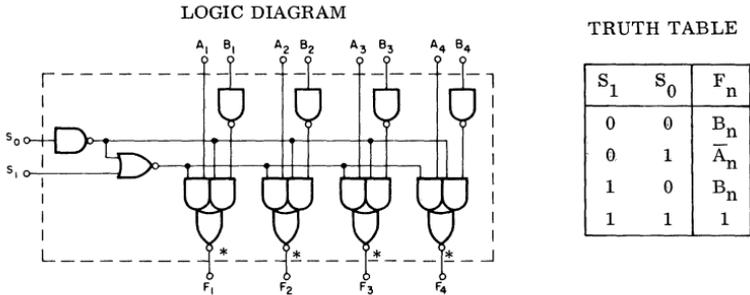
The 8266 is a 2-input, 4-bit multiplexer which finds extensive applications in selecting which data from two different sources is to be processed. This mode of operation is the multiplex mode.

The second area of applications for the 8266 is found in central processors. When the two inputs for each bit position (A_i, B_i) are connected together, the 8266 performs as a conditional complementor required in conjunction with adders to provide ADDITION/SUBTRACTION subsystems. Also while operating in this mode, the 8266

is ideal for parallel data transfer within an arithmetic section.

The logic diagram and truth table are shown in Figure 3.

Figure 3. 8266 2-Input, 4-Bit Multiplexer



*8267 has open collectors.

Both Military (-55°C to +125°C) and Industrial (0°C to +75°C) devices are available in 16 pin dual-in-line and flat packages.

Conservative design practices require that the user decouple the 8266 by placing a .01µf between V_{CC} and ground. Decoupling capacitors should be non-inductive.

DEVICE DESCRIPTION: 8267

The 8267 has the same logic configuration and truth table as the 8266 (Figure 3). The 8267 features open collector output switching transistors to facilitate expansion of the number of input terms per bit when used in multiplex applications.

Since there is no active pull-up, it is not necessary for the user to capacitively decouple this device. However, an external pull-up resistor must be selected by the user. Guidelines for selecting pull-up resistors are the same as those described earlier for the 8242. The 8267 is available in both Military (-55°C to +125°C) and Industrial (0°C to +75°C) temperature range and in 16 pin dual-in-line and flat package configurations.

APPLICATIONS:

HIGH SPEED EQUALITY COMPARATORS

The Exclusive-OR may be used to check the equality of two binary coded words. From the truth table (Figure 1), the output of the Exclusive-OR is "1" when the inputs are not equal and "0" when the inputs are equal. By connecting the output of the Exclusive-OR to one input of a NOR gate (Figure 4), the output (f_0) will be "1" if and only if all bits of the two words are equal. Figure 4 shows a high speed equality comparator capable of comparing two 4-bit words.

Figure 4. Equality Comparator for Two 4-Bit Words

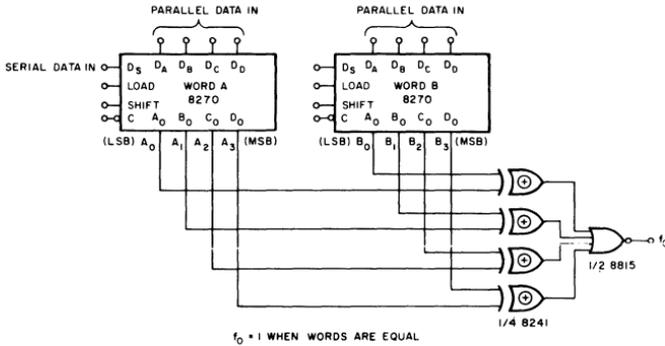
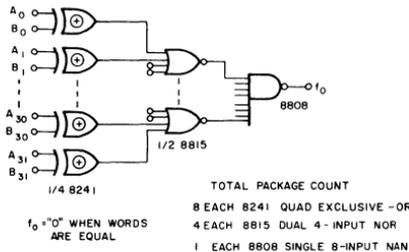


Figure 5 demonstrates a method of designing a high speed equality comparator for a maximum word length of 32 bits using TTL elements. This method may also be used to design high speed equality comparators for other word lengths between 4-bits and 32-bits. The addition of the single 8-input NAND (8808) provides $f_0 = "0"$ when words A ($A_0, A_1, A_2 \dots A_{n-1}, A_n$) and B ($B_0, B_1, B_2 \dots B_{n-1}, B_n$) are equal and $f_0 = "1"$ when words A and B are unequal.

Figure 5. High Speed 32-Bit Word Equality Comparator

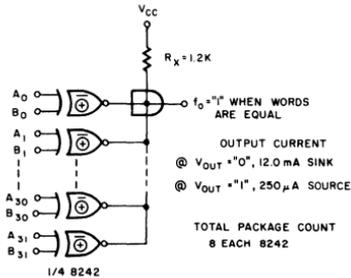


MAXIMUM LENGTH EQUALITY COMPARATORS

The 8242 is specifically designed for use in equality comparison of word lengths in excess of 4 bits, while providing minimum can-counts. From the truth table (Figure 2) the 8242 will provide a "1" output when the inputs are equal and "0" when the inputs are unequal. The open collector outputs of the 8242 can be connected together to perform a logical AND of the output terms when returned to V_{CC} through an external resistor.

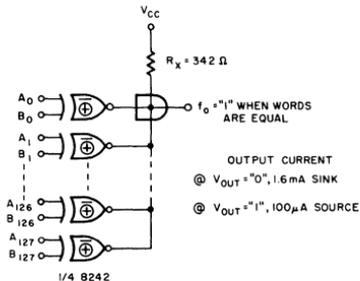
Guidelines for selecting the pull-up resistor value are given under DEVICE DESCRIPTION: 8242. The can-count reduction for the 32-bit word length equality comparator shown in Figure 5 is demonstrated in Figure 6.

Figure 6. Implementation of 32-Bit Word Comparator



The maximum word length equality comparator which can be implemented under worst case specifications is shown in Figure 7. In this implementation, two words of 128 bits each can be compared for equality.

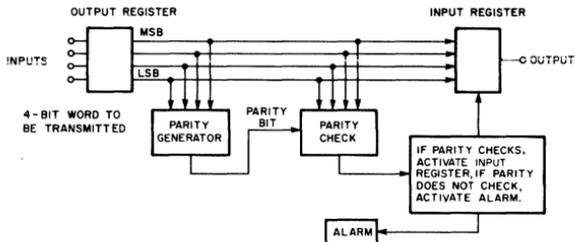
Figure 7. Maximum Length Equality Comparator (128-Bit Words)



PARITY TESTER/GENERATOR

The Exclusive-OR and EQUALITY COMPARATOR may be used in parity testing or generating applications. Parity generators find wide application in output equipment which records or transmits data. A parity bit is generated to ensure that the total number of logical ones in the word being recorded or transmitted is either even or odd. On the reading or receiving end of the data transmission a parity check is performed on the transmitted data (including the parity bit) to ensure that no word bit has been "dropped" (i.e., no "1" has been lost). Figure 8 shows a general case implementation of parity generation and parity check in the recording or transmission of a 4-bit word. Note that there are five bits of transmitted data, the 4-bit word plus the parity bit.

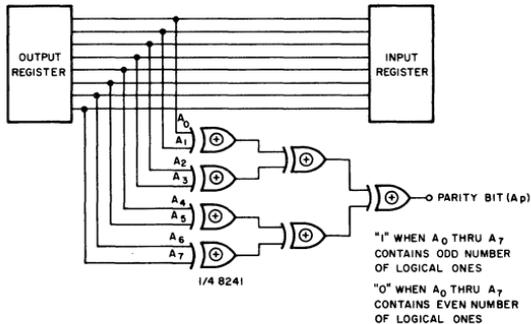
Figure 8. General Case Parity Generator and Parity Check



In data transmissions which include a parity bit, the designer chooses between the EVEN PARITY system and the ODD PARITY system. In the even parity system, an even number of logical ones is always transmitted (data plus parity bit). Therefore, the EVEN PARITY GENERATOR examines the data to be transmitted and produces an additional "1" if the data contains an odd number of logical ones. If the data to be

transmitted already contains an even number of logical ones, the EVEN PARITY GENERATOR produces a parity bit equal to "0". In either case an even number of logical ones (data plus parity bit) will be transmitted. The 8241 may be used to design an EVEN PARITY GENERATOR, as shown in Figure 9.

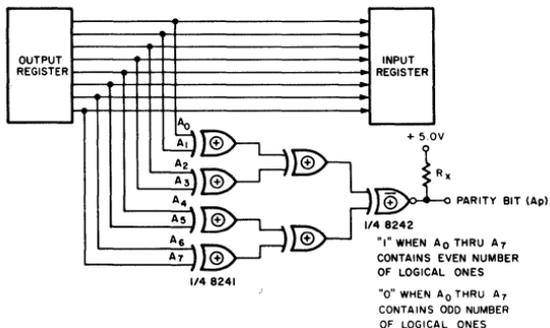
Figure 9. Even Parity Generator Used with 8-Bit Word



Conversely, the ODD PARITY GENERATOR examines the terms in the data to be transmitted and produces a "0" when the data already contains an odd number of logical ones. If, however, the data contains an even number of logical ones, the odd parity generator produces an additional "1". In either case the total number of logical ones (data and parity bit) transmitted is odd. An advantage of odd parity is that transmission of "0" data is not mistaken for no information (always have one "1" bit).

The odd parity generator is shown in Figure 10. It differs from the even parity generator only in the output stage which incorporates 1/4 of an 8242.

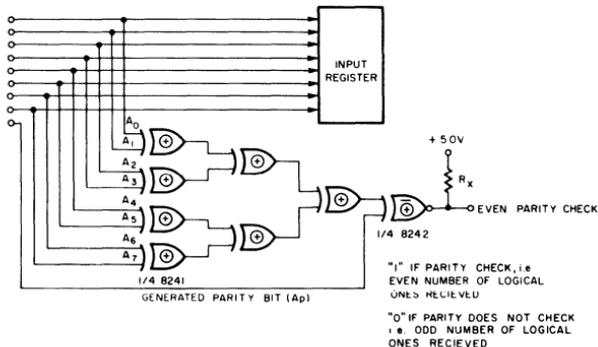
Figure 10. Odd Parity Generator Used with 8-Bit Word



As described in Figure 8, the receiving equipment must check all incoming lines to ensure that no bits have been dropped in data recording or transmission.

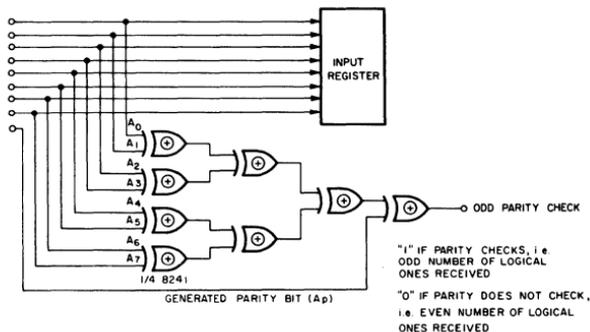
In the even parity system, an EVEN PARITY CHECKER examines all incoming terms (data plus parity bit) and provides a "1" output if there are still an even number of logical ones contained in the data received. If a bit has been dropped and an odd number of logical ones is received, the output of the even parity checker will be "0". An example of an even parity checker is shown in Figure 11.

Figure 11. Even Parity Checker Used with 8-Bit Word



The ODD PARITY CHECKER provides a "1" output when the total number of logical ones received (data plus parity bit) is odd and produces a "0" when the total number of logical ones received is even. Figure 12 shows an example of an odd parity checker.

Figure 12. Odd Parity Checker Used with 8-Bit Word

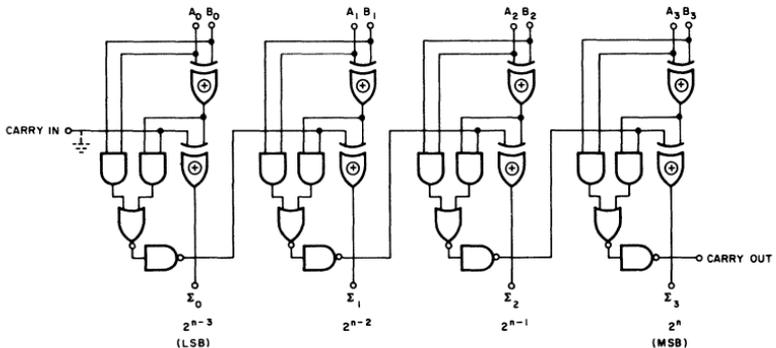


Parity generators and checkers find wide application in I/O (input-output) equipment such as magnetic tape writers and readers. In addition parity generators and checkers may be used anywhere within a system where there is concern about "dropping" bits due to the nature of the equipment used to send and/or receive information. A parity system may also be incorporated in equipment where high ambient noise is of concern when recording or transmitting data.

ADDERS

The Exclusive-OR is the heart of an adder system. Figure 13 shows 4-bits of a binary adder with ripple carry.

Figure 13. Binary Adder with Ripple Carry (4-Bits).

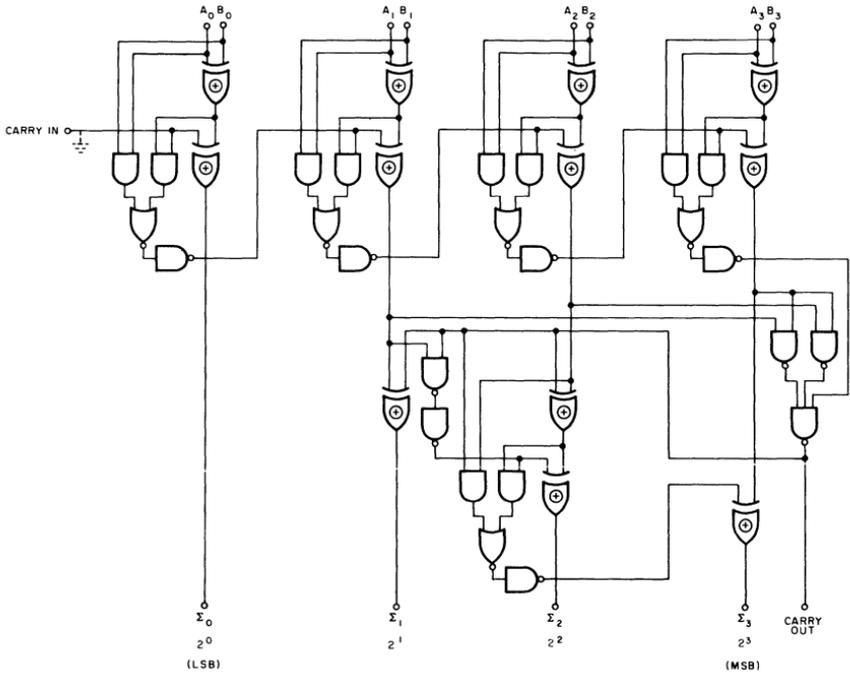


Each 2-wide 2-input AND-OR-INVERT gates shown in Figure 13 may be 1/2 8440 and each inverters 1/6 of 8490 is power consumption is of prime concern. If speed is of prime concern, the 8440 may be replaced by 8840 and the 8490 by 8H90.

The binary adder shown in Figure 13 may be expanded to arbitrary length by simply continuing the pattern of interconnection shown. The CARRY IN term of the least significant bit (LSB) is grounded in actual implementation.

Figure 14 shows the construction of a BCD adder. A second decade of addition would be constructed exactly as shown in Figure 14. The CARRY IN term of the least significant decade is grounded in actual implementation.

Figure 14. BCD Adder with Ripple CARRY (ONE DECADE)



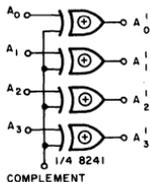
Each 2-wide, 2-input AND-OR-INVERT gate shown in Figure 14 may be 1/2 8440 (low power) or 1/2 8840 (high speed). Each inverter shown may be 1/6 8490 (low power) or 1/6 8H90 (very high speed). Each 2-input NAND may be 1/4 8480 (low power), 1/4 8880 (high speed) or 1/4 8H80 (very high speed). The 3-input NAND may be 1/3 8470 (low power), 1/3 8870 (high speed) or 1/3 8H70 (very high speed).

CONDITIONAL COMPLEMENTORS

ADD-SUBTRACT subsystems require the ability to present information to the inputs of the adder in its TRUE form for addition and in its COMPLEMENT form for subtraction.

The Exclusive-OR may be used to implement a 4-bit conditional complementor as shown in Figure 15.

Figure 15. 4-Bit Conditional Complementor



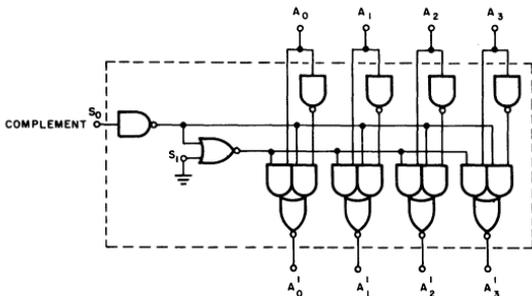
TRUTH TABLE

INPUTS		OUTPUT
Complement	A_i	A_i
0	0	A_i
0	1	A_i
1	0	$\overline{A_i}$
1	1	$\overline{A_i}$

The Conditional Complementor may be expanded by connecting the COMPLEMENT inputs together. The designer should consider the additional fan-out required to drive the COMPLEMENT input on expanded Conditional Complementors designed with 8241's. The gate driving the COMPLEMENT input of Figure 15 must sink 12.8mA at $V_o = "0"$ and source 200 μ A at $V_o = "1"$.

The 8266 and 8267 are devices specifically applicable in performing the Conditional Complement function for long word lengths. Because the Select line inputs are buffered, the 8266 and 8267 can be expanded without particular concern about the fan-out to the COMPLEMENT input which delivers 1.6mA in the "0" state and requires 25 μ A in the "1" state, for each four bits. Figure 16 shows an example of a 4-bit Conditional Complementor using the 8266.

Figure 16. 4-Bit Conditional Complementor



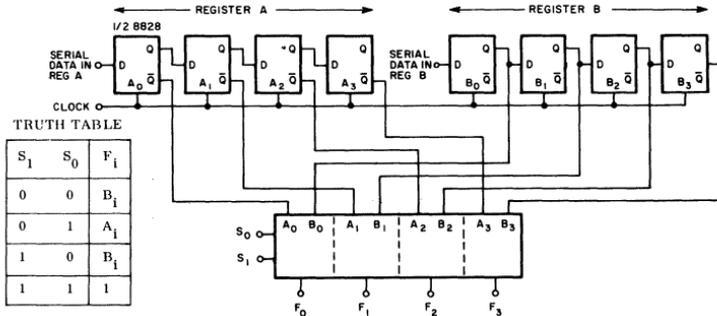
TRUTH TABLE

INPUTS		OUTPUT
Complement	A_i	A_i
0	0	A_i
0	1	A_i
1	0	$\overline{A_i}$
1	1	$\overline{A_i}$

MULTIPLEXERS

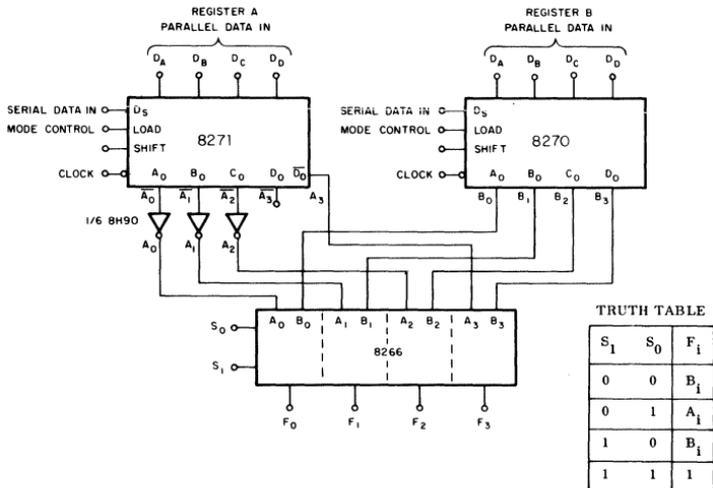
The 8266 and 8267 also find application in multiplex circuits. The 8266 is specifically intended for application as a 2-input 4-bit multiplexer. Examples of 4-bit multiplexers using the 8266 are shown in Figures 18 and 19. These examples assume the designer wishes to multiplex TRUE data inputs only.

Figure 18. 2-Input 4-Bit Multiplexer



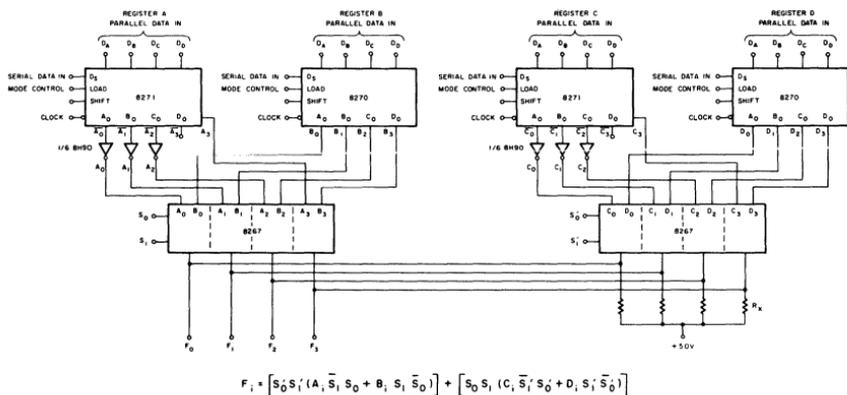
Note that the \bar{Q} (not true) outputs of the A register were used to accomplish multiplex of the true terms. When the not true outputs are unavailable, the A_0 , A_1 , A_2 and A_3 input terms to the 8266 must be inverted to provide the multiplex of the true terms only, as shown in Figure 19.

Figure 19. 2-Input 4-Bit Multiplexer



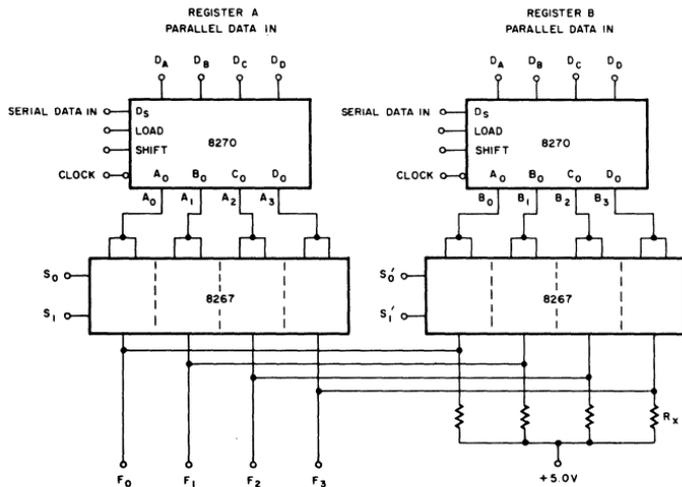
The 8267 was specifically designed for use in multiplex of conditional complement terms and general multiplex applications requiring expansion of input terms. The 8267 features open collector output switching transistors which may be used to perform the collector AND function, thus increasing the number of input terms to be multiplexed per bit. The maximum expansion requires an external pull-up resistor of 342 ohms and provides a 128-INPUT 4-BIT MULTIPLEXER. Selection of input terms is accomplished by applying the desired code on the S_0, S_1 lines of the appropriate 8267 while $S_0 = S_1 = 1$ is applied to the unselected 8267's as shown in Figure 20.

Figure 20. 4-Input 4-Bit Multiplexer



The 8267 is well suited for multiplex applications of Conditional Complement terms in ADD-SUBTRACT subsystems as shown in Figure 21.

Figure 21. 2-Input 4-Bit Conditional Complementor/Multiplexer



$$F_i = [S_0' S_1' (A_i \bar{S}_0 S_1 + \bar{A}_i S_0 \bar{S}_1)] + [S_0 S_1 (B_i \bar{S}_0' S_1' + \bar{B}_i S_0' \bar{S}_1')]$$

SECTION 4
COUNTERS, SHIFT REGISTERS, AND MEMORIES



APPLICATIONS MEMO

8270/8271 FOUR BIT SYNCHRONOUS SHIFT REGISTER

1. GENERAL DESCRIPTION

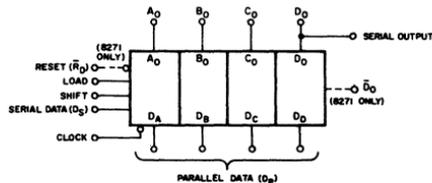
The Four Bit Shift Register is available in different configurations:

- A. S8270J - 14 pin flat pack, -55° C to +125° C.
- B. N8270J - 14 pin flat pack, 0° C to +75° C.
- C. S8270A - 14 pin Dual-In-Line, -55° C to +125° C.
- D. N8270A - 14 pin Dual-In-Line, 0° C to +75° C.
- E. S8271B - 16 pin Dual-In-Line, -55° C to +125° C.
- F. N8271B - 16 pin Dual-In-Line, 0° C. to +75° C.

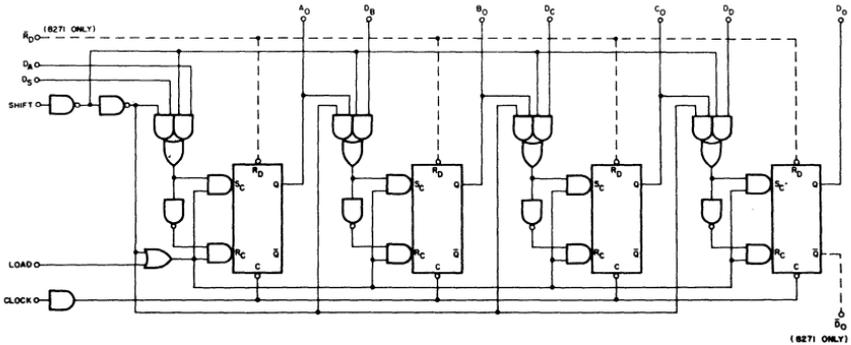
The 8270 has serial and parallel entry, serial and parallel output. Further there are two control inputs, LOAD and SHIFT, which have the following effect:

State	LOAD	SHIFT	Effect (If CLOCK-Input Level Falls)
0	0	0	Store - No entry
1	0	1	Shift Right (D_s data)
2	1	0	Parallel Load (D_p data)
3	1	1	Shift Right (D_s data)

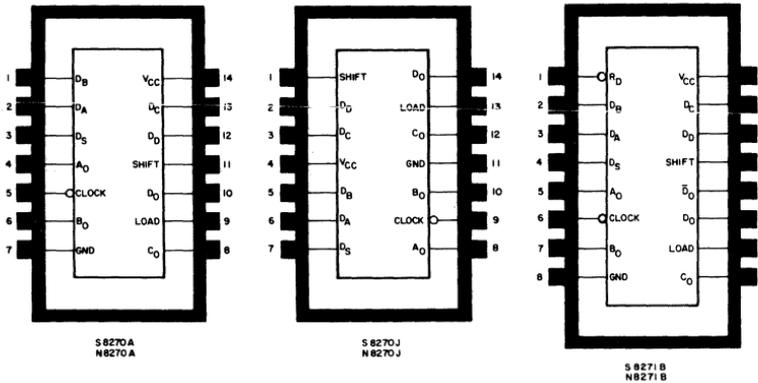
Therefore, depending on the control states 0 . . . 3, the shift register operates in the different modes. Thus a free-running clock signal can be applied. The buffered clock stage triggers the shift register with the falling edge. In addition to the 8270 features, the 8271 provides the not-true output of the fourth stage (\bar{D}_0) and a RESET input (\bar{R}_D), which is common for all four flip-flops. If the \bar{R}_D input is low, all stages are cleared independent of the CLOCK or the logic input state. The clock transition dominates over the RESET. Thus,



a positive going spike may be expected at the output although the RESET input is low.

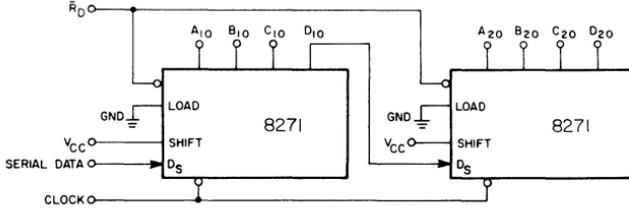


PIN CONFIGURATIONS



2. SOME SHIFT REGISTER APPLICATIONS

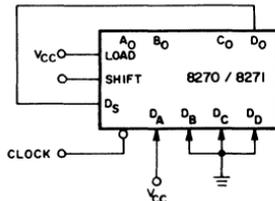
2.1 Simple 8-Bit Right Shift Register



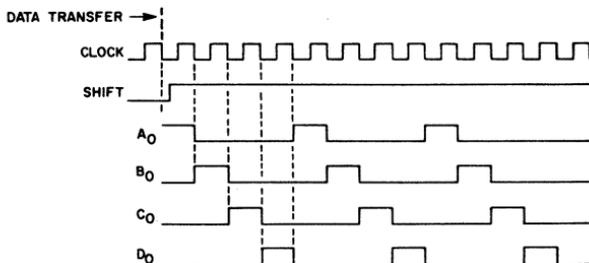
Let us assume first that the shift register flip-flops are reset to zero, applying a logic low to the \bar{R}_D input. Now the first bit X_1 , ($X_1 = 1$ or 0) using the serial data input is shifted in the first flip-flop A_{10} by the first falling transition of the clock signal. The second trigger pulse of the clock shifts the first bit X_1 to the second flip-flop B_{10} and at the same time the second bit X_2 is loaded in the first flip-flop A_{10} . To make it more clear, let us study an example with the serial data ($X_1 X_2 X_3 0 0 0 \dots 0$):

CLOCK PULSE	STATE	SERIAL DATA ($X_1 X_2 X_3 00\dots 0$)	FLIP-FLOP								
			A_{10}	B_{10}	C_{10}	D_{10}	A_{20}	B_{20}	C_{20}	D_{20}	
		RESET	0	0	0	0	0	0	0	0	0
0		X_1	X_1	0	0	0	0	0	0	0	0
1		X_2	X_2	X_1	0	0	0	0	0	0	0
2		X_3	X_3	X_2	X_1	0	0	0	0	0	0
3		0	0	X_3	X_2	X_1	0	0	0	0	0
4		0	0	0	X_3	X_2	X_1	0	0	0	0
5		0	0	0	0	X_3	X_2	X_1	0	0	0
6		0	0	0	0	0	X_3	X_2	X_1	0	0
7		0	0	0	0	0	0	X_3	X_2	X_1	0
8		0	0	0	0	0	0	0	X_3	X_2	X_1
9		0	0	0	0	0	0	0	0	X_3	X_2
10		0	0	0	0	0	0	0	0	0	X_3
11		0	0	0	0	0	0	0	0	0	0

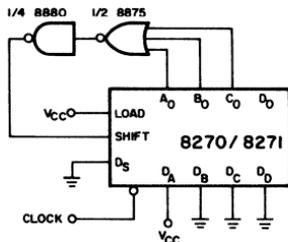
2.2 Ring Circuit



To demonstrate the parallel loading and serial shift operations we intend to preload the shift register with the data $(D_A, D_B, D_C, D_D) = (1, 0, 0, 0)$. Therefore, we apply a logic one to the pin D_A and a logic zero to the pins D_B, D_C, D_D . A logic zero at the control input SHIFT enables the falling clock signal to transfer the data $(D_A, D_B, D_C, D_D) = (1, 0, 0, 0)$ to the shift register. To shift right now the SHIFT input must stay on a logic one level permanently. The following diagram results:



A ring circuit is applied successfully if gating problems should be solved. A modified version of a ring circuit with self-correcting feature is shown below:



We start with an arbitrary state (A, B, C, D) after maximum three shift pulses we reach the state (0, 0, 0, D) and for this state the SHIFT input is low. Thus the word (1, 0, 0, 0) is preloaded by the next negative going transition of the clock signal. The truth table for the ring circuit is given below:

1	0	0	0	0	preloaded data
0	1	0	0	0	
0	0	1	0	0	
0	0	0	1	0	
0	0	0	1	1	feedback logic detects this state
1	0	0	0	0	preloaded data

2.3 Ring Counter

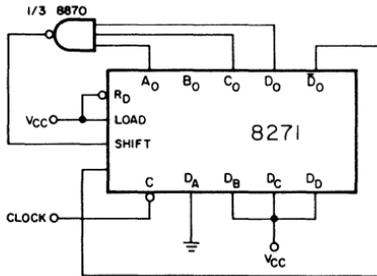
A ring counter built with an n-stage shift register counts through $2n$ states. For $n = 4$ the eight states are listed below:

STATE	A	B	C	D	BCD	REMARK
1	1	1	1	1	15	FEEDBACK LOGIC DETECTS THIS STATE PARALLEL LOADED DATA
2	0	1	1	1	7	
3	0	0	1	1	3	
4	0	0	0	1	1	
5	0	0	0	0	0	
6	1	0	0	0	8	
7	1	1	0	0	12	
8	1	1	1	0	14	
1	1	1	1	1	15	END OF PERIOD

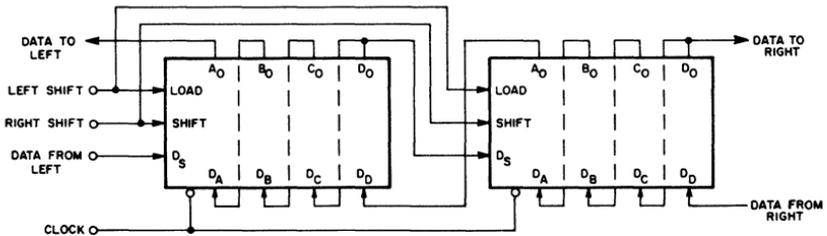
Note, another stable loop exists with the remaining unused states.

STATE	A	B	C	D	BCD	REMARK
1	1	0	1	1	11	FEEDBACK LOGIC DETECTS THIS STATE AND (0111) IS PRELOADED
2	0	1	0	1	5	
3	0	0	1	0	2	
4	1	0	0	1	9	
5	0	1	0	0	4	
6	1	0	1	0	10	
7	1	1	0	1	13	
8	0	1	1	0	6	
1	1	0	1	1	11	END OF PERIOD

With an additional feedback loop the ring counter will correct itself from stable loop conditions which exist in the unused states.



2.4 Left-Right Shift Registers (8270/8271)

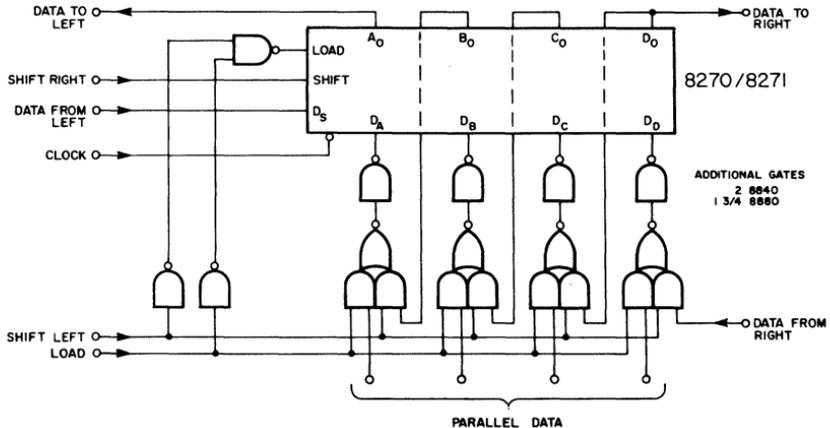


The example shows an 8-bit serial entry, left-right shift application. Note, that a free running clock can be applied.

THE DIFFERENT MODES ARE:

LOAD	SHIFT	REMARK
0	0	DATA STORED
0	1	DATA SHIFTED RIGHT
1	0	DATA SHIFTED LEFT

A left-right shift register with parallel entry is shown in the next example



2.5 Variable 4-bit Modulo N Counter ($2 \leq N \leq 15$)

It is well known that an n-stage binary shift register, when provided with suitably designed feedback paths, can count through $2^n - 1$ distinct states without any external input. For $n = 4$ there are two linear recurrences for a maximum period $p = 2^4 - 1 = 15$.

$$X_1 = A_0 \bar{D}_0 + \bar{A}_0 D_0 \quad (\bar{X}_1 = \bar{A}_0 \bar{D}_0 + A_0 D_0)$$

or

$$X_1 = C_0 \bar{D}_0 + \bar{C}_0 D_0 \quad (\bar{X}_1 = \bar{C}_0 \bar{D}_0 + C_0 D_0)$$

X_1 : Generated bit, which is feedbacked to the first flip-flop.

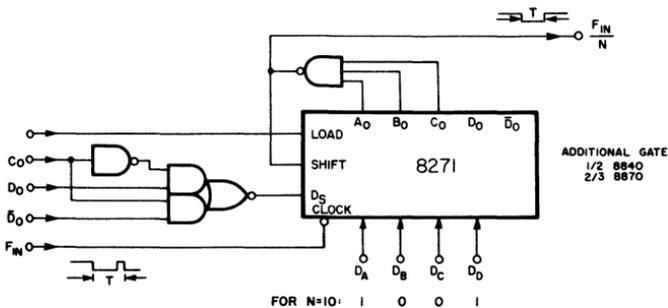
As an example, we note the different states for the recurrence $\bar{X}_1 = \bar{C}_0 \bar{D}_0 + C_0 D_0$, starting with $A_0 B_0 C_0 D_0 = (0 \ 1 \ 1 \ 1)$

STATE	$\bar{X}_1 \equiv A_0 B_0 C_0 D_0$	N
1	0 1 1 1	15
2	1 0 1 1	14
3	1 1 0 1	13
4	0 1 1 0	12
5	0 0 1 1	11
6	1 0 0 1	10
7	0 1 0 0	9
8	1 0 1 0	8
9	0 1 0 1	7
10	0 0 1 0	6
11	0 0 0 1	5
12	0 0 0 0	4
13	1 0 0 0	3
14	1 1 0 0	2
15	1 1 1 0	-
16#1	0 1 1 1	

$\bar{C}_0 \bar{D}_0 + C_0 D_0 = 1 = \bar{X}_1$
FOR STATE 2

We note that only the state 1 1 1 is not generated. Starting with 1 1 1 1 and applying the rule $\bar{X}_1 = \bar{C}_0 \bar{D}_0 + C_0 D_0$, the combination 1 1 1 1 will be generated once again. Therefore, it is obvious that the long period ($p = 15$) cannot include this state.

To implement a variable modulo N counter, we preload the shift register with the logic configuration $N = (A_0 B_0 C_0 D_0)$ whenever the end of the period (1 1 1 0) is reached. (For N see the truth table).



The counter can be locked at the end of each period with the control input 'LOAD'. Further the counter has a self-correcting feature for all N , because every possible state leads back to the original period (truncated period for $2 \leq N \leq 14$). Note, that the special state (1 1 1 1) influences the shift input as well as the state (1 1 1 0).

2.6 Error-Correcting Code Generator

A four bit shift register with a feedback loop is preloaded with an arbitrary four bit number. The shift register feedback path is given by the equation

$$X_1 = A_0 \oplus B_0 \oplus D_0 = Y \oplus D_0 = Y\bar{D}_0 + \bar{Y}D_0$$

and

$$Y = A_0 \oplus B_0 = A_0\bar{B}_0 + \bar{A}_0B_0$$

The preloaded numbers are shifted seven times, generating the following output sequences.

	INPUT INFORMATION				OUTPUT CODEWORDS						
	A_0	B_0	C_0	D_0	b_1	b_2	b_3	b_4	b_5	b_6	b_7
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	1	1	0	0	0	1
2	0	0	1	0	1	1	0	0	0	1	0
3	0	0	1	1	1	0	1	1	0	0	1
4	0	1	0	0	1	1	1	0	0	1	0
5	0	1	0	1	1	0	0	0	1	0	1
6	0	1	1	0	0	0	1	0	1	1	0
7	0	1	1	1	0	1	0	0	1	1	1
8	1	0	0	0	1	0	1	1	0	0	0
9	1	0	0	1	1	1	0	1	0	0	1
10	1	0	1	0	0	1	1	1	0	1	0
11	1	0	1	1	0	0	0	0	1	0	1
12	1	1	0	0	0	1	0	1	1	0	0
13	1	1	0	1	0	0	1	1	0	1	0
14	1	1	1	0	1	0	0	1	1	1	0
15	1	1	1	1	1	1	1	1	1	1	1

THE RELATIONS ARE

$$b_1 = A_0 \oplus B_0 \oplus C_0$$

$$b_2 = B_0 \oplus C_0 \oplus D_0$$

$$b_3 = A_0 \oplus B_0 \oplus D_0$$

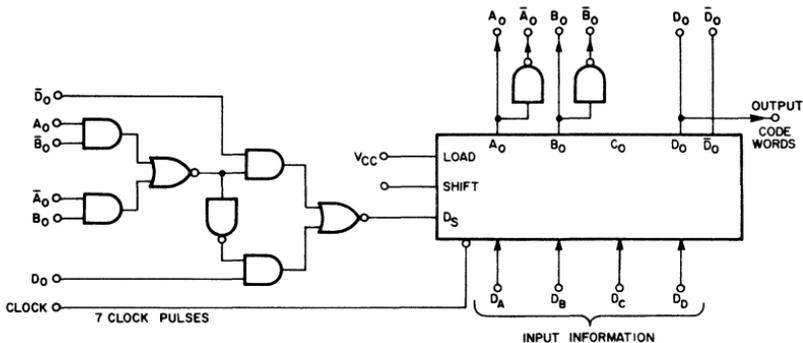
$$b_4 = A_0$$

$$b_5 = B_0$$

$$b_6 = C_0$$

$$b_7 = D_0$$

The value of this procedure is that the set of sixteen codewords thus generated has the property that any two of them differ in at least three of their seven bits. Further the additional bits $b_1 b_2 b_3$ enable to correct the code, if one but only one error occurs.



Additional gates 3/4 8880

1 8840

SHIFT = 0 Preload the input information

SHIFT = 1 Shift Right

To check and correct if necessary the received message, we form the sums S_1, S_2, S_3 .

$$S_1 = b_2 + b_5 + b_6 + b_7$$

$$S_2 = b_1 + b_4 + b_5 + b_6$$

$$S_3 = b_3 + b_4 + b_5 + b_7$$

If each sum is even no correction is necessary.

If, as an example, S_1 is odd one of the bits b_2, b_5, b_6, b_7 is not correct. Assuming further the sum S_2 is also odd, only one of the bits b_5, b_6 being contained in S_1 as well as in S_2 can be incorrect. If the sum S_3 is even the bit b_5 has the correct binary value implying b_6 is the erroneous bit. Assigning now the logic value $Z = 1$ if the corresponding sum is odd

and $Z = 0$ whenever the sum is even we are able to construct a truth table for the erroneous bit.

Z_3	Z_2	Z_1	ERRONEOUS BIT
0	0	1	b_2
0	1	0	b_1
1	0	0	b_3
0	1	1	b_6
1	0	1	b_7
1	1	0	b_4
1	1	1	b_5

} INFORMATION

$$Z_1 = b_2 \oplus b_5 \oplus b_6 \oplus b_7$$

$$Z_2 = b_1 \oplus b_4 \oplus b_5 \oplus b_6$$

$$Z_3 = b_3 \oplus b_4 \oplus b_5 \oplus b_7$$

Reference: Solomon W. Golomb "Shift Register Sequences" Holden-Day, Inc. San Francisco, Cambridge, London; 1967.



APPLICATIONS MEMO

W. Booth

ASYNCHRONOUS DATA REGISTERS

A problem frequently encountered in computer peripherals (and similar devices) is that of synchronizing input information with the internal functions of the peripheral.

This memo discusses several solutions to the problem.

The circuit of Figure 1 is used when the problem is to detect whether or not input data was present during the sampling interval. As soon as Data goes to "1", the flip-flop will go to "1" and will remain "1" until the next Reset pulse.

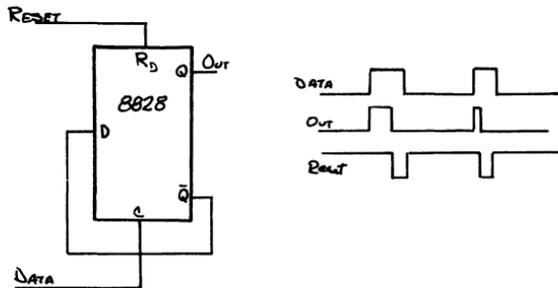


Figure 1

The circuit of Figure 2 performs the same function as that of Figure 1. Again, the flip-flop goes to "1" at the rising edge of Data and will go to "0" at the rising edge of Reset unless Data is high; in this case the flip-flop will remain "1".

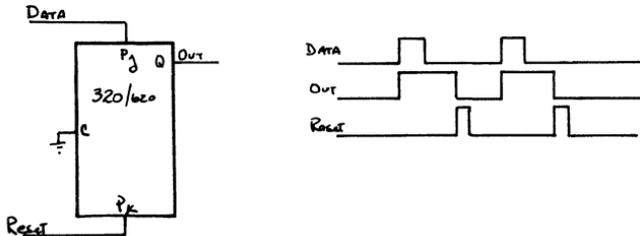


Figure 2

The circuit of Figure 3 performs the same function as that of Figures 1 and 2. However input polarities are different. Also, if Data is low while Reset is low, Out will be correctly at "1", but Out will also be "1".

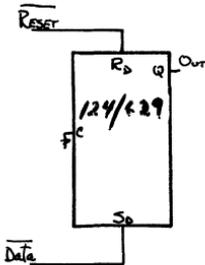


Figure 3

The circuit of Figure 4 is used when one wishes to sample an asynchronous input with a synchronous sample or clock pulse. The flip-flops will take the state of the data at the rise of the clock pulse. Changes in Data while the clock is high will have no effect.

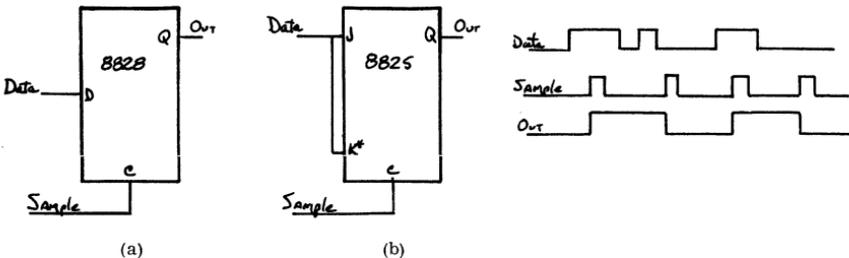


Figure 4

The circuit of Figure 5 is essentially the same as that of Figure 4 with the exception that the sampling will occur at the falling (negative going) edge of the clock pulse. If Data changes while clock is high, the output may be somewhat ambiguous if the change is within 75ns of the fall of the clock pulse. Generally this kind of sampling accuracy is acceptable.

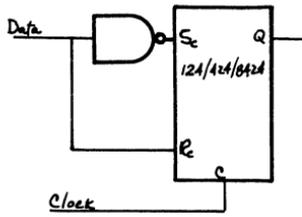


Figure 5

If the requirement is to convert RZ input information to NRZ information, the circuits of Figures 6, 7, 8 and 9 may be used. The waveforms are as in Figure 10.

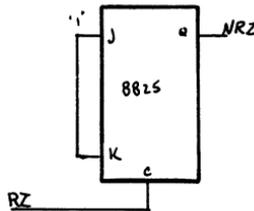


Figure 6

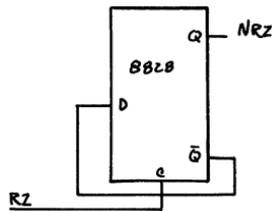
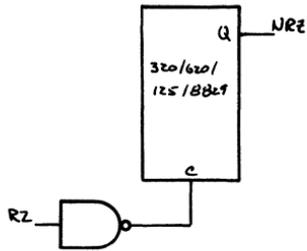


Figure 7



for 125, ground J* and K*

Figure 8

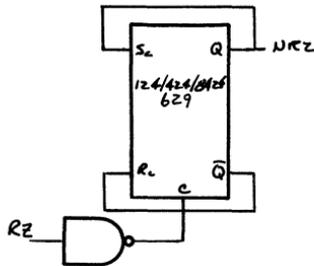


Figure 9



Figure 10



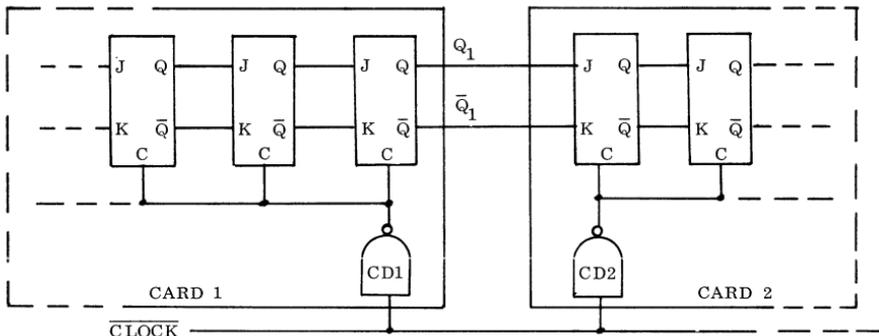
Tom McCarthy

APPLICATIONS MEMO

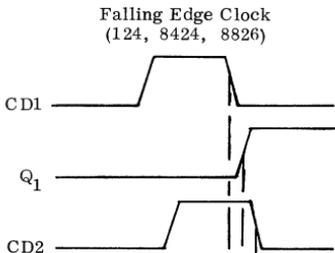
PREVENTION OF CLOCK SKEW IN LONG SHIFT REGISTERS

Clock skew is a common problem to the logic designer, particularly when a clock has to drive long shift registers. With long registers it is often necessary to use multi-clock drivers per printed circuit card (P.C. Card) or split the register on several P.C. Cards. A method for preventing clock skew is shown by example as follows:

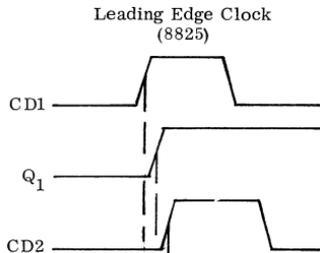
Clock drivers are provided on each card to avoid high current spikes between cards.



A clock skew problem occurs when CD1 (Clock Driver No. 1) has a significantly shorter propagation delay than CD2 (Clock Driver No. 2). The output of the F/F on Card 1 (Input to Card 2) may change before CD2 switches, resulting in transfer of incorrect data. The clock skew problem is illustrated in the sketches shown below for both leading edge triggering binaries.

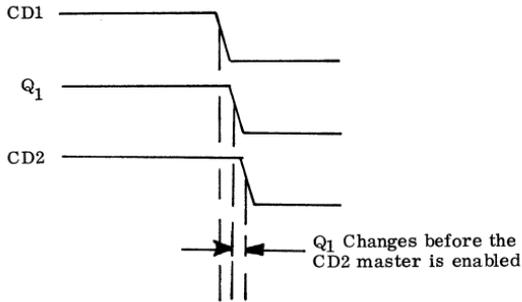


Q_1 Changes prior to fall of CD2

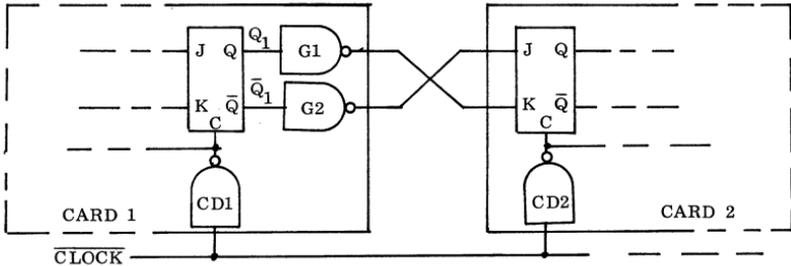


Q_1 Changes prior to rise of CD2

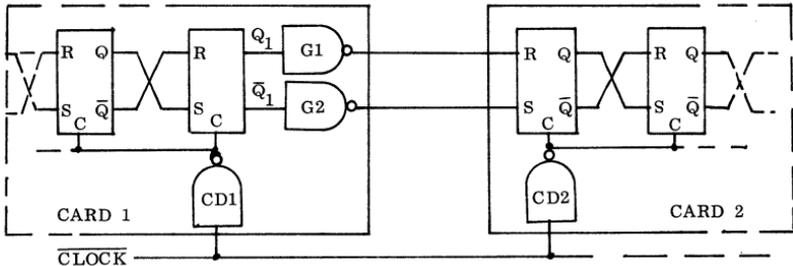
Master/Slave Clock — 125, 320 and 620



To compensate for the delay difference between CD1 and CD2 a NAND gate on each output of the F/F on Card 1 is used to provide added propagation delay. The overall propagation delay of $Q_1 + G1$ and $\bar{Q}_1 + G2$ is sufficient to prevent clock skew.



For JK F/F — 125, 320, 620, 8825, 8826



For RS F/F — 124 and 8424

The same technique can be employed where multi-drivers are used on each card.

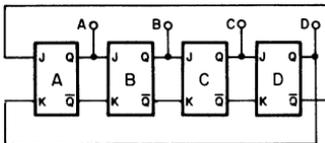


APPLICATIONS MEMO

SELF-CORRECTING RING COUNTERS

Ring counters are special adaptations of shift registers and are used for commutators, sequence generators, and decoders. They can be made out of R-S or J-K binaries. One problem that has been associated with them is that stable sub-loops may be set up during power turn-on or transient noise conditions. These sub-loops cause the counter to oscillate between two states, thus stopping the desired count. Here is an example:

Suppose we have a twisted ring counter (this is a ring counter which gives a $2N$ count for N binaries):



The truth table for this counter is as follows:

TRUTH TABLE				
A	B	C	D	Count
0	0	0	0	1
1	0	0	0	2
1	1	0	0	3
1	1	1	0	4
1	1	1	1	5
0	1	1	1	6
0	0	1	1	7
0	0	0	1	8
0	0	0	0	

In order to make the sequence, we have used 8 states of the 4 binaries. But there are actually 2^4 states, or 16. Therefore the counter does not use 8. We will call these "unused states," and list them here:

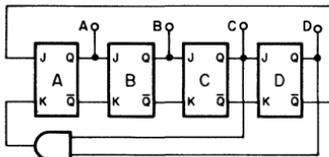
UNUSED STATES

A	B	C	D
0	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	0	0	1
0	1	0	1
1	1	0	1
1	0	1	1

Now to see how a sub-loop is set up, let us assume that the counter is at 1100 (3), when transient noise causes it to jump to the unused state 1011. From there, the counter proceeds to the next state, which is 0101 (keep in mind that a twisted ring counter sends the complement of the last binary output up to the first binary, and passes the interior bits along). 0101 is also an unused state. Next it goes to 1010, still another unused state. Then it goes back to 0101 again, and continues to oscillate back and forth between the two.

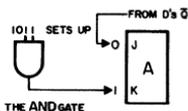
The Solution

The way to avoid this is by hooking up an external AND gate, as shown below, which automatically brings the counter back to a used state.



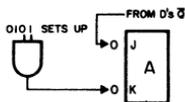
Let us follow through what happens with the AND gate in place after the counter has jumped to the first unused state, 1011.

The AND gate sees two 1's on its inputs, and therefore feeds a 1 into the K terminal of the A binary. The \bar{Q} output of the D binary is a 0, hence there is a 0 in the J terminal of the A binary. Therefore the next state of the counter is 0101.

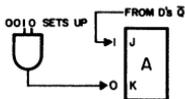


on the A binary, which makes
the next state of the counter: 0101

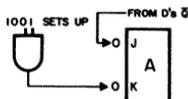
Following through in this manner, we see the following sequence:



on the A binary, which makes
the next state of the counter: 0010



on the A binary, which makes
the next state of the counter: 1001



on the A binary, which makes
the next state of the counter: 1100

1100 is a used state -- in fact, it is the number 3, the original jumping off place (this doesn't always happen, however). Hence we are back on the track again. The next count will be 1110, or 4, etc.

The reader can, by inspection, prove that the presence of the AND gate does not alter the count sequence when it is correct, that is, when it is proceeding through the used states.

Formulas for number of inputs to AND gate

In the example above, there were two inputs to the AND gate. The number of inputs, however, varies with the number of binaries in the counter. For a twisted ring counter, use the following formula:

$$\text{No. of inputs} = \text{next integer above } \frac{N}{3}$$

where N is the number of binaries

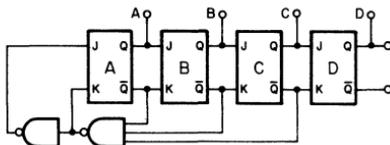
Thus, in our example, N was 4, $\frac{N}{3}$, is 1.333, and the next higher integer is 2. The AND gate needed 2 inputs. These inputs are always taken off the Q terminals of the least significant bits (LSB's) of the counter: the last 2 LSB's, or the last 3, or whatever.

For a standard ring counter (one that gives a count of N for N binaries), the principal is the same, but the inputs are taken from all the Q terminals except the last one. Thus the formula for the number of inputs in the case of the standard ring counter is:

$$\text{No. of inputs} = N - 1$$

where N is the number of binaries

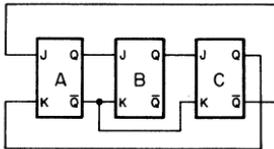
Here is a self-correcting standard ring counter:



A note on some unusual self-correcting twisted ring counters

Twisted ring counters, as mentioned above, normally give a 2N count for N binaries. It is possible, however, to make them give a 2N-1 or odd count. As shown in the

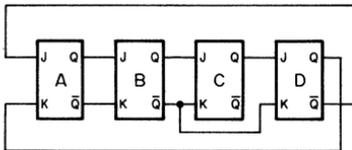
diagrams below, the 3, 4, and 5-bit counters (5, 7 and 9 counts) happen to be self-correcting without additional gating.



3 Bit Twisted Ring Self-Correcting -
5 Output States ($2N-1$)

TRUTH TABLE

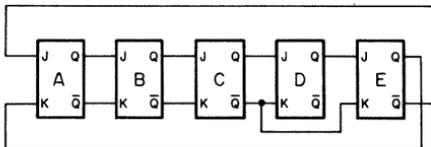
	A	B	C
1	0	0	0
2	1	0	0
3	1	1	0
4	1	1	1
5	0	1	1
	0	0	0



4 Bit Twisted Ring Self-Correcting -
7 Output States ($2N-1$)

TRUTH TABLE

	A	B	C	D
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1
	0	0	0	0

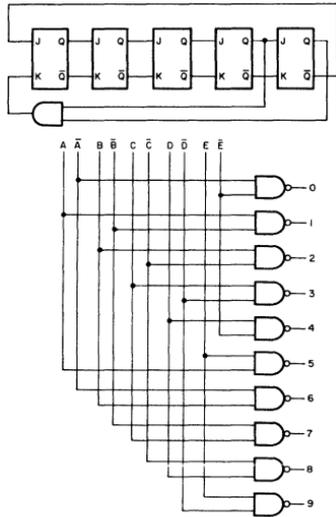


5 Bit Twisted Ring Self-Correcting -
9 Output States ($2N-1$)

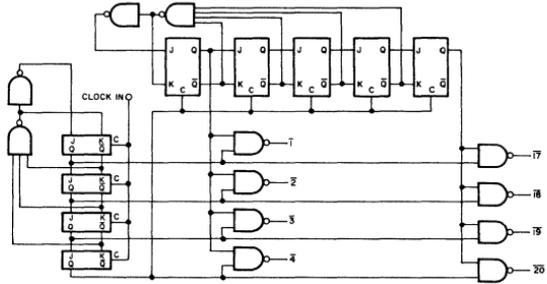
TRUTH TABLE

	A	B	C	D	E
0	0	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
1	1	1	0	0	0
1	1	1	1	0	0
1	1	1	1	1	0
0	1	1	1	1	1
0	0	1	1	1	1
0	0	0	1	1	1
0	0	0	0	1	1
0	0	0	0	0	0

Typical application using ring counters.



Decimal self correcting ring counter.



20 Channel Commutator.



APPLICATIONS MEMO

321 DUAL J-K BINARY APPLICATIONS

Because of its common clock and reset inputs, the 321 Dual J-K Binary Element requires special attention in certain applications where well established interconnection patterns can no longer be used. This memo presents typical systems applications of the 321 which are intended to be used as guide lines for future designs. Systems applications covered are: Ripple, Synchronous, Up-Down and Ring type counters as well as Shift Registers.

1. Ripple Counters

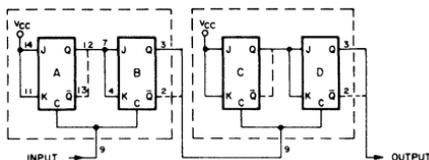


Figure 1. 321 Implementation of a Ripple Type Binary Counter

NOTE: Connections shown in plain line on Figure 1, are for straight binary up-counting, connections shown in dotted lines are for binary down-counting.

Figure 2 represents a ripple type Decade Counter, complete with parallel entry data strobing.

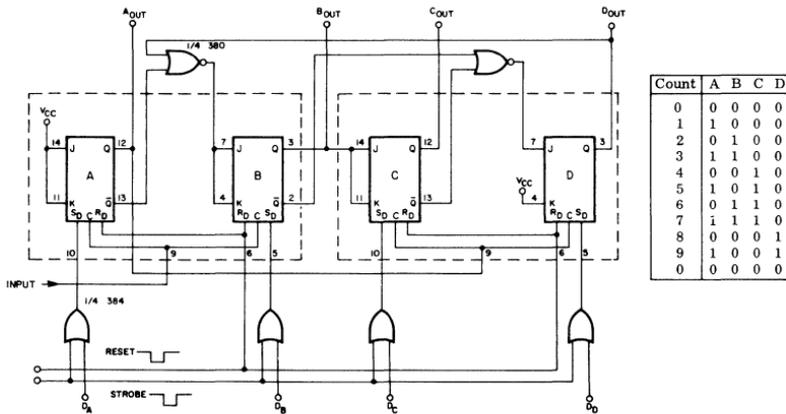
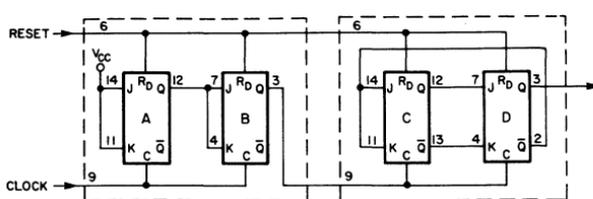


Figure 2. Ripple Type Decade Counter with Parallel Entry Data Strobing

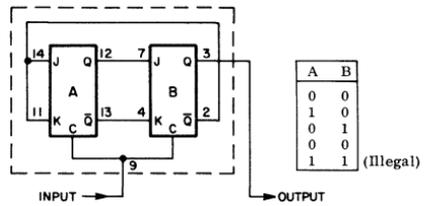


Count	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
0	0	0	0	0

Figure 3. Divide By 12 Ripple Counter

2. Synchronous Counters

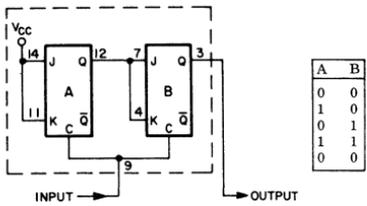
Figures 4 through 10 represent divide by 3 through divide by 10 counters implemented with 321 Dual J-K Binary Element in the synchronous mode.



A	B
0	0
1	0
0	1
0	0
1	1

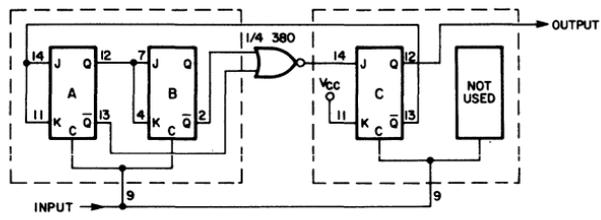
(Illegal)

Figure 4. 3 Count



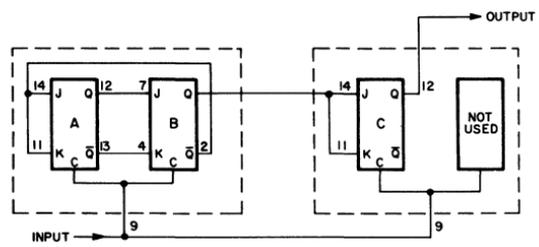
A	B
0	0
1	0
0	1
1	1
0	0

Figure 5. 4 Count



A	B	C
0	0	0
1	0	0
0	1	0
1	1	0
0	0	1
0	0	0

Figure 6. 5 Count



A	B	C
0	0	0
1	0	0
0	1	0
0	0	1
1	0	1
0	1	1
0	0	0

Figure 7. 6 Count

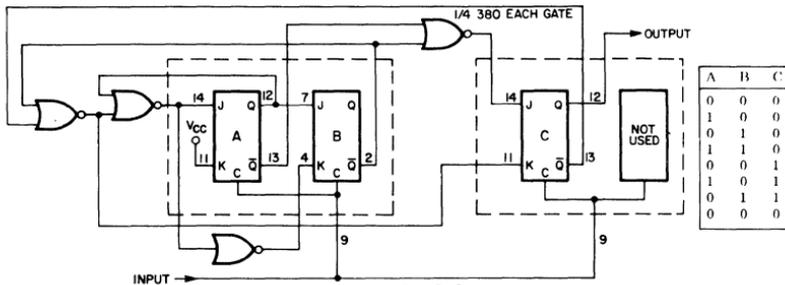


Figure 8. 7 Count

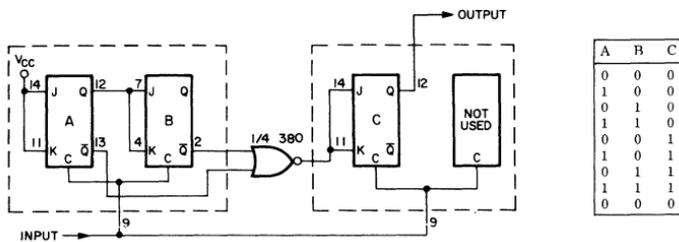


Figure 9. 8 Count

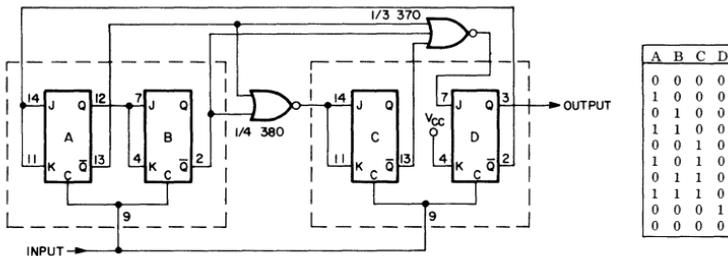


Figure 10. 9 Count

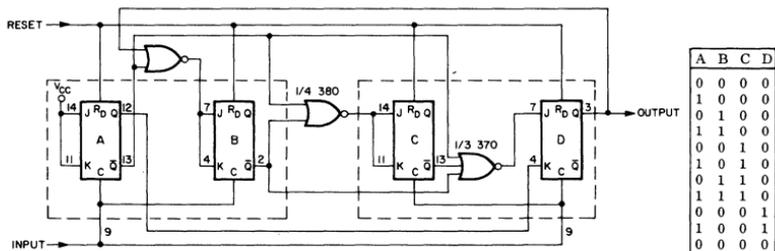


Figure 11. 10 Count

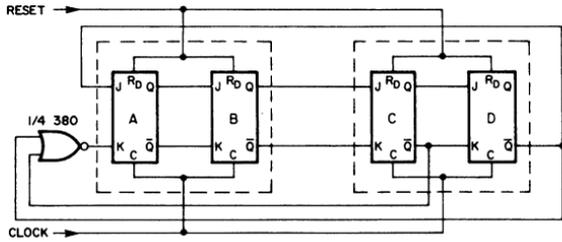


Figure 15. 4-Bit Self-Correcting Twisted Ring Counter

NOTE: Truth Table same as in Figure 14.

5. Shift Registers

Two types of shift registers are shown here: a Standard Gated Shift Register (Figure 16) and a Left-Right Shift Register (Figure 17).

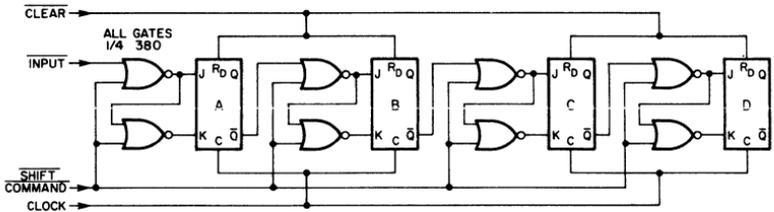


Figure 16. Gated Shift Register

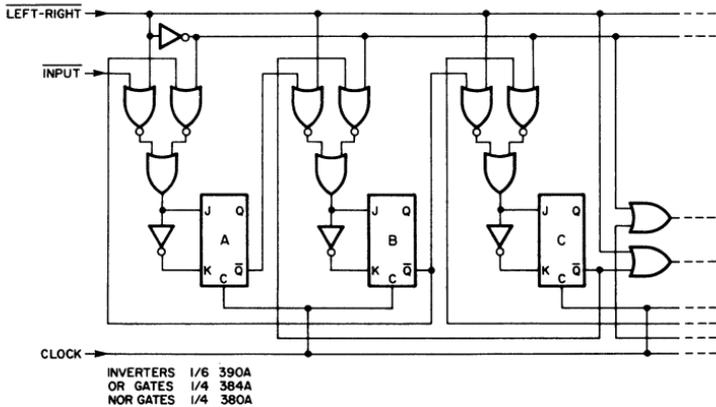


Figure 17. Left-Right Shift Register

6. Mixed Implementation

Figure 18 shows a 10 count system implemented with 321 and 322 binaries. Note reduction in number of circuits achieved by mixing binary types.

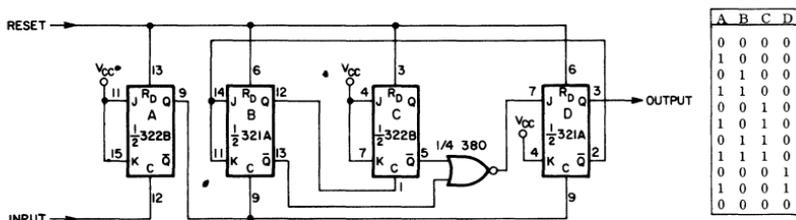


Figure 18. 10 Count Mixed 321/322 Implementation

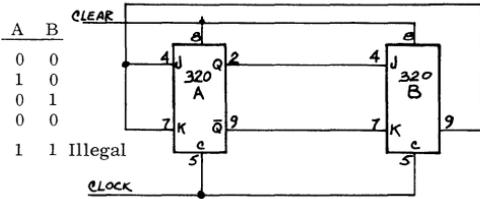


APPLICATIONS MEMO

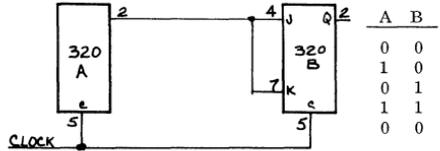
W. T. Booth

UTILOGIC COUNTERS

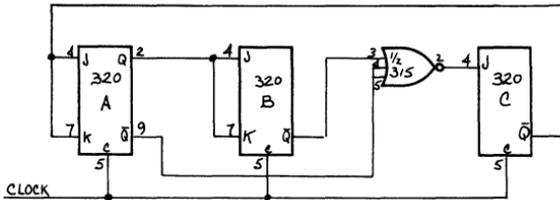
This memo shows 8 synchronous counters for counts from 3 to 10 inclusively. All use the familiar BCD weighting 1-2-4-8.



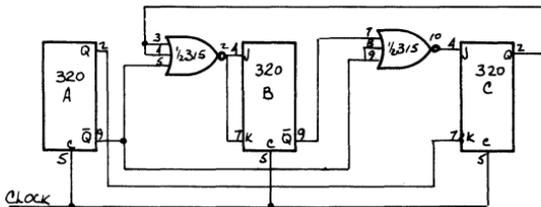
3 COUNT



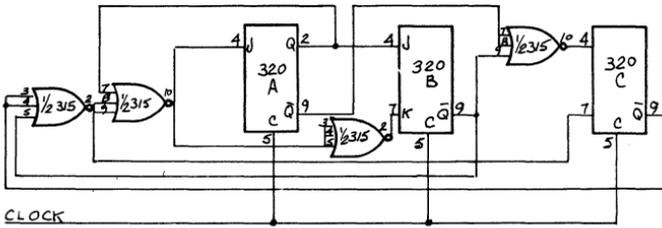
4 COUNT



5 COUNT

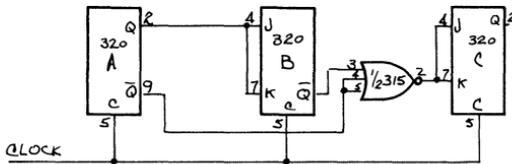


6 COUNT



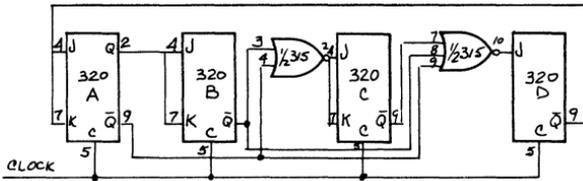
A	B	C
0	0	0
1	0	0
0	1	0
1	1	0
0	0	1
1	0	1
0	1	1
0	0	0

7 COUNT



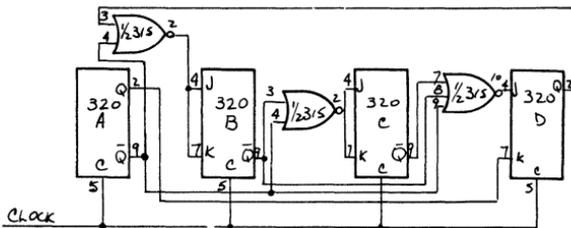
A	B	C
0	0	0
1	0	0
0	1	0
1	1	0
0	0	1
1	0	1
0	1	1
1	1	1
0	0	0

8 COUNT



A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
0	0	0	0

9 COUNT



A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1
0	0	0	0

10 COUNT



APPLICATIONS MEMO

Joe Echer

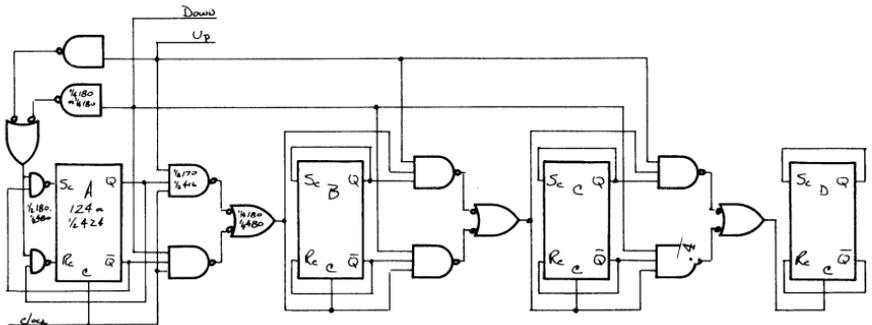
UP-DOWN BINARY COUNTERS

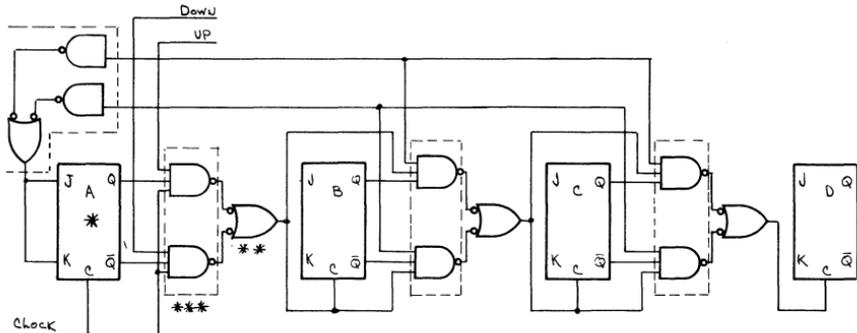
Up-down Binary counters can be implemented using synchronous or ripple techniques. Synchronous up-down counting has two undesirable features; 1) clock loading becomes excessive for counters of more than a few bits, 2) the gating structure for a flip-flop input is a function of all lower order bits in the counter.

Up-down ripple counters have neither of these disadvantages. However, simple up-down ripple counters will give incorrect counts under some conditions when control is changed from up to down or down to up. One solution to this problem requires external capacitors; this solution has critical thresholds and high frequency limitations.

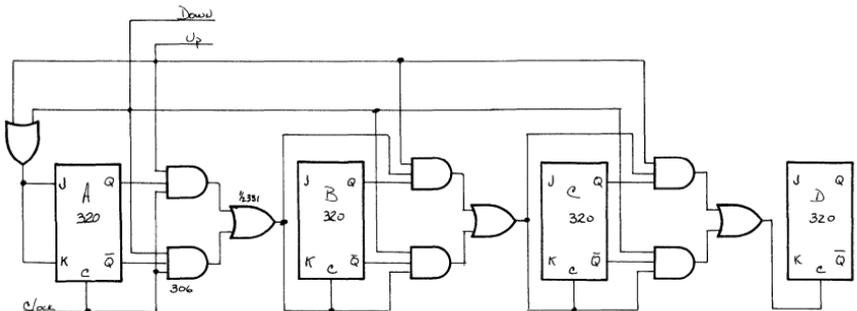
The solution shown in this memo uses a gating structure which is controlled by the clock. Whenever the clock line is low, all flip-flop clock inputs are unconditionally low. Changing the control lines from up to down, or down to up, has no effect on the state of the flip-flops when the clock line is low.

Three diagrams are attached which show how this type of counter can be implemented with SIGNETICS' Integrated Circuits.





* 8822, 8826, 322, 620, or 125 ** $\frac{1}{4}$ 8880, 8480, 180 or 670
 *** $\frac{2}{3}$ 8870, 3470, 170 or 670



UP	DOWN	RESPONSE
0	0	No Count
0	1	Count Down
1	0	Count Up
1	1	Forbidden

NOTE:

1. The levels of the Up-Down lines should not be changed when the clock input line is high.
2. All unused flip-flop inputs should be tied up or down as appropriate: J, K, R_D, and S_D high; J*, K*, P_j and P_k low.



APPLICATIONS MEMO

THE USE OF 9'S COMPLEMENT TO PROGRAM DECADE COUNTERS

Some problems have arisen in using 9's complement thumbwheel switches to program data into 8280's for a variable modulus type of operation. This memo is an attempt to clarify the use of 9's complement switches in this application.

The 9's complement of a number, N_c , is simply the number n subtracted from 9, or $N_c = 9 - n$. When the 8280 is used as a single stage variable modulus counter, as in Figure 1, it is never allowed to ripple through from a 9's condition to all zeros, or "overflow." If more than one stage is cascaded for a higher modulus operation, the last or most significant stage is never allowed to "overflow."

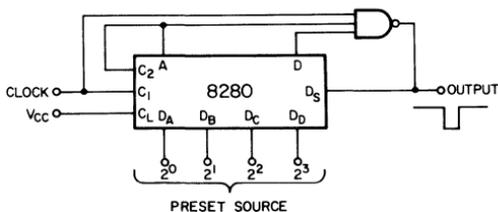


Figure 1

The clock falls and the counter enters the 9's condition ($A = 1, B = 0, C = 0$ and $D = 1$). This 1 0 0 1 condition is detected and (on the next leading edge of the clock pulse) the modulus data is strobed into the counter which has been determined by the setting of the thumbwheel switches. If a modulus of 4 is desired, the 9's complement of 4 (which is 5) is strobed into the counter, leaving only 4 states for the counter to assume, these being 6, 7, 8 and 9; then before 9 is again detected, the process starts over.

The problem that has arisen is how to connect the 9's complement switches to the counter data inputs. The 9's complement switch has its outputs connected to the common terminal of the switch for any given code. For example, if 3 is showing on the dial of the switch, a BCD code of 6 appears at the output (B and C connected to the common and A and D floating). This 6 must be presented to the data inputs on the 8280 as A and D = 0 or GND, and B and C = 1 or V_{CC} . Therefore, the common terminal of the switch would be connected to V_{CC} . However, the A and D switch outputs, which are floating, must be presented as zeros to the 8280. An unterminated multiple emitter input on TTL type circuitry appears as a "1"; therefore, a 220 ohm pulldown resistor must be connected from the floating input to GND, to ensure a "0" input. The value of this resistor cannot be increased appreciably before the "0" level noise immunity is seriously affected. When the input code is changed so as to cause the A or D input to be "1", the 220 ohm resistor is now between GND and V_{CC} , causing additional current drain on the V_{CC} supply. Since any input could be floating, according to the input code, resistors must be tied on all the inputs. If a code of 2 is present (preset of 7), three resistors are between V_{CC} and GND. For a V_{CC} supply of 5 volts, the extra current drain for only one decade is 70mA.

This situation can be overcome by connecting the switch common to GND and adding 10k pullup resistors to ensure "1" levels from each switch output to V_{CC} . The inverse of the code is now generated and must be inverted by gates before the data is presented to the 8280. Although the additional current drain problem is solved, we have added a quad two input gate package for every decade. The 220 ohm pulldown resistors required 350mW per decade vs. 88mW with the 10k pullup resistors and an 8880 gate package. (Preset code of 7 assumed for the above calculations.) This is a 75% reduction in power.

There are switches available with outputs of both the 9's complement and the inverted 9's complement, such as the Digitran No. 327⁽¹⁾. By connecting the common to GND and using $\bar{1}$, $\bar{2}$, $\bar{4}$ and $\bar{8}$ outputs along with 10k pull-up resistors, the switch outputs can go directly to the data inputs of the 8280, and the inverting gates are no longer required. By using these techniques, current requirements are reduced to 8mW per decade (preset code of 7 being assumed).

(1) The Digitran Company, 855 South Arroyo Parkway, Pasadena, California 91105

If the user is able to obtain a switch with true and complemented outputs and separate commons for each, the true common can be connected to V_{CC} and the complement common to GND. The outputs are then paralleled. For example: 1 to $\bar{1}$, 2 to $\bar{2}$, etc. No external resistors are now required. The switch must have a break-before-make type of action so as not to short the V_{CC} supply to GND while changing the switch position. If this is not the case, a single 1k resistor can be connected from the true common to V_{CC} .

If the designer has some logic source of BCD or complemented BCD that he wishes to convert to 9's complement, Figures 2 and 3 show the logic for accomplishing this.

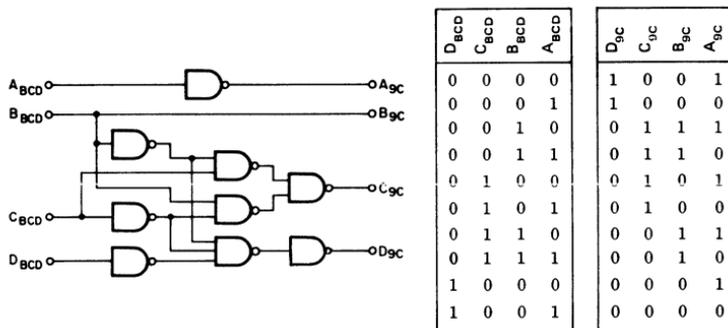
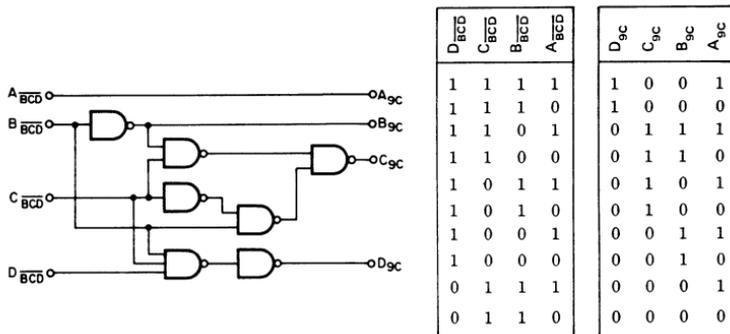


Figure 2. BCD to 9's Complement



Complemented BCD to 9's Complement

Most of the common problems and their solutions have been presented on the use of the 9's complement code and switches. Hopefully, these suggestions will help the designer to a better understanding of variable modulus counter design and programming.



APPLICATIONS MEMO

APPLICATION OF 8-BIT MEMORY ELEMENT, N1283L *

1. Introduction:

Logic arrays are a natural development in the improvement of integrated circuits. The advantages offered by the integrated circuit are provided by the integrated logic array to an even higher degree: greater density, fewer external connections, greater reliability, and lower cost per logic element. There is also a problem inherent in the concept of the logic array: how to configure a network of logic elements with a small number of terminals (10 to a TO-5 pack) to be sufficiently flexible to serve a broad class of uses in digital design. The Signetics N1283L 8-bit memory element has been designed to answer this problem.

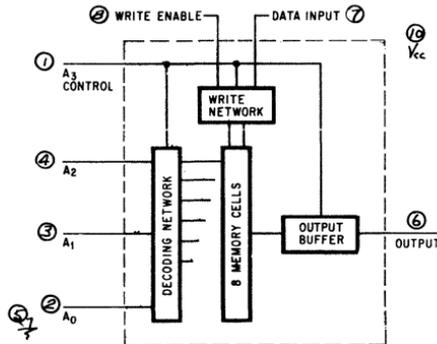


Figure 1. Block Diagram of 8-Bit Memory Element, N1283L

Figure 1 is a block diagram and Figure 2 is a schematic of the N1283L. It consists of 8 flip-flops with address decoding logic and an output buffer packaged in a TO-5 can. A 3-bit address on leads 2, 3, and 4 selects one of the eight flip-flops for reading or writing as determined by the status of the Write Enable input, lead 8. Input data are provided to the selected flip-flop on lead 7; output data appear on lead 6. Lead 1 is an additional selection control lead which serves several functions. When this lead is true, high level, it switches the supply voltage to the input and output circuits permitting writing or reading. When the input is false, low level, these functions are inhibited and power is provided only to the flip-flop memory elements themselves. This permits reduction of the unit's power dissipation to 45% of that expended when the control is always true. The control

* Also available in the "A" Dual In-Line package

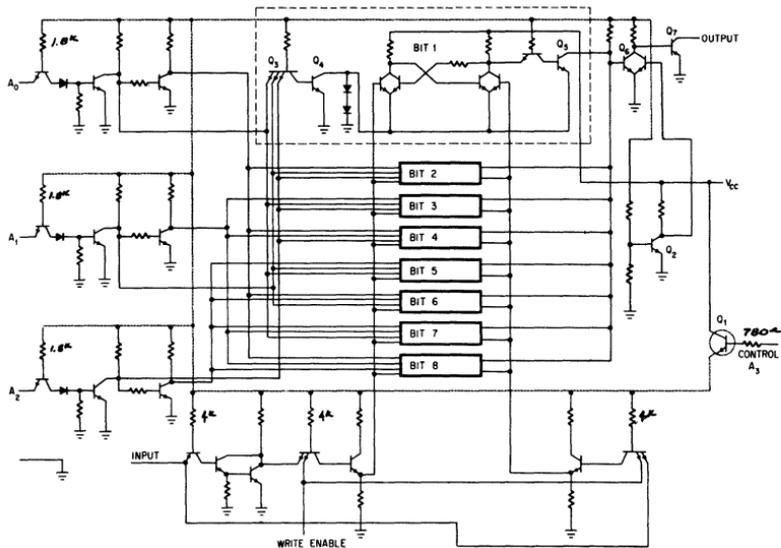


Figure 2. Schematic Diagram of N1283L

is also an extension of the address selection logic which permits selection of one out of many 8-bit elements for reading and writing. For reading, the outputs of several 8-bit elements may be tied together provided only one will be selected (lead 1 = T) at any one time.

The flexible addressing scheme, non-destructive read-out, buffered output and high speed (90 nsec for writing and 60 nsec for reading) permit the use of the 8-bit memory elements in a variety of applications. These include: scratchpad memory, buffers, pushdown stacks, ripple counters, shift registers, associative memories, character translators, and others. Following, is a discussion of some of the applications.

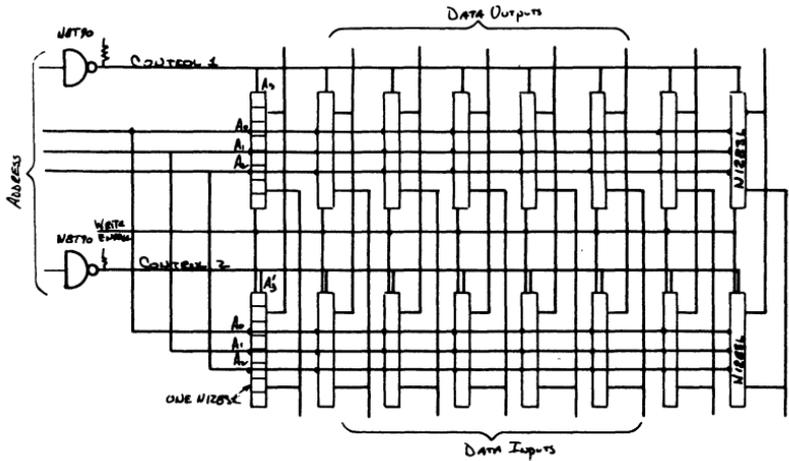


Figure 3. Scratch Pad Memory - 16 Words at 1 Byte Each

2. Scratchpad Memory

In many areas of computer design and elsewhere, it is desirable to have a high speed random access memory. Reference 1 discusses a number of these applications. Figure 3 illustrates a typical scratchpad memory organization.

Each N1283L unit provides one bit for each of eight words. The number of bits in a word is determined by the number of elements in a row of Figure 3. Therefore, word length is completely flexible. The number of words can be increased by multiples of 8 through the addition of rows. A_0 - A_3 are used to address a given word. A_0 - A_2 select a given word of each row; A_3 , driven by an n -term AND gate for a 2^{n+3} word memory, selects the appropriate row. The data input and output lines would normally connect to a common external data register. Note that this arrangement of the elements permits word transfer in bit parallel form.

The N1283L memory element is well-suited to scratchpad memory applications. A complete read-write cycle takes only 150 nsec which is about 6 times as fast as most core memories. In addition, its NDRO operation permits the cycle time to be reduced to 90 nsec for write-only and 60 nsec for read-only operations, which are sufficient in most cases. These high speeds permit the scratchpad cycle times to be masked by the core memory cycle time, permitting such functions as memory protection, memory mapping, and rapid interrupt recovery with little or no additional delay. The high current output buffer facilitates interfacing with

external logic. As many as 32 outputs can be tied together to form a 256 word memory. The node will carry the data bit read from that N1283L whose Control is true.

3. High Speed Buffer

An elaboration of the scratchpad configuration is the first-in-first-out memory, which can be used as a high speed buffer. The buffer can transfer data asynchronously between high speed devices such as core memories, discs, and magnetic tapes. Figure 4 illustrates the configuration.

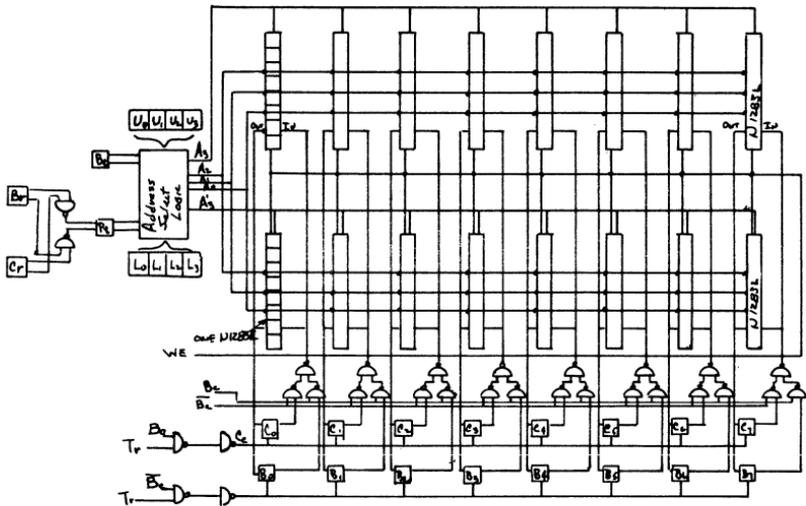


Figure 4. High Speed Buffer

The arrangement shown permits data to be transferred in either direction between two devices, B and C, e.g., a magnetic core memory and a disc. B_0 - B_7 is a one byte (8-bit) flip-flop register associated with a device B. C_0 - C_7 is a one byte register associated with device C. The buffer itself, consisting of 16 8-bit memory elements arranged as shown, can store zero to 16 bytes of data. Of course, the buffer dimensions shown are arbitrary.

L_0 - L_3 and U_0 - U_3 are 16 state binary counters which at any time designate the byte in buffer which is to be loaded and the byte which is to be unloaded. L_0 - L_3

is incremented by 1 after each byte is loaded into buffer. U_0-U_3 is incremented by 1 after each byte is unloaded. The difference between the contents of the two counters indicates the number of bytes in buffer. An extra flip-flop can distinguish between the empty buffer and full buffer states.

Flip-flop Bc tells whether the transfer is to be from B to C or C to B. Flip-flop Br tells when the B_0-B_7 register is ready either to transmit a byte of data to the buffer or to receive a byte from the buffer. Cr performs a similar function for C_0-C_7 . Pt is a priority toggle (cross-coupled NAND gates) which determines whether B_0-B_7 or C_0-C_7 is to be processed next. Pt is set by $\text{Br} \cdot \overline{\text{Cr}}$ and reset by $\overline{\text{Br}} \cdot \text{Cr}$; hence Pt means that B_0-B_7 should be processed (loaded or unloaded), and $\overline{\text{Pt}}$ means that C_0-C_7 should be. The purpose in using a toggle is to resolve races between Br and Cr turning on.

Consider the case of transferring data from B to C. At the outset, L_0-L_3 and U_0-U_3 are both zero, indicating the buffer is empty and that address zero will be first to be loaded. Bc gates the B_0-B_7 outputs onto the data input lines. As soon as device B places a byte of data into B_0-B_7 , Br turns on. $\text{Br} \cdot \overline{\text{Cr}}$ turns on toggle Pt; Pt · Bc causes the address line, A_0-A_3 , A_3' to be determined by L_0-L_3 . A_0-A_2 follow L_0-L_2 . A_3 and A_3' , which determine the appropriate half of buffer, follow L_3 and L_3 respectively at write time, Tw. The turning on of Br initiates a timing sequence (controlled by circuitry not shown) which develops the writing pulse, Tw. Tw is gated with L_3 to produce A_3 . It is gated with $\overline{L_3}$ to produce A_3' . Thus, the byte in B_0-B_7 is written into the addressed byte of buffer at Tw time. L_0-L_3 is then incremented and Br turned off.

Transfer of data out of the buffer to device C follows a similar sequence. When C is ready to accept the byte, Cr is turned on. $\text{Cr} \cdot \overline{\text{Br}}$ turns off the toggle causing A_0-A_3 , A_3' to be determined by U_0-U_3 . The timing sequence is also initiated; however, instead of producing a write pulse, it produces a read pulse, Tr, which is gated with $\overline{\text{Bc}}$ to produce a pulse on Cc. This clock pulse strobes the data output into C_0-C_7 . Finally, U_0-U_2 is incremented and Cr turned off.

Devices B and C can be completely asynchronous provided the buffer cycle time is less than half the shorter byte period of the two devices, B and C.

4. Push Down Stack

The buffer described in Section 3 is a first-in-first-out memory. It is sometimes useful to have a last-in-first-out memory or pushdown stack. If finds uses in list processing, processing of expressions in Polish notation, and reversal of data order. The configuration is like that of the scratchpad memory except that there is a single address register which is an up-down counter. This counter is incremented by one after each word is written; it is decremented by one before each such word is read.

5. Binary Ripple Counters

Eight-bit memory elements used as multiplexed binary ripple counters are useful in systems where only one counter is incremented (or read out) as any given time. The number of devices required to implement eight counters using this technique is considerably less than if conventional flip-flops were used.

The eight-bit memory elements (N1283L) implement multiplexed binary counters with the aid of a few additional components as shown in Figure 5. Each memory element provides one binary digit position for eight binary counters, hence the length of the counters is determined by the number of memory elements used. Switches S_1 , S_2 , and S_3 select the desired counter (1 of 8), and S_4 is a guard switch that prevents false counts during counter select switching. S_4 must be in the ground position during counter select switching, and in the V_{CC} position when counting. Switches S_1 through S_4 may be replaced with gates or flip-flops for fully electronic operation. Counting rates of several MHz have been obtained.

6. Shift Registers

The eight-bit memory elements can be organized to operate in a way resembling a set of circulating registers, Figure 6. Actually, the registers do not shift but are scanned. As the address registers count up, corresponding bits of all registers are selected in sequence. The selected bits can be read and changed.

The registers are conveniently mechanized in 8-bit multiples; however, other lengths can be achieved by sacrificing some of the bits in a unit. The number of registers is arbitrary, depending only upon the number of units used.

7. The Associative Memory

An interesting organization can be achieved by combining a set of shift registers, as described in Section 6, with a scratchpad memory, as in Section 2, both implemented from 8-bit memory elements. Figure 7 shows an associative memory formed in this way.

The associative memory, or content addressable memory (CAM), does not use addresses or addressing mechanism to locate a word. Instead, part of the contents of each stored word, the key, is used to identify a desired record. An external key is transmitted to all word locations; there, comparisons are made simultaneously between the stored and transmitted keys. Assuming that only one word stores

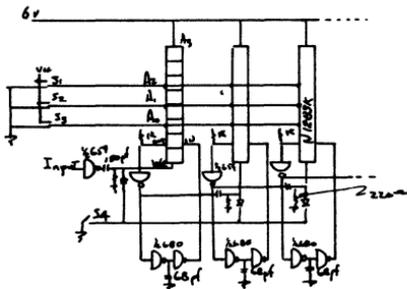


Figure 5. Multiplexed Ripple Counter

a matching key, that word is tagged for writing or reading. There are many variations and elaborations of this technique as described in references 2 - 4. The system described here is a relatively simple version. It can be used as a memory map^{1, 5}, as a virtual memory⁶, or in a number of the applications described in the literature. See reference 4 for a more extensive bibliography. In general, the associative memory is useful in circumstances where it is difficult to keep track of the locations in which records are stored so that a serial search would be required if a random access memory were used.

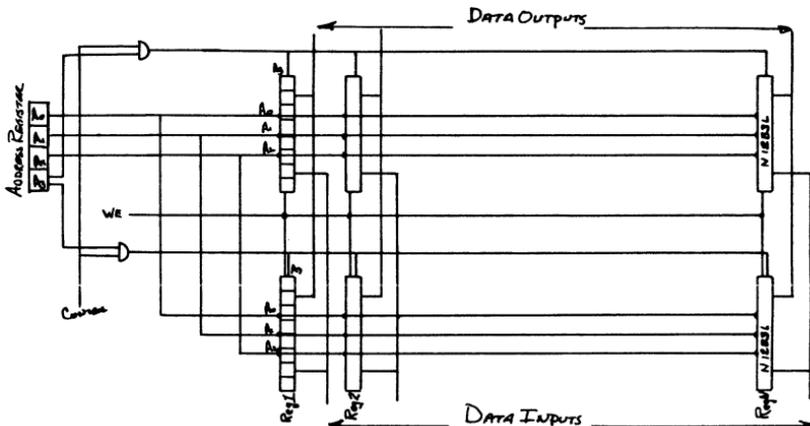


Figure 6. Shift Register

The left half of Figure 7 shows a set of n shift registers. Each register contains one or more keys which can serve as the basis of a search. The D register is an external shift register which holds the search key. It is compared simultaneously with the corresponding field of all the other shift registers. This is accomplished bit serially but in all words at once by the comparison networks, C_1-C_n , associated with the n words of memory. If the comparison is satisfied, in word i , then a flip-flop in C_i is turned on.

The address register counts through a specified range selecting the appropriate field of all registers for comparison against the search key in D . Arbitrary fields of the key register can be chosen to represent the key by causing the address register to count through an appropriate sequence. The key can even consist of non-contiguous fields. This is useful in certain information retrieval applications. For instance suppose each stored key consists of a number of separate attribute indicators, e.g., part number, serial number, price, size, color, and weight. Then any combination of these indicators could be used to identify an item.

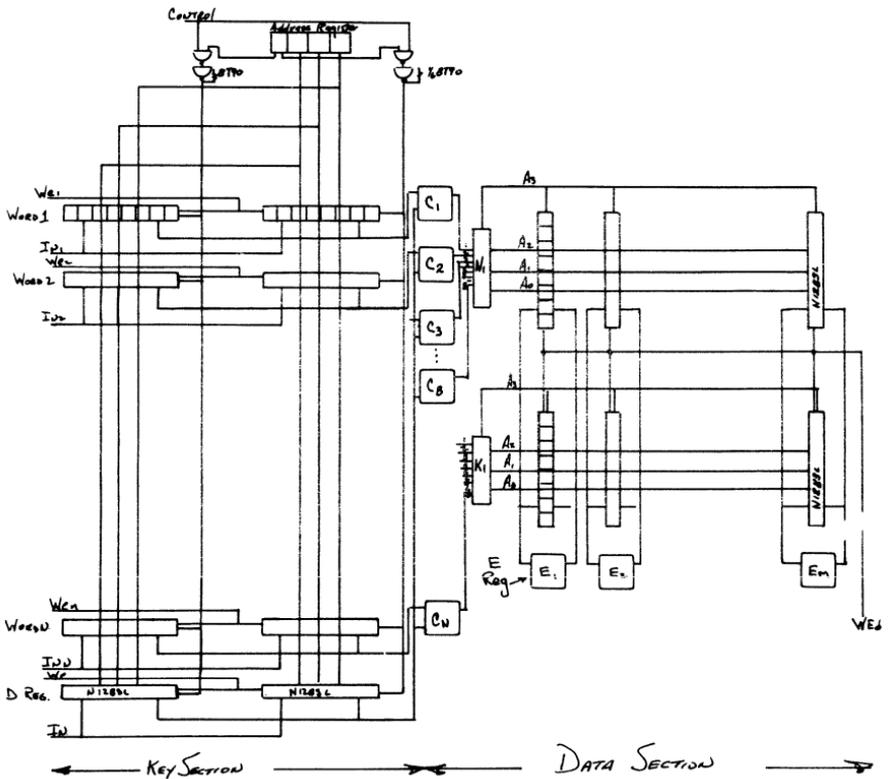


Figure 7. Associative Memory

The right half of Figure 7 shows the Data Section consisting of n words of scratchpad memory, each associated with a key register on the left. When one of the n select flip-flops has been turned on by the comparison networks, that select flip-flop is used to designate the scratchpad word for reading or writing. Addressing a word in the scratchpad section is accomplished by the addressing networks, $N_1 - N_k$. Each N_i network has 8 inputs from comparison networks and four output address lines, $A_0 - A_3$. The equations for the N_1 network are:

$$A_0 = C2 + C4 + C6 + C8$$

$$A_1 = C3 + C4 + C7 + C8$$

$$A_2 = C5 + C6 + C7 + C8$$

$$A_3 = A_0 + A_1 + A_2 + C1$$

Once a word has been selected, it can be read or written by means of the Write Enable signal, W_{ed} . Information is written into and read from the Data Section by means of the external flip-flop data register, $E1 - E_m$. Notice that unlike comparison transfer with the Key Section, the data transfers with the Data Section are done in bit parallel.

8. Usage Rules

Supply Voltage

The N1283L is designed for use with a 4 volt power supply. When used in systems which operate from a higher supply level, it is recommended that a separate power supply be utilized.

A_3 Control

The circuit shown in Figure 8 is recommended for driving the A_3 input. It utilizes the 8T90 interface unit and will ensure adequate drive while maintaining low power consumption levels.

Timing Requirements

During writing operations, the address should be selected at least 45 nsec prior to raising the Write Enable input to "1" to preclude any possibility of writing into the wrong memory location. The address selection should be retained for 20 nsec after Write Enable has gone to "0". Data should precede Write Enable by at least 25 ns and must be held for at least 5 ns after the removal of Write Enable. The Write Enable pulse should be at least 30 nsec wide (2.3 volts).

Output Load Resistor

The output load resistor should be chosen to maintain an adequate "1" margin at the input of any driven gate; e.g., 2.6 volt level in 8000-series systems; 3.3 volt level in Utilogic systems. The current through the load resistor will be the sum of all of "1" output current of the N1283L's connected together and the "1" input

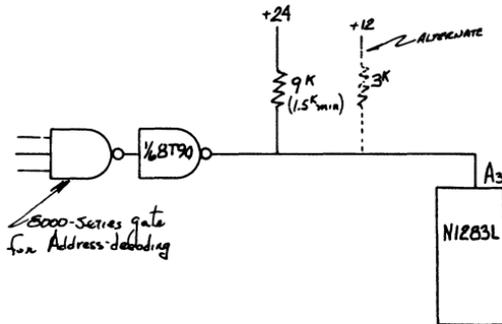


Figure 8. A₃ Drive Using 8T90 Interface Element

current of all driven gates. The resistor may be returned to +5 in 8000-series systems. The minimum resistor value which may be connected to 5 volts is 300 ohms.

Loading Rules

The inputs of the N1283L are 3 8000-series loads, 1.4 100-series loads, 4 400-series loads, or 1.2 Utilogic sink loads. In all cases, the supply voltage for the N1283L is 4.0 volts. Fan out is 50 8000-series loads, 22 100-series loads, 66 400-series loads, or 20 Utilogic loads.

9. References

1. Potter, Mendelson and Sirkin, "Integrated Scratch Pads Sire New Generation of Computers," Electronics, April 4, 1966.
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5. C. T. Gibson, "Time-Sharing in the IBM System/360: Model 67", Proc. Spring Joint Computer Conference, 1966.
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APPLICATIONS MEMO

SYNCHRONOUS UP/DOWN COUNTERS

8284 Binary Hexadecimal

8285 BCD Decade

INTRODUCTION

The 8284 Hexadecimal (4-bit binary) Synchronous UP/DOWN Counter has sixteen unique 4-bit output codes which occur synchronously. The 8285 is a BCD Decade Synchronous UP/DOWN Counter and has ten unique binary-coded-decimal (8421) synchronous output states. The input/output functions of the 8284 and 8285 permit cascading of ten stages at the guaranteed operating frequency of 20 MHz.

The operation and applications of these counters are discussed in detail. To help the system designer use the 8284 and 8285 more effectively, a section has been included on design precautions.

One of the major advantages of synchronous counters over ripple or asynchronous counters is that all output change at the same time, eliminating false output transition codes.

DEVICE DESCRIPTION

Operation

The 8284 and 8285 are synchronous UP/DOWN counters with reset to "0" and set to 15 (8284) or 9 (8285) asynchronous entry clock override (refer to Figure 1). Carry-Out and propagation of data occur synchronously with the falling edge of the clock input. The Q outputs of all four binaries are available, together with \overline{Q}_4 and Carry-Out.

The Count-Enable input goes to an AND gate which is tied to the toggle enable input of each binary element. This toggle enable AND gate also has the Carry-In, Set and Reset inputs connected to it. As shown in Figure 1, if one of these inputs are "0", the counter is disabled and will not count.

The Carry-In input, besides being tied to the toggle enable AND gate, also enables the Carry-Out output. The Count-Enable input has no effect on the Carry-Out. Therefore,

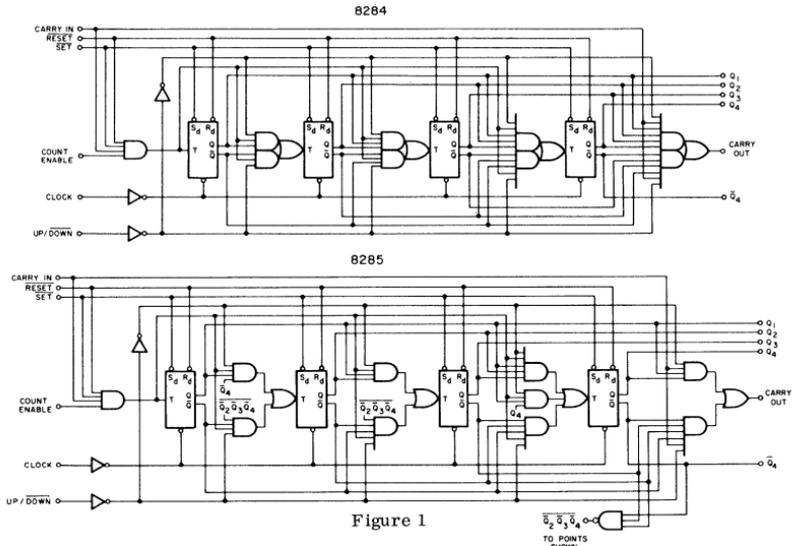


Figure 1

Table 1
 8284 Binary Synchronous Up/Down Counter
 8285 BCD Synchronous Up/Down Counter

MODE OF OPERATION

	Set	Reset	Carry In	Count Enable	Up/Down	Function
A. Asynchronous						
8284 Only	1	0	X	X	X	"0" (0 0 0 0)
8285 Only	0	1	X	X	X	"15" (1 1 1 1)
8285 Only	0	1	X	X	X	"9" (1 0 0 1)
B. Synchronous						
	1	1	0	X	X	Hold *
	1	1	X	0	X	Hold *
	1	1	1	1	0	"Down" Count *
	1	1	1	1	1	"Up" Count *

*Function is synchronous with NEGATIVE going transition of the Clock pin.
 X = don't care.

$$\text{CARRY OUT}_{8284} = \text{Carry In} (Q_1 Q_2 Q_3 Q_4 \text{ UP} \cdot \overline{Q_1} \overline{Q_2} \overline{Q_3} \overline{Q_4} \overline{\text{UP}})$$

$$\text{CARRY OUT}_{8285} = \text{Carry In} (Q_1 Q_4 \text{ UP} \cdot \overline{Q_1} \overline{Q_2} \overline{Q_3} \overline{Q_4} \overline{\text{UP}})$$

the carry term can propagate through the counter while counting is inhibited by the Count-Enable ("0"). This input/output configuration makes it possible to cascade up to eleven stages of 8284's or 8285's with completely synchronous operation at 20 MHz.

For the 8284 Hexadecimal Counter, a binary coded fifteen ($Q_1 = Q_2 = Q_3 = Q_4 = "1"$) in the count up mode ($\text{UP}/\overline{\text{DOWN}} = "1"$ level) will generate a Carry-Out ($C_0 = "1"$ level) when Carry-In goes high. The 8285 BCD Decade Counter in the count up mode generates a Carry-Out for a binary coded nine ($Q_1 = Q_4 = "1"$, $Q_2 = Q_3 = "0"$) when the Carry-In input goes to a "1" logic level. In the count down mode ($\text{UP}/\overline{\text{DOWN}} = "0"$ level), both counters generate a Carry-Out when the Carry-In is a logic "1" level and a binary coded zero ($Q_1 = Q_2 = Q_3 = Q_4 = "0"$) is detected. The propagation delay from Carry-In going

Design Precautions

Certain precautions must be taken to ensure optimum system performance of MSI circuit designs using TTL techniques.

High frequency distribution techniques should be used for V_{CC} and GROUND. These techniques should include large ground planes to minimize DC offsets and provide an extremely low impedance path to reduce transient noise on the printed circuit boards. The V_{CC} power supply should be +5V, $\pm 5\%$ with R-F (1 GHz) bypassing.

The current spike produced by the totem-pole output structures during "0" to "1" switching transitions can cause MSI elements to malfunction if V_{CC} is not properly decoupled to GROUND. A ceramic disc capacitance of 2000 pF or more for each totem-pole structure should be connected between V_{CC} and GROUND in close proximity to the MSI device to provide proper bypassing. The six output and two internal totem-pole structures of the 8284 and 8285 require a $0.02\mu\text{F}$ ceramic disc capacitor V_{CC} bypass.

Electrically open inputs degrade the AC and DC noise immunity as well as the switching speed of an MSI circuit. All inputs must be connected to low impedance sources for optimum noise immunity and switching speed. Unused inputs should be tied to a driving source, V_{CC} or GROUND. Unused inputs may be tied directly to V_{CC} if the power supply voltage never exceeds 6.0V; otherwise, the input should be tied to V_{CC} through a resistor (1K Ω). More than one unused input may be tied to V_{CC} through the same resistor.

For the 8284 and 8285, Reset and Set should be connected to V_{CC} when unused. Count-Enable when unused should be connected to the Carry-In input or to V_{CC} . The Carry-In input for a single counter or the first in a series of cascaded counters can be used to inhibit counting ("0" logic level) by a gate or, when unused, should be tied to V_{CC} .

All rise and fall times (10% to 90%) should be less than 200 nsec for a pulse amplitude of 2.6V or greater (not to exceed 6.0V).

If interconnections between devices are longer than 8 inches, precautions should be taken to minimize line reflections and ringing. All inputs to the 8284 and 8285 counters are protected with diffused diode clamps. These diodes will limit negative excursions to -1V or less.

SYSTEM APPLICATIONS

Cascading Counters

Their unique input and output functions make possible the cascading of up to ten 8284 Hexadecimal and 8285 BCD Decade Counters while operating at their guaranteed maximum frequency of 20 MHz. Being able to cascade ten stages permits the designer to count to

2^{40} or 1,099,511,627,776 counts for the 8284 and to 10^{10} or 10,000,000,000 counts for the 8285. These total counts can be achieved in both the up and down count modes with completely synchronous output code transitions at 20 MHz. Further cascading past the eleventh stage is possible "if necessary" but the Carry-Out of the first stage (C_{O1}) would have to be buffered.

The following example is intended to clarify the interconnection scheme shown in Figure 2a. The example will show the cascading of ten 8285 BCD Decade Counters. The counters will be connected to take full advantage of the "anticipated-carry" capability to achieve 20 MHz synchronous UP/DOWN counter operation. This example will only show the count up mode:

Decade No. 1 has the Carry-In and Count-Enable inputs tied together. This input is used as the Count Enable (CE) for the entire ten stage counter. The Carry-In (C_I) to Carry-Out (C_O) propagation delay is typically 15 nsec (as shown in Figure 2b) and the typical propagation delay from the falling edge of the Clock (C_L) to C_O is 30 nsec (as shown in Figure 2c for the ninth and tenth clocking transition).

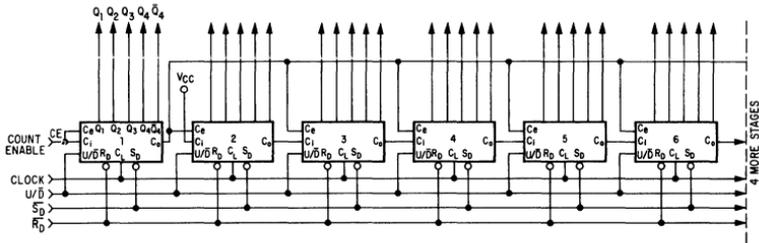


Figure 2a

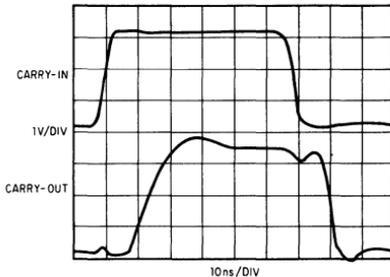


Figure 2b

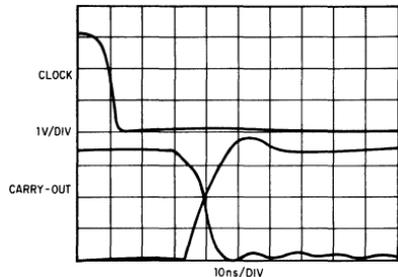


Figure 2c

The second decade (2) has the C_{i2} tied to V_{cc} . The C_{o2} is therefore always enabled. The C_{o1} of the first decade which is connected to the C_e of the other nine decades enables the second decade to count one count for every ten counts in the first decade. C_{o2} is allowed to ripple through all successive decades. The propagation delays are shown below:

For the

9 9 9 9 9 9 9 8 9 to 9 9 9 9 9 9 9 9 0 transition

C_L to $C_{o2} = 30 \text{ nsec} \times 1 \text{ decade} = 30 \text{ nsec}$

C_{i3} to $C_{o3} = 15 \text{ nsec} \times 8 \text{ decades} = 120 \text{ nsec}$

	-150 nsec	
10 more counts in the first decade at 20 MHz = 500 nsec		+500 nsec
		+350 nsec

The 500 nsec between Count-Enables for the second through tenth decade allows three times the delay required for the carry term to propagate through nine decades. If the designer has a requirement for more than ten stages (either BCD Decade or Hexadecimal) of synchronous UP/DOWN counters, it is possible to buffer the C_o of the first stage and drive the C_e inputs of 24 stages at the maximum operating frequency of 20 MHz. A 25 stage Hexadecimal Counter is able to store 2^{100} counts. It would take approximately $2 \cdot 10^{15}$ years at 20 MHz to overflow this counter. A ten stage Hexadecimal will take over fifteen hours to overflow at 20 MHz. Therefore, few requirements ever exceed ten stages.

1's Complement Generator

In the count down mode, the 8284 (Hexadecimal) generates the 2's complement (Table 2) of any negative count. The 2's complement permits addition of positive and negative binary numbers without code conversion of the negative number. However, if the 1's complement or the reciprocal of the positive binary number is desired, 2^0 (LSB) must be subtracted from the 2's complement number: -6 in 2's complement = 1 0 1 0

$$-2^0 \qquad \underline{-0 \ 0 \ 0 \ 1}$$

then: -6 in 1's complement = 1 0 0 1

where: $2(\bar{A}) - 2^0 = 1(\bar{A})$

To generate the 1's complement automatically in the normal counting sequence of a system using 8284's requires the addition of a single 8H70 (Triple 3-Input NAND Gate). As shown in Figure 3, the combined Carry-Out ($C_e \cdot C_i$) detects all zero crossings. The 1's complement has two states for zero, all 0's and all 1's. All outputs are Set ($\bar{S}_D = "0"$) to "1's" when all "0's" are detected in the count "DOWN" ($U/\bar{D} = "0"$) mode. Conversely,

all outputs are Reset ($\overline{R}_D = "0"$) to "0"s when all 1's are detected in the count "UP" ($U/\overline{D} = "1"$) mode. An example of the generated "1"s complement counting sequence is shown in Table 3.

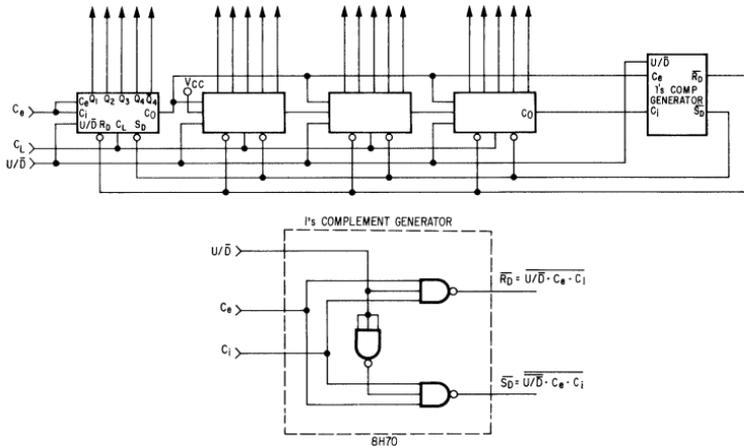


Figure 3

Table 3. "1" s COMPLEMENT COUNTING SEQUENCE

Clock	Decimal	Binary	$C_e \cdot C_i$	U/\overline{D}	S_D	R_D
0	+3	0 0 1 1	0	0	1	1
1	+2	0 0 1 0	0	0	1	1
2	+1	0 0 0 1	0	0	1	1
3		0 0 0 0	1	0	0	1
		1 1 1 1	0	0	1	1
4	-1	1 1 1 0	0	0	1	1
5	-2	1 1 0 1	0	0	1	1
6	-1	1 1 1 0	0	1	1	1
7		0 1 1 1	1	1	1	0
		0 0 0 0	0	1	1	1
8	+1	0 0 0 1	0	1	1	1

Magnitude and Sign Generator

The 1's and the 2's complement representations of negative numbers are insufficient for some applications. When decoding the outputs of 8285's for numeric readouts, it is desirable to produce the absolute value of a number and its sign. A decoding system with these features eliminates any further decoding to display negative numbers. The magnitude and sign capability of the configuration shown in Figure 4 simplifies the decoding of negative numbers for both the 8284 and the 8285.

Circuit Description

As shown in Figure 4, Gates 1, 2, 3 and 4 form a D-type latch. The U/\bar{D} input is transferred to point P (Gate 3) when the combined Carry-Out ($C_e \cdot C_i$) goes to a "1" level. The function generated at the output U/\bar{D} is:

$$U/\bar{D}_O = S \cdot P + \bar{S} \cdot \bar{P}$$

where: P = "1" (\bar{P} = "0") then $N \geq 0$
 P = "0" (\bar{P} = "1") then $N \leq 0$
 N = Number of counts
 S = "1", count positive
 S = "0", count negative

The latch (P) is enabled when Carry-In ($C_e \cdot C_i$) goes to "1" which occurs at all zero crossings.

Table 4 shows the count sequences generated for a single 8285 BCD Decade Counter with the magnitude and sign generator connected.

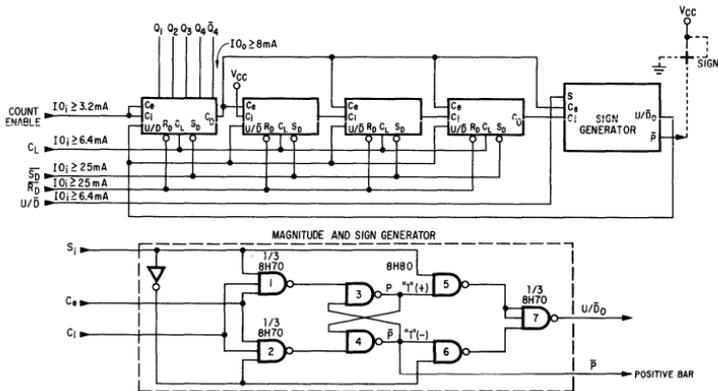


Figure 4

Magnitude and Sign Generator

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$$U/\overline{D}_O = S \cdot P + \overline{S} \cdot \overline{P}$$

where:

- P = "1" (\overline{P} = "0") then $N \geq 0$
- P = "0" (\overline{P} = "1") then $N < 0$
- N = Number of counts
- S = "1", count positive
- S = "0", count negative

The latch (P) is enabled when Carry-In ($C_e \cdot C_i$) goes to "1" which occurs at all zero crossings.

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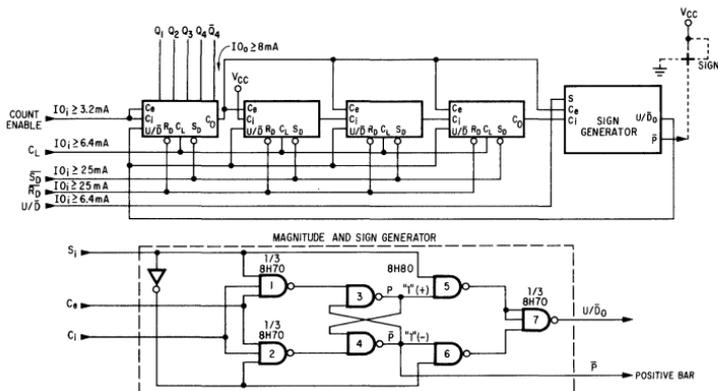


Figure 4

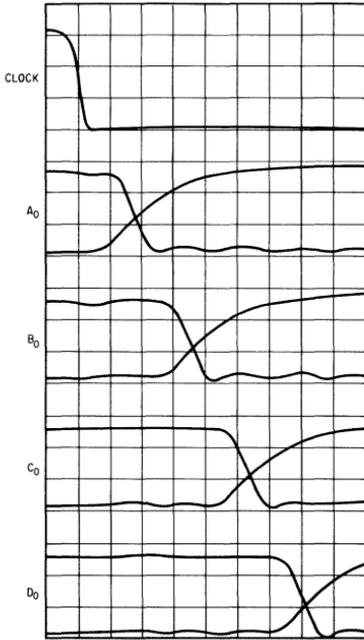


Figure 5a

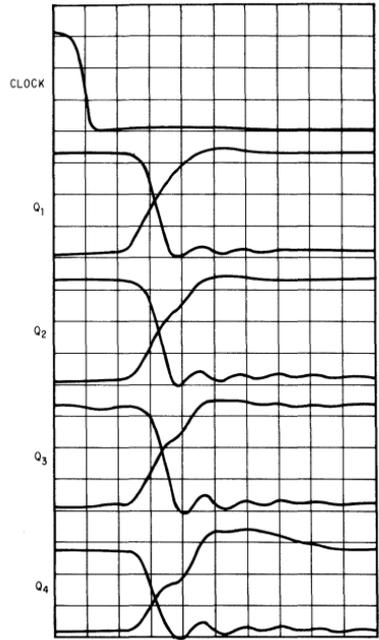


Figure 5c

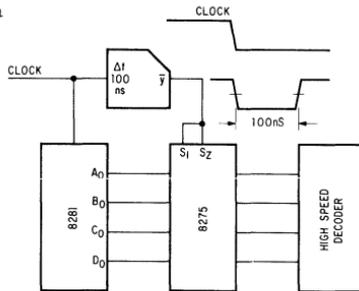


Figure 5b

1-Out-of-N Decoding

A 1-in-16 decoder (4 lines to 16 lines) using an 8284 (Hexadecimal Counter) and two 8250's (Binary to Octal Decoders) is shown in Figure 6a. The necessity of having the \overline{Q}_4 output is apparent in this application. If \overline{Q}_4 was not available, an inverter would have to be connected to the Q_4 output to generate \overline{Q}_4 at some finite delay time after Q_4 . This delay could cause possible decoding errors.

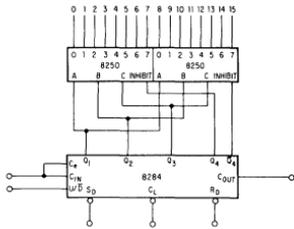


Figure 6a

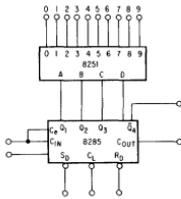


Figure 6b

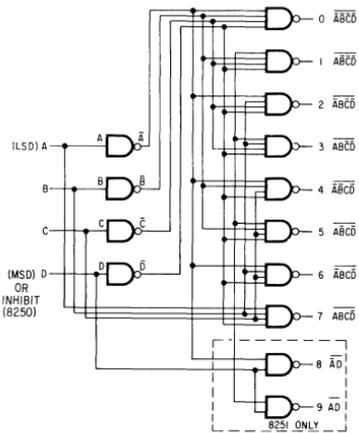


Figure 6c

Figure 6b shows the use of an 8285BCD Decode Counter in conjunction with an 8251 BCD to Decimal Decoder (Figure 6c).

The typical propagation delay for both counter decoder systems from Clock input to decoded output is 30 nsec.

Frequency Multiplexer

The frequency multiplexer shown in Figure 7a uses two 8284's and one 8232, 8-Input Digital Multiplexer (Figure 7b). This circuit permits any one of the 8 outputs of the 8-bit synchronous binary counter (two 8284's) to be decoded. The decoded output frequency is determined by the inputs N_0 , N_1 , N_2 and Inhibit as shown in the truth table in Figure 7.

The propagation delay from the falling edge of the clock to the outputs of the multiplexer (8232) is the same for all decoded frequencies. This propagation delay is typically 37 nsec for true output (f_0) and 30 nsec for the inverted output (\bar{f}_0).

Variable Modulus Counter

Figure 8 shows a variable modulus counter or programmable frequency divider using synchronous counters (8284's or 8285's) and 4-bit Digital Comparators (8242's). The 8242 (see truth table) has open-collector outputs. As shown in Figure 8 for four 8284's or 8285's, a "1" logic level is generated at point Z when the counters outputs digitally compare with the input binary (8284) or BCD (8285) sixteen bit word. The counter must be connected in the count UP (U/\bar{D} = "1") mode. R_L was calculated for minimum propa-

SECTION 5
INTERFACE AND DISPLAY ELEMENTS



APPLICATIONS MEMO

INTERFACE CONSIDERATIONS

Interfacing problems exist with systems at data transfer points, as well as at communication links between systems. These numerous interface problems with their variety of solutions come about because there are different interface situations to solve. Interface translations may be classified into four basic categories:

1. Impedance translations
2. Voltage translations
3. Current translations
4. Time translations

Several examples of each of these categories are to be shown in the following examples. Some of the examples may be a combination of these classes of interface situations. Some techniques provide advantages over others as far as speed and cost are concerned. These techniques have been summarized at the conclusion of this material. Analysis of the summary will provide the best interface solution for a specific interface environment.

The first consideration generally given to potential interface problems is with the interface between systems. Systems may have no common mode connections and require a communication link or there may be a specified common mode voltage range between the two systems. Either of these techniques are classified as impedance translations. Complete DC common mode isolation accomplishes impedance isolation between the common power systems and the limited common mode isolation may be accomplished in various satisfactory ways. The specific techniques follow.

An example of complete common mode isolation for a safe data communication link is shown in Figure 1. Here the use of integrated circuits to drive a transformer coupled data link provides a sure and economical data transfer. Data transfer of this type may be rapid and proper design can allow immunity to both magnetic and electrostatic coupling noises. These techniques lend themselves to rapid data transmission.

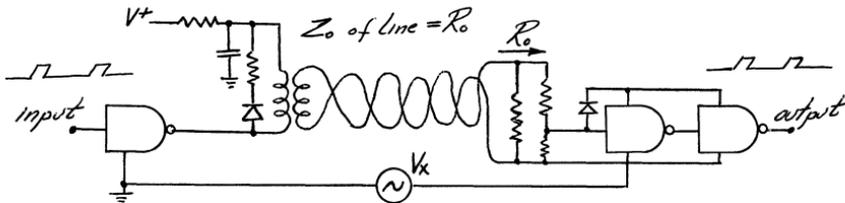


Figure 1

Where a known common mode voltage difference exists direct coupled techniques may be employed to provide the data communication. A number of methods which are covered utilize techniques which improve the noise rejection characteristics of a system.

Logic transitions from "normal to higher voltage" may be satisfied using a specially designed high voltage integrated circuit such as that shown in Figure 2. This gate operates as a conventional NAND gate; but interface voltage transition gates can provide logic transitions as high as 40 volts. For those cases where the current sinking capability of one gate is not sufficient, gates may be connected by paralleling both input and output. Such a power translation techniques may be used for driving 28 volt lamps. Very high currents may also be driven with the addition of a transistor as shown in Figure 2 by the dotted connection. The speed limitations of this techniques are limited to the speed of the gate and the load time constants. The economics of such a data transfer are quite good.

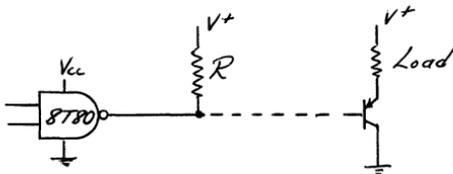


Figure 2

Another such voltage interface is that of the voltage translation to a "NIXIE" tube. Only recently, this interface problem has been satisfied with an integrated circuit such as the 8T01. This element performs the required one of ten decoding but also has stable high voltage switching characteristics.

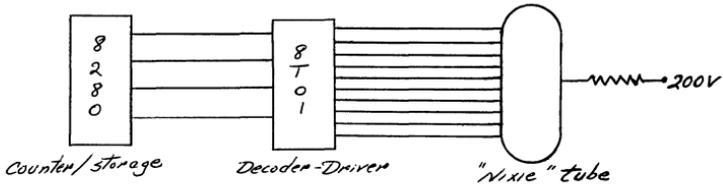


Figure 3

A second such element which satisfies display interface problems is the seven segment decoder driver (8T02). Here special decoding is performed as well as provide the required drive for incandescent lamps. Usage of these two elements effect a reduction in decoding package count and also the normally required discretes to drive the lamps.

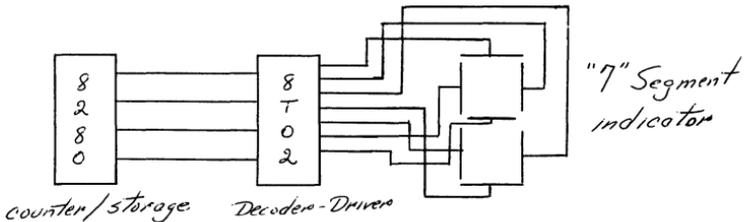


Figure 4

A high voltage to normal voltage logic transition problem is quite often encountered at system and subsystem interfaces. Three techniques are found in Figure 5.

Use the specially designed high threshold input gates such as the 8T18 element (Figure 5a) or make use of some of the known characteristics of the logic elements (5b, 5c).

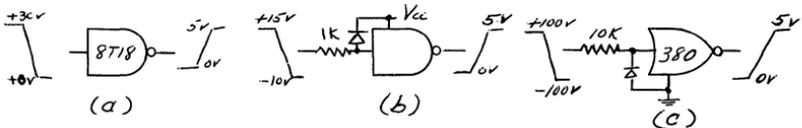


Figure 5

In the Figure 5b and 5c cases current through the series resistor should be limited to less than 10mA. It must also be realized that the logic threshold levels will shift for these second two cases since some current is required to flow through the series resistor. The Utilogic gate of 5c will result in the smallest shift in threshold since the input impedance of this gate is an order of magnitude larger than the gate of Figure 5b.

One of the most common interfacing situations is that of logic common mode level translations. These can be level translations to higher DC voltage levels or to lower DC voltage levels or to bipolar voltage translations. There are numerous cases where these translations require special characteristics so only typical circuits will be shown in Figure 6a, b, and c.

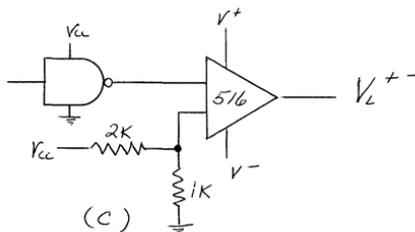
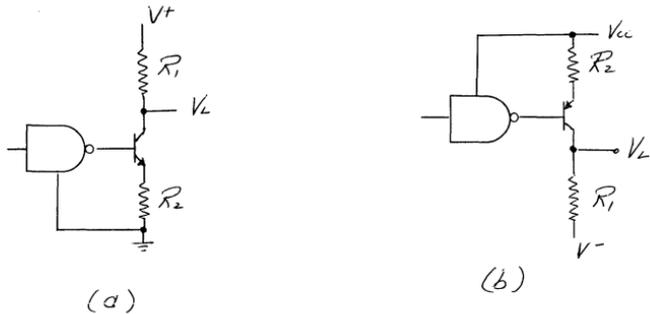


Figure 6

The positive and negative voltage logic translations make use of the external circuit current source drivers to accomplish the logic translations. The amplitude of the logic changes after level translation is related to the following equation:

$$V_L^\pm = (V_L^0 - V_{BE}) R_1 R_2^{-1}$$

Where: V_L^\pm = The logic change after level translation

V_L^0 = The logic change before level translation

V_{BE} = The transistor base emitter voltage

The bipolar logic translator utilizes a linear amplifier to provide the bipolar outputs.

Another important data transfer network is that of the long transmission line. These can be anything from one foot to one mile. When does a data link become a transmission line? A long line can be generally defined as follows. When an input pulse transition is faster than the transmission characteristics of the line and the gate connected to this line responds to the differential characteristics of the gate and line, then the data link must be considered a long line data link. There are three desirable methods by which data can be transmitted over such lines. The discussion of separating these into categories of a reasonably long line and that of a very long line follows.

A reasonably long line can be handled by merely properly terminating the line in the line characteristic impedance. An example of this impedance and voltage translation is shown in Figure 7.

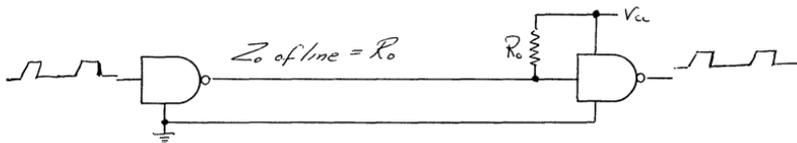


Figure 7

The ratio of mismatch of the termination resistor and the line impedance will determine the magnitude of the undesirable noise reflection.

The very long line should be handled using different techniques. There are two desirable methods to solve this data transmission problem. Both require a transmitting pair of lines and both require the line to be terminated in its characteristic impedance. The first of these methods must be considered a voltage mode solution where gates are used both as the driver and receiver termination. This method functions quite well for both low and high speed data transmission but does not lend itself to transmission line sharing. The circuit is shown in Figure 8.

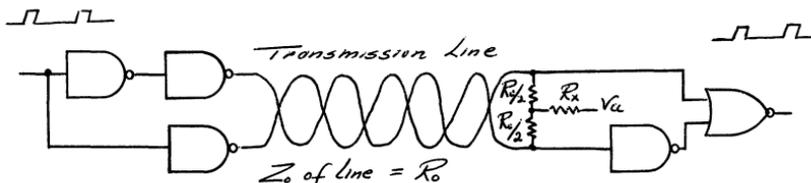


Figure 8

The values of resistors $R_o/2$ provide the proper termination for the line so as to minimize reflections. The value of R_x will be dependent upon the driver gate. Its function is to provide an improvement in the input logic "1" levels and to not change the line termination impedance. The specific value of R_x may be calculated using the gate sinking and sourcing characteristics and the line termination resistors $R_o/2$.

A second technique which must be considered a current mode data link is shown in Figure 9. This circuit functions well for both low and high data rates and also lends itself to load sharing of the data lines. Because of the current mode logic a low level detector such as the analog comparator shown is required.

It can be seen that a finite common mode voltage tolerance exists with either of these circuits. Other techniques such as transformer coupling are required if common mode differences greater than those acceptable above are expected.

To this point we have been concerned with voltage translations of data but time translations are often necessary when asynchronous input data must be used in a synchronous system. This information transfer can be handled very easily with specially designed circuit elements such as the 8829 Signetics element. This

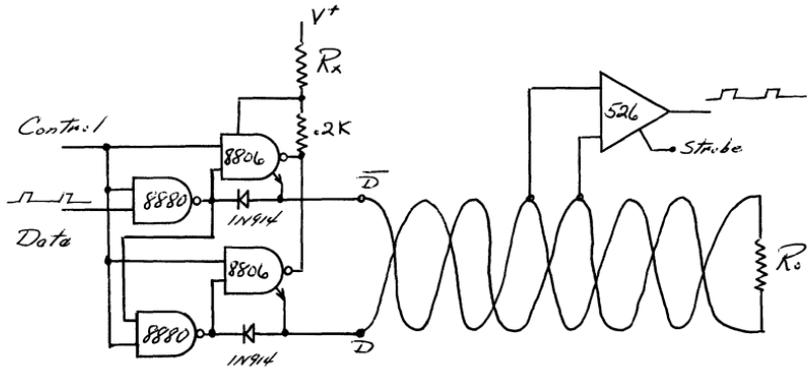


Figure 9

element lends itself very nicely to asynchronous data entry since it allows a sampling of the J and K inputs when the clock goes to a logic "1" and then transfers this intelligence to the outputs on the logic "1" to logic "0" transition. The only restrictions to this type of data entry is that the data rate be less than clock rate. This type of data entry is shown in Figure 10.

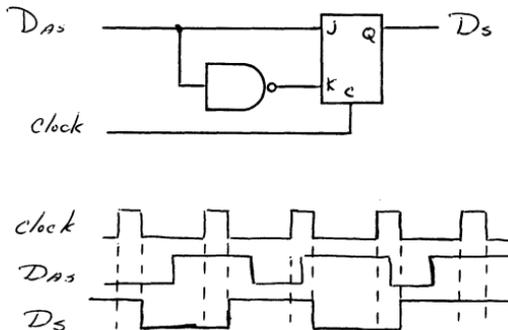


Figure 10

A summary of the previously shown techniques are provided in table form showing the relative rating of each technique on a per unit basis for the terms speed, noise rejection, and cost. The comparison of common mode range is shown as positive and negative voltage limits.

Technique	Speed	Noise Rejection	Cost	Common Mode Range	
				High	Low
Logic transformer coupling Figure 1	1	1	3	Complete Isolation	
High voltage output coupling Figure 2	1/3	1/3	1	V^+	-0
High voltage input coupling Figure 5a	1/1.5	1/2	1	8V	-0
Figure 5b	1/2	1	1	5V	-10V
Figure 5c	1/2	1	1	4V	-100V
Logic level translations to higher voltages Figure 6a	1/1.5	1/2	2	V^+	$(V^+) - V_L$
To lower voltages Figure 6b	1/1.5	1/2	2	$V^- + V_L$	V^-
To Bipolar Figure 6c	1/2	1/2	4	+15	-15
Line Driver Figure 7	1/1.5	1/1.5	1	1.0	-0.6
Differential Line Driver volt- age mode Figure 8	1	1	4	1.0	-0.6
Current mode Figure 9	1	1	3	1.5	-1.5

Speed

The per unit comparison of the rate at which data may be transmitted across the interface data link. The per unit scale of 1 has the best speed rating while the per unit ratings of 1/2 and 1/3 have successively lower data transmission rates.

Common Mode Voltage Range

The common mode range is the differential voltage change which may be allowed from the driver zero voltage reference. The normal voltage to the positive voltage limit is the positive common mode limit and the normal voltage to negative voltage limit is the negative common mode limit.

Noise Rejection

The per unit comparison of each circuit for its dynamic noise rejection susceptibility.

Cost

The per unit cost of each data interface technique from best to most expensive. Circuit complexity and the circuit sharing considerations have been made for this evaluation.



APPLICATIONS MEMO

APPLICATION OF INTERFACE ELEMENTS 8T18, 8T90, 8T80

Integrated circuit logic is typically characterized by 5 volt signals switching a few milliamps of current. The power level is intentionally minimized to achieve the highest possible efficiency and the speed is optimized to achieve the highest possible speed. Speed and power are two important factors to be considered when selecting a family of integrated circuits. The Signetics' 8000 is a family of logic that has excellent speed and power capability. Unfortunately the achievement of low power and high speed also results in higher noise susceptibility and broadens the gap between medium power output requirements and the logic output capability.

Low power logic signals are more easily influenced by high power non-logic (noise) signals. High speed circuits are more susceptible to high speed noise. Low speed circuits tend to filter high speed noise. Thus, there is a need to isolate and protect integrated circuits from the high power and high speed noise.

Integrated circuits must also, from time to time, communicate with external circuits such as input-output hardware, relays and lamps. Typically, these devices operate at a power level ten times or more above that of the logic. Thus there is a need for an interface circuit to communicate between the logic and the external environment. The 8T90 low to high driver couples the low level (typically 5V and 25 mw) logic to a higher level (typically 28V and 280 mw). The power level has been raised by over a factor of ten. The noise susceptibility has been reduced by a factor of ten and the signal is more closely matched to the medium power output requirements. The 8T90 couples low level logic information out of the protected logic area and provides the protection of buffer isolation and the advantage of power amplification. The information can now be transmitted through the high noise environment. If a signal needs to enter or re-enter a low logic area then the process needs to be reversed. The 8T18 performs the high to low transition. The 8T18 has an extremely stable (6.5 volt minimum) logic threshold and can entirely eliminate up to 6.5 volts of noise riding on top of the information signal. Thus, the 8T18 effectively couples the high signal down to the lower level while providing digital threshold noise separation and buffer isolation.

When using the interface buffer units the speed of response should be noted. The 8T18 high to low buffer is comparable with the 8480 gate speed for load capacitance up to 200 pf. The 8T90 has a fast 10 ns turn on speed, but due to the high voltage design requirements of the output stage, the 8T90 has a 50 ns storage time.

The 8T90 High Voltage Hex Interface Driver is a new addition to the 8000 family of integrated circuits. It provides a transition from a low to a higher level of logic signal. The schematic showing typical values and the pin configuration diagram are presented in Figure 1. The input structure is a TTL configuration with only one input. The bare collector output permits a wide variety of loads to be used and in addition, it facilitates paralleling two or more stages to perform collector logic or to drive higher current loads. The V_{CC} voltage for this unit is tested to be greater than 40 volts. This limit should not be exceeded even on a transient basis.

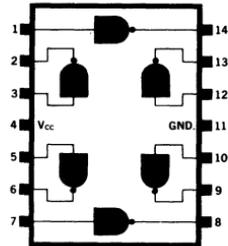
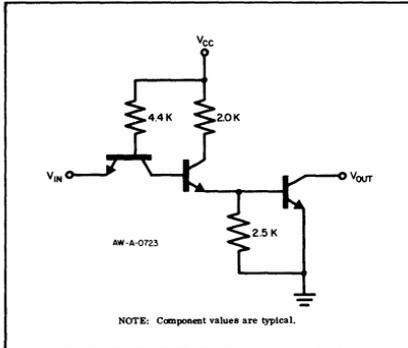


Figure 1. 8T90 Schematic and Pin Diagram

The 8T18 interface element complements the 8T90 in performing the opposite transition from high level to low level signals. Figure 2 shows the schematic and pin configuration. The terminal V_{CC}^{++} is returned to a power supply of 20 volts or more. If the V_{CC}^{++} voltage exceeds 30 volts a series current limiting resistor (limit current < 2 ma) or a shunt 20 - 30 volt zener diode must be used. The input diodes are rated at 50 volts reverse breakdown. If input signals exceed or equal 50 volts, another diode must be added externally in series to protect the internal diodes from breakdown. An important fact about the 8T18 is that its threshold voltage (typically 7.4 to 7.8 volts) is independent of temperature. The various junctions being equal in number and opposite in polarity. Thus, the 8T18 is an accurate high level threshold detector.

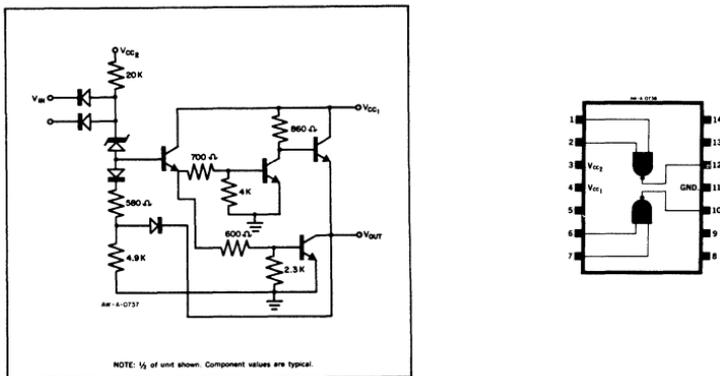


Figure 2. 8T18 Schematic and Pin Diagram

BUFFER INTERFACE APPLICATION

The most general application for the interface elements is that of a buffer element to provide isolation between low level integrated circuit logic and the high level noisy outside world. The most common causes of output to input noise are shown in Figure 3. In Figure 3a, logic is being transmitted to a typical electromechanical device such as a typewriter, tape punch, printer, tape reader, etc. The electromechanical device frequently will have high energy solenoids, SCR, etc, that tend to generate a noise voltage between the logic ground and the device ground. Logic output lines are well isolated from the internal logic.

Note that the 8T90 collector pull-up resistor is attached to the receiving end (i.e., near the 8T18). This helps to lower the 8T18 input impedance. Since there is no connection back into the logic area (even the power supply is isolated) the collector noise is not coupled into the low level logic. The most critical interface is the connection from the electromechanical device or transmitting end into the low level logic area. Here the noise source is in series with signal and looks directly at the

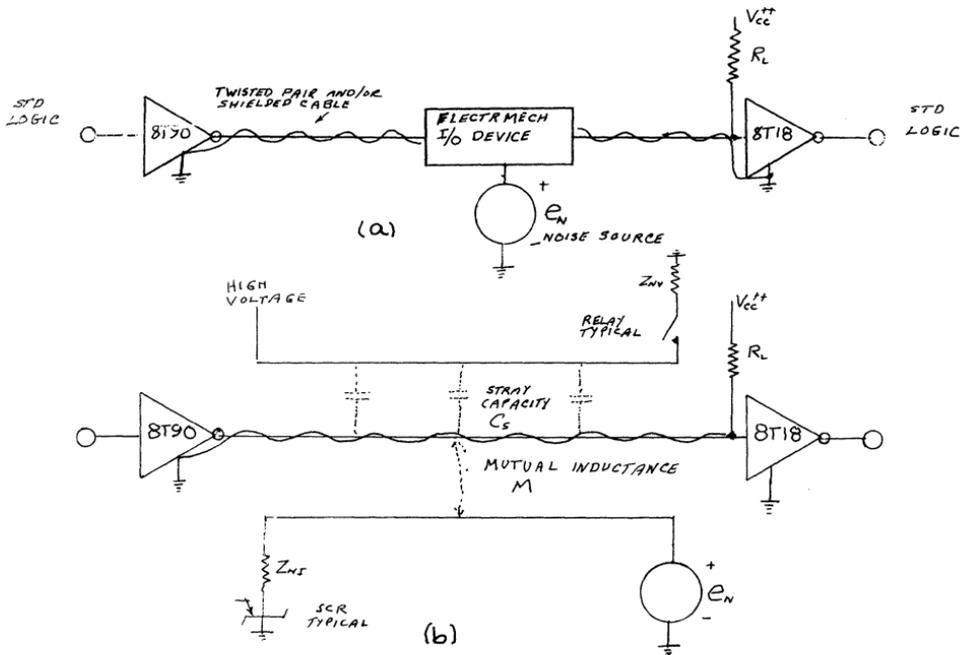


Figure 3. Common Sources of Noise

logic input circuitry. Without the 8T18 high threshold buffer element, the noise would only have to overcome the normal 1 to 2 volt threshold to cause false inputs. The 8T18 has an input threshold guaranteed to be at least 6.5 volts worst case. This means that conducted noise spikes up to 6.5 volts will not cause false inputs.

Figure 3b depicts an application where one logic area is connected to another logic area. The distance between the two areas may be as much as one hundred feet or more and may pass through areas of high electric and magnetic fields. The magnetic and electric fields plus conduction are responsible for almost all noise coupling, but, seldom is electromagnetic radiation the source of noise coupling. The electric field couples via stray capacitance, and Figure 4 shows the stray capacitance coupling noise from a voltage source e_n . For example, the noise source could be a voltage being switched by relays. Any mass whose potential is varying rapidly in time with respect to ground will couple some voltage into the

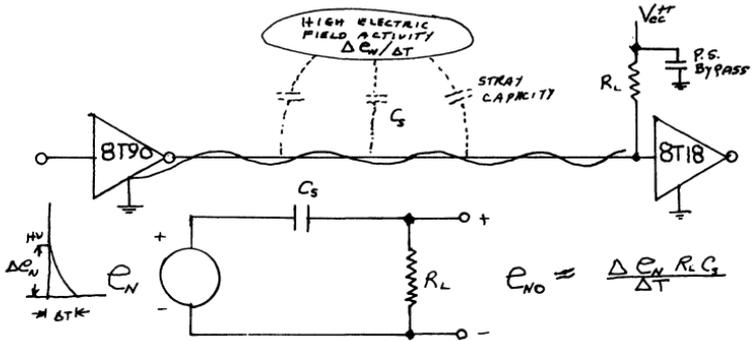


Figure 4. Electric Field Coupling

signal line via the stray capacity. The stray capacity can be minimized by separating signal line physically apart from potential varying circuits and by shielding. Some stray capacitance will remain, however, and the voltage coupled can be approximated by

$$e_{no} = \frac{\Delta e_n R_L C_S}{\Delta T}$$

Where e_n is the change potential, R_L is the logic load resistor (8T90 collector pull-up resistor), C_S is the residual stray capacity, and ΔT is the time it takes the voltage to change.

The noise is coupled during the logic "1" level. During the logic "0" level, R_L is shunted by the 8T90 collector saturation resistance.

Considering the example depicted in Figure 5, the logic signal line is run in proximity to a high voltage line that is switching 10 ma by a relay. A switch speed limiting network consisting of a 150Ω resistor and a .0067μf capacitor has been added to slow the switching speed and has a time constant of 1μsec.

$$\begin{aligned} \Delta e_n &= 150V \\ \Delta T &= 150 \times 0.0067 \times 10^{-6} = 1\mu\text{sec} \\ C_S &= \text{Unknown} \\ e_{no} &= 6.5 \text{ volts max permissible} \\ R_L &= 1.9K \text{ min at } 28V \end{aligned}$$

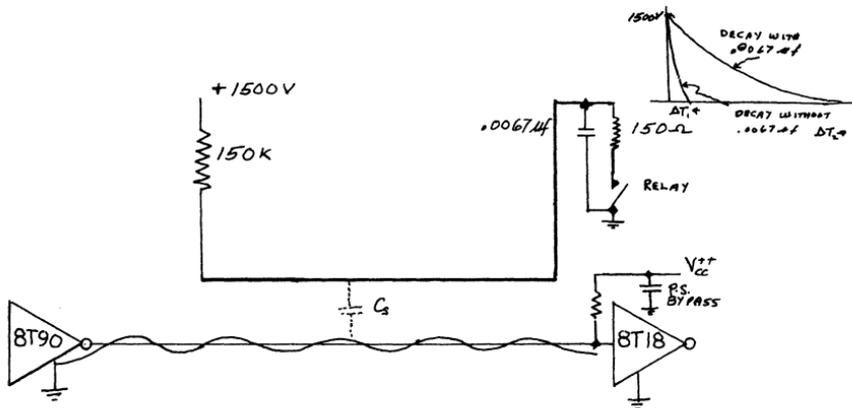


Figure 5. Example Electric Field Coupling

The maximum permissible stray capacitance is

$$C_S = \frac{6.5 \times 10^{-6}}{1.5 \times 10^2 \times 1.9 \times 10^3} = 23 \text{ pico farad}$$

Good layout techniques will easily hold the stray capacitance below this value. The example illustrates the mechanism of electric field interference coupled into signal lines and the techniques used to minimize the coupling. In summary, the following action will minimize electric field coupling.

1. Minimize stray capacitance C_S by
 - (a) avoid bringing signal lines close to potential varying wires or masses.
 - (b) use as much shielding as is economically feasible.
2. Slow rate of electrostatic field collapse, ΔT , by use of networks as shown in the example.
3. Hold the resistive impedance, R_I , as low as practically feasible.
4. Use the high threshold gate, 8T18, to provide the highest possible voltage margin.

To understand the mechanism of inductive noise coupling into the logic lines consider the circuit of Figure 6. All circuits must have self inductance just as all circuits must have capacitance. There exists then some mutual inductance between the signal circuit and the current noise source I_n . Mutual inductance is given by

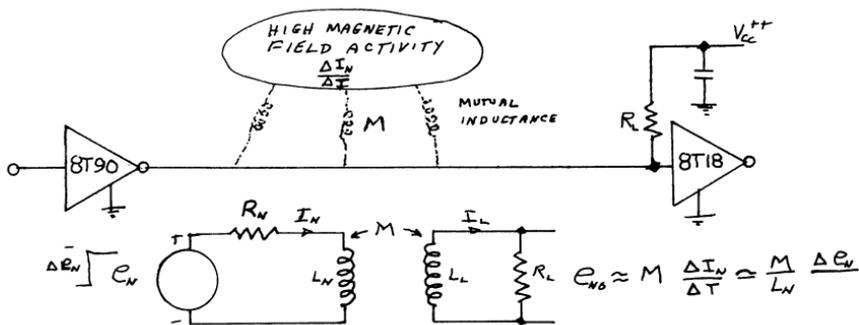


Figure 6. Magnetic Field Coupling

$$M = k \sqrt{L_S L_N}$$

where k is the coefficient of coupling and L_S and L_N are the signal and noise circuit self inductances. The best defense against noise is to keep the mutual coupling low. The coefficient of coupling is reduced by using twisted pair wires and magnetic shielding of both the noise circuit and the signal circuit. The self inductances are minimized by using twisted pairs and the largest wire size economically feasible. A simplified equivalent circuit is shown in Figure 6. Note that the induced voltage due to inductive coupling appears only during the "0" level. During the "1" level, R_L is in series with the off resistance of the 8T90. The analysis assumes that the mutual inductance is very much smaller than the self inductances. The result indicates that the induced voltage is directly proportional to the current switched, the mutual coupling and inversely proportional to the time taken to switch. Written in another form the equation indicates that the induced voltage is proportional to the mutual inductance divided by the noise circuit self inductance times the voltage being switched. Note that the induced voltage is not a function of R_L , the signal lead resistive impedance. From these equations, one can summarize the following:

1. Keep signal lines physically separated (reduce coefficient of coupling or mutual inductance).
2. Minimize the signal inductance by using largest practicable wire size and using twisted pair or coax where necessary.
3. Slow down the current switching rate ΔT (e.g. insert charging reactors thereby increasing L_N).
4. Use the high threshold logic element 8T18 to increase noise margin.

ALL PURPOSE DRIVER

The 8T90 is the most versatile integrated circuit device for output interface applications in the 8000 family. To utilize the element to its utmost capability, some understanding of the limitations of output voltage and current are necessary. A curve of typical output current versus saturation voltage and temperature is shown in Figure 7. The driver current rating at a specific operating point is given in the data sheet. However, if other operating points are desired, then the curve of Figure 12 indicates currents expected versus saturation voltages. In designing for maximum current rating the maximum device dissipation rating of 167 milliwatts at 125°C must not be exceeded.

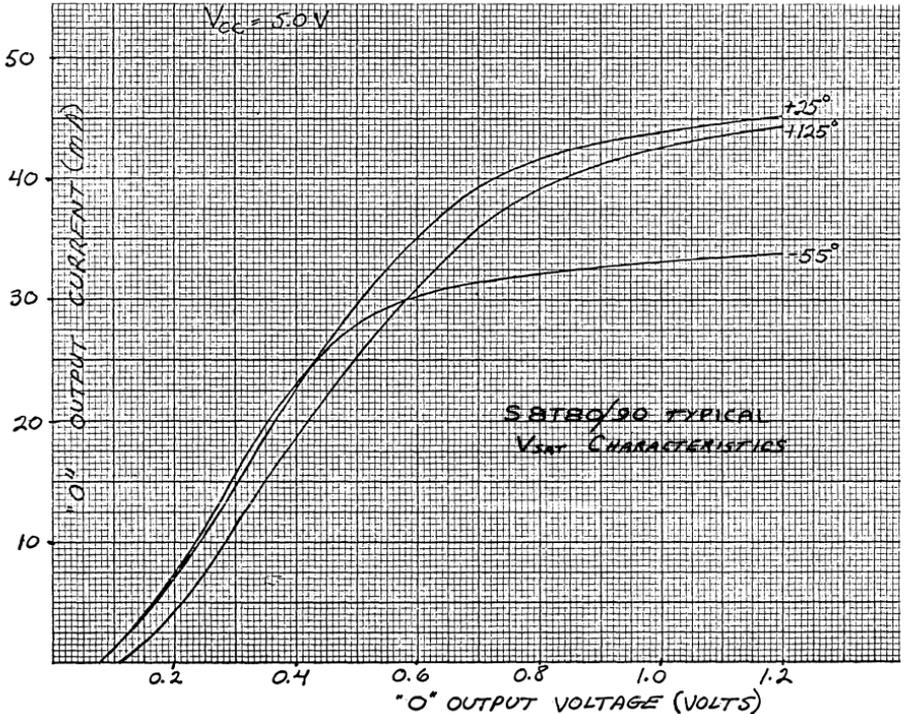


Figure 7. Typical Output Volts Vs Output Current

Each gate draws 20 ma from the V_{CC} power supply when turned on and with zero collector current. If all six inverters are on at the same time, the device is dissipating $(6 \times 20) = 120$ milliwatts and $167 - 120$ or 47 milliwatts are available for collector circuit dissipations. The current available is quite naturally sensitive to the V_{CC} voltage. The sensitivity is typically 5 ma/volt at a 1 volt collector saturation level. The V_{CC} has an absolute maximum value of 6 volts.

RELAY DRIVER

Figure 8 shows the 8T90 used as a relay driver when driven from a logic level. The free wheeling diode is used to dissipate the energy stored in the relay inductance. When the relay is released the 8T90 collector current is diverted through the IN 3064 diode, thereby restricting the induced voltage. Due to the three transistor TTL structure, the reverse transfer is negligible and noise existing on relay wiring, etc., will not be coupled back into the logic. Thus, the inverter performs the function of interfacing and provides buffer isolation.

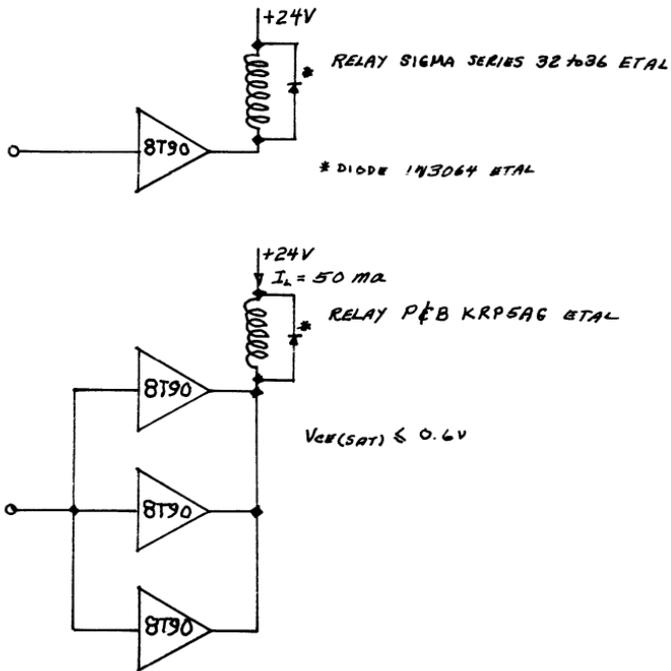


Figure 8. 8T90 Relay Driver Application

In Figure 8a, a low power relay is driven by a single inverter stage. In Figure 8b, three drivers are paralleled to drive a 10 ampere double throw general purpose relay. The expected saturation voltage is less than 0.6 volts and the total dissipation in the three circuits is $3 \times 20 + 30 = 90$ milliwatts, slightly over one half of the total available dissipation.

LAMP DRIVER

Another application of the 8T90 Hex Inverter is as an incandescent lamp driver. For lamps requiring less than 20 ma drive, the circuit of Figure 9 is used. For lamps requiring more than 20 ma, more than one driver may be connected in parallel as shown in (b).

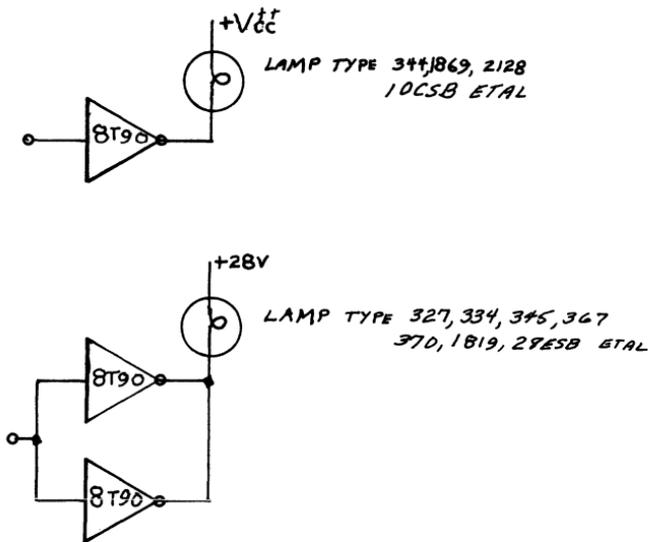


Figure 9. 8T90 Lamp Driver Application

SCRATCH PAD N1283L CONTROL

The Scratch Pad element requires a 6.6 volt minimum to a 10 volt maximum input on the A_3 control pin. The maximum input current is less than 2 ma. The 8T90 is suitable for driving pin A_3 . The circuit is shown in Figure 10.

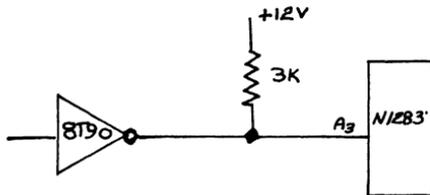
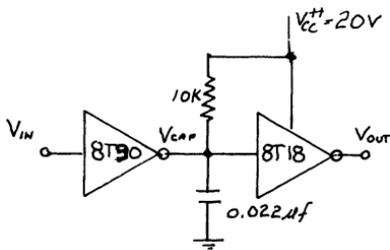


Figure 10. Hex Driver Controls Scratch Pad Memory

STABLE DELAY FOR ONE SHOT, ETC.

The circuit for the basic signal delay is shown in Figure 11. The 10K pull-up resistor is necessary to help stabilize the delay with temperature. Without the 10K resistor, the pulse width increases 20% going from room temperature to 125°C. The threshold voltage is very stable, the variation being due to TTL input sinking current changes. The test was run with the capacitor at room temperature.



$\tau_{DELAY} = 76 \mu\text{SEC} \quad 25^\circ\text{C}$
 $= 80 \quad 125^\circ\text{C}$
 $= 75 \quad -55^\circ\text{C}$

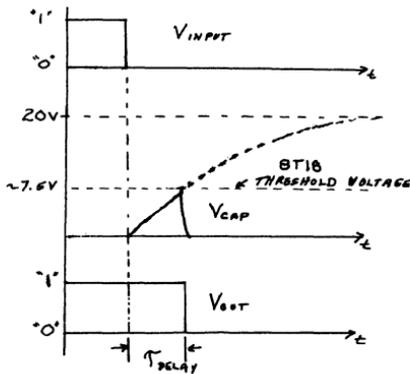


Figure 11. Basic Delay Circuit

MILLER INTEGRATOR

The 8T90 may be used as a Miller integrator. The basic circuit is shown in Figure 12. The down ramp is independent of the load resistor R_L and has good stability with temperature. The main source of error is the input TTL V_{BE} drop. This can be minimized by using a current source in place of V_{CC} and providing additional input shunt current into the 8T90. This circuit is valuable for use as an integrator for lamp circuits and in general slowing down the output of the driver. Figure 13 shows the basic integrator used as a down ramp sweep generator. Because of the 8T18 stable threshold voltage, the sweep has very good temperature stability.

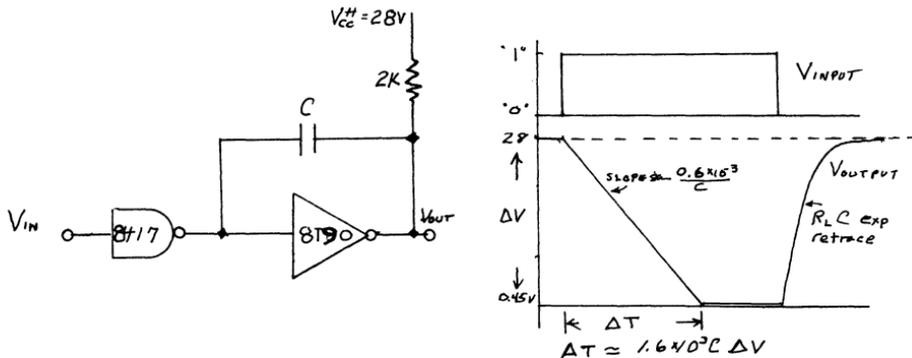


Figure 12. Basic Integrator Circuit

8T80 QUAD GATE INTERFACE ELEMENT

The 8T80 is a quad 2-input NAND gate whose output structure and drive capability is identical to that of the 8T90. Since there are two less stages per package the 8T80 can dissipate proportionately more power per stage relative to the 8T90. Figure 14 shows some latching-driver applications of the 8T80.

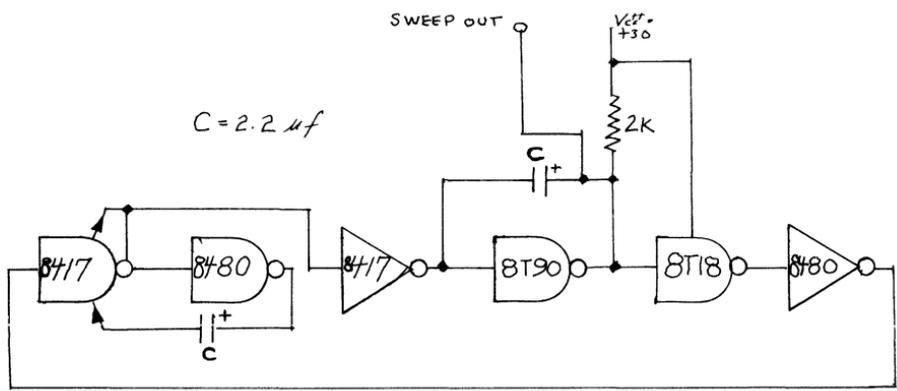
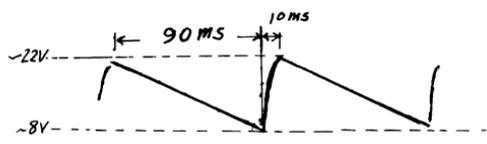


Figure 13. Sweep Generator

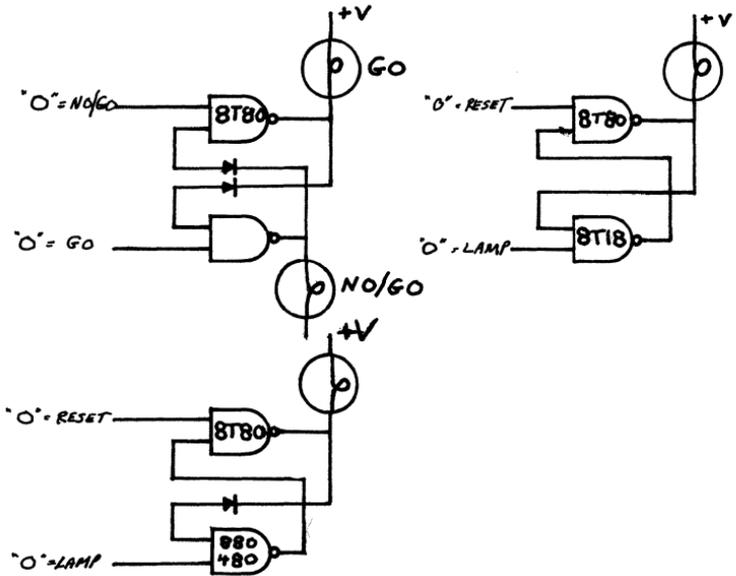


Figure 14. 8T80 Quad Gate Applications



APPLICATIONS MEMO

W. T. Booth

RELAY AND LAMP DRIVING

To drive relays, lamps, and other high current or high voltage devices, it is often necessary to interface discrete transistors with Signetics integrated circuits. This requires the use of the "1" output level which is generally not as thoroughly understood as the "0" output level. A current-limiting resistor is generally all the interface circuitry required. This resistor should be kept as large as possible to limit the power dissipation in the integrated circuit. The simplest way to determine the required value is to first determine the equivalent circuit of the IC output circuitry when in the "1" state.

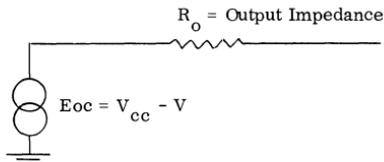


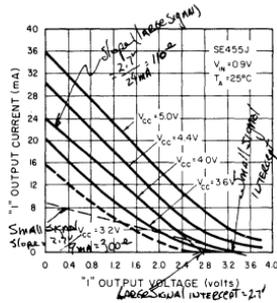
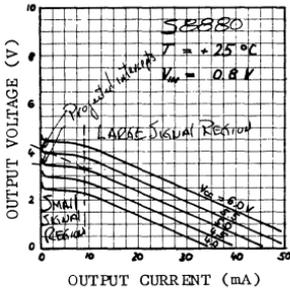
Figure 1 Equivalent Circuit for IC Output in "1" State

Device	V (Volts)	R _o (Ohms)	Device	V (Volts)	R _o (Ohms)
150	1.5	50	455, 8455	0.7*	300*
				1.3†	110†
155	0.9	200	480, 8480	0.6*	1.2K*
				0.9†	800†
180	0	4K	680	0	4K
315	0.9	95	8855	1.6*	10*
				1.0†	70†
331	0.9	95	8880	1.6*	25*
				1.0†	80†

*Small Signal †Large Signal

Figure 2 Equivalent Circuits Values

Values of the table were obtained from V_{out}/I_{out} characteristics for the "1" output state. The zero current intercept is V (I_{oc} for that particular V_{cc} value). R_o is obtained from the slope of the characteristic $\frac{\Delta V}{\Delta I}$. Some devices, as 8880, have a compound characteristic; for these the slope in the large signal operating region must be projected to the zero current intercept to obtain V .



To illustrate the use of the above information, assume that a user wishes to drive a 250mA load with the 8880 as driver. One possible transistor is the 2N3108 which has a t_{he} (min) of about 25 and V_{BE} of 1.5 volts at 250mA. Thus, the required DC base drive is 10mA.

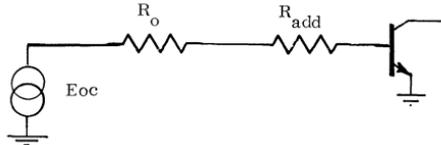


Figure 3 Total Equivalent Circuit

$$R_{add} = \frac{E_{oc} - V_{BE}}{I_B} - R_O = \frac{(V_{cc} - V) V_{BE}}{I_B} - R_O = \frac{4.5 - 1.0 - 1.5}{10} - 80 = 120 \text{ ohms}$$

To improve the switching time of the discrete transistor, a capacitor may be parallel with R_{add} .

Check power dissipation and maximum current at max. V_{CC} , min. V_{BE} , and min. R (assume 20 percent resistor tolerance)

$$I_B = \frac{E_{oc} - V_{BE}}{.8 (R_{add} + R_O)} = \frac{4.5 - 1.0}{.8 (200)} = \frac{3.5}{160} = 22\text{mA}$$

$$P \text{ output} = I_B V + I_B^2 (.8) R_O$$

$$= 22 (1.0) + (22)^2 64 = 22 + 31 = 53\text{mW}$$

The power dissipated in the output stage will cause an additional 10°C to 15°C temperature rise over that established by the remainder of the circuit.

Other suitable transistor types include: 2N3723, 2N3678, or 2N3734.



Dale Mrazek

APPLICATIONS MEMO

HIGH VOLTAGE DECODERS WITH CONVENTIONAL ELEMENTS

Let's consider what is really desirable for a Nixie decoder and driver. First of all we would like to decode using only the true inputs or the Q outputs of a binary and decode the one out of ten outputs. We would like each of the inputs to be compatible with DTL or TTL type outputs so that compatibility within a family is assured. The output characteristics of the decoders must be stable at the high voltage condition and thus eliminate the necessity of clamping these points. This is especially important since additional discrete components are required to achieve this clamp. If this is not obtained, the advantages of the Nixie Decoder are not great at all. Keep this point in mind when analyzing the monolithic elements currently available. Some require a diode clamp to stabilize the Nixie Decoder, others are unstable at elevated temperatures. We have now established the ground rules for a well-designed Nixie Driver; it would have DTL or TTL input structures and have stable high voltage characteristics at its decoded outputs.

The most obvious decoder of BCD (binary coded decimal) inputs would be the complete decoding of the ten possible outputs. Decoding in this manner results in a gate count of ten and a package count of 4-1/2 using existing elements. This decoding arrangement is shown in Figure 1. The true inputs are decoded to the 1 out of 10 line outputs. This simple decoder would not be capable of driving Nixies unless the gate output structures have high voltage characteristics. Neglecting the high voltage problem on the gate output, the package count would necessarily limit its effectiveness to compete with a single monolithic Nixie Driver element. We have now reached the reason for this report. How can we reduce the package count for this solution and obtain proper high voltage stability.

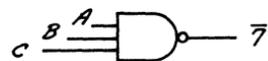
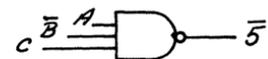
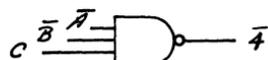
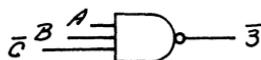
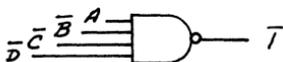
Figure 2 shows a solution including high voltage discrete transistors which will provide not only the decoding requirements but also the voltage stability required for proper design. The technique used to drive the output transistors assures that all unselected Nixie output transistors cannot be forced into a switch back mode or relaxation oscillatory mode. Any breakdown which does result will be zener in form, thus causing a very much more desirable output characteristic than that which is presently available on the market today. Note also that only the true inputs are required for the decoder design making it quite compatible with the Sigmetics 1280 counter element.

This solution requires only 2-1/4 packages using elements which are available today. In addition to these, two resistors and the ten high voltage transistors must be provided as shown in Figure 2. If we were to sum the cost of all elements shown in Figure 2, this solution is now quite competitive with the single element monolithic solution since present monolithic solutions have some undesirable design characteristics. All the requirements as desired in the beginning of this memo have been satisfied.

Let us now consider other possibilities for this same decoding arrangement. Quite often it is desired to select one of many logic circuits. In other words, drive from the one of ten decoder into another logic decoding group. This cannot be accomplished easily with currently available elements; however, it would be no special problem with the solution of Figure 2 if "fan-out" requirements were low.

Some applications require selecting and driving one of many 28V lamps. This same circuit decoding and drive technique may be used for these situations. The arrangement of Figure 2 must be modified if decoded binary data is desired (example decode one of 16). This change has been shown in Figure 3. With either decoding configuration, Figure 2 or Figure 3, it is important that sufficient base current is available to properly drive the selected output transistor. This will vary from system to system and will therefore be left to the individual designer to select. The resistor values shown in Figure 2 are those necessary for Nixie Drivers.

BCD to One of Ten Decoder



Package Count

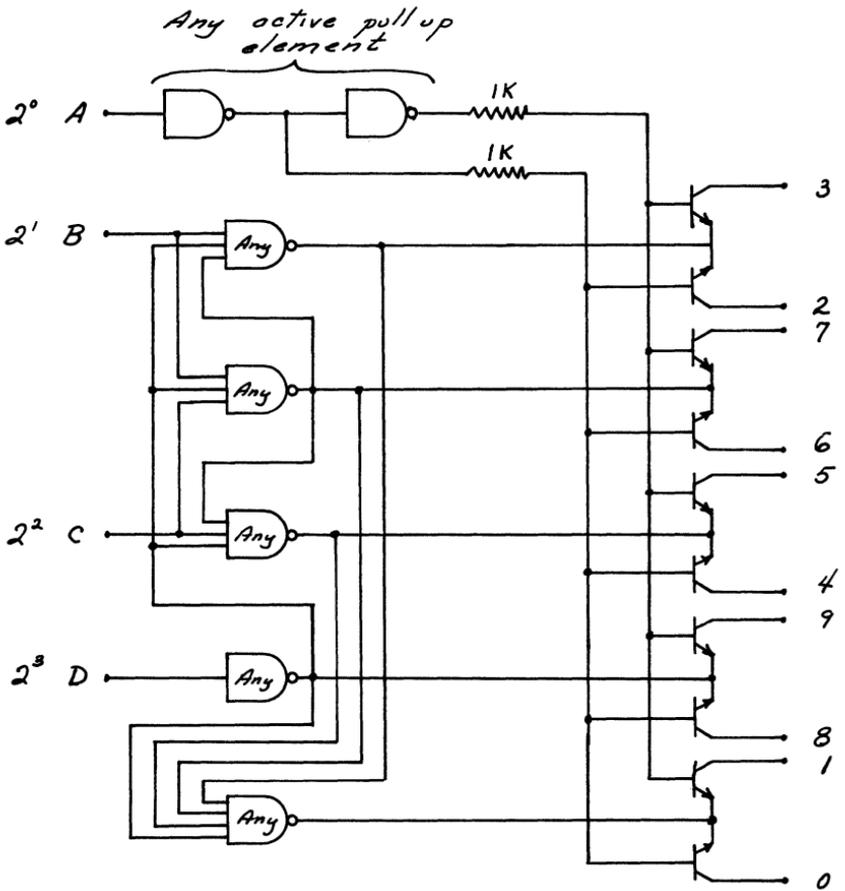
- 1 Dual 4 input gate
- 2 Triple 3 input gate
- 1/2 Quad 2 input gate

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	0	1	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	1	1	0	1	1	1	1
1	0	0	0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	1	1	1	1	1	1	1	0	1	1

Logic 1 = the more positive voltage state
 0 = the more negative voltage state

FIGURE 1

"Nixie" Driver Circuit



Transistor = 2N697 or equivalent

FIGURE 2

High Voltage 1 of 16 Decoder

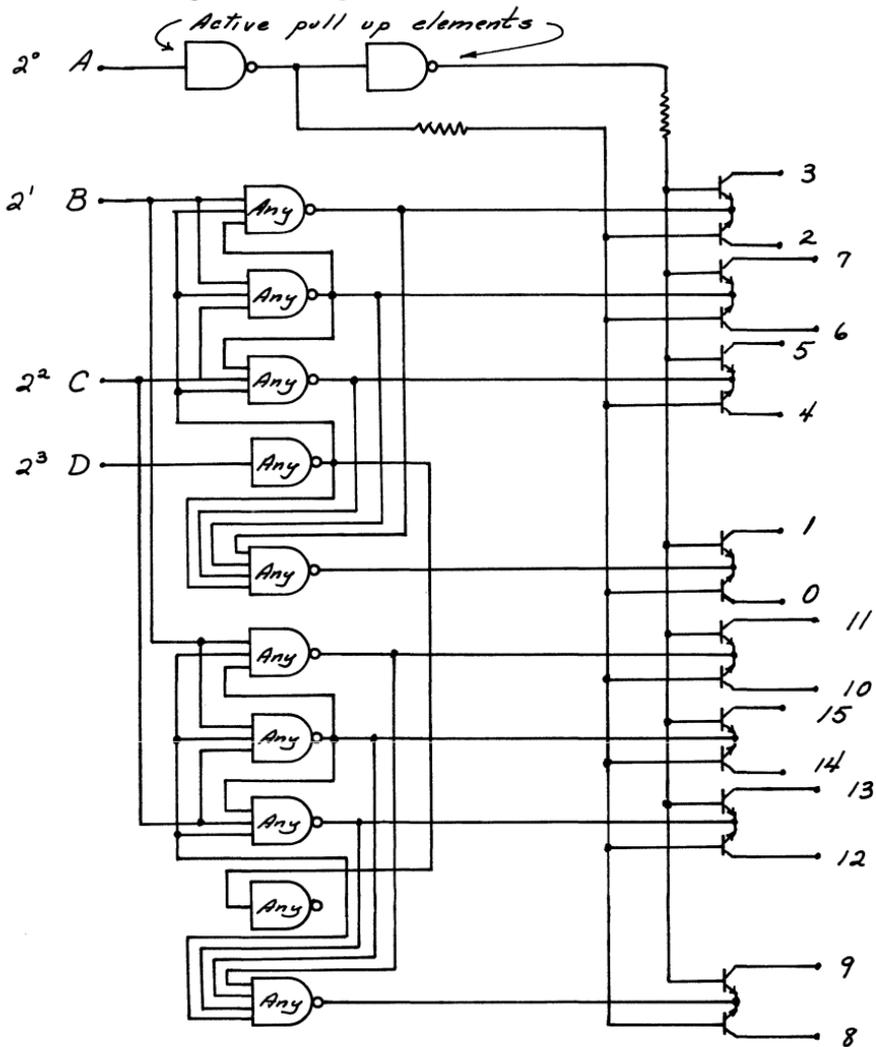


FIGURE 3



APPLICATIONS MEMO

PREVENTION OF ERRONEOUS DATA RECORDING ON 7 SEGMENT DIGITAL DISPLAYS

When using a seven segment display for readouts, see Figure 1, there is a possibility of the observer recording an erroneous reading without realizing that there is an error. The incorrect reading is caused by a segment (bulb) not being turned on due to the fact that it is burnt out (i. e. open circuit for incandescent bulb). For an example, suppose the digit "8" is to be displayed and segment bulb #7 (refer to Figure 1) is burnt out. The observer sees the digit "0" and does not realize that something is wrong. One possible way to protect against such an error is to ensure that when any individual bulb burns out, the #3 and #4 segment bulbs are inhibited from turning on. No recognizable number can exist if bulb #3 and #4 are turned off. A logic circuit that performs such a task is shown in Figure 2 (for 1 bulb) the complete logic implementation is shown in Figure 3.

Operation:

Referring to Figure 2, if it is desired to light segment bulb #1 then both inputs to gate 1 are High (logic "1"), and the bulb turns on via current thru the base-emitter of T_1 thru the Vce sat of gate 1 to ground. Gate 3 is held "off" thru the Vce sat of T_1 and gate 1. Should the bulb burn out then the collector of T_1 is floating (open CKT), the output of gate 2 is a logic "1" (due to Vce sat of gate 1), and gate 3 and 4. The logic "0" output of gate 3 cuts off the #1 gate thus inhibiting the #3 and #4 segment bulbs.

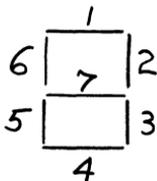
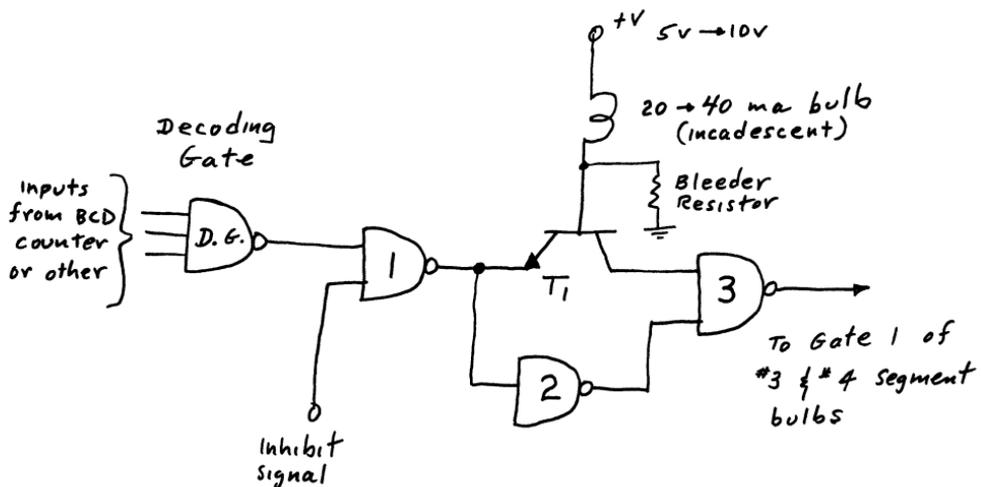


Figure 1



Note: The number of inputs shown on the decoding gate has no bearing on the actual number of inputs

Suggested Choice

$T_1 = 2N3019, 2N3020, 2N3510, 2N3511$

$2N3498 \rightarrow 2N3501$

$2N3647 \rightarrow 2N3648$

FIG. 2



APPLICATIONS MEMO

MULTIPLEX OPERATION OF NIXIE[®] TUBES USING SIGNETICS' COMPLEX ARRAYS AND NIXIE DRIVER

With the advent of the new Burroughs Nixie Tube designed for multiplexing techniques, a new approach to readouts can be taken which will result in substantial can count savings. Specifically only one decoder/driver will be necessary to drive up to 20 Nixie Tubes, though a memory element will be necessary to store the BCD codes, i.e., for 20 tubes one needs 20 four-bit words (assuming that the digits 0 through 9 are to be displayed). This technique can be achieved by combining the 8270 (four-bit shift), 8101 (Nixie[®] decoder/driver) and 8281 (four-bit binary counter), 7491 (8-bit shift register), in a small subsystem (see Figure 2).

1. All Discrete Devices
 - a. Advantage - large selection of components
 - b. Disadvantage - complexity of interconnects and large number of devices
2. Gates and Flip-Flops
 - a. Advantages - fewer components - many types offered
 - b. Disadvantages - high can count and complex interconnect
3. Complex Arrays
 - a. Advantages - fewest components and interconnects should be most economical.
 - b. Disadvantages - small selection of the market; therefore, possible single sourcing.

Concluding then, the best approach from an economic and least number of components viewpoint, which are essential to the desk top calculator or instrumentation market, is the third approach listed above.

Functional Description

Figure 1 is a block diagram of a logic subsystem for multiplexing that recently appeared in an application note by Burroughs Corporation.¹ (See Figure 2 for detailed drawing.) The system has a sequentially

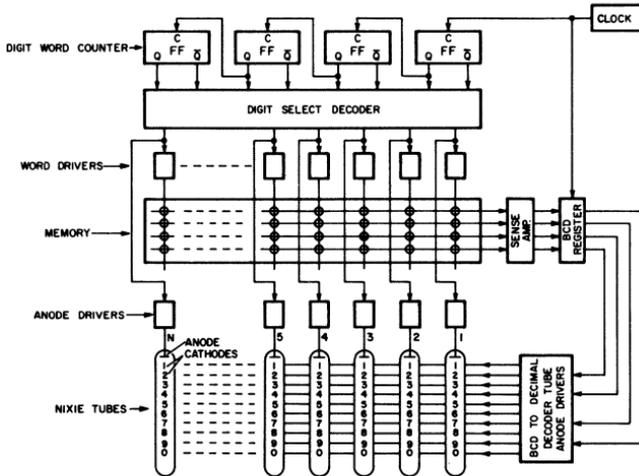


Figure 1 General Multiplexed System

addressable word select memory with a capacity of N words where N is also the number of Nixie indicators in the system. Each word consists of at least four bits which represent, in binary form, the number of the corresponding decimal digit. The recirculation loop and the write circuits for the memory are not shown in Figure 1, but they would normally be required.

When displaying an N digit number, as illustrated in Figure 1, the N words of the memory are sequentially read out at a constant rate that is determined by the system Clock. Each time a word is read out, it is rewritten in the same position of the Memory, thus the information is preserved. When the displayed information is to be altered in one or more of the digit positions, the new information is written into the corresponding word position in the memory, just after the existing words are read.¹

Figure 3 shows a constant voltage anode driver circuit. In the circuit, one of the transistors, Q_1 , Q_2 , Q_3 , etc., is turned on while the other are held off. Diode CR_1 , in conjunction with the base resistors, R_1 , R_3 , R_5 , serve to back-bias the off transistors. To turn transistor Q_1 on, a negative pulse is applied to input number one. The components R_2 and C_1 are chosen to maintain transistor Q_1 in the on condition for the full period required by the system timing.

- $R_1 = 4.7K$
- $R_2 = 1K$
- $R_7 = 3.3K$
- $C_1 = 1\mu F \ 250V$
- $Q_1 = 2N4036$

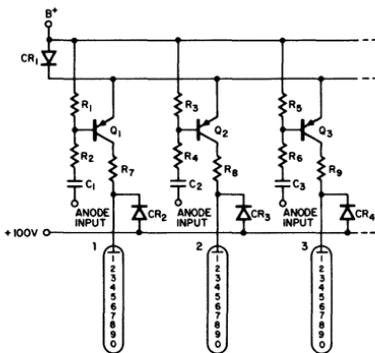


Figure 3 Anode Driving Circuit

The collectors of the constant current drivers are connected through catching diodes CR_2 , CR_3 , and CR_4 to a +100 volt buss. This is done to prevent excessive voltages from appearing across these transistors. Without these diodes, overshoots would tend to occur due to the characteristics of the Nixie tube.

The 3.2kHz oscillator results in a 50Hz signal to an individual anode input. This is sufficiently greater than minimum eye "flicker" frequency (approximately 24Hz). The upper limit of this oscillator could be 10kHz which will result in a minimum "ON" time of 100 microseconds for each tube.³ If the main clock repetition rate falls between these limits, there is no need for the oscillator.

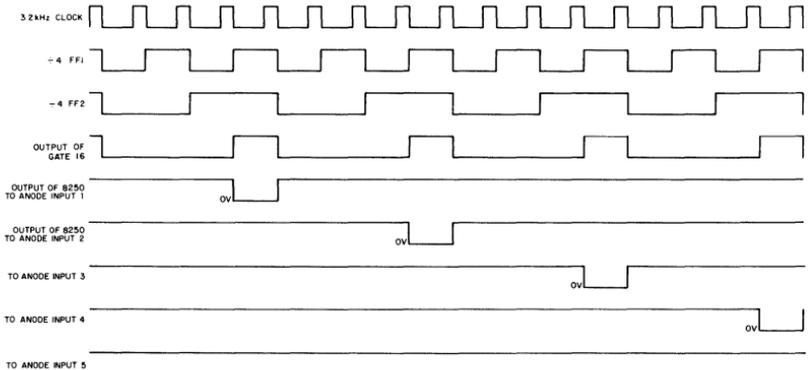


Figure 4 Timing Diagram for 16 Tube Subsystem

(Assumes the 64-bit shift register has been loaded. Note that after every 4th clock (negative-going edge) one anode input out of 16 is energized. Thus all 16 tubes will have been energized after 64 clock pulses have occurred.)

Detailed Description

Refer to Figure 2 and Figure 3. The 64-bit shift right register is loaded from the main memory with the coded numbers to be displayed by each tube. The operation is as follows:

The write information input (Figure 1) normally logic "1" is set to a logic "0" level (pulsed operation). This allows the words in main memory to be shifted into the register. Also, the main clock from the calculator advances a counter such that after 64 counts the display input is set to logic "0" (pulsed operation), inhibiting any further counter advancement, or loading of the shift register. Simultaneously, as the display input goes to a logic "0", the 3.2kHz oscillator starts cycling the 64-bit shift register. Simultaneously, as the display input goes to a logic "0", the 3.2kHz oscillator starts cycling the 64-bit shift register.

The above is accomplished via the following individual steps.

The latch formed by gates 8 and 9 is initially set such that the output of 8 is a logic "0" level. The output of 8 inhibits the $\div 4$ (divide by four) counter, the 8281 (Digit Word Counter), and conditions the latch formed by gates 13 and 14 such that the output of 14 is set to a logic "0" level. As a result of this action, the output of 16 is a logic "0" level which forces the output of gates 17 and 18 to logic "1" levels.

Logic "1" levels at the "D" input of an 8250 (one out of eight decoder) inhibits the output by forcing them all to logic "1" levels.

At the point in time just prior to the negative-going-edge of the 64th clock pulse, all anode inputs to the NIXIE tubes have been at logic "1" levels. (Logic "1" from the 8250's).

After the 64th pulse (from the main system clock), the $\div 64$ (divide by 64) counter is decoded and the output of gate 7 goes to logic "0", forcing the latch formed by gates 8 and 9 such that the output of 8 is set to a logic "1" level, thereby releasing the inhibit on the $\div 4$ and 8281 counters.

Also, all the codes for the digits to be displayed are in the 64 bit shift register and the system is now ready for multiplexing to commence.

Now the system is in the multiplex routine, which is as follows:

The system is clocked by the 3.2kHz oscillator.

The $\div 4$ counter controls the anode strobing by holding the outputs of the 8250's at logic "1" levels for 4 clock pulses, then allowing one output to make the "1" to "0" transition thus firing the number one NIXIE tube viz. the input capacitor (1 μ f).

The TC time constant (1K, 1 μ f) allows the tube to conduct for approximately 300 microseconds.

The next clock (5th pulse) shuts off the 8251's. When the negative-going-edge of the 8th (eighth) pulse has occurred, then the number 2 NIXIE will be fired. The process repeats for all 16 tubes.

The 8281 (Digit Word Counter) is advanced by the $\div 4$ counter. Therefore, the 8281 gets advanced after the negative-going-edge of every 4th pulse issued by the oscillator.

The outputs of the 8281 are decoded by the 8250's which fire the anodes of the NIXIE tubes.

The 64-bit shift register circulates the 16 BCD coded words that are to be displayed.

The 8270 (4-bit shift register) receives the BCD information from the 64-bit shift register and in turn is decoded by the 8T01 (BCD to Decimal) which drives the Cathodes of all 16 tubes simultaneously.

Thus the operation is complete. The automatic blanking control ensures that the tubes are not conducting for 4 shift pulses while the next BCD coded word is shifted into the 8270.

NOTES

1. Reprinted from Burroughs Application Note "Multiplexed Operation of NIXIE Tubes," by A. Somlyody; Manager, Applications Engineering.
2. "The conclusion is that for high-current pulsed operation, the NIXIE indicator requires a higher prebias voltage to minimize "off" cathode glow. For a peak anode current of $i_A < 15\text{mA}$, the cathode driver transistors should have a minimum collector breakdown voltage of 100 volts. Integrated circuit drivers that have lower than 100 volts breakdown voltage, therefore, are not suitable for use in timesharing systems." Refer to Burroughs Application Note "Multiplexed Operation of NIXIE Tubes," Page 5, by A. Somlyody.

"Nixie" is a trademark of the Burroughs Corp.



APPLICATIONS MEMO

APPLICATIONS OF THE 8163 DUAL ZERO-CROSSING DETECTOR

- ZERO-CROSSING DETECTOR
- FREQUENCY TO VOLTAGE CONVERTER
- HIGH STABILITY ONE-SHOT

The 8163 is a monolithic zero-crossing detector incorporating a differential amplifier input and a logic gate output. The input amplifier is referenced to 0V and employs temperature compensation to ensure stable thresholds. The output is DTL/TTL compatible.

The 8163 shown in Figures 1 and 2 requires +5V, -6V and GROUND or +5V, -12V and GROUND. In the -6V configuration, the -12V pin must be tied to the -6V pin. In the -12V configuration, the -6V pin must be left open. (The -12V pin must be tied to the most negative supply used with the circuit.)

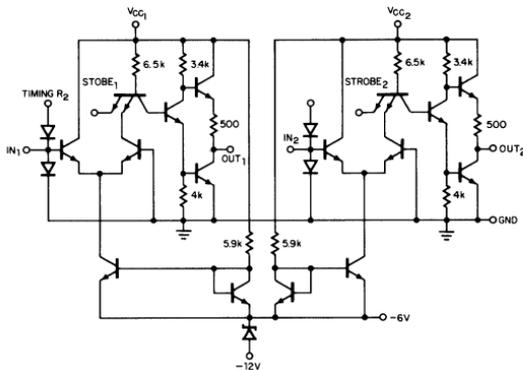


Figure 1. 8163 Schematic

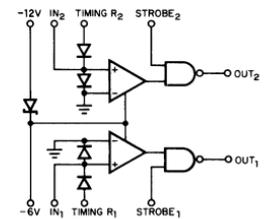


Figure 2. 8163 Logic Diagram

ZERO-CROSSING DETECTOR

A zero-crossing detector (Figure 3) is a device that changes state each time the analog input signal passes through zero. The input signal is thus converted into a train of pulses, as shown in Figure 4. The width of the pulses is frequency dependent.

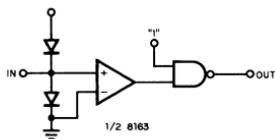


Figure 3. Zero-Crossing Detector

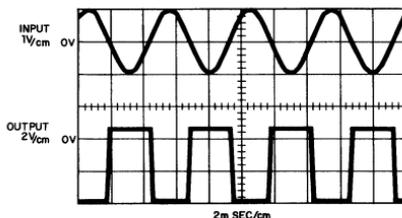


Figure 4. Input and Output of Zero-Crossing Detector

This "infinite" clipping of the signal virtually eliminates distortion caused by amplitude fluctuations and noise. Further data processing is simplified through the use of digital techniques.

A variation of this circuit is one that produces a pulse each time the input signal passes through zero. This circuit, utilizing the 81G3, is shown in Figure 5. The duration of the pulse is determined by the time required to pass through the threshold limits (Figure 6).

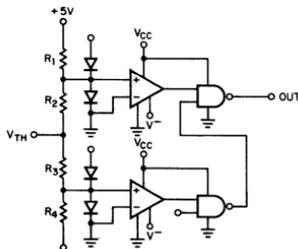


Figure 5. Variation of Zero-Crossing Detector

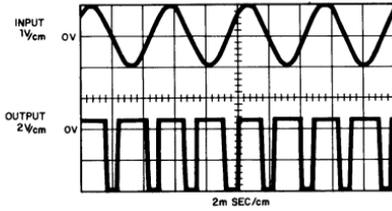


Figure 6. Input and Output of A Variation of the Zero-Crossing Detector

FREQUENCY TO VOLTAGE CONVERTER

A practical method of detecting a frequency modulated (FM) signal, using pulse counting discriminators, is possible using two integrated circuits. No inductors are required for this design.

The circuit diagram of the FM detector, or as it is sometimes called, a Frequency to Voltage converter, is shown in Figure 7. A variable input frequency up to 2 MHz is applied through a current limiting resistor to one-half of the 8163. The output drives a one-shot (the other half of the 8163). Constant width +5V pulses are obtained at a rate determined by the input frequency. The timing resistor is adjusted to give the best linearity for the input frequency range.

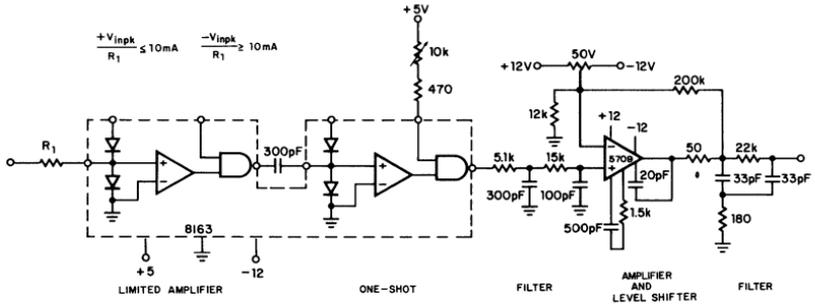


Figure 7. Frequency to Voltage Converter

1. Positive Threshold: $V_{TH} = \frac{0.02(R_3 + R_4)}{R_4} - (V^-) \frac{R_3}{R_4}$
2. Negative Threshold: $V_{TH} = \frac{-0.02(R_1 + R_2)}{R_1} - V_{CC} \frac{R_2}{R_1}$
3. Limits: $\frac{V_{(1)in}}{R_2} \leq 10\text{mA}$ $\frac{V_{(1)in}}{R_3} \leq 10\text{mA}$
4. $\frac{V_{CC} - (V^-)}{R_1 + R_2 + R_3 + R_4} > 200 \times 10^{-6}$ amperes

If: $R_1 = 24\text{K}$
 $R_2 = 1\text{K}$
 $R_3 = 1\text{K}$

$R_4 = 30\text{K}$
 $V_{CC} = 5\text{V}$
 $V^- = -6\text{V}$

$$V_{TH} = \frac{-0.02(24\text{K})}{24\text{K}} - 5 \frac{1\text{K}}{24\text{K}}$$

$$= -0.021 - 0.208 = -0.230\text{V}$$

$$V_{TH} = 0.02 \frac{31}{30} - (-6) \frac{1}{30}$$

$$= 0.0206 - 0.200 = -0.220\text{V}$$

$$V_{(1)in \text{ limit}} = 10^3 (10 \times 10^{-3}) = 10\text{V}$$

$$\text{Bias Current: } \frac{5 - (-6)}{(24 + 1 + 1 + 30) \times 10^3} = \frac{11}{56 \times 10^3} = 20\mu\text{A}$$

The constant width pulses are passed through the RC filter network. The output of the filter network is the demodulated signal superimposed on an average positive DC level.

The 5709 is used to level shift and amplify the demodulated signal. The 50KΩ potentiometer is used to null the average positive DC level which is well within the common mode range of the 5709. Frequency compensation is applied at two points to stabilize the amplifier. The output of the amplifier is the demodulated signal amplified and restored to an average DC level of 0V. The output is filtered, through a bridge-T network, to attenuate the remaining carrier components.

When used as an FM discriminator with a carrier frequency of 1.5 MHz and a deviation of ±80 KHz, the system has an audio bandwidth (-3dB) of 5 Hz to 35 KHz. Distortion at 1 KHz is less than 1%.

Figure 8 is a comparison of the modulating signal and the recovered signal from the Frequency to Voltage converter using a 2 KHz square wave.

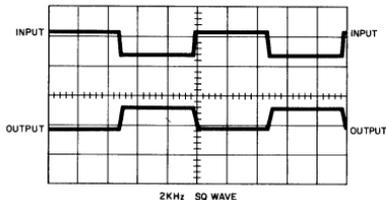


Figure 8. Comparison of Modulating Signal and Recovered Signal

HIGH STABILITY ONE-SHOT

The 8163 may be utilized with a NOR gate to implement a one-shot that is insensitive to temperature and power supply variations. The circuit diagram is shown in Figure 9.

The pulse width is determined by $R_2 C_1$. C_1 may be a polarized capacitor.

$$P. W. = 0.69 R_2 C_1 \text{ seconds}$$

Pulse widths in excess of one minute have been obtained.

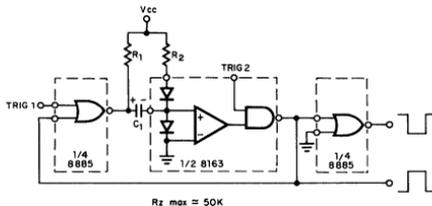


Figure 9. One-Shot

The recovery time is determined by the current limiting resistor of the 8885 up to its output "1" level. From the output "1" level to V_{CC} the recovery time is determined by R_1 , C_1 .

The one-shot timing period may be started by a positive-going logic level at $Trig^1$ with $Trig^2$ disabled (high or open). A negative-going logic level at $Trig^2$ with $Trig^1$ disabled (low) will have the same effect. Although the circuit will operate with shorter trigger pulse widths due to the overdrive conditions, conservative design practices require 75ns pulse widths.

The operation of the circuit is as follows:

When the output of the 8885 is high, the capacitor charges from V_{CC} through R_1 , C_1 and the lower diode to GROUND (Figure 10). The voltage drop across the lower diode causes the input of the 8163 to be high. The output will be low ($Trig^2$ high or open).

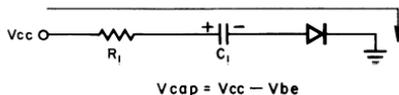


Figure 10. Charge Path During Recovery Time

The timed period is initiated when the output of the 8885 is forced low. When the gate output saturates, the negative-going transition causes a similar transition at the input of the 8163. The resulting negative voltage at the input causes the output of the 8163 to go high. This signal is returned to the input of the 8885 to hold its output low until the timed period is ended. The capacitor charges from $-(V_{CC} - V_{be} - V_{ce(sat)})$ to $(V_{CC} - V_{be})$ through R_2 , C_1 (Figure 11). When the 8163 input voltage has reached 0V the output goes low and the timed period ends.

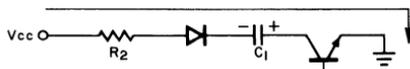


Figure 11. Charge Path During Timed Interval

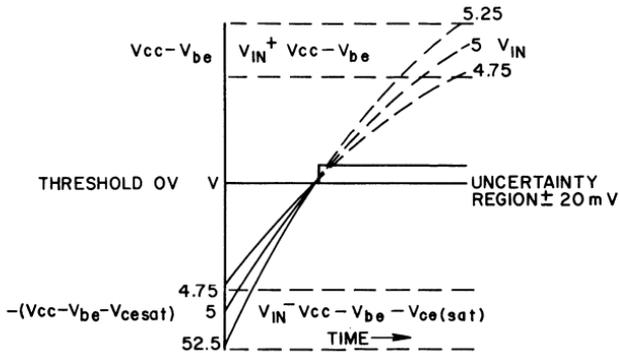


Figure 12. Waveform at Input of 8163.

The pulse width stability is better than 1% because the threshold of the 8163 is centered between the extremes of the voltage, independent of V_{CC} . Since the V_{be} s are matched, it is also relatively independent of temperature.

Figure 12 shows the calculated charging curve of capacitor C_1 (dotted). The measured voltage at the input of the 8163 is shown by solid lines in the same figure.

SECTION 6
LINEAR CONSIDERATIONS



APPLICATIONS MEMO

SE501 CRYSTAL OSCILLATORS

A crystal oscillator can be made from the SE501 Video Amplifier by the addition of a few discrete components. Two methods of doing this are shown in the drawing. The Type A circuit has better load driving capability than the Type B circuit. However, the Type B circuit uses only the optional emitter follower stage of the SE501 leaving the voltage amplifier portion of the device free for other applications. This helps reduce system can count.

The capacitors C_1 and C_2 for the oscillators are selected by the following formulas:

$$\text{Type A: } C_1 = C_2 = \frac{1}{2 \pi (75 \text{ ohms}) f} = \frac{2.12(10)^{-3}}{f}$$

$$\text{Type B: } C_1 = \frac{1}{2 \pi (150 \text{ ohms}) f} = \frac{1.06(10)^{-3}}{f}$$

$$C_2 = \frac{1}{2 \pi (400 \text{ ohms}) f} = \frac{3.98(10)^{-4}}{f}$$

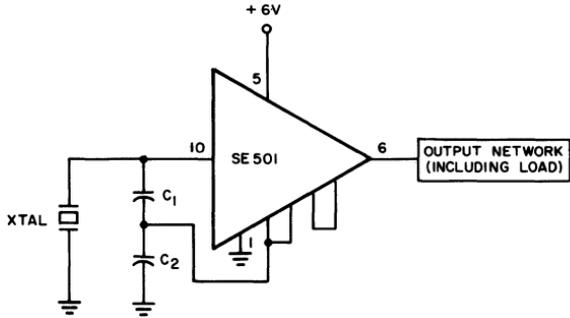
where f = crystal frequency.

These capacitor values are only approximate since they are also functions of circuit layout and whether a ground plane is present or not. The performance of the oscillator may be improved in a given situation if some experimentation is done with capacitor values somewhat different from those calculated.

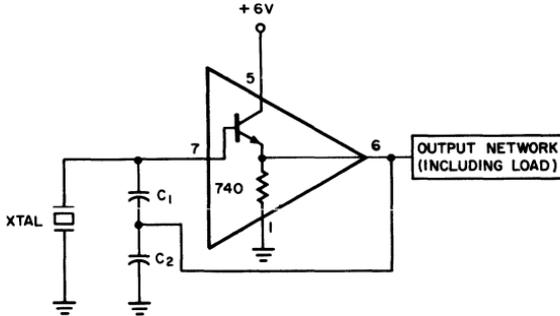
Whether either of the circuits will oscillate or not is also a function of the input impedance of the amplifier. For the Type B oscillator the input impedance is high enough that no problems should be encountered. This may not be the case with the Type A oscillator. If the Type A oscillator does not operate, a large capacitor can be connected between pin 9 and ground. If this does not raise the input impedance enough, connecting the large capacitor between pin 9 and pin 3 instead may raise the input impedance sufficiently.

The characteristics of the output signal are very much a function of the network used at the output of the oscillator. The drawing shows two networks that may be used. Output Network 1 may be used if no filtering is needed. C_3 is made large enough to appear as a short at the crystal frequency. The output voltage swing across R_L is

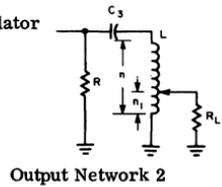
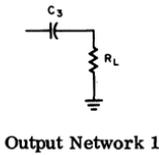
about 3 volts p-p for the Type A oscillator and about 4 volts p-p for the Type B oscillator when R_L is 1000 ohms.



Type A SE501 Crystal Oscillator



Type B SE501 Crystal Oscillator



If the fundamental or a particular harmonic of the crystal frequency is desired at the output, Output Network 2 may be used. C_3 and L form a series resonant circuit which is tuned to the desired harmonic. R in Output Network 2 is a DC load resistor which has some effect on the magnitude of the output voltage swing. For the Type A oscillator, lowering the value of R will increase the output voltage swing. For the Type B oscillator, lowering the value of R will decrease the output swing. In most cases, with the Type B oscillator, R can be eliminated from the circuit altogether. R should be kept larger than 400 ohms for both types of oscillators.

To maximize power transfer and minimize distortion it is usually necessary to match the output impedance of the oscillator to the impedance of the load. This can be done by using a tap on the coil L or making L the primary of a transformer.

The output impedance of the oscillator varies drastically with the size of L so it must be measured for each situation. This can be done by finding the load which if connected across L makes the output voltage swing exactly half of what it is in the unloaded case. Once the output impedance and the load impedance are known, the position of the tap or the number of turns in the secondary of the transformer can be calculated by:

$$n_1 = n(R_L/Z_{out})^{1/2}$$

where Z_{out} , R_L , n , and n_1 are shown in the drawing of Output Network 2. If a transformer is used, n is the number of turns in the primary and n_1 is the number of turns in the secondary.

The output voltage swing across the load is a function of the impedances, the Q of the resonant circuit, and the turns ratio of the coil or the transformer. The Type A oscillator can drive a wider range of loads than the Type B oscillator since the output stage of the Type A oscillator is not required to oscillate, but only supply current to the load.



Dan Nelson

APPLICATIONS MEMO

SE501 LC OSCILLATORS

The drawing shows two simple LC oscillators that can be made from the SE501 Video Amplifier. The Type A oscillator circuit can be used where stability is important since the load is isolated from the LC circuit. The Type B oscillator uses only the optional emitter follower circuit leaving the voltage amplifier portion of the SE501 free for further application.

The maximum frequency obtainable from the Type A oscillator is about 60mHz. The Type B oscillator will operate up to 100mHz. L_1 and C_1 are picked to be resonant at the desired frequency.

The rest of the component values must be selected with the given application in mind. Some experimentation with different values is usually necessary to optimize performance. Some "rules of thumb" which give approximate values for these components are given below.

C_2 in both circuits should be large enough to appear as a short circuit at the oscillator frequency. However, if it is made too large it can cause either oscillator circuit to "motor boat." This is due to the RC network formed by C_2 and the amplifier bias resistor causing the amplifier to act like a multivibrator. If C_2 is chosen so that its impedance is about 1 ohm generally no problems will arise.

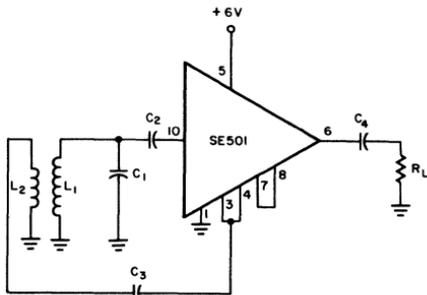
The value of C_3 , the feedback capacitor, is usually a little more difficult to optimize since it is a function of circuit layout and the size of L_2 as well as frequency. In most cases it should present an impedance of about 100 ohms at the oscillator frequency, but it may be necessary to make it as high as 1K ohms or as low as 50 ohms to achieve the desired performance.

In the tests performed to generate this memo, L_2 was made by winding a few turns of "hookup" wire over the existing winding of a Miller sub-miniature adjustable RF coil (0.265-0.413 uh., Miller 40A337CBI). The number of turns used decreased from 7 at 20mHz to 2 at 110mHz. The sense of the winding is shown in the drawing.

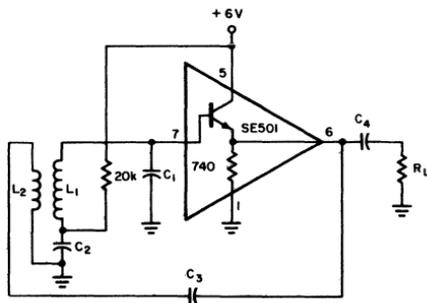
The load impedance, R_L , does not affect the waveform in the Type A oscillator but it does in the Type B circuit. The output voltage swing of the Type A oscillator is typically 1 to 2 volts p-p unloaded. The output swing for the Type B oscillator is

2 to 3 volts p-p unloaded. The output voltage swings of both oscillators tend to decrease with increasing frequency and decreasing load. The Type A oscillator will drive loads as low as 50 ohms. The Type B oscillator will drive loads down to about 100 ohms at which point the circuit will not oscillate.

Either of the oscillators may be used to drive a tuned circuit. The output impedances of the two circuits are functions of the kind of output network used, so the impedances must be measured for a given application to match them with the driven circuit.



Type A Oscillator



Type B Oscillator



R. Seymour

APPLICATIONS MEMO

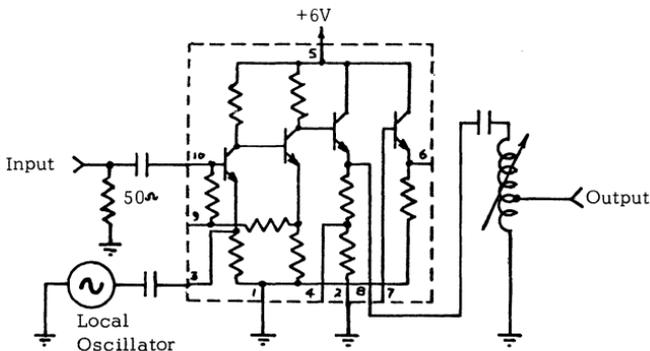
THE SE501 AS A MIXER/FREQUENCY CONVERTER

The SE501 may be used as a mixer or a frequency converter in a superhetrodyne radio receiver.

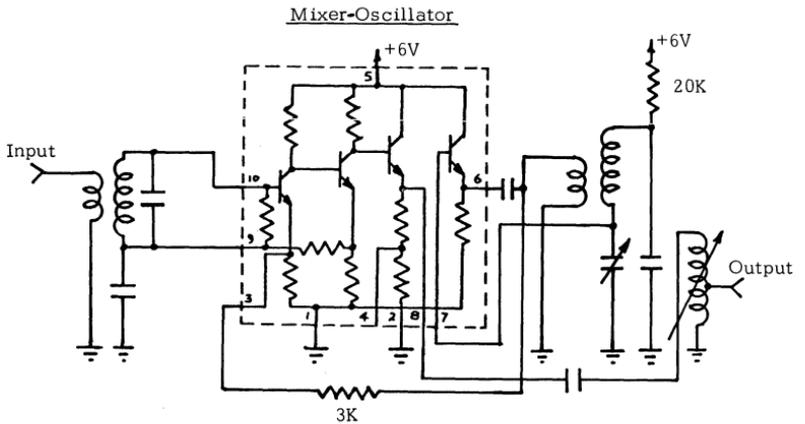
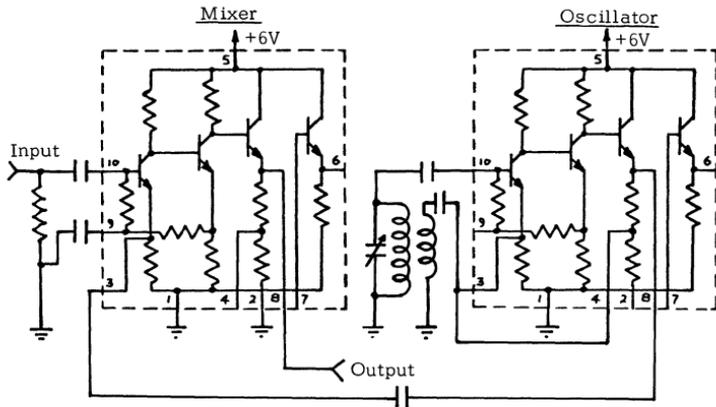
In a superhet receiver, the signal to be detected is caused to beat, with a signal that is generated locally, in a non-linear device called a mixer. The output of the mixer consists of the input signal, the local oscillator signal and their sum and difference frequencies. A bandpass filter is connected to the output of the mixer to remove the input signal, local oscillator signal and the unwanted sum or difference frequency signal. The bandpass filter usually has a number of sections separated by active devices and is called an intermediate frequency amplifier (IF amplifier). It amplifies the selected sum or difference frequency signal.

A mixer may be a diode, or as in the examples to be described in this memo, an active element. An active element is to be preferred for this application for it has a conversion gain rather than a conversion loss that is a characteristic of diode mixers.

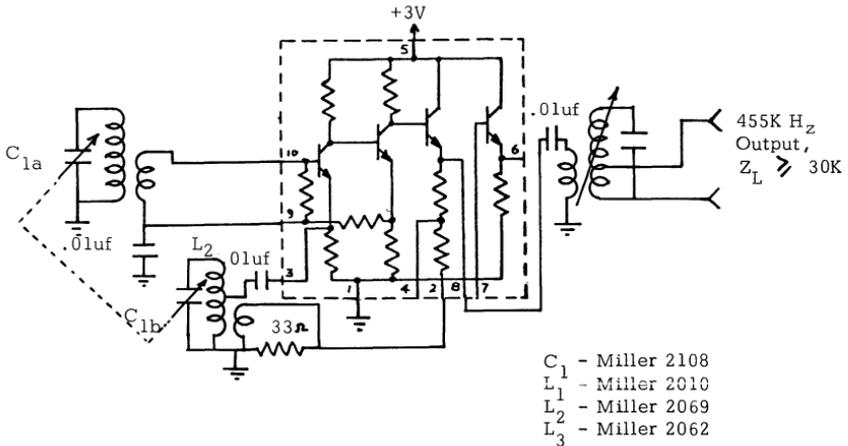
The SE501 will operate as a mixer when it is driven into the non-linear operating region by a local oscillator. The local oscillator signal is injected at the emitter of the first stage (pin 3).



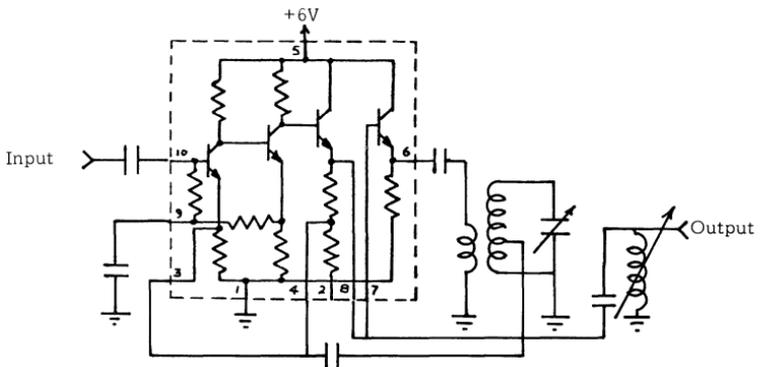
The local oscillator may be a second SE501, or the independent emitter follower output circuit may be used as the oscillator.



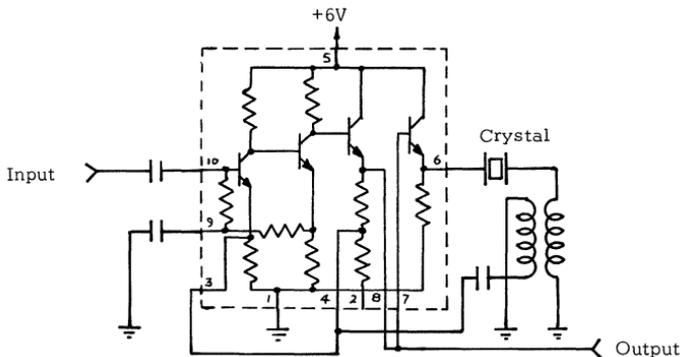
When an SE501 mixer is made to oscillate, it becomes a frequency converter and a separate local oscillator is no longer needed. The circuit below is for a receiver operating in the standard AM broadcast band.



At frequencies over 2 MHz, the feedback point may need to be isolated from the output circuit to ensure oscillation. This circuit uses the independent emitter follower to give the isolation and allow operation to at least 10 MHz.



If the local oscillation frequency must be fixed and stable, the circuit below should be selected. It uses a quartz crystal to obtain the required oscillator stability. The transformer shown is necessary to obtain the proper phase relationships.



The size of the capacitive and inductive components in the above circuits is a function of the operating frequencies and must be selected for each application. The input coupling circuit should be selected to drive an impedance of about 1000 ohms and the output coupling circuit should be selected to be driven from a 50 ohm source. To ensure stable operation, the device power input, pin 5, should be well bypassed for the operating frequencies.

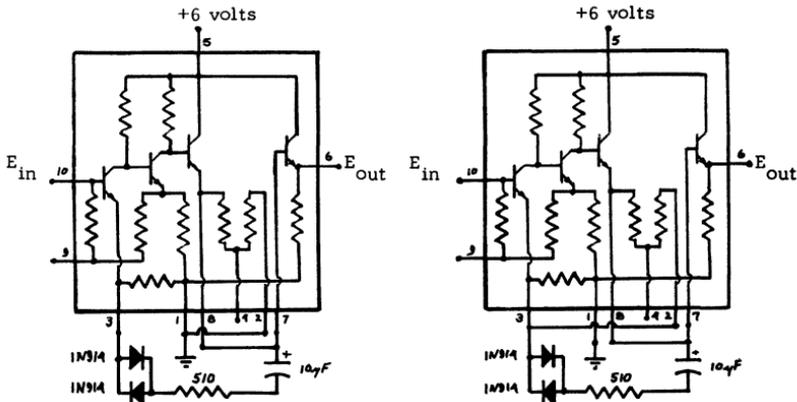


Ralph Seymour

APPLICATIONS MEMO

THE SE501 AS A LOGARITHMIC AMPLIFIER

The SE501 may be made to operate in a logarithmic manner by the inclusion of an element in an external negative feedback loop that has an impedance which is a logarithmic function of the current passing through it. A semiconductor diode will perform this function to a reasonable approximation and for this application is quite satisfactory. Three amplifier configurations may be made, each having slightly different logarithmic characteristics, using four discrete components.

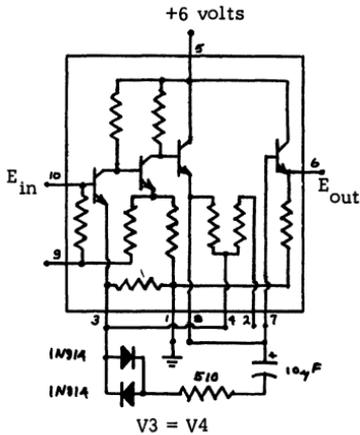


$$\underline{V1 = V2}$$

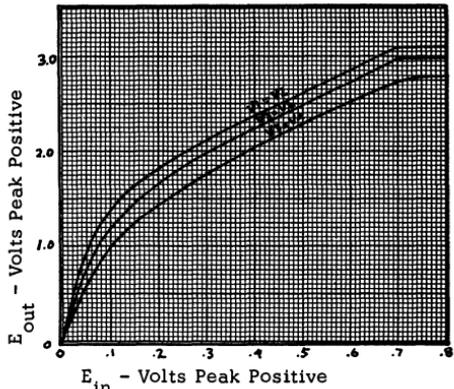
Low Signal Level Gain - 34 db
 Low Signal Level Bandwidth - 4 MHz

$$\underline{V2 = V3}$$

Low Signal Level Gain - 26 db
 Low Signal Level Bandwidth - 12 MHz



Low Signal Level Gain - 19 db
 Low Signal Level Bandwidth - 30 MHz



AMPLIFIER TRANSFER CHARACTERISTIC

The capacitance is included in the feedback loop to prevent the D.C. bias present across the feedback network from affecting the operating point of the diodes. It and the input and output coupling components (capacitors) will determine the low frequency logarithmic response. Two diodes are used so that the logarithmic action will take place for input signals of both polarities. The 510 ohm resistor is necessary to limit the amount of negative feedback applied to a point where the amplifier will be stable at high input signal levels. The inclusion of this resistor, as well as the paralleled internal feedback resistors in configurations V2=V3 and V3=V4, prevent ideal logarithmic action. The resulting circuit is an amplifier with the gain determined by the internal feedback loop for low signal levels, changing logarithmically to the gain determined by the 510 ohm resistor in parallel with the internal feedback resistor for high signal levels.

Use of the second emitter follower allows isolation of the feedback network take off point from the capacitive reactance of the load and, although its use is not mandatory, it is considered advisable to ensure stable operation under all loading conditions.

The diodes should be selected for low capacity and high speed. The 1N914 was used for the tests because of its low cost and availability.

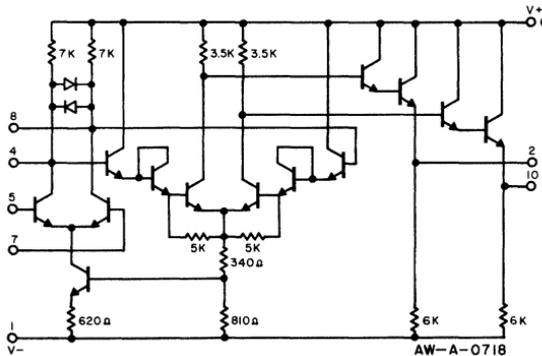


APPLICATIONS MEMO

AMPLIFIER APPLICATIONS OF THE 515

The 515 is a medium gain (4500 V/V) general purpose differential amplifier designed for operation from a single power supply of up to 9 volts or from two power supplies of +6 volts and -3 volts. It is similar to the 505 and will perform all functions of which the 505 is capable and many more. All new designs should use the 515. The applications given in Application Note 107 apply, but may require frequency compensation adjustments for optimum performance.

The input stage of the 515, Figure 1, consists of a differential pair of transistors with a transistor current generator for emitter coupling. A pair of diodes, connected in parallel (back-to-back) between the collectors of the first stage, is incorporated to limit the drive to the second stage when the first stage is over driven. Coupling between the first and second stages consists of emitter followers and level shifting diodes. Use of emitter followers as coupling elements enables optimum utilization of the voltage gain of the differential stages. The currents in the emitters in the second differential stage are passed through an 810 ohm resistor to set the reference voltage for the current generator of the input stage. This configuration provides common mode negative feedback which helps stabilize the operating points of the circuit. The second stage is also loaded with emitter followers to keep the load on the second stage light. A second set of emitter followers is incorporated to provide the circuit with low output impedance. The collectors of the first stage are made available for frequency compensation.



Schematic 515 - Figure 1.

The open loop frequency response of the 515 is plotted in Figure 2. The two major break points of the BODE plot are shown as 800 KHz and 4.5 MHz. A third break occurs at 35 MHz.

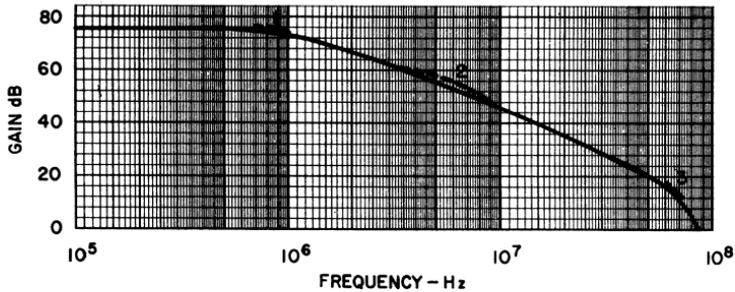


Figure 2.

Since the amplifier has more than one break point the amplifier must be compensated to ensure stable operation when used in low gain applications. The simplest compensation technique is to force the amplifier to have only one break point as in Figure 3, and a roll-off in gain of 20db per decade. This is accomplished by connecting a capacitor of 0.02 mfd between the frequency compensating terminals at the collectors of the input stage. The capacitor was selected in conjunction with the total resistance of the collector circuits, to cause the amplifier to have unity gain at 2 MHz.

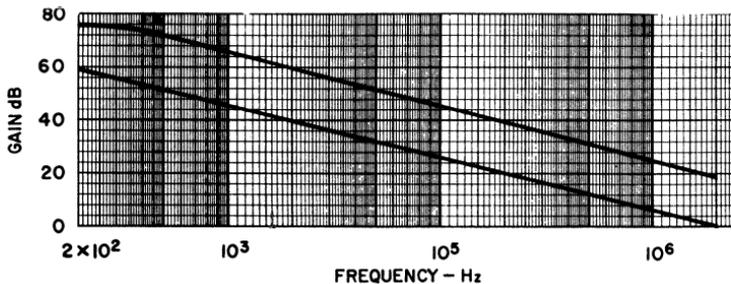
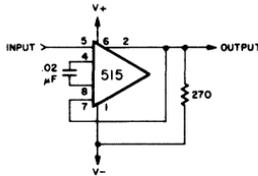


Figure 3.

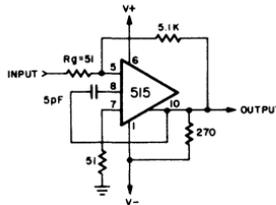
The voltage follower of Figure 4 is an example of the use of this type of frequency compensation. This technique may be used in all amplifier applications where bandwidth is not a critical parameter.



Bandwidth - 2.7 MHz
 $V^+ = 6$ volts
 $V^- = 3$ volts

Voltage Follower - Figure 4.

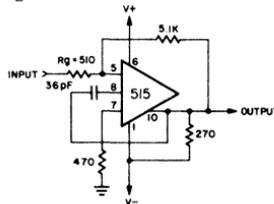
When optimum bandwidth is to be realized, more sophisticated compensating techniques must be used. The higher gain, closed loop, amplifier applications require the simplest frequency compensating networks. The compensation of Figure 5 is the simplest and will be quite satisfactory for all closed loop gains of 40db or larger.



Bandwidth - 13 MHz
 $V^+ = 6$ volts
 $V^- = 3$ volts

Gain = 40db - Figure 5.

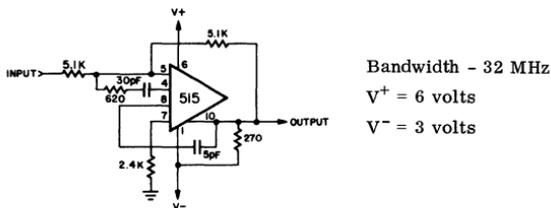
Figure 6 is an amplifier with a gain of 20db. Frequency compensation here is accomplished with the same technique as with the 40db amplifier but the compensating capacitor is larger.



Bandwidth - 22 MHz
 $V^+ = 6$ volts
 $V^- = 3$ volts

Gain - 20db - Figure 6.

When the amplifier gain is to be reduced to unity (0db) in the inverting configuration, an additional compensating network is required. Figure 7 is an example.



Gain = 0db - Figure 7.

The frequency response of the inverting amplifiers, Figures 5, 6, 7 is shown in Figure 8.

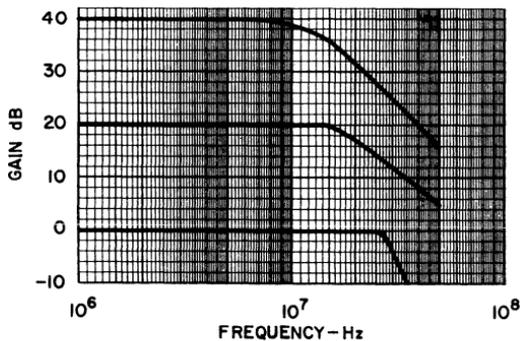


Figure 8.

A 270 ohm pull-down resistor has been included in the above amplifiers to ensure optimum output swing at higher frequencies.



Ralph Seymour

APPLICATIONS MEMO

SELECTING PULL-DOWN RESISTORS FOR THE 515

The output circuits of the 515 consist of emitter followers with 6000 ohm load resistors, Figure 1. When the 515 is to be used to drive loads requiring sink capability of greater than is possible with the 6000 ohm load resistor, an external pull-down resistor may be connected between the 515 output and negative power supply to obtain the necessary sink capability.

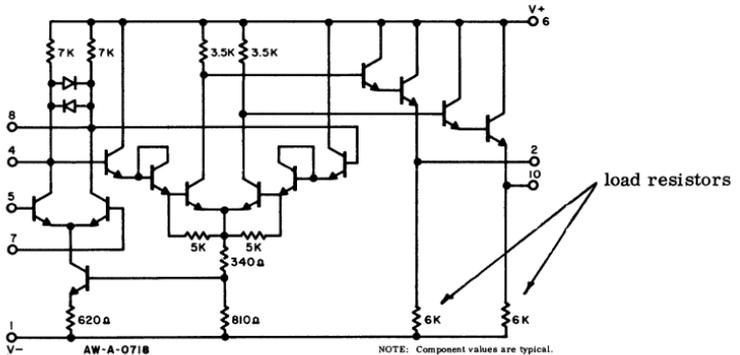
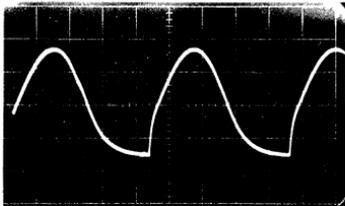
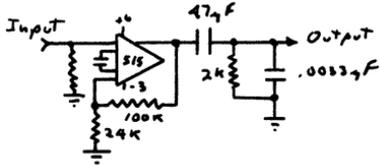


Figure 1 - 515 Schematic

Distortion of the 515 output for negative swings, is indicative of insufficient sink capability. It occurs by "Voltage Divider Action" when the load resistance is reduced, approaching the value of the internal pull-down resistor, and in amplifiers where the 515 output is capacitively loaded and the capacitor discharge rate through the output resistance, is not sufficient for the amplifier output to follow the input for negative going output excursions. Figure 2 (a), shows the effect of insufficient sink capability as obtained in the circuit of Figure 2 (b), Figure 3 (b) shows the effect of the external pull-down resistor as used in Figure 3 (a).

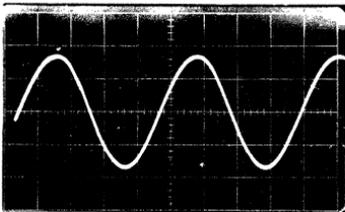


(a)

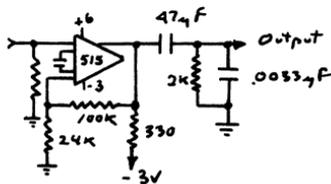


(b)

Figure 2



(a)



(b)

Figure 3

Care must be taken in the selection of the pull-down resistor to ensure that neither the maximum current output rating, 30mA, nor the maximum allowable junction temperature of the device is exceeded. Calculations to determine its minimum value will be shown here.

The maximum allowable junction temperature, T_j , is 150°C and the thermal resistance from junction to case for each package type is:

Package	TO - #	θ_{J-C}
A	116	0.16°C/mW
G	91	0.2°C/mW
K	100	0.2°C/mW

From this data, the maximum allowable 515 internal power dissipation for each package type for each operating temperature range may be obtained.

$$\text{Maximum Internal Power Dissipation} = \frac{T^{\circ}(\text{Junction}) - T^{\circ}(\text{Ambient})}{\theta_{J-C}}$$

<u>Device</u>	<u>Maximum Internal Power Dissipation</u>
SE515G/K	$\frac{150^{\circ} - 125^{\circ}}{0.2^{\circ}\text{C/mW}} = 125\text{mW}$
NE515G/K	$\frac{150^{\circ} - 75^{\circ}}{0.2^{\circ}\text{C/mW}} = 375\text{mW}$
NE515A	$\frac{150^{\circ} - 75^{\circ}}{0.16^{\circ}\text{C/mW}} = 468\text{mW}$

From the Data Sheets, the maximum unloaded power dissipation of the 515 may be obtained by multiplying the total applied voltage (sum of V+ and V-) by the maximum power supply current.

$$P_{\text{max}} = EI = 9 \times 7 \times 10^{-3} = 63\text{mW}$$

Subtracting the maximum internal dissipation from the maximum allowed dissipation, given the excess power capability of the 515.

<u>Device</u>	<u>Excess Power Capability</u>
SE515G/K	125mW - 63mW = 62mW
NE515G/K	375mW - 63mW = 312mW
NE515A	468mW - 63mW = 405mW

For any given load, the power dissipated in the 515 will be a maximum when E_{out} equals one half of the total power supply voltage, therefore if the pull-down resistor is selected to dissipate power equal to the excess power capability of the 515 at a voltage equal to 1/2 the total power supply voltage, the power ratings of the 515 will not be exceeded. The pull-down resistor for single-ended output is selected as follows:

<u>Device</u>	$R = \frac{E^2}{P} = \frac{(E_{\text{supply}} \times 1/2)^2}{P_{\text{ex}}} = \frac{4.5^2}{P_{\text{ex}}} =$
SE515G/K	327 ohms
NE515G/K	65 ohms
NE515A	50 ohms

Note: If both outputs are to have pull-down resistors, the minimum value of each resistor will be twice the values given above.

The resistors tabulated above were calculated with no consideration to the maximum current rating of the device. The minimum pull-down resistance, to limit this output current to the current rating of the device, is determined as follows:

$$R = \frac{E}{I} = \frac{\text{Maximum High Output Level} + |V^-|}{I_{\text{out (maximum)}}$$

$$= \frac{5V + |-3V|}{0.03\text{mA}}$$

$$= 267 \text{ ohms}$$

The minimum value of pull-down resistances for 515 operation at $v^+ = 6V$ and $V^- = 3V$ are:

<u>Device</u>	<u>Single Output</u>	<u>Dual Outputs</u>
SE515G/K	327 ohm	654 ohm
NE515G/K	267 ohm	267 ohm
NE515A	267 ohm	267 ohm

The resistor values tabulated above were calculated with the assumption of infinite load impedance and must be adjusted upward as the circuit load increases. It is recommended that the maximum value of pull-down resistance be used in each application so as to minimize the total power consumed.

It can be concluded, that for single output operation below 116°C , the limiting parameter is output current and from 116°C to 125°C the limiting parameter is internal power dissipation. For dual outputs, the crossover temperature is 99°C .



APPLICATIONS MEMO

LOW VOLTAGE POWER SUPPLIES UTILIZING THE 515

Differential Amplifiers, when using large amounts of negative feedback have very low output impedance, as in the voltage follower of Figure 1.

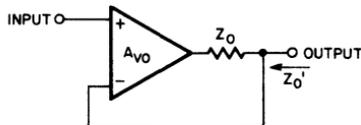


Figure 1

The output impedance of this circuit configuration is the most important characteristic of a constant voltage power supply and indicates that high gain monolithic differential amplifiers or operational amplifiers make excellent constant voltage power supplies. Since monolithic amplifiers have limited current handling capability, they are often used with external power amplifiers to provide the load current required.

This memo will describe the design of two low voltage power supplies utilizing the 515, one suitable for operating Digital Integrated Circuits at +5V and one to supply up to +12V.

Connecting the 515 in the configuration of Figure 2 and adding frequency compensation to ensure stable operation provides the simplest 515 power supply possible.

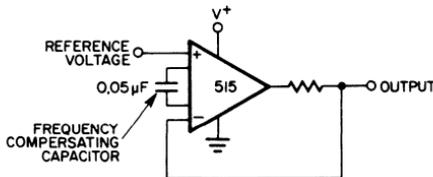


Figure 2

The output voltage of this circuit will be equal to the reference voltage (within a few millivolts) but the range of output voltage adjustment is limited by the +2V to +4.5V common mode range of the 515. The output voltage range may be expanded as shown in Figure 3, by modifying the circuit to give it voltage gain. When $R_1 = R_2$, the voltage gain will be 2 and as the reference voltage is adjusted through the +2V to +4.5V common mode range of the 515, the output voltage range possible will be double or +4V to +9V.

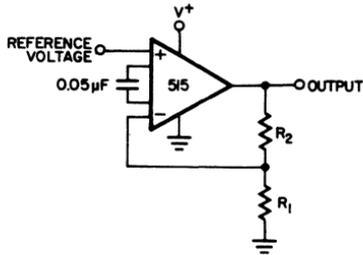


Figure 3

This circuit, while in general is quite satisfactory, will perform somewhat better when the reference voltage is fixed. The output voltage is then set by adjusting the resistance of R_2 (R_2 may be a potentiometer) (Figure 4).

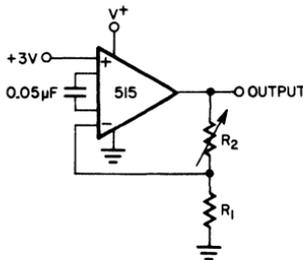


Figure 4

The reference voltage was selected to be near the midpoint of the common mode range, +3V, and will allow power supply output voltages of 3V or more. If lower output voltages are required, the reference voltage may be reduced, but care must be used to ensure that the input common mode range of the 555 is not exceeded. The output voltage of this circuit is:

$$V_{\text{out}} = V_{\text{ref}} \left(\frac{R_1 + R_2}{R_1} \right)$$

Since the absolute maximum supply voltage rating of the 555 is +12 volts, it cannot be used in this circuit configuration to supply voltages larger than approximately 10V. It is ideally suited for applications requiring +5V for integrated circuit logic systems and, if only 30mA of load current is required, it may be used with no power amplifier. Power amplifiers for the 555 may be simple single emitter followers or cascaded emitter followers depending upon the load current requirements. Figure 5 is an example of this type of design.

The output current capability is primarily a function of the power dissipation rating Q_1 and if Q_1 is selected as a 2N697, load regulation of about 1% may be obtained at an output level of +5V at a load of 150mA. Changing Q_1 to a 2N3054 and operating on a heat sink, will allow output currents of over 250mA with 1% load regulation at the +5V level.

R_1 is selected to limit the rectifier 1/2 cycle peak surge current to the rating of the rectifiers selected. R_1 should be as small as possible and the transformer losses should be kept to a minimum to ensure the +5V output level is maintained at the high output current levels and for low AC line voltages.

If the rectifier system is changed to a full wave bridge that utilizes the voltage available across the whole transformer secondary winding, and if an output circuit with voltage gain is incorporated, output currents of over 1 ampere and voltages as high as +12V may be obtained.

Figure 6 is the schematic of such a power supply. Since the voltage across the rectifier output is well over the absolute maximum supply $V+$ rating of the 515, the 515 must be operated from its own power supply consisting of a zener diode, CR5, R_4 and C_6 . In this circuit, the reference voltage is developed from the 515 supply by a voltage divider consisting of R_2 and R_3 . If more stable output voltage versus temperature characteristics is required, a 6.2V temperature compensated zener diode may be used in the reference voltage supply as is done in the circuit of Figure 5. The output circuit consists of a NPN transistor driving a PNP power transistor connected for an unloaded non-inverting gain of about 7. Capacitor C_4 ensures stable operation of the output circuit. If the line in the emitter circuit of transistor Q_2 is broken and the circuit consisting of an epitaxial silicon PNP transistor, Q_3 , and a one ohm resistor, R_{10} , is inserted, a current limiting function is incorporated and the output current cannot exceed 0.85 amps, even under short circuit conditions. Adjusting the value of resistor R_{10} downwards will raise the current limit level. Figure 7 shows the output voltage/output current capability of the supply. The vertical line near the center of the curve shows the effect on the output characteristic when current limiting is inserted.

Figure 8 shows the response of the power supply output to a 0.7 amp pulsed load.

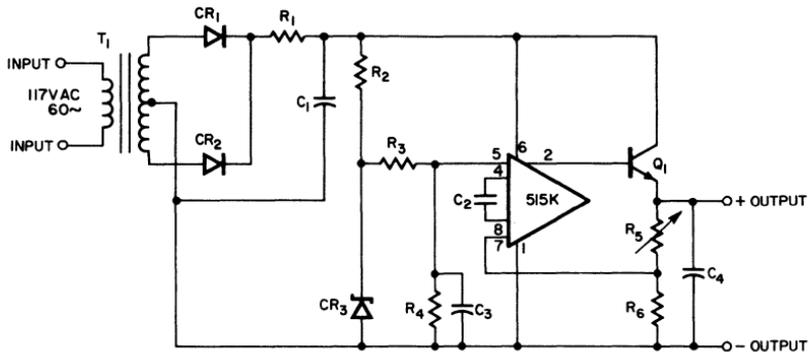


Figure 5

Table 1. Parts List for Figure 5.

C ₁	2000 μ F at 10V
C ₂	.05 μ F
C ₃	10 μ F at 10V
C ₄	10 μ F at 10V
R ₁	See text
R ₂	56 ohms, 1/2 watt, 5%
R ₃	3.3K, 1/2 watt, 5%
R ₄	3.0K, 1/2 watt, 5%
R ₅	5K, potentiometer
R ₆	3K 1/2 watt, 5%
T ₁	12.6V, C.T. Filament Transformer, (Stancor, P-8130)
Q ₁	2N697 for 150mA output 2N3054 for 250mA output
CR ₁	Silicon rectifier
CR ₂	Silicon rectifier
CR ₃	6.2V, 1/2 watt, zener diode

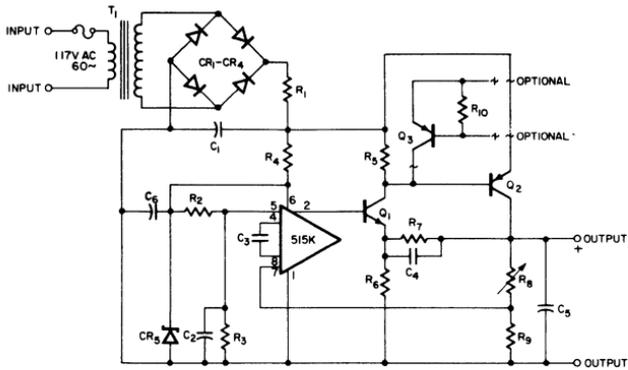


Figure 6

Table 2. Parts List for Figure 6 - Power Supply

C ₁	4000 μ F, 25V, Sprague Type 39D
C ₂	10 μ F, 10V
C ₃	0.033 μ F
C ₄	0.1 μ F disc
C ₅	22 μ F at 25V
C ₆	10 μ F at 10V
R ₁	0.5 ohms, 5 watts 10%
R ₂	6.2K, 1/2 watt, 5%
R ₃	3.0K, 1/2 watt, 5%
R ₄	240, " "
R ₅	68, " "
R ₆	39, " "
R ₇	240, 2 watt, 5%
R ₈	5K potentiometer
R ₉	1.5K, 1/2 watt, 5%
R ₁₀	1 ohm, 5 watts, 5%
T ₁	12.6V at 2 amp, Stancor, P-8130
Q ₁	2N3054
Q ₂	2N4901
Q ₃	2N2905
CR ₁ through CR ₄	1.5 amp bridge - Motorola MDA 942-1
CR ₅	9.1V, 1/2 watt, zener, 1N5239

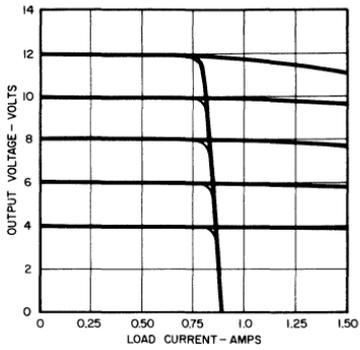


Figure 7. Loading Characteristic



Figure 8. Response to Pulsed Load

APPLICATIONS MEMO

FREQUENCY COMPENSATION FOR THE 516

The 516 is a high gain differential amplifier with differential output. Its characteristics make it useful as an operational amplifier.

When operational techniques are used, i.e., control of circuit characteristics with negative feedback, the open loop response of the amplifier must be adjusted to ensure stable closed loop operation.

Figure 1 is the open loop frequency response of the 516 with a Bode plot superimposed. Three significant corner frequencies are present.

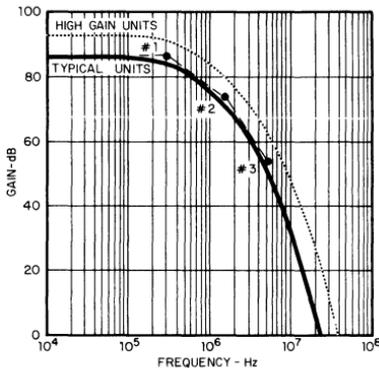


Figure 1

In applications which do not require the bandwidth to be optimized, the amplifier may be compensated for the ideal roll-off condition of 20dB per decade or 6dB per octave with a single capacitor connected between the collectors of the first stage. This technique lowers the first corner frequency of the amplifier and depresses the second corner frequency to the unity gain level. The new first corner frequency may be determined by dividing the second corner frequency of the open loop response of the amplifier by its open loop gain in volts per volt.

$$f_c = \frac{1.6 \times 10^6}{18,000} \text{ Hz}$$

$$f_c = 50 \text{ Hz}$$

The capacitor is selected to have a reactance at 50 Hz that is equal to the low frequency impedance between the collectors of the first stage. This impedance is approximately 32,000 ohms. It may be readily measured by operating the amplifier in the open loop configuration and connecting a resistor between the collectors. The resistor value that causes the gain to be reduced by one half, will be equal to the impedance level at the compensation terminals.

$$C = \frac{1}{\omega R}$$

$$C = \frac{1}{6.28 \times 50 \times 32,000}$$

$$C = 0.1\mu\text{F}$$

Figure 2, is the open loop response of the 516 with the 0.047 μF capacitor connector between the compensating pins.

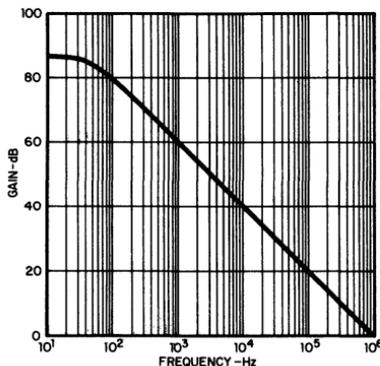


Figure 2

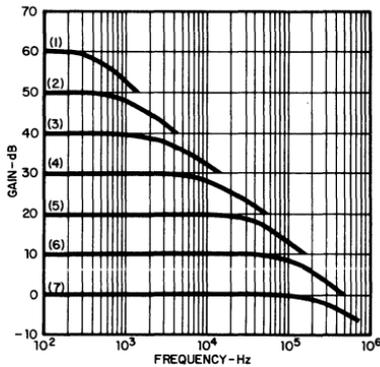
This compensating technique is used for the amplifiers of Figure 3, and should also be used for voltage follower and integrator applications.

If instability occurs in the unity gain configurations, add a 4.7 resistor in series with the 0.1 μF capacitor.

When amplifiers of greater bandwidth than those shown in Figure 3, are desired, a modification of the previous compensating technique is required. The compensating network is altered to include a resistor in series with the capacitor (Figure 4) and the value of each is selected to give the desired response. The most useful technique for selecting the resistor and capacitor value is graphical and may be done on the open loop frequency response plot.

The technique is as follows:

- Construct a vertical line at the frequency of the second corner figure, 1.6 MHz.
- Extend the desired low frequency gain line to its intersection with the second corner frequency line.
- From the intersection of the gain line and the second corner frequency line construct a line, back toward the origin, with a slope of -20dB decade. The intersection of this line with the open loop frequency response curve is the new first corner frequency.



GAIN (dB)	R_{in}	R_f	R_b
60 (1)	1k	1M	1k
50 (2)	3.16k	1M	3k
40 (3)	10k	1M	10k
30 (4)	10k	316k	10k
20 (5)	10k	100k	9.1k
10 (6)	10k	31.6k	7.5k
0 (7)	10k	10k	5.1k

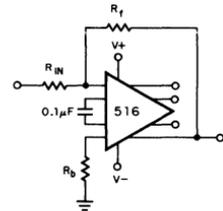


Figure 3

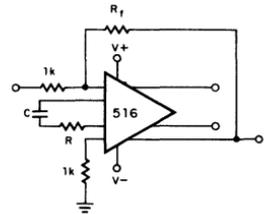
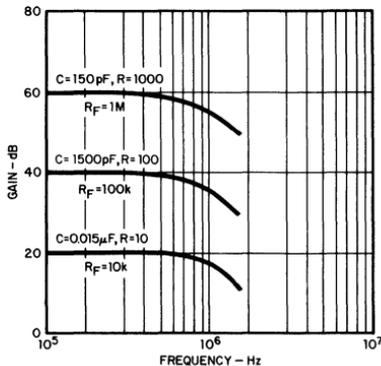


Figure 4

- (d) The compensating capacitor is selected in the manner identical to that used in the first compensating technique.
- (e) The resistor is selected to cancel the roll-off (caused by the compensating capacitor) at high frequencies.

$$\begin{aligned}
 R &= \frac{\text{Closed Loop Gain (V/V)}}{\text{Open Loop Gain (V/V)}} \times \text{Compensating Terminal Impedance} \\
 &= \frac{\text{Closed Loop Gain (V/V)}}{32,000} \times 32,000 \\
 &= \text{Closed Loop Gain} \times 1 \text{ ohm}
 \end{aligned}$$

Figure 5 shows the graphic construction for the three amplifiers of Figure 4.

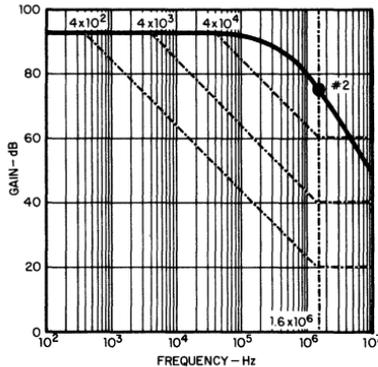


Figure 5

In the examples given above, $V^+ = V^- = 15$ volts.



APPLICATIONS MEMO

SE518 AS AN ANALOG COMPARATOR

Basically the SE518 is a medium gain, high frequency, differential amplifier with its output stage designed to drive digital circuits. Fan-out for typical DTL loads is "1", however, provision is made to increase the sinking capability with the connection of an external resistance. A strobe input is available that will allow the user to disable the device through the application of a gating signal:

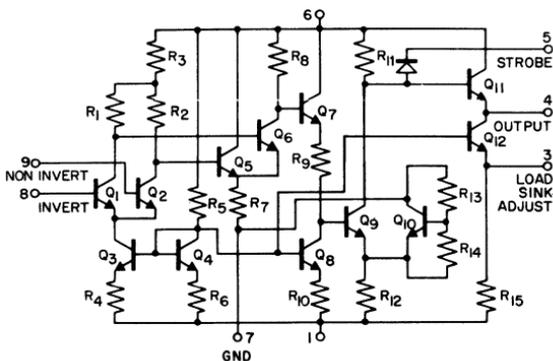


Figure 1

The circuit is designed to be operated from two power supplies, the negative supply voltage being one-half of the positive supply voltage. The sum of these two voltages should be in the range of 6 to 9 volts. The open loop gain is a function of power supply voltages, increasing from 500 with +4 volt and -2 volt supplies to 2200 with +6 volt and -3 volt supplies.

The input offset voltage is that voltage measured at the input when the output level is adjusted to +1 volt and will be within 5mV of 0 volts. The common mode input range

increases with increasing power supply voltages, being +2.0, -0.8 volts for +4 volt, -2 volt power supplies and +2.8, -1.3 volts for +6 volt, -3 volt power supplies. Large differential input overdrives (up to 3 volts) will cause no change in the output state.

The output impedance is typically 50 ohms. The output source current is limited primarily by H_{fe} of the output emitter follower (Q11) and its pull-up resistor (about 1.4K), however, it should never be allowed to become so large that any of the device maximum ratings are exceeded. The output sink capability will be a minimum of 2mA and may be adjusted up to 10mA. The sink current may be doubled by placing a resistor (R_A) between pins 1 and 3 (about 200 ohms). When the SE518 is used to drive a digital device and is operating at its negative output limit (about -1.0 volts), it will cause the isolation diode of the digital device to become slightly forward biased. Since the sink current of the SE518 is limited, this is of no consequence in most of Signetics' devices, but circuits that employ resistor/capacitor/diode input configurations (SE124, SE161) will present operational difficulties and their inputs should be buffered by a gate (BG).

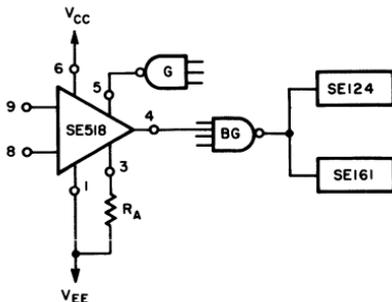


Figure 2

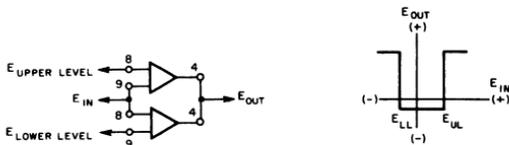
Connecting the strobe input to a voltage in the range between V_{CC} and V_{EE} will inhibit all output signals more positive than the strobe input voltage. When the SE518 is used to drive logic loads, grounding the strobe input with a logic signal from a logic gate will give the desired gating. For linear applications where complete signal cut-off is required, the strobe input must be returned to pin 1. Electronic gating requires sink capability determined by the output emitter follower transistor pull-up resistor (1.4K) and the voltage at pin 6.

The following systems and circuits are given as possible applications for the SE518. Some have been tested and some have not, so the user is cautioned to evaluate all applications on his own breadboard before incorporating them into the system.

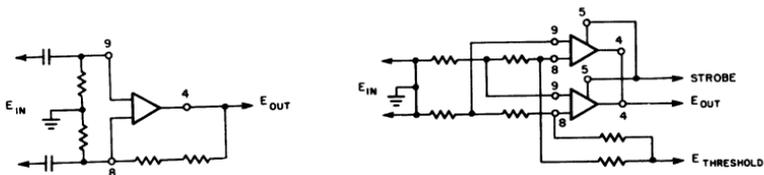
1. Level Detector



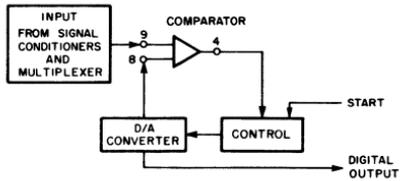
2. Double Ended Level Detector



3. Sense Amplifiers



4. Analog To Digital Converter





APPLICATIONS MEMO

K. Wehrli

UTILOGIC NOR GATES AS LINEAR AMPLIFIERS *

1. Introduction

The transfer characteristics of the Dual Nor Gate SU315 and SU316 (V_{in} vs. V_{out}), as given on SU315 data sheet Figure 2, show a possible application as a linear amplifier. The data below is presented so as to provide the user with sufficient information to allow him to develop his own linear amplifiers incorporating this device.

Only connection as an AC amplifier was taken into consideration.

2. Open Loop Gain

The device is biased for linear operation with resistor R_B (See Figure 1). The open loop gain was measured at a frequency of 1 kHz. Inputs not used are tied to the ground.

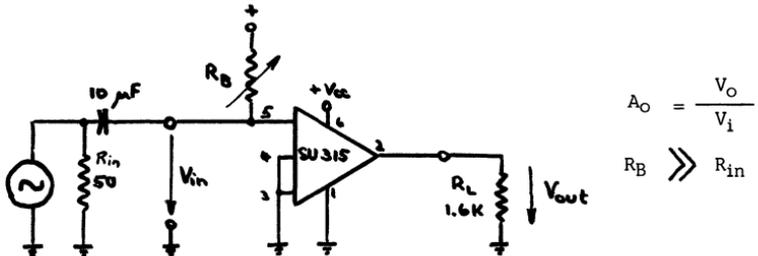


Figure 1 - CONFIGURATION FOR MEASUREMENT OF OPEN LOOP GAIN

The open loop gain increases with increasing supply voltage and is also a function of the input bias voltage (see Figure 6).

3. Negative Feedback

The output voltage is fed back through resistor R_F (see Figure 2). This negative feedback stabilizes the gain and increases the bandwidth.

* This information also applies to the Utilogic II NOR gates.

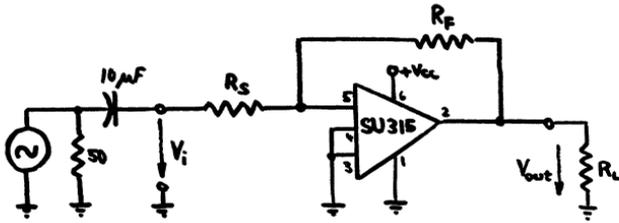


Figure 2 - VOLTAGE FEEDBACK

The voltage gain of above circuit can be approximately determined through the equation:

$$A_v \approx \frac{A_o}{1 + \frac{R_S}{R_F} A_o}$$

A_o = open loop gain valid at the corresponding operating point.

First, the feedback resistor (R_F) is selected to bias the input for linear operation and maximum output swing, and then R_S is selected to obtain the desired gain.

The curves (see Figure 7) show output voltage vs. input voltage of the amplifier with DC negative feedback.

The output DC level is stable for power supply voltage changes. When the power supply is changed from +4 to +5.5 volts, the output level increases 30 mV for $R_F = 10$ kOhms and 70 mV for $R_F = 22$ kOhms.

3.1 Frequency Response

The frequency response was measured with negative feedback set for a voltage gain of approximately 5 and 10 for each of the power supply voltages, namely $V_{CC} = +4.5$ and $V_{CC} = +5.5$ volts. The bandwidth may be considerably enlarged through insertion of a small bypass capacitor between the center of R_F and ground. The bypass capacitor is selected to provide this maximum bandwidth without high frequency peaking (see Figure 8).

Following values are typical for the SU315:

V_{CC} (volts)	R_S ($k\Omega$)	R_F ($k\Omega$)	C (pf)	$V_{O\ DC}$ (volts)	A_V		f_{3dB} (MHz)
					(V/V)	(dB)	
+4.5	1.2	10	0	2.0	5.1	14.2	8.0
			2		5.1	14.2	9.1
+4.5	0.27	10	0	2.2	10.6	20.5	4.1
			15		10.6	20.5	5.0
+5.5	3	22	0	2.2	4.9	13.8	6.4
			2		4.9	13.8	6.9
+5.5	1	22	0	2.2	10	20	4.5
			6		10	20	5.5

3.2 Output Swing

The maximum output swing corresponds to that value which might be expected from the transfer characteristic V_{in} vs. V_{out} (Figure 7). No decrease has been observed within the useful frequency band. It will be 3.5 volts peak to peak when $V_{CC} = +4.5$ volts and 4.4 volts peak to peak when $V_{CC} = 5.5$ volts, and it can vary ± 0.1 volt from unit to unit.

4. Input and Output Impedance

The applied feedback reduces input and output impedance. The input impedance may be determined by the following equation:

$$Z_{in} \approx R_S + \left(\frac{R_F \cdot Z_i}{R_F + A_O Z_i} \right)$$

All measurements are taken under the following conditions:

feedback ratio for voltage gain of 5 and 10

power supply voltage $V_{CC} = +4.5$ volts, or $V_{CC} = +5.5$ volts

frequency $f = 1$ kHz

temperature $T = 25^\circ\text{C}$

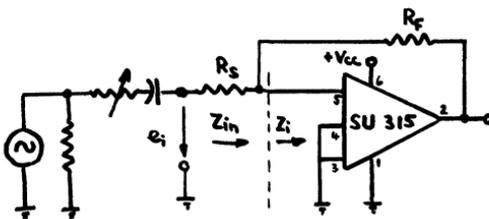


Figure 3 - CONFIGURATION FOR INPUT MEASUREMENTS

Following input impedances have been measured:

V_{CC} (volts)	R_F (kOhms)	R_S (kOhms)	Z_{in} kOhms)
4.5	10	1.2	1.8
5.5	22	1.0	1.9
4.5	∞	0	25
5.5	∞	0	25

Output impedance was measured with input shorted through capacitor C_S as shown in the diagram below:

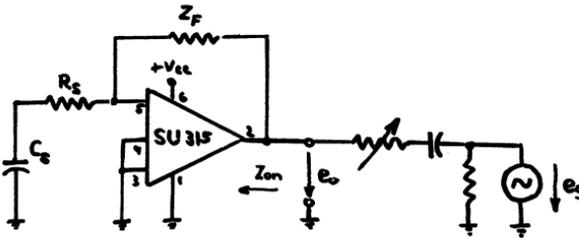


Figure 4- CONFIGURATION FOR OUTPUT IMPEDANCE MEASUREMENT

The following are results of Z_{on} measurements made on several typical devices:

V_{CC} (volts)	R_F (Ohms)	Z_{on} (Ohms)
+4.5	∞	70
+5.5	∞	70
+4.5	10	24
+5.5	22	36

5. Amplifier Gating

The amplifier may be gated with one of the unused inputs.

The following schematic shows the configuration for a gated amplifier:

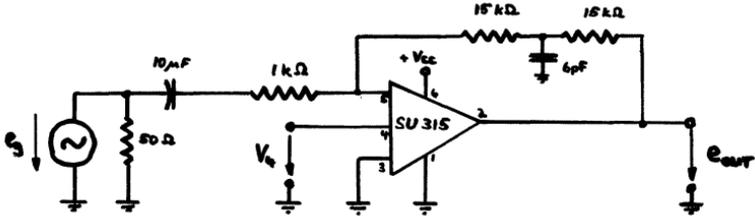
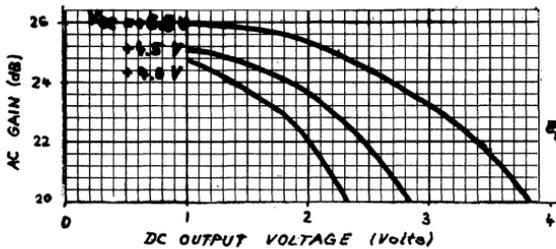


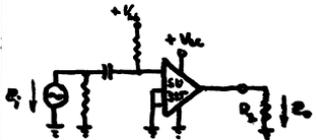
Figure 5- GATED AMPLIFIER

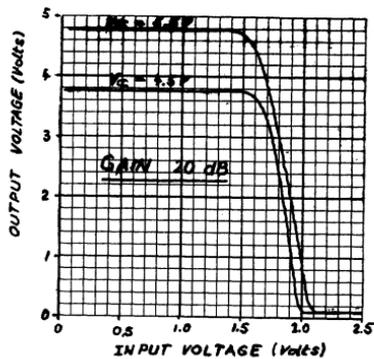
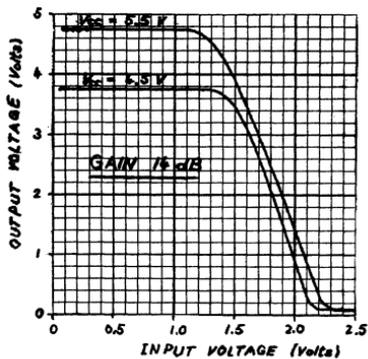
The feedthrough was measured at 3 different frequencies. Gating action begins at approximately +1.7 volts.

Gate voltage $-V_4$ (volts)	Feed through (dB)		
	50 kHz	2 MHz	9MHz
2.2	-62	-59	-50
3.0	-67	-60	-48
3.5	-70	-61	-48

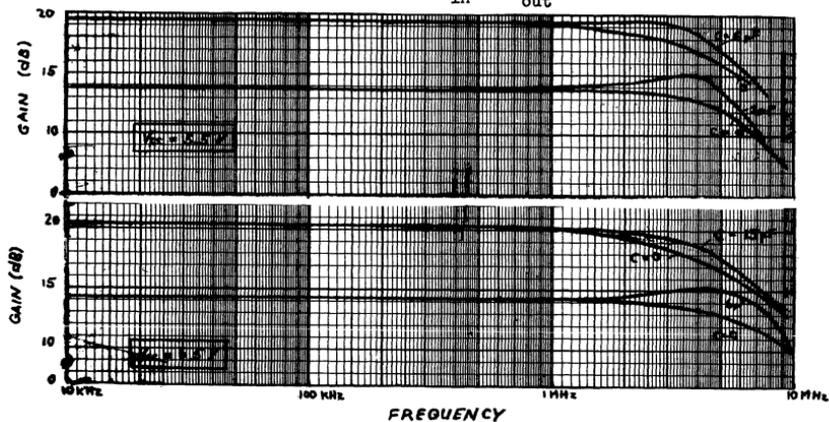


-Figure 6- OPEN LOOP GAIN vs OUTPUT VOLTAGE





-Figure 7- TRANSFER CHARACTERISTIC V_{in} vs V_{out} with FEEDBACK



- Figure 8- FREQUENCY RESPONSE

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APPLICATIONS MEMO

A DOUBLY BALANCED MODULATOR

The Signetics 510 consists of a pair of differentially connected transistor pairs, each with its own current generator. Proper interconnection of the pairs, Figure 1, permits the circuit to function as a doubly balanced modulator. (The bias network is left open or both bias connections are tied to the common emitter substrate pin at the option of the user.) A typical output waveform is shown in Figure 2.

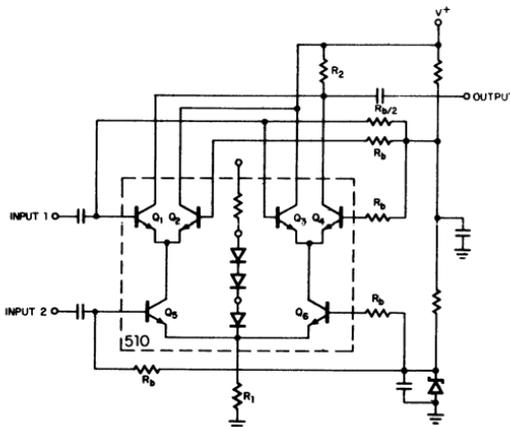


Figure 1

Applications for doubly balanced modulators will be found in many types of systems, in particular, communications and control systems. Application examples are:

1. Phase Comparators
2. Product Detectors
3. FM Detectors
4. Synchronous Demodulators (Color TV Receivers)
5. Suppressed Carrier Amplitude Modulators (with proper filtering, single sideband)
6. Balanced Mixers - local oscillator not present in the output signal

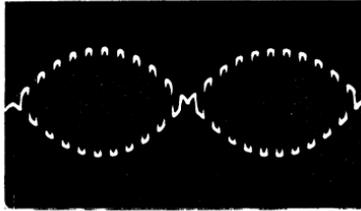


Figure 2

The design of a doubly balanced modulator using the 510 is not difficult. First to be determined is the manner in which the inputs are biased. If only one power supply is available, the suggested biasing technique uses a voltage divider consisting of resistors or resistors and a zener diode with capacitive coupling of the inputs. Figure 1 is an example of this configuration. However, if both positive and negative power supplies are available, the configurations of Figure 3a and 3b may be used. These circuits will provide a direct coupled input which will prove most useful when very low input frequencies (to DC) are to be used.

The load impedance may be either resistive or reactive, depending upon the user requirements. R_1 determines the total output current and should be selected in conjunction with the load impedance and power supply voltages to prevent transistors Q_1 through Q_4 from saturating under any condition.

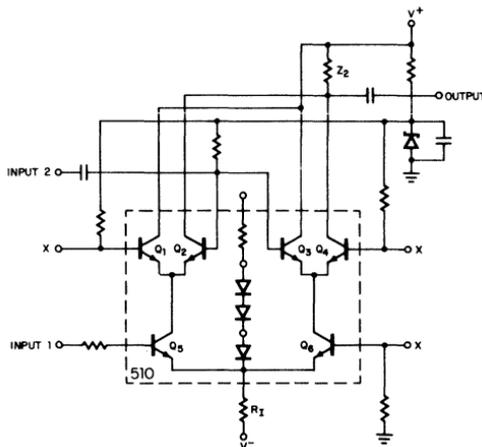


Figure 3a

Although the 510 is a monolithic device and the transistors are well matched, additional circuitry is required to give the optimum carrier and/or modulation balance. The inherent balance of the circuit is best realized by minimizing the value of the resistors in the transistor base circuits. The smaller these resistors can be made, the smaller the effect of the input bias current offsets and the better the circuit balance will be.

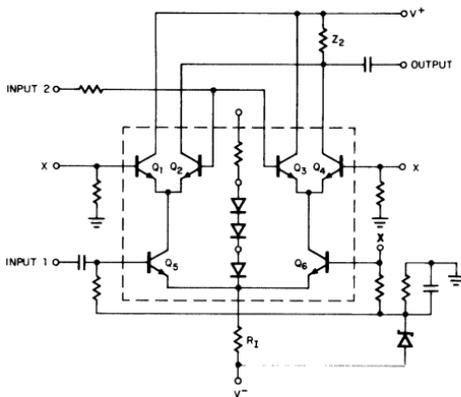


Figure 3b

None of the circuits in Figures 1, 3a or 3b shows any provision for circuit balance. Two balancing techniques are available for use with these circuits. The simplest involves making one base resistor for each differential pair adjustable as is shown in Figure 4. For non-critical applications, the number of potentiometers may be reduced, but each reduction in the number will impair the carrier suppression or modulation balance. For most applications, two potentiometers, one in the base circuit of Q_4 and one in the base circuit of Q_6 , will prove adequate. The second balancing technique is indicated by the circuit of Figure 5. Connecting a circuit of this type with "X" of Figure 5 to each or any "X" of Figures 3a and 3b will allow the base currents of each differential pair to be adjusted for circuit balance.

Modulation input levels should be small, in the order of 50mV peak-to-peak, or less, if low distortion is desired. If a sinusoidal output waveform is desired, the carrier input level should also be in the order of 50mV peak-to-peak. If a square wave output is satisfactory, input levels of up to 5V peak-to-peak are permissible if care is taken in selecting the load impedance to ensure that saturation of the output transistors does not occur.

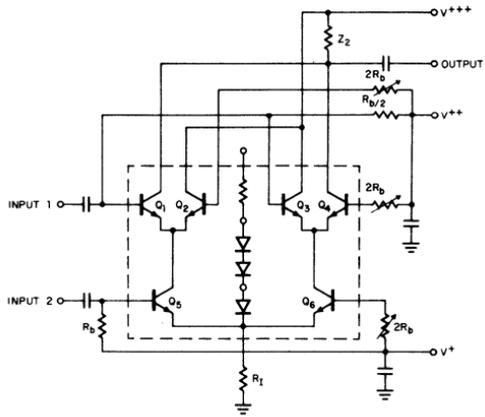


Figure 4



Figure 5



APPLICATIONS MEMO

FREQUENCY COMPENSATION OF THE 5709

When high gain operational amplifiers like the Signetics 5709 are used in practical amplifier circuits, compensation networks must be used to prevent oscillations. This memo discusses the requirement and lists some widely used compensation networks.

The stability of a practical feedback amplifier can be predicted by inspection of an asymptotic Bode plot of the loop gain of the circuit. A commonly used rule is that stability of the circuit is ensured if the asymptotic Bode plot of the loop gain crosses the 0db axis at a slope of 20db/decade. This corresponds to a "phase margin" of at least 45° , and indicates that the total accumulated phase shift around the amplifier feedback loop at frequencies where the loop gain is unity or better will be less than 315° (135° plus the 180° DC amplifier inversion), or 45° less than that required to sustain oscillations.

The need for operational amplifier compensation in a practical circuit can be illustrated by an example. Suppose a designer, needing an amplifier circuit with a gain of 40 db starts with an operational amplifier whose uncompensated gain is shown by the asymptotic Bode plot of Figure 1(a). Applying the usual formulas, he arrives at the circuit illustrated in Figure 2.

The asymptotic Bode plot of the uncompensated closed loop gain for this circuit is shown in Figure 1(b).

When the designer constructs this amplifier circuit, he will find that it exhibits severe high frequency peaking and may even oscillate if stray circuit capacitances are sufficient to induce slight additional phase shifts. This behavior could have been predicted by examination of the Bode plot of the loop gain of the circuit, shown in Figure 1(c). This plot crosses the 0db axis at a slope of 40db/decade. Note that the plot of the loop gain is not the same as the plot of the closed loop gain, it is the algebraic difference (in db) between the plot of open loop gain and closed loop gain.

AMPLIFIER BODE PLOTS

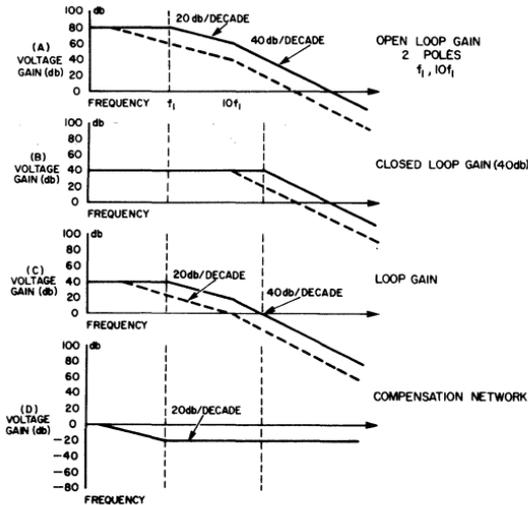


Figure 1

To correct the peaking or oscillations in the above circuit, the designer must add a compensating network to the operational amplifier. The characteristics of this network are such that the open loop gain will be modified to cause the loop gain of the circuit to cross the 0db axis at a slope of 20db/decade. The asymptotic Bode plot of a compensating network is given in 1(d). The resulting modified gain plots for the compensated amplifier are shown as dotted lines in Figures 1(a), 1(b), and 1(c).

While calculations for obtaining the correct values of the compensation network can be tedious, as the example may suggest, the user of the 5709 is fortunate in that these values have been known for some time. 5709 compensation network values are shown, along with the appropriate Bode plots, in Figure 3. These networks are given for the non-inverting configuration. If it is desired to utilize the inverting amplifier configuration, the capacitance values shown for unity gain compensation have to be halved. The exact relationship is $C_{inv} = C_{non\ inv} \cdot \frac{1}{1 + \text{inverting gain}}$. Note that, for gains of greater than 20 dB, the difference is less than 10% and may be neglected. This means that the values shown may be used for both inverting and non-inverting configurations where the closed loop gain is 20 dB or greater.

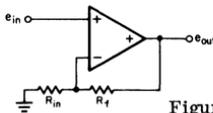


Figure 2

$$G_v \approx \frac{R_f + R_{in}}{R_{in}}$$

$$G_v = 100 \text{ (40db)}$$

$$R_f = 99 R_{in}$$

Although for best results the compensating networks should be chosen for the exact gain required, stability may be ensured for all possible gain configurations by use of the network calculated for unity gain. This results in the so-called "unconditionally stable" operational amplifier. Use of the unity gain network with the 5709, although convenient, results in a circuit limited to slew rates of around 0.1 volt per microsecond. For this reason, it is recommended that unity gain compensation be used with the 5709 only where necessary; for example, in integrators and unity gain amplifiers.

It has been found that the networks shown work well over a wide range of R_f and R_{in} . An exception appears to be where very large (≈ 10 meg) resistors are used in high gain (1000 or greater) circuit configurations. In these circumstances, oscillations can result if the 60 db compensation network is used. This situation may always be corrected by use of the 40 db networks.

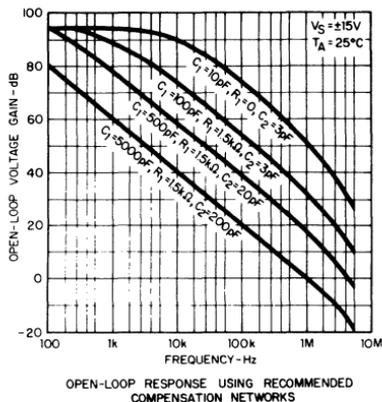
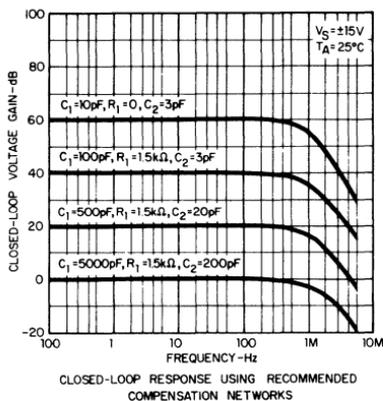
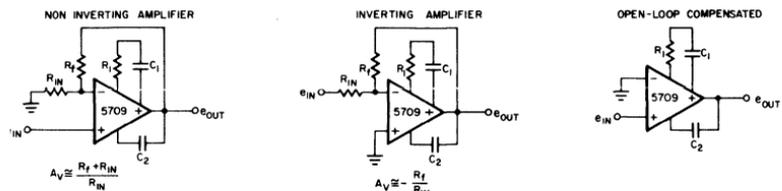


Figure 3



APPLICATIONS MEMO

A SIMPLE LINEAR INTEGRATED CIRCUIT CURVE TRACER

Two of the most important parameters of Linear Integrated Circuits having differential inputs are voltage gain and input offset voltage. These parameters may be read directly from a plot of the transfer characteristic of the device. This memo will describe a very simple curve tracer which, when used with an oscilloscope, will display the transfer characteristic of most Signetics linear devices.

Figure 1 shows the transfer characteristic of a typical linear device, the Signetics 5709. Note that the unit saturates at approximately +12 and -12 volts and exhibits a linear transfer characteristic between +10 and -10 volts. From the slope of this linear portion

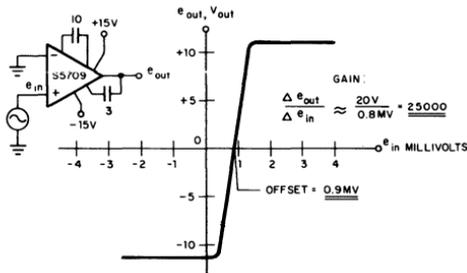


Figure 1

of the transfer characteristic, and from the point where it crosses the e_{in} axis, the voltage gain and offset voltage may be determined. It can be seen that the voltage gain of the device under test (D. U. T.) is 25,000 and its input offset voltage is 0.9mV. Figure 2 shows an alternate curve from a window detector type of device, the Signetics 525 Sense Amplifier.

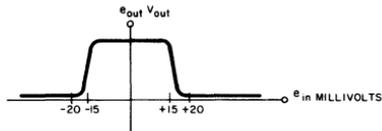


Figure 2

A simple circuit to display the curves of Figures 1 and 2 on an oscilloscope is shown in Figure 3. A 60 Hz, 44V p-p sinewave is applied to the horizontal input of the

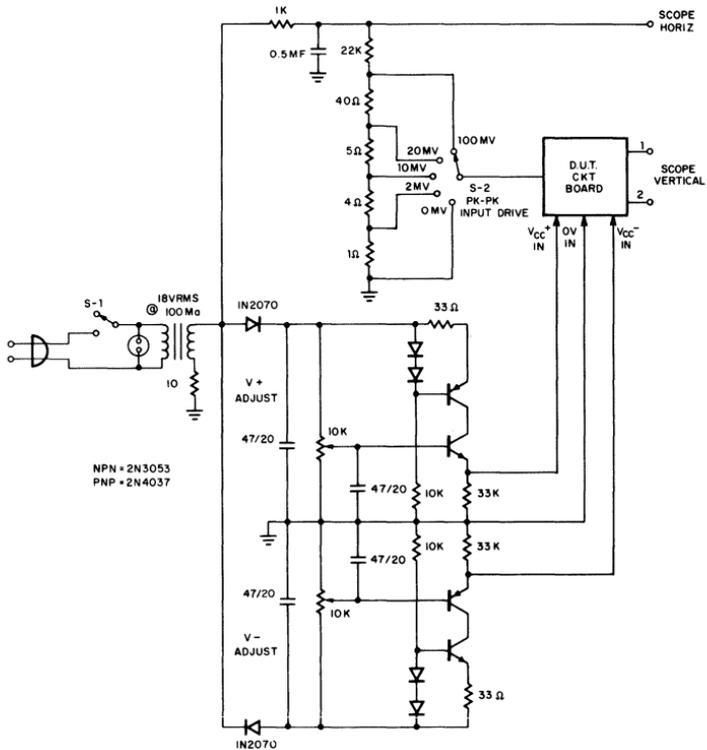


Figure 3

oscilloscope and an attenuated version of this sinewave is applied to the input of the D.U.T. The output of the D.U.T. drives the vertical input of the scope. For providing V^+ and V^- to the D.U.T., the tester uses two simple adjustable supply regulators, both current limited at 25mA. D.U.T. sockets are shown for most Signetics linear devices. Input drive to the D.U.T. may be selected by means of S-2 as shown.

To use the curve tracer, first preset the V^+ and V^- supplies with an accurate meter. The supply voltages are somewhat dependent on AC line regulation and should be checked periodically. The horizontal gain of the scope may be set to give a convenient readout

of the peak-to-peak D.U.T. input signal corresponding to the setting of S-2. As some devices have two outputs, a second output line (vertical 2) has been provided for these devices. The 515, 516, 518, 526, 517, 5709 and 5710 will display curves of the form of Figure 1. For the 515 and 516, output 2 will be inverted from Figure 1. (These are amplifiers having differential outputs.) For the 526 comparator, output 2, which is the output of the Digital buffer, will be inverted in form from Figure 1. The 525 sense amplifier will have an output of the form of Figure 2, while the 5711, which has been arranged to perform a similar function, will have an output inverted from Figure 2.

This Curve Tracer is not intended to perform highly rigorous tests of all device parameters. It is, however, a reasonably accurate means of determining the gains and offsets of actual devices.

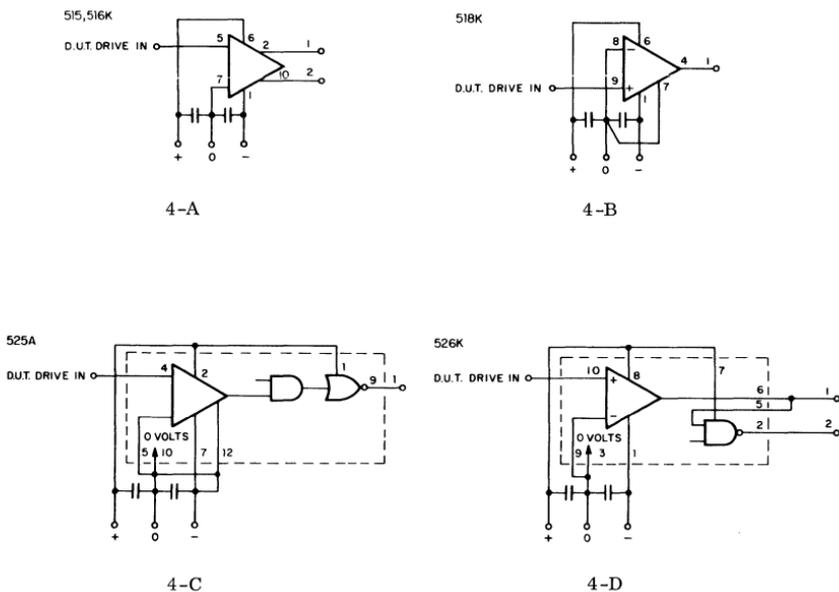
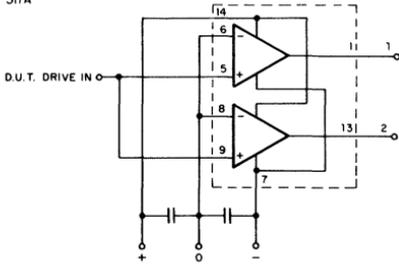


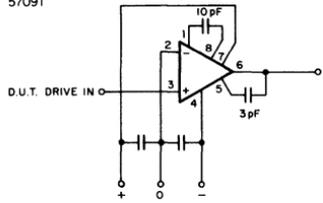
Figure 4

517A



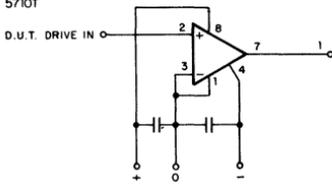
4-E

5709T



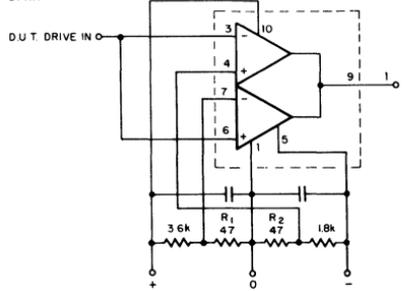
4-F

5710T



4-G

5711K



4-H

Figure 4 (cont)



APPLICATIONS MEMO

5733 VIDEO AMPLIFIER

The 5733 is a high quality, differential input/differential output, video amplifier with voltage gains as high as 400 and bandwidths as great as 120 MHz. Included among its numerous applications are video amplifiers for communication and display devices and sense amplifiers for state-of-the-art memory and magnetic recording systems.

The 5733 has four gain options. The first three options are provided by simply interconnecting two gain select pins (Figure 1). Interconnecting G_{1A} and G_{1B} gives the highest gain available, 400, and interconnecting G_{2A} and G_{2B} produces a gain of 100. When all gain select pins are left open, the lowest gain setting of 10 is obtained. If gains other than those obtained by direct pin interconnection are required, a gain setting resistor, selected according to the curve of Figure 2, may be connected between pins G_{1A} and G_{1B} .

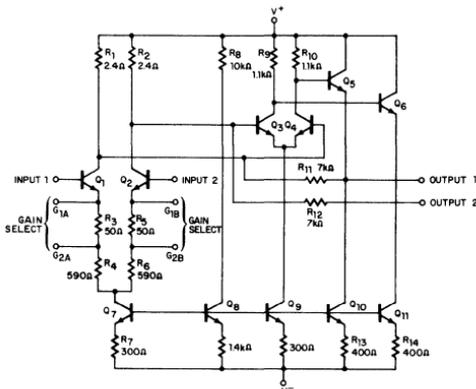


Figure 1. Application of the 5733 Video Amplifier (Schematic)

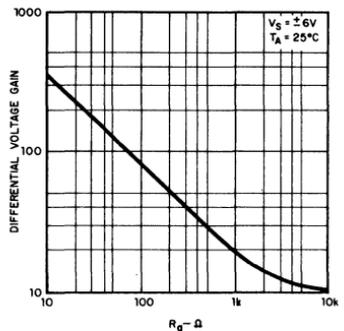


Figure 2. Voltage Gain as a Function of R_g

Three facts are called to the user's attention:

1. The gains given above are differential gains and the single-ended output gains of the 5733 are one-half of the differential output gains.

2. The circuit 3dB bandwidths are a function of and are inversely proportional to the gain settings.
3. The differential input resistance is an inverse function of the gain setting. The approximate input resistance of a typical unit is given by the following equation:

$$R_{in} \approx 200 \left[\frac{1280 R_g}{1280 + R_g} + 20 \right] \text{ ohms}$$

In applications where the source is a magnetic transducer, the input bias current path may be directly through the transducer to ground. In the event that capacitive coupling to the source is required, a resistor from each input to ground is needed (see Figures 3 and 4). Because all 5733s are not ideal devices and have input offset currents, the selection of the input bias resistors is a compromise. To reduce the loading on the source, the resistors should be large; but to minimize the output DC offset, they should be small - ideally 0 ohms. Their maximum value is set by the maximum allowable output offset and may be determined as follows:

1. Define the allowable output offset (assume 1.5V).
2. Subtract the maximum 5733 output offset (from the data sheet). This gives the output offset allowed as a function of input offset currents ($1.5V - 1.0V = 0.5V$)
3. Divide by the circuit gain (assume 100). This refers the output offset to the input.

$$\frac{0.5}{100} = .005V$$

4. The maximum input resistor size is:

$$\begin{aligned} R_{max} &= \frac{\text{Input Offset Voltage}}{\text{Max Input Offset Current}} \\ &= \frac{.005V}{3\mu A} \\ &= 1,667\Omega \end{aligned}$$

In the design of the 5733, one of the prime requirements was speed. In a monolithic device, this precludes the use of PNP transistors and the use of standard level shifting techniques which are required to provide an output level equal to the input level. The 5733 will therefore have an output common mode voltage, typically +2.9V, which means that for most applications, capacitive coupling to the load is necessary. An exception to the rule is a differential amplifier with an input common mode range greater than +2.9V as is shown in Figure 3. In this circuit, the 5733 drives a Signetics 511B

Linear Integrated Circuit connected as a differential cascode amplifier. This amplifier is capable of differential output voltages of 48V peak-to-peak with a 3dB bandwidth of approximately 10 MHz (depending on the capacitive load). For optimum operation, R_I is set for a no signal output level of +18V. The emitter resistors, R_E , were selected to give the cascode amplifier a differential gain of 10. The gain of the composite amplifier is adjusted at the gain select point of the 5733.

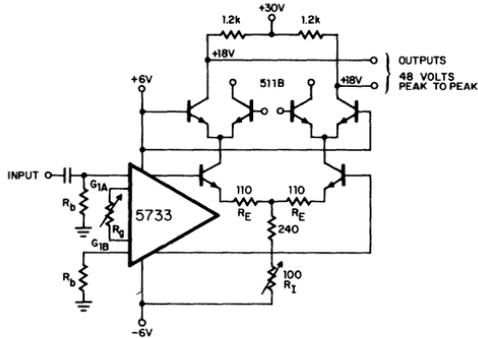


Figure 3. Video Amplifier with High Level Differential Output

In sense amplifier applications, interfacing directly with logic gates may be desirable. The circuits of Figure 4 show typical techniques. Note that the gates shown are high input impedance types, Utilogic in Figure 4a and DTL in Figure 4b. No TTL gates are shown. Attempts to utilize this technique for TTL gates were made but results were poor because of the instability of the gates in their threshold region.

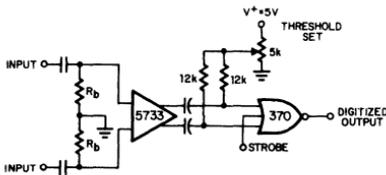


Figure 4b.

Interfacing to Utilogic DTL NAND Gates

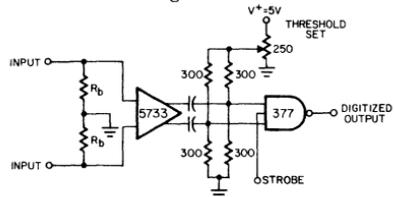


Figure 4a.

Interfacing to Utilogic NOR Gates

The 5733 is well suited as a preamplifier for magnetic tape or disc memories. A typical NRZ (Non-Return-to-Zero) system is illustrated in Figure 5. The requirements for the preamplifier are not extreme, but the following parameters are desirable:

1. Differential Input with a good Common Mode Rejection Ratio
2. High Gain
3. High Input Impedance

4. Low Phase Distortion

The 5733 meets all of the above requirements, needs no frequency compensation and requires a minimum of additional discrete components for biasing and interfacing to the remainder of the system.

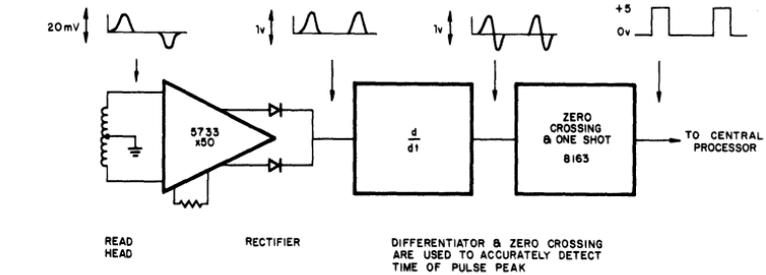


Figure 5. NRZ Encoded Tape Playback System

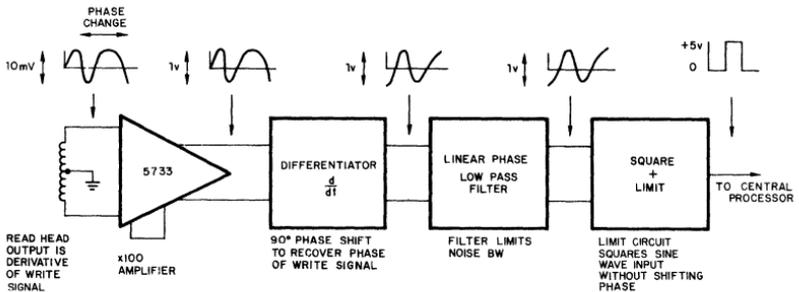


Figure 6. Typical Phase Encoded Playback System

For memories requiring a higher bit rate, phase encoded systems, as shown in Figure 6, are used. Since the information in this system is incorporated in the phase content of the signal rather than the amplitude as with the NRZ system, excellent phase linearity as well as large bandwidth is required. The high input resistance and low input capacity of the 5733 ensures that the loading on the read head will be minimized preventing Q reduction.

In the application of the 5733, the power supplies should be well by passed and a reasonable amount of isolation is required between input and output circuitry to ensure stable operation.

SECTION 7
TIMING CIRCUITS



APPLICATIONS MEMO

W. T. Booth

DTL MULTIVIBRATORS

Frequently, users have a need for oscillators to use as clock pulse generators, etc. Also, they may have need for a one-shot, but are reluctant to stock SE160's or SE161's due to cost or parts inventories. Several possibilities exist for generating multivibrators from the standard DTL product.

SE161's may be connected back-to-back to form a very simple oscillator. The Y output of each is used to trigger the other. However, some means must be provided for starting. The addition of an inverting gate as "C" in Figure 1 serves very nicely; closing and opening SW1 will generate the necessary starting pulse. The device may be made self-starting by adding gates "A" and "B". The capacitance at input b will cause a delay and allow the output of "C" to go high. When the voltage at b reaches the switching threshold, the outputs of "A" and "C" will fall and the oscillator will be started. The oscillator may be gated by pulses entered at a or c - when the input pulse is low the feedback loop is opened. The use of gating pulse will cause oscillations to begin at the first rise at the gating pulse.

The period of oscillation will be approximately $2 C_T$; if C_T is picofarads, T is nanoseconds. The range of operation is about 5 mcs to 0.25 cycles. The C_T 's do not have to be equal, but should not be unbalanced enough to require a duty cycle in excess of 75%.

Figure 2 shows an oscillator based on the split-clock binary. The interval is determined by the RC time-constant of C_T and the 2K input resistor of the SE116. When the threshold voltage is reached, the fall of the SE116 output will generate a clock pulse to cause the binary to change state. The frequency will be about 900 kc at $C_T = 0.1$ uf and will change quite linearly with changes in C_T . Because switching occurs at the temperature-dependent threshold of the gate, frequency will increase (exponentially) as temperature increases.

For frequencies below 25 kc the fall-time at the gate output is not sharp enough to effect triggering. Maximum frequency is about 2mc.

The oscillator may be made to lock to sync frequencies greater than the natural frequency by introducing the sync through the optional input gates. If this option is not used, fan-out may be increased by connecting R_C and S_C to ground.

The oscillator of Figure 3 is similar to that above but is not frequency sensitive since the direct inputs are utilized. However, it has a stable state with both Q and \bar{Q} of the Binary high so either the SE180 or some other auxiliary starting method must be provided.

Frequencies are the same as for the CS729 version above, but may be extended to 100 cps at $C_O = 2\mu f$. A pulse output with as high as 80% duty cycle may be obtained by the use of unbalanced individual capacitors to ground rather than a common capacitor between expansion inputs. Capacitance to ground is only one-half as effective as when in common.

This oscillator may also be locked to input frequencies above the natural frequency. The sync signal is entered at the clock input. Also, S_C must be connected to Q and R_C to \bar{Q} as indicated. It may be gated by introducing a gating pulse at "a".

A one-shot version of the above oscillator is shown in Figure 4. For a given C_T , timed intervals will be about one-fourth of the periods of oscillation for the preceding oscillators. The period of this oscillator is quite sensitive to temperature, but may be stabilized appreciably by paralleling C_T with a thermistor.

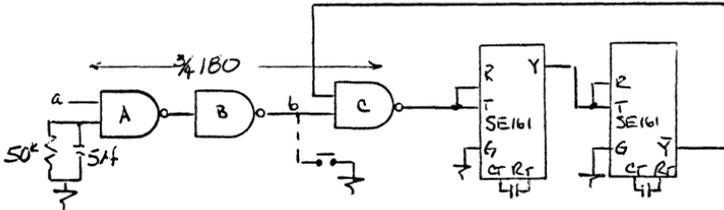


Figure 1 - SE 161 Oscillator

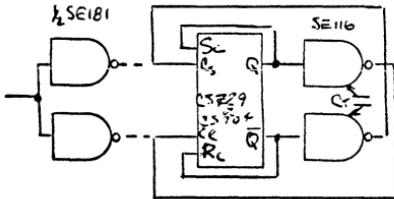


Figure 2 - CS729 Oscillator

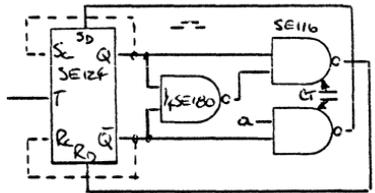


Figure 3 - SE 124 Oscillator

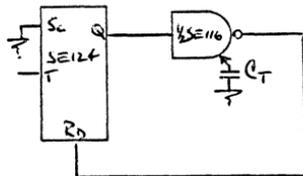


Figure 4 - SE 124 One Shot



APPLICATIONS MEMO

K. Wehrli

A TECHNIQUE TO INCREASE PULSE WIDTH OF THE SE160

One shots are frequently required with pulse widths larger than those obtainable with the build-in RC time constant. The technique described below increases the width of the SE160 output pulse by 80% which is generally sufficient to allow a capacitor case-size reduction.

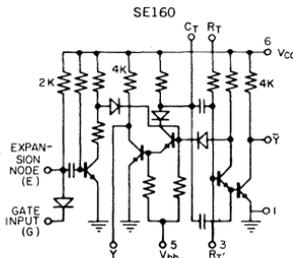
The output pulse width may be increased by connecting the external capacitor between pins 3 and 7 instead of pins 3 and 4. (See Figure 1). Use of this technique requires that the Y output should not be used to drive loads since this output is no longer buffered. If Y output is required, it may be obtained by inverting \bar{Y} . When the external capacitor is connected from pin 3 to pin 7, the maximum obtainable duty cycle will be approximately 30%. An external pull-up resistor of 1.5k ohms from pin 7 to V_{CC} increases the maximum obtainable duty cycle to about 80% and improves the rise time of the output pulse Y.

The following variation may be useful if both outputs are required. The same pulse width increase of 80% may be obtained when inverting output \bar{Y} with a power gate (e.g. SE155) and connecting the external capacitor between inverter output and pin 3. In this configuration, output characteristics Y and \bar{Y} remain the same as given in the data sheets except for the increased pulse width.

The relative pulse width change with temperature is slightly improved. (See Figure 3).

See Application Memo #17 which describes a solution for obtaining extremely large RC time constants.

Note: The maximum value for the resistor of the RC time constant (9k ohms/20pF) should not exceed 10k ohms to provide sufficient base current for transistor saturation.



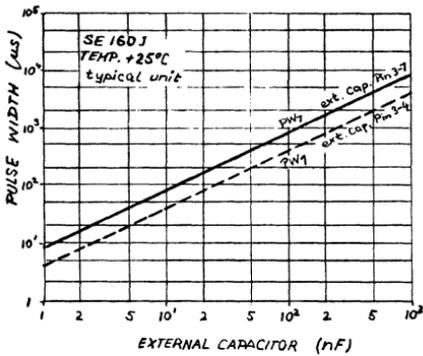


Figure 1

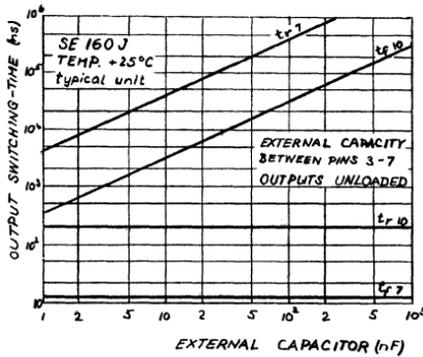


Figure 2

$$V_6 = V_2 = +4 \text{ V}$$

$$V_5 = -2 \text{ V}$$

$$V_1 = 0$$

$$R_L = 510 \text{ Ohms}$$

$$C_{\text{ext}} = 100 \text{ pF}$$

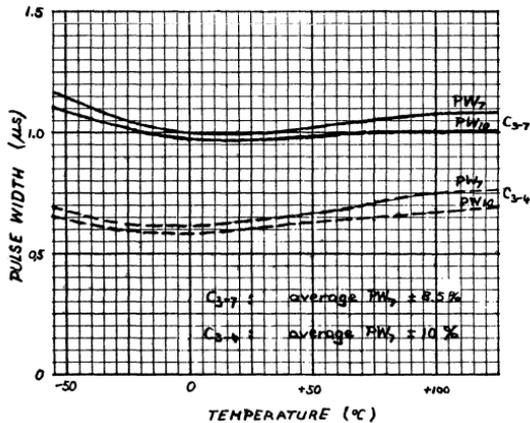


Figure 3



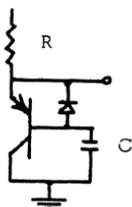
APPLICATIONS MEMO

W. T. Booth

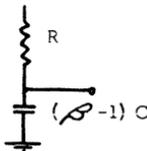
MULTIPLICATION OF CAPACITOR VALUES

Occasionally there arises a need for very long RC time-constants, but capacitor values cannot be allowed to grow to the huge values required because of physical size or recharging currents.

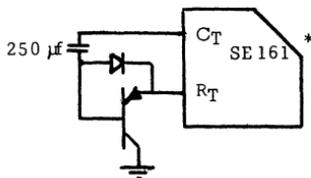
An emitter-follower transistor stage may be employed to multiply the capacitor size by the current gain of the transistor ($B - 1$) as in the sketch below. The diode provides a discharge path on negative-going edges and should be a high-conductance type.



Approximate equivalent



This technique has been used as shown below to increase the output pulse width of the SE161J to 14 seconds. Recovery currents normally limit the output pulse width of the SE161 to 2 seconds. Maximum duty cycle is determined by the $250\mu\text{f}$, not the $14,000\mu\text{f}$ equivalent. Transistor beta was approximately 50.



*Also applies to SE161J, SE162J and S8162A/J



APPLICATIONS MEMO

GENERATION OF 3-PHASE SQUARE WAVES

Accurate three phase reference signals that are square waves phased 120° apart may be easily generated with digital integrated circuits. Three phase signals of this type may be used as a reference for DC to AC converters, as clock signals for three phase logic systems, or in any application requiring accurate three phase signals.

The three phase square wave signals are shown in Figure 1 with respect to the clock input which is not required to be a square wave. The truth table indicates the various states that are in the required sequence. The possibility of the three phase generator locking up in a secondary loop (000,111) during power turn on or due to noise is eliminated with a gate which detects the 111 state and steers the generator into the correct sequence.

Implementation of the three phase generator with the various Signetics binaries and gates is shown in Figures 2 through 6. The D-binary is used in Figure 2, the J-K binary with NAND gates in Figure 3, the J-K binary with OR, NOR gates in Figure 4, the R-S binary with NAND gates and collector logic in Figure 5, and the dual R-S binary (424) with the 440 in Figure 6. The inverter in Figure 6 may be the other half of the 440 gate with the input applied to one AND gate and the inputs to the other AND gate grounded.

The input clock frequency must be six times greater than the desired three phase output frequency because the three phase generator divides the input frequency by six. The binaries are synchronously clocked, hence the phase relationship errors at the outputs are only the differences in switching speeds of the binaries, typically a few nanoseconds.

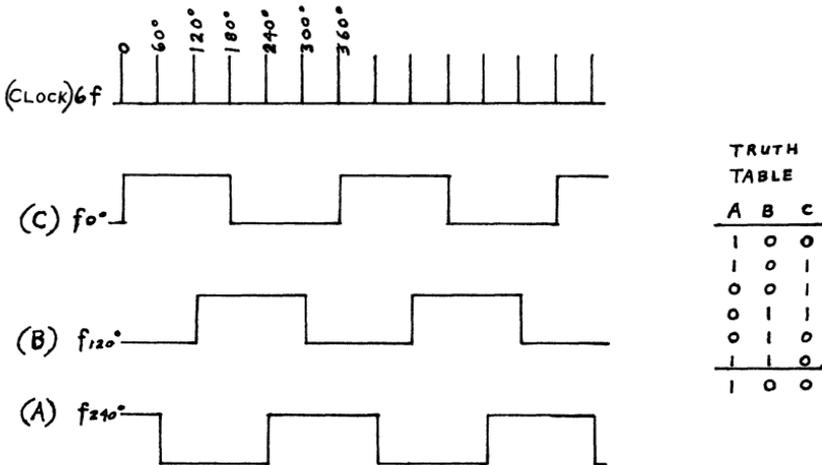


Figure 1

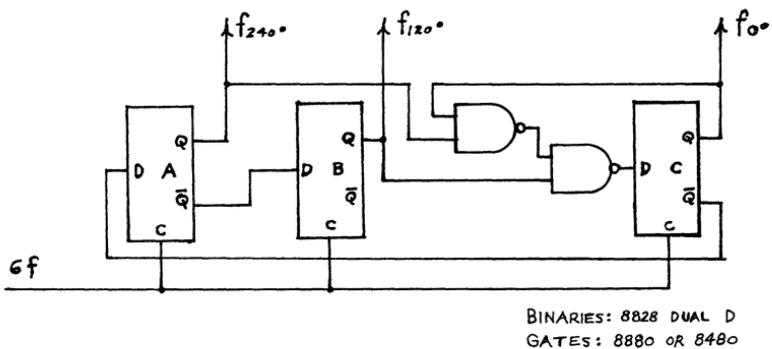


Figure 2

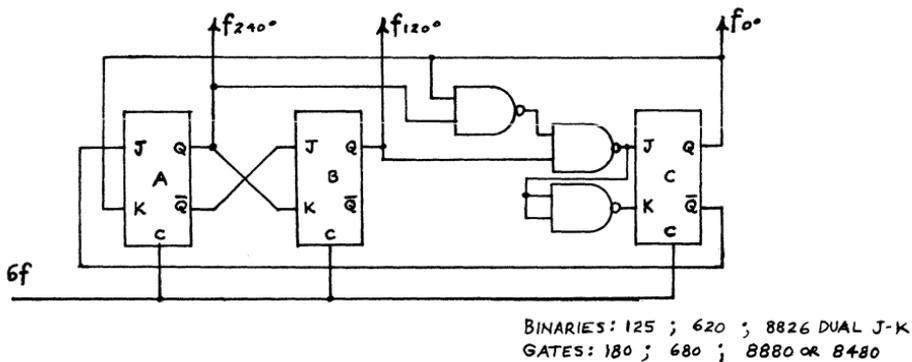


Figure 3

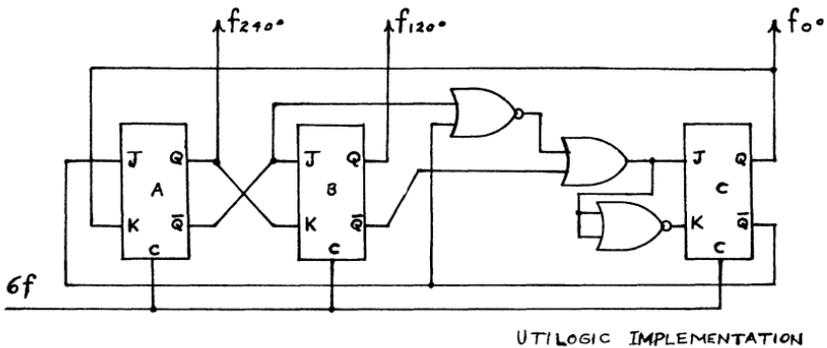


Figure 4

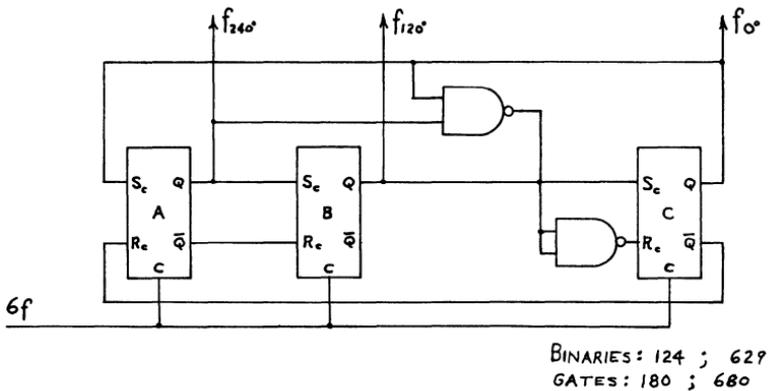


Figure 5

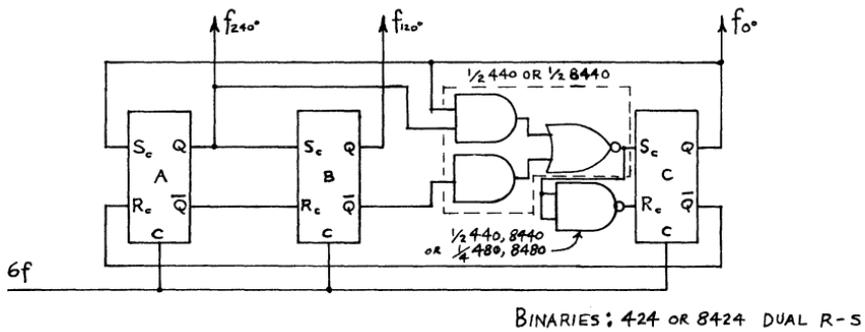


Figure 6



APPLICATIONS MEMO

TV SYNC GENERATORS

Typical television systems use a display system that scans twice during each frame. The first scan sweeps the odd numbered lines and the second scan sweeps the even numbered lines. This is called interlaced scan and is used to reduce the flicker perceived by the human eye. To maintain the interlace, the ratio of the horizontal scan frequency to the vertical scan frequency must be accurately controlled. This is the function performed by the synchronizing generator.

The horizontal and vertical sync pulses required may be accurately generated using digital techniques. Two methods for generating sync pulses for 525 line TV systems will be described in this memo with emphasis on the frequency divider portion of the generators.

A block diagram of the first method is shown in Figure 1. A 31.5 KHz voltage controlled master oscillator is divided by 2 to generate horizontal sync pulses and by 525 to generate vertical sync pulses. This method then generates $525/2 = 262\ 1/2$ horizontal pulses for each vertical sync pulse and provides a stable fixed interlace.

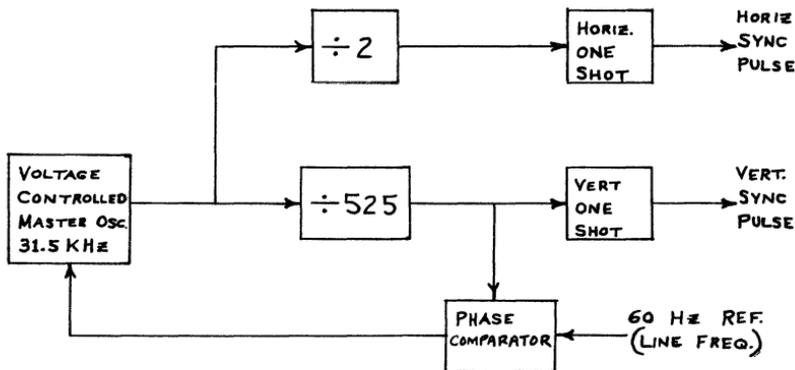


Figure 1

The divide by 525 may be implemented with a single 10 bit counter as shown in Figure 2. The divider counts a binary sequence up through 524 and is then reset to 0 via the gating structure. Gate G_1 detects the 524 state and provides feedback to prevent the A binary from becoming a ONE, the output of gate G_2 allows the 525th clock pulse to reset the C and J binaries and the ONE-ZERO transition of the C output ripples the D binary to ZERO. The E binary is prevented from becoming a ONE by the feedback from J. The P₁ and K inputs of the I binary are connected to gates G_1 and G_2 to prevent the counter from lock-up should the counter enter a forbidden state when power is first applied.

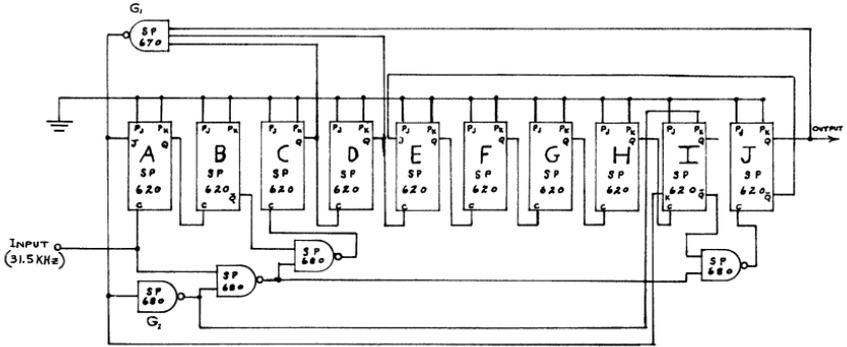


Figure 2

The divide by 525 may also be broken up into subdivisions. Typical subdivisions are 3, 5, and 7 which may be cascaded ($3 \cdot 5 \cdot 5 \cdot 7 = 525$) to yield a frequency division of 525. Logic diagrams for 3, 5, and 7 dividers are shown in Figures 3, 4, and 5 implemented with 600-series devices. The 5 divider may be implemented very efficiently with the 1280 array as shown in Figure 6. The A flip-flop of the 1280 is not required for division by 5, hence it may be used to provide the divide by 2 for the horizontal sync pulse. Other Signetics logic lines may be used to implement the 3, 5, and 7 dividers with only minor design modifications.

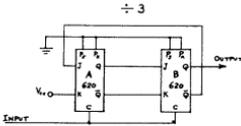


Figure 3

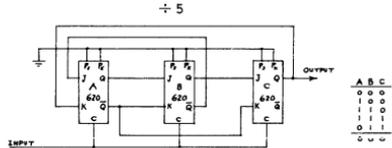


Figure 4

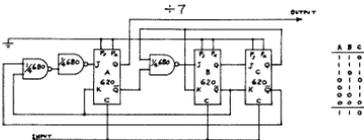


Figure 5

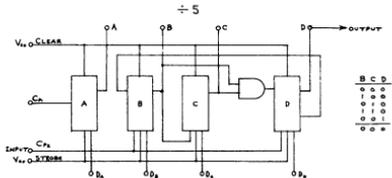


Figure 6

the counter will skip to one of the two counts shown in Figure 8 depending upon the state of the Y binary. The A through E binaries are disabled by the feedback from \bar{Q} of the I binary to the J input of the A binary. The input clock pulse is gated through gate G_1 which is enabled by feedback from the Q output of the I binary. Gate G_2 logically OR's the output of the E binary and gate G_1 . Gates G_3 and G_4 enable the G binary to toggle to the logical ONE state and also enable one input to the G_6 binary. The output of gate G_6 is then determined by the state of the Y binary, i. e., when Y is logical ZERO the output of gate G_6 will be ZERO and the F binary will remain ZERO at the next clock time, when Y is logical ONE the output of G_6 will be ONE allowing F binary to toggle to logical ONE at the next clock time. The input pulse now clocks the F, G, H, and I binaries until overflow occurs. At this time the A binary is enabled and the feedback gates disabled, hence the counter again counts the normal binary sequence until the 256 count is reached. The connections to the K and P_K inputs of the E binary prevent the counter from locking up should the counter enter a forbidden state when power is first applied. The \bar{Q} outputs of the I and Y binaries are applied to the vertical sync one-shots as shown in Figure 9. The waveform at Z is a function of \bar{I} and \bar{Y} , the Z output switches to logical ZERO when the \bar{Y} input switches to ZERO and switches to a logical ONE for time T_1 when \bar{I} is ZERO and \bar{Y} switches to ONE. The width of T_1 is adjustable from 0 to approximately $50\mu\text{sec}$ with the 10K ohm potentiometer. The waveform at Z is applied to a second one-shot that triggers on trailing edges, i. e., each time waveform Z makes a transition from logical ONE to ZERO the vertical sync output is a logical ONE for time T_2 ($T_2 \approx 0.6 (R + 4K) C$, $R_{\text{max}} = 4K$ ohms). The T_1 time delay allows adjustment of the vertical sync pulse timing with respect to the horizontal sync pulses to provide the variable interlace.

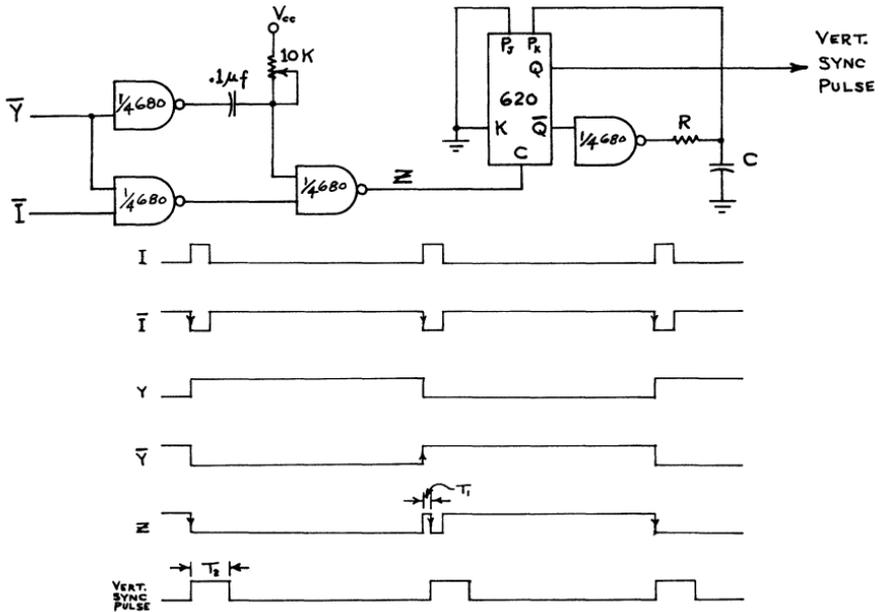


Figure 9



R. Seymour

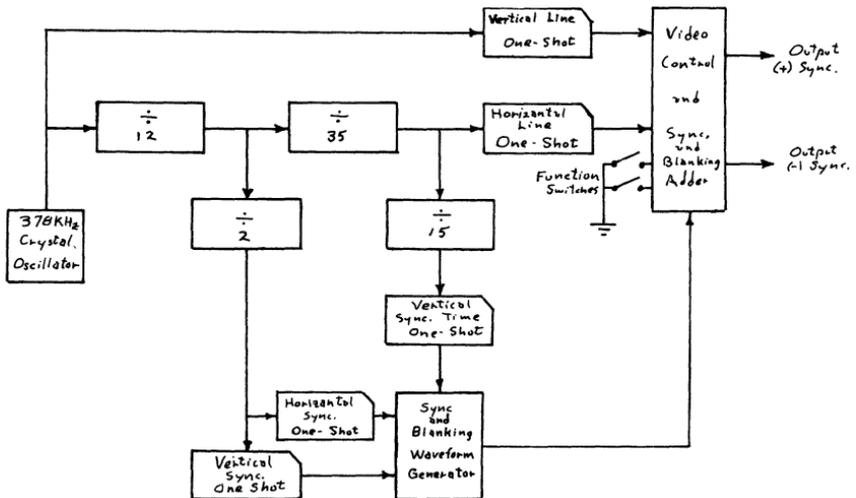
APPLICATIONS MEMO

TELEVISION PATTERN GENERATOR

For a television display system to provide a good rendition of the video information presented to it, its sweep circuits must be adjusted for optimum linearity. In addition, color television display systems, using the shadow mask tube, will require beam convergence adjustments to ensure color registration over the complete screen surface.

The linearity adjustments are divided into two groups, those affecting the horizontal linearity and those affecting the vertical linearity. Horizontal adjustments may be made with a vertical line presentation and vertical adjustments may be made with a horizontal line presentation. The convergence adjustments may be made with a white dot presentation.

Figure 1 is the block diagram of a system to provide the video signals that will cause the desired line or dot display to appear on the screen, or if both horizontal and vertical lines are activated simultaneously, a cross-hatch pattern to be displayed.

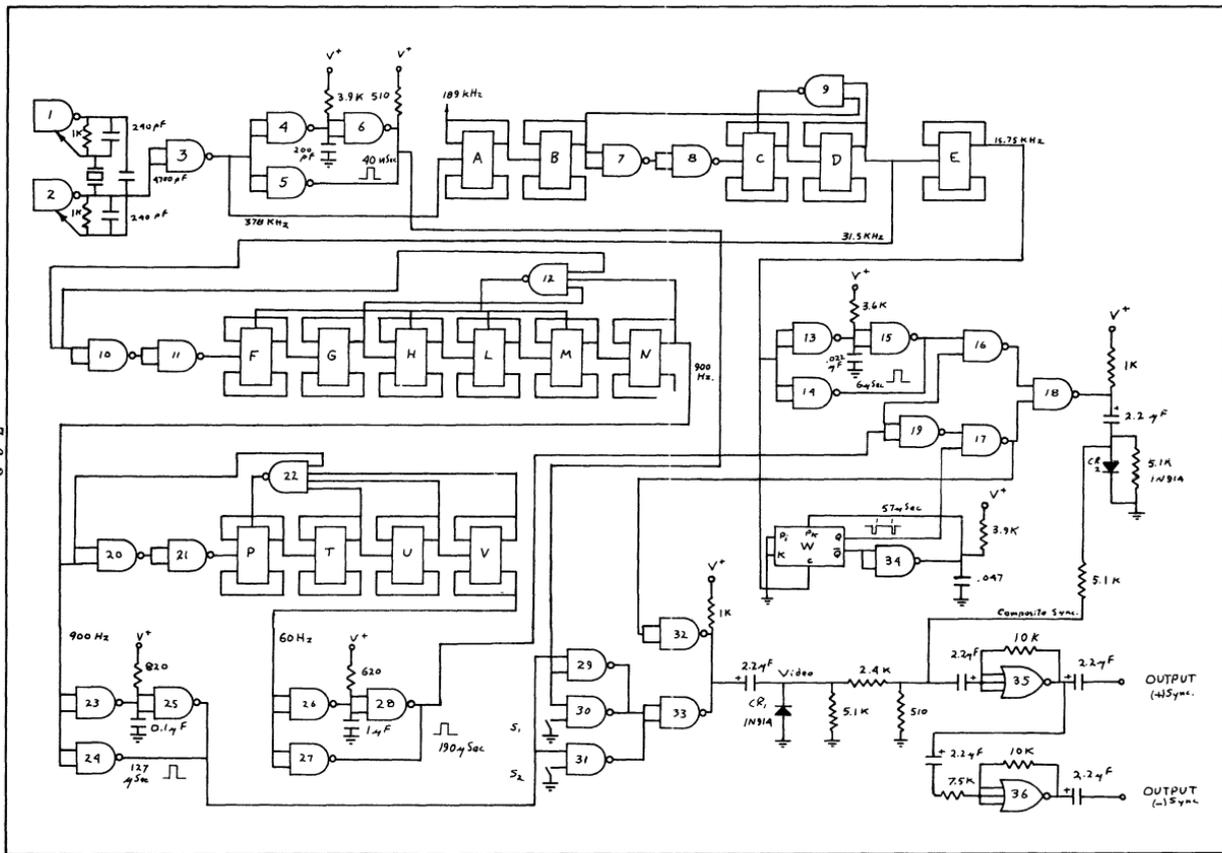


BLOCK DIAGRAM - FIGURE 1.

The system uses counting techniques, as described in Application Memo No. 55, to generate the required video signals and to provide a synchronizing waveform for stable sweep synchronization. Since digital techniques are used, the system is insensitive to power supply variations and no warm-up period is required to ensure a stable display. Although the counters will not be disturbed by power supply variations, the one-shots, used to generate the lines and dots, are constructed from NAND gates and are somewhat power supply sensitive. They, therefore, should be set-up for the desired pulse width at the selected power supply voltage (a power supply voltage fluctuation will only cause the dot and line widths to change and in no way affect the operation of the system).

The clock frequency was chosen as 378 kHz. and is obtained from a crystal controlled oscillator. The oscillator drives the vertical line one-shot and a divide by 12 counter which provides the 31.5 kHz. pulse needed for the generation of the 525 line, interlaced scan, synchronizing waveform. The 31.5 kHz. pulse is divided by 2 to obtain 15.75 kHz. and divided by 35 to obtain 900Hz. The 15.75 kHz. pulse is used to drive the horizontal synchronizing pulse one-shot and the vertical sync pulse one-shot. The 900 Hz. pulse drives the horizontal line one-shot and the divide by 15 counter. The output of the divide by 15 counter is 60 Hz. and operates the vertical synchronizing time one-shot which controls the synchronizing and blanking waveform generator. The outputs of the horizontal line and vertical line one-shots, under the control of the function switches, and the synchronizing and blanking waveforms are mixed in the video control section where they are amplified and inverted, making composite video outputs of both polarities available for either the direct application to the video input of the display system or for the modulation of a Radio Frequency carrier that may be inserted at the antenna input of a television receiver.

Figure 2 is the schematic representation of the system. Gates 1, 2, and 3 form the buffered 378KHz. crystal oscillator. Binaries A, B, C, and D and Gates 7, 8, and 9 are the divide by 12 counter that provide the 31.5kHz. signal. Binary E is the divide by 2 counter to provide the 15.75KHz. signal. Binaries F, G, H, L, M, and N and Gates 10, 11, and 12 are the divide by 35 counter giving the 900 Hz. signal. Binaries P, T, U, V and Gates 20, 21, and 22 are the divide by 15 counter giving the 60Hz. signal. Gate triads 4, 5, and 6; 13, 14, and 15; 23, 24, and 25; and 26, 27, and 28 are pulse stretching type one-shots that are triggered on the falling edge of a positive pulse. Triad 4, 5, and 6 is the vertical line one-shot and has a period of 40 nSec. Triad 13, 14, and 15 is the horizontal synchronizing one-shot and has a 6uSec period. Triad 23, 24, and 25 is the horizontal line one-shot and has a period of two horizontal sweep lines (127uSec.). Triad 26, 27, and 28 determines the vertical synchronizing time and has a period of three horizontal sweep lines (190uSec.). The remaining one-shot is formed from Binary W and Gate 34. It has a period of 57.5 uSec. Gates 16, 17, 18, and 19, under the control of the 190 uSec. vertical time pulse, form the synchronizing waveform at the output of Gate 18 by switching from the 6 uSec. pulse to the 57 uSec. pulse for three horizontal line periods and then back to the 6



SCHEMATIC DIAGRAM -- FIGURE 2.

uSec. pulse. The video signals are controlled in NAND gates 29, 30 and 31. When switch S_1 and switch S_2 are open, a cross-hatch pattern is generated. When switch S_1 is closed, vertical line information is inhibited and a horizontal line pattern is generated. When switch S_2 is closed, horizontal line information is inhibited and a vertical line pattern is generated. When both switches are closed, both a white dot pattern is generated and lines are inhibited except where they intersect. Gate 32 inserts a blanking pulse to inhibit video output during the synchronizing periods.

The video output at Gates 31 and 32 is DC restored by CR_1 and will be positive in polarity. The synchronizing output at Gate 18 is DC restored by diode CR_2 and will be negative in polarity. These two signals are added in the 510 ohm resistor. NOR gates 35 and 36 are biased in the linear portion of their transfer characteristic and are used as video amplifiers. Two amplifiers are used so that both polarities of composite video information is available. The output of the generator will appear as shown in the photographs of Figure 3.

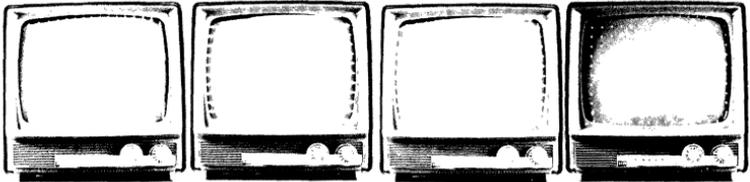


FIGURE 3

With the exception of Binary W, all binaries may be of the 124, 629, or 424 types. Binary W should be a 320 or 620. Gates 1, 2, 12, and 22 should be 116 or 616 and Gates 35 and 36 should be a SU/LU315 and 316. All other gates should be 180's or 680's.

The system was designed for operation at the power supply of 4.5V. The timing resistors and capacitors were selected to give proper pulse widths with this power supply voltage. At different power supply voltages the one-shot pull-up resistors must be selected to give proper pulse width.



June 15, 1967

APPLICATIONS MEMO

TELEVISION SYNCHRONIZING WAVEFORM GENERATOR

Typical television systems use a display system that scans vertically twice during each frame. The first scan sweeps the odd numbered lines and the second scan sweeps the even numbered lines. This is called interlaced scan and is used to reduce the flicker perceived by the human eye. To maintain the interlace, the ratio of the horizontal scan frequency to the vertical scan frequency must be accurately controlled. This function is performed by synchronizing generators as are described in Application Memo #55.

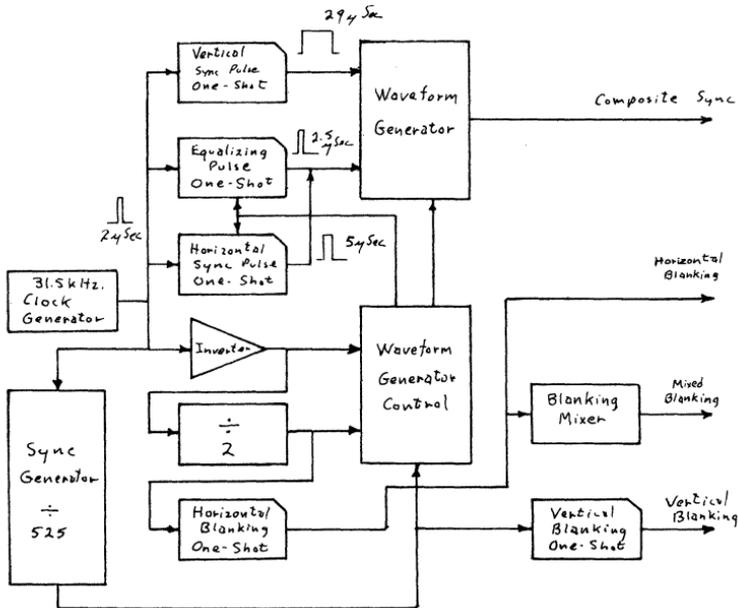
When the camera and the display devices are to be located in the same area, the required drive and blanking pulses may be easily derived at the synchronizing generator and supplied to the equipment via direct multiple cable connections. However, when the display equipment is located remotely from the camera, all information, including video, sound, blanking and synchronizing must share the same communication channel and a different method of transmitting the synchronizing and blanking information must be used. From the Synchronizing Generator, the Synchronizing Waveform Generator derives synchronizing and blanking pulse waveforms that may be added to the video and sound information for transmission over a single communication channel.

Two Synchronizing Waveform Generators will be described in this memo.

The first type is designed to provide the waveform that is required for the 525 line RETMA standard used in the Western Hemisphere, Japan, and the Philippines. Figure 1 is a block diagram of the system.

All pulses required to form the synchronizing waveform, horizontal synchronizing, vertical synchronizing and equalizing pulses, are generated in one-shots triggered from the trailing edge of the $2 \mu\text{sec}$ clock pulse, thereby ensuring good leading edge control of the output waveform. This clock pulse is the input signal for the sync. generator. Also, it is inverted to drive the divide by 2 counter and the waveform generator control. Inverting the clock pulse causes its leading edge to be negative going and since the binary used in the divide by 2 counter and those used in the waveform generator control are triggered by a negative going change, a $2 \mu\text{sec}$ lead over the sync. pulses is obtained, ensuring that no waveform switching will take place during the time any of the one-shots is on the ONE state. This lead also allows the "Front Porch" of the horizontal blanking pulse to be generated.

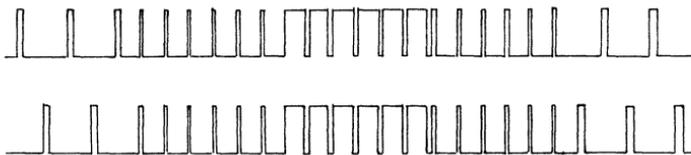
The waveform generator control forms gate pulses that cause the waveform generator to connect the output of the proper one-shot to the composite sync. output line at the correct time and in the correct sequence. When it is triggered by a 60 Hz. pulse from the sync. generator, it switches off the horizontal one-shot and activates the Equalizing pulse one-shot. It counts off 6 equalizing pulses, then 6 vertical sync.



RETMA Synchronizing Waveform Generator

Block Diagram - Figure 1.

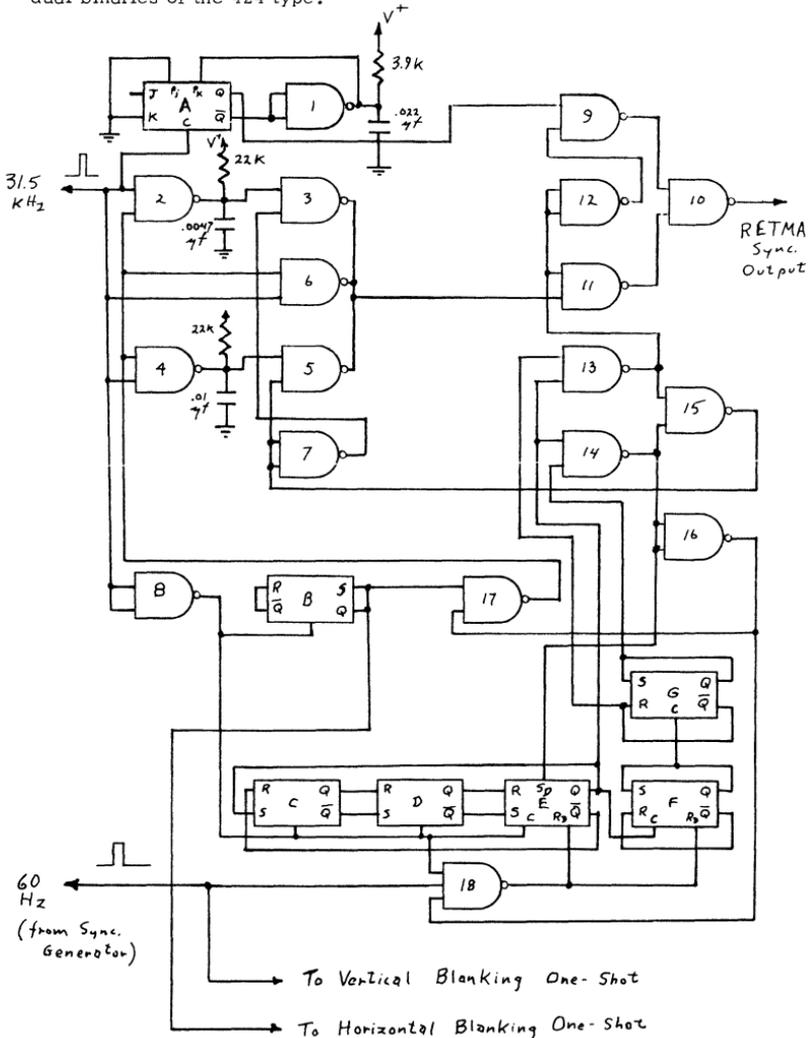
pulses and finally 6 more equalizing pulses before it resets and returns the horizontal sync. pulse one-shot to the output sync. line. At all times, except the vertical sync. period, the divide by 2 counter disables the horizontal sync. one-shot for alternate clock pulses. The output waveform is shown in Figure 2. Horizontal blanking and vertical blanking one-shots and a blanking mixer are also included.



Synchronizing Waveform

Figure 2.

Figure 3 is the schematic diagram of the system. It was designed to use DTL NAND gates of the 180/680 type. The J-K binary, A, is a 320/620 type. All remaining binaries may be the 124/629 type or all, except binary E, may be dual binaries of the 424 type.

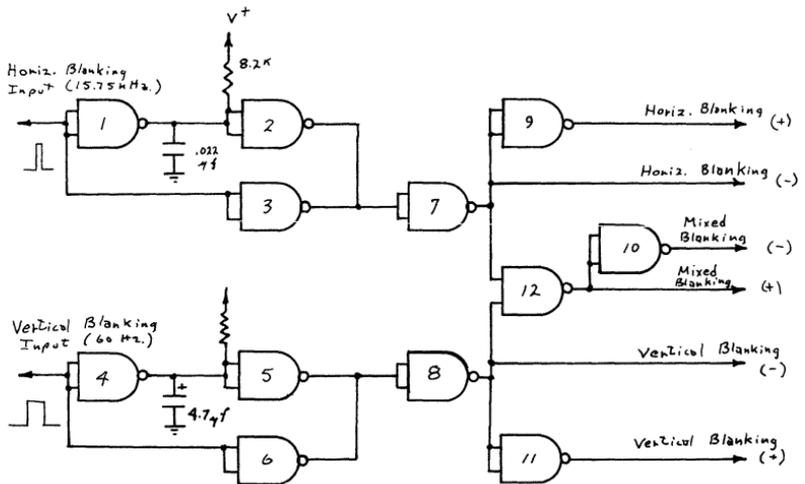


RETMA Synchronizing Waveform Generator

Schematic Diagram - Figure 3.

Binary A and Gate 1 form the vertical sync., pulse one-shot. Gates 2, 3, and 6 form the equalizing pulse one-shot. Gates 4 and 5 share Gate 6 with the equalizing pulse one-shot to form the horizontal sync. pulse one-shot. Gate 7 is an inverter and is connected so that the equalizing pulse and horizontal pulse cannot be present simultaneously. Gates 9, 10, 11, and 12 switch either the output of the Horizontal/Equalizing pulse one-shots or the vertical sync. pulse one-shot to the composite sync. output line. Binary B is the divide by 2 counter and, under the control of Gate 17, inhibits the output of the Horizontal/Equalizing pulse one-shots for every other clock pulse. Binaries C, D, E, F, and G and Gates 16 and 18 are the sync. waveform generator control. When activated by a pulse from the Synchronizing Generator, it switches in the proper one-shot and causes the RETMA vertical sync. waveform to be generated at the sync. output line.

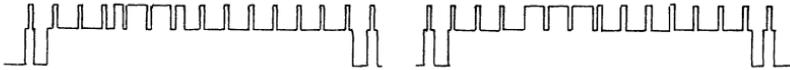
Figure 4 is a schematic for a blanking pulse generator for use with this waveform generator. Gates 1, 2, and 3 are the horizontal blanking one-shot and Gates 4, 5, and 6 are the vertical Blanking one-shot. They are constructed from NAND Gates of the 180/680 type. Gates 7 through 11 are used to drive the output lines. Gate 12 mixes the blanking pulses and also drives an output line. These gates should be capable of driving the necessary lines and should be of the 156/659 type. If it is not necessary for one of the gates to drive a line, a 180/680 type gate may be used rather than the 156/659 type.



Blanking Pulse Generator

Figure 4.

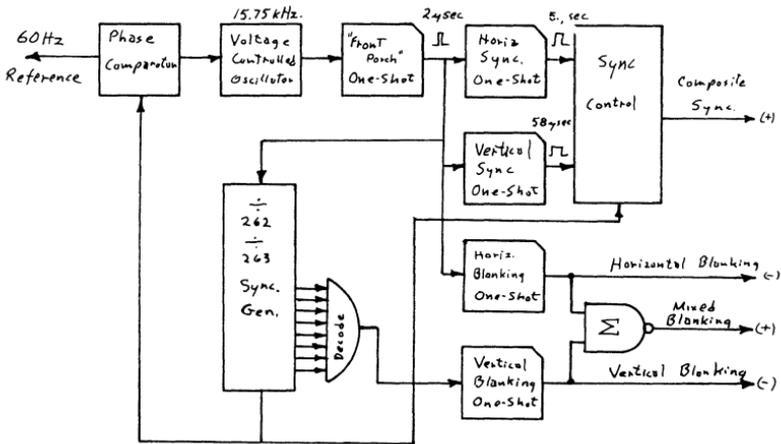
The second waveform generator is designed to be used with the synchronizing generator described in Figures 7, 8, and 9 of Application Memo #55. The highest frequency required for its operation is 15.75kHz., one half that required for the RETMA synchronizing generator, therefore, different techniques must be used to derive the synchronizing waveform. This generator will develop the waveform shown in Figure 5.



Combined Synchronizing and Blanking Waveform

Figure 5.

It is not a standard waveform, but it will be quite adequate where an inexpensive waveform generator is required.



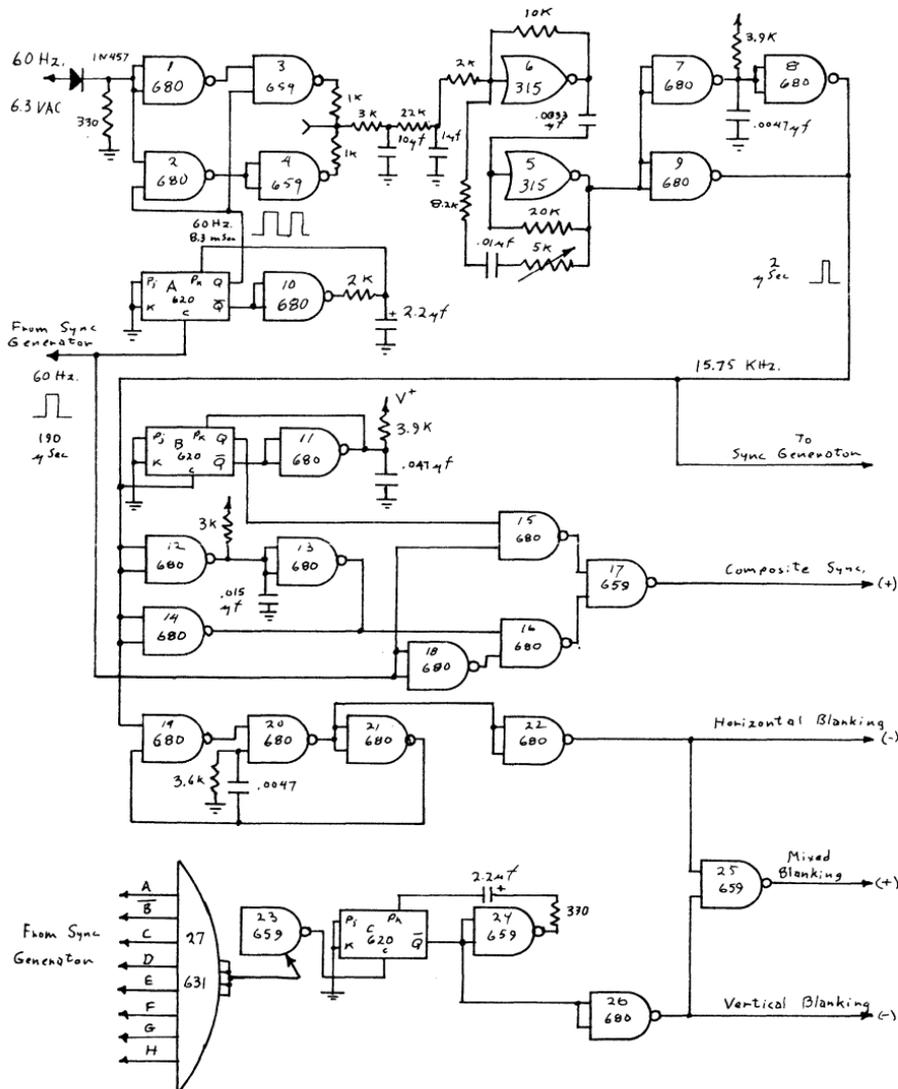
Synchronizing Waveform Generator

Figure 6

Figure 6 is the block diagram of the generator. A voltage controlled oscillator is used to drive a 2 μ Sec. one-shot which provides the clock pulse for Synchronizing Generator, horizontal sync. pulse, vertical sync. pulse, and horizontal blanking pulse one-shots. The horizontal blanking one-shot is triggered by the leading edge of the 2 μ Sec. pulse while the other one-shots are triggered on its trailing edge, thereby producing the "Front Porch" delay required between the leading edge of the horizontal blanking pulse and the horizontal sync. pulse. The Sync. Control, when a 60 Hz. pulse is received from the Sync. Generator, replaces the horizontal sync. pulse present on the composite sync. output line with the vertical synchronizing pulse. This exchange of pulses lasts for three horizontal lines or 190 μ Sec. The vertical blanking one-shot is started three horizontal sync. pulses in advance of the vertical synchronizing period by a signal derived by decoding the counter in the synchronizing generator. The vertical and horizontal blanking pulses are passed through a NAND gate to provide the mixed blanking pulse waveform. If the output pulses are not of the desired polarity, they may be inverted by passing through an additional gate. If the waveform generator outputs are to have heavy capacitive loads, it is suggested that gates having active pull-up transistors, e.g., 659, in the output stages be used to drive the load. The 60 Hz. output of the Synchronizing Generator is compared with the 60 Hz. power line frequency in the Phase Detector. The error output of the phase detector is applied to the input of the voltage controlled oscillator forming a phase locked control loop, ensuring the proper operating frequency.

Figure 7. is the Schematic Diagram of the waveform generator shown in Figure 6. Gates 1, 2, 3, and 4 are the phase detector. Binary A and Gate 10 is a one-shot used to stretch the 60Hz signal from the Synchronizing Generator to a length similar to the 60 Hz. reference signal. NOR Gates 5 and 6 are the voltage controlled oscillator. Gates 7, 8, and 9 are a 2 μ Sec. one-shot. Binary B and Gate 11 are the vertical sync. pulse one-shot and Gates 12, 13, and 14 are the horizontal sync. one-shot. Gates 15, 16, 17, and 18 are the sync. control. Gates 19, 20, and 21 are the horizontal blanking one-shot and Binary C and Gates 23 and 24 are the vertical blanking one-shot. Gates 22, 25, and 26 are inverters and the blanking mixer.

The phase detection and voltage controlled oscillator used in this system may be adapted for use with the waveform generator of Figures 1 and 2.



Synchronizing Waveform Generator

Schematic Diagram - Figure 7.

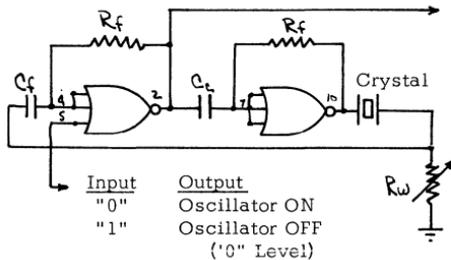


APPLICATIONS MEMO

Ralph Seymour

CRYSTAL CONTROLLED OSCILLATOR*

The circuit described below may be found useful when there is a system requirement for a stable high frequency oscillator. It uses one dual NOR gate of the SU315/316 type.



Output, 4 volts p-p

$V_{CC} = +5v$
 $R_f = 10K$
 $R_w = 1K$ (waveform
adjust)
 $C_c = .047\mu f$
 $C_f = .047\mu f$
Crystal - 100KHz to
2MHz

Each gate is made to operate in a linear condition by the application of negative feedback through R_f . The resulting amplifiers have a voltage gain of about 10, a 3db bandwidth of about 3 MHz and a 4 volt p-p output swing. C_c connects the amplifiers in cascade. Section B drives the crystal (a series resonant circuit) causing a current of crystal frequency to pass through C_f to the input of section A, forming a positive feedback loop. Any disturbance to the loop, like turning the circuit on, will cause oscillations to start at the frequency of the crystal. R_w controls the amount of positive feedback and as a result may be used to control the output waveform, giving sinusoidal or square wave output. The circuit has been operated at 5 MHz when C_c was reduced to 3pf.

* Also applies to Utilogic II NOR Gates

SECTION 8
PARALLEL DATA HANDLING



APPLICATIONS MEMO

PARALLEL ADDERS

Basic requirements for parallel adders are fast carry propagation and low device count. Two designs meeting these requirements are shown in Figures 1 and 2.

The design shown in Figure 1 may be implemented with 100 series devices. The carry propagation delay is minimized by alternating between CARRY and $\bar{\text{CARRY}}$ in the carry propagation path. This technique results in a carry propagation per stage of only one gate delay. Collector logic is used throughout the Adder to minimize device count. The inverting input of the SE125J eliminates the need for inverting the SUM outputs. This design may be implemented with 600 series devices (Figure 1), however an inverter will be required to provide SUM.

The design shown in Figure 2 may be implemented with 800 series devices. The carry propagation delay of this design is also minimized by alternating between CARRY and $\bar{\text{CARRY}}$ in the carry propagation path. The carry propagation is determined by the 840 (or 8440, 440) Exclusive-Or gate. The 840 delay is equivalent to one level of logic, therefore the carry propagation per stage is only one gate delay. The 840 is used to implement the equivalent of collector logic to minimize device count. The inverting inputs of the 825 flip-flop eliminate the need for inverting the SUM outputs. This design may be implemented with 400 series devices, however an inverter will be required to invert the SUM outputs.

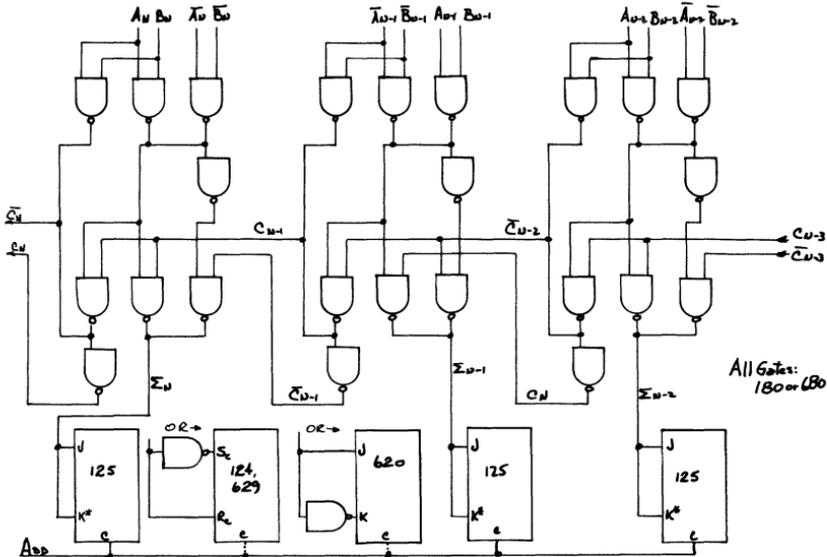


Figure 1

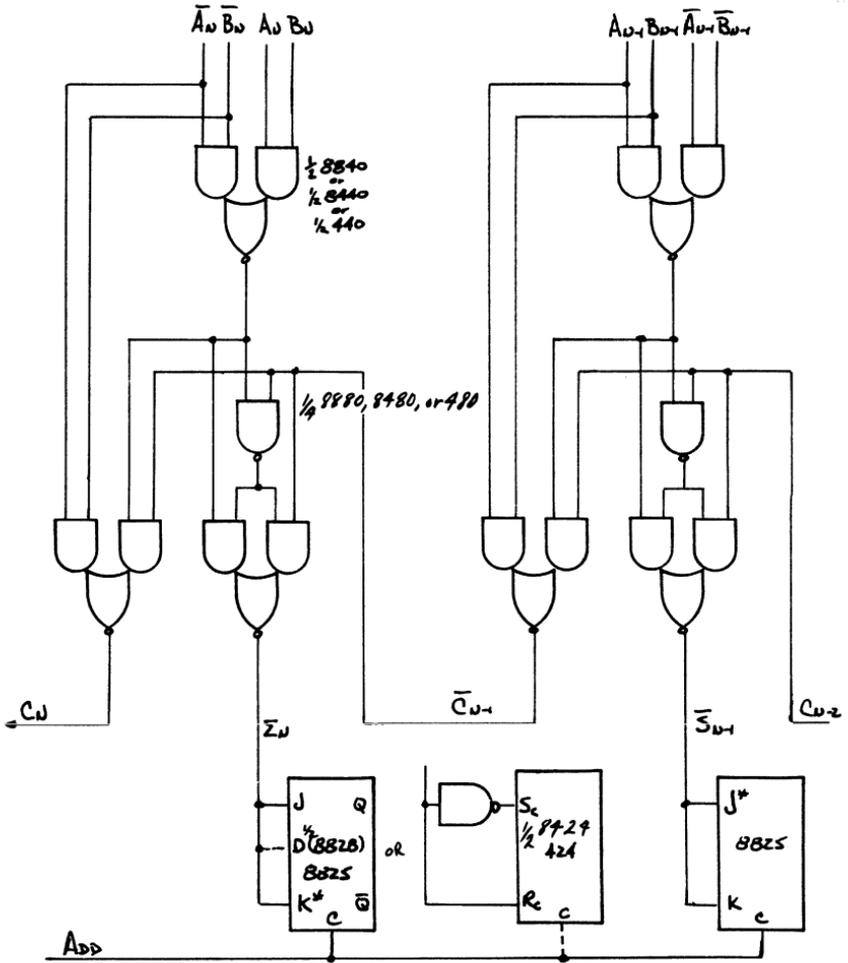


Figure 2

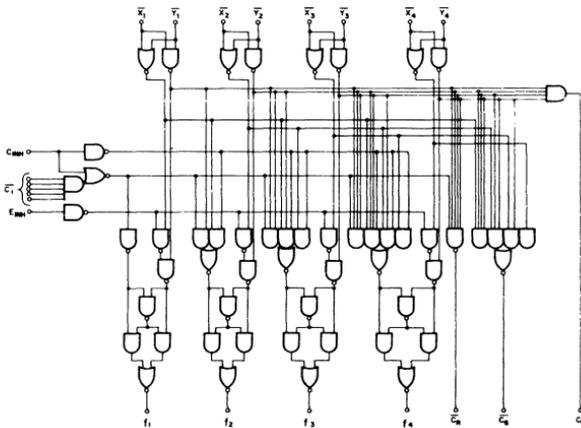


APPLICATIONS MEMO

ARITHMETIC LOGIC ELEMENT S/N 8260
 AND
 FAST CARRY EXTENDER S/N 8261

ARITHMETIC LOGIC ELEMENT S/N 8260

The S/N 8260 consists of a high speed, four bit full adder with anticipated carry.
 This is a medium scale integration (MSI) product with 24 pins.



The Arithmetic Logic Element is available in three different configurations.

- A. S8260P - 24 pin flat pack, -55°C to +125°C
- B. N8260P - 24 pin flat pack, 0°C to +75°C
- C. N8260N - 24 pin Dual-in-Line, 0°C to +75°C

The inputs are $\bar{X} = (\bar{X}_1, \bar{X}_2, \bar{X}_3, \bar{X}_4)$, $\bar{Y} = (\bar{Y}_1, \bar{Y}_2, \bar{Y}_3, \bar{Y}_4)$, which represent the two 4 bit words to be added. The CARRY INPUT \bar{C}_1 is split in five carry-terms, which

will form the carry-in. The outputs are labeled as $f = (f_1, f_2, f_3, f_4)$, whereas the functions f_i are listed in Table I.

The carry outputs are split in the following manner:

\overline{C}_G : NOT-TRUE GENERATED CARRY

The GENERATED CARRY indicates that a carry originated within the two 4 bit words (characters) to be added and is propagated to the next higher order character. It is not a function of \overline{C}_I .

$$\overline{C}_G = \overline{(X_4 Y_4) + (X_3 Y_3)(X_4 + Y_4) + (X_2 Y_2)(X_3 + Y_3)(X_4 + Y_4) + (X_1 Y_1)(X_2 + Y_2)(X_3 + Y_3)(X_4 + Y_4)}$$

C_P : PROPAGATED CARRY

The PROPAGATED CARRY indicates that a carry generated within the lower order character is propagated to the next higher order character, but does not consider the state of \overline{C}_I .

$$C_P = (X_1 + Y_1)(X_2 + Y_2)(X_3 + Y_3)(X_4 + Y_4)$$

\overline{C}_R : NOT-TRUE RIPPLE CARRY

In certain adder configurations the full carry look-ahead capabilities of the 8260 will not be utilized. For these cases the RIPPLE CARRY output combined with the GENERATED CARRY output will form the carry-in for the next following package.

$$C_R = C_P \cdot C_I$$

Besides the normal adder applications, the S/N 8260 acts as multi-purpose logic element. The control input CARRY INHIBIT (C_{INH}) provides the capability of inhibiting the bit-to-bit carries. In this case the device will operate as four independent Exclusive-OR gates. The device also has an EXCLUSIVE-OR-INHIBIT (E_{INH}) to permit a single logical combination of the input bit pairs (X_i, Y_i) and $i = 1, \dots, 4$.

We assume that we apply not true values to the inputs. Depending on the values of C_{INH} and E_{INH} , the resultant functions of the pin f_i are listed in Table I.

On the other hand, we may assume that we apply true values to the inputs. In this case, the pins f_i have the values shown in the lower half of the table.

TABLE I

INPUTS	Least Significant \bar{C}_{in} Inputs to be:	CONTROLS		f_i	FUNCTION
		C_{inh}	E_{inh}		
\bar{X}_i, \bar{Y}_i ↓	1	0	0	$\bar{\Sigma}_i$	Add
	1	0	1	--	not used
	1	1	0	$\bar{X}_i \bar{Y}_i + X_i Y_i$	Coincidence
	1	1	1	$\bar{X}_i \bar{Y}_i$	AND
X_i, Y_i ↓	0	0	0	Σ_i	Add
	0	0	1	--	not used
	0	1	0	$X_i Y_i + \bar{X}_i \bar{Y}_i$	Coincidence
	0	1	1	$X_i Y_i$	AND

ADDER SYSTEM

Ripple Adder System

If we do not extend the look-ahead technique beyond one package, the RIPPLE CARRY signal will ripple through between the different adder packages.

The Ripple Adder System is the simplest but also the slowest application with the S/N 8260. The typical total addition time (input to sum output) for a Ripple Adder System is listed below:

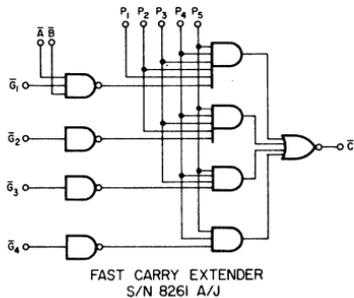
Bit	Total Addition Time
4	28ns
8	42ns
12	56ns
16	70ns
20	84ns
24	98ns
28	112ns
32	126ns
36	140ns
40	154ns

The size of a Ripple Adder System is not limited.

Fast Adder Systems – Fast Carry Extender S/N 8261

To avoid the RIPPLE CARRY addition time, we replace C_R by the logically equivalent CARRY EXTENDER term C_E . Every term C_{Ei} is generated for the i -th package simultaneously and replaces the slower RIPPLE CARRY signal. The FAST-CARRY EXTENDER, S/N 8261, will form the C_{Ei} - terms.

The S/N 8261 is available as 14 pin Dual-in-Line and as 14 pin flat pack with the normal temperature ranges of -55°C to $+125^{\circ}\text{C}$ and 0°C to $+75^{\circ}\text{C}$.

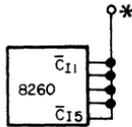


The typical addition time (Input to Sum Output) for a Fast Adder System is listed below. (See also "Adder System".)

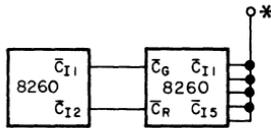
Bit	Total Addition Time
4	28ns
8	42ns
12-28	56ns

The Fast Adder System is the fastest application of the S/N 8260/61 units. The Fast Adder System provides complete carry look-ahead addition for words to 88 bits in length. For longer efficient adders, a combination of anticipated carry techniques (Fast Adder System) and ripple carry techniques are used whereas Optimum Adder Systems represent the most economical solutions among them.

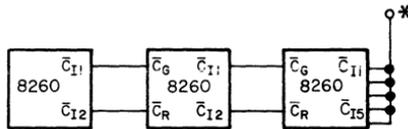
ADDER SYSTEMS



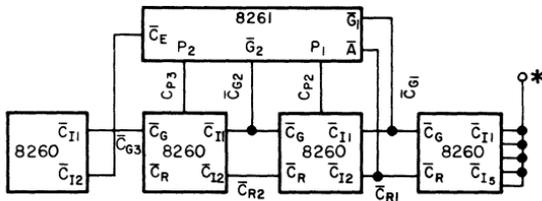
4 Bit, $T_A = 28\text{ns}$, typ. T_A : Total Addition Time



8 Bit, $T_A = 42\text{ns}$, typ. (Ripple Adder)

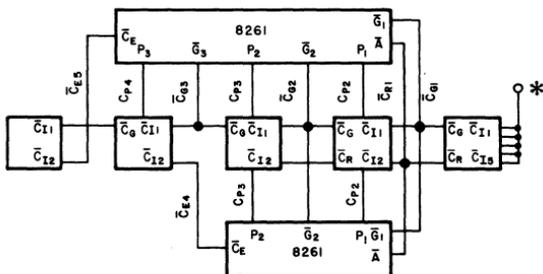


12 Bit, $T_A = 56\text{ns}$, typ. (Ripple Adder)

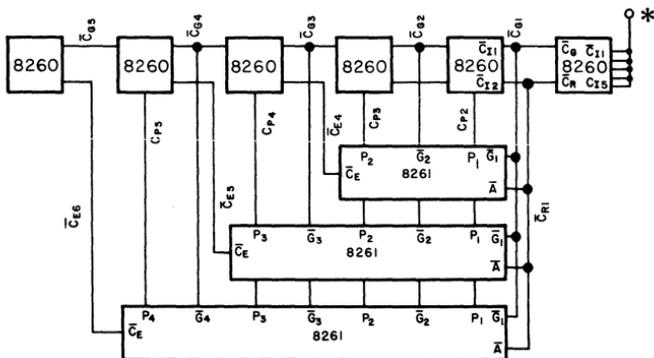


16 Bit, $T_A = 56\text{ns}$, typ. Fast Adder System
(5 packages)

* Tied to V_{CC} if not-true inputs are used, otherwise to ground. Unused 8261 pins should be tied to V_{CC} .

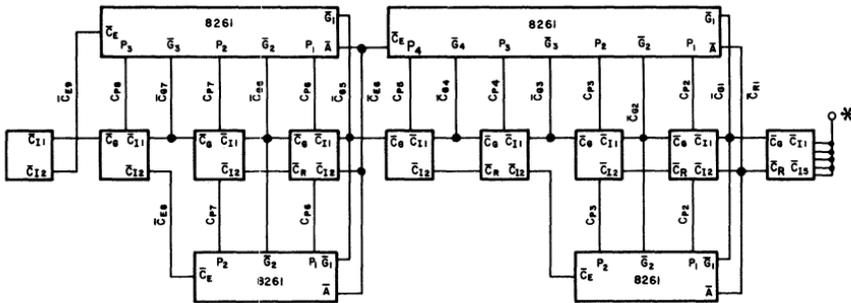


20 Bit, $T_A = 56\text{ns}$, typ. Fast Adder System
(7 packages)

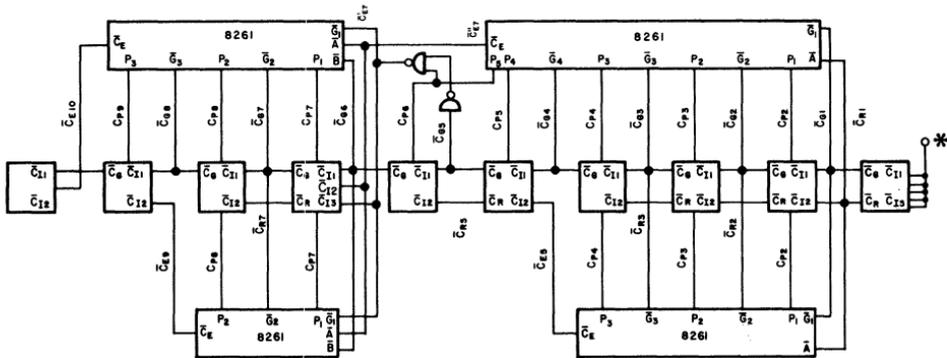


24 Bit, $T_A = 56\text{ns}$, typ. Fast Adder System
(9 packages)

* Tied to V_{cc} if not-true inputs are used, otherwise to ground.

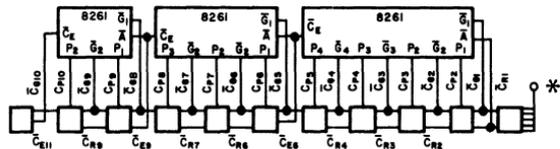


36 bit, $T_A = 70$ ns, typ. (13 packages)

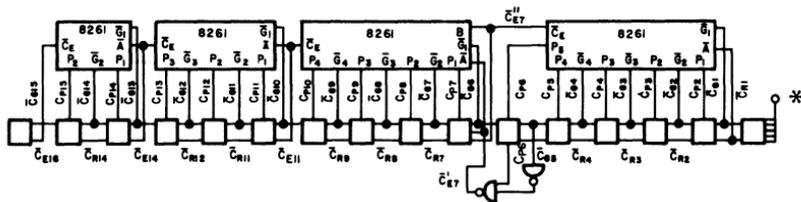


40 bit, $T_A = 70$ ns, typ. Optimum Adder with 2-Bridge Structure (14-1/2 packages)

* Tied to V_{CC} if not-true inputs are used, otherwise to ground.



44 Bit, $T_A = 84\text{ns}$, typ. Optimum Adder with 1-Bridge Structure (14 packages)



64 Bit, $T_A = 98\text{ns}$, typ. Optimum Adder with 1-Bridge Structure (20-1/2 packages)

* Tied to Vcc if not-true inputs are used, otherwise to ground.





APPLICATIONS MEMO

GATED FULL ADDER

8268

INTRODUCTION

The 8268 is a binary Full Adder with gated complementary inputs sum and $\overline{\text{sum}}$ outputs and inverted Carry Out ($\overline{\text{Carry Out}}$). The MSI circuit is designed with Diode-Transistor inputs and T^2L output, completely compatible with DTL and T^2L devices.

The Full Adder is designed especially for serial and Ripple Carry parallel ADD/SUB arithmetic units. This array has single-ended inputs and outputs, so that only the true or complement information is necessary. The logic diagram and truth table for the 8268 are shown in Figure 1.

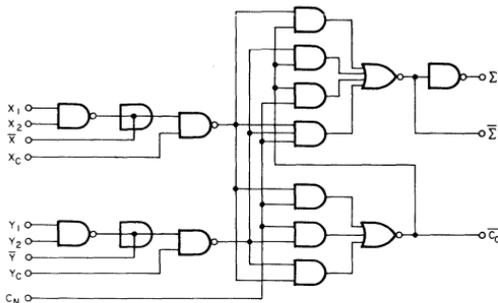


Figure 1A. 8268 Gated Full Adder

TRUTH TABLE (SEE NOTES 1,2 AND 3)					
C_N	Y	X	\overline{C}_O	$\overline{\Sigma}$	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

- NOTES: 1. $X = \overline{X} \cdot X_c$; $Y = \overline{Y} \cdot Y_c$
 where $\overline{X} = X_1 \cdot X_2$; $\overline{Y} = Y_1 \cdot Y_2$
2. When \overline{X} or \overline{Y} are used as inputs, X_1 and X_2 or Y_1 and Y_2 respectively must be tied to GND.
3. When X_1 and X_2 or Y_1 and Y_2 are used as inputs, \overline{X} or \overline{Y} respectively must be left open or used to perform the dot-AND function.

Figure 1B.

The 8268 is available in both Military (-55°C to $+125^\circ\text{C}$) and Industrial (0°C to $+75^\circ\text{C}$) temperature ranges in 14 pin dual-in-line and flat packages.

DEVICE DESCRIPTION

The factor which determines the maximum operating frequency for an N-bit parallel adder with ripple carry is the total propagation of the ripple carry term, or $NX \text{ CARRY}_{\text{DELAY}}$. To avoid the delay of an additional inversion required to provide $\text{CARRY}_{\text{OUT}} (C_0)$, the 8268 provides $\overline{\text{CARRY}}_{\text{OUT}} (C_0)$. The $\overline{C_0}$ term when used with the appropriate gated inputs (\overline{X} and \overline{Y}) at the next significant bit, the desired result is available at the $\overline{\text{SUM}} (\overline{\Sigma})$ output. This arrangement is used in every even numbered bit in an N-bit parallel adder as shown in Bit 2 and Bit 4 of Figure 2. For each even numbered bit, input control is accomplished through gated inputs X_C and Y_C . With $\text{INPUT CONTROL} (X_C \cdot Y_C) = 0$, the adder bit is disabled and all output terms are "0". This use of input control is twofold.

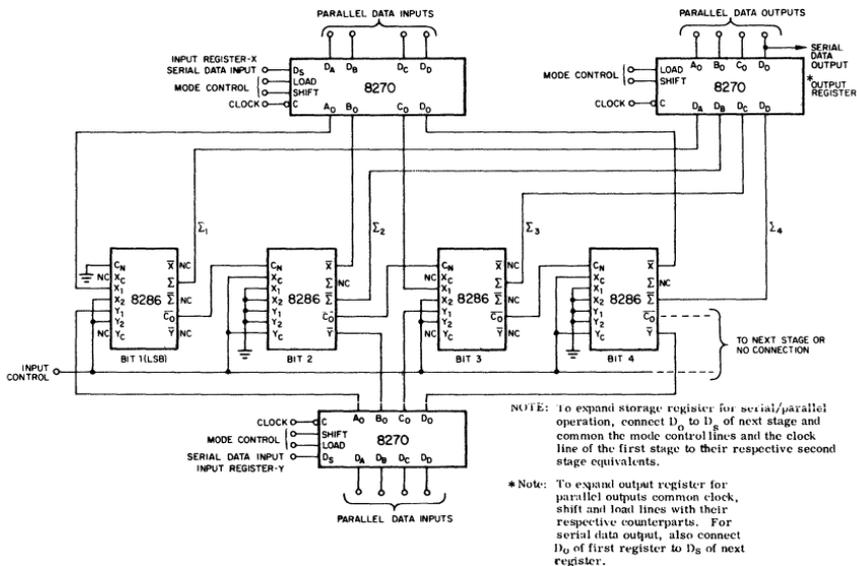


Figure 2. N-Bit Parallel Adder

First, with the adder disabled, data in the input registers may be shifted without activating the adder subsystem. Second, with all output terms at "0" the outputs can be used to clear the output storage register by parallel loading the output register with all "0"s.

Notice that the \overline{C}_0 of the second, fourth, etc. (all even numbered bits) constitutes a TRUE carry output. Therefore, to arrive at the TRUE sum at the output of all odd numbered bits \overline{C}_0 is used in conjunction with the TRUE data inputs X_1 and Y_1 . The desired output result for all odd numbered bits is available at the Σ terminal.

INPUT CONTROL is accomplished in the odd number bits of an N-bit adder by inhibiting or enabling the gated inputs $X_2 \cdot Y_2$. From the logic diagram of Figure 1, it is apparent that a "0" at X_2 and Y_2 will inhibit the transfer of the bits to be added (X_1 and Y_1). When INPUT CONTROL = "1", the information at X_1 and Y_1 will be enabled and addition will occur. Since the data inputs used are the TRUE inputs, the desired result will be available at the SUM output (Σ_1). This operating mode is shown in Bit 1 and Bit 3 of Figure 2.

Note that the CARRY IN (C_n) term of the least significant bit of the binary adder in Figure 2 is tied to GND, since C_n is a TRUE term (activates on "1") and there is no carry term into the least significant bit.

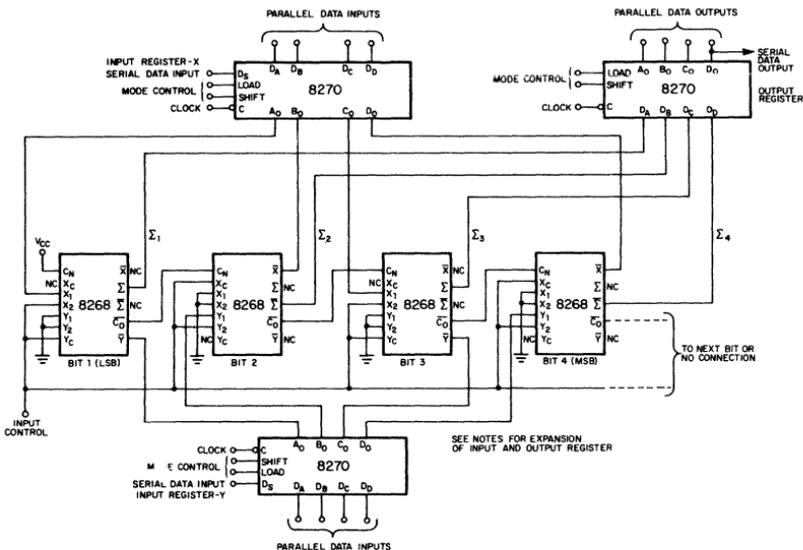


Figure 3 N-Bit Parallel Subtractor

To construct an N-bit binary subtractor (Figure 3), the logic input of the subtrahend (register Y) is inverted on a bit basis from the input arrangement for the binary adder.

In addition, the input used for the Y register input control is effectively inverted (compared to the adder). Thus:

for all odd numbered bits (1, 3, etc.)

$$\text{INPUT CONTROL} = X_2 \cdot Y_C$$

for all even numbered bits (2, 4, etc.)

$$\text{INPUT CONTROL} = X_C \cdot Y_2$$

The input control connection pattern results from the inversion of the Y-register logic inputs.

Note that to provide the SUBTRACT function, the C_n input of the least significant bit must be connected to a logical 1 level.

EXAMPLES OF APPLICATION

Serial Binary ADD-SUBTRACT

Figure 4 illustrates a 4-bit serial ADD/SUB arithmetic unit. The unit will add $X + Y$ or subtract $X - Y$ upon command. The interconnect scheme is uncomplicated.

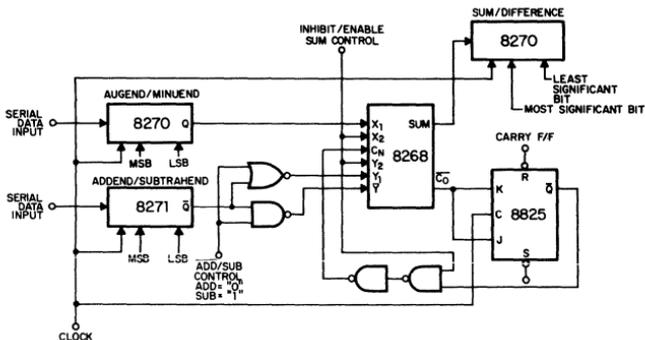


Figure 4. 4-Bit Serial Add/Subtractor

Operation:

Assume the two binary numbers to be added/subtracted are present in the Augend/Minuend and Addend/Subtrahend Registers. For addition, set control line to logic "0". Also, initially set Carry F/F ($\bar{Q} = 0$). This allows the data in the Addend/Subtrahend register to be entered into the sum/difference register and the Carry Flip-Flop has been conditioned for the addition of the next two binary bits. The sum is formed Least Significant Bit first. This process continues until 4 clock pulses

have occurred. At the end of the 4th clock pulse, the result is in the sum/difference register (i.e. LSB appears at D_0 ; MSB appears at A_0). For subtraction, the ADD/SUB control is set to a logic "1". Also, the Carry Flip-Flop should be reset (i.e., $\bar{Q} = 1$). Now the subsystem is ready to perform subtraction viz one's complement addition. Once again, after 4 clock pulses have occurred, the result is in the sum/difference register.

As an option, the inhibit/enable sum control may be used to force the sum output to logic "0" in between shift pulses or as a "jam" function. The X_2 and Y_2 inputs force the sum to "0" when $X_2 = Y_2 = "0"$.

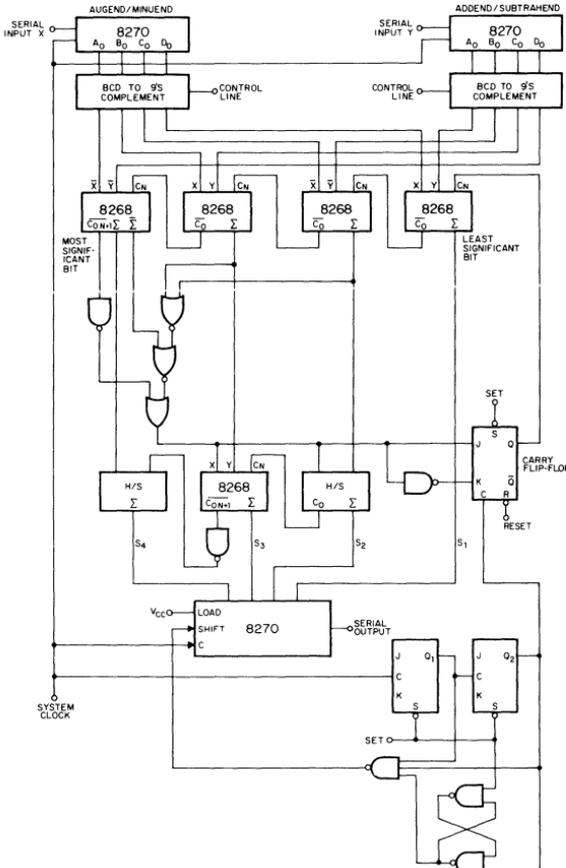


Figure 5. Serial BCD ADD/SUB Unit

Serial BCD ADD/SUBTRACT

Figure 5 shows a BCD ADD/SUBTRACT serial subsystem. This subsystem uses nine's complement addition to perform subtraction. One should be aware that the nine's complement of the smaller (absolute value) number must be formed in order to get the correct result.

Operation:

The Augend and Addend are shifted into the 8270 (4 bit shift registers). The divide by four counter is initially set to $Q_1 = 1$ and $Q_2 = 1$. The subsystem is now ready to perform Addition or Subtraction. If it is desired to perform addition, then the control lines on the nine's complement converters are at logic "1" and Carry Flip-Flop is initially reset (i.e., $Q = "0"$).

To perform subtraction, the control line associated with the smaller of the two numbers (absolute value) is at logic "0", the other control line at at logic "1" and the Carry Flip-Flop is initially set (i.e., $Q = "1"$).

The Carry Flip-Flop is clocked at one-fourth the system rate due to the fact that a BCD code is 4 binary bits long.

The sum outputs of the Adder are allowed to enter the sum/difference register in parallel on every 4th clock. Thus, no information is entered into the sum/difference register while shifting takes place.

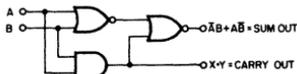


Figure 6. Half Adder (H/A)

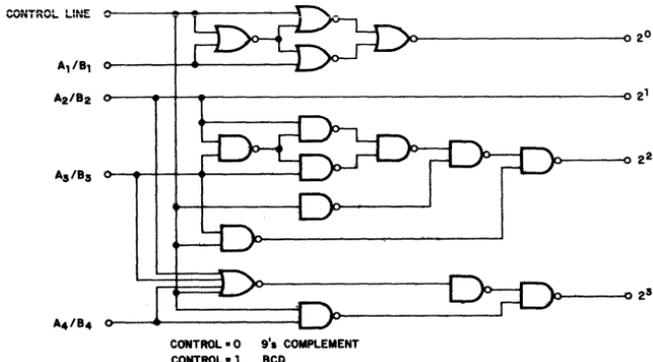


Figure 7. Conditional BCD to 9's Complement

