signetics FULLY ENCODED, 9046 X N, RANDOM ACCESS WRITE-ONLY-MEMORY

25120

FINAL SPECIFICATION[10]

DESCRIPTION

The Signetics 25000 Series 9C46XN Random Access Write-Only-Memory employs both enhancement and depletion mode P-Channel, N-Channel and Neu[1] channel MOS devices. Although a static device, a single TTL level clock phase is required to drive the on-board multi-port clock generator. Data refresh is accomplished during CB and LH periods [11]. Quadri-state outputs (when applicable) allow expansion in many directions, depending on organization.

The static memory cells are operated dynamically to yield extremely low power dissipation. All inputs and outputs are directly TL compatible when proper interfacing circuitry is employed.

Device construction is more or less S.O.S.[2]

FEATURES

- **FULLY ENCODED MULTI-PORT ADDRESSING**
- **WRITE CYCLE TIME 80nS (MAX. TYPICAL)**
- **WRITE ACCESS TIME[3]**
- **POWER DISSIPATION 10µW/BIT TYPICAL**
- **CELL REFRESH TIME 1mS (MIN. TYPICAL)**
- **TTL/DTL COMPATIBLE INPUTS[4]**
- **AVAILABLE OUTPUTS "n"**
- **CLOCK LINE CAPACITANCE 2pF MAX.[5]**
- **V^{CC} = +10V**
- **V^{DD} = 0V ±2%**
- **V^{FF} = 6.3V[ac(6)]**

APPLICATIONS

DON'T CARE BUFFER STORES
LEAST SIGNIFICANT CONTROL MEMORIES
POST MORTEM MEMORIES (WEAPON SYSTEMS)
ARTIFICIAL MEMORY SYSTEMS
NON-INTELLIGENT MICRO CONTROLLERS
FIRST-IN NEVER-OUT (FINO) ASYNCHRONOUS BUFFERS.
OVERFLOW REGISTER (BIT BUCKET)

PROCESS TECHNOLOGY

The use of Signetics unique SEX[7] process yields Vth (var.) and allows the design[8] and production[9] of higher performance MOS circuits than can be obtained by competitor's techniques.

BIPOLAR COMPATIBILITY

All data are clock input pins applicable output will interface directly or nearly directly with bipolar circuits of suitable characteristics in any event use 1 amp fuses in all power supply and data lines.

INPUT PROTECTION

All terminals are provided with slip-on latex protectors for the prevention of Voltage Destruction. (PILL packaged devices do not require protection.)

SILICON PACKAGING

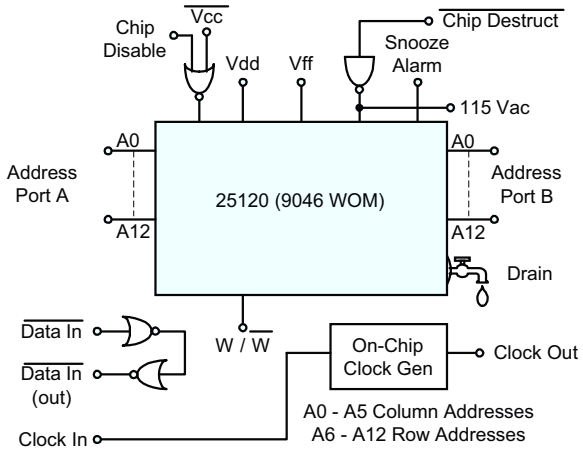
Low cost silicon DIP packaging is implemented and reliability is assured by the use of a non-hermetic sealing technique which prevents the entrapment of harmful ions,, but which allows the free exchange of friendly ions.

SPECIAL FEATURES

Because of the employment of the Signetics' proprietary Sanderson-Rabbet Channel the 25120 will provide 50% higher speed than you will obtain.

COOLING

The 25120 is easily cooled by the employment of a six foot fan ⅓" from the package. If the device fails you have exceeded the ragings. In such cases, more air is recommended.



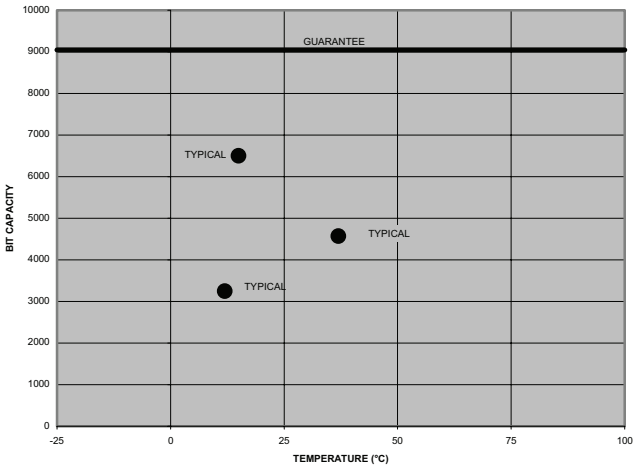
PART IDENTIFICATION

TYPE	"n"	TEMP. RANGE	PACKAGE
25120	0	0 to –70°C	Whatever's Right

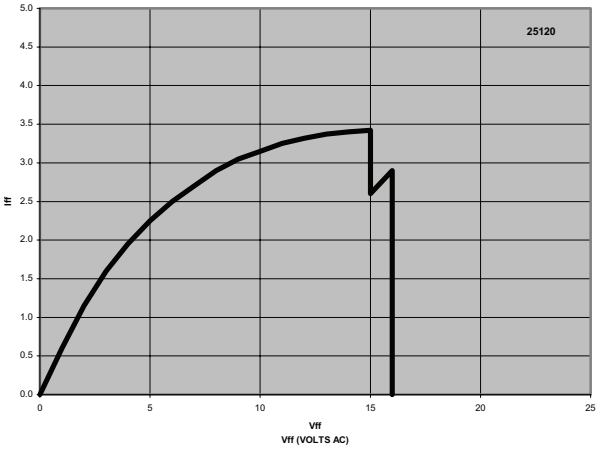
1. "Neu" channel 16V CMOS enhances or depletes regardless of gate polarity, either simultaneously or randomly. Sometimes not at all.
2. "S.O.S" copyrighted U.S. Army Commissary, 1940.
3. Not applicable.
4. You can somehow drive these inputs from TTL, the method is obvious.
5. Measure at 1MHz, 25mvac, 1.8pf in series.
6. For filaments, what else!
7. You have a dirty mind. S.E.X. is a Signetics Extra Secret process. "One Shovel Full to One Shovel Full", patented by Yagura, Kashkooli, Converse and AL, Circa 1921.
8. J. Kana calls it design (we humor him).
9. See "Modern Production Techniques" by T. Arrieta (not yet written).
10. Final until we got a look at some actual parts.
11. Coffee breaks and lunch hours.
12. Due credit to EIMAC for inspiration.

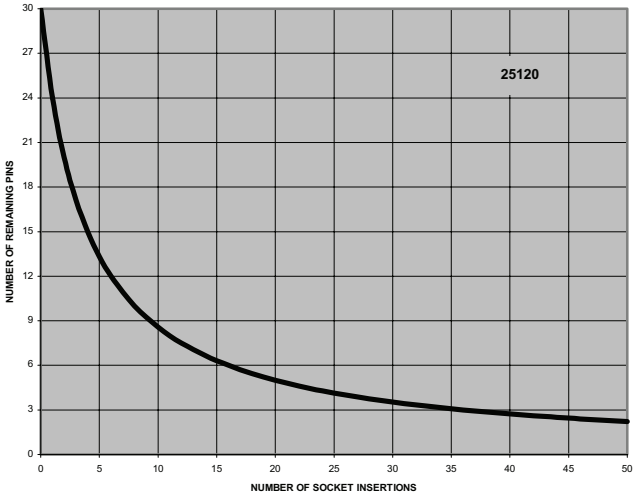
TYPICAL CHARACTERISTIC CURVES

BIT CAPACITY VS. TEMP.

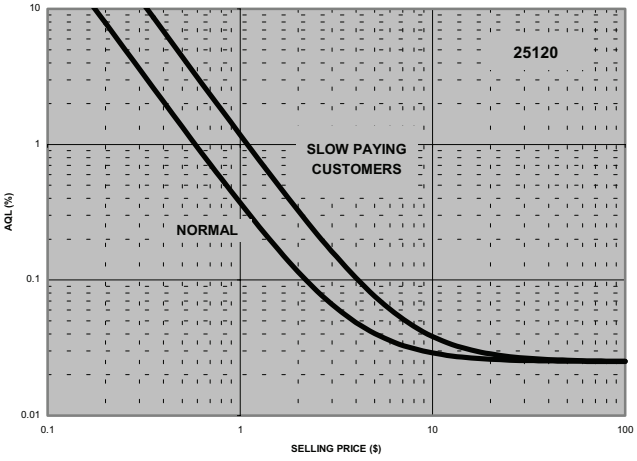


Iff VS. Vff





AQL VS. SELLING PRICE



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