Solid State Micro Technology for Music

SSM 2100

SSM 2100 MONOLITHIC LOG/ANTILOG AMPLIFIER

DESCRIPTION

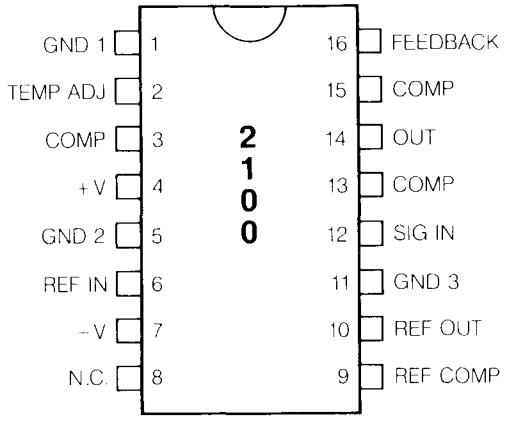
The SSM 2100 is a complete monolithic subsystem for the realization of logarithmic and exponential transfer characteristics. Included are two precision op-amps, a high conformance transistor pair and a precision bandgap voltage reference. Additionally, the chip has a substrate temperature regulator which stabilizes the scale factor and greatly attenuates drift of the reference. A negative reference voltage is also available to facilitate external trimming.

FEATURES

- 500pA Input Bias Current (untrimmed)
- 50pA Input Bias Current (trimmed)
- 4mV Input Offset Voltage
- 10ppm/°C Reference Drift
- 30ppm/°C Scale Factor Drift
- 0.25% Conformance
- 3 Decade Dynamic Range (Voltage Input)
- 5 Decade Dynamic Range (Current Input)

APPLICATIONS

- Photodiode Preamplifier
- Absorption Measurement
- Log Sweep Generators
- High Resolution Data Acquisition
- Analog Computation Circuits
- Analog Compression/Expansion
- Linear to dB Conversion



PIN OUT (TOP VIEW)

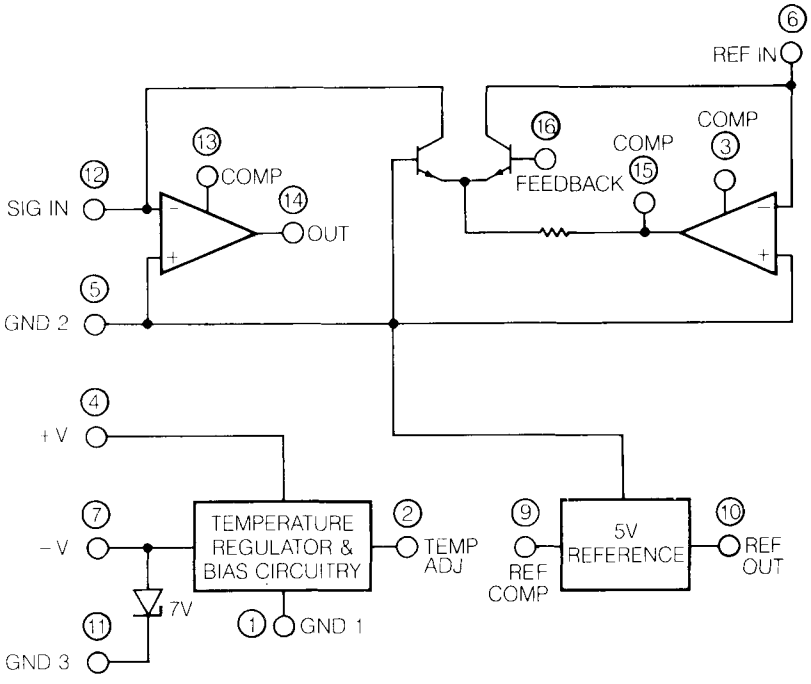


FIGURE 1. BLOCK DIAGRAM

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SPECIFICATIONS*

OPERATING TEMPERATURE
−10°C to +55°C

STORAGE TEMPERATURE
−55°C to +125°C

The following specifications apply for $V_s = \pm 15V$, $R_{LIMIT} = 1.6k\Omega$, $5°C \leq T_A \leq 50°C$, $I_{REF} = 1mA$, unless otherwise noted.

PARAMETER (SYMBOL)	MIN	TYP	MAX	UNITS	CONDITIONS
Conformity Error (V_{error}) (Note 1)		0.25 0.4		% %	I_{IN} = 100nA to 100μA I_{IN} = 10nA to 1mA (Input Offset Trimmed)
Scale Factor (V_{scale})	65	70	75	mV/Decade	Measured at Pin 16
Scale Factor Temperature Drift (TC V_{scale})		30		ppm/°C	
Input Offset Voltage (V_{ios}) (Note 2)		4	8	mV	
Input Bias Current (I_b) (Notes 1, 2)		500	2000	pA	
Output Offset Voltage (V_{oos})		30	70	mV	$I_{IN} = I_{REF}$ = 1mA Scale Factor Set at 1V/Decade
Power Supply Rejection Ratio (PSRR) (Note 3)		500 250		μV/V μV/V	$+12V \leq V+ \leq +17V$ $-12V \geq V- \geq -17V$ Scale Factor Set at 1V/Decade
Output Voltage Swing (V_{OUT})	−1 −0.2		+10 +10	V V	$R_L \geq 10K$ $R_L \geq 2K$
Reference Output Voltage ($V_{REF}+$)	4.7	5.0	5.2	V	No Load
Reference Output Voltage Temperature Coefficient (TC V_{REF})		10		ppm/°C	
Reference Output Current	5			mA	
Reference Load Regulation		0.015		%/mA	$R_L \geq 1K\Omega$
Reference Supply Rejection		0.04		%/V	$+12V \leq V+ \leq +17V$
Voltage at Pin 7 ($V_{REF}-$)	6	7	8	V	
Positive Supply Current (I_S+)		35 20 50 5		mA mA mA mA	T_A = 25°C T_A = 50°C T_A = 5°C Heater Disabled
Negative Supply Current (I_s-)		5		mA	
Heater Start up Current		80	120	mA	
Regulated Chip Temperature (T_{REG})	53	60	75	°C	

Notes
1). Guaranteed by design but not directly measured.
2). Applies to both signal and reference inputs.
3). Referred to output in log mode, or to input in antilog mode.
4). Specifications apply after a 50 second warmup period.

*Final specifications may be subject to change.

Principle of Operation

The 2100 uses the predictable logarithmic relationship between the collector currents and differential input voltage of an NPN transistor pair, given by:

$$\Delta V_{IN} = \frac{kT}{q} \ln \frac{I_{C1}}{I_{C2}}$$

where k = Boltzmann's constant (1.38×10^{-23} J/K)
q = charge on the electron (1.6×10^{-19} C)
T = absolute temperature (K)

The absolute temperature term is eliminated on the 2100 by regulating the chip temperature at 60°C (333K), producing a constant scale factor set by two external resistors.

Referring to figure 1, two high gain op amps force the collector currents of the transistor pair to equal the input and reference currents. These currents can be easily generated by external resistors since both op amp inputs rest at virtual ground.

In the logarithmic mode, the overall circuit provides the transfer function:

$$V_{OUT} \propto \frac{kT}{q} \ln \left(\frac{V_{REF}}{V_{IN}} \times \frac{R_{IN}}{R_{REF}}\right) \text{ or } V_{OUT} = K \log_{10} \left(\frac{V_{REF}}{V_{IN}} \times \frac{R_{IN}}{R_{REF}}\right)$$

where $K = \dfrac{0.07\,(R_1 + R_2)}{R_2}$ volts/decade in the case of the 2100.

For most applications, K will be set equal to 1V/decade.

An on chip 5V reference has been included for applications needing a true log, rather than a log ratio function. Both I_{IN} and I_{REF} should be kept at 1mA or less for best results.

2100 Inputs

The 2100, like all log amplifiers, has limited dynamic range for voltage inputs due partially to input offset voltage (which is trimmable) and to various second order effects (which are not). Therefore, for widest dynamic range current inputs are recommended. Since most wide range transducer inputs (such as photodiodes) closely resemble current inputs, this is not usually a problem. Untrimmed, the 2100 can handle about 5 decades of dynamic range in log mode, or about 10 decades in log ratio mode. When trimmed, this can be extended to at least 6 decades (12 decades in log ratio mode).

The following application circuits are, for convenience, shown for voltage inputs, though all configurations can be used for current inputs in which case R_{IN} can be omitted. To ensure unconditional stability, however, it is recommended that the input be shunted to ground with a 10kΩ resistor in series with a 10nF capacitor when using a true current input.

2100 Negative Supply

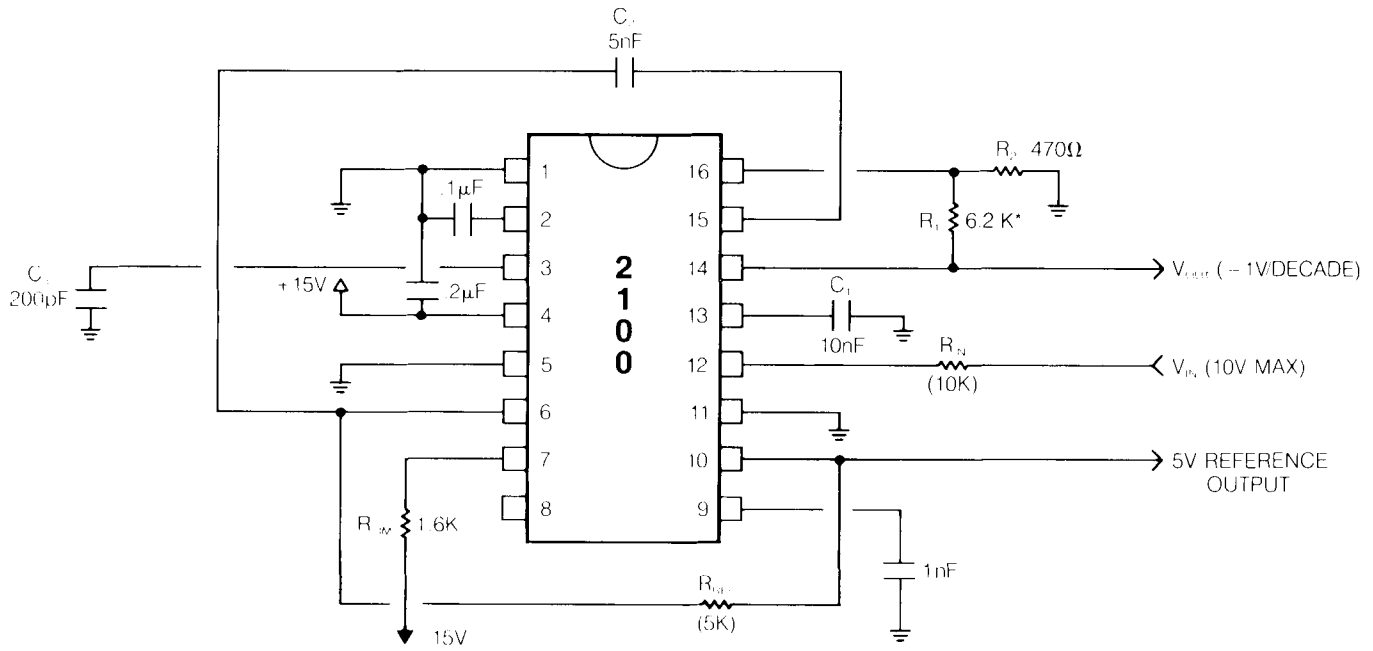
The 2100 negative supply is internally regulated at −7V, and a current limiting resistor (R_{LIMIT}) is required in series with pin 7. For most applications, a value of 1.6kΩ for −15V supplies is recommended. The voltage at pin 7 is thus quite stable and is useful when trimming the unit externally.

Power Supply Decoupling and Grounding

Because of the high gain of the temperature regulator circuit, generous positive supply decoupling should be used. The 0.2μF decoupling capacitor shown on the application circuits should be of ceramic type and mounted as close to pins 1 and 4 as possible. An additional capacitor of about 50μF or more should also be included on the board. It should also be noted that pin 1 carries all the heater current, and care should be taken when laying out ground lines to prevent this from causing errors. The negative supply is internally regulated and needs no decoupling.

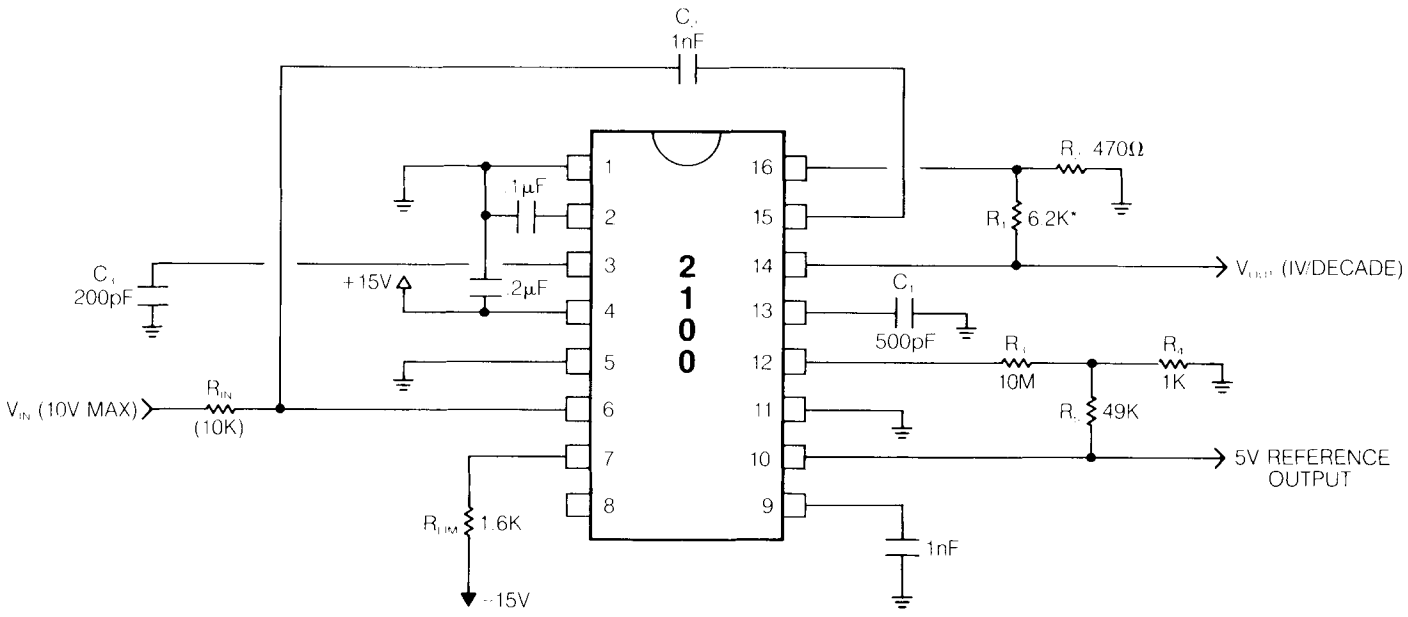
Temperature Control

The internal chip temperature is regulated at about 60°C but this can be adjusted by means of pin 2. To decrease the temperature by N° C, a resistor of value $\frac{3.5}{N}$ MΩ should be connected between pins 2 and 10. To increase the temperature by N° C, a resistor of value $\frac{6}{N}$ MΩ should be connected between pins 2 and 7. The regulator can be shut off entirely with a 100kΩ resistor from pin 2 to +V. This is useful in low power applications. With no regulation, the reference drift is about 70 ppm/°C, and the scale factor drift about −3300 ppm/°C. The latter can be compensated using a temperature compensating resistor (e.g. Tel Labs Q 81) instead of R_2.



*ADJUST FOR DIFFERENT SCALE FACTOR

FIGURE 2. INVERTING LOGARITHMIC AMPLIFIER



*ADJUST FOR DIFFERENT SCALE FACTOR

FIGURE 3. NON INVERTING LOGARITHMIC AMPLIFIER

Inverting Log Amplifier

Figure 2 shows the 2100 used in the inverting log mode. With $I_{IN} = I_{REF}$ ($V_{IN} = 10V$ with values shown) the output will be zero, and will increase at 1V/decade as I_{IN} reduces. The 10V input range optimizes dynamic range in +15V systems, but can be changed proportionally by adjusting R_{IN}. Adjusting R_1 will alter the scale factor, while adjustment of R_{REF} will alter the output offset at a given V_{IN}.

C_1 C_2 & C_3 provide phase compensation for the system, yielding a 30kHz small signal bandwidth at I_{IN} = 1mA, 8kHz at I_{IN} = 1μA and 1.6kHz at I_{IN} = 100nA. This can be improved by a factor of 3 by increasing C_2 to 10nF and reducing C_1 to 2nF, at the expense of some peaking at the upper range of input current.

Non Inverting Log Amplifier

Interchanging the signal and reference inputs yields a non inverting log amplifier (figure 3). In this case the output crosses zero with the input five decades below full scale, but this can be altered by adjusting R_3. A slight inaccuracy is caused by R_1 and R_2 adding to the base resistance of the logging transistors, but this is minimized by keeping these as small as possible.

The small signal bandwidth is 5kHz with I_{IN} from 1μA to 1mA and is better than 2kHz over the full five decade range.

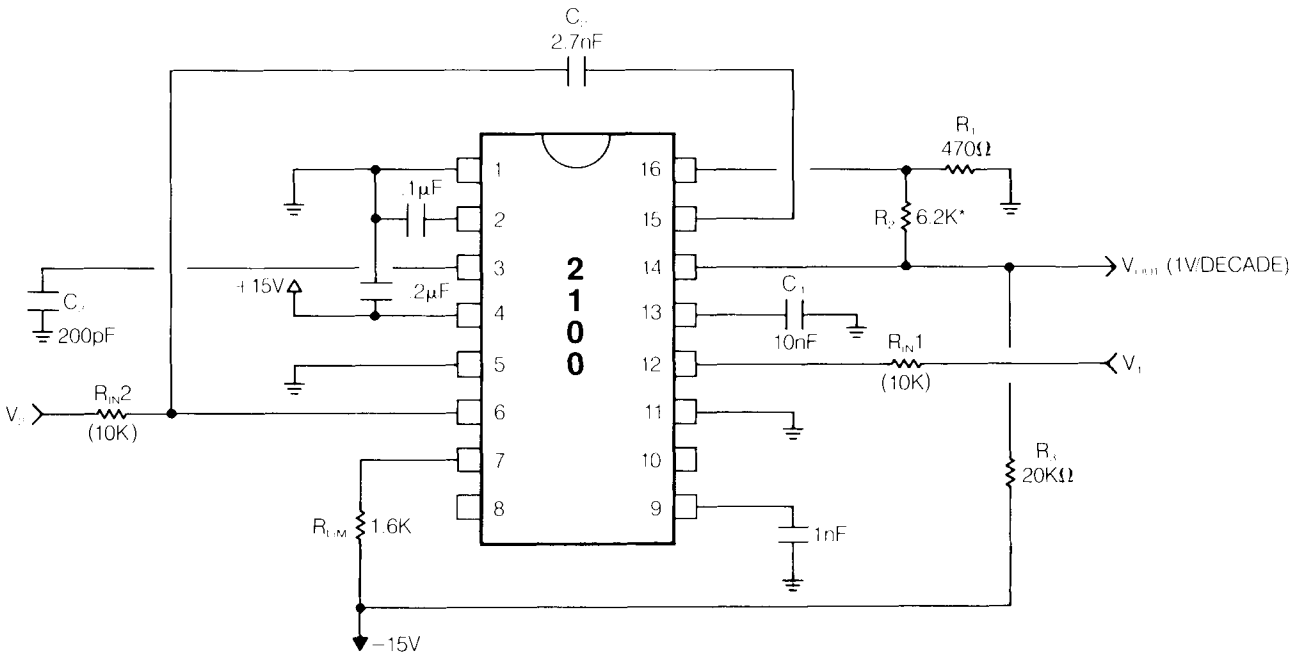
Log Ratio Applications

The 2100 is well suited to log ratio applications where the output is proportional to the logarithm of the ratio of two input currents or voltages. This is because both the signal and reference inputs operate at true virtual ground eliminating the need for a true current found in many other configurations.

However, the output amplifier of the 2100 can only swing about 1.5V below ground and can only sink about 300μA of current. This causes problems if the reference current is more than 1 decade below the signal current.

If the latter criterion is not exceeded, the circuit of figure 4 is recommended. R_3 provides the extra sink current to provide a −1V output with an additional 10k load.

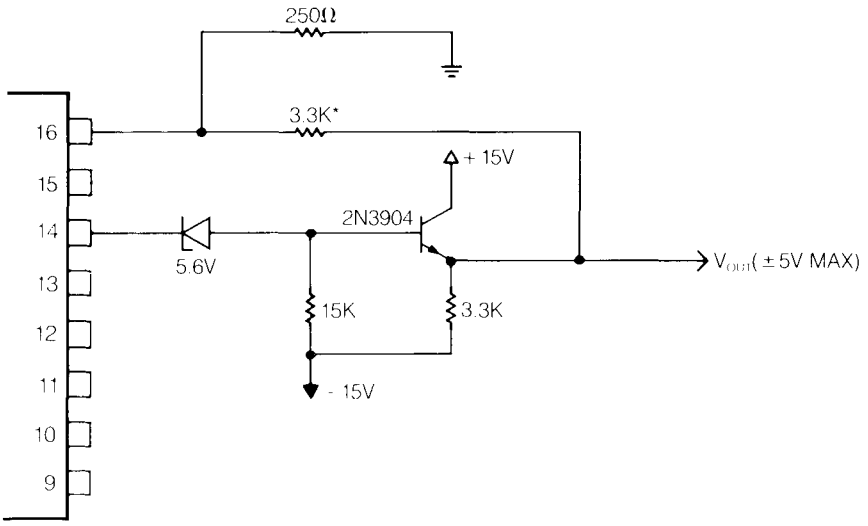
If full four quadrant capability is necessary, the output buffer shown in figure 5 can be added. This will provide a ±5V output for reference/signal ratios from 10^5 to 10^{-5} (a 10 decade dynamic range).



*ADJUST FOR DIFFERENT SCALE FACTOR.

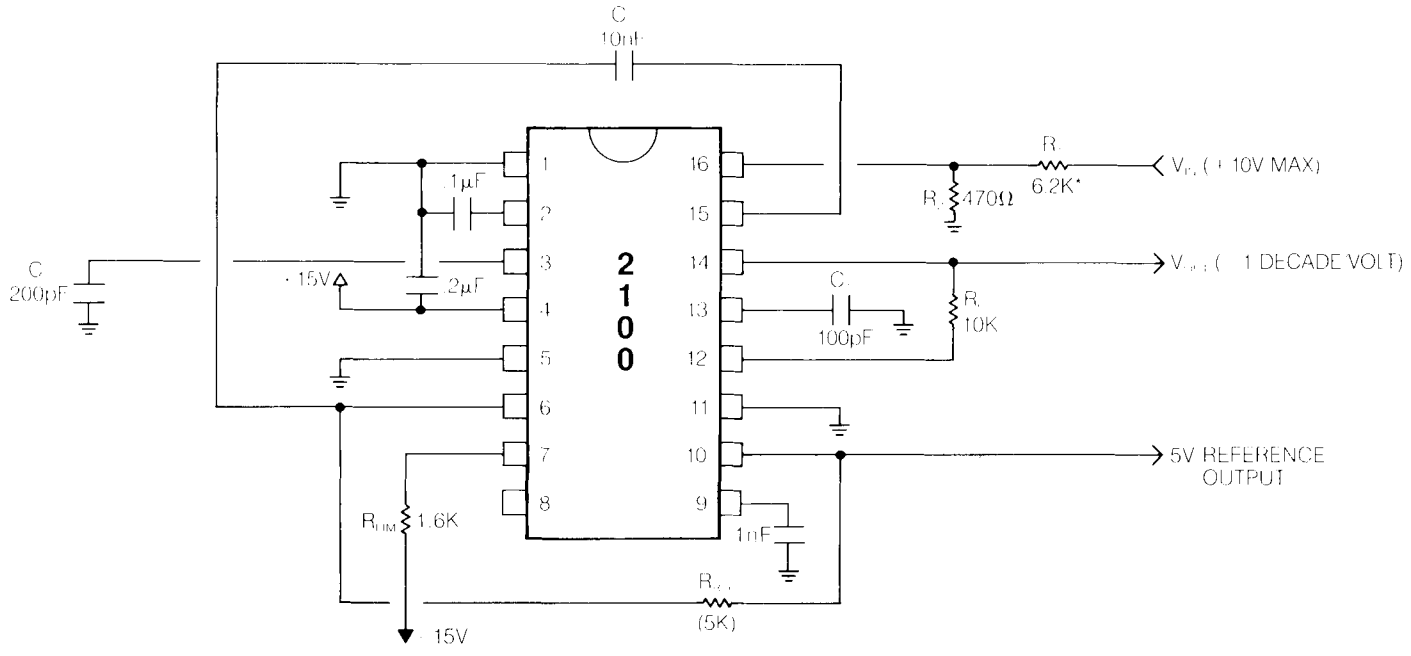
$V_{OUT} = K \log V_2/V_1$ (K = 1V/DECADE WITH VALUES SHOWN).

FIGURE 4. LOG RATIO AMPLIFIER



*ADJUST FOR DIFFERENT SCALE FACTOR

FIGURE 5. MODIFICATION OF FIGURE 4 FOR FOUR QUADRANT OPERATION



*ADJUST FOR DIFFERENT SCALE FACTOR

FIGURE 6. ANTILOGARITHMIC AMPLIFIER

R_{IN}	R_X	R_Y
1K	470K	∞
10K	4.7MΩ	∞
100K	10MΩ	6.8K
∞*	20MΩ	680Ω

*(Current Input)

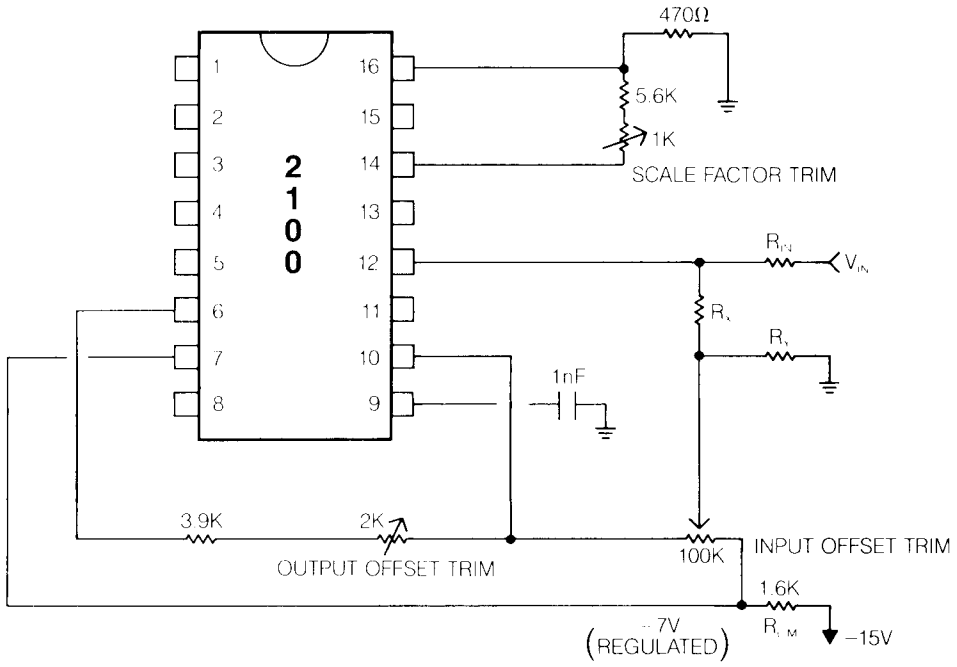


FIGURE 7. TRIMMING THE 2100

Antilog (Exponential) Amplifier

Figure 6 shows the connections required to generate the exponential function. The input range as shown is zero to 10V but this can be changed by adjusting R_1. The output scale factor is −1 decade/volt but can be changed by adjusting R_{OUT}. The bandwidth of the circuit is about 500kHz.

Trimming the 2100

Figure 7 shows general trimming techniques for input offset, output offset and scale factor. The input offset adjustment can be duplicated for the reference input in the case of log ratio applications.

The input offset trim removes errors due to both amplifier offset and input bias current, and the use of the positive and negative reference voltages gives a high rejection to supply voltages changes.

Unlike an op amp, a log amp cannot be trimmed with $V_{IN} = 0$ since the log of zero theoretically gives an infinite output voltage. A suggested technique is to trim output offset and scale factor first, and then apply a small signal to the input and adjust the input offset trim for correct reading at the output.