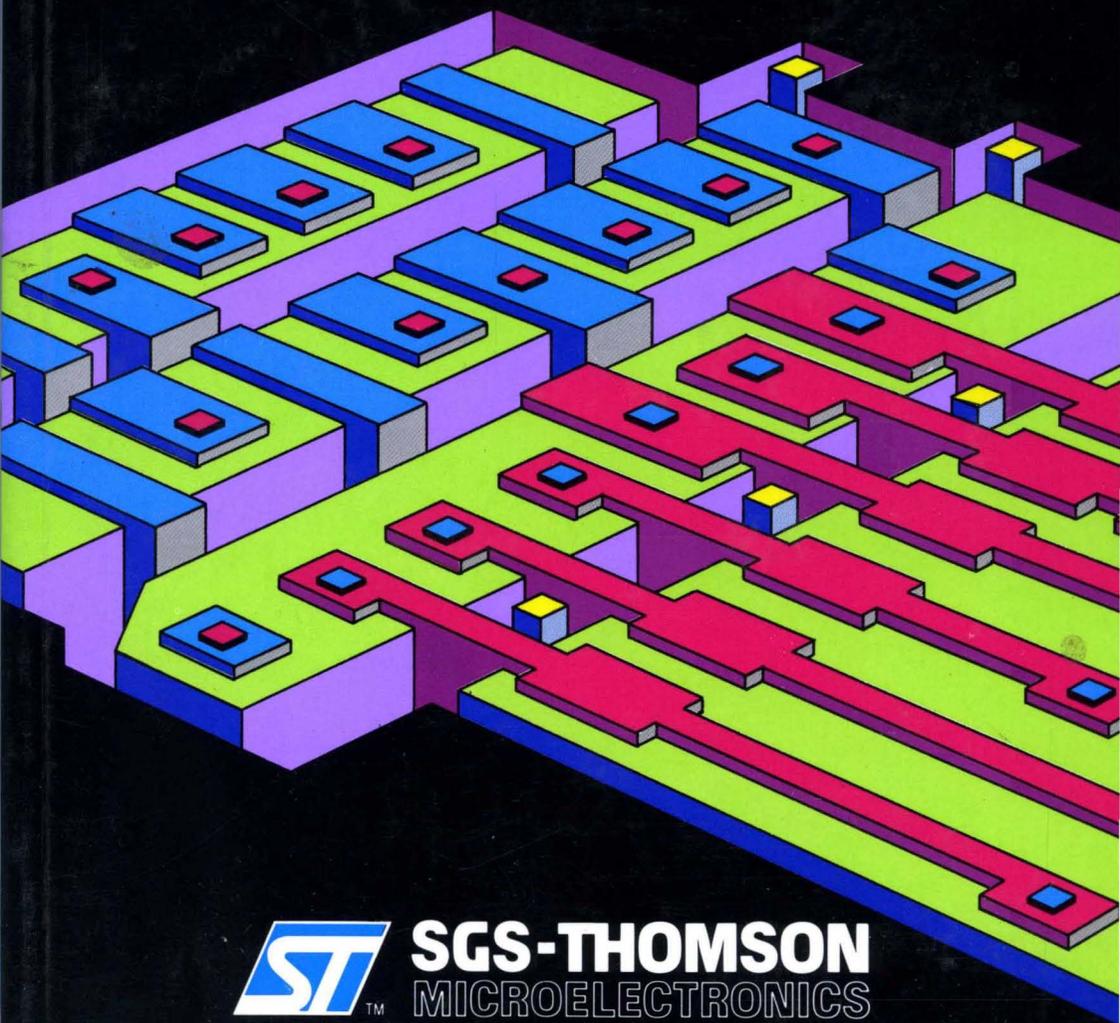


# GRAPHIC PROCESSORS

DATABOOK

1<sup>st</sup> EDITION



**SGS-THOMSON**  
MICROELECTRONICS

# **GRAPHIC PROCESSORS**

**DATABOOK**

**1<sup>st</sup> EDITION**

**MARCH 1989**



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# INTRODUCTION

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The SGS-THOMSON Graphics data book contains comprehensive data on three groups of graphics products: alphanumeric/semigraphics processors, full graphics processors and colour palettes. The optimised price/performance characteristics of the proven HMOS 2 technology, coupled with SGS-THOMSON's six years of successful participation in the graphics market, makes these products particularly suitable for low- to mid-range applications such as video games, home computers and CAD workstations.

The alphanumeric/semigraphic range is based around the highly successful EF9345 architecture. For applications requiring flexible character display with simple graphics support, these devices provide a low-cost, single-chip solution that includes a built-in character generator and attribute controller.

For applications requiring direct pixel addressing, with screen resolutions from  $256 \times 256$  up to  $2048 \times 2048$ , SGS-THOMSON offers several products based on the established EF9367 and the TS68483 advanced graphics processor. With integral drawing processors and character generators, these products combine high performance with cost-effectiveness.

Colour palette devices are now widely used to increase the number of displayable colours and to provide a direct interface with monitors. SGS-THOMSON is established in the low-end market with a number of devices that allow 16 of 4096 colours to be selected.

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# GENERAL INDEX

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# **PRODUCT GUIDE**



## ALPHANUMERIC and SEMI-GRAPHIC CRT CONTROLLERS

Part Number	Description	Format	Package	Page
<b>EF9345</b>	Single Chip Color CRT Controller On-Chip Attributes Controller On-Chip Character Generator R,G,B,I Video Shift Registers Page Memory up to 16K x 8 Bits	25/21 Rows of 40 or 80 Characters	DIP40 PLCC44	13
<b>TS9347</b>	Single Chip Color or B/W CRT Controller On-Chip Attributes Controller On-Chip Character Generator R,G,B,I Video Shift Registers Analog Output: 8 Grey Levels Page Memory up to 32K x 8 Bits	25/21 Rows of 40 or 80 Characters	DIP40 PLCC44	63

## GRAPHICS CONTROLLERS

Part Number	Description	Format	Package	Page
<b>EF9365</b> <b>EF9366</b>	Graphics Coprocessor DRAMs Interface On-Chip ASCII Character Generator High-Speed Vector Drawing	512(256) x 512 Pixels 50 Hz	DIP40	107
<b>EF9367</b>	Graphics Coprocessor DRAMs Interface On-Chip ASCII Character Generator High-Speed Vector Drawing	512 x 1024 Pixels 50 Hz, 60 Hz	DIP40	137
<b>TS68483</b>	Alphanumeric and Graphic Drawing Capabilities Upto 256 Colors Four Video Shift Registers For Video rate Less than 18 Md/s Command Set: Vector, Arc, Circle Area Filling, Character	2048 x 2048 8-Bit Pixels	DIP64	171

## COLOR PALETTE

Part Number	Description	Format	Package	Page
<b>EF9369</b>	4-Bit DACs with Gamma Law Correction Marking Bit Upto 30 Mdots/s	16 Colors Among 4096	DIP28 PLCC28	215
<b>TS9370</b>	4-Bit DACs Marking Bit Upto 45 Mdots/s	16 Colors Among 4096	DIP28 PLCC28	231

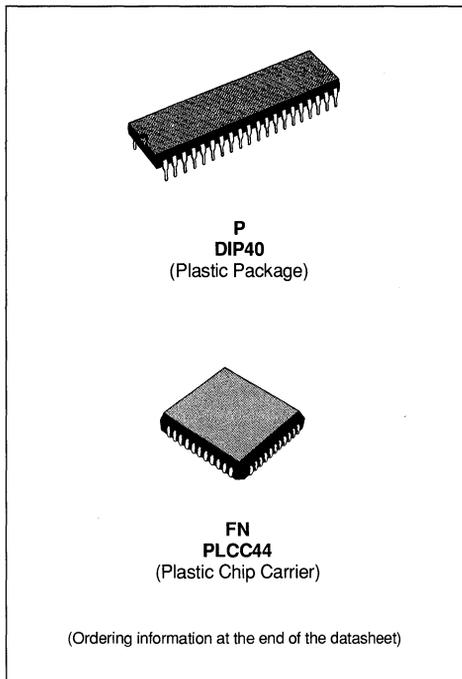


**ALPHANUMERIC and SEMI-GRAPHIC  
CRT CONTROLLERS**



**HMOS2 SINGLE CHIP SEMI-GRAPHIC  
DISPLAY PROCESSOR**

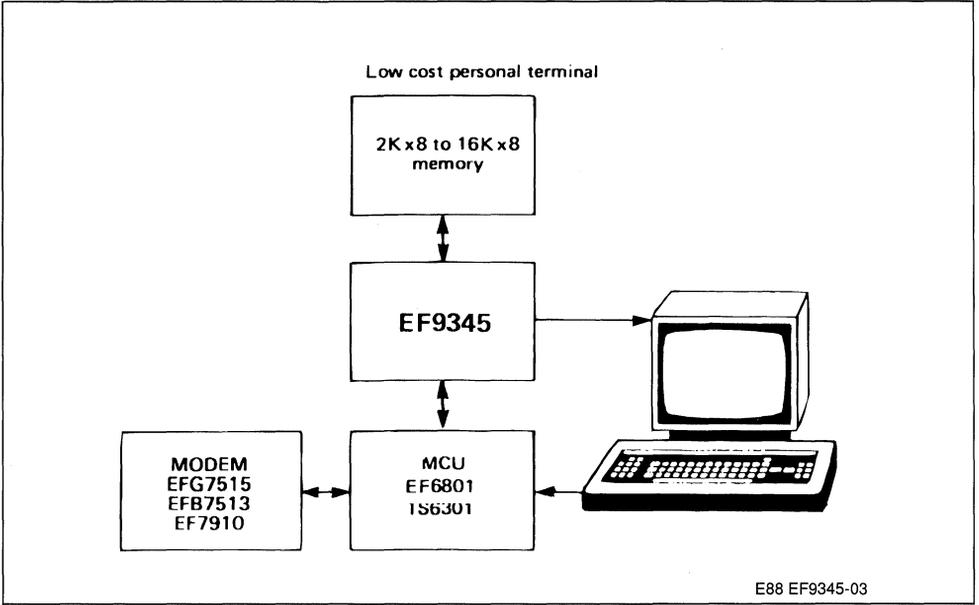
- SINGLE CHIP LOW-COST COLOR CRT CONTROLLER
- TV STANDARD COMPATIBLE (50 Hz or 60 Hz)
- 2 SCREEN FORMATS :
  - 25 (or 21) ROWS OF 40 CHARACTERS
  - 25 (or 21) ROWS OF 80 CHARACTERS
- ON-CHIP 128 ALPHANUMERIC AND 128 SEMI-GRAPHIC CHARACTER GENERATOR  
THREE STANDARD OPTIONS AVAILABLE FOR ALPHANUMERIC SETS
- EASY EXTENSION OF USER DEFINED ALPHANUMERIC OR SEMI-GRAPHIC SETS (> 1 K characters)
- 40 CHARACTERS/ROW ATTRIBUTES : foreground and background color, double height, double width, blinking, reverse, underlining, conceal, insert, accentuation of lower case characters
- 80 CHARACTERS/ROW ATTRIBUTES: Underlining, blinking, reverse, color select
- PROGRAMMABLE ROLL-UP, ROLL DOWN, AND CURSOR DISPLAY
- ON-CHIP R, G, B, I VIDEO SHIFT REGISTERS
- EASY SYNCHRONIZATION WITH EXTERNAL VIDEO SOURCE : ON-CHIP PHASE COMPARATOR
- ADDRESS/DATA MULTIPLEXED BUS DIRECTLY COMPATIBLE WITH STANDARD MICROCOMPUTERS SUCH AS 6801, 6301, 8048, 8051
- ADDRESSING SPACE : 16 K x 8 OF GENERAL PURPOSE PRIVATE MEMORY
- EASY USE OF ANY LOW COST MEMORY COMPONENTS : ROM, SRAM, DRAM
- UPWARD COMPATIBLE WITH EF9340/41 CHIP SET



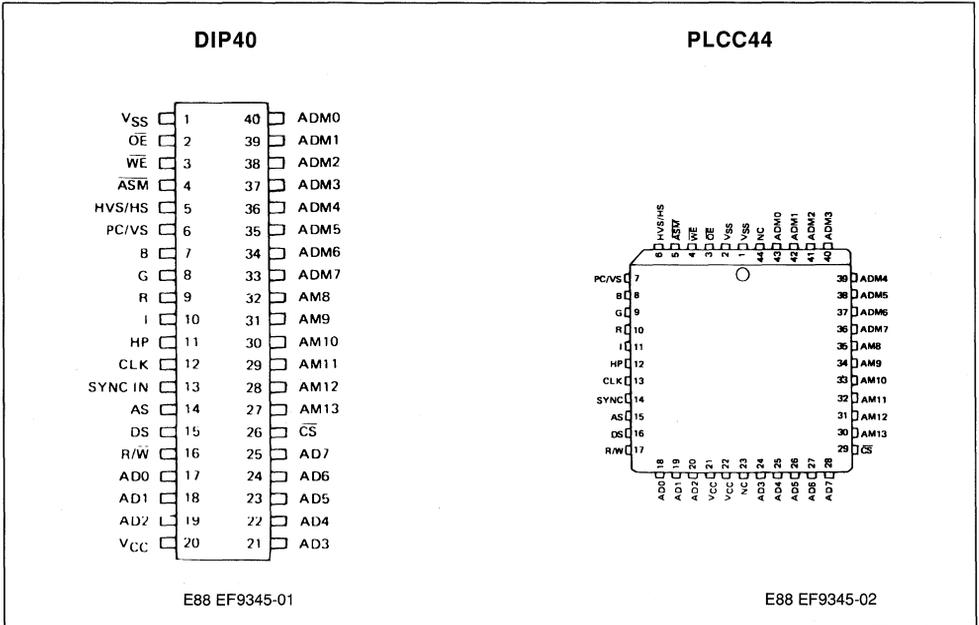
**DESCRIPTION**

The EF9345, new advanced color CRT controller, in conjunction with an additional standard memory package allows full implementation of the complete display control unit of a color or monochrome low-cost terminal, thus significantly reducing IC cost and PCB space.

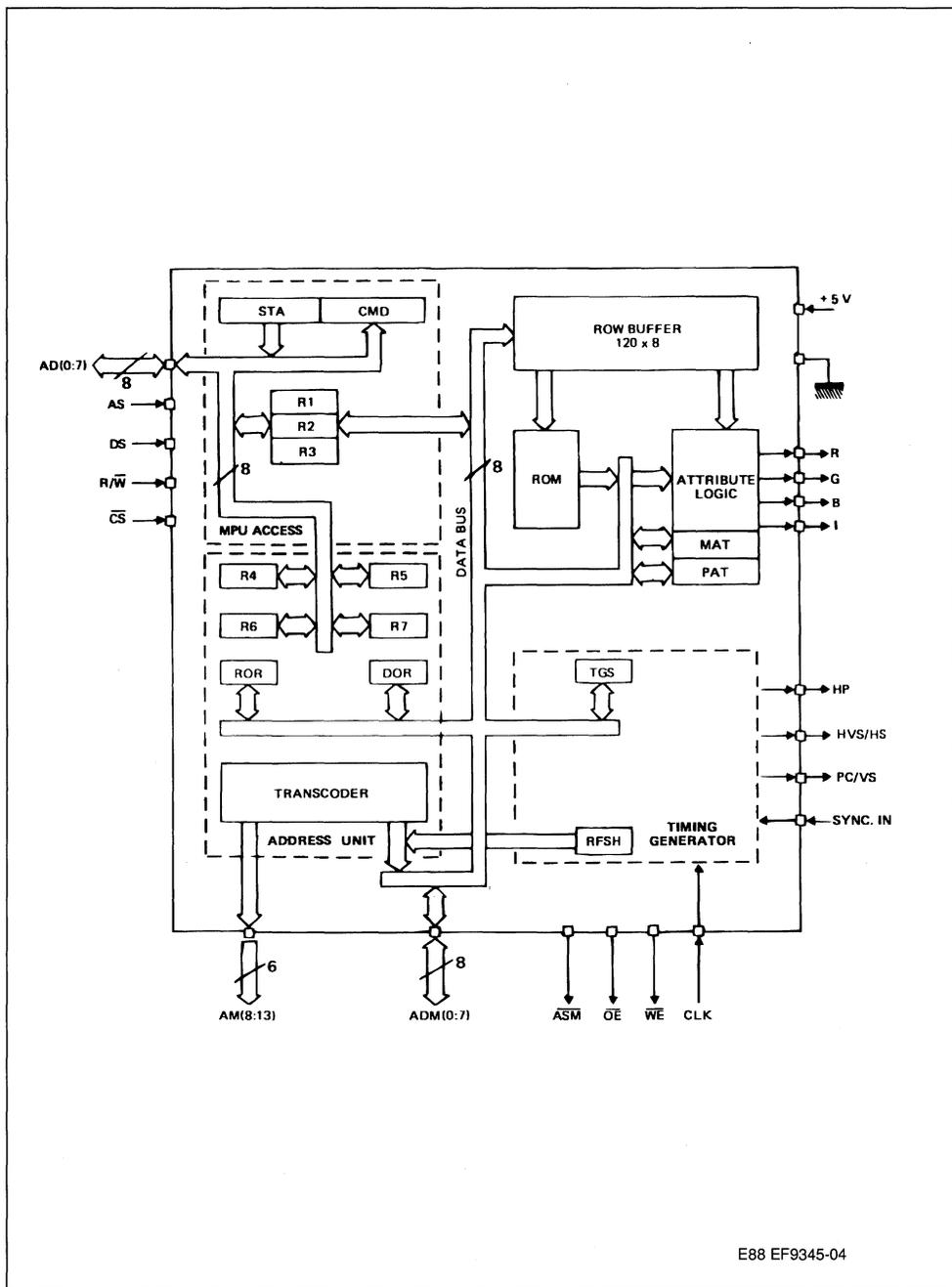
TYPICAL APPLICATION



PIN CONNECTION



BLOCK DIAGRAM



E88 EF9345-04

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}^*$	Supply Voltage	- 0.3 to 7.0	V
$V_{in}^*$	Input Voltage	- 0.3 to 7.0	V
$T_A$	Operating Temperature Range	0 to + 70	°C
$T_{stg}$	Storage Temperature	55 to + 150	°C
$P_{Dm}$	Max Power Dissipation	0.75	W

\* With respect to  $V_{SS}$ .

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0 V \pm 5\%$ ,  $V_{SS} = 0$ ,  $T_A = 0$  to  $70^\circ C$ )

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{CC}$	Supply Voltage	4.75	5	5.25	V
$V_{IL}$	Input Low Voltage	- 0.3	-	0.8	V
$V_{IH}$	Input High Voltage CLK	2.2	-	$V_{CC}$	V
	Other Inputs	2	-	$V_{CC}$	-
$I_{in}$	Input Leakage Current	-	-	10	$\mu A$
$V_{OH}$	Output High Voltage ( $I_{load} = - 500 \mu A$ )	2.4	-	-	V
$V_{OL}$	Output Low Voltage $I_{load} = 4 mA$ ; AD (0:7), ADM (0:7), AM (8:13) $I_{load} = 1 mA$ ; Other Outputs	0.4	-	-	V
		0.4	-	-	
$P_D$	Power Dissipation	-	250	-	mW
$C_{in}$	Input Capacitance	-	-	15	pF
$I_{TSI}$	Three State (off state) Input Current	-	-	10	$\mu A$

## MEMORY INTERFACE

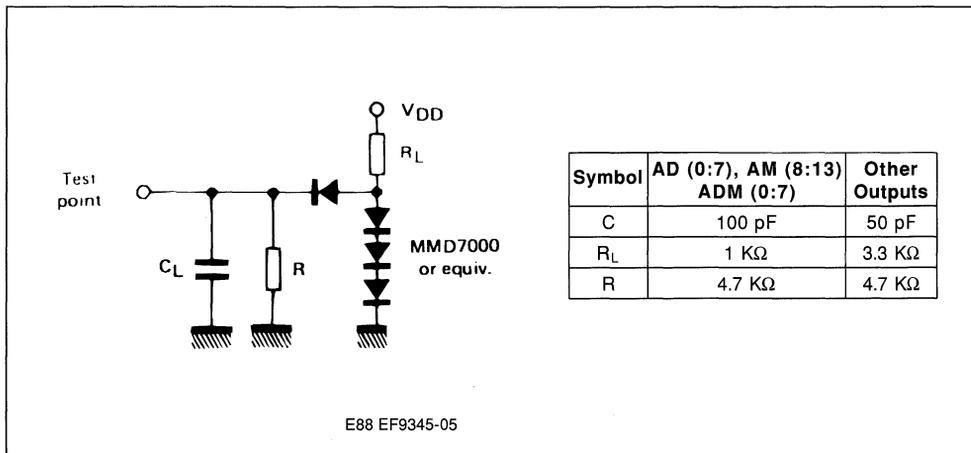
$V_{CC} = 5.0 \text{ V} \pm 5\%$ ,  $T_A = 0^\circ \text{ to } +70^\circ \text{ C}$ .

Clock :  $f_{in} = 12 \text{ MHz}$  ; Duty Cycle 40 to 60 % ;  $t_r, t_f < 5 \text{ ns}$

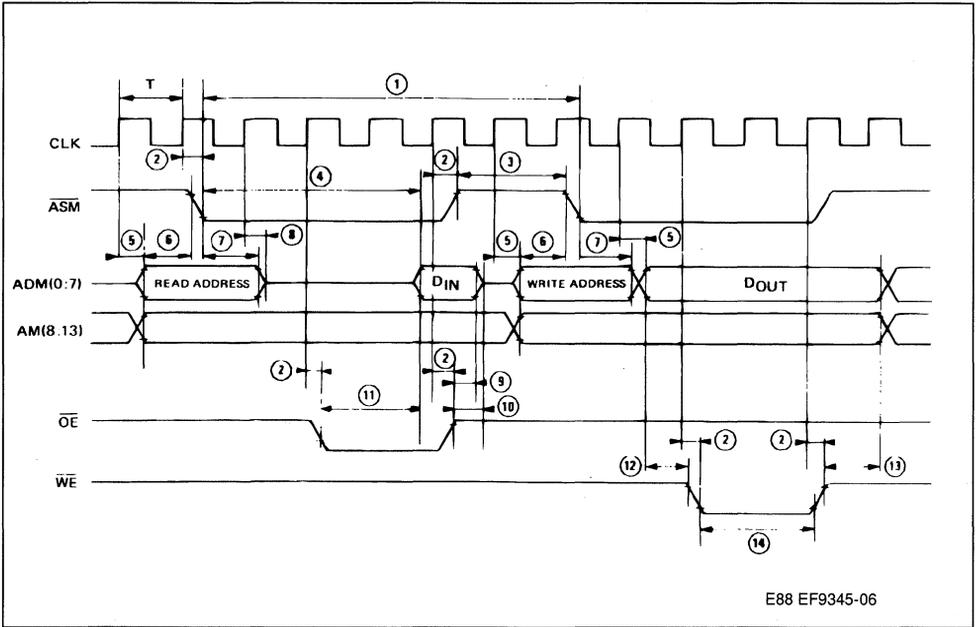
Reference Levels :  $V_{IL} = 0.8 \text{ V}$  and  $V_{IH} = 2 \text{ V}$ ,  $V_{OL} = 0.4 \text{ V}$  and  $V_{OH} = 2.4 \text{ V}$ .

Symbol	Ident. Number	Parameter	Min.	Typ.	Max.	Unit
$t_{EHEL}$	1	Memory Cycle Time	–	500	–	ns
$t_D$	2	Output Delay Time from CLK Rising Edge ( $\overline{ASM}$ , $\overline{OE}$ , $\overline{WE}$ )	–	–	60	ns
$t_{EHEL}$	3	$\overline{ASM}$ High Pulse Width	120	–	–	ns
$t_{ELDV}$	4	Memory Access Time from $\overline{ASM}$ Low	–	–	290	ns
$t_{DA}$	5	Output Delay Time from CLK Rising Edge (ADM (0:7), AM (8:13))	–	–	80	ns
$t_{AVEL}$	6	Address Setup Time to $\overline{ASM}$	30	–	–	ns
$t_{ELAX}$	7	Address Hold Time from $\overline{ASM}$	55	–	–	ns
$t_{CLAZ}$	8	Address Off Time	–	–	80	ns
$t_{GHDX}$	9	Memory Hold Time	10	–	–	ns
$t_{OZ}$	10	Data Off Time from $\overline{OE}$	–	–	60	ns
$t_{GLDV}$	11	Memory $\overline{OE}$ Access Time	–	–	150	ns
$t_{QVWL}$	12	Data Setup Time (write cycle)	30	–	–	ns
$t_{WHQX}$	13	Data Hold Time (write cycle)	30	–	–	ns
$t_{WLWH}$	14	$\overline{WE}$ Pulse Width	110	–	–	ns

## TEST LOAD



**MEMORY INTERFACE TIMING DIAGRAM**



**MICROPROCESSOR INTERFACE**

EF9345 is motel compatible. It automatically selects the processor type by using AS input to latch to state of the DS input.

No external logic is needed to adapt bus control signals from most of the common multiplexed bus microprocessors.

EF9345	6801	INTEL Family
	<b>Timing 1</b>	<b>Timing 2</b>
AS	AS	ALE
DS	DS, E <sub>1</sub> , φ 2	RD
R/W	R/W	WR

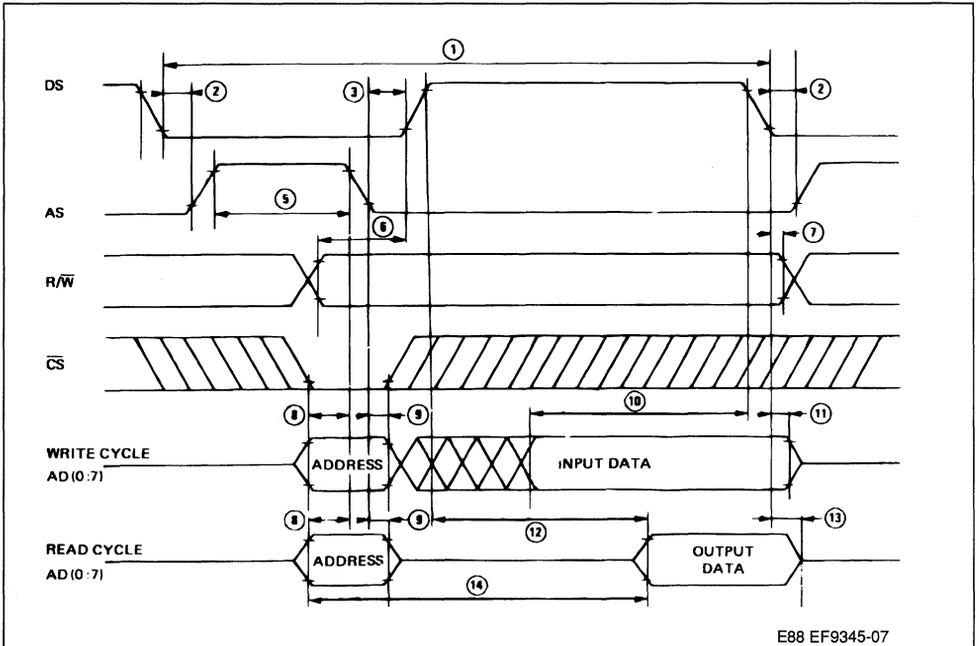
**MICROPROCESSOR INTERFACE TIMING AD (0:7), AS, DS, R/W, CS**

$V_{CC} = 5.0 \pm 5\%$ ,  $T_A = 0^\circ$  to  $+70^\circ\text{C}$ ,  $C_L = 100\text{ pF}$  on AD (0:7)

Reference Levels :  $V_{IL} = 0.8\text{ V}$  and  $V_{IH} = 2\text{ V}$  on All Inputs ;  $V_{OL} = 0.4\text{ V}$  and  $V_{OH}$  on All Outputs.

Symbol	Ident. Number	Parameter	Min.	Typ.	Max.	Unit
$t_{CYC}$	1	Cycle Time	400	-	-	ns
$t_{ASD}$	2	DS Low to AS High (timing 1) DS High or R/W High to AS High (timing 2)	30	-	-	ns
$t_{ASED}$	3	AS Low to DS High (timing 1) AS Low to DS Low or R/W Low (timing 2)	30	-	-	ns
$t_{PWEH}$	4	Write Pulse Width	200	-	-	ns
$t_{PWASH}$	5	AS Pulse Width	100	-	-	ns
$t_{RWS}$	6	R/W to DS Setup Time (timing 1)	100	-	-	ns
$t_{RWH}$	7	R/W to DS Hold Time (timing 1)	10	-	-	ns
$t_{ASL}$	8	Address and CS Setup Time	20	-	-	ns
$t_{AHL}$	9	Address and CS Hold Time	20	-	-	ns
$t_{DSW}$	10	Data Setup Time (write cycle)	100	-	-	ns
$t_{DHW}$	11	Data Hold Time (write cycle)	10	-	-	ns
$t_{DDR}$	12	Data Access Time from DS (read cycle)	-	-	150	ns
$t_{DHR}$	13	DS Inactive to High Impedance State Time (read cycle)	10	-	80	ns
$t_{ACC}$	14	Address to Data Valid Access Time	-	-	300	ns

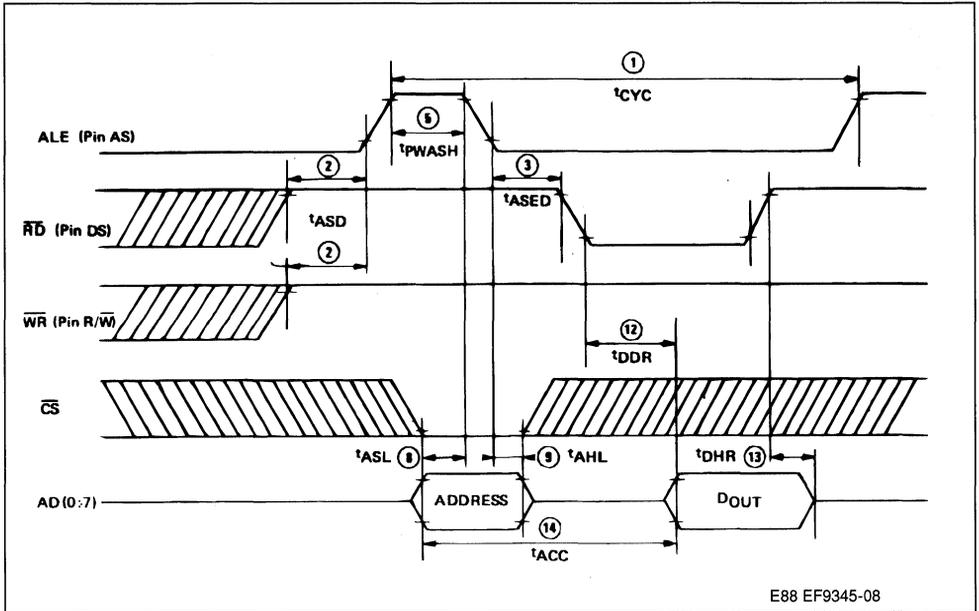
**MICROPROCESSOR INTERFACE TIMING DIAGRAM 1 (6801 type)**



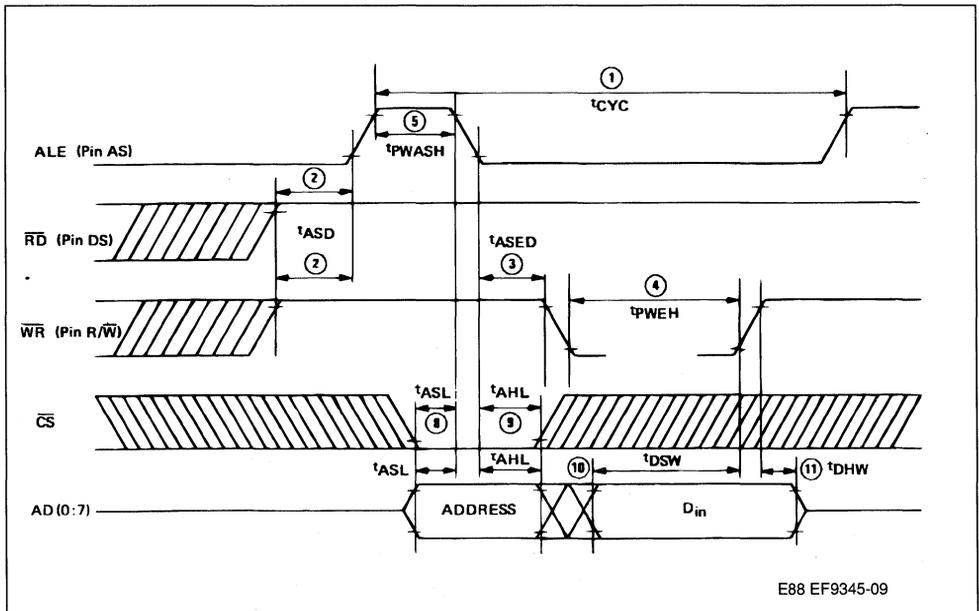
E88 EF9345-07

MICROPROCESSOR INTERFACE TIMING DIAGRAM 2 (INTEL type)

READ CYCLE



WRITE CYCLE

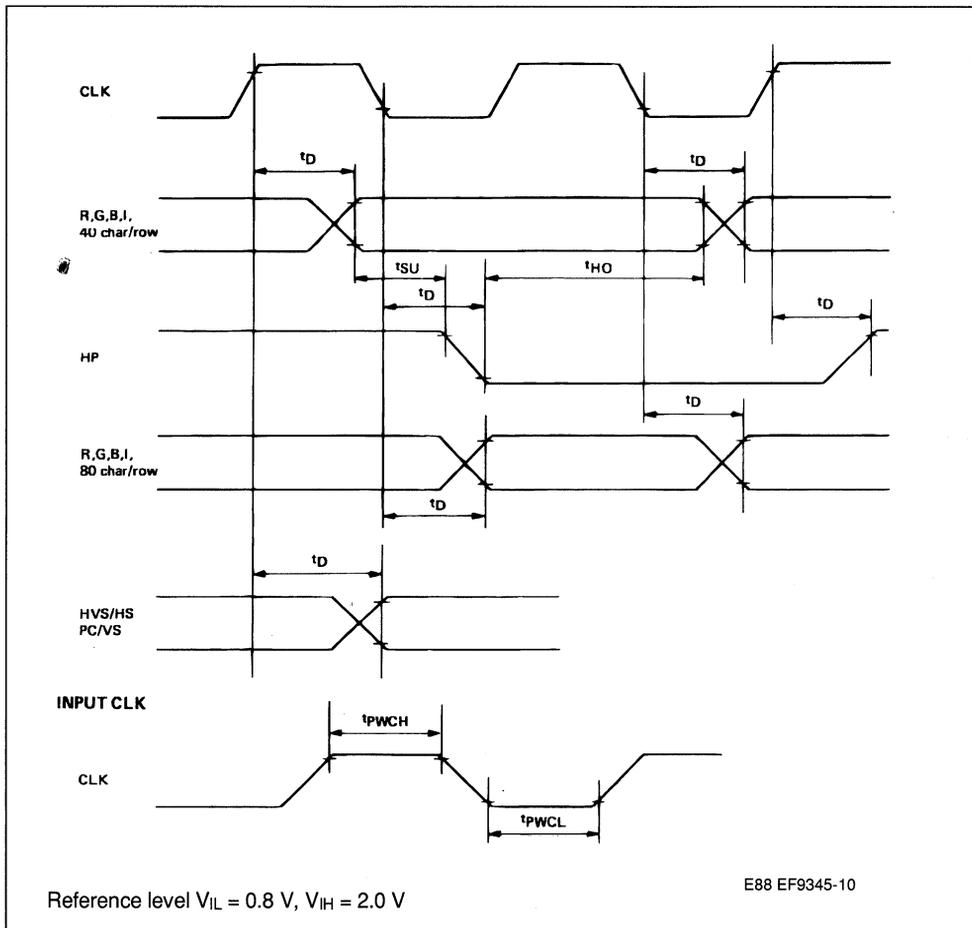


**VIDEO INTERFACE R, G, B, I, HP, HVS / HS, PC / VS**

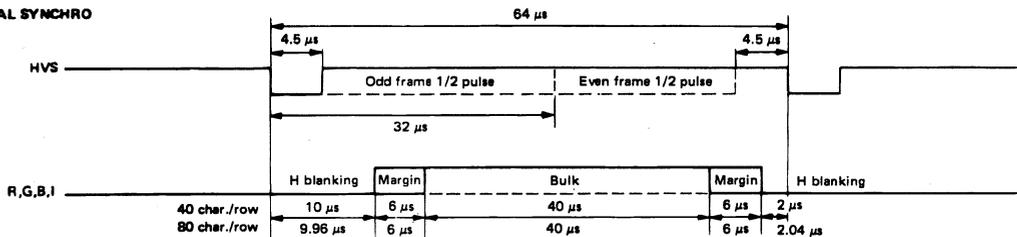
$V_{CC} = 5.0\text{ V} \pm 5\%$ ,  $T_A = 0^\circ\text{ to } +70\text{ }^\circ\text{C}$ , CLK Duty Cycle = 50 %,  $C_L = 50\text{ pF}$

Reference Levels :  $V_{IL} = 0.8\text{ V}$  and  $V_{IH} = 2.2\text{ V}$  on CLK input.  $V_{OL} = 0.4\text{ V}$  and  $V_{OH} = 2.4\text{ V}$  on all outputs.

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{SU}$	Setup Time R, G, B, I to HP	10	–	–	ns
$t_{HO}$	Hold Time R, G, B, I from HP	50	–	–	ns
$t_D$	Output Delay from CLK Edge	–	–	60	ns
$t_{PWCH}$	CLK High Pulse Width	30			ns
$t_{PWCL}$	CLK Low Pulse Width	30			ns

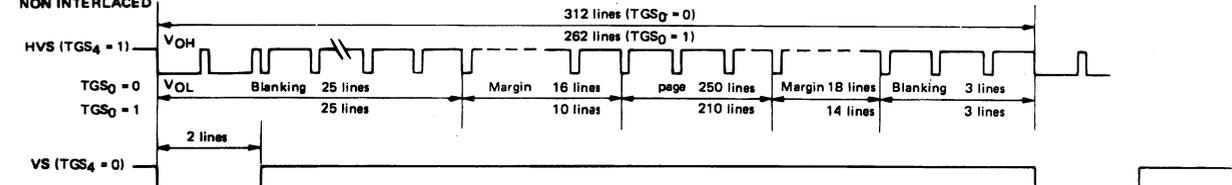


**HORIZONTAL SYNCHRO**

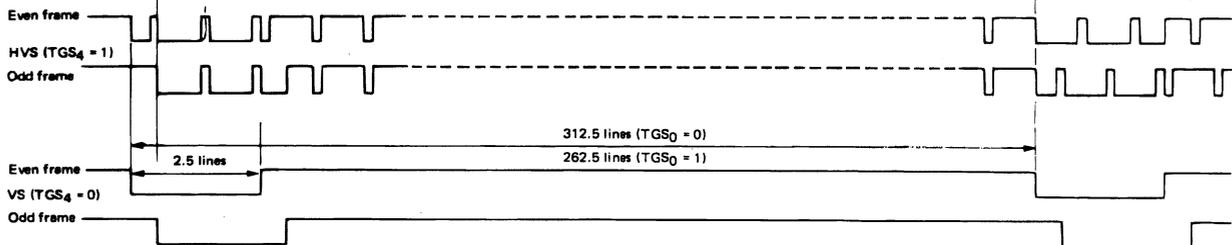


**VERTICAL SYNCHRO**

**NON INTERLACED**



**INTERLACED**



E88 EF9345-11

## EF 9345 PIN DESCRIPTION

All the input/output pins are TTL compatible.

### MICROPROCESSOR INTERFACE

Name	Pin Type	N°	Function	Description
AD (0:7)	I/O	17 – 19 21 – 25	Multiplexed Address/Data Bus	These 8 bidirectional pins provide communication with the microprocessor system bus.
AS	I	14	Address Strobe	The falling edge of this control signal latches the address on the AD (0:7) lines, the state of the Data Strobe (DS) and Chip Select (CS) into the chip.
DS	I	15	Data Strobe	When this input is strobed high by AS, the output buffers are selected while DS is low for a read cycle ( $R/\overline{W} = 1$ ). In write cycle, data present on AD (0:7) lines are strobed by $\overline{R/W}$ low (see timing diagram 2). When this input is strobed low by AS, $R/\overline{W}$ gives the direction of data transfer on AD (0:7) bus. $\overline{DS}$ high strobes the data to be written during a write cycle ( $R/\overline{W} = 0$ ) or enables the output buffers during a read cycle ( $R/\overline{W} = 1$ ). (see timing diagram 1).
$R/\overline{W}$	I	16	Read/Write	This input determines whether the internal registers get written or read. A write is active low ("0").
$\overline{CS}$	I	26	Chip Select	The EF9345 is selected when this input is strobed low by AS.

### MEMORY INTERFACE

Name	Pin Type	N°	Function	Description
ADM(0:7)	I/O	40 – 43	Multiplexed Address/Data Bus	Lower 8 bits of memory address appear on the bus when $\overline{ASM}$ is high. It then becomes the data bus when $\overline{ASM}$ is low.
AM (8:13)	O	32 – 27	Memory Address Bus	These 6 pins provide the high order bits of the memory address.
$\overline{OE}$	O	2	Output Enable	When low, this output selects the memory data output buffers.
$\overline{WE}$	O	3	Write Enable	This output determines whether the memory gets read or written. A write is active low ("0").
$\overline{ASM}$	O	4	Memory Address Strobe	This signal cycles continuously. Address can be latched on its falling edge.

### OTHER PINS

Name	Pin Type	N°	Function	Description
CLK	I	12	Clock Input	External TTL clock Input. (nominal value : 12 MHz, duty cycle : 50 %).
$V_{SS}$	S	1	Power Supply	Ground.
$V_{CC}$	S	20	Power Supply	+ 5 V

## VIDEO INTERFACE

Name	Pin Type	N°	Function	Description
R G B	O O O	7 8 9	Red Green Blue	These outputs deliver the video signal. They are low during the vertical and horizontal blanking intervals.
I	O	10	Insert	This active high output allows to insert R : G : B : in an external video signal for captioning purposes, for example. It can also be used as a general purpose attribute or color.
HVS/HS	O	5	Sync. Out	This output delivers either the composite synchro (bit TGS <sub>4</sub> = 1) or the horizontal synchro signal (bit TGS <sub>4</sub> = 0).
PC/VS	O	6	Phase Comparator / Vertical Sync	When TGS <sub>4</sub> = 1, this signal is the phase comparator output. When TGS <sub>4</sub> = 0, this output delivers the vertical synchro signal.
SYNC IN	I	13	Synchro In	This input allows vertical and/or horizontal synchronizing the EF9345 on an external signal. It must be grounded if not used.
HP	O	11	Video Clock	This output delivers a 4 MHz clock phased with the R, G, B, I signals

## GENERAL DESCRIPTION

The EF9345 is a low cost, semigraphic, CRT controller.

It is optimized for use with a low cost, monochrome or color TV type CRT (64  $\mu$ s per line, 50 or 60 Hz refresh frequency).

The EF9345 displays up to 25 rows of 40 characters or 25 rows of 80 characters.

The on-chip character generator provides a 128 standard, 5 x 7, character set and standard semigraphic sets.

More user definable (8 x 10) alphanumeric or semigraphic sets may be mapped in the 16 K x 8 private memory addressing space.

These user definable sets are available only in 40 characters per row format.

## MICROPROCESSOR INTERFACE.

The EF9345 provides an 8-bit, address/data multiplexed, microprocessor interface.

It is directly compatible with popular (6801, 8048, 8051, 8035...) microprocessors.

## REGISTERS.

The microprocessor directly accesses 8 registers :

- R0 : Command/status register
- R1, R2, R3 : Data registers
- R4, R5 } : Each of these register pairs points  
R6, R7 } into the private memory.

Through these registers, the microprocessors indirectly accesses the private memory and 5 more registers :

- ROR, DOR : Base address of displayed page memory and of used external character generators.
- PAT, MAT, TGS : Used to select the page attributes and format, and to program the timing generator option.

## PRIVATE MEMORY

The user may partition the 16 K x 8 private memory addressing space between :

- pages of character codes (2 K x 8 or 3 K x 8),
- external character generators,
- general purpose user area.

Many types of memory components are suitable :

- ROM, DRAM or SRAM,
- 2 K x 8, 8 K x 8, 16 K x 4 organizations,
- Modest 500 ns cycle time and 250 ns access time is required.

## 40 CHARACTERS PER ROW : CHARACTER CODE FORMATS AND ATTRIBUTES.

Once the 40 characters per row format has been selected, one character code format out of three must be chosen :

- 24-bit fixed format :  
All the attributes are provided in parallel.
- 8/24-bit compressed format :  
All the attributes are latched.
- 16-bit fixed format :  
Some parallel attributes, other are latched.

The 16-bit fixed format is compatible with EF9340/41 CRT controller.

Character attributes provided :

- Background and foreground color (3 bits each),
- Double height, double width,
- Blinking,
- Reverse,
- Underlining,
- Conceal,
- Insert,
- Accentuation of lower case characters
- 3 x 100 user definable character generator in memory
- 8 x 100 semi-graphic quadrichrome characters.

80 CHARACTERS PER ROW FORMAT : CHARACTER CODE FORMAT AND ATTRIBUTES.

Two character code formats are provided :

- Long (12 bits) with 4 parallel attributes :
  - Blinking,
  - Underlining,
  - Reverse,
  - Color select.
- Short (8 bits) : no attributes.

TIMING GENERATOR.

The whole timing is derived from a 12 MHz main clock input.

The RGB outputs are shifted at 8 MHz for the 40 character/row format and at 12 MHz for the 80 character/row.

Besides, the user may select :

- 50 Hz or 60 Hz vertical sync. frequency,
- Interlaced or not,
- Separated or composite vertical and horizontal sync. outputs.

Furthermore, a composite sync. input allows, when it is required :

- An on-chip vertical resynchronization,
- An on-chip crude horizontal resynchronization,
- An off-chip high performance horizontal resynchronization by use of a simple external VCXO controlled by the on-chip phase comparator.

## MEMORY ORGANIZATION

LOGICAL AND PHYSICAL ADDRESSING.

The physical 16-Kbyte addressing space is logically partitioned by EF9345 into 40-byte **buffers** (figure 1). More precisely, a logical address is given by an X, Y, Z triplet where :

- X = (0 to 39) points to a byte inside a buffer,
- Y = (0, 1 ; 8 to 31) points to a buffer inside a 1 Kbyte block,
- Z = (0 to 15) points to a **block**.

Obviously,  $1\text{ K} = 2^{10} = 1024$  cannot be exactly divided by 40. Consequently, any block holds 25 full buffers and a 24-byte remainder. Provided that the physical memory is a multiple of 2 Kbytes, the remainders are paired in such a way as to make available :

- a full buffer (Y = 1) in each even block,
- a partial buffer (Y = 1 ; X = 32 to 39) in each odd block.

POINTERS.

Each X, Y and Z component of a logical address is binary encoded and packed in two 8-bit registers. Such a register pair is a pointer (figure 2). EF9345 contains two pointers :

- R4, R5 : **auxiliary pointer**,
- R6, R7 : **main pointer**.

R5 and R7 have the same format. Each one holds an X component and the two LSB's of a Z component. This packing induces a partitioning of Z in 4 **districts** of 4 blocks each.

R5, R7 points to a block number in a district. R4 and R6 have a slightly different format : Each one holds a Y component and the LSB of the district number. But R6 holds both district MSB.

Figure 4 gives the logical to physical address trans-coding scheme performed on chip.

Figure 1 : Memory Row Buffer.

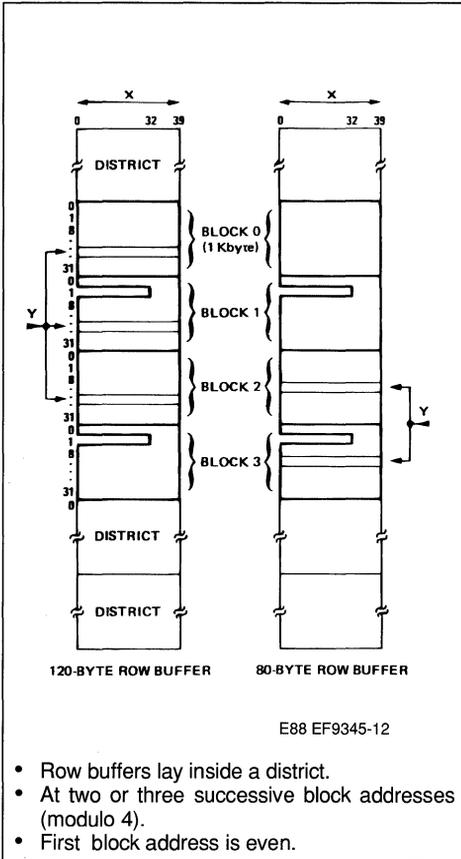
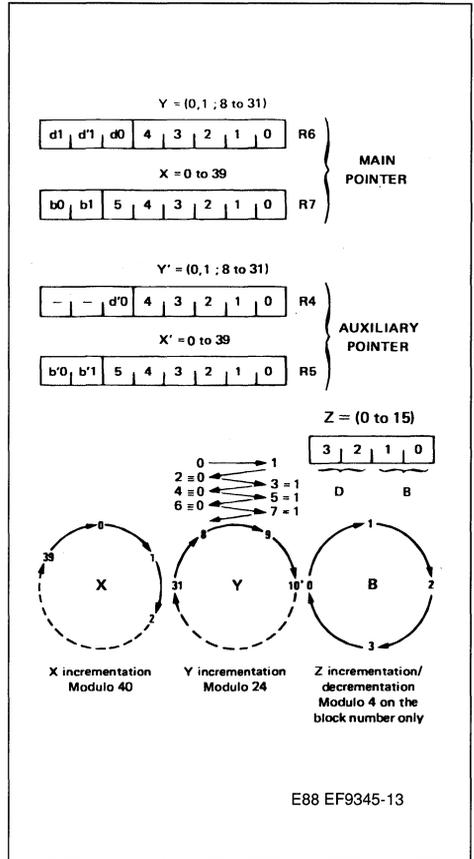


Figure 2 : Pointer Auto Incrementation.



DATA STRUCTURES IN MEMORY.

A **page** is a data structure displayable on the screen up to 25 rows of characters. According to the character code format, each row on the screen is associated with 2 (or 3) 40-byte buffers. This set of 2 (or 3) buffers constitutes a row **buffer** (figure 1). The buffers belonging to a row buffer must meet the following requirements :

- they have the same Y address,
- they have the same district number,
- they lie at 2 (or 3) successive (modulo 4) block addresses in their common district.

Consequently, a row buffer is defined by its first buffer address and its format.

A page is a set of successive row buffers :

- with the same format,
- with the same district number,

- with the same block address of first buffer. This block address must be even.
- lying at successive (modulo 24) Y addresses.

Consequently, a page should not cross a district boundary. General purpose memory area may be used but should respect the buffer or row buffer structure. See figure 2 for pointer incrementation implied by these data structures.

MEMORY TIME SHARING (see figure 3).

The memory interface provides a 500 ns cycle time. That is to say a 2 Mbyte/s memory bandwidth. This bandwidth is shared between :

- reading a row buffer from memory to load the internal row buffer (up to 120 bytes once each row),
- reading user defined characters slices from memory (1 byte each  $\mu$ s),

- indirect microprocessor read or write operation,
- refresh cycles to allow DRAM use, with no overhead.

A fixed allocation scheme implements the sharing.

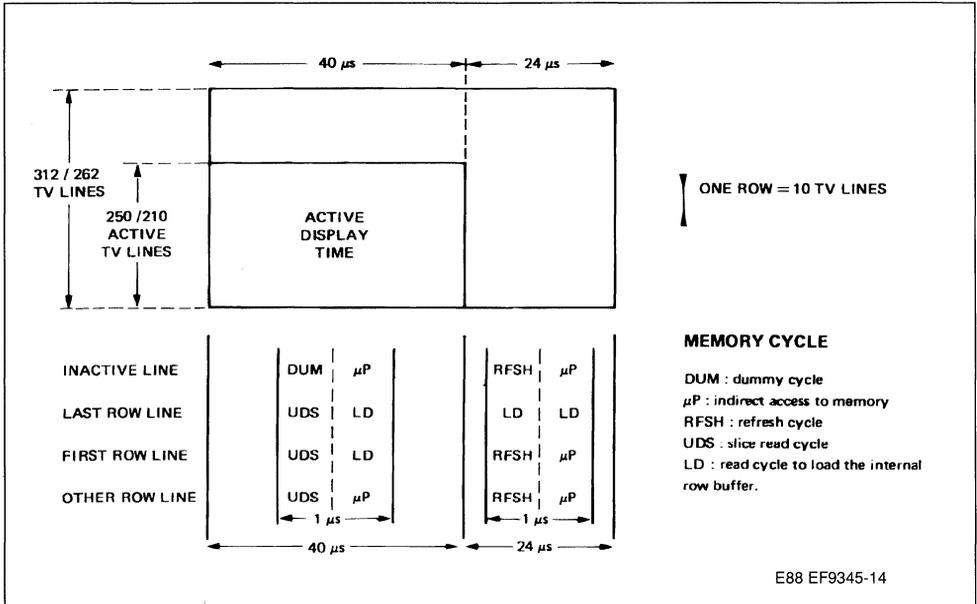
Notes on Figure 3.

1. Dummy cycles are read cycles at dummy addresses.
2. RFSH cycles are read cycles performed by an 8-bit auto-incrementing counter. Low order address byte ADM (0:7) cycles through its 256 states in less than 1 ms.

3. The microprocessor may indirectly access the memory once every  $\mu\text{s}$ , except during the first and the last line of a row, when the internal buffer must be loaded.

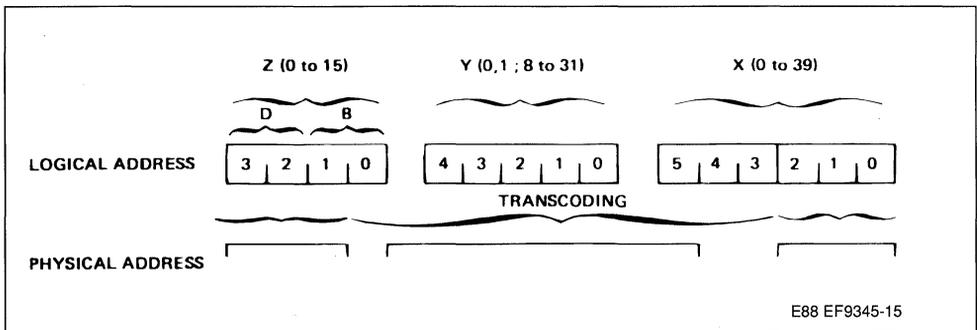
During these lines, no microprocessor access is provided for  $104 \mu\text{s}$ ; this hold too when no user defined character slices are addressed.

Figure 3 : Memory Cycle Allocation.



E88 EF9345-14

Figure 4 : Logical to Physical Address Transcoding Performed On-chip.



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X and Y Condition			PHYSICAL ADDRESS AM (3:10)							
			10	9	8	7	6	5	4	3
Y ≥ 8	X5 = 0		b0	Y4	Y3	Y2	Y1	Y0	X4	X3
	X5 = 1		b0	0	0	Y2	Y1	Y0	Y4	Y3
Y < 8	Y0 = 0		b0	0	0	X5	X4	X3	0	0
	Y0 = 1	b0 = 0	X3	0	0	1	$\overline{X5}$	$\overline{X4}$	0	0
		b0 = 1	1	0	0	1	X5	X4	0	0

## SCREEN FORMAT AND ATTRIBUTES

The screen format and attributes are programmed through 5 indirectly accessible registers : **ROR**, **TGS**, **PAT**, **MAT** and **DOR**. IND command allows accessing these registers. TGS is also used to select the timing generator options (see Screen Format Table).

### ROW AND CHARACTER CODE FORMAT

PAT<sub>7</sub> ; TGS<sub>(6:7)</sub>.

Two row formats and 5 character code formats are available but cannot be mixed in a given screen. DOR register interpretation is completely row format dependent and is discussed in the corresponding 40 char./row and 80 char./row section.

### SCREEN PARTITION - PAGE POINTER ROR (see top of the Screen Format Table).

The screen is partitionned into 3 areas :

- the margin,
- the service row,
- the bulk of remaining rows.

MAT<sub>(0:3)</sub> declares the color of the margin and the value  $I_M$  of its insert attribute.

ROR register points to the page to be displayed and gives the 3 MSB's of the Z address : Z<sub>0</sub> = 0 implicitly ; the page block address must be even. YOR gives the first row buffers to be displayed at the top of the bulk area. The next row buffers to be displayed are fetched sequentially by incrementing the Y address (modulo 24). This address never gets out of the origin block. Incrementation of YOR by the microprocessor yields a roll up.

### SERVICE ROW : TGS<sub>5</sub> - PAT<sub>0</sub>.

The service row is displayed for 10 TV lines on top of the screen and does not roll. Following TGS<sub>5</sub>, it is fetched from the origin block at either Y = 0 or Y = 1. The Y = 1 is a partial row buffer. It can be used only with variable 40 char./row and an 8 byte attribute file. The service row may be disabled by PAT<sub>0</sub> = 0 ; it is then displayed as a margin extension.

BULK : TGS<sub>0</sub> ; PAT<sub>(1:2)</sub> ; MAT<sub>7</sub>.

It is displayed after the service row for 200 or 240 TV lines according to TGS<sub>0</sub>. Each row buffer is usually displayed for 10 TV lines. However, MAT<sub>7</sub> = 1 doubles this figure. Then every character appears in double height (double height characters are quadrupled).

PAT<sub>1</sub> = 0 and/or PAT<sub>2</sub> = 0 disables respectively the upper 120 lines and/or the lower 80/120 lines of the bulk.

When disabled, the corresponding TV lines are displayed as a margin extension.

### CURSOR MAT<sub>(4:6)</sub>

To be displayed with the cursor attributes, a character must be pointed by the main pointer (R6, R7) and MAT<sub>6</sub> must be set. The cursor attributes are given by MAT<sub>(4:5)</sub> :

- **Complementation** : the R, G and B of each pixel is logically negated.  
R, G, B →  $\overline{R}$ ,  $\overline{G}$ ,  $\overline{B}$
- **Underline** : the underline attribute of this character is negated.
- **Flash** : the character is periodically displayed with, then without, its cursor attributes (50 % / 50 % ; ≈ 1 Hz).

### FLASH ENABLE (PAT<sub>6</sub>) - CONCEAL ENABLE (PAT<sub>3</sub>).

Any character flashing attribute is a "don't care" when PAT<sub>6</sub> = 0. When PAT<sub>6</sub> = 1, a character flashes if its flashing attribute is set. It is then periodically displayed as a space (50 % / 50 % ; ≈ 0.5 Hz).

PAT<sub>3</sub> is a "don't care" for 80 char./row formats. When any 40 char./row format is in use :

- if PAT<sub>3</sub> = 0, the conceal attribute of any character is a don't care.
- if PAT<sub>3</sub> = 1, the conceal attribute of each character is interpreted : a concealed character appears as a space on the screen.

**INSERT MODES : PAT<sub>(4;5)</sub>.**

During retrace, margin and extended margin periods, the I output pin delivers the value of the insert margin attribute.

$$I = I_M = MAT_4.$$

During active line period, the I output state is controlled by the Insert Mode and i, the insert attribute of each character. The I output pin may have several uses : (see figure below) :

- As a margin/active area signal in the active area mark mode.

- As a character per character marker signal in the character mark mode.
- As a video mixing signal in the two remaining modes, provided that the EF9345 has been vertically and horizontally synchronized with an external video source : the I pin allows mixing RGB outputs (I = 1) and the external video signal (I = 0). This mixing can be achieved by switching or ORing. It may occur for the complete character window (Boxing Mode) or only for the foreground pixels (Inlay Mode).

**VIDEO OUTPUTS DURING ACTIVE PERIODS**

Insert Mode	Char. Level		Outputs		NOTES :
	i	Pixels (1)	I	R, G, B (2)	
Active Area Mark	-	-	1	X	(1) <b>PIXEL TYPE</b> - : Don't care FOREGND = A foreground pixel is :
Character Mark	0	-	0	X	
Boxing	1	-	1	X	• Any pixel of a quadrichrome character, • A Pixel of a bichrome character generated from a "1" in the character generator cell.
	0	-	0	BLACK	
Inlay	1	-	1	X	(2) <b>RGB OUTPUTS</b> X : Not affected. BLACK : forced to low level.
	0	-	0	BLACK	
	1	BACKGND	0	BLACK	
	1	FOREGND	1	X	

**TIMING GENERATOR OPTIONS : TGS<sub>(0;4)</sub>**

TGS<sub>(0;1)</sub> select the number of lines per frame :

TGS <sub>1</sub>	TGS <sub>0</sub>	LINES	
0	0	312	NON INTERLACED
0	1	262	
1	0	312.5	INTERLACED
1	1	262.5	

The composite incoming SYNC IN signal is separated into 2 internal signals :

- Vertical Synchronization In (VSI),
- Horizontal Synchronization In (HSI).

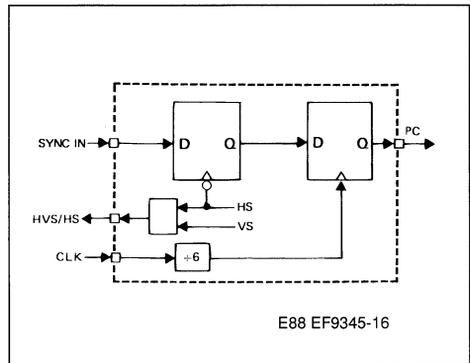
TGS<sub>3</sub> enables VSI to reset the internal line count. SYNC IN input is sampled at the beginning of the active area of each line. When the sample transits from 1 to 0, the line count is reset at the end of the current line.

TGS<sub>2</sub> enables HSI to control an internal digital phase lock loop. HSI and on-chip generated HS Out are considered as in phase if their leading edges match at ±1 clock period.

When they are out of phase, the line period is lengthened by 1 clock period (≈ 80 ns).

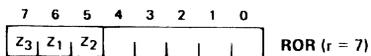
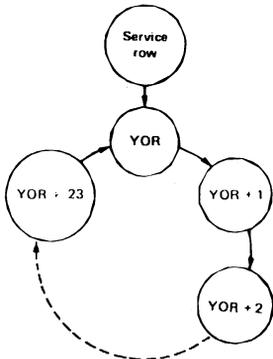
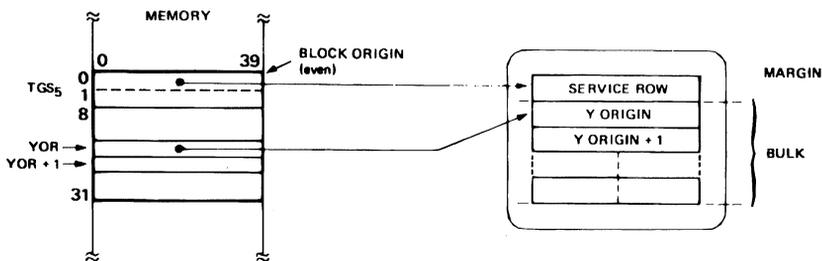
TGS<sub>4</sub> controls the SYNC OUT pins configuration :

TGS <sub>4</sub>	HVS / HS	PC / VS
1	Composite Sync	PC
0	H Sync Out	V Sync Out

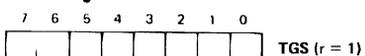


PC is the output of the on-chip phase comparator. An external VCXO allows a smoother horizontal phase lock than the internal scheme.

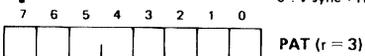
SCREEN FORMAT TABLE



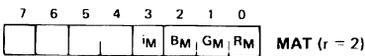
Origin row address  
YOR = (8 to 31)  
Block origin (even)  
Service row select  
(Y = 1/0)



525/525 lines  
Interlaced  
Horizontal resync enable  
Vertical resync enable  
Sync out pins configuration  
1 : Composite sync + phase comparator  
0 : V sync + H sync



Service row enable  
Upper bulk enable  
Lower bulk enable  
Conceal enable  
Flash enable



Margin color  
Margin insert  
Cursor display enable  
Double height

CHAR CODE	PAT <sub>7</sub>	TGS <sub>7</sub>	TGS <sub>6</sub>
40 CHAR LONG	0	0	0
40 CHAR VAR	0	0	1
40 CHAR SHORT	1	0	0
80 CHAR LONG	0	1	1
80 CHAR SHORT	0	1	0

INSERT MODE	PAT <sub>5</sub>	PAT <sub>4</sub>
INLAY	0	0
BOXING	0	1
CHARACTER MARK	1	0
ACTIVE AREA MARK	1	1

CURSOR DISPLAY MODE	MAT <sub>5</sub>	MAT <sub>4</sub>
FIXED COMPLEMENTED	0	0
FLASH COMPLEMENTED	1	0
FIXED UNDERLINED	0	1
FLASH UNDERLINED	1	1

NOTE : PROGRAMMING BIT VALUE  
1 = True  
0 = False

### 40 CHAR/ROW CHARACTER CODES

To display pages in 40 character per row format, one out of three character code formats must be selected :

- Fixed long (24 bits) code : all parallel attributes.
- Fixed short (16 bits) code : mix of parallel and latched attributes.
- Variable (8/24 bits) code : all latched attributes.

Fixed short and variable codes are translated into fixed long codes by EF9345 during the internal row buffer loading process. The choice of the character code format is obviously a display flexibility/memory size trade off, left up to the user.

#### FIXED LONG CODES.

This is the basic 40 char./row code. Each 8 pixels x 10 lines character window, on the screen is associated with a 3-byte code in memory, namely the C, B and A bytes (figure 5). A row on the screen is associated with a 120 byte row buffer in memory.

#### 3-BYTE CODE STRUCTURE.

1. C7 is a don't care. Up to 128 characters may be addressed in each set. Each user definable set holds only 100 characters : C byte value ranges from 00 to 03 and 20 to 7F (hexa).
2. B(4:7) give the type and set number of the character.
3. All the bichrome characters have the same attributes except that alphanumerics may be underlined, semi-graphics cannot. Accentuated alphanumerics allow orthogonal accentuating of any one of the 32 lower case ROM characters with any of 8 accents (see figure 19).

4. Bichrome and quadrichrome characters use two different coloring schemes.

For bichrome characters, character code byte A defines a two color set by giving directly two color values (figure 6). The negative attribute exchanges the two values. Each bit of the slice byte selects one color value out of two.

The "A" byte in a quadrichrome character code defines an ordered 4 color set (figure 7). When more than 4 bits are set, higher ranking bits are ignored. When less than 4 bits are set, the color set is completed with implicit "white" value. The slice byte is shifted 2 bits at once at half the dot frequency ( $\approx 4$  MHz).

Each bit pair designates one color out of the 4 color sets.

Quadrichrome characters allow displaying up to 4 different colors (instead of 2) in any 8 x 10 window at the penalty of an halved horizontal resolution.

By programming the R attribute in byte B, one may chose to keep the full vertical resolution (1 slice per line) or to halve it (each slice is repeated twice). In any case, it is possible to change the color set freely from window to window and to mix freely all the character types. So, fairly complex pictures may be displayed at low memory cost.

#### HANDLING LONG CODES.

The KRF command allows an easy X, Y random access or an X sequential access to/from the micro-processor from/to a memory row buffer (figure 8).

Figure 5 : 40 Char / Row Fixed Long Codes.

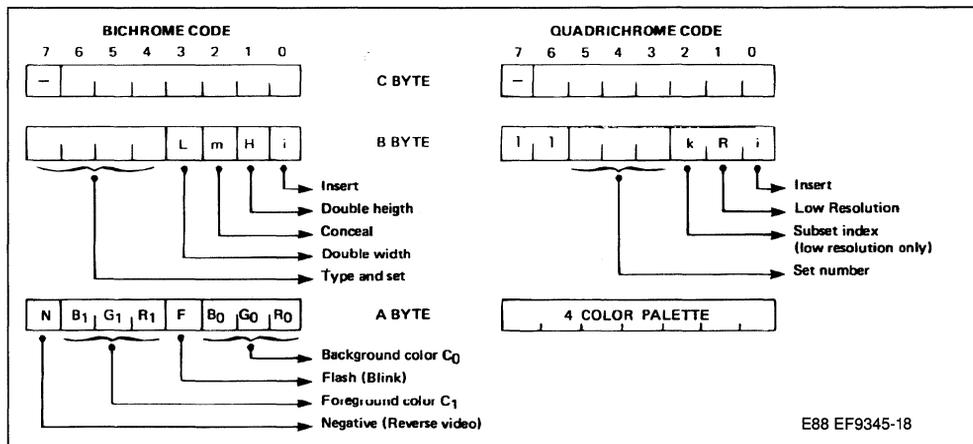


Figure 5 : (continued).

Type and Set Code : B(4:7)				Number of Character Per Set	Set Name	Set Type	Cell Location
7	6	5	4				
				C(0:6)			
0	0	1	0	128 Standard Mosaics 32 Strokes	G <sub>10</sub> G <sub>11</sub>	SEMI-GR.	B I C H R O M E
	0	1	1				
	0	0	0	128 Alphanumerics	G <sub>0</sub>	ALPHA	
1	0	1	Accented Lower Case Alpha	G <sub>20</sub> G <sub>21</sub> G' <sub>0</sub>			
1	1	1					
				100-Alpha UDS			
1	0	0	0	100 Semi-graphic UDS 100 Semi-graphic UDS	G' <sub>10</sub> G' <sub>11</sub>	SEMI-GR.	EXTERNAL MEMORY
	0	1	0				
	1	1	1	8 Sets of 100	Q <sub>0</sub> to Q <sub>7</sub>	QUADRICHROME	
				Quadrichrome Character			

Note : Programming bit value : 1 = True ; 0 = False.

Figure 6 : Coloring with Bichrome Characters.

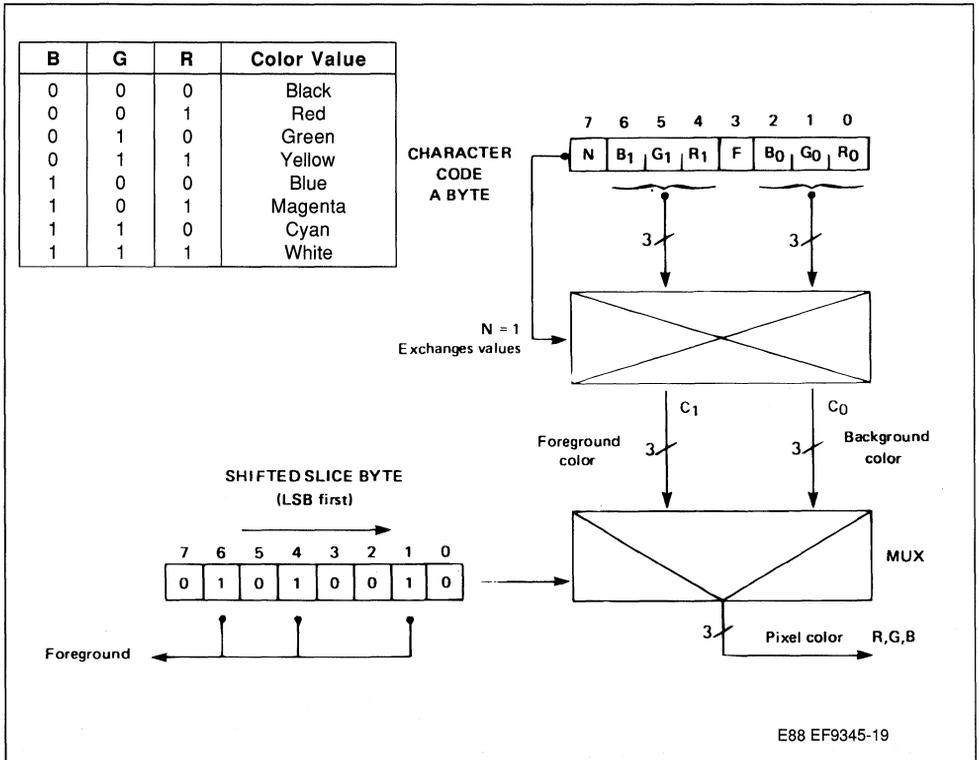


Figure 7 : Coloring with Quadrichrome Characters.

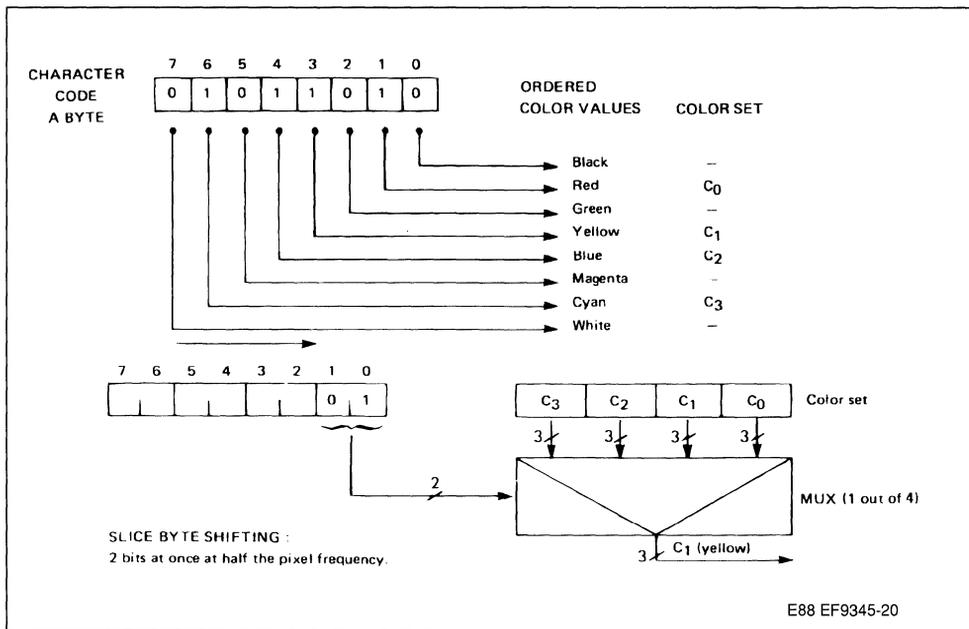
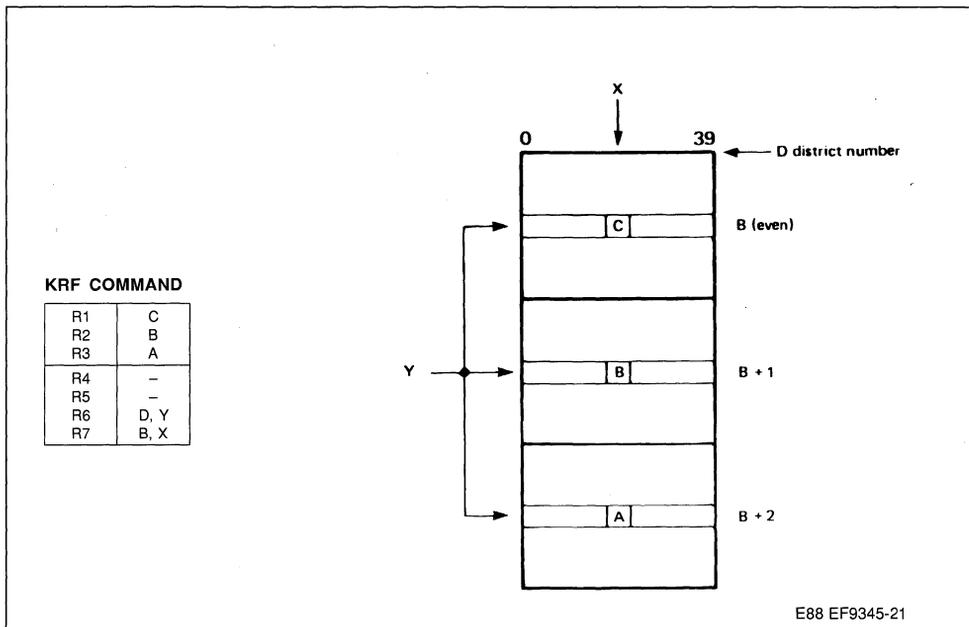


Figure 8 : Fixed Long Codes in Memory 120 Byte Row Buffer.



**VARIABLE CODES**

In many cases, successive characters on screen belong to the same character set and have the same attributes. Variable codes achieve memory saving by storing B and A bytes only when it is required by exploiting the C7 bit.

C7 = 1 This is a long 3-byte code.

Character set and attribute values are completely redefined by B and A bytes.

C7 = 0 This is a short 1-byte code.

Character set and attributes value are identical to the previous code.

A further saving comes from the fact that an accentuated alphabetic character is, more often than not, followed by a not accentuated alphabetic character.

So, G<sub>20</sub> or G<sub>21</sub> sets are processed as one-shot escape with return to G<sub>0</sub>. For normal operation, variable codes should obey the following rules :

- the first character code of any row (X = 0) should be long,
- a character code may be short when it has the same attributes as the previous character code and belongs to the same set.

However :

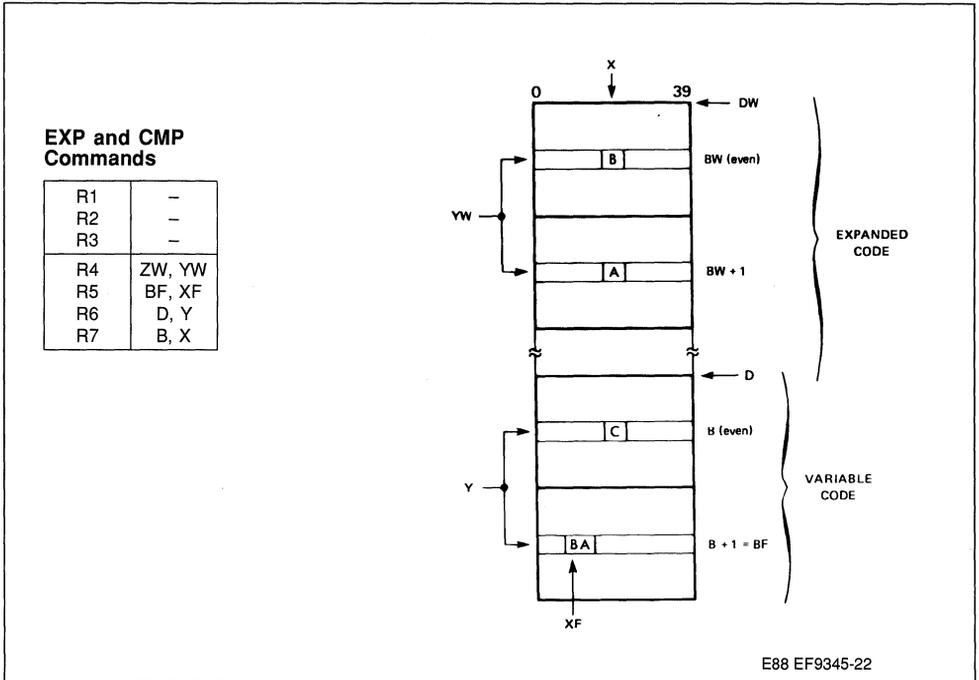
- any code belonging to G<sub>20</sub> or G<sub>21</sub> must be long and must be repeated if the character is double width,
- a code belonging to G<sub>0</sub> following a G<sub>20</sub> or G<sub>21</sub> code may be short.

**HANDLING THE VARIABLE CODES.**

During the display process, a row of variable code should be laid in an 80/120 byte row buffer. The first buffer holds the C bytes. The second buffer holds the B, A file providing up to 20 long codes per row (figure 10). In the exceptional case when this is not enough, the second buffer overflows in the third one. Every code may then be long. Variable codes can almost always achieve a memory saving over long fixed codes and can never be worse.

The KRV command gives a very easy sequential access to/from a row buffer from/to the microprocessor. This command automatically updates the C byte and the B, A file pointers (the last one when C7 is set).

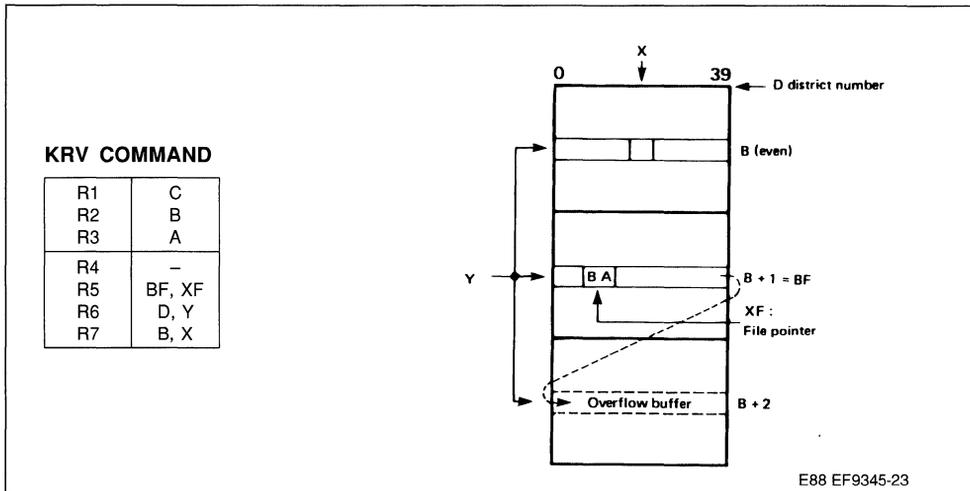
**Figure 9 :** Expansion / Compression Move.



Random access to a variable code is obviously not as easy. The EXP, KRE are CMP commands are designed to facilitate this task (figure 9).

The EXP command translates a full row of variable codes into a row of expanded codes. Expanded codes are generally not displayable but very similar to the long codes.

Figure 10 : Variable Codes in Memory.



**FIXED SHORT CODES.**

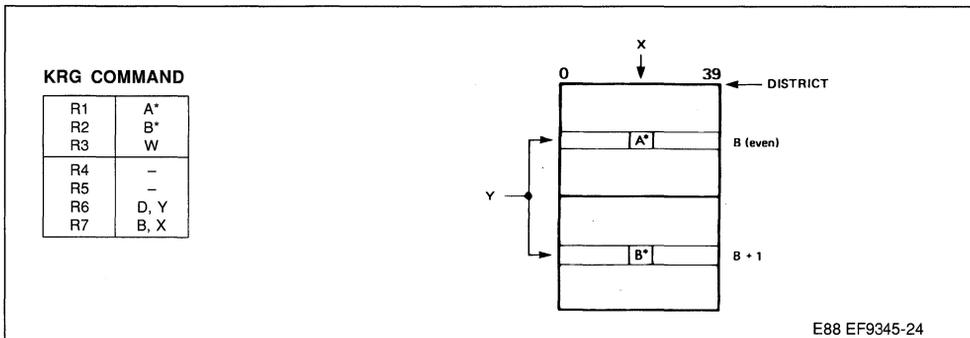
These fixed 16-bit codes are compatible with EF9340/41 display controllers. They achieve memory saving by another way. They may be easier to handle than variable codes. The penalty is in lesser display capabilities :

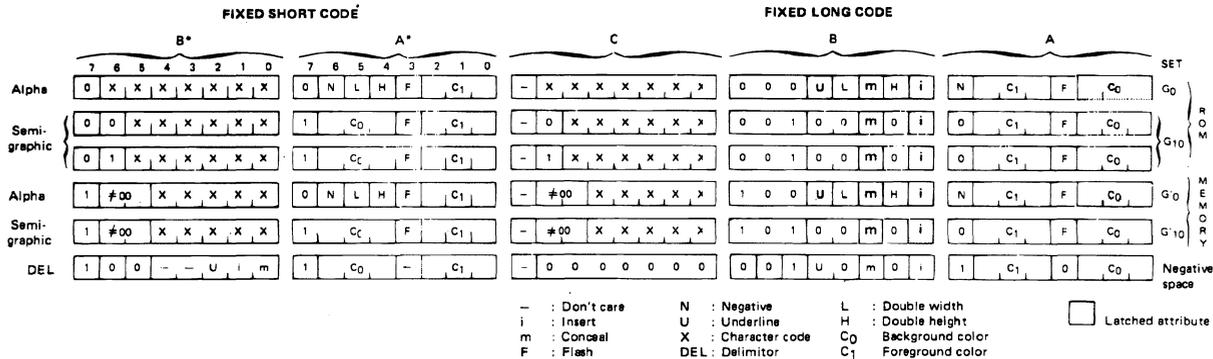
- accentuated character sets are no longer available : accentuated characters must be individually provided by the character generators.

- G<sub>11</sub> and quadrichrome sets cannot be reached,
- some attributes are latched and can be changed only while displaying a space (delimiter code).

The KRG command allows an easy access from/to an 80-byte row buffer in memory to/from the micro-processor (figure 11). Figure 12 gives the fixed short to fixed long translation process which occurs for each row - while loading the internal row buffer - before display.

Figure 11 : Fixed Short Codes in Memory 80 Byte Row Buffer.



**Notes :****1. Translation Process.**

The translation process operates through 3 elementary operations :

- Field-to-field : a character code or an attribute value (i.e : C<sub>0</sub>, flashing) is directly loaded from short to long code.
- Field-to-constant : the decoding of a short code forces the value of the equivalent long code attribute. For example, semigraphic short characters forces normal size (H = 0, L = 0) attributes.
- Latched attributes : at the beginning of each row, these attributes are reset (no underline, not concealed, black background). Then, they keep their current value until modified by either a field to field or field to constant operation.

**2. EF9340.41 Compatibility.**

It is binary code compatible with few exceptions :

- Flashing attribute is negated,
- A7 is negated in delimiters.

It is also display compatible with 2 exceptions concerning the underling :

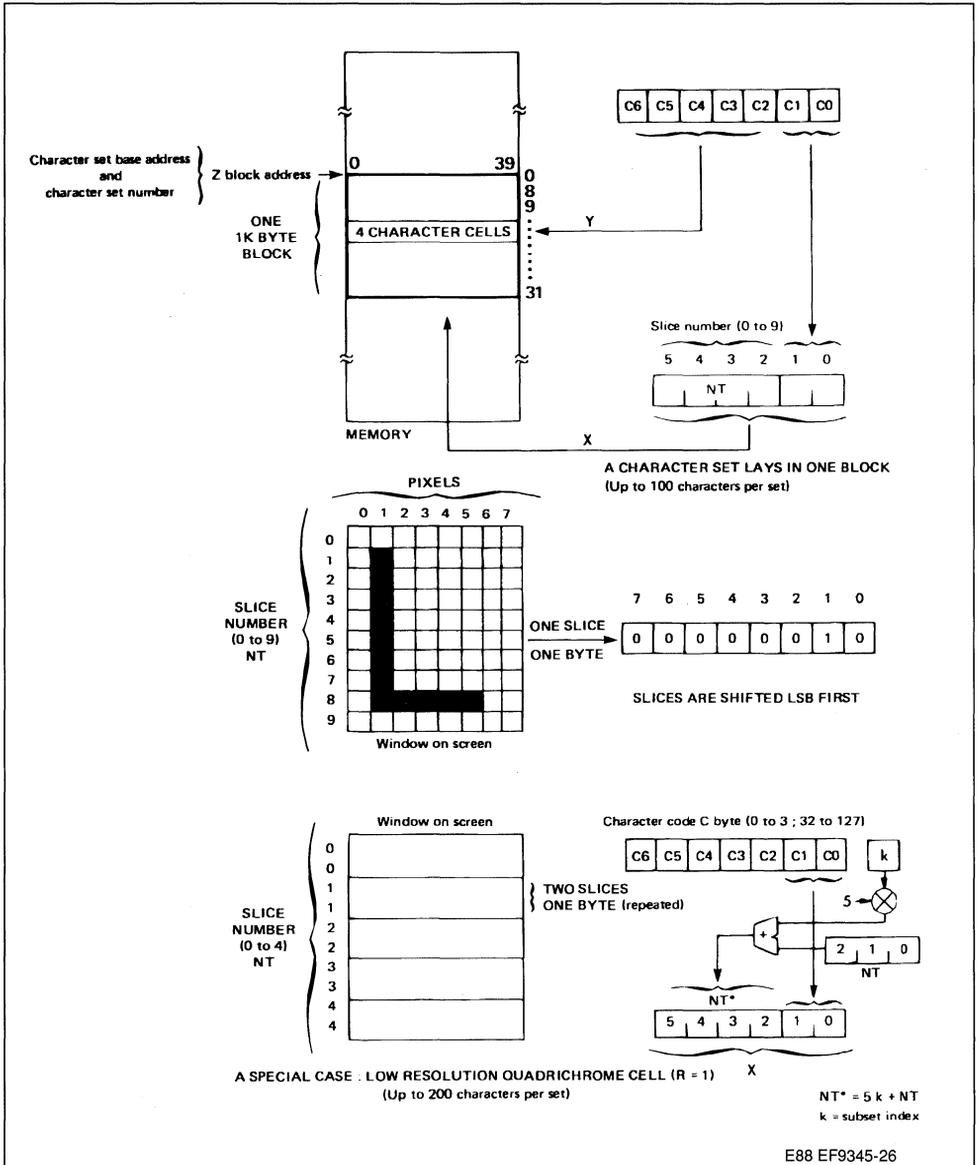
- An alphanumeric belonging to G<sub>0</sub> may be underlined,
- Any alphanumeric following a semigraphic cannot be underlined.

**USED DEFINED CHARACTER GENERATOR IN MEMORY : DOR REGISTER**

With 40 char /row, the elementary window dimensions on the screen are 10 slices x 8 pixels. Thus, a character cell holds 10 bytes in memory and 4 character cells are packed in one 40-byte buffer (fi-

gure 13). However, 5 bytes of a low resolution quadrichrome cell are enough to fill up to window. In this case, 8 character cells can be packed in one 40-byte buffer.

**Figure 13 : Packing UDS Cells in Memory.**

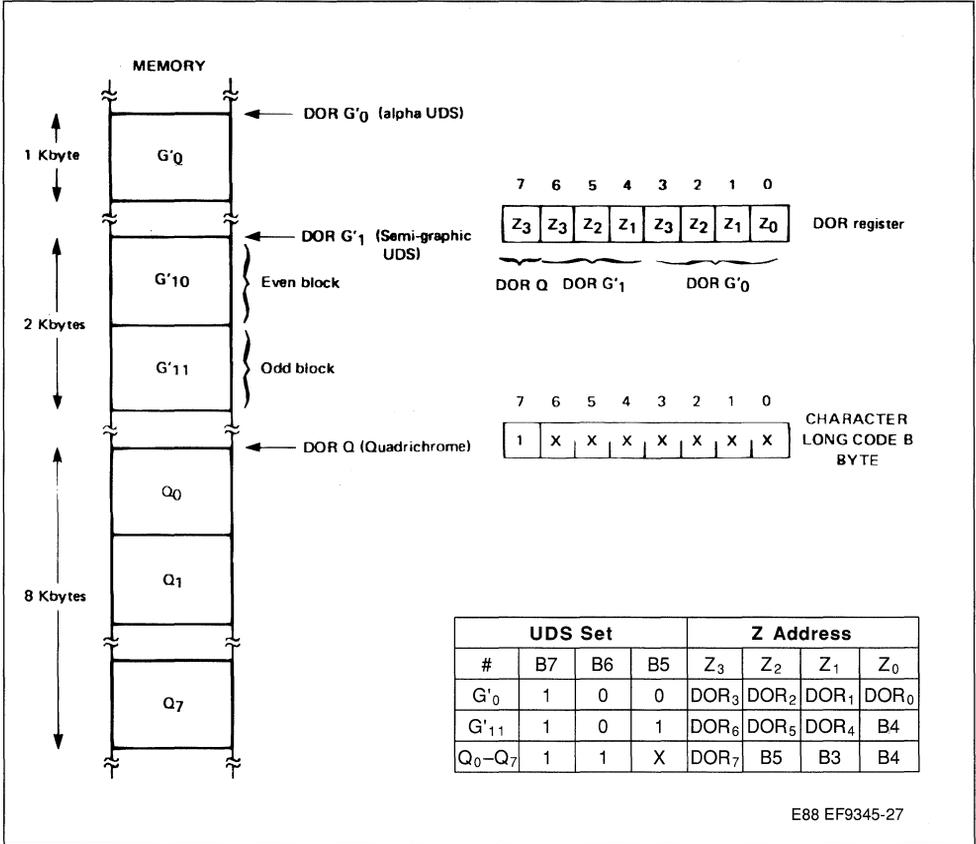


The cells of one given character set should be layed in one block.

Up to 100 character cells may be addressed in each set (or 200 for low resolution quadrichrome only). The location in memory, where to fetch the sets in use, are declared by DOR register (figure 14). For

each type of set, it gives the MSB(s) of the Z block address. EF9345 reads the Z LSB(s) in the B byte of the (equivalent) long code. As usual, the character code is read in the C byte. NT is derived from the TV line rank in the row and the double height status.

Figure 14 : UDS Fetch to Display.



LOADING USER DEFINED CHARACTER SET.

Before loading a character set into RAM, the user must :

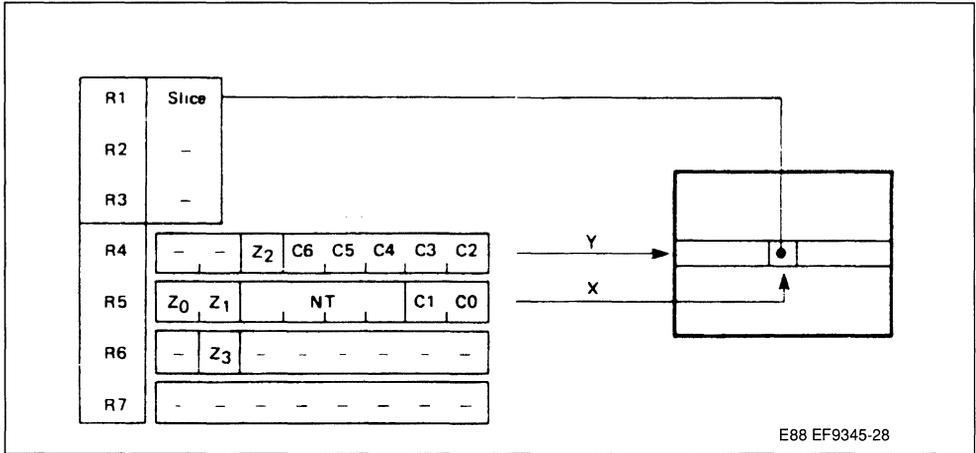
- Assign a name to the set :
  - G'0, G'10 or G'11 for bichrome characters.
  - From Q0 to Q7 for quadrichrome characters.
- Assign a character number to each character belonging to this set, character numbers range from 0 to 3 and 32 to 127.
  - It is binary coded into 7 bits C(0:6) – C(0:6) will be loaded later on into a C byte character

- code in order to display the character.
- A pointer to a character slice in memory is then manufactured from :
  - the character number C(0:6)
  - the slice number NT(0:3)
  - the block number assigned to the set Z(0:3).

Figure 15 shows how to proceed with the auxiliary pointer and the OCT command.

Note : The main pointer may be also used. When sequentially accessing slices of a given character, auto incrementation is helpless.

**Figure 15** : Accessing a Character Slice in Memory Using OCT Command with Auxiliary Pointer.



#### ON-CHIP CHARACTER GENERATOR.

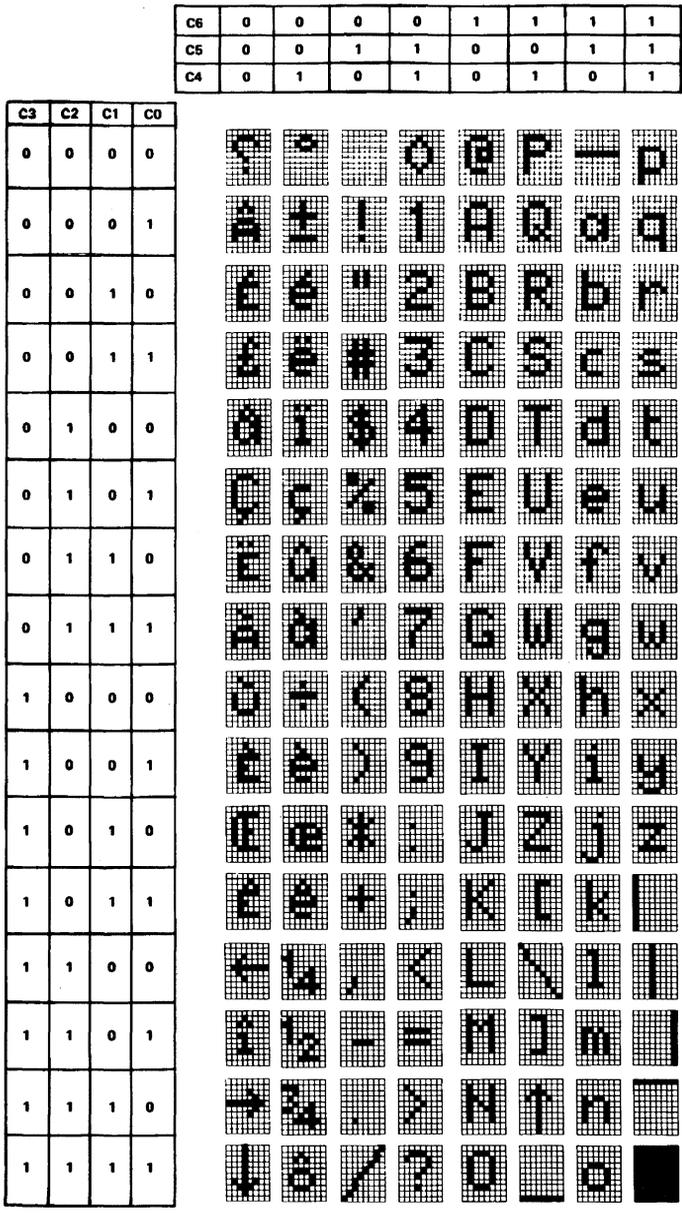
- G<sub>0</sub> set is common to 40 and 80 char./row modes (figure 16 and figure 25).
- G<sub>10</sub> is the standard mosaic set for videotex (figure 17).
- G<sub>11</sub>, G<sub>20</sub> and G<sub>21</sub> cannot be reached from the 16-bit short fixed codes (figure 18 and figure 19).

#### DISPLAYING THE ATTRIBUTES.

1. For normal operation, a double height and/or double width character must be repeated in memory in two successive Y and/or X positions. The user may otherwise freely mix any character size.
2. The attributes are logically processed in the following order :

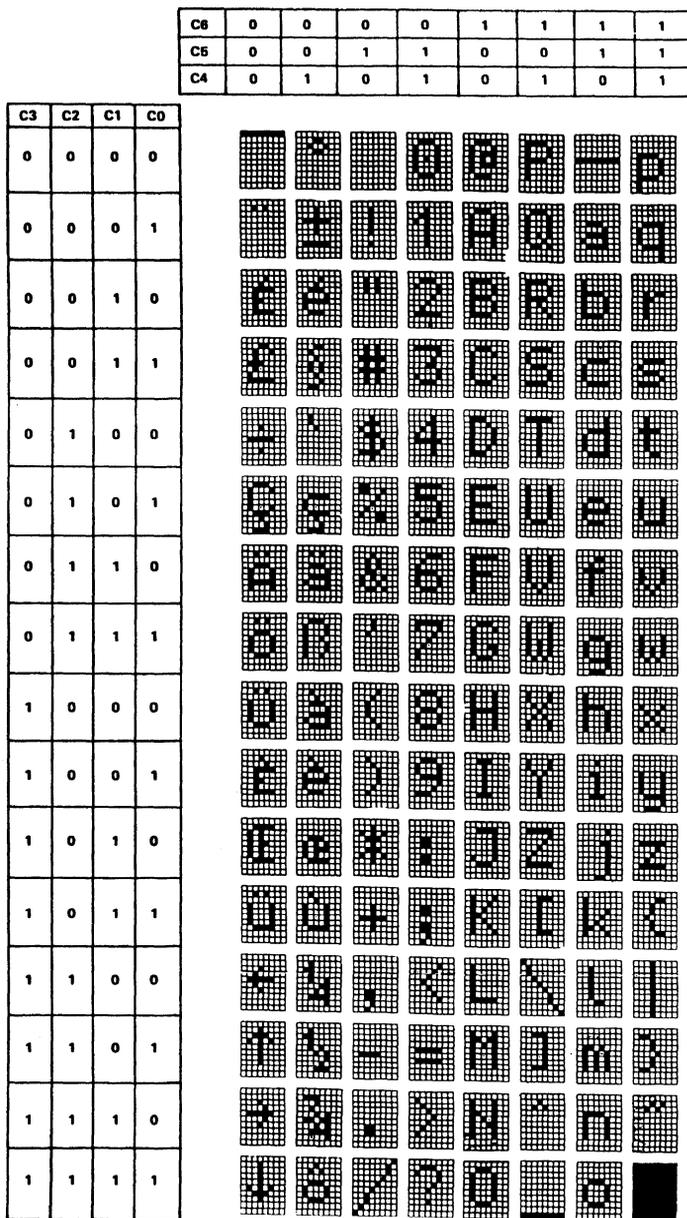
- Underline or underline cursor : foreground forced on the last slice (NT = 9).
  - Flash : background periodically forced on the whole window ( 0.5 Hz). The phase depends on the negative attribute.
  - Conceal : background forced permanently on the whole window. A concealed character neither blinks nor is underlined.
  - Negative : exchange the background and foreground color values when set.
  - Coloring.
  - Complemented cursor mode.
  - Insert : black color forced when required.
3. Basic pixel shift frequency :  $f_{CLK} \times 2/3 = 8 \text{ MHz}$ .

Figure 16 : G<sub>0</sub> Alphanumeric Character Set in 40 Character/Row Mode – EF9345.



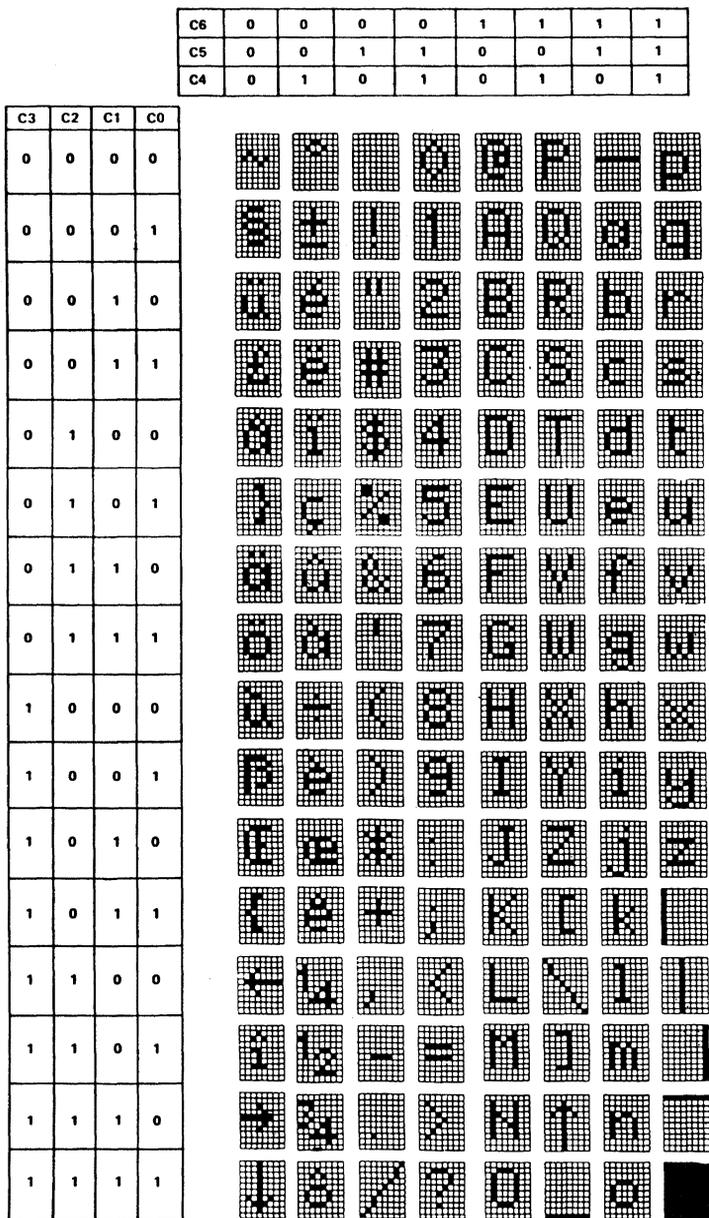
E88 EF9345-29

Figure 16 bis : G<sub>0</sub> Alphanumeric Character Set in 40 Character/Row Mode – EF9345 R003.



E88 EF9345-30

Figure 16 ter : G<sub>0</sub> Alphanumeric Character Set in 40 Character/Row Mode – EF9345 R005.



E88 EF9345-31

Figure 17 : G<sub>10</sub> Semigraphic Character Set.

				MOSAIC Semi-graphic				SEPARATED Semi-graphic			
C6	1	1	1	1	0	0	0	0	0	0	0
C5	0	0	1	1	0	0	1	1	0	1	1
C4	0	1	0	1	0	1	0	1	0	1	1

C3	C2	C1	C0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

E88 EF9345-32

Figure 18 : G11 Stroke Set.

				C5	0	0
				C4	0	1
C3	C2	C1	C0			
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

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Figure 19 ter : G<sub>20</sub> and G<sub>21</sub> Accentuated Character Sets for 9345 – R005.

	C6	0	0	1	1
	C5	0	1	0	1
B5					
0					
1					

Example :

	7	6	5	4	3	2	1	0
Byte C	X	0	1	0	0	0	0	1
Byte B	0	1	0	0	X	X	X	X
Byte A	X	X	X	X	X	X	X	X

X = bits defined by user.



	C4	0	1		
C3	C2	C1	C0		
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

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**80 CHAR/ROW CHARACTER CODES**

To display pages in 80 character per row format, one of two character code formats must be selected :

- Long (12 bits) code : 4 parallel attributes and large on-chip 1024 semigraphic character set,
- Short (8 bits) code : no attribute, no semigraphic set.

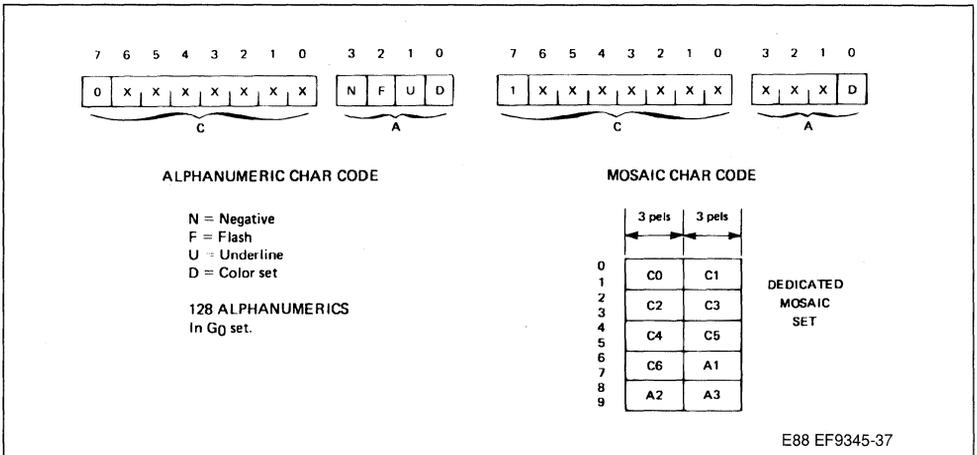
Both formats address the on-chip G<sub>0</sub> set (128 characters 6 x 10). None allows UDS addressing.

**LONG CODES.**

Each 6 pixels x 10 lines character window on the screen is associated with a 12-bit code in memory, namely a C byte and an attribute nibble A (figure 10). C7 bit designates the set.

- Alphanumeric set : C7 = 0.  
C(0:6) designates one out of 128 alphanumeric characters in the G<sub>0</sub> on-chip set. This set is common to the 40 char/row format, with the 2 right most columns truncated (see figure 25). A(0:3) gives 4 parallel attributes.
- Mosaic set : C7 = 1.  
A(1:3) and C(0:6) address a dedicated mosaic character. Each of these address bits controls the foreground/background status of a 3 pixels x 2 lines sub-window : foreground when the bit is set. A0 provides a color select attribute.

**Figure 20 : 80 Char/Row Character Code.**



**SHORT CODES.**

They are derived from the long code by giving a 0 implicit value to each bit of the A nibble : positive, not underlined, not flashing.

**PACKING THE CODES IN MEMORY.**

Long codes are paired. A pair is packed in a 3-byte word. Therefore, the 80 codes of a row fill a 120-byte row buffer (figure 21). The left most position on the screen is even. Its corresponding C byte is at the beginning of the first buffer. The next position on the screen is odd. Its corresponding C byte is at the beginning of the second buffer. Both nibbles are packed in the third buffer. With short codes, the same scheme yields 80-byte row buffers.

**ACCESS TO THE CODES IN MEMORY.**

KRL command transfers 12 bits from/to the R1 and R3 registers to/from memory. The read modify write operation, necessary to write the A nibble in memory, is automatically performed provided that the A nibble is repeated in the R3 register (figure 22). Dedicated auto-incrementation is also performed when required.

KRC command does a similar job for the short codes (figure 23).

A very simple scheme allows the microprocessor to transcode an horizontal screen location into a pointer (figure 24). The joint use of this scheme with the dedicated command alleviates all the packing/unpacking troubles.

Figure 21 : 80 Char/Row Code Packing.

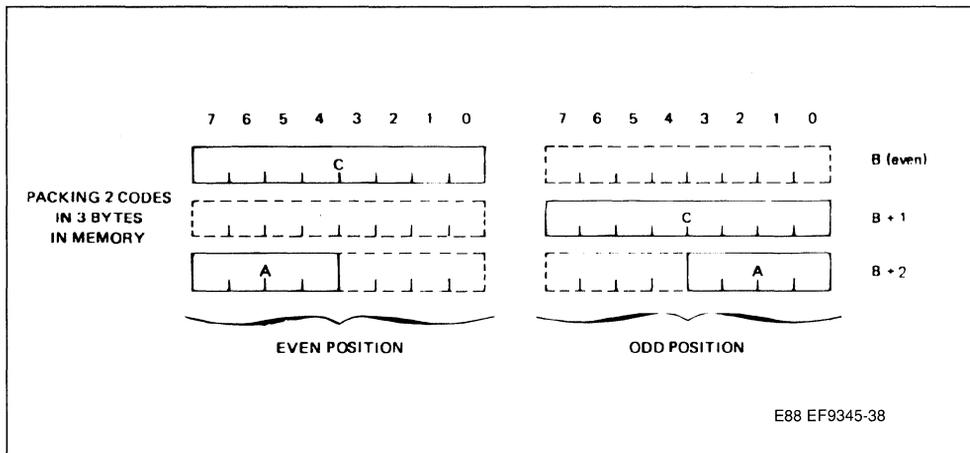


Figure 22 : KRL Command : Sequential Access to Long Codes.

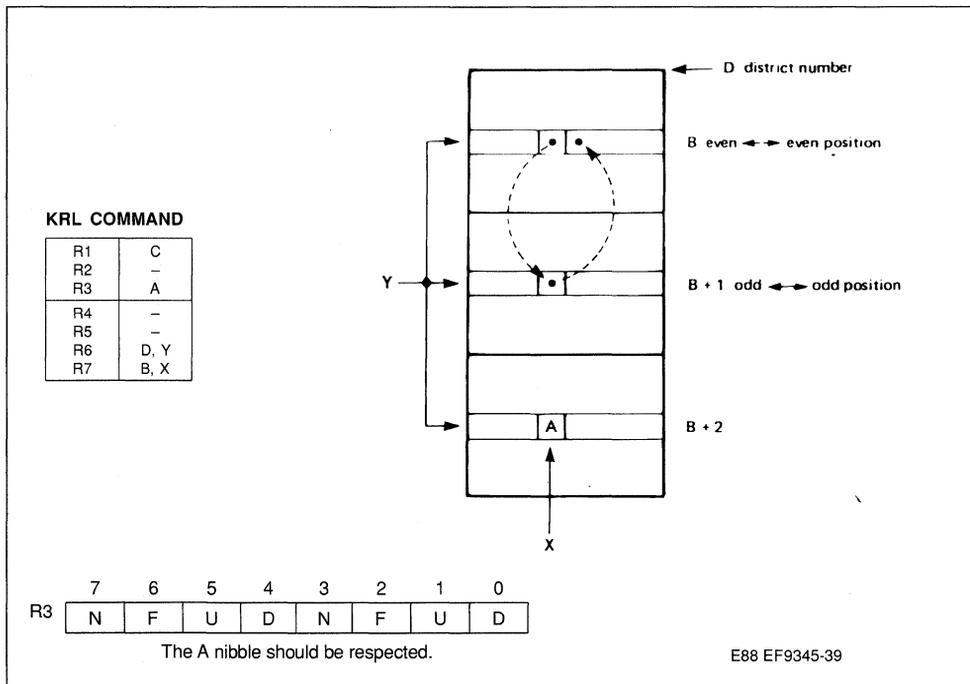


Figure 23 : KRC Command : Sequential Access to Short Codes.

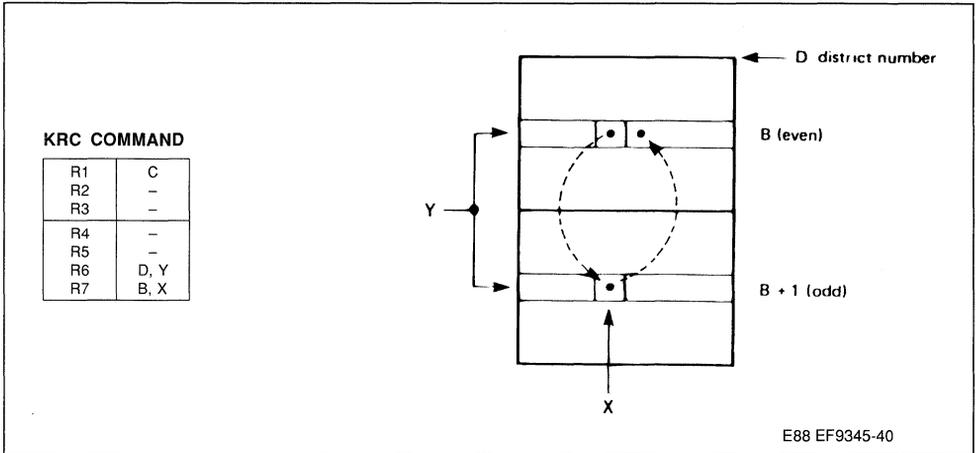
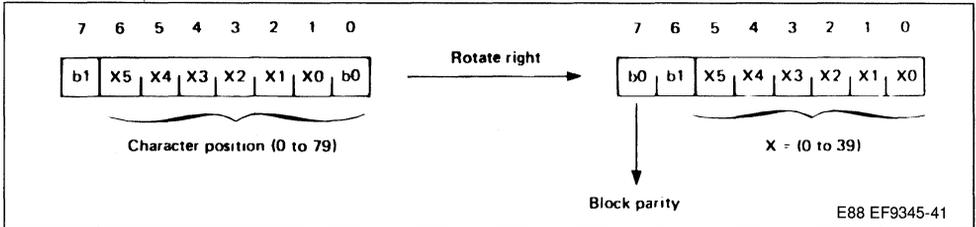


Figure 24 : Transcoding an Horizontal Screen Location into a R7 Pointer.



**DISPLAYING THE ATTRIBUTES - DOR REGISTER.**

Short code and mosaic characters are not flashing, not underlined and "positive".

The attributes are processed in the following order :

- Underline or underlined cursor : foreground is forced on the last slice (NT = 9).
- Flash : background is periodically (0.5 Hz - 50 %) forced on all the window. The phase depends on the negative attribute.

- Color select : a "positive" character is displayed with a background color same as the margin color. The foreground color is selected in DOR register by the D attribute.
- Negative : when the character is negative, background and foreground colors are exchanged. In complemented CURSOR position, these colors are complemented.
- Insert : the D attribute selects one insert value in DOR register. This attribute is then processed up to the current insertion mode (see screen format and attribute insert section).

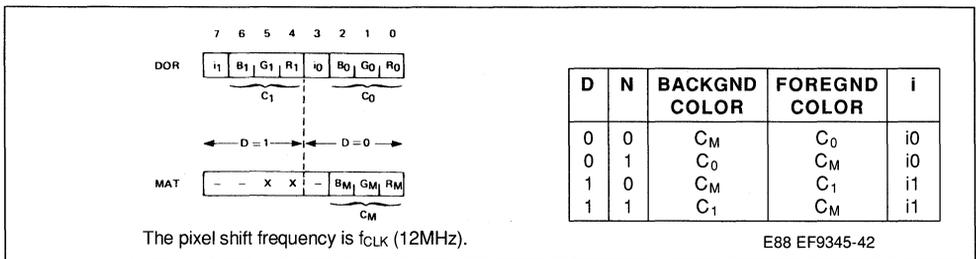
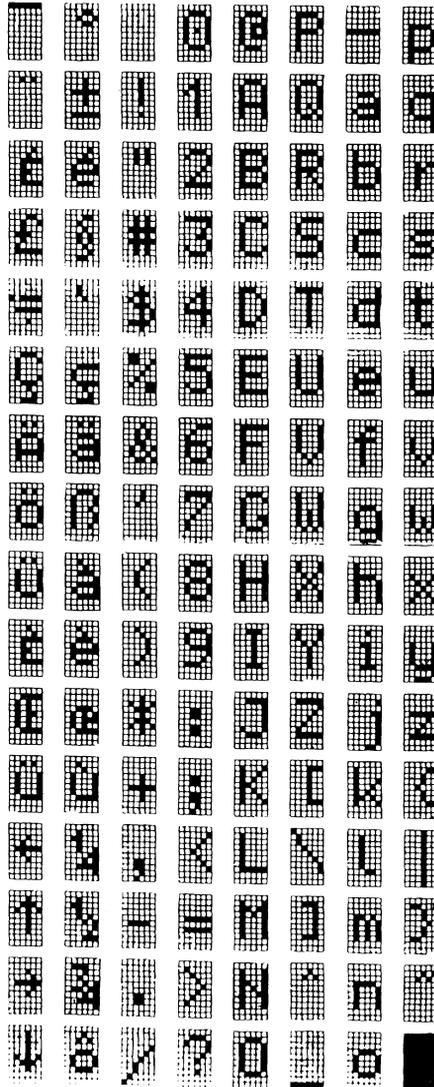




Figure 25 bis : G<sub>0</sub> Alphanumeric Character Set in 40 Character/Row Mode – EF9345 R003.

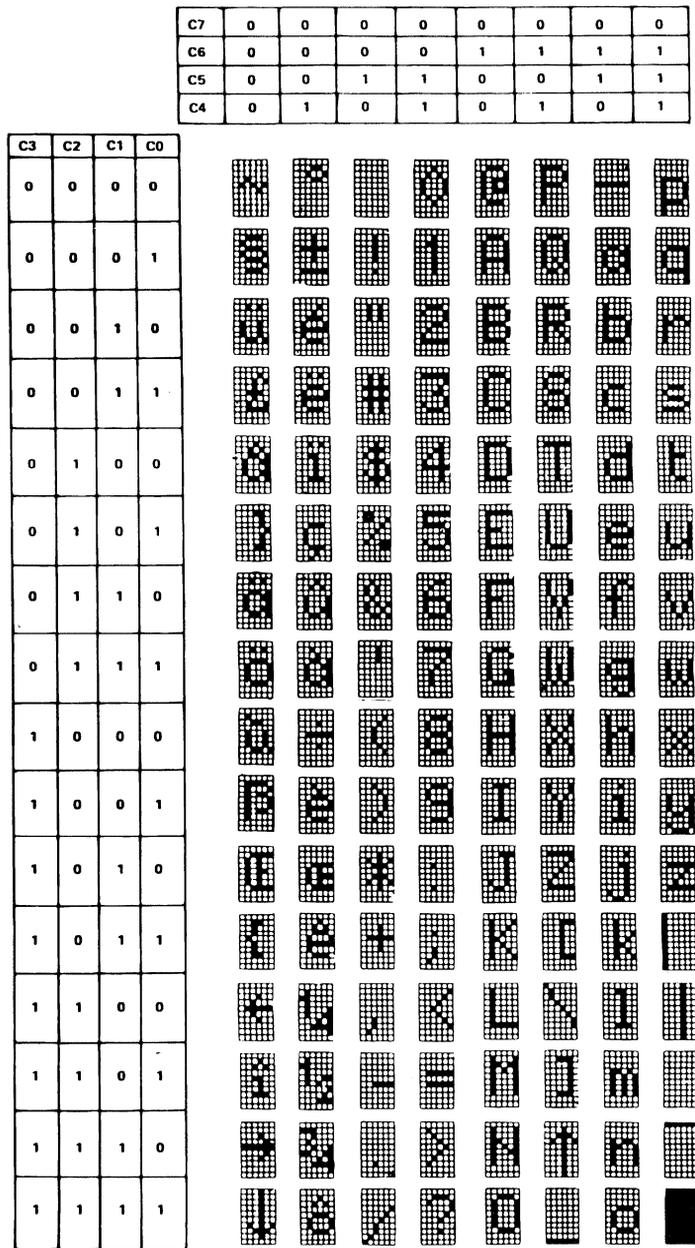
C7	0	0	0	0	0	0	0	0
C6	0	0	0	0	1	1	1	1
C5	0	0	1	1	0	0	1	1
C4	0	1	0	1	0	1	0	1

C3	C2	C1	C0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



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Figure 25 ter : G<sub>0</sub> Alphanumeric Character Set in 40 Character/Row Mode – EF9345 R005.



E88 EF9345-45

**MICROPROCESSOR ACCESS COMMANDS**

A microprocessor bus cycle may transfer one byte from/to the microprocessor to/from a directly addressable register. These registers provide an indirect access :

- to/from 5 on-chip indirect registers : ROR, DOR, MAT, PAT and TGS.
- to/from the private memory.

Due to address/data multiplexing, a bus cycle is a 2 phase process (see Timing diagram 1 or Timing diagram 2).

**ADDRESS PHASE.**

The falling edge of AS latches to AD(0:7) bus state and CS signal into the temporary A address register (figure 26).

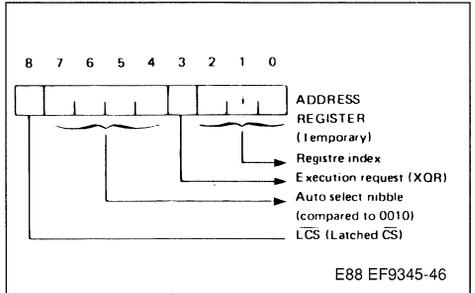
- $A(0:2) = i$   
This register index designates one out of 8 direct access registers  $R_i$ .
- $A3 = XQR$   
This is the execution request bit.
- $A(4:7) = ASN$   
This is the Auto-Selection Nibble.

- $A8 = \overline{LCS}$

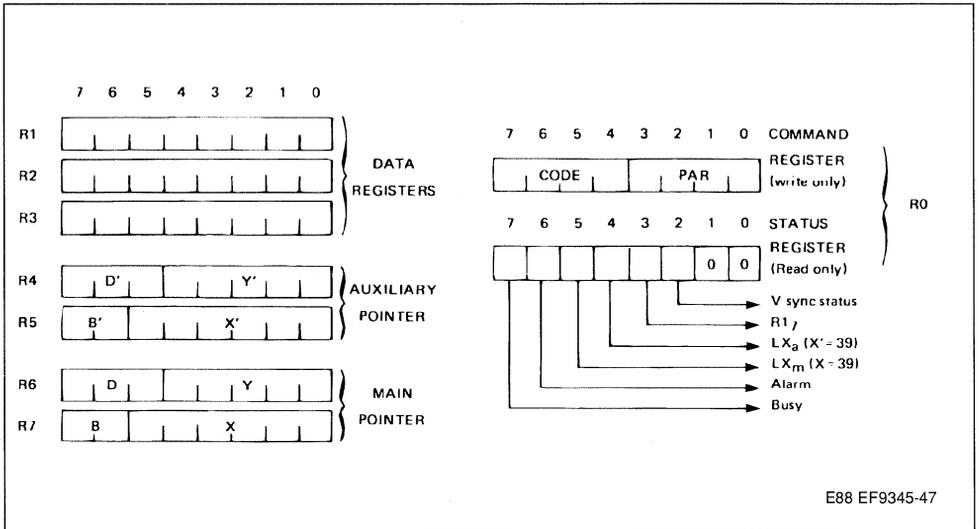
This is the latched value of  $\overline{CS}$  input pin.

EF9345 is selected when the following condition is met :  $ASN = 2$  (Hexa) and  $LCS = 0$ .

Therefore, EF9345 is mapped in the hexadecimal microprocessor addressing space from XX20 to XX2F, where XX is up to the user. When EF9345 is not selected, its AD bus pins float and no register can be modified.



**Figure 26 : Direct Access Registers.**



**DATA PHASE - REGISTERS.**

When EF9345 is selected and while AS input is low, the R<sub>i</sub> register is accessed.

R0 designates a write-only COMMAND register or a read-only STATUS register.

R1 to R7 hold the arguments of a command. They are read/write registers.

R1, R2, R3 are used to transfer the data.

R4, R5 hold the Auxiliary Pointer (AP).

R6, R7 hold the Main Pointer (MP).

(see memory organization ; pointer section for pointer structure).

**COMMAND REGISTER.**

This register holds a 4-bit command type and 4 bits of orthogonal parameters (see command table).

**Type**

There are 4 groups of command :

- The IND command which gives access to on-chip resources,
- The fixed format character code transfer commands,
- The variable character code handling commands,
- The general purpose commands.

**Parameters.**

R/W : Direction  
 1 : to DATA registers (R1, R2, R3)  
 0 : from DATA registers.

r : Internal resource index (see figure 27).

l : Auto-incrementation  
 1 : with post auto-incrementation

- 0 : without auto-incrementation.
- p : Pointer select  
 1 : auxiliary pointer  
 0 : main pointer
- s, s̄ : Source, destination select  
 01 : source : MP ; destination : AP  
 10 : source : AP ; destination : MP
- a, a : Stop condition  
 01 : stop at end of buffer  
 10 : no stop.

**STATUS REGISTER**

This is a read-only, direct access register.

S7 : BUSY BUSY is set at the beginning of any command execution. It is reset at completion.

S6 : AL } LX<sub>m</sub> or LX<sub>a</sub> is set when respectively  
 S5 : LX<sub>m</sub> } the main pointer or the auxiliary pointer  
 S4 : LX<sub>a</sub> } holds X = 39 before a possible incrementation.  
 The alarm bit S6 is set when LX<sub>m</sub> or LX<sub>a</sub> is set and an incrementation is performed after access.

S3 : Gives the MSB value of R1.

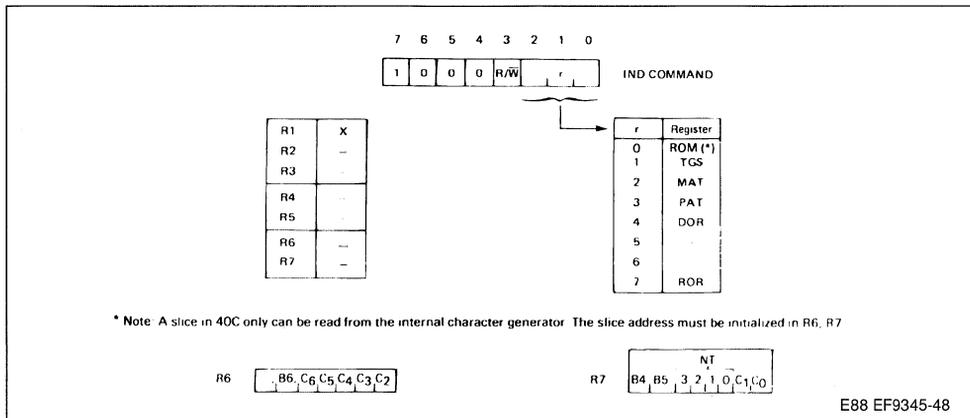
S2 : Gives the vertical synchronization signal state.  
 This is maskable by the VRM command.

S1 = S0 = 0 Not used.

S3 to S6 are reset at the beginning of any command.

The COMMAND TABLE shows every command able to set, each of these status bits, after completion.

**Figure 27 : Indirect On-chip Resource Access.**



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## NOTES ON COMMAND EXECUTION.

1. The execution of any command starts at the trailing edge of DS when (and only when) :
  - EF9345 has been selected,
  - XQR has been set,
 at the previous AS falling edge.

This scheme allows loading a command and its argument in any order. For instance, a command, once loaded, may be re-executed with new or partly new arguments.

2. At power on, the busy state is undetermined. It is recommended to load first a dummy command with XQR = 1 before any effective command.
3. While Busy is set, the current command is under execution. Register access is then restricted.

**Register access with XQR = 0**

- Read STATUS is effective.
- Write COMMAND or any other register access are ineffective.

That is to say, the microprocessor reads undetermined values and may not modify a register.

**Register access with XQR = 1**

- Read STATUS or write COMMAND are effective,
- Access to other registers is ineffective.

However, the previous command is aborted and the new command execution launched (with an initial state undetermined for registers and memory locations handled by the aborted command).

4. Execution suspension.

The execution of any command (except VRM, VSM) is suspended during the last and first TV line of an active row. This is because the memory bus cannot be allocated for microprocessor access during this 104  $\mu$ s period.

This holds too for internal resource access because on-chip data transfer uses internal data memory bus.

IND COMMAND (see figure 27).

This command transfers one byte between R1 and an internal resource. The r parameter designates one on-chip indirect register.

FIXED FORMAT CHARACTER CODE ACCESS :  
KRF, KRG, KRL KRC

Each of these commands is dedicated to transfer one complete character code between DATA registers and memory. MP is exclusively used.

KRF transfers 24 bits.

KRG transfers 16 bits.

KRL transfers 12 bits.

KRE transfers 8 bits.

Code packing, pointer and data structures are explained in the corresponding character code section.

When auto-incrementation is enabled, MP is automatically updated after access so as to point to the next location. This location corresponds to the next right position on screen. When last position ( $X = 39$ ) is accessed,  $LX_m$  is set. When last position is accessed with auto-incrementation, alarm is also set. MP is then pointing back at the beginning of the row : there is no automatic Y incrementation.

VARIABLE CODE HANDLING COMMANDS :  
KRV EXP, CMP, KRE

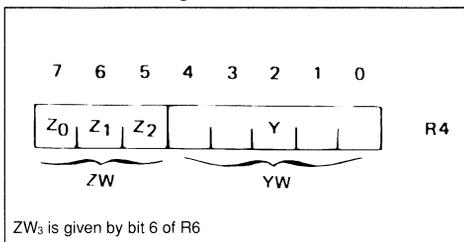
An overview on these commands is given in "handling the variable codes" (40 char./row section).

KRV uses R5 to point the attribute file.  $LX_a$  is set when this file is full (the last attribute pair has been accessed).

EXP and CMP use MP and R5 in the same way as KRV. Furthermore, R4 points to a working double buffer. These two commands process a whole row buffer and stop either at the end of the row buffer or when the file overflows. In the last case, the alarm bit is set.

KRE uses MP to point to a buffer and R4 to point to a working double buffer. R5 is unused. In other respects, KRE is identical to KRL.

For these commands, R4(5:7) hold the LSB's block dress of the working buffer W.



**GENERAL PURPOSE ACCESS TO A BYTE-OCT.**

This command uses either MP or AP pointer.

When MP is in use, an overflow yields to a Y incrementation.

**MOVE BUFFER COMMANDS : MVB, MVD, MVT.**

These are memory to memory commands which use R1 as working register.

MVB transfers a byte from source to destination, post-increments the 2 pointers and iterates until the stop condition is met. MVD and MVT are similar but work respectively with 2 byte word and 3 byte word. That is to say, MVB works on buffers, MVD on double buffers and MVT on triple buffers. If the parameter a = 1, the process stops when either source or destination buffer end is reached. If the parameter a = 0, the process never stops until aborted. In this case, main pointer overflow yields to a Y incrementation in MP. So, a whole block or page may be initialized.

**MISCELLANEOUS COMMANDS : INY, VRM and VSM.**

INY command increments Y in MP.

VRM and VSM respectively reset and set a vertical synchronization status mask. When the mask is set, status bit S2 remains at 0. When the mask is reset, status S2 follows the vertical sync. state : it is reset for 2 TV lines per frame and stays at 1 during the remaining period. It becomes readable by the microprocessor from the status register. After power on, the mask state is undetermined.

## COMMAND TABLE

Type	Memo	Code				Parameter				Status				Arguments							Execution Time (1)	
		7	6	5	4	3	2	1	0	AI	LX <sub>m</sub>	LX <sub>a</sub>	R17	R1	R2	R3	R4	R5	R6	R7	Write	Read
Indirect	IND	1	0	0	0	R $\overline{W}$	r			0	0	0	0	D	-	-	-	-	MP	2	3.5	
40 Characters - 24 Bits	KRF	0	0	0	0	R $\overline{W}$	0	0	l	X	X	0	0	C	B	A	-	-	MP	4	7.5	
40 Characters - 16 Bits	KRG	0	0	0	0	R $\overline{W}$	0	1	l	X	X	0	0	A*	B*	W	-	-	MP	5.5	7.5	
80 Characters - 8 Bits	KRC	0	1	0	0	R $\overline{W}$	0	0	l	X	X	0	0	C	-	-	-	-	MP	9	9.5	
80 Characters - 12 Bits	KRL	0	1	0	1	R $\overline{W}$	0	0	l	X	X	0	0	C	-	A	-	-	MP	12.5	11.5	
40 Characters Variable	KRV	0	0	1	0	R $\overline{W}$	0	0	l	X	X	X	X	C	B	A	-	XF	MP	(2) 3 + 3 + j	3.5 + 6 * j	
Expansion	EXP	0	1	1	0	0	0	0	0	X	0	X	0	C	B	A	PW	XF	MP	(3) < 247	-	
Compression	CMP	0	1	1	1	0	0	0	0	X	0	X	0	C	B	A	PW	XF	MP	(3) < 402	-	
Expanded Characters	KRE	0	0	0	1	R $\overline{W}$	0	0	l	X	X	0	0	C	B	A	PW	-	MP	4	7.5	
Byte	OCT	0	0	1	1	R $\overline{W}$	p	0	l	X	X	X	0	D	-	-	AP	MP	4	4.5		
Move Buffer	MVB	1	1	0	1	s	$\overline{s}$	$\overline{a}$	a	0	0	0	0	W	-	-	AP	MP	(2) 2 + 4. n	-		
Move Double Buffer	MVD	1	1	1	0	s	$\overline{s}$	$\overline{a}$	a	0	0	0	0	W	-	-	AP	MP	(2) 2 + 8. n	-		
Move Triple Buffer	MVT	1	1	1	1	s	$\overline{s}$	$\overline{a}$	a	0	0	0	0	W	-	-	AP	MP	(2) 2 + 12. n	-		
Clear Page (4) - 24 Bits	CLF	0	0	0	0	0	1	0	1	X	X	0	0	C	B	A	-	-	MP	< 4700 (1 K code)	-	
Clear Page (4) - 16 Bits	CLG	0	0	0	0	0	1	1	1	X	X	0	0	A*	B*	W	-	-	MP	< 5800 (1 K code)	-	
Vertical Sync Mask Set	VSM	1	0	0	1	1	0	0	1	0	0	0	0	-	-	-	-	-	-	1	-	
Vertical Sync Mask Reset	VRM	1	0	0	1	0	1	0	1	-	-	-	-	-	-	-	-	-	-	1	-	
Increment Y	INY	1	0	1	1	0	0	0	0	0	0	0	0	-	-	-	-	-	Y	-	2	-
No Operation	NOP	1	0	0	1	0	0	0	1	-	-	-	-	-	-	-	-	-	-	1	-	

P : Pointer select  
 1 : auxiliary pointer  
 0 : main pointer.

s,  $\overline{s}$  : Source, destination  
 01 : source = MP ; destination = AP  
 10 : source = AP ; destination = MP

$\overline{a}$ , a : Stop condition  
 01 : stop at end of buffer  
 10 : no stop

r : Indirect register number

- : Not affected  
 W : Used as working register  
 PW (Z, YW) : Working buffer  
 X : Set or Reset  
 XF : X File  
 l : Pointer incrementation  
 D : Data  
 MP : Main pointer  
 AP : Auxiliary pointer

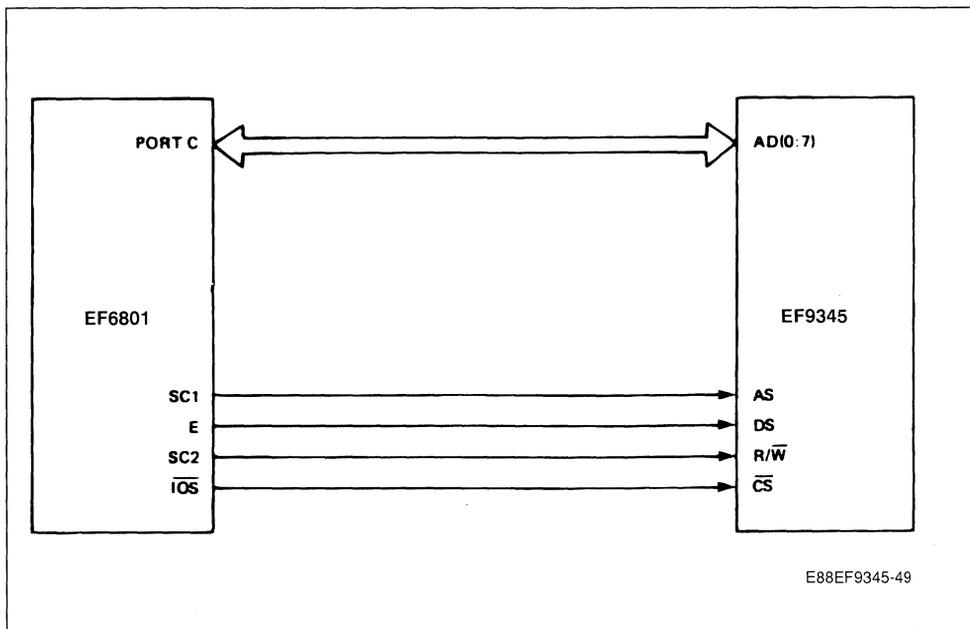
(1) Unit : 12 clock periods ( $\approx 1 \mu\text{s}$ ) without possible suspension.

(2) n : total number of words  $\leq 40$  ; j = 1 for long codes, j = 0 for short codes.

(3) : Worst case (20 long codes + 20 short codes).

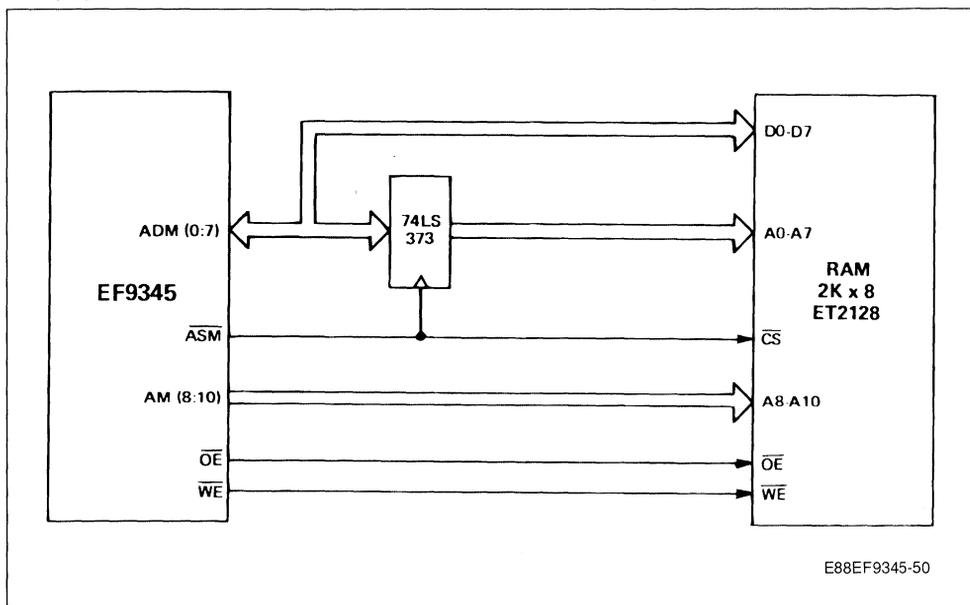
(4) : These commands repeat KRF or KRG with Y incrementation when X overflows. When the last position is reached in a row. Y is incremented and the process starts again on the next row

INTERFACE WITH EF6801



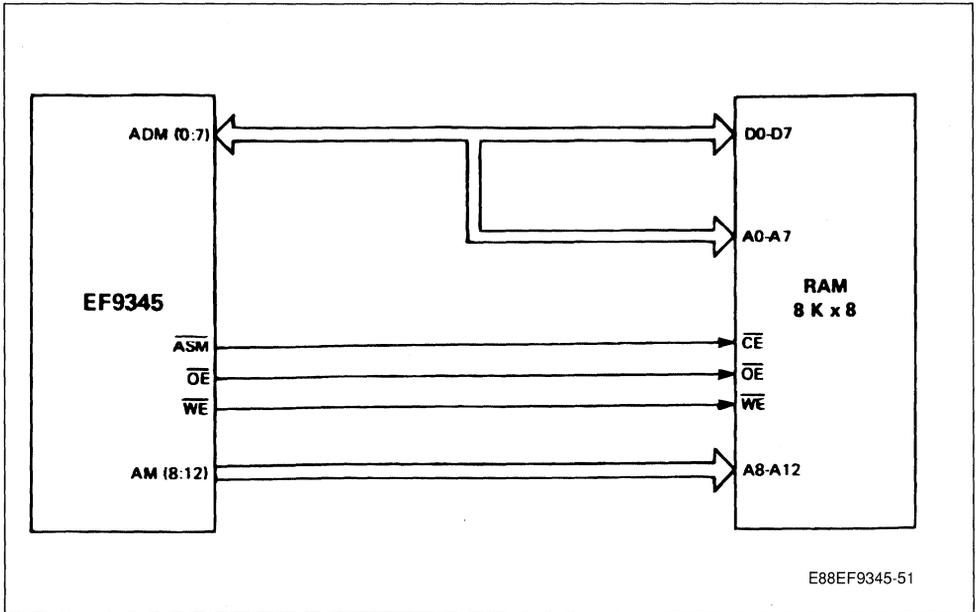
MINIMUM APPLICATION WITH 2K X 8 MEMORY

One page memory terminal in 16-bit fixed format or 24-bit compressed format.



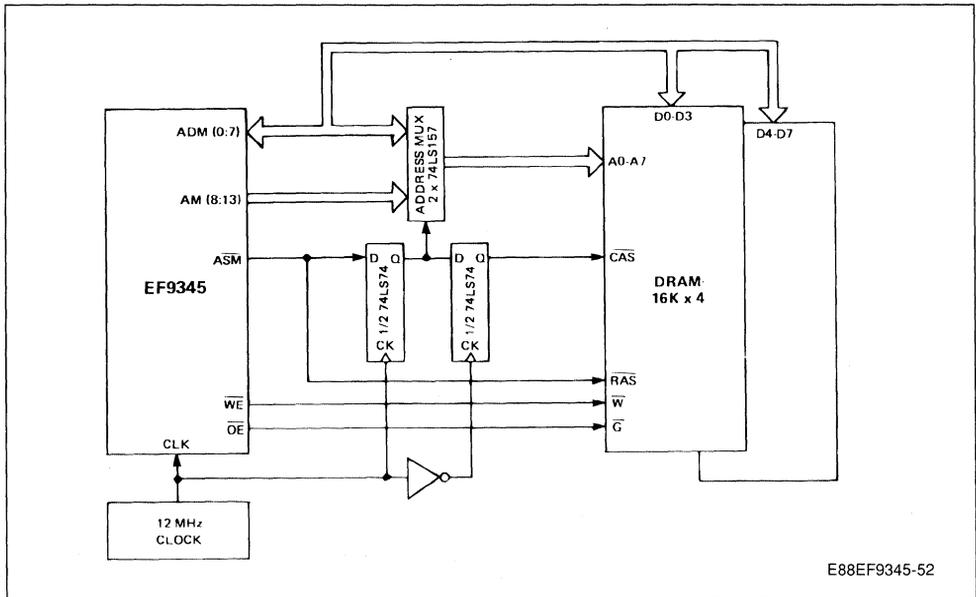
**TYPICAL APPLICATION WITH 8 K X 8 DYNAMIC OR PSEUDO-STATIC RAM**

Multipage terminal with possibility of multiple user definable character sets.



**MAXIMUM APPLICATION WITH 16 K X 8 MEMORY**

Multipage terminal with user definable character sets and buffer areas.

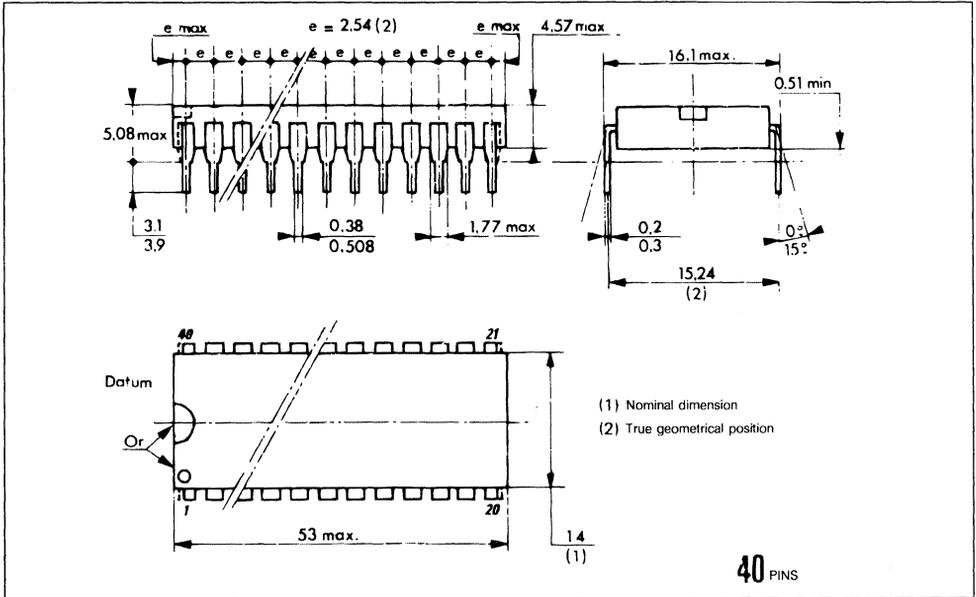


## ORDERING INFORMATION

Part Number	Package	Character Generator
EF9345PRYYY	DIP40	RYYY
EF9345FNRYYY	PLCC44	RYYY

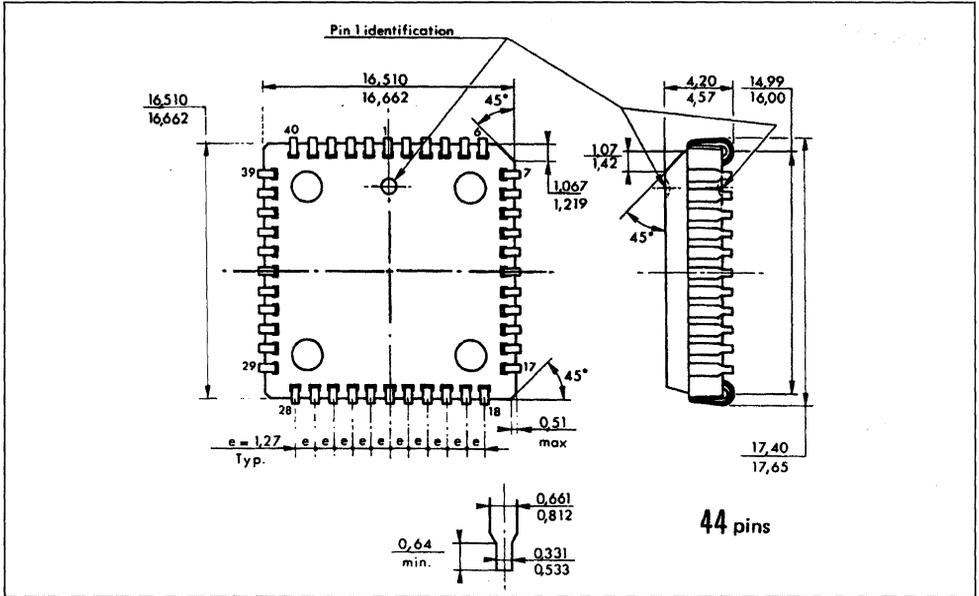
## PACKAGE MECHANICAL DATA

40 PINS – PLASTIC DIP



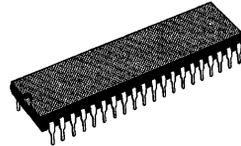
PACKAGE MECHANICAL DATA (continued)

44 PINS – PLASTIC CHIP CARRIER

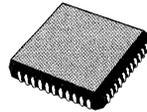


**SINGLE CHIP SEMI-GRAPHIC DISPLAY PROCESSOR**

- SINGLE CHIP LOW-COST CRT CONTROLLER
- UP TO 60 Hz SCREEN REFRESH RATE
- 32 KBYTE DEDICATED MEMORY ADDRESSING SPACE
- 2 SCREEN FORMATS :
  - 25 ROWS OF 40 CHARACTERS
  - 25 ROWS OF 80 CHARACTERS
- ON-CHIP 154 ALPHANUMERIC AND 128 SEMI-GRAPHIC CHARACTER GENERATOR
- EASY EXTENSION OF USER DEFINED ALPHANUMERIC OR SEMI-GRAPHIC SETS (>1K characters)
- 40 CHARACTERS/ROW ATTRIBUTES : FOREGROUND AND BACKGROUND COLOR, DOUBLE HEIGHT, DOUBLE WIDTH, BLINKING, CONCEAL, INSERT
- 80 CHARACTERS/ROW ATTRIBUTES : UNDERLINING, BLINKING, REVERSE, COLOR SELECT
- PROGRAMMABLE ROLL-UP, ROLL-DOWN, UPPER OR LOWER SERVICE ROW
- ON-CHIP R, G, B SHIFT REGISTERS
- ANALOG COMPOSITE LUMINANCE SIGNAL OUTPUT
- VERSATILE I/O CONFIGURATION : VIDEO AND SYNC OR GENERAL PURPOSE I/O PORTS
- ADDRESS/DATA MULTIPLEXED BUS DIRECTLY COMPATIBLE WITH STANDARD MICROCOMPUTERS SUCH AS 6801, 6301, 8048, 8051



**P  
DIP40**  
(Plastic package)

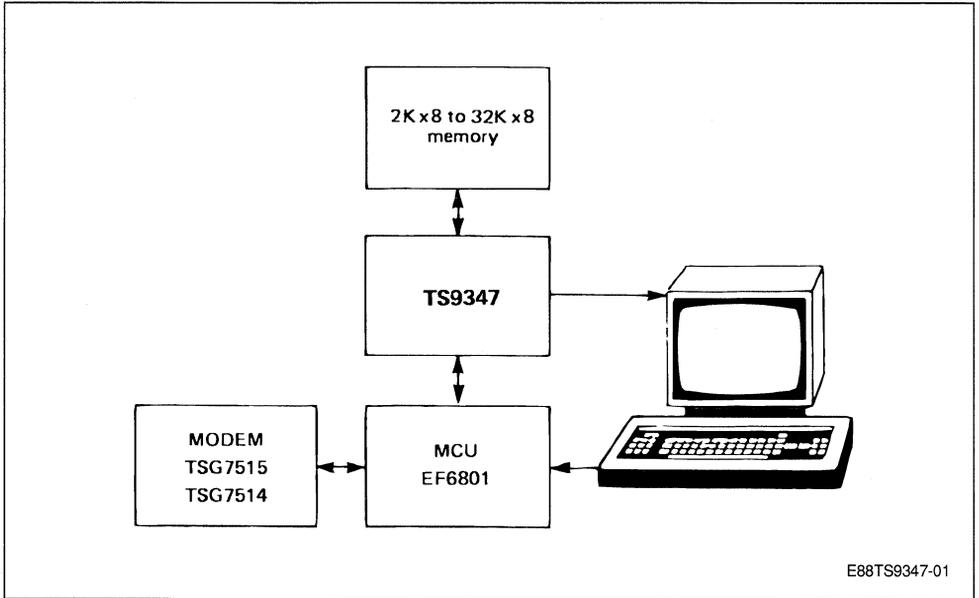


**FN  
PLCC44**  
(Plastic Chip Carrier)

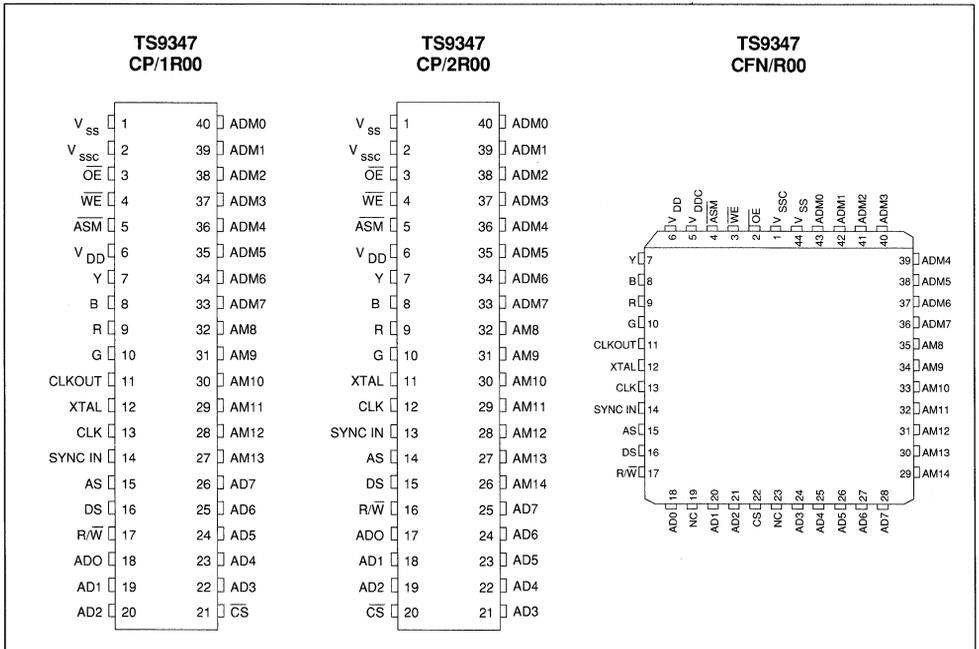
**DESCRIPTION**

A complete display control unit may be implemented with TS9347 and a single standard memory package. This new advanced CRT controller drastically reduces IC cost and PCB area for low-end color or monochrome terminal.

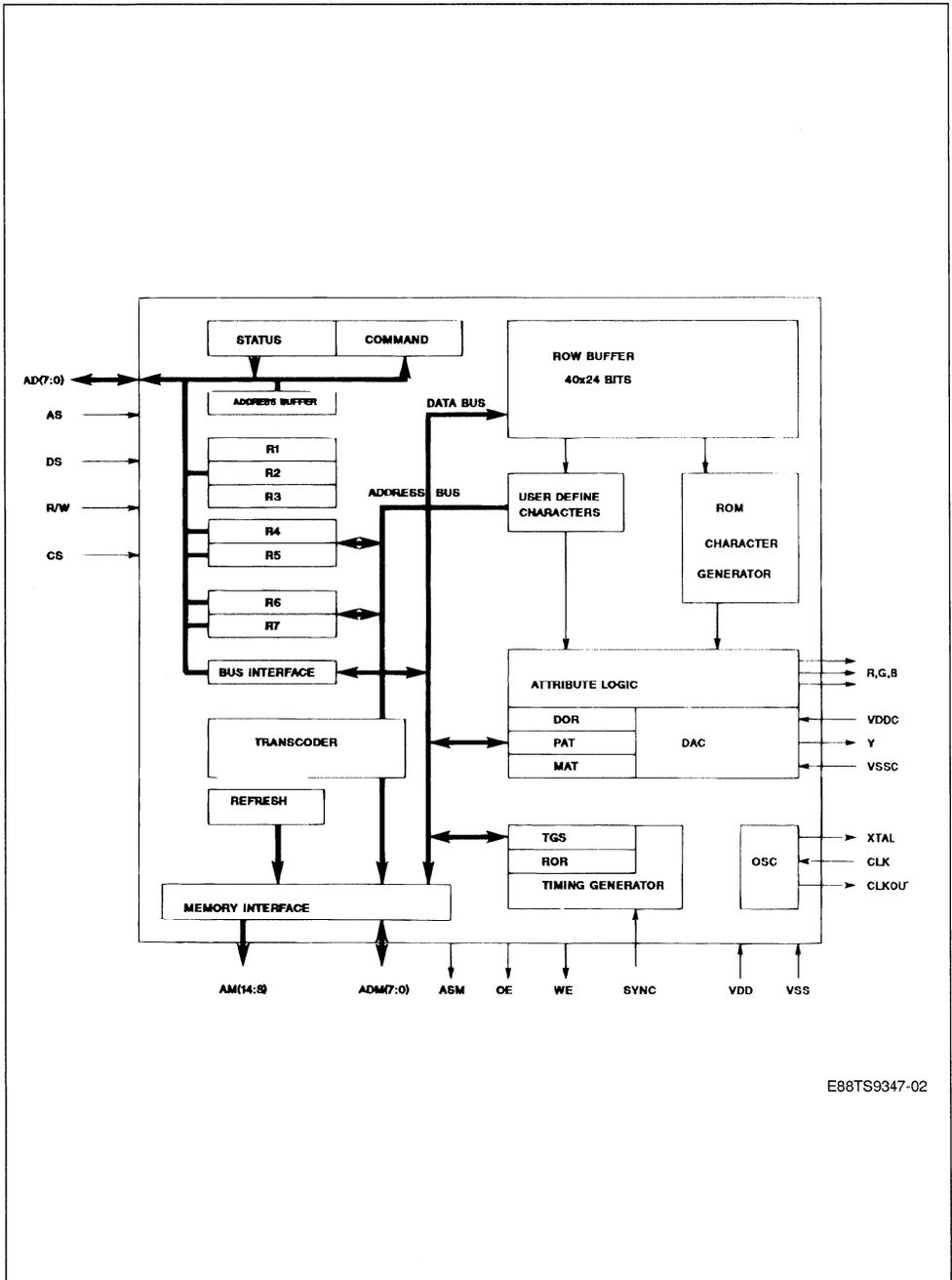
TYPICAL APPLICATION



PIN CONNECTIONS



BLOCK DIAGRAM



E88TS9347-02

**PIN DESCRIPTION**

All the input/output pins, XTAL and Y excepted, are TTL compatible.

**MICROPROCESSOR INTERFACE**

Name	Pin Type	Function	Description
AD (0:7)	I/O	Multiplexed Address/Data Bus	These 8 bidirectional pins provide communication with the microprocessor system bus.
AS	I	Address Strobe	The falling edge of this control signal latches the address on the AD (0:7) lines, the state of the Data Strobe (DS) and Chip Select (CS) into the chip.
DS	I	Data Strobe	When this input is strobed high by AS, the output buffers are selected while DS is low for a read cycle (R/W = 1). In write cycle, data present on AD (0:7) lines are strobed by R/W low (see timing diagram 2). When this input is strobed low by AS, R/W gives the direction of data transfer on AD (0:7) bus. DS high strobes the data to be written during a write cycle (R/W = 0) or enables the output buffers during a read cycle (R/W = 1). (see timing diagram 1).
R/W	I	Read/Write	This input determines whether the internal registers get written or read. A write is active low ("0").
CS	I	Chip Select	The TS9347 is selected when this input is strobed low by AS.

**MEMORY INTERFACE**

Name	Pin Type	Function	Description
ADM (0:7)	I/O	Multiplexed Address/Data Bus	Lower 8 bits of memory address appear on the bus when ASM is high. It then becomes the data bus when ASM is low.
AM (8:14)	O	Memory Address Bus	These 7 pins provide the high order bits of the memory address.
$\overline{OE}$	O	Output Enable	When low, this output selects the memory data output buffers.
$\overline{WE}$	O	Write Enable	This output determines whether the memory gets read or written. A write is active low ("0").
$\overline{ASM}$	O	Memory Address Strobe	This signal cycles continuously. Address can be latched on its falling edge.

## VIDEO INTERFACE

Name	Pin Type	Function	Description
R	O	Red/Composite Sync	<ul style="list-style-type: none"> <li>* When <math>TGS_5 = 0</math>, this output delivers the Red component of the video signal. It is low during the H and V blanking intervals.</li> <li>* When <math>TGS_5 = 1</math>, this output delivers the composite synchronization signal.</li> </ul>
G	O	Green/Insert/Port 1	<ul style="list-style-type: none"> <li>* When <math>TGS_4 = TGS_5 = 0</math>, this output delivers the green component of the video signal. It is low during the V and H blanking intervals.</li> <li>* When <math>TGS_4 = 1</math>, this output delivers the Insert attribute. It allows to insert the video signals in another external video for captioning purposes for example. It can also be used as a general purpose attribute or color.</li> <li>* When <math>TGS_5 = 1</math> and <math>TGS_4 = 0</math>, this pin is a general purpose output port. Its state is programmed by the value of PAT2.</li> </ul>
B	O	Blue/Port 2	<ul style="list-style-type: none"> <li>* When <math>TGS_5 = 0</math>, this output delivers the blue component of the video signal. It is low during the V and H blanking intervals.</li> <li>* When <math>TGS_5 = 1</math>, this pin is a general purpose output port programmed by the value of PAT7.</li> </ul>
Y	O	Composite Luminance	This analog output delivers the composite luminance signal with 8 different grey levels plus the synchronization level.
Sync	I	Sync. Input/Input Port	<ul style="list-style-type: none"> <li>* When <math>TGS_3 = 1</math>, this input allows to vertically and, if <math>TSG_2</math>, is set, horizontally synchronize the TS9347 on an external signal.</li> <li>* When <math>TGS_2 = TGS_3 = 0</math>, the logic state of this input may be read by the microprocessor, and acts as a general purpose input port.</li> <li>* This input must be grounded if not used.</li> </ul>

## OTHER PINS

Name	Pin Type	Function	Description
CLK XTAL	I/O	Crystal/Clock Input Crystal Output	These pins allow to connect a crystal to generate the input frequency from 12 to 15 MHz. If an external signal is used, it must be applied on CLK input, XTAL is left unconnected.
CLKOUT	O	Clock Output	When internal oscillator is used, this pin provides a TTL compatible oscillator output for general operation.
$V_{SS}$	S	Power Supply	Ground.
$V_{DD}$	S	Power Supply	+ 5 V
$V_{SSC}$ $V_{DDC}$	S	Power Supply Power Supply	These pins provide separate 0 V and 5 V power supply for the Y analog converter, allowing easier noise reduction.

**FUNCTIONAL DESCRIPTION**

The TS9347 is a low cost, semigraphic, CRT controller.

The TS9347 displays up to 25 rows of 40 characters or 25 rows of 80 characters, including either an upper or lower service row.

The on-chip character generator provides a standard, 5 x 7, character set and standard semigraphic sets.

More user definable (8x10) alphanumeric or semigraphic sets may be mapped in the 32 K x 8 private memory addressing space.

These user definable sets are available only in 40 characters per row format.

**MICROPROCESSOR INTERFACE**

The TS9347 provides an 8-bit, address/data multiplexed, microprocessor interface.

It is directly compatible with popular (6801, 8048, 8051, 8085....) microprocessors.

**REGISTERS**

The microprocessor directly accesses 8 registers :

- R0 : Command/status register
- R1, R2, R3 : Data registers
- R4, R5 ] Each of these register pairs points into
- R6, R7 ] the private memory.

Through these registers, the microprocessor indirectly accesses the private memory and 5 more registers :

- ROR, DOR : Base address of displayed page memory and of user external character generators.
- PAT, MAT, TGS : Used to select the I/O configuration, the page attributes and format, and to program the timing generator options.

**PRIVATE MEMORY**

The user may partition the 32 K x 8 private memory addressing space between :

- pages of character codes (2 K x 8 or 3 K x 8),
- external character generators,
- general purpose user area.

Many types of memory components are suitable :

- ROM, DRAM or SRAM,
- 2 K x 8, 8 K x 8, 16 K x 4, 32 K x 8 organization,
- Modest 400 ns cycle time and 240 ns access time is required.

**40 CHARACTERS PER ROW : CHARACTER CODE FORMATS AND ATTRIBUTES**

Once the 40 characters per row format has been selected, one character code format out of two must be chosen :

- 24-bit format  
All the attributes are provided in parallel.
- 16-bit format :  
Some parallel attributes, others are latched.

The 16-bit fixed format is compatible with EF9345 CRT controller.

Character attributes provided :

- Back ground and foreground color (3 bits each),
- Double height, double width,
- Blinking,
- Reverse,
- Underlining,
- Conceal,
- Insert,
- 11 x 100 user definable character generator in memory.

**80 CHARACTERS PER ROW FORMAT : CHARACTER CODE FORMAT AND ATTRIBUTES**

Two character code formats are provided :

- Long (12 bits) with 4 parallel attributes :
  - Blinking,
  - Underlining,
  - Reverse,
  - Color select
- Short (8 bits) : no attributes.

**TIMING GENERATOR**

The whole timing is derived from a 12 to 15 MHz on chip oscillator.

The RGB outputs are shifted at 8 to 10 MHz for the 40 character/row format and at 12 to 15 MHz for the 80 character/row.

The timing generator allows different display modes :

- Interlaced or not
- Master or slave synchronization.

**VIDEO OUTPUT**

The video output is always available as a composite luminance signal on the analog output Y ; the logic R, V, B, Syncout and Insert components may be selected on the RGB output pins.

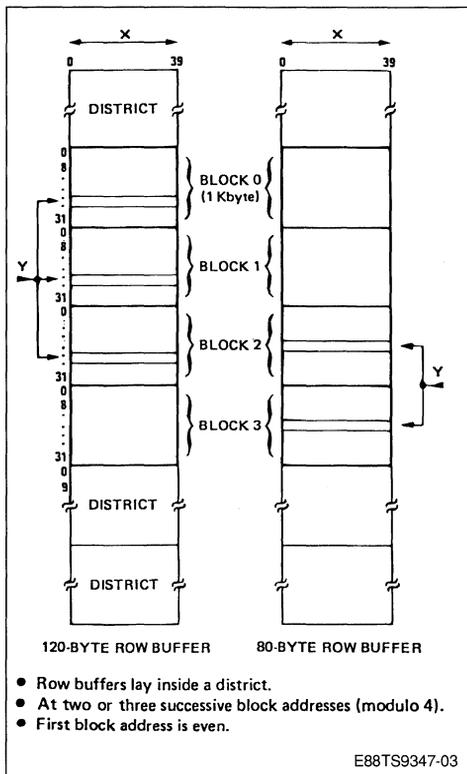
**MEMORY ORGANIZATION**

**LOGICAL AND PHYSICAL ADDRESSING**

The physical 32 Kbyte addressing space is logically partitioned by the TS9347 into 40-byte buffers (Figure 1). More precisely, a logical address is given by an X, Y, Z triplet where :

- X = (0 to 39) points to a byte inside a buffer,
- Y = (0,8 to 31) points to a buffer in a 1 Kbyte block,
- Z = (0 to 31) points to a block.

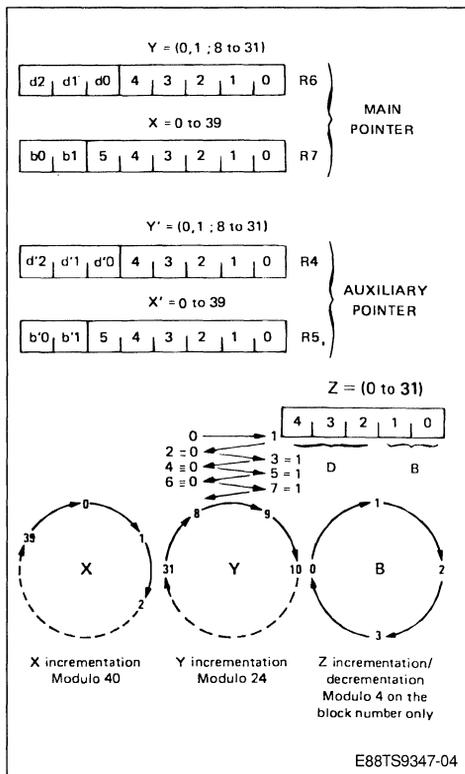
**Figure 1 : Memory Row Buffer.**



Both pointers have the same format. R7 (resp. R5) holds the X component and the two LSB's of the Z component. R6 (resp R4) holds the Y component and the three MSB's of the Z component. This package induce a partitioning of Z in 8 districts of 4 blocks each.

Logical to physical translation is performed on chip following Figure 4 scheme.

**Figure 2 : Pointer Auto Incrementation.**



**POINTERS**

Each X, Y, and Z component of a logical address is binary encoded and packed in two 8-bit registers. Such a register pair is a pointer (Figure 2). TS9347 contains two pointers :

- R6, R7 : main pointer
- R4, R5 : auxiliary pointer.

**DATA STRUCTURES IN MEMORY**

A page is a data structure displayable on the screen up to 25 rows of characters. According to the character code format, each row on the screen is associated with 2 (or 3) 40-byte buffers. This set of 2 (or 3) buffers constitutes a row buffer (Figure 1). The buffers belonging to a row buffer must meet the fol-

lowing requirements :

- they have the same Y address,
- they have the same district number,
- they lie at 2 (or 3) successive (modulo 4) block addresses in their common district.

Consequently, a row buffer is defined by its first buffer address and its format.

A Page is a set of successive row buffers :

- with the same format,
- with the same district number,
- with the same block address of first buffer. This block address must be even.
- lying at successive (modulo 24) Y addresses.

Consequently, a page should not cross a district boundary. General purpose memory area may be used but should respect the buffer or row buffer structure. See Figure 2 for pointer incrementation implied by these data structures.

**MEMORY TIME SHARING (see Figure 3)**

The memory interface provides a 500 ns cycle time at Fin = 12 MHz. That it to say a 2 Mbyte/s memory bandwidth is shared between :

- reading a row buffer from memory to load the internal row buffer (up to 120 bytes once each row),
- reading user defined characters slices from memory (1 byte each  $\mu$ s),
- indirect microprocessor read or write operation,
- refresh cycles to allow DRAM use, with no overhead.

A fixed allocation scheme implements the sharing.

Notes on Figure 3.

1. Dummng cycles are read cycles at dummy addresses.
2. RFSH cycles are read cycles performed by an 8-bit auto-incrementing counter. Low order address byte ADM (0:7) cycles through its 256 states in less than 1 ms.
3. The microprocessor may indirectly access the memory once every  $\mu$ s, except during the first and the last line of a row, when the internal buffer must be reloaded.

During these lines, no microprocessor access is provided for 104  $\mu$ s ; this holds too when no user defined character slices are addressed.

**Figure 3 : Memory Cycle Allocation (12 MHz operation).**

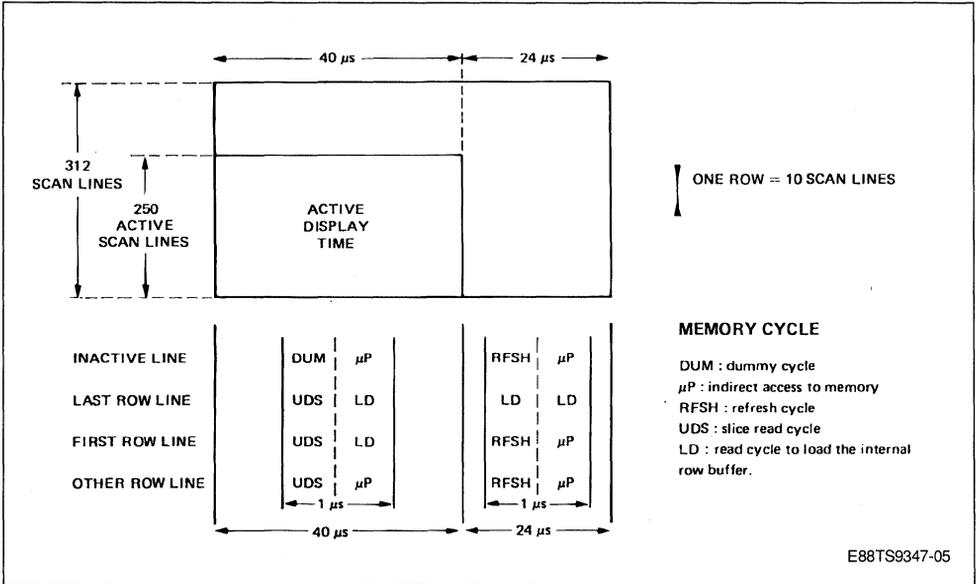
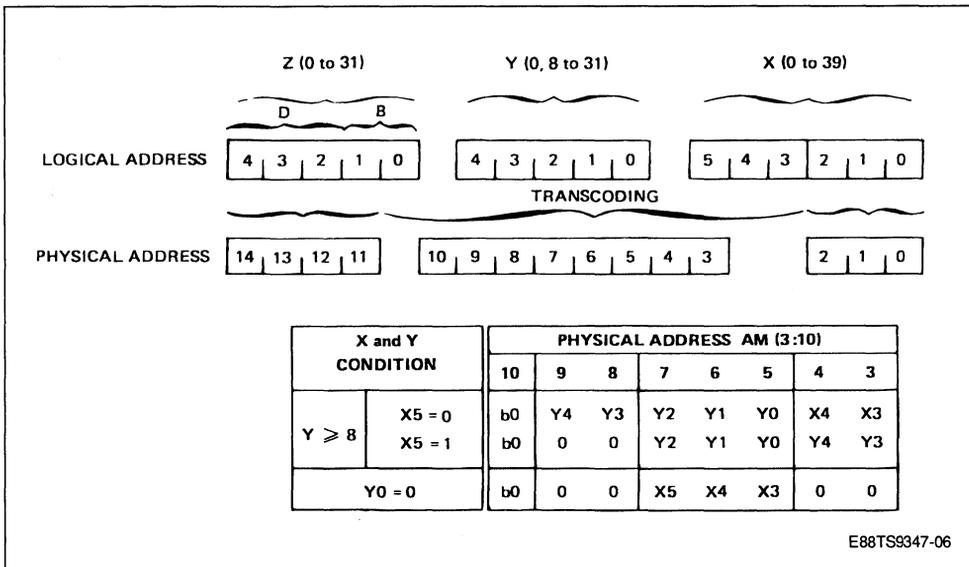


Figure 4 : Logical to Physical Address Transcoding Performed on-chip.



**SCREEN FORMAT AND ATTRIBUTES OUTPUTS CONFIGURATION**

The screen format and attributes are programmed through 5 indirectly accessible registers : ROR, TGS, PAT, MAT, and DOR. IND command allows accessing to these registers. TGS is also used to select the timing generator options (see Screen Format Table).

**ROW AND CHARACTER CODE FORMAT : TGS (6:7)**

Two row formats and 4 character code formats are available but cannot be mixed in a given screen.

**TIMING GENERATOR AND CONFIGURATION OPTIONS : TGS (1:5)**

**TGS1 = 0** : noninterlaced mode, 312 lines/frame.

**TGS1 = 1** : interlaced mode, 312.5 lines/frame.

**TGS (2,3)** : input synchronization configuration.

The SYNC input may be interpreted as a synchronization signal or as a general purpose input port, which state can be read by the microprocessor in the status register (bit 2). Alternatively, the vertical synchronization output from the timing generator can be read in the same register.

The composite incoming SYNC IN signal is separated into two internal signals :

- Vertical Synchronization In (VSI)
- Horizontal Synchronization In (HSI)

**TGS3 = 1** enables VSI to reset the internal line count : SYNC IN input is sampled at the beginning of the active area of each line. When the sample transits from 0 to 1, the line count is reset at the end of the current line.

**TGS3 = TGS2 = 1** enables HSI to control an internal digital PLL : HSI and on-chip generated H. SYNC OUT are considered as in phase if their leading edges match at plus or minus 1 clock period. When they are out of phase, the line period is lengthened by 1 clock period (80 ns at 12 MHz).

Screen Format Table resumes the different combinations.

**TGS (4,5)** : output configuration

Three output pins may be configured to output either video signals or general purpose output ports. The Screen Format Table summarizes the possible configurations, with the following definitions :

R, V, B : Red, Green and Blue Video components

I : Insert signal

HVS : Composite H and V synchro output

P1, P2 : General purpose output ports

PAT2 gives the value of P1, PAT7 gives the value of P2 : a logical "1" will cause a "high" on the corresponding output, while a "0" results in a "low".

SCREEN PARTITION, PAGE POINTER ROR  
(see top of the Screen Format Table)

The screen is partitioned in three areas :

- \* The margin
- \* The service row
- \* The bulk or remaining rows

MAT (0:3) declares the color of the margin and the value IM of its insert attribute.

DOR7 and ROR register point to the page to be displayed : DOR7 gives the MSB of the Z address, ROR (7:5) three next bits, the LSB is implicitly ZO = 0 (the page block address must be even). YOR (= ROR (4:0)) gives the first row to be displayed at the top of the bulk area. The next row buffers to be displayed are fetched sequentially by incrementing the Y address (modulo 24). This address never gets out of the origin block. Incrementation of YOR by the microprocessor yields a roll up.

SERVICE ROW : TGSO ; PATO

The 10 scan line service row can be displayed at the top or the bottom of the screen, depending on the value of TGSO. The service row is fetched from the origin block at Y = 0 ; it does not roll ; it may be disabled by PATO = 0 ; it is then displayed as a margin extension.

BULK : PAT1 ; MAT7

The bulk is displayed for 240 scan lines. Each row buffer is usually displayed for 10 scan lines. However, MAT7 = 1 doubles this figure : then every character appears in double height (double height characters are quadrupled).

PAT1 = 0 disables the bulk. When disabled, the corresponding scan lines are displayed as a margin extension.

CURSOR : MAT (4:6)

To be displayed with the cursor attribute, a character must be pointed by the main pointer (R6, R7) and MAT6 must be set. The cursor attributes are given by MAT (4,5) :

- Complementation :

The R, G, B or each pixel is logically negated :

R, G, B →  $\bar{R}$ ,  $\bar{G}$ ,  $\bar{B}$

- Underline :

The underline attribute is negated

- Flash :

The character is periodically displayed with, then without the cursor attribute (50%/50% ≈ 1 Hz).

FLASH ENABLE (PAT 6) - CONCEAL ENABLE (PAT3)

Any character flashing attribute is a "don't care" when PAT6 = 0. When PAT6 = 1, a character flashes if its flashing attributes is set. It is then periodically displayed as a space (50%/50% ≈ 0.5 Hz).

PAT3 is a "don't care" for 80 char./row formats. When any 40 char./row format is in use :

\* if PAT3 = 0, the conceal attribute of any character is a "don't care"

\* if PAT3 = 1, the conceal attribute of each character is interpreted : a concealed character appears as a space on the screen.

**INSERT MODES : PAT (4:5)**

These modes make sense only if the insert signal I is available on the G pin, that is to say when TGS4 = 1.

During retrace, margin and extended margin periods, the I signal outputs the value of the insert margin attribute : I = IM = MAT3.

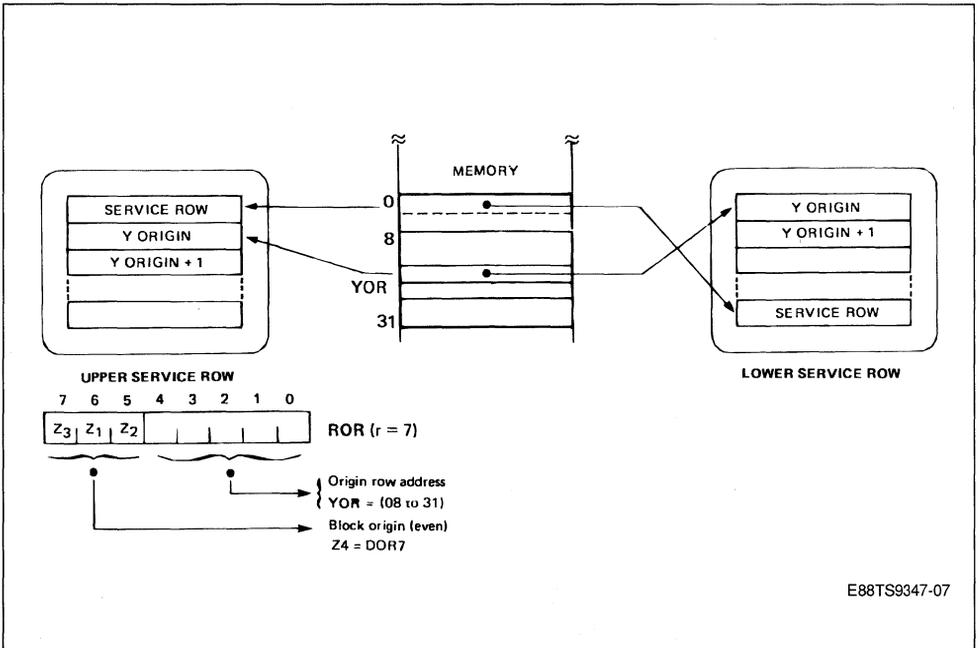
During active line period, the I output is controlled by the insert mode, and I1 and I2, the insert attributes of each characters. The I output may have several uses : (See figure below).

- \* As a margin/active area signal in the Active Area Mark mode
- \* As a character per character marker signal in the Character Mark mode
- \* As a video mixing signal in the other modes, provided that the TS9347 has been vertically and horizontally synchronized with an external video source : the I output allows mixing TS9347 video output (I = 1) and external video signal (I = 0). This mixing may occur for the complete character window (Boxing mode) or only for the foreground pixels (Inlay mode).

**VIDEO OUTPUT DURING ACTIVE PERIODS**

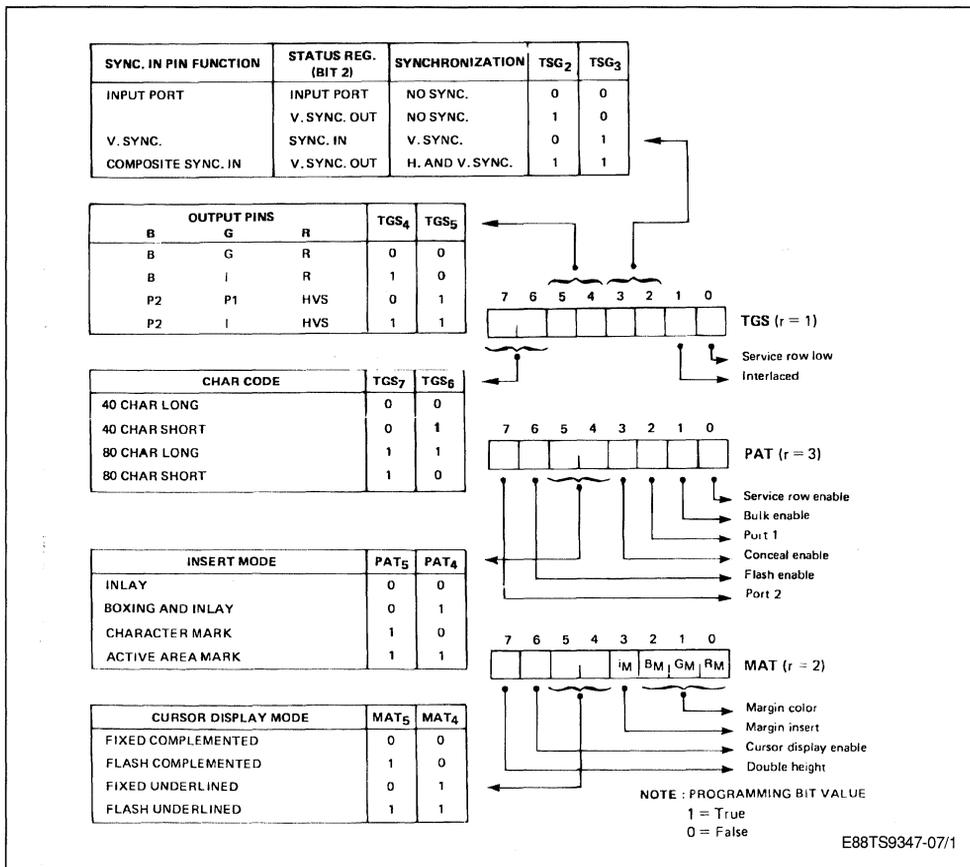
Insert Mode	I1	I2	Char. Level Pixels	I	Video Output	Comments
Active Area Mark	-	-	-	1	Unchanged	
Character Mark	0	-	-	0	Unchanged	
	1	-	-	1	Unchanged	
Inlay	0	-	-	0	Black	Non Insert
	1	-	Background	0	Black	
	1	-	Foreground	1	Unchanged	Inlay
Boxing and Inlay	0	-	-	0	Black	Non Inserted
	1	0	-	1	Unchanged	
	1	1	Background	0	Black	
	1	1	Foreground	1	Unchanged	Inlay

**SCREEN FORMAT TABLE**



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SCREEN FORMAT TABLE (continued)



E88TS9347-07/1

40 CHAR/ROW CHARACTER CODES

To display pages in 40 character per row format, one out of two character code formats must be selected :

- \* Long (24 bits) code : all parallel attributes.
- \* Short (16 bits) code : mix of parallel and latched attributes.

Short codes are translated into long codes by the TS9347 during the internal row buffer loading process. The choice of the character code format is obviously a display flexibility/memory size trade off, left up to the user.

LONG CODES

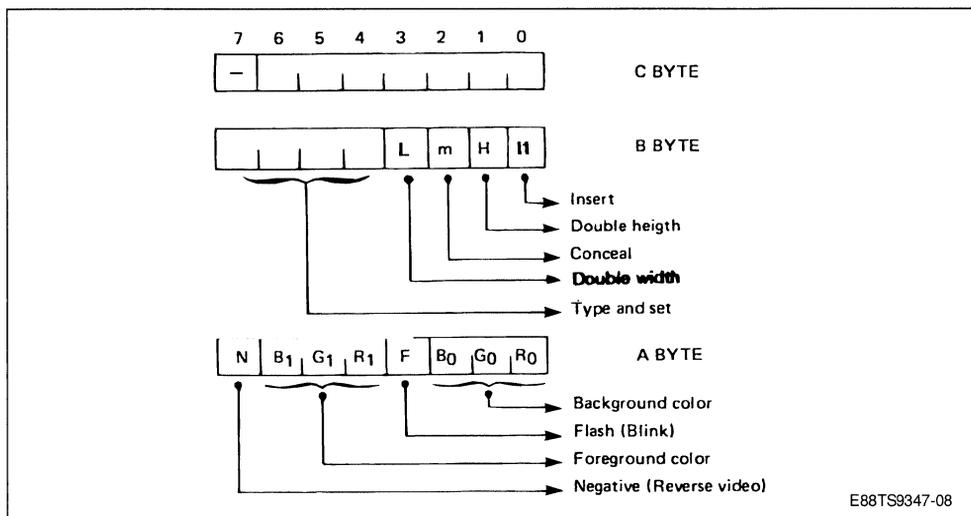
This is the basic 40 char/row code. Each 8 pixel x 10 lines character window on the screen is associated with a 3-byte code in memory, namely the C, B,

and A bytes (Figure 5). A row on the screen is associated with a 120 byte row buffer in memory.

3-byte code structure

1. C7 is a don't care. Up to 128 characters may be addressed in each set. Each user definable set holds only 100 characters : C-byte value ranges from 00 to 03 and 20 to 7F (hexa).
2. B (3:7) give the type and the set number of the character.
3. When I2, U, L are not programmable, the default value of these attributes is 0.
4. Character code byte A defines a two color set giving directly (Figure 6) the two values (B1, G1, R1) and (B0, G0, R0) respectively affected to the 1's and the 0's of the character pattern. The negative attribute, when set, exchanges the two values.

Figure 5 : 40 Character Long Codes.



Type and Set B (3:7)					Number of Character Per Set	Set Name	Set Type	Cell Location
B7	B6	B5	B4	B3	C (0:6)			
0	12	1	0	L	128 STANDARD MOSAIC	G10	SEMI GRAPH	ON CHIP ROM
	12	1	1	L	32 COMPLEMENT. CELLS	GOE		
	12	0	U	L	128 ALPHANUMERICS	G0	ALPHA	
1	0	0	U	L	100 ALPHA UDS	G'0	SEMI GRAPH	EXTERNAL RAM
	0	1	0	L	100 SEMI-GRAPHIC UDS	G'10		
			1	L	100 SEMI-GRAPHIC UDS	G'11		
	1	X	X	X	800 SEMI-GRAPHIC UDS	Q0:7		

L = Double width  
 U = Underlined

**Note 1 :** Double height, double width : a correct operation assumes that the same character code had been repeated in the page memory (Twice for double height or double width, four times for double size).

**2 :** Double height : each slice of the character is repeated : twice to get a 8 x 20 pattern. However for the alphanumeric characters, these scheme is slightly different : the upper slice (SN = 0) is tripled, the next (SN = 1 to 8) are doubled, and the last (SN = 9) is displayed only once.



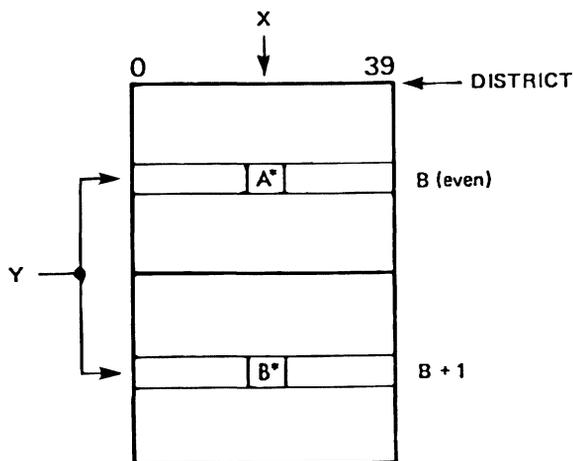
Figure 9 : Short Codes in Memory Double Row Buffer.

**TSM COMMAND**

R1	A*
R2	B*
R3	W
R4	—
R5	—
R6	D, Y
R7	B, X

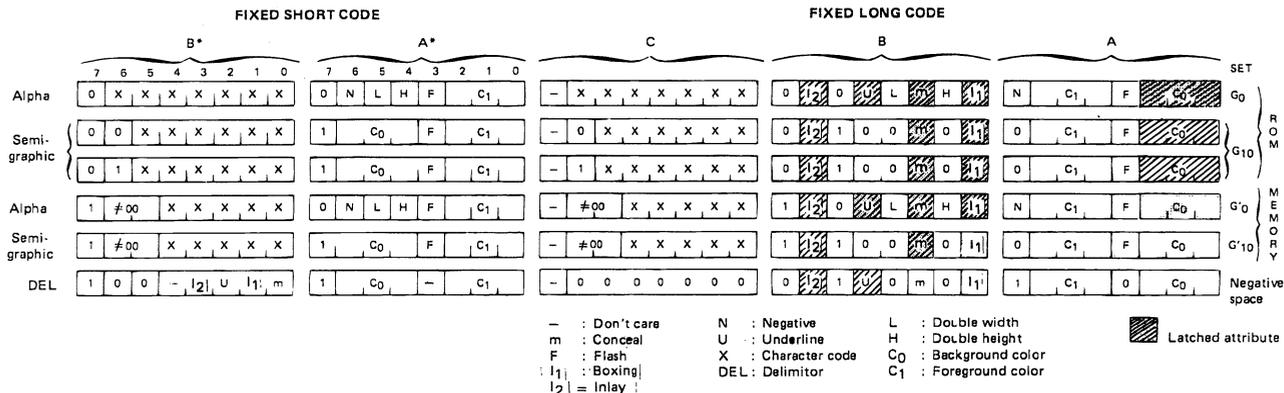
**TSA COMMAND**

R1	A*
R2	B*
R3	W
R4	D, Y
R5	B, X
R6	
R7	



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Figure 10 : Fixed Short Code to Fixed Long Code Translation.



NOTES

1/ Translation process

The translation process operates through 3 elementary operations :

- Field-to-field : a character code or an attribute value (i.e : C<sub>0</sub>, flashing) is directly loaded from short to long code.
- Field-to-constant : the decoding of a short code forces the value of the equivalent long code attribute. For example, semigraphic short characters forces normal size (H = 0, L = 0) attributes.
- Latched attributes : at the beginning of each row, these attributes are reset (no underline, not concealed, no insert, black background). Then, they keep their current value until modified by either a field to field or field to constant operation.

2/ Insert attribute

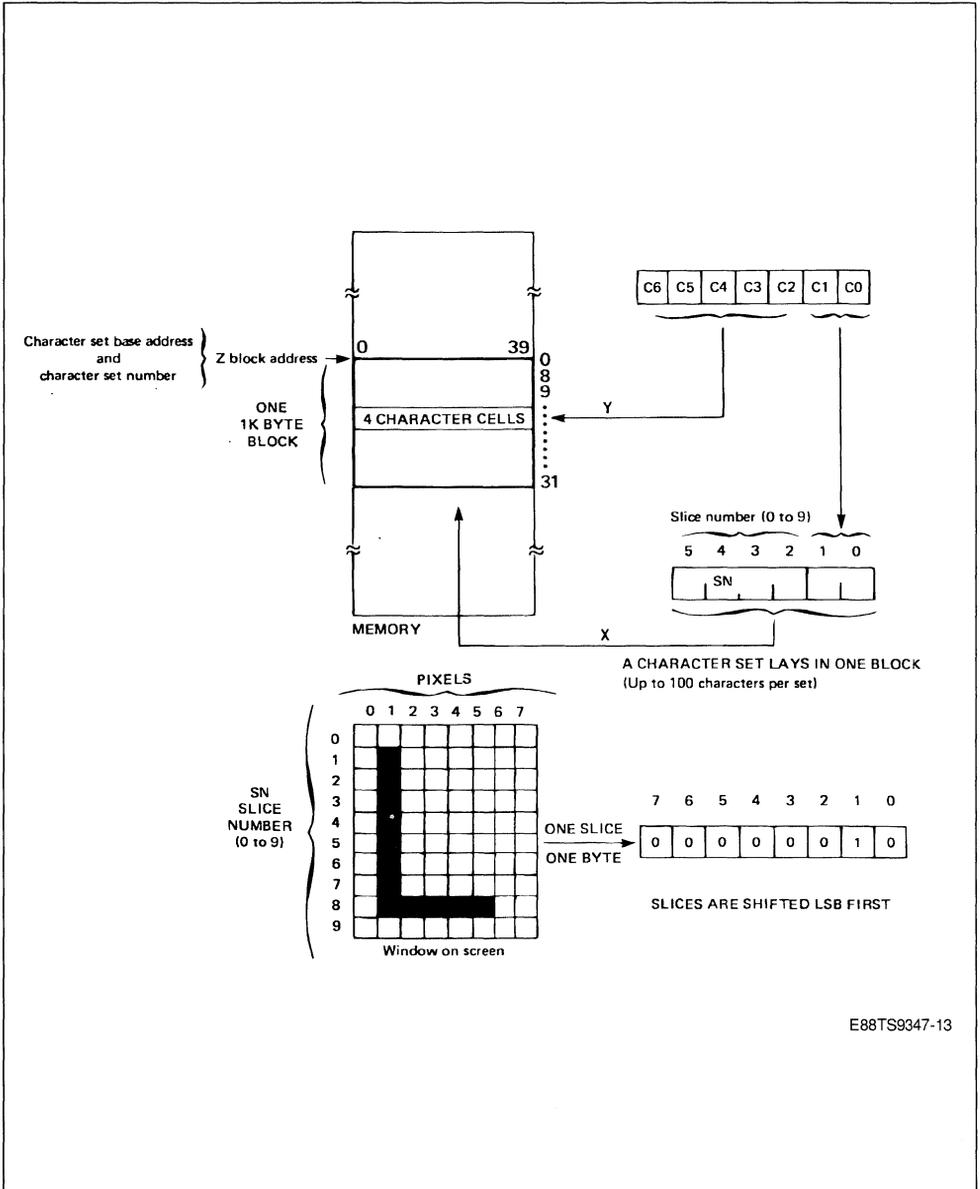
l<sub>2</sub> is interpreted both in G<sub>0</sub> and G<sub>10</sub>, contrary to long code mode.

**USER DEFINED CHARACTER GERATOR IN MEMORY : DOR REGISTER**

With 40 char./row, the elementary window dimensions on the screen are 10 slices x 8 pixels. Thus,

a character cell holds 10 bytes in memory and 4 character cells are packed in one 40-byte buffer (Figure 11).

**Figure 11 : Packing Uds Cells in Memory.**

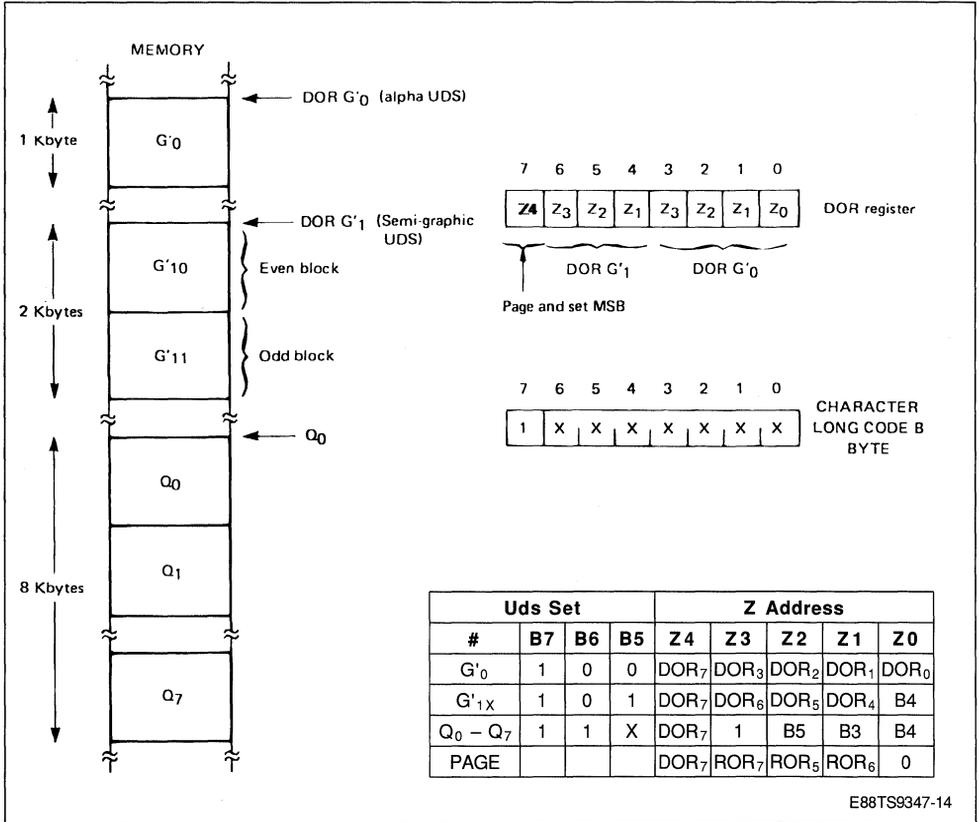


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The cells of one given character set should be layed in one block.  
 Up to 100 character cells may be addressed in each set.  
 The location in memory, where to fetch the sets in use, are declared by DOR register (Figure 12).

For each type of set, it gives the MSB(s) of the Z block address. TS9347 reads the Z LSB(s) in the B byte of the (equivalent) long code. As usual, the character code is read in the C byte. SN is derived from the scan line rank in the row and the double height status.

**Figure 12 : Uds Fetch to Display.**



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**LOADING USER DEFINED CHARACTER SET**

Before loading a character set into RAM, the user must

- Assign a name to the set :  
G<sub>0</sub>, G<sub>10</sub>, G<sub>11</sub>, or Q<sub>0-7</sub>
- Assign a character number to each character belonging to this set. Character numbers range from 0 to 3 and 32 to 127.  
It is binary coded into 7 bits C (0.6) - C (0.6) will be loaded later into a C byte character code in order to display the character.
- A pointer to a character slice in memory is then manufactured from

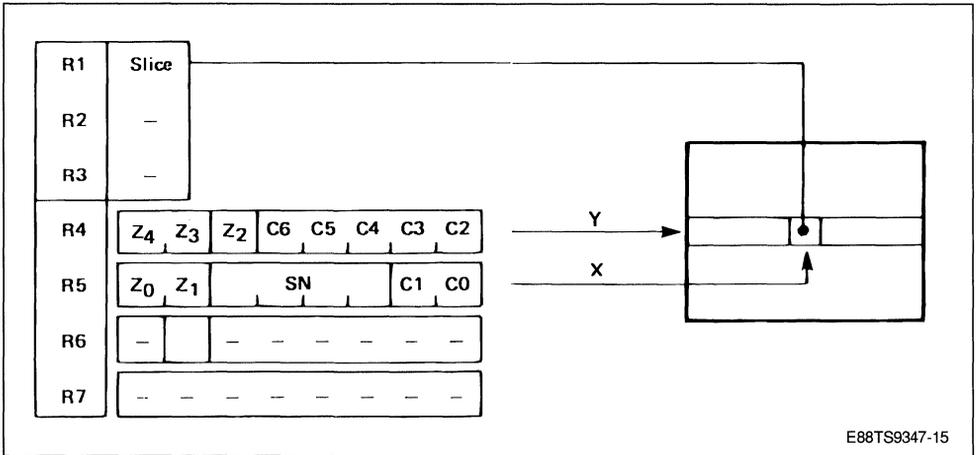
- the character number C (0.6)
- the slice number SN (0.3)
- the bloc number assigned to the set Z (0.4)

Note : Different sets may be mixed in the same block, as long as the character have different code numbers.

Figure 13 shows how to proceed with the auxiliary pointer and the TBM and TBA commands.

Note : The main pointer may be also used. When sequentially accessing slices of a given character, auto incrementation is helpless.

**Figure 13 : Accessing a Character Slice in Memory using TBA Command.**



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**ON-CHIP CHARACTER GENERATOR**

- G<sub>0</sub> and G<sub>0E</sub> are common to 40 and 80 char./row modes (Figure 14 and Figure 23).
- G<sub>10</sub> is the standard mosaic set for videotex (Figure 15).
- G<sub>0E</sub> cannot be reached from the 16 bit short codes (Figure 16).

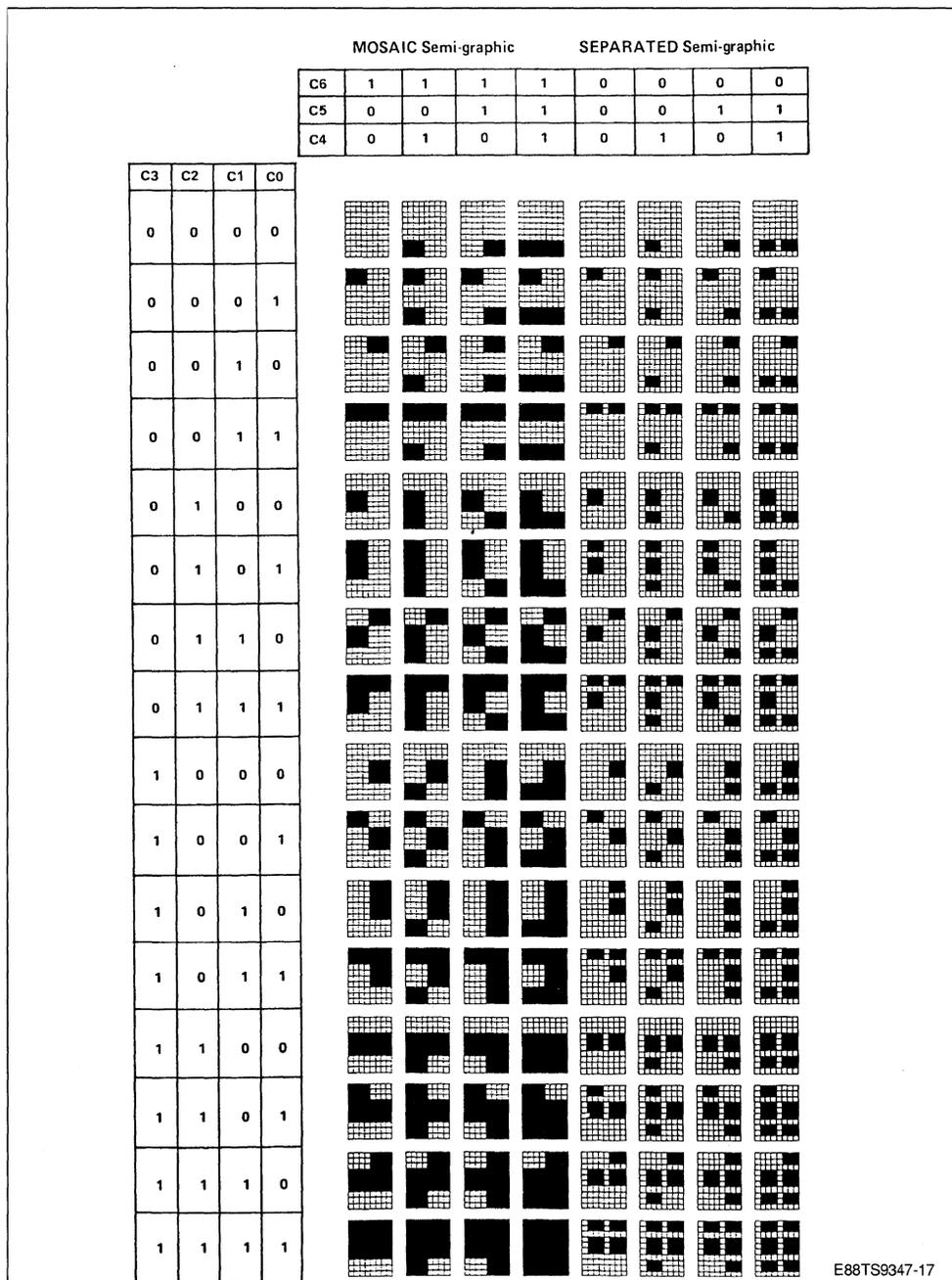
**DISPLAYING THE ATTRIBUTES**

1. For normal operation, a double height and/or double width character must be repeated in memory in two successive Y and/or X positions. The user may otherwise freely mix any character size.
2. The attributes are logically processed in the following order :

- Underline or underline cursor : foreground forced on the last slice (SN = 9).
  - Flash : background periodically forced on the whole window (≈ 0.5 Hz). The phase depends on the negative attribute.
  - Conceal : background forced permanently on the whole window. A concealed character neither blinks nor is underlined.
  - Negative : exchange the background and foreground color values when set.
  - Coloring.
  - Complemented cursor mode.
  - Insert : black color forced when required.
3. Basic pixel shift frequency :  $f_{CLK} \times 2/3 = 8$  to 10 MHz



Figure 15 : G<sub>10</sub> Semigraphic Character Set.



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Figure 16 : GOE Extension Character Set.

				C5	0	0
				C4	0	1
C3	C2	C1	C0			
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

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**80 CHAR / ROW CHARACTER CODES**

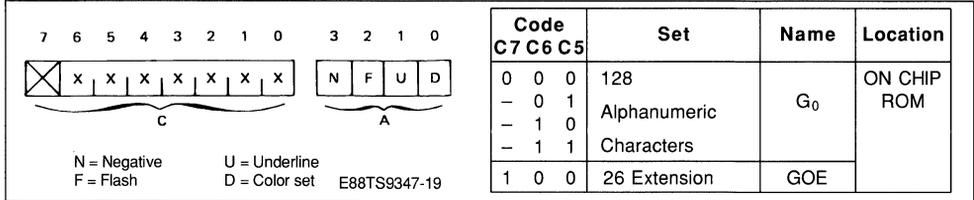
To display pages in 80 character per row format, one of two character code formats must be selected :

- Long (12 bits) code : 4 parallel attributes

- Short (8 bits) code : no attribute.

Both formats address the on-chip G<sub>0</sub> and GOE sets (154 characters 6 x 10) sets. None allows UDS addressing.

**Figure 17 : 80 Char/Row Character Code.**



**LONG CODES**

Each 6 pixels x 10 lines character window on the screen is associated with a 12-bit code in memory, namely a C byte and an attribute nibble A (Figure 17).

**SHORT CODES**

They are derived from the long code by giving a 0 implicit value to each bit of the A nibble positive, not underlined, not flashing.

**PACKING THE CODES IN MEMORY**

Long codes are paired. A pair is packed in a 3-byte word. Therefore, the 80 codes of a row fill a 120-byte row buffer (Figure 18). The left most position on the screen is even. Its corresponding C byte is at the beginning of the first buffer. The next position on the screen is odd. Its corresponding C byte is at the beginning of the second buffer. Both nibbles are

packed in the third buffer. With short codes, the same scheme yields 80-byte row buffers.

**ACCESS TO THE CODES IN MEMORY**

KRL command transfers 12 bits from/to the R1 and R3 registers to/from memory. The read modify write operation, necessary to write the A nibble in memory, is automatically performed provided that the A nibble is repeated in the R3 register (Figure 19). Dedicated auto-incrementation is also performed when required.

KRS command does a similar job the short codes (Figure 20).

A very simple scheme allows the microprocessor to transcode an horizontal screen location into a pointer (Figure 21). The joint use of this scheme with the dedicated command alleviates all the packing/unpacking troubles.

**Figure 18 : 80 Char / Row Code Packing.**

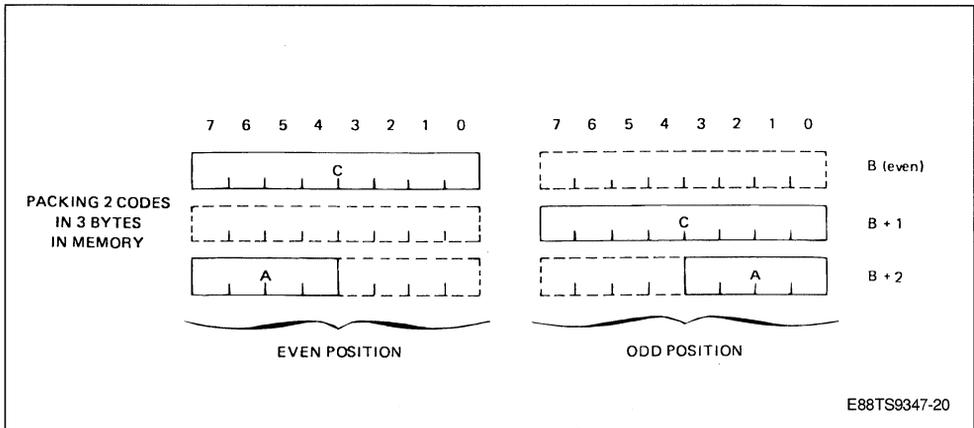


Figure 19 : KRL Command : Sequential Access to Long Codes.

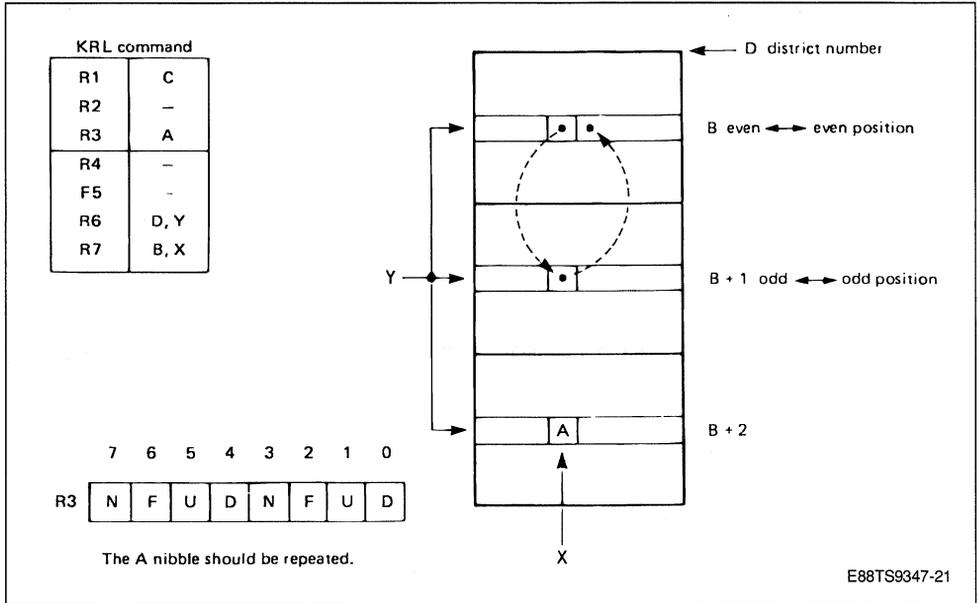
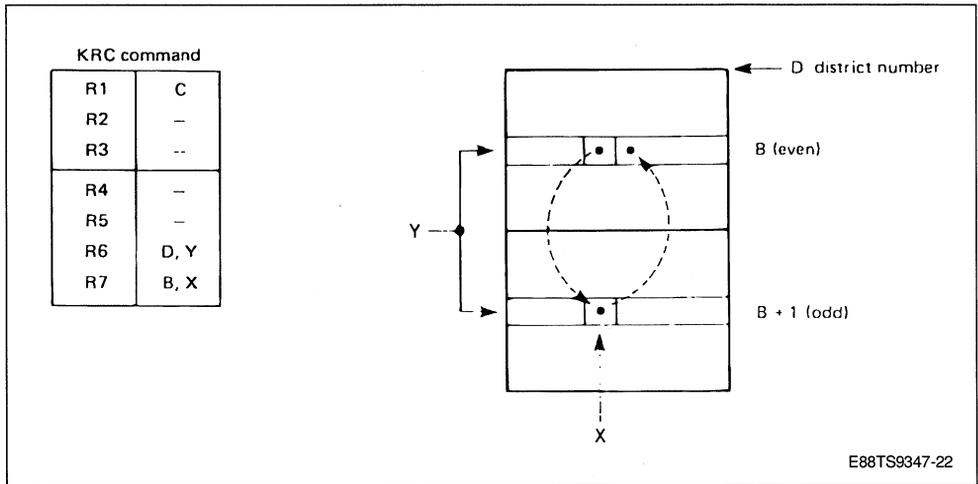
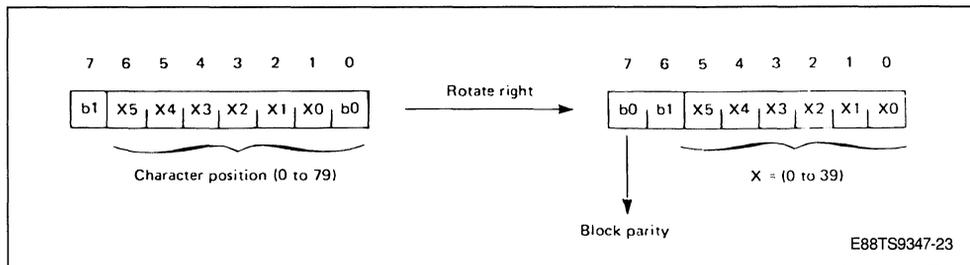


Figure 20 : KRS Command Sequential Access to Short Codes.



**Figure 21 : Transcoding an Horizontal Screen Location into a R7 Pointer.**



**DISPLAYING THE ATTRIBUTES : DOR REGISTER**

Short code character are not flashing, not underlined and "positive".

The attributes are processed in the following order :

- Underline or underlined cursor : foreground is forced on the last slice (SN = 9).
- Flash : background is periodically (0.5 Hz - 50%) forced on all the window. The phase depends on the negative attribute.
- Color select : a "positive" character is displayed with a background color same as the margin co-

lor. The foreground color is selected in DOR register by the D attribute.

- Negative : when the character is negative, background and foreground colors are exchanged. In complemented CURSOR position, these colors are complemented.
- Insert : The D attribute selects one insert value in DOR register. This attribute is then processed up to the current insertion mode (see screen format and attribute insert section).

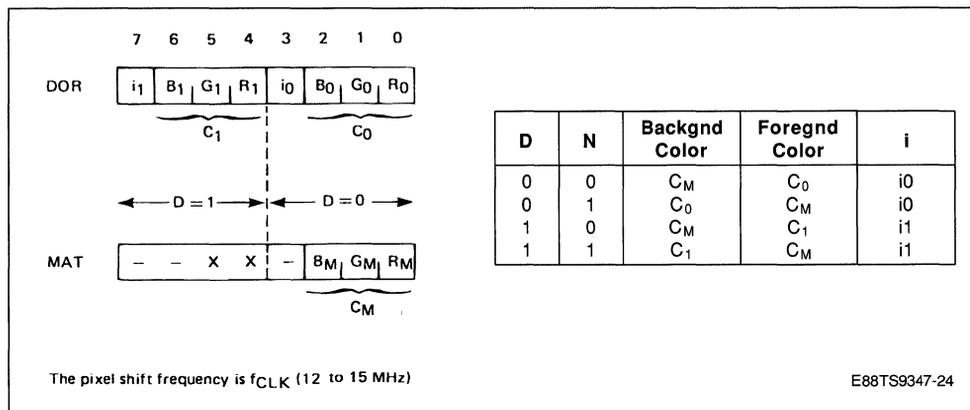
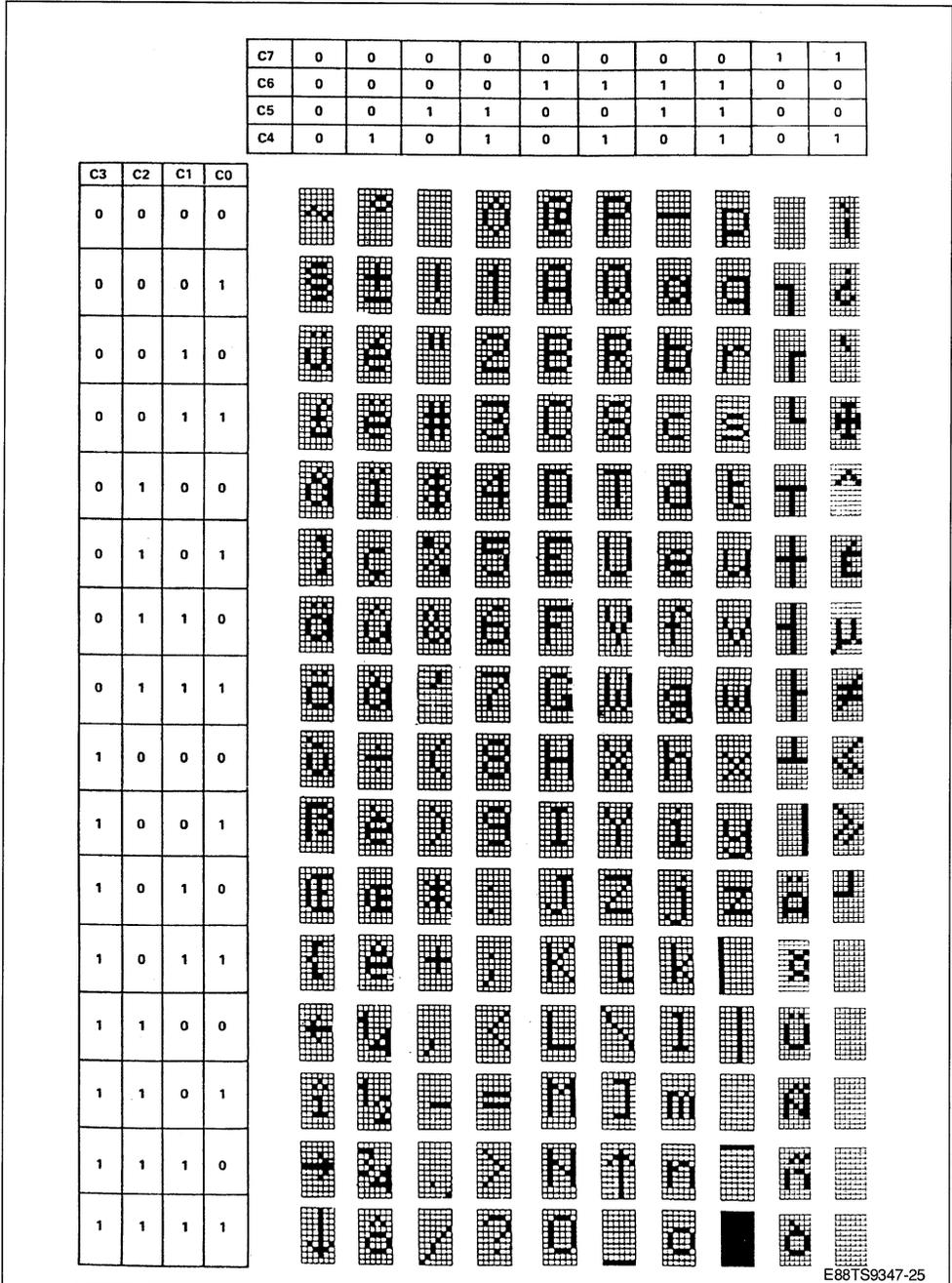


Figure 22 : GoE Alphanumeric Character Set in 80 Character/Row Mode - TS9347.



E88TS9347-25

**MICROPROCESSOR ACCESS COMMANDS**

A microprocessor bus cycle may transfer one byte from/to the microprocessor to/from a directly addressable register. These registers provide an indirect access :

- to/from 5 on-chip indirect registers : ROR, DOR, MAT, PAT and TGS.
- to/from the dedicated memory.

Due to address/data multiplexing, a bus cycle is a 2 phase process (see Timing diagram 1 or Timing diagram 2).

**ADDRESS PHASE**

The falling edge of AS latches the AD (0.7) bus state and CS signal into the temporary A address register (Figure 23).

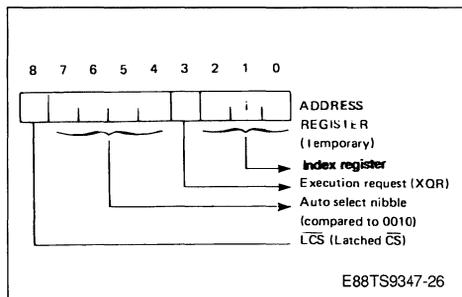
- A (0:2) = i  
This register index designates one out of 8 direct access registers  $R_i$ .
- A3 = XQR  
This is the execution request bit.
- A (4:7) = ASN  
This is the Auto-Selection Nibble.

- $A8 = \overline{LCS}$

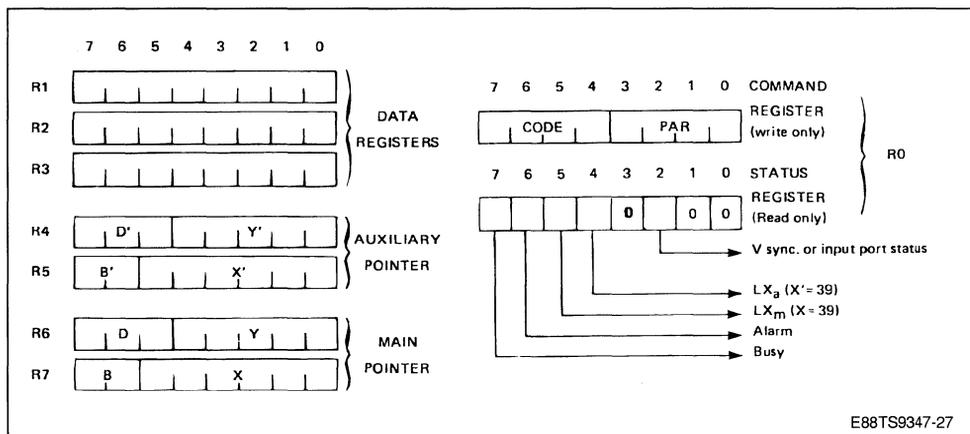
This is the latched value of  $\overline{CS}$  input pin.

TS9347 is selected when the following condition is met : ASN = 2 (Hexa) and LCS = 0.

Therefore, TS9347 is mapped in the hexadecimal microprocessor addressing space from XX20 to XX2F, where XX is up to the user. When TS9347 is not selected, its AD bus pins float and no register can be modified.



**Figure 23 : Direct Access Registers.**



**DATA PHASE - REGISTERS**

When TS9347 is selected and while AS input is low, the  $R_i$  register is accessed.

R0 designates a write-only COMMAND register or a read-only STATUS register.

R1 to R7 hold the arguments of a command. They are read/write registers.

R1, R2, R3 are used to transfer the data.

R4, R5 hold the Auxiliary Pointer (AP).

R6, R7 hold the Main pointer (MP).

(See memory organization ; Pointer section for pointer structure).

**COMMAND REGISTER**

This register holds a 4-bit command type and 4 bits of orthogonal parameters (see COMMAND TABLE).

Type

There are 3 groups of command :

- The IND command which gives access to on-chip resources,

- The character code transfer commands,
- The general purpose commands.

Parameters

R/W : Direction

- 1 : to DATA registers (R1, R2, R3)
- 0 : from DATA registers.

r : Internal resource index (see Figure 24)

l : Auto-incrementation

- 1 : with post auto-incrementation
- 0 : without auto-incrementation.

p : Pointer select

- 1 : auxiliary pointer
- 0 : main pointer

s,  $\bar{s}$  : Source, destination select

- 01 : source : MP ; destination : AP
- 10 : source : AP ; destination : MP

$\bar{a}$ , a : Stop condition

- 01 : stop at end of buffer
- 10 : no stop.

STATUS REGISTER

This is a read-only, direct access register.

S7 : BUSY

BUSY is set at the beginning of any command execution. It is reset at completion.

S6 : AI

S5 : LX<sub>m</sub>

S4 : LX<sub>a</sub>

LX<sub>m</sub> or LX<sub>a</sub> is set when respectively the main pointer or the auxiliary pointer holds X = 39 before a possible incrementation. The alarm bit S6 is set when LX<sub>m</sub> or LX<sub>a</sub> is set and an incrementation is performed after access.

S2 :

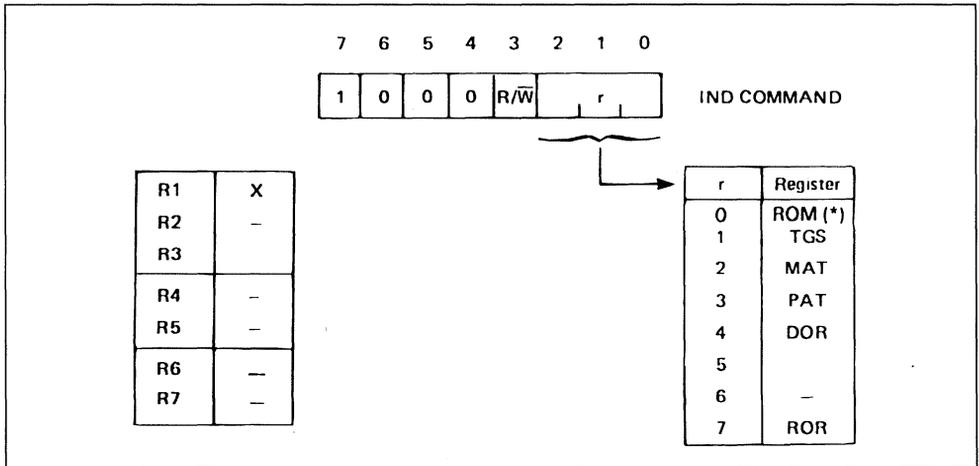
Gives the vertical synchronization signal state, or the input port value.

This is maskable by the VRM command. In this case, its values is 0.

S3 = S1 = S0 = 0 Not used.

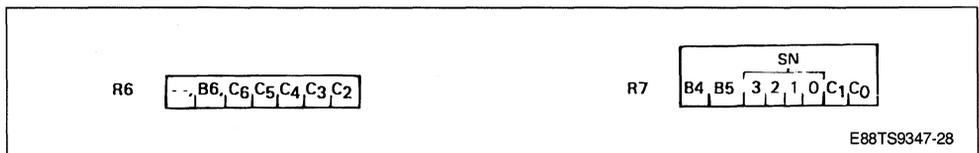
S3 to S6 are reset at the beginning of any command.

The COMMAND TABLE shows every command able to set, each of these status bits, after completion.



\* Note : A slice in 40C only can be read from the internal character generator. The slice address must be initialized in R6, R7.

Figure 24 : Indirect on-chip Ressource Access.



E88TS9347-28

## NOTES ON COMMAND EXECUTION

1. The execution of any command starts at the trailing edge of DS when (and only when) :

- TS9347 has been selected,
- XQR has been set,

at the previous AS falling edge.

This scheme allows loading a command and its argument in any order. For instance, a command, once loaded, may be re-executed with new or partly new arguments.

2. At power on, the busy state is undetermined.

It is recommended to load first a NOP command with XQR = 1 before any effective command.

3. While Busy is set, the current command is under execution. Register access is then restricted.

Register access with XQR = 0

- Read STATUS is effective.
- Write COMMAND or any other register access are ineffective.

That is to say, the microprocessor reads undetermined values and may not modify a register.

Register access with XQR = 1

- Read STATUS or write COMMAND are effective,
- Access to other registers is ineffective.

However, the previous command is aborted and the new command execution launched (with an initial state undetermined for registers and memory locations handled by the aborted command).

## 4. Execution suspension

The execution of any command (except VRM, VSM) is suspended during the last and first scan line of an active row. This is because the memory bus cannot be allocated for microprocessor access during this 208 memory cycle period. This holds too for internal resource access because on-chip data transfer uses internal data memory bus.

IND COMMAND (see figure 24)

This command transfers one byte between R1 and an internal resource. The r parameter designates on-chip indirect register.

CHARACTER CODE ACCESS, TLM, TLA, TSM, TSA, KRL, KRS.

Each of these commands is dedicated to transfer one complete character code between DATA registers and memory.

TLM, TLA transfers 24 bits with Main/Auxiliary Pointer

TSM, TSA transfers 16 bits with Main/Auxiliary Pointer

KRL transfers 12 bits with Main Pointer

KRS transfers 8 bits with Main Pointer

Code packing, pointer and data structures are explained in the corresponding character code section.

When auto-incrementation is enabled, MP or AP is automatically updated after access so as to point to the next location.

This location corresponds to the next right position on screen. When last position ( $X = 39$ ) is accessed,  $LX_m$  is set. When last position is accessed with auto-incrementation, alarm is also set. MP or AP is then pointing back at the beginning of the row : there is no automatic Y incrementation.

GENERAL PURPOSE ACCESS TO A BYTE - TBM, TBA

This command uses either MP or AP pointer.

When MP is in use, an overflow yields to a Y incrementation.

MOVE BUFFER COMMANDS : MVB, MVD, MVT

These are memory to memory commands which use R1 as working register.

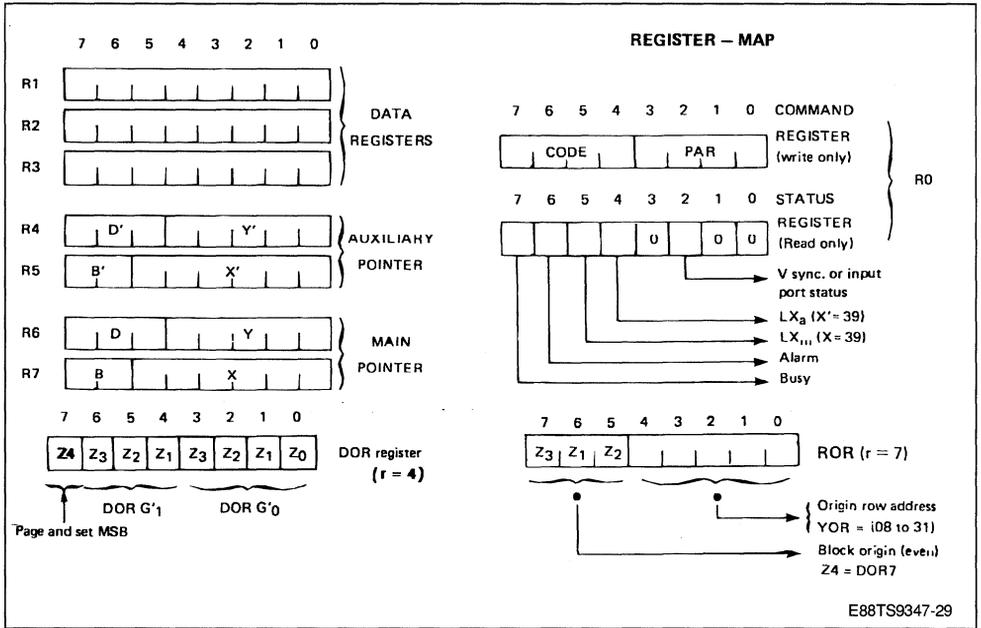
MVB transfers a byte from source to destination, post-increments the 2 pointers and iterates until the stop condition is met. MVD and MVT are similar but work respectively with 2 byte word and 3 byte word. That is to say, MVB works on buffers, MVD on double buffers and MVT on triple buffers. If the parameter  $a = 1$ , the process stops when either source or destination buffer end is reached. If the parameter  $a = 0$ , the process never stops until aborted. In this case, main pointer overflow yields to a Y incrementation in MP. So, a whole block or page may be initialized.

MISCELLANEOUS COMMAND : INY, VRM and VSM

INY command increments Y in MP.

VRM and VSM respectively reset and set a vertical synchronization status mask. When the mask is set, status bit S2 remains at 0. When the mask is reset, status S2 follows the vertical sync. state : it is reset for 2 TV lines per frame and stays at 1 during the remaining period. It becomes readable by the microprocessor from the status register. After power on, the mask state is undetermined.

REGISTER - MAP



REGISTER – MAP (continued)

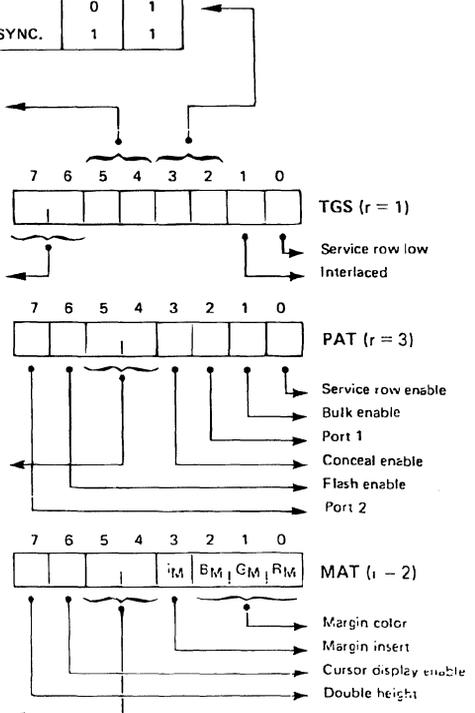
SYNC. IN PIN FUNCTION	STATUS REG. (BIT 2)	SYNCHRONIZATION	TSG <sub>2</sub>	TSG <sub>3</sub>
INPUT PORT	INPUT PORT	NO SYNC.	0	0
V. SYNC.	V. SYNC. OUT	NO SYNC.	1	0
COMPOSITE SYNC. IN	SYNC. IN	V. SYNC.	0	1
	V. SYNC. OUT	H. AND V. SYNC.	1	1

OUTPUT PINS			TGS <sub>4</sub>	TGS <sub>5</sub>
B	G	R		
B	G	R	0	0
B	I	R	1	0
P2	P1	HVS	0	1
P2	I	HVS	1	1

CHAR CODE	TGS <sub>7</sub>	TGS <sub>6</sub>
40 CHAR LONG	0	0
40 CHAR SHORT	0	1
80 CHAR LONG	1	1
80 CHAR SHORT	1	0

INSERT MODE	PAT <sub>5</sub>	PAT <sub>4</sub>
INLAY	0	0
BOXING AND INLAY	0	1
CHARACTER MARK	1	0
ACTIVE AREA MARK	1	1

CURSOR DISPLAY MODE	MAT <sub>5</sub>	MAT <sub>4</sub>
FIXED COMPLEMENTED	0	0
FLASH COMPLEMENTED	1	0
FIXED UNDERLINED	0	1
FLASH UNDERLINED	1	1



NOTE : PROGRAMMING BIT VALUE  
 1 = True  
 0 = False

E88TS9347-29/1

## COMMAND TABLE

Type	Memo	Code				Parameter				Status			Arguments							Execution Time (1)	
		7	6	5	4	3	2	1	0	AI	LX <sub>m</sub>	LX <sub>s</sub>	R1	R2	R3	R4	R5	R6	R7	Write	Read
Indirect	IND	1	0	0	0	R/W	-	r	-	0	0	0	D	-	-	-	-	MP	2	3.5	
40 Characters - 24 Bits	TLM	0	0	0	0	R/W	0	0	1	X	X	0	C	B	A	-	-	MP	4	7.5	
40 Characters - 24 Bits	TLA	0	0	1	0	R/W	0	1	1	X	0	X	C	B	A	AP	-	-	4	7.5	
40 Characters - 16 Bits	TSM	0	1	1	0	R/W	0	0	1	X	X	0	A*	B*	-	-	-	MP	3	5.5	
40 Characters - 16 Bits	TSA	0	1	1	1	R/W	0	0	1	X	0	X	A*	B*	-	AP	-	-	3	5.5	
80 Characters - 8 Bits	KRS	0	1	0	0	R/W	0	0	1	X	X	0	C	-	-	-	-	MP	9	9.5	
80 Characters - 12 Bits	KRL	0	1	0	1	R/W	0	0	0	X	X	0	C	-	A	-	-	MP	12.5	11.5	
Byte	TBM	0	0	1	1	R/W	0	0	1	X	X	0	D	-	-	-	-	MP	4	4.5	
Byte	TBA	0	0	1	1	R/W	1	0	1	X	0	X	D	-	-	AP	-	-	4	4.5	
Move Buffer	MVB	1	1	0	1	s	s	a	a	0	0	0	W	-	-	AP	MP	(2) 2 + 4.n	-		
Move Double Buffer	MVD	1	1	1	0	s	s	a	a	0	0	0	W	-	-	AP	MP	(2) 2 + 8.n	-		
Move Triple Buffer	MVT	1	1	1	1	s	s	a	a	0	0	0	W	-	-	AP	MP	(2) 2 + 12.n	-		
Clear Page (4) - 24 Bits	CLL	0	0	0	0	0	1	0	1	X	X	0	C	B	A	-	-	MP	< 4700 (1 K code)	-	
Clear Page (4) - 16 Bits	CLS	0	1	1	0	0	1	0	1	X	X	0	A*	B*	-	-	-	MP	< 3500 (1 K code)	-	
Vertical Sync Mask Set	VSM	1	0	0	1	1	0	0	1	0	0	0	-	-	-	-	-	-	1	-	
Vertical Sync Mask Reset	VRM	1	0	0	1	0	1	0	1	0	0	0	-	-	-	-	-	-	1	-	
Increment Y	INY	1	0	1	1	0	0	0	0	0	0	0	-	-	-	-	Y	-	2	-	
No Operation	NOP	1	0	0	1	0	0	0	1	-	-	-	-	-	-	-	-	-	1	-	

s, s̄ : Source, Destination

01 : Source = MP ; Destination = AP

10 : Source = AP ; Destination = MP

a, a : Stop Condition

01 : Stop at End of Buffer

10 : No Stop

r : Indirect Register Number

- : Not Affected

W : Used as Working Register

X : Set or Reset Buffer

I : Pointer Incrementation

D : Data

MP : Main Pointer

AP : Auxiliary Pointer

(1) Unit : 12 clock periods (≈ 1 μs) without possible suspension.

(2) n : Total Number of Words ≤ 40

(3) These commands repeat TLM or KRO with Y incrementation When X overflows. When the last position is reached in a row Y is incremented and the progress starts again on the next row these command stop only. They can also be used to initialize the page 80 char/row by writing character pairs

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	0.3 to 7.0	V
$V_{in}$	Input Voltage	0.3 to 7.0	V
$T_A$	Operating Temperature Range	0 to 70	°C
$T_{stg}$	Storage Temperature Range	- 55 to 150	°C
$P_{Dm}$	Max Power Dissipation	0.75	W

\* With respect to  $V_{SS}$ .

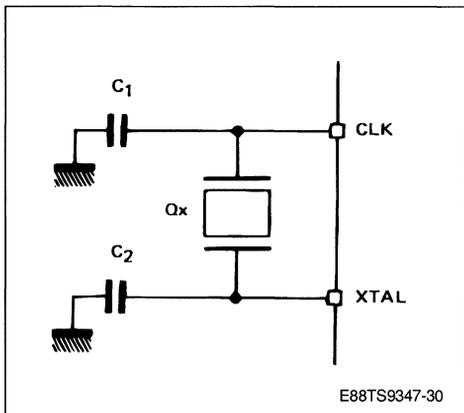
Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operations (sections of this specification

is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

**ELECTRICAL OPERATING CHARACTERISTICS**  $V_{CC} = 5.0 V \pm 5\%$ ,  $V_{SS} = 0$ ,  $T_{amb} = 0$  to  $70\text{ }^\circ\text{C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{CC}$	Supply Voltage	4.75	5	5.25	V
$V_{IL}$	Input Low Voltage	- 0.3	-	0.8	V
$V_{IH}$	Input High Voltage CLK (external CLK) Other Inputs	2.2 2	-	$V_{CC}$ $V_{CC}$	V -
$I_{in}$	Input Leakage Current	-	-	10	$\mu\text{A}$
$V_{OH}$	Output High Voltage ( $I_{load} = 500\text{ }\mu\text{A}$ )	2.4	-	-	V
$V_{OL}$	Output Low Voltage $I_{load} = 4\text{ mA}$ : AD (0:7), ADM (0:7) $I_{load} = 1\text{ mA}$ : Other Outputs Except Y	-	-	0.4	V
$P_D$	Power Dissipation	-	350	500	mW
$C_{in}$	Input Capacitance	-	-	15	pF
$I_{TSI}$	Three State (off state) Input Current	-	-	10	$\mu\text{A}$
$t_{start}$	Crystal Oscillator Start Time	-	-	1	ms

**ON CHIP OSCILLATOR**



**TYPICAL CRYSTAL PARAMETERS**

- Parallel resonance fundamental mode AT CUT
- $f = 12$  to  $15\text{ MHz}$
- $r_s = 30\text{ }\Omega$
- $C_s = 0,001\text{ pF}$
- $C_L \leq 7\text{ pF}$
- $C_1 = C_2 = 30\text{ pF}$

**MEMORY INTERFACE**

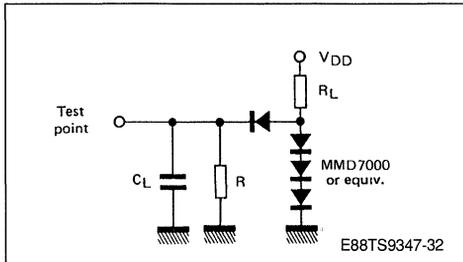
$V_{CC} = 5.0 V \pm 5\%$   $T_{amb} = 0^\circ$  to  $+70^\circ C$

Clock : Duty Cycle 40 to 60 % ;  $t_r, t_f < 5 ns$   $V_{IH} = 2.2 V$

Reference Levels :  $V_{IL} = 0.8 V$  and  $V_{IH} = 2 V$ ,  $V_{OL} = 0.4 V$  and  $V_{OH} = 2.4 V$

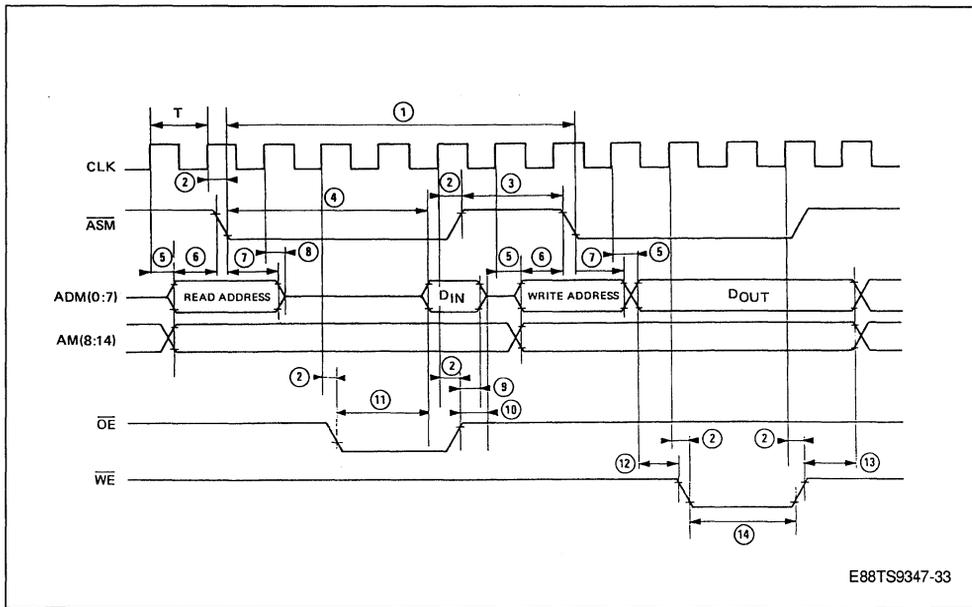
Ident. Number	Symbol	Parameter	$F_{in} = 12 MHz$		$F = 1/T$		Unit
			Min.	Max.	Min.	Max.	
1	$t_{E L E L}$	Memory Cycle Time	500		6 T		ns
2	$t_D$	Output Delay Time from CLK Rising Edge (ASM ; OE, WE)	-	60	-	60	ns
3	$t_{E H E L}$	ASM High Pulse Width	120	-	2 T - 33	-	ns
4	$t_{E L D V}$	Memory Access Time from $\overline{A S M}$ Low	-	250	-	4 T - 43	ns
5	$t_{D A}$	Output Delay Time from CLK Rising Edge ADM (0, 7), AM (8,14)	-	80	-	80	ns
6	$t_{A V E L}$	Address Setup Time to ASM	30	-	T - 49	-	ns
7	$t_{E L A X}$	Address Hold Time from ASM	55	-	T - 21	-	ns
8	$t_{C L A Z}$	Address off Time	-	80	-	80	ns
9	$t_{G H D X}$	Memory Hold Time	10	-	10	-	ns
10	$t_{O Z}$	Data off Time from $\overline{O E}$	-	60	-	T - 19	ns
11	$t_{G L D V}$	Memory $\overline{O E}$ Access Time	-	150	-	2 T - 16	ns
12	$t_{Q V W L}$	Data Setup Time (write cycle)	30	-	T - 49	-	ns
13	$t_{W H Q X}$	Data Hold Time (write cycle)	30	-	T - 49	-	ns
14	$t_{W L W H}$	$\overline{W E}$ Pulse Width	110	-	2 T - 48	-	ns

**TEST LOAD**



	ADM (0.7) AD (0.7)	Other Outputs Except Y
C	100 pF	50 pF
$R_L$	1 k $\Omega$	3.3 k $\Omega$
R	4.7 k $\Omega$	4.7 k $\Omega$

MEMORY INTERFACE TIMING DIAGRAM



**MICROPROCESSOR INTERFACE**

TS9347 is MOTEL compatible. It automatically selects the processor type by using AS input to latch to state of the DS input.

No external logic is needed to adapt bus control signals from most of the common multiplexed bus microprocessors.

TS9347	6801	INTEL Family
	Timing 1	Timing 2
AS DS R/W	AS DS, E <sub>1</sub> , $\emptyset$ 2 R/W	ALE RD WR

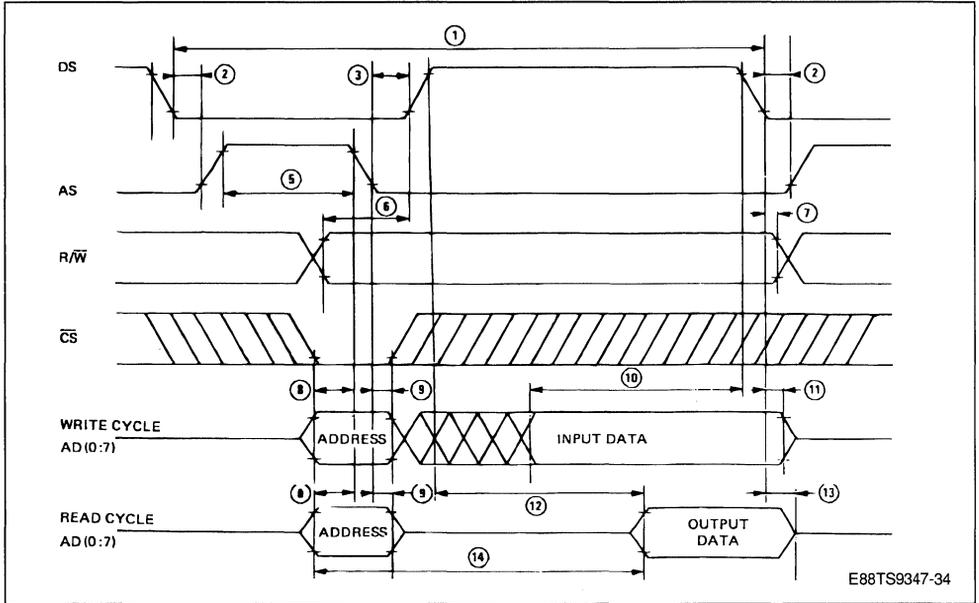
**MICROPROCESSOR INTERFACE TIMING AD (0:7), AS, DS, R/W, CS**

V<sub>CC</sub> = 5.0 ± 5 %, T<sub>A</sub> = 0° to 70 °C, C<sub>L</sub> = 100 pF on AD (0 : 7)

Reference Levels : V<sub>IL</sub> = 0.8 V and V<sub>IH</sub> = 2 V on All Inputs ; V<sub>OL</sub> = 0.4 V and V<sub>OH</sub> = 2.4 V on All Outputs.

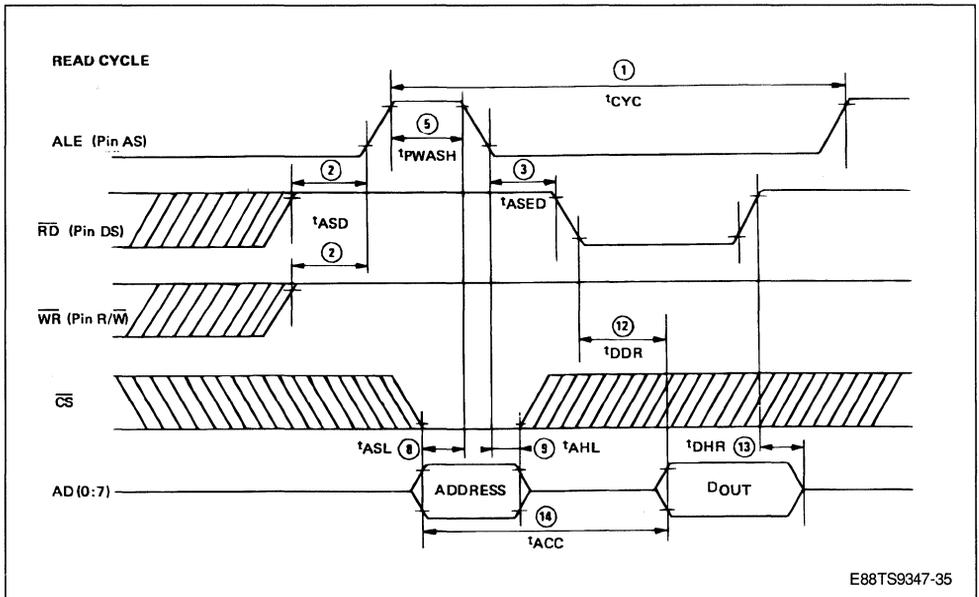
Ident. Number	Symbol	Parameter	Min.	Typ.	Max.	Unit
1	t <sub>CYC</sub>	Cycle Time	400	-	-	ns
2	t <sub>ASD</sub>	DS Low to AS High (timing 1) DS High or R/W High to AS High (timing 2)	26	-	-	ns
3	t <sub>ASED</sub>	AS Low to DS High (timing 1) AS low to DS LOW or R/W Low (timing 2)	30	-	-	ns
4	t <sub>PWEH</sub>	Write Pulse Width	200	-	-	ns
5	t <sub>PWASH</sub>	AS Pulse Width	93	-	-	ns
6	t <sub>RWS</sub>	R/W to DS Setup Time (timing 1)	100	-	-	ns
7	t <sub>RWH</sub>	R/W to DS Hold Time (timing 1)	10	-	-	ns
8	t <sub>ASL</sub>	Address and CS Setup Time	20	-	-	ns
9	t <sub>AHL</sub>	Address and CS Hold Time	20	-	-	ns
10	t <sub>DSW</sub>	Data Setup Time (write cycle)	100	-	-	ns
11	t <sub>DHW</sub>	Data Hold Time (write cycle)	10	-	-	ns
12	t <sub>DDR</sub>	Data Access Time from DS (read cycle)	-	-	150	ns
13	t <sub>DHR</sub>	DS Inactive to high Impedance State Time (read cycle)	10	-	63	ns
14	t <sub>ACC</sub>	Address to Data Valid Access Time	-	-	300	ns

MICROPROCESSOR INTERFACE TIMING DIAGRAM 1 (6801)

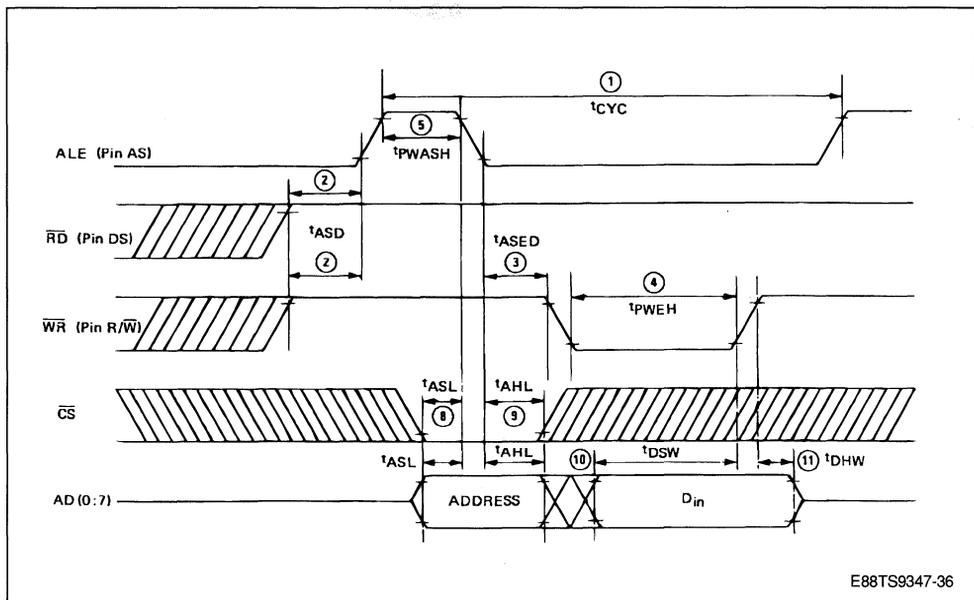


MICROPROCESSOR INTERFACE TIMING DIAGRAM 2 (INTEL type)

READ CYCLE



WRITE CYCLE



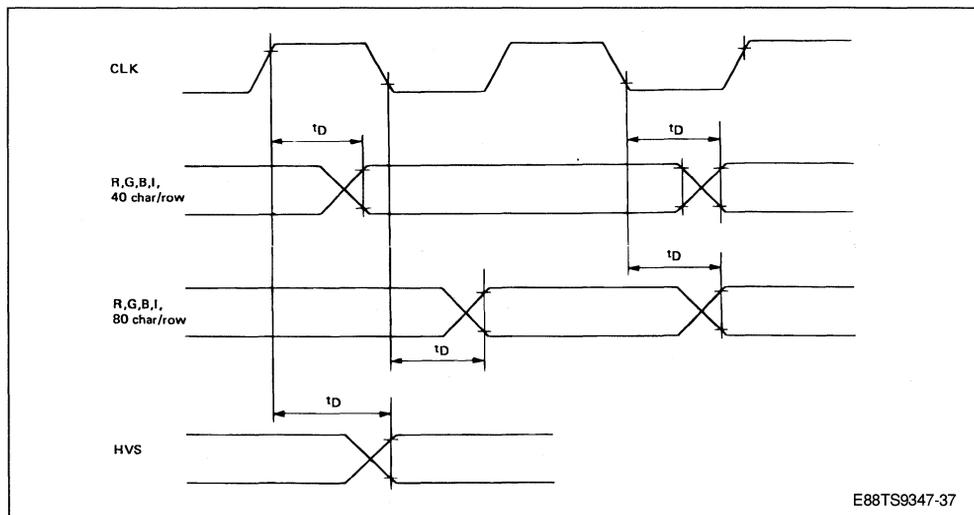
E88TS9347-36

VIDEO INTERFACE R.G.B.I.

$V_{CC} 5.0 V \pm 5\%$   $T_{amb} 0^\circ$  to  $+70^\circ C$  CLK Duty Cycle 50%.  $C_L 50 pF$

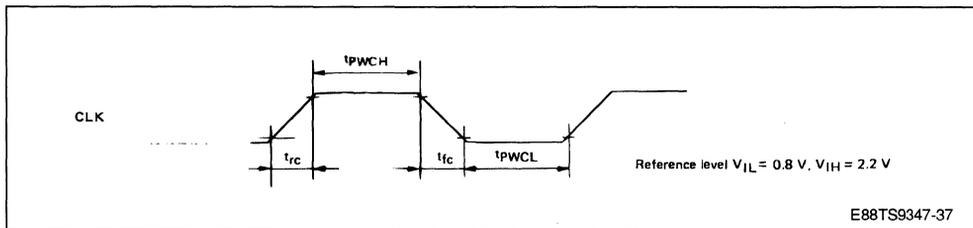
Reference Levels :  $V_{IL} = 0.8 V$  and  $V_{IH} = 2.2 V$  on CLK Input  $V_{OL} = 0.4 V$  and  $V_{OH} = 2.4 V$  All Outputs

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_D$	Output Delay from CLK Edge	-	-	60	ns

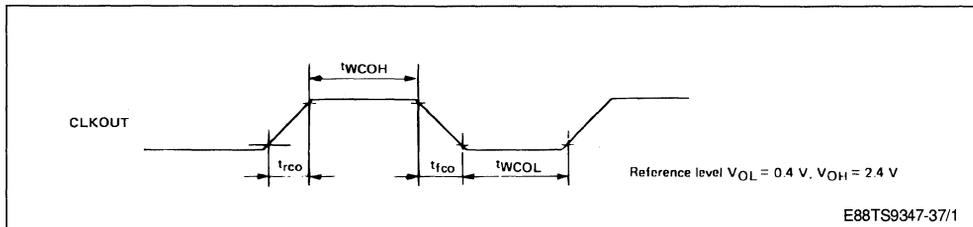


E88TS9347-37

**INPUT CLK** (case of external CLK generation)



**INPUT CLK** (case of internal oscillator – fin = 12MHz)



Symbol	Parameter	Min.	Max.	Unit
tPWCH	CLK High Pulse Width	25	-	ns
tPWCL	CLK Low Pulse Width	25	-	ns
trc, tfc	CLK Rise and Fall Time	-	10	ns
tWCOH	CLKOUT High Pulse Width	20	-	ns
tWCOL	CLKOUT Low Pulse Width	20	-	ns
trco, tcco	CLKOUT Rise and Fall Time	-	20	ns

**Y OUTPUT** : Composite Luminance.

**REFERENCE LEVEL**

$V_{DDC} = V_{DD} = 5 V$  ;  $V_{SSC} = V_{SS} = 0 V$

G	R	B	Signal	Level
0	0	0	SYNC	0.06 V
0	0	0	BLACK	0.50 V
0	0	1	BLUE	0.80 V
0	1	0	RED	0.92 V
0	1	1	MAGENTA	1.03 V
1	0	0	GREEN	1.15 V
1	0	1	CYAN	1.26 V
1	1	0	YELLOW	1.38 V
1	1	1	WHITE	1.50 V

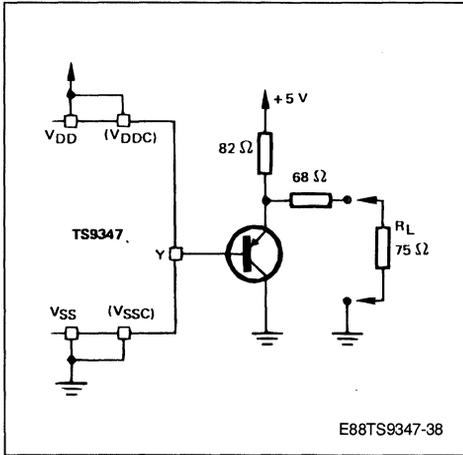
**ELECTRICAL SPECIFICATION**

Over Full Temperature Range :  $V_{DDC} = V_{DD} = 5\text{ V}$  (see note 1)  
 $V_{SSC} = V_{SS} = 0\text{ V}$  ;  $C_L = 20\text{ pF}$ ,  $R_L > 100\text{ K}$  to  $V_{SS}$  or  $V_{DD}$

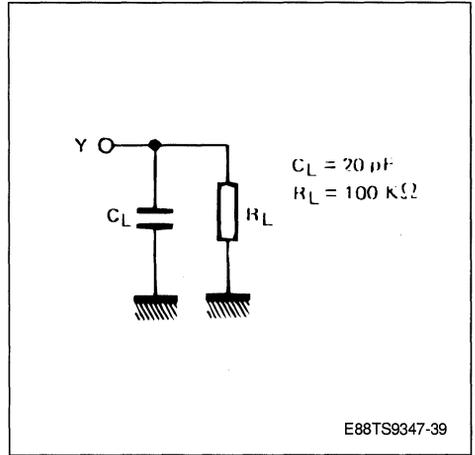
Parameter	Min.	Typ.	Max.	Unit
Monotonicity	Guaranteed			
Output Level Dispersion	-	10	50	mV
Propagation Delay (clock edge to 50 % output)	-	-	60	ns
Rise and Fall Time (10 – 90 %)	-	-	30	ns
Output Static Impedance	-	-	600	$\Omega$

Note : 1. The DAC is a 9 output potentiometric divider : therefore, each voltage variation on  $V_{DDC}$  is repercutated on the output with the same relative value with respect to  $V_{SSC}$ .

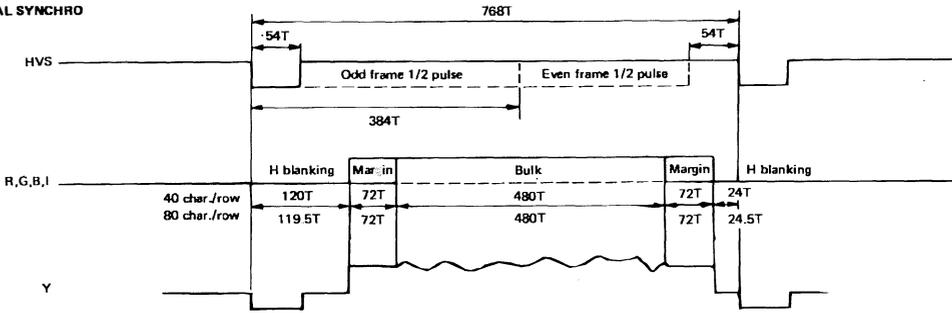
**TYPICAL APPLICATION**



**TEST CONDITION**

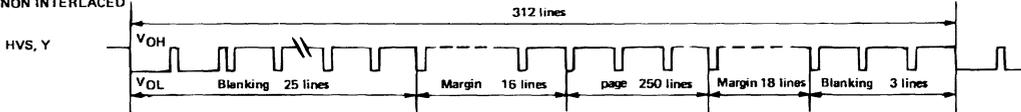


HORIZONTAL SYNCHRO

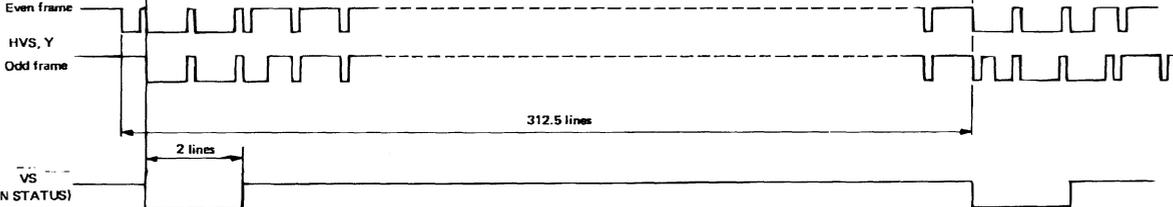


VERTICAL SYNCHRO

NON INTERLACED



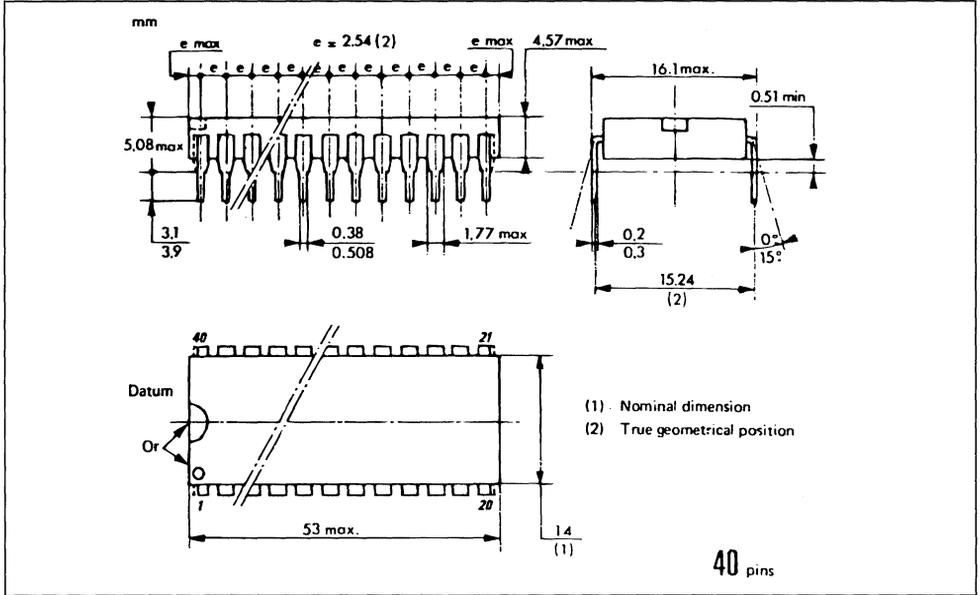
INTERLACED



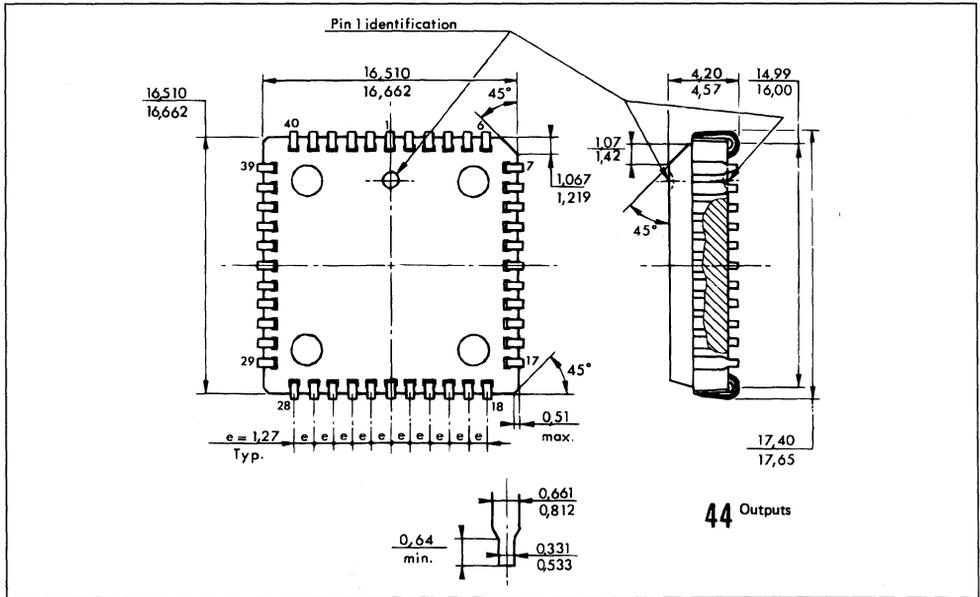
E88TS9347-40

PACKAGE MECHANICAL DATA

40 PINS – PLASTIC DIP



44 PINS – PLASTIC LEADED CHIP-CARRIER



# **GRAPHICS CONTROLLERS**



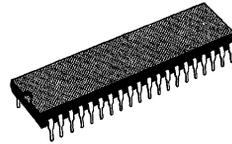
## MOS GRAPHIC DISPLAY PROCESSOR (GDP)

- SELECTABLE RESOLUTIONS IN BLACK AND WHITE OR COLOR :
  - EF9365** : 512 x 512 (interlaced scan)  
256 x 256, 128 x 128, 64 x 64 (non interlaced scan)
  - EF9366** : 512 x 256 (non interlaced scan)
- HIGH SPEED VECTOR PLOT WELL SUITED TO ANIMATION (up to 1 500 000 dots/s. and an average value of 900 000 dots/s.) 4 TYPES OF LINES.
- MULTIPLEXED ADDRESS AND REFRESH FOR 16 K OR 64 K DYNAMIC RAMs
- NO LIMITATION ON THE NUMBER OF SELECTABLE MEMORY PLANES (colors, grey levels or any other attributes)
- MULTIPAGE APPLICATION CAPABILITY
- ON-CHIP FULL ASCII CHARACTER GENERATOR (96) MAXIMUM ALPHANUMERIC SCREEN DENSITY : 85 x 57 - PROGRAMMABLE SIZES AND ORIENTATIONS
- DIRECT INTERFACING WITH THE MONITOR THROUGH THE COMPOSITE SYNCHRO AND BLANKING SIGNALS
- AUTOMATIC ALLOCATION OF DISPLAY MEMORY IN REFRESH, WRITE, DUMP, AND DISPLAY CYCLES
- LIGHT PEN REGISTERS AND CONTROL SIGNALS
- THREE TYPES OF INTERRUPT REQUESTS
- FULLY STATIC DESIGN
- TTL COMPATIBLE I/O
- SINGLE + 5 VOLT SUPPLY.

### DESCRIPTION

The GDP is a true high resolution graphic display processor, which contains all the functions required to process vector generation at a very high speed and to generate all the timing signals required for interfacing interlaced or non interlaced video data on a raster scan CRT display compatible with the CCIR 625 line 50 Hz standard.

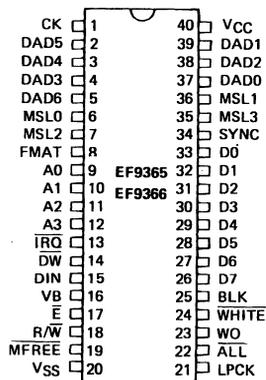
The GDP flexibility results from its direct interfacing with any 8 bit MPU bus and its 11 internal registers.



**P**  
**DIP 40**  
 (Plastic Package)

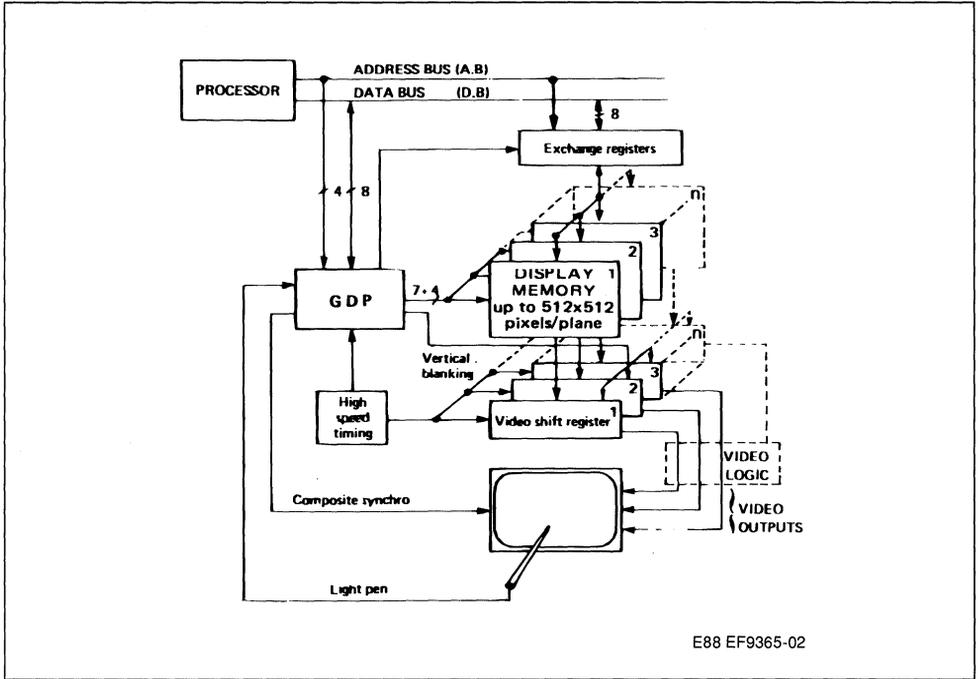
**ORDER CODE** : EF9365P  
 EF9366P

### PIN CONNECTIONS

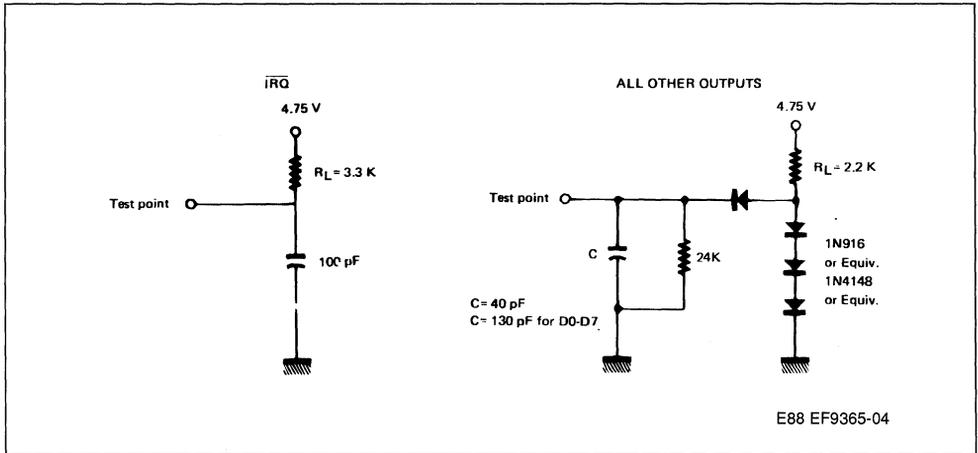


E88 EF9365-01

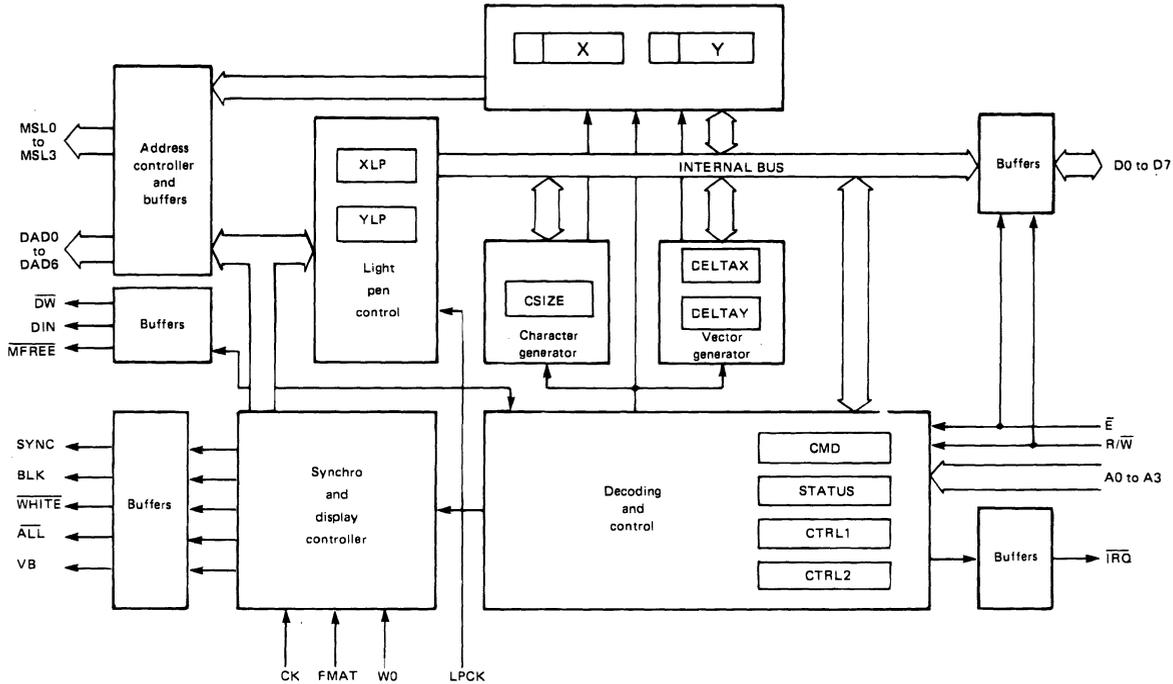
TYPICAL APPLICATION



TEST LOADS



BLOCK DIAGRAM



E88 EF9365-03

**GENERAL DESCRIPTION**

Developed using NMOS technology, the GDP is an intelligent raster scan video display controller, fully programmable via an eight-bit microprocessor bus. Besides all the timing logic functions required to generate the video, sync and blanking signals, the GDP includes two hardwired display processors : a vector and a character generator.

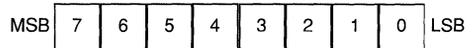
This unique feature allows an ultrafast screen writing speed (the 512 dot diagonal may be written in less than 700  $\mu$ s) at almost no microprocessor processing cost.

The GDP is particularly well-suited to all applications in which the display memory is not directly addressed by the MPU. This feature allows a total asynchronism between the MPU and the GDP memory cycles and preserves the whole MPU memory addressing space.

Nevertheless, where direct exchange between the microprocessor and the memory is necessary, the on-chip allocation controller will allow this exchange without display interference.

The GDP is programmable using 11 internal registers occupying 16 consecutive addresses. These registers can also be modified by the GDP's hardwired processors while a command is being executed.

**Note** : A summary of data codes and registers is given in the Register address table. Hexadecimal values are subscripted 16 and the register bits are numbered as follows :



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	- 0.3 to + 7.0	V
$V_{in}$	Input Voltage	- 0.3 to + 7.0	V
$T_A$	Operating Temperature	0 to + 70	$^{\circ}$ C
$T_{stg}$	Storage Temperature	- 55 to + 150	$^{\circ}$ C

The GDP inputs are protected against high static voltages and electric fields ; nevertheless, normal precautions should be taken to avoid voltages above the limit values on this high impedance circuit.

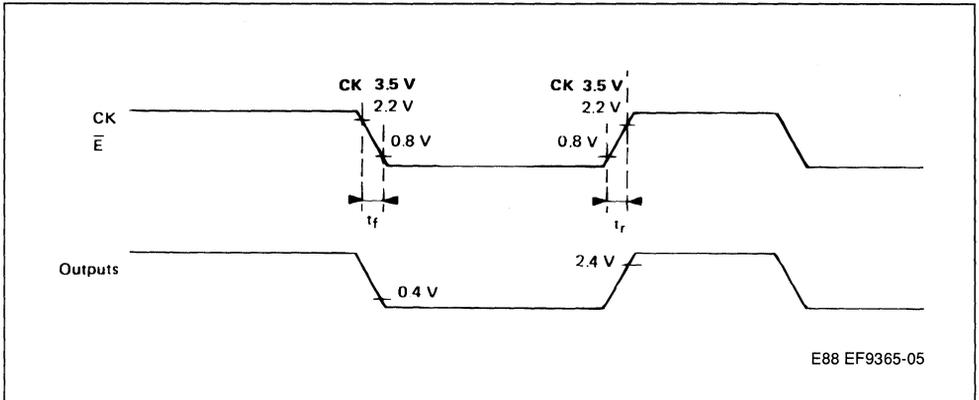
**STATIC ELECTRICAL PARAMETERS** ( $V_{CC} = 5 V \pm 5 \%$ ,  $V_{SS} = 0$ ,  $T_A = 0$  to  $70^{\circ}$  C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{IH}$	Input High Voltage Except CK	$V_{SS} + 2.2$	-	$V_{CC}$	V
$V_{IHCK}$	Input High Voltage CK	$V_{SS} + 3.5$	-	$V_{CC}$	V
$V_{IL}$	Input Low Voltage	$V_{SS} - 0.3$	-	$V_{SS} + 0.8$	V
$I_{in}$	Input Leakage Current ( $V_{in} = 0$ to $5.25 V$ , $V_{CC} = \max$ )	-	1.0	2.5	$\mu$ A
$V_{OH}$	Output High Voltage ( $I_{load} = - 100 \mu A$ , $V_{CC} = \min$ )	$V_{SS} + 2.4$	-	-	V
$V_{OL}$	Output Low Voltage ( $I_{load} = 1.6 mA$ , $V_{CC} = \min$ )	-	-	$V_{SS} + 0.4$	V
$I_{CC}$	Supply Current $\bar{f}$	-	80	-	mA
$C_{in}$	Capacitance ( $V_{in} = 0$ , $T_A = + 25^{\circ}$ C, $f = 1.0 MHz$ )	-	-	12	pF
$C_{out}$		-	-	12	pF

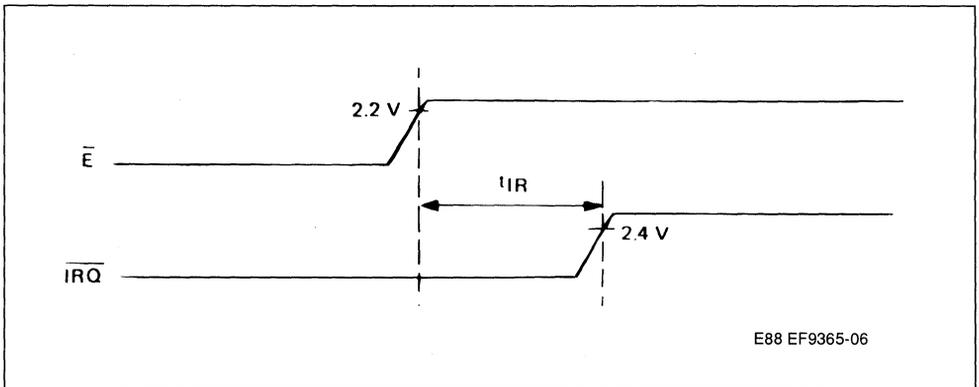
**DYNAMIC OPERATING CONDITIONS** ( $V_{DD} = 5.0\text{ V} \pm 5\%$  ;  $T_A = 0\text{ to } +70\text{ }^\circ\text{C}$  unless otherwise noted)

Symbol	Time (ns)	Min.	Max.
$t_{CK}$	Clock Period	560	
$t_{CLK}$	CK Pulse Width, Low	330	
$t_{CKH}$	CK Pulse Width, High	190	
CKLDAD	CK Low to Valid DAD		320
CKHDAD	CK High to Valid DAD		180
CKLSYNC	CK Low to Valid SYNC		300
CKLCLK	CK Low to Valid CLK		310
CKLVB	CK Low to Valid VB		500
CKLALL	CK Low to Valid $\overline{\text{ALL}}$		300
CKLMSL	CK Low to Valid MSL		300
CKLDW	CK Low to Valid $\overline{\text{DW}}$		310
CKLMFR	CK Low to Valid $\overline{\text{MFR}}$		500
CKLDIN	CK Low to Valid DIN		310
CKLIRQ	CK Low to Valid IRQ		1500
CKLWHI	CK Low to Valid WHITE		530
$t_{EL}$	$\overline{\text{E}}$ Pulse Width, Low	450	
$t_{EH}$	$\overline{\text{E}}$ Pulse Width, High	430	
$t_{AS}$	Address Pre-Setup Time	160	
$t_{AH}$	Address Hold Time	10	
$t_{DSW}$	Data Pre-Setup Time (write)	260	
$t_{DDR}$	Data Setup Time (read)		320
$t_{DHR}$	Data Hold Time (read)	10	
$t_{IR}$	IRQ Release Time		1600
LPHW	LPCK High to $\overline{\text{WHITE}}$ High (if command 08 <sub>16</sub> )		1600
LPHIRQ	LPCK High to IRQ Low		1600
$t_{PCKH}$	LPCK High Hold Time	150	
$t_r$	CK and $\overline{\text{E}}$ Rise Times		20
$t_f$	CK and $\overline{\text{E}}$ Fall Times		20

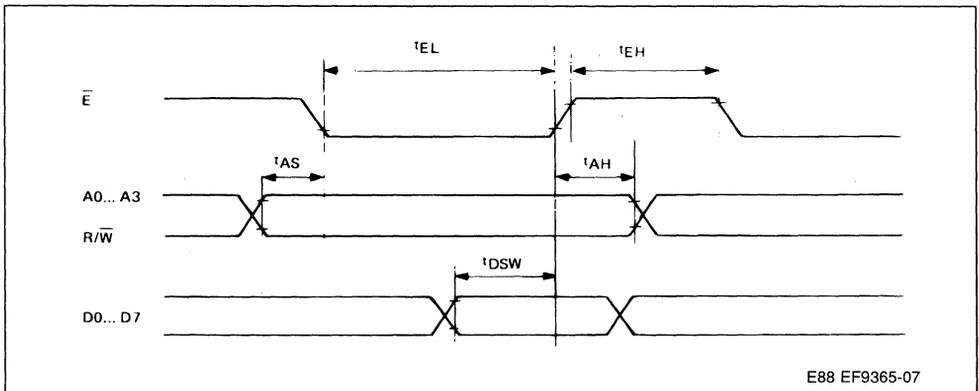
CLOCK AND OUTPUT CHARACTERISTICS



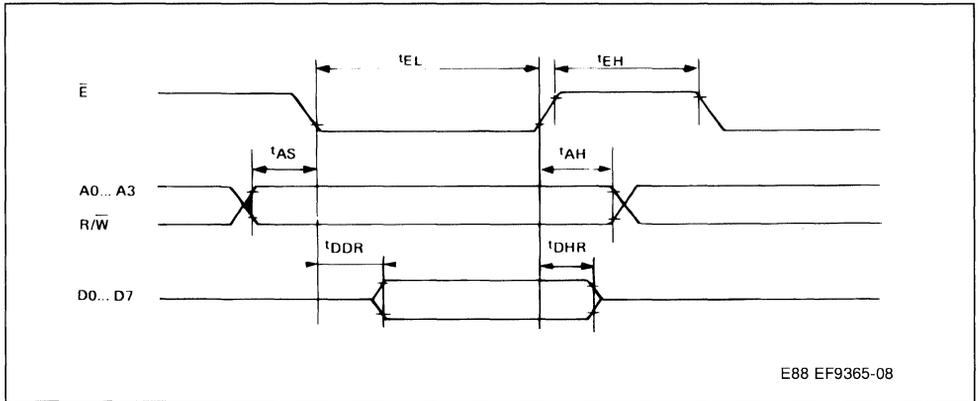
IRQ RELEASE TIME



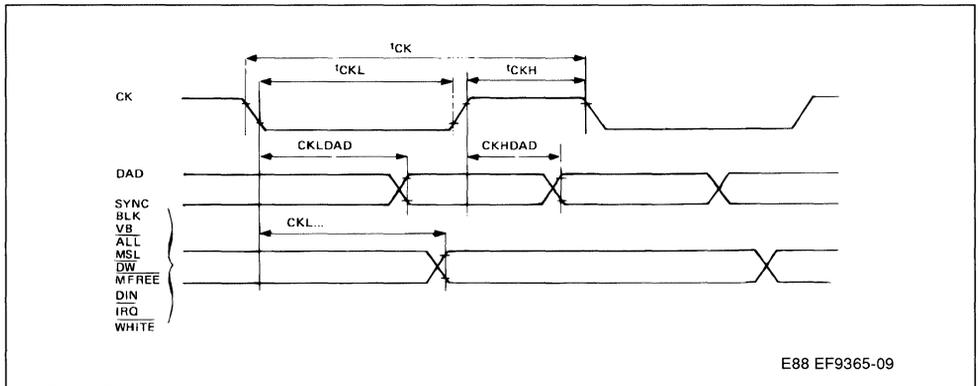
MICROPROCESSOR BUS, WRITE ACCES



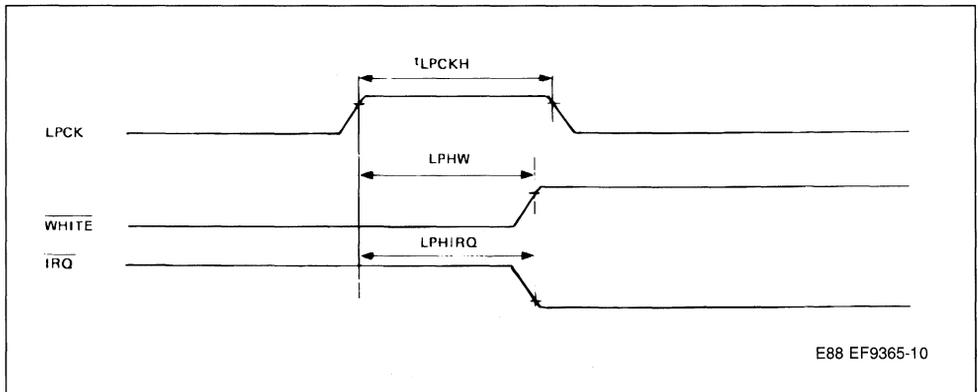
**MICROPROCESSOR BUS, READ ACCESS**



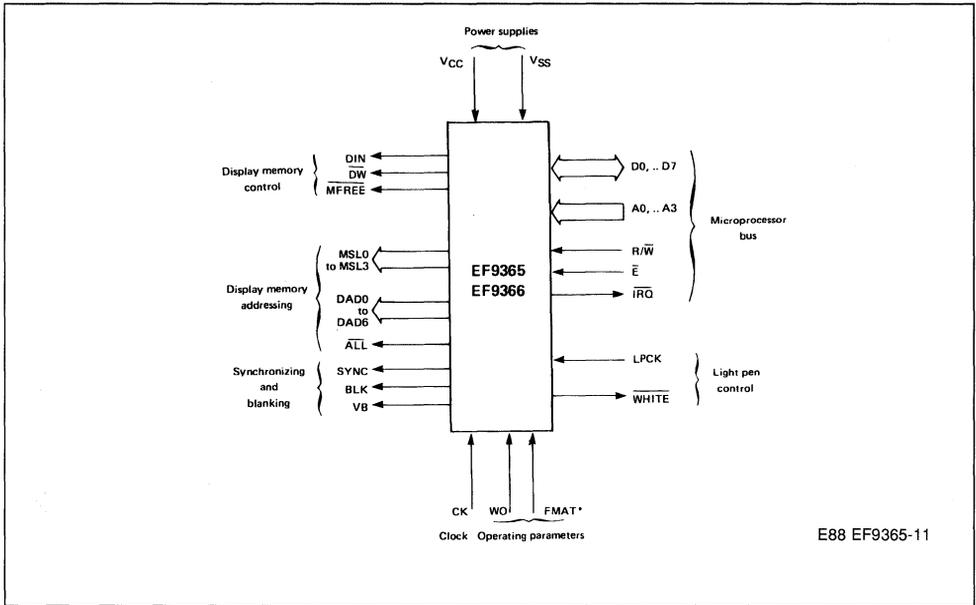
**SYNCHRONOUS SIGNALS WITH CK INPUT**



**LIGHT PEN SIGNALS**



PIN DESCRIPTION



\* FMAT should be connected to V<sub>CC</sub> in the EF9366.

POWER SUPPLY, CLOCK AND OPERATING PARAMETERS

Name	Pin Type	N°	Function	Description
V <sub>SS</sub>	S	20	Power Supply	Ground
V <sub>CC</sub>	S	40	Power Supply	+ 5 V
CK	I	1	Clock	Master Clock. All internal processor states are modified on the falling edge of this signal. The whole circuit logic is static and the cycle of this clock needs only to be adjusted according to the shape and accuracy the synchronizing signals should feature. DAD Memory Address Multiplexing Signal. If CK is low, low addresses (or row addresses for the memory) are those that are output on DAD. For SYNC to be in compliance with the applicable CCIR standards (FMAT high) the input frequency on CK should be 1.750 MHz. If FMAT is low or for the EF9366, the frame frequency equals 50 Hz provided that the input frequency on CK is 1.7472 MHz.
FMAT	I	8	Format	EF9365 should be connected to V <sub>CC</sub> for a 512 line vertical resolution (interlaced scan) and to V <sub>SS</sub> for 256 lines or less (non-interlaced scan). The shape of the synchronizing signals, the address distribution on DAD and the MSL output functions are changed by this input.  EF9366 : not used (should be connected to V <sub>CC</sub> ).
WO	I	23	Write Only	When WO is high, memory refresh nor display no longer exist. The hard wired write processors may operate without being interrupted. The ALL signals is always high.

## SYNCHRONIZING AND BLANKING SIGNALS

Sync	O	34	Video Monitor Synchronizing	Video Monitor Line and Frame Sync Signal. The SYNC signal complies with CCIR 625-line 50 Hz standard provided the CK frequency is 1.750 MHz and FMAT is high. If FMAT is low or for the EF9366, the frames are no longer interlaced and all comprise 312 lines. This output is not affected by the WO input and CTRL1 register.
BLK	O	25	Blanking	This signal is high apart the display window (writing or refresh). It is always high if bit 2 in register CTRL1 is high, but it is not affected by the WO input.
VB	O	16	Vertical Blanking	This signal is not affected by WO and register CTRL1. High during vertical blanking.

## DISPLAY MEMORY ADDRESSING SIGNALS

DAD0 to DAD6	O	37, 39, 38, 43, 2, 5	Display Address	Addresses that are multiplexed by the CK signal. Provided for the Automatic Refresh of the 16 K or 64 K Dynamic Memories.
MSL0 to MSL3	O	6, 36, 7, 35	Memory Select	Pixel write select signals (see section : <b>display memory configuration</b> ).
ALL	O	22	Access to all Memory Units	This signal makes it possible to discriminate between the collective memory accesses to all chips (display, refresh or erase), and the memory accesses to a single pixel for a vector or character writing purposes. This signal is low for collective access.

## DISPLAY MEMORY CONTROL SIGNALS

DIN	O	15	Display In	Selection of the memory data code corresponding to the display screen in the 'off' condition (active when high). For a black-and-white display (1 bit per pixel), DIN may directly be the storage entry data.
DW	O	14	Display Write	Display memory write signal. Active when Low
MFREE	O	19	Memory Free	Signal low during the next memory idle period following the OF <sub>16</sub> command. This signal allows exchanges between the microprocessor and the X and the Y flagged memory segment without affecting the display.

## MICROPROCESSOR BUS SIGNALS

D0-D7	I/O	33 to 26	Data Bus	I/O buffers opening is controlled through $\bar{E}$ , and the related direction through R/W.
A0/A3	I	9 to 12	Address Bus	Address of the register involved in microprocessor access.
R/W	I	18	Read/Write Signal	Read/Write Signal. Write when Low.
$\bar{E}$	I	17	Enable	Bus exchange synchronizing and enabling signal.
IRQ	O	13	Interrupt Request	Interrupt request towards the microprocessor, programmable through register CTRL1. Open Drain Output

**LIGHT PEN OPERATING SIGNALS**

WHITE	O	24	Forcing to White Level	Forces white level on video signal, for use of the light pen. Active when Low.
LPCK	I	21	Light Pen Strobe	Light Pen Input. When the mechanism is set, a rising edge loads into registers XLP and YLP the current display address and sets the XLP register's LSB high.

**REGISTER DESCRIPTION**

X AND Y REGISTERS (Addresses : 8<sub>16</sub>, 9<sub>16</sub>, A<sub>16</sub>, B<sub>16</sub>)

The X and Y registers are 12-bit read-write registers. They indicate the position of the next dot to be written into the display memory. They have no connection at all with the video signal generating scan, but they point the write address, in the same way as the pen address on a plotter.

These 2 registers are incremented or decremented, prior to each write operation into the display memory, by the internal vector and character generators, or they may be directly positioned by the microprocessor.

This 2 x 12 bit write address covers a 4096 x 4096 point addressing space. Only the LSBs are used here, since the maximum definition of the picture actually stored is 512 x 512 pixels (picture elements).

The MSBs are either ignored or used to inhibit writing where the actual screen is regarded as being a window within a 4096 x 4096 space.

The above features along with the relative mode description of all picture component elements make it possible to automatically solve the great majority of edge cut-off problems.

DELTAX AND DELTAY REGISTERS (Addresses : 5<sub>16</sub>, 7<sub>16</sub>).

The DELTAX and DELTAY registers are 8-bit read-write registers. They indicate to the vector generator the projections of the next vector to be plotted, on the X and Y axes respectively. Such values are unsigned integers. The plotting of a vector is initiated by a write operation in the command register (CMD).

CSIZE REGISTER (Address : 3<sub>16</sub>)

The CSIZE register is an 8-bit read-write register. It indicates the scaling factors of X and Y registers for the symbols and characters. 98 characters are generated from a 5 x 8 pixel matrix defined by an internal ROM. In the standard version, it contains the alphanumeric characters in the ASCII code which may be printed, together with a number of special symbols.



Each symbol can be increased by a factor P(X) or Q(Y). These factors are independent integers which may each vary from 1 to 16 and which are defined by the CSIZE register. The symbol generation sequence is started after writing the ASCII code of the symbol to be represented in the CMD register.

CTRL1 REGISTER (Address : 1<sub>16</sub>).

The CTRL1 register is a 7-bit read-write register, through which the general circuit operation may be fed with the required parameters.

Bit 0 : When low, this bit inhibits writing in display memory (equivalent to pen or eraser up).

When high, this bit enables writing in display memory (pen or eraser down).  
This bit controls the DW output.

Bit 1 : When low, this bit selects the eraser.

When high, this bit selects the pen.  
This bit controls the DIN output.

Bit 2 : When low, this bit selects normal writing mode (writing apart from the display and refresh periods, which are a requirement for the dynamic storages) in display memory.

When high, this bit selects the high speed writing mode : the display periods are deleted. Only the dynamic storage refresh periods are retained.

Bit 3 : When low, this bit indicates that the 4096 x 4096 space is being used (the 12 X and Y bits are significant).

When high, this bit selects the cyclic screen operating mode.

Bit 4 : When low, this bit inhibits the interrupt triggered by the light pen sequence completion.

When high, this bit enables the interrupt.

Bit 5 : When low, this bit inhibits the interrupt release by vertical blanking.

When high, this bit enables the interrupt.

Bit 6 : When low, this bit inhibits the interrupt indicating that the system is ready for a new command.

When high, this bit enables the interrupt.

Bit 7 : Not used. Always low in read mode.

#### CTRL2 REGISTER (Address : 2<sub>16</sub>)

The CTRL2 register is a 4-bit read/write register, through which the plotting of vectors and characters may be denoted by parameters.

Bit 0, 1 : These 2 bits define 4 types of lines (continuous, dotted, dashed, dash-dotted).

Bit 2 : When low, this bit defines straight writing.  
When high, it defines tilted characters.

Bit 3 : When low, this bit defines writing along an horizontal line.  
When high, this bit defines writing along a vertical line.

Bit 4, 5, 6, 7 : Not used. Always low in read mode.

#### CMD COMMAND REGISTER (Address : 0<sub>16</sub>)

The CMD register is an 8-bit write-only register. Each write operation in this register causes a command to be executed, upon completion of the time necessary for synchronizing the microprocessor access and the GDP's CK clock.

Several types of command are available :

- vector plotting
- character plotting
- screen erase
- light pen circuitry setting
- access to the display memory through an external circuitry.
- indirect modification of the other registers (commands that make it possible for the X, Y, DELTAX, DELTAY, CTRL1, CTRL2 and CSIZE registers to be amended or scratched).

#### STATUS REGISTER (Address 0<sub>16</sub>)

The STATUS register is an 8-bit read-only register. It is used to monitor the status of the executing statements entered into the circuit, and more specifically to avoid the need for modifying a register that is already used for the command currently executing.

Bit 0 : When low, this bit indicates that a light pen sequence is currently executing.  
When high, it indicates that no light pen sequence is currently executing.

Bit 1 : This bit is high during vertical blanking. It is the VB signal recopy.

Bit 2 : When low, this bit indicates that a command is currently executing.

When high, this bit indicates that the circuit is ready for a new command.

Bit 3 : When low, this bit indicates that the X and Y registers point within the display window.

When high, this bit indicates that the X and Y registers are pointing outside the memory display.

This bit is the logic OR of the unused MSBs of the X and Y registers.

Bit 4 : When high, this bit indicates that an interrupt has been initiated by the completion of a light pen running sequence. Such an interrupt is enabled by bit 4 in CTRL1 register.

Bit 5 : When high, this bit indicates that an interrupt has been initiated by vertical blanking. Such an interrupt is enabled by bit 5 in CTRL1 register.

Bit 6 : When high, this bit indicates that an interrupt has been initiated by the completion of execution of a command. Such an interrupt is enabled by bit 6 in CTRL1 register.

Bit 7 : When high, this bit indicates that an interrupt has been initiated. It is the logic OR of bits 4, 5 and 6 in STATUS register. The IRQ output state is always the opposite of the status of this bit.

**Note :** Bits 4, 5, 6 and 7 are reset low by a read of the STATUS register.

#### XLP AND YLP REGISTERS (Addresses C<sub>16</sub> and D<sub>16</sub>)

The XLP and YLP registers are read-only registers, with 7 and 8 bits respectively. Upon completion of a light pen running sequence, they contain the display address sampled by the first edge appearing rising on the LPCK input. The use of such registers is discussed in section : **Use of light pen circuitry.**

**Notes : 1.** All internal registers may be read or written at any time by the microprocessor. However, the precautions outlined below should be observed :

- Do not write into the CMD register if execution of the previous command is not completed (bit 2 of STATUS register).
- Do not alter any register if it is used as an input parameter for the internal hardwired systems (e. g. : modifying the DELTAX register while a vector plotting sequence is in progress).
- Do not read a register that is being asynchronously modified by the internal hardwired systems (e. g. : rea-

ding the X register while a vector plotting sequence is in progress may be erroneous if CK and  $\bar{E}$  are asynchronous).

**Note : 2.** On powering up, the writing devices may have any status. Before entering a

command for the first time, it is necessary to wait until all functions currently underway are completed, which information can be derived from the STATUS register.

**SYSTEM OPERATING PRINCIPLE**

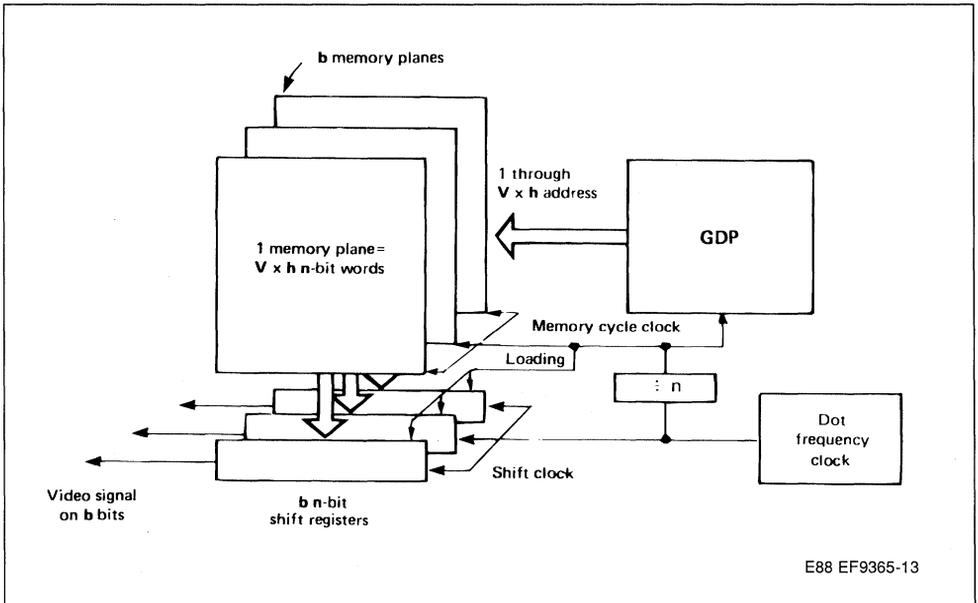
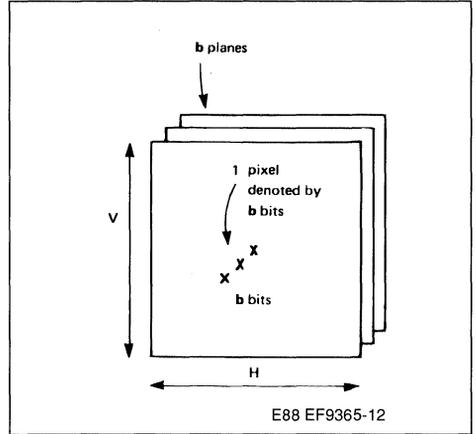
**DISPLAY MEMORY CONFIGURATION**

Assume a  $V \times H$  pixel picture. Assume that each pixel is able to adopt  $2^b$  different states. A  $V \times H \times b$  bit display memory is thus required.

In those applications where  $H$  features a high value, the video signal frequency exceeds the maximum frequency of memory read access.

Example :  $H = 512$  with a television line frequency : the pixel succession period on the video signal is 70 ns.

It is mandatory that a line of  $H$  dots be cut into  $h$  adjoining segments of  $n$  bits each, read at the same time in the display memory, and thereafter converted to serial form to produce the video signal.  $h$  memory accesses per line are necessary. Each access loads  $b n$ -bit shift registers. The memory contains  $V \times h \times b n$ -bit words.



EF9365

The EF9365 circuit is designed to accommodate the following picture formats :

- 1.  $V = H = 512$  or a lower of 2
- 2.  $h = 64$
- 3.  $n = 8, 4, 2$  or 1
- 4. Any value for  $b$  (the addressing is similar for all memory planes. These planes are managed outside the actual circuit).

Circuit operation in the various formats outlined above occurs as described below :

**512 x 512 pixel format (V = 512, h = 64, n = 8).**

The FMAT input should be high. The memory is made up of  $V \times h$  bytes = 32 K bytes per memory plane.

The byte address is made up of 15 bits :

- 14 are output in 2 runs on the DAD pins for the purpose of using 16 K x 1 bit dynamic RAMs,
- the 15th one is output on pin MSL3.

The 3 MSL0, 1 and 2 outputs allow to select one pixel out of the 8 featuring the same address, for pixel-to-pixel write applications. They issue the number of the involved pixel, encoded on 3 bits.

**256 x 256 pixel format (V = 256, h = 64, n = 4).**

The FMAT input should be low. The memory is made up of  $V \times h \times n$  bits, i. e. 16 K 4-bit words. The address of a 4-bit word is made up of 14 bits, which are output in 2 runs on the DAD pins.

Each of the 4 MSL pins is used to select one pixel in a 4-bit word for writing purposes. The 2 LSBs in the horizontal writing address are decoded before being output on the MSL pins. Such outputs are active when low.

**Format less than 256 x 256 pixels (V = 128 or 64, h = 64, n = 2 or 1).**

Such formats are achieved in the same way as for the 256 x 256 pixel format discussed above. Unrequired address bits are output on DAD7.

EF9366

The EF9366 circuit is designed to accommodate a (512 x 256) picture format : **V = 256, H = 512, h = 64, n = 8, b = any value.**

The memory is made up of 16 K bytes per memory plane. The byte address is made up of 14 bits which are output in two runs on the DAD pins. The 3 MSL0, MSL1, MSL2 outputs are used to select one pixel out of the 8 featuring the same address. They issue the number of the pixel, encoded on 3 bits. MSL3 is high, and is not used.

SIGNALS OUTPUT THROUGH THE DAD AND MSL PINS

The internal counters which address the display memory are made up of :

- 6 horizontal address bits ( $h = 64$ )  
 $h_0, h_1, h_2, h_3, h_4, h_5$
- 9 vertical address bits ( $V \leq 512$ )  
 $t, V_0, V_1, V_2, V_3, V_4, V_5, V_6, V_7$

$t$  is here the LSB. It denotes the line parity and changes every frame because of interlaced scan. Within a same frame,  $V_0$  denotes the LSB.

The write address is made up of the 9 LSBs of the X and Y internal registers.

$$X_0, X_1, X_2, X_3, X_4, X_5, X_6, X_7, X_8$$

$$Y_0, Y_1, Y_2, Y_3, Y_4, Y_5, Y_6, Y_7, Y_8$$

The display address and write address are cross-referenced as follows :

EF9365

FMAT = 1

$h_0$	$h_1$	$h_2$	$h_3$	$h_4$	$h_5$	$t$	$V_0$	$V_1$	$V_2$	$V_3$	$V_4$	$V_5$	$V_6$	$V_7$
$X_3$	$X_4$	$X_5$	$X_6$	$X_7$	$X_8$	$Y_0$	$Y_1$	$Y_2$	$Y_3$	$Y_4$	$Y_5$	$Y_6$	$Y_7$	$Y_8$

FMAT = 0

$h_0$	$h_1$	$h_2$	$h_3$	$h_4$	$h_5$	$V_0$	$V_1$	$V_2$	$V_3$	$V_4$	$V_5$	$V_6$	$V_7$
$X_2$	$X_3$	$X_4$	$X_5$	$X_6$	$X_7$	$Y_0$	$Y_1$	$Y_2$	$Y_3$	$Y_4$	$Y_5$	$Y_6$	$Y_7$

EF9366

$h_0$	$h_1$	$h_2$	$h_3$	$h_4$	$h_5$	$V_0$	$V_1$	$V_2$	$V_3$	$V_4$	$V_5$	$V_6$	$V_7$
$X_3$	$X_4$	$X_5$	$X_6$	$X_7$	$X_8$	$Y_0$	$Y_1$	$Y_2$	$Y_3$	$Y_4$	$Y_5$	$Y_6$	$Y_7$

DAD AND MSL OUTPUT STATUS TABLES

EF9365

FMAT = 1

		MSL				DAD						
ALL	CK	0	1	2	3	0	1	2	3	4	5	6
0	0	$X_0$	$X_1$	$X_2$	$V_1$	$h_5$	$h_4$	$h_3$	$h_2$	$h_1$	$h_0$	$V_0$
0	1					$V_7$	$V_6$	$V_5$	$V_4$	$V_3$	$V_2$	$t$
1	0	$X_0$	$X_1$	$X_2$	$Y_2$	$X_8$	$X_7$	$X_6$	$X_5$	$X_4$	$X_3$	$Y_1$
1	1					$Y_8$	$Y_7$	$Y_6$	$Y_5$	$Y_4$	$Y_3$	$Y_0$

EF9365

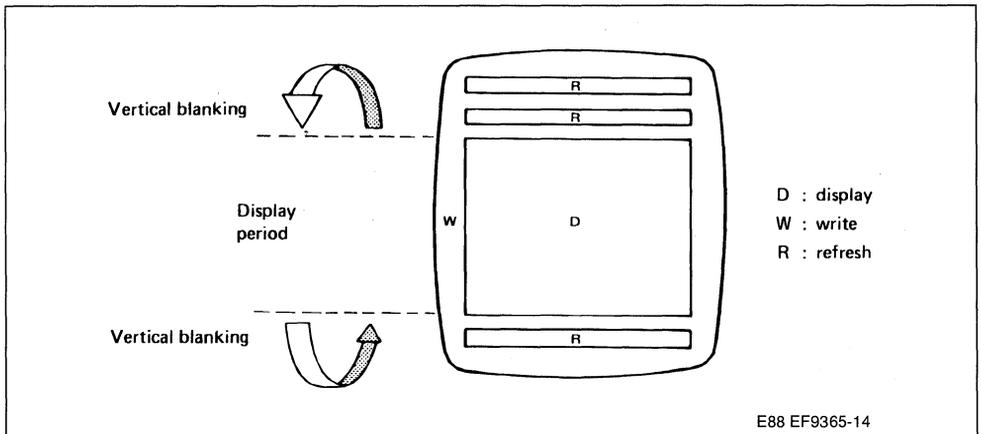
FMAT = 0

		MSL				DAD						
ALL	CK	0	1	2	3	0	1	2	3	4	5	6
0	0	0	0	0	0	h <sub>5</sub>	h <sub>4</sub>	h <sub>3</sub>	h <sub>2</sub>	h <sub>1</sub>	h <sub>0</sub>	V <sub>0</sub>
0	1					V <sub>7</sub>	V <sub>6</sub>	V <sub>5</sub>	V <sub>4</sub>	V <sub>3</sub>	V <sub>2</sub>	V <sub>1</sub>
1	0	X <sub>0</sub> and X <sub>1</sub> decoded (active low)				X <sub>7</sub>	X <sub>6</sub>	X <sub>5</sub>	X <sub>4</sub>	X <sub>3</sub>	X <sub>2</sub>	Y <sub>0</sub>
1	1					Y <sub>7</sub>	Y <sub>6</sub>	Y <sub>5</sub>	Y <sub>4</sub>	Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>

If FMAT is high, the 128 refresh accesses are executed at 2 line intervals, for only one half of the memory, the 32 K-bytes being split into two 16 K-byte blocks. The V<sub>1</sub> output on MSL3 is used to switch over from one block to the other at 2 line intervals.

MEMORY OPERATION SEQUENCE ALONG ONE FRAME

Apart from the window where the memory is used for display purposes exclusively, write operations may be performed, except during 3 refresh periods.



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The three period types, D, W and R, respectively, are indicated outside the circuit through the BLK and ALL signals :

	BLK	ALL
D	0	0
W	1	1
R	1	0

Exceptions :

- If bit 2 in register CTRL1 is high (high speed write), the display period is suppressed and 19

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		MSL				DAD						
ALL	CK	0	1	2	3	0	1	2	3	4	5	6
0	0	X <sub>0</sub>	X <sub>1</sub>	X <sub>2</sub>	1	h <sub>5</sub>	h <sub>4</sub>	h <sub>3</sub>	h <sub>2</sub>	h <sub>1</sub>	h <sub>0</sub>	V <sub>0</sub>
0	1					V <sub>7</sub>	V <sub>6</sub>	V <sub>5</sub>	V <sub>4</sub>	V <sub>3</sub>	V <sub>2</sub>	V <sub>1</sub>
1	0					X <sub>8</sub>	X <sub>7</sub>	X <sub>6</sub>	X <sub>5</sub>	X <sub>4</sub>	X <sub>3</sub>	Y <sub>0</sub>
1	1					Y <sub>7</sub>	Y <sub>6</sub>	Y <sub>5</sub>	Y <sub>4</sub>	Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>

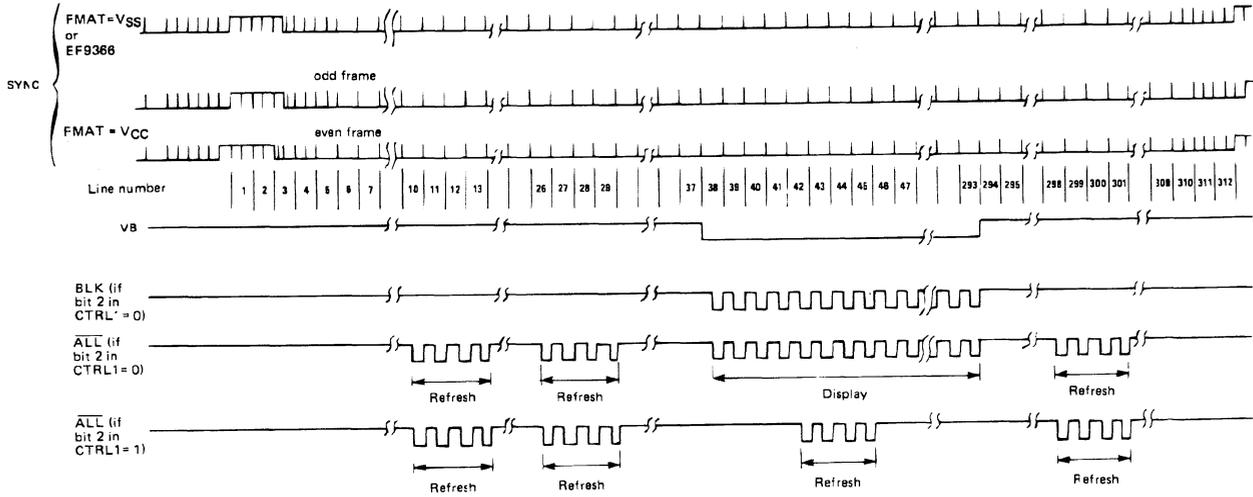
During vertical blanking, such a refresh is achieved using 4 lines at 16 line intervals.

If FMAT is low or for the EF9366 : the 128 refresh accesses are executed at 2 display line intervals.

refresh cycles of 4 lines each are executed during one frame.

- As long as the WO input is high, the circuit is set to write mode, and BLK retains the same outline as it has under normal operating conditions.

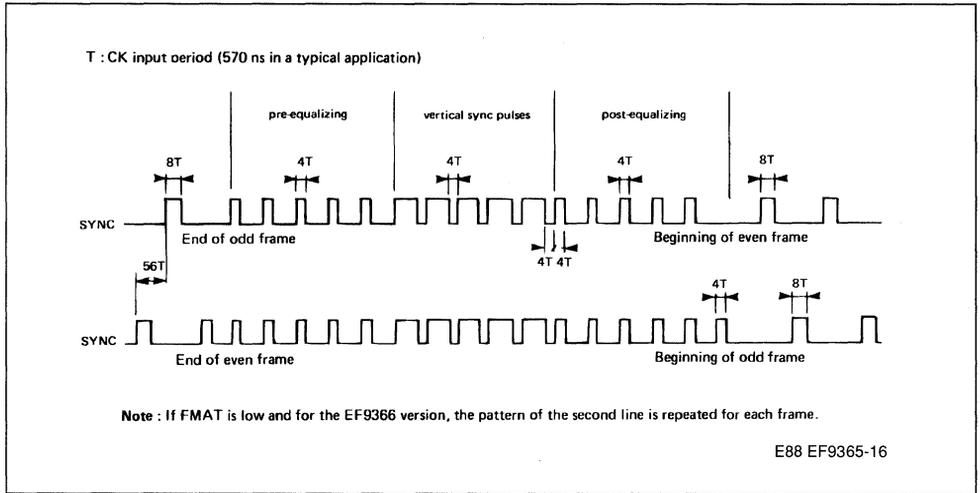
In these two cases, executing codes 04<sub>16</sub>, 06<sub>16</sub>, 07<sub>16</sub> and 0C<sub>16</sub> triggers a complete D sequence for a highspeed scan of all addresses. This lasts two frames if FMAT is high or one frame if FMAT is low and for the EF9366 version.



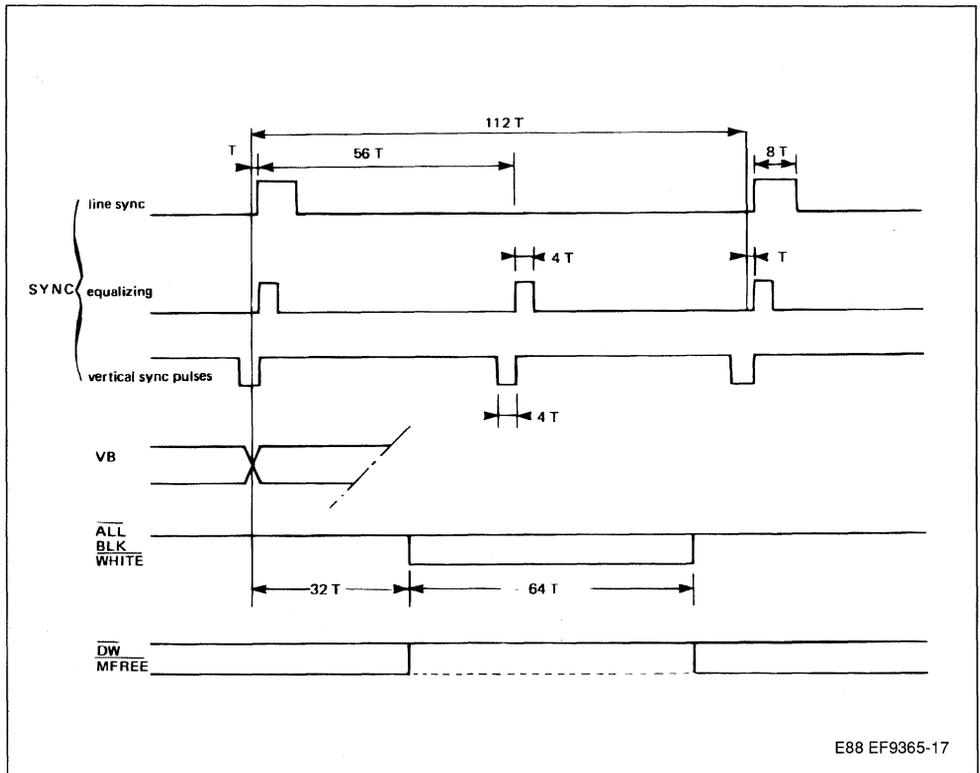
Note : ALL signal high denotes write periods.

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COMPOSITE SYNC AROUND FRAME SYNC



DETAILED LINE DIAGRAM



**HARDWIRED WRITE PROCESSOR OPERATION IN DISPLAY MEMORY**

The hardwired write processors are sequenced by the master clock CK. They receive their parameters from the microprocessor bus. They control the X, Y write address, and the DIN, DW, MFREE and IRQ outputs.

These hardwired processors operate in continuous mode. In the event of conflicting access to the display memory, the display and refresh processors have priority.

Since command decoding is synchronous with the CK master clock, any write operation into the (CMD) command register triggers a synchronizing mechanism which engages the circuit for a maximum of 2 CK cycles when the E input returns high. The circuit remains engaged throughout command execution.

No further command should be entered as long as bit 2 in STATUS register is low.

**VECTOR PLOTTING**

The internal vector generator makes it possible to modify, within the display memory, all the dots which form the approximation of a straight line segment. All vectors plotted are described by the origin dot and the projections on the axes.

The starting point co-ordinates are defined by the X, Y register value, prior to the plotting operation.

Projections into the axes are defined as absolute values by the DELTAX and DELTAY registers, with the sign in the command byte that initiates the vector plotting process.

The vector approximation achieved here is that established by J. F. BRESENHAM ("Algorithm for computer control of a digital plotter"). This algorithm is executed by a hardwired processor which allows for a further vector component dot to be written in each CK clock cycle.

During plotting, the display memory is addressed by the X, Y registers, which are incremented or decremented.

On completion of vector plotting, they point to the end of this vector.

All vectors may be plotted using any of the following line patterns : continuous, dotted, dashed, dash-dotted, according to the 2 LSBs in register CTRL2.

Irrespective of such patterns, the plotting speed remains unchanged. The "pen down-pen up" statement required for plotting non-continuous lines is controlled by the DW output.

For a specified non-continuous line plotted vector, defined by DELTAX, DELTAY, CTRL2, CMD, the

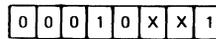
DW sequencing during the plotting process is always the same, irrespective of vector origin and of the nature of previous plots. This feature guarantees that a specified vector can be deleted by plotting it again after moving X and Y to the starting point, and complementing bit 1 in register CTRL1.

Since the vector plotting initiation command defines the sign of the projections into the axes, all vectors may be plotted using 4 different commands.

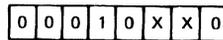
For increased programming flexibility, the system incorporates 16 different commands, supplemented by a set of 128 commands which make it possible to plot small size vectors by ignoring the DELTAX and DELTAY registers.

Such commands are as follows :

- Basic Commands
- commands which allow ignoring the DELTAX or DELTAY registers by considering them as of zero value



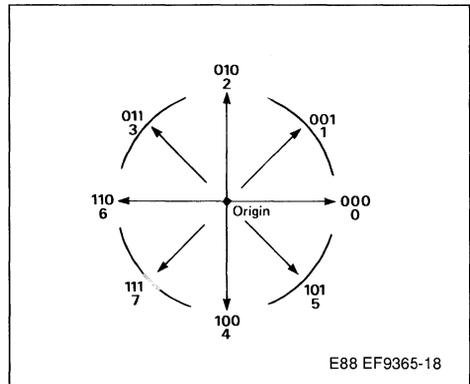
DELTA X sign } 0 if positive  
 DELTA Y sign } 1 if negative



0 0 DELTAY ignored, DELTAX > 0  
 0 1 DELTAX ignored, DELTAY > 0  
 1 0 DELTAX ignored, DELTAY < 0  
 1 1 DELTAY ignored, DELTAX < 0

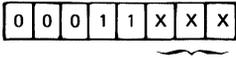
**Notes** :Bits 1 and 2 always have the same sign meaning.

These 8 codes may be summarized by the following diagram :

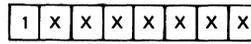


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- Commands which allow ignoring the smaller of the two DELTAX and DELTAY registers, by considering it as being equal to the larger one, which is the same as plotting vectors parallel to the axes or diagonals, using a single DELTA register.
- Commands in which the two registers DELTAX and DELTAY may be ignored by specifying the projections through the CMD register (0 to 3 steps for each projection).



Same direction codes as above.



(Unsigned integer values) Same direction code as previously

EXAMPLE : PLOTTING A DOTTED VECTOR

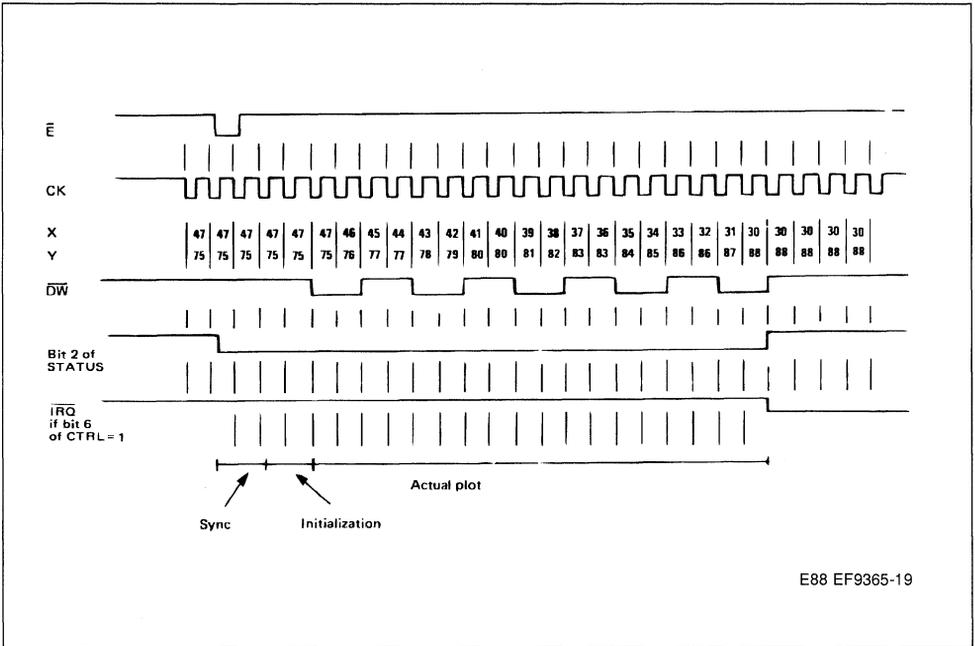
Origin :  $\left\{ \begin{array}{l} X = 47_{10} \\ Y = 75_{10} \end{array} \right.$

Projection :  $\left\{ \begin{array}{l} \text{DELTA X} = 17_{10} \\ \text{DELTA Y} = 13_{10} \end{array} \right.$

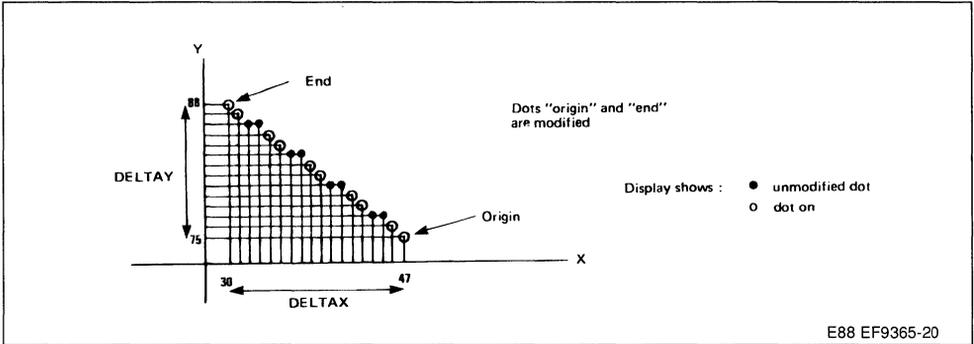
CMD = 13<sub>16</sub> Corresponding to  
 - Basic command  
 - DELTAX < 0  
 - DELTAY > 0

CTRL1 = 03<sub>16</sub> Pen down,  
 CTRL2 = 116 Dotted vector :  
 2 dots on,  
 2 dots off.

**Plotting cycle sequence :** (it is assumed that the vector generator is not interrupted by the display or refresh cycle).



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**Note :** Plotting a vector with DELTAX = DELTAY = 0 writes the dot X, Y in memory. It occupies the vector generator for synchronization, initialization and one write cycle.

**CHARACTER AND SYMBOL GENERATOR**

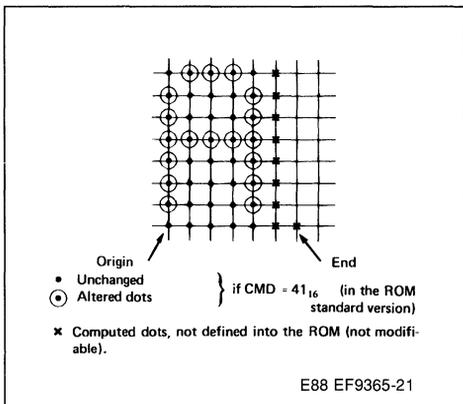
The character generator operates in the same way as the vector generator, i. e. through incrementing or decrementing the X, Y registers, in conjunction with a DW output control.

It receives parameters from the CSIZE, CTRL2 and CMD registers. The characters plotted are selected, according to the CMD value, out of 98 matrices (97 8-dot high x 5-dot wide rectangular matrices, and one 4 dot x 4 dot matrix) defined in an internal ROM.

Two scaling factors may be applied to the characters plotted using X and Y defined by the CSIZE register. The characters may be tilted, according to the content of register CTRL2.

**Basic matrix**

Upon completion of a character writing process, the X and Y registers are positioned for writing a further character next to the previous one, with a 1 dot spacing, i. e. Y is restored to its original value and X is incremented by 6.



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**Scaling factors**

Each individual dot in the 5 x 8 basic matrix may be replaced by a P x Q size block.

- P : X co-ordinate scaling factor
- Q : Y co-ordinate scaling factor

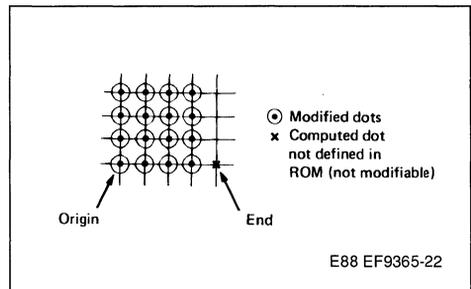
The character size becomes 5 P x 8 Q. Upon completion of the writing process, X is incremented by 6 P. The CK clock cycle count required is 6 P x 8 Q.

P and Q may each take values from 1 through 16. They are defined by the CSIZE register. Each value is encoded on 4 bits, value 16 being encoded as 016.

In register CSIZE, P is encoded on the 4 MSBs and Q on the 4 LSBs.

Among the 97 rectangular matrices available in the standard ROM, 96 correspond to CMD values ranging from 2016 to 7F16, and the 97th matrix to 0A16. In the standard version, these values correspond to the 96 printable characters in the ASCII set. The 97th character is a 5 P x 8 Q block which may be used for deleting the other characters.

The 98th code (0B16) is used to plot a 4 P x 4 Q graphic block. It locates X, Y, without spacing for the next symbol. Such a block makes it possible to pad uniform areas on the screen.



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**Tilted characters**

All characters may be modified to produce tilted characters or to mark the vertical co-ordinate with straight or tilted type symbols. Such changes may be achieved using bits 2 and 3 in register CTRL2.

**Note :** Scaling factors P and Q are always applied within the co-ordinates of the character before conversion.

**Character deletion**

A character may be deleted using either the same command code or command code 0A<sub>16</sub>. In either case, bit 1 in register CTRL1 should be inverted, the origin should be the same as prior to a character plotting operation, as should the scaling factors.

**Note :** Vector generator and character generator operate in similar ways :

	Vector	Character
Dimensions	DELTAX, DELTAY	CSIZE, tilting
DW Modulation	Type of Line	Character Code

**USE OF LIGHT PEN CIRCUITRY**

A rising edge on the LPCK input is used to sample the current display address in the XLP and YLP registers, provided that this edge is present in the frame immediately following loading of the 08<sub>16</sub> or 09<sub>16</sub> code into the CMD register.

Here, the frame origin is counted starting with the VB falling edge. With code 08<sub>16</sub>, the WHITE output recopies the BLK signal from the frame origin up to the rising edge on the LPCK input, or when VB starts rising again, if the LPCK input remains low for the entire frame. With code 09<sub>16</sub>, the WHITE output is not activated.

The YLP address is 8-bit coded since there are 256 display lines in each frame. The XLP address is 6-bit coded since there are 64 display cycles in each line.

These 6 bits are left justified in the XLP register. XLP and YLP register contents match the write address if FMAT is low (or for the EF9366), but should be multiplied by 2 if FMAT is high, so as to be able to match the write address.

The address sampled into XLP corresponds to the current memory cycle. Dots detected by the light pen were addressed in the memory during the previous cycle. Hence, 1 should be subtracted from bit 2 in XLP register where the light pen electronic circuitry does not produce any additional delay.

If the rising edge on input LPCK occurs while VB is low, then the LSB in XLP is set high. This bit acts as

a status signal which is reset to the low state by reading register XLP or YLP.

The rising edge first received (LPCK or VB) sets bit 0 in STATUS register high. An interrupt is initiated if bit 4 bin CTRL1 is high.

When commands 08<sub>16</sub> or 09<sub>16</sub> have been decoded, bit 2 of the status register goes high (circuit ready for any further command) and bit 0 goes low (light pen operating sequence underway).

**SCREEN BLANKING COMMANDS**

Three commands (04<sub>16</sub>, 06<sub>16</sub>, 07<sub>16</sub>) will set the whole display memory to a status corresponding to a "black display screen" condition. Another command (0C<sub>16</sub>) may be used to set the whole memory to a status other than black (this condition being determined by bit 1 in register CTRL1).

The 4 commands outlined above use the planned scanning of the memory addresses achieved by the display stage. The X and Y registers are not affected by commands 04<sub>16</sub> and 0C<sub>16</sub>. Hence, the time required is that corresponding to one frame (EF9366 or FMAT low) or two frames (FMAT high). The time corresponding to the completion of the frame currently executing when the CMD register is loaded, should be added to the above time.

For the screen blanking process, the frame origin is counted starting with the VB falling edge.

The only signals affected here are the DW output, which remains low when VB is low, and the DIN output which is forced high where the 04<sub>16</sub>, 06<sub>16</sub> and 07<sub>16</sub> commands are entered.

Such commands are activated without requiring action by WO input or bit 2 in register CTRL1. While these commands are executing, bit 2 in STATUS register remains low.

**EXTERNAL REQUEST FOR DISPLAY MEMORY ACCESS (MFRREE OUTPUT)**

On writing code 0F<sub>16</sub> into the CMD register, the MFRREE output is set low by the circuitry, during the next free memory cycle.

Apart from the display and refresh periods, this cycle is the first complete cycle that occurs after input E is reset high.

During this cycle, those addresses output on DAD and MSL correspond to the X and Y register contents : DW is high, ALL is high.

Should the memory be engaged in a display or refresh operation, (which is the case when ALL is low), then this cycle is postponed to be executed after ALL is reset high. The maximum waiting time is thus 64 cycles.

The  $\overline{\text{MFree}}$  signal may be used e. g. for performing a read or write operation into a register located between the display memory and the microprocessor bus.

### INTERRUPTS OPERATION

An interrupt may be initiated by three situations denoted by internal signals :

- Circuit ready for a further command
- Vertical blanking signal
- Light pen sequence completed.

These three signals appear in real time in the STATUS register (bits 0, 1, 2). Each signal is cross-referenced to a mask bit in the register CTRL1 (bits 4, 5, 6).

If the mask bit is high, the first rising edge that occurs on the interrupt initiating signal sets the related interrupt flip-flop circuit high.

The outputs from these three flip-flop circuits appear in the STATUS register (bits 4, 5, 6). If one flip-flop circuit is high, bit 7 in the STATUS register is high, and pin  $\overline{\text{IRQ}}$  is forced low.

A read operation in the STATUS register resets its 4 MSBs low, after input  $\overline{\text{E}}$  is reset high.

The three interrupt control flip-flops are duplicated to prevent the loss of an interrupt coming during a read cycle of the status register.

The status of bits 4, 5 and 6 corresponds to the interrupt control flip-flop circuit output, before input  $\overline{\text{E}}$  goes low.

An interrupt coming during a read cycle of the STATUS register does not appear in bits 4, 5 and 6 during this read sequence, but during the following one. However, it may appear in bits 0, 1, 2 or on pin  $\overline{\text{IRQ}}$ .

**Table 1 : Register Address.**

Address Register					Register Functions		Number of Bits
Binary				Hexa	Read R/W = 1	Write R/W = 0	
A3	A2	A1	A0				
0	0	0	0	0	STATUS	CMD	8
0	0	0	1	1	CTRL 1 (write Control and Interrupt Control)		7
0	0	1	0	2	CTRL 2 (Vector and Symbol Type Control)		4
0	0	1	1	3	CSIZE (Character Size)		8
0	1	0	0	4	Reserved		-
0	1	0	1	5	DELTA X		8
0	1	1	0	6	Reserved		-
0	1	1	1	7	DELTA Y		8
1	0	0	0	8	X MSBs		4
1	0	0	1	9	X LSBs		8
1	0	1	0	A	Y MSBs		4
1	0	1	1	B	Y LSBs		8
1	1	0	0	C	XLP (light-pen)	Reserved	7
1	1	0	1	D	YLP (light-pen)	Reserved	8
1	1	1	0	E	Reserved		-
1	1	1	1	F	Reserved		-

Reserved : These addresses are reserved for future versions of the circuit. In read mode, output buffers D0-D7 force a high state on the data bus.

Table 2 : Command Register.

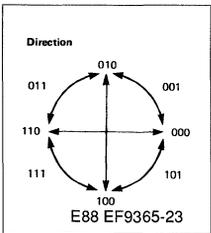
b7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
b6	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	1
b5	0	0	1	1	0	0	1	1	0	0	1	0	0	1	1	1
b4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
b3 b2 b1 b0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
<b>Vector Generation</b> (for b2, b1, b0 see small vector definition)																
0 0 0 0	0	Set Bit 1 of CTRL 1 : Pen Selection	Space !	0	@	P	`	p								
0 0 0 1	1	Clear Bit 1 of CTRL 1 : Eraser selection	!	1	A	Q	a	q								
0 0 1 0	2	Set Bit 0 of CTRL 1 : Pen/Eraser Down Selection	"	2	B	R	b	r								
0 0 1 1	3	Clear Bit 0 of CTRL 1 : Pen/Eraser up Selection	#	3	C	S	c	s								
0 1 0 0	4	Clear screen	\$	4	D	T	d	t								
0 1 0 1	5	X and Y Registers Reset to 0	%	5	E	U	e	u								
0 1 1 0	6	X and Y Reset to 0 and Clear Screen	&	6	F	V	f	v								
0 1 1 1	7	Clear Screen, set CSIZE to code "minsize". All other registers reset to 0. (except XLP, YLP)	'	7	G	W	g	w								
<b>Special Direction Vectors</b> (for b2, b1, b0 see small vector definition)																
1 0 0 0	8	Light-pen initialization (WHITE forced low)	(	8	H	X	h	x								
1 0 0 1	9	Light-Pen initialization	)	9	I	Y	i	y								
1 0 1 0	A	5 x 8 Block Drawing (size according to CSIZE)	*	:	J	Z	j	z								
1 0 1 1	B	4 x 4 Block Drawing (size according to CSIZE)	+	;	K	[	k	{								
1 1 0 0	C	Screen Scanning : Pen or Eraser as defined by CTRL1	,	<	L	\	l									
1 1 0 1	D	X Register Reset to 0	-	=	M	]	m	}								
1 1 1 0	E	Y Register Reset to 0	.	>	N	↑	n	→								
1 1 1 1	F	Direct Image Memory access request for the next free cycle.	/	?	O	←	o	⊗								

**Small Vector Definition**

b7	b6 b5	b4 b3	b2 b1 b0
1	ΔX	ΔY	Direction

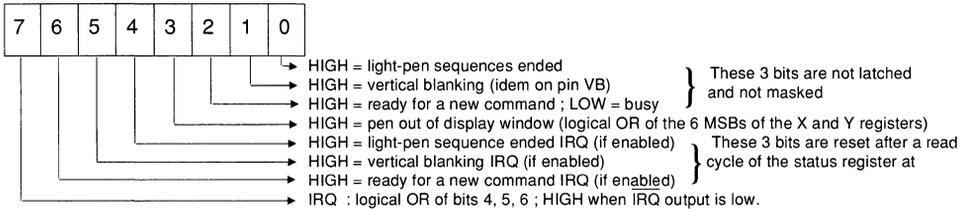
**Dimension**

ΔX or ΔY	Vector Length
0 0	0 Step
0 1	1 Step
1 0	2 Steps
1 1	3 Steps

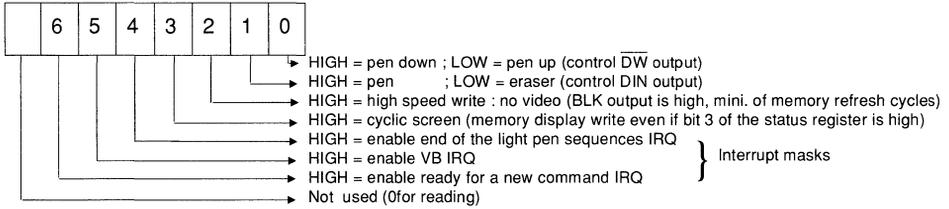


**OTHER REGISTERS**

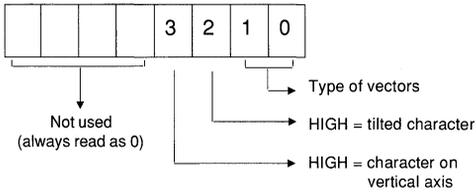
**STATUS REGISTER (read only)**



**CONTROL REGISTER 1 (read/write)**

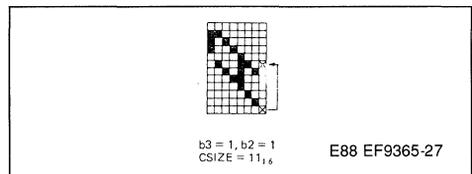
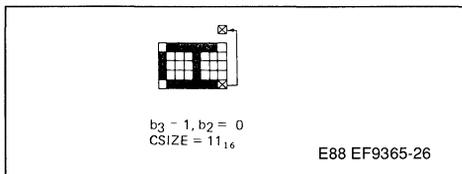
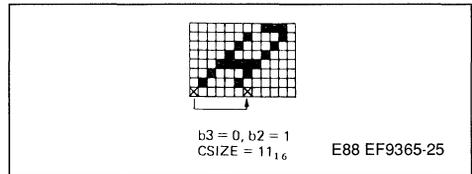
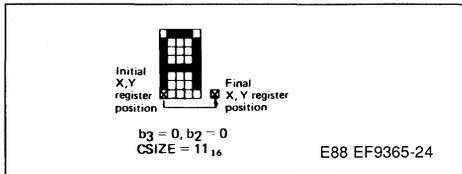


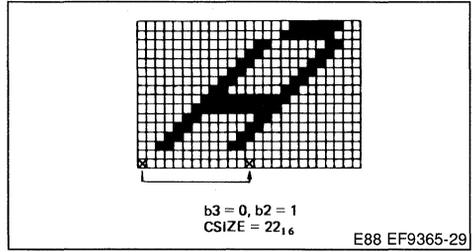
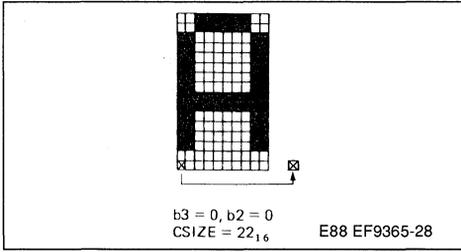
**CONTROL REGISTER 2 (read/write)**



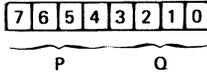
b1	b0	Type of Vectors
0	0	Continuous
0	1	Dotted 2 dots on, 2 dots off
1	0	Dashed 4 dots on, 4 dots off
1	1	Dotted- 10 dots on, 2 dots off
		Dashed 2 dots on, 2 dots off

**Types of character orientations**





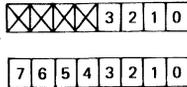
C-SIZE REGISTER (read/write)



P : Scaling factor on X axis  
 Q : Scaling factor on Y axis

P and Q may take any value between 1 and 16. This value is given by the leftmost or rightmost 4 bits for P and Q respectively. Binary value (0) means 16.

X AND Y REGISTERS (read/write)

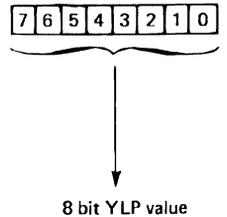
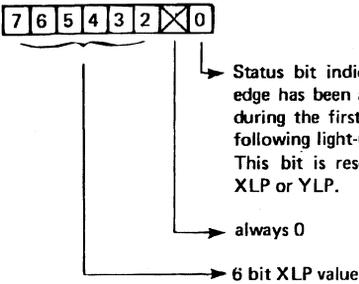


MSBs

LSBs

The 4 leftmost MSBs are always 0.

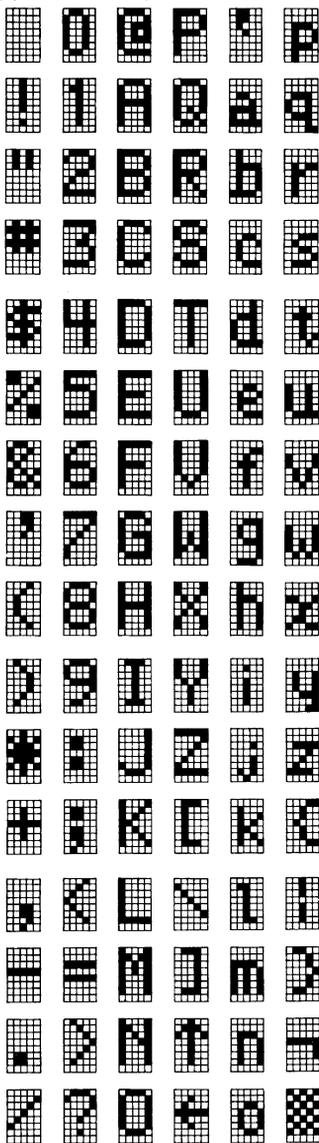
XLP AND YLP REGISTERS



ASCII CHARACTER GENERATOR (5 x 8 matrix)

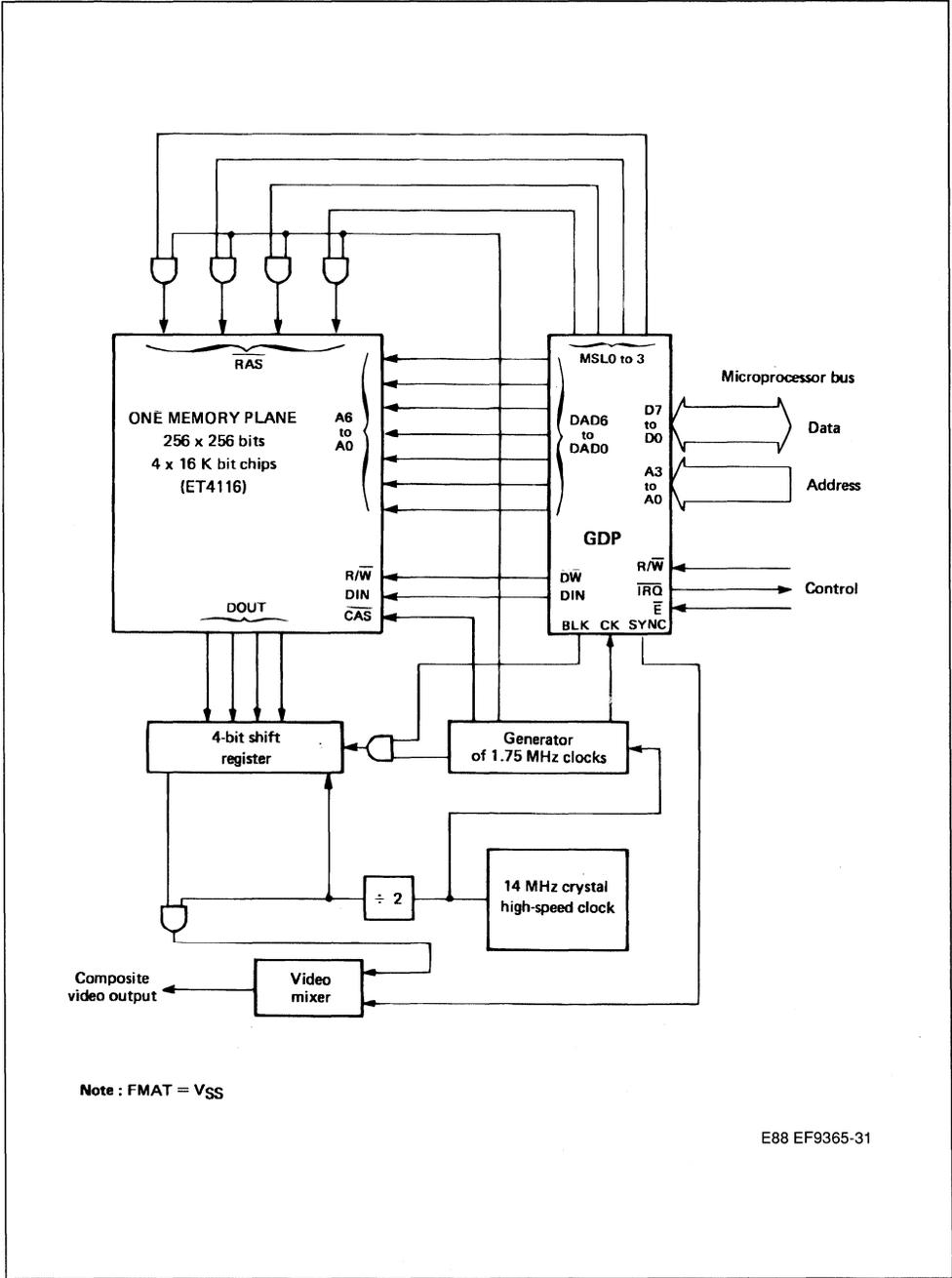
b7	0	0	0	0	0	0
b6	0	0	1	1	1	1
b5	1	1	0	0	1	1
b4	0	1	0	1	0	1

b3	b2	b1	b0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



E88 EF9365-30

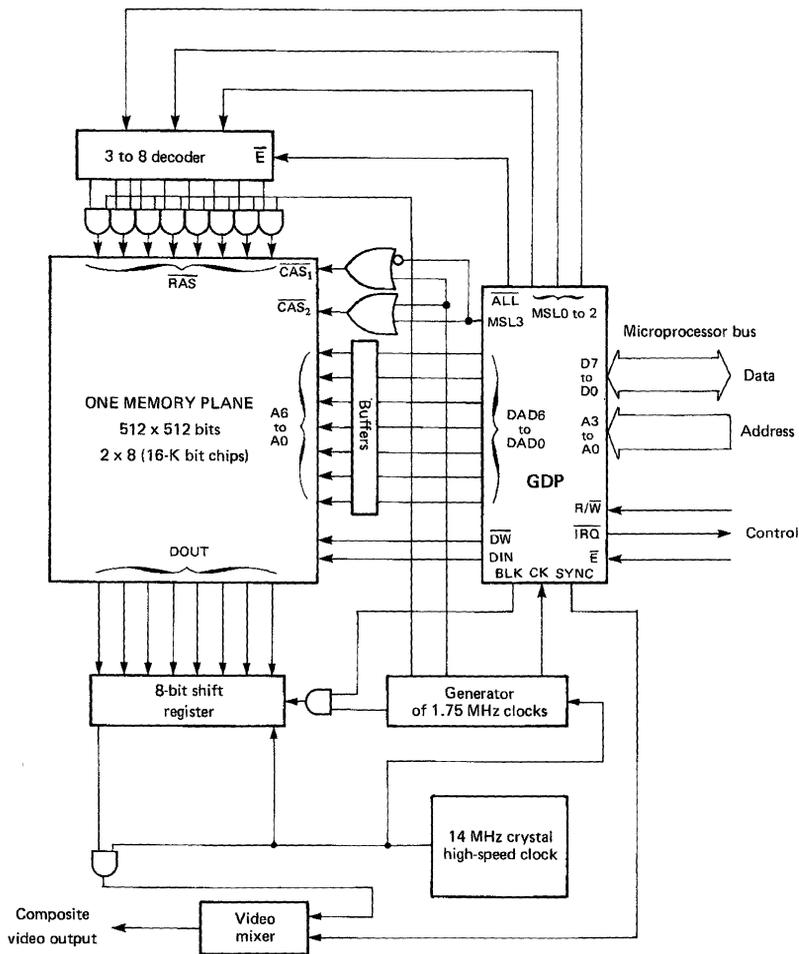
EXAMPLE OF AN APPLICATION OF THE EF9365 : 256 x 256 BLACK AND WHITE



Note : FMAT = VSS

E88 EF9365-31

EXAMPLE OF AN APPLICATION OF THE EF 9365 : 512 x 512 BLACK AND WHITE

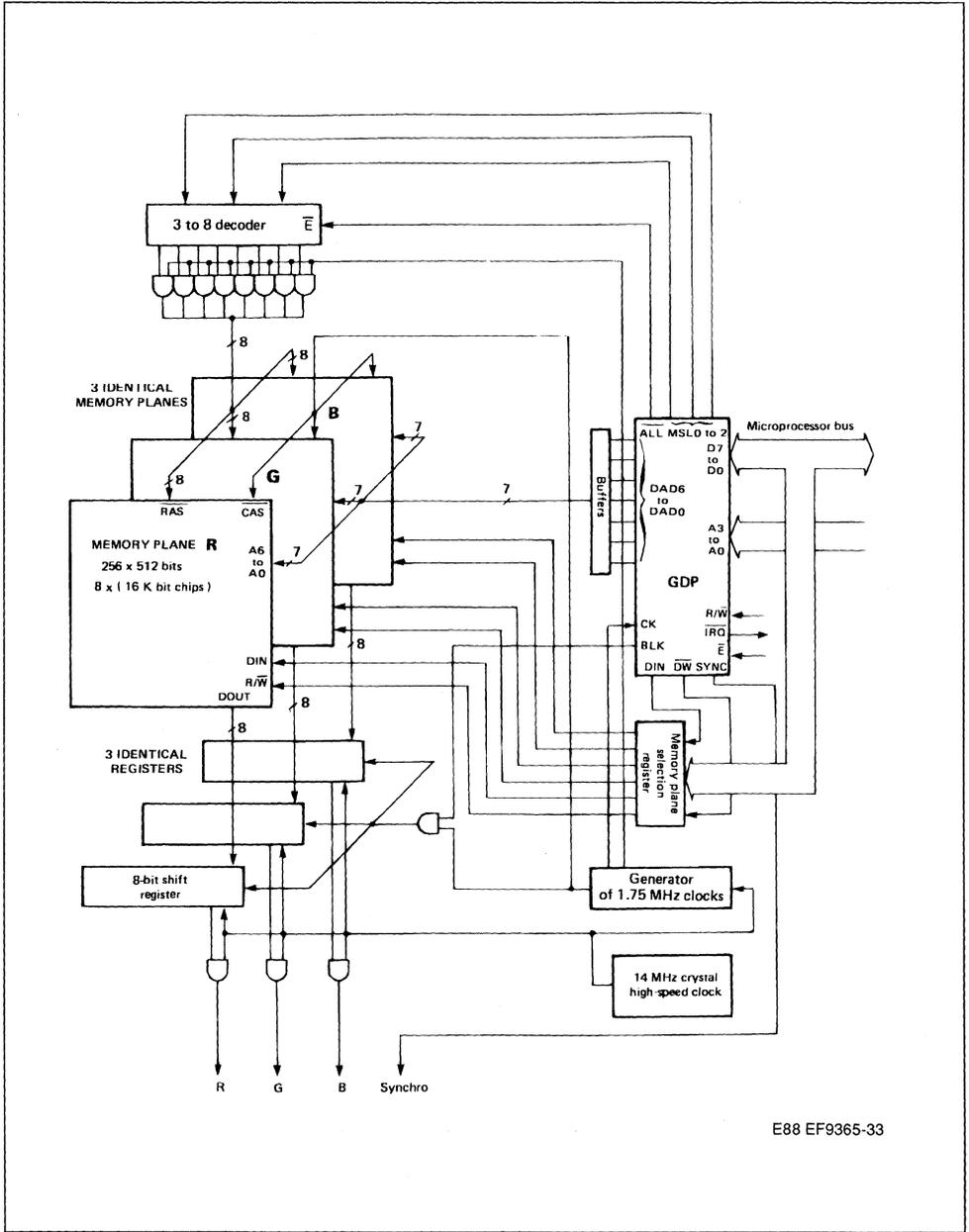


Note : FMAT = VCC

E88 EF9365-32

EXAMPLE OF AN APPLICATION OF THE EF9366 : 256 x 512 COLOUR.

Eight colours may be obtained from the three basic colours red (R), green (G), blue (B).

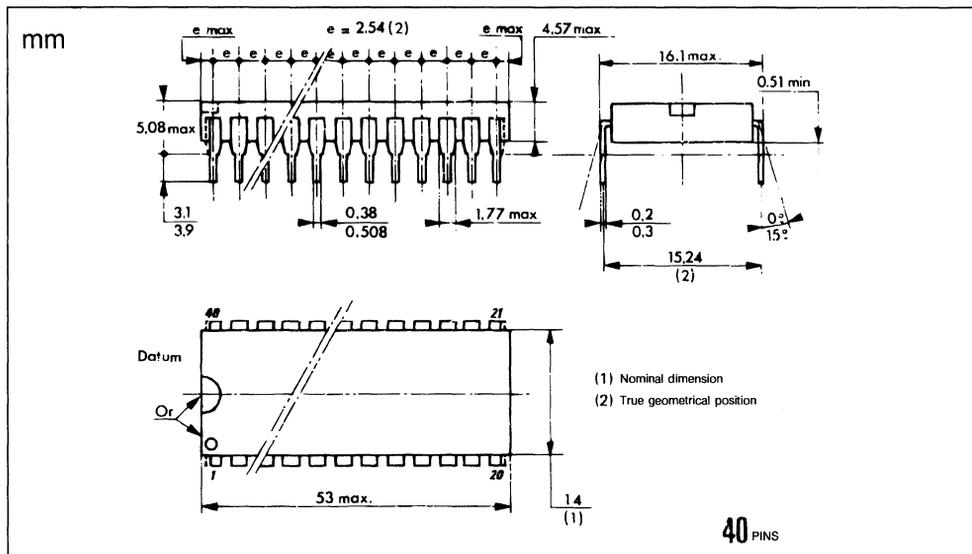


E88 EF9365-33

Note : FMAT = V<sub>CC</sub>.

PACKAGE MECHANICAL DATA

40 PINS - PLASTIC DIP



ORDERING INFORMATION

Part Number	Temperature Range	Package
EF9365P	0 to 70 °C	DIP 40
EF9366P	0 to 70 °C	DIP 40

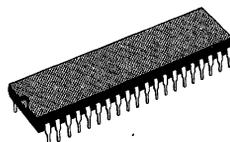


## MOS GRAPHIC DISPLAY PROCESSOR (GDP)

- SELECTABLE RESOLUTIONS IN BLACK AND WHITE OR COLOR :  
 VERTICAL RESOLUTION : 525 LINE MONITOR (208 OR 416), 625 LINE MONITOR (256 or 512)  
 HORIZONTAL RESOLUTION : 256, 320\*, 384\*, 512, 640\*, 768\*, 1024, FULL SCREEN.(\*) with external PROM
- HIGH SPEED VECTOR PLOT WELL SUITED TO ANIMATION - 4 TYPES OF LINES
- MULTIPLEXED ADDRESS AND REFRESH FOR 16 K OR 64 K DYNAMIC RAMs
- NO LIMITATION ON THE NUMBER OF SELECTABLE MEMORY PLANES (colors, grey levels or any other attributes)
- MULTIPAGE APPLICATION CAPABILITY
- ON-CHIP FULL ASCII CHARACTER GENERATOR (96) - MAXIMUM ALPHANUMERIC SCREEN DENSITY : 170 x 57 - PROGRAMMABLE SIZES AND ORIENTATIONS
- DIRECT INTERFACING WITH THE MONITOR THROUGH THE COMPOSITE SYNCHRO AND BLANKING SIGNALS
- AUTOMATIC ALLOCATION OF DISPLAY MEMORY IN REFRESH, WRITE, DUMP, AND DISPLAY CYCLES
- LIGHT PEN REGISTERS AND CONTROL SIGNALS
- THREE TYPES OF INTERRUPT REQUESTS
- FULLY STATIC DESIGN
- TTL COMPATIBLE I/O
- SINGLE + 5 V SUPPLY

### DESCRIPTION

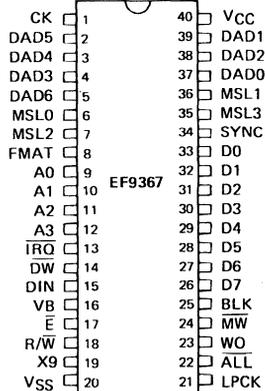
This GDP is a true high resolution graphic display processor, which contains all the functions required to process vector generation at a very high speed and to generate all the timing signals required for interfacing interlaced or non interlaced video data on a raster scan CRT display compatible with 525 line or the CCIR 625 line standards.



**P**  
**DIP 40**  
 (Plastic Package)

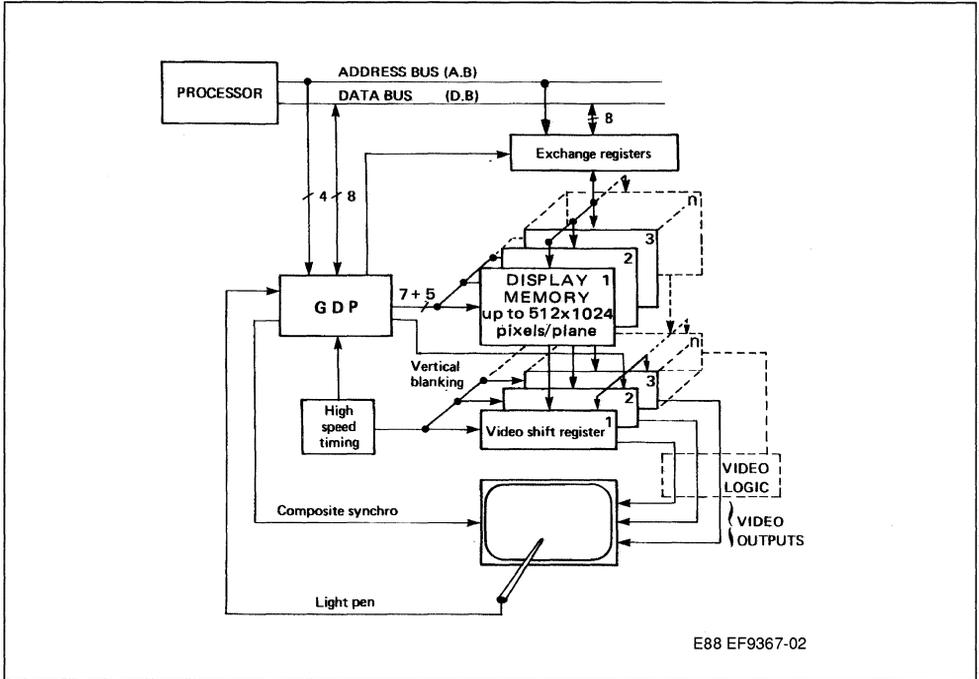
**ORDER CODE : EF9367P**

### PIN CONNECTIONS

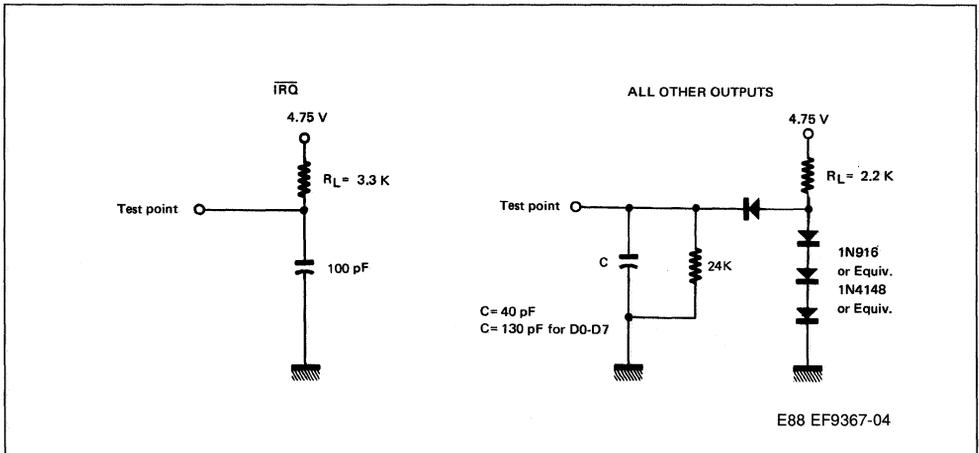


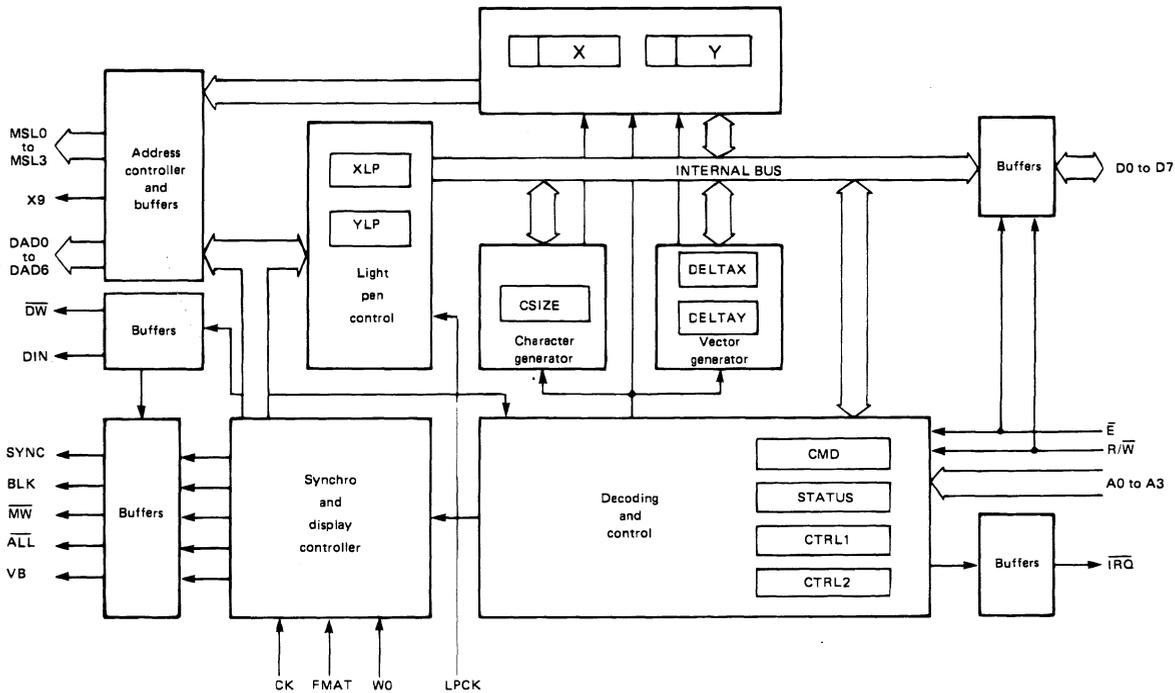
E88 EF9367-01

TYPICAL APPLICATION



TEST LOADS





E88 EF9367-03

## GENERAL DESCRIPTION

Developed using NMOS technology, the GDP is an intelligent raster scan video display controller, fully programmable via an eight-bit microprocessor bus. Besides all the timing logic functions required to generate the video, sync and blanking signals, the GDP includes two hardwired display processors : a vector and a character generator.

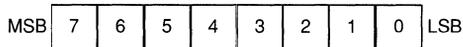
This unique feature allows an ultrafast screen writing speed (the 1024 dot diagonal may be written in less than 1.4 ms) at almost no microprocessor processing cost.

The GDP is particularly well-suited to all applications in which the display memory is not directly addressed by the MPU. This feature allows a total asynchronism between the MPU and the GDP memory cycles and preserves the whole MPU memory addressing space.

Nevertheless, where direct exchange between the microprocessor and the memory is necessary, the on-chip allocation controller will allow this exchange without display interference.

The GDP is programmable using 11 internal registers occupying 16 consecutive addresses. These registers can also be modified by the GDP's hardwired processors while a command is being executed.

**Note** : A summary of data codes and registers is given in the **Register address table**. Hexadecimal values are subscripted 16 and the register bits are numbered as follows :



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	- 0.3 to + 7.0	V
$V_{in}$	Input Voltage	- 0.3 to + 7.0	V
$T_A$	Operating Temperature	0 to + 70	°C
$T_{stg}$	Storage Temperature	- 55 to + 150	°C

The GDP inputs are protected against high static voltages and electric fields ; nevertheless, normal precautions should be taken to avoid voltages above the limit values on this high impedance circuit.

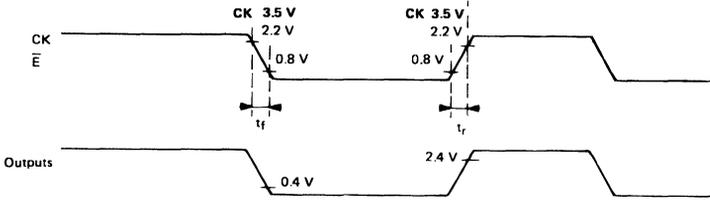
**STATIC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5 V \pm 5\%$ ,  $V_{SS} = 0$ ,  $T_A = 0$  to 70 °C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{IH}$	Input High Voltage Except CK	$V_{SS} + 2.2$	-	$V_{CC}$	V
$V_{IHCK}$	Input High Voltage CK	$V_{SS} + 3.5$	-	$V_{CC}$	V
$V_{IL}$	Input Low Voltage	$V_{SS} - 0.3$	-	$V_{SS} + 0.8$	V
$I_{in}$	Input Leakage Current ( $V_{in} = 0$ to 5.25 V, $V_{CC} = \max$ )	-	1.0	2.5	$\mu A$
$V_{OH}$	Output High Voltage ( $I_{load} = - 100 \mu A$ , $V_{CC} = \min$ )	$V_{SS} + 2.4$	-	-	V
$V_{OL}$	Output Low Voltage ( $I_{load} = 1.6$ mA, $V_{CC} = \min$ )	-	-	$V_{SS} + 0.4$	V
$I_{CC}$	Supply Current	-	80	-	mA
$C_{in}, C_{out}$	Capacitance ( $V_{in} = 0$ , $T_A = 25$ °C, $f = 1.0$ MHz)	-	-	12	pF

**DYNAMIC OPERATING CONDITIONS**(V<sub>DD</sub> = 5.0 V ± 5 %, V<sub>SS</sub> = 0 V ; T<sub>A</sub> = 0 to + 70 °C unless otherwise noted)

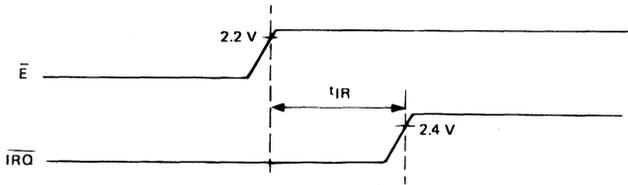
Symbol	Time (ns)	Min.	Max.
t <sub>CK</sub>	Clock Period	560	
t <sub>CKL</sub>	CK Pulse Width, Low	330	
t <sub>CKH</sub>	CK Pulse Width, High	190	
CKLDAD	CK Low to Valid DAD		320
CKHDAD	CK High to Valid DAD		180
CKLSYNC	CK Low to Valid SYNC		300
CKLBLK	CK Low to Valid BLK		310
CKLVB	CK Low to Valid VB		500
CKLALL	CK Low to Valid ALL		300
CKLMSL	CK Low to Valid MSL		300
CKLDW	CK Low to Valid DW		310
CKLMFRL	CK Low to Valid $\overline{\text{M}}\text{FREE}$ Low		330
CKLMFRH	CK Low to Valid $\overline{\text{M}}\text{FREE}$ High		500
CKLDIN	CK Low to Valid DIN		310
CKLIRQ	CK Low to Valid $\overline{\text{I}}\text{RQ}$		1500
CKLWHI	CK Low to Valid $\overline{\text{W}}\text{HITE}$		530
t <sub>EL</sub>	$\overline{\text{E}}$ Pulse Width, Low	450	
t <sub>EH</sub>	$\overline{\text{E}}$ Pulse Width, High	430	
t <sub>AS</sub>	Address Pre-Setup Time	160	
t <sub>AH</sub>	Address Hold Time	10	
t <sub>DSW</sub>	Data Pre-Setup Time (write)	195	
t <sub>DDR</sub>	Data Setup Time (read)		320
t <sub>DHR</sub>	Data Hold Time (read)	10	
t <sub>IR</sub>	$\overline{\text{I}}\text{RQ}$ Release Time		1600
LPHW	LPCK High to $\overline{\text{W}}\text{HITE}$ High (if command 08 <sub>16</sub> )		1600
LPHIRQ	LPCK High to $\overline{\text{I}}\text{RQ}$ Low		1600
t <sub>LPCKH</sub>	LPCK High Hold Time	150	
t <sub>r</sub>	CK and $\overline{\text{E}}$ Rise Times		20
t <sub>f</sub>	CK and $\overline{\text{E}}$ Fall Times		20

CLOCK AND OUTPUT CHARACTERISTICS



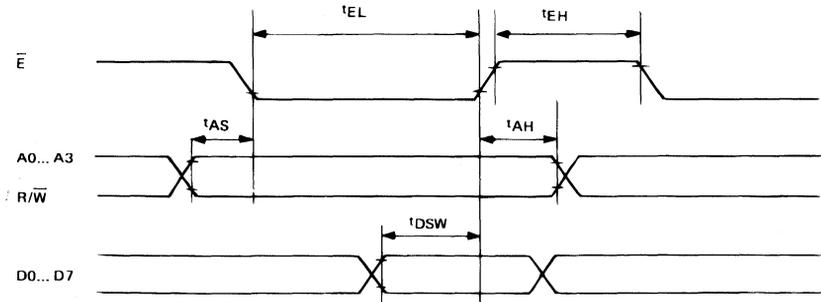
E88 EF9365-05

$\overline{\text{IRQ}}$  RELEASE TIME



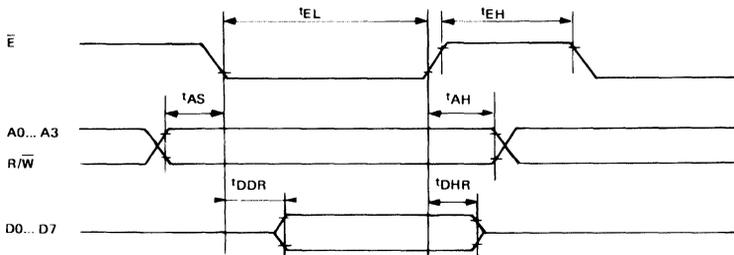
E88 EF9365-06

MICROPROCESSOR BUS, WRITE ACCESS



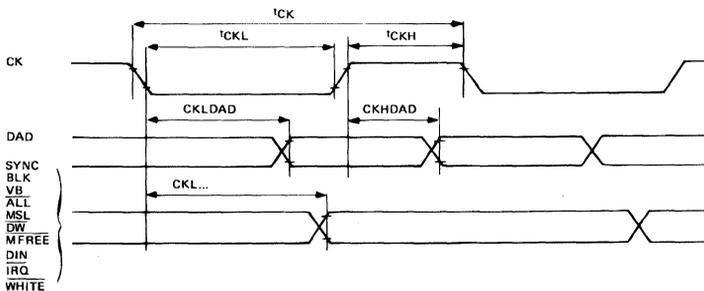
E88 EF9365-07

MICROPROCESSOR BUS, READ ACCESS



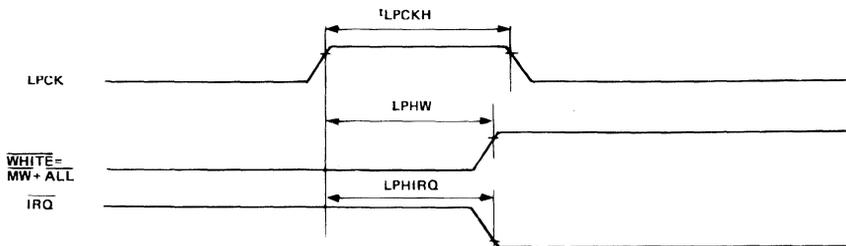
E88 EF9365-08

SYNCHRONOUS SIGNALS WITH CK INPUT



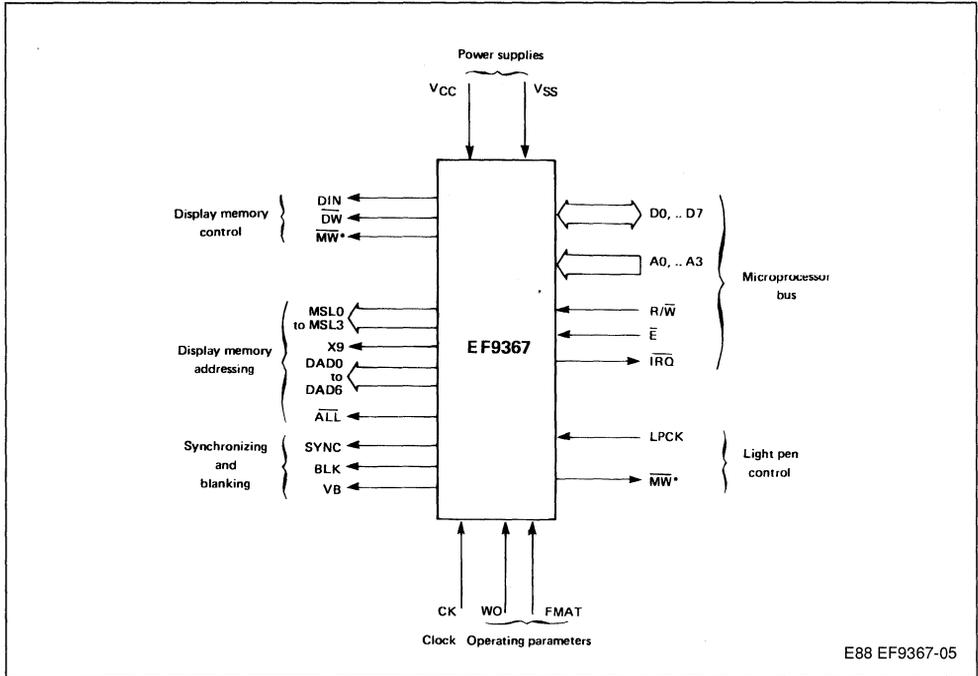
E88 EF9365-09

LIGHT PEN SIGNALS



E88 EF9367-04

PIN DESCRIPTION



\* This pin outputs two items of data multiplexed by signal ALL.

POWER SUPPLY, CLOCK AND OPERATING PARAMETERS

Name	Pin Type	N°	Function	Description
V <sub>SS</sub>	S	20	Power Supply	Ground
V <sub>CC</sub>	S	40	Power Supply	+ 5 V
CK	I	1	Clock	Master Clock. All internal processor states are modified on the falling edge of this signal. The whole circuit logic is static and the cycle of this clock needs only to be adjusted according to the shape and accuracy the synchronizing signals should feature. DAD Memory Address Multiplexing Signal. If CK is low, low addresses (or row addresses for the memory) are those that are output on DAD. The frequency of CK is a multiple of the image refresh frequency : - Interlaced scanning : f (CK) = f (1/2 frame) x (625 or 525) x 96 - Non-interlaced scanning : f (CK) = f (frame) x (312 or 262) x 96.
FMAT	I	8	Format	This pin is connected to V <sub>CC</sub> , V <sub>SS</sub> , CK or $\overline{CK}$ and sets the number of monitor and image lines : V <sub>CC</sub> : 625 line monitor, interlaced synchronization, 512 lines displayed CK : 525 line monitor, interlaced synchronization, 416 lines displayed $\overline{CK}$ : 525 line monitor, non-interlaced synchro, 208 lines displayed V <sub>SS</sub> : 625 line monitor, non-interlaced synchro, 256 lines displayed
WO	I	23	Write Only	When WO is high, memory refresh nor display no longer exist. The hard wired write processors may operate without being interrupted. The ALL signal is always high.

## SYNCHRONIZING AND BLANKING SIGNALS

Name	Pin Type	N°	Function	Description
SYNC	O	34	Video Monitor Synchronizing	Video Monitor Line and Frame Synchronization Signal. For example, if CK is at 1.5 MHz and FMAT is high, signal SYNC is to CCIR 625 line 50 Hz standard. This output is independent of input WO and of register CTRL1.
BLK	O	25	Blanking	This signal is high apart from the display window (writing or refresh). It is always high if bit 2 in register CTRL1 is high, but it is not affected by the WO input.
VB	O	16	Vertical Blanking	This signal is not affected by WO and register CTRL1. High during vertical blanking.

## DISPLAY MEMORY ADDRESSING SIGNALS

Name	Pin Type	N°	Function	Description
DAD0 to DAD6	O	37,39 38,4 3,2,5	Display Address	Addreses that are multiplexed by the CK signal. Provided for the automatic refresh of the 16 K or 64 K dynamic memories.
X9	O	19	Memory Address	Horizontal pointer extension bit for write operations (horizontal resolution greater than 512).
MSL0 to MSL3	2	6, 36 7, 35	Memory Select	Pixel write select signals (see section : <b>display memory configuration</b> ).
ALL	O	22	Access to all Memory Units	The signal makes it possible to discriminate between the collective memory access to all chips (display, refresh or erase), and the memory accesses to a single pixe for vector or character writing purposes. The signal is low for collective access.

## DISPLAY MEMORY CONTROL SIGNALS

Name	Pin Type	N°	Function	Description
DIN	O	15	Display In	Selection of the memory data code corresponding to the display screen in the "off " condition (active when high). For a black-and-white display (1 bit per pixel), DIN may directly be the storage entry data.
DW	O	14	Display Write	Display memory write signal. Active when Low.
MW	O	24	Memory Available	This pin outputs MFREE and WHITE signals which are externally demultiplexed by signal ALL : MFREE = MW + ALL ; WHITE = MW + ALL <b>Memory Free (MFREE) :</b> Signal low during the next memory idle period following the OF <sub>16</sub> command. This signal allows exchanges between the microprocessor and the X and the Y flagged memory segment without affecting the display. <b>Forcing to White Level (WHITE) :</b> Forces white level on video signal, for use of the light pen. Active when Low.

MICROPROCESSOR BUS SIGNALS

Name	Pin Type	N°	Function	Description
D0-D7	I/O	33 to 26	Data Bus	I/O buffers opening is controlled through $\bar{E}$ , and the related direction through R/W.
A0 - A3	I	9 to 12	Address Bus	Address of the register involved in microprocessor access.
$\overline{R/W}$	I	18	Read/Write Signal	Read/Write Signal. Write when Low.
$\bar{E}$	I	17	Enable	Bus exchange synchronizing and enabling signal.
$\overline{IRQ}$	O	13	Interrupt Request	Interrupt request towards the microprocessor, programmable through register CTRL1. Open drain output.

LIGHT PEN OPERATING SIGNALS

Name	Pin Type	N°	Function	Description
LPCK	I	21	Light Pen Strobe	Light Pen Input. When the Mechanism is set, a rising edge loads into registers XLP and YLP the current display address and sets the XLP register's LSB high.

REGISTER DESCRIPTION

X AND Y REGISTERS (addresses : 8<sub>16</sub>, 9<sub>16</sub>, A<sub>16</sub>, B<sub>16</sub>)

The X and Y registers are 12-bit read-write registers. They indicate the position of the next dot to be written into the display memory. They have no connection at all with the video signal generating scan, but they point the write address, in the same way as the pen address on a plotter.

These 2 registers are incremented or decremented, prior to each write operation into the display memory, by the internal vector and character generators, or they may be directly positioned by the microprocessor.

This 2 x 12 bit write address covers a 4096 x 4096 point addressing space. Only the LSBs are used here, since the maximum definition of the picture actually stored is 512 x 1024 pixels (picture elements).

In practice, the GDP assumes that it has a memory space of 1024 x 512 (FMAT = V<sub>CC</sub> or CK) or 1024 x 256 (FMAT = V<sub>SS</sub> or CK) and disables writing outside this space, unless bit 3 of CTRL 1 is set.

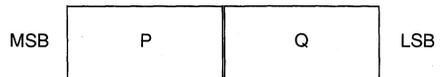
The above features along with the relative mode description of all picture component elements make it possible to automatically solve the great majority of edge cut-off problems.

DELTAX AND DELTAY REGISTERS (addresses 5<sub>16</sub>, 7<sub>16</sub>)

The DELTAX and DELTAY registers are 8-bit read-write registers. They indicate to the vector generator the projections of the next vector to be plotted, on the X and Y axes respectively. Such values are unsigned integers. The plotting of a vector is initiated by a write operation in the command register (CMD)

CSIZE REGISTER (address : 3<sub>16</sub>)

The CSIZE register is an 8-bit read-write register. It indicates the scaling factors of X and Y registers for the symbols and characters. 98 characters are generated from a 5 x 8 pixel matrix defined by an internal ROM. In the standard version, it contains the alphanumeric character in the ASCII code which may be printed, together with a number of special symbols.



Each symbol can be increased by a factor P(X) or Q(Y). These factors are independent integers which may each vary from 1 to 16 and which are defined by the CSIZE register. The symbol generation se-

quence is started after writing the ASCII code of the symbol to be represented in the CMD register.

#### CTRL1 REGISTER (address : 1<sub>16</sub>)

The CTRL1 register is a 7-bit read-write register, through which the general circuit operation may be fed with the required parameters.

Bit 0 : When low, this bit inhibits writing in display memory (equivalent to pen or eraser up).  
When high, this bit enables writing in display memory (pen or eraser down).  
This bit control the DW output.

Bit 1 : When low, this bit selects the eraser.  
When high, this bit selects the pen.  
This bit controls the DIN output.

Bit 2 : When low, this bit selects the normal writing mode (writing apart from the display and refresh periods, which are a requirement for the dynamic storages) in display memory.  
When high, this bit selects the high speed writing mode : the display periods are deleted. Only the dynamic storage refresh periods are retained.

Bit 3 : When low, this bit indicates that the 4096 x 4096 space is being used (the 12 X and Y bits are significant).  
When high, this bit selects the cyclic screen operating mode.

Bit 4 : When low, this bit inhibits the interrupt triggered by the light pen sequence completion.  
When high, this bit enables the interrupt.

Bit 5 : When low, this bit inhibits the interrupt release by vertical blanking.  
When high, this bit enables the interrupt.

Bit 6 : When low, this bit inhibits the interrupt indicating that the system is ready for a new command.  
When high, this bit enables the interrupt.

Bit 7 : Not used. Always low in read mode.

#### CTRL2 REGISTER (address : 2<sub>16</sub>)

The CTRL2 register is a 4-bit read-write register, through which the plotting of vectors and characters may be denoted by parameters.

Bit 0,1 : These 2 bits define 4 types of lines (continuous, dotted, dashed, dash-dotted).

Bit 2 : When low, this bit defines straight writing.  
When high, it defines tilted characters.

Bit 3 : When low, this bit defines writing along an horizontal line.  
When high, this bit defines writing along a vertical line.

Bit 4, 5, 6, 7 : Not used. Always low in read mode.

#### CMD COMMAND REGISTER (address : 0<sub>16</sub>)

The CMD register is an 8-bit write-only register. Each write operation in this register causes a command to be executed, upon completion of the time necessary for synchronizing the microprocessor access and the GDP's CK clock.

Several types of command are available :

- vector plotting
- character plotting
- screen erase
- light pen circuitry setting
- access to the display memory through an external circuitry
- indirect modification of the other registers (commands that make it possible for the X, Y, DELTAX, DELTAY, CTRL1, CTRL2, and CSIZE registers to be amended or scratched).

#### STATUS REGISTER (address 0<sub>16</sub>, F<sub>16</sub>)

The STATUS register is an 8-bit read-only register. It is used to monitor the status of the executing statements entered into the circuit, and more specifically to avoid the need for modifying a register that is already used for the command currently executing.

Bit 0 : When low, this bit indicates that a light pen sequence is currently executing.  
When high, it indicates that no light pen sequence is currently executing.

Bit 1 : This bit is high during vertical blanking. It is the VB signal recopy.

Bit 2 : When low, this bit indicates that a command is currently executing.

When high, this bit indicates that the circuit is ready for a new command.

Bit 3 : This bit when low indicates that registers X and Y are pointing within the assumed memory space.

This bit is obtained by applying the logical OR function to the unused most significant bits of registers X and Y.

If FMAT = V<sub>CC</sub> or CK, the assumed memory space is 1024 x 512.

If FMAT = V<sub>SS</sub> or CK, the assumed memory space is 1024 x 256.

Bit 4 : When high, this bit indicates that an interrupt has been initiated by the completion of a light pen running sequence and that this interrupt has been enabled by bit 4 in CTRL1 register.

Bit 5 : When high, this bit indicates that an interrupt has been initiated by vertical blanking and that

this interrupt has been enabled by bit 5 in CTRL1 register.

Bit 6 : When high, this bit indicates that an interrupt has been initiated by the completion of execution of a command and that this interrupt has been enabled by bit 6 in CTRL1 register.

Bit 7 : When high, this bit indicates that an interrupt has been initiated. It is the logic OR of bits 4, 5 and 6 in STATUS register. The IRQ output state is always the opposite of the status of this bit.

**Notes** : Bits 4, 5, 6 and 7 are reset low by reading the STATUS register at address 0<sub>16</sub>. Reading at address F<sub>16</sub> does not modify their state.

XLP AN YLP REGISTERS (addresses C<sub>16</sub> and D<sub>16</sub>)

The XLP and YLP registers are read-only registers, with 7 and 8 bits respectively. Upon completion of a high pen running sequence, they contain the display address sampled by the first edge appearing rising on the LPCK input. The use of such registers is discussed in section : **Use of light pen circuitry.**

**SYSTEM OPERATING PRINCIPLE**  
**DISPLAY MEMORY CONFIGURATION**

Assume a **V** x **H** pixel picture. Assume that each pixel is able to adopt 2<sup>b</sup> different states. A **V** x **H** x **b** bit display memory is thus required.

In those applications where **H** features a high value, the video signal frequency exceeds the maximum frequency of memory read access.

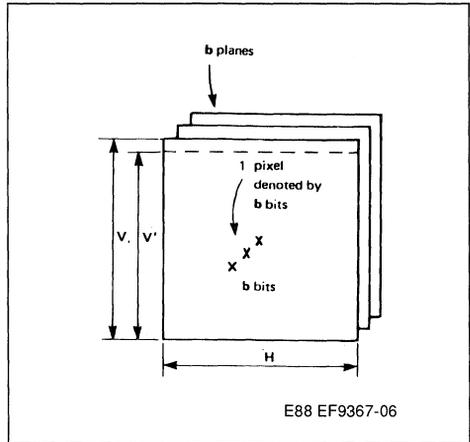
Example : **H** = 512 with a television line frequency : the pixel succession period on the video signal is 83 ns.

It is mandatory that a line of **H** dots be cut into **h** adjoining segments of **n** bits each, read at the same time in the display memory, and thereafter converted to serial form to produce the video signal, **h** memory accesses per line are necessary. Each access loads **b** **n**-bit shift registers. The memory contains **V** x **h** x **b** **n**-bit words.

**Notes** :1. All internal registers may be read or written at any time by the microprocessor. However, the precautions outlined below should be observed :

- Do not write into the CMD register if execution of the previous command is not completed (bit 2 of STATUS register).
- Do not alter any register if it is used as an input parameter for the internal hardwired systems (e.g. : modifying the DELTAX register while a vector plotting sequence is in progress).
- Do not read a register that is being asynchronously modified by the internal hardwired systems (e.g. : reading the X register while a vector plotting sequence is in progress may be erroneous if CK and E are asynchronous).

2. On powering up, the writing devices may have any status. Before entering a command for the first time, it is necessary to wait until all functions currently underway are completed, which information can be derived from the STATUS register.



The EF9367 is designed for the following stored image formats :

V = 512 or 256 (50 Hz)

V' = 416 or 208 (60 Hz)

H = h x n

H = 1024 or lower multiples of 64

h = 64

n = 16, 8, 4, 2, 1 (or any value below 16 using external PROM encoding)

b = any value (addressing is same for all memory planes, management of these planes is external to the GDP).

In so far as the overflow tests are concerned, the

circuit assumes that it still has the maximum memory space for X (1024) . The test for Y is effected in the following memory spaces :

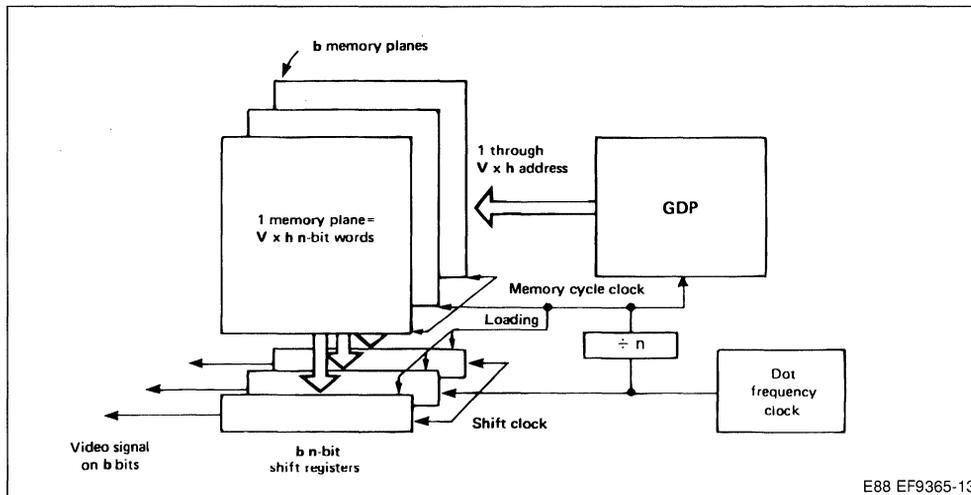
512 if FMAT = V<sub>CC</sub> or  $\overline{CK}$

256 if FMAT = V<sub>SS</sub> or CK

**512 or 256 vertical resolution** : the displayed space is identical to the space in memory (unless a greater memory capacity is deliberately selected).

**416 or 208 vertical resolution** : the displayed space is smaller than the memory space.

Lines not displayed are displayable using an external adder to dejustify the display addresses (this arrangement may be used for smooth roll-up/roll down).



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**DAD AND MSL STATUS TABLE**

The internal counters which address the display memory are made up of :

- 6 horizontal address bits (h = 64)  
h<sub>0</sub>, h<sub>1</sub>, h<sub>2</sub>, h<sub>3</sub>, h<sub>4</sub>, h<sub>5</sub>, (h<sub>0</sub> = LSB)

- 9 vertical address bits (V ≤ 512)  
t, V<sub>0</sub>, V<sub>1</sub>, V<sub>2</sub>, V<sub>3</sub>, V<sub>4</sub>, V<sub>5</sub>, V<sub>6</sub>, V<sub>7</sub>

t is here the LSB. It denotes the line parity and changes every frame because of interlaced scan. Within a same frame, V<sub>0</sub> denotes the LSB.

FMAT = V<sub>CC</sub> or CK

		MSL				X <sub>9</sub>	DAD						
ALL	CK	0	1	2	3		0	1	2	3	4	5	6
0	0	X <sub>0</sub>	X <sub>1</sub>	X <sub>2</sub>	V <sub>1</sub>	X <sub>9</sub>	h <sub>5</sub>	h <sub>4</sub>	h <sub>3</sub>	h <sub>2</sub>	h <sub>1</sub>	h <sub>0</sub>	V <sub>0</sub>
0	1	X <sub>0</sub>	X <sub>1</sub>	X <sub>2</sub>	V <sub>1</sub>	X <sub>9</sub>	V <sub>7</sub>	V <sub>6</sub>	V <sub>5</sub>	V <sub>4</sub>	V <sub>3</sub>	V <sub>2</sub>	t
1	0	X <sub>0</sub>	X <sub>1</sub>	X <sub>2</sub>	Y <sub>2</sub>	X <sub>9</sub>	X <sub>8</sub>	X <sub>7</sub>	X <sub>6</sub>	X <sub>5</sub>	X <sub>4</sub>	X <sub>3</sub>	Y <sub>1</sub>
1	1	X <sub>0</sub>	X <sub>1</sub>	X <sub>2</sub>	Y <sub>2</sub>	X <sub>9</sub>	Y <sub>8</sub>	Y <sub>7</sub>	Y <sub>6</sub>	Y <sub>5</sub>	Y <sub>4</sub>	Y <sub>3</sub>	Y <sub>0</sub>

The write address is made up of the LSBs of the X and Y internal registers.

X<sub>0</sub>, X<sub>1</sub>, X<sub>2</sub>, X<sub>3</sub>, X<sub>4</sub>, X<sub>5</sub>, X<sub>6</sub>, X<sub>7</sub>, X<sub>8</sub>, X<sub>9</sub>  
Y<sub>0</sub>, Y<sub>1</sub>, Y<sub>2</sub>, Y<sub>3</sub>, Y<sub>4</sub>, Y<sub>5</sub>, Y<sub>6</sub>, Y<sub>7</sub>, Y<sub>8</sub>

The GDP produces addressing signals in the sequences shown in the following tables :

FMAT = V<sub>SS</sub> or  $\overline{CK}$

		MSL				X <sub>9</sub>	DAD						
ALL	CK	0	1	2	3		0	1	2	3	4	5	6
0	0	X <sub>0</sub>	X <sub>1</sub>	X <sub>2</sub>	1	X <sub>9</sub>	h <sub>5</sub>	h <sub>4</sub>	h <sub>3</sub>	h <sub>2</sub>	h <sub>1</sub>	h <sub>0</sub>	V <sub>0</sub>
0	1	X <sub>0</sub>	X <sub>1</sub>	X <sub>2</sub>	1	X <sub>9</sub>	V <sub>7</sub>	V <sub>6</sub>	V <sub>5</sub>	V <sub>4</sub>	V <sub>3</sub>	V <sub>2</sub>	V <sub>1</sub>
1	0	X <sub>0</sub>	X <sub>1</sub>	X <sub>2</sub>	1	X <sub>9</sub>	X <sub>8</sub>	X <sub>7</sub>	X <sub>6</sub>	X <sub>5</sub>	X <sub>4</sub>	X <sub>3</sub>	Y <sub>0</sub>
1	1	X <sub>0</sub>	X <sub>1</sub>	X <sub>2</sub>	1	X <sub>9</sub>	Y <sub>7</sub>	Y <sub>6</sub>	Y <sub>5</sub>	Y <sub>4</sub>	Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>

DESCRIPTION OF DISPLAYABLE FORMATS

**Non Interlacing Scanning**

**256 x 512 or 208 x 512 pixel formats (H = 512, n = 8).** Input FMAT must be low or connected to CK.

The memory is made up of 16 K bytes per memory plane. The byte address is made up of 14 bits which are output on two runs on the DAD pins. The three MSL0, MSL1, MSL2 outputs are used to select one pixel out of the eight featuring the same address. They issue the number of the pixel, encoded on three bits. MSL3 is high, and is not used.

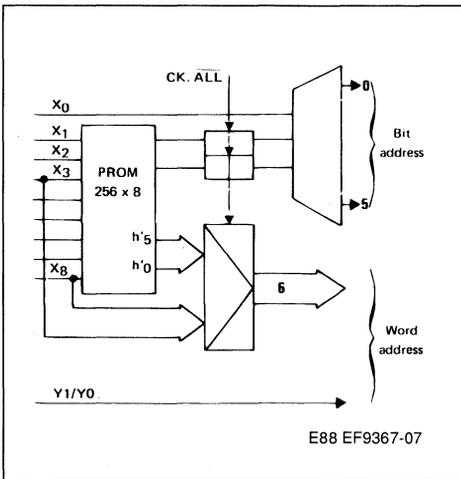
**256 x 384 or 208 x 384 pixel formats (H = 384, n = 6).** Input FMAT must be low or connected to CK. The memory is organized as 16 K words x 6 bits.

The signals produced by the chip in the sequence indicated for the 256 x 512 format are transcoded externally as shown in the opposite diagram.

**256 x 320 or 208 x 320 pixel formats (H = 320, n = 5).** The same schematic as for 384 horizontal resolution should be used with a memory organized in 5 bit words.

**256 x 256 or 208 x 256 pixel formats (H = 256, n = 4).** Input FMAT must be low or connected to CK.

The memory is made up of 16 K words x 4 bits. The word address up of 14 bits which are output in two runs on the DAD pins. One of the four chips is selected by decoding pins MSL1 and MSL2 (that leads to ignore X<sub>0</sub> : the X computation space is changed to 2048 pixels horizontal overflow detected at 512 pixels).



**Interlaced Scanning**

**512 x 1024 or 416 x 1024 pixel formats (H = 1024, n = 16).** Input FMAT must be connected to V<sub>CC</sub> or CK

The memory comprises 32 K words x 16 bits, organized in two blocks of 16 K words each.

The signals produced by the circuit in the sequence indicated for the 512 x 512 format are combined externally as shown at the end of the data sheet.

**512 x 768 or 416 x 768 pixel formats (H = 768, n = 12).** Input FMAT must be connected to V<sub>CC</sub> or CK. The memory comprises 32 K words x 12 bits, organized in two blocks of 16 K words each.

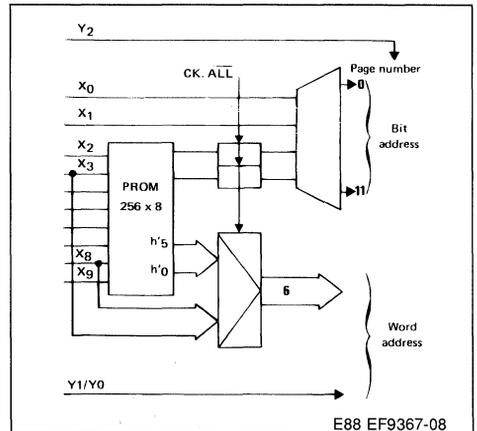
The signals produced by the chip in the sequence indicated for the 512 x 512 format are transcoded externally as shown in the diagram below.

**512 x 640 or 416 x 640 pixel formats (H = 640, n = 10).** The same schematic as below should be used with a memory organized in 10 bit words.

**512 x 512 or 416 x 512 pixel formats (H = 512, n = 8).** The FMAT input should be tied to V<sub>CC</sub> or CK. The memory is made up of V x h bytes = 32 K bytes per memory plane.

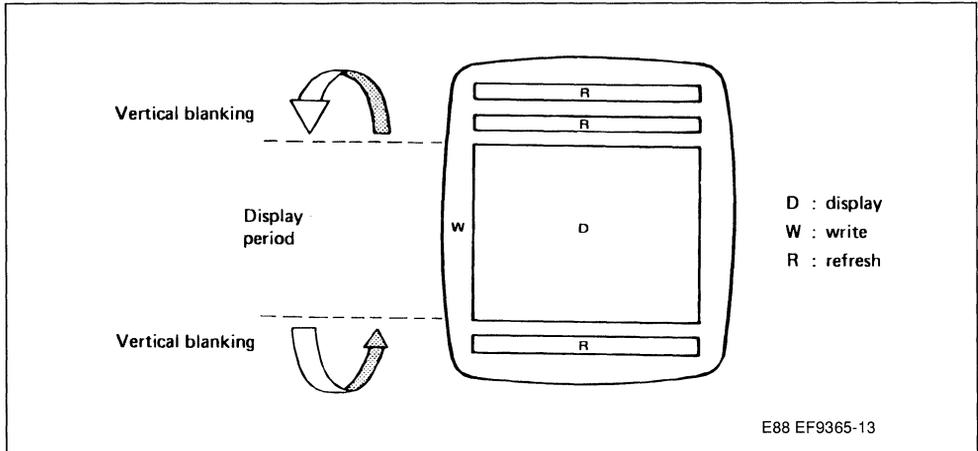
- The byte address is made up of 15 bits :
- 14 are output in 2 runs on the DAD pins for the purpose of using 16 K x 1 bit dynamic RAMs.
  - the 15th one is output on pin MLS3.

The MLS0, 1 and 2 outputs allow to select one pixel out of the 8 featuring the same address, for pixel-to-pixel write applications. They issue the number of the involved pixel, encoded on 3 bits.



## MEMORY OPERATION SEQUENCE ALONG ONE FRAME

Apart from the window where the memory is used for display purposes exclusively, write operations may be performed, except during 3 refresh periods.



The three period types, D, W and R, respectively, are indicated outside the circuit through the BLK and ALL signals :

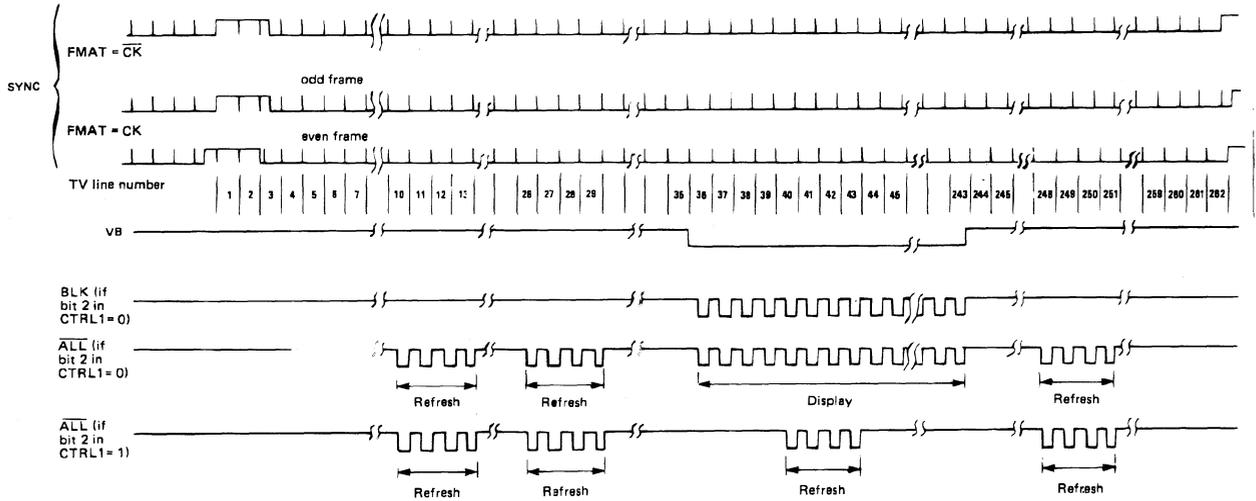
	BLK	ALL
D	0	0
W	1	1
R	1	0

The refresh of dynamic RAMs is automatically performed by the GDP. During display, the memory is entirely refreshed each 4 lines (256 accesses). During vertical blanking, 3 refresh cycles of 4 lines each are executed.

**Exceptions :**

- If bit 2 in register CTRL1 is high (high speed write), the display period is suppressed and 19 refresh cycles of 4 lines each are executed during one frame.
- As long as the WO input is high, the circuit is set to write mode, and BLK retains the same outline as it has under normal operating conditions.

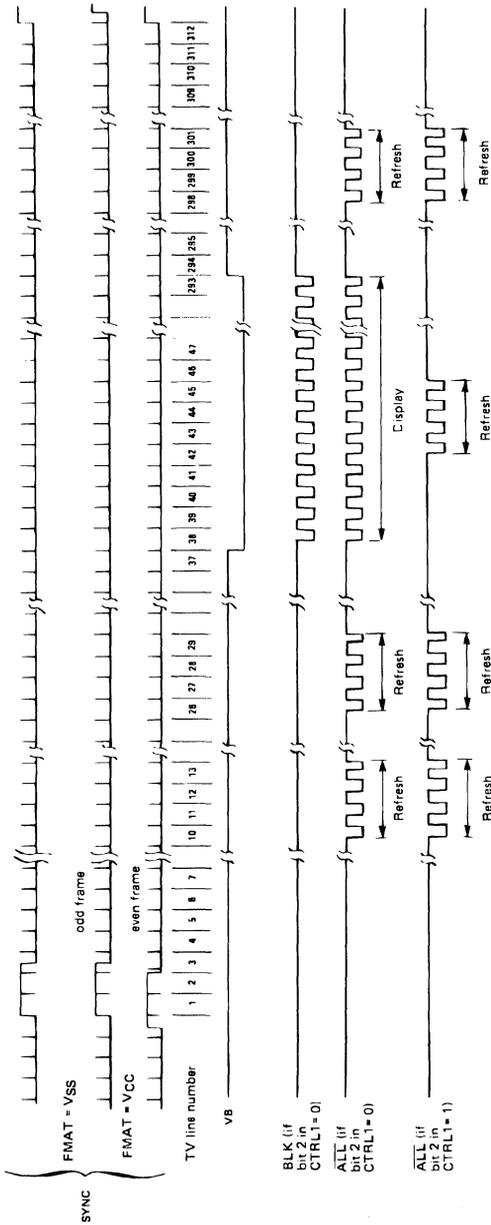
In these two cases, executing codes 04<sub>16</sub>, 06<sub>16</sub>, 07<sub>16</sub> and 0C<sub>16</sub> triggers a complete D sequence for a high-speed scan of all addresses. This last two frames if FMAT is high (or tied to CK) and one frame if FMAT is low (or tied to CK).



Note : ALL signal high denotes write periods.

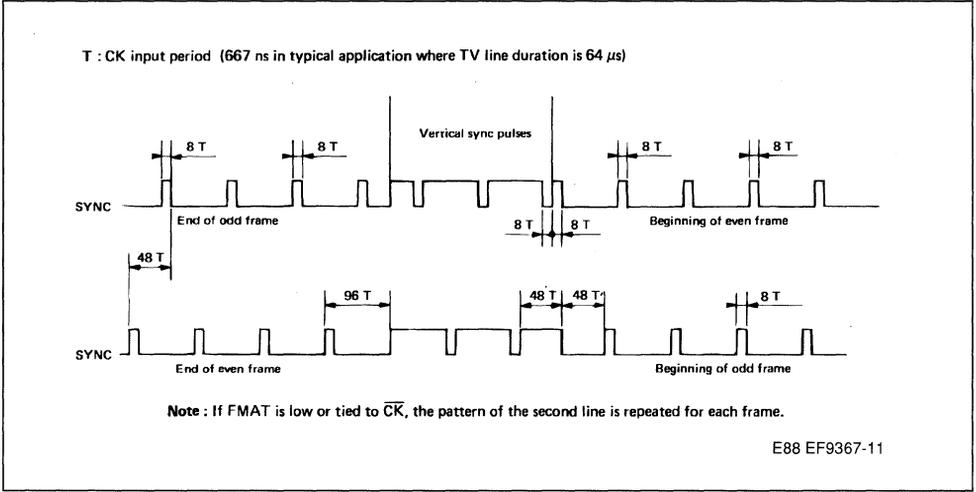
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FRAME SEQUENCE - 625 LINE SYNCHRONIZATION

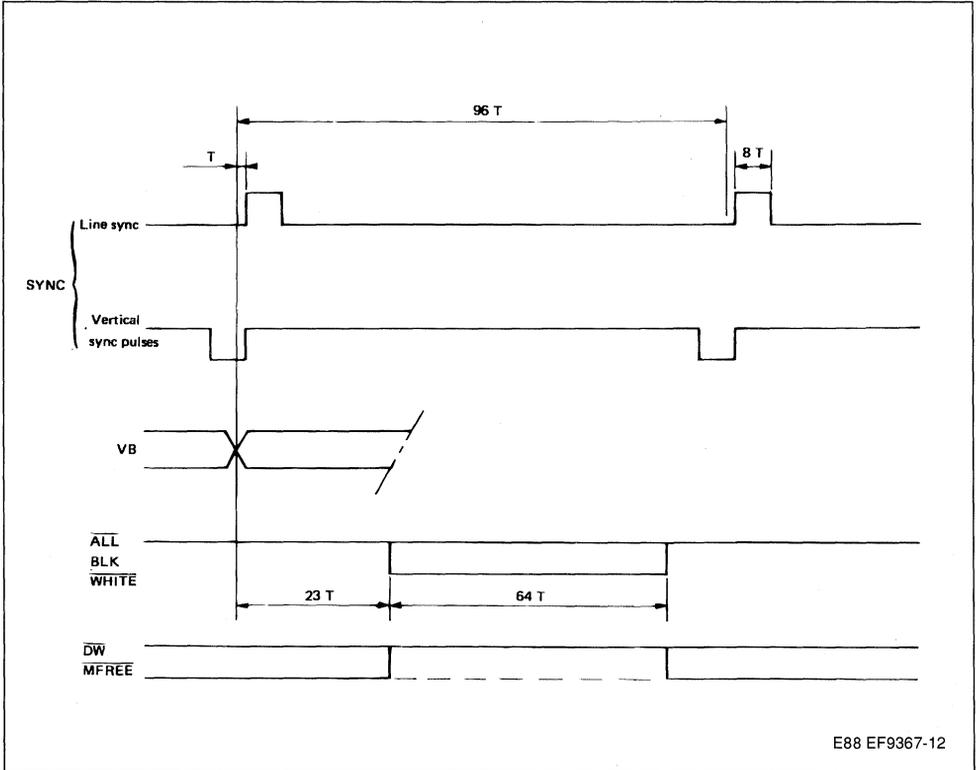


Note : ALL signal high denotes write periods.

COMPOSITE SYNC AROUND FRAME SYNC



DETAILED LINE DIAGRAM



**HARDWIRED WRITE PROCESSOR OPERATION IN DISPLAY MEMORY**

The hardwired write processors are sequenced by the master clock CK. They receive their parameters from the microprocessor bus. They control the X, Y write address, and the DIN, DW, MW and IRQ outputs.

These hardwired processors operate in continuous mode. In the event of conflicting access to the display memory, the display and refresh processors have priority.

Since command decoding is synchronous with the CK master clock, any write operation into the (CMD) command register triggers a synchronizing mechanism which engages the circuit for a maximum of 2 CK cycles when the  $\bar{E}$  input returns high. The circuit remains engaged throughout command execution.

No further command should be entered as long as bit 2 in STATUS register is low.

**VECTOR PLOTTING**

The internal vector generator makes it possible to modify, within the display memory, all the dots which form the approximation of a straight line segment. All vectors plotted are described by the origin dot and the projections on the axes.

The starting point co-ordinates are defined by the X, Y register value, prior to the plotting operation.

Projections onto the axes are defined as absolute values by the DELTAX and DELTAY registers, with the sign in the command byte that initiates the vector plotting process.

The vector approximation achieved here is that established by J.F. BRESENHAM ("Algorithm for computer control of a digital plotter"). This algorithm is executed by a hardwired processor which allows for a further vector component dot to be written in each CK clock cycle.

During plotting, the display memory is addressed by the X, Y registers, which are incremented or decremented.

On completion of vector plotting, they point to the end of this vector.

All vectors may be plotted using any of the following line patterns : continuous, dotted, dashed, dash-dotted, according to the 2 LSBs in register CTRL2.

Irrespective of such patterns, the plotting speed remains unchanged. The "pen down-pen up" statement required for plotting non-continuous lines is controlled by the DW output.

For a specified non-continuous line plotted vector, defined by DELTAX, DELTAY, CTRL2, CMD, the

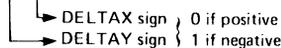
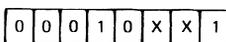
DW sequencing during the plotting process is always the same, irrespective of vector origin and of the nature of previous plots. This feature guarantees that a specified vector can be deleted by plotting it again after moving X and Y to the starting point, and complementing bit 1 in register CTRL 1.

Since the vector plotting initiation command defines the sign of the projections onto the axes, all vectors may be plotted using 4 different commands.

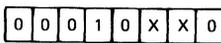
For increased programming flexibility, the system incorporates 16 different commands, supplemented by a set of 128 commands which make it possible to plot small size vectors by ignoring the DELTAX and DELTAY registers.

Such commands are as follows :

- Basic commands

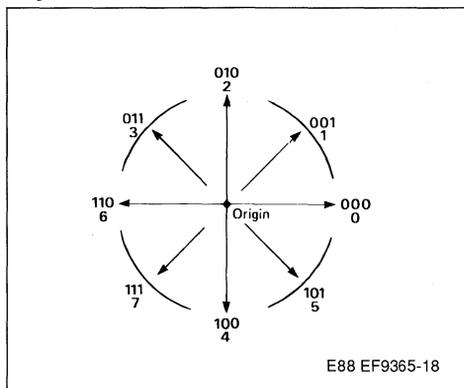


- commands which allow ignoring the DELTAX or DELTAY registers by considering them as zero value



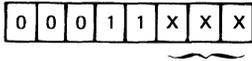
**Notes :** Bits 1 and 2 always have the same sign meaning.

These 8 codes may be summarized by the following diagram :



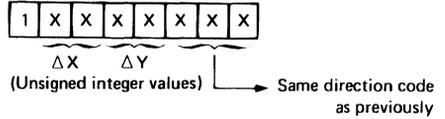
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- Commands which allow ignoring the smaller of the two DELTAX and DELTAY registers, by considering it as being equal to the larger one, which is the same as plotting vectors parallel to the axes or diagonals, using a single DELTA register.



Same direction codes as above.

- Commands in which the two registers DELTAX and DELTAY may be ignored by specifying the projections through the CMD register (0 to 3 steps for each projection).



EXAMPLE : PLOTTING A DOTTED VECTOR

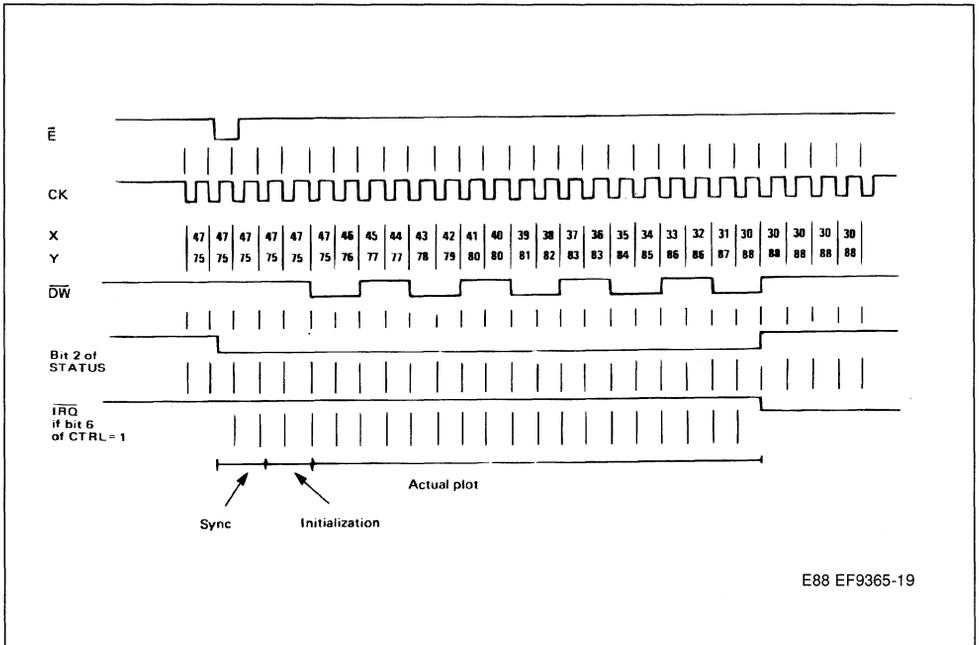
Origin :  $\left\{ \begin{array}{l} X = 47_{10} \\ Y = 75_{10} \end{array} \right.$

Projection :  $\left\{ \begin{array}{l} \text{DELTA } X = 17_{10} \\ \text{DELTA } Y = 13_{10} \end{array} \right.$

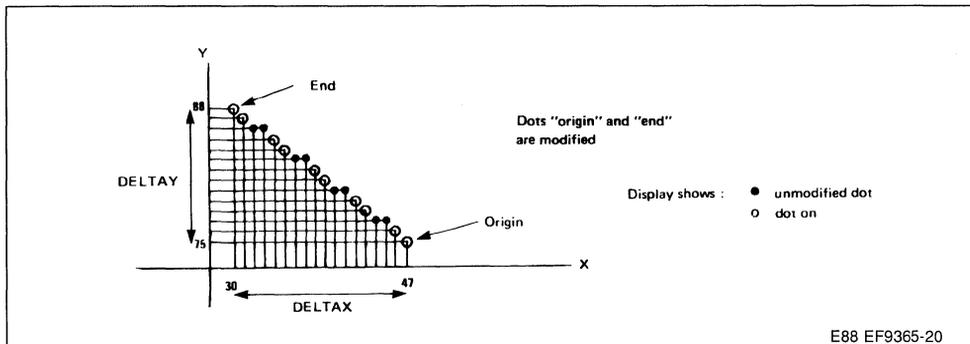
CMD = 13<sub>16</sub> Corresponding to  
 - Basic command  
 - DELTAX < 0  
 - DELTAY > 0

CTRL1 = 03<sub>16</sub> Pen down,  
 CTRL2 = 116 Dotted vector :  
 2 dots on,  
 2 dots off.

**Plotting cycle sequence :** (it is assumed that the vector generator is not interrupted by the display or refresh cycle).



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**Note :** Plotting a vector with DELTAX = DELTAY = 0 writes the dot X, Y in memory. It occupies the vector generator for synchronization, initialization and one write cycle.

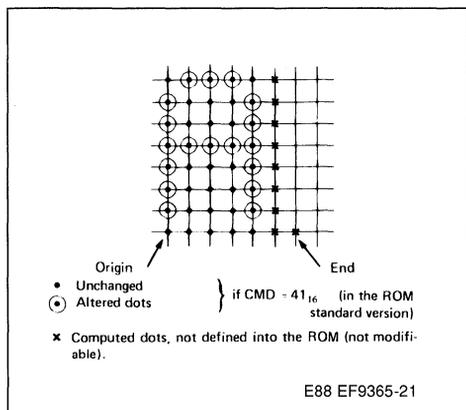
**CHARACTER AND SYMBOL GENERATOR**

The character generator operates in the same way as the vector generator, i.e. through incrementing or decrementing the X, Y registers, in conjunction with a DW output control.

It receives parameters from the CSIZE, CTRL2 and CMD registers. The characters plotted are selected, according to the CMD value, out of 98 matrices (97 8-dot high x 5-dot wide rectangular matrices, and one 4 dot x 4 dot matrix) defined in an internal ROM. Two scaling factors may be applied to the characters plotted using X and Y defined by the CSIZE register. The characters may be tilted, according to the content of register CTRL2.

**BASIC MATRIX**

Upon completion of a character writing process, the X and Y registers are positioned for writing a further character next to the previous one, with a 1 dot spacing, i.e. Y is restored to its original value and X is incremented by 6.



**SCALING FACTORS**

Each individual dot in the 5 x 8 basic matrix may be replaced by a P x Q size block.

P : X co-ordinate scaling factor

Q : Y co-ordinate scaling factor

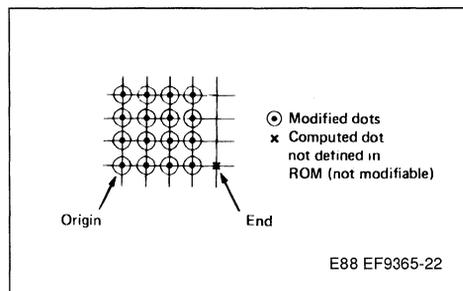
The character size becomes 5 P x 8 Q. Upon completion of the writing process, X is incremented by 6P. The CK clock cycle count required is 6 P x 8 Q.

P and Q may each take values from 1 through 16. They are defined by the CSIZE register. Each value is encoded on 4 bits, value 16 being encoded as 0<sub>16</sub>.

In register CSIZE, P is encoded on the 4 MSBs and Q on the 4 LSBs.

Among the 97 rectangular matrices available in the standard ROM, 96 correspond to CMD values ranging from 20<sub>16</sub> to 7F<sub>16</sub>, and the 97th matrix to 0A<sub>16</sub>. In the standard version, these values correspond to the 96 printable characters in the ASCII set. The 97th character is a 5 P x 8 Q block which may be used for deleting the other characters.

The 98th code (0B<sub>16</sub>) is used to plot a 4 P x 4 Q graphic block. It locates X, Y, without spacing for the next symbol. Such a block makes it possible to pad uniform areas on the screen.



TILTED CHARACTERS

All characters may be modified to produce tilted characters or to mark the vertical co-ordinate with straight or tilted type symbols. Such changes may be achieved using bits 2 and 3 in register CTRL2.

**Note :** Scaling factors P and Q are always applied within the co-ordinates of the character before conversion.

CHARACTER DELETION

A character may be deleted using either the same command code or command code 0A<sub>16</sub>. In either case, bit 1 in register CTRL1 should be inverted, the origin should be the same as prior to a character plotting operation, as should the scaling factors.

**Note :** Vector generator and character generator operate in similar ways :

	Vector	Character
Dimensions	DELTA <sub>X</sub> , DELTA <sub>Y</sub>	CSIZE, tilting
DW Modulation	Type of Line	Character Code

USE OF LIGHT PEN CIRCUITRY

A rising edge on the LPCK input is used to sample the current display address in the XLP and YLP registers, provided, that this edge is present in the frame immediately following loading of the 08<sub>16</sub> or 09<sub>16</sub> code into the CMD register.

Here, the frame origin is counted starting with the VB falling edge. With code 08<sub>16</sub>, the MW output recopies the BLK signal from the frame origin up to the rising edge on the LPCK input, or when VB starts rising again, if the LPCK input remains low for the entire frame. With code 09<sub>16</sub>, the MW output is not activated.

The YLP address is 8-bit coded since there are 256 display lines in each frame. The XLP address is 6-bit coded since there are 64 display cycles in each line.

These 6 bits left-justified in register XLP indicate the number of the segment (h = 0 to 63) to which the point indicated by the light pen belongs.

The address sampled into XLP corresponds to the current memory cycle. Dots detected by the light pen were addressed in the memory during the previous cycle. Hence, 1 should be subtracted from bit 2 in XLP register where the light pen electronic circuitry does not produce any additional delay.

If the rising edge on input LPCK occurs while VB is low, then the LSB in XLP is set high is set high. This bit acts as a status signal which is reset to the low state by reading register XLP or YLP.

The rising edge first received (LPCK or VB) sets bit 0 in STATUS register high. An interrupt is initiated if bit 4 in CTRL1 is high.

When commands 08<sub>16</sub> or 09<sub>16</sub> have been decoded, bit 2 of the status register goes high (circuit ready for any further command) and bit 0 goes low (light pen operating sequence underway).

SCREEN BLANKING COMMANDS

Three commands (04<sub>16</sub>, 06<sub>16</sub>, 07<sub>16</sub>) will set the whole display memory to a status corresponding to a "black display screen", condition. Another command (0C<sub>16</sub>) may be used to set the whole memory to a status other than black (this condition being determined by bit 1 in register CTRL1).

The 4 commands outlined above use the planned scanning of the memory addresses achieved by the display stage. The X and Y registers are not affected by commands 04<sub>16</sub> and 0C<sub>16</sub>. Hence, the time required is that corresponding to one frame (FMAT = 0 or CK) or two frames (FMAT = 1 or CK). The time corresponding to the completion of the frame currently executing when the CMD register is loaded, should be added to the above time.

For the screen blanking process, the frame origin is counted starting with the VB falling edge.

The only signals affected here are the DW output, which remains low when VB is low, and the DIN output which is forced high where the 04<sub>16</sub>, 06<sub>16</sub> and 07<sub>16</sub> commands are entered.

Such commands are activated without requiring action by WO input or bit 2 in register CTRL1. While these commands are executing, bit 2 in STATUS register remains low.

EXTERNAL REQUEST FOR DISPLAY MEMORY ACCESS (MW output)

One writing code 0F<sub>16</sub> into the CMD register, the MW output is set low by the circuitry, during the next free memory cycle.

Apart from the display and refresh periods, this cycle is the first complete cycle that occurs after input E is reset high.

During this cycle, those addresses output on DAD and MSL correspond to the X and Y register contents : DW is high, ALL is high.

Should the memory be engaged in a display or refresh operation, (which is the case when ALL is low), then this cycle is postponed to be executed after ALL is reset high. The maximum waiting time is thus 64 cycles.

The MW signal may be used e.g. for performing a read or write operation into a register located be-

tween the display memory and the microprocessor bus.

### INTERRUPTS OPERATION

An interrupt may be initiated by three situations denoted by internal signals :

- Circuit ready for a further command.
- Vertical blanking signal.
- Light pen sequence completed.

These three signals appear in real time in the STATUS register (bits 0, 1, 2). Each signal is cross-referenced to a mask bit in the register CTRL1 (bits 4, 5, 6).

If the mask bit is high, the first rising edge that occurs on the interrupt initiating signal sets the related interrupt flip-flop circuit high.

The outputs from these three flip-flop circuits appear

in the STATUS register (bits 4, 5, 6). If one flip-flop circuit is high, bit 7 in the STATUS register is high, and pin IRQ is forced low.

A read operation in the STATUS register at address 0<sub>16</sub> resets its 4 MSBs low, after input  $\bar{E}$  is reset high (a read at address F<sub>16</sub> maintains their value).

The three interrupt control flip-flops are duplicated to prevent of an interrupt coming during a read cycle of the STATUS register.

The status of bits 4, 5 and 6 corresponds to the interrupt control flip-flop circuit output, before input  $\bar{E}$  goes low.

An interrupt coming during a read cycle of the STATUS register does not appear in bits 4, 5 and 6 during this read sequence, but during the following one. However, it may appear in bits 0, 1, 2 or on pin IRQ.

**Table 1** : Register Address.

Address Register					Register Functions		Number of Bits
Binary				Hexa	Read R/W = 1	Write R/W = 0	
A3	A2	A1	A0				
0	0	0	0	0	STATUS	CMD	8
0	0	0	1	1	CTRL 1 (Write Control and Interrupt Control)		7
0	0	1	0	2	CTRL 2 (Vector and Symbol Type Control)		4
0	0	1	1	3	CSIZE (Character Size)		8
0	1	0	0	4	Reserved		–
0	1	0	1	5	DELTA X		8
0	1	1	0	6	Reserved		–
0	1	1	1	7	DELTA Y		8
1	0	0	0	8	X MSBs		4
1	0	0	1	9	X LSBs		8
1	0	1	0	A	Y MSBs		4
1	0	1	1	B	Y LSBs		8
1	1	0	0	C	XLP (light-pen)	Reserved	7
1	1	0	1	D	YLP (light-pen)	Reserved	8
1	1	1	0	E	Reserved		–
1	1	1	1	F	STATUS	Reserved	8

Reserved : These addresses are reserved for future versions of the circuit. In read mode, output buffers D0-D7 force a high state on the data bus.

**Table 2 : Command Register.**

b7	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
b6	0	0	0	0	1	1	1	1	1	0	0	1	1	0	1	1	1
b5	0	0	1	1	0	0	1	1	1	0	0	1	1	0	0	1	1
b4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
b3 b2 b1 b0	0	1	2	3	4	5	6	7		8	9	A	B	C	D	E	F
<b>Vector Generation</b> (for b2, b1, b0 see small vector definition)																	
0 0 0 0	0	Set Bit 1 of CTRL 1 : Pen Selection	Space	0	@	P	`	p									
0 0 0 1	1	Clear Bit 1 of CTRL 1 : Eraser selection	!	1	A	Q	a	q									
0 0 1 0	2	Set Bit 0 of CTRL 1 : Pen/Eraser Down Selection	"	2	B	R	b	r									
0 0 1 1	3	Clear Bit 0 of CTRL 1 : Pen/Eraser up Selection	#	3	C	S	c	s									
0 1 0 0	4	Clear screen	\$	4	D	T	d	t									
0 1 0 1	5	X and Y Registers Reset to 0	%	5	E	U	e	u									
0 1 1 0	6	X and Y Reset to 0 and Clear Screen	&	6	F	V	f	v									
0 1 1 1	7	Clear Screen, set CSIZE to code "minsize". All other registers reset to 0. (except XLP, YLP)	'	7	G	W	g	w									
<b>Special Direction Vectors</b> (for b2, b1, b0 see small vector definition)																	
1 0 0 0	8	Lignt-pen initialization (WHITE forced low)	(	8	H	X	h	x									
1 0 0 1	9	Lignt-Pen initialization	)	9	I	Y	i	y									
1 0 1 0	A	5 x 8 Block Drawing (size according to CSIZE)	*	:	J	Z	j	z									
1 0 1 1	B	4 x 4 Block Drawing (size according to CSIZE)	+	;	K	[	k	{									
1 1 0 0	C	Screen Scanning : Pen or Eraser as defined by CTRL1	,	<	L	\	l										
1 1 0 1	D	X Register Reset to 0	-	=	M	]	m	}									
1 1 1 0	E	Y Register Reset to 0	.	>	N	↑	n	¬									
1 1 1 1	F	Direct Image Memory access request for the next free cycle.	/	?	O	←	o	⊗									

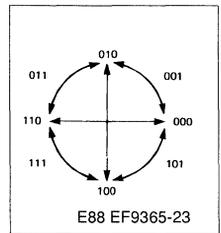
**SMALL VECTOR DEFINITION**

b7	b6 b5	b4 b3	b2 b1 b0
1	ΔX	ΔY	Direction

**DIMENSION**

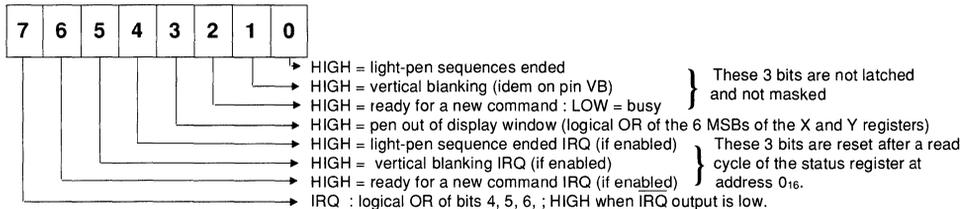
ΔX or ΔY	Vector Length
0 0	0 Step
0 1	1 Step
1 0	2 Steps
1 1	3 Steps

**DIRECTION**

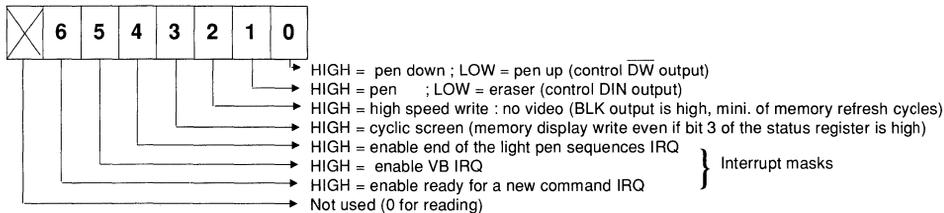


**OTHER REGISTERS**

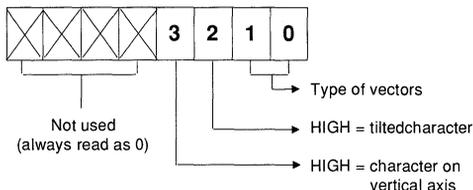
**STATUS REGISTER (read only)**



**CONTROL REGISTER 1 (read/write)**

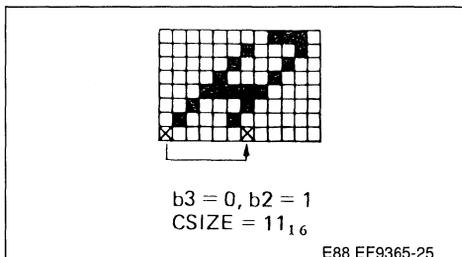
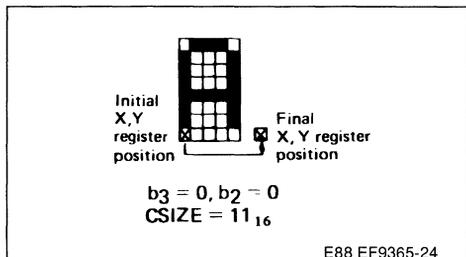


**CONTROL REGISTER 2 (read/write)**

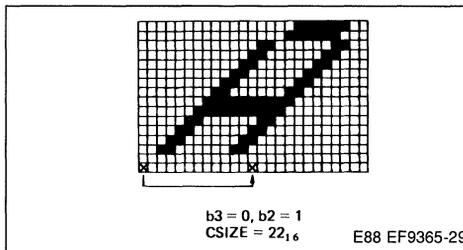
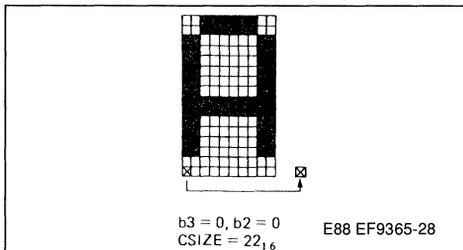
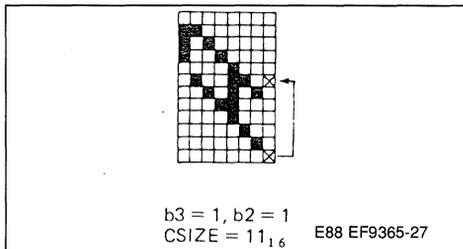
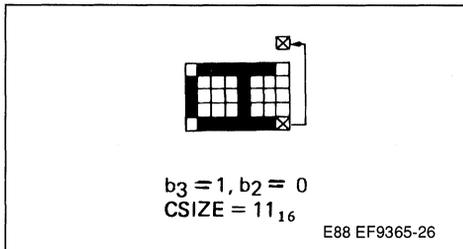


b1	b0	Type of Vectors
0	0	Continuous
0	1	Dotted 2 dots on, 2 dots off
1	0	Dashed 4 dots on, 4 dots off
1	1	Dotted-Dashed 10 dots on, 2 dots off
		Dashed 2 dots on, 2 dots off

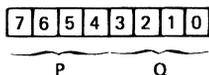
**Types of character orientations**



Types of character orientations



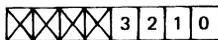
C-SIZE REGISTER (read/write)



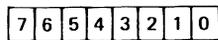
P : Scaling factor on X axis  
 Q : Scaling factor on Y axis

P and Q may take any value between 1 and 16. This value is given by the leftmost or rightmost 4 bits for P and Q respectively. Binary value (0) means 16.

X AND Y REGISTERS (read/write)



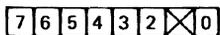
MSBs



LSBs

The 4 leftmost MSBs are always 0.

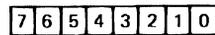
XLP and YLP REGISTERS



Status bit indicating if a rising edge has been applied on LPCR during the first complete frame following light-pen initialization. This bit is reset by a read on XLP or YLP.

always 0

6 bit XLP value



8 bit YLP value

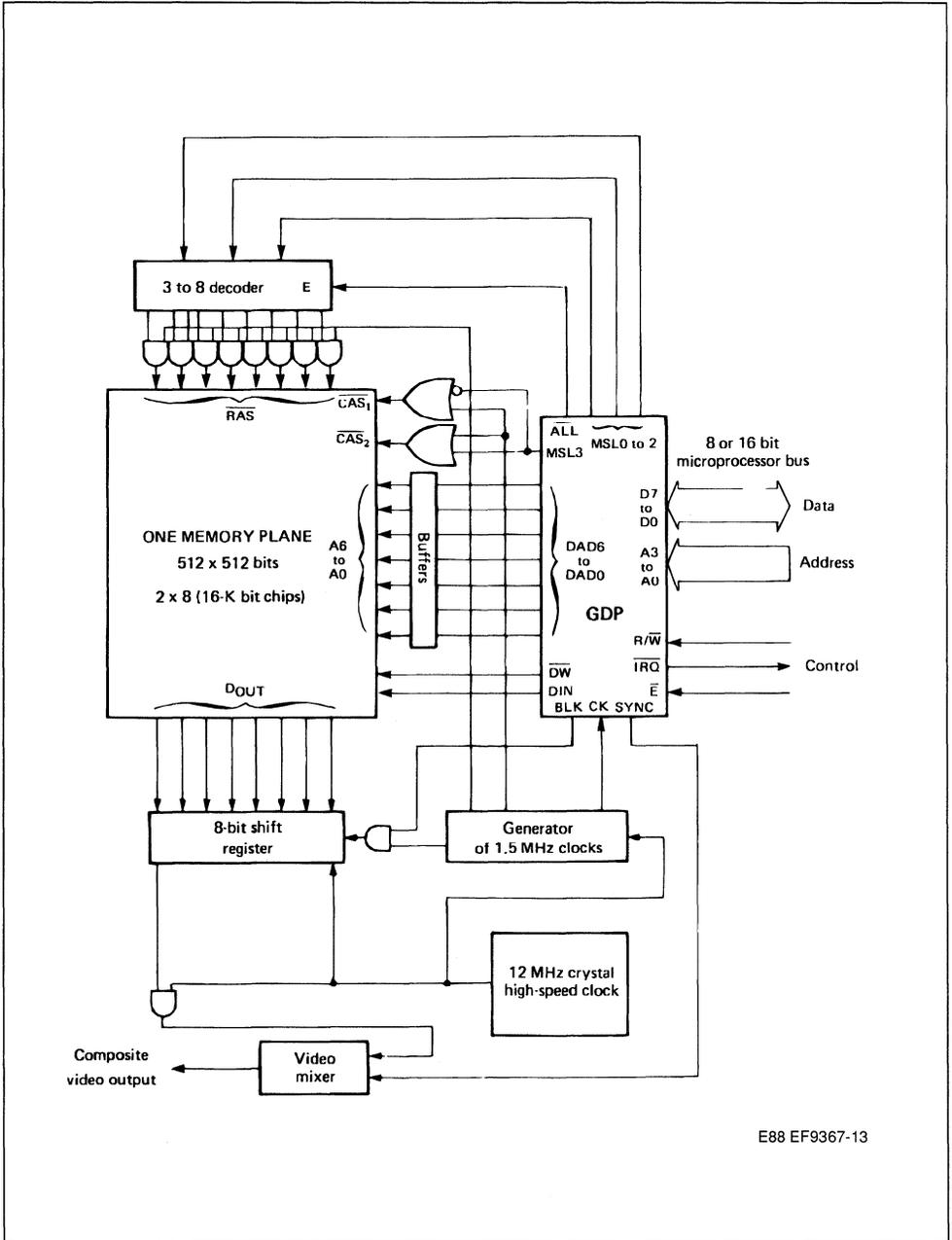
ASCII CHARACTER GENERATOR (5 x 8 matrix)

b7	0	0	0	0	0	0
b6	0	0	1	1	1	1
b5	1	1	0	0	1	1
b4	0	1	0	1	0	1

b3	b2	b1	b0						
0	0	0	0						
0	0	0	1						
0	0	1	0						
0	0	1	1						
0	1	0	0						
0	1	0	1						
0	1	1	0						
0	1	1	1						
1	0	0	0						
1	0	0	1						
1	0	1	0						
1	0	1	1						
1	1	0	0						
1	1	0	1						
1	1	1	0						
1	1	1	1						

E88 EF9365-30

EXAMPLE OF A MONOCHROME APPLICATION : 512 x 512 or 416 x 512

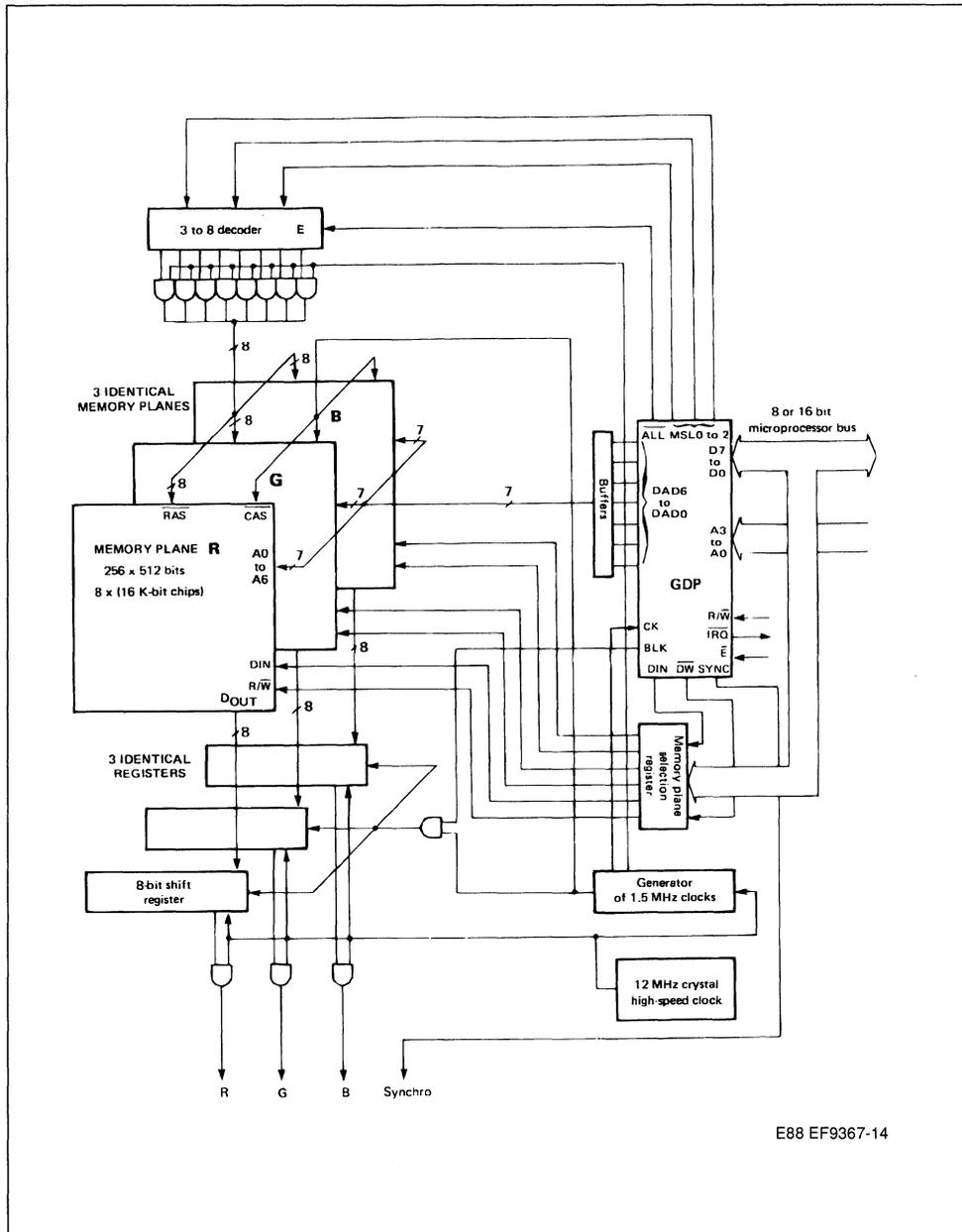


E88 EF9367-13

Notes : F<sub>MAT</sub> = V<sub>CC</sub> : 512 x 512 resolution - 50 Hz 625 line non interlaced scanning.  
 F<sub>MAT</sub> = CK : 416 x 512 resolution - 60 Hz 525 line non interlaced scanning.

EXAMPLE OF A COLOR APPLICATION : 208 x 512 or 256 x 512

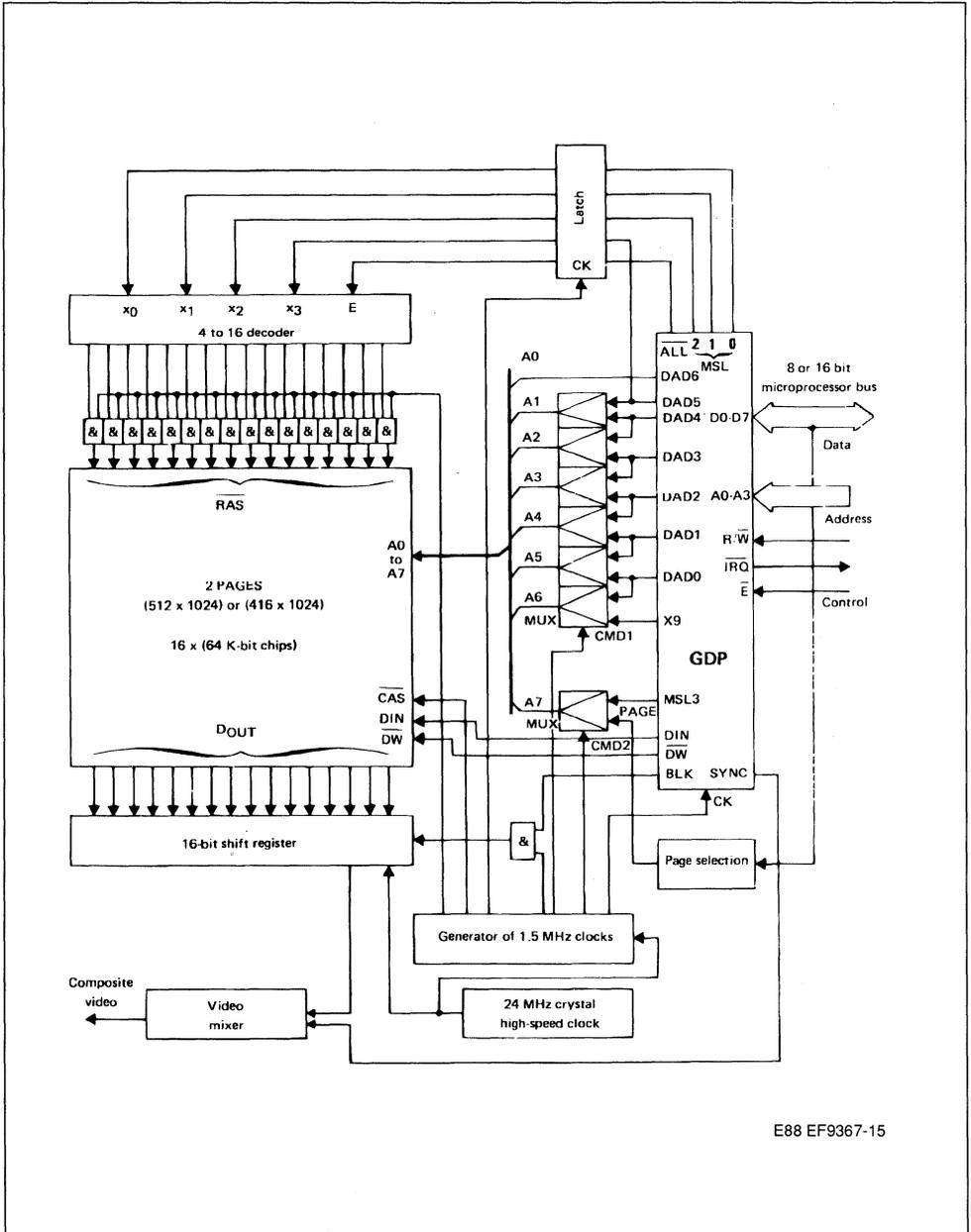
Eight colours may be obtained from the three basic colours red (R), green (G), blue (B).



E88 EF9367-14

Notes : FMAT =  $V_{SS}$  : 256 x 512 resolution - 50 Hz 625 line non interlaced scanning.  
 FMAT = CK : 208 x 512 resolution - 60 Hz 625 line non interlaced scanning.

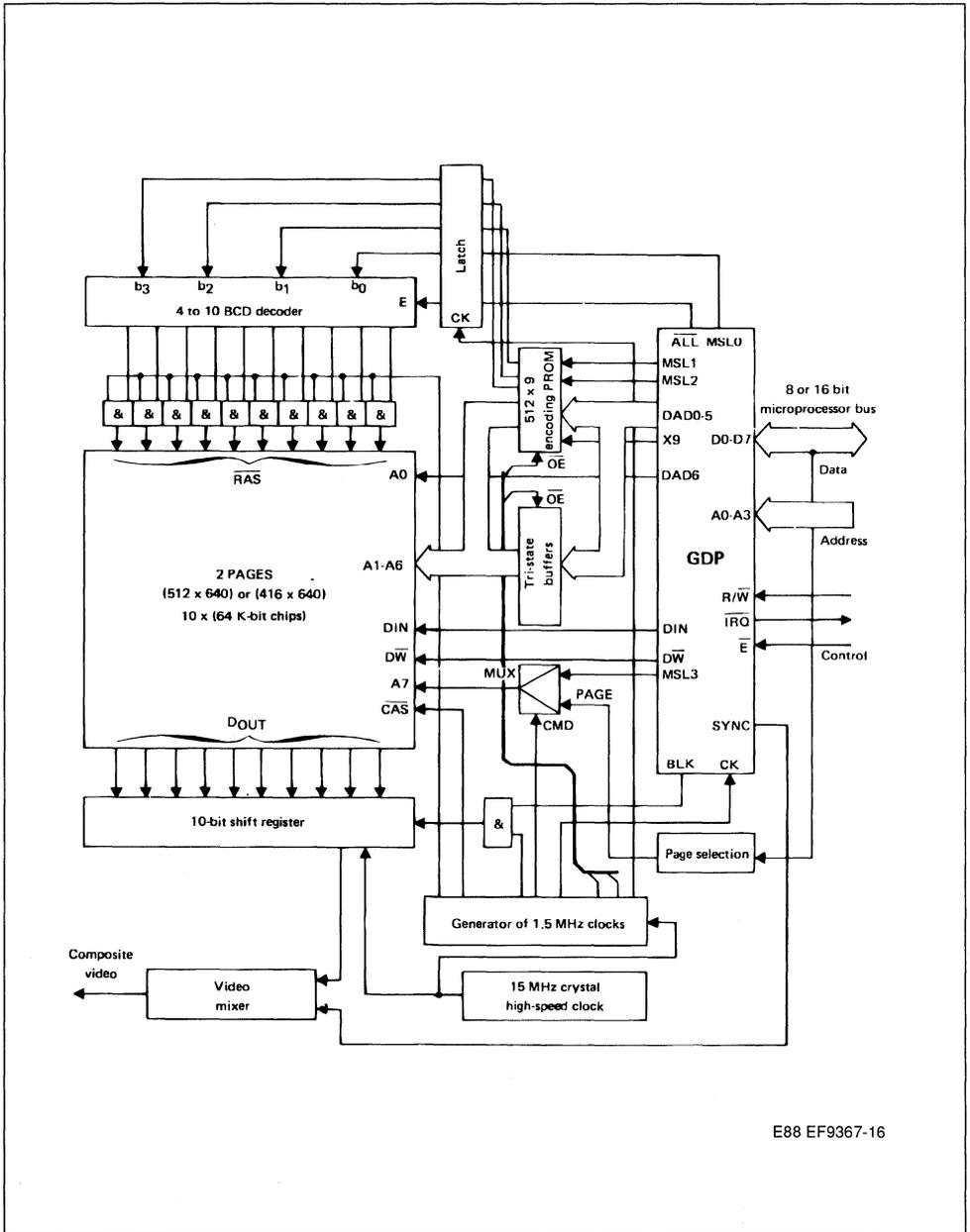
EXAMPLE OF A MONOCHROME, MULTIPAGE APPLICATION : 512 x 1024 or 412 x 1024  
 (see page 32 for MUX command law)



E88 EF9367-15

Notes : FMAT = V<sub>cc</sub> : 512 x 1024 resolution - 50 Hz 625 line non interlaced scanning.  
 FMAT = CK : 416 x 1024 resolution - 60 Hz 625 line non interlaced scanning.

EXAMPLE OF A MONOCHROME, MULTIPAGE APPLICATION : 512 x 640 or 416 x 640  
 (see page 32 for PROM encoding)



E88 EF9367-16

Notes : FMAT = V<sub>CC</sub> : 512 x 640 resolution - 50 Hz 625 line non interlaced scanning.  
 FMAT = CK : 416 x 640 resolution - 60 Hz 625 line non interlaced scanning.

MUX COMMAND LAW

Following table indicates MUX command principles.

Selected MUX Input		Output			Comment
Read Cycles		Write Cycles		Address Bit	
RAS	CAS	RAS	CAS		
DAD6	DAD6	DAD6	DAD6	A <sub>0</sub>	No Mux
DAD5(h <sub>0</sub> )	DAD5	DAD4(X <sub>4</sub> )	DAD5	A <sub>1</sub>	These six MUX are driven identically by CMD1.
DAD4(h <sub>1</sub> )	DAD4	DAD3(X <sub>5</sub> )	DAD4	A <sub>2</sub>	
DAD3(h <sub>2</sub> )	DAD3	DAD2(X <sub>6</sub> )	DAD3	A <sub>3</sub>	
DAD2(h <sub>3</sub> )	DAD2	DAD1(X <sub>7</sub> )	DAD2	A <sub>4</sub>	
DAD1(h <sub>4</sub> )	DAD1	DAD0(X <sub>8</sub> )	DAD1	A <sub>5</sub>	
DAD0(h <sub>5</sub> )	DAD0	X <sub>9</sub>	DAD0	A <sub>6</sub>	
MSL3	PAGE	MSL3	PAGE	A <sub>7</sub>	Driven by CMD2

PROM CODING PRINCIPLES

The PROM coding consists in the use of the 10 horizontal address bits (X<sub>0</sub>, ..... , X<sub>9</sub>) to access the 640 pixels (organized in 64 segments of 10 pixels each).

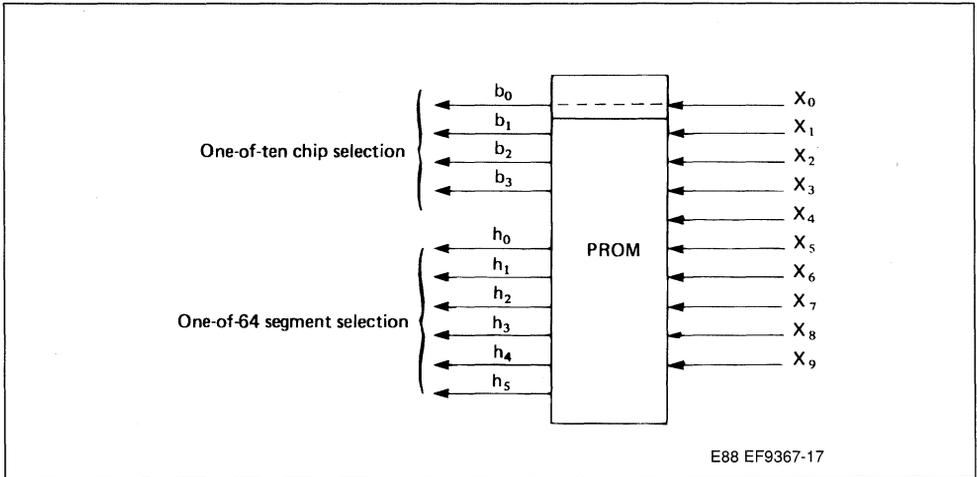
The 4 bits (b<sub>0</sub>, b<sub>1</sub>, b<sub>2</sub>, b<sub>3</sub>) are coding decimal numbers. Parity is maintained by BCD coding : X<sub>0</sub> signal is therefore not coded inside the PROM and provides directly b<sub>0</sub>.

Example : Considering the pixel with decimal abscissa X = 378 (17A in hexadecimal). This pixel is inside the 38th segment (h = 37 dec. or 25 hex.) with an abscissa x = 8.

The binary number 0101111010 (17A hex.) must be encoded into 1001011000 (258 hex.).

This principle allows transcoding of all horizontal address values. Transcoding must only be active (PROM selection) during write cycles (ALL = 1) when horizontal addresses are output (RAS).

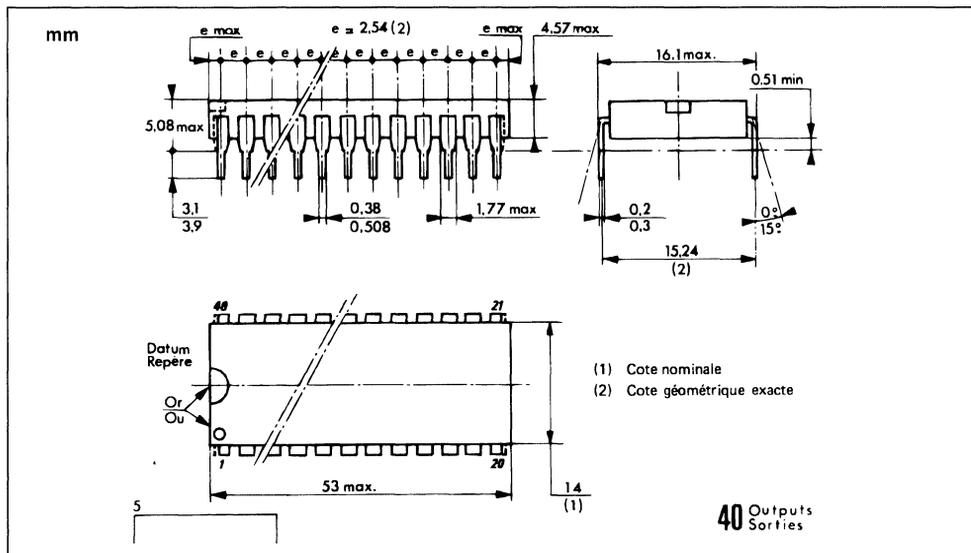
**Note** : This transcoding system may be adapted to other horizontal resolutions as 320, 384, 768. Horizontal resolutions are multiples of 64.



E88 EF9367-17

PACKAGE MECHANICAL DATA

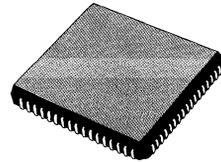
40 PINS - PLASTIC DIP





**HMOS2 ADVANCED GRAPHIC  
AND ALPHANUMERIC CONTROLLER**

- FULLY PROGRAMMABLE TIMING GENERATOR
- ALPHANUMERIC AND GRAPHIC DRAWING CAPABILITY
- EASY TO USE AND POWERFUL COMMAND SET :
  - VECTOR, ARC, CIRCLE WITH DOT OR PEN CONCEPT AND PROGRAMMABLE LINE STYLE,
  - FLEXIBLE AREA FILL COMMAND WITH TILING PATTERN,
  - VERY FAST BLOCK MOVE OPERATION,
  - CHARACTER DRAWING COMMAND, ANY SIZE AND FONTS AVAILABLE
- LARGE FRAME BUFFER ADDRESSING SPACE (8 megabytes) UP TO 16 PLANES OF 2048 x 2048
- UP TO 256 COLOR CAPABILITIES
- MASK BIT PLANES FOR GENERAL CLIPPING PURPOSE
- FRAME BUFFER CAN BE BUILT WITH STANDARD 64 K OR 256 K DRAM OR DUAL-PORT-MEMORIES (video-RAM)
- EXTERNAL SYNCHRONIZATION CAPABILITY
- ON CHIP VIDEO SHIFT REGISTERS FOR DOT RATE UP TO 18 MEGADOTS/S
- 8 OR 16-BIT BUS INTERFACE COMPATIBLE WITH MARKET STANDARD MICROPROCESSORS
- HMOS 2 TECHNOLOGY
- 68 - PIN PLCC PACKAGE, AND 64 - PIN PLASTIC DIP



**FN**  
**PLCC68**  
(Plastic leaded chip carrier)



**P**  
**DIP64**  
(Plastic Package)

**DESCRIPTION**

The TS68483 is an advanced color graphic processor that drastically reduces the CPU software overhead for all graphic tasks in medium and high range graphic applications such as business and personal computer, industrial monitoring system and CAD systems.

(Ordering information at the end of the datasheet)

PIN CONNECTIONS

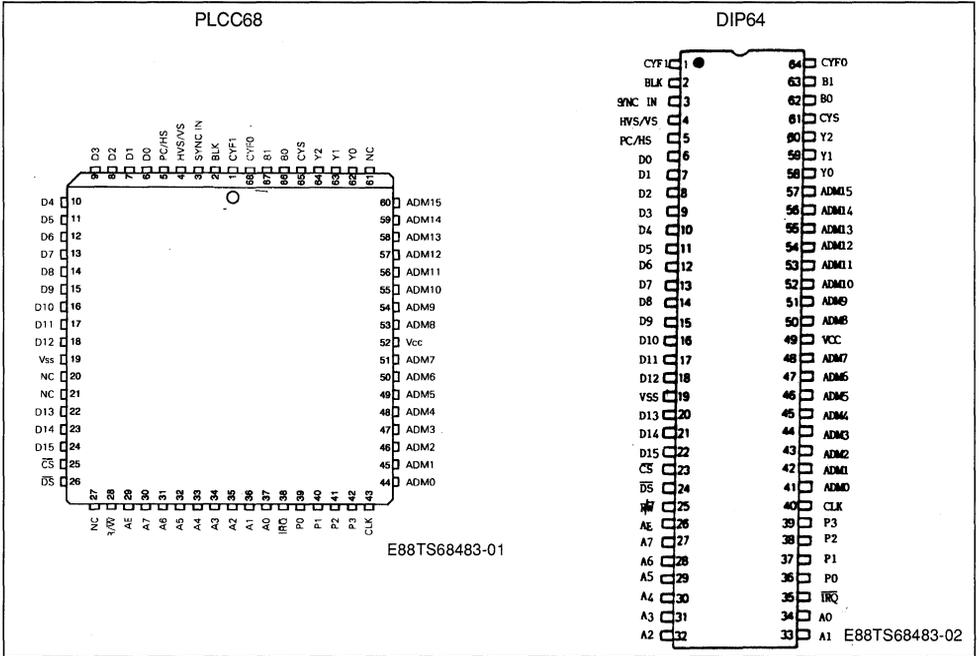
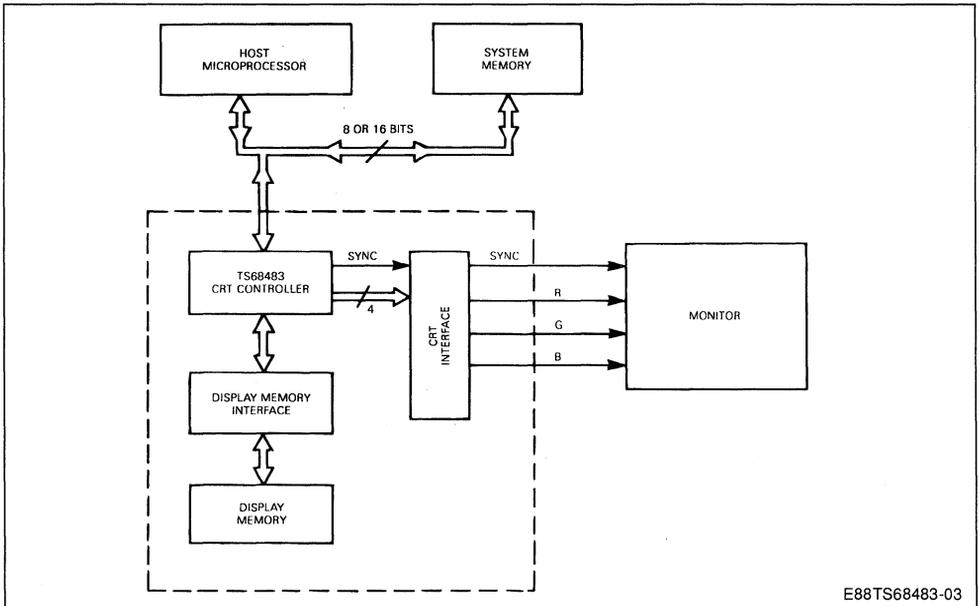


Figure 1.1 : Typical Application.



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2. COMMANDS
3. MICROPROCESSOR INTERFACE
4. THE VIDEO TIMING GENERATOR RAM REFRESH AND DISPLAY PROCESS
5. MEMORY ORGANIZATION
6. TIMING DIAGRAM
7. REGISTER MAP AND COMMAND TABLE
8. ORDERING INFORMATION AND PACKAGE MECHANICAL DATA

## 1. GENERAL OPERATION

### 1.1. INTRODUCTION

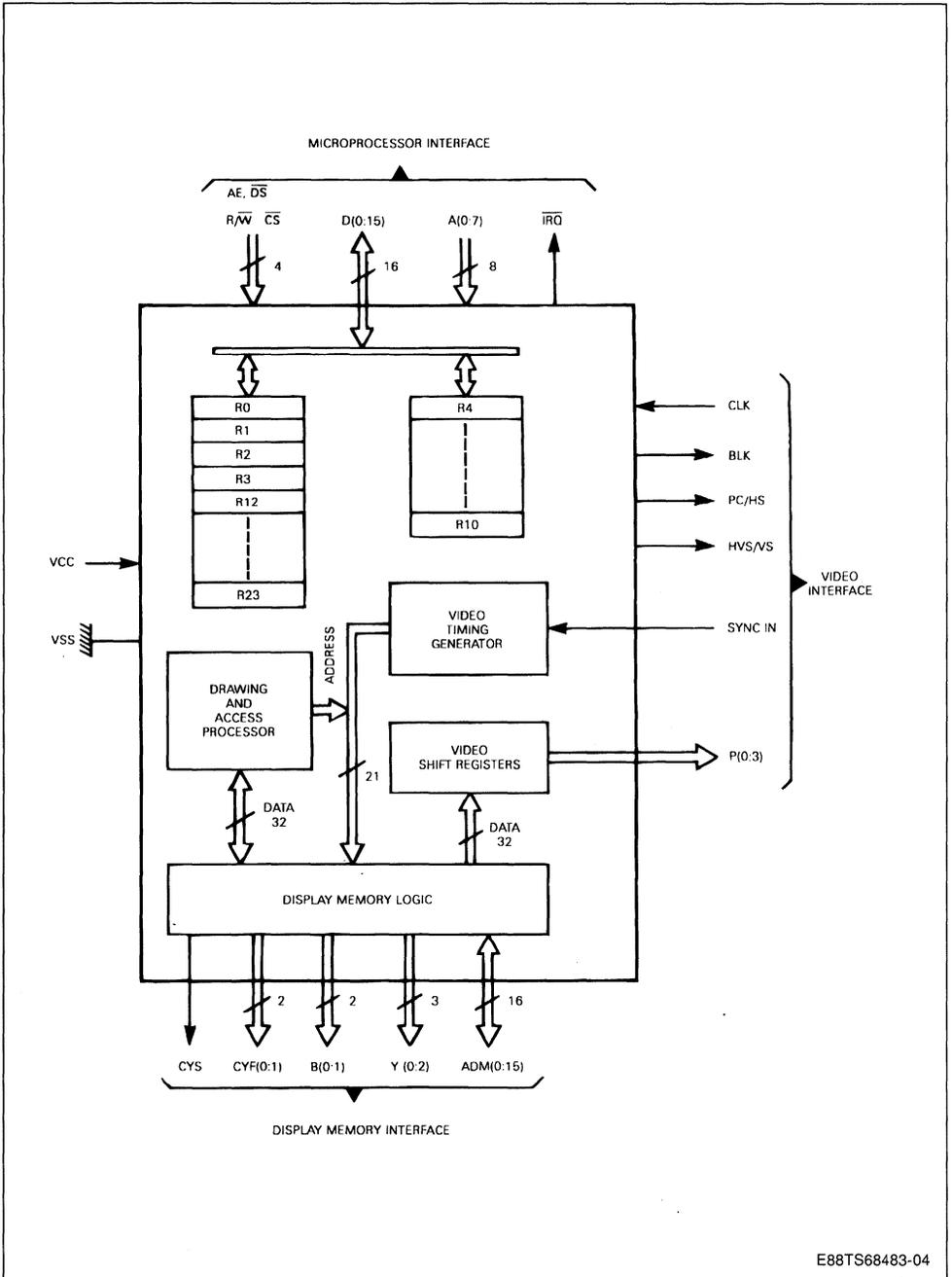
The TS68483 is an advanced color graphics controller chip. It is directly compatible with most popular 8 or 16-bit microprocessors.

Its display memory, containing the frame buffer and the character generators, may be assembled from standard dynamic RAM components.

On-chip video shift registers and fully programmable Video Timing Generator allow the TS68483 to be used in a wide range of terminals or computer design.

Additional informations on applications can be found in the TS68483 User's Manual.

BLOCK DIAGRAM



E88TS68483-04

## PIN DESCRIPTION

## MICROPROCESSOR INTERFACE

Name	Pin Type	Function	Description
D (0 : 15)	I/O	Data Bus	These sixteen bidirectional pins provide communication with either an 8 or 16-bit host microprocessor data bus.
A (0 : 7)	I	Address Bus	These eighth pins select the internal register to be accessed. The address can be latched by AE for direct connection to address/data multiplexed microprocessor busses.
AE	I	Address Enable	When TS68483 is connected to a non-multiplexed microprocessor bus, this input must be wired to VCC. For direct connection to a multiplexed microprocessor bus, the falling edge of AE latches the address on A (0 : 7) pins and the CS input. With an Intel type microprocessor, AE is connected to the processor Address Latch Enable (ALE) signal.
$\overline{DS}$	I	Data Strobe	Active Low – In non-multiplexed bus mode, $\overline{DS}$ low enables the bidirectional data buffers and latches the A (0 : 7) lines on its high to low transition. Data to be written are latched on the rising edge of this signal. – In multiplexed bus mode, this signal low enables the output data buffers during a read cycle. With intel microprocessors, this pin is connected to the RD signal.
$\overline{R/W}$	I	Read/Write	– In non-multiplexed bus mode, this signal controls the direction of data flow through the bidirectional data buffers. – In multiplexed bus mode, this signal low enables the input data buffers. The entering data are latched on its rising edge. With Intel microprocessors, this pin is connected to the WR signal.
$\overline{CS}$	I	Chip Select	This input selects the TS68483 registers for the current bus cycle. A low level corresponds to an asserted chip select. In multiplexed mode, this input is strobed by AE.
$\overline{IRQ}$	O	Interrupt Request	This active-low open drain output acts to interrupt the microprocessor.

## MEMORY INTERFACE

Name	Pin Type	Function	Description
ADM (0 : 15)	I/O	Address/Data Memory	These multiplexed pins act as address and data bus for display memory interface.
CYS	O	Memory Cycle Start	The falling edge of this output indicates the beginning of a memory cycle.
Y (0 : 2)	O	Memory Address	These outputs provide the least significant bits of the Y logical address.
B (0 : 1)	O	Bank Number	These outputs provide the number of the memory bank to be accessed during the current memory cycle.
CYF (0 : 1)	O	Memory Cycle Status	These outputs indicate the nature of the current memory cycle (Read, Write, Refresh, Display).

## VIDEO INTERFACE

Name	Pin Type	Function	Description
P (0 : 3)	O	Video Shift Register Outputs	These four pins correspond to the outputs of the internal video shift registers.
PC/HS	O	Phase Comparator/ Horizontal Sync.	This output can be programmed to provide either the phase comparator output or the horizontal sync. signal.
HVS/VS	O	Composite or Vertical Sync.	This output can be programmed to provide either the composite sync. signal or the vertical sync. signal.
SYNC IN	I	External Sync Input	This input receives an external composite sync. signal to synchronize TS68483. This input must be grounded if not used.
BLK	O	Blanking	This output provides the blanking interval information.

## OTHER PINS

Name	Pin Type	Function	Description
VCC	S	Power Supply	+ 5 V Supply
VSS	S	Ground	Ground
CLK	I	Clock	Clock Input

## 1.2. TYPICAL APPLICATION BUILDING BLOCKS

In a typical using TS68483, a host processor drives a display unit which drives in turn a color CRT monitor.

The display unit consists of four hardware building blocks :

- an TS68483 advanced graphics controller,
- a display memory (dynamic RAM),
- a display memory interface, comprising a few TTL parts,
- a CRT interface of CRT drivers.

For enhanced graphics, the CRT interface may include a color look-up table circuit such as EF9369. For high pixel rate (over 18 Mpixels/s), the CRT interface must include high speed video shift registers.

The display memory interface and organization are discussed in full details in the User's Manual.

## 1.3. TS68483 FUNCTIONS.

All the TS68483 functions are under the control of the host microprocessor via 24 directly accessible 16-bit registers. These registers are referred to by their decimal index (R0-R23). See figure 1.2.

## 1. Video timing and display processor (R4 to R10).

The video timing generator is fully programmable :

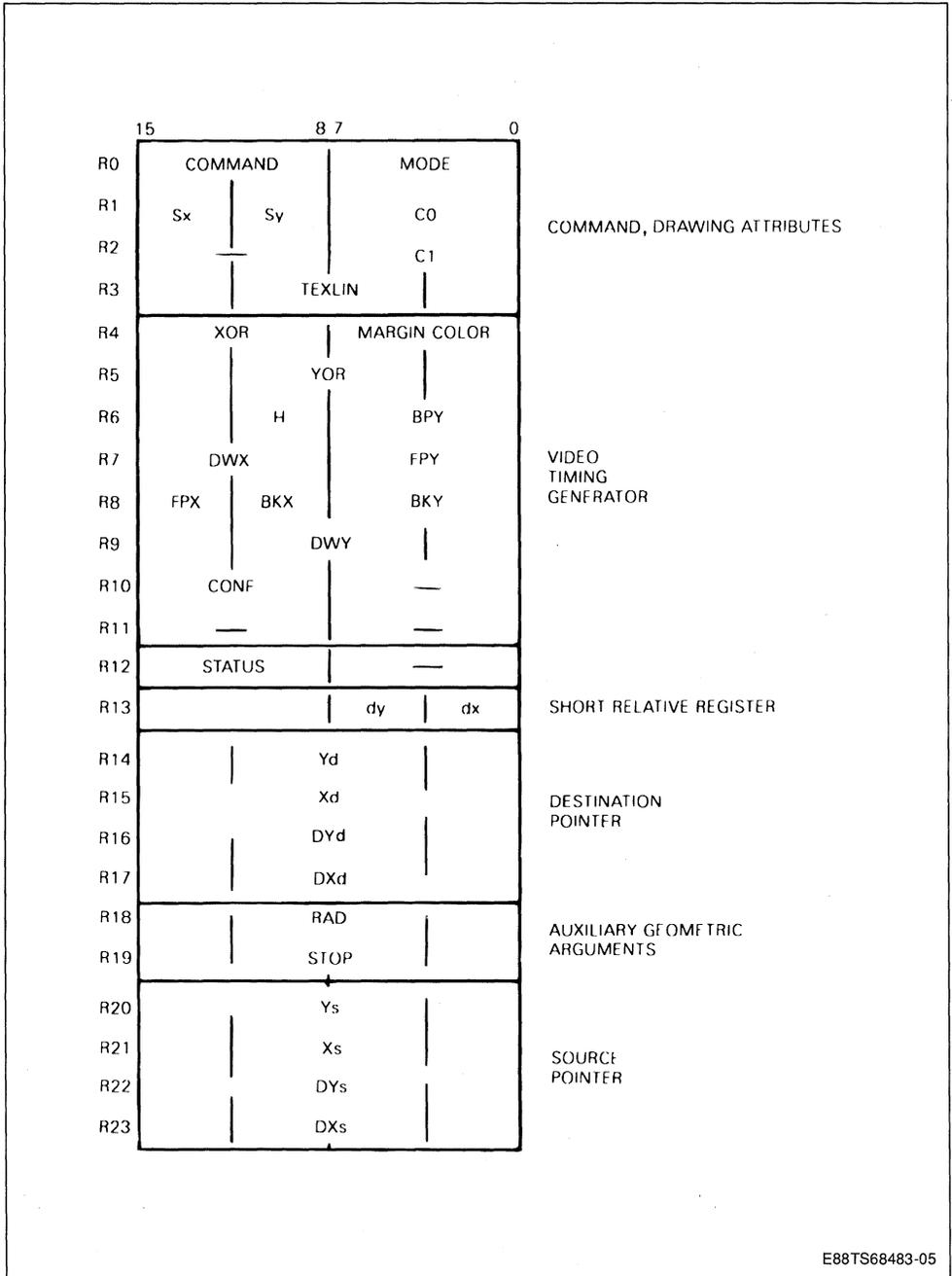
any popular horizontal scanning period from 20  $\mu$ s to 64  $\mu$ s may be freely combined with any number of lines per field (up to 1024). The address of the display viewport (this part of the display memory to be actually displayed on the screen) is fully programmable. The display processor provides the display dynamic RAM refresh (see video timing generator section for details).

## 2. Drawing and access commands (R0 to R3, R12 to R23).

The 16 remaining registers are used to specify a comprehensive set of commands. The highly orthogonal drawing command set allows the user to "draw" in the display memory such basic patterns as lines, arcs, polylines, polyarcs, rectangles and characters. Efficient procedures are available for either area filling and tiling or line drawing and texturing. Lines may be drawn with a PEN in order to get thick strokes. Any drawing is specified in a  $2^{13} \times 2^{13}$  drawing coordinate system.

To access the display memory, the host microprocessor has an indirect, sequential access to any "window". Access commands can be used to load the character generators as well as to load or save arbitrary windows stored in the frame buffer.

Figure 1.2. : Register Map.



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#### 1.4. DATA TYPE DEFINITIONS.

**PIXEL** : this is the smallest color spot displayable on the CRT.

**PEL** : a Picture Element is the coding of a PIXEL in the display memory. The TS68483 can handle 4 different PEL formats :

- 4 color bits - short
- 4 color bits + 1 mask bit - short masked
- 8 color bits - long
- 8 color bits + 1 mask bit - long masked

**DRAWING COORDINATES** : (see figure 1.3).

The drawing commands are specified and computed in a  $2^{13} \times 2^{13}$  cyclical coordinate system. The drawing coordinates are clipped and mapped into the  $2^{11} \times 2^{11}$  display memory addressing space. Further clipping to the actual frame buffer size may be performed by the user designed memory interface.

**DISPLAY MEMORY** :

This is the private memory dedicated to the display unit. This memory is addressed as four banks of 4-bit plane each.

**BIT PLANE** :

Each bit plane has a maximum capacity of  $2^{11} \times 2^{11}$  bits. A byte wide organization of each bit plane is required.

**MEMORY ADDRESS** : (see figure 1.4).

In order to address one bit in the display memory, the user must specify :

- A bank number (2 bits) B = 0 to 3
- A bit plane number (2 bits) Z = 0 to 3
- A Y address (11 bits) Y = 0 to 2047
- An X address (11 bits) X = 0 to 2047

**MEMORY WORD** : (see figure 1.4).

A 32-bit memory word can be either read or written during each memory cycle (8 CLK periods), one byte at a time in each bit plane in the addressed bank. The memory bandwidth is in the 6 to 8 Mbytes/s range.

**VIEWPORT** :

This is any rectangular array of pels located in the display memory.

**FRAME BUFFER** :

This is the biggest viewport which can be held in the display memory. The frame buffer maps a window at the origin of the drawing coordinates. A short pel frame buffer may be located in any bank. A long pel frame buffer must be located in the "bank 0, bank 1" pair.

**DISPLAY VIEWPORT** :

This is the viewport which is displayed on screen.

**MASK BIT PLANE** :

When masked pels are used, a mask bit plane must be associated to a frame buffer. Mask bit planes may be located in any plane of bank 3.

**CELL** :

A CELL is any pattern stored in the display memory as a rectangular array of bit mapped elements. The drawing of any CELL may be specified with a scaling factor.

**CHARACTER** :

This is a one bit per element CELL. It may be stored in any bit plane, then colored and drawn in a frame buffer by use of PRINT CHARACTER command.

**OBJECT** :

This is a one short pel per element CELL. It may be drawn or loaded in a frame buffer. A source mask bit may be associated to each element. An OBJECT may then be printed in another location by use of a PRINT OBJECT command.

**PEN** :

This is the pattern which is repeatedly drawn along the coordinates defined by either a LINE or an ARC command.

The PEN may be a DOT (single pel), a CHARACTER or an OBJECT.

Figure 1.3 : Cyclical Drawing Coordinates to Display Memory Mapping.

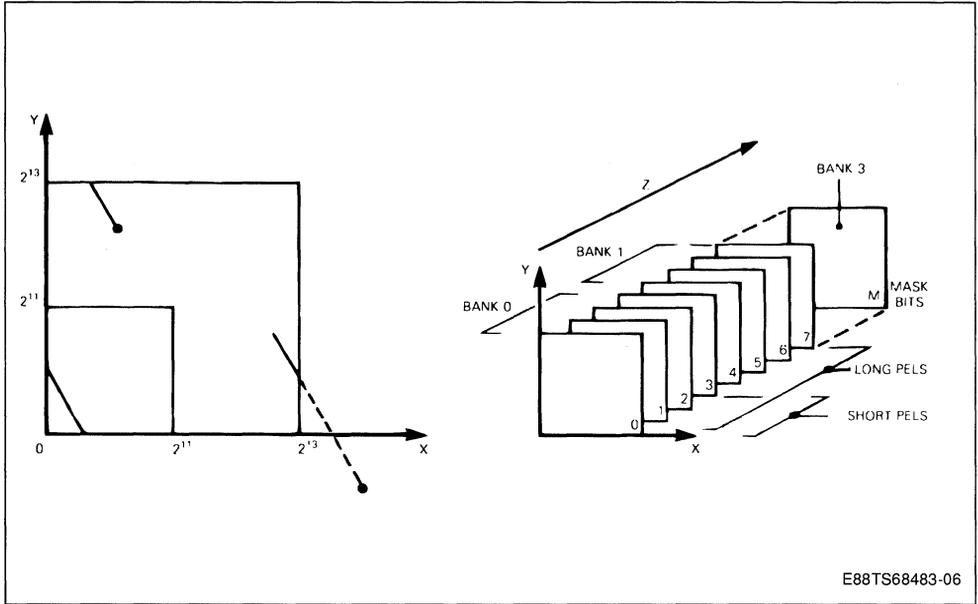
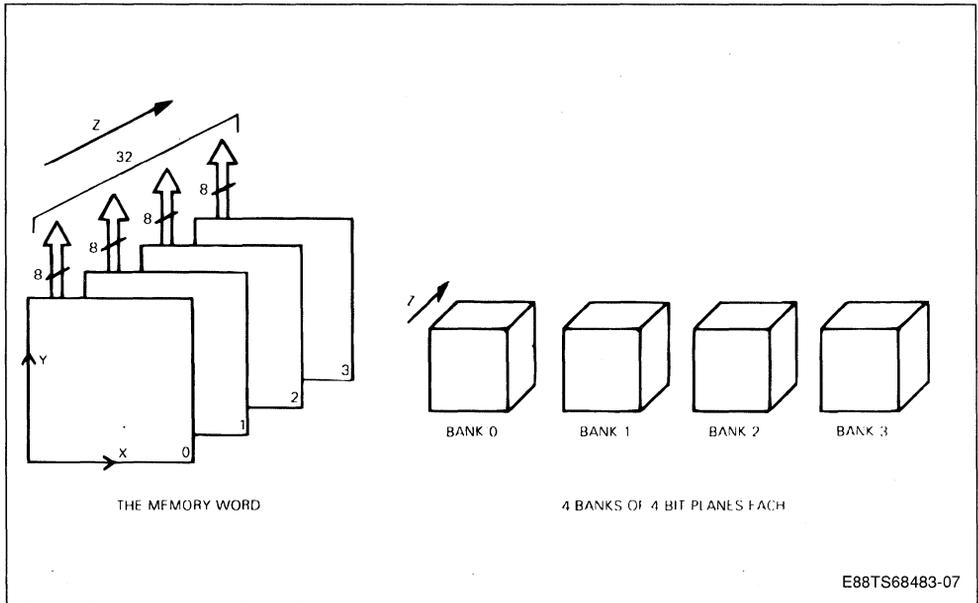


Figure 1.4 : The Display Memory Addressing Space.



## 2. COMMANDS

### 2.1. INTRODUCTION

The command set is strongly organized in five sub-set or command types.

#### DRAWING COMMANDS :

- \_ LINEAR (line, arc)
- \_ AREA (rectangle, trapezium, polygon, polyarc)
- \_ PRINT CELL (print character, print object)

#### ACCESS COMMANDS

#### CONTROL COMMANDS (move cursor, abort).

The commands are parametered ; this means that any command can be executed with options freely selected out of a given option set. This option set is common for any command of a given type. For example, any drawing command may be parametered for destination mask bit use.

The command code also defines the command type and its parameters. A command is completely defined when a value has been set for each of its arguments.

These arguments are :

- \_ the geometric arguments given in the drawing coordinate system for every drawing command. They are automatically mapped into the destination frame buffer ;
- \_ the parametric values are the values required by the selected parameters ;
- \_ the attribute values are the other values required by a drawing command ; colors or scaling factors for example ;
- \_ the display memory addresses.

The command code is specified in register R0. Before initiating a command execution, each argument must be specified in its dedicated register : - an Xd, Yd drawing coordinate pair for example, is always located in registers R14, R15.

The monitoring of a command execution is done by reading the status register R12 or using the IRQ signal.

**Figure 2. 1. :** Command Set Structure.

Command	Drawing Mode	Type	Group
Line Arc	Up to the Pen	Linear	Drawing
Rectangle Trapezium Polygon Polyarc	Monochrome	Area	
Print Char Print Object	Bichrome Polychrome	Cell	
Load Viewport Save Viewport Modify Viewport		Access	Management
Move Cursor Abort		Control	

### 2.2. POINTERS AND GEOMETRIC ARGUMENTS.

Pointers are used to specify main geometric arguments and display memory addresses.

**2.2.1. Display Memory Address.** A bit in the display memory is addressed by :

- \_ a bank number      B = 0 to 3
- \_ a plane number     Z = 0 to 3
- \_ an X address       X = 0 to 2047
- \_ a Y address        Y = 0 to 2047

**2.2.2. Destination Pointer : Registers R14 to R17.**

This pointer gives the coordinate (Xd, Yd) and di-

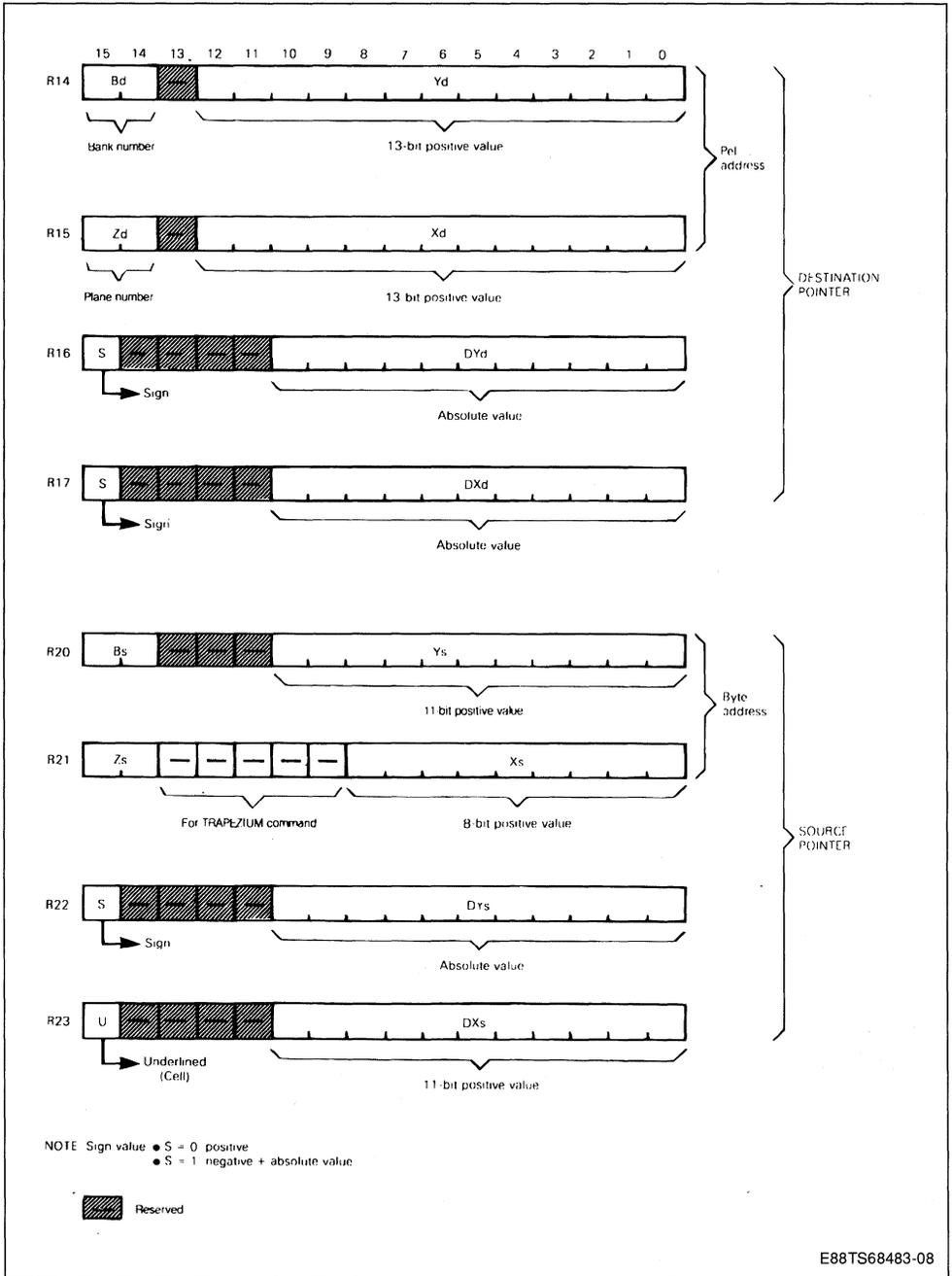
mension (DXd, DYd) of either a line or a window in the drawing coordinate system. These drawing coordinates are easily mapped into a PEL DISPLAY MEMORY address.

(X, Y) coordinates are clipped to 11 bits in order to get the Xd, Yd destination pel addresses.

A bank number Bd must be explicitly provided to address a destination frame buffer. When long pels are used, Bd must be even.

When masked pels are used, the destination mask plane number Zd (implicitly in bank 3) must also be provided.

Figure 2.2. : Pointers.



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**2.2.3. Source Pointer : Registers R20 to R23.** A source cell such as a character, a pen or an object, is addressed by the source pointer in the display memory.

A source pointer specifies :

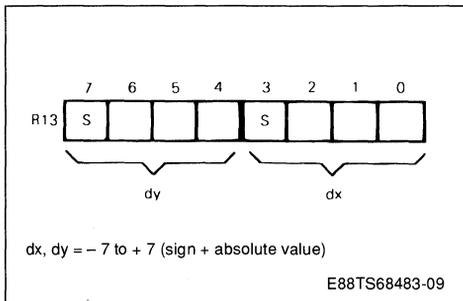
- a bank number Bs = 0 to 3
- a Ys address Ys = 0 to 2047
- an Xs address ; this address is a byte address so that the 3 LSBs are not specified Xs = 0 to 255
- a cell dimension DXs, DYs
- a bit plane address Zs.

When a character is addressed, Zs gives the plane number into the bank Bs. When an object is addressed Zs gives the source mask plane number in the bank B3.

**2.2.4. Notes :**

1. The TRAPEZIUM command makes a special use of R21. In this case, R21 holds an X1 drawing coordinate which has the same format as Xd.
2. The ARC and POLYARC commands require two extra geometric parameters (RAD and STOP). They are specified in the drawing coordinates system and stored in registers R18, R19.
3. Any drawing command may be parametered to use short incremental dimensions, DXY in register R13 instead of the standard DXd, DYd in the "R16, R17" register pair (see figure 2.3).
4. The access commands use the destination pointer location as a data buffer. The memory addresses and dimension of the access viewport are then specified in the source pointer, independently of the data transfer.
5. DXd, DYd and DYs may specify a negative value. In this case, they must be coded by a sign (0 = positive, 1 = negative) and an 11-bit absolute value.

**Figure 2.3. :** Short Dimension Register R13.



**2.3. DESTINATION MASK AND SOURCE MASK.**

A mask bit may be associated to any pel stored in the display memory.

**2.3.1. Destination Mask Use (DMU).** Any drawing command may be parametered for destination mask use. In this case, any destination pel cannot be modified when its mask bit is reset.

In other words :

When the destination mask use (DMU) parameter is set :

- a pel may be modified when its mask bit is set
- a pel cannot be modified when its mask bit is reset.

When the destination mask use (DMU) parameter is cleared :

- a pel may be modified, independently of its mask bit value.

This provides a very flexible clipping mechanism not restricted to rectangular windows. (See destination pointer section for destination mask bit addressing).

**2.3.2. Source Mask Use (SMU).** A PRINT OBJECT command may be parametered for source mask use. In this case, the source mask bit associated with any source pel is read first. When its mask bit is cleared, a source pel is considered as transparent. (See source pointer section for source mask bit addressing).

In other words :

When the SMU parameter is set, the color of a destination pel, mapped by a given source pel, may take this source color value only when this source bit mask is set. The destination pel keeps its own color value when the source bit mask is cleared.

When the SMU parameter is cleared, a source pel color may be mapped into destination pel color independently of the source bit mask value.

The source bit mask acts as a TRANSPARENCY/OPACITY flag which is enabled by SMU. A PRINT OBJECT command may be independently parametered by both SMU and DMU. This provides a very powerful tiling, print object or move mechanism.

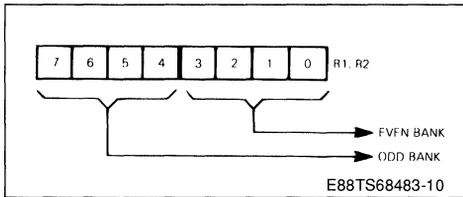
**2.4. DRAWING ATTRIBUTES.**

The general drawing attributes are the colors, the drawing mode, and the scaling factor.

**2.4.1. Colors : Registers R1 and R2** (see figure 2.4.). Two 8-bit color values, C0 and C1, may be specified in registers R1 and R2. The low order 4-

bit nibble of a color value is drawn in an even bank. The high order color nibble is drawn in an odd bank. When long pels are used, banks 0 and 1 are generally addressed as the frame buffer. When short pels are used, any bank may hold a frame buffer. In this case, the bank parity selects the color nibble used. (See destination pointer section for bank addressing).

Figure 2.4. : Color Register.



**2.4.2. Drawing Mode : Register R0.** The drawing mode defines the transforms to be applied to the pels designated by the drawing commands. There are three drawing modes.

**2.4.3. Monochrome Mode.** Any AREA drawing command, RECTANGLE for instance, defines through its geometric arguments an active set of destination pels, that is to say a set of pels to be modified.

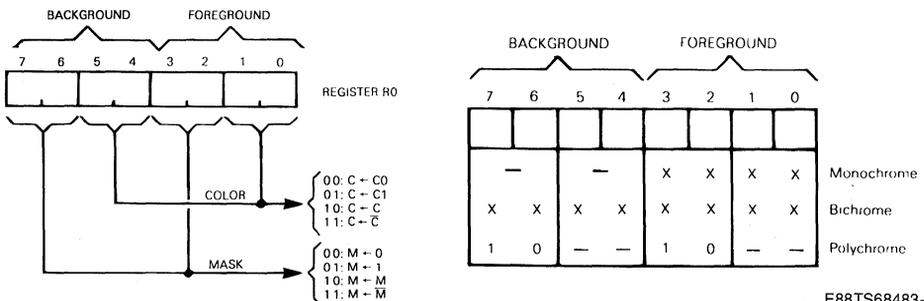
When DMU = 1, this active set is further reduced by the masking mechanism to only these destination pels with a bit mask set.

The active destination pels are then modified according to two elementary transforms coded in R0.

A bichrome drawing mode is defined by 4 elementary and independent transforms : (see figure 2.5)

- a color transform ) For the FOREGROUND PELS
- a mask transform )
- a color transform ) For the BACKGROUND PELS
- a mask transform )

Figure 2.5. : Drawing Mode Register R0.



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**COLOR TRANSFORM :**

The color value C of each active pel is modified according to one color transform selected out of four :

- \_ 00 - printed in C0 : C ← C0
- \_ 01 - printed in C1 : C ← C1
- \_ 10 - printed in "transparent" : C ← C
- \_ 11 - complemented : C ← C̄

This yields to a reversible marker mode.

**MASK BIT TRANSFORM :**

The destination mask bit of each active pel is modified according to one mask transform selected out of four :

- \_ 00 - reset bit mask : M ← 0
- \_ 01 - set bit mask : M ← 1
- \_ 10 - no modification : M ← M
- \_ 11 - complement bit mask : M ← M̄

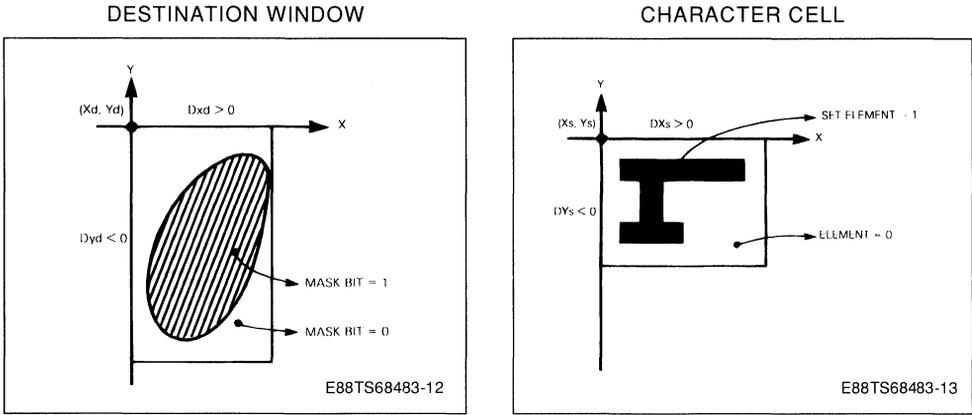
This scheme allows the color bits and the mask bit of any pel belonging to the active set to be modified independently. The color transform is performed first.

**2.4.4. Bichrome Mode.** A PRINT CHARACTER command is more complex because it involves two different active sets : FOREGROUND and BACKGROUND.

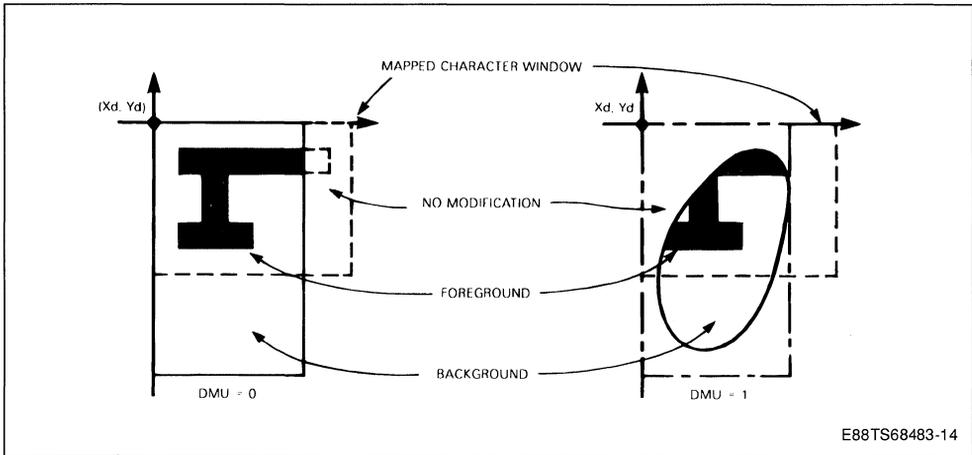
The FOREGROUND is that set of destination pels printed from set elements in the character cell. The BACKGROUND is made of all the remaining pels belonging to the destination window.

When DMU = 1, the FOREGROUND and BACKGROUND are further reduced by the destination masking mechanism. (see figure 2.6).

Figure 2.6. : Print Character Command.



MAPPED CHARACTER WINDOW



**2.4.5. Polychrome Mode.** A print object command defines a source window through the source pointer :

When SMU = 0, any pel of this window is active, mapped and clipped to the destination window dimension.

When SMU = 1, only pels which have a source mask bit set are active, mapped and clipped to the destination window dimension.

In both cases, when DMU = 1, the active source pels are further reduced by the destination masking mechanism.

Both mask transforms must be programmed at "NO MODIFICATION" for correct operations. (see figure 2.5).

**2.4.6. The Linear Drawing Command Case.** A LINE or ARC drawing command may be executed in any drawing mode depending on the PEN.

When the pen is a DOT, this pel is printed at each active coordinate according to monochrome mode.

When the pen is a CELL, this cell is printed at each active coordinate. In the bichrome mode when the cell is a character, and in the polychrome mode when the cell is an object.

For each active coordinates, the active destination set is defined by the cell dimensions (DXs, DYs).

Note : when the cell is an object, SMU is not programmable and is implicitly set. A calculated coordinate is active when the rotated LSB linear texture bit in (R3) is set.

**2.4.7. Scaling Factor and Cell Mapping :** (see figure 2.7 and 2.8). Any cell may be printed with a scaling factor.

This scaling factor is an integer pair  $S_x, S_y = 1$  to 16.

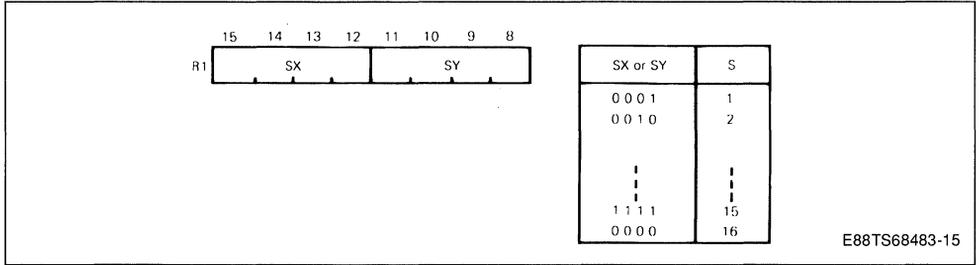
This scaling factor is interpreted with the PRINT CHARACTER, PRINT OBJECT and LINEAR commands when the pen is a cell. The AREA or AC-

CESS or LINEAR (DOT) commands are never scaled.

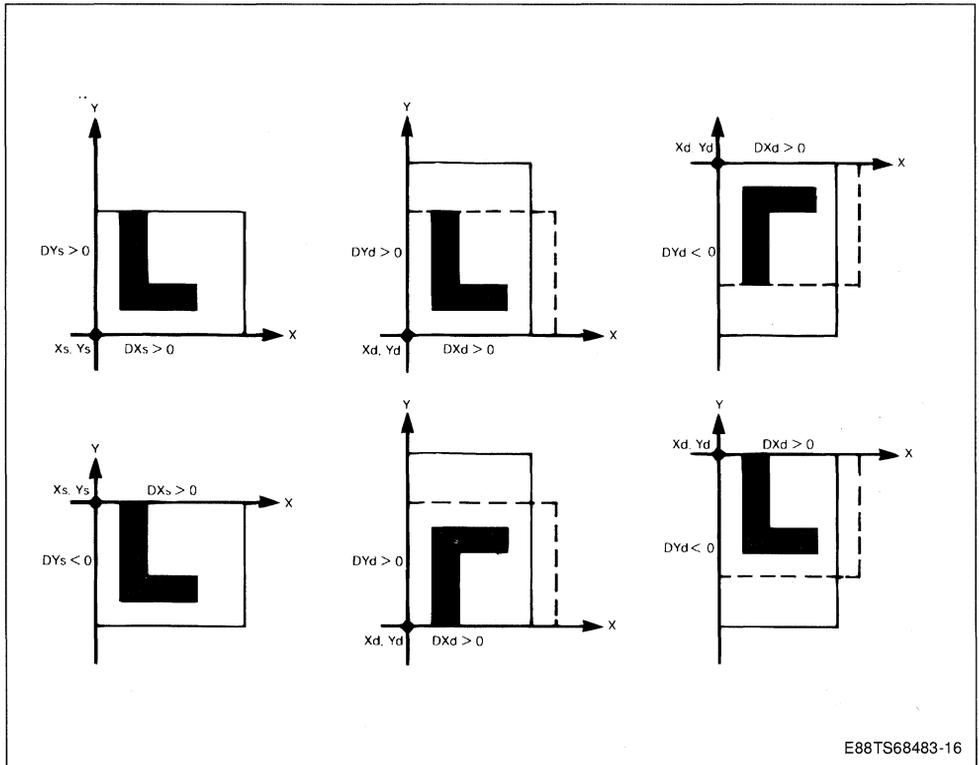
The LINEAR (PEN) command should be used with a scaling factor of 1 because the pen is clipped at  $DX_s, DY_s$ .

The scaling factor is first applied to the source cell before mapping and drawing. The drawing and mapping is processed with sign bit of  $DY_d$  and  $DY_s$  values. (see figure 2.8).

**Figure 2.7. :** Scaling Factor.

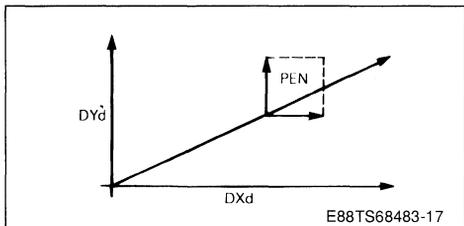


**Figure 2.8. :** Cell Mapping Versus  $DY_d, DY_s$  SIGN.



**Note :**

- DXs is always positive
- The DYs sign mirrors the cell
- DXd must be positive with a PRINT CELL command
- DXd and DYd may get any sign with a LINEAR DRAWING command. If a pen is used, these signs are then irrelevant to the pen drawing. The pen is mapped with positive increment values.



**2.5. COMMAND SET OVERVIEW**

**2.5.1. Linear Drawing.** LINE (Xd, Yd, DXd, DYd). ARC (Xd, Yd, DXd, DYd, RAD, STOP).

The curve may be drawn with any pen and with any linear texture (register R3). For each set of computed coordinates, R3 is right rotated and the pen is printed when the shifted bit is set.

**2.5.2. Area Drawing.**

- RECT (Xd, Yd, DXd, DYd)
- TRAPEZIUM (Xd, Yd, DXd, DYd, X1)
- POLYGON (Xd, Yd, DXd, DYd)
- POLYARC (Xd, Yd, DXd, DYd, RAD, STOP)

Either RECT or TRAPEZIUM allows to draw directly all the pels inside the boundary.

Any other closed boundaries may be filled by a 3-step process :

1. The mask bits inside a boundary box must be re-set by a RECT command.
2. A sequence of mixed POLYGON and POLYARC commands describing the closed boundary sets the mask bits of the pels inside this boundary.
3. This area may then be painted by a RECTANGLE command defined for a bounding box, with destination masking. It may also be tiled by use of a PRINT CELL command.

**Note :** the mask bit of any pel lying on the boundary itself is not guaranteed to be set by step 2.

**2.5.3. Print Cell Commands.** PRINT CELL (Xd, Yd, DXd, DYd ; Xs, Ys, DXs, DYs).

The cell addressed by Xs, Ys, DXs, DYs is scaled then printed at location Xd, Yd and clipped at the dXd, dYd dimensions.

When dXd, dYd is much larger than DXs, DYs the command may be parametered for repeat drawing.

These commands may also be parametered for destination mask use.

Further more the PRINT OBJECT command may be parametered for source mask use.

These commands have a wide range of applications : text drawing, area tiling, print or move objects, scale and move viewpoints.

**Note :** an underlined cell is drawn when the MSB of R23 is set.

**2.5.4. Access Commands.**

- LOAD VIEWPORT (Xs, Ys, DXs, DYs)
- SAVE VIEWPORT (Xs, Ys, DXs, DYs)
- MODIFY VIEWPORT (Xs, Ys, DXs, DYs)

These commands provide sequential access to a viewport in a frame buffer from the microprocessor data base.

Data are transferred to/from the display memory, word sequentially.

The R14 to R17 registers are used as a two memory word FIFO (memory word is 8 short pels, i.e. 4 bytes).

The source pointer (R20-R23) is used to address the viewport for all access commands.

When long pels are used, the command must be executed once more when the bank number in R20 has been updated.

**2.5.5. Command Execution.** Each on-chip 16-bit register has four addresses. One address is used for plain read or write. The other addresses are used to initiate command execution automatically on completion of the register access.

This scheme allows the command code and its arguments to be loaded or modified in any other. An incremental line drawing command, for example, may be executed again and again with successive incremental dimensions and without need to re-load the command code itself.

As soon as a command execution is started, the FREE bit is cleared in the STATUS register. This bit is automatically set when the execution is completed.

The commands are generally executed only during retrace intervals. However full time execution is possible when either the display is disabled or video RAM components are used.

**2.5.6. Status Register** (see figure 2.9). This register holds four read-only status bits :

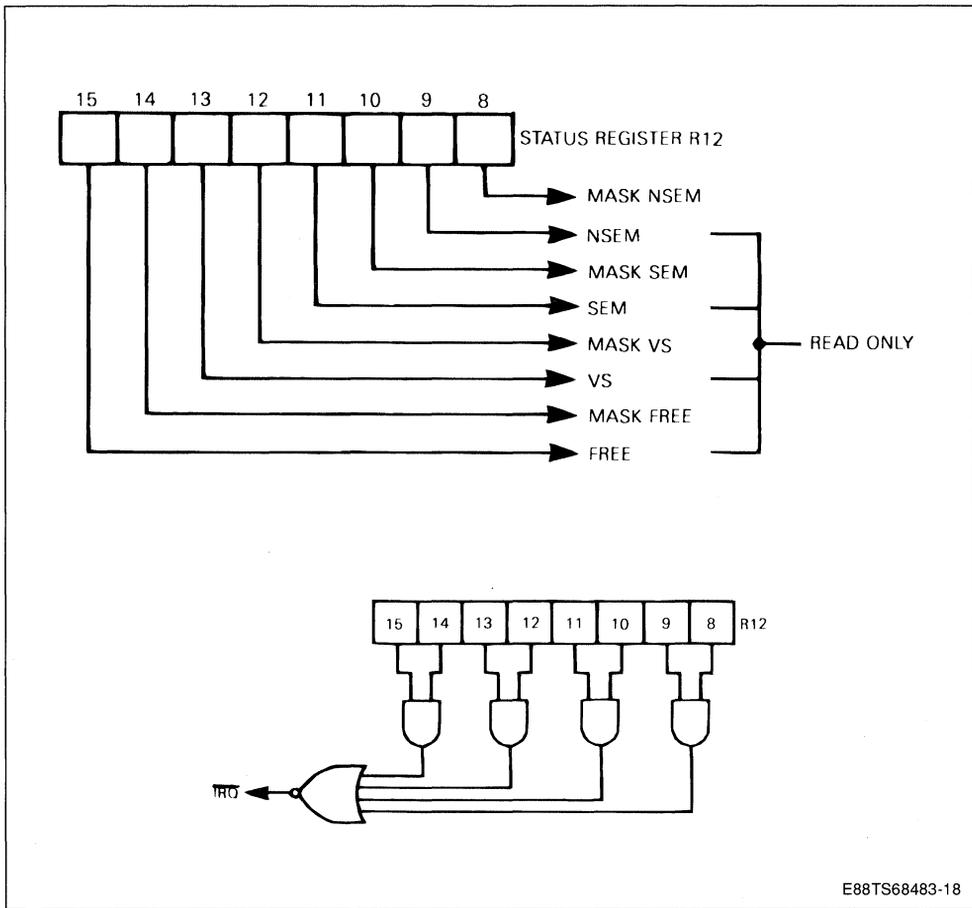
- FREE : this status bit is set when no execution is pending
- VS : vertical synchronization state
- SEM : this status bit is set when the FIFO memory word is inaccessible to the microprocessor during a viewport transfer

ring a viewport transfer

- NSEM : this status bit is set when the FIFO memory word is accessible to the microprocessor during a viewport transfer.

Each of these status bits is maskable. The masked status bits are NORed to the IRQ output pin.

Figure 2.9. : Status Register.



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### 3. MICROPROCESSOR INTERFACE

#### 3.1. INTRODUCTION

The TS68483 is directly compatible with any popular 8 or 16-bit host microprocessor ; either Motorola type (6809, 68008, 68000) or Intel type (8088, 8086).

The host microprocessor has direct access to any of the twenty four 16-bit on-chip registers through the microprocessor interface pins :

- D(0:15) : 16 bidirectional data pins.
- A(0:7) : 8 address inputs
- AE, DS, R/ W, CS : 4 control inputs.

The twenty four registers are mapped in the host addressing space as 256 byte addresses. (see figure 3.2)

- A(1:5) select one out of 24 registers.
- A0 selects the low order byte (A0 = 1) or the high order byte (A0 = 0) of the selected register.
- A(6:7) provide the command execution condition.

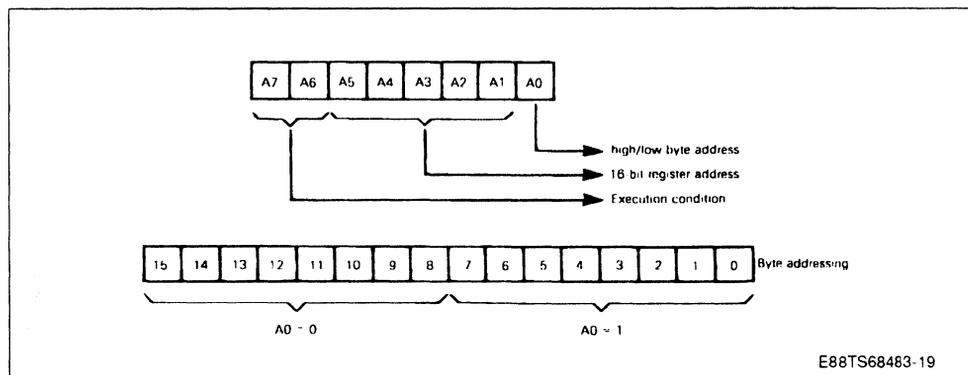
The host microprocessor bus may be either 8 or 16-bits wide and may be address/data multiplexed or not.

The two flags MB and BW in the CONFIGURATION register R10 allow the data bus size and multiplexed/non-multiplexed organization to be specified. (see figure 3.1).

Figure 3.1. : MPU Selection.

Type of MPU Bus		Conf. Reg.		TS68483 Pins					
		BW	MB	AE	DS or LDS	R/W	AO	A (1 : 7)	D (8 : 15)
Non Mux	16-bit (68000)	0	0	1	UDS or LDS	R/W	O	A (1 : 7)	D (8 : 15)
	8-bit (68008)	1	0	1	DS	R/W	AO	A (1 : 7)	D (0 : 7)
Mux	16-bit (8086)	0	1	ALE	RD	WR	O	AD (1 : 7)	AD (8 : 15)
	8-bit (8088)	1	1	ALE	RD	WR	ADO	AD (1 : 7)	AD (0 : 7)

Figure 3.2. : On-Chip Address and Byte Packing.



3.2. HARDWARE RECOMMENDATIONS (see timing diagrams 1 and 2).

A0-PIN :

1. When using a 16-bit data bus, the A0 input pin must be grounded. No single byte access can be performed.

2. In order to conform with the high byte/low byte on-chip packing, the A0 input pin must be inverted when using an 8-bit bus Intel type microprocessor (8088 for example).

A(1:7), D(0:7), D(8:15) pins :

1. With any 8-bit data bus, the D(0:7) and D(8:15) pins must be paired in order to demultiplex the low order data bytes and the high order data bytes.

2. When using address/data multiplexed bus, the D(0:7) pins are paired with A(0:7) in order to demultiplex data from address.

$\overline{AE}$ ,  $\overline{DS}$ , R/  $\overline{W}$ ,  $\overline{CS}$  :

See pin description.

3.3 SOFTWARE RECOMMENDATIONS

1. The CONFIGURATION register R10 must be first initialized.

The BW 15 flag is interpreted by the bus interface to recognize an 8-bit/16-bit data bus.

The MB and BW 15 flags are used to decide when to initiate a command execution.

2. Each register byte has 4 addresses in the microprocessor memory map. These 4 addresses differ only by A(6:7). This scheme allows a 68008 programmer to read or write any data type (byte, word, long word) and automatically initiate or not a command execution at the end of this transfer. The transfer lasts one, two or four bus cycles.

A 68000 programmer is restricted to only word and long word data types. (see figure 3.3).

Figure 3.3. : Command Execution Condition.

Address		Execution Condition	Data Type Transfer	
A7	A6		8-bit Data Bus	16-bit Data Bus
0	0	no Exec	Any Type	Any Type
0	1	Exec after a Bus Cycle	1 Byte	1 Word
1	0	Exec After 2 Bus Cycles	1 Word	1 Long Word
1	1	Exec after 4 Bus Cycles	1 Long Word*	ILLEGAL

Notes : Word transfer must respect word boundary.  
 Long word transfer must respect long word boundary.  
 \* Not available with 8088 MPU type.

Figure 3.4. : Interface with TS68000/68008 MPU.

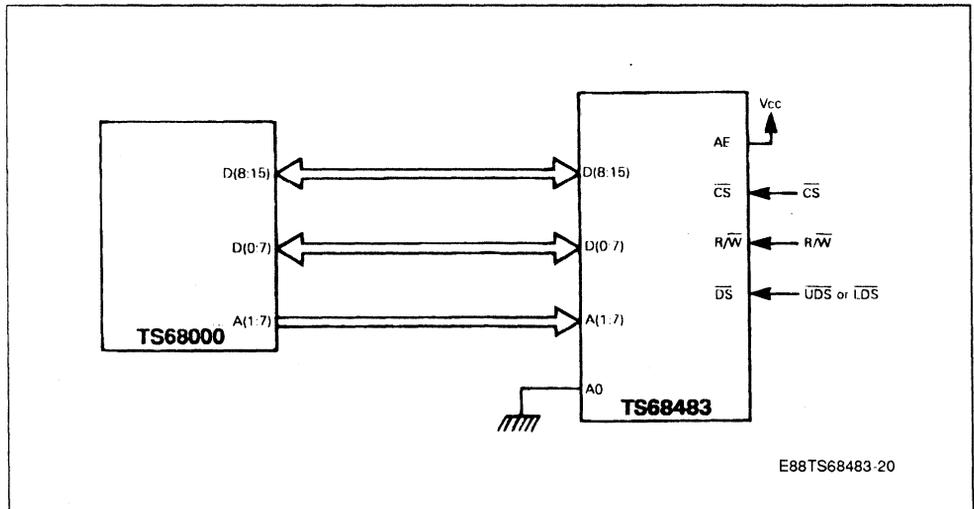


Figure 3.4. : Interface with TS68000/68008 MPU (continued).

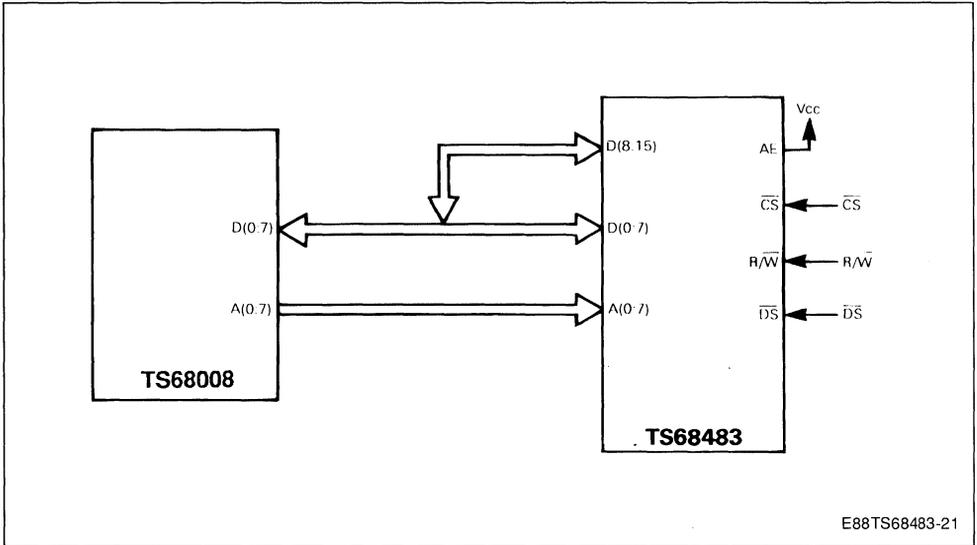


Figure 3.5. : Interface with 8086/8088 MPU.

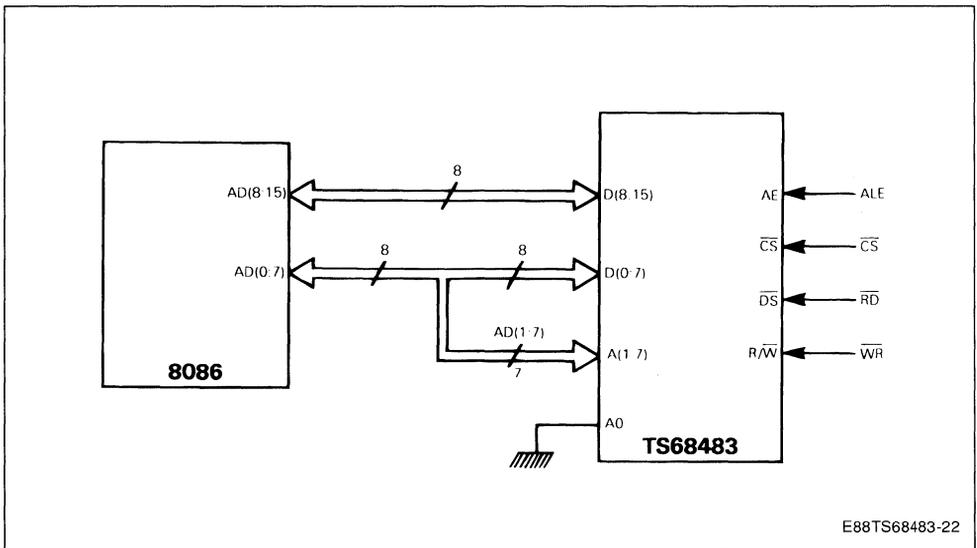
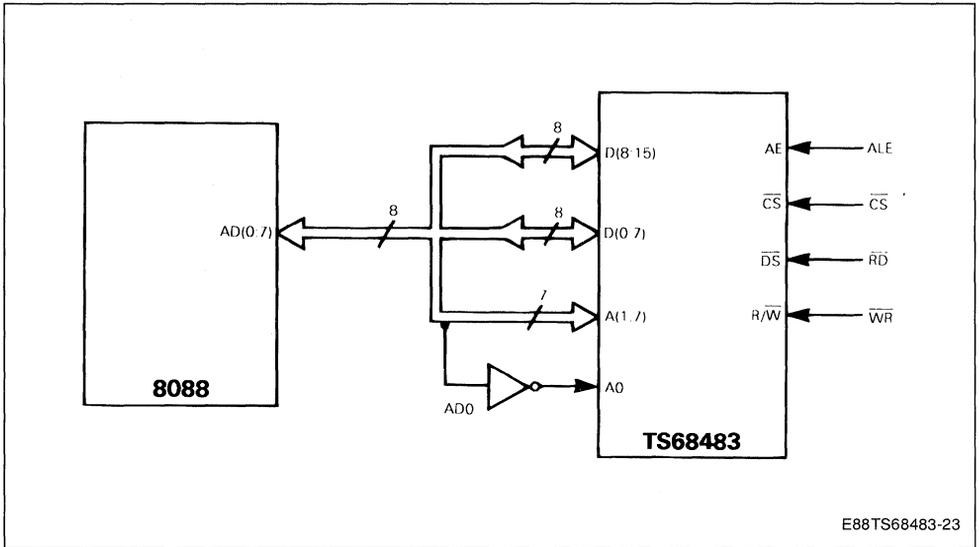


Figure 3.5. : Interface with 8086/8088 MPU (continued).



**4. THE VIDEO TIMING GENERATOR RAM REFRESH AND DISPLAY PROCESS**

**4.1. INTRODUCTION**

The Video Timing Generator is completely synchronous with the CLK input, which provides a pixel shift frequency (up to 18 MHz). The Video Timing Generator :

- delivers the blanking signal (BLK), the horizontal (HS) and vertical (VS) synchronization signals on respective output pins,
- schedules the memory time allocated to the display process, dynamic RAM refresh and command execution,
- is fully programmable
- can be synchronized with an external composite video sync signal connected to the SYNC IN input.

**4.2. SCAN PARAMETERS** (see table 1 and timing diagram 5)

**4.2.1. Timing Units.** The time unit of any vertical parameter is the scan line.

The time unit of any horizontal parameter is the memory cycle, which is 8 periods of the CLK input signal.

These two parameters are internally programmed :

- Horizontal sync pulse duration = 7 cycles
- Vertical sync pulse duration = 2.5 lines.

**4.2.2 Blanking Interval.** The blanking interval starts :

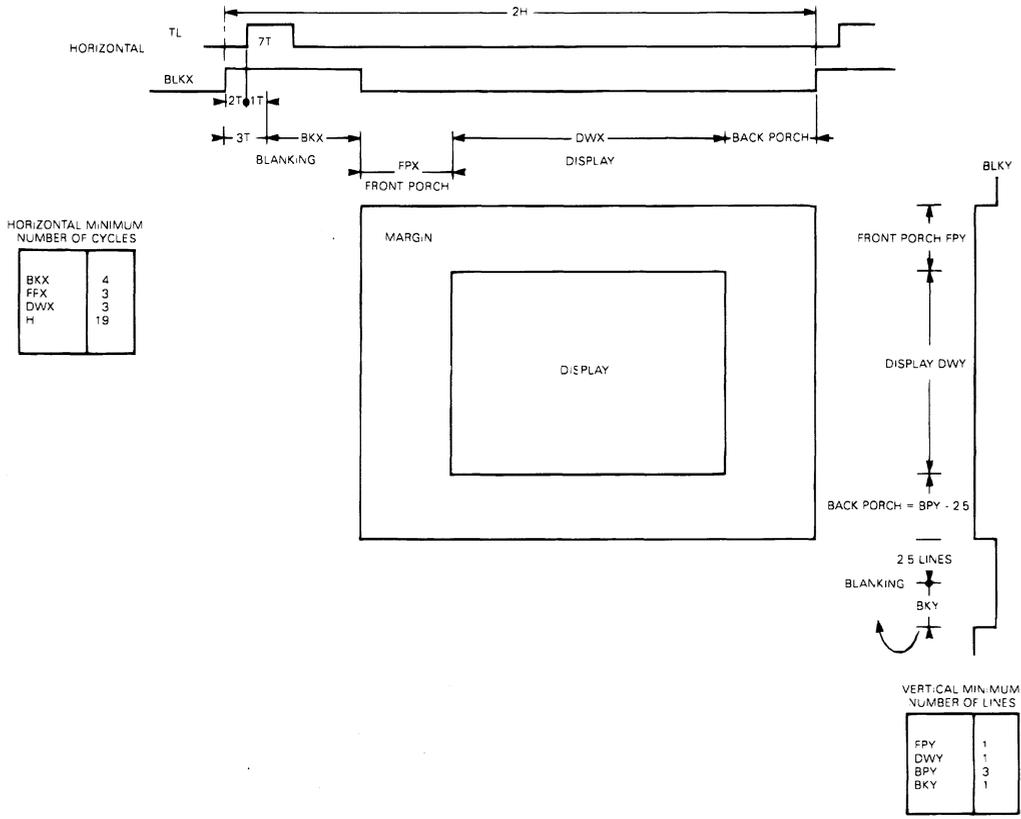
- at the leading edge of the vertical sync pulse. Vertical blanking interval actual duration is 2.5 lines more than the programmed value.
- two cycles before the leading edge of the horizontal sync pulse. The actual horizontal blanking interval duration is 3 cycles more than the programmed value.

**Note :** During the programmed blanking interval, the video output pins P(0:3) are forced low.

**4.2.3. Porch and Margin Color.** During the porch interval, the programmable margin color is displayed on the P(0:3) outputs.

The display process may be disabled by setting DPD flag. This will be interpreted as a porch extension.

Figure 4.1 : Video Programming.



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**4.2.4. Memory Time Sharing** (see figure 4.1). The Video Timing Generator allocates memory cycles to either the display process, RAM refresh or command execution. In this respect, the scan lines per field are split between :

- the DWY displayable lines.

When VRE = 0, Video RAMs are not used.

The DWY x DWX cycles in the display interval are allocated to the display process when it is enabled (DPD = 0). When the display process is disabled, these cycles are allocated as for non displayable lines.

When VRE = 1, one cycle per display line is allocated to the display process. Other cycles are allocated as for non displayable lines. The last period of the BLKX signal may be used to load the internal video RAM shift register.

- the non displayable lines. In one out of nine non displayable lines, DWX cycles are allocated to the refresh process when it is enabled (RFD = 0).
- In Float cycle, an external X address must be provided. The Y address is still provided on ADM(0:7) and Y(0:2), while ADM(8:15) are in high impedance state.

**4.2.5. Command Access Ratio.** This allocation scheme leaves about 50 % of the memory bandwidth for command access when programming a standard TV scan. This ratio drops to the 30 % range when a better monitor is in use (32 µs out of 43 µs displayable per line, 360 lines out of 390 for a 60 Hz field rate). The higher resolution means more memory accesses in order to edit a given percentage of the screen area. In this case Video RAMs are very helpful to keep 90 % of the memory bandwidth available for command access.

**4.3. DISPLAY PROCESS**

The Video Timing Generator allocates memory cycles to the Display Processor in order to read the Display Viewport from memory. The Display Viewport upper left corner address is programmable through DIB, YOR and XOR. The display viewport dimensions are related to the display interval of DWY lines by DWX cycles per field.

**4.3.1. Y Addresses.** When INE = 0, the fields are not interlaced. The Y Display Viewport address is

**Table : 4.3.2.**

MODX1	MODX0	X INCR	Video Shift Register	Memory Cycle Type
0	0	+ 1	Internal	Read
0	1	+ 1	External	Dummy Read
1	0	+ 2	External	Dummy Read
1	1		External	Float

initialized with YOR at the first displayable line then decremented by 1 at each scan line. The Display Viewport is thus DWY pel high.

When INE = 1, the fields are interlaced. The Y Display Viewport address is initialized as shown in the table below. It is then decremented by two at each scan line. The viewport is thus 2 x DWY pel high.

	Even Field	Odd Field
Yor Even	Yor	Yor + 1
Yor Odd	Yor - 1	Yor

Y Display Viewport address initialization when INE = 1.

**4.3.2. X Addresses and MODX Flags.** The X Display Viewport address is initialized with XOR at the first displayable cycle of each displayable line. It is then incremented at each subsequent cycle according to MODX flags.(see table 4.3.2)

- In internal mode, the Display Viewport is 8. DWX pel wide. The on-chip video shift register are used.
- In Dummy read, the memory is read but the on-chip video shift registers are not loaded, instead they retain their margin color. External video shift registers are presumed to be loaded by either 8 pels or 16 pels per cycle according to the programmed increment value.
- In Float cycle, an external X address must be provided. The Y address is still provided on ADM(0:7) and Y(0:2), while ADM(8:15) are in high impedance state.

**Note :** See Memory Organization and Memory Timing for further details on the memory cycles.

**4.3.3. The Video RAM Case (VRE = 1).** In this case, the last cycle of the horizontal blanking interval is systematically allocated to the display process for DWY scan lines per field.

This cycle bears the scan line address, the bank number and the X address which is always XOR.

MODX must be programmed to use external shift register (Dummy read).

**4.3.4. PAN and TILT.** The host can tilt or pan the Display Viewport through the frame buffer by modifying YOR or XOR arguments. Panning is performed on 8 pel boundaries.

#### 4.4. DYNAMIC RAM REFRESH

No memory cycles are explicitly allocated to the RAM refresh when RFD = 1.

When VRE = 0 and DPD = 0, the Display Process is supposed to be able to over-refresh dynamic components. This can be done by careful logical to component address mapping. During the remaining non displayable lines, the Display Viewport address continues to be incremented : Y address on each line according to INE, X address initialized by XOR then incremented according to MODX. This Display viewport address is allowed to address the memory for DWX cycles in only one line out of nine for refresh purposes.

When VRE = 1 or DPD = 1, any line is processed as a non displayable line with respect to the refresh process.

#### 4.5. CONFIGURATION AND EXTERNAL SYNCHRONIZATION

The R10 register holds eight configuration flags. Six of these flags are dedicated to the Video Timing Generator.

\_ SSP : this flag selects the synchronization output pin configuration :

\_ NPC, NHVS, NBLK : these three flags invert the PC/HS, HVS/VS and BLK outputs respectively. (Ex. : When NBLK = 1 blanking is active high).

The SYNC IN input pin provides an external composite synchronization signal input from which a Vertical Sync In (VSI) signal is extracted. The SYNC IN signal is sampled on-chip at CLK frequency. Its rising sampled edge is compared to the leading edge of HS. A PC comparison signal is externally available (see SSP and NPC flags).

VSIE : this flag enables VSI to reset the internal line count.

HSIE : this flag enables the rising edge of SYNC IN to act directly on the Video Timing Generator. When the leading edge of HS does not match at 1 clock period a rising edge of SYNC IN, one extended cycle is performed (nine clock periods instead of eight).

Flag	Output Pins	
	PC/HS	HVS/VS
SSP = 1	HS	VS
SSP = 0	PC	HVS

Table 1.

Name	Number of Bits	Minimum Values	Register	Description	Function
DWY	10	1	R9	Number of Display lines per Field	Vertical Scan
INE	1		R8	Interlace Enable when INE = 1	
BKY	5	1	R8	Number of Lines in Vertical Blanking – 2.5	
FPY	5	1	R7	Number of Lines in Vertical Front Porch	
BPY	8	3	R6	Number of Lines in Vertical Back Porch + 2.5	Horizontal Scan
H	6	19	R6	Number of Double Cycles per Line	
FPX	4	3	R8	Number of Cycles in Horizontal Front Porch	
BKX	4	4	R8	Number of Cycles in Horizontal Blanking – 3	
DWX	7	3	R7	Number of Cycles of the Display Window	Display Process
XOR	8		R4	X, Y, and bank logical address in the display memory of the display viewport upper left corner	
YOR	11		R5		
DIB	2		R4		
MODX	2		R9	Selection of the X Addressing Mode	Memory Time Sharing
MC	4		R4	Margin Color	
RFD	1		R7	RAM Refresh Disable when RFD = 1	
DPD	1		R7	Display Process Disable when DPD = 1	
VRE	1		R8	Video RAM Enable When VRE = 1	

Note : one cycle = 8 periods of CLK Clock.

## 5. MEMORY ORGANIZATION

### 5.1. INTRODUCTION

The display memory is logically organized as four banks of 4-bit planes. Thus a bit address in the display memory is given by the quadruplet :

- \_ B = bank number, from 0 to 3
- \_ Z = plane number, from 0 to 3
- \_ X = bit address into the plane, from 0 to 2047
- \_ Y = bit address into the plane, from 0 to 2047.

In one memory cycle (8 CLK periods), the controller can access a memory word. This 32-bit memory word holds one byte from each plane in a given bank. In order to address this memory word, the controller supplies :

- \_ B(0:1) : binary value of the bank number
- \_ X(3:10) : binary value of the word address
- \_ Y(0:10) : binary value of the word address.

Z and X(0:2) are not supplied. They give only a bit address in a memory word.

### 5.2. MEMORY CYCLES

24 pins are dedicated to the memory interface.

- \_ ADM(0:15) : these 16 bidirectional pins are multiplexed three times during a memory cycle (see Timing Diagram 3) :

TA : address period. Output of the X(3:11) and Y(3:11) address

TO : even data period. The even Z bytes are either input or output.

T1 : odd data period. The odd Z bytes are either input or output.

- \_ Y(0:2) : three LSB Y address output pins (non-multiplexed)
- \_ B(0:1) : two bank address output pins (non-multiplexed)
- \_ CYS : Cycle start strobe output (non-multiplexed).

CYS is at CLK/8 frequency. A CYS pulse is delivered only when a command, display or refresh cycle is performed.

- \_ CYF(0:1) : Two cycle status outputs (non-multiplexed). Four cycle types are defined :

Command read

Command write

RAM refresh

Display access.

Because several options may be selected for RAM refresh and display access by the MODX and VRE flags (see Video Timing Section), there are more than four memory cycle types (see Timing Diagram 3 and table 2).

### 5.3. DISPLAY MEMORY DESIGN OVERVIEW

The display memory implementation is application dependant. The basic parameters are :

- \_ the number of pixels to be displayed Nx.Ny
- \_ the number of bits per pel
- \_ the vertical scanning frequency, which must be picked in the 40 Hz to 80 Hz range (non interlaced) or in the 60 Hz to 80 Hz range (interlaced).

This yields a rough estimate of the pixel frequency. When the pixel frequency is in the 15 to 18 MHz range and 4 bits per pixel or least are required, the on-chip video registers and standard dynamic RAM components may be used. When higher pixel rates or up to 8 bits per pixel are required, the designer must provide external shift registers. Video RAM components may also be considered.

In either case, the user must design :

- \_ A memory block. This is the hardware memory building block. It includes the video shift registers if on-chip VSR cannot be used. It implies a RAM component choice.
- \_ An Address Mapper, which maps the logical address into hardware address : block selection, Row Address (RAD), Column Address (CAD).
- \_ A memory cycle controller. This controller monitors the CYF and CYS output pins from TS68483 and block address from the Mapper. It provides :
  - The CLK signal to the TS68483 and a shift clock SCLC when external video shift registers are used
  - $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{OE}}$ , R/  $\overline{\text{W}}$  signals to the memory blocks
  - RAD and CAD Enable signals to the Mapper.

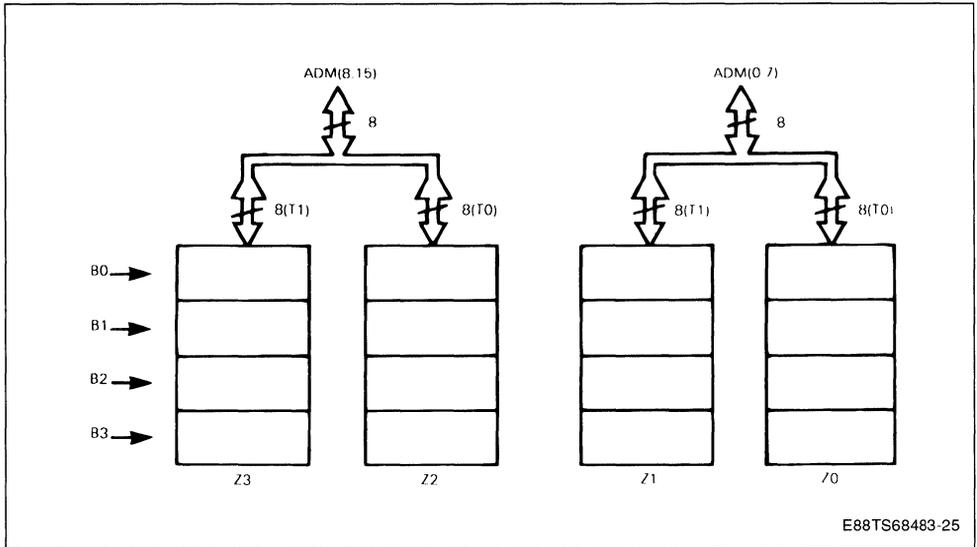
**5.3.1. Frame Buffer** (see figure 5.1.). A byte wide organization of each bit plane is required. Obviously a bit plane must contain the Display Viewport size. A straight organization implements only one bit plane per block.

It may be cost effective to implement several bit planes per block. Two basic schemes may be used :

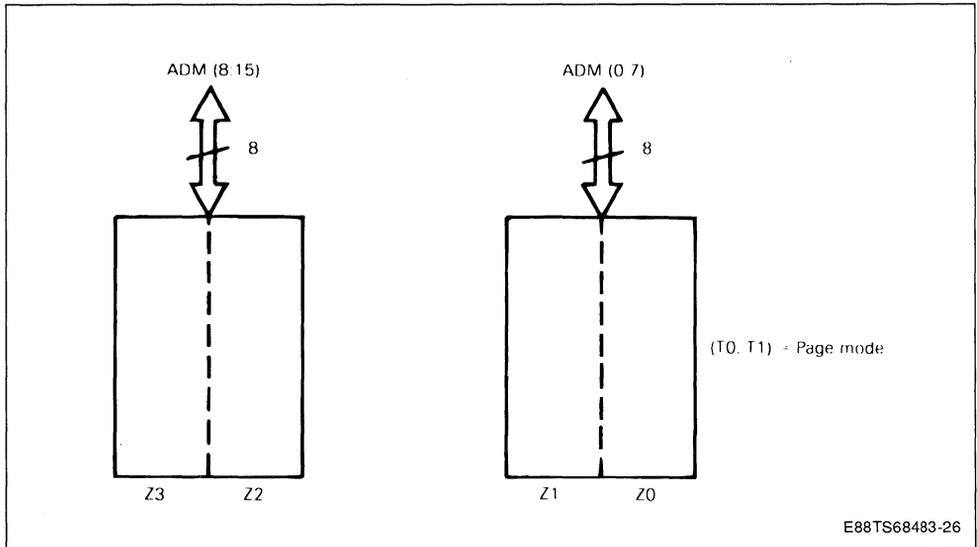
- \_ One block, one Z : several bit planes, belonging to different banks, but addressed by the same Z, share a given block. There is little time constraint if any.
- \_ One block, two Z : two bit planes, belonging to the same bank share a given block. In this case, this block must be accessed twice during a memory cycle. This can be solved by two successive page mode accesses.

**5.3.2. Masking Planes.** Masking planes are very useful for general purpose area filling or clipping. It

ONE BLOCK-ONE Z



ONE BLOCK-TWO Z



(T0, T1) = Page mode

Figure 5.1. : Frame Buffer Organization.

Typical Block Size	16 k x 8	32 k x 8	64 k x 8	256 k x 8
One Block-one Bit Planes	512 x 256	512 x 512	1024 x 512	2048 x 1024
One Block-two Bit Planes	256 x 256	512 x 256	512 x 512	

COMPONENTS :

64K BITS : 16K x 4 or 64K x 1

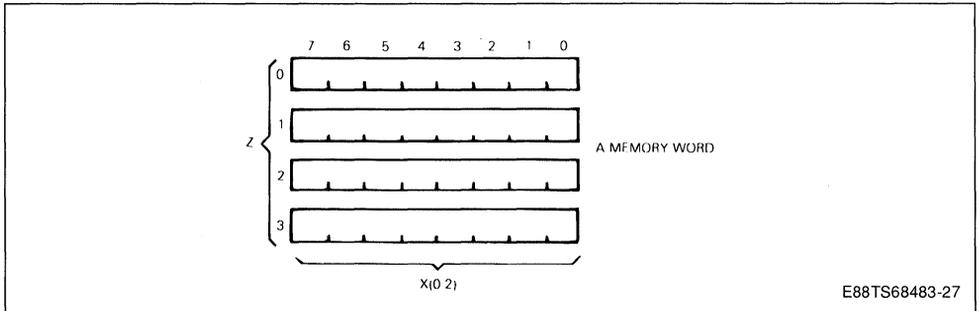
256K BITS : 32K x 8, 64K x 4, 256K x 1

VIDEO RAM : 64K x 1, 64K x 4

Table 2 : Memory Cycle Types.

Output Pins		Function	Modx Flags 1 0	Multiplexed ADM			Cycle Type
CYF1	CYF0			TA	T0	T1	
1	0	Command Read		Y,X	Z0,Z2	Z1,Z3	Read
1	1	Command Write		Y,X	Z0,Z2	Z1,Z3	Write
0	1	Display	0 0 0 1	Y,X Y,X	Z0,Z2	Z1,Z3	Read Dummy Read + 1
0	0	Refresh	1 0 1 1	Y,X Y,Hi-Z			Dummy Read + 2 Float X

Refresh : dummy read cycle is performed.



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Figure 5.2. : The Multiplexing Scheme.

HIGHER BYTES

ADMS Multiplexed Pins	15	14	13	12	11	10	9	8
TA : Address Period	10			X			3	
T0 : Even Z Byte Period	7			Z = 2			0	
T1 : Odd Z Byte Period	7			Z = 3			0	

LOWER BYTES

ADMS Multiplexed Pins	7	6	5	4	3	2	1	0
TA : Address Period	10			Y			3	
T0 : Even Z Byte Period	7			Z = 0			0	
T1 : Odd Z Byte Period	7			Z = 1			0	

may be practical to use one or two planes smaller than the color bit plane if they cyclically cover a frame buffer.

The masking planes must be in bank 3.

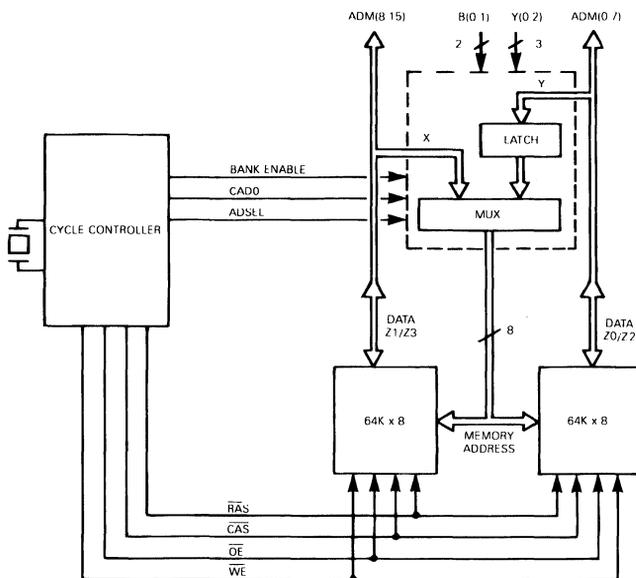
**5.3.3. Objects and Characters.** Objects may be located in unused parts of the frame buffer.

Character generators can be implemented in any plane of any bank. They can also be implemented in ROM. In this case, plane Z = 1 or 3 offer relaxed access time requirements.

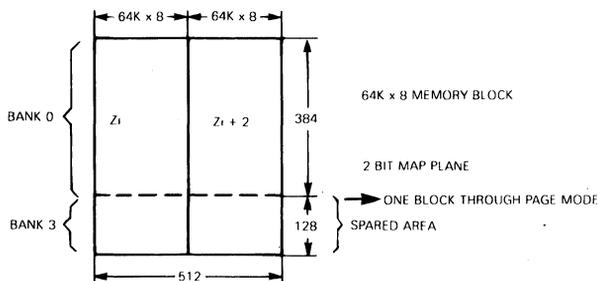
5.4. EXAMPLES

Figure 5.3. gives the schematic for a 512 x 384 non interlaced application. A CLK signal in the 15 to 18 MHz range should produce a 50 to 60 Hz refresh rate. The on-chip video shift registers may be used if no more than four bits per pixel are required. One 64 K x 8 memory block may be implemented using either eight 64 K x 1 or two 64 K x 4 components. One memory block holds two 512 x 384 color bit planes.

Figure 5.3. : Memory Organization for 512 x 384 Application.



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**6. TIMING DIAGRAM**

**6.1. MICROPROCESSOR INTERFACE**

TS68483 has an eight bit address bus and a sixteen bit data bus. Little external logic is needed to adapt bus control signals from most of the common multiplexed or non-multiplexed bus microprocessors.

Microprocessor interface timing : A(0:7), D(0:15), AE, DS, CS, R/ W

$V_{CC} = 5.0\text{ V} \pm 5\%$ ,  $T_A = T_L$  to  $T_H$ ,  $C_L = 100\text{ pF}$  on D(0:15)

Reference levels :  $V_{IL} = 0.8\text{ V}$  and  $V_{IH} = 2\text{ V}$  on all inputs

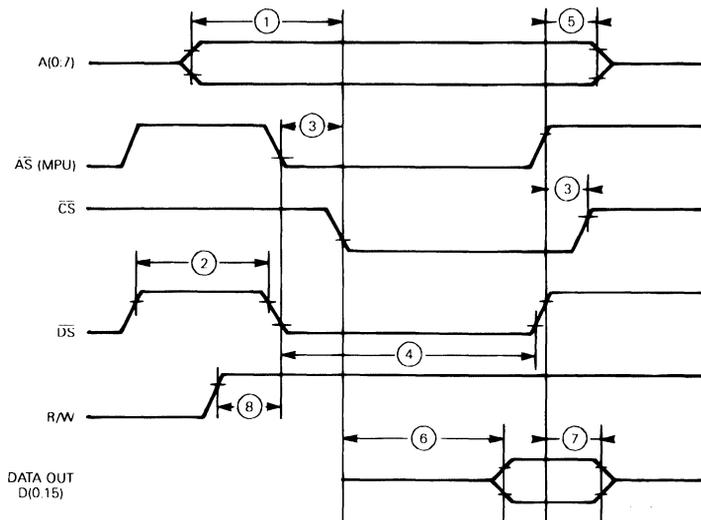
$V_{OL} = 0.4\text{ V}$  and  $V_{OH} = 2.4\text{ V}$  on all outputs

**UNMUX MODE**

<b>Id. Numb.</b>	<b>Parameter</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
1	Address Set up Time from $\overline{CS}$	0		ns
2	Data Strobe Width (high)	65		ns
3	$\overline{AS}$ Set up Time from $\overline{CS}$	0		ns
4	Data Strobe Width-low (read cycle)	160		ns
5	Address Hold Time from $\overline{DS}$	0		ns
6	Data Access time from $\overline{CS}$ (read cycle)		130	ns
7	$\overline{DS}$ Inactive to High Impedance State (read cycle)	10	80	ns
8	R/W Set up Time from $\overline{DS}$	20		ns
9	$\overline{DS}$ Width-low (write cycle)	80		ns
10	$\overline{CS}$ Set up Time from $\overline{DS}$ Active (write Cycle)	0		ns
11	Data in Set up Time from $\overline{DS}$ active (write cycle)	10		ns
12	Data in Hold Time from $\overline{DS}$ Inactive (write cycle)	15		ns

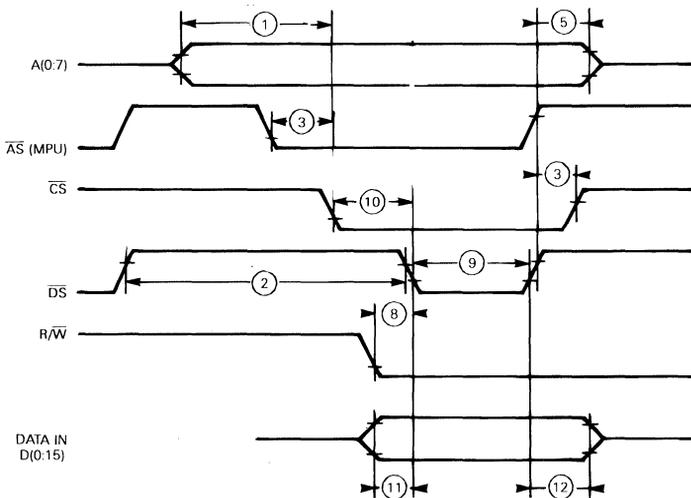
UNMUX MODE

READ CYCLE



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WRITE CYCLE



E88TS68483-31

**MUX MODE**Microprocessor Interface Timing : A (0 : 7), D (0 : 15),  $\overline{AE}$ ,  $\overline{DS}$ ,  $\overline{CS}$ ,  $\overline{R/W}$  $V_{CC} = 5.0 \text{ V} \pm 5\%$ ,  $T_A = T_L$  to  $T_H$ ,  $C_L = 100 \text{ pF}$  on D (0 : 15)Reference Levels :  $V_{IL} = 0.8 \text{ V}$  and  $V_{IH} = 2 \text{ V}$  on All Inputs $V_{OL} = 0.4 \text{ V}$  and  $V_{OH} = 2.4 \text{ V}$  on All Outputs

Id. Numb.	Parameter	Min.	Max.	Unit
1	AE Width High	90		ns
2	Address Set up Time to AE Inactive	55		ns
3	Address and $\overline{CS}$ Hold Time to AE Inactive	55		ns
4	$\overline{CS}$ Set up Time to AE Inactive	40		ns
5	$\overline{DS}$ and $\overline{R/W}$ High	150		ns
6	$\overline{DS}$ Width-low (read)	240		ns
7	$\overline{R/W}$ Width-low (write)	110		ns
8	Data Access Time From $\overline{DS}$ (read)		210	ns
9	Data in Set up time from $\overline{R/W}$ Inactive (write)	150		ns
10	$\overline{DS}$ Inactive to High Impedance State (read)	10	100	ns
11	Data in Hold Time from $\overline{R/W}$ Inactive (write)	30		ns
12	AE Inactive to $\overline{DS}$ Active	20		ns
13	AE Inactive to $\overline{R/W}$ Active	20		ns
14	$\overline{DS}$ Inactive to AE Active	10		ns
15	$\overline{R/W}$ Inactive to AE Active	10		ns
16	$\overline{R/W}$ Inactive to Next Address Valid	100		ns
17	$\overline{DS}$ Inactive to Next Address Active	100		ns
18	Data in Set up Time from $\overline{R/W}$ Active (fast write cycle)	10		ns

**6.2. MEMORY INTERFACE**

ADM (0 : 15), B (0 : 1), CYF (0 : 1), Y (0 : 2), CYS

 $V_{CC} = 5.0 \text{ V} \pm 5\%$ ,  $T_A = T_L$  to  $T_H$ 

CLK Duty Cycle = 50 %, Period T

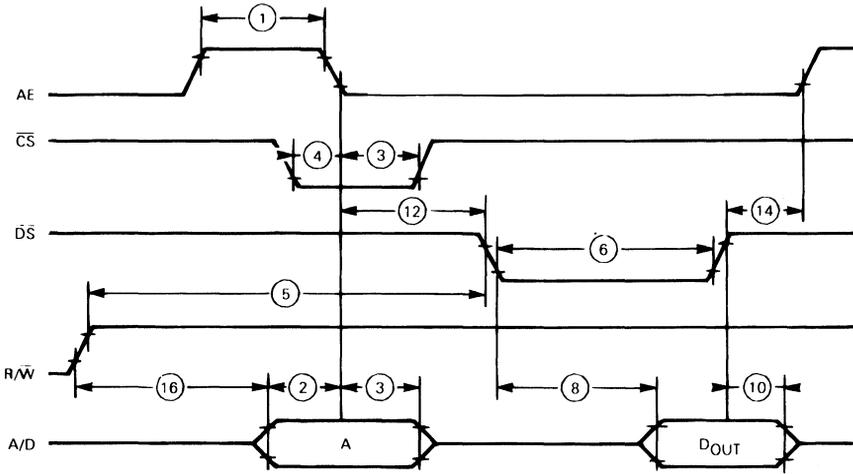
Reference Levels :  $V_{IL} = 0.8 \text{ V}$  and  $V_{IH} = 2 \text{ V}$ ,  $V_{OL} = 0.4 \text{ V}$  and  $V_{OH} = 2.4 \text{ V}$ 

Indent Number	Parameter	TS68483-15		TS68483-18		Unit
		Min.	Max.	Min.	Max.	
1	TCLK Clock Period	66	166	55	166	ns
2	Memory Cycle Time ( $T = 8 \times \text{TCLK}$ )					ns
3	Output Delay Time from CLK		40		35	ns
4	Output Data HI-Z Time from CLK		40		35	ns
5	Output Hold Time from CLK	10		10		ns
6	Input Data Hold Time from CLK (read cycle)	10		6		ns
7	Input Data Set up Time from CLK (read cycle)	20		10		ns
8	Input Data HI-Z Time from CLK		TCLK		TCLK	ns

**Note** : All timing is referenced to the rising edge of CLK (see timing diagram 3).

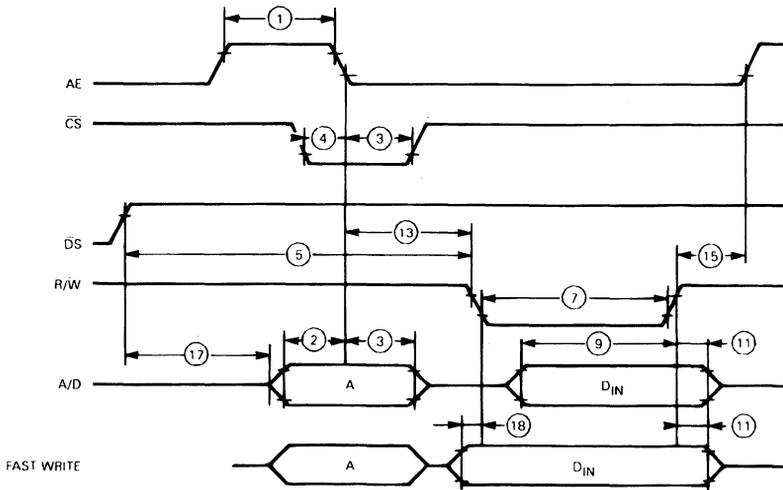
MUX MODE

READ CYCLE



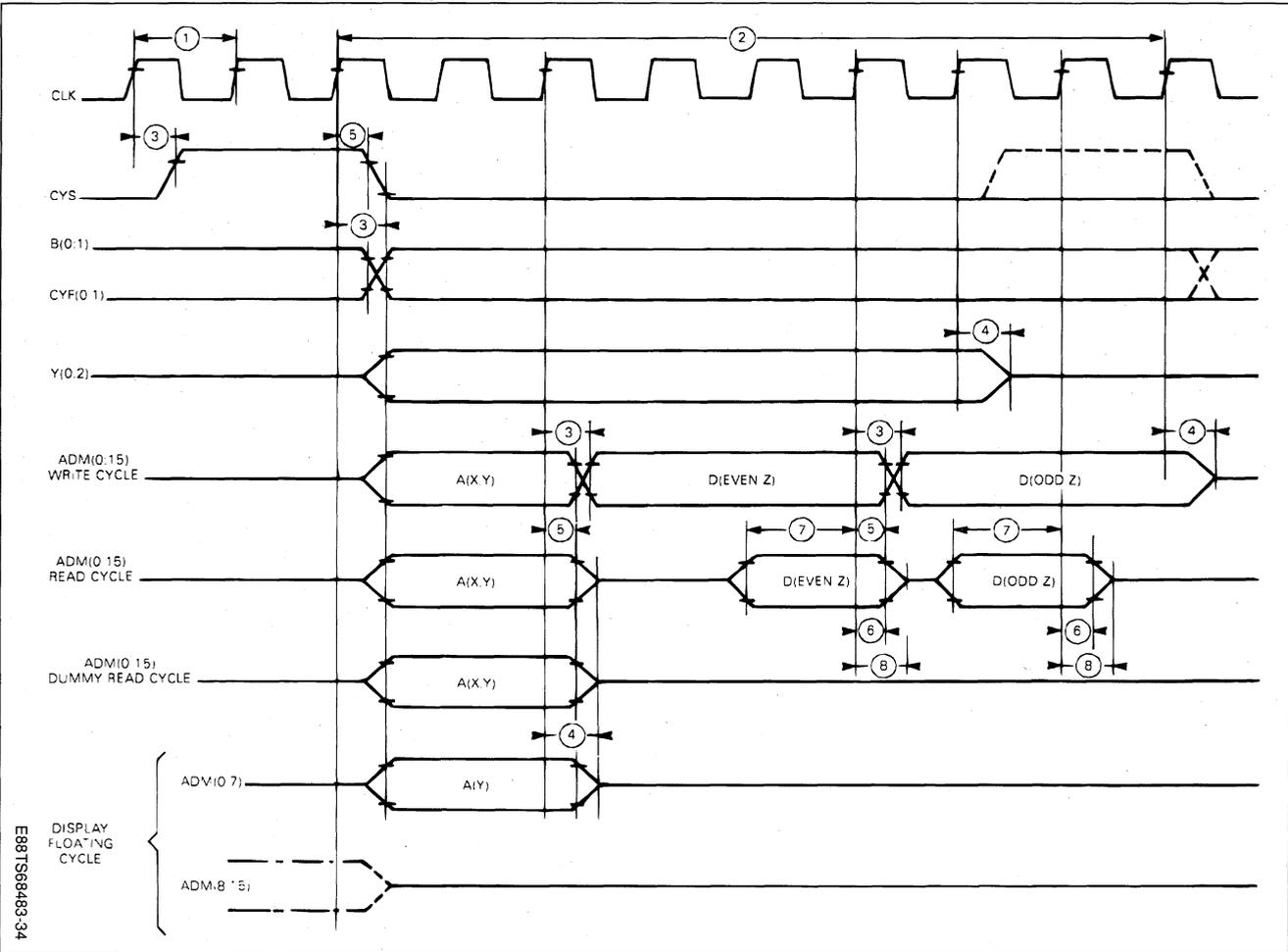
E88TS68483-32

WRITE CYCLE



FAST WRITE

E88TS68483-33



E88TS68483-34

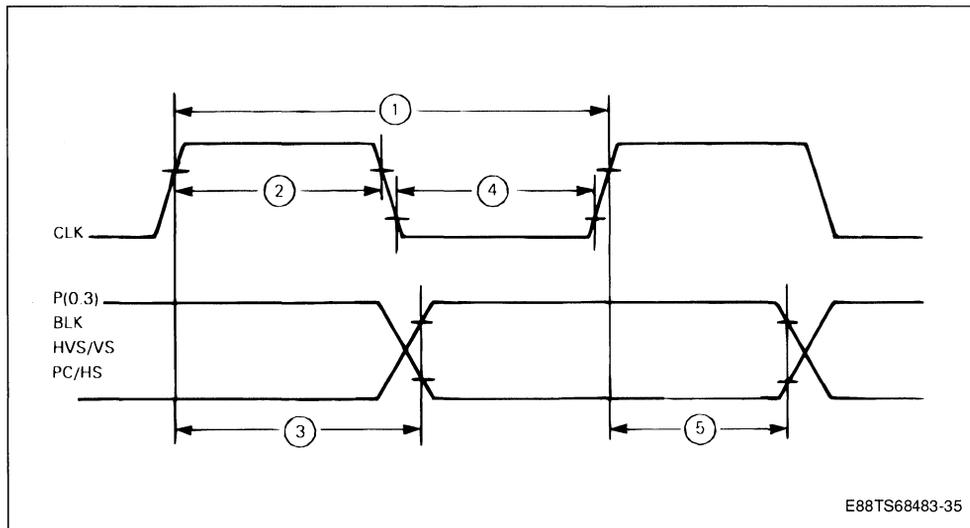
6.3. VIDEO INTERFACE

P0, P1, P2, P3, BLK, HVS/VS, PC/HS

$V_{CC} = 5.0\text{ V} \pm 5\%$ ,  $T_A = T_L$  to  $T_H$ , CLK duty cycle = 50 %

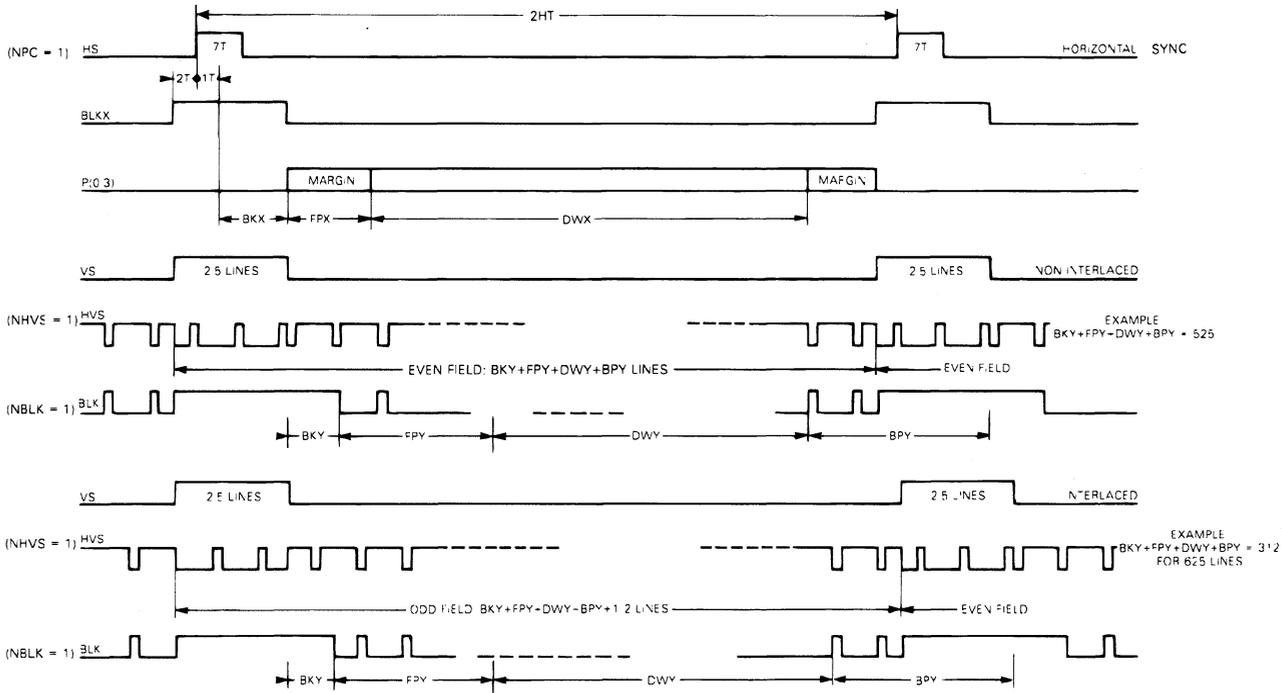
Reference levels :  $V_{IL} = 0.8\text{ V}$  and  $V_{IH} = 2\text{ V}$ ,  $V_{OL} = 0.4\text{ V}$  and  $V_{OH} = 2.4\text{ V}$ ,  $C_L = 50\text{ pF}$

TIMING DIAGRAM 4.



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Indent Number	Parameter	TS68483-15		TS68483-18		Unit
		Min.	Max.	Min.	Max.	
1	TCLK : CLK Period	66	166	55	166	ns
2	CLK High Pulse Width	28		23		ns
3	Output Delay from CLK Rising Edge		40		30	ns
4	CLK Low Pulse Width	28		23		ns
5	Output Hold Time	10		10		ns



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**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$ *	Supply Voltage	- 0.3 to 7.0	V
$V_{in}$ *	Input Voltage	- 0.3 to 7.0	V
$T_A$	Operating Temperature Range	$T_L$ to $T_H$ 0 to 70	°C
$T_{stg}$	Storage Temperature Range	- 55 to 150	°C
$P_{Dm}$	Max Power Dissipation	1.5	W

\* With respect to  $V_{SS}$ .

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specifications is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

**ELECTRICAL CHARACTERISTICS**

( $V_{CC} = 5.0\text{ V} \pm 5\%$ ,  $V_{SS} = 0$ ,  $T_A = T_L$  to  $T_H$ ) (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{CC}$	Supply Voltage	4.75	5	5.25	V
$V_{IL}$	Input Low Voltage	- 0.3		0.8	V
$V_{IH}$	Input High Voltage	2		$V_{CC}$	V
$i_{in}$	Input Leakage Current			10	$\mu\text{A}$
$V_{OH}$	Output High Voltage ( $I_{load} = - 500\ \mu\text{A}$ )	2.4			V
$V_{OL}$	Output Low Voltage $I_{load} = 4\ \text{mA}$ ; ADM (0 : 15) $I_{load} = 1\ \text{mA}$ ; other Outputs			0.4	V
$P_D$	Power Dissipation		700		mW
$C_{in}$	Input Capacitance			15	pF
$I_{TSI}$	Three State (off state) Input Current			10	$\mu\text{A}$

SECTION 7

7.1. REGISTER MAP AND COMMAND TABLE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
R0	COMMAND								MODE												
R1	SX				SY				Odd bank		C0	Even bank									
R2									Odd bank		C1	Even bank									
R3	TEXLIN																				
R4	XOR								0		DIB1	DIB0	MARGIN COLOR								
R5									YOR												
R6					H				BPY												
R7					DWX				DPD	RFD					FPY						
R8	FPX				BKX				VRE	INE					BKY						
R9	0					MODX1					MODX0							DWY			
R10	BW	MB	VSIE	HSIE	NBLK	NHVS	NPC	SYNC													
R11																					
R12	STATUS																				
R13									S	DY				S	DX						
DEST. POINTER	R14	Bd	-									Yd									
	R15	Zd	-									Xd									
	R16	S	-	-	-	-					UYd										
	R17	S	-	-	-	-					DXd										
R18	ACW									RAD											
R19	XY	QF1	QF0					STOP													
SOURCE POINTER	R20	Bs									Ys										
	R21	Zs									Xs										
	R22	S									DYs										
	R23	U									DXs										

\* Don't care  
 - Used or not, according to the command

E88TS68483-37

## 7.2. COMMAND TABLE

TYPE			MNEM	CODE					PARAMETERS					ARGUMENTS							POINTERS							END COMMAND		EXECUTION TIME		
				7	6	5	4	3	2	1	0	RO	R1	R2	R3	R13	R18	R19	R14	R15	R16	R17	R20	R21	R22	R23	CURSOR POSITION	INIT	LOOP	Per		
DRAWINGS	LINEAR	DOT LINE	DLI	0	0	0	0	0	DMU	SP	SRU	X	X	X	X	X			X	X	X	X					Xd+DXd	Yd+DYd	5T	4T	DOT	
		PEN LINE	PLI	0	0	0	POL	PEN	DMU	SP	SRU	X	X	X	X	X			X	X	X	X	X	X	X	X	Xd+DXd	Yd+DYd	5T	CELL+4T	CELL	
		DOT ARC	DAR	0	0	1	0	0	DMU	SP	SRU	X	X	X	X	X	X	X	X	X	X	X					XF	YF	15T	10T	DOT	
		PEN ARC	PAR	0	0	1	POL	PEN	DMU	SP	SRU	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	XF	YF	15T	CELL+10T	CELL	
	AREA	RECTANGLE	REC	1	1	1	1	0	DMU	SP	SRU	X	X	X	X			X	X	X	X					Xd	Yd+DYd	10T	4T	AREA MEMORY WORD		
		TRAPEZIUM	TRA	0	1	0	1	0	DMU	SP	SRU	X	X	X	X			X	X	X	X	X			Xd+DXd	Yd+DYd	10T	10T				
		POLYGON	FLL	0	1	0	0	BEG	DMU	SP	SRU	X	X	X	X			X	X	X	X					Xd+DXd	Yd+DYd	10T	4T (NOTE 1)			
		POLYARC	FLA	0	1	1	0	BEG	DMU	SP	SRU	X	X	X	X	X	X	X	X	X	X					XF	YF	15T	15T			
	CELL	PRINT CHARACTER	PCA	1	0	1	1	REP	DMU	SP	SRU	X	X	X	X			X	X	X	X	X	X	X	X	Xd+DXd	Yd	4T	6T	MEMORY WORD		
		PRINT OBJECT	PVS	1	0	0	SMU	REP	DMU	1	SRU	X	X		X			X	X	X	X	X	X	X	X	Xd+DXd	Yd					
		PVF	1	0	1	0	REP	DMU	1	SRU	X	X		X			X	X	X	X	X	X	X	X	Xd+DXd	Yd						
ACCESS	LOAD VIEWPORT	LDV	1	1	1	0	XFT	0	0	INC								X	X	X	X	X	X	X	X	Xs	Ys	2T	5T	MEMORY WORD		
	SAVE VIEWPORT	SAV	1	1	1	0	XFT	0	1	INC								X	X	X	X	X	X	X	X	Xs	Ys	2T	4T			
	MODIFY VIEWPORT	RMV	1	1	1	0	XFT	1	0	INC								X	X	X	X	X	X	X	X	Xs	Ys	2T	10T			
CURSOR	UP-DOWN MOVE	UDM	1	1	0	0	0	1	DWN	SRU				X			X	X	X						Xd	Yd+DYd	3T					
	LEFT-RIGHT MOVE	LRM	1	1	0	1	LEF	0	0	SRU			X				X	X		X					Xd+DXd	Yd	3T					
	DIAGONAL MOVE	CDM	1	1	0	1	LEF	1	DWN	SRU			X				X	X	X	X					Xd+DXd	Yd+DYd	4T					
CONTROL	NO OPERATION	NOP	1	1	0	0	0	0	0																			1T				
	ABORT	BRT	1	1	1	1	1	1	1																			1T				

- DMU = 1 : Destination mask use.  
 SP = 1 : Short pel; long pel when SP=0.  
 SRU = 1 : Short relative register use (R13).  
 PEN = 0 : The pen is a single pel.  
 PEN = 1 : POL=0: the pen is the character cell addressed by the source pointer.  
 POL = 1: the pen is the object associated with a source mask addressed by the source pointer.  
 BEG = 1 : Initiate a polygon or polyarc filling.  
 This parameter should be reset only when the second drawing is not identical to the first one (Ex: first polygon, then polyarc).  
 INC = 0 : The source pointer is not auto-incremented.  
 INC = 1 : XFT = 1: the source pointer is auto-incremented, X direction first.  
 XFT = 0: The source pointer is auto-incremented or auto-decremented, Y direction first.  
 REP = 1 : The cell is stepped and repeated through the destination window.  
 When REP=0, only one cell is printed.  
 SMU = 1 : The source mask is used.  
 DWN = 1 : The cursor is moved down (up if DWN=0).  
 LEF = 1 : The cursor is moved left (right if LEF=0).

NOTE: With PVF command, any pel with color different from 0 has its source mask implicitly set and used. In other words, pels with color value 0 are transparent.  
 - DXd, DYd, and DYs are signed values.  
 - DXs is always positive.  
 - T = memory cycle = 8 CLK clock periods.  
 - For execution time, add to the short pel loop in the table:  
 · 1T if DMU=1  
 · 1T if SMU=1  
 · 2T if long pen are used  
 · 2T if mask printing is required.  
 Command execution is performed only out of the display periods.  
 NOTE 1: for FLL and FLA commands, add 4T and 8T respectively per pel belonging to the boundary.

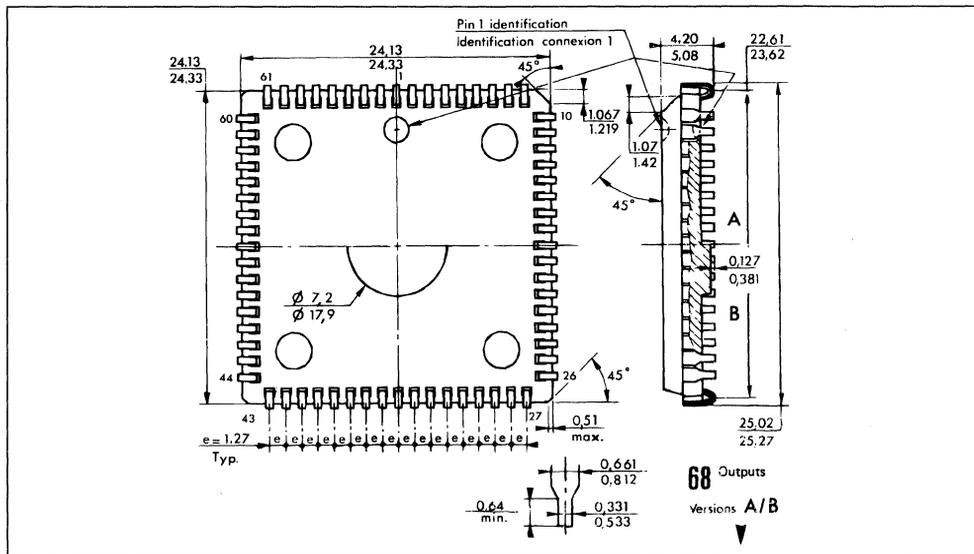
8. ORDERING INFORMATION AND MECHANICAL DATA

8.1. ORDERING INFORMATION

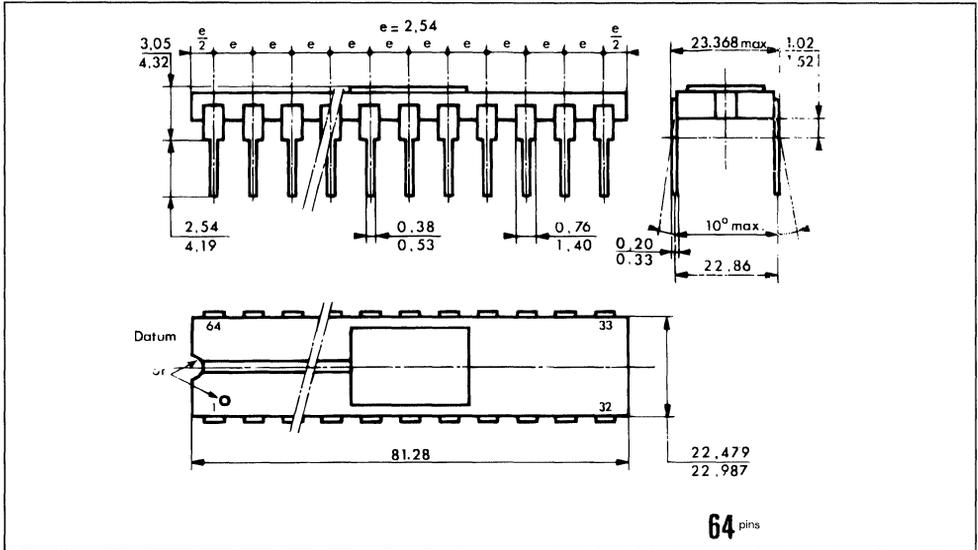
Part Number	Temperature Range	Package	Clock
TS68483CP15	0 °C to + 70 °C	DIP 64	15 MHz
TS68483CP18			18 MHz
TS68483CFN15	0 °C to + 70 °C	PLCC 68	15 MHz
TS68483CFN18			18 MHz

8.2 PACKAGE MECHANICAL DATA

68 PINS – PLASTIC LEADED CHIP CARRIER



64 PINS – PLASTIC DIP



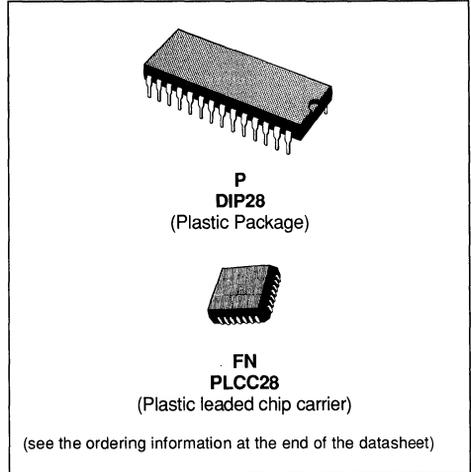


# **COLOR PALETTE**



## HMOS2 - SINGLE CHIP COLOR PALETTE

- ON CHIP COLOR LOOK-UP TABLE
- 4096 COLOR PALETTE (16 colors selected from 4096)
- ON-CHIP THREE 4-BIT RESOLUTION VIDEO DACs WITH  $\gamma$  LAW CORRECTION
- DOT RATE UP TO 30 MEGADOTS PER SECOND
- MARKING BIT FOR INLAY PURPOSE
- VERSATILE MICROPROCESSOR INTERFACE :
  - DIRECTLY COMPATIBLE WITH ADDRESS/DATA MULTIPLEXED 8-BIT MICROPROCESSOR BUS SUCH AS 6801, 8051...
  - DIRECTLY COMPATIBLE WITH NON-MULTIPLEXED 8 OR 16-BIT MICROPROCESSOR BUS (6809, 6502, 68008...).
- SINGLE 5 V SUPPLY
- HMOS 2 TECHNOLOGY

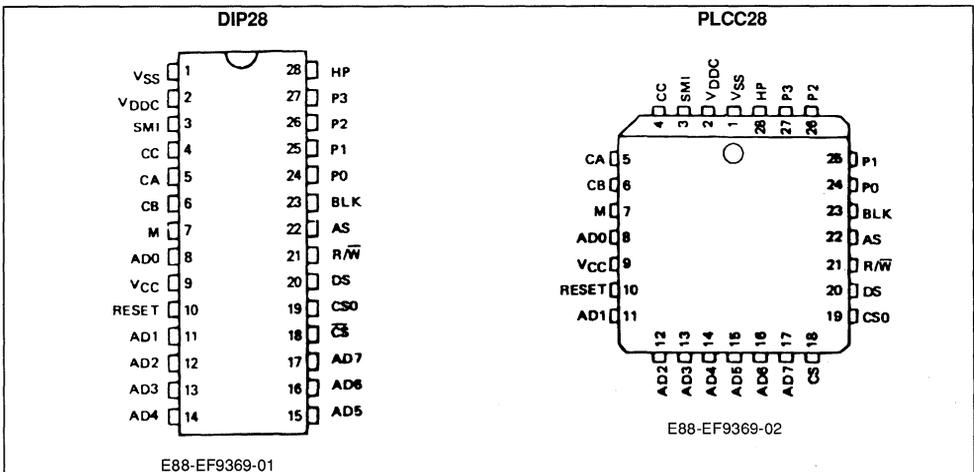


### DESCRIPTION

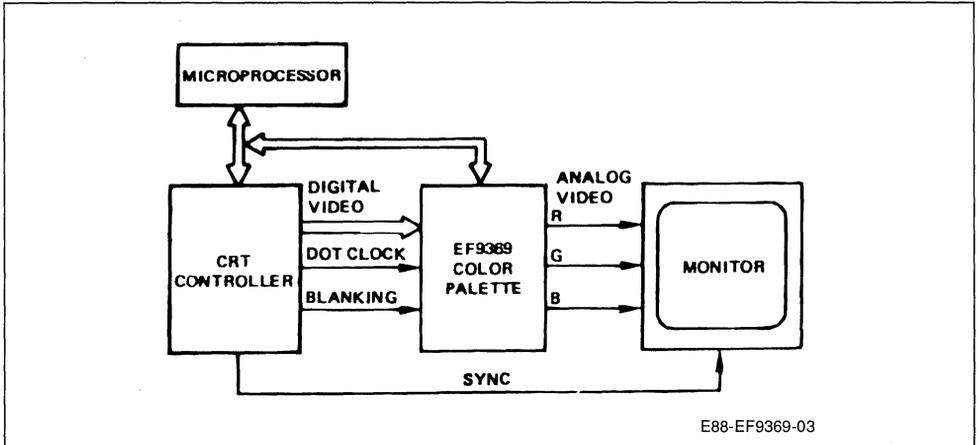
The EF9369 single chip palette provides a low cost, yet remarkable enhancement for any low to mid-range color graphics application. It allows displaying up to 16 different colors, each of these colors being

freely selected out of 4096 preset values. EF9369 contains a 16 register color look-up table, three 4-bit D/A converters and a microprocessor interface for color loading.

### PIN CONNECTIONS



TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub> *	Supply Voltage	- 0.3 to 7.0	V
V <sub>in</sub> *	Input Voltage	- 0.3 to 7.0	V
T <sub>A</sub>	Operating Temperature Range	0 to 70	°C
T <sub>stg</sub>	Storage Temperature Range	- 55 to 150	°C
P <sub>Dm</sub>	Max Power Dissipation	0.45	W

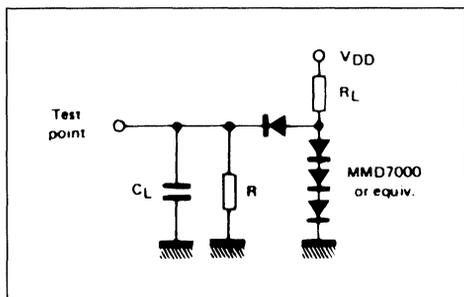
Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

\* With respect to V<sub>SS</sub>.

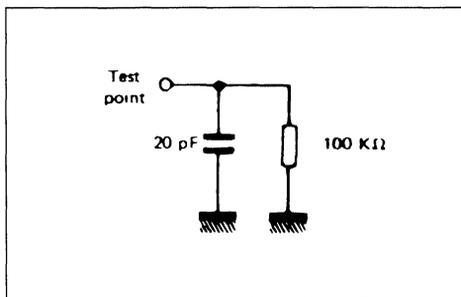
ELECTRICAL OPERATING CHARACTERISTICS (V<sub>CC</sub> = 5.0 ± 5 %, V<sub>SS</sub> = 0, T<sub>A</sub> = 0 to 70 °C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>DDC</sub>	Analog Supply Voltage	-	V <sub>CC</sub>	TBD	V
I <sub>DDC</sub>	Analog Supply Current	-	20	-	mA
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	V
V <sub>IH</sub>	Input High Voltage	RESET	3	-	V <sub>CC</sub>
		All Other Inputs	2	-	V <sub>CC</sub>
I <sub>in</sub>	Input Leakage Current	-	-	20	µA
V <sub>OH</sub>	Output High Voltage (I <sub>oad</sub> = - 500 µA)	2.4	-	-	V
V <sub>OL</sub>	Output Low Voltage (I <sub>oad</sub> = 1.6 mA)	-	-	0.4	V
P <sub>D</sub>	Power Dissipation	-	250	-	mW
C <sub>in</sub>	Input Capacitance	-	-	15	pF
I <sub>TSI</sub>	Three State (off state) Input Current	-	-	10	µA

## Test Load for Digital Output



## Test Load for Analog Output



	AD (0 : 7)	M
C	100 pF	50 pF
R <sub>L</sub>	1 kΩ	3.3 kΩ
R	4.7 kΩ	4.7 kΩ

## MICROPROCESSOR INTERFACE TIMING AD (0 : 7), AS, DS, R/W, CS, CS0

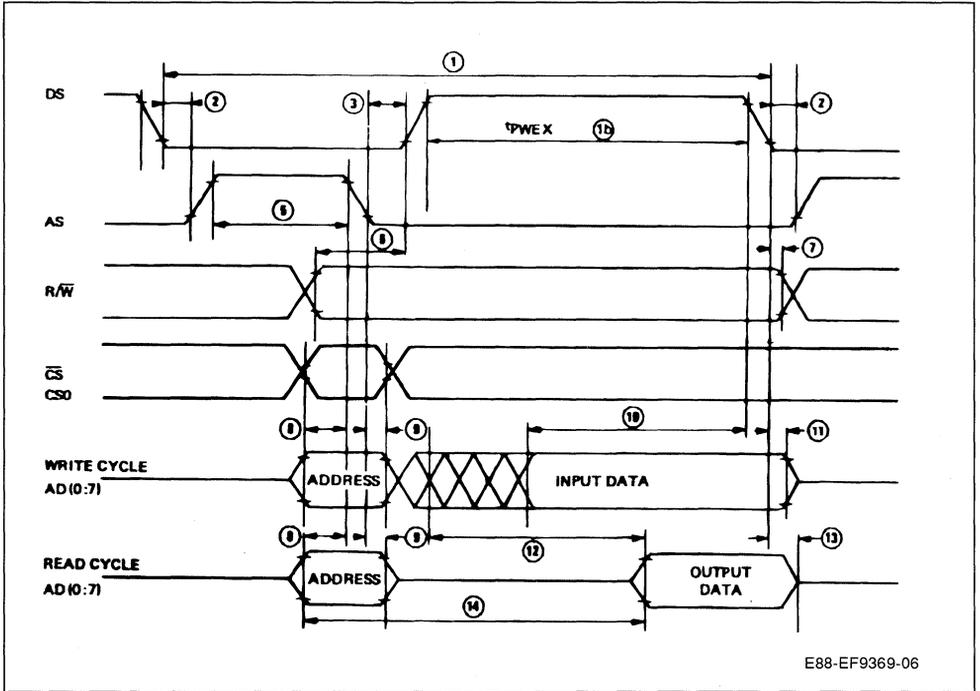
$V_{CC} = 5.0 \pm 5\%$ ,  $T_A = 0\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $C_L = 100\text{ pF}$  on AD (0 : 7)

TTL inputs are 0 to 3 volts, with input rise/fall time  $\leq 3\text{ ns}$ , measured between 10 % and 90 % points.

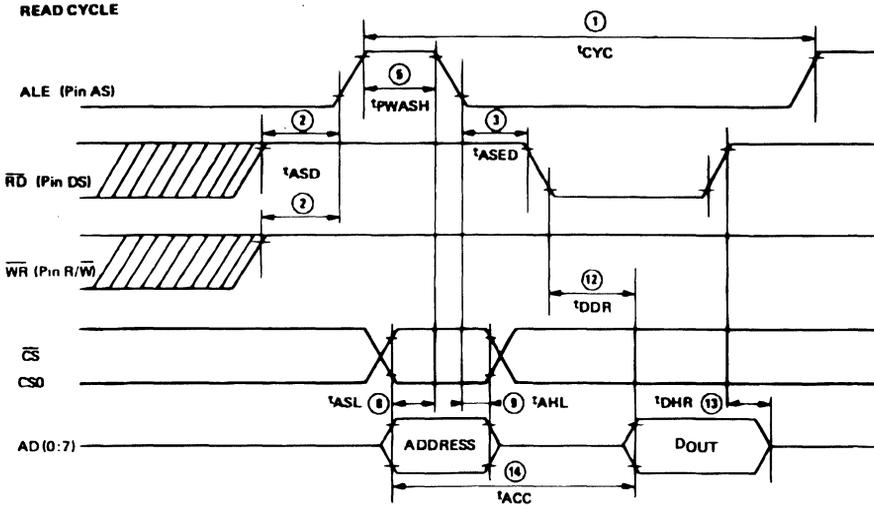
Timing reference at 50 % for inputs and outputs.

Indent. Number	Symbol	Parameter	Min.	Typ.	Max.	Unit
1	$t_{CYC}$	Cycle Time	400	–	–	ns
1b	$t_{PEWX}$	DS Pulse Width High Time	200	–	–	ns
1c	$t_{PEWL}$	DS Pulse Width Low Time (timing 3)	100	–	10000	ns
2	$t_{ASD}$	DS Low to AS High (timing 1) DS High or R/W high to AS high (timing 2)	30	–	–	ns
3	$t_{ASED}$	AS Low to DS High (timing 1) AS Low to DS Low or R/W Low (timing 2)	30	–	–	ns
4	$t_{PWEH}$	Write Pulse Width	200	–	–	ns
5	$t_{PAWSH}$	AS Pulse Width	100	–	–	ns
6	$t_{RWS}$	R/W to DS Setup Time (timing 1)	100	–	–	ns
6b		R/W, AS, CS, CS0 to DS Setup Time (timing 3)	100	–	–	ns
7	$t_{RWH}$	R/W to DS Hold Time (timing 1)	10	–	–	ns
8	$t_{ASL}$	Address and CS, CS0 Set Up Time	20	–	–	ns
9	$t_{AHL}$	Address and CS, CS0 Hold Time	20	–	–	ns
10	$t_{DSW}$	Data Setup Time (write cycle)	100	–	–	ns
11	$t_{DHW}$	Data Hold Time (write cycle)	10	–	–	ns
12	$t_{DDR}$	Data Access Time from DS (read cycle)	–	–	150	ns
13	$t_{DHR}$	DS Inactive to High Impedance State Time (read cycle)	10	–	80	ns
14	$t_{ACC}$	Address to Data Valid Access Time	–	–	300	ns

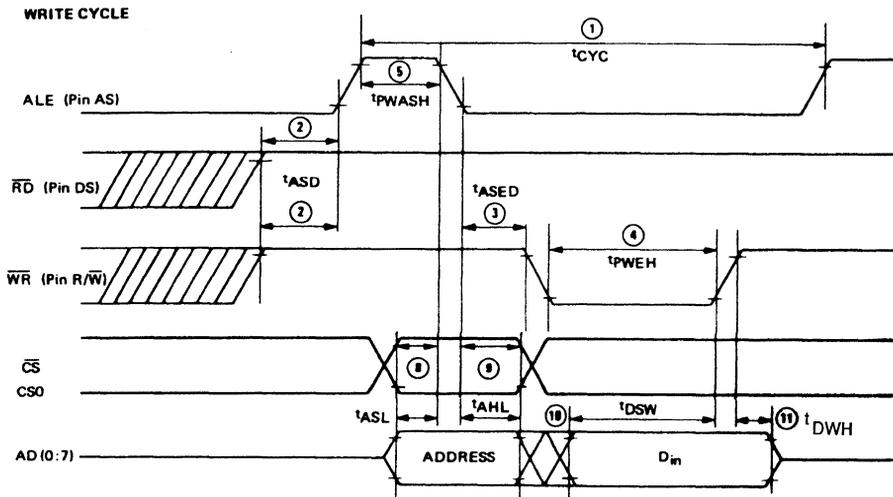
TIMING DIAGRAM 1 - MULTIPLEXED MODE - MOTOROLA TYPE (SMI = V<sub>SS</sub>)



TIMING DIAGRAM 2 - MULTIPLEXED MODE - INTEL TYPE (SMI = V<sub>SS</sub>)

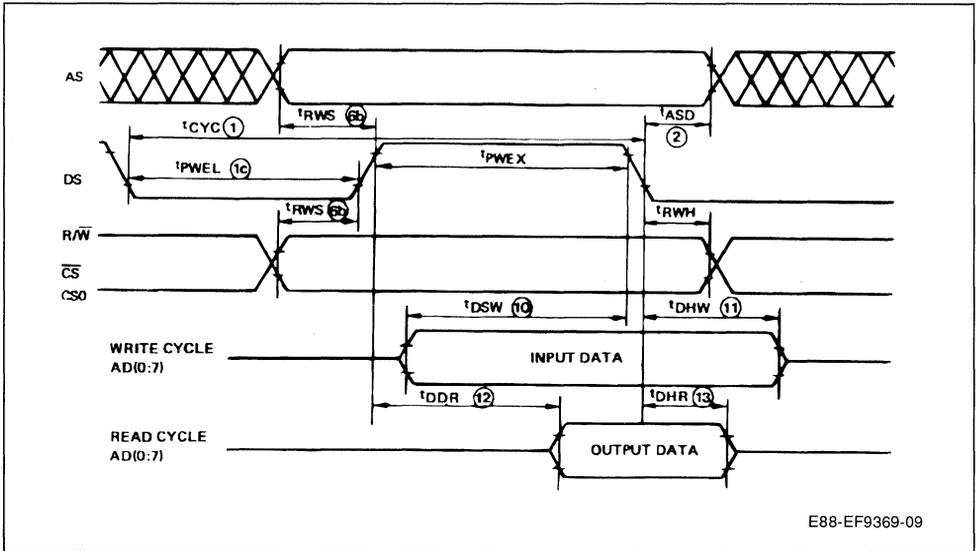


E88-EF9369-07



E88-EF9369-08

**TIMING DIAGRAM 3 - NON-MULTIPLEXED MODE (SMI = V<sub>CC</sub>)**



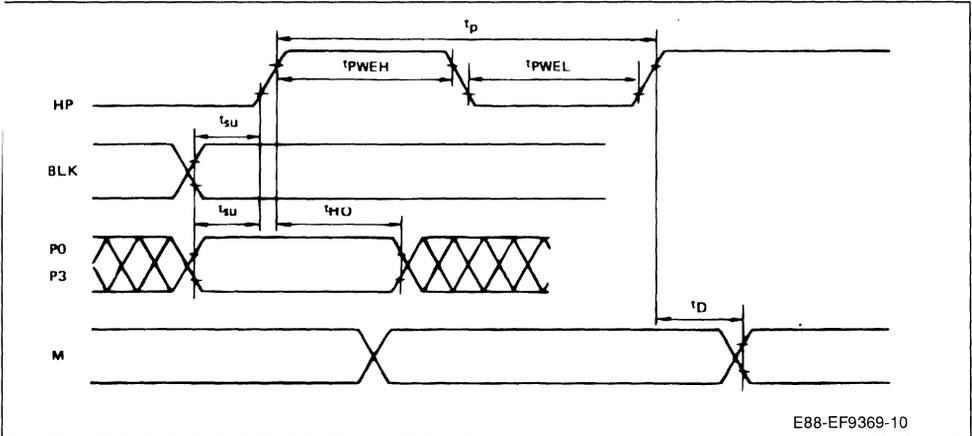
**DIGITAL VIDEO SIGNALS - HP, P(0 : 3), BLK, M, RESET**

V<sub>CC</sub> = 5.0 ± 5 %, T<sub>A</sub> = 0 °C to + 70 °C, C<sub>L</sub> = 50 pF on M.

TTL inputs are 0 to 3 volts, with input rise/fall time ≤ 3 ns, measured between 10 % and 90 % points. Timing reference at 50 % for inputs and outputs.

Symbol	Parameter	EF9369		EF9369-30		Unit
		Min.	Max.	Min.	Max.	
t <sub>P</sub>	HP Clock Period	58	1000	33	1000	ns
t <sub>PEWH</sub>	HP High Pulse Width	25	-	13	-	ns
t <sub>PEWL</sub>	HP Low Pulse Width	25	-	13	-	ns
t <sub>SU</sub>	BLK and P(0 : 3) Set Up Time to HP	5	-	5	-	ns
t <sub>HO</sub>	BLK and P(0 : 3) Hold Time from HP	10	-	10	-	ns
t <sub>D</sub>	M Output Delay from HP	-	45	-	45	ns
t <sub>PWRL</sub>	RESET High Pulse Width	400	-	400	-	ns

**TIMING DIAGRAM 4**



**ANALOG VIDEO OUTPUTS - CA, CB, CC**

V<sub>DCC</sub> > 5 V, T<sub>A</sub> = 0°C to + 70°C, C<sub>L</sub> = 20 pF, R<sub>L</sub> = 100 kΩ

**Table 1.**

Binary Input		Analog Output (V)		
		Min.	Typ.	Max.
Low Level	0000	–	0.8	–
	0001	–	1.18	–
	0010	–	1.28	–
	0011	–	1.36	–
	0100	–	1.42	–
	0101	–	1.47	–
	0110	–	1.52	–
	0111	–	1.56	–
	1000	–	1.60	–
	1001	–	1.63	–
	1010	–	1.66	–
	1011	–	1.69	–
	1100	–	1.72	–
	1101	–	1.75	–
	1110	–	1.78	–
High Level	1111	–	1.80	–

**Note :** The internal A/D converters deliver on CA, CB and CC outputs 16 levels with  $\gamma$  law correction ( $\gamma = 2.8$ ). The typical transfer characteristic is given by :

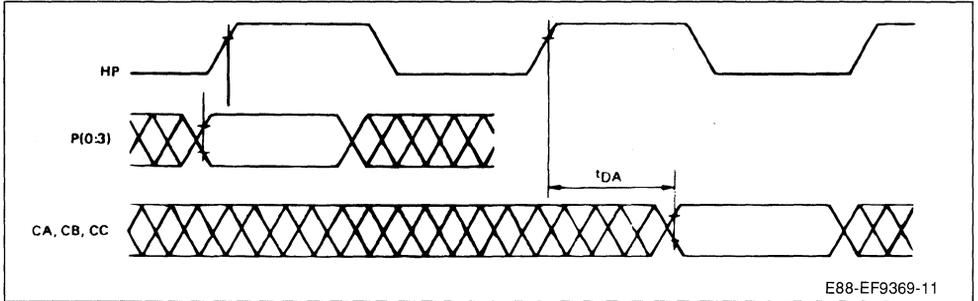
$$V = \left( \frac{N}{15} \right)^{2.8} \cdot \frac{V_{DCC}}{5} + 0.16 V_{DCC}$$

Where N is the binary input value.

The typical analog video output impedance is 300 Ω for EF9369-30 and 400 Ω for EF9369.

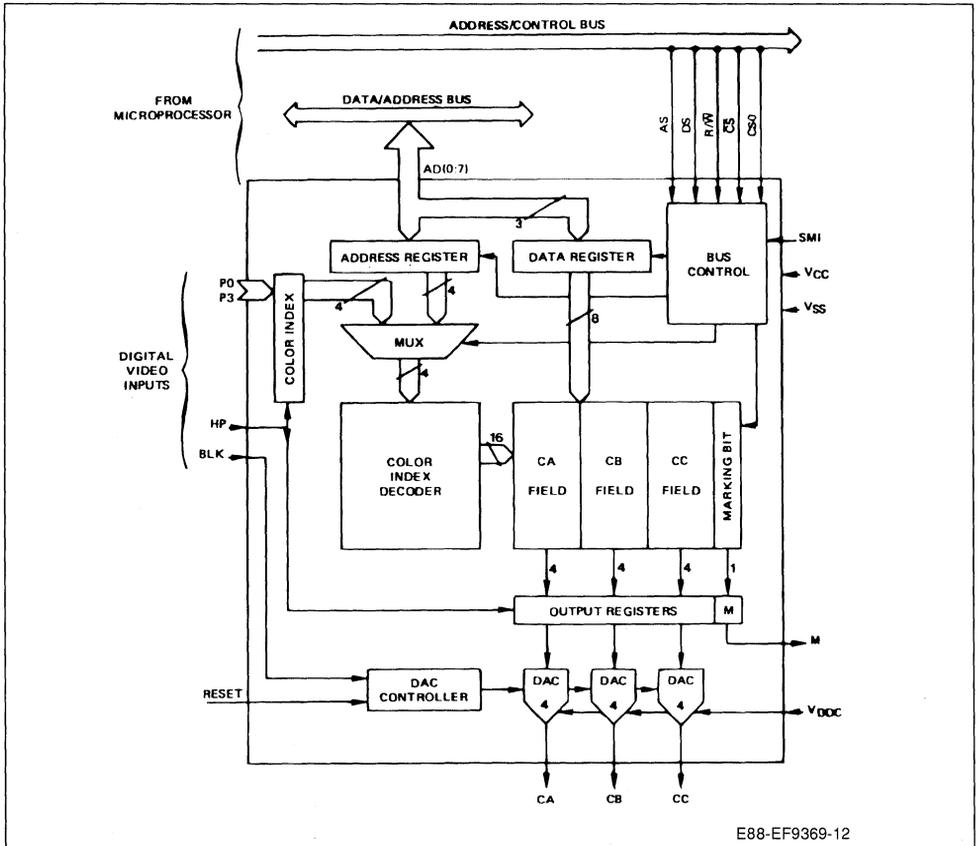
Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{DA}$	CA, CB, CC Outputs from HP	-	80	-	ns

TIMING DIAGRAM 5



E88-EF9369-11

BLOCK DIAGRAM



E88-EF9369-12

## PIN DESCRIPTION

## MICROPROCESSOR INTERFACE

All the input/output pins are TTL compatible.

Name	Pin Type	N°	Function	Description
AD(0:7)	I/O	8-11-14 15-17	Multiplexed Address/data Bus	These 8 bidirectional pins are to be connected to the microprocessor system bus.
SMI	I	3	Interface Mode Select	When this input is connected to V <sub>CC</sub> , the EF9369 is in the non multiplexed mode. When this input is connected to V <sub>SS</sub> (ground), the EF9369 is in a multiplexed mode to provide a direct interface with either Motorola or Intel Type Microprocessor.
AS	I	22	Address Strobe	In non-multiplexed mode, this input selects either the address register (AS = 1) or the data register (AS = 0) to be accessed. In multiplexed mode, the falling edge of this control signal latches on the AD(0:7) lines, the state of the Data Strobe (DS) and Chip Select lines (CS, CS0). When using Intel type microprocessor, this input must be connected to the ALE control line.
DS	I	20	Data Strobe	In non multiplexed mode, this active high control signal enables the AD(0:7) input/output buffers and strobes data to/from the EF9369. This signal is usually derived from the processor E (Ø2) clock. In multiplexed mode, the input is strobed by the falling edge of AS. The strobe value selects either Motorola or Intel type. When using an Intel type microprocessor, DS must be connected to the RD control line. With a Motorola type microprocessor, DS must be connected to E(Ø2) clock.
R/W	I	21	Read/write	This control signal determines whether the EF9369 is read (R/W = 1) or written (R/W = 0). When using Intel type microprocessor, this input must be connected to the WR control line.
CS CS0	I	18 19	Chip Select	CS must be low and CS0 must be high to select the EF9369. In non multiplexed mode, the EF9369 remains selected as long as the selection condition is met. In multiplexed mode, the selection condition is latched when AS is low.

## OTHER PINS

Name	Pin Type	N°	Function	Description
V <sub>CC</sub>	S	9	Power Supply	+ 5 V
V <sub>DDC</sub>	S	2	Analog Power Supply	Power supply for the internal DACs. This input can be connected to V <sub>CC</sub> .
V <sub>SS</sub>	S	1	Power Supply	Ground

VIDEO INTERFACE

Name	Pin Type	N°	Function	Description
P(0:3)	I	24-27	Pixel Inputs	These four TTL compatible inputs are strobed by HP into the color index register to address the color look-up table.
HP	I	28	Dot Clock	The rising edge of this input latches the P(0:3) and BLK inputs into the EF9369 and the data out of color look-up table into the output registers.
M	O	7	Marking	This output is synchronised by HP and delivers the marking bit value from the color look-up table.
CA CB CC	O	5 6 4	Color Outputs	These three analog high impedance outputs deliver the color signal levels from the internal D/A converters (DAC). The delay between CA, CB, CC outputs and the latched value P(0:3) is one HP clock period plus tDA (see timing diagram 5).
BLK	I	23	Blanking	A high level on this input forces the CA, CB, CC and M outputs to low level.
RESET	I	10	Reset	This active high input forces the CA, CB, CC, outputs to low level until the next microprocessor access to the device.

FUNCTIONAL DESCRIPTION

EF9369 contains a 16 register Color-Look Up Table (CLUT). Each of these 13-bit register holds three 4-bit color fields CA (0:3), CB (0:3) and CC (0:3) and a marking bit M.

These registers can be accessed (read or write) by the microprocessor through the microprocessor interface. These registers are also read by the video process : a 4-bit pixel value and a clock must be provided at pixel rate to the P (0:3) and HP input pins. These signals may be delivered either by 4 video shift registers and the shifting clock of a bit map CRT controller or by an alphanumeric or semigraphic CRT controller. The pixel value, after clock resynchronization, is used as a color index : it selects one out of the 16 CLUT registers. Each color field of the selected register is converted to an analog signal and delivered to one of the CA, CB or CC output. The marking bit is directly routed to the M output. When the CA, CB and CC outputs are used as RGB analog signals, one color out of 4096 is associated to each pixel value. In short this process freely maps a 16 color index set into a 4096 color set.

MICROPROCESSOR INTERFACE.

The 8-bit microprocessor interface gives access (read or write) to the CLUT which is addressed as a 32 byte table. The 13-bit color register # N (N = 0 to 15) is accessed at address 2N and 2N + 1. Even address holds CA (0:3) and CB (0:3), odd address holds CC (0:3) and M (see fig. 1).

EF9369 provides two bus modes through the SMI programming pin :

- Multiplexed mode for address/data multiplexed 8 bit microprocessor bus.
- Non-multiplexed mode for non-multiplexed 8 or 16-bit microprocessor bus.

MULTIPLEXED MODE (SMI connected to V<sub>SS</sub>).

In this mode, EF9369 can be directly connected to popular address/data multiplexed microprocessor, either Motorola type (6801...) or Intel type (8048, 8051, 8088...). In this last case the EF9369 AS, DS and R/W inputs must be connected respectively to the ALE, RD and WR microprocessor control lines.

In this mode, EF9369 maps into the microprocessor addressing space as 32 CLUT byte address. Random access to one byte takes one cycle : on the falling edge of the AS input, EF9369 latches AD (0:7) into the on-chip address register, the DS and chip select lines into dedicated flip-flops. The strobed value of DS allows recognition of Intel or Motorola type for further processing. (See pin description section and microprocessor timing diagrams for details). When the EF9369 chip select lines enable selection, the addressed byte is accessed during the data phase of the cycle.

NON MULTIPLEXED MODE (SMI connected to V<sub>CC</sub>).

In this mode EF9369 can be directly connected to any 8 or 16-bit, non multiplexed, microprocessor bus (6800, 6809, 6502, 68008...).

This mode provides an indirect, auto-incremented addressing scheme. EF9369 maps into the micro-

Figure 1 : Clut Addressing

Color Look-up Table (CLUT)								CLUT Byte Address								Register Index #
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	X	X	X	0	0	0	0	0	0
X	X	X	M	CC3	CC2	CC1	CC0	X	X	X	0	0	0	0	1	
CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	X	X	X	0	0	0	1	0	1
X	X	X	M	CC3	CC2	CC1	CC0	X	X	X	0	0	0	1	1	
CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	X	X	X	1	1	1	1	0	15
X	X	X	M	CC3	CC2	CC1	CC0	X	X	X	1	1	1	1	1	

X = Don't Care.

processor addressing space as 2 byte address only. AS is used to select one out of 2 registers :

- the write only address (5 bits) addressed when AS = 1.
- the read/write data register (8 bits) addressed when AS = 0.

Random access to a CLUT byte takes two bus cycles :

1/ Load the CLUT address into the address register.

2/ Access (read or write) the value in the data register.

After each access to the data register, the address register is automatically incremented modulo 32. This scheme allows sequential addressing to the CLUT without address reloading, the complete CLUT can so be reloaded in 33 bus cycles.

#### VIDEO PROCESS.

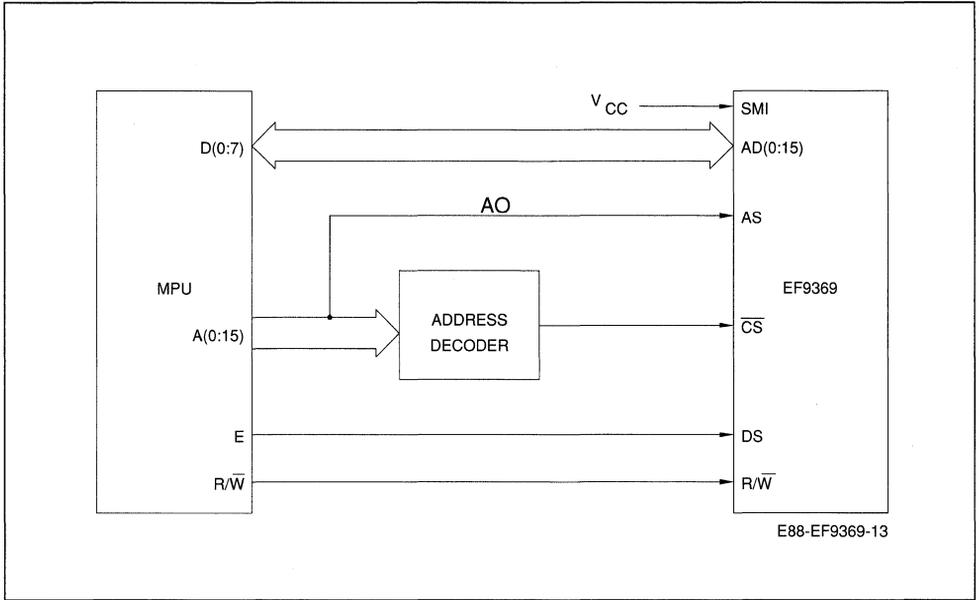
The CRT controller sends to EF9369 a pixel value on pins P (0:3), a pixel rate clock on HP input and a blanking signal on pin BLK. The pixel value is latched into the color index register by the rising edge of HP. The color index register selects one register in the CLUT. The color fields of the selected register are routed to 3 DACs and M is directly routed to the M digital output.

After impedance matching, the CA, CB, and CC outputs can be used to drive a RGB analog color monitor. Alternatively one of these outputs can be used to drive a monochrome monitor thus providing up to 16 grey levels. The marking digital output can be used to drive analog video switches, thus providing video overlay facility on a color per color basis.

The blanking input forces the analog outputs and the M output to low level thus allowing the beam to be switched off during retrace intervals.

- Notes :**
1. Each 4 bit-D/A converter is  $\gamma$  corrected in order to linearize the luminance driven on the screen versus the digital value. The typical digital to voltage conversion law is given table 1. The output voltages are proportional to the analog supply voltage  $V_{DDC}$ . When required, setting  $V_{DCC}$  allows a gain adjustment. But in most applications,  $V_{DDC}$  and  $V_{DD}$  can be derived from the same supply through independent decoupling.
  2. CA, CB and CC are high impedance outputs (500  $\Omega$  typical) which require proper adaptation in most applications. SGS-THOMSON TEA5114 provides such a 1 V - 75  $\Omega$  low cost adaptation (See fig. 2).
  3. As the CLUT is shared between microprocessor access and video access, a low level is forced on the CA, CB, CC and M outputs during any chip select periods. To avoid to spoil the screen with black strokes it is recommended to access the CLUT from the microprocessor only during the retrace periods.
  4. RESET - This input forces CA, CB, CC and M outputs to a low level until the next microprocessor access. At power on or at the beginning of a session RESET allows to keep a clean black screen proper initialization.

NON-MULTIPLEXED BUS INTERFACE



MULTIPLEXED BUS INTERFACE

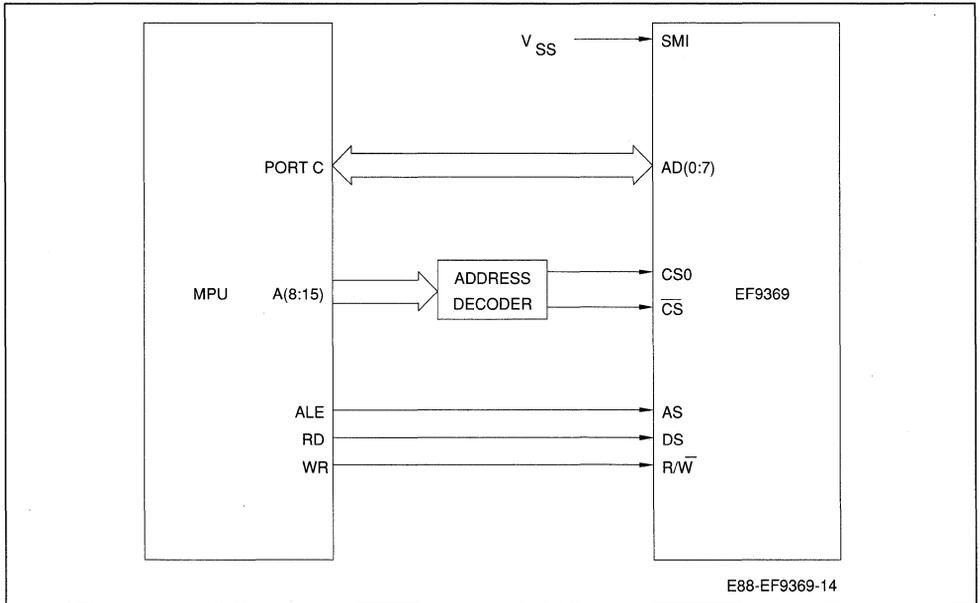
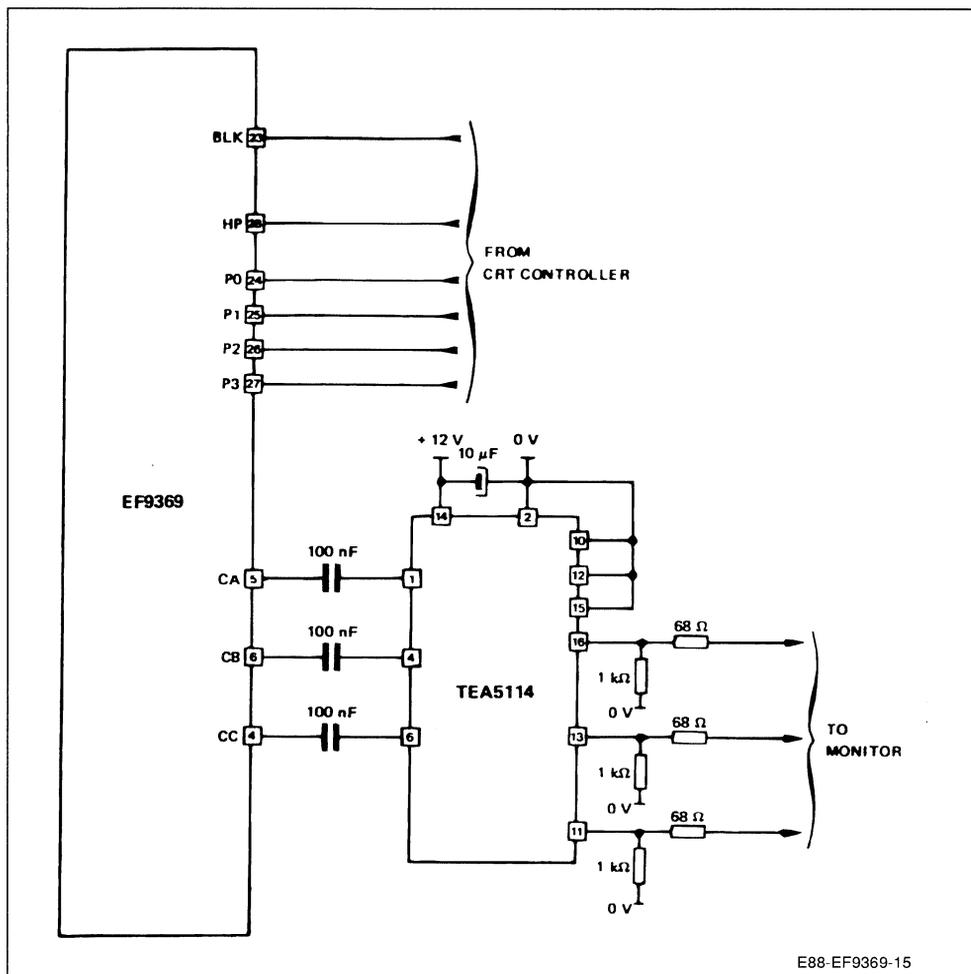


Figure 2 : Typical 1 V - 75  $\Omega$  Video Interface

E88-EF9369-15

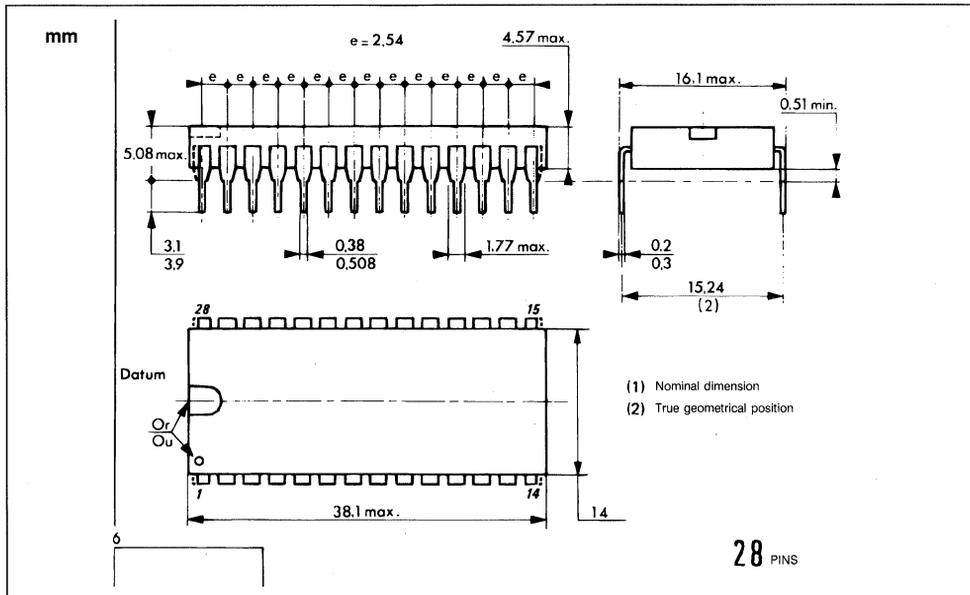
**Note :** Each digital or analog ground must be separately connected to EF9369 pin 1.

ORDERING INFORMATION

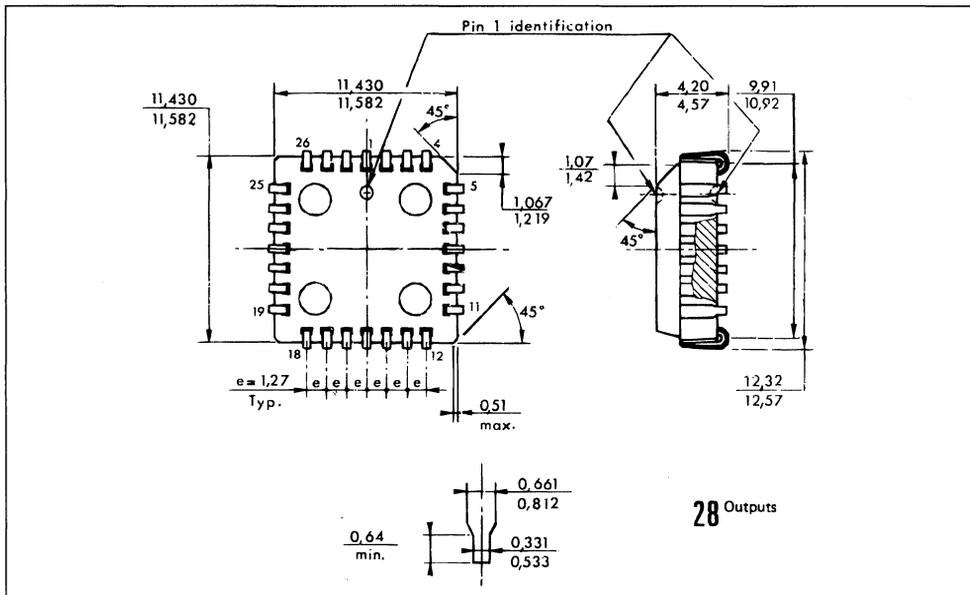
Part Number	Temperature	Package
EF9369P	0 to 70 °C	DIP28
EF9369P30	0 to 70 °C	DIP28
EF9369FN	0 to 70 °C	PLCC28

PACKAGE MECHANICAL DATA

28 PINS - PLASTIC DIP



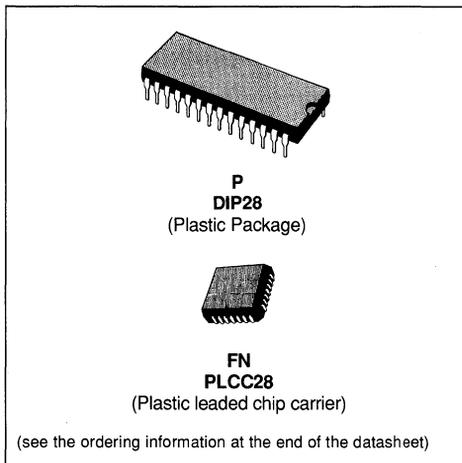
28 PINS - PLASTIC LEADED CHIP CARRIER





## HMOS2 - SINGLE CHIP COLOR PALETTE

- ON CHIP COLOR LOOK-UP TABLE
- 4096 COLOR PALETTE (16 colors selected from 4096)
- ON-CHIP THREE 4-BIT RESOLUTION VIDEO DACs
- DOT RATE UP TO 45 MEGADOTS PER SECOND
- MARKING BIT FOR INLAY PURPOSE
- VERSATILE MICROPROCESSOR INTERFACE :
  - DIRECTLY COMPATIBLE WITH ADDRESS/DATA MULTIPLEXED 8-BIT MICROPROCESSOR BUS SUCH AS 6801, 8051...
  - DIRECTLY COMPATIBLE WITH NON-MULTIPLEXED 8 OR 16-BIT MICROPROCESSOR BUS (6809, 6502, 68008...)
- SINGLE 5 V SUPPLY
- LOW POWER DISSIPATION
- 28 PINS DIP AND PLCC PACKAGE

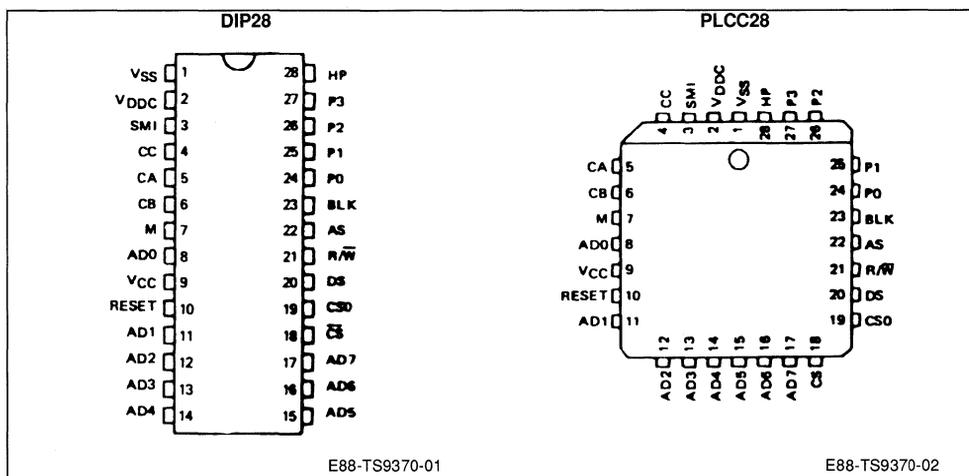


### DESCRIPTION

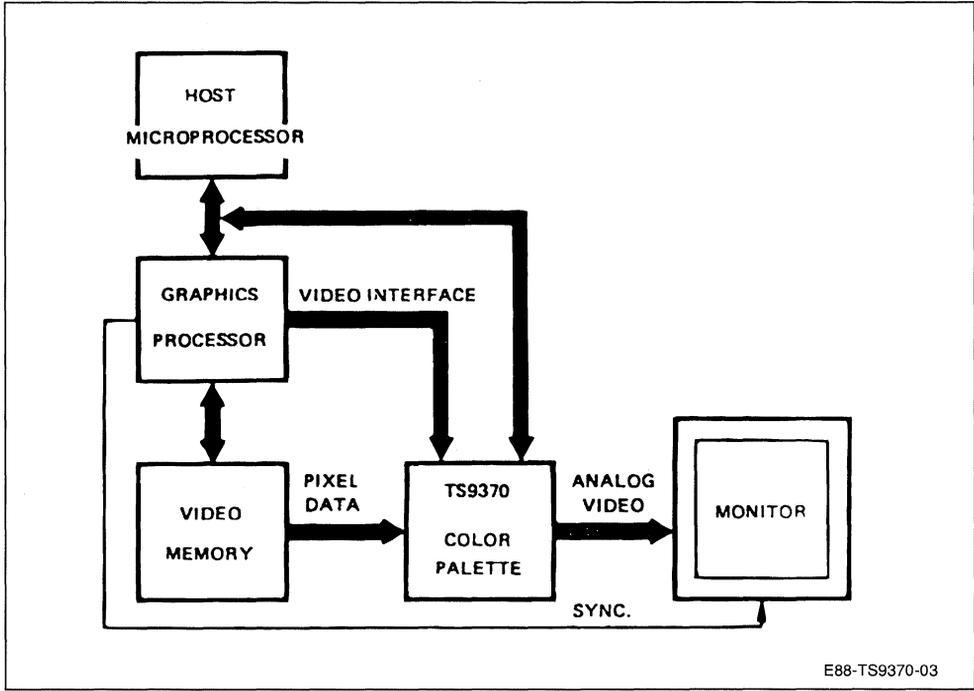
The TS9370 single chip palette provides a low cost, yet remarkable enhancement for any low to mid-range color graphics application. It allows displaying

up to 16 different colors, each of three colors being freely selected out of 4096 preset values. TS9370 contains a 16 register color look-up table, three 4-bit D/A converters and a microprocessor interface for color loading.

### PIN CONNECTIONS

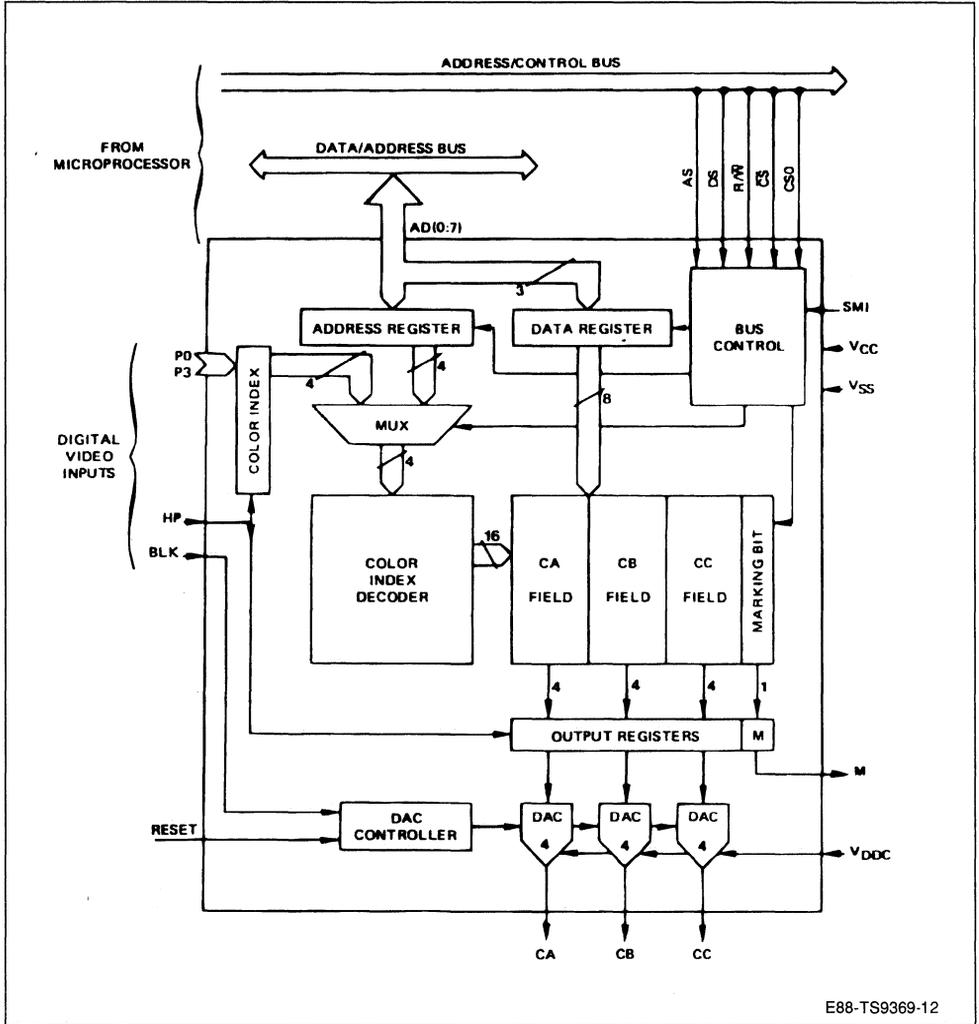


TYPICAL APPLICATION



E88-TS9370-03

BLOCK DIAGRAM



E88-TS9369-12

**PIN DESCRIPTION**

**MICROPROCESSOR INTERFACE**

All the input/output pins are TTL compatible.

Name	Pin Type	N°	Function	Description
AD(0:7)	I/O	8-11-14 15-17	Multiplexed Address/data Bus	These 8 bidirectional pins are to be connected to the microprocessor system bus.
SMI	I	3	Microprocessor Interface Mode Select	When this input is connected to V <sub>CC</sub> , the TS9370 is in the non multiplexed mode. When this input is connected to V <sub>SS</sub> (ground), the EF9370 is in a multiplexed mode to provide a direct interface with either Motorola or Intel Type Microprocessor.
AS	I	22	Address Strobe	In non-multiplexed mode, this input selects either the address register (AS = 1) or the data register (AS = 0) to be accessed. In multiplexed mode, the falling edge of this control signal latches the address on the AD(0:7) lines, the state of the Data Strobe (DS) and Chip Select lines (CS, CSO). When using Intel type microprocessor, this input must be connected to the ALE control line.
DS	I	20	Data Strobe	In non multiplexed mode, this active high control signal enables the AD(0:7) input/output buffers and strobes data to/from the TS9370. This signal is usually derived from the processor E (Ø2) clock. In multiplexed mode, the input is strobed by the falling edge of AS. The strobe value selects either Motorola or Intel type. When using an Intel type microprocessor, DS must be connected to the RD control line. With a Motorola type microprocessor, DS must be connected to E(Ø2) clock.
R/W	I	21	Read/write	This control signal determines whether the TS9370 is read (R/W = 1 ) or written (R/W = 0). When using Intel type microprocessor, this input must be connected to the WR control line.
CS CSO	I	18 19	Chip Select	CS must be low and CSO must be high to select the TS9370. In non multiplexed mode, the TS9370 remains selected as long as the selection condition is met. In multiplexed mode, the selection condition is latched when AS is low.

## VIDEO INTERFACE

Name	Pin Type	N°	Function	Description
P(0:3)	I	24-27	Pixel Inputs	These four TTL compatible inputs are strobed by HP into the color index register to address the color look-up table.
HP	I	28	Dot Clock	The rising edge of this input latches the P(0:3) and BLK inputs into the TS9370 and the data out of color look-up table into the output registers.
M	O	7	Marking	This output is synchronised by HP and delivers the marking bit value from the color look-up table. The logical delay between M output and the latched value P(0:3) is one HP clock period.
CA CB CC	O	5 6 4	Color Outputs	These three analog outputs deliver the color signal levels from the internal D/A converters (DAC). The delay between CA, CB, CC outputs and the latched value P(0:3) is one HP clock period (see timing diagram 5).
BLK	I	23	Blanking	A high level on this input forces the CA, CB, CC and M outputs to low level.
RESET	I	10	Reset	This active high input forces the CA, CB, CC, outputs to low level until the next microprocessor access to the device.

## OTHER PINS

Name	Pin Type	N°	Function	Description
V <sub>CC</sub>	S	9	Power Supply	+ 5 V
V <sub>DDC</sub>	S	2	Analog Power Supply	Power supply for the internal DACs. This input can be connected to V <sub>CC</sub> .
V <sub>SS</sub>	S	1	Power Supply	Ground

## FUNCTIONAL DESCRIPTION

TS9370 contains a 16 register Color-Look Up Table (CLUT). Each of these 13-bit register holds three 4-bit color fields CA (0:3), CB (0:3) and CC (0:3) and a marking bit M.

These registers can be accessed (read or write) by the microprocessor through the microprocessor interface. These registers are also read by the video process : a 4-bit pixel data and a clock must be provided at pixel rate to the P(0:3) and HP input pins. These signals may be delivered either by 4 video shift registers and the shifting clock of a bit map CRT controller or by an alphanumeric or semi-graphic CRT controller. The pixel value, after clock resynchronisation, is used as a color index : it selects one out of the 16 CLUT registers. Each color field of the selected register is converted to an analog signal and delivered to one of the CA, CB or CC output. The marking bit is directly routed to the M output. When the CA, CB and CC outputs are used as RGB analog signals, one color out of 4096 is associated to each pixel value. In short this process freely maps a 16 color index set into a 4096 color set.

## MICROPROCESSOR INTERFACE

The 8-bit microprocessor interface gives access (read or write) to the CLUT which is addressed as a 32 byte table. The 13-bit color register # N (N = 0 to 15) is accessed at address 2N and 2N + 1. Even address holds CA (0:3) and CB (0:3), odd address holds CC (0:3) and M (see fig. 1).

TS9370 provides two bus modes through the SMI programming pin :

- Multiplexed mode for address/data multiplexed 8-bit microprocessor bus.
- Non-multiplexed mode for non-multiplexed 8 or 16 bit microprocessor bus.

MULTIPLEXED MODE (SMI connected to V<sub>SS</sub>)

In this mode, TS9370 can be directly connected to popular address/data multiplexed microprocessor, either Motorola type (6801) or Intel type (8048, 8051, 8088...). In this last case the TS9370 AS, DS and R/W inputs must be connected respectively to the ALE, RD and WR microprocessor control lines.

Figure 1 : Clut Addressing.

Color Look-up Table (CLUT)								CLUT Byte Address								Register Index
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	#
CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	X	X	X	0	0	0	0	0	0
X	X	X	M	CC3	CC2	CC1	CC0	X	X	X	0	0	0	0	1	
CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	X	X	X	0	0	0	1	0	1
X	X	X	M	CC3	CC2	CC1	CC0	X	X	X	0	0	0	1	1	
CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	X	X	X	1	1	1	1	0	15
X	X	X	M	CC3	CC2	CC1	CC0	X	X	X	1	1	1	1	1	

X = Don't Care.

In this mode, TS9370 maps into the microprocessor addressing space as 32 CLUT byte address. Random access to one byte takes one cycle : on the falling edge of the AS input, TS9370 latches AD (0:7) into the on-chip address register, the DS and chip select lines into dedicated flip-flops. The strobed value of DS allows recognition of Intel or Motorola type for further processing. (See pin description section and microprocessor timing diagrams for details). When TS9370 chip select lines enable selection, the addressed byte is accessed during the data phase of the cycle.

**NON MULTIPLEXED MODE**  
(SMI connected to Vcc)

In this mode TS9370 can be directly connected to any 8 or 16-bit, non-multiplexed, microprocessor bus (6800, 6809, 6502, 68008...).

This mode provides an indirect, auto-incremented addressing scheme. TS9370 maps into the microprocessor addressing space as 2 byte address only. AS is used to select one out of 2 registers :

- the write only address register (5 bits) addressed when AS = 1.
- the read/write data register (8 bits) addressed when AS = 0.

Random access to a CLUT byte takes two bus cycles :  
1/ Load the CLUT address into the address register.  
2/ Access (read or write) the value in the data register.

After each access to the data register, the address register is automatically incremented modulo 32. This scheme allows sequential addressing to the CLUT without address reloading, the complete CLUT can so be reloaded in 33 bus cycles.

**VIDEO PROCESS**

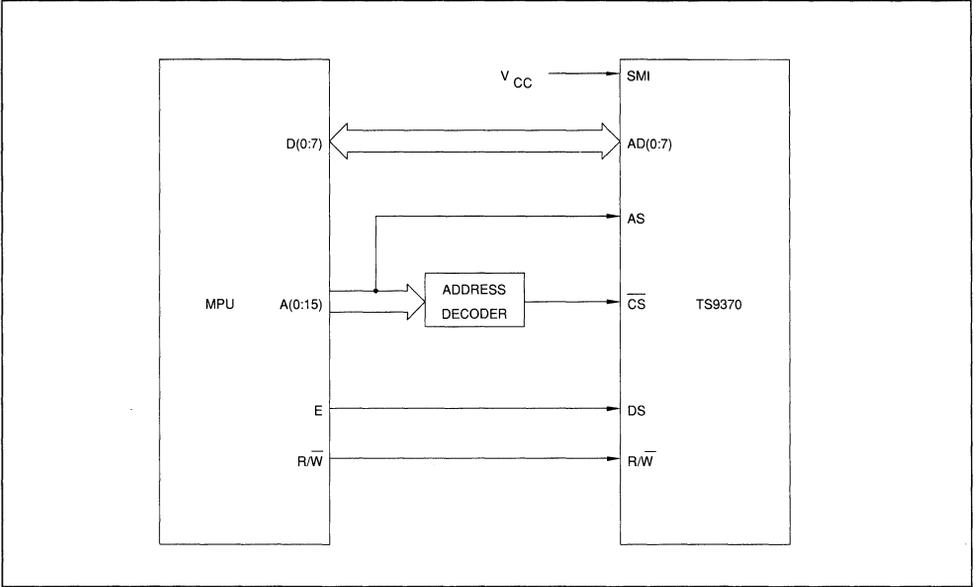
The CRT controller sends to TS9370 a pixel value

on pins P (0:3), a pixel rate clock on HP input and a blanking signal on pin BLK. The pixel value is latched into the color index register by the rising edge of HP. The color index register selects one register in the CLUT. The color fields of the selected register are routed to 3 DACs and M is directly routed to the M digital output. After impedance matching, the CA, CB, and CC outputs can be used to drive a RGB analog color monitor. Alternatively one of these outputs can be used to drive a monochrome monitor thus providing up to 16 grey levels. The marking digital output can be used to drive analog video switches, thus providing video overlay facility on a color per color basis.

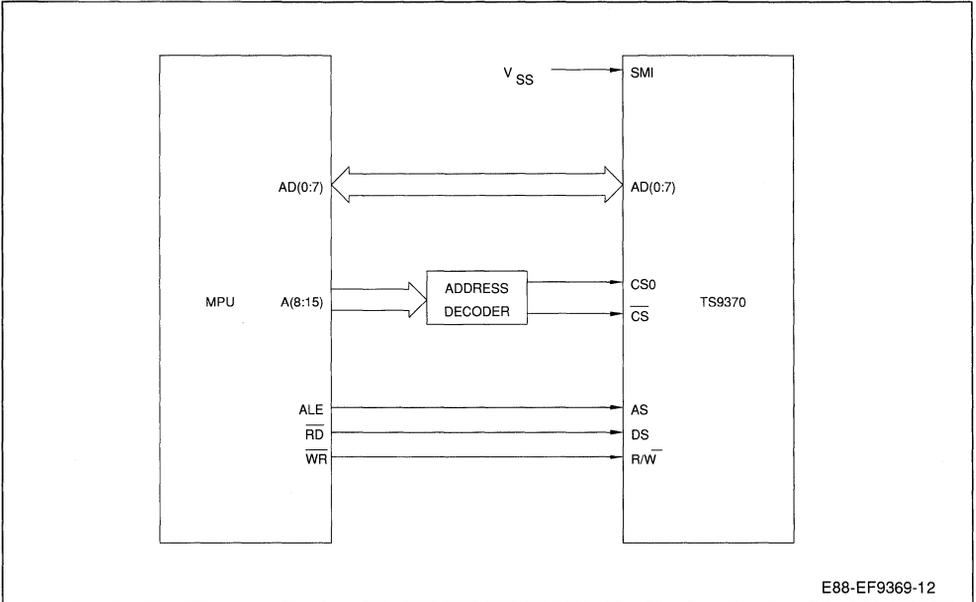
The blanking input forces the analog outputs and the M output to low level thus allowing the beam to be switched off during retrace intervals.

- Notes :**
- 1.The output voltages are proportionnal to the analog supply voltage V<sub>DDC</sub>. When required, setting V<sub>DDC</sub> allows a gain adjustment. But in most applications, V<sub>DDC</sub> and V<sub>DD</sub> can be derived from the same supply through independent decoupling.
  - 2.As the CLUT is shared between microprocessor access and video access, a low level is forced on the CA, CB, CC and M outputs during any chip select periods. To avoid to spoil the screen with black strokes it is recommended to access the CLUT from the microprocessor only during the retrace periods.
  - 3.RESET - This input forces CA, CB, CC and M outputs to a low level until the next microprocessor access. At power on or at the beginning of a session RESET allows to keep a clean black screen until proper initialization.

NON MULTIPLEXED MODE



MULTIPLEXED MODE - INTEL TYPE



E88-EF9369-12

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub> *	Digital Power Supply	- 0.3 to 7.0	V
V <sub>in</sub> *	Input Voltage	- 0.3 to 7.0	V
T <sub>A</sub>	Operating Temperature Range	0 to 70	°C
T <sub>stg</sub>	Storage Temperature Range	- 55 to 150	°C
V <sub>DDC</sub> *	Analog Power Supply	- 0.3 to 9.0	V

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

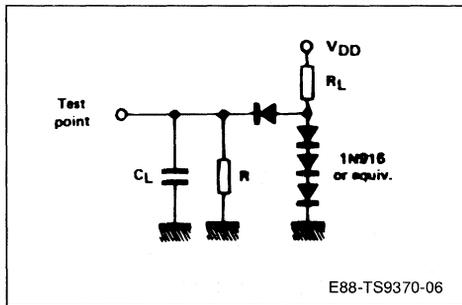
\* With respect to V<sub>SS</sub>.

**ELECTRICAL OPERATING CHARACTERISTICS**

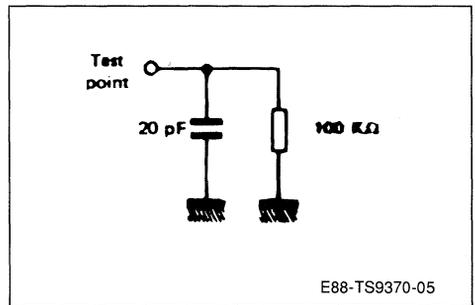
(V<sub>CC</sub> = 5.0 ± 5 %, V<sub>SS</sub> = 0, T<sub>A</sub> = - 25 °C to + 85 °C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>DDC</sub>	Analog Supply Voltage	-	V <sub>CC</sub>	7	V
I <sub>DDC</sub>	Analog Supply Current	-	20	-	mA
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	V
V <sub>IH</sub>	Input High Voltage	RESET	3	-	V <sub>CC</sub>
		All Other Inputs	2	-	V <sub>CC</sub>
I <sub>in</sub>	Input Leakage Current	-	-	20	µA
V <sub>OH</sub>	Output High Voltage (I <sub>oad</sub> = - 500 µA)	2.4	-	-	V
V <sub>OL</sub>	Output Low Voltage (I <sub>oad</sub> = 1.6 mA)	-	-	0.4	V
P <sub>D</sub>	Power Dissipation	-	300	500	mW
C <sub>in</sub>	Input Capacitance	-	-	15	pF
I <sub>TSI</sub>	Three State (off state) Input Current	-	-	10	µA

Test Load for Digital Output



Test Load for Analog Output



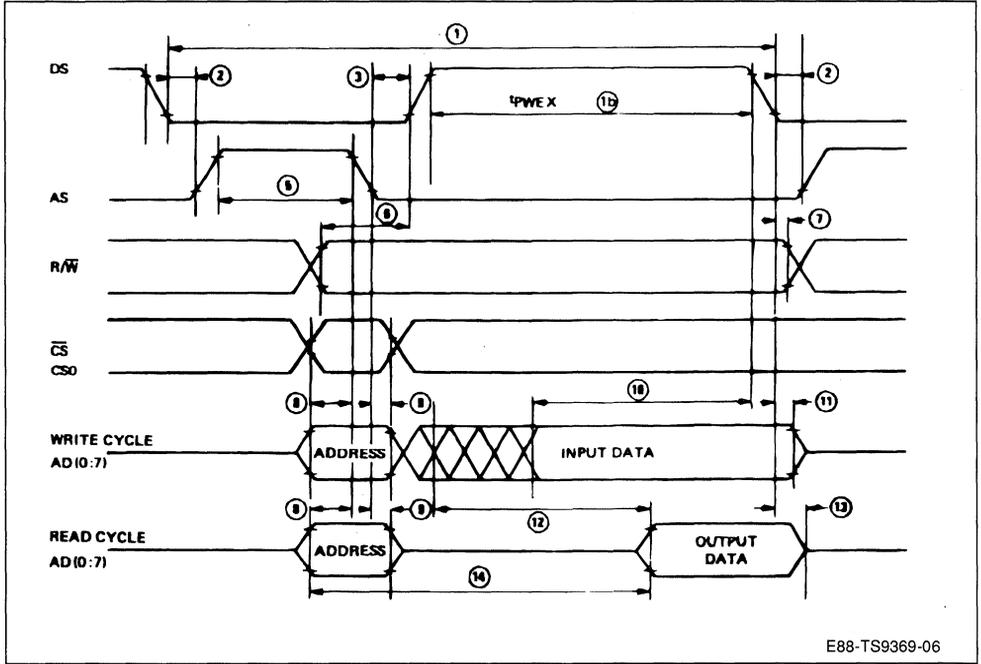
	AD (0 : 7)	M
C <sub>L</sub>	100 pF	50 pF
R <sub>L</sub>	1 kΩ	3.3 kΩ
R	4.7 kΩ	4.7 kΩ

**MICROPROCESSOR INTERFACE TIMING** AD (0 : 7), AS, DS, R/W,  $\overline{CS}$ , CS0
 $V_{CC} = 5.0 \pm 5\%$ ,  $T_A = -25\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $C_L = 100\text{ pF}$  on AD (0 : 7)

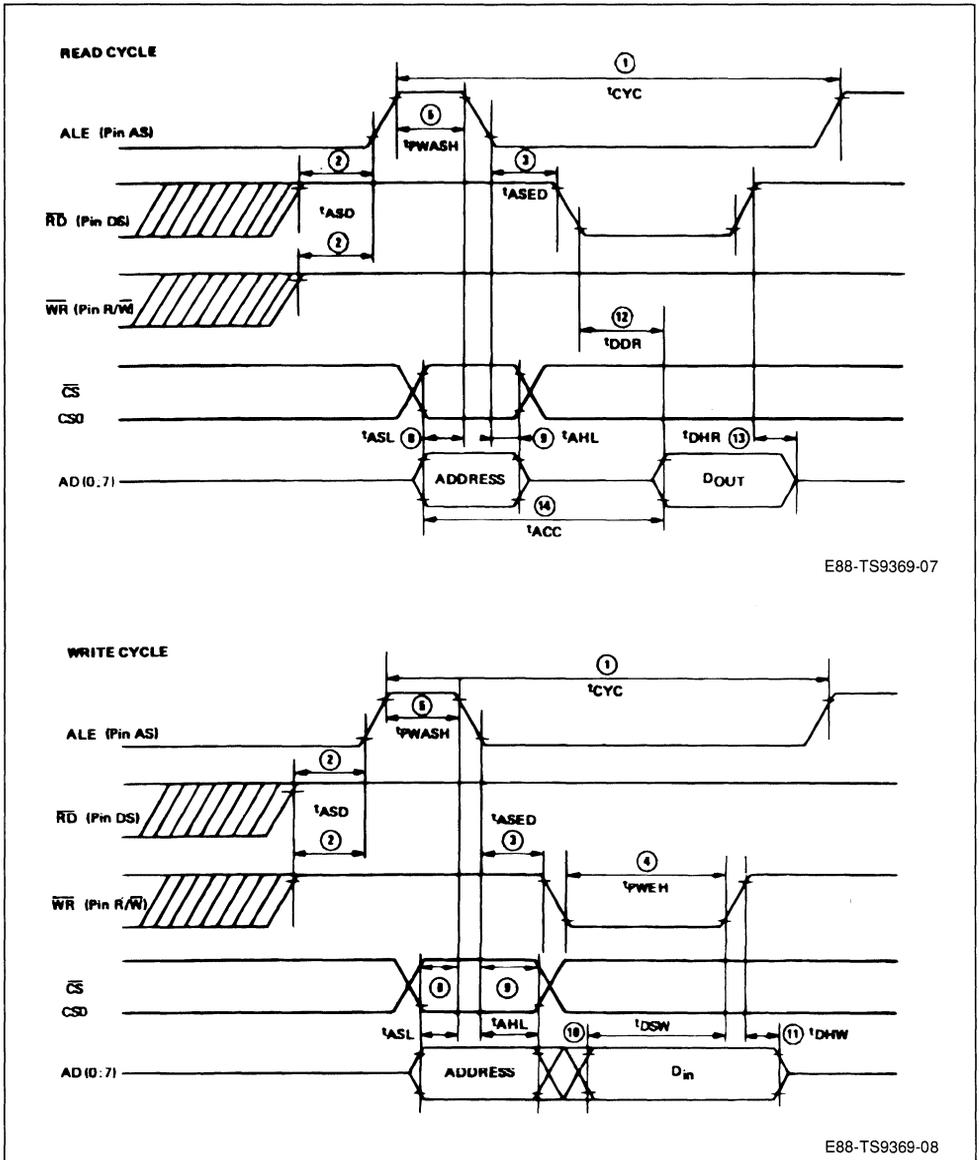
 TTL input values are 0 to 3 volts, with input rise/fall time  $\leq 3\text{ ns}$ , measured between 10 % and 90 % points. Timing reference at 50 % for inputs and outputs.

Indent. Number	Symbol	Parameter	Min.	Typ.	Max.	Unit
1	$t_{CYC}$	Cycle Time	400	–	–	ns
1b	$t_{PEWX}$	DS Pulse Width High Time	200	–	–	ns
1c	$t_{PEWL}$	DS Pulse Width Low Time (timing 3)	120	–	–	ns
2	$t_{ASD}$	DS Low to AS High (timing 1 and 3) DS High or R/W high to AS high (timing 2)	20	–	–	ns
3	$t_{ASED}$	AS Low to DS High (timing 1) AS Low to DS Low or R/W Low (timing 2)	20	–	–	ns
4	$t_{PWEH}$	Write Pulse Width	200	–	–	ns
5	$t_{PWASH}$	AS Pulse Width	100	–	–	ns
6	$t_{RWS}$	R/W to DS Setup Time (timing 1)	20	–	–	ns
6b		R/W, AS, $\overline{CS}$ , CS0 to DS Setup Time (timing 3)	20	–	–	ns
7	$t_{RWH}$	R/W to DS Hold Time (timing 1)	10	–	–	ns
8	$t_{ASL}$	Address and $\overline{CS}$ , CS0 Set Up Time	20	–	–	ns
9	$t_{AHL}$	Address and $\overline{CS}$ , CS0 Hold Time	20	–	–	ns
10	$t_{DSW}$	Data Setup Time (write cycle)	50	–	–	ns
11	$t_{DHW}$	Data Hold Time (write cycle)	10	–	–	ns
12	$t_{DDR}$	Data Access Time from DS (read cycle)	–	–	150	ns
13	$t_{DHR}$	DS Inactive to High Impedance State Time (read cycle)	10	–	80	ns
14	$t_{ACC}$	Address to Data Valid Access Time	–	–	300	ns

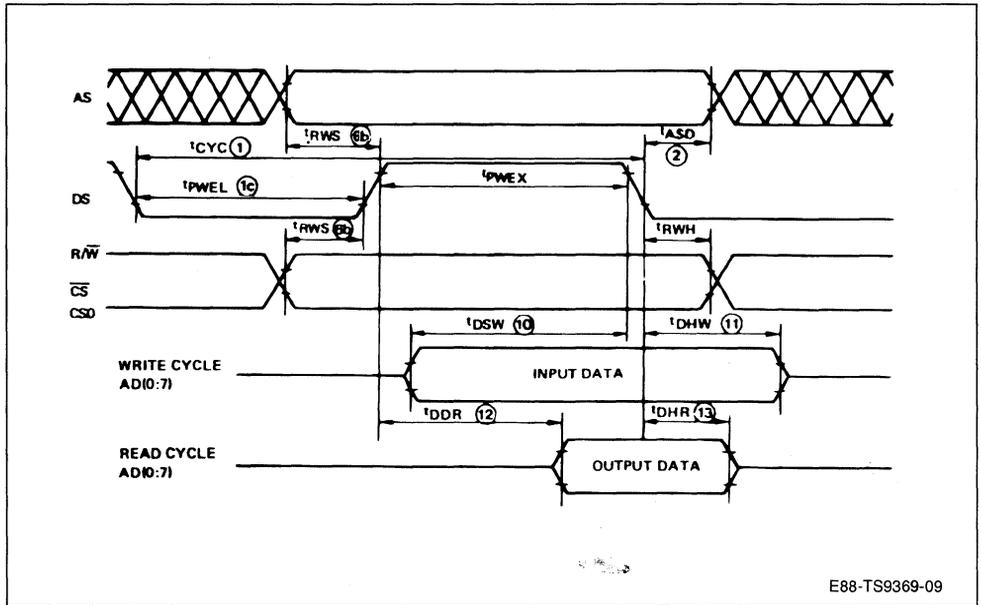
TIMING DIAGRAM 1 - MULTIPLEXED MODE - MOTOROLA TYPE (SMI = V<sub>SS</sub>)



TIMING DIAGRAM 2 - MULTIPLEXED MODE - INTEL TYPE (SMI = V<sub>SS</sub>)



**TIMING DIAGRAM 3 - NON-MULTIPLEXED MODE (SMI = V<sub>CC</sub>)**



E88-TS9369-09

**DIGITAL VIDEO SIGNALS - HP, P(0:3), BLK, M, RESET**

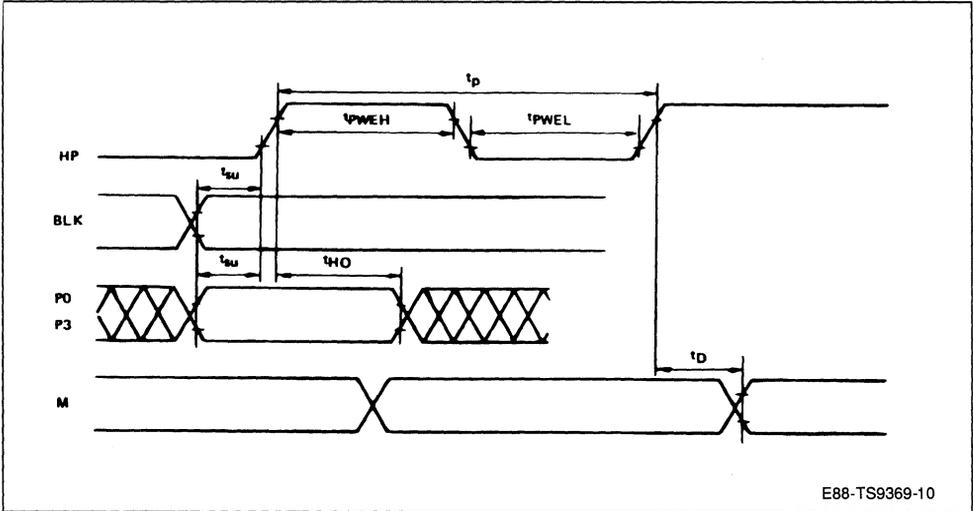
V<sub>CC</sub> = 5.0 ± 5 %, T<sub>A</sub> = - 25 °C to + 85 °C. TS9370-20 and TS9370-30

T<sub>A</sub> = 0 °C to 70 °C. TS9370-45

TTL input values are 0 to 3 volts, with inputs rise/fall time ≤ 3 ns, measured between 10 % and 90 % points. Timing reference at 50 % for inputs and outputs.

Symbol	Parameter	TS9370-20		TS9370-30		TS9370-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>p</sub>	HP Clock Period	50	1000	33	1000	22.5	1000	ns
t <sub>PEWH</sub>	HP High Pulse Width	20	-	11	-	6	-	ns
t <sub>PEWL</sub>	HP Low Pulse Width	20	-	11	-	6	-	ns
t <sub>SU</sub>	BLK and P(0:3) Set Up Time to HP	5	-	5	-	5	-	ns
t <sub>HO</sub>	BLK and P(0:3) Hold Time from HP	10	-	10	-	5	-	ns
t <sub>D</sub>	M Output Delay from HP	-	30	-	30	-	22.5	ns
t <sub>PWRL</sub>	RESET High Pulse Width	400	-	400	-	400	-	ns

TIMING DIAGRAM 4



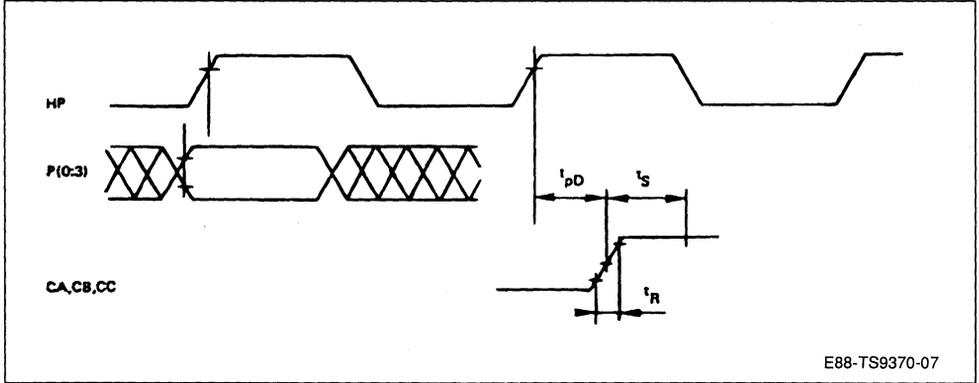
E88-TS9369-10

**ANALOG VIDEO OUTPUTS CA, CB, CC**

$V_{DDC} = 5V, C_L = 20 \text{ pF}, R_L = 100 \text{ k}\Omega$   
 $T_A = -25 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}, \text{TS9370-20, TS9370-30}$   
 $0 \text{ }^\circ\text{C to } +70 \text{ }^\circ\text{C}, \text{TS9370-45}$

Symbol	Parameter	TS9370-20		TS9370-30		TS9370-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
	Analog Outputs V White	2.10	2.16	2.10	2.16	2.10	2.16	V
	V Black	0.76	0.82	0.76	0.82	0.76	0.82	V
	Output Impedance	-	440	-	290	-	230	$\Omega$
	Differential non Linearity	- 1/2	+ 1/2	- 1/2	+ 1/2	- 1/2	+ 1/2	LSB
	Monotonicity	Guaranted						
$t_{pd}$	Propagation Delay CA, CB, CC Outputs from HP	-	30	-	30	-	20	ns
$t_R$	10 to 90 % Rise Time	-	16	-	12	-	8	ns
$t_s$	Output Setting Time to 1/2 LSB	-	20	-	15	-	10	ns

TIMING DIAGRAM 5



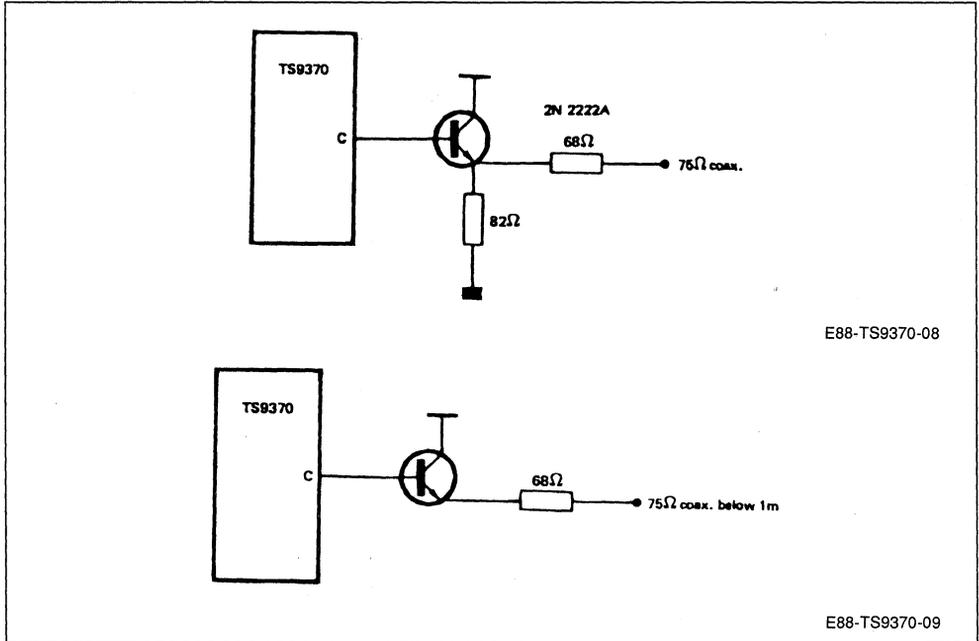
E88-TS9370-07

VIDEO INTERFACE

The function of the video amplifier is to match up the output impedance of TS9370 with a 75 Ω Monitor input. With the example of video amplifier shown in figure 2, the output video signal is compatible with the RS170 video standard.

A lot of care is needed when linking the TS9370 colors outputs to video amplifier.  
 Currently :  $3.4 RC < 0.7 t_p$   
 $R$  = output impedance of TS9370 DAC  
 $C$  = input capacitance of video amplifier  
 $t_p$  = video clock period

Figure 2 : Typical Low Cost Video Interface



E88-TS9370-08

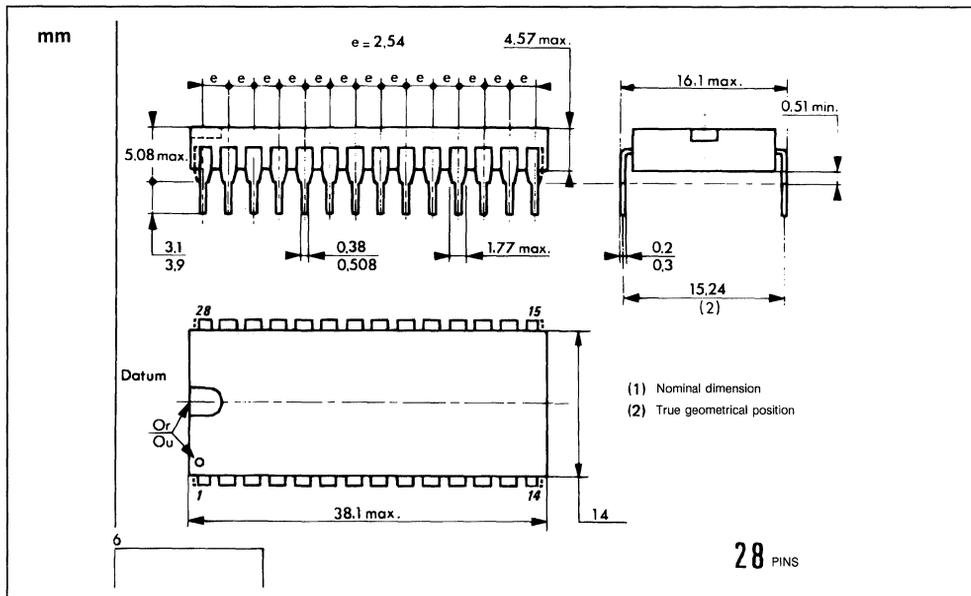
E88-TS9370-09

ORDER INFORMATION

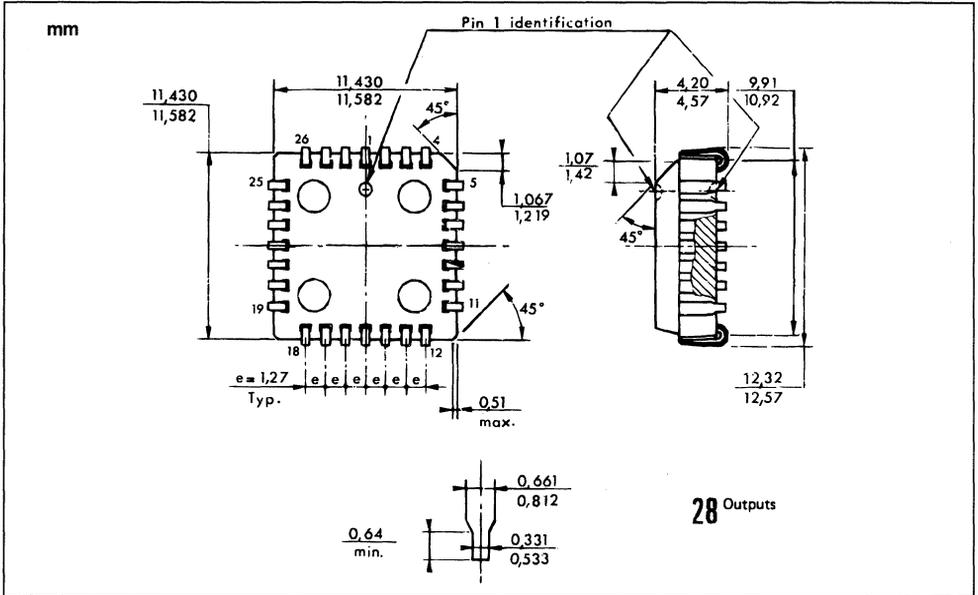
Part Number	Temperature	Package
TS9370IP20	- 25 °C to + 85 °C	DIP28
TS9370IFN20	- 25 °C to + 85 °C	PLCC28
TS9370IP30	- 25 °C to + 85 °C	DIP28
TS9370IFN30	- 25 °C to + 85 °C	PLCC28
TS9370CP45	0 °C to 70 °C	DIP28

PACKAGE MECHANICAL DATA

28 PINS - PLASTIC DIP



28 PINS - PLASTIC LEADED CHIP CARRIER



# **APPLICATION NOTES**



## EF9369 COLOR PALETTE

By J.F. FEVRE

### DISPLAY UNIT AND MEMORY PLANE

On a monitor, the screen is partitioned into X dots and Y lines. This number of dots and lines gives the definition. For example 256 x 256, 640 x 480, etc.

Each dot or pixel is associated with a bit in a memory plane. On a monochrome monitor, each pixel will be on or off according to its value in the memory plane. That kind of monitor has got only one gun to drive the screen.

A color monitor owns three guns (a red, a green and a blue) since it is known that all the colors are available with these three primary colors.

To drive these three guns, at least three memory planes are needed. Each memory plane can be as-

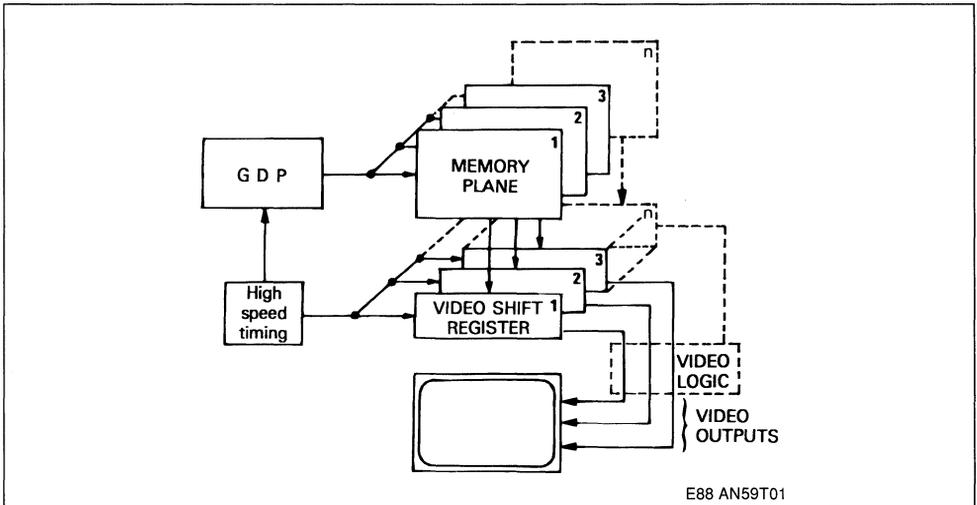
sociated to a gun. So we get a red plane, a green plane and a blue plane which give eight fixed colors on the screen.

If more colors are needed on the screen at the same time, more memory planes must be used.

With  $n$  planes it will be possible to get  $2^n$  colors on the screen at the same time. But in this case, the problem is to deal with the three red, green and blue inputs of a color monitor.

Another problem is that all these sets of colors are fixed, and most of the time, in a graphic application much more colors are needed.

All these problems can be solved by using the EF9369 single chip color palette.



### PALETTE DESCRIPTION

Each pixel's intensity is represented by 1, 2, 4, 8 or more bits of memory. Several methods can be used to encode colored pictures for storage in a frame buffer. The simplest method is to define the color components of each pixel. The bits representing the pixel can be divided into three groups of bits, each

indicating the intensity of one of the three primary color components.

The simple color component encoding scheme (as described in page 1) has the disadvantage of limiting the range of colors. A more flexible scheme involves the use of a color look-up table (CLUT).

A color palette (actually a color look-up table stored in RAM) both eases the host's task and cuts the amount of memory needed in the frame buffer. At any one time, the RAM is able of mapping all the graduations possible for each of the three primary colors.

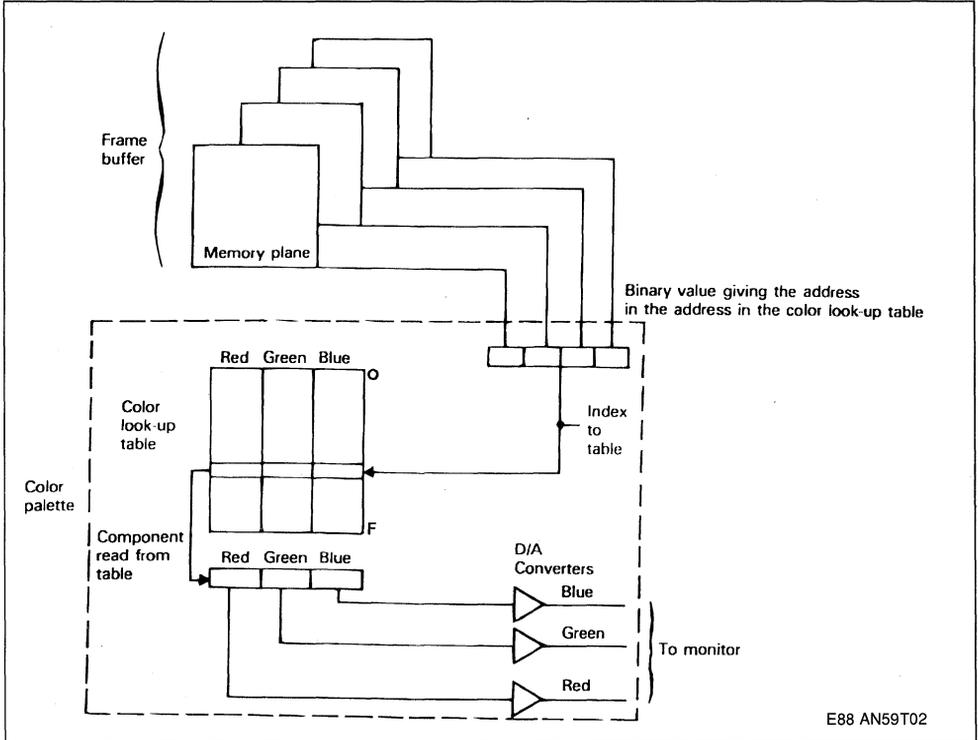
Consequently, instead of storing these color intensities directly, the frame buffer is free to store merely their locations within the color map.

The values stored in the frame buffer are treated as addresses into the table of colors defined by their red, green and blue components. (see figure 2.1).

A major advantage of this approach is that it alleviates the chore of changing colors because the system's host processor must write each color change to only one address in the palette.

For maximum utility, the color look-up table uses read-write memory. It is then possible to assign a different set of colors to different application programs and to mix a set of colors interactively for painting purposes.

**Figure 2.1.**



E88 AN59T02

**EF9369**

EP9369 contains a 16 register CLUT. Each of these 13-bit register holds three 4-bit color field CA(0:3) ; CB(0:3) ; CC(0:3) and a marking bit M. (see figure 4).

So to use this chip ; four memory planes are needed. It is then possible to choose a set of colors amongst 4096.

The marking bit may be used for blinking or highlight purposes.

Each binary value coming from the CLUT is then converted in an analogic value in order to drive a monitor.

Each 4-bit D/A converter is  $\gamma$  corrected in order to linearize the luminance driven on the screen versus the digital value. The typical digital to voltage conversion law is given table 2.2.

The output voltages are proportional to the analog supply voltage  $V_{DDC}$ . When required, setting  $V_{DDC}$  allows a gain adjustment. But in most applications,  $V_{DDC}$  and  $V_{DD}$  can be derived from the same supply through independent decoupling.

Table 2.2.

Binary Input		Analog Output (V)		
		Min.	Typ.	Max.
Low Level	0000	–	0.8	–
	0001	–	1.18	–
	0010	–	1.28	–
	0011	–	1.36	–
	0100	–	1.42	–
	0101	–	1.47	–
	0110	–	1.52	–
	0111	–	1.56	–
	1000	–	1.60	–
	1001	–	1.63	–
	1010	–	1.66	–
	1011	–	1.69	–
	1100	–	1.72	–
	1101	–	1.75	–
	1110	–	1.76	–
	High Level	1111	–	1.80

**Note :** The internal A/D converters deliver on CA, CB and CC outputs 16 levels with  $\gamma$  law correction ( $\gamma = 2.8$ ). The typical transfer characteristic is given by :

$$V = \left(\frac{N}{15}\right) \frac{1}{2.8} \frac{V_{DDC}}{5} + 0.16 V_{DDC}$$

Where N is the binary value.

## MICROPROCESSOR INTERFACE

EF9369 interfaces to a microprocessor through :

- a multiplexed 8-bit address/data bus ;
- non-multiplexed mode.

The mode selection is programmed through the SMI pin.

Multiplexed mode : SMI connected to  $V_{SS}$ .

Non-multiplexed mode : SMI connected to  $V_{CC}$

- Non-multiplexed mode : (see figure 3.1).
- $V_{CC}$ ,  $V_{DD}$  and SMI pins must be connected to + 5 volts.
- $V_{SS}$  pin must be connected to ground.

The  $\overline{CS}$  signal is obtained from an address decoder.

In this mode, EF9369 maps into the microprocessor addressing space as two byte address only.

- Multiplexed mode : (see figure 3.2).
- $V_{CC}$  and  $V_{DD}$  pins must be connected to + 5 volts.
- SMI and  $V_{SS}$  pins must be connected to ground.

In this mode, EF9369 maps into the microprocessor addressing space as 32 byte locations.

A lot of care must be taken with the  $\overline{CS}$ .CS0 signal.

Figure 3.1: Non-multiplexed Mode - Motorola Type Microprocessor.

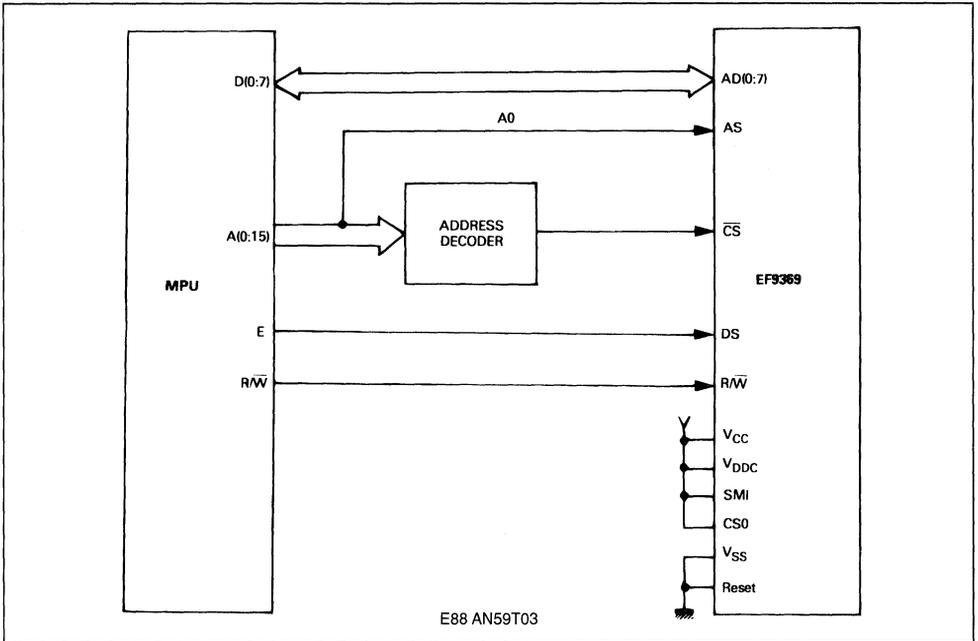
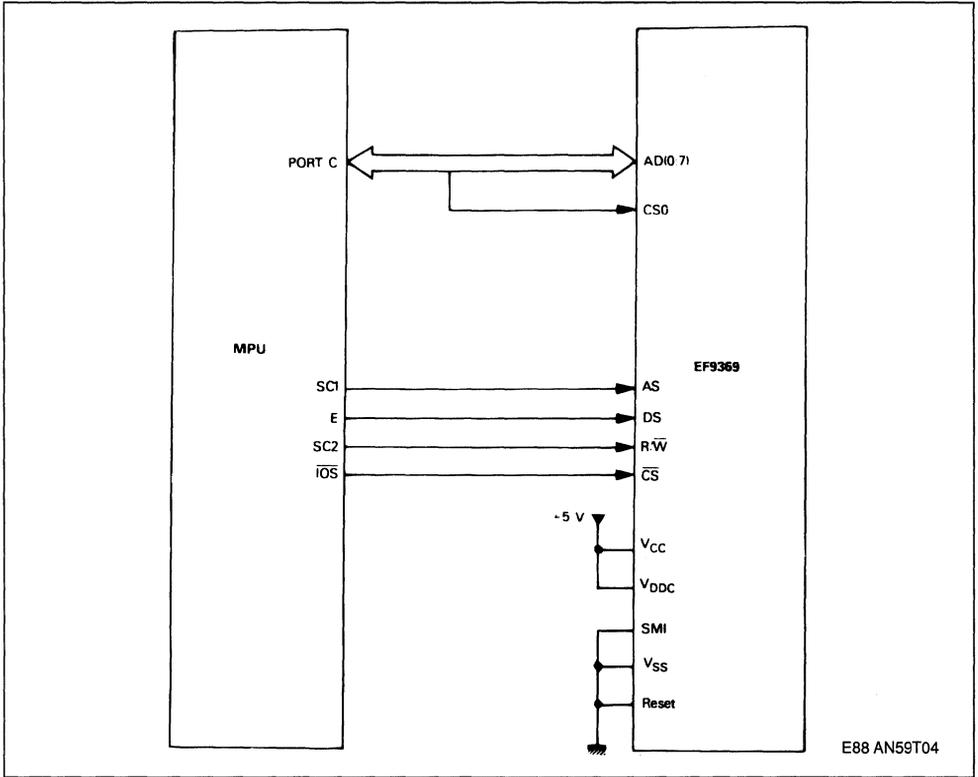
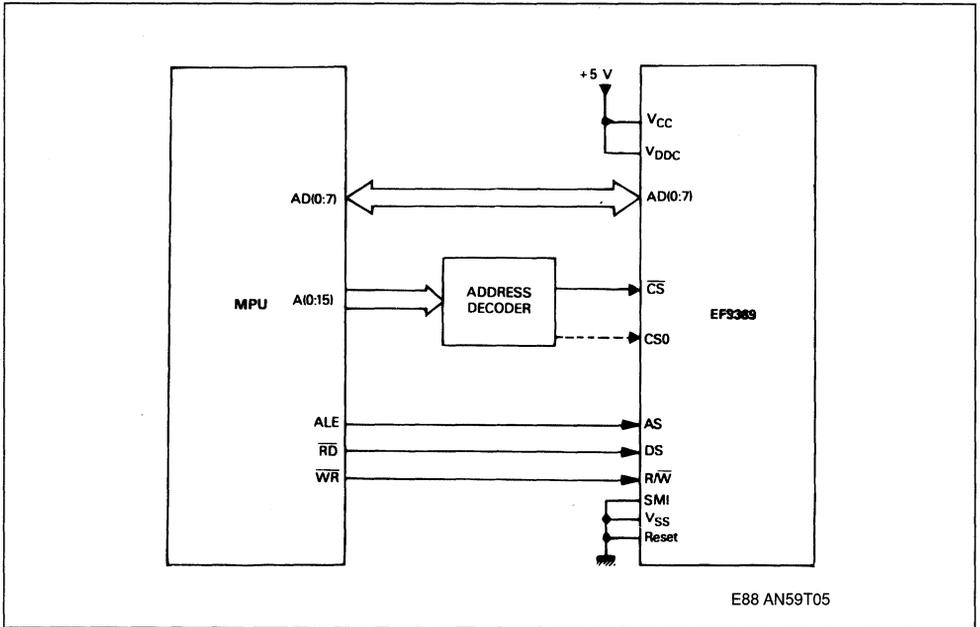


Figure 3.2 : Multiplexed Mode - Motorola Type Microprocessor.



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**Figure 3.3 : Multiplexed Mode - Intel Type Microprocessor.**



**PROGRAMMING THE EF9369**

It is very important to access the CLUT only during retrace intervals to avoid to spoil the screen with black spots.

**PROGRAMMING THE EF9369 IN NON-MULTI- PLEXED MODE**

EF9369 is located into the microprocessor addressing space in 2 addresses only.

The first one is the data register and the next one is the address register.

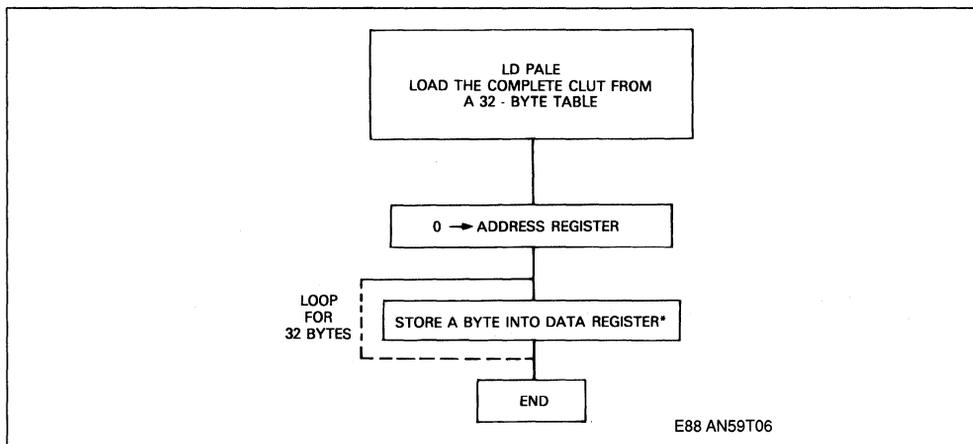
After each access to the data register the address register is automatically incremented modulo 32. This scheme allows sequential addressing to the CLUT without address reloading.

The flow chart and the source listing in 6809 assembler language given below show an example for loading the complete color look up table. The CLUT addressing table is given in figure 4.

Figure 4 : Clut Addressing.

Color Look-Up Table (CLUT)								CLUT Byte Address								Register Index #
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	X	X	X	0	0	0	0	0	0
X	X	X	M	CC3	CC2	CC1	CC0	X	X	X	0	0	0	0	1	
CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	X	X	X	0	0	0	1	0	1
X	X	X	M	CC3	CC2	CC1	CC0	X	X	X	0	0	0	1	1	
↓																↓
CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	X	X	X	1	1	1	1	0	15
X	X	X	M	CC3	CC2	CC1	CC0	X	X	X	1	1	1	1	1	

X = Don't care



\* Note : The address register is automatically incremented after this instruction.

**APPLICATION NOTE**

PAGE 001 EF9369 .SA : 0

```

00001                OPT   LLE = 110
00002                *
00003                *EF9369 PROGRAMMING EXAMPLE
00004                *THIS PROGRAM IN 6809 ASSEMBLER LANGUAGE
00005                *SHOWS HOW THE WHOLE COLOR LOOK-UP TABLE (CLUT)
00006                *CAN BE SEQUENTIALLY LOADED WHEN THE EF9369
00007                *IS CONNECTED TO A NON-MULTIPLEXED
00008                *MICROPROCESSOR.
00009                *

00011                F440  A  DATA  EQU  $F440  EF9369 DATA REGISTER
00012                F441  A  ADDR   EQU  DATA + 1  EF9369 ADDRESS REGISTER

00014                2000  A  STACK  EQU  $2000
00015                1F80  A  STACKU EQU  STACK-128

00017A 1000                ORG  $1000
00018A 1000 10CE 2000  A  LDS  #STACK
00019A 1004 CE 1F80  A  LDU  #STACKU
00020A 1007 8E 1026  A  MAIN LDX #CLOR1  INIT INDEX REGISTER
00021A 100A BD 100F  A  JSR  LDPALE
00022A 100D 20 FE 100D  HERE  BRA  HERE  END OF MAIN PROGRAM

00024                *
00025                *LDPALE : LOAD THE WHOLE CLUT
00026                *ARGUMENT : X POINTS TO A 32-BYTE TABLE WHICH
00027                *IS TO BE LOADED INTO CLUT.
00028                *FOR EVERY 2-BYTE SET, THE FIRST BYTE HOLDS
00029                *CB (0 : 3) AND CA (0 : 3) FIELD.
00030                *THE SECOND BYTE MARKING BIT M
00031                *AND CC (0 : 3) FIELD.
00032                *EXIT : A AND B ARE DESTROYED
00033                *X = X INITIAL + 32
00034                *
00035                100F  A  LDPALE  EQU  *
00036A 100F 4F                CLRA
00037A 1010 B7 F441  A  STA  ADDR  INIT EF9369 ADDRESS REGISTER
00038A 1013 86 10  A  LDA  #16
00039A 1015 A7 C2  A  STA  -U  STORE LOOP COUNTER

00041A 1017 EC 81  A  LDPA10 LDD .X++  READ 2 BYTES FROM TABLE
00042A 1019 B7 F440  A  STA  DATA  LOAD DATA REGISTER
00043A 101C F7 F440  A  STB  DATA  LOAD DATA REGISTER
00044A 101F 6A C4  A  DEC  .U  DEC LOOP COUNTER
00045 1021 26 F4 1017  BNE  LDPA10

00047A 1023 33 41  A  LEAU  1.U  UPDATE U
00048A 1025 39                RTS

00051                1026  A  CLOR1  EQU  *
00052A 1026 01  A  FCB  $01, $0A, $15, $08, $9A, $04, $06, $0F
00053A 102E 49  A  FCB  $49, $03, $83, $0F, $0E, $04, $AD, $04
00054A 1036 F9  A  FCB  $F9, $0C, $3A, $08, $A0, $0A, $F8, $05
00055A 103A 3C  A  FCB  $3C, $0D, $C8, $0B, $18, $09, $49, $07
00056                END

TOTAL ERRORS 00000--00000
TOTAL WARNINGS 00000--00000

```



Figure 5.2.

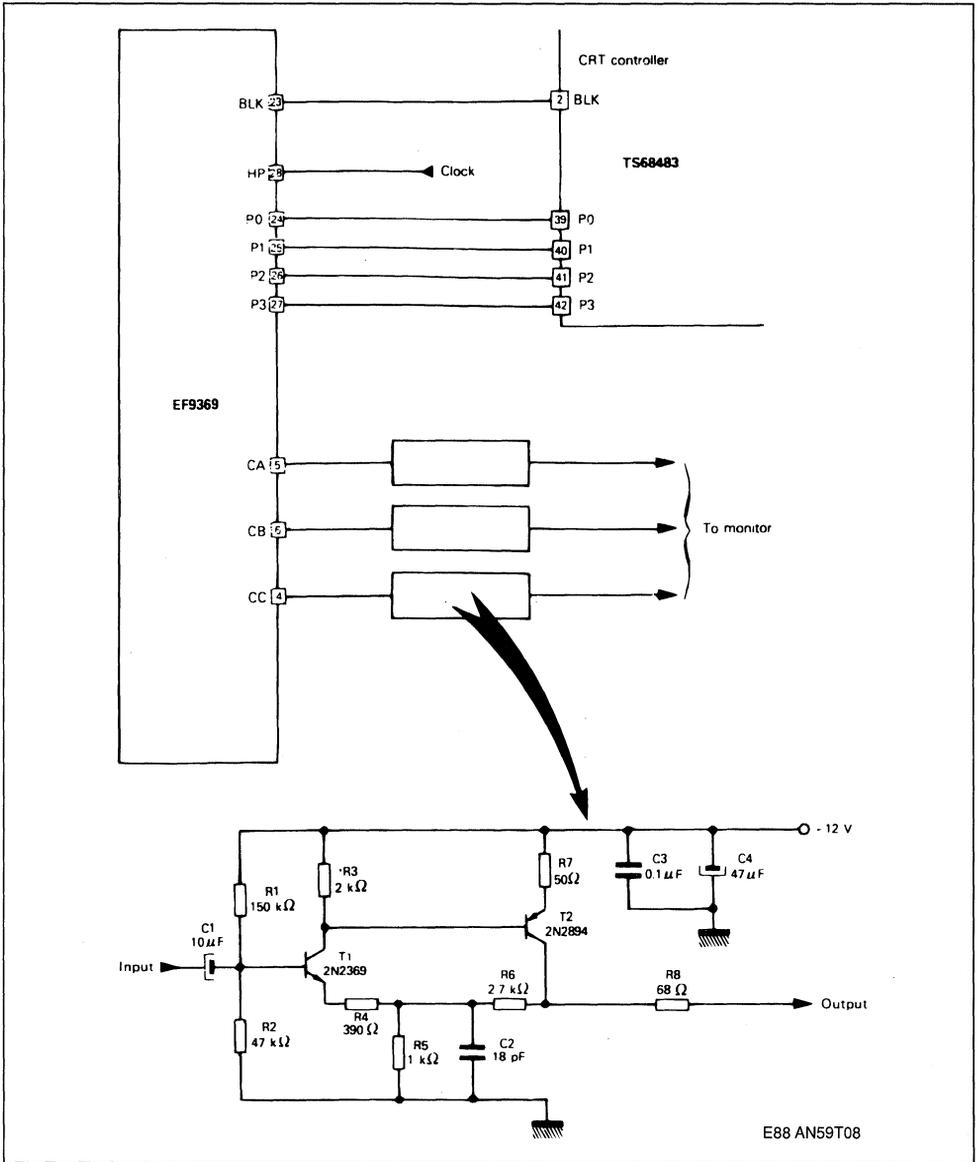
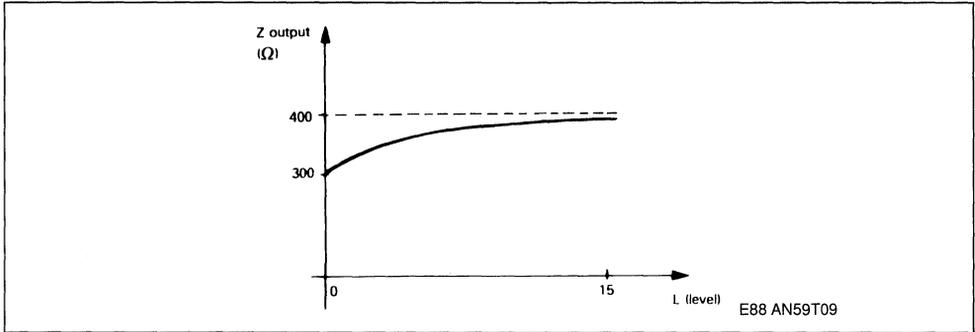


Table 5.3.



The set-up time of the color levels at the circuit output roughly follows the equation ( $T_s = 5RC$ ) :

$T_s$  : Set-up time

R : The output of the EF9369 may be considered as a static resistor (see table 5.3)

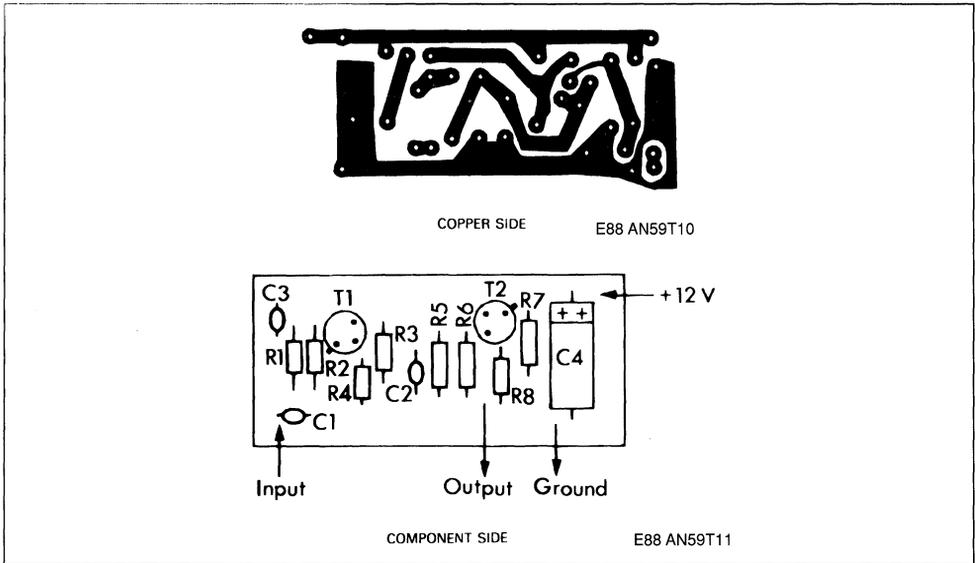
C : Input capacitance of the video amplifier

So if the set-up time  $T_s$  has to be improved, the solution is to get a video amplifier input capacitance as low as possible.

Example :  $R = 400 \Omega - C = 20 \text{ pF}$

$$T_s = 5 \times 400 \times 20 = 40 \text{ ns}$$

Figure 5.4: Video Amplifier Layout.



**COLOR COMPOSITION**

When the sun light is split through a prism, one can see three main colored zones :

- blue,
- green,
- red.

These colors are called "primary colors", because by mixing them in various proportions, it is possible

to get all the colors that the human eye can see. So far with a common CRT controller it is possible to get only eight basic colors because each "primary color" can get only the value 0 or 1.

- no color = black
- red + green = yellow
- blue + red = magenta
- green + blue = cyan

## APPLICATION NOTE

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With the EF9369 each "primary color" can get sixteen different values which give the possibility of choosing a tint amongst 4096.

### A FEW EXAMPLES

The sixteen values will go from 0 to F for each "primary color" in the CLUT.

- Dark and light :

Cyan is the addition of green and blue. For a dark cyan each value of green and blue must be low.

Ex : green = 3, blue = 3, red = 0

For a light cyan the blue and green values must be high.

Ex : green = D, blue = D, red = 0

- Purple :

Ex : green = 6, blue = 9, red = 8

- Pink : high value of red and equal value of green and blue.

Ex : green = 3, blue = 3, red = D

- Orange :

Ex : green = 3, blue = 0, red = D

- Brown :

Ex : green = 3, blue = 1, red = F

All these examples are only indications. If other colors are needed, each value of each "primary color" must be changed in order to get the right one.

4096 possibilities are available !



**EF9345 SEMI-GRAPHIC DISPLAY PROCESSOR  
GENERAL APPLICATION PRINCIPLES**

**AUGUSTIN GIADIN**

**ABSTRACT**

Associated with a standard memory package, the EF9345 allows full implementation of a low-cost terminal display unit.

The aim of this Application Note is to aid the user in using the EF9345. Design considerations and programming of the circuit in the various operating modes will be discussed.

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ACCESS TO UDS SLICES IN MEMORY

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SCREEN MAPPING WITH UDS CHARACTERS

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**PROGRAMMING THE EF9345 IN 80 CHAR/ROW MODE**

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ACCESS TO CHARACTER CODE

**PROGRAMMIN EXAMPLE EN 80 CHAR/ROW**

## MICROPROCESSOR INTERFACE

### GENERAL PRINCIPLES

The EF9345 interfaces to a microprocessor by :

- an 8-bit address/data multiplexed bus AD(0:7)
- four control signals : AS (Address Strobe), DS (Data Strobe), R/W (Read/Write) and CS (Chip Select).

Each microprocessor access is made as follows :

- First the AS signal falling edge latches the DS, CS and AD(0:7) input. The EF9345 is selected only when CS is strobed low and AD(7:4) most significant bits of the address lines are strobed with the binary value 0010. The latched level of DS signal selects either the Intel mode (DS high) or the 6801 mode (DS low).
- During the second part of the access cycle, the AD(0:7) lines become the data bus. In the 6801 mode, data exchange is made while DS is high and the R/W signal specifies the data transfer direction (a write operation into the circuit is performed when R/W is low). In the Intel mode, DS is generally used as a RD (Read) signal and R/W as a WR (Write) signal.

So connecting the EF9345 to a multiplexed bus microprocessor is quite simple. Figures 1 and 2 show the interface with an EF6801 and an Intel type microprocessor (8085, 8051...).

**Note :** As the EF9345 is selected when the latched address binary value is 0010XXXX (or 2X in hexadecimal), the circuit takes 16 consecutive address locations in the microprocessor addressing space. These addresses correspond to 8 internal registers of the circuit, with each register selected by the three LSB of the address value (see programming description).

### INTERFACE WITH A NON-MULTIPLEXED BUS MICROPROCESSOR

When the EF9345 is used with a non-multiplexed bus microprocessor such as EF6800, EF6809, Z80..., the microprocessor address and data lines must be generally multiplexed to pins AD(0:7). The address strobe and multiplexer command signals must also generated. Figure 3 shows an example

of interfacing the EF9345 to an EF6800/6809 microprocessor, where address and data multiplexing is made with three-state buffers. The AS signal and the buffer enable signals are generated from the E signal with a few TTL-LS circuits. Figure 4 shows the associated timing diagram.

By using the principle described below, it is possible to realize the EF9345 interface with a non-multiplexed bus microprocessor without multiplexing the address and data lines. This principle allows reducing the number of TTL parts for the hardware interface implementation, but requires a few additional instructions when programming the circuit.

Figure 5 illustrates the principle for an EF6800/6809 application. The AD(0:7) pins are directly connected to the microprocessor data bus and the CS input is grounded. An address decoder provides two chip-select signal CS0 and CS1. Any microprocessor write operation to the address which generates CS0 low will result in an AS pulse while E is high and the data present on AD(0:7) are latched into the EF9345 as an "address". During an access to the address generating CS1 low, a DS pulse is generated while E is high and AD(0:7) act as a normal data bus, provided that the circuit has been previously selected.

So any microprocessor access to the EF9345 is made in two steps :

- first the microprocessor must write at address CS0 a data whose binary value is 0010XXXX to select the circuit and to specify by XXXX what register is to be accessed,
- a normal data exchange (read or write operation) can then be made at address CS1 between the microprocessor and the EF9345 register selected during the first cycle.

Flowchart given in figure 6 shows how the microprocessor can read the status register RO.

This principle can be applied to any microprocessor type. Figure 7 shows an implementation example for interfacing with a Z80, where the AS pulse is generated during an I/O write operation at address A7 = 1, A6 = A5 = 0. Access to an EF9345 register is made by an I/O read or write at address A7 = 1, A6 = 1 and A5 = 0. As DS (CS1) is high when AS occurs, the EF9345 is here in the Intel mode.

Figure 1 : Interface with EF6801.

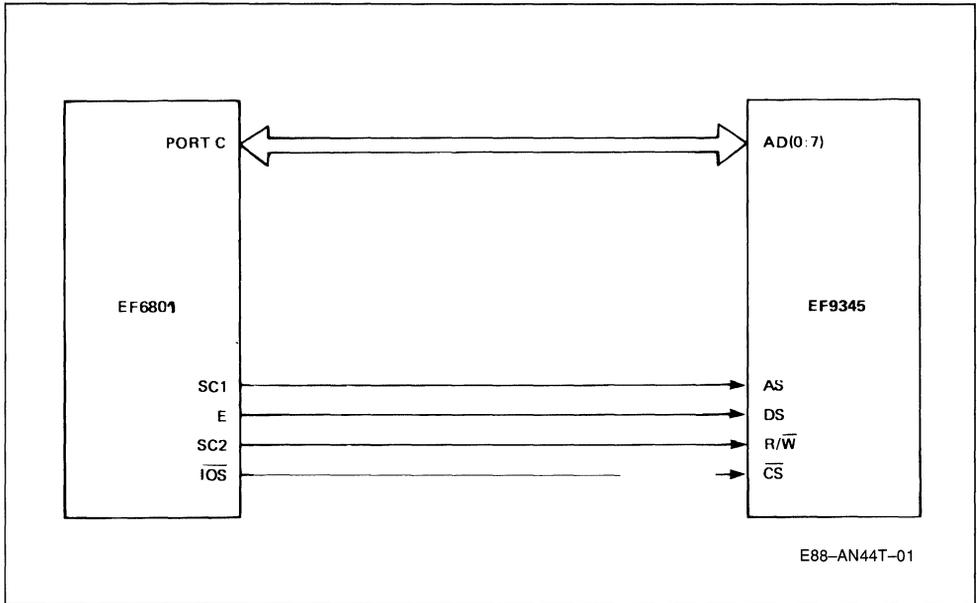


Figure 2 : Interface with a Multiplexed Bus Intel Type Microprocessor.

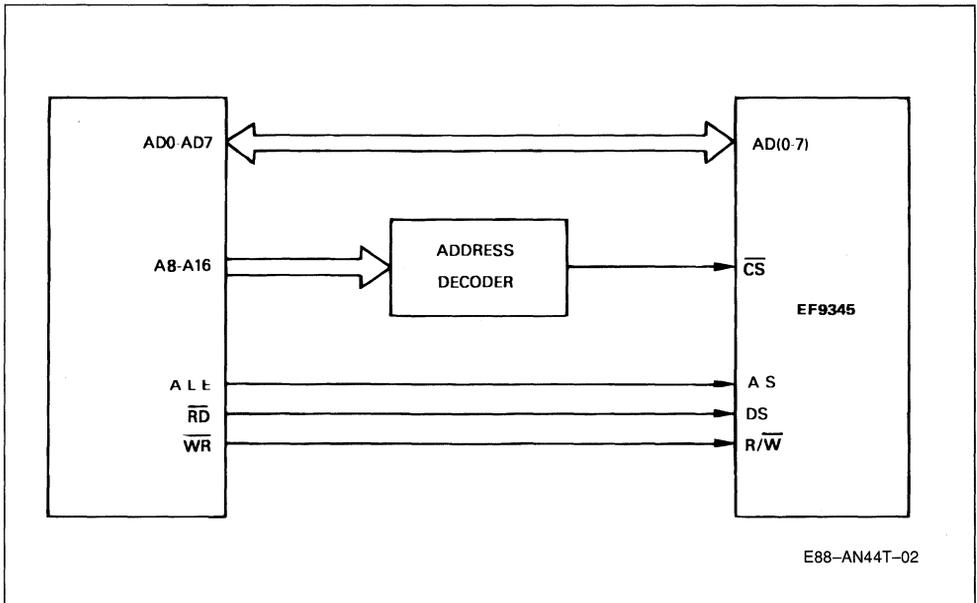
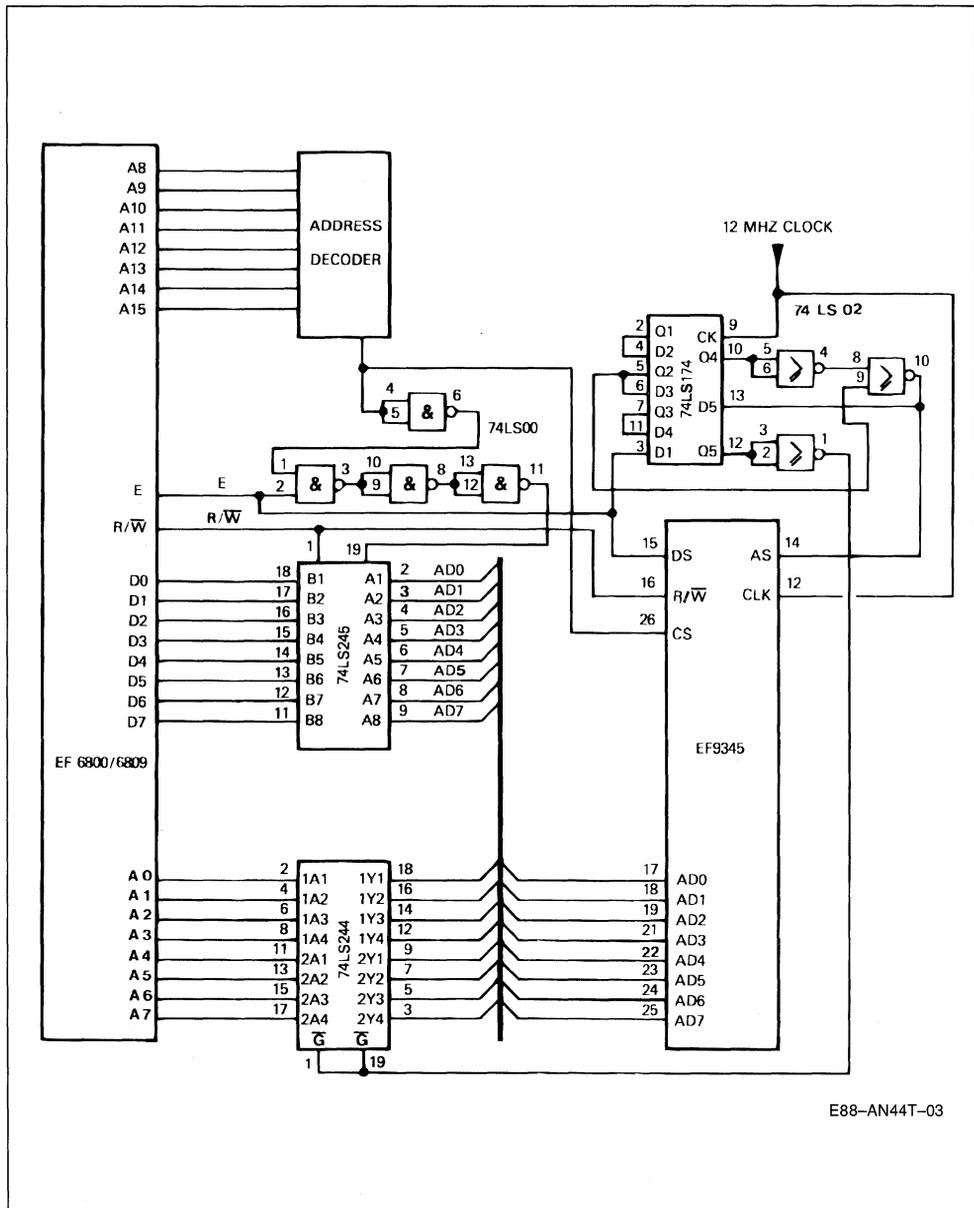


Figure 3 : Interface with EF6800/6809 by Multiplexing Address and Data Bus.



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Figure 4 : Timing Diagram Associated with Figure 3.

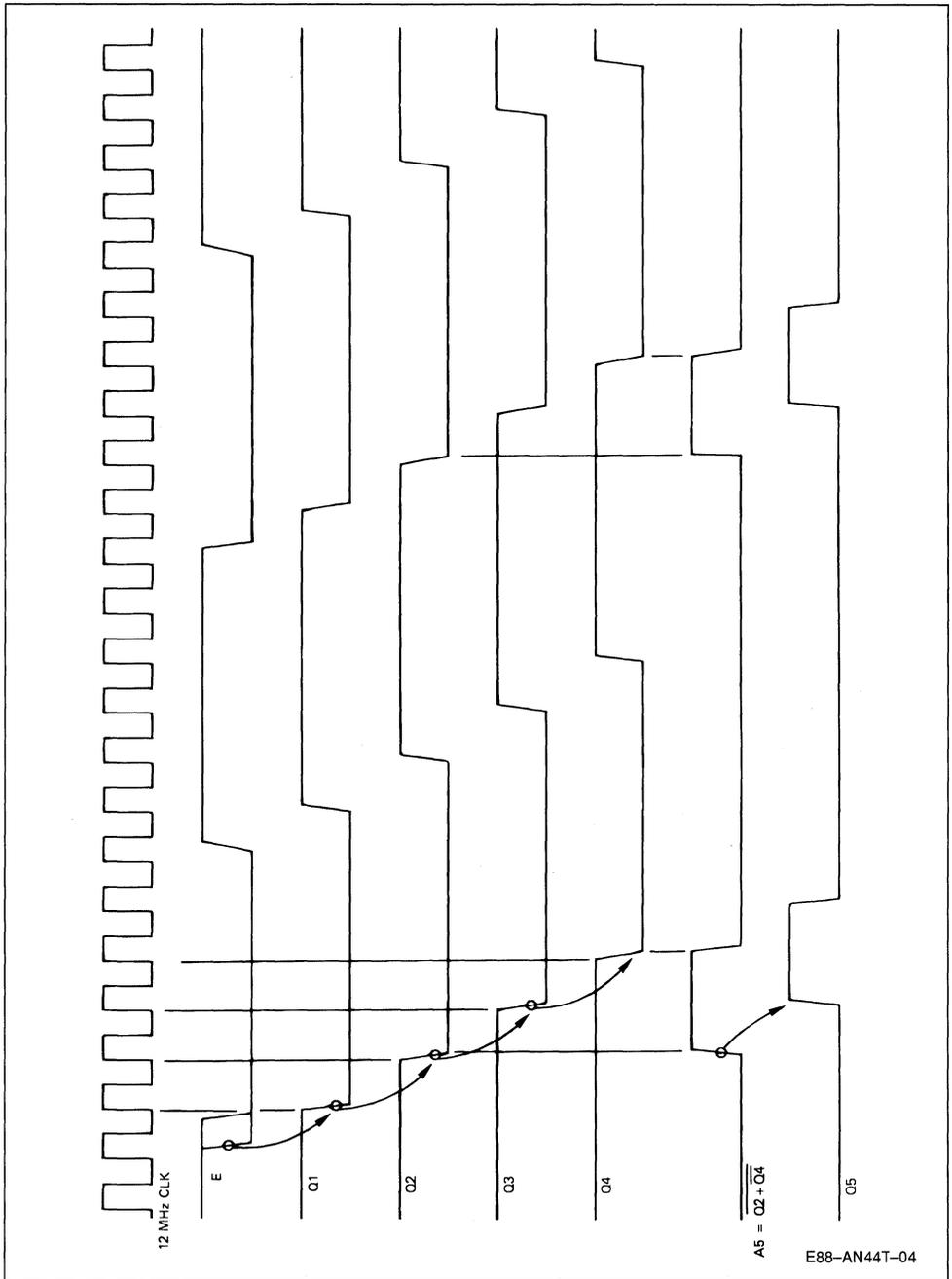


Figure 5 : Interface with EF6800/6809 without Multiplexing Address and Data Bus.

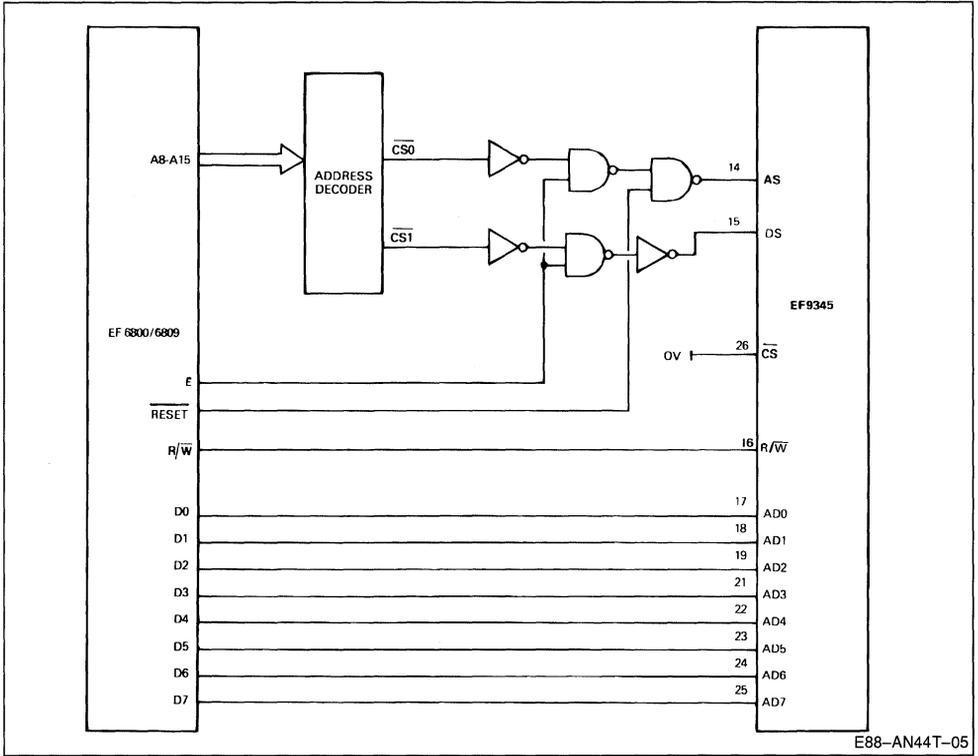


Figure 6 : Access to an EF9345 Register when Using the Non-Multiplexing scheme Interface.

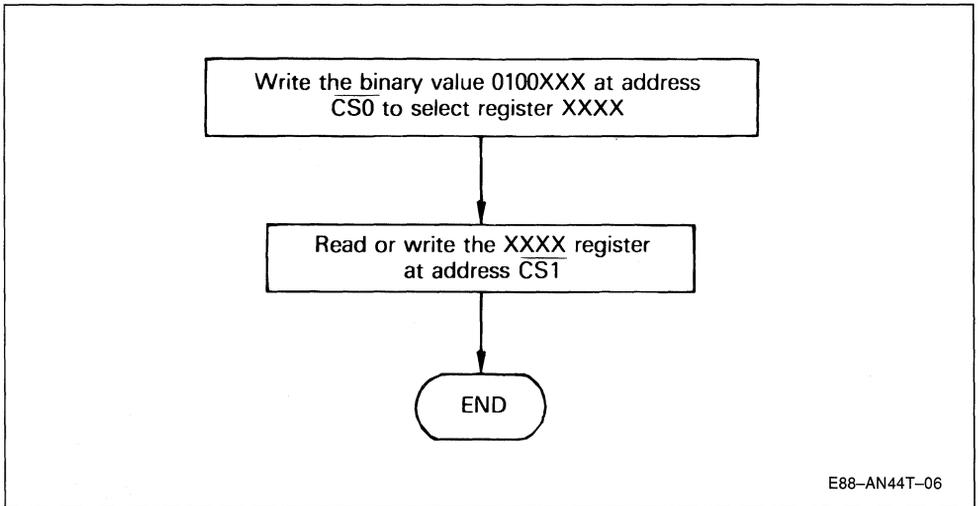
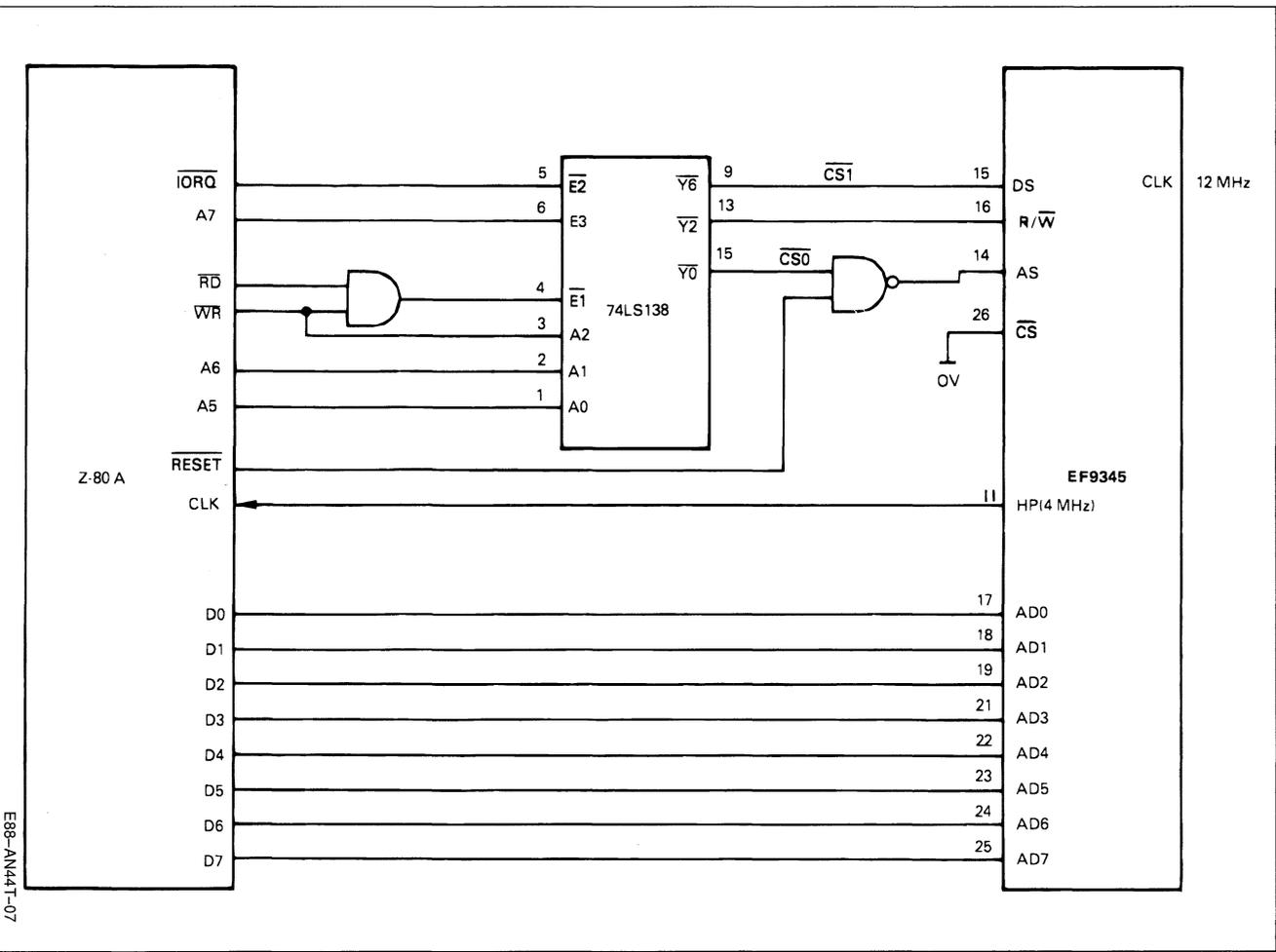


Figure 7 : EF9345 Interface with a Z-80 without Multiplexing Address and Data Bus:



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## MEMORY INTERFACE

The EF9345 can be used with a wide variety of standard memories and manages up to 16 kbytes of private memory.

The memory interfaces is made by :

an 8-bit address/data multiplexed bus ADM(0:7)

a 6-bit high order address bus AM(8:13)

three control signals :  $\overline{OE}$  (Output Enable),  $\overline{ASM}$  (Address Strobe Memory),  $\overline{WE}$  (Write Enable).

During each memory cycle, the EF9345 outputs to ADM(0:7) low order address byte while ASM is high. The high order address bits are provided on AM(8:13) during the whole memory cycle. When ASM goes low, the ADM(0:7) lines become the memory data bus. For a read operation, the OE signal is active low to enable the memory output buffers. A write operation is made when WE is low.

## INTERFACE WITH 2K\*8 STATIC MEMORY

As the address lines are generally not latched by static RAMs, an external 8-bit latch (74LS373) must be used to store the low order address bits ADM(0:7) on the falling edge of ASM signal.

## INTERFACE WITH 8K\* 8 PSEUDO-STATIC RAM

The EF9345 can be directly connected to an 8K\*8 pseudo-static RAM (NEC  $\mu$ PD 4168, INTEL 2187, INMOS 2630...). The ASM signal is fed to the CE input which latches the address lines. As the EF9345 performs DRAM refresh, the memory internal refresh circuitry is not use.

The schematic diagram of figure 8 gives a design example which allows interfacing the EF9345 to 2K\*8 or 8K\*8 memory. With static memory, the 8 jumpers of S8 are connected to provide the low order address lines from the 8-bit latch 74LS373. With pseudo-static memory, the 74LS373 is useless and the 8 jumpers of S7 are connected. Jumpers S1 to S6 are set in position 2 for 2K\*8 RAMs, and in position 1 for 8K\*8 RAMs.

## INTERFACE WITH 16K\*8 DRAM (see figure 9)

When using 16K\*4 dynamic RAMs, the address provided by the EF9345 must be multiplexed to obtain the Row and Column address. ASM can be used directly as the RAS (Row Address Strobe) signal, but the CAS signal must be externally generated. Figure 9 shows an example of generating CAS and the multiplexer command signals from ASM.

As previously, refresh operation is performed by the EF9345.

## PROGRAMMING THE EF9345 - GENERAL PRINCIPLES

### DIRECT ACCESS REGISTERS

As described in the microprocessor interface chapter, the EF9345 is accessed by the microprocessor at 16 consecutive locations from address XX20 to XX2F (hexadecimal), where XX is determined by the user's address decoding. These 16 addresses correspond to 8 internal registers RO to R7 (see figure 10). Each register can be accessed at two addresses : a lower address (bit 3 = 0) and an upper address (bit 3 = 1). For example, if the EF9345 is mapped in the microprocessor addressing space from F420 to F42F, register R1 can be read or written at both addresses F421 and F429.

However, a command present in register RO is executed only after an access to a register at an upper address. This scheme allows re-executing a same command by loading only one argument into an upper address register.

### COMMAND EXECUTION

RO is a write command register and a read status register. A command present in RO is executed with the arguments in the other direct access registers after any access to a register at an upper address (from XX28 to XX2F).

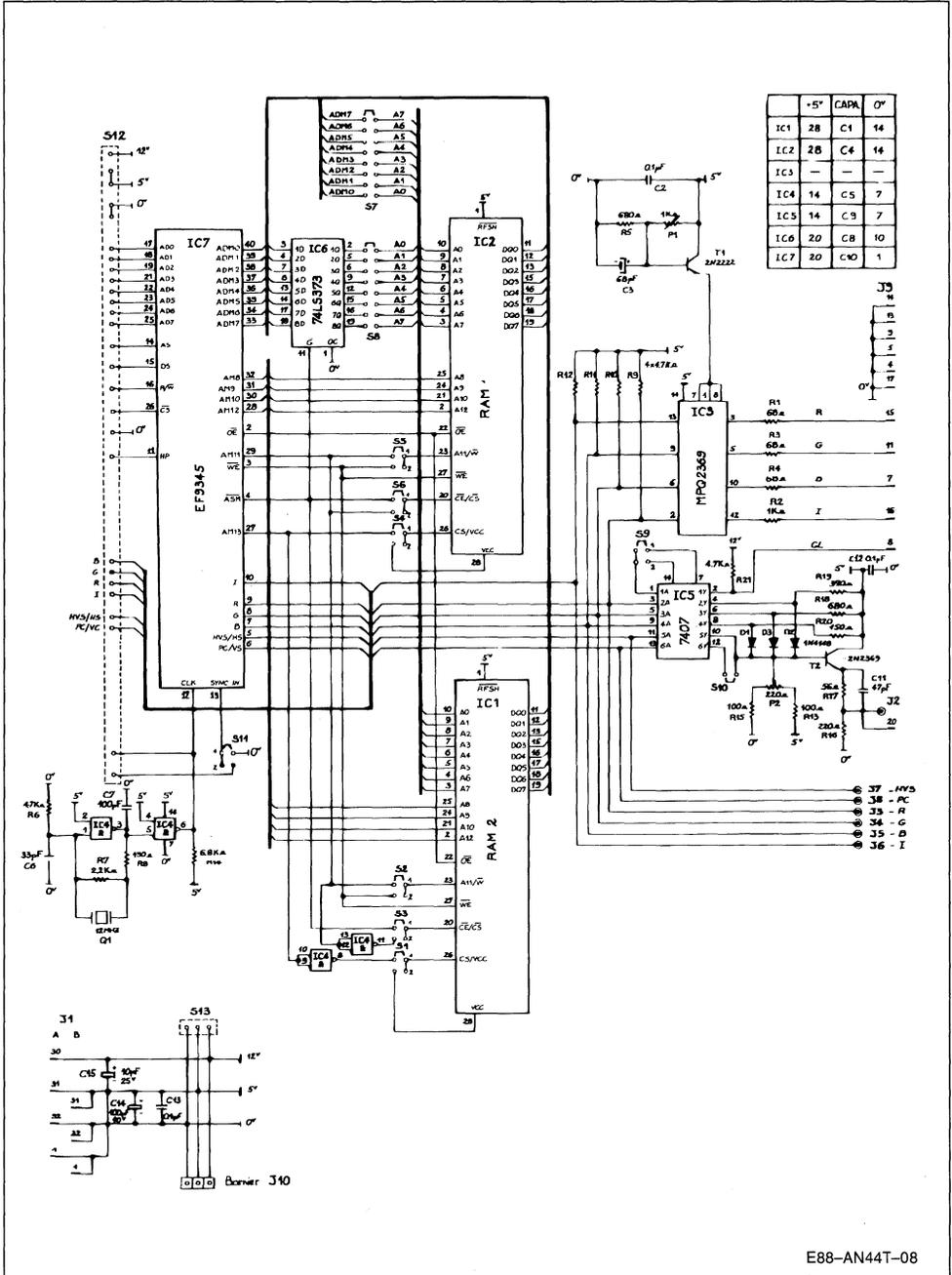
Before any access to a register, the Busy status in the Status register bit 7 must be tested to check a command is not currently executing. However, after power-up a NOP command should be executed without testing the Busy state to set the circuit into a determined state before further operation. A move command with no stop condition can also be aborted by executing a NOP command.

### INDIRECT ACCESS REGISTER (figure 11)

The EF9345 has 5 indirect access registers which define the various operating modes of the circuit : TGS, MAT, PAT, DOR, ROR. Each of these registers is assigned an index r and is indirectly accessed through register R1. Data is transferred between R1 and an indirect access register with the IND command, which specifies the transfer direction (bit R/W) and the register index r (bits 0 to 2).

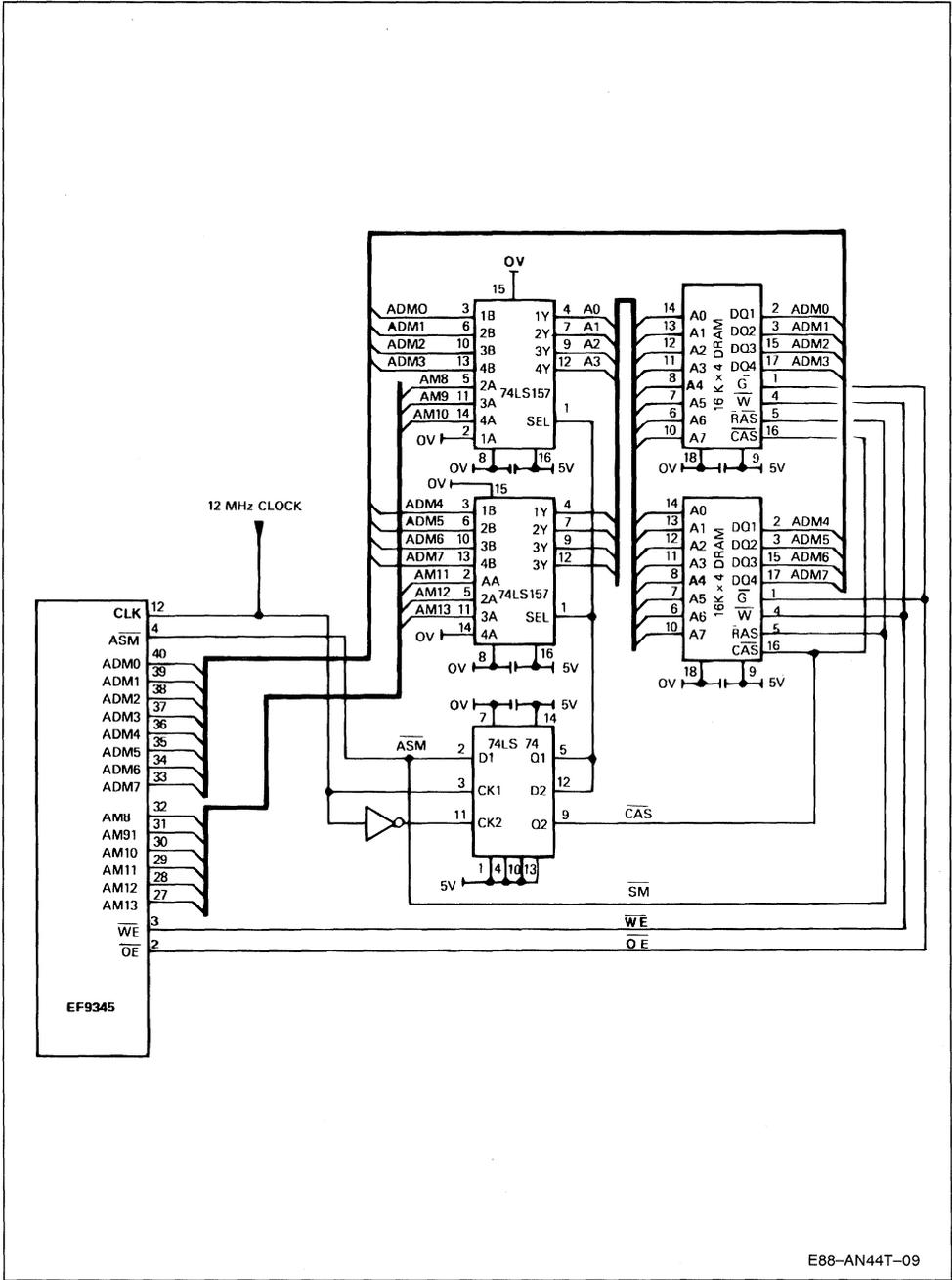
Flowchart of figure 12 gives an example of indirect access register loading.

Figure 8 : EF9345 Interface with 2K x 8 and 8K x 8 Memory.



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**Figure 9 : Interface with 16 x 4 Dram.**



E88-AN44T-09

Figure 10 : Direct Access Registers.

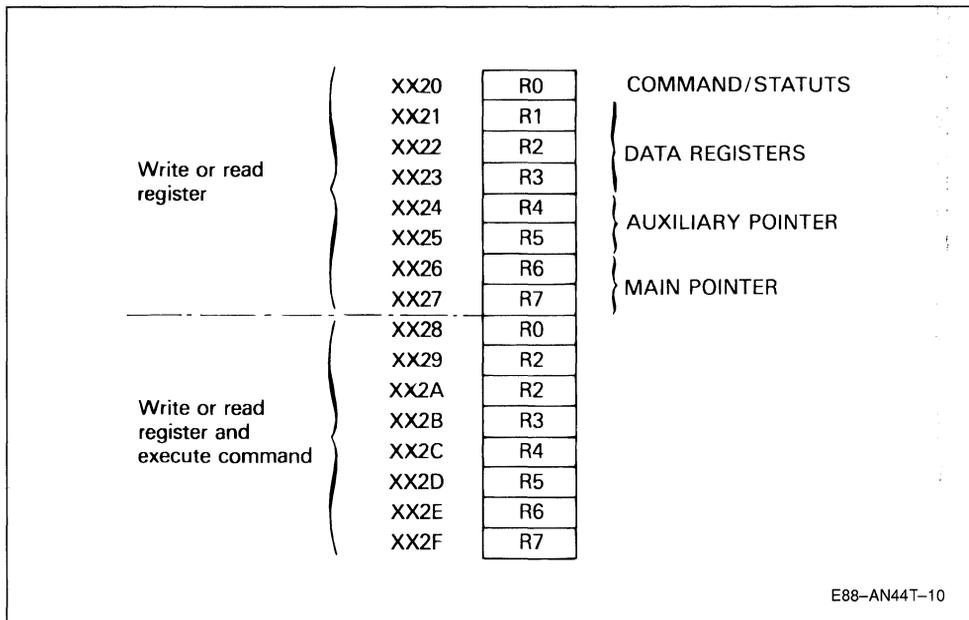
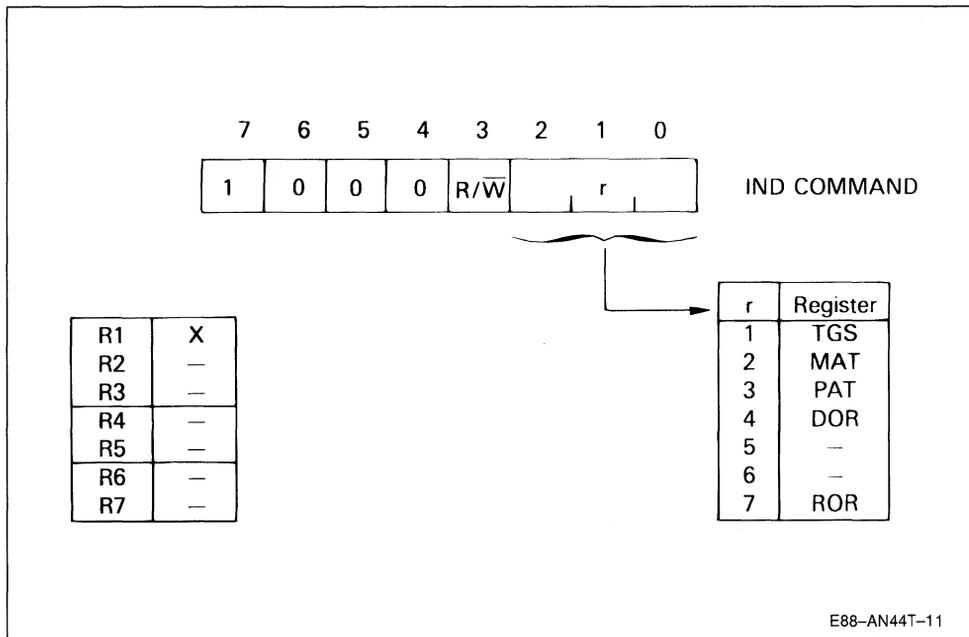
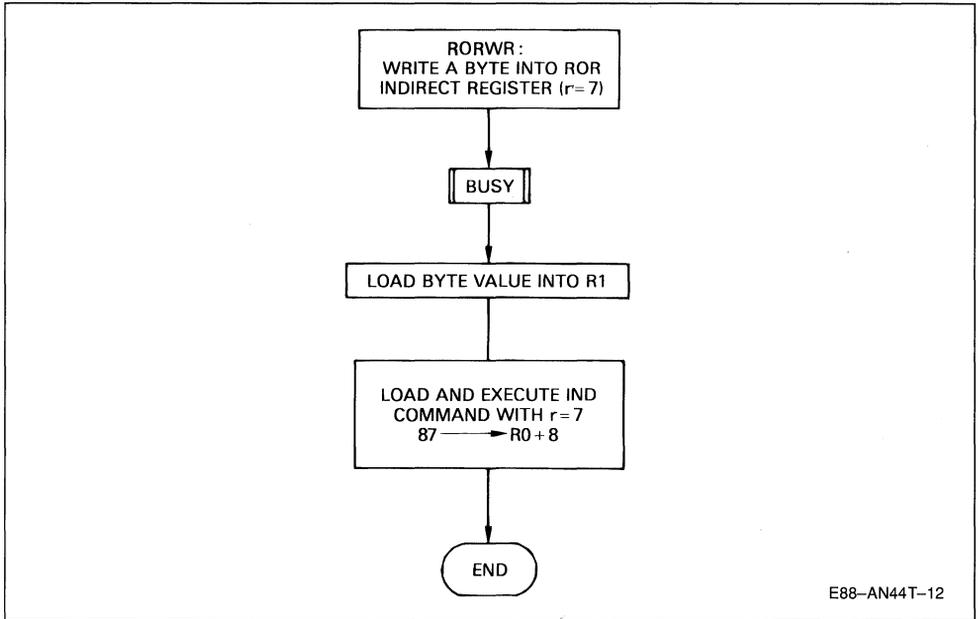


Figure 11 : Indirect Access Registers.



**Figure 12 :** Indirect Register Loading Example.



E88-AN44T-12

**PROGRAMMING THE EF9345 IN 40 CHAR/ROW MODE**

In the char/row mode, a page displayed by the EF9345 is made of 25 or 21 rows, each containing 40 character windows. A window is composed by 8 pixels and 10 lines.

Each window is associated with a character code in a page memory. One of three character code formats can be selected for a page :

- Fixed long codes (24 bits)
- Fixed short codes (16 bits)
- Variable codes (8/24 bits).

In this document, only fixed long code format will be discussed. With this format, each character window on the screen is associated with a 3 byte code, namely the C, B and A bytes. Interpretation of these bytes depends on the character type.

**BICHROME CHARACTER CODE**

For a bichrome character, the A byte defines :

- a background color
- a foreground color

- the negative (reverse video) attribute N
- the flash (blink) attribute F.

The B byte defines :

- a character set
- insert, double height, double width, and conceal attributes.

For bichrome characters, bits B (7:6) must differ from 11.

The C byte selects one of 128 characters in a character set. With the fixed long code format, bit C7 is don't care.

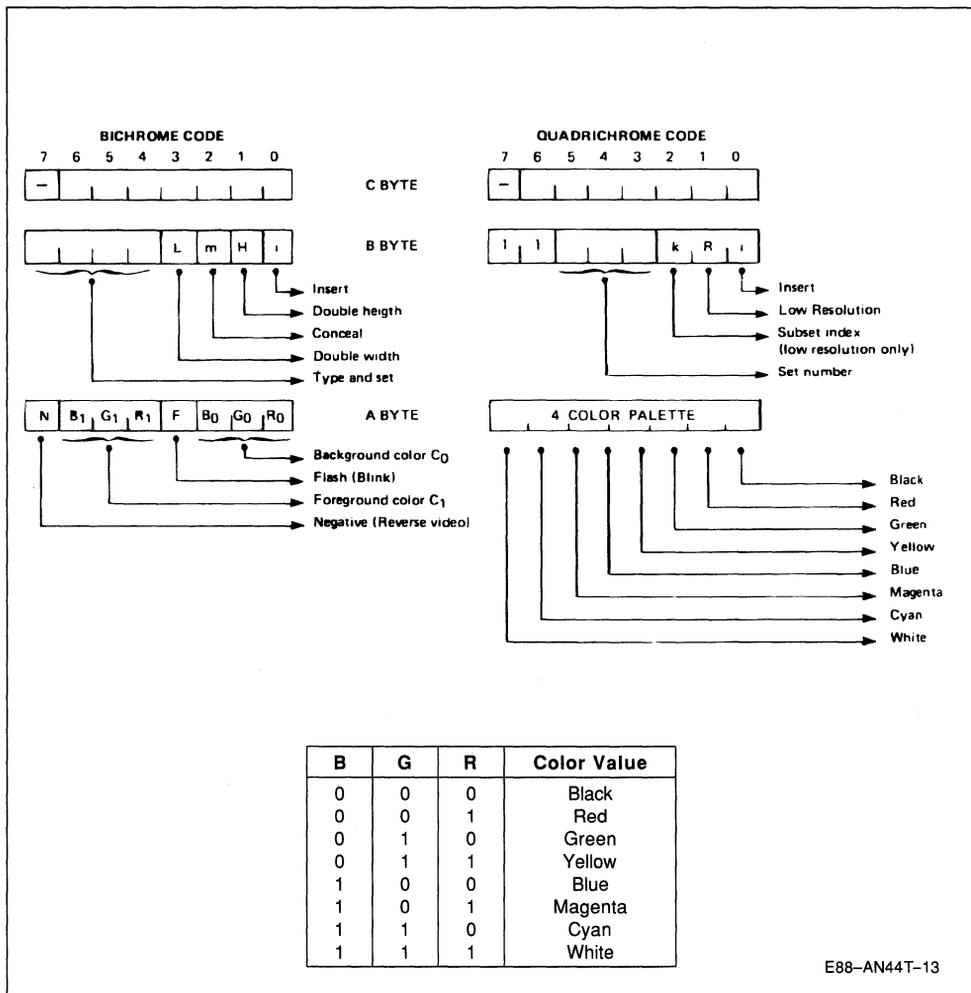
Example : to write a "B" with the following attributes :

- background color = blue
- foreground color = yellow
- flashing
- alphanumeric set G<sub>0</sub>.

The hexadecimal values for the character code bytes are :

- C byte = 42
- B byte = 00
- A byte = 3C.

Figure 13 : 40 Char/Row Fixed Long Codes.



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**QUADRICHROME CHARACTER CODE**

Quadrichrome characters allow displaying up to 4 different colors in any 8 pixels by the 10 lines window, at the penalty of a halved horizontal resolution. By programming the R attribute in the character code B byte, the vertical resolution can be kept or halved.

For each quadrichrome character window, the A byte defines an ordered 4 color palette from 8 possible colors. Each bit is associated with a color which is selected when the corresponding bit is set. If more than 4 bits are set, higher ranking bits are ignored. When less than 4 bits are set, the color palette is implicitly completed with "white" value.

Example : A = 54 selects the red, yellow, blue and cyan colors.

A = 73 selects the black, red, blue and magenta colors. Bit 6 is set but ignored.

The character code B byte defines :

- a set number Q0 to Q7 by bits B (3:5)
- high or low resolution bit R. Bit R = 0 selects a high resolution quadrichrome and bit k is don't care.
- If R = 1, the character is a low resolution quadrichrome and k defines a subset index.
- bit i defines the character to be inserted or not.

The character code C byte selects one from 100 characters in a set. This byte can take values from 00 to 03 and from 20 to 7F (hexa).

**HANDLING LONG CHARACTER CODE**

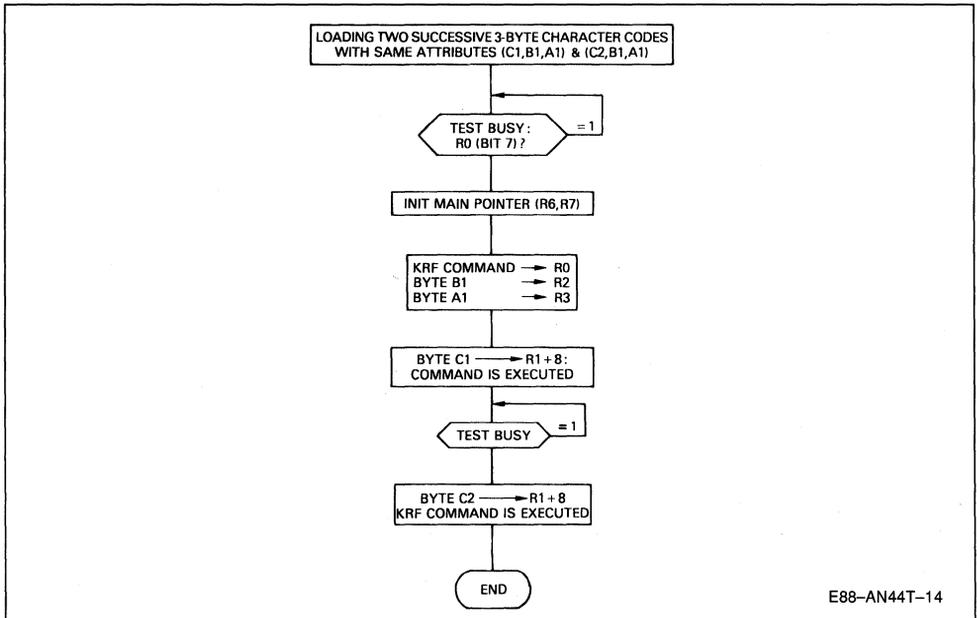
The KRF command allows an easy, X, Y random access or an X sequential access to the page memory. Data registers R1, R2 and R3 are used to transfer respectively the character code C, B and A bytes. The Main Pointer is used to address the page memory and specifies :

- a row number Y = (0 ; 8 to 31)
- a column position on a row X = (0 to 39)
- the first block number of the page memory Z (0:3).

- Notes :**
1. R6(6) is used by the Auxiliary Pointer
  2. Order of bits Z0-Z1 are reversed in R7
  3. When using pointer incrementation in KRF command (bit 0 = 1 in the command code), only the X part of R7 is incremented modulo 40 after the command execution. No Y incrementation is made when X overflows from 39 to 00.
  4. The cursor position on the screen is given by the Main Pointer.

A character code loading flowchart example is given in figure 14.

**Figure 14 : Long Character Code Loading Example.**



E88-AN44T-14

## PAGE MEMORY SELECTION

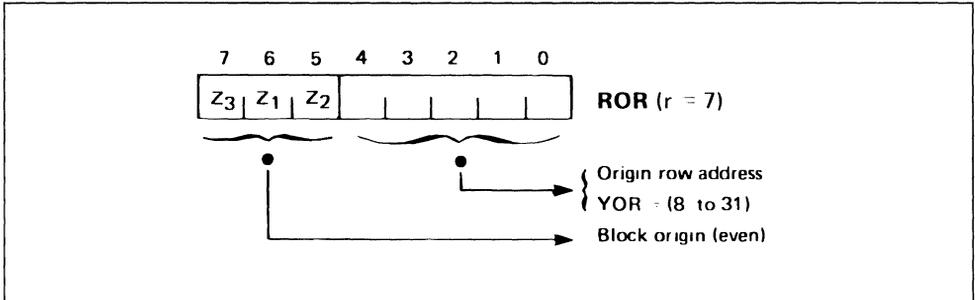
In 40 char/row with the long code format, each character window on the screen is associated with 3 bytes in a page memory. As each displayed page contains up to 1000 windows (25 rows of 40 characters each), a page memory is made of three 1 Kbyte blocks. The first block holds the C bytes, the second one the B bytes and the last one the A bytes.

As the EF9345 can address up to 16 Kbytes of external memory, a page memory address must be

selected by the user with the following requirements :

- the three blocks must be consecutive and lie in the same district, i.e. the two MSB Z3-Z2 of the block numbers must be the same
- the first block number must be even (Z0 = 0).

The base address of the page memory to be displayed on the screen, which is the first block number, is given in register ROR(5:7). As Z0 is implicitly 0, it is not specified in ROR.



Example : with the displayed page memory starting from block number 4, Z3-Z2-Z1-Z0 = 0100 and ROR7-ROR6-ROR5 = 001.

**Notes** : 1. Order of bits Z1-Z2 is reversed in ROR.

2. Each page displayed by the EF9345 comprises a service row, which is always displayed on the top of the screen, and 24 remaining rows. When accessing to the page memory, the service row number is Y = 0 and the remaining row number ranges from 08 to 31. Bits ROR(0:4) constitute the YOR origin register, which specifies the number of the first row displayed after the service row. By programming YOR from 8 to 31, the user can realise roll-up and roll-down operation.

## USER DEFINED CHARACTER SET (UDS)

In 40 char/row mode, the User Defined Character Set (UDS) allows the user to define additional characters whose shapes can be dynamically loaded into the external character generator. The EF9345 can provide up to :

- 100 alphanumeric type UDS character (G<sub>0</sub> set)
- 200 semi-graphic type UDS characters (G<sub>1x</sub> set)
- 800 quadrichrome UDS characters (Q<sub>0</sub> to Q<sub>7</sub> sets).

Alphanumeric and semi-graphic UDS are bichrome characters, with the difference that only alphanumeric can be underlined.

## BICHROME UDS CHARACTERS

The shape of a bichrome character is defined in a 8 pixels by 10 lines dot matrix. Each line of the dot matrix is coded in the external character generator by an 8 bit value, or a slice byte. So a bichrome UDS character is defined by 10 slice bytes.

A slice byte value is obtained in the following way : on a line of the dot matrix, the dots defining the character shape are coded by a "1", the other dots by a "0". This eight bit result is then order reversed to obtain the value to be loaded into the external character generator. Figure 15 shows a slice coding example for a bichrome UDS character.

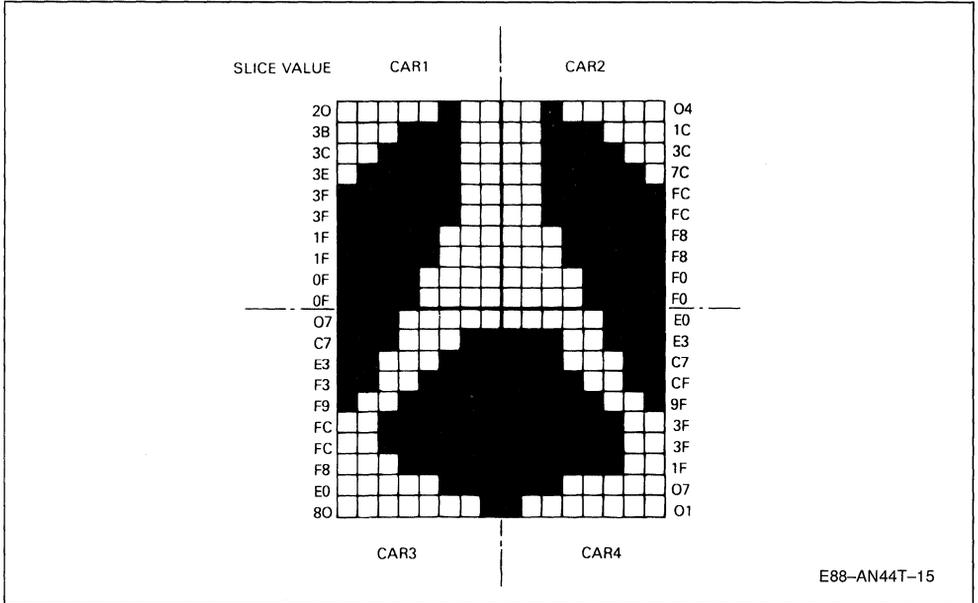
## QUADRICHROME UDS CHARACTERS

An 8 pixels by 10 lines window displaying a quadrichrome character on the screen is composed by elementary "dots" whose size is :

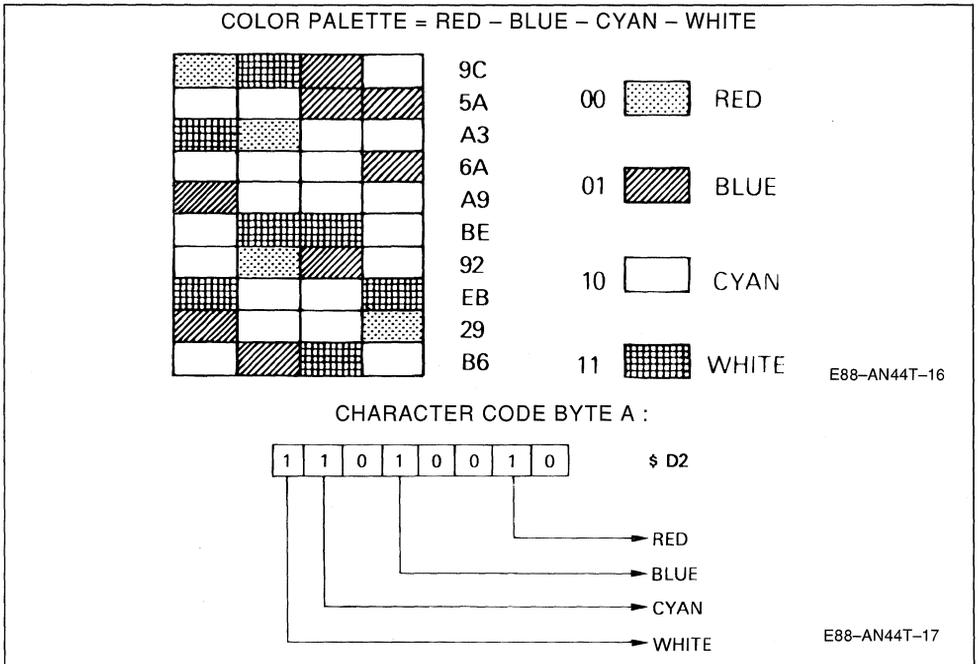
- 2 pixels by 1 line for high resolution quadrichrome
- 2 pixels by 2 lines for low resolution quadrichrome.

Each dot can take one of the 4 colors selected by the palette A byte of the character code associated to the window. So a quadrichrome character shape is defined by a 4 \* 10 or 4 \* 5 dot matrix, with each dot coded bit a two-bit value. Each line of the dot matrix is coded by a slice byte in the external character generator. A high resolution quadrichrome requires 10 slice bytes to be defined, and a low resolution quadrichrome 5 slice bytes.

**Figure 15 : Bichrome UDS Slice Coding Example.**



**Figure 16 : Quadrichrome Slice Coding Example.**



The 4 colors selected by the character code A byte are ordered. For example, if the A byte hexadecimal value is 5A, the 4 ordered colors are :

- Red with the binary rank 00
- Yellow with the binary rank 01
- Blue with the binary rank 10
- Cyan with the binary rank 11.

A slice byte is obtained by assigning to each dot the binary rank of its color, with the value for the right dots placed in the most significant position of the slice byte. Figure 16 shows a slice coding example for a quadrichrome character.

#### DOR REGISTER

During the display process, the base address for each UDS character generator is given in DOR register (see figure 17) :

- DOR(0:3) hold the number of the block which contains the alphanumeric UDS slices (G'0).
- For semi-graphic UDS, the slice block number is given by DOR(4:6) and bit 4 of the character code B byte. So for UDS G'10 the slice block number is even (B4 = 0) and the following block contains slices for UDS G'11 (B4 = 1).
- For each quadrichrome UDS (Q0 to Q7), the slice block number is given by DOR7 and bits B(5:3) of the character code, which select also the set.

#### ACCESS TO UDS SLICES IN MEMORY

A UDS slice address in memory is given by :

- a block number Z(0:3)
- the character code C byte : C(0:6)
- the slice number NT. For bichrome and high resolution quadrichrome, NT ranges from 0 to 9. For low resolution, quadrichrome, NT ranges from 0 to 9. For low resolution quadrichrome, NT ranges from 0 to 4 when K = 0 and from 5 to 9 when k = 1 (k is in bit 2 of character code B byte).

A UDS slice can be written into or read from the EF9345 private memory with the OCT command. This command uses register R1 for slice transfer and the Main or Auxiliary Pointer for slice addressing. As the Main Pointer generally points to the cursor position on the screen and is used for character code access, the Auxiliary Pointer should rather be used for slice access. Figure 18 shows how the Auxiliary Pointer value is obtained from the slice address :

- R4 holds bits C(2:6) of the character code and bit Z2 of the block number
- R5 holds bits C(0:1), the slice number NT and bits Z0-Z1
- Bit 6 of R6 holds bit Z3 of the block number.

Figure 19 shows a flowchart example for loading 10 slices.

**Note :** As the slice number NT is not in the least significant bits of R5, executing the OCT command with pointer incrementation does not result in slice number incrementation.

#### SCREEN MAPPING WITH UDS CHARACTERS

In 40 char/row mode, the screen is made of 1000 windows. Each window can be assigned a UDS character to obtain a likely bit-mapped screen and to produce complex pictures. Up to 300 screen windows can be mapped with a 320 by 250 resolution and independant two color set in each window by bichrome characters. In the same way, quadrichrome characters allow mapping up to 800 (resp. 1600) windows with a 160 \* 250 (resp. 160 \* 125) resolution and with a selectable four color set for each window.

Figure 17 : UDS Fetch to Display.

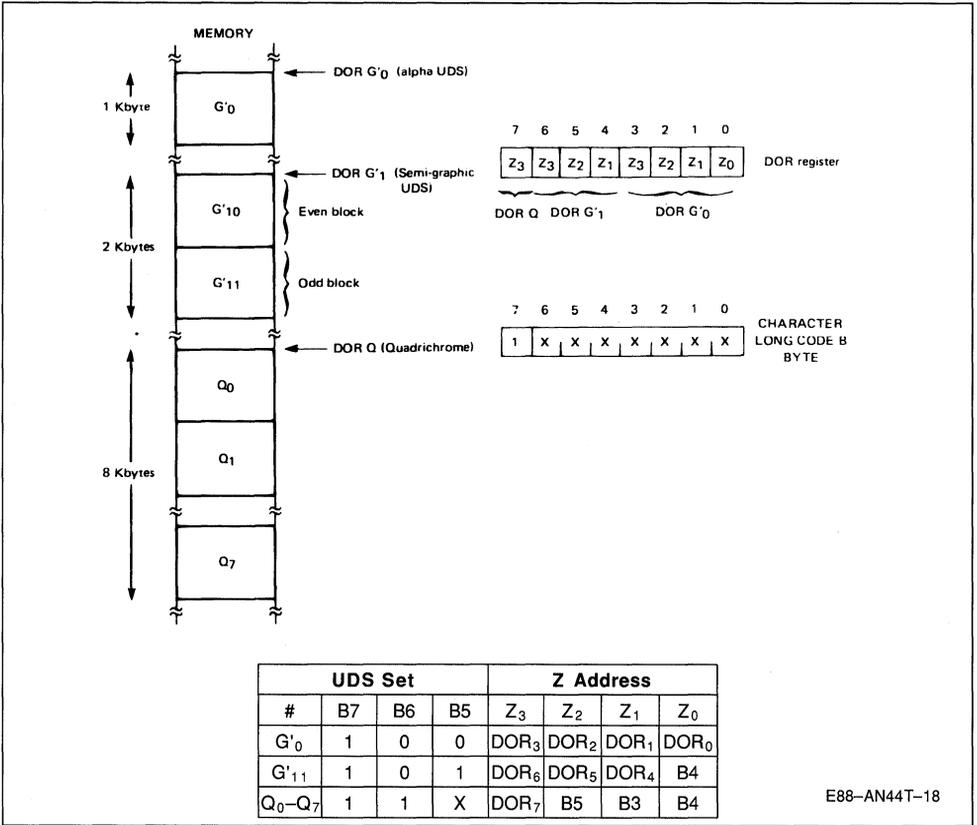


Figure 18 : Accessing a Character Slice in Memory Using Oct Command with Auxiliary Pointer.

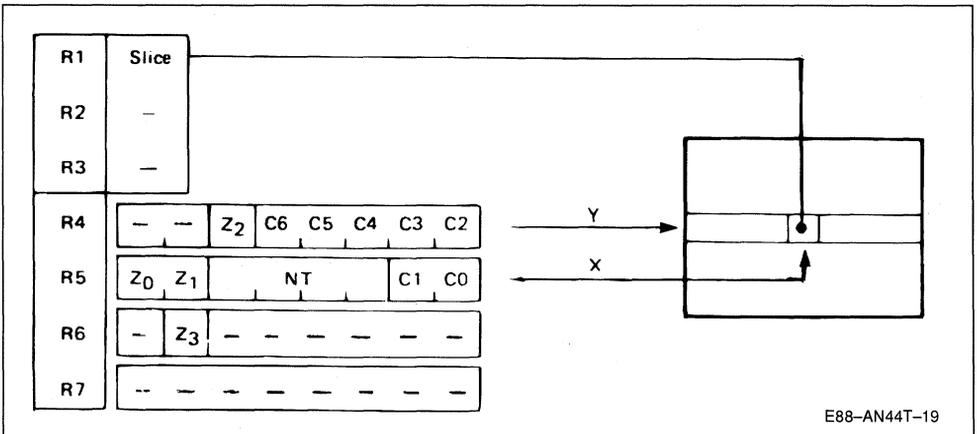
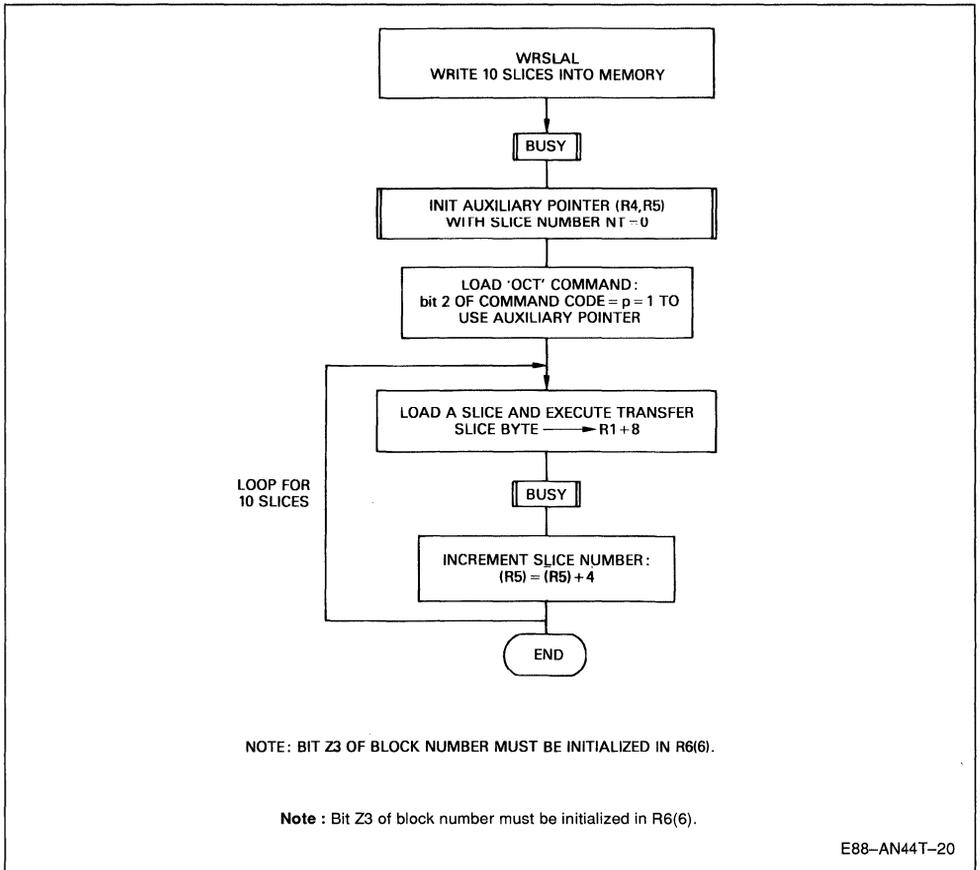


Figure 19 : UDS Slice Loading Flowchart.



## PROGRAMMING EXAMPLE IN 40 CHAR/ROW

```

PAGE 001 EF40 .SA:0

00001          OPT    LLE=110
00002          *
00003          * EF9345 PROGRAMMING EXAMPLE IN 40 CHAR/ROW
00004          * THIS PROGRAM IS WRITTEN IN 6809 ASSEMBLER LANGUAGE.
00005          * AFTER INITIALIAZING THE EF9345 INDIRECT REGISTERS
00006          * AND CLEARING THE SCREEN, THE THOMSON LOGO OF FIGURE 15
00007          * AND THE UDS CHARACTER OF FIGURE 16 ARE DISPLAYED
00008          * ON THE SCREEN.
00009          *

00011          * EF9345 REGISTER ADDRESS

00013          F420  A R0   EQU   $F420  COMMAND/STATUS REGISTER
00014          F421  A R1   EQU   R0+1   DATA REGISTERS
00015          F422  A R2   EQU   R0+2
00016          F423  A R3   EQU   R0+3
00017          F424  A R4   EQU   R0+4   AUXILIARY POINTER (Y)
00018          F425  A R5   EQU   R0+5   AUXILIARY POINTER (X)
00019          F426  A R6   EQU   R0+6   MAIN POINTER (Y)
00020          F427  A R7   EQU   R0+7   MAIN POINTER (X)

00022          F425  A XA   EQU   R5
00023          F424  A YA   EQU   R4
00024          F427  A XP   EQU   R7
00025          F426  A YP   EQU   R6

00027          4000  A STACK EQU   $4000
00028          3F80  A STACKU EQU  STACK-128

00030A 1000          ORG    $1000

00032          1000  A MAIN  EQU   *

00034A 1000 10CE 4000  A     LDS   #STACK  STACK INITIALIZATION
00035A 1004 CE  3F80  A     LDU   #STACKU

00037A 1007 86  91    A     LDA   #$91   LOAD AND EXECUTE A "NOP" COMMAND
00038A 1009 B7  F428  A     STA   R0+8   WITHOUT TESTING BUSY

00040          *
00041          * TGS REGISTER INITIALIZATION :
00042          * TGS0 = 0 : 625 LINES (50 HZ)
00043          * TGS1 = 0 : NOT INTERLACED
00044          * TGS2 = 0 : HORIZONTAL RESYNC. DISABLED
00045          * TGS3 = 0 : VERTICAL RESYNC. DISABLED
00046          * TGS4 = 0 : HORIZONTAL SYNC. ON HVS/HS PIN AND
00047          *          VERTICAL SYNC. ON PC/VS PIN
00048          * TGS5 = 0 : SERVICE ROW Y = 0
00049          * TGS(7:6) = 00 : 40 CHAR/ROW MODE, LONG CHAR CODE (3 BYTES)
00050          *

00052A 100C B0  10DB  A     JSR   BUSY
00053A 100F 86  00    A     LDA   #$00   LOAD VALUE INTO R1
00054A 1011 B7  F421  A     STA   R1
00055A 1014 86  81    A     LDA   #$81   "IND" COMMAND TO LOAD TGS (r=1)
00056A 1016 B7  F428  A     STA   R0+8   LOAD AND EXECUTE COMMAND.

```

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00058          *
00059          * MAT REGISTER INITIALIZATION :
00060          * MAT(2:0) = 100 : MARGIN COLOR = BLUE
00061          * MAT3 = 1 : I SIGNAL IS HIGH DURING MARGIN PERIOD
00062          * MAT(5:4) = 00 : FIXED COMPLEMENTED CURSOR
00063          * MAT6 = 1 : CURSOR DISPLAY ENABLED
00064          * MAT7 = 0 : NO ZOOM MODE
00065          *

00067A 1019 9D 10DB A JSR BUSY
00068A 101C 86 4C A LDA #$4C LOAD VALUE INTO R1
00069A 101E 87 F421 A STA R1
00070A 1021 86 82 A LDA #$82 "IND" COMMAND TO LOAD MAT (r=2)
00071A 1023 B7 F428 A STA R0+8 LOAD AND EXECUTE COMMAND.

00073          *
00074          * PAT REGISTER INITIALIZATION :
00075          * PAT0 = 1 : SERVICE ROW ENABLED
00076          * PAT1 = 1 : UPPER BULK ENABLED
00077          * PAT2 = 1 : LOWER BULK ENABLED
00078          * PAT3 = 1 : CONCEAL ENABLED
00079          * PAT(5:4) = 11 : I SIGNAL IS HIGH DURING THE
00080          * ACTIVE DISPLAYED AREA.
00081          * PAT6 = 1 : FLASHING ENABLED
00082          * PAT7 = 0 : 40 CHAR/ROW MODE, LONG CODE
00083          *

00085A 1026 BD 10DB A JSR BUSY
00086A 1029 86 7F A LDA #$7F LOAD VALUE INTO R1
00087A 102B B7 F421 A STA R1
00088A 102E 86 83 A LDA #$83 "IND" COMMAND TO LOAD PAT (r=3)
00089A 1030 B7 F428 A STA R0+8 LOAD AND EXECUTE COMMAND.

00091          *
00092          * DOR REGISTER INITIALIZATION :
00093          * DOR(3:0) = 0011 : ALPHA UDS SLICES IN BLOCK 3
00094          * DOR(6:4) = 001 : SEMIGRAPHIC UDS SLICES IN BLOCKS 2 AND 3
00095          * DOR 1 = 0 : QUADRICHROME SLICES FROM BLOCK 0
00096          *

00098A 1033 BD 10DB A JSR BUSY
00099A 1036 86 13 A LDA #$13 LOAD VALUE INTO R1
00100A 1038 B7 F421 A STA R1
00101A 103B 86 84 A LDA #$84 "IND" COMMAND TO LOAD DOR (r=4)
00102A 103D B7 F428 A STA R0+8 LOAD AND EXECUTE COMMAND.

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00104          *
00105          * ROR REGISTER INITIALIZATION :
00106          * ROR(4:0) = 01000 : ORIGIN ROW = 8
00107          * ROR(7:5) = 000 : DISPLAYED PAGE MEMORY STARTS FROM BLOCK D
00108          *

00110A 1040 BD 10DB A JSR BUSY
00111A 1043 86 08 A LDA #S08 LOAD VALUE INTO R1
00112A 1045 B7 F421 A STA R1
00113A 1048 86 87 A LDA #S87 "IND" COMMAND TO LOAD ROR (r=7)
00114A 104A B7 F42B A STA R0+8 LOAD AND EXECUTE COMMAND.

00116          *
00117          * CLEAR PAGE MEMORY WITH ALPHANUMERIC SPACES
00118          * FOREGROUND AND BACKGROUND COLORS = BLACK
00119          *
00120A 104D 86 20 A LDA #S20
00121A 104F 8E 0000 A LDX #S0000 CHAR CODE BYTES B & A
00122A 1052 BD 10E1 A JSR MPFILL

00124          * STORE SLICES FOR THE 4 CHARACTERS OF THE THOMSON LOGO.
00125          * CHARACTER CODE C BYTES ARE : $00,$01,$02,$03

00127A 1055 86 03 A LDA #S03 BLOCK NUMBER Z(3:0)
00128A 1057 C6 00 A LDB #S00 INITIAL CHAR CODE C BYTE
00129A 1059 ED C3 A STD ,--U SAVE ACC. A & B INTO U STACK
00130A 105B 8E 1167 A LDX #CAR1 SLICE BUFFER ADDRESS

00132A 105E EC C4 A ET1 LDD 0,U GET ARGUMENTS FOR WRSLAL
00133A 1060 C1 04 A CMPB #S04 SLICES LOADED FOR 4 CHAR ?
00134A 1062 27 07 106B BEQ ET2 YES, BRANCH
00135A 1064 BD 1149 A JSR WRSLAL NO, LOAD TEN SLICES
00136A 1067 6C 41 A INC 1,U INCREMENT CHAR CODE C BYTE
00137A 1069 20 F3 105E BRA ET1

00139A 106B 33 42 A ET2 LEAU 2,U UPDATE U POINTER

00141          * WRITE THE 4 UDS CHAR CODES INTO PAGE MEMORY.
00142          * BACKGROUND = BLACK, FOREGROUND = WHITE : A BYTE = $70

00144A 106D BD 10DB A JSR BUSY
00145A 1070 86 01 A LDA #S01 LOAD "KRF" COMMAND WITH CURSOR INCREM.
00146A 1072 B7 F420 A STA R0 NO EXECUTION !

00148A 1075 86 26 A LDA #S8 INIT MAIN POINTER TO COLUMN 38, ON THE FI
00149A 1077 B7 F427 A STA R7 ROW AFTER SERVICE ROW
00150A 107A 86 08 A LDA #8
00151A 107C B7 F426 A STA R6

```

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00153A 107F 86 80 A LDA #580 STORE CHAR CODE B BYTE INTO R2
00154A 1081 B7 F422 A STA R2
00155A 1084 86 70 A LDA #570 CHAR CODE A BYTE INTO R3
00156A 1086 B7 F423 A STA R3

00158A 1089 86 00 A LDA #500 WRITE THE UPPER LEFT CHAR
00159A 108B B7 F429 A STA R1+8
00160A 108E B0 10DB A JSR BUSY
00161A 1091 4C INCA WRITE THE UPPER RIGHT CHAR
00162A 1092 B7 F429 A STA R1+8
00163A 1095 B0 10DB A JSR BUSY

00165A 1098 86 26 A LDA #38 INIT MAIN POINTER FOR THE 2 LOWER CHAR
00166A 109A B7 F427 A STA R7
00167A 109D 86 09 A LDA #9
00168A 109F B7 F426 A STA R6 Y=9

00170A 10A2 86 02 A LDA #502 WRITE THE 2 LOWER CHAR
00171A 10A4 B7 F429 A STA R1+8
00172A 10A7 B0 10DB A JSR BUSY
00173A 10AA 4C INCA
00174A 10AB B7 F429 A STA R1+8

00176 * LOAD THE 10 SLICES FOR THE QUADRICHROME CHARACTER

00178A 10AE 86 03 A LDA #503 BLOCK NUMBER Z(3:0)
00179A 10B0 C6 48 A LDB #54B CHAR CODE C BYTE
00180A 10B2 8E 118F A LDX #QUADRI SLICE BUFFER ADDRESS
00181A 10B5 B0 1149 A JSR WRSLAL

00183 * WRITE THE QUADRICHROME CHAR CODE INTO PAGE MEMORY
00184 * PALETTE = RED-BLUE-CYAN-WHITE : A BYTE = 5D2
00185 * QUADRICHROME SET Q3, HIGH RESOLUTION (R=0) : B BYTE = 5D8
00186 * C BYTE = 54B

00188A 10B8 B0 10DB A JSR BUSY
00189A 10BB 86 14 A LDA #20 INIT MAIN POINTER : X=20
00190A 10BD B7 F427 A STA R7
00191A 10C0 86 14 A LDA #20 Y=20
00192A 10C2 B7 F426 A STA R6

00194A 10C5 86 01 A LDA #501
00195A 10C7 B7 F420 A STA R0 LOAD "KRF" COMMAND
00196A 10CA 86 48 A LDA #54B LOAD CHAR CODE C BYTE INTO R1
00197A 10CC B7 F421 A STA R1
00198A 10CF 86 D8 A LDA #5D8 CHAR CODE B BYTE INTO R2
00199A 10D1 B7 F422 A STA R2
00200A 10D4 86 D2 A LDA #5D2 CHAR CODE A BYTE INTO R3 AND
00201A 10D6 B7 F42B A STA R3+8 EXECUTE TRANSFER COMMAND

00203A 10D9 20 FE 10D9 HERE BRA HERE

```

# APPLICATION NOTE

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```

00205          *
00206          * BUSY : TEST BUSY STATE IN STATUS REGISTER BIT 7.
00207          *

00209          10DB A BUSY EQU *
00210A 10DB 7D F420 A TST RO
00211A 10DE 2B FB 10DB BMI BUSY LOOP IF BIT 7 = 1
00212A 10E0 39 RTS

00214          *
00215          * MPFILL : FILL THE 3-BLOCK PAGE MEMORY STARTING FROM BLOCK 0
00216          * WITH THE SAME LONG CHARACTER CODE
00217          * ENTRY : THE 1ST BLOCK IS FILLED WITH ACC. A CONTENTS
00218          * THE 2ND BLOCK WITH X REG. (MSB) CONTENTS
00219          * THE 3RD BLOCK WITH X REG. (LSB) CONTENTS.
00220          *

00222          10E1 A MPFILL EQU *

00224A 10E1 BD 10DB A JSR BUSY TEST BUSY STATUS
00225A 10E4 B7 F421 A STA R1 STORE CHAR CODE INTO R1,R2,R3
00226A 10E7 BF F422 A STX R2

00228A 10EA 4F CLRA INIT MAIN POINTER TO THE BEGINNING
00229A 10EB B7 F426 A STA R6 OF THE SERVICE ROW : R6 = R7 = 0.
00230A 10EE B7 F427 A STA R7

00232A 10F1 86 05 A LDA #$05 LOAD AND EXECUTE "CLF" COMMAND
00233A 10F3 B7 F428 A STA RO+8

00235A 10F6 8E 07D0 A LDX #2000
00236A 10F9 30 1F A FILL30 LEAX -1,X WAIT ABOUT 15 MILLISECONDS
00237A 10FB 26 FC 10F9 BNE FILL30

00239A 10FD 86 91 A LDA #$91 EXECUTE A "NOP" COMMAND
00240A 10FF B7 F428 A STA RO+8 TO ABORT "CLF"

00242A 1102 39 RTS

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00244      *
00245      * AXPNT : AUXILIARY POINTER SET SUBROUTINE
00246      * ENTRY : ACC.A = 0-0-0-0-Z3-Z2-Z1-Z0
00247      *          ACC.B = 0-C6-C5-C4-C3-C2-C1-C0, WHERE C(0:6)
00248      *          IS BYTE C OF CHAR. CODE
00249      * EXIT : R4 = YA = 0-0-Z2-C6-C5-C4-C3-C2
00250      *          R5 = XA = Z0-Z1-0-0-0-0-C1-C0
00251      *          R6(6)=YP(6)=Z3
00252      * OPERATION : TEMPORARY STORAGE :
00253      *          M(0,S) = Z0-Z1-0-0-0-0-0-0
00254      *          M(1,S) = 0-0-Z2-0-0-0-0-0
00255      *          M(2,S) = 0-0-0-0-Z3-Z2-Z1-Z0
00256      *          M(3,S) = 0-C6-C5-C4-C3-C2-C1-C0
00257      *
00258      1103  A AXPNT EQU      *

00260A 1103 32 7C  A      LEAS  -4,S  RESERVE 4 BYTE TEMPORARY STORAGE
00261A 1105 ED 62  A      STD    2,S  SAVE ARGUMENT A & B.

00263A 1107 5F          CLR B
00264A 1108 46          RORA
00265A 1109 46          RORA
00266A 110A 46          RORA      CY=Z2,A7=Z1,A6=Z0.
00267A 110B 56          RORB      B7=Z2
00268A 110C 49          ROLA
00269A 110D 56          RORB      B7=Z1,B6=Z2
00270A 110E 49          ROLA
00271A 110F 56          RORB      B7=Z0,B6=Z1,B5=Z2
00272A 1110 1F 98  A      TFR    B,A  DUPLICATE RESULT INTO ACC.A

00274A 1112 C4 20  A      ANDB  #$20  B = 0-0-Z2-0-0-0-0-0
00275A 1114 84 C0  A      ANDA  #$C0  A = Z0-Z1-0-0-0-0-0-0
00276A 1116 ED E4  A      STD    0,S  SAVE A & B

00278A 1118 BD 10DB A      JSR   BUSY
00279A 111B E6 63  A      LDB   3,S  RESTORE INITIAL ARGUMENT
00280A 111D C4 03  A      ANDB  #$03  KEEP ONLY THE 2 LSB
00281A 111F EA E4  A      ORB   0,S  B = Z0-Z1-0-0-0-0-C1-C0
00282A 1121 F7 F425 A      STB   R5  STORE INTO R5=XA
00283A 1124 E6 63  A      LDB   3,S
00284A 1126 54          LSRB
00285A 1127 54          LSRB      B = 0-0-0-C6-C5-C4-C3-C2
00286A 1128 EA 61  A      ORB   1,S  B = 0-0-Z2-C6-C5-C4-C3-C2
00287A 112A F7 F424 A      STB   R4  STORE INTO R4 = YA

```

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```

00289A 112D A6 62 A LDA 2,S RESTORE Z3-Z0 ARGUMENT
00290A 112F 84 08 A ANDA #S08 TEST Z3
00291A 1131 27 08 113E BEQ AXPNT5
00292A 1133 B6 F426 A LDA YP Z3=1 : YP(6)=1.
00293A 1136 8A 40 A ORA #S40
00294A 1138 B7 F426 A STA YP

00296A 113B 32 64 A LEAS 4,S UPDATE STACK POINTER
00297A 113D 39 RTS

00299A 113E B6 F426 A AXPNT5 LDA YP Z3=0 : YP(6)=0.
00300A 1141 84 BF A ANDA #S8F
00301A 1143 B7 F426 A STA YP

00303A 1146 32 64 A LEAS 4,S UPDATE STACK POINTER
00304A 1148 39 RTS
00305 *
00306 * WRSLAL : WRITE 10 UDS SLICES.
00307 * ENTRY : ACC.A = 0-0-0-0-Z3-Z2-Z1-Z0, WHERE Z(3:0) IS
00308 * BASE ADDRESS FOR UDS SLICES.
00309 * ACC.B = 0-C6-C5-C4-C3-C2-C1-C0, WHERE C(0:6) IS
00310 * BYTE C OF CHAR CODE
00311 * X POINTS TO THE SLICE BUFFER.
00312 * EXIT : A & B DESTROYED
00313 * X = X + 10.
00314 *
00315 * AUXILIARY POINTER IS USED : BIT 2 = p OF
00316 * "BYTE LOAD" COMMAND =1

00318A 1149 BD 1103 A WRSLAL JSR AXPNT SET AUXILIARY POINTER.

00320A 114C 86 34 A LDA #S34 "BYTE WRITE COMMAND "
00321A 114E B7 F420 A STA RO STORE COMMAND WITHOUT EXEC.
00322A 1151 C6 0A A LDB #10 INIT LOOP COUNTER FOR 10 SLICES.

00324A 1153 A6 80 A WRSLA1 LDA 0,X+ STORE A SLICE AND EXECUTE
00325A 1155 B7 F429 A STA R1+8 TRANSFER INTO MEMORY
00326A 1158 BD 10DB A JSR BUSY

00328A 115B 86 04 A LDA #S04 INC. SLICE COUNTER = R5(5:2)
00329A 115D BB F425 A ADDA R5
00330A 1160 B7 F425 A STA R5

00332A 1163 5A DEC B DEC. LOOP COUNTER
00333A 1164 26 ED 1153 BNE WRSLA1

00335A 1166 39 RTS

```

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00337          *
00338          * SLICE VALUES FOR UDS CHARACTERS OF FIGURE 15
00339          *
00340A 1167    20    A CAR1  FCB    $20,$38,$3C,$3E,$3F,$3F,$1F,$1F,$0F,$0F
00341A 1171    04    A CAR2  FCB    $04,$1C,$3C,$7C,$FC,$FC,$F8,$F8,$F0,$F0
00342A 117B    07    A CAR3  FCB    $07,$C7,$E3,$F3,$F9,$FC,$FC,$F8,$E0,$80
00343A 1185    E0    A CAR4  FCB    $E0,$E3,$C7,$CF,$9F,$3F,$3F,$1F,$07,$01
00344          *
00345          * SLICE VALUES FOR QUADRICHROME CHARACTER (FIGURE 16)
00346          *
00347A 118F    9C    A QUADRI FCB    $9C,$5A,$A3,$6A,$A9,$BE,$92,$EB,$29,$B6

00349          END
TOTAL ERRORS 00000--00000
TOTAL WARNINGS 00000--00000

```

## PROGRAMMING THE EF9345 IN 80 CHAR/ROW MODE

### CHARACTER CODE (figures 20 and 21)

In 80 char/row mode, the screen is made of 25 or 21 rows of 80 characters.

Each character is displayed in a 6 pixels by 10 lines window, which is associated with a character code in a page memory.

For a page, one of two character code formats must be selected :

- Long codes (12 bits), which consist of a C byte and an attribute A nibble.
- Short codes (8 bits), which consist of only a C byte (see figure 20).

With short codes, the C byte selects one of the 128 internal alphanumeric characters (G<sub>0</sub> set), and characters are displayed without attributes.

Long code format provides an additional 1024 mosaic character set and four attributes : D (color select), N (negative), U (underline) and F (flash). For each character, the foreground/background colors and the insert attribute are selected by bits D and N from the values programmed in DOR and MAT registers.

### PAGE MEMORY

With long character code format, a page memory consists of three 1 Kbyte blocks. The same rules as in 40 char/row mode apply to page memory selection. The first (resp. second) block holds the C bytes of the characters in even (resp. odd) position on the rows. Every two consecutive characters have their A nibble concatenated to make a byte stored in the third block.

Short character codes are similarly packed in two consecutive blocks which hold only C bytes.

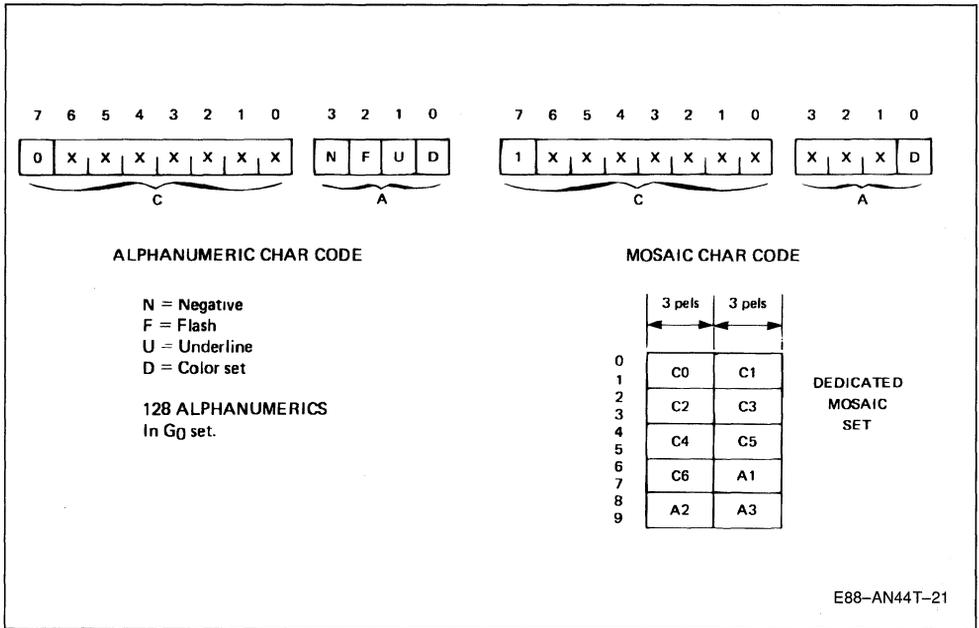
### ACCESS TO CHARACTER CODE

KRL command performs long character code transfer between registers R1-R3 and the memory. R1 is used for C byte transfer and R3 for A nibble transfer. When loading a character code, the A nibble must be repeated in R3.

KRC command is similarly used for short character code access between R1 and the memory.

Both KRL and KRC commands use the Main Pointer (R6, R7) for memory addressing. With a page memory starting from block number Z(0:3), R6 holds the Y row number and Z3-Z2. As the character position on a row is given by X(0:5) and Z0, it must be transcoded to obtain the R7 value with Z0-Z1 in the most significant bits (see figure 22).

**Figure 20 : 80 Char/Row Character Code.**



**Figure 21 : Color Selection.**

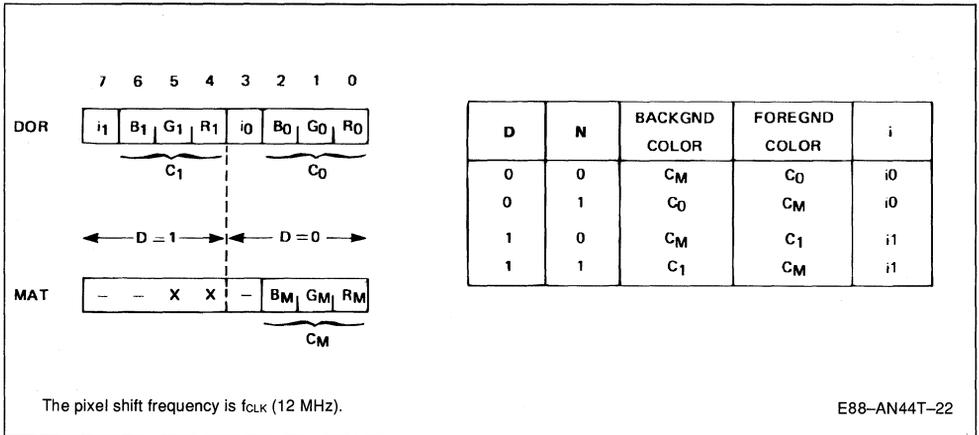
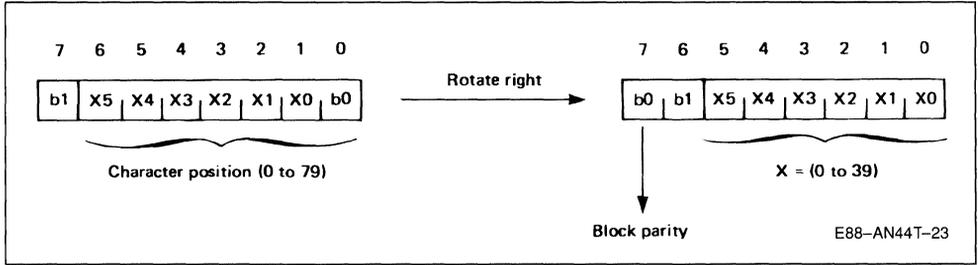


Figure 22 : Transcoding an Horizontal Screen Location into a R7 Pointer.



## PROGRAMMING THE EF9345 IN 80 CHAR/ROW MODE

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00001          OPT    LLE=110

00003          *
00004          * EF9345 PROGRAMMING EXAMPLE IN 80 CHAR/ROW
00005          * THIS PROGRAM IS WRITTEN IN 6809 ASSEMBLER LANGUAGE.
00006          * AFTER INDIRECT REGISTERS INITIALIZATION, TWO
00007          * CHARACTER STRINGS ARE DISPLAYED AND A ROLL-UP
00008          * OPERATION IS MADE.
00009          *

00011          * EF9345 REGISTER ADDRESS

00013          F420    A R0    EQU    $F420    COMMAND/STATUS REGISTER
00014          F421    A R1    EQU    R0+1     DATA REGISTERS
00015          F422    A R2    EQU    R0+2
00016          F423    A R3    EQU    R0+3
00017          F424    A R4    EQU    R0+4     AUXILIARY POINTER (Y)
00018          F425    A R5    EQU    R0+5     AUXILIARY POINTER (X)
00019          F426    A R6    EQU    R0+6     MAIN POINTER (Y)
00020          F427    A R7    EQU    R0+7     MAIN POINTER (X)

00022          F425    A XA    EQU    R5
00023          F424    A YA    EQU    R4
00024          F427    A XP    EQU    R7
00025          F426    A YP    EQU    R6

00027          4000    A STACK EQU    $4000
00028          3F80    A STACKU EQU    STACK-128

00030A 1000          ORG    $1000

00032          1000    A MAIN    EQU    *

00034A 1000 10CE 4000 A      LDS    #STACK  STACK INITIALIZATION
00035A 1004 CE 3F80 A      LDU    #STACKU

00037A 1007 86 91  A      LDA    #S91   LOAD AND EXECUTE A "NOP" COMMAND
00038A 1009 87 F428 A      STA    R0+8   WITHOUT TESTING BUSY

00040          *
00041          * TGS REGISTER INITIALIZATION :
00042          * TGS0 = 0 : 625 LINES (50 HZ)
00043          * TGS1 = 0 : NOT INTERLACED
00044          * TGS2 = 0 : HORIZONTAL RESYNC. DISABLED
00045          * TGS3 = 0 : VERTICAL RESYNC. DISABLED
00046          * TGS4 = 0 : HORIZONTAL SYNC. ON HVS/HS PIN AND
00047          * VERTICAL SYNC. ON PC/VS PIN
00048          * TGS5 = 0 : SERVICE ROW Y = 0
00049          * TGS(7:6) = 11 : 80 CHAR/ROW MODE, LONG CHAR CODE (12 BITS)
00050          *

00052A 100C 8D 10D2 A      JSR    BUSY
00053A 100F 86 C0  A      LDA    #C0    LOAD VALUE INTO R1
00054A 1011 87 F421 A      STA    R1
00055A 1014 86 81  A      LDA    #S81   "IND" COMMAND TO LOAD TGS (r=1)
00056A 1016 87 F428 A      STA    R0+8   LOAD AND EXECUTE COMMAND.

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00058      *
00059      * MAT REGISTER INITIALIZATION :
00060      * MAT(2:0) = 100 : MARGIN COLOR = BLUE
00061      * MAT3 = 1 : I SIGNAL IS HIGH DURING MARGIN PERIOD
00062      * MAT(5:4) = 00 : FIXED COMPLEMENTED CURSOR
00063      * MAT6 = 1 : CURSOR DISPLAY ENABLED
00064      * MAT7 = 0 : NO ZOOM MODE
00065      *

00067A 1019 BD 10D2 A JSR BUSY
00068A 101C 86 4C A LDA #$4C LOAD VALUE INTO R1
00069A 101E B7 F421 A STA R1
00070A 1021 86 82 A LDA #$82 "IND" COMMAND TO LOAD MAT (r=2)
00071A 1023 B7 F428 A STA R0+8 LOAD AND EXECUTE COMMAND.

00073      *
00074      * PAT REGISTER INITIALIZATION :
00075      * PAT0 = 1 : SERVICE ROW ENABLED
00076      * PAT1 = 1 : UPPER BULK ENABLED
00077      * PAT2 = 1 : LOWER BULK ENABLED
00078      * PAT3 = 1 : CONCEAL ENABLED
00079      * PAT(5:4) = 11 : I SIGNAL IS HIGH DURING THE
00080      * ACTIVE DISPLAYED AREA.
00081      * PAT6 = 1 : FLASHING ENABLED
00082      * PAT7 = 0 : 80 CHAR/ROW MODE, LONG CODE
00083      *

00085A 1026 BD 10D2 A JSR BUSY
00086A 1029 86 7F A LDA #$7F LOAD VALUE INTO R1
00087A 102B B7 F421 A STA R1
00088A 102E 86 83 A LDA #$83 "IND" COMMAND TO LOAD PAT (r=3)
00089A 1030 B7 F428 A STA R0+8 LOAD AND EXECUTE COMMAND.

00091      *
00092      * DOR REGISTER INITIALIZATION :
00093      * DOR(3:0) = 1111 : COLOR C0 = WHITE
00094      * DOR(7:4) = 1000 : COLOR C1 = BLACK
00095      * INSERT ATTRIBUTE i IS SET FOR ANY CHARACTER.
00096      *

00098A 1033 BD 10D2 A JSR BUSY
00099A 1036 86 8F A LDA #$8F LOAD VALUE INTO R1
00100A 1038 B7 F421 A STA R1
00101A 103B 86 84 A LDA #$84 "IND" COMMAND TO LOAD DOR (r=4)
00102A 103D B7 F428 A STA R0+8 LOAD AND EXECUTE COMMAND.

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00104          *
00105          * ROR REGISTER INITIALIZATION :
00106          * ROR(4:0) = 01000 : ORIGIN ROW = 8
00107          * ROR(7:5) = 001 : DISPLAYED PAGE MEMORY STARTS FROM BLOCK 0
00108          *

00110A 1040 BD 10D2 A JSR BUSY
00111A 1043 86 28 A LDA #S28 LOAD VALUE INTO R1
00112A 1045 87 F421 A STA R1
00113A 1048 86 87 A LDA #S87 "IND" COMMAND TO LOAD ROR (r=7)
00114A 104A 87 F428 A STA R0+8 LOAD AND EXECUTE COMMAND.

00116          *
00117          * CLEAR PAGE MEMORY WITH ALPHANUMERIC SPACES
00118          * BACKGROUND COLOR = CM (MARGIN COLOR)
00119          *

00120A 104D 86 20 A LDA #S20 C BYTE FOR EVEN POSITION CHAR.
00121A 104F 8E 2000 A LDX #S2000 C BYTE FOR ODD POSITION AND A NIBBLES
00122A 1052 C6 04 A LDB #4 PAGE MEMORY FIRST BLOCK NUMBER
00123A 1054 BD 10D8 A JSR MPFILL

00125          * WRITE "ABCD..." WITH FLASH AND NEGATIVE ATTRIBUTES
00126          * ATTRIBUTE BITS (D,N)=01 :
00127          * BACKGROUND COLOR = C0 DEFINED IN DOR
00128          * FOREGROUND COLOR = CM (MARGIN COLOR)

00130A 1057 BD 10D2 A JSR BUSY
00131A 105A 86 51 A LDA #S51 LOAD "KRL" COMMAND WITH
00132A 105C 87 F420 A STA R0 CURSOR INCREMENTATION

00134A 105F 86 28 A LDA #S28 INIT MAIN POINTER (CURSOR)
00135A 1061 87 F426 A STA R6
00136A 1064 86 00 A LDA #S00
00137A 1066 87 F427 A STA R7

00139A 1069 86 CC A LDA #S$C LOAD ATTRIBUTE NIBBLE (REPEATED
00140A 106B 87 F423 A STA R3 INTO R3).

00142A 106E C6 0A A LDB #10 LOOP COUNTER FOR 10 CHARACTERS
00143A 1070 86 41 A LDA #'A FIRST CHAR CODE C BYTE

00145A 1072 B7 F429 A LOOP STA R1+8 STORE C.C. C BYTE AND EXEC COMMAND
00146A 1075 4C INCA INCREMENT C BYTE
00147A 1076 BD 10D2 A JSR BUSY
00148A 1079 5A DECB DEC LOOP COUNTER
00149A 107A 26 F6 1072 A BNE LOOP

```

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00151 \* WRITE "KLM...." WITH UNDERLINING  
 00152 \* (D,N) = (0,0) : BACKGROUND COLOR = CM  
 00153 \* FOREGROUND COLOR = CO

00155A 107C 86 2A A LDA #S2A INIT CURSOR  
 00156A 107E 87 F426 A STA R6  
 00157A 1081 86 00 A LDA #S00  
 00158A 1083 87 F427 A STA R7

00160A 1086 86 22 A LDA #S22 ATTRIBUTE NIBBLE INTO R3  
 00161A 1088 87 F423 A STA R3

00163A 108B C6 0A A LDB #10  
 00164A 108D 86 4B A LDA #'K

00166A 108F 87 F429 A LOOP1 STA R1+8  
 00167A 1092 4C INCA  
 00168A 1093 8D 10D2 A JSR BUSY  
 00169A 1096 5A DECB  
 00170A 1097 26 F6 108F BNE LOOP1

00172 \* ROLL-UP OPERATION EXAMPLE

00174A 1099 8D 10D2 A JSR BUSY

00176A 109C 86 8F A LDA #S8F EXECUTE "IND" COMMAND TO READ ROR REGISTE  
 00177A 109E 87 F428 A STA R0+8

00179A 10A1 8D 10D2 A JSR BUSY COMMAND EXECUTED?  
 00180A 10A4 86 F421 A LDA R1 READ RESULT FROM R1

00182A 10A7 C6 87 A LDB #S87 STORE "IND" COMMAND FOR LOADING ROR  
 00183A 10A9 F7 F420 A STB R0

00185 10AC A LOOP3 EQU \*

00187A 10AC 87 F429 A STA R1+8 STORE VALUE TO BE LOADED INTO ROR

00188A 10AF 8D 10D2 A JSR BUSY

00189A 10B2 8D 10C6 A JSR WAIT TEMPO

00190A 10B5 4C INCA

00191A 10B6 34 02 A PSHS A

00192A 10B8 84 1F A ANDA #S1F YOR = ROR(4:0) = 31 ?

00193A 10BA 81 1F A CMPA #31

00194A 10BC 35 02 A PULS A

00195A 10BE 26 EC 10AC BNE LOOP3

00197A 10CD 84 E0 A ANDA #SE0 IF YOR=31, SET YOR=8

00198A 10C2 8B 08 A ADDA #8

00199A 10C4 20 E6 10AC BRA LOOP3

00201 10C6 A WAIT EQU \*

00202A 10C6 34 10 A PSHS X

00203A 10C8 8E FFFF A WAIT1 LDX #SFFFF

00204A 10CB 30 1F A WAIT2 LEAX -1,X

00205A 10CD 26 FC 10CB BNE WAIT2

00206A 10CF 35 10 A PULS X

00207A 10D1 39 RTS

APPLICATION NOTE

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00209          *
00210          * BUSY : TEST BUSY IN STATUS REGISTER RO(7)
00211          *

00213          10D2  A  BUSY  EQU  *
00214A 10D2 7D  F420  A      TST  RO
00215A 10D5 2B  FB   10D2      BMI  BUSY    LOOP IF BIT 7 = 1
00216A 10D7 39                RTS

00218          *
00219          * MPFILL : FILL THE 3-BLOCK PAGE MEMORY STARTING FROM BLOCK 0
00220          *           WITH THE SAME LONG CHARACTER CODE
00221          *           ENTRY : THE 1ST BLOCK IS FILLED WITH ACC. A CONTENTS
00222          *           THE 2ND BLOCK WITH X REG. (MSB) CONTENTS
00223          *           THE 3RD BLOCK WITH X REG. (LSB) CONTENTS.
00224          *

00226          10D8  A  MPFILL EQU  *

00228A 10D8 BD  10D2  A      JSR  BUSY    TEST BUSY STATUS
00229A 10D8 B7  F421  A      STA  R1      STORE CHAR CODE INTO R1,R2,R3
00230A 10DE BF  F422  A      STX  R2

00232A 10E1 4F                CLRA      INIT MAIN POINTER TO THE BEGINNING
00233A 10E2 B7  F426  A      STA  R6      OF THE SERVICE ROW : R6 = R7 = 0.
00234A 10E5 B7  F427  A      STA  R7

00236A 10E8 86  05   A      LDA  #05     LOAD AND EXECUTE "CLF" COMMAND
00237A 10EA B7  F428  A      STA  R0+8

00239A 10ED 8E  07D0 A      LDX  #2000
00240A 10F0 30  1F   A  FILL30 LEAX  -1,X    WAIT ABOUT 15 MILLISECONDS
00241A 10F2 26  FC   10F0 BNE  FILL30

00243A 10F4 86  91   A      LDA  #91     EXECUTE A "NOP" COMMAND
00244A 10F6 B7  F428  A      STA  R0+8    TO ABORT "CLF"

00246A 10F9 39                RTS

00248          END

TOTAL ERRORS 00000--00000
TOTAL WARNINGS 00000--00000
    
```

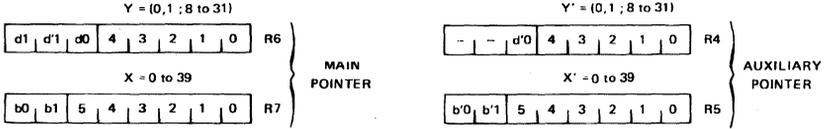
**COMMAND TABLE**

Type	Memo	Code				Parameter				Status			Arguments							Execution Time (1)		
		7	6	5	4	3	2	1	0	AI	LX <sub>m</sub>	LX <sub>r</sub>	R1 <sub>7</sub>	R1	R2	R3	R4	R5	R6	R7	Write	Read
Indirect	IND	1	0	0	0	R/W	-	r	-	0	0	0	0	D	-	-	-	-	MP	2	3.5	
40 Characters - 24 Bits	KRF	0	0	0	0	R/W	0	0	1	X	X	0	0	C	B	A	-	-	MP	4	7.5	
40 Characters - 16 Bits	KRG	0	0	0	0	R/W	0	1	1	X	X	0	0	A*	B*	W	-	-	MP	5.5	7.5	
80 Characters - 8 Bits	KRC	0	1	0	0	R/W	0	0	1	X	X	0	0	C	-	-	-	-	MP	9	9.5	
80 Characters - 12 Bits	KRL	0	1	0	1	R/W	0	0	1	X	X	0	0	C	-	A	-	-	MP	12.5	11.5	
40 Characters Variable	KRV	0	0	1	0	R/W	0	0	1	X	X	X	X	C	B	A	-	XF	MP	(2) 3 + 3 + j	3.5 + 6 * j	
Expansion	EXP	0	1	1	0	0	0	0	0	X	0	X	0	C	B	A	PW	XF	MP	(3) < 247	-	
Compression	CMP	0	1	1	1	0	0	0	0	X	0	X	0	C	B	A	PW	XF	MP	(3) < 402	-	
Expanded Characters	KRE	0	0	0	1	R/W	0	0	1	X	X	0	0	C	B	A	PW	-	MP	4	7.5	
Byte	OCT	0	0	1	1	R/W	p	0	1	X	X	X	0	D	-	-	AP	MP	4	4.5		
Move Buffer	MVB	1	1	0	1	s	ā	ā	a	0	0	0	0	W	-	-	AP	MP	(2) 2 + 4.n	-		
Move Double Buffer	MVD	1	1	1	0	s	ā	ā	a	0	0	0	0	W	-	-	AP	MP	(2) 2 + 8.n	-		
Move Triple Buffer	MVT	1	1	1	1	s	ā	ā	a	0	0	0	0	W	-	-	AP	MP	(2) 2 + 12.n	-		
Clear Page (4) - 24 Bits	CLF	0	0	0	0	0	1	0	1	X	X	0	0	C	B	A	-	-	MP	< 4700 (1 K code)	-	
Clear Page (4) - 16 Bits	CLG	0	0	0	0	0	1	1	1	X	X	0	0	A*	B*	W	-	-	MP	< 5800 (1 K code)	-	
Vertical Sync Mask Set	VSM	1	0	0	1	1	0	0	1	0	0	0	0	-	-	-	-	-	-	1	-	
Vertical Sync Mask Reset	VRM	1	0	0	1	0	1	0	1	-	-	-	-	-	-	-	-	-	-	1	-	
Increment Y	INY	1	0	1	1	0	0	0	0	0	0	0	0	-	-	-	-	-	Y	-	TBD	-
No Operation	NOP	1	0	0	1	0	0	0	1	-	-	-	-	-	-	-	-	-	-	1	-	

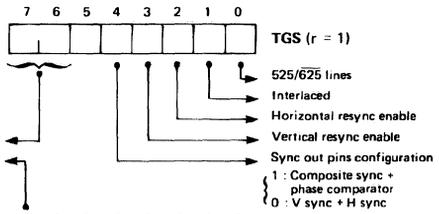
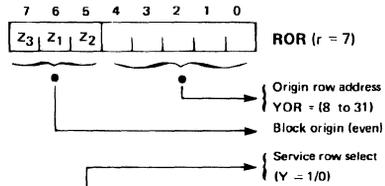
p : Pointer Select  
     1 : Auxiliary Pointer  
     0 : Main Pointer.  
 - :  
 s.s : Source Destination  
     01 : Source = MP ; Destination = AP  
     10 : Source = AP ; Destination = mP  
 - :  
 ā.a : Stop Condition  
     01 : Stop at End of Buffer  
     10 : No Stop  
 r : Indirect Register Number  
 - : Not Affected  
 W : Used as Working Register  
 PW (ZW, YW) : Working Buffer  
 X : Set or Reset  
 XF : X File  
 I : Pointer Incrementation  
 D : Data  
 MP : Main Pointer  
 AP : Auxiliary Pointer.

- (1) Unit : 12 clock periods (= 1 μs) without possible suspension.
- (2) n : total number of words ≤ 40 ; j = 1 for long codes, j = 0 for short codes.
- (3) Worst case (20 long codes + 20 short codes).
- (4) These commands repeat KRF or KRG with Y incrementation when X overflows. When the last position is reached in a row, Y is incremented and the process starts again on the next row. These commands stop only with abort.

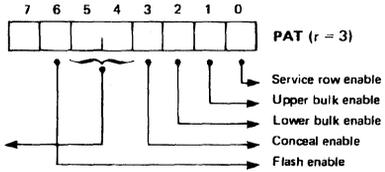
POINTERS



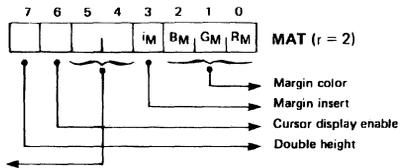
INDIRECT REGISTERS



CHAR CODE	PAT <sub>7</sub>	TGS <sub>7</sub>	TGS <sub>6</sub>
40 CHAR LONG	0	0	0
40 CHAR VAR	0	0	1
40 CHAR SHORT	1	0	0
80 CHAR LONG	0	1	1
80 CHAR SHORT	0	1	0



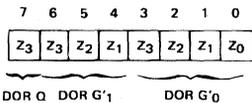
INSERT MODE	PAT <sub>5</sub>	PAT <sub>4</sub>
INLAY	0	0
BOXING	0	1
CHARACTER MARK	1	0
ACTIVE AREA MARK	1	1



CURSOR DISPLAY MODE	MAT <sub>5</sub>	MAT <sub>4</sub>
FIXED COMPLEMENTED	0	0
FLASH COMPLEMENTED	1	0
FIXED UNDERLINED	0	1
FLASH UNDERLINED	1	1

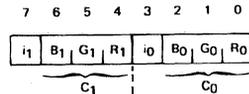
NOTA : PROGRAMMING BIT VALUE  
1 = True  
0 = False

DOR in 40 char/row

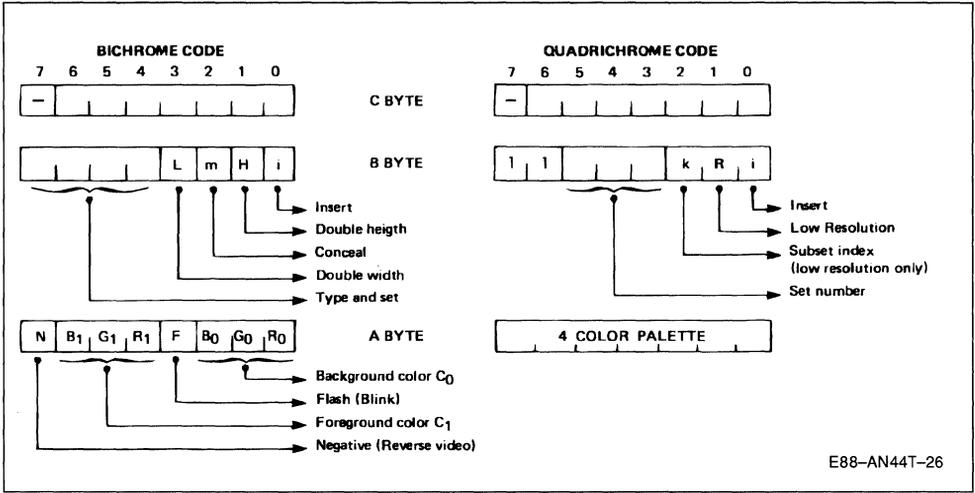


DOR in 80 char/row

I=4



40 Char/Row Fixed Long Codes

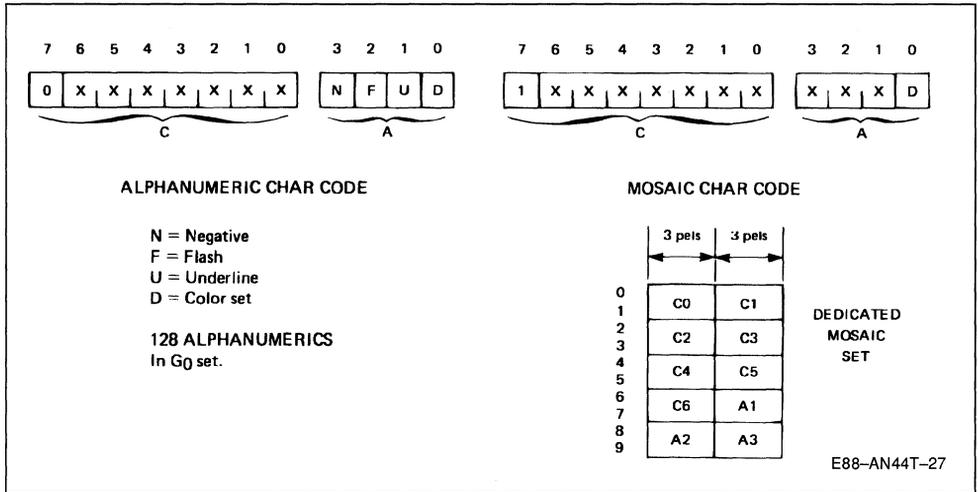


Type and Set Code : B (4 : 7)				Number of Character Per Set	Set Name	Set Type	Cell Location
7	6	5	4	C (0 : 6)			
0	0	1	0	128 Standard Mosaics 32 Strokes	G <sub>10</sub> G <sub>11</sub>	SEMI-GR.	ON-CHIP ROM
		0	1	128 Alphanumerics	G <sub>0</sub>	ALPHA	
	0	0	Accentuated Lower Case Alpha	G <sub>20</sub> G <sub>21</sub>			
1	0	1	1	100 Alpha UDS	G'0	SEMI-GR.	EXTERNAL MEMORY
		0	1	100 Semi-graphic UDS 100 Semi-graphic UDS	G'10 G'11		
	1	X	X	8 Sets of 100 Quadrichrome Character	Q <sub>0</sub> to Q <sub>7</sub>	QUADRICHROME	

Nota : Programming bit value  
 1 = True  
 0 = False.

# APPLICATION NOTE

## 80 Char/Row Character Code



## COLOR SELECTION

D	N	BACKGND COLOR	FOREGND COLOR	i
0	0	C <sub>M</sub>	C <sub>0</sub>	i0
0	1	C <sub>0</sub>	C <sub>M</sub>	i0
1	0	C <sub>M</sub>	C <sub>1</sub>	i1
1	1	C <sub>1</sub>	C <sub>M</sub>	i1

(C<sub>0</sub>, C<sub>1</sub>, i0, i1) : defined in DOR  
 C<sub>M</sub> : margin color defined in MAT



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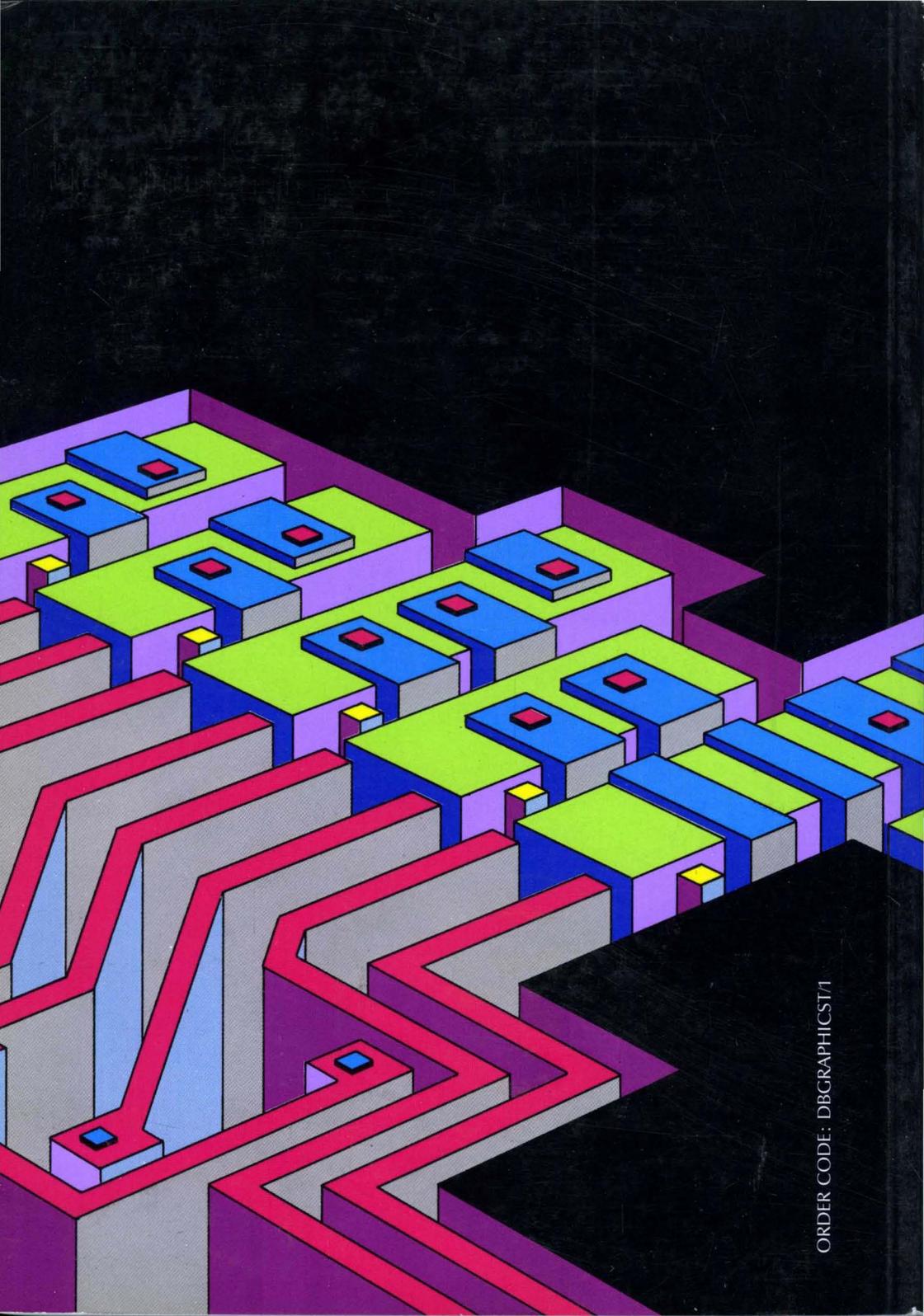
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