

TMS320 DSP Product Overview



The Leader in DSP Solutions

DSP Market

Texas Instruments (TI) has been the digital signal processor (DSP) market leader since 1982, with the introduction of the TMS32010 DSP. TI continues to be the largest manufacturer of programmable DSPs.

Three factors have driven TI's success:

- Product breadth and DSP solutions
- Development support
- Customizable DSP technology

Because of TI's heavy focus in DSP, TI has been able to build more products to better fit specific application needs. With more than 100 DSPs to choose from, TI has the device that gives you the right performance at the right price. Along with this extensive line of DSPs, TI offers complete system-level DSP solutions, including mixed-signal products and memory, to meet application requirements.

TI continues to help you get your products to market faster because of our broad and innovative development support program. Support is also available from the more than 250 TMS320 third parties.

TI also provides the ability to integrate DSP, logic, and analog and mixed-signal products onto one piece of silicon. When an application requires the ultimate in integration, TMS320 products are the only DSPs that offer a proven migration path to customizable DSPs (cDSP™).

When industry-standard algorithms become solid, TI has the ability to produce application-specific DSPs with maximum cost savings when flexibility is not necessary (e.g., specialized digital compression products).

TI continues to gain market share in this expanding market. This growth is fueled by growth in the communication, computer, consumer products, industrial control, instrumentation, military, and office automation arenas. TI is the DSP market share leader.

A fixed-point processor is a processor that does arithmetic operations using integer arithmetic with no exponents. Devices in the TMS320 DSP family which have fixed-point processors are the 'C20x, 'C24x, 'C5x, 'C54x, and 'C62x generations.

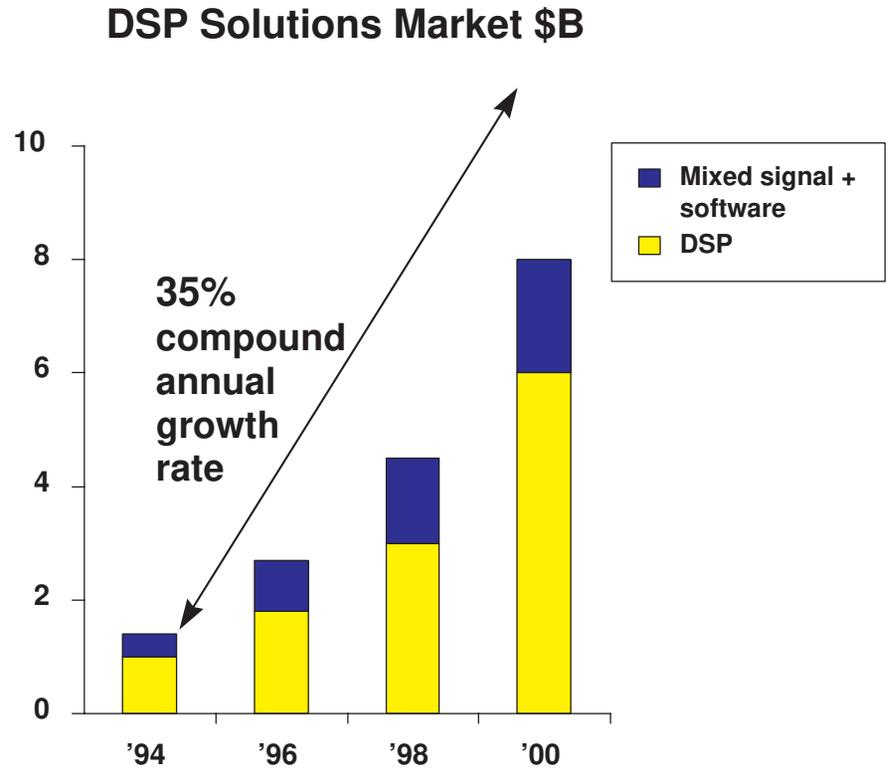
A floating-point processor is a processor capable of handling floating-point arithmetic where real operands are represented using exponents. Devices in the TMS320 DSP family that have floating-point processors are the 'C3x, 'C4x, and 'C67x generations.

***cDSP is a trademark of Texas Instruments*

The Leader in DSP Solutions - 2



Exploding Growth in DSP Applications



DSP Product Generations

TMS320C2xx generation: The TMS320C2xx was introduced in 1995. Manufactured with triple-level metal and full complementary CMOS static logic, the 'C2xx provides 20-40 MIPS performance. The 'C2xx, also available as a core for TI's customizable DSPs, is the low-cost, fixed-point DSP of the future. The TMS320C24x generation high-speed central processing unit (CPU) allows the use of advanced algorithms, yielding better performance and reducing system component count.

TMS320C3x generation: The TMS320C3x is an easy-to-use 32-bit floating-point DSP that achieves 33–60 million floating-point operations per second (MFLOPS) and 16.67–30 MIPS. The architecture of the 'C3x is specifically designed to be an efficient compiler platform. The highly optimized C compiler, the parallel instruction set, and the 'C3x general-purpose features ensure shorter time to market.

TMS320C4x generation: The TMS320C4x is a high-performance parallel processor with up to 488 Mbytes/s of data throughput, 40-80 MFLOPS, and 20-40 MIPS. It accepts source code from the 'C3x. Parallel processing development tools are available for the 'C4x.

TMS320C5x generation: The TMS320C5x is a high-performance fixed-point DSP that achieves 20-50 MIPS and accepts source code from the 'C1x, 'C2x, and 'C2xx generations. The architecture of the 'C5x generation includes flexible power-management features. The 'C5x is available in low-voltage versions.

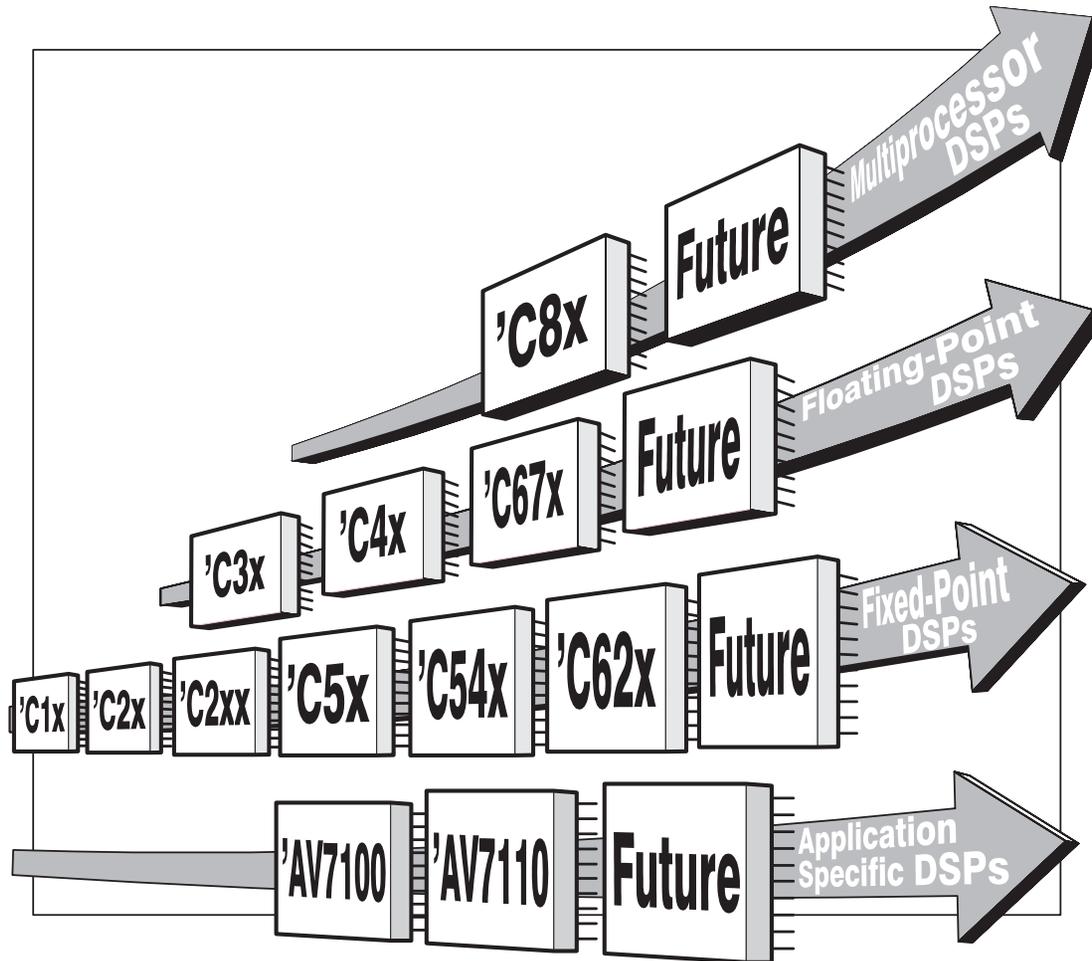
TMS320C54x generation: The TMS320C54x provides the cost-effective combination of high performance and low power. The 'C54x executes up to 66 MIPS and can operate at 3.0 V, 3.3 V, or 5 V. The specialized architecture is optimized to meet the needs of a variety of existing and emerging worldwide telecommunication and wireless applications.

TMS320C6x generation: The TMS320C6x generation offers cost-effective solutions to high-performance DSP programming challenges. The 'C6x devices are the first to feature *VelociTI™*, which allows performance of up to 1600 million instructions per second (MIPS).

TMS320C8x generation: The TMS320C8x integrates multiple (up to four) 32-bit advanced DSPs, a 32-bit RISC master processor with a 100-MFLOPS floating-point unit, a transfer controller with up to 400-Mbytes/s off-chip transfer rate, and up to 50K bytes of on-chip RAM—on a single piece of silicon. The 'C80 also includes two on-chip frame timers.

TMS320AVxxx generation: The TMS320AVxxx high-speed, application-specific digital compression products meet the demand of compressed audio and video playback in applications such as videoconferencing, digital broadcasting, high-definition TV, graphic workstations, and others supported by international compression standards.

DSP Product Generation



TMS320C2xx Generation

The combination of advanced Harvard architecture, on-chip peripherals, on-chip memory, and a highly specialized instruction set is the basis of the operational flexibility and speed of the 'C2xx devices.

The 'C2xx generation offers these advantages:

- Enhanced TMS320 architectural design for increased performance and versatility
- Advanced integrated circuit processing technology for increased performance
- Source code compatibility with the 'C1x and 'C2x DSPs
- Upward compatibility with fifth generation DSPs ('C5x)
- New static-design techniques for minimizing power consumption and increasing radiation tolerance

TMS320C2xx Generation Subfamilies

The 'C2xx generation includes two subfamilies: the general-purpose 'C20x DSPs and the 'C24x DSP controllers that are optimized for digital-control-system type applications.

TMS320C2xx	
20x	24x
C203	F240
LC203	C240
F206	F241
C206	C241
LC206	F243
C209	C242

TMS320C20x Features

The features for 'C20x are:

- Up to 4.5K data/program RAM on chip
- 32K words of flash memory on chip ('F206 only)
- 32-bit ALU accumulator
- 16 x 16-bit parallel multiplier with a 32-bit product
- Repeat instructions for efficient use of program space and enhanced execution
- 16-bit on-chip timer
- 16-bit barrel shifter
- 8-level hardware stack
- Built-in power-down mode
- Software wait-state generator
- 80- or 100-pin TQFP packages
- Various PLL options for reduced electromagnetic interference (EMI) and system power dissipation
- 'C203, 'LC203, 'C206, 'LC206, and 'F206 are pin-for-pin compatible in a 100-pin TQFP package

TMS320C203/LC203

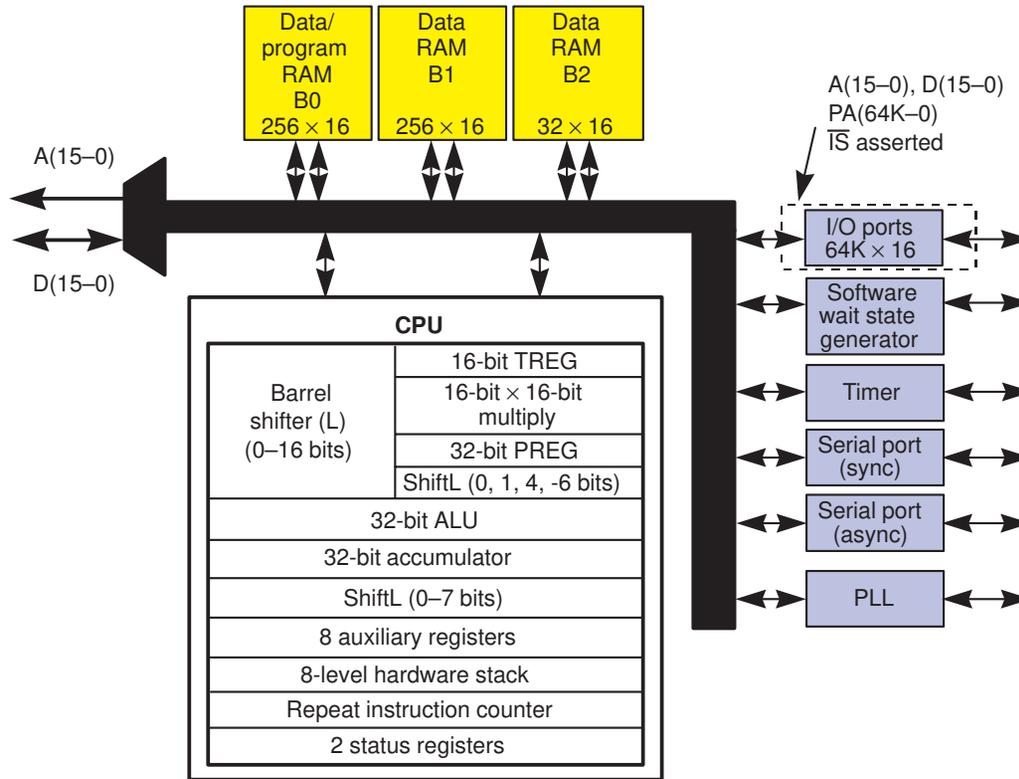
The 'C203 features the core CPU of the 'C2xx generation and several peripherals that optimize it for low-cost, high-volume applications.

The 'C203 has one enhanced synchronous serial port (ESSP) with a 4-level-deep FIFO, which results in less intervention from the CPU, at a low cost. There is also a universal asynchronous receive transmit (UART), a 16-bit timer, and a software wait-state generator. The serial ports, timer, and wait-state generator are each mapped into I/O space.

Features of the 'C203 and 'LC203 include:

- 25-, 35-, and 50-ns instruction cycle times ('LC203 50-ns instruction cycle time)
- 3.3-V version, 20 MIPS ('LC203)
- 192K-word external address reach
- 544 words RAM
- Accepts source code from the 'C1x and 'C2x generations
- ANSI C compiler
- $\div 2$, $\times 1$, $\times 2$, and $\times 4$ PLL options
- IEEE 1149.1-standard (JTAG) emulator control
- Boot ROM option
- Full-duplex enhanced synchronous serial port (ESSP) with 4-level-deep FIFO
- Full duplex asynchronous serial port
- 100-pin TQFP package

TMS320C203/LC203 Block Diagram



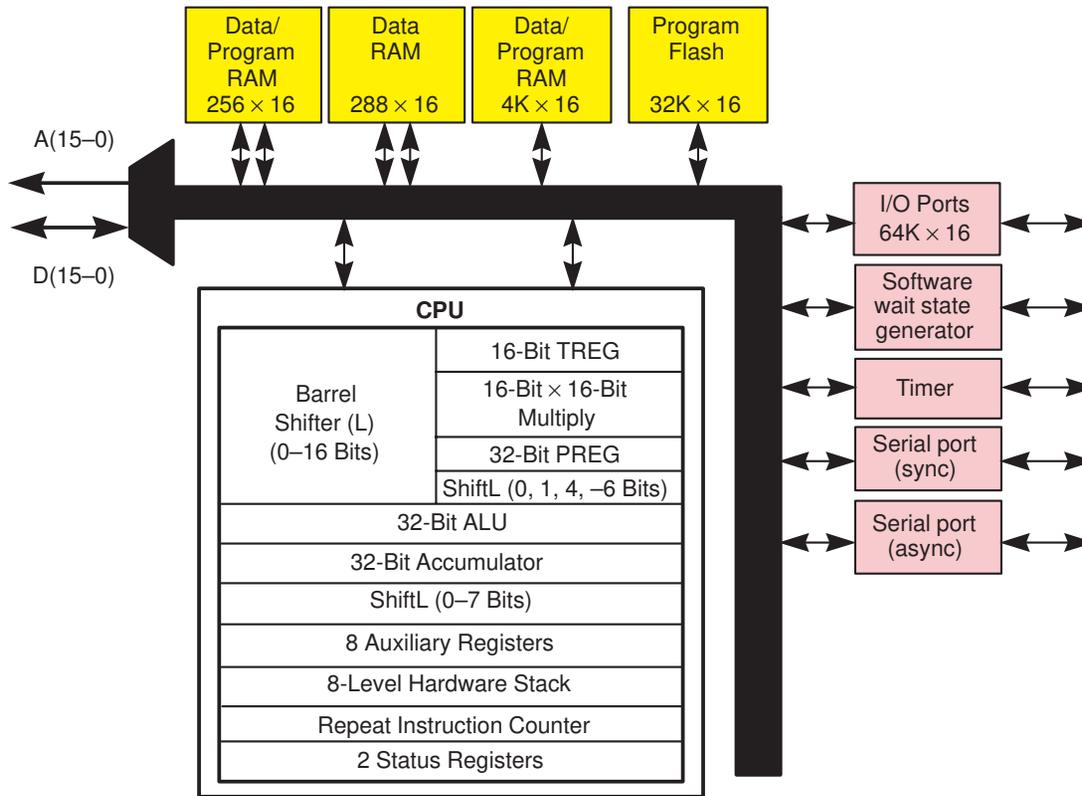
TMS320F206

The 'F206 is the first digital signal processor from Texas Instruments with on-chip flash memory. The 'F206 features the core CPU of the 'C2xx generation, several fast, flexible peripherals, and 32K words of flash memory for high-volume, low-cost memory integration. The flash memory can be reprogrammed either by another processor or through an emulator. The 'F206 has the same peripherals as the 'C203 and is pin-for-pin compatible with the 'C203.

Features of the 'F206 include:

- 50-ns instruction cycle time
- 192K-word external address reach
- 4.5K words on-chip RAM
- 32K 16-bit words of flash memory
- Accepts source code from the 'C1x and 'C2x generations
- ANSI C compiler
- $\div 2$, $\times 1$, $\times 2$, and $\times 4$ PLL options
- IEEE 1149.1-standard (JTAG) emulator control
- Full-duplex enhanced synchronous serial port (ESSP) with 4-deep FIFO
- Full duplex asynchronous serial port
- 100-pin TQFP package
- Flash programming utility software

TMS320F206 Block Diagram



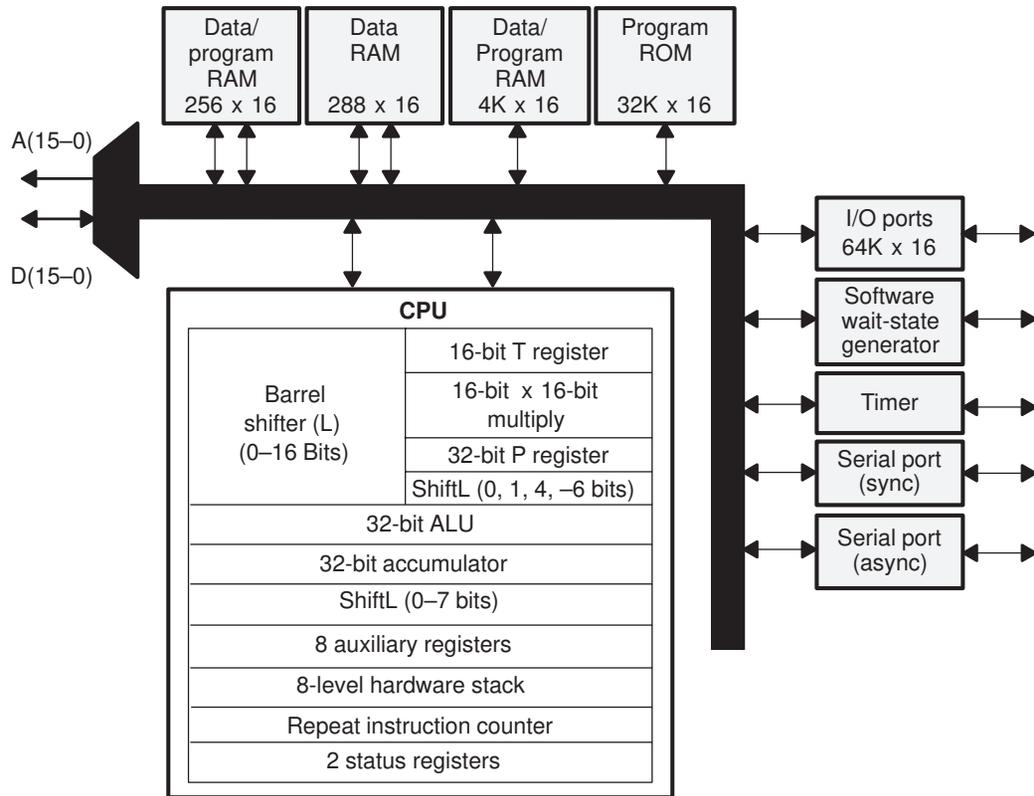
TMS320C206/LC206

The architecture of the 'C206 is based on that of the TMS320C2xx series and is optimized for low-power operation. The 'C206 is scheduled for sample availability in 2Q '98 and for production in 4Q '98.

Features of the 'C206 include:

- 5-V version (3.3-V 'LC206)
- 4.5K-word RAM
- 32K-word ROM
- 192K-word external address reach
- Accepts source code from the 'C1x and 'C2x generations
- ANSI C compiler
- $\div 2$, x1, x2, and x4 PLL options
- IEEE 1149.1-standard JTAG emulator control
- Full-duplex enhanced synchronous serial port (ESSP) with 4-level deep FIFO
- Full duplex asynchronous serial port
- 100-pin TQFP packaging
- On-chip bootloader

TMS320C206/LC206 Block Diagram



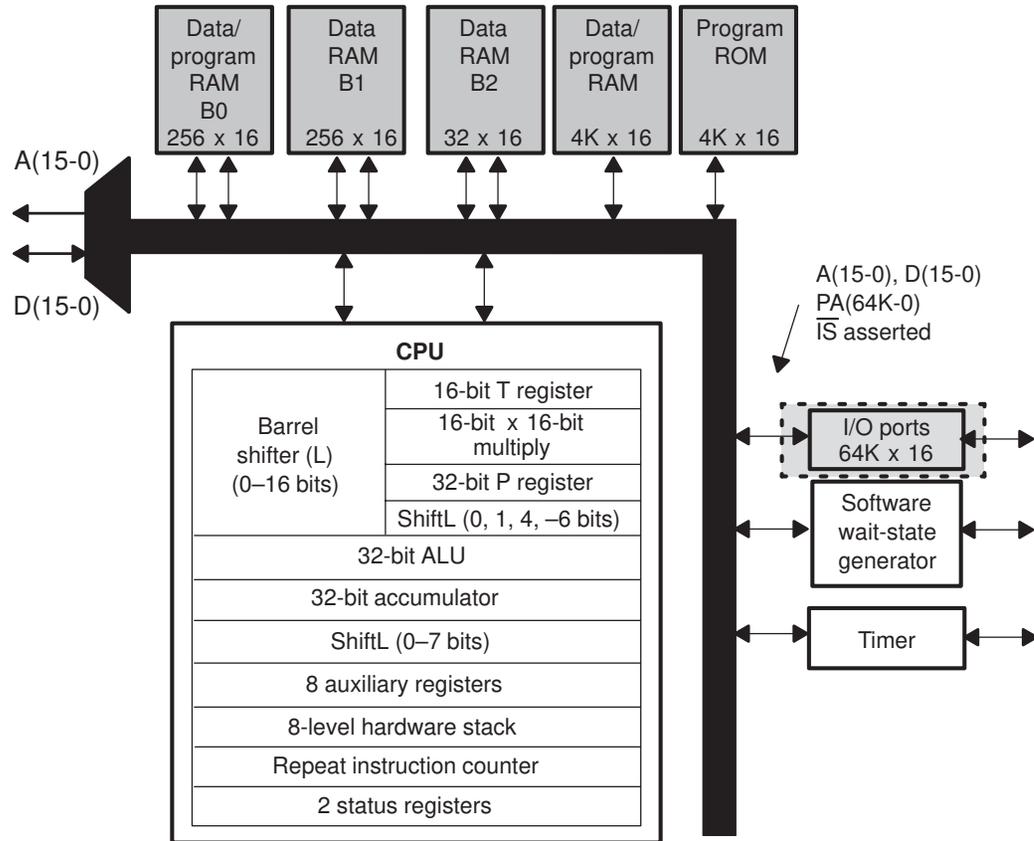
TMS320C209

The 'C209 incorporates the 'C2xx core CPU and adds 4K words of RAM and 4K words of ROM on chip. The device has a 16-bit timer and a software wait-state generator; it is packaged in an 80-pin thin quad flat pack (TQFP). The large on-chip memory, small packaging, and low cost make this device attractive for space-constrained applications such as small form factor hard-disk drives.

The 'C209 features:

- 35- and 50-ns instruction cycle times
- 4K 16-bit words of RAM
- 4K 16-bit words of ROM
- 192K-word external address reach
- Accepts source code from the 'C1x and 'C2x generations
- ANSI C compiler
- $\div 2$, $\times 2$ PLL option
- IEEE 1149.1-standard (JTAG) emulator control
- 80-pin TQFP package

TMS320C209 Block Diagram



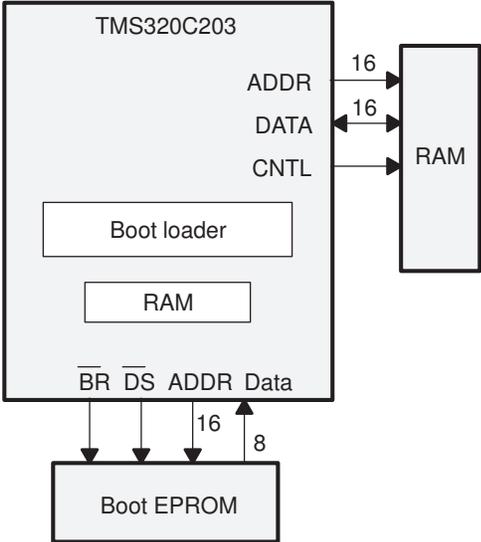
TMS320C20x Boot Loader

The 'C203 has an on-chip hard-coded boot loader, which allows you to load code from an 8-bit external EPROM into internal or external RAM. The EPROM is mapped into global data memory. Once the boot loading operation begins, 8-bit data is read by the device and reassembled into 16-bit words to a user-specified destination. When complete, control of the device is passed to the start of the program.

Features of the 'C20x boot loader are:

- Load from 8-bit external EPROM into internal/external RAM
- EPROM is mapped into global data memory space
- Dedicated boot loader pin
- Backward compatible with 8-bit data in 'C203
- Supports
 - 8-bit and 16-bit EPROM
 - 8-bit and 16-bit parallel I/O boot
 - 8- and 16-bit enhanced synchronous serial ports (ESSPs)
 - 8-bit asynchronous serial ports

TMS320C20x Bootloader Block Diagram



TMS320C20x Enhanced Synchronous Serial Port (ESSP)

The TMS320C20x offers a full-duplex framed synchronous serial port with up to 20 Mbps throughput (@ 25-ns instruction cycle time). The transfer rate is one-half the device clockout rate. This bidirectional synchronous serial port provides direct communication with serial devices such as codecs, serial ADCs, and other serial systems. The serial port can also be used for intercommunication between processors in multiprocessing applications.

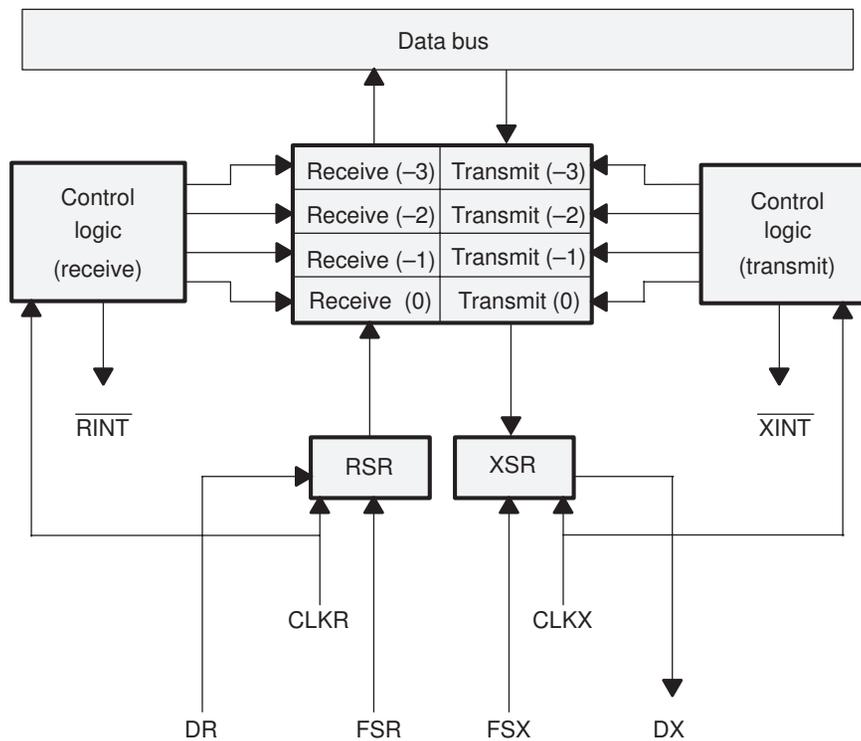
Both the receive and transmit sides of the serial port have a 4-level-deep FIFO buffer which allows the CPU to accept an interrupt at either 1, 2, 3, or 4 levels deep. This capability means less intervention from the CPU, as well as increased flexibility and efficiency with respect to data transfers.

The 'C20x enhanced synchronous serial port (ESSP) features:

- Full-duplex framed synchronous serial port
- Two 4-word \times 16-bit buffers to reduce interrupt service routine (ISR) overhead
- Serial port performance
 - 20 Mbps at 25 ns
 - 14.28 Mbps at 35 ns
 - 10 Mbps at 50 ns
- Transfer rate is 1/2 of CPU rate

All 'C2xx devices, except the 'C209, feature this serial port.

TMS320C20x ESSP Block Diagram



TMS320C20x Asynchronous Serial Port

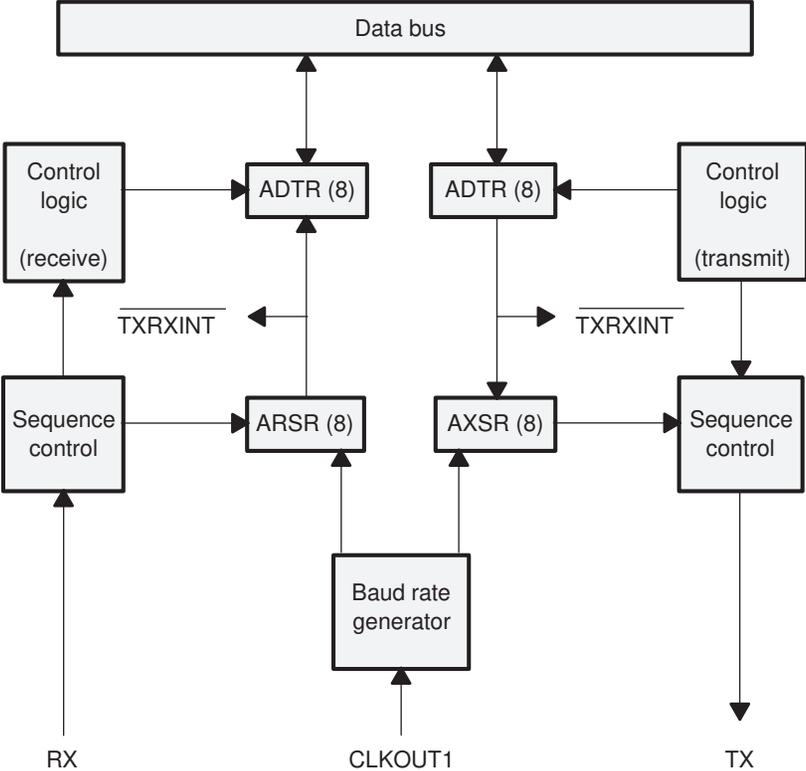
The TMS320C20x offers an asynchronous serial port that is full-duplex and double-buffered. It accepts 8-bit data and can be programmed via a register to accept baud rates of up to 2.5 Mbps. The asynchronous serial port can be used to communicate with other devices such as microcontrollers or for RS-232 connections supporting data transfers of up to 250.0 bps.

Features included with the 'C20x asynchronous serial port are:

- Full duplex
- Double buffered
- 8-bit data transfers
- 16-bit register for baud-rate generation
- Baud rates up to 2.5 Mbps (@ 25-ns instruction cycle time)
- Serial-peripheral interface (SPI) module, multi-channel

All 'C2xx devices, except the 'C209, feature this asynchronous serial port.

TMS320C20x Asynchronous Serial Port Block Diagram



TMS320C2xx Memory Bus

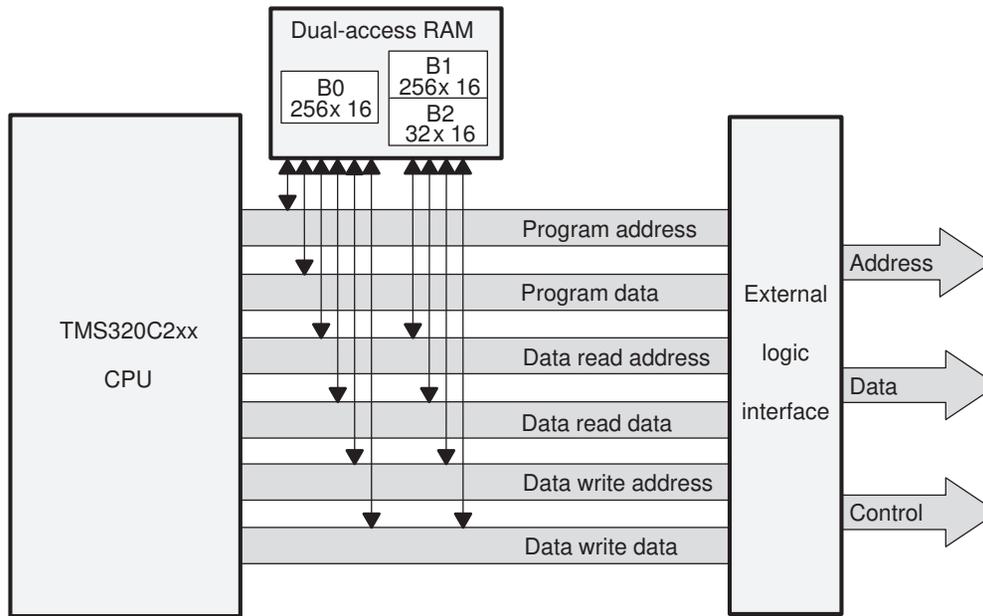
The 'C2xx advanced Harvard-type architecture maximizes processing power by maintaining two separate memory bus structures, program and data, for full-speed execution. This multiple bus structure allows reading both data and instructions simultaneously. Instructions support data transfers between the two spaces. This architecture lets you store coefficients in program memory to be read in RAM, eliminating the need for a separate coefficient ROM. This, coupled with a 4-level-deep pipeline, allows the TMS320C2xx to execute most instructions in a single cycle.

The 'C2xx dual-access RAM (DARAM) allows writes-to and reads-from the RAM in the same cycle without the address restrictions of SARAM. The dual-access RAM is configured in three blocks: block B0, block B1, and block B2. Block B0 is a 256-word block that can be configured as data or program memory. Block B1 is 256 words in data memory and block B2 is 32 words in data memory.

Some 'C2xx devices also have single-access RAM (SARAM) and/or ROM. Additionally, the 'F206 has flash memory.

The ability of the DARAM to perform two accesses in one cycle, coupled with the parallel nature of the 'C2xx architecture, enables the 'C2xx devices to perform three concurrent memory accesses in any given machine cycle.

TMS320C2xx Memory Bus Block Diagram



TMS320C20x Generation Summary

All TMS320C20x devices share the same CPU architecture and accept source code from all 'C1x, 'C2x, and 'C2xx devices. This table gives a 'C20x generation product summary so that you can choose the best combination of performance, memory, power, package, and peripherals for your system.

TMS320C20x Generation Summary Table

Product	MIPS	On-Chip Memory (Words)			Memory Off-Chip	Serial Ports		I/O		Package (TQFP)
		RAM	ROM	Flash		Sync	Async	Parallel	DMA	
TMS320C203	20/28.5/40	544	–	–	64K/64K	1	1	64K x 16	Ext.	100
TMS320LC203	20	544	–	–	64K/64K	1	1	64K x 16	Ext.	100
TMS320F206	20	4.5K	–	32K	64K/64K	1	1	64K x 16	Ext.	100
TMS320C206	40	4.5K	32K	–	64K/64K	1	1	64K x 16	Ext.	100
TMS320LC206	40	4.5K	32K	–	64K/64K	1	1	64K x 16	Ext.	100
TMS320C209	20/28.5	4.5K	4K	–	64K/64K	–	–	64K x 16	–	80

TMS320C24x Features

The features for 'C24x are:

- Processing hardware
 - 32-bit arithmetic logic unit (CALU)
 - 32-bit accumulator
 - 16-bit \times 16-bit parallel multiplier with a 32-bit product capability
 - Three scaling shifters
 - Eight 16-bit auxiliary registers with a dedicated arithmetic unit for indirect addressing of data memory
- Memory
 - 192K words \times 16-bit maximum addressable memory space
 - On-chip dual-access RAM (DARAM)
 - On-chip ROM or flash memory
 - External memory interface module with software wait state, 16-bit address lines, and 16-bit data lines
 - Support of hardware wait states
- Program control
 - Four-level pipeline operation
 - Eight-level hardware stack
 - User-maskable interrupts

TMS320C24x Features (continued)

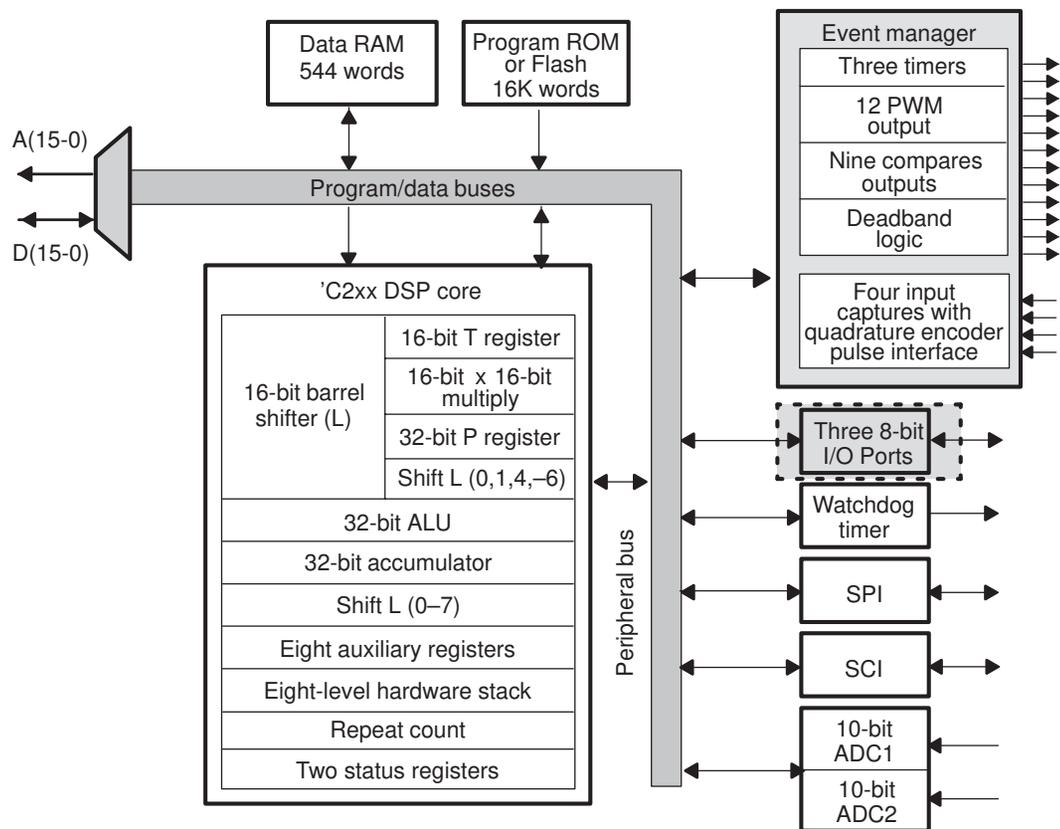
- Instruction set
 - Single-instruction repeat operation
 - Single-cycle multiply/accumulate instructions
 - Memory block move instructions for program/data management
 - Indexed-addressing capability
 - Bit-reversed indexed-addressing capability for radix-2 FFTs
- Power
 - Static CMOS technology
 - Four power-down modes to reduce power consumption
- Emulation: IEEE Standard 1149.1 boundary-scan logic interfaced to on-chip scan-based emulation logic
- Speed: 50-ns instruction cycle time, with most instructions single cycle
- Code compatibility with TMS 320 fixed-point devices
 - Source code compatible with the 'C25 and 'C2xx devices, and upwardly compatible with the 'C5x generation of DSPs
- On-chip peripherals

TMS320C240/F240

These are key features of the 'C240x and 'F240x:

- High-performance static CMOS technology
- Includes the T320C2xLP core CPU
 - Source code compatible with TMS320C25;
 - Upwardly compatible with TMS320C5x
 - 50-ns instruction cycle time
- Memory
 - 544K words \times 16-bits of on-chip data/program dual-access RAM
 - 16K words \times 16 bits of on-chip program ROM ('C240) / flash memory ('F240)
 - 192K words \times 16 bits of total memory address reach
- Event-manager module (12 PWM outputs)
- Dual 10-bit analog-to-digital conversion module
- 28 individually programmable, multiplexed I/O pins
- Phase-locked loop (PLL)-based clock module
- Watchdog timer module (with real-time interrupt)
- Serial communication interface (SCI) module
- Serial peripheral interface (SPI) module
- Six external interrupts
- Four power-down modes for low-power operation
- Scan-based emulation
- Extended temperature range options available

TMS320C240/F240 Block Diagram

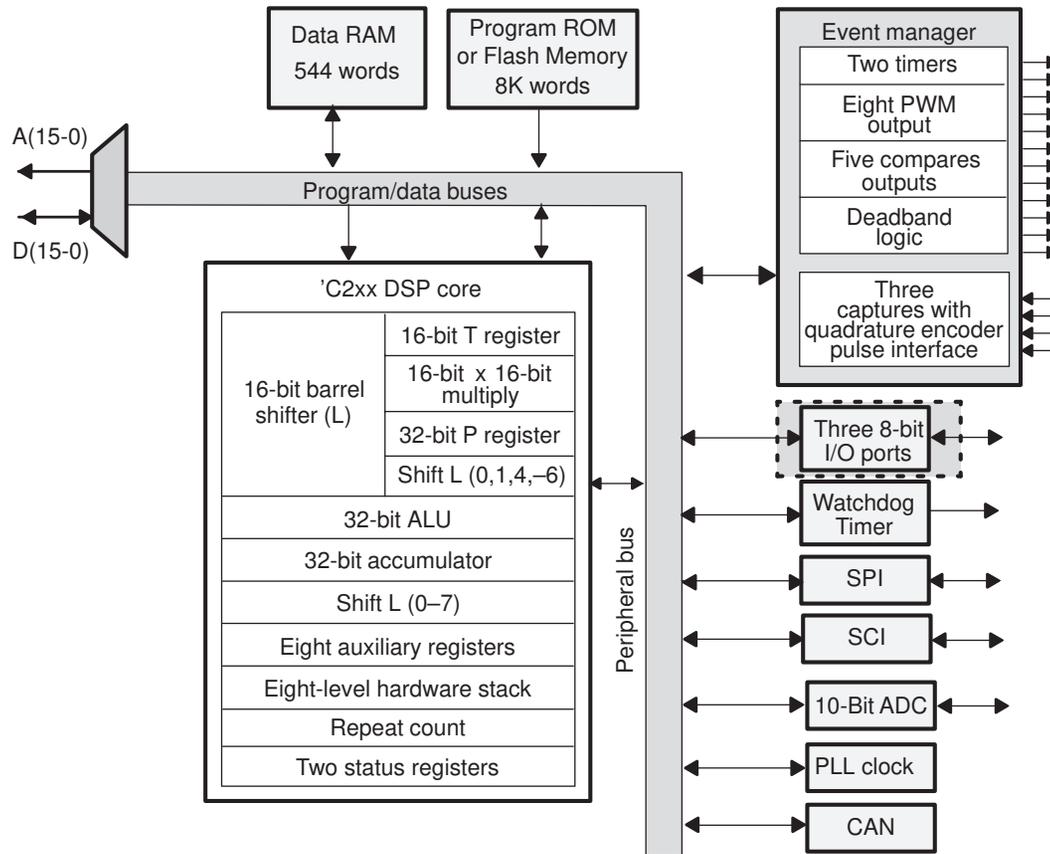


TMS320C241/F241

The 'C241 device has the following features:

- 'C2xx DSP core, 5-V
- 8K words × 16 bits of on-chip ROM (Flash memory for 'F241)
- Motor control-optimized event manager (8 PWM outputs)
- 10-bit A/D converter with 800-ns conversion time
- On-chip CAN module (meets specification 2.0B)
- 'C241 supported by the 'F241 for prototyping/preproduction needs
- Extended temperature range options
- 68-pin PLCC, 64-pin PQFP package
- 'F241 footprint-compatible with 'C241 for preproduction prototyping

TMS320C241/F241 Block Diagram

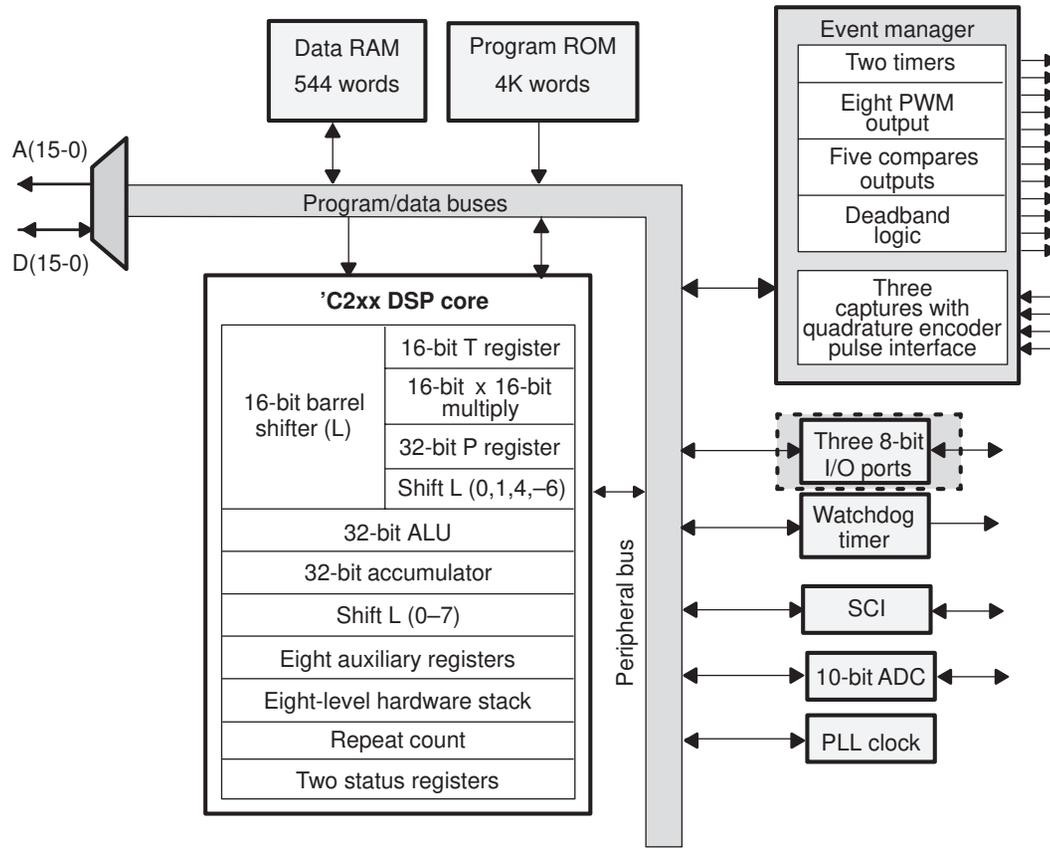


TMS320C242

The 'C242 device has the following features:

- 'C2xx DSP core, 5-V
- 4K words of on-chip ROM
- Motor control-optimized event manager (8 PWM outputs)
- 10-bit A/D converter with 800-ns conversion time
- Supported by the 'F243 for prototyping/preproduction needs
- No CAN and SPI
- Extended temperature range options
- 68-pin PLCC, 64-pin PQFP package

TMS320C242 Block Diagram

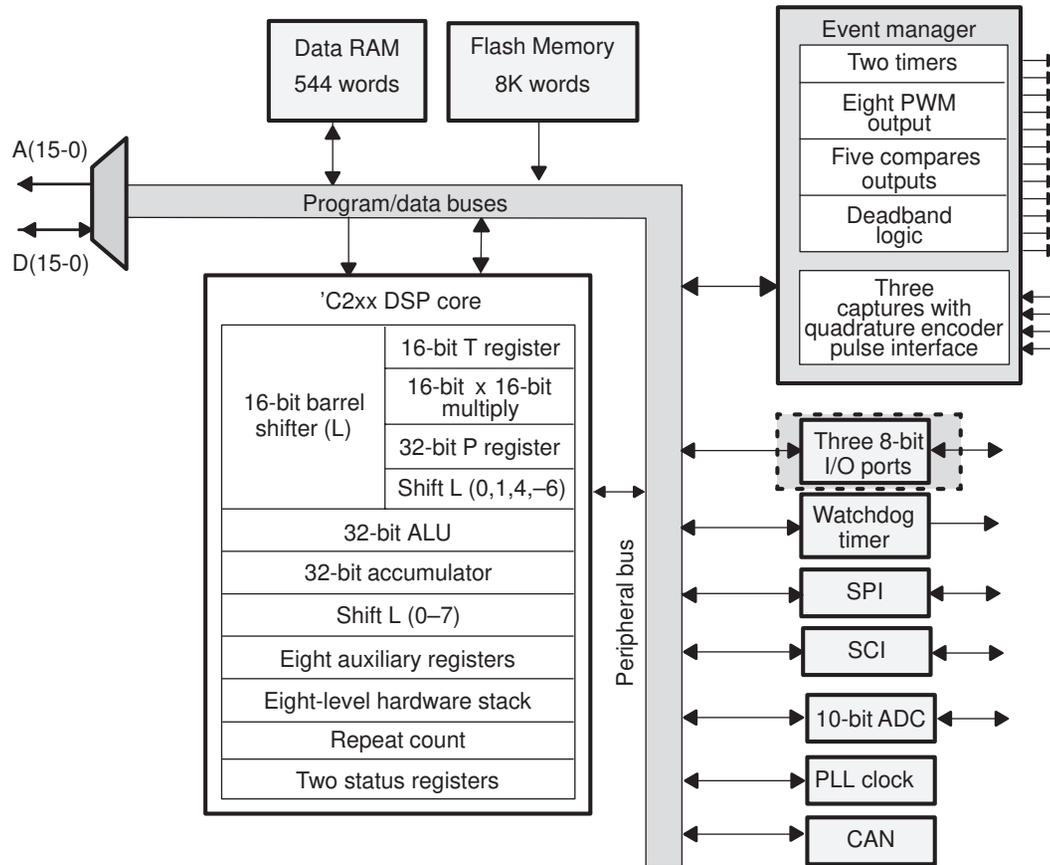


TMS320F243

The 'F243 device has the following features:

- 'C2xx DSP core, 5-V
- 8K words of on-chip flash memory
- Motor control-optimized event manager (8 PWM outputs)
- 10-bit A/D converter with 800-ns conversion time
- On-chip CAN module (meets specification 2.0B)
- 16-bit **external memory interface**
- Extended temperature range options
- 144-pin TQFP package

TMS320F243 Block Diagram



Controller Area Network (CAN) Module

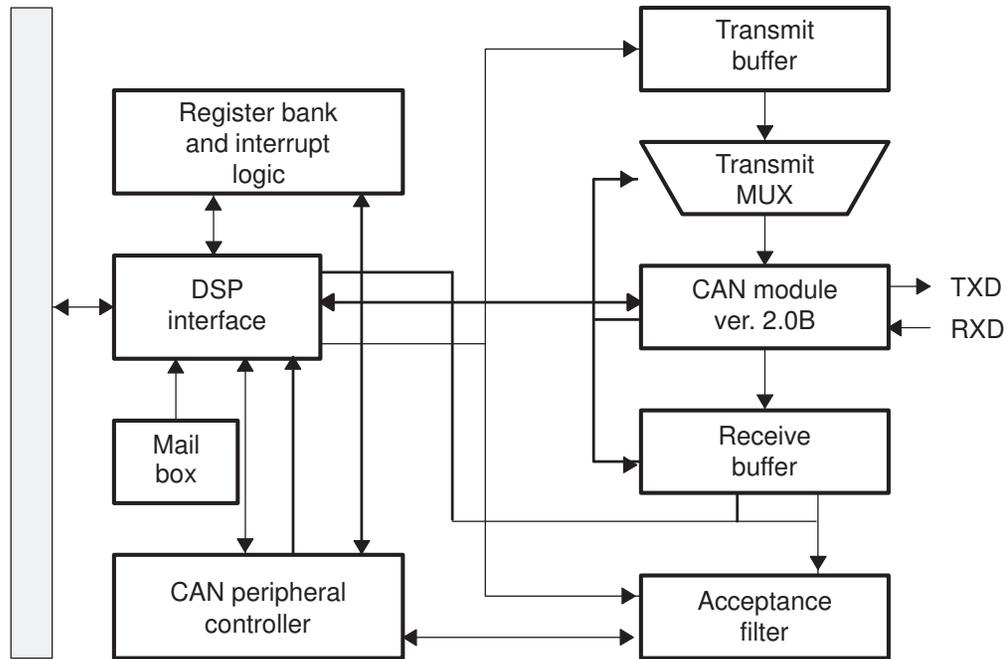
The 'C241, 'F241, and 'F243 devices include a CAN module. The CAN network uses a serial mutimaster communication protocol that efficiently supports distributed-time control, with a very high level of security and a communication rate of up to one megabit per second ((@ 20-MHz system clock). The CAN bus is ideal for applications operating in a noisy and harsh environment, such as in the automotive or other industrial fields requiring reliable serial communication or multiplexed wiring.

The CAN module provides the CPU with full functionality of the CAN specification, version 2.0B. The module minimizes the CPU's load in communication overhead and enhances the CAN standard by providing additional features.

The following are features of the CAN module:

- Full support for CAN specification 2.0B
- Programmable transmission rate
- Low DSP load for CAN operation and management
- Definition of up to 6 mail boxes
- Selectable interrupt sources
- Internal fault test and confinement
- Automatic transmission timeout
- Low power mode

Controller Area Network (CAN) Module



TMS320C24x Generation Summary

All TMS320C24x devices share the same CPU architecture and accept source code from all 'C1x, 'C2x, and 'C2xx devices. This table gives a 'C24x-generation product summary so that you can choose the best combination of performance, memory, power, package, and peripherals for your system.

TMS320C24x Generation Summary Table

Product	MIPS	On-Chip Memory (Words)			Ext. Memory	A/D	PWM	Compares/ Captures	Timers			I/O Pins	Package
		RAM	ROM	Flash					DAT/PRO	Gen. Purp.	Watch-dog		
TMS320F240	20	544	–	16K	64K/64K	Dual 10-bit	12	9/4	3	1	1	28	132 PQFP
TMS320C240	20	544	16K	–	64K/64K	Dual 10-bit	12	9/4	3	1	1	28	132 PQFP
TMS320F241	20	544	–	8K	–	10-bit	8	5/3	2	1	–	26	68 PLCC 64 PQFP
TMS320F243*	20	544	–	8K	64K/64K	10-bit	8	5/3	2	1	–	32	144 TQFP
TMS320C241	20	544	8K	–	–	10-bit	8	5/3	2	1	–	26	68 PLCC 64 PQFP
TMS320C242	20	544	4K	–	–	10-bit	8	5/3	2	1	–	26	68 PLCC 64 PQFP

* includes external memory interface

TMS320C3x Generation

The TMS320C3x generation is the first of TI's 32-bit floating-point digital signal processors. The 'C3x devices provide an easy-to-use, high-performance architecture, that allows users to develop breakthrough products quickly. 'C3x devices can be used in a wide variety of areas including automotive applications, digital audio, industrial automation and control, data communication, and office equipment that include multifunction peripherals, copiers, and laser printers.

The CPU has an independent multiplier and ALU to offer up to 60 million floating-point operations per second (MFLOPS) and up to 30 MIPS.

The direct memory access (DMA) controller has its own data bus and operates in parallel with the CPU. The DMA controller is programmed to input and output data sets, freeing the CPU for arithmetic operations. The DMA controller can reach anywhere in the memory map, including on-chip, off-chip, and memory-mapped peripheral registers.

The total memory space of the 'C3x is 16 million 32-bit words. Having the data, program, and I/O space contained in this 16M-word address range maximizes memory usage and allows you to allocate the memory space as desired.

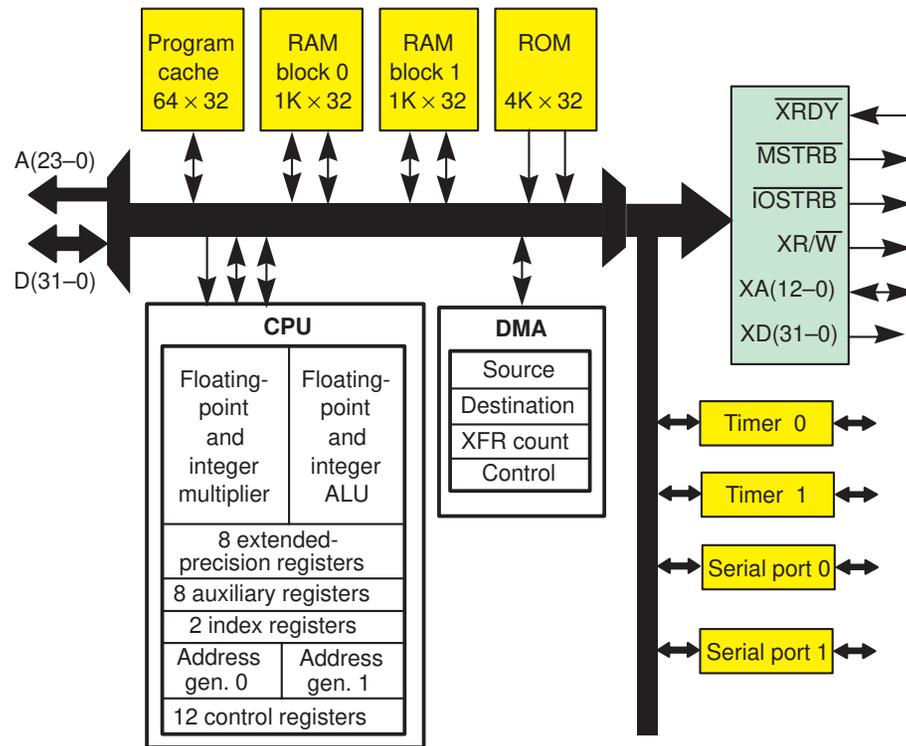
TMS320C30

The TMS320C30 features two external data buses, two timers, and two serial ports. The primary bus has a 24-bit address bus. The expansion bus has a 13-bit address bus. Both have a 32-bit data bus. Each serial port has independent double-buffered transmit and receive sections with a maximum data rate of 15 Mbps with a 60-MHz input clock.

Features of the 'C30 include:

- 40-, 50-, and 60-ns instruction cycle times
- 16M-word external address reach
- Single-cycle multiply and accumulate operation
- Two serial ports
- Two timers
- 4K-words on-chip ROM
- Optimizing ANSI C compiler
- On-chip DMA
- 181-pin PGA package

TMS320C30 Block Diagram



TMS320C31

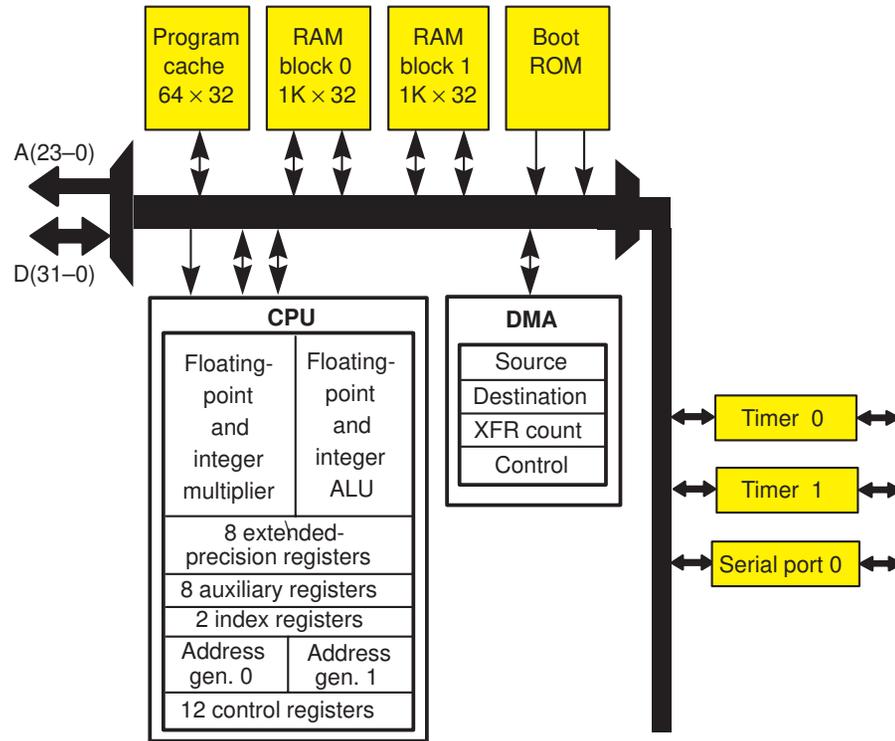
The TMS320C31 is the second member of the 'C3x generation and is object-code compatible with the 'C30. The 'C31 has the same fast CPU as all other members of the 'C3x generation but offers a different mix of peripherals to achieve a unique price/performance point.

The 'C31 offers a lower cost than the 'C30 by removing the expansion bus and one of the serial ports, and replacing the 4K 32-bit words of internal ROM with a boot ROM. A low-power version of the 'C31 is available at 40 MHz at 3.3 V that significantly reduces power consumption. The 'C31 comes in a 132-pin plastic quad flat pack (PQFP) package.

The 'C31 features:

- 33-, 40-, and 50-ns instruction cycle times
- 16M-word external address reach
- Single-cycle multiply and accumulate operation
- Optimizing ANSI C compiler
- On-chip DMA
- Boot ROM
- 3.3-V version at 40 MHz
- Two low-power modes
- Two 32-bit timers
- Serial port
- 64-word cache
- 132-pin PQFP package

TMS320C31 Block Diagram



TMS320C32

The TMS320C32 is the lowest-cost 32-bit floating-point device TI offers. The 'C32 is object-code compatible with the 'C30 and 'C31.

The 'C32 has a flexible memory interface that allows access to 8-, 16-, or 32-bit memory. This can lead to considerable savings in system cost.

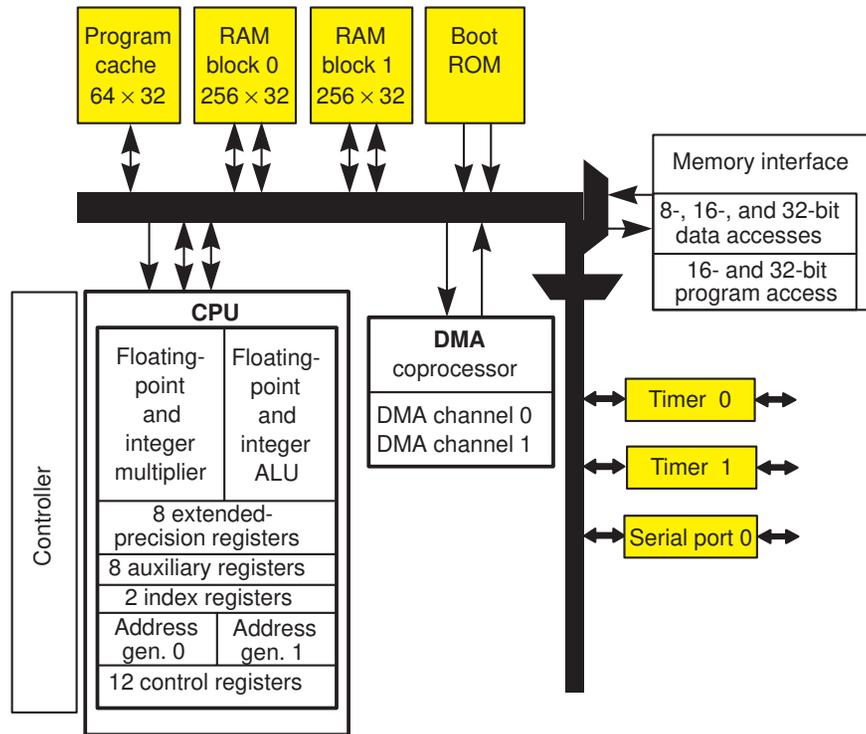
There are also two low-power modes on the 'C32. One reduces the clock rate of the device but continues execution, while the other suspends instruction execution and puts the device on hold. These are valuable features in power-critical applications.

The 'C32 features the same boot ROM as the 'C31, has two 256-word \times 32-bit blocks of on-chip RAM, and comes in a 144-pin PQFP package.

Features of the 'C32 include:

- 33-, 40-, and 50-ns instruction cycle times
- Object-code compatible with the 'C30 and 'C31
- 16M-word external address reach
- Flexible memory interface (8, 16, or 32 bits)
- Two-channel DMA with configurable priorities
- Low-power modes
- 64-word program cache
- Two 32-bit timers
- 144-pin PQFP package
- Serial port

TMS320C32 Block Diagram



TMS320C3x CPU

The TMS320C3x CPU has an independent multiplier and accumulator and achieves up to 60 MFLOPS. Results are stored in any one of eight extended-precision registers. These are 40-bit registers that store values with a 32-bit mantissa and an 8-bit exponent. These registers can serve as both the source and destination for any arithmetic operation. The extended-precision registers are an extremely valuable resource for programming in assembly or C. These registers allow you to maintain intermediate results without storing data in memory. This results in higher-performance assembly code and a more efficient C compiler.

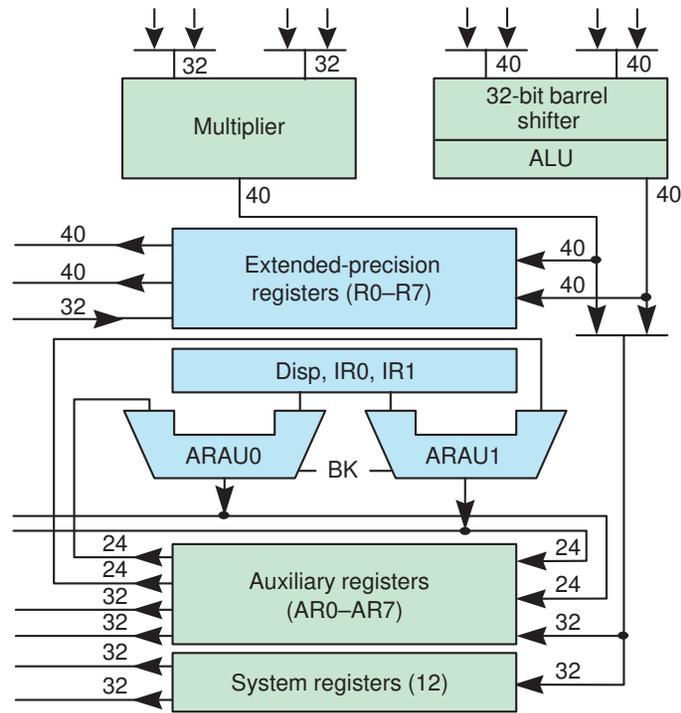
To sustain 60 MFLOPS, the CPU has two independent auxiliary register arithmetic units (ARAUs). The two ARAUs generate 24-bit addresses that are accessed via the eight auxiliary registers. The ARAUs can perform any of these functions:

- Pre or postincrement or decrement
- Index offset for increment and decrement values other than 1
- Circular addressing to support circular buffers
- Bit-reversed addressing for FFTs

Features of the 'C3x CPU include:

- 60-MFLOP CPU
- Register-based CPU
- 32 or 40 floating-point/integer multiplier
- 32 or 40 floating-point/integer ALU
- 32-bit barrel shifter
- Eight 40-bit extended-precision registers
- Two address generators
- Two index registers
- Eight indirect-address registers

TMS320C3x CPU Block Diagram



TMS320C3x Memory

To realize the full performance of the 'C3x CPU, it is important to have a bus and memory architecture that can keep pace. The 'C3x fetches up to four words each cycle. These consist of a program opcode, two CPU data operands, and a DMA data transfer. The internal buses can transfer all four words in parallel, relying on seven memory sources for data.

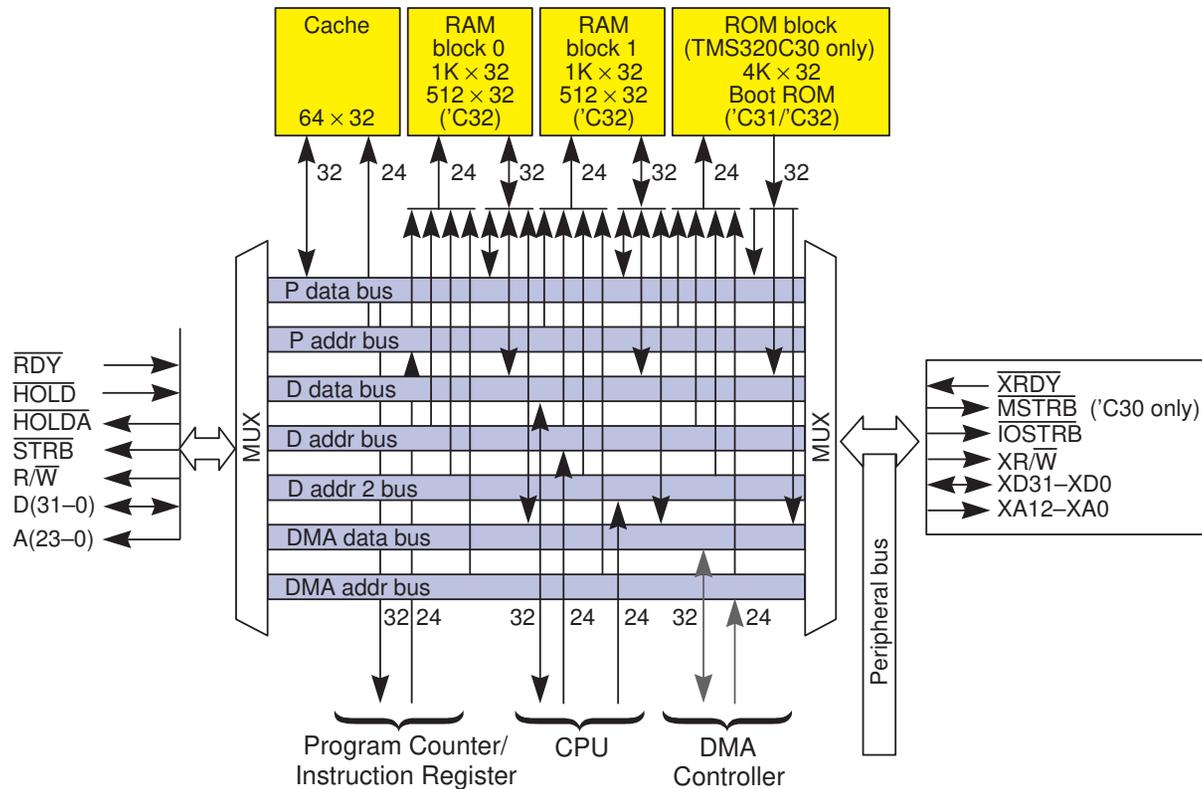
The 'C3x uses seven internal buses to access on-chip resources:

- Program address/data: The CPU uses these buses to maintain instruction fetches every cycle.
- Data address/data: In any cycle, the CPU can fetch two data operands, because it has two data address buses and one data bus that can be accessed twice in a single cycle.
- DMA address/data: The DMA uses these buses to perform DMA transfers in parallel with CPU operation.

With the internal buses in place to feed the DMA and CPU, the 'C3x devices can use both internal and external data and program memory. The 'C30 and 'C31 have two 1K 32-bit word blocks of dual-access RAM, while the 'C32 has two 256 32-bit word on-chip RAMs. This memory provides up to four words of program or data in a single cycle. All 'C3x devices feature an on-chip cache to boost system performance. The primary bus for each device has 16M words of address reach. The 'C30 features an expansion bus that has an 8K-word address reach, which is often used to interface to peripherals.

The 'C32 offers the ability to access 8-/16-/32-bit data stored in 8-/16-/32-bit wide external memory giving the flexibility of nine memory interface options. This feature can significantly affect total system cost savings. Additionally, the 'C32 memory interface allows for storage of the 32-bit instruction word in either 16- or 32-bit-wide external memory.

TMS320C3x Memory Block Diagram



TMS320C3x DMA Controller

The DMA controller transfers data between memory resources. The serial ports and timers on the 'C3x are memory-mapped, allowing DMA transfers to and from these peripherals. To perform a transfer, the DMA reads a memory location pointed to by the source address register and then writes to the memory location pointed to by the destination address register. The source and destination addresses are incremented or decremented after each transfer, depending on the value of the global control register. The DMA controller performs continuous transfers over the DMA bus until the value in the transfer counter register reaches 0, and a programmable interrupt is sent to the CPU.

For example, an application might use the DMA to transfer 512 words from slow external memory to the on-chip RAM. At the completion of the transfer, an interrupt is sent to the CPU to process and output results while the DMA transfers a new set of 512 words to on-chip RAM. By off-loading data input, the DMA controller allows sustained CPU performance for arithmetic calculations. In this case, the CPU always has zero-wait-state access to data, even though the external memory requires one or more wait states.

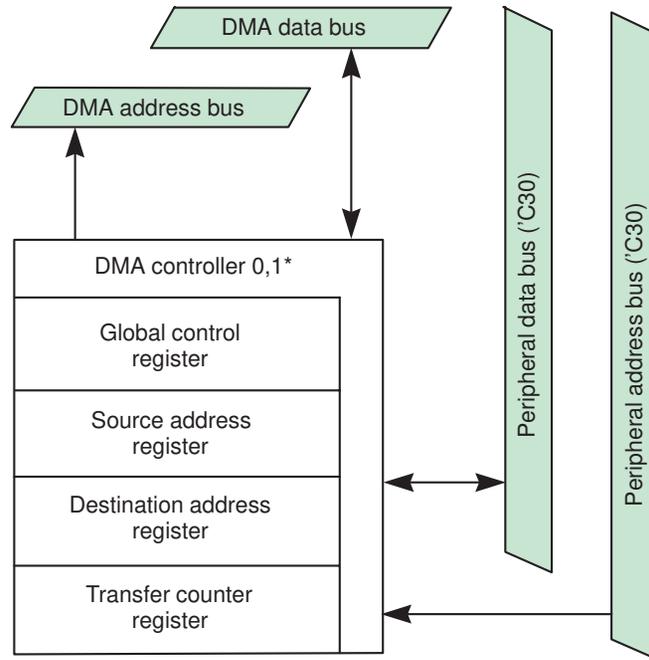
The 'C32 offers the programmer the flexibility of designating priority on the bus. There are three options:

- The CPU has priority over the DMA at all times ('C30 and 'C31)
- The DMA controller has priority over the CPU
- The CPU and DMA share a rotating priority with the CPU having first access

Features of the DMA controller include:

- Increased CPU-sustained performance by virtually eliminating CPU I/O
- Memory-to-memory transfers
- 2-channel configurable priority ('C32 only)
- Programmable increment or decrement of addresses

TMS320C3x DMA Controller Block Diagram



* DMA1 is available only on the 'C32.

TMS320C3x Sum of Products Example

The following code for a sum of products is typical of DSP algorithms and demonstrates the power of the 'C3x architecture. First, note that the repeat single instruction (RPTS) is used for a zero-overhead loop. The parallel bars next to the ADDF instruction indicate that the addition is executed in parallel with the multiplication. Auxiliary registers 0 and 1 are used to fetch the two data operands with a post-increment of one. The multiplier results are placed in one of the eight extended-precision registers. The extended-precision register set is further used as the input and output for the addition. Finally, the DMA can transfer the next set of data for the CPU to process in parallel with the multiply and accumulate. All of these operations take place in a single cycle, illustrating the parallelism in the 'C3x architecture.

TMS320C3x Sum of Products Example

$$y = a1 * x1 + a2 * x2 + \dots + an * xn$$

```
MPY  *AR0++, *AR1++, R0
```

```
MPY  *AR0++, *AR1++, R2
```

```
RPTS  n-3
```

```
MPYF *AR0++, *AR1++, R0
```

```
|| ADDF  R0 , R2 , R2
```

```
ADDF  R0 , R2
```

TMS320C3x Generation Summary

All TMS320C3x devices share the same CPU architecture and accept source code from all 'C1x, 'C2x, and 'C2xx devices.

This table gives a 'C3x-generation product summary so that you can choose the best combination of performance, memory, power, package, and peripherals for your system.

TMS320C3x Generation Summary Table

Data Type	Device	Cycle Time (ns)	Memory On Chip		Memory Off Chip	Peripherals			Package
			RAM (Words)	ROM (Words)		On-Chip Timers	Serial	DMA	
32-Bit	TMS320C30†	60	2K	4K	16M × 32	2	2	1	181-pin PGA
Floating-point word	TMS320C30-40†	50	2K	4K	16M × 32	2	2	1	181-pin PGA
	TMS320C30-50	40	2K	4K	16M × 32	2	2	1	181-pin PGA
	TMS320C31-40†‡	50	2K	Boot	16M × 32	2	1	1	132-pin PQFP
	TMS320LC31-40	50	2K	Boot	16M × 32	2	1	1	132-pin PQFP
	TMS320C31-50†‡	40	2K	Boot	16M × 32	2	1	1	132-pin PQFP
	TMS320C31-60	33	2K	Boot	16M × 32	2	1	1	132-pin PQFP
	TMS320C32-40‡	50	512	Boot	16M × 8/16/32	2	1	2	144-pin PQFP
	TMS320C32-50†‡	40	512	Boot	16M × 8/16/32	2	1	2	144-pin PQFP
	TMS320C32-60	33	512	Boot	16M × 8/16/32	2	1	2	144-pin PQFP

† Military version available

‡ Extended temperature version is available

TMS320C4x Generation

The TMS320C4x devices are 32-bit floating-point digital signal processors optimized for parallel processing. The 'C4x family combines a high-performance CPU and DMA controller with up to six communication ports to meet the needs of multiprocessor and I/O-intensive applications. All 'C4x devices are compatible with TI's multichip development environment. Each device contains an on-chip analysis module that supports hardware breakpoints for parallel-processing development and debugging. The 'C4x family accepts source code from the TMS320C3x family of floating-point DSPs. Key applications of the 'C4x family include 3-dimensional graphics, image processing, networking, and telecommunications base stations.

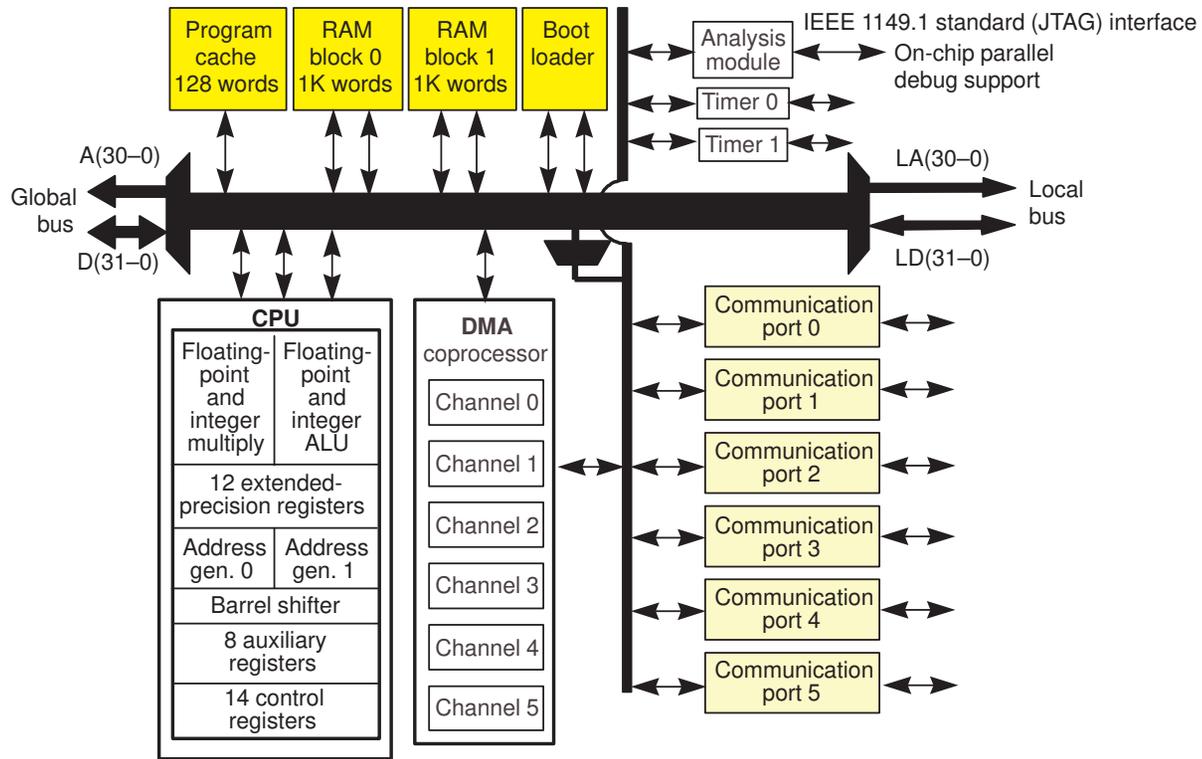
TMS320C40

The TMS320C40 is the original member of the 'C4x family. It features a CPU that can deliver up to 30 MIPS/60 MFLOPS with a maximum I/O bandwidth of 384 Mbytes/s. The 'C40 has 2K words of on-chip RAM, 128 words of program cache, and a boot loader. Two external buses provide an address reach of four gigawords of unified memory space. The 'C40 is available in a 325-pin CPGA package.

Features of the 'C40 include:

- 33-/40-ns instruction cycle times for the 'C40
- 4G-word external address reach
- Accepts source code from the 'C3x
- Optimizing ANSI C compiler
- IEEE floating-point conversion for ease of use
- 6- or 12-channel on-chip DMA
- Six communication ports
- 325-pin PGA package

TMS320C40 Block Diagram



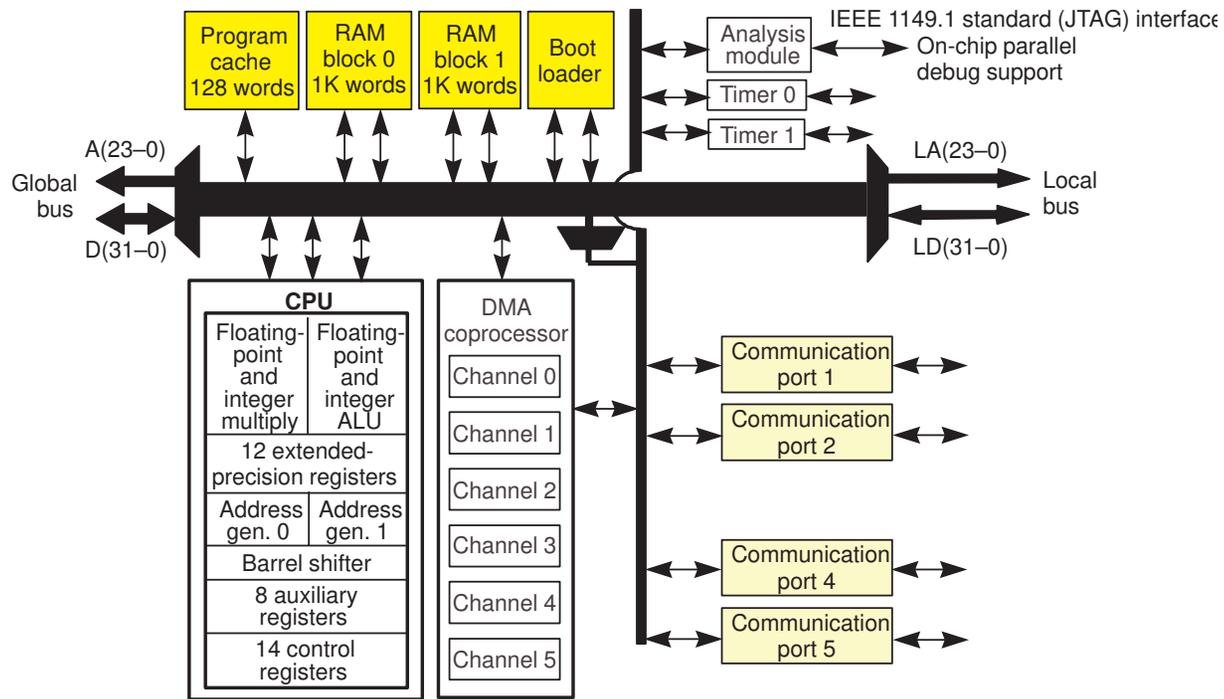
TMS320C44

The TMS320C44 is a lower-cost version of the 'C40 for parallel-processing applications that are more price sensitive. The 'C44 features four communications ports and has an external address reach of 32M words over two external buses. To further reduce cost, the 'C44 comes in a 304-pin PQFP package or a 388-pin BGA. The 'C44 can deliver up to 30 MIPS/60 MFLOPS performance with a maximum I/O bandwidth of 336 Mbytes/s. The 'C44 source code can be used with the 'C40.

Features of the 'C44 include:

- 33- and 40-ns instruction cycle times
- Idle mode for reduced power consumption
- Four communication ports
- 32M-word external address reach
- 6- or 12-channel on-chip DMA
- Optimizing ANSI C compiler
- IEEE floating-point conversion for ease of use
- The 'C44 source code can be used with the 'C40
- 304-pin PQFP package
- 388-pin BGA

TMS320C44 Block Diagram



TMS320C4x CPU

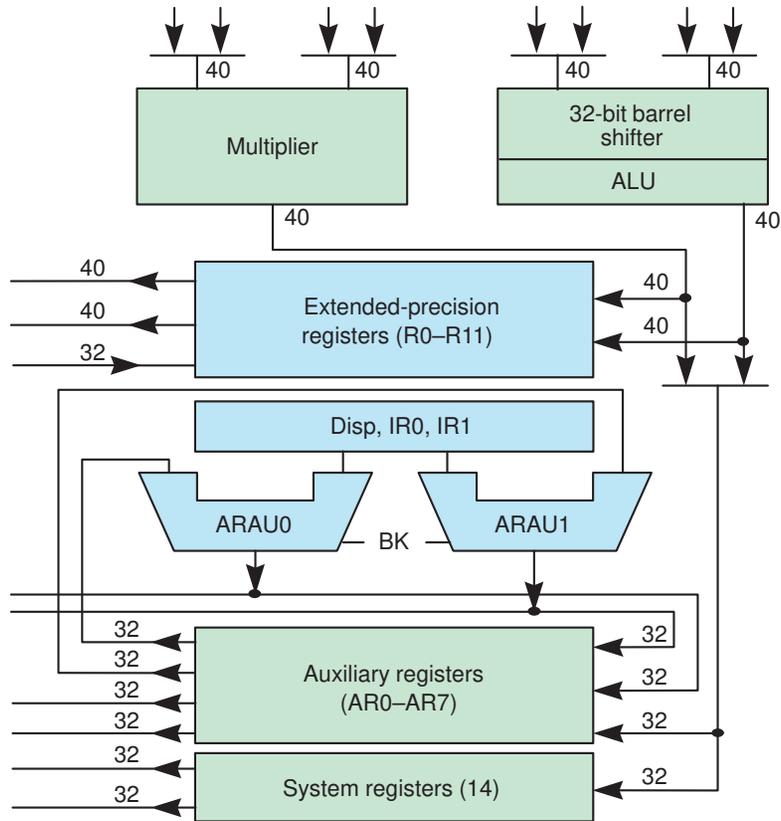
The TMS320C4x has an independent multiplier and accumulator, and achieves up to 60 MFLOPS. Results are stored in any one of 12 extended-precision registers. These are 40-bit registers that store values with a 32-bit mantissa and an 8-bit exponent. These registers can serve as both the source and the destination for any arithmetic operation. The extended-precision registers are an extremely valuable resource for programming in assembly or C. These registers allow you to maintain intermediate results without storing data in memory. This results in higher performance assembly code and a more efficient C compiler.

To sustain 60 MFLOPS, the CPU has two independent auxiliary register arithmetic units (ARAUs), which can generate two addresses in a single cycle. The two ARAUs operate in parallel with the multiplier and ALU. They support addressing with displacements, addressing with index registers (IR0 and IR1), circular addressing, and bit-reversed addressing.

Features of the 'C4x CPU are:

- High-speed internal parallelism: eight operations/cycle for maximum sustained performance
 - Floating-point/integer multiply
 - Floating-point/integer addition
 - Two data accesses
 - Zero-overhead branch and loop counter update
- IEEE floating-point conversion
- Divide and square root support for improved performance
- Single-cycle byte and halfword manipulation capabilities
- Register-based CPU

TMS320C4x CPU Block Diagram



TMS320C4x Memory and Bus Structure

To realize the full performance of the 'C4x CPU, it is important to have a bus and memory architecture that can keep pace. The 'C4x fetches up to four 32-bit words each cycle: a program opcode, two CPU data operands, and a DMA data transfer. The internal buses can transfer all four words in parallel, relying on seven memory sources for data.

The 'C4x uses seven internal buses to access on-chip resources:

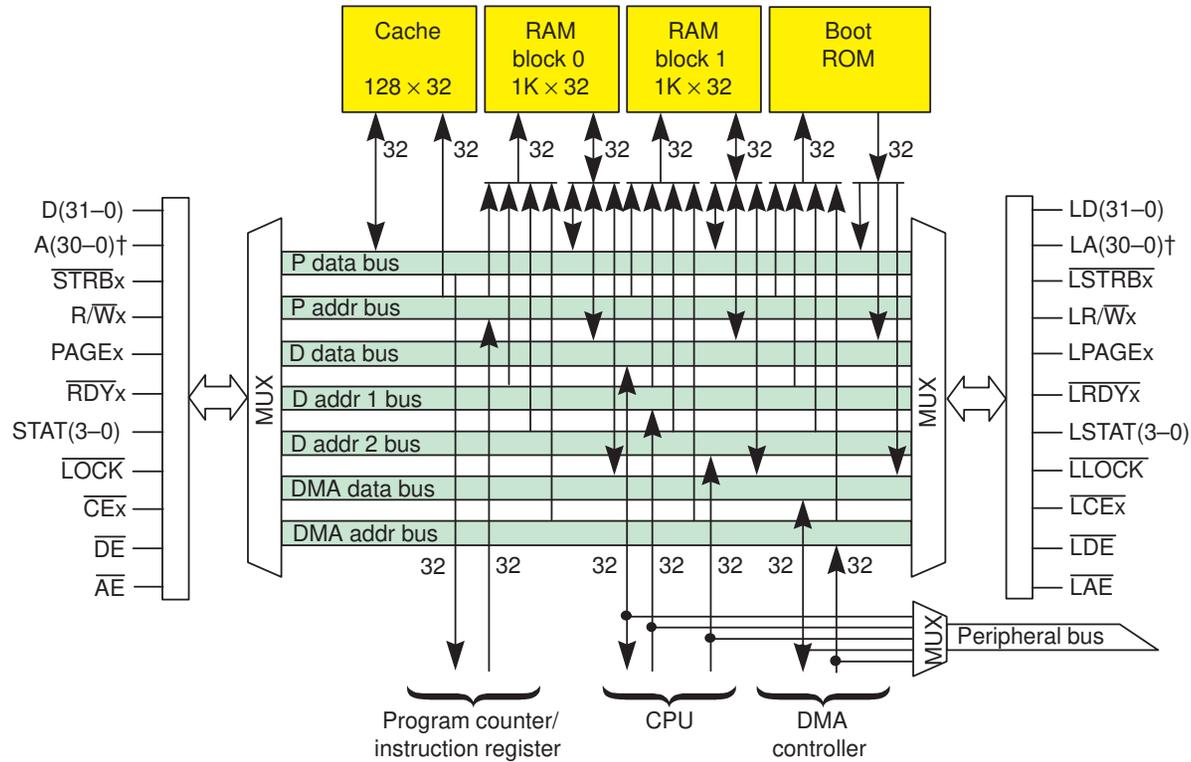
Program address/data: The CPU uses these buses to maintain instruction fetches every cycle.

Data address/data: In any cycle, the CPU can fetch two data operands because it has two data address buses and one data bus that can be accessed twice in a single cycle.

DMA address/data: The DMA uses these buses to perform DMA transfers in parallel with CPU operation.

With the internal buses in place to feed the DMA and CPU, the 'C4x-generation devices can use both internal and external data and program memory. Internally, the 'C4x has two $1K \times 32$ -bit word blocks of dual-access RAM, providing up to four words of program or data in a single cycle. For external memory, the 'C40 has two identical 32-bit buses, which address up to 2G words of memory each. The 'C44 has two 24-bit external address buses, which address up to 16M words each. Each device has an on-chip instruction cache to boost performance when using slower external memory.

TMS320C4x Memory and Bus Structure Block Diagram



† 24-bit address bus in TMS320C44

TMS320C4x Communication Ports

The communication ports on the 'C4x generation transfer up to 24 Mbytes/s each for asynchronous interprocessor communications or for servicing intensive I/O needs. The 'C40 has six ports, and the 'C44 has four. Each port has four control pins and eight data pins. These 12 pins provide a glueless interface to another 'C4x. The control pins, combined with the control logic, arbitrate with another device to determine data transfer timing and direction. Because the communication ports have built-in arbitration and control circuitry, you simply need to read data from and write data to the memory-mapped input and output FIFOs.

In a typical transfer, the DMA coprocessor or the CPU first writes to the output FIFO. Next, the communication port sends a request signal to the destination processor, which responds with an acknowledge. The communication port then transfers the word as four successive bytes. The destination processor receives the word in its input FIFO, where the destination DMA or CPU can read the contents. Note that the input and output FIFOs provide a 16-word \times 32-bit buffer between communications ports.

Features of the 'C4x communication ports include:

- Up to 24 Mbytes/s bidirectional interface on each communication port for high-speed and low-cost parallel-processor interface
- 8-word deep input FIFO and 8-word deep output FIFO buffer
- Automatic arbitration and handshaking for direct processor-to-processor connection

TMS320C4x DMA Coprocessor

With as many as six communication ports and two external buses, the TMS320C4x has an I/O capability of as much as 384 Mbytes. To service this speed, the 'C4x has a 6- or 12-channel DMA which operates independently of the CPU and has dedicated address and data buses to avoid bus conflicts.

The DMA is programmed to transfer data from one memory location to another (communication ports are memory-mapped). The DMA can begin a task based on CPU or external interrupts and can interrupt the CPU at the completion of a task. The DMA also includes a link pointer register that allows the DMA to program its next task without CPU intervention.

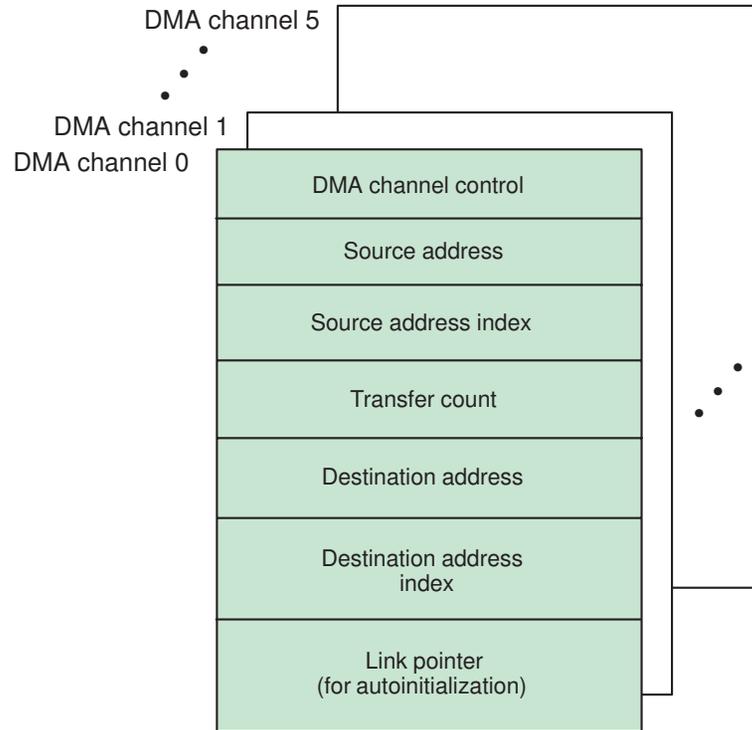
Since each communication port has transmit and receive capability, 12 DMA channels are needed if all six communication ports are being used in a bidirectional mode. The DMA has a split-mode operation dedicated to this function, allowing it to service the 12 input and output FIFOs in the communication ports.

In the event that both the CPU and DMA are accessing the same resource, priorities can be assigned to the CPU, the DMA, or mixed, where the CPU gets the first access followed by the DMA, to resolve the conflict.

The 'C4x DMA coprocessor features:

- Concurrent I/O to maximize sustained CPU performance
- Autoinitialization
- Up to 6 or 12 DMA channels for parallel data transfers
 - Data transfers to and from anywhere in memory
 - Three operations/cycle
 - 32-bit data transfer
 - Address register update
 - Transfer counter update
 - Performance up to 90 MOPS

TMS320C4x DMA Coprocessor Block Diagram



TMS320C4x Generation Summary

This table gives a 'C4x-generation product summary so you can choose the best combination of performance, memory, power, package, and peripherals for your system.

TMS320C4x Generation Summary Table

Data Type	Device	Cycle Time (ns)	Memory On-Chip		Memory Off-Chip	Peripherals			On-Chip Timers	Package
			RAM (Words)	ROM (Words)		Parallel Bus	Comm Ports	DMA Coprocessor		
point	TMS320C40-50†	40	2K × 32	Boot	4G × 32	2 ext.	6	6/12 channels	2	325-pin PGA
32-bit	TMS320C40-60	33	2K × 32	Boot	4G × 32	2 ext.	6	6/12 channels	2	325-pin PGA
word	TMS320C44-50	40	2K × 32	Boot	32M × 32	2 ext.	4	6/12 channels	2	304-pin PQFP/388-pin BGA
	TMS320C44-60	33	2K × 32	Boot	32M × 32	2 ext.	4	6/12 channels	2	304-pin PQFP/388-pin BGA

† Military version available

‡ Extended temperature version available

TMS320C5x Generation

The 'C5x generation performs 20-50 million instructions per second (MIPS). The 3-V versions maintain 40 MIPS performance and reduce power consumption to 1.15 mA/MIPS. For more information on power consumption, TI provides the *Calculation of TMS3205x Power Dissipation Application Report* (SPRA030).

The 'C5x generation offers devices with a variety of memory mixes and peripheral options.

The standard synchronous, double-buffered serial port operates at up to 12.5 Mbps with independent transmit and receive sections. The time-division multiplexed (TDM) serial port has all of the same features as the standard serial port, yet TDM features make the serial port well suited for interprocessor communication in multiprocessor DSP systems. The buffered serial port (BSP) operates at up to 40 Mbps with no CPU intervention. The host port interface (HPI) is an 8-bit parallel port used to interface a host processor to the 'C5x.

Multiple on-chip phase-locked loop (PLL) options are available depending upon which 'C5x is used. The on-chip PLL allows lower frequency clocks, reducing power and electromagnetic emissions.

For systems requiring significant off-chip resources, the 'C5x family addresses 64K 16-bit words externally in program, data, and I/O spaces; each space has its own pin.

TMS320C5x

The TMS320C5x accepts source code from the 'C1x, 'C2x, and 'C2xx generations. Faster cycle times, on-chip memories, a parallel logic unit (PLU), zero-overhead context switching, and block repeats differentiate the 'C5x. The integration of the IEEE 1149.1 (JTAG) test bus increases system reliability, allowing 99% fault grade testing and on-chip emulation. There is also an ANSI C compiler designed for the 'C5x, which translates the widely used ANSI C language directly into highly optimized assembly language for the 'C5x.

TMS320C5x Enhancements

- 20-, 25-, 35-, and 50-ns instruction cycle times
- Zero-overhead context switching
- Parallel logic unit (PLU) for fast bit manipulation
- Up to 32K words on-chip memory
- IEEE 1149.1-standard (JTAG) scan-path test bus for system test and emulation
- Zero-overhead block repeats
- Delayed branch, call, and return instructions
- Two indirectly addressed circular buffers
- Software wait-state generation
- Various phase-locked loop (PLL) options for reduced EMI and system power dissipation

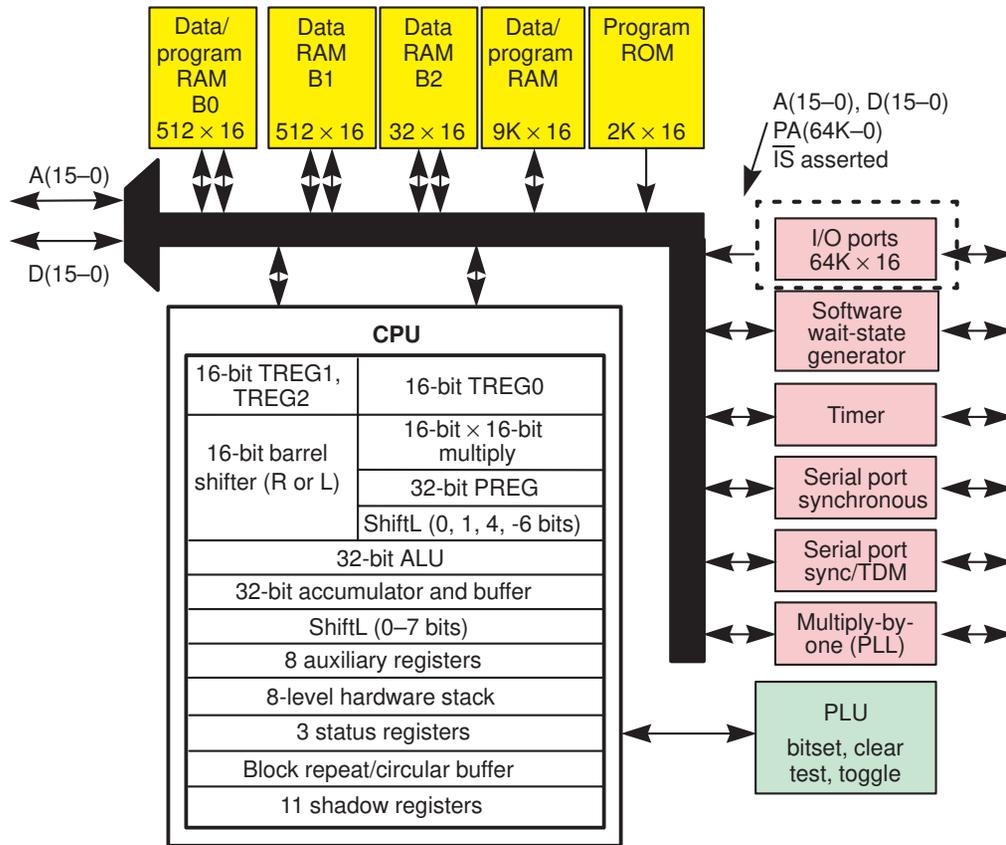
TMS320C50

The TMS320C50 is a highly integrated DSP, offering a complete system on a single chip. With a boot ROM and 10K 16-bit words of on-chip RAM, an entire DSP system can be integrated into the 132-pin QFP package. By integrating the memory on chip, you reduce both power and board space. Integrating the off-chip memory can be especially important in high-performance systems to eliminate expensive high-speed SRAM.

Features of the 'C50 include:

- 25-, 35-, and 50-ns instruction cycle times
- 192K-word external address reach
- Accepts source code from the 'C1x/'C2x/'C2xx generations
- ANSI C compiler
- IEEE 1149.1-standard (JTAG) emulator control
- Standard boot loader
- Full-duplex synchronous serial port
- Time-division multiplexed (TDM) serial port
- 132-pin BQFP package

TMS320C50 Block Diagram



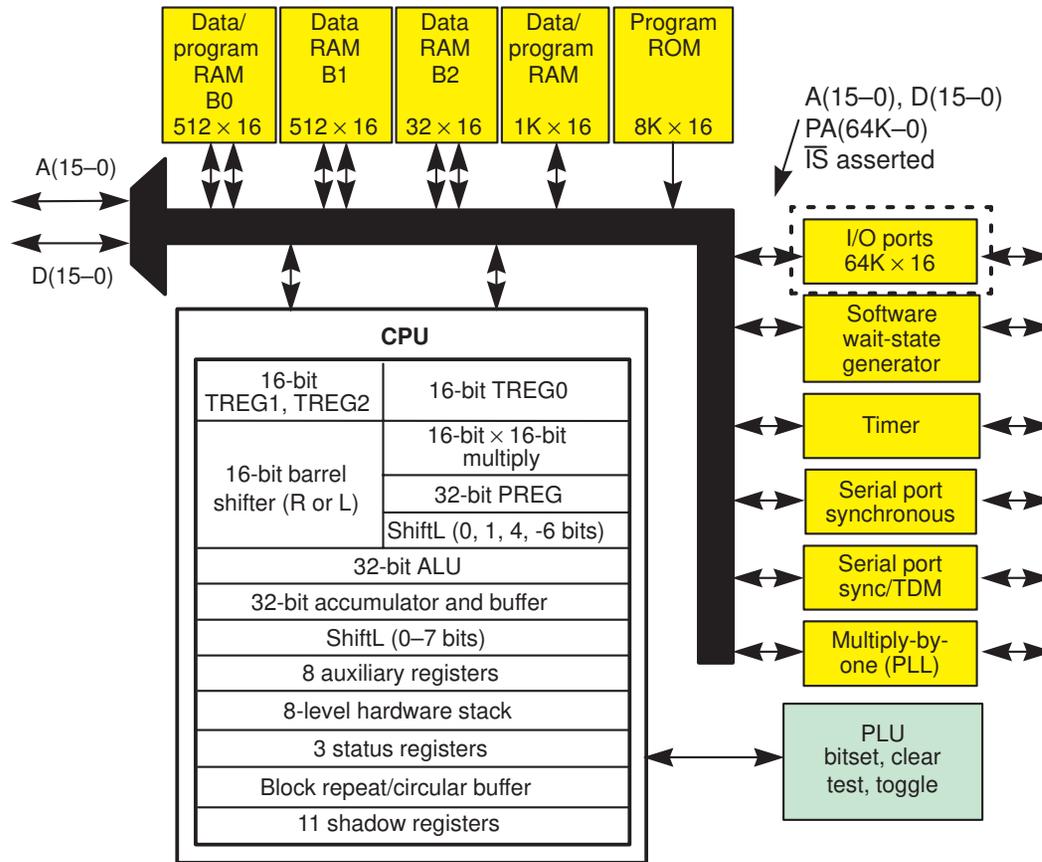
TMS320C51

In the TMS320C51, the 'C50's 9K-word block of RAM is replaced by 8K 16-bit words of on-chip ROM. This provides a considerable advantage in cost and performance for those who require large amounts of on-chip program space. With this ROM and 2K 16-bit words of RAM, sophisticated DSP algorithms can fit on a single device. This device is available in a 132-pin BQFP and a 100-pin TQFP that measures only 14 × 14 × 1.4 mm, for designs that require both small board area and reduced height.

Features included on the 'C51 are:

- 20-, 25-, 35-, and 50-ns instruction cycle times
- 192K-word external address reach
- Accepts source code from the 'C1x/'C2x/'C2xx generations
- ANSI C compiler
- IEEE 1149.1-standard (JTAG) emulator control
- Boot ROM option
- Full-duplex synchronous serial port
- TDM serial port
- 132-pin BQFP and 100-pin TQFP packages

TMS320C51 Block Diagram



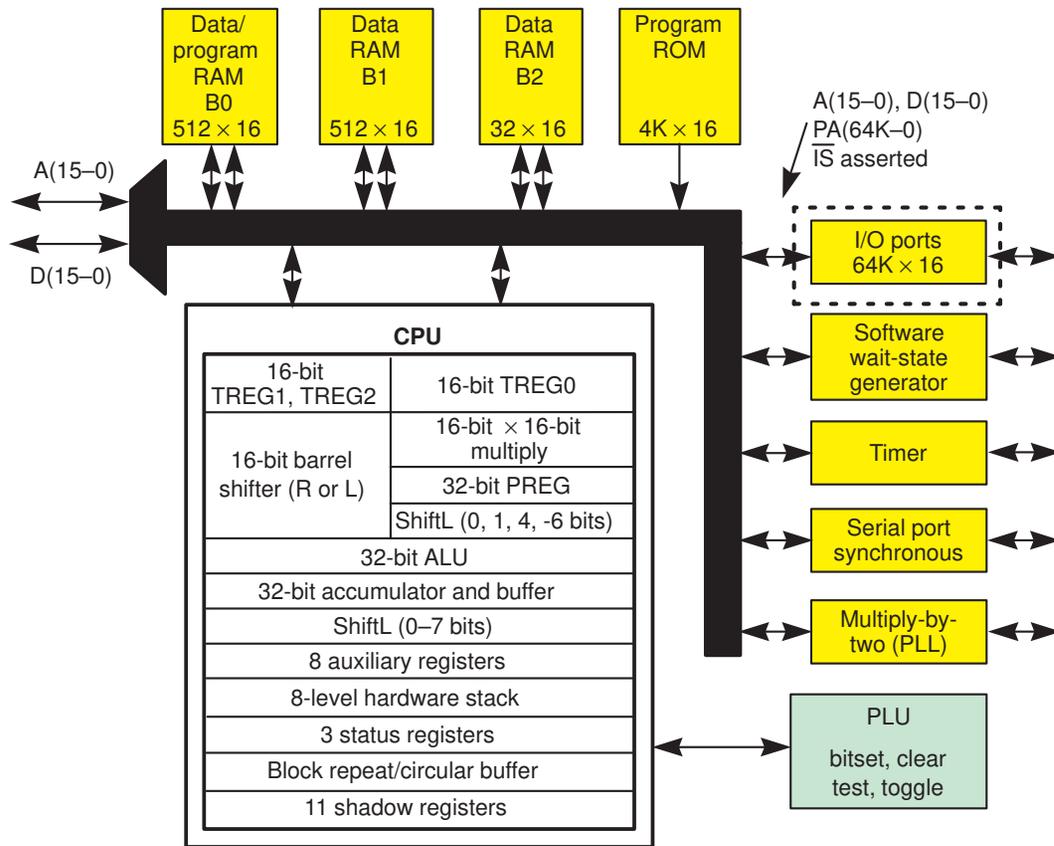
TMS320C52

The TMS320C52 has a superb combination of both low cost and high performance. Traditionally, devices in the same price range have offered 10 MIPS performance. The 'C52 provides twice the performance (20 MIPS) and room to grow into a 50-MIPS version. The 4K 16-bit words of ROM can be configured with your code or purchased preprogrammed with a boot loader.

Additional features of the 'C52 include:

- 20-, 25-, 35-, 40-ns, and 50-ns instruction cycle times at 5V
- 192K-word external address reach
- Accepts source code from the 'C1x/'C2x/'C2xx generations
- ANSI C compiler
- IEEE 1149.1-standard (JTAG) emulator control
- Boot ROM option
- Full-duplex synchronous serial port
- 100-pin BQFP and TQFP packages
- 3.31-V version

TMS320C52 Block Diagram



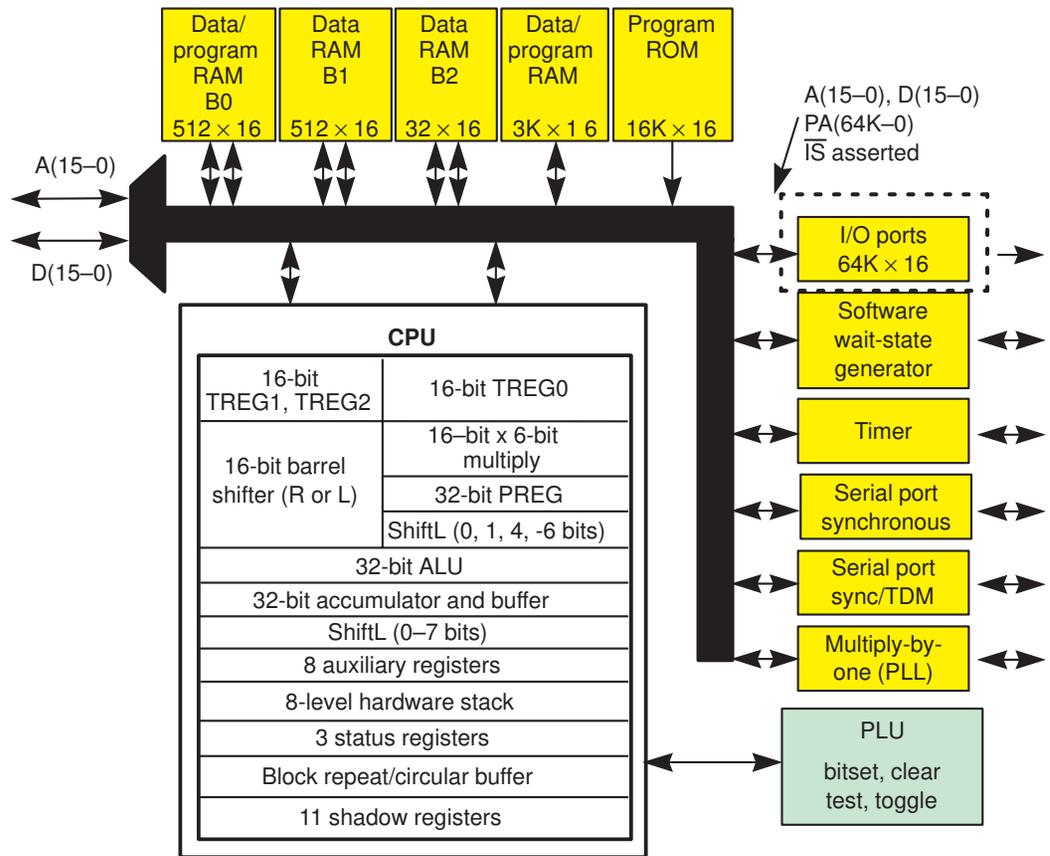
TMS320C53

The TMS320C53 provides greater integration of on-chip ROM than the 'C51. With 16K 16-bit words of on-chip ROM and 4K 16-bit words of on-chip RAM, an entire DSP system can be integrated into the 132-pin BQFP package. By bringing the memory on-chip, TI reduces both power and board space; on-chip memory also provides a considerable advantage in cost and performance.

The 'C53 features:

- 25-, 35-, and 50-ns instruction cycle times at 5V
- 192K-word external address reach
- Accepts source code from the 'C1x/'C2x/'C2xx generations
- ANSI C compiler
- IEEE 1149.1-standard (JTAG) emulator control
- Boot ROM option
- Full-duplex synchronous serial port
- TDM serial port
- 132-pin BQFP package

TMS320C53 Block Diagram



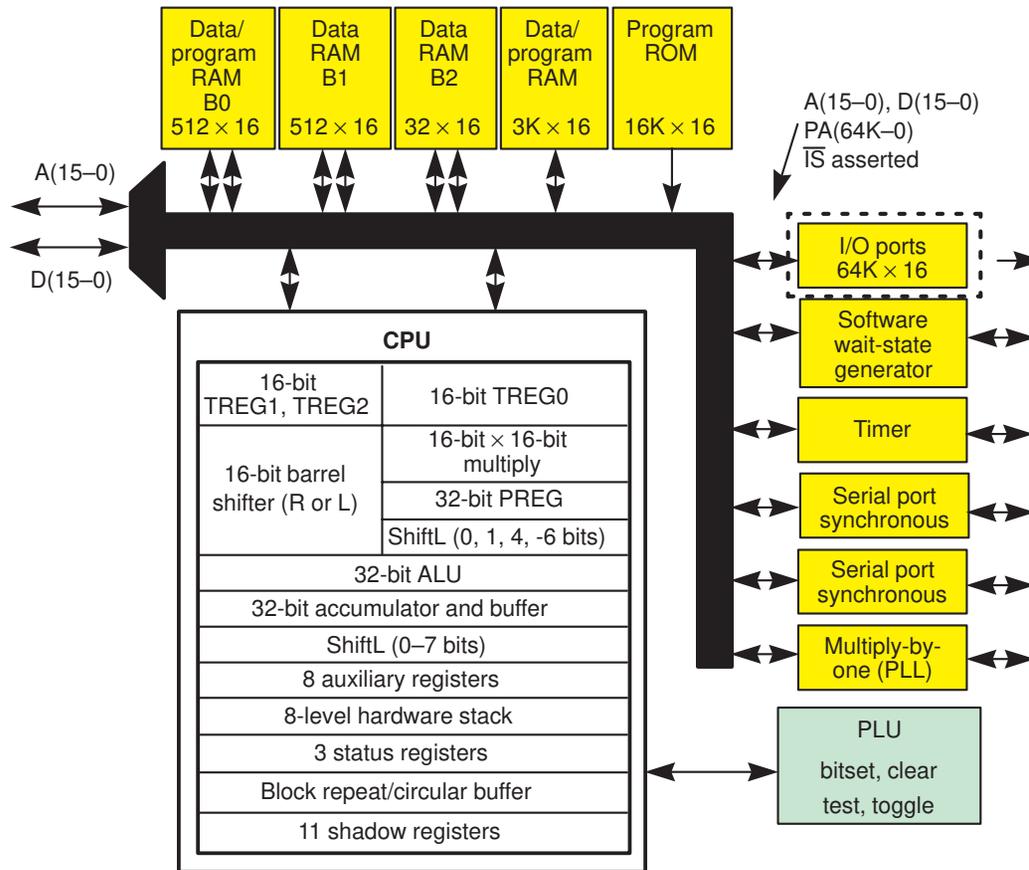
TMS320C53S

There are slight differences between the 'C53 and the 'C53S. In order to accommodate the integration capabilities of the 'C53 into a 100-pin TQFP package, some features were removed from the standard 'C53. The 'C53S offers two standard serial ports instead of the TDM and standard serial ports in the 'C53. The 'C53S has reduced capability of the on-chip analysis block and has no boundary scan.

Features included on the 'C53S are:

- 25-, 35-, and 50-ns instruction cycle times at 5V
- 192K-word external address reach
- Accepts source code from the 'C1x/'C2x/'C2xx generations
- ANSI C compiler
- IEEE 1149.1-standard (JTAG) emulator control
- Boot ROM option
- Full-duplex synchronous serial port
- 100-pin TQFP package
- 40-ns (TMSLC320C53S) 3.3-V version

TMS320C53S Block Diagram



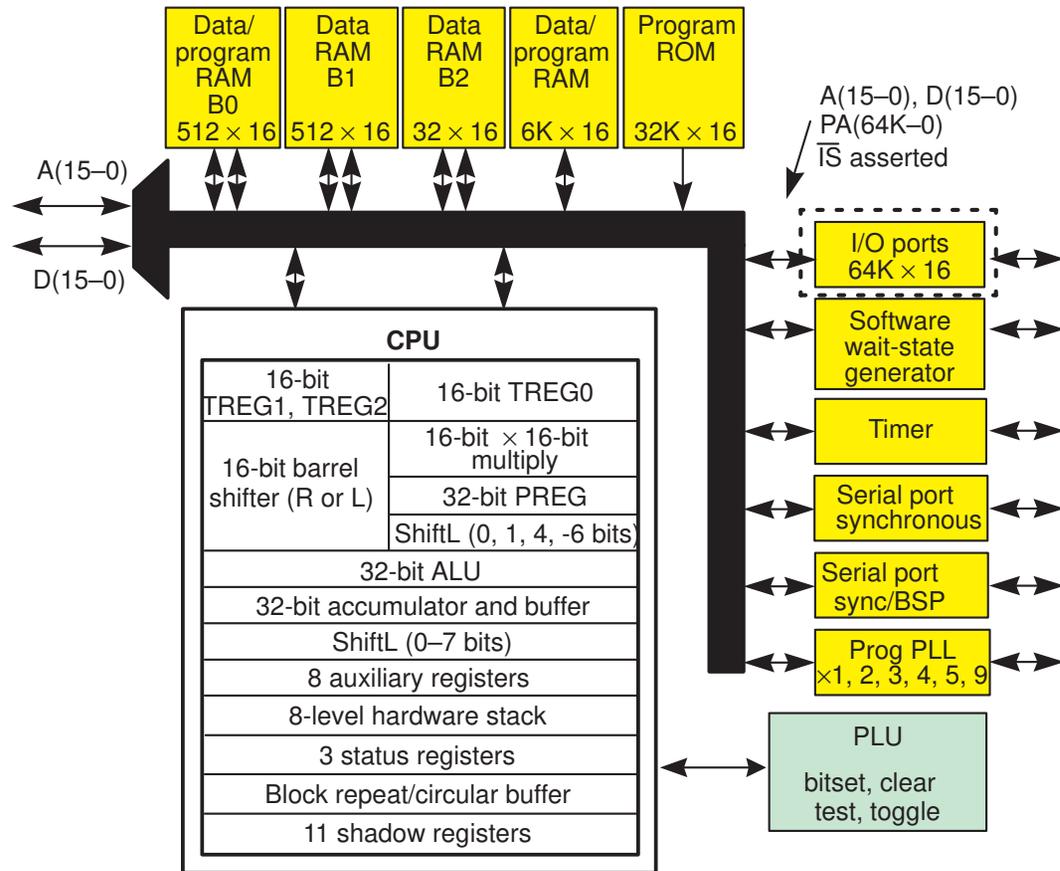
TMS320LC56

The TMS320LC56 provides greater integration of on-chip ROM than the 'C53. With 32K 16-bit words of on-chip ROM and 7K 16-bit words of on-chip RAM, the 'LC56 can accommodate large program and data spaces on-chip, minimizing off-chip accesses. The 'LC56 also provides a very fast buffered serial port (BSP) capable of 40 Mbps at 25-ns instruction cycle time. The 'LC56 is optimized for high-performance, low-power applications; as a result, it operates at 3.3 V only.

Key features of the 'LC56 are:

- 25-, 35-, and 50-ns instruction cycle times at 3.3 V
- 192K-word external address reach
- Accepts source code from the 'C1x/'C2x/'C2xx generations
- ANSI C compiler
- IEEE 1149.1-standard (JTAG) emulator control
- Programmable PLL
- Full-duplex synchronous serial port
- Buffered serial port with dedicated bus
- 100-pin TQFP package

TMS320LC56 Block Diagram



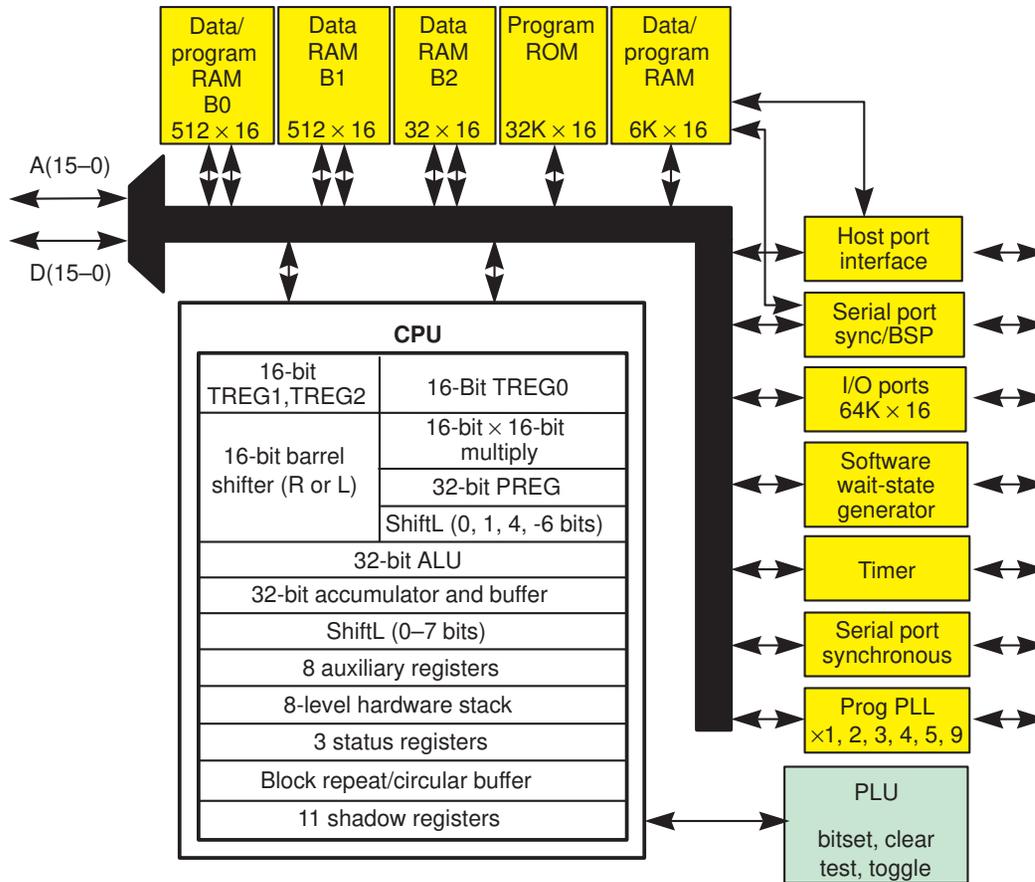
TMS320LC57

The TMS320C57 incorporates the same amount of on-chip memory as the 'LC56 and offers a high-throughput buffered serial port (BSP). In addition, the 'LC57 provides an 8-bit wide host port interface (HPI) which can be used to communicate with other 'LC57 devices or embedded microprocessors. The 'LC57, like the 'LC56, is capable of a 25-ns instruction cycle time at 3.3 V.

The 'LC57 features:

- 25-, 35-, and 50-ns instruction cycle times at 3.3 V
- Boot load through HPI or standard serial port
- 192K-word external address reach
- Accepts source code from the 'C1x/'C2x/'C2xx generations
- ANSI C compiler
- IEEE 1149.1-standard (JTAG) emulator control
- Boot ROM option
- Full-duplex synchronous serial port
- Programmable PLL
- Buffered serial port with dedicated bus
- Host port interface with dedicated bus
- 128-pin TQFP package

TMS320LC57 Block Diagram



TMS320C57S

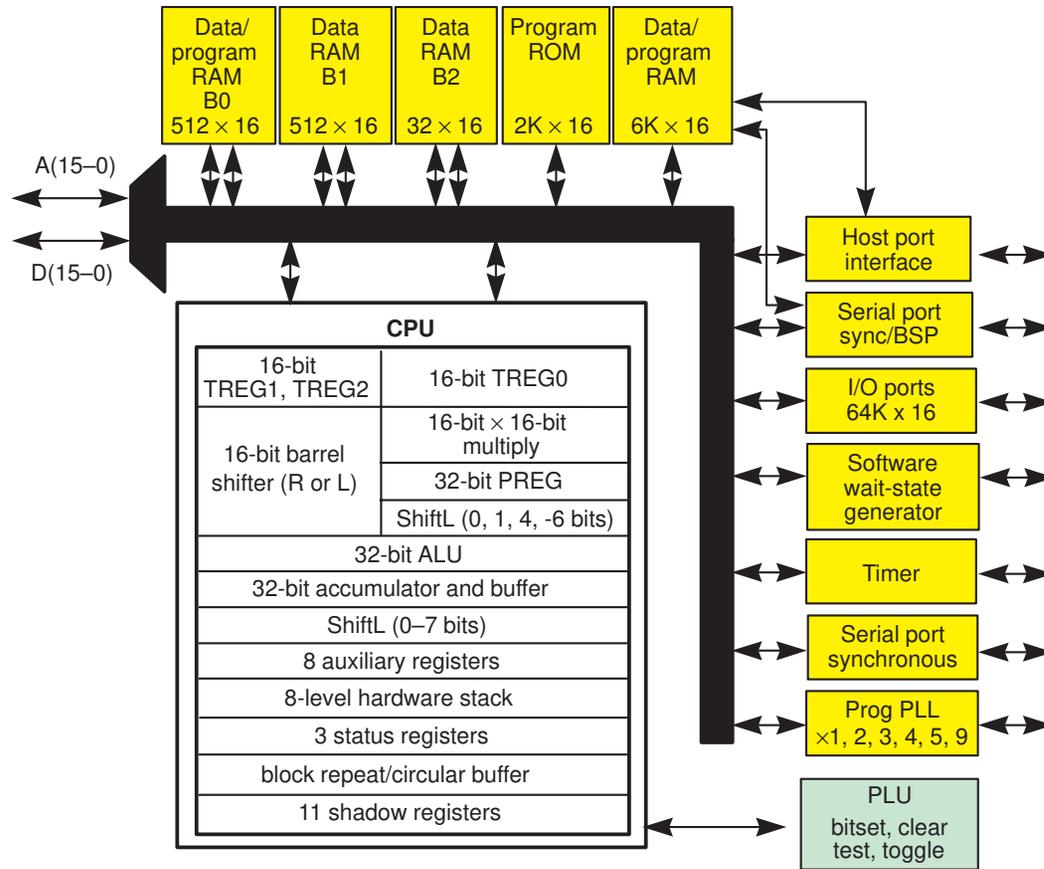
The TMS320C57S takes advantage of the same peripherals that are on the 'LC57 to make the 'C57S a cost-effective embedded data I/O engine. In order to provide a broad-based appeal, the 'C57S differs from the 'LC57 in four ways:

- The 32K 16-bit words of ROM space has been replaced with a boot ROM
- The 'BC57S can operate at 5V
- The 144-pin package of the 'BC57S has a wider lead pitch than the package of the 'LC57
- The 'BC57S is lower in cost

Features of the 'C57S include:

- 25-, 35-, and 50-ns cycle times at 5V
- Standard boot loader
- 7K-word RAM
- Boot load through HPI or standard serial port
- 192K-word external address reach
- Accepts source code from the 'C1x/'C2x/'C2xx generations
- ANSI C compiler
- IEEE 1149.1-standard (JTAG) emulator control
- Full-duplex synchronous serial port
- Buffered serial port with dedicated bus
- Host port interface with dedicated bus
- 144-pin TQFP package

TMS320C57S Block Diagram



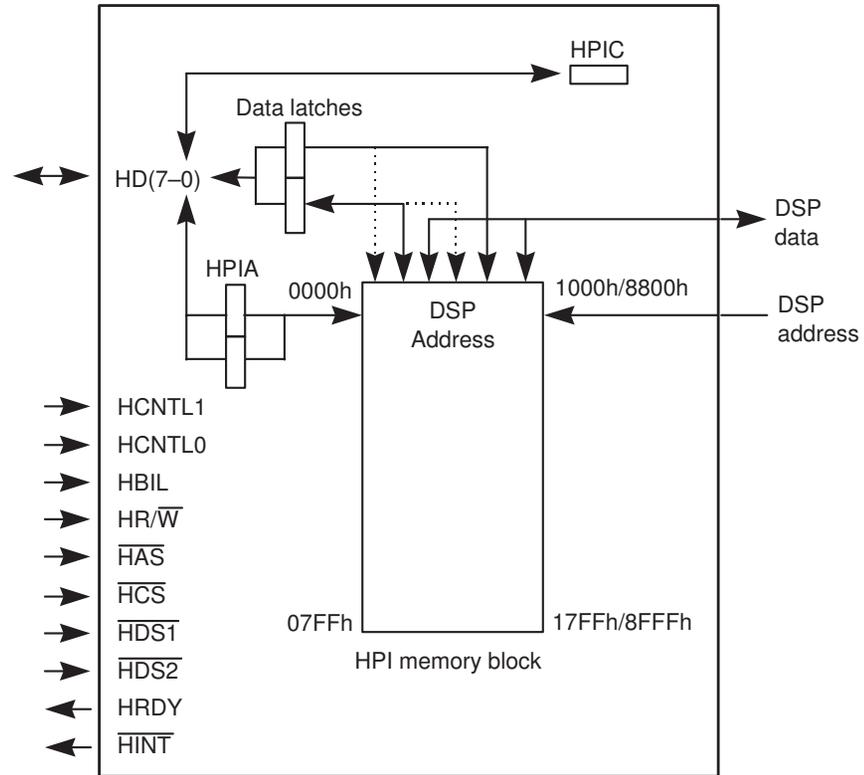
TMS320LC57/'C57S Host Port Interface

The host port interface (HPI) is an 8-bit parallel port available on the TMS320LC57 and the TMS320C57S. The HPI provides a glueless interface to standard microprocessors as well as to other TI devices. The HPI appears as a 2K-word block of shared memory that is available in either a FIFO or standard random-access configuration. Most importantly, the HPI has the ability to maintain its high level of functionality as the interface between an external CPU and the 'C57, even while the 'C57 is idle or in reset. This significantly reduces system power consumption by offloading standard I/O tasks from the DSP.

Features of the HPI include:

- Byte-wide register addressability
- 8-bit parallel port
- High-speed back-to-back accesses
- Dedicated bus to a 2K 16-bit words of SARAM
- Shared-access mode (SAM)
 - Normal mode of operation
 - Allows DSP and host to have HPI memory access
 - Asynchronous host accesses are resynchronized internally
 - 45.7 Mbps at 57 MHz
 - 64.0 Mbps at 80 MHz
- Host-only mode (HOM)
 - Allows host to access HPI memory while 'C57 is in IDLE2 or in reset mode
 - 5 μ A power dissipation (IDLE2)
 - 160 Mbps, independent of clock

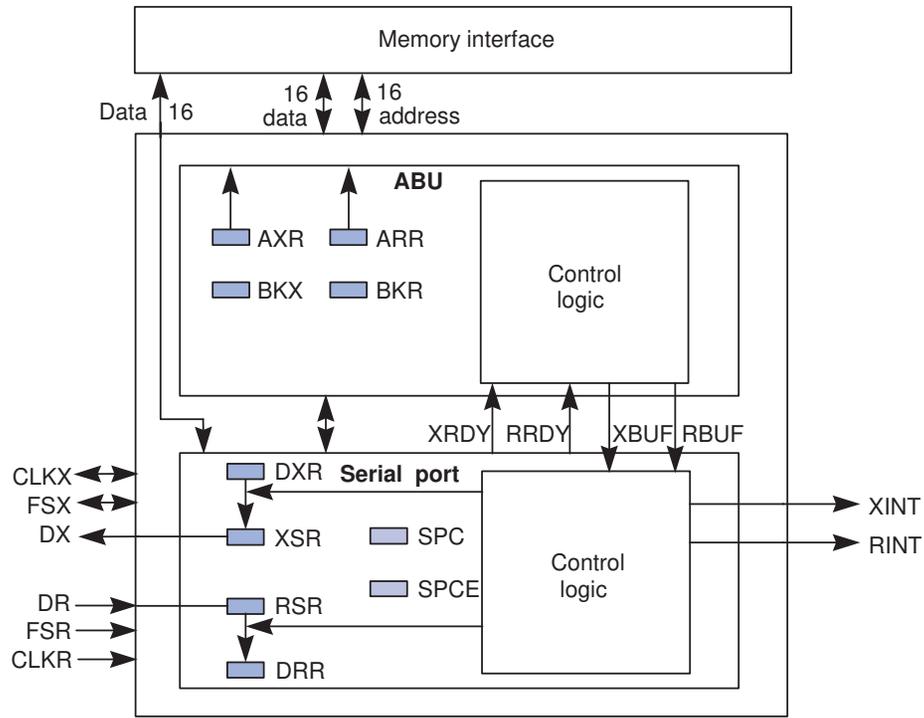
TMS320LC57/C57S Host Port Interface Block Diagram



TMS320LC56/'LC57/'C57S Buffered Serial Port

The buffered serial port (BSP) provides a no-overhead mechanism to interface serially with CODECs, ADCs, and other peripherals. The BSP supports 8-, 10-, 12-, and 16-bit serial data packets and uses a 2K-byte buffer to hold input or output data. Downward code compatible with the standard serial ports, the BSP is designed to be completely flexible and programmable. The BSP has the ability to simultaneously receive data from and transmit data to a programmable on-chip buffer via a dedicated memory bus, freeing the CPU to execute other tasks without memory bus contention.

TMS320LC56/'LC57/'C57S BSP Block Diagram



TMS320C5x Multiplier/ALU Features

The performance and parallelism of the 'C5x architecture become evident by studying the multiplier and accumulator sections of the device. The on-chip multiplier performs a 16-bit \times 16-bit multiply with a 32-bit product in a single cycle.

To double the performance, the 'C5x devices can fetch two data operands when executing the multiply and accumulate (MAC) instruction.

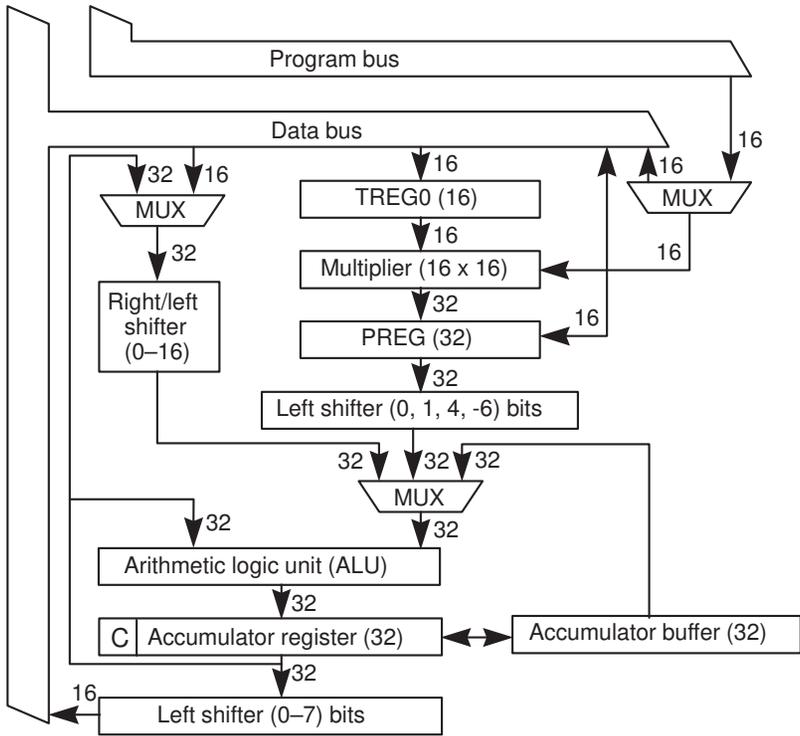
Scaling and fractional math shifts occur in parallel with all arithmetic operations.

The 'C5x devices are the first to include an accumulator buffer. The accumulator buffer provides quick comparisons to the accumulator contents to determine the minimum or maximum in a table of values, a common operation for both general-purpose and DSP algorithms. This is very useful in implementing Viterbi-decoding algorithms. Additionally, the accumulator buffer allows quick temporary storage of a commonly referenced value, which eliminates the extra cycles it takes to store the value in memory. It also allows up to 65 bit shifts among accumulator, accumulator buffer, and carry.

Features of the 'CC5x multiplier/ALU include:

- Single-cycle 16-bit \times 16-bit multiply, yielding a 32-bit product
- Can access program and two data operands simultaneously
- CPU performs simultaneous ALU and multiplier operations
- Zero-overhead shift registers
- Accumulator buffer with path back into ALU

TMS320C5x Multiplier/ALU Features Block Diagram



TMS320C5x Parallel Logic Unit

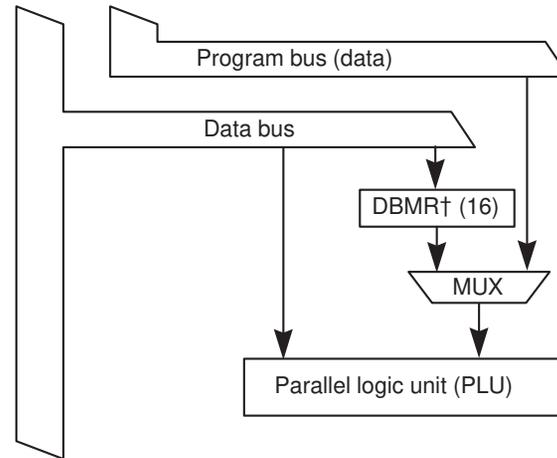
The parallel logic unit (PLU) performs logical operations without corrupting the ALU contents. This allows data to be checked and decisions made without the overhead of storing and restoring the ALU content.

The PLU supports AND, OR, XOR, and compare functions. These functions are commonly used to set, clear, and toggle bits within a data-memory location. To make these functions easy to use, dedicated instructions perform them, using either immediate or register data to compare with the data-memory location.

Features of the 'C5x PLU are:

- Performs logical operations without disturbing arithmetic registers in ALU
- Sets, clears, and toggles any number or combinations of bits in data memory
- Compares bits individually or collectively
- Supports long immediate and register values

TMS320C5x Parallel Logic Unit Block Diagram



PLU Instructions

Mnemonic	Description
APL #	AND DBMR†/constant with data memory
CPL #	Compare DBMR/constant with data memory
OPL #	OR DBMR/constant with data memory
XPL #	XOR DBMR/constant with data memory
SPLK #	Store long immediate to data memory

†DBMR: Dynamic bit-manipulation register

TMS320C5x Interrupts

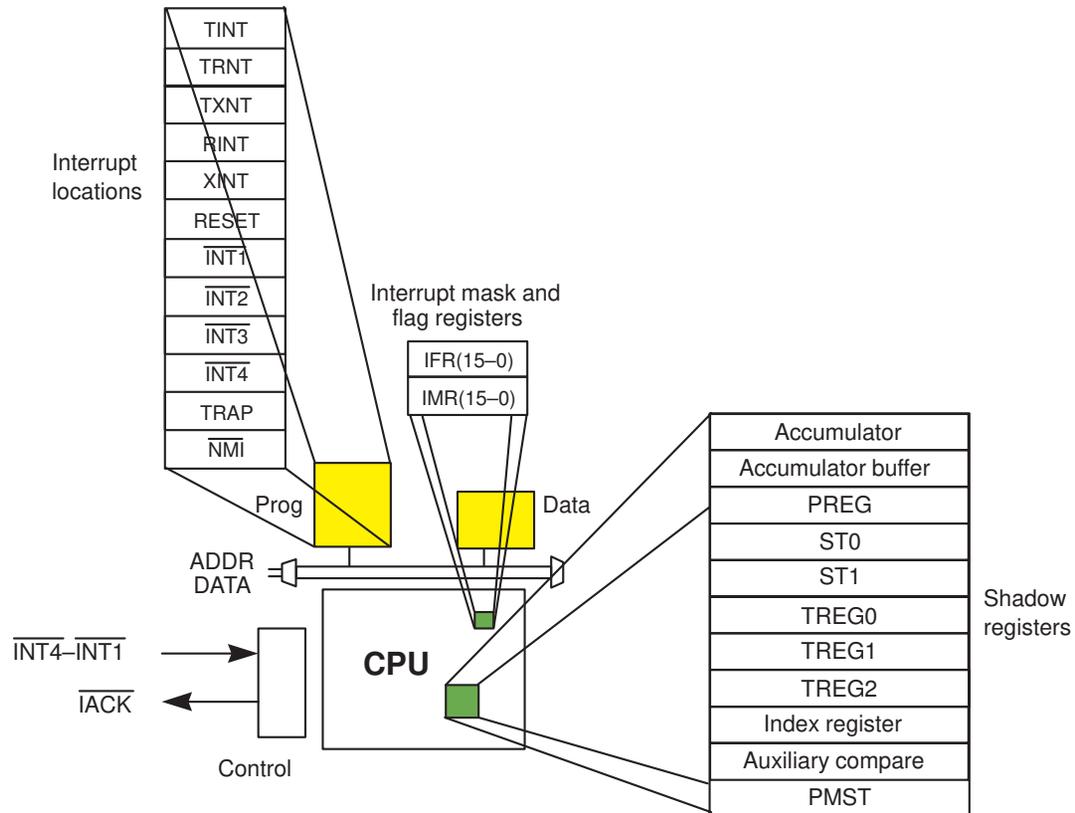
The TMS320C5x supports four external interrupts, two serial port interrupts, one timer interrupt, and a trap instruction.

To speed up interrupt service routines (ISR), the key registers are shadowed with a 1-level deep stack and are saved in a single cycle. This saves 22 cycles when an interrupt occurs by eliminating the need to push and pop these 11 registers.

The 'C5x interrupt features include:

- Interrupt sources: four external, two serial ports, one timer, one trap instruction
- 1-level deep stack on strategic registers for zero-overhead context switching
- Program-accessible interrupt flag register for software interrupt polling
- Automatic global interrupt enable on return from interrupt service routine
- Interrupt vectors are relocatable

TMS320C5x Interrupts Block Diagram



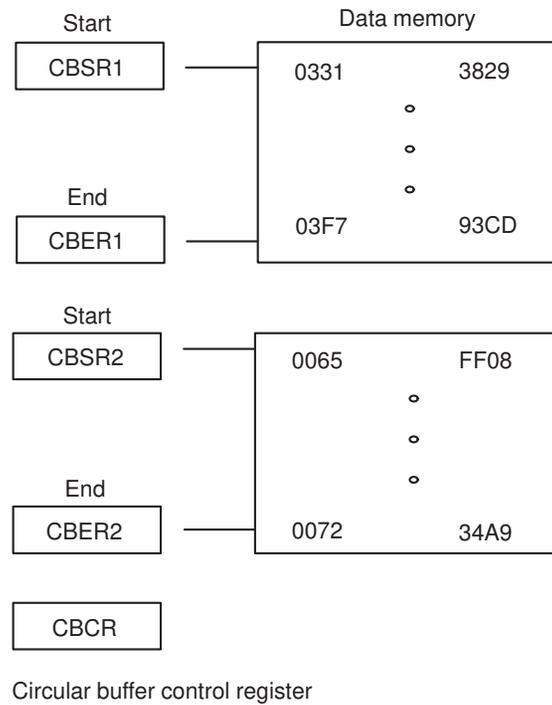
TMS320C5x Circular Addressing

Circular addressing is a method to address *aging* data sets for common DSP algorithms. For example, after performing the first set of calculations on an FIR filter data set, a new data value must be brought in and the oldest value discarded. DMOV allows you to do this by treating data in a circular fashion, with the oldest and newest values located side by side. At the end of each calculation, a new data value is placed in memory at the location of the oldest value. You update the circular buffer start address to correspond to the newest value and the circular buffer end address to correspond to the oldest value.

Circular addressing features:

- Two circular addressing data buffers
- Auxiliary registers are memory-mapped to indirectly address each circular buffer
- Effective use of data-memory space while increasing performance

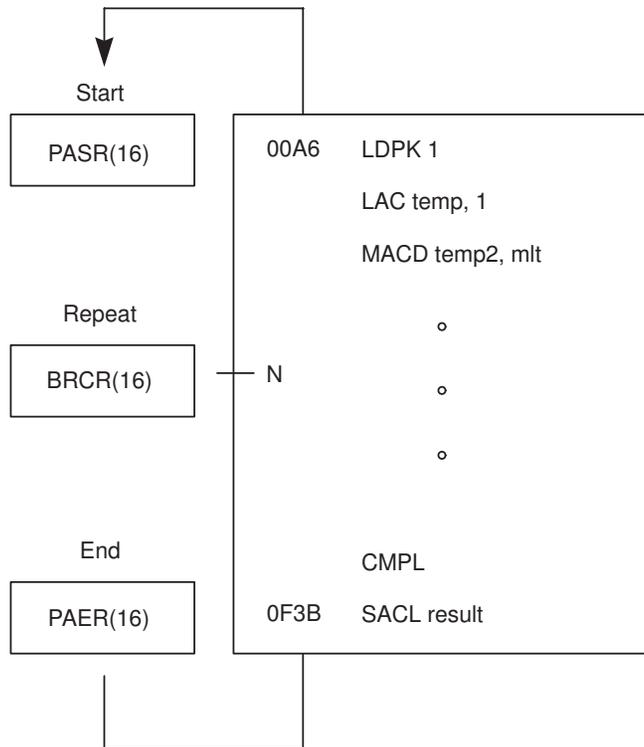
TMS320C5x Circular Addressing Block Diagram



Repeat and Block Instructions

The TMS320C25 was the first device to offer a zero-overhead looping instruction, the RPT instruction. The 'C5x expands this capability with the RPTZ and RPTB instructions. The RPTZ command is a logical extension of the RPT command that also clears the accumulator and product registers. This saves two cycles in typical routines. The repeat block instruction (RPTB) allows you to repeat a block of code up to 64K times without any overhead required to branch to the beginning of the code segment. This allows you to benefit from a faster instruction cycle (due to the pipeline) without paying a penalty for program discontinuity.

Repeat and Block Instructions Block Diagram



RPT: Repeat next instruction—number specified by a long immediate constant

RPTZ: Clear accumulator and PREG and repeat instruction—number specified by a long immediate constant

RBTB: Repeat block of code up to 65536 times

TMS320C5x Generation Summary

All TMS320C5x devices share the same CPU architecture and accept source code from all 'C1x, 'C2x, and 'C2xx devices.

This table gives a 'C5x-generation product summary so that you can choose the best combination of performance, memory, power, package, and peripherals for your system.

TMS320C5x Generation Summary Table

Device	Cycle Time (ns)	Voltage (V)	On-Chip ROM (Words)	On-Chip RAM (Words)	External Address Range	Peripherals			Package
						Serial Port(s)	HPI	Timers	
TMS320C50†	25/35/50	5.0V	2K	10K	192K	2‡	–	1	132-pin BQFP
TMS320LC50	25/40/50	3.3V	2K	10K	192K	2‡	–	1	132-pin BQFP
TMS320C51	20/25/35/50	5.0V	8K	2K	192K	2‡		1	100-pin TQFP 132-pin BQFP
TMS320LC51	25/40/50	3.3V	8K	2K	192K	2‡	–	1	100-pin TQFP 132-pin BQFP
TMS320C52	20/25/35/50	5.0V	4K	1K	192K	1§	–	1	100-pin TQFP 100-pin TQFP
TMS320LC52	25/40/50	3.3V	4K	1K	192K	1§	–	1	100-pin TQFP 100-pin TQFP
TMS320C53	25/35/50	5.0V	16K	4K	192K	2‡	–	1	132-pin BQFP
TMS320LC53	25/40/50	3.3V	16K	4K	192K	2‡	–	1	132-pin BQFP
TMS320C53S	25/35/50	5.0V	16K	4K	192K	2‡	–	1	100-pin TQFP
TMS320LC53S	25/40/50	3.3V	16K	4K	192K	2§	–	1	100-pin TQFP
TMS320LC56	25/35/50	3.3V	32K	7K	192K	2¶	–	1	100-pin TQFP
TMS320LC57	25/35/50	3.3V	32K	7K	192K	2¶	1	1	128-pin TQFP
TMS320C57S	25/35/50	5.0V	Boot	7K	192K	2¶	1	1	144-pin TQFP
TMS320LC57S	35/50	3.3V	Boot	7K	192K	2¶	1	1	144-pin TQFP

† Military version available

‡ =Standard serial port and TDM serial port

§ =Standard serial port

¶ =Standard serial port and 1 buffered serial port

TMS320C54x Generation

The TMS320C54x generation of DSPs integrate functions to improve performance, lower chip count, and reduce power consumption to enable greater system cost savings. The devices combine high-performance, a large degree of parallelism, and a specialized instruction set to effectively implement a variety of complex algorithms and applications.

Features include a Viterbi accelerator, four internal buses, dual-address generators, 40-bit adder, two 40-bit ALUs, eight auxiliary registers, and a software stack.

TMS320C54x Enables High Performance, Emerging Applications

The 'C54x architectural efficiencies — high MIPS and low power dissipation — make it an ideal device for a variety of wireless and wireline communications systems. Standard wireless applications like cellular handsets can take advantage of the 'C54x's power-down modes, high performance, and large ROM memory spaces for integrating entire algorithms on chip. The high performance and large RAM are useful for reconfigurable systems where a variety of different algorithms must be executed from on-chip memory. Data communications or telephony applications can increase the functionality of their systems while lowering systems costs by allowing the 'C54x to absorb the existing system functionality of multiple-DSP implementations.

TMS320C54x Enables High Performance, Emerging Applications

- Digital cellular basestations
- Personal communications systems (PCS)
- V.34/ISDN modems
- Mobile radios
- Personal digital assistants (PDAs)
- Networking
- T1/E1 or PBX trunks
- Wireless data (CDPD)
- Wireless handsets (TDMA or CDMA standards)
- Digital Cordless (DECT, CT2, PHS)
- Pagers
- Satellite modems
- Voice-over internet protocol
- Multifunction telephony line cards in LAN
- Wireless local loop
- Multimedia/telephony integration (fax/data + 3-D sound, etc.)
- Cable modems
- Set-top boxes

TMS320C54x CPU Key Features

The TMS320C54x and TMS320LC54x fixed-point digital signal processors are fabricated with an advanced modified Harvard architecture that has one program memory bus, three data memory buses, and four address buses. The core's key features include a 17-bit \times 17-bit multiplier (16-bit signed or unsigned), a dedicated 40-bit adder for nonpipelined MAC (multiply/accumulate) operation, a separate 40-bit ALU for increased parallelism, two 40-bit accumulators, and a compare, select, store unit (Viterbi accelerator). The 'C54x utilizes a highly specialized dual-operand instruction set, which is the basis of the operational flexibility and speed of these DSPs. The 'C54x also includes eight auxiliary registers and a software stack to enable a highly-optimized C compiler. The device's lower power consumption and reduced chip count, and enable system cost savings for communications applications.

TMS320C54x CPU Key Features

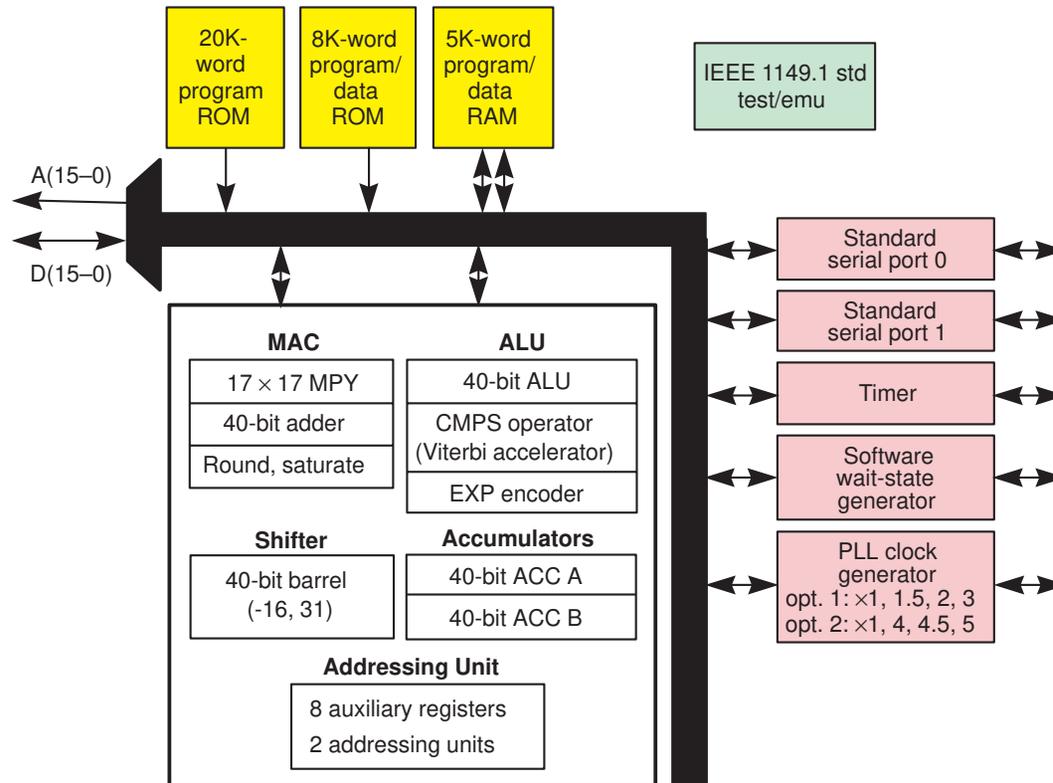
- Advanced multibus architecture with three separate 16-bit data buses and one program bus, three data buses, and four address buses
- 40-bit arithmetic logic unit (ALU), including a 40-bit barrel shifter and two independent 40-bit accumulators
- 17-bit \times 17-bit parallel multiplier coupled to a 40-bit dedicated adder for nonpipelined, single-cycle multiply/accumulate (MAC) operation
- Compare, select, store unit (CSSU) for the add/compare selection of the Viterbi operator
- Exponent encoder to compute the exponent of a 40-bit accumulator value in a single cycle
- Two address generators, including eight auxiliary registers and two auxiliary register arithmetic units (ARAUs)

TMS320LC541

Features of the 'LC541 include:

- 25-ns (40 MIPS) or 20-ns (50 MIPS) instruction cycle time ('C541 available only at 25 ns)
- Various operating voltages
 - 3.3 V ('LC541)
 - 5.0 V ('C541)
- 28K 16-bit words of ROM and 5K 16-bit words of RAM on chip
- Integrated Viterbi accelerator
- Powerful single-cycle instructions (dual-operand, parallel, and conditional instructions)
- Low active-mode power dissipation
 - Less than 35 mW to run VSELP
- Low-power standby modes
- 100-pin TQFP package
- Multiple PLL options

TMS320LC541 Block Diagram



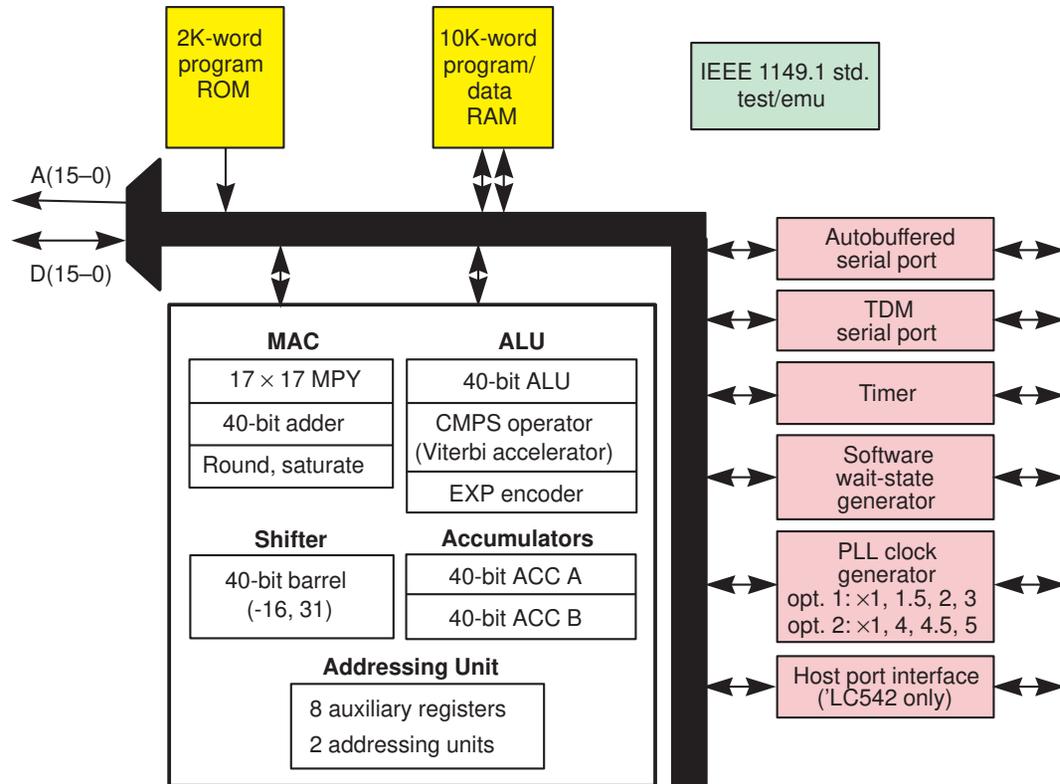
Note: The 'LC541 is available with one of two different PLL options. You choose one of the options listed.

TMS320LC542 and TMS320LC543

The 'LC542 and 'LC543 feature:

- 25-ns (40 MIPS) or 20-ns (50 MIPS) instruction cycle time ('C542 available only at 25 ns)
- Various operating voltages
 - 3.3 V ('LC542, 'LC543)
 - 5.0 V ('C542)
- 10K 16-bit words of RAM and 2K 16-bit words of on-chip boot ROM
- Autobuffered serial port (BSP)
- Time-division multiplexed serial port (TDM)
- Host port interface (HPI)
- Integrated Viterbi accelerator
- Powerful single-cycle instructions (dual-operand, parallel, and conditional instructions)
- Low active-mode power dissipation
 - Less than 35 mW to run VSELP
- Low-power standby modes
- 'LC542: 128- and 144-pin TQFP packages
- 'LC543: 100-pin TQFP package (without HPI)

TMS320LC542 and TMS320LC543



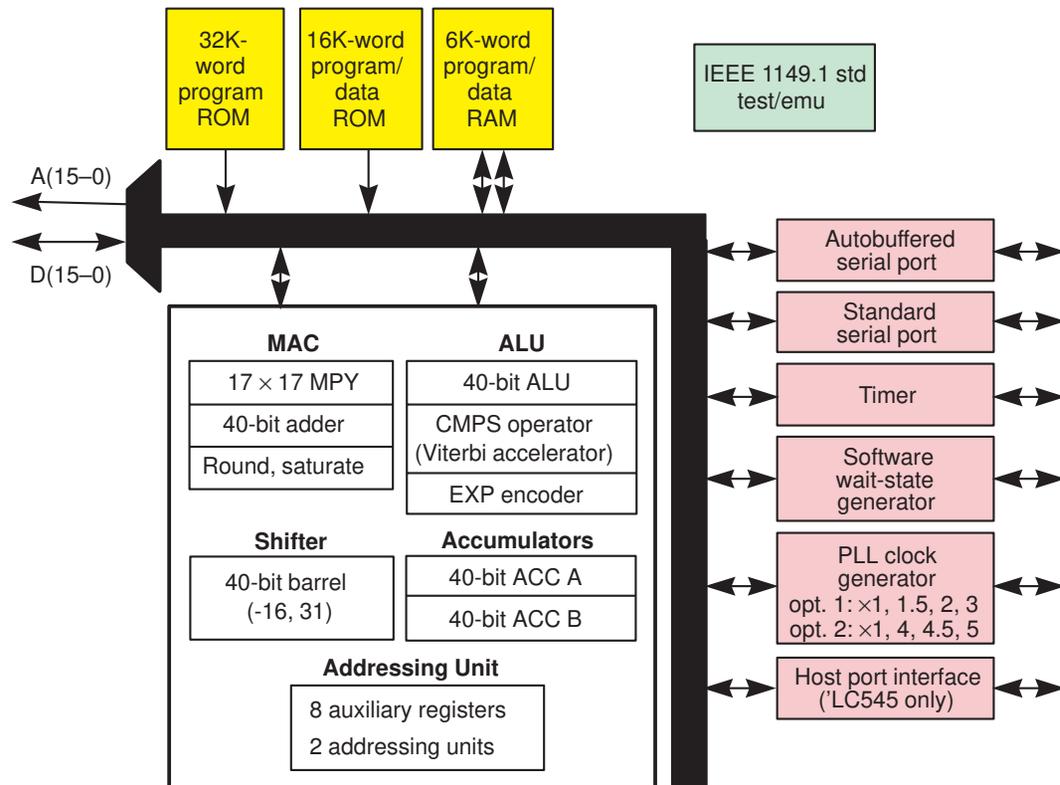
Note: The 'LC542 and 'LC543 are available with one of two different PLL options. You choose one of the options listed.

TMS320LC545 and TMS320LC546

The 'LC545 and 'LC546 feature:

- 25-ns (40 MIPS) or 20-ns (50 MIPS) instruction cycle time
- Various operating voltages
 - 3.3 V ('LC545, 'LC546)
- 48K 16-bit words of ROM and 6K 16-bit words of RAM on chip
- Autobuffered serial port (BSP)
- Host port interface (HPI)
- Integrated Viterbi accelerator
- Powerful single-cycle instructions (dual operand, parallel instructions, conditional instructions)
- Low active-mode power dissipation
 - Less than 35 mW to run VSELP
- Low-power standby modes
- 'LC545: 128-pin TQFP package
- 'LC546: 100-pin TQFP package (without HPI)

TMS320LC545 and TMS320LC546



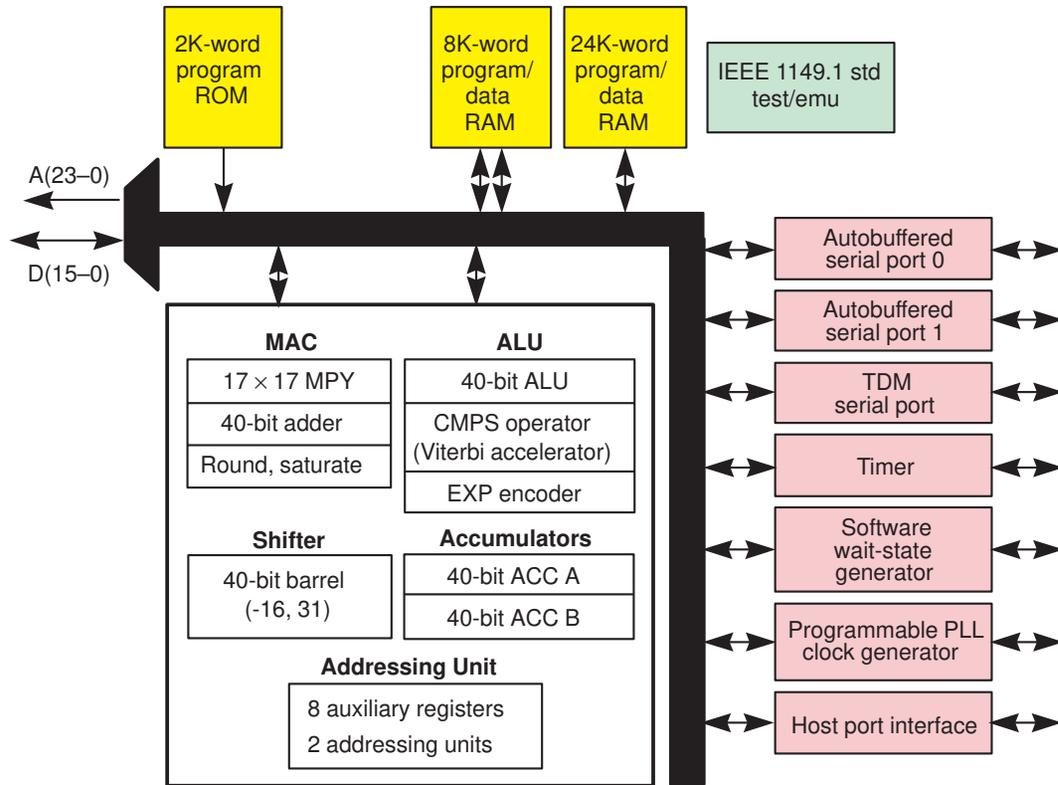
Note: The 'LC545 and 'LC546 are available with one of two different PLL options. You choose one of the options listed.

TMS320LC548

The 'LC548 features:

- 12.5-ns (80 MIPS) or 15-ns (66 MIPS) instruction cycle times
- 3.3-V operation
- 32K 16-bit words of RAM and 2K 16-bit words of boot ROM on-chip
- Extended addressing mode for $8M \times 16$ -bit maximum addressable external program space
- Two autobuffered serial ports (BSPs)
- TDM serial port (HPI)
- Host port interface
- Integrated Viterbi accelerator
- Powerful single-cycle instructions (dual operand, parallel instructions, conditional instructions)
- Low active-mode power dissipation
 - Less than 35 mW to run VSELP
- Low-power standby modes
- JTAG with boundary scan
- 16-bit on-chip timer

TMS320LC548

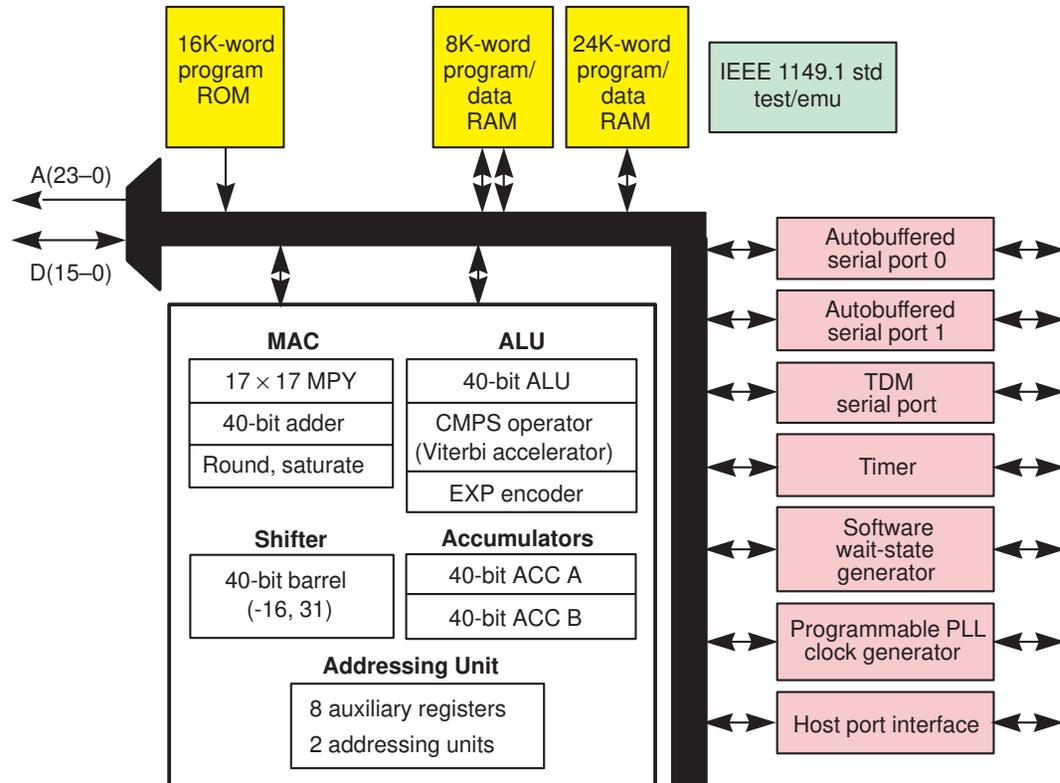


TMS320LC549/'VC549

The 'LC549 and 'VC549 features:

- 10-ns (100 MIPS), 12.5-ns (80 MIPS), or 15-ns (66 MIPS) instruction cycle times
- 'VC549
 - 2.5V core and 3.3V input/output
- 'LC549
 - 3.3V operation
- 32K 16-bit words of RAM and 16K 16-bit words of boot ROM on-chip
- Extended addressing mode for 4M x 16-bit maximum addressable external program space
- Two autobuffered serial ports (BSPs)
- TDM serial port
- Host port interface (HPI)
- Integrated Viterbi accelerator
- Powerful single-cycle instructions (dual operand, parallel instructions, conditional instructions)
- Low active-mode power dissipation
 - Less than 35 mW to run VSELP
- Low-power standby modes
- JTAG with boundary scan
- 16-bit on-chip timer

TMS320LC549/VC549



TMS320C54x Generation Summary

All TMS320C54x devices share the same CPU architecture. This table gives a 'C54x-generation product summary so that you can choose the best combination of performance, memory, power, package, and peripherals for your system.

TMS320C54x Generation Summary Table

Device	Nominal Voltage (V) (± 10%)	Cycle Time (ns)	On-Chip Memory		Peripherals			Package
			RAM (Words)	ROM (Words)	Serial Port(s)	HPI	Timers	
TMS320C541	5.0	25	5K	28K	2	No	1	100-pin TQFP
TMS320LC541	3.3	20/25	5K	28K	2	No	1	100-pin TQFP
TMS320C542	5.0	25	10K	2K	2†	Yes	1	144-pin TQFP
TMS320LC542	3.3	20/25	10K	2K	2†	Yes	1	128-pin TQFP/144-pin TQFP
TMS320LC543	3.3	20/25	10K	2K	2	No	1	100-pin TQFP
TMS320LC545	3.3	20/25	6K	48K	2‡	Yes	1	128-pin TQFP
TMS320LC546	3.3	20/25	6K	48K	2‡	No	1	100-pin TQFP
TMS320LC548	3.3	12.5/15	32K	2K	3§	Yes	1	144-pin TQFP; 144-pin BGA
TMS320LC549	3.3	12.5/15	32K	16K	3§	Yes	1	144-pin TQFP; 144-pin BGA
TMS320VC549	2.5/3.3	10	32K	16K	3§	Yes	1	144-pin TQFP; 144-pin BGA

† Buffered serial port and TDM serial port

‡ Buffered serial port and standard serial port

§ 2 buffered serial ports and TDM serial ports

TMS320C6x Generation

The TMS320C6x devices are the first devices to feature VelociTI™, an advanced, very long instruction word (VLIW) architecture developed by Texas Instruments, which allows performance of up to 1600 million instructions per second (MIPS). The first device in the series is the TMS320C6201, a fixed-point digital signal processor (DSP). TI has also announced the VelociTI-based TMS320C67x floating-point DSP core CPU, which performs 1 GFLOP (one billion floating-point operations per second).

TMS320C6x with VelociTI Enables Cost-Effective Solutions for Emerging Applications

The 'C6x devices offer cost-effective solutions to high-performance DSP programming challenges. The 'C6x development tools include a new C compiler, an assembly optimizer, and a Windows-based debugger. VelociTI combines an advanced VLIW architecture with a high degree of parallelism to produce a device that enables applications such as:

- Unlimited Internet bandwidth
- Universal wireless communication
- New telephony features
- Remote medical diagnostics
- Automated cruise control
- Personal home base station
- Personalized home security

TMS320C6x with VelociTI Energizes Existing Applications

In addition to offering the ability to create new applications, the 'C6x with VelociTI also combines an advanced VLIW architecture with a high degree of parallelism to revitalize existing applications such as:

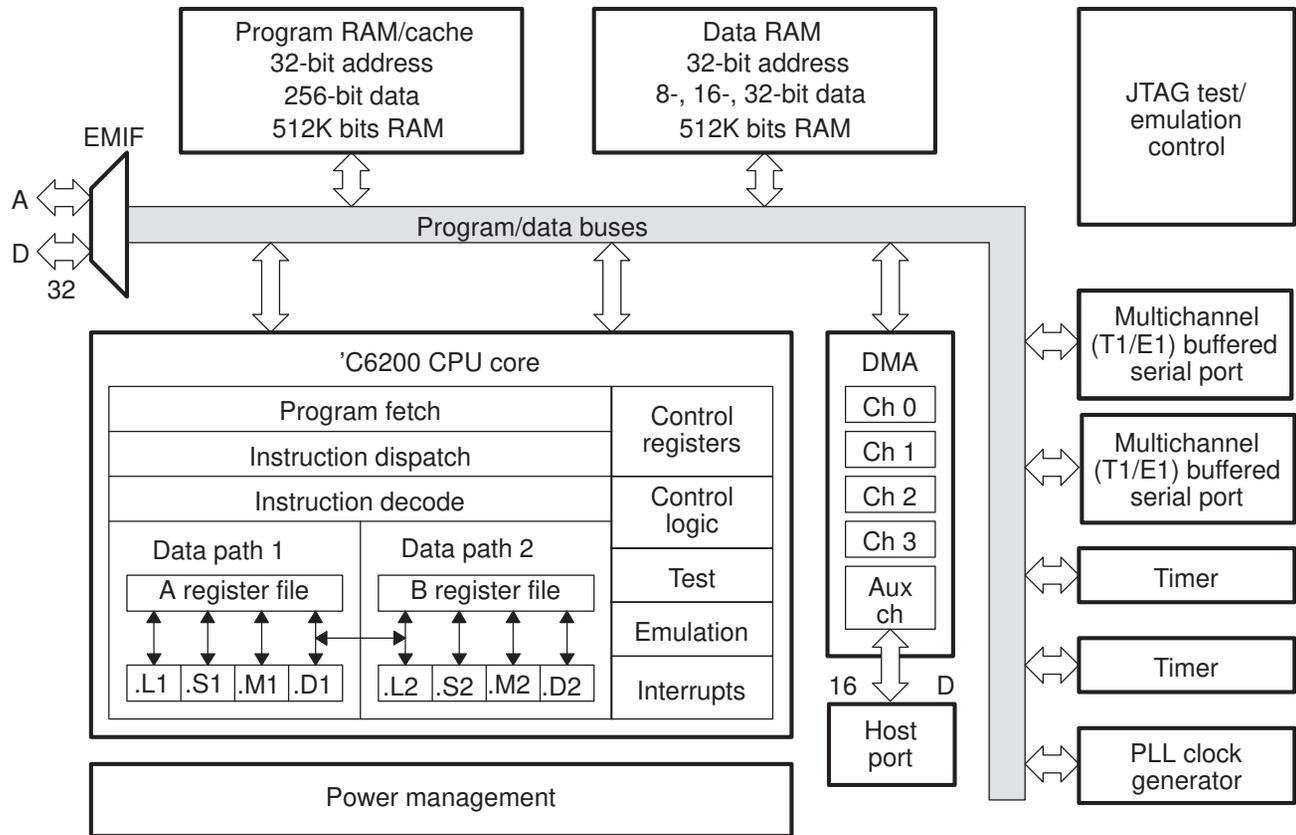
- Base stations
- Pooled modems
- Digital subscriber loop systems (DSL)
- Remote access servers (RAS)
- Central office switches
- Cable modems

TMS320C6201

The 'C6201 is the first fixed-point processor in the 'C6x generation. Its key features include:

- VelociTI advanced very long instruction word (VLIW) architecture
- Eight independent functional units (including two 16-bit multipliers with 32-bit results and six arithmetic logic units [ALUs] with 32/40-bit results)
- 32 32-bit registers
- 1600 million instructions per second (MIPS)
- 5-ns cycle time
- Up to eight 32-bit instructions per cycle
- Byte-addressable 8-, 16-, 32-bit data
- Dual-endian support
- Synchronous external memory interface (EMIF)
- Two multichannel buffered serial ports (McBSPs)
- Four-channel direct memory access (DMA)
- Two timers
- $\times 4$ phase-locked-loop (PLL) option
- Host-port interface (HPI)
- 1M-bit on-chip memory (divided into 2K by 256 bits of program memory and 64 bytes of data memory)
- 352-pin ball-grid array package

TMS320C6201 CPU Core with Peripherals



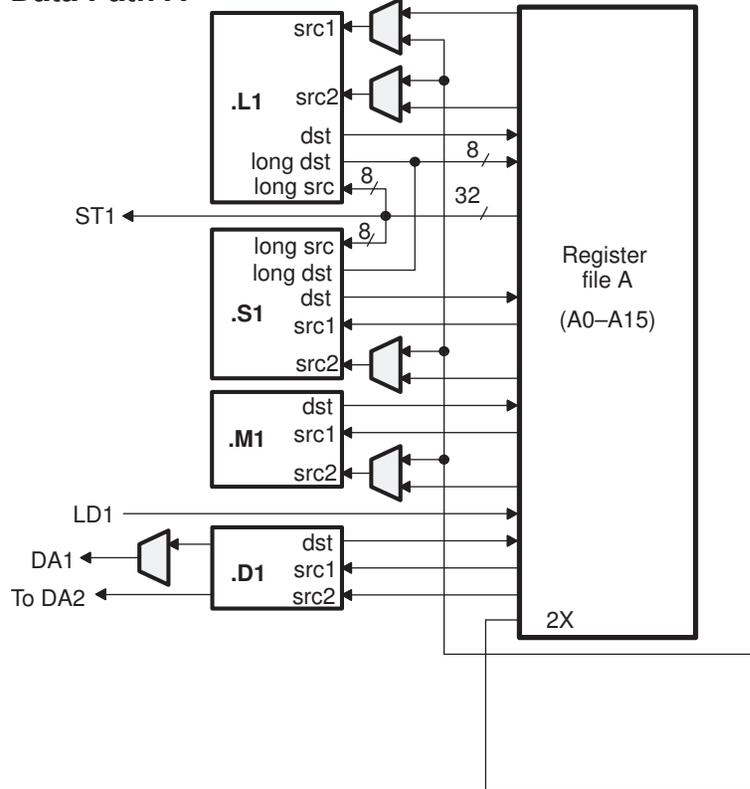
TMS320C62x

The 'C62x central processing unit (CPU) is the central building block of all the TMS320C62x devices. The CPU contains:

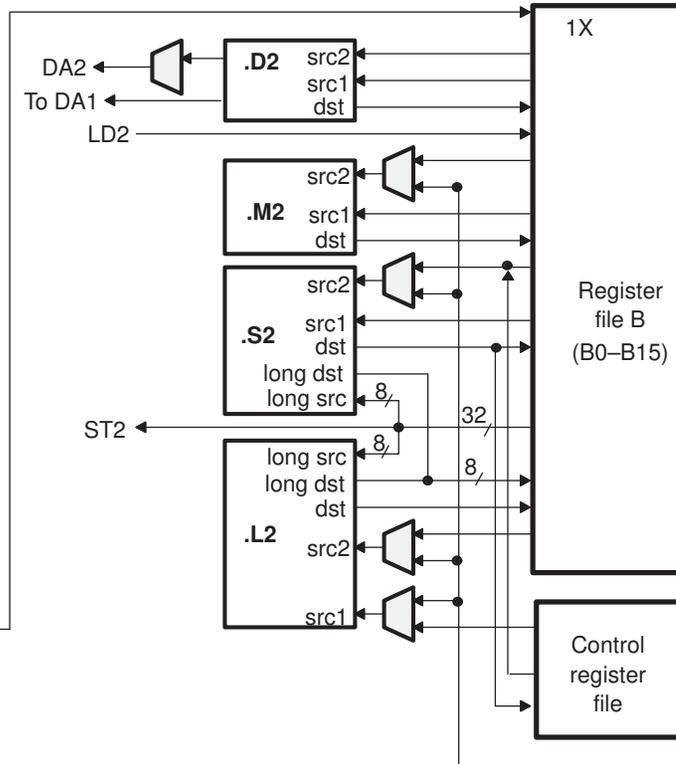
- Program fetch unit
- Instruction dispatch unit
- Instruction decode unit
- 32 general-purpose registers
- Two data paths, each with four functional units
- Control registers
- Control logic
- Test, emulation, and interrupt logic

TMS320C62x CPU Data Paths

Data Path A



Data Path B

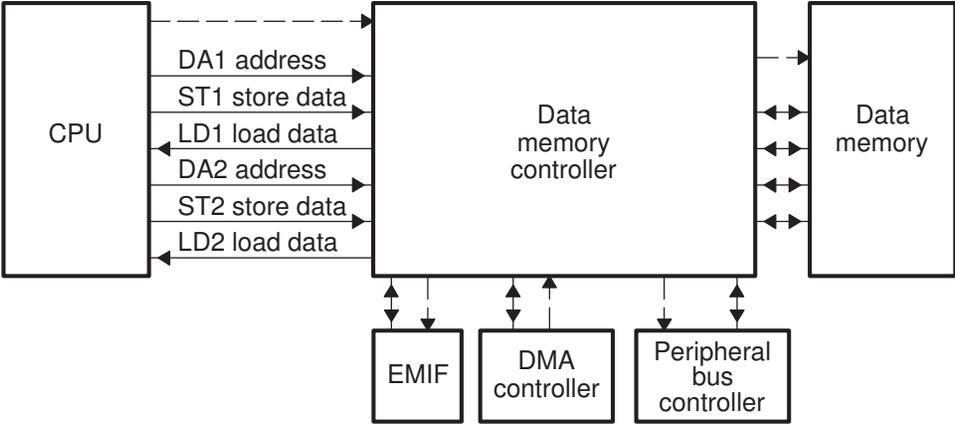


Direct Memory Access (DMA)

The direct-memory access (DMA) controller transfers data between points in the memory map without intervention by the CPU. The DMA controller has the following features:

- Background operation
- High throughput
- Four channels
- Auxiliary channel
- Split operation
- Multiframe transfer
- Programmable priority
- Programmable address generation
- Full-address 32-bit address range
- On-chip program memory
- External memory interface (EMIF)
- Programmable width transfers
- Autoinitialization
- Event synchronization
- Interrupt generation

DMA Controller Interconnect to TMS320C62x Memory-Mapped Modules



- Solid line indicates data
- - Dashed line indicates requests
- ◀ ▶ Arrowheads indicate direction of data or request

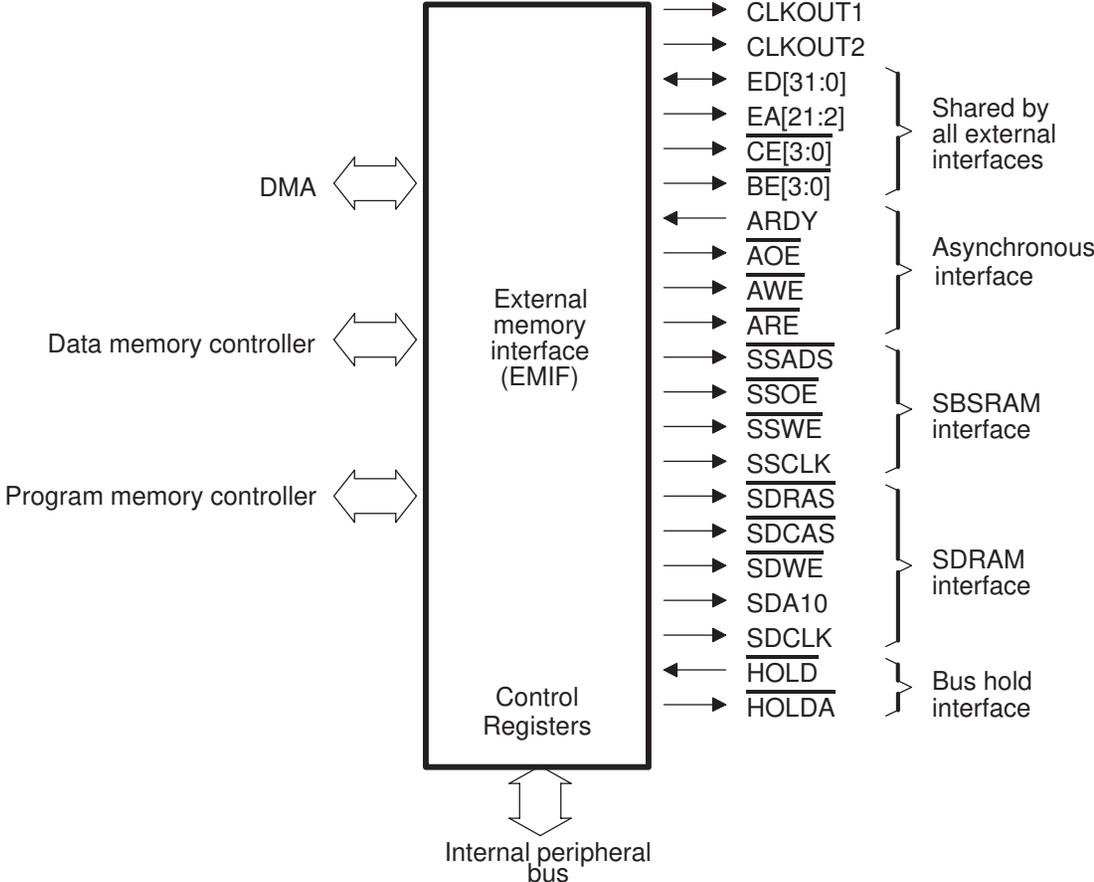
External Memory Interface (EMIF)

The external memory interface (EMIF) supports a glueless interface to several external devices, including:

- Synchronous DRAM (SDRAM) running at half the CPU clock rate
- Asynchronous devices, including asynchronous SRAM, ROM, and FIFOs. The EMIF provides highly programmable timing parameters to these interfaces.
- The on-chip program memory controller (PMC) that services CPU program fetches
- The on-chip data memory controller (DMC) that services CPU data fetches
- An external shared-memory device

If multiple access requests arrive simultaneously, the EMIF must prioritize them and perform the necessary cycles. A block diagram of the EMIF is shown on the following page.

EMIF Block Diagram



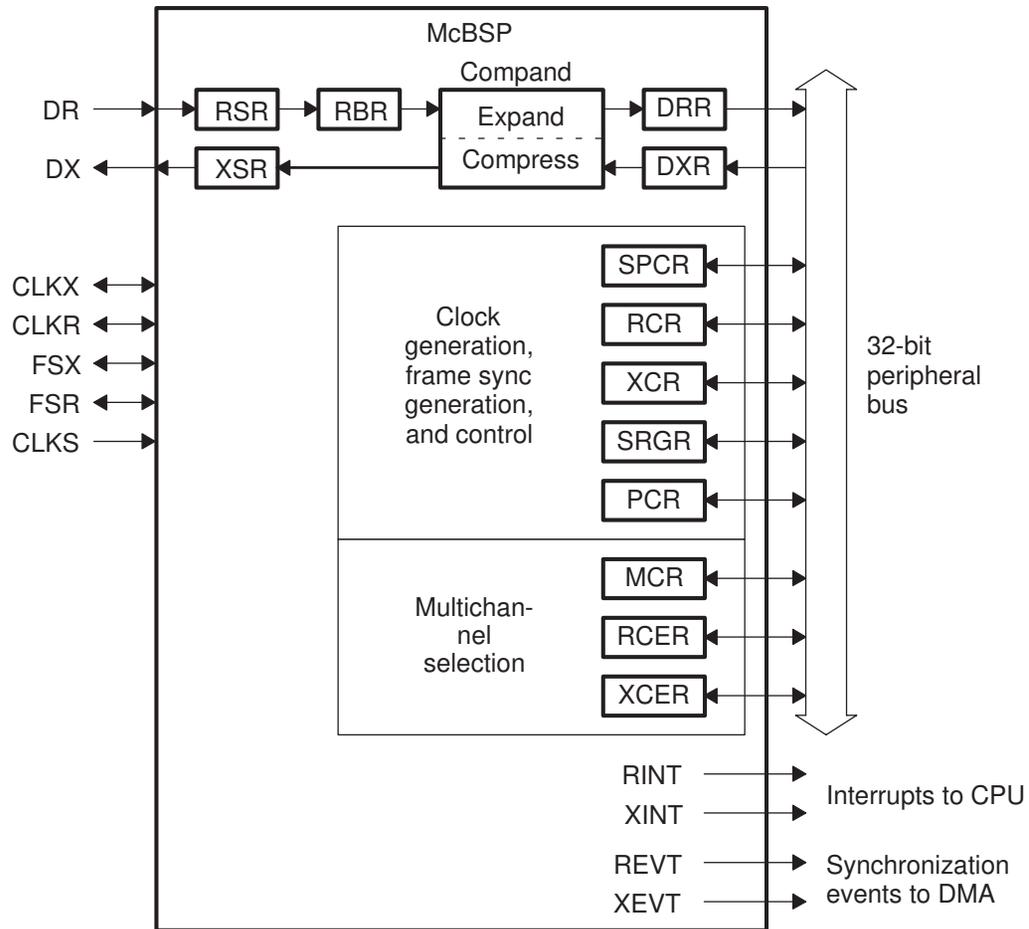
Multichannel Buffered Serial Port (McBSP)

The 'C62x multichannel buffered serial port (McBSP) is based on a standard serial port interface found on the 'C2x, 'C2xx, 'C5x, and 'C54x devices. Like its predecessors, it provides:

- Full duplex communication
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected A/D and D/A devices
- External shift clock generation or an internal programmable frequency shift clock

The McBSP consists of a data path and control path. Seven pins connect the control and data paths to external devices as shown in the following figure.

McBSP Internal Block Diagram

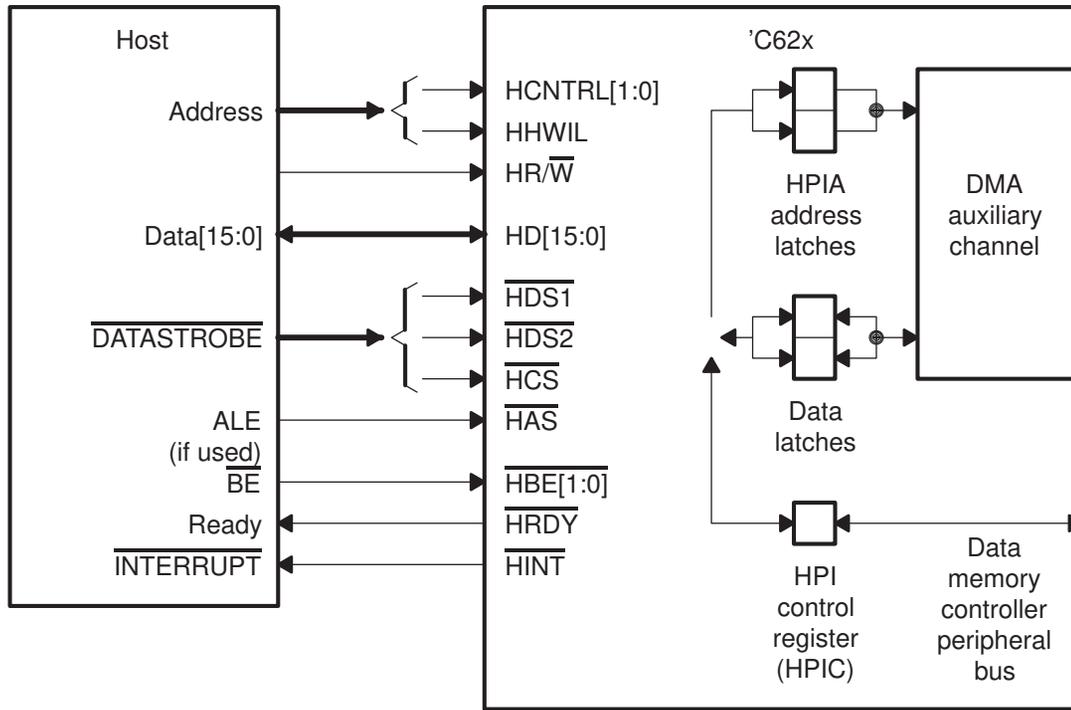


Host Port Interface (HPI)

The host port interface (HPI) is a parallel port through which a host processor can directly access the CPU's memory space. The host device is the master of the interface, therefore increasing its ease of access. The host and the CPU can exchange information via internal or external memory. In addition, the host has direct access to memory-mapped peripherals. Connectivity to the CPU's memory space is provided through the DMA controller. Dedicated address and data registers not accessible to the CPU connect the HPI to the DMA auxiliary channel, which, in turn, connects the HPI to the CPU's memory space.

To configure the interface, the HPI and the CPU can access the HPI control (HPIC) register. The host can access the host address register (HPIA) and host data register (HPID), as well as the HPIC register, using the external data and interface control signals. The diagram on the following page is a simplified version of the interface between the host and the 'C62x HPI.

HPI Block Diagram



TMS320C67x

The TMS320C67x CPU will be the first floating-point CPU in the 'C6x generation. The 'C67x key features include:

- VelociTI advanced very long instruction word (VLIW) architecture
- 32 32-bit registers
- 6-ns cycle time
- Six 32-bit floating-point instructions per cycle
- IEEE floating-point format
- One billion floating-point operations per second (1 GFLOP) single precision
- 420 million floating-point operations per second double precision
- 32-bit address range
- Dual-endian support

TMS320C6x Generation Summary Table

Product	Cycle Time (ns)	On-Chip (16-bit Words) RAM		Memory Off-Chip	Peripherals				Package
		Program	Data		Timers	Serial	Host Port	DMA Channels	
TMS320C6201	5	32K	32K	52M x 8	2	2†	1‡	4	352 BGA

† Multichannel buffered serial ports

‡ 16 bit

TMS320C8x Generation

The processing power of the TMS320C8x devices supports any application that requires high-performance digital signal processing. The first member of the 'C8x generation, the TMS320C80, is a single-chip, parallel processor that can be used for applications such as real-time audio/video processing, high-end data communications, and image processing. The 'C82 is the second member of the 'C8x family that can be used in high-volume applications like desktop videoconferencing, high-speed telecommunications, and 3-dimensional graphics.

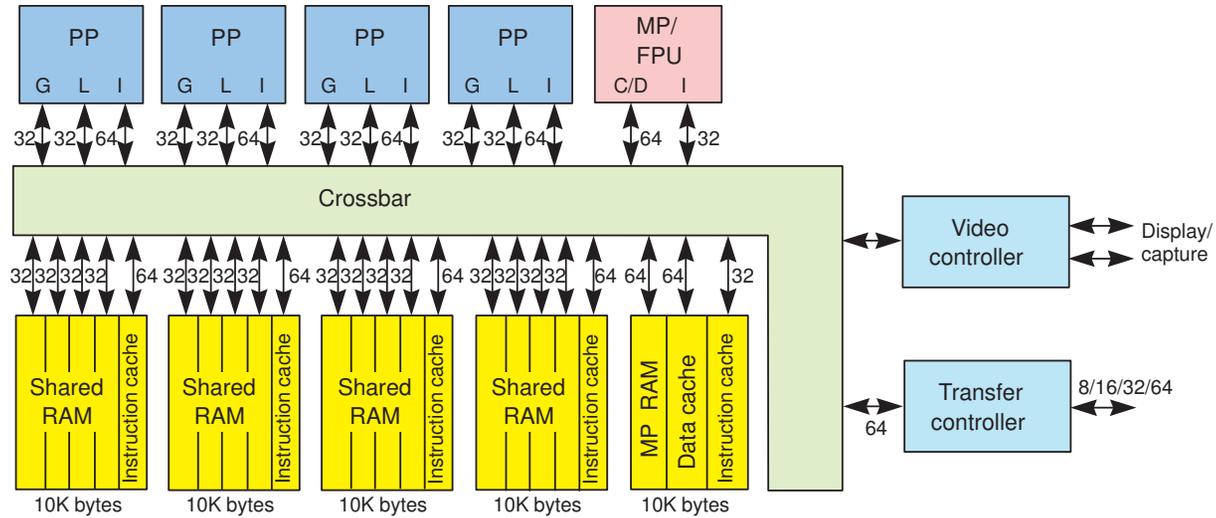
Since the 'C8x devices are fully programmable, you can blend industry-standard algorithms with proprietary software to optimize system performance and differentiate products in the market. You receive added flexibility, because a 'C8x-based system can be adapted to evolving technologies through software modifications rather than hardware redesigns. This enables you to upgrade as new standards emerge.

TMS320C80

Key features of the 'C80:

- More than 2 billion operations per second (BOPS)
- Four parallel processing advanced DSPs (PPs) with 64-bit instructions and 32-bit fixed-point data
 - Each PP is capable of many parallel operations per cycle.
 - The PPs perform pixel/field processing as well as digital signal processing.
- RISC master processor with 120-MFLOPS IEEE-754 floating-point unit
- 50K bytes of on-chip RAM
 - Supports many parallel accesses per cycle
- Crossbar switch supports up to 4.2G bytes/s transfer rates
 - 2.4G bytes/s of data and 1.8G bytes/s of instructions
 - 32K bytes of RAM can be shared by all processors and the transfer controller
- Transfer controller supports multidimensional packet transfers
 - 400M bytes/s on- and off-chip memory transfers
 - 4G-byte memory address space
 - Access to 8-, 16-, 32-, or 64-bit SRAM, VRAM, DRAM, SDRAM
 - Offloads memory manipulations from the processors
- Video controller supports any display or capture resolution
- 0.5- μ m CMOS technology
- Efficient packaging:
 - 305-pin PGA
 - 352-pin BGA

TMS320C80 Block Diagram

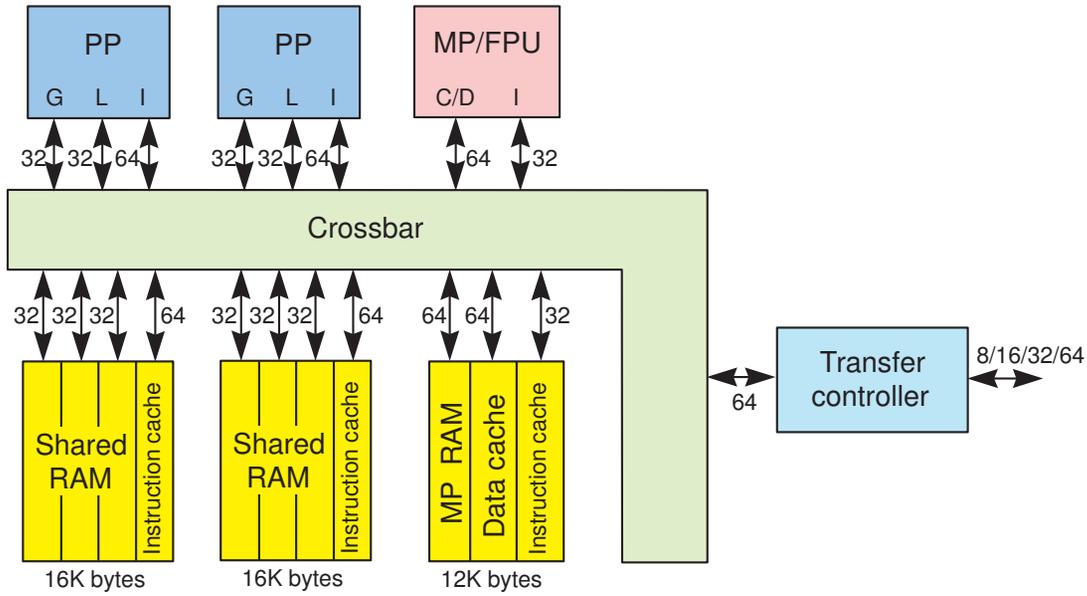


TMS320C82

Features of the 'C82 include:

- More than 1.5 billion operations per second (BOPS)
- Two parallel-processing advanced DSPs with 64-bit instructions and 32-bit fixed-point data
 - Each PP is capable of many parallel operations per cycle.
 - The PPs perform pixel/field processing as well as digital signal processing.
- RISC master processor with 120-MFLOPS IEEE-754 floating-point unit
- 44K bytes of on-chip RAM
 - Supports many parallel accesses per cycle
- Crossbar switch supports up to 2.6G bytes/s transfer rates
 - 1.6G bytes/s of data and 1.0G bytes/s of instructions
 - 32K bytes of RAM can be shared by all processors and the transfer controller
- Transfer controller supports multidimensional packet transfers
 - 400M-bytes/s on- and off-chip memory transfers
 - 4G-byte memory address space
 - Access to 8-, 16-, 32-, or 64-bit SRAM, VRAM, DRAM, SDRAM
 - Offloads memory manipulations from the processors
 - On-chip memory configuration cache consisting of six 32-bit words to describe the properties of six banks of external memory
- 0.5- μ m CMOS technology
- Efficient packaging: 352-pin plastic BGA package

TMS320C82 Block Diagram



TMS320C8x Master Processor (MP)

The master processor (MP) is a 32-bit RISC processor with an integral IEEE-754 floating-point unit. As with other RISC processors, all accesses to memory are performed with load and store instructions, and most integer and logical operations are performed on registers in a single cycle. The floating-point instructions are pipelined; therefore, you can start a single-precision multiply or any floating-point add instruction on each clock cycle. Moreover, the floating-point unit approaches 120 MFLOPS in performance at 60-MHz internal clock rate.

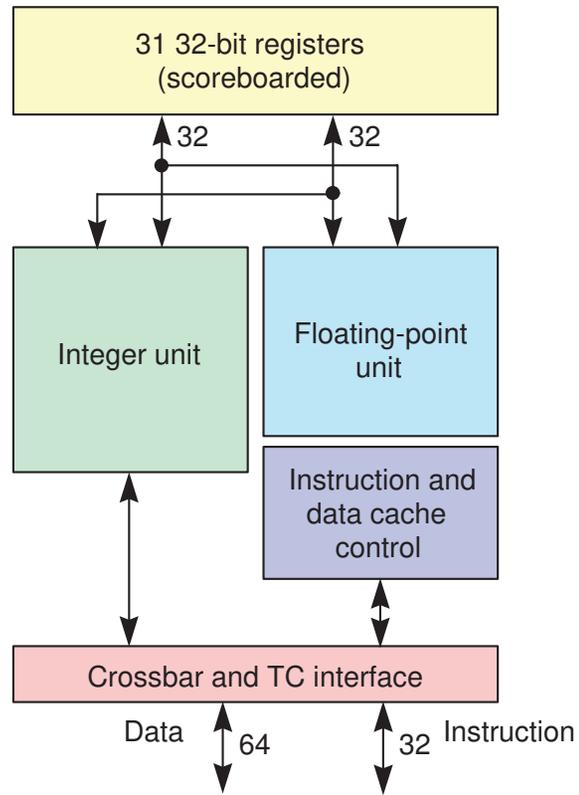
Floating-point operations use the same register file as the integer and logic unit. A register scoreboard ensures that correct register-access sequences are maintained.

The MP is structured for efficient execution of C code. For example, the MP contains an R0 register, often called a zeroing register, used by C. Also, the MP instruction set is tailored to contain many of the C executables found in compiler technology.

Features of the master processor include:

- 32-bit RISC CPU delivering 60 MIPS @ 60 MHz
 - Targeted for high-level languages
- IEEE-754/20-MFLOP floating-point unit
 - Parallel multiply, add, and load/store
- 31 32-bit registers
 - Single file for integer and floating point
 - Loads and FPU results are scoreboardd
- Instruction and data cache control
 - 4K-byte instruction cache
 - 4K-byte data cache
 - 2K-byte parameter RAM ('C80), 4K-byte parameter RAM ('C82)

TMS320C8x Master Processor Block Diagram



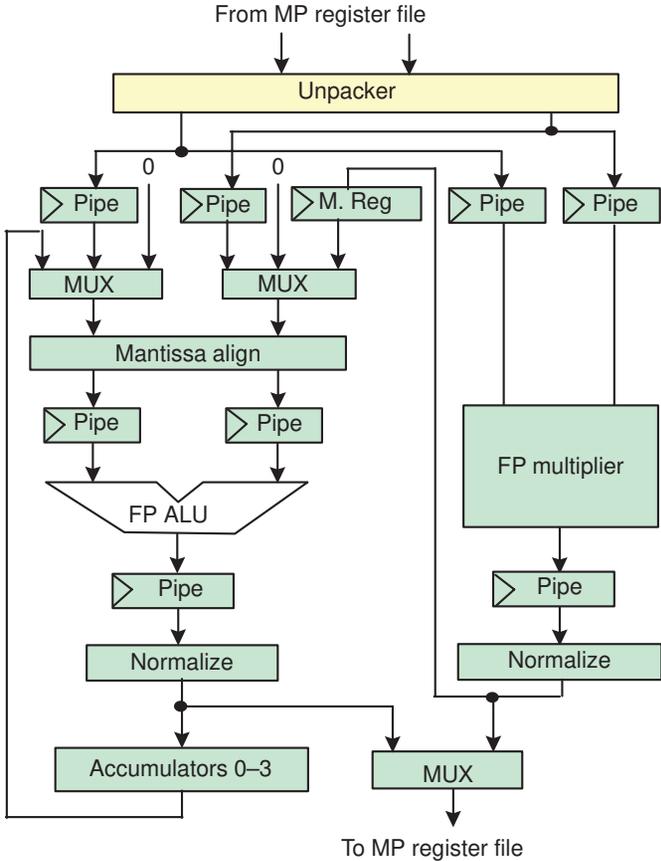
TMS320C8x MP Floating-Point Unit

The MP's floating-point unit is capable of performing IEEE-754 floating-point operations in 32-bit single-precision and 64-bit double-precision floating point. Conversion between different formats is also supported. In addition, the floating-point unit provides vector floating-point operations with the option of performing a parallel load or store to improve program efficiency.

Hardware support for the floating-point unit consists of a full double-precision floating-point add unit and a 32-bit single-precision floating-point multiply unit:

- IEEE-754 floating point
 - Hardware exception handling
- FP add unit with double-precision ALU
 - 1-cycle adds/subs/compares (single and double) and conversions
 - 6-cycle single- and 20-cycle double-precision divide
 - 9-cycle single- and 26-cycle double-precision square root
- The floating-point multiply unit performs all multiplies (integer and floating-point), divides, and square roots.
 - 1-cycle single-precision multiply
 - 4-cycle double-precision multiply
- Pipelined—can start a new instruction every cycle
 - 3-stage pipeline
 - Register file scoreboard prevents *races*
- Vector FP for 120-MFLOP operation
 - Parallel multiply, add, and 64-bit load (p++) in one cycle
 - 4 double-precision accumulator registers support pipelining
 - Supports matrix multiplies, DCTs, and FFTs
- FP status and interrupt-enable registers
 - MP's test-and-branch instructions access FP status

TMS320C8x MP Floating-Point Unit Block Diagram



TMS320C8x Parallel Processing Advanced Digital Signal Processors (PP)

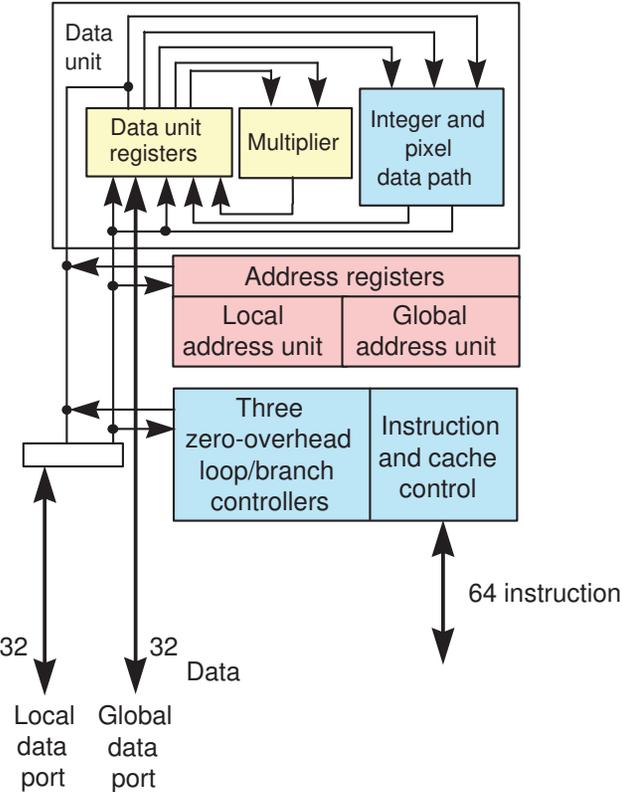
The parallel processing advanced digital signal processors (PPs) provide much of the 'C8x's performance. The PPs are designed to perform digital signal processing along with bit-field and multiple-pixel manipulation. These processors have advanced features that are not found in any other DSP or general-purpose processor and can perform in excess of ten RISC-like operations in each cycle.

In order to specify the multiple parallel operations that the PPs can perform, a wide instruction word of 64 bits is used. The instruction has fields that independently control the data unit and the two address units. All instructions execute in a minimum of a single cycle.

Each PP has a register file of 44 user-visible registers. All registers can be the source or destination of ALU or memory operations. The register set is divided into files according to each register's function. The PP features:

- 3-input ALU with mixed arithmetic and Boolean operations
 - Can perform masking at the same time as an add or subtract
- Flexible data path feeding 3-input ALU
 - Fast bit and file processing
- Address data paths can be used for general-purpose arithmetic
- Byte/halfword multiple arithmetic
 - Single instruction stream, multiple data stream (SIMD) processing within each processor
 - Better handling of pixels and Z-buffers than in other DSPs or general-purpose processors

TMS320C8x Parallel Processing Advanced Digital Signal Processors (PP) Block Diagram



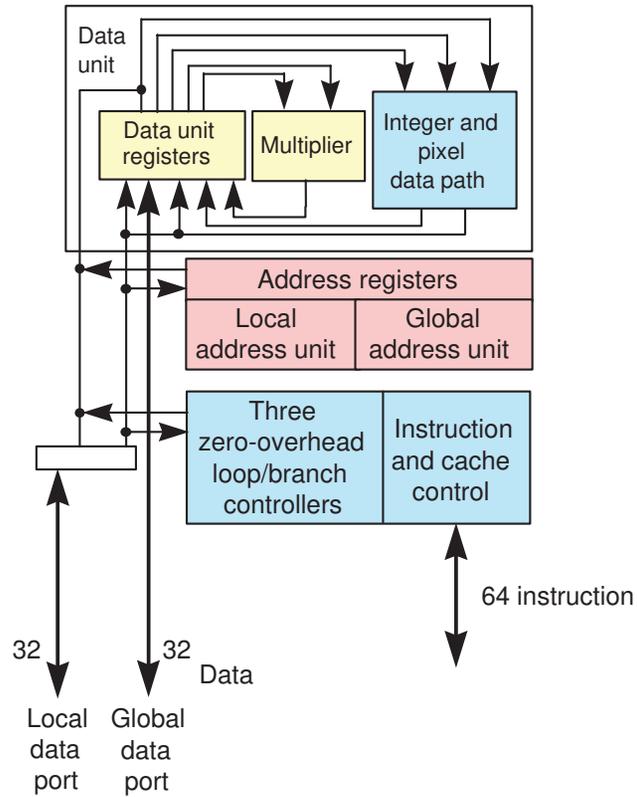
TMS320C8x Parallel Processing Advanced Digital Signal Processors (PP) (Continued)

- Eight primary data registers, d0 to d7 (D registers), that can perform up to seven reads and four writes
 - Two multiplier sources, three ALU sources, one multiplier result, one ALU result, and three LD/ST/MOVE
- Splittable multiplier for fast pixel math
 - Any D register can be used on a multiply-with-parallel-add
- Three levels of zero-overhead loops
- Conditional operations (for ALU, load/store, and/or register source)

Additional features include:

- Two address units
 - Up to two memory operations/cycle
- Single-cycle multiplier
 - One 16- or two 8-bit results/cycle
- Splittable 3-input ALU
 - Multiple operations in each pass
 - Up to four 8-bit results/cycle
- Pixel and bit field hardware

TMS320C8x Parallel Processing Advanced Digital Signal Processors (PP) Block Diagram



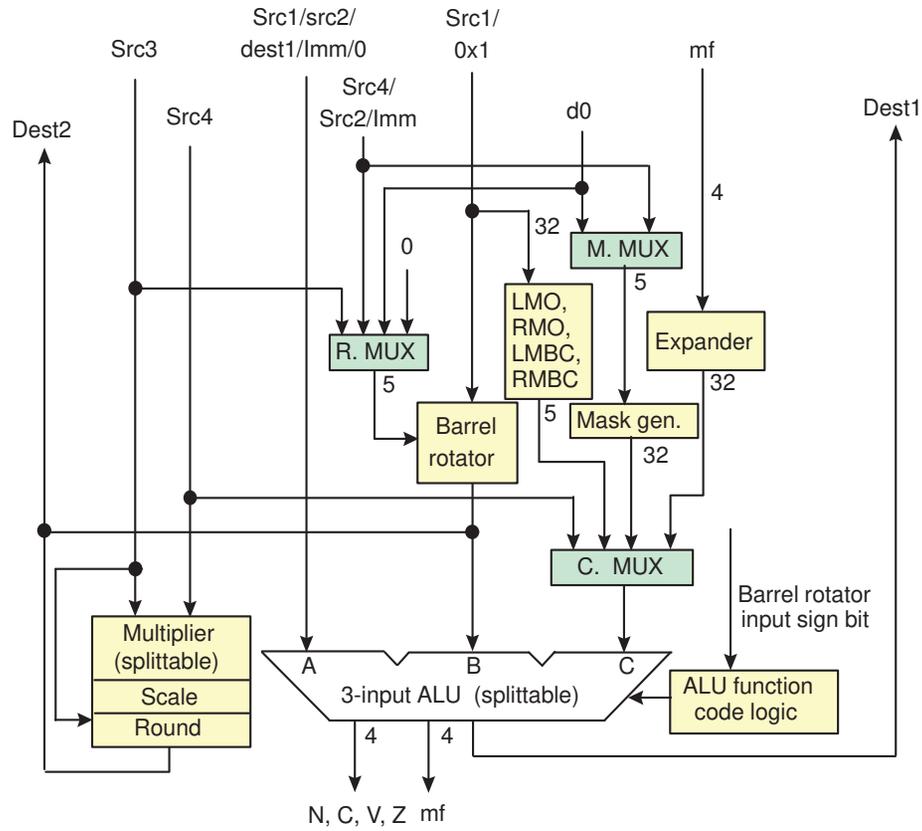
TMS320C8x PP Data Unit

The parallel-processing advanced DSP (PP) data unit has two data paths; each with its own set of hardware that functions independently of the other. The ALU data path includes a barrel rotator, mask generator, 1-bit to n-bit expander, and a 3-input ALU that can combine the mask or expander output with register data to create over 2000 different processing options. The 3-input ALU can perform 512 logical and/or mixed logical and arithmetic operations that support masking or merging and addition/subtraction in a single pass. The ALU can also be split to perform multiple 8-bit or 16-bit operations in parallel.

The PP data unit features are:

- 3-input ALU (512 operations)
 - Mixed arithmetic and Boolean in one cycle (mask and add/sub in one pass)
 - Mask/merge and field processing
 - Splittable for multibyte operations
- 16-bit × 16-bit multiplier (32-bit results)
 - Rounding for DCT accuracy
 - Splittable into two 8-bit × 8-bit multipliers (16-bit results)
- Flexible data path
 - Barrel rotator
 - Mask generator
 - N-to-1 and 1-to-N translations via mf register
 - Left/rightmost one and bit-change
- 44 user-visible registers
 - Any register can be operand of ALU
- Eight D registers
- Conditional operations
 - Conditional choice of register pair source
 - Conditional save of result

TMS320C8x PP Data Unit Block Diagram



TMS320C8x Transfer Controller (TC)

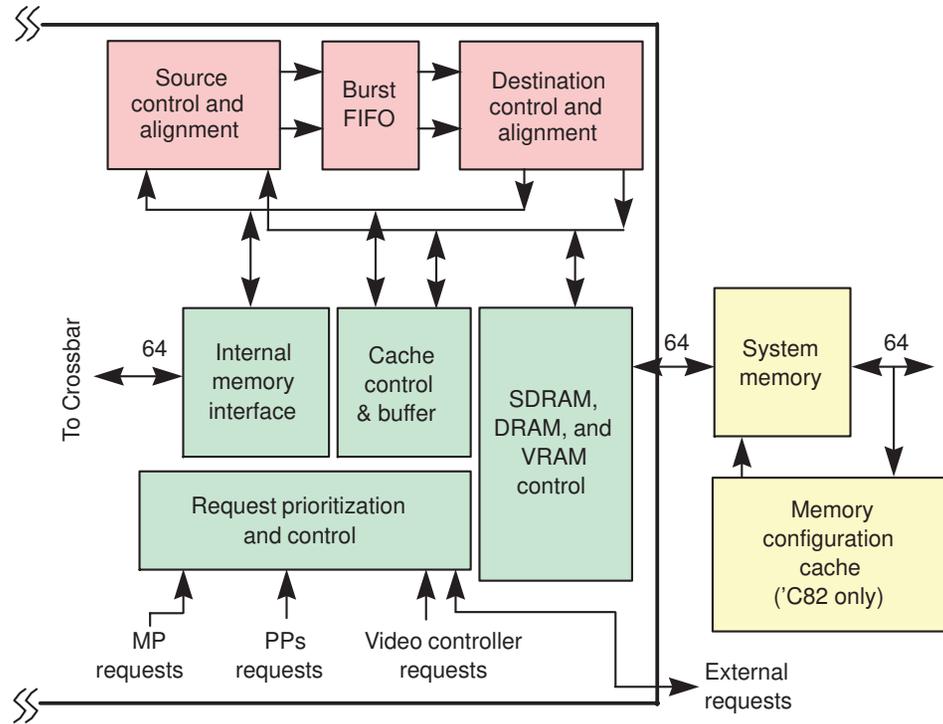
The transfer controller (TC) is a combined DMA machine and memory interface that intelligently queues, prioritizes, and services the data requests and cache misses of the MP and the PPs. The transfer controller interfaces directly with the on-chip SRAMs. Through the TC, all of the processors can access the system external to the chip. In addition, data-cache or instruction-cache misses are automatically handled by the TC.

Data transfers are specifically requested by the PPs or the MP in the form of linked-list packet transfers, which are handled by the TC. These requests allow multidimensional blocks of information to be transferred between a source and destination, either of which can be on-chip or off-chip. Packet-oriented data transfers offer compatibility with several local area network standards, such as ATM.

The TC performs:

- Cache fills and writes
- Direct loads and stores from/to off-chip memory via DEA request
- Block movement of data via packet transfers
- Refresh and SRT (shift register transfer) cycles needed to maintain DRAMs and VRAM capture/display buffer

TMS320C8x Transfer Controller Block Diagram



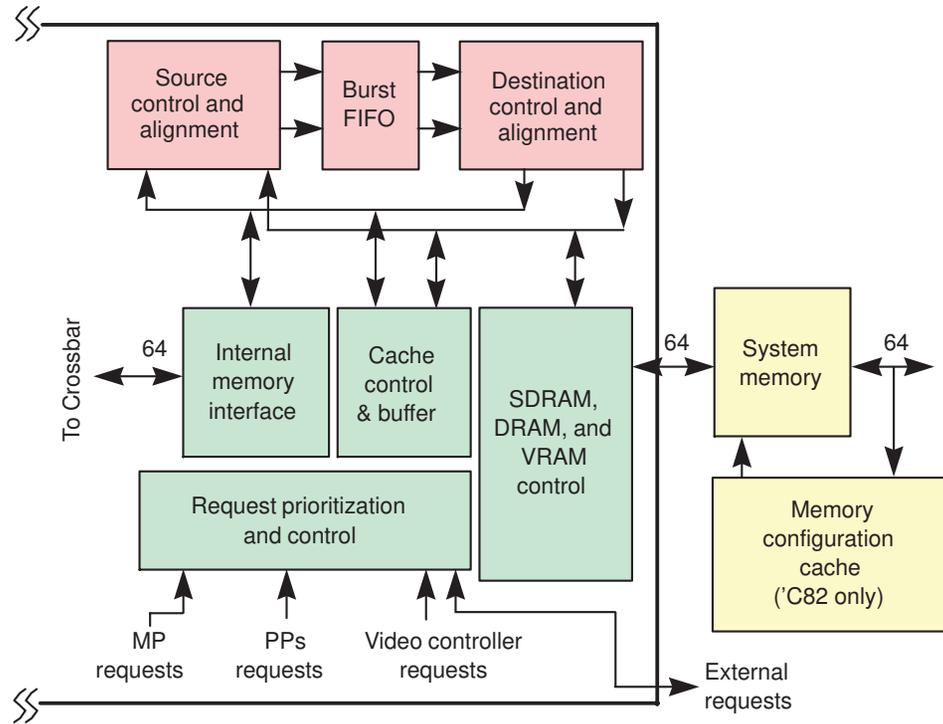
TMS320C8x Transfer Controller (TC) (Continued)

Features of the TC include:

- 400 Mbytes/s external bandwidth
- Direct DRAM, VRAM, SRAM, and SDRAM control
- Dynamic bus sizing (64, 32, 16, or 8 bits)
- Packet transfers controlled autonomously by transfer controller
- Linear x/y addressing
 - Independent source and destination
 - Automatic byte alignment
- Intelligent request
 - Queuing and prioritization

The 'C82 TC includes a memory configuration cache that consists of six 32-bit words that describe the properties of the six most recently-used banks of memory. The cache automatically loads configuration words each time an access to a new bank is made and it can be locked into a set high or low priority. The configuration cache reduces the number of pins necessary in the 'C82 and in support chips.

TMS320C8x Transfer Controller Block Diagram



TMS320C80 Video Controller (VC)

The video controller (VC) is included only in the architecture of the 'C80 and is the interface between the device and image capture and display systems. The 'C80 has two sets of frame timing counters and registers. The VC keeps track of horizontal and vertical synchronization and blanking timing, as well as supports a 2-dimensional border region. Each counter has its own asynchronous clock inputs. These synchronization signals can individually be set up as outputs (for display) or inputs (for capture).

The shift register transfer (SRT) controller has comparators that cause shift register transfer cycles for VRAMs or cause packets transfers for DRAM-based display memories.

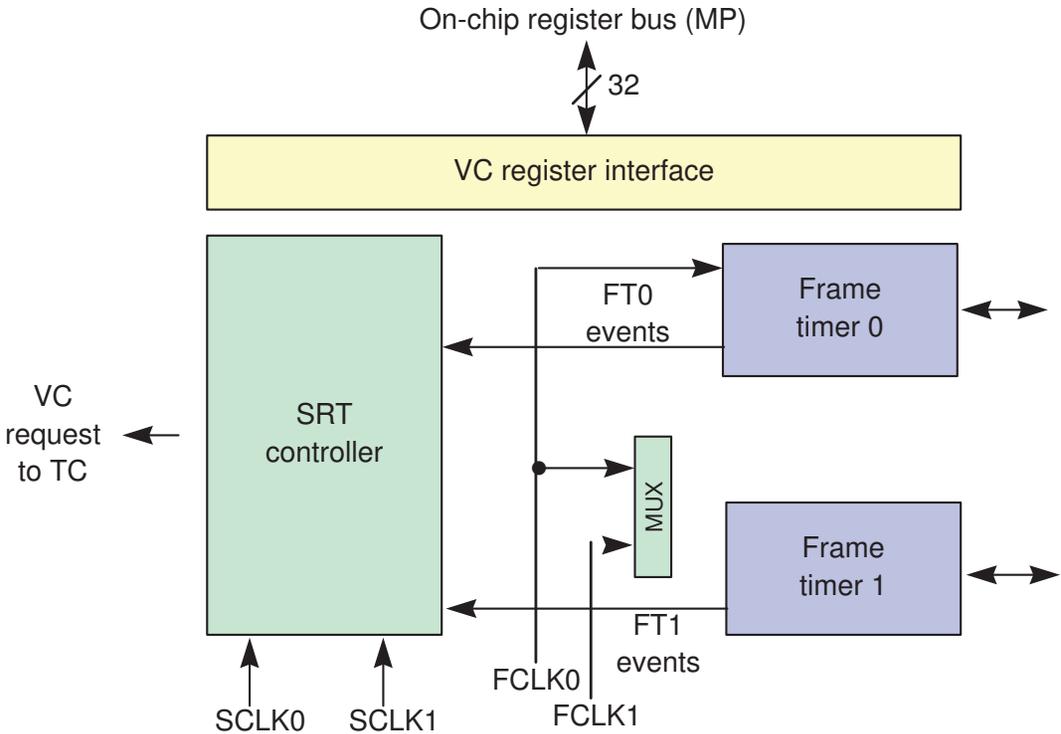
These four main sections make up the VC:

- Frame timers
- Serial register transfer controller
- Register interface
- Multiplexer

Features of the VC include:

- Two identical frame timers
 - They can be used for display or capture
 - Each has an asynchronous clock
 - They generate fully-programmable horizontal, vertical, blank, and border timing
- SRT controller
 - Controls two display/capture regions
 - VRAM shift register transfer control
 - Generates timer interrupts to the MP
 - Generates timer packet requests to the TC

TMS320C80 Video Controller (VC) Block Diagram



TMS320C8x Generation Summary

All TMS320C8x devices share the same RISC processor and advanced DSPs.

This table gives a 'C8x-generation product summary in order to choose the best combination of performance, memory, power, package, and peripherals for your system.

TMS320C8x Generation Summary Table

Data Type	Device	Cycle Time (ns)	Memory On-Chip		Memory Off Chip	Bandwidth (Mbytes/s)	DSPs	Intelligent DMA	On-Chip Timers	Package
			Data (KB)	Program (KB)						
Multi-processor	TMS320C80-40	25	38	12	4G × 8	400	4	1	3	305-pin PGA 352-pin BGA
	TMS320C80-50	20	38	12	4G × 8	400	4	1	3	305-pin PGA 352-pin BGA
	TMS320C82-60	16	32	12	4G × 8	320	2	1	1	352-pin BGA

TMS320AVxxx Generation

The transition from analog to digital video storage and transmission has created a large demand for products conforming to open standards. Audio and video compression standards such as MPEG, broadcast transmission standards such as DVB, and demodulation standards such as QAM, QPSK, and VSB, demand high-performance DSP technology.

Texas Instruments developed the TMS320AVxxx product family for this exciting new market. Current products generally available are included in this section. For more information on other DSP developments for digital audio and video applications, please contact your local TI sales representative.

TMS320AV110

The Texas Instruments TMS320AV110 MPEG audio decoder implements the International Standards Organization — Moving Picture Expert Group (ISO-MPEG) audio decompression algorithm in a single chip. The 'AV110 accepts an MPEG-compliant compressed audio stream at any of the valid MPEG data and sampling rates and produces decompressed audio output in either 16- or 18-bit serial pulse-code modulation (PCM) format. The PCM data stream is suitable for direct input to most commercially available digital-to-analog converters (DACs).

Both MPEG layers 1 and 2 are implemented. The 'AV110 decodes a single monaural channel, two independent mono channels, stereo channels, and joint stereo channels. The compressed audio can be input either as MPEG audio frames or as the full-multiplexed system stream containing multiple audio and/or video packets. The input can be at the actual bit rate or it can be in bursts at up to 15 Mbps.

Compressed audio can be input in either bit-serial or byte-parallel formats. An 8-bit microprocessor interface is provided for control and status register access with maskable interrupts for the critical status and error flag registers.

While the 'AV110 operates as a single, stand-alone decoder, provision is also made for using a 256K × 4 DRAM device if buffering of the audio stream is required. With the external memory in place, up to one second of audio can be buffered for synchronization purposes. The external memory also allows the employment of more robust error-concealment techniques if cyclic redundancy check (CRC) or synchronization errors are detected by the decoder.

The 'AV110 is implemented in Texas Instruments EPIC™ submicron, triple-level-metal technology.

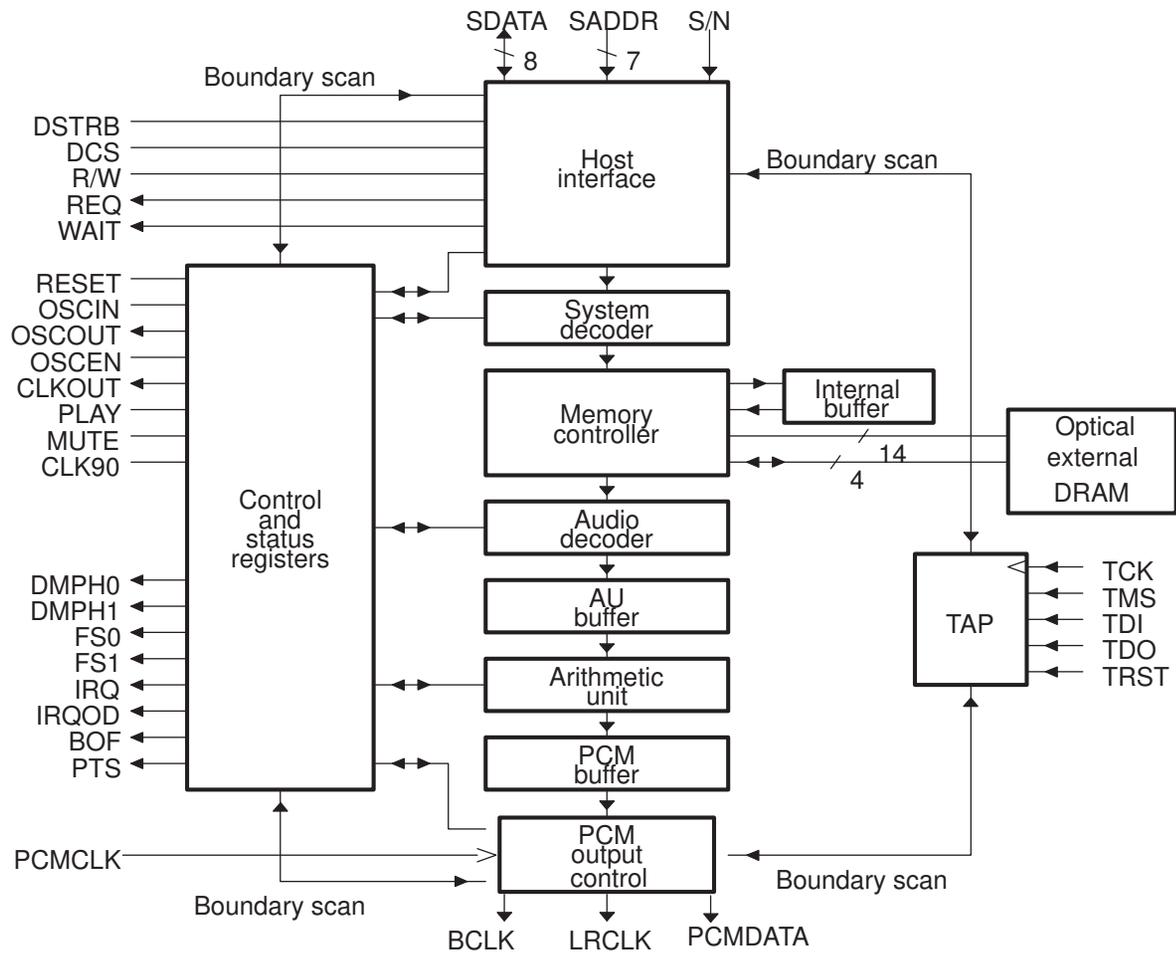
EPIC (enhanced performance implanted CMOS) is a trademark of Texas Instruments

TMS320AV110 Features

Features of the 'AV110 include:

- Single-chip ISO-MPEG (layers 1 and 2) audio decoder
- Decodes mono, dual, stereo, and joint-stereo modes
- Supports all MPEG sampling and data rates, including free format
- Complete with stereo level control
- Input can be MPEG audio frames or the full-multiplexed MPEG system stream
- Accepts compressed audio at up to 15-Mbps burst rate
- Bit-serial or byte-parallel compressed data input
- 16- or 18-bit serial PCM output directly interfaces to most serial DACs
- 8-bit microprocessor control interface
- Supports up to 1-second audio delay for audio/video synchronization (with optional external DRAM)
- Low-power, submicron CMOS technology; fully TTL compatible
- Small-footprint, 120-pin PQFP package

TMS320AV110 Block Diagram



TMS320AV120

The Texas Instruments TMS320AV120 is a low-cost, stand-alone MPEG audio decoder. It implements the ISO-MPEG audio decompression algorithm for layers 1 and 2. MPEG-compliant audio data streams at any of the valid MPEG data and sampling rates are accepted, producing decompressed PCM audio output. Mono, dual, stereo, and joint-stereo modes are supported. The serial-output data stream is suitable for direct input to most commercially available 1-bit D/A converters.

The 'AV120 design produces a simple *plug and play* audio decoder that does not require a host microprocessor for initialization and/or operation. The input is in MPEG audio frame format with provisions for audio/video synchronization. It is a single-chip solution with no provision or need for external buffer memory. The input data rate should match the actual compressed audio bit rate, although the 'AV120 has an input buffer to absorb short-term input bit rate variations. Ancillary data in the bit stream is recovered and output serially. When the compressed audio data is at the actual bit rate, a pulse-width-modulated (PWM) error signal is generated if the PCM output clock is not at the required frequency.

The decoded sampling rate, stereo mode, error status, and deemphasis information is available in the serial status register synchronously with the beginning of the associated PCM data frame. The complete MPEG frame header can also be read from the chip.

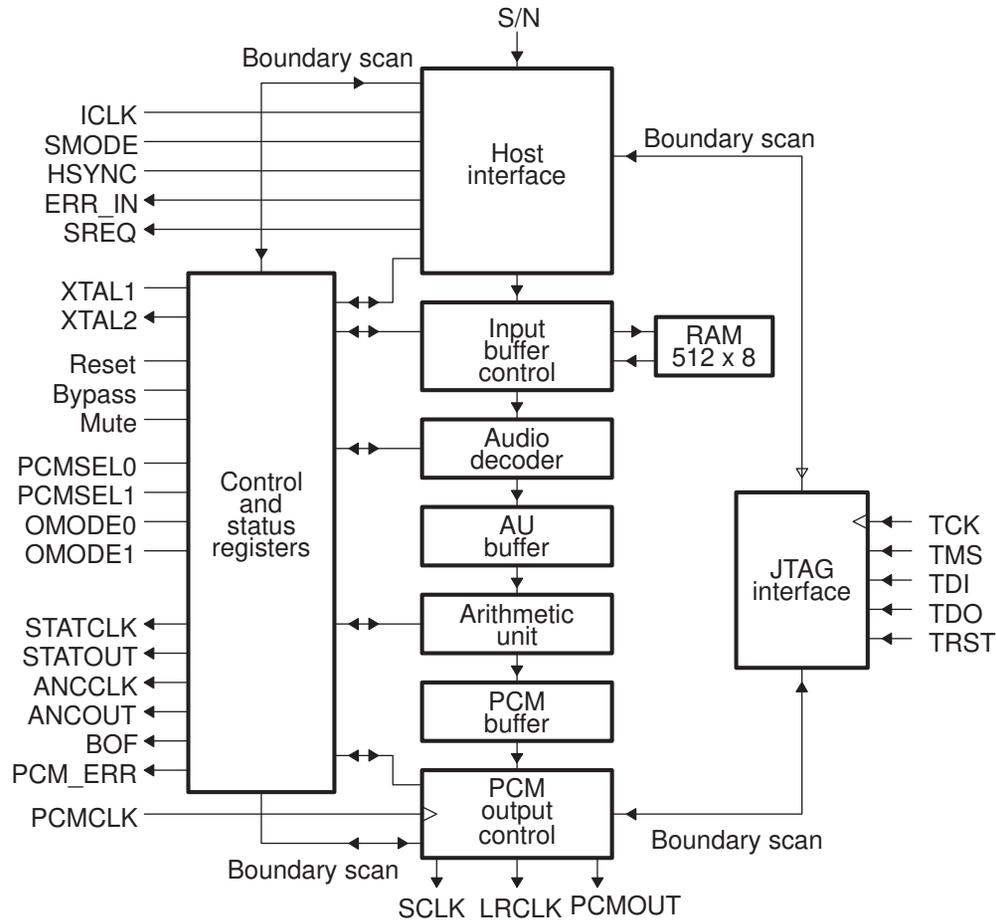
In systems where audio/video synchronization is required, the 'AV120 accepts the system SCR and the audio PTS information and synchronizes the audio output to these time stamps.

TMS320AV120 Features

Features of the 'AV120 are:

- Single-chip ISO-MPEG (layers 1 and 2) audio decoder
- Decodes mono, dual, stereo, and joint-stereo modes
- Supports all MPEG sampling and data rates
- Does not require a host microprocessor for initialization or operation
- Accepts SCR and audio PTS and provides automatic synchronization
- Provides status information at the beginning of every frame
- Interfaces directly to the TMS320AV220 video decoder
- Hardware frame synchronization input
- Supports 16- and 18-bit PCM data
- Recovers and outputs all ancillary data
- PCMCLK-to-input-data-rate synchronization signal
- IEEE standard 1149.1 (JTAG) compatible
- Low-power submicron CMOS technology: fully TTL compatible

TMS320AV120 Block Diagram



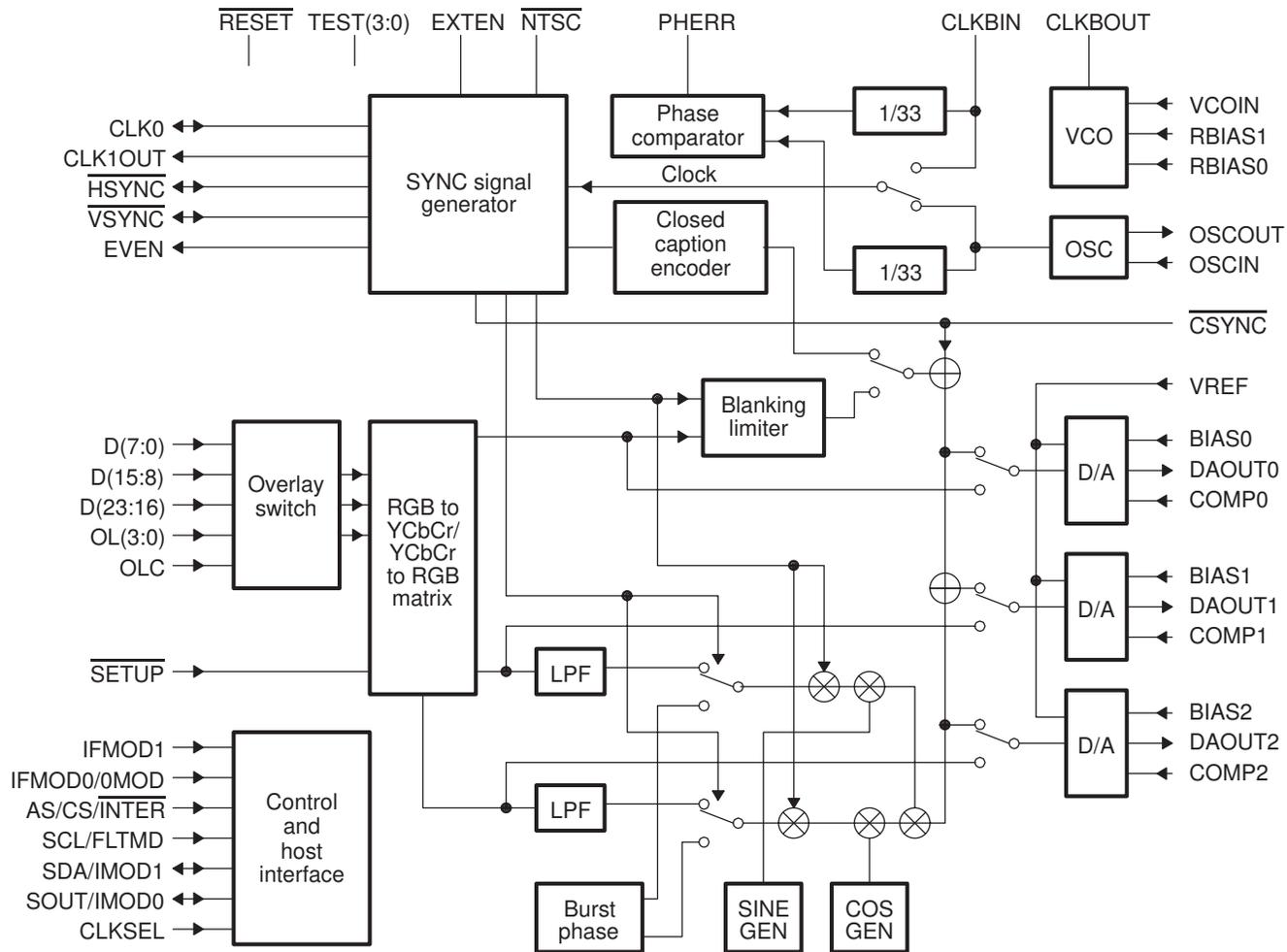
TMS320AV411/410

The 'AV411 is a digital NTSC/PAL encoder targeted toward the television and consumer electronics markets. (For support of the Macrovision anticopy function, the 'AV410 is available to Macrovision licensees.) Multiple input and output formats are available to the user. Digital RGB and luminance [Y], chrominance-blue [Cb], chrominance-red [Cr] (YCbCr) are two common input options. Y and CbCr can be demultiplexed and delivered through two separate data ports (according to the CCIR601 specification).

Key features of the 'AV411/410:

- Input: RGB or YUV
- Output: RGB, Y/C (S-video), or composite video
- On/off-chip synchronized signal generation
- Closed-caption encoding
- 16-color overlay with color lookup table for on-screen display
- Interlaced and noninterlaced operation
- 100-pin PQFP package

TMS320AV411/410 Block Diagram



TMS320AVxxx Generation Summary

This table gives an 'AVxxx-generation product summary so that you can choose the best combination of performance, memory, power, package, and peripherals for your system.

TMS320AVxxx Generation Summary Table

Device Name	Function	Input Format	Output Format	Controller Interface	Off-Chip Memory	Package
TMS320AV110	MPEG audio decoder	MPEG audio stream or MPEG system stream	16- or 18-bit serial PCM	8-bit	Optional 1-MB DRAM	120-pin PQFP
TMS320AV120	MPEG audio decoder	MPEG audio stream serial PCM	16- or 18- bit	None	None	44-pin PLCC
TMS320AV410/411	Digital NTSC/PAL encoder	RGB, YUV	RGB, Y/C (S-vid- eo), or composite video			100-pin PQFP

Mixed Signal Products

Digital signal processing solutions (DSPS) are composed of a DSP core, software, system expertise, and a mixed signal product with peripheral devices such as memory and logic used in embedded systems where the DSP is the primary processor.

The following pages include information on mixed signal products that are well suited to provide interfaces for TMS320 DSPs.

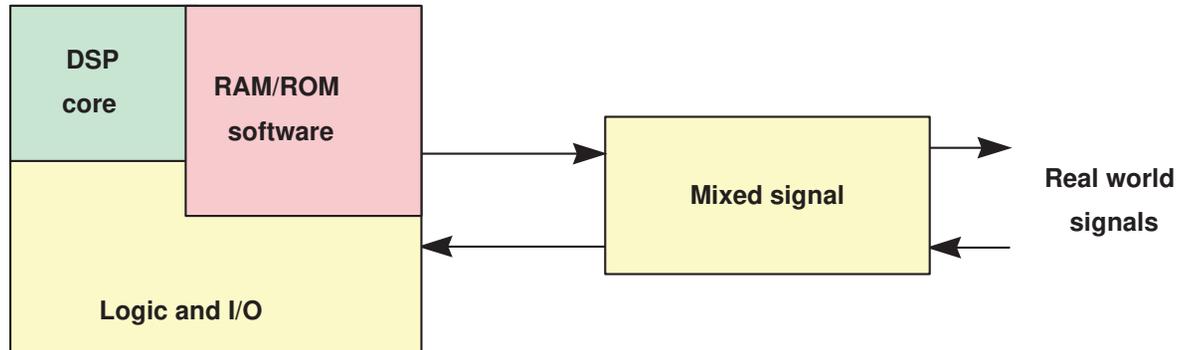
TI Defines DSP Solutions Market

A mixed signal product is one that provides an interface between the digital and the analog world. Digital signal processing solutions can often include a DSP, software, an I/O interface, and mixed-signal products.

TI Defines DSP Solutions Market

DSPS =

- DSP core + mixed signal + system expertise + software
- Embedded systems where DSP is the primary processor



Examples of DSP Solutions

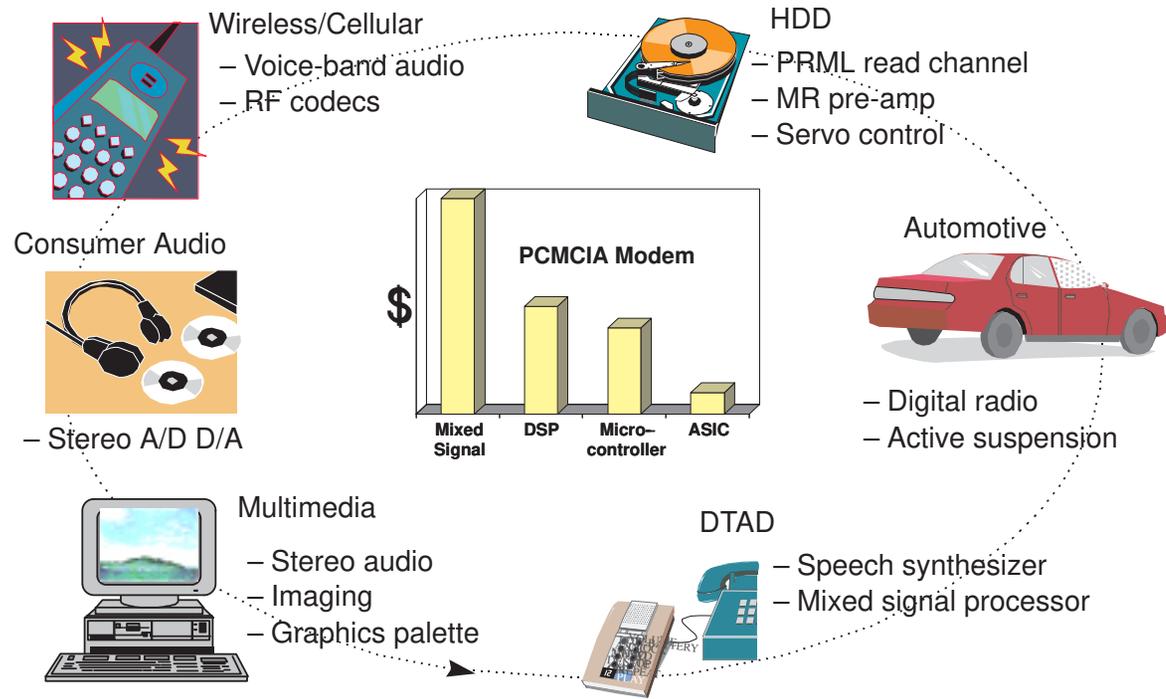
Examples of DSP solutions are:

- Hard disk drives
- Digital telephone answering devices
- Automotive audio and suspension systems
- Multimedia
- Consumer audio
- Wireless/cellular

One of the best examples is the wireless/cellular solution. Originally, cell telephones were the size and weight of a brick, with talk times of 30 minutes. Now, cellular phones fit in your pocket, weigh less than a pound, and have talk times of three hours. These changes have been made possible because of DSP solutions.

The integration of various functions and features within DSP software, the use of an RF CODEC, and the voice band audio processor have made this progress possible.

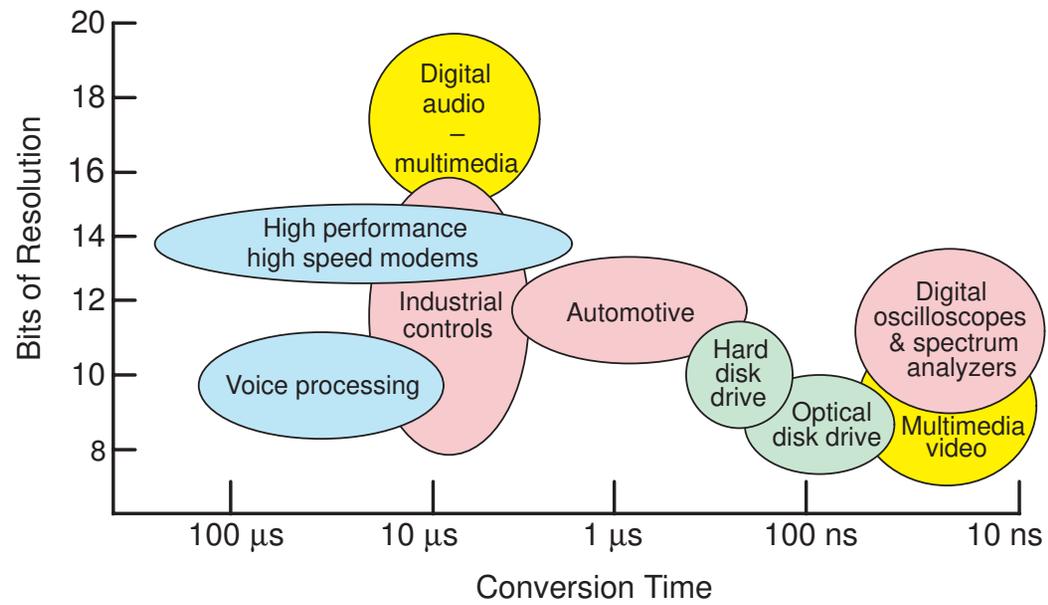
Examples of DSP Solutions



Mixed Signal Enables DSP Solutions

Data converters are the classic forms of DSP peripherals from the analog point of view. Classic data converters — 10- to 12-bit data converters with a ten-microsecond (10- μ s) conversion rate — have been supplied by Texas Instruments and other manufacturers for several years. The new equipment driven by DSPs calls for change in both the audio and visual directions. For video, the need is for greater speed versus a priority on resolution. Generally, speed of 10-ns or below conversion times is acceptable. For audio, resolution takes precedence. Therefore, for the 10- μ s conversion time, 18-bit type conversion is necessary.

Data Converters Span the Range of DSP Markets



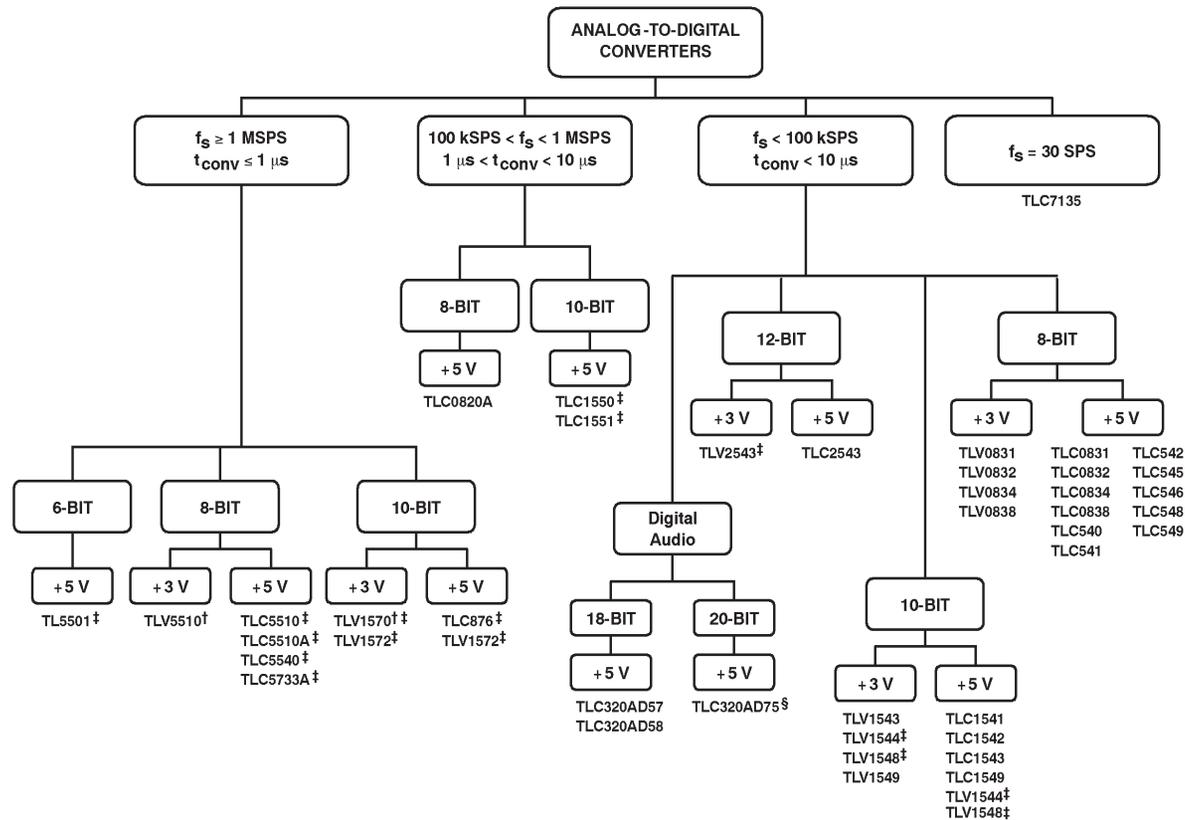
Analog-to-Digital Converters Decision Tree

Analog-to-digital converters (ADCs) are usually chosen based on speed and resolution. This chart is designed to help select the appropriate converter for the desired application.

The first decision is based on speed and is grouped into three speed (sample rate) ranges. The next selection is based on operating voltage, with the last selection based on bits of resolution.

This chart helps with the selection as well as illustrating the range of general-purpose ADCs.

Analog-to-Digital Converters (ADC) Decision Tree Chart

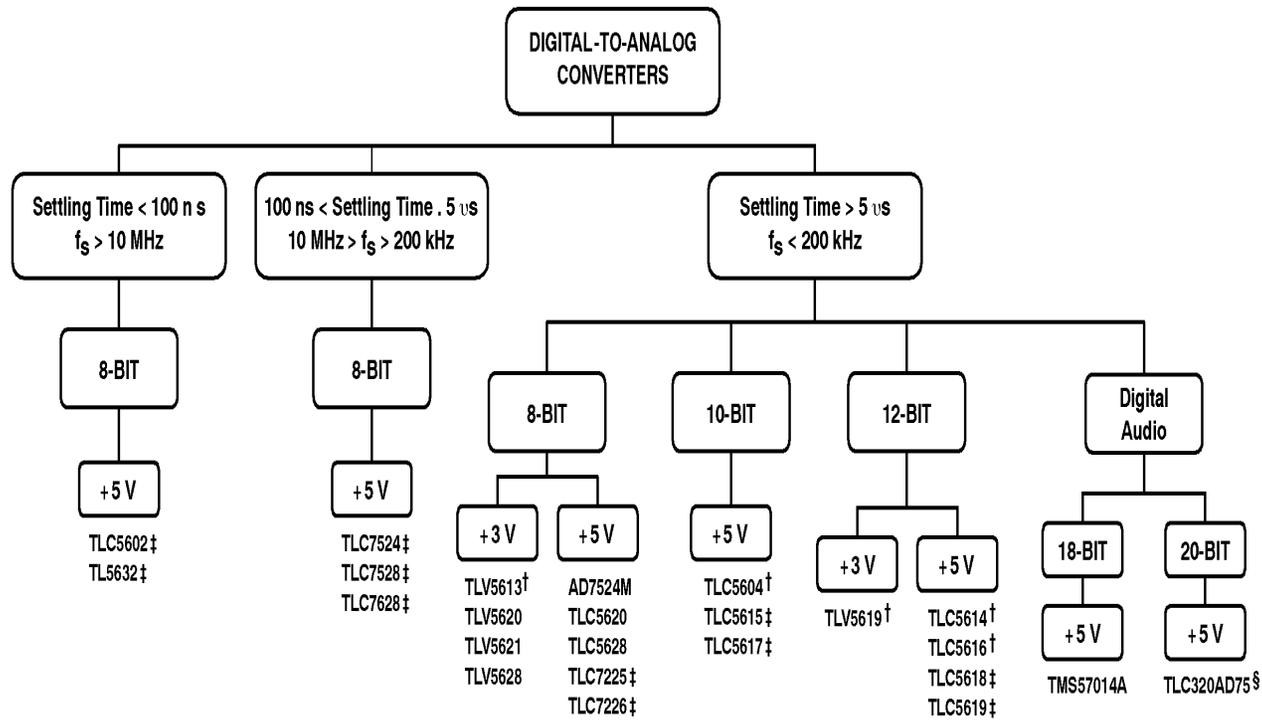


† This part is in the Product Preview stage of development.
 ‡ This part is TMS320 compatible.
 § For this part see Section 4, *Analog Interface Circuits*, for more information.

Digital-to-Analog Converters Decision Tree

This decision tree presents digital-to-analog converters (DACs) with selection based on general applications (general purpose, video graphics, and stereo). This tree is then divided by output type (voltage or current). Although speed is not specifically stated, it is implied that the fastest devices are located in the video graphics path.

Digital-to-Analog Converters (DAC) Decision Tree Chart



† This part is in the Product Preview stage of development.

‡ This part is TMS320 compatible.

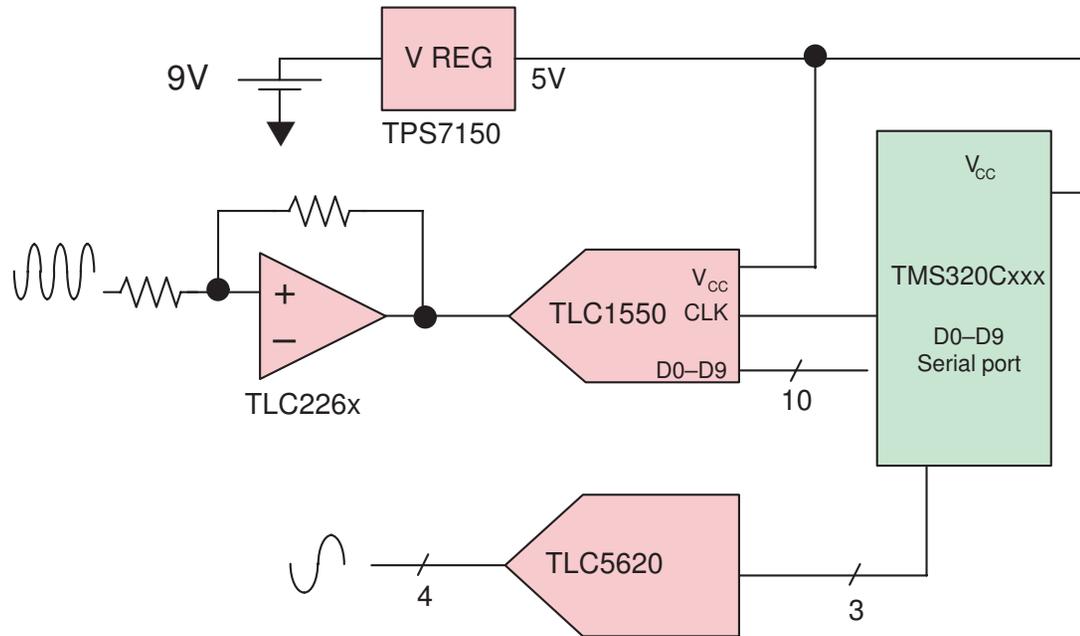
§ For this part see Section 4, *Analog Interface Circuits*, for more information.

DSPS: The Total Solution

A DSP solution for a closed-loop-control system can include both an ADC to sense real world conditions and a DAC to provide proportional feedback or control. Often the requirements for the DAC and ADC are significantly different, requiring separate components for these functions.

This example shows a TLC1550 ADC, which is a 10-bit single-channel converter interfaced through a parallel port to a TMS320Cxxx DSP. The feedback path is from the DSP through a serial port to a TLC5620 which is a quad 8-bit DAC.

DSPs: The Total Solution Block Diagram



10-Bit, 6- μ s ADC: TLC1550, TLC1551

The TLC1550 and TLC1551 ADCs are successive approximation converters that offer a high sample rate (166 Ksps) with a low-cost architecture. They feature a parallel interface for speed and a selectable external or internal clock for versatility.

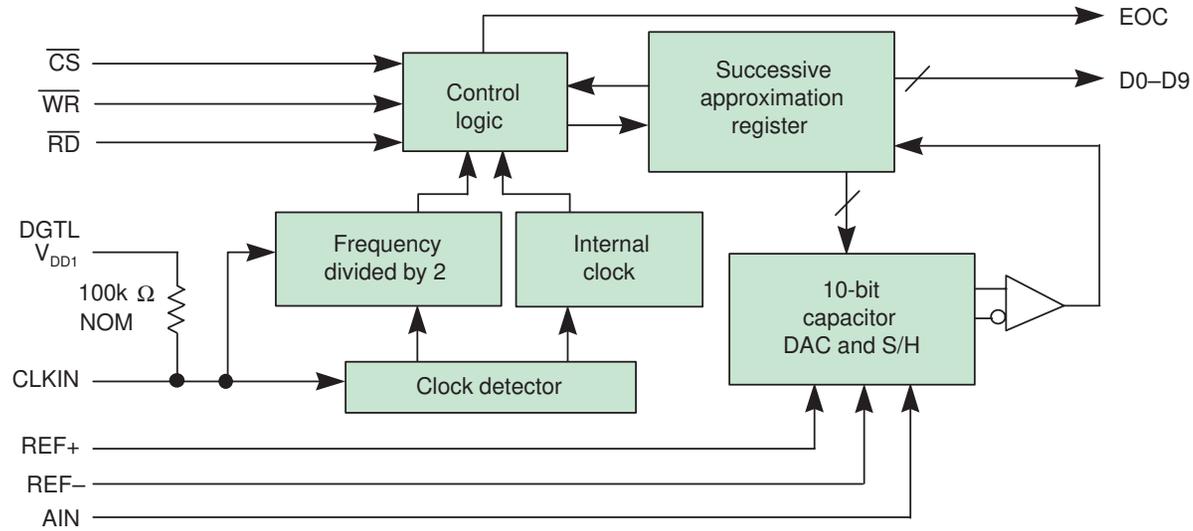
Key features:

- Single 5-V power supply
- 3-state outputs
- Power dissipation of 40 mW maximum
- Fast parallel processing for DSP and μ P interface
- Either external or internal clock can be used
- DSP/ μ P interface compatible
- Conversion time of 6 μ s
- 166-Ksps sample rate
- Total unadjusted error
 - TLC1550— ± 0.5 LSB maximum
 - TLC1551— ± 1.0 LSB maximum

Applications/end equipment:

- Vehicle active suspension
- Data acquisition systems
- DSP front ends
- Industrial controls
- Digital motor control

10-Bit, 6- μ s ADC: TLC1550, TLC1551 Functional Block Diagram



TLC5620 Quad DAC

The TLC5620 quad DAC has individual reference inputs for each of the four DACs. This feature enables this circuit to be used as four DACs with separate ranges, as programmable gain blocks, or a combination of both. The flexibility, simple serial interface, and small (14-pin) package make this circuit well suited to a number of control feedback circuit applications.

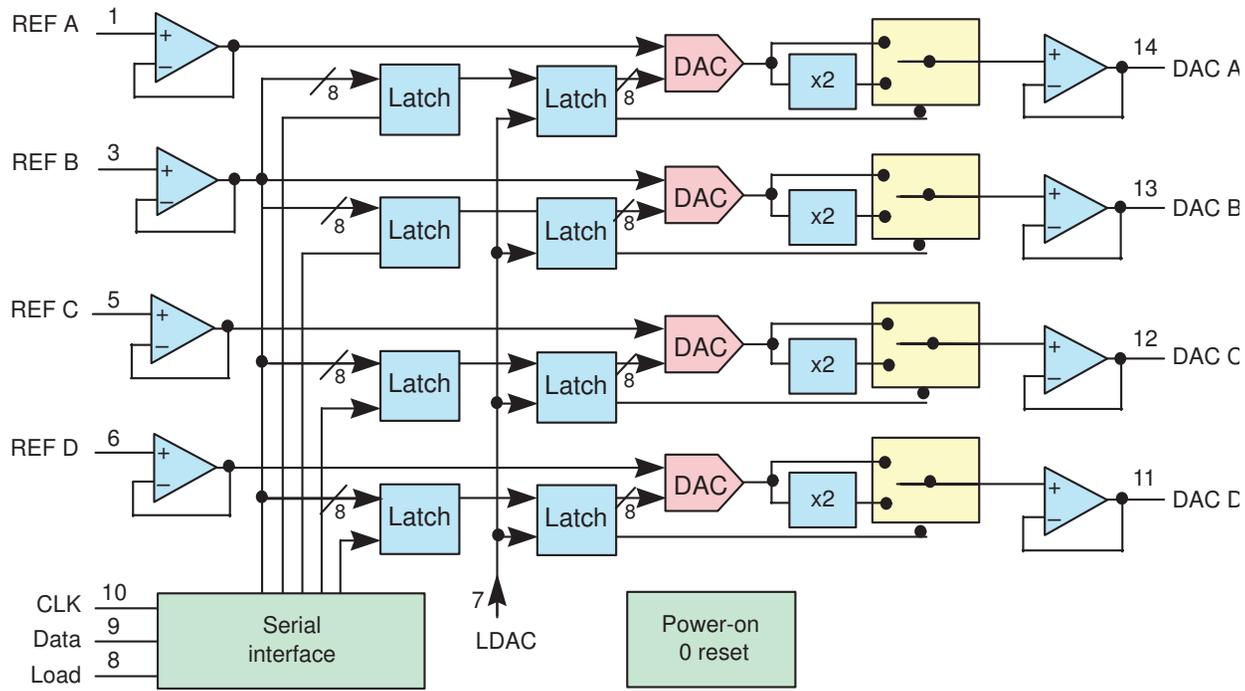
Key features:

- Four 8-bit voltage output DACs
- Each DAC has own V_{REF}
- Serial input clock rate—1 MHz maximum
- Buffered reference inputs
- Programmable 1 or 2 times output range
- Double buffered registers for synchronous updates
- Internal power-on reset
- Low power consumption—20 mW maximum
- Characterized operating temperatures:
 - TLC5620C: 0° to 70°C
 - TLC5620: 40° to 85°C

Applications/end equipment:

- Programmable voltage sources
- Digitally-controlled amplifiers/attenuators
- Wireless communications
- Automatic test equipment
- Process monitoring and control
- Signal synthesis

TLC5620 Quad DAC Functional Block Diagram



What is an Analog Interface Circuit?

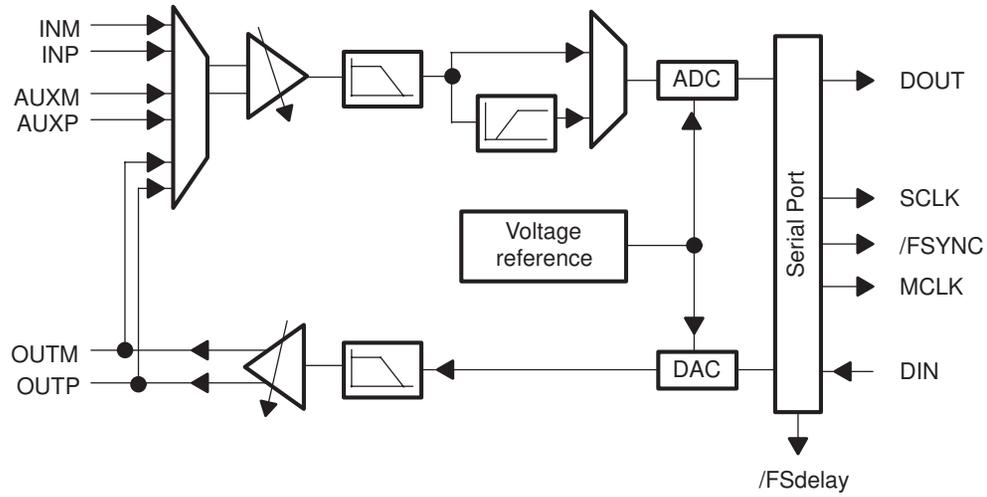
The analog interface circuit (AIC) is a complete analog interface system designed to convert audio-signal data into digital format by the ADC channel. It provides the interface and control logic to transfer data between its serial input and output terminal and a DSP.

The system consists of an ADC with input amplifier MUX and antialiasing filter, DAC path with reconstruction filter and output amplifier, and the necessary serial data interfaces.

The AIC products were originally designed for modem-type applications; however, they are currently being used with DSPs in applications such as:

- Modems (V.34+, telephony, DSVD)
- Speech processing
- Speech analysis
- Voice encryption/decryption
- Industrial process controls
- General 16-bit DSP applications

Analog Interface Circuit



TLC320AD50 16-bit Sigma-Delta Analog Interface Circuit

The TLC320AD50 is a 16-bit analog interface circuit (AIC). It is a versatile analog front end for business audio and modem applications. It provides high resolution signal conversion using an oversampling sigma-delta technique.

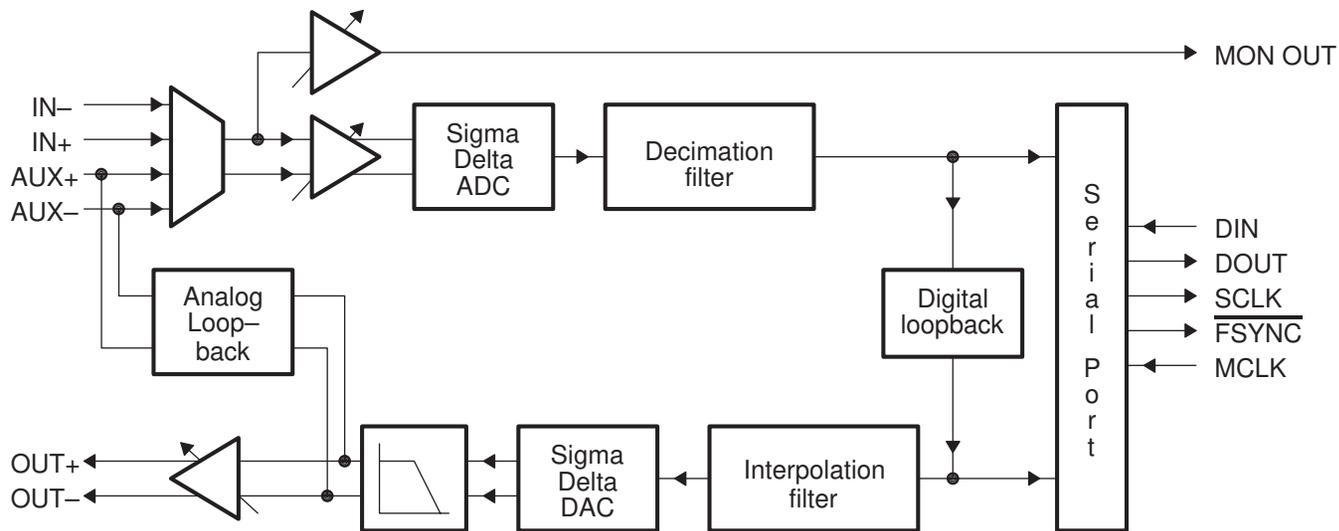
Key features:

- Master/slave mode (supports up to 3 slaves)
- Differential output drives 600 ohm load
- Single 5-V supply or 5-V analog and 3-V digital
- Power-down mode to 7.5 mW
- Input and output gain control
- Glueless DSP interface
- Characterized for operation from 0° and 70° C

Applications:

- Modems (V.34+, DSVD, telephony)
- PCMCIA fax modems
- DSP analog interface
- Noise suppression/cancellation
- Acoustical signal processing
- General purpose 16-bit signal processing
- Industrial process control

TLC320AD50 16-bit Sigma-Delta Functional Block Diagram



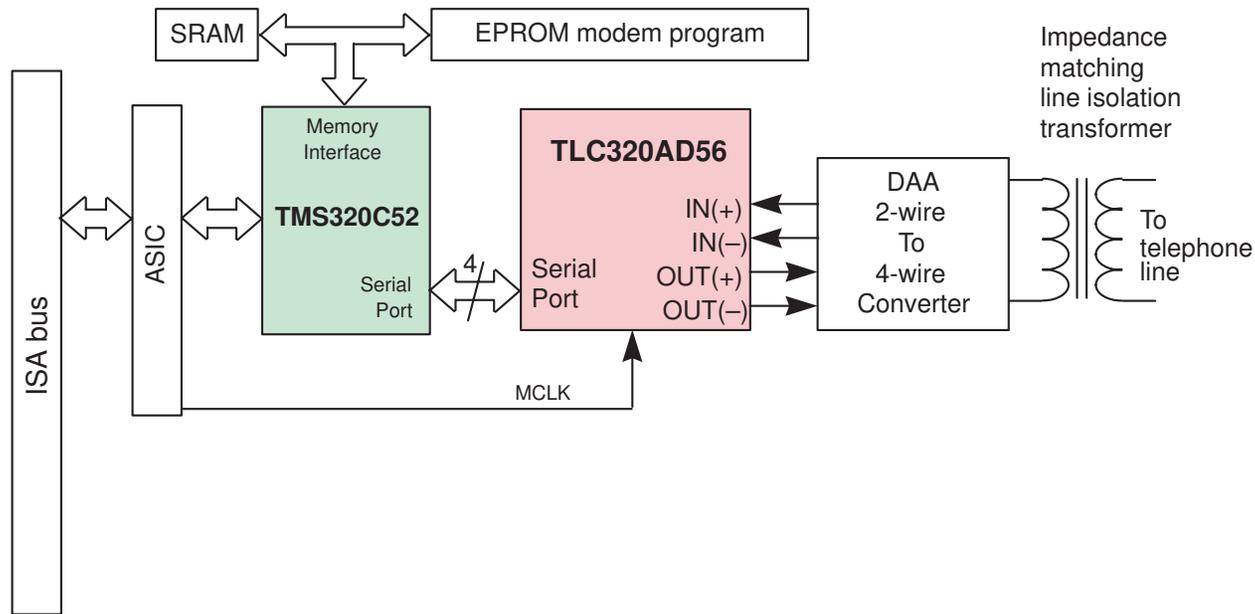
V.34+ Modem Architecture

The V.34+ modem performance is specified up to 33.6 kbps. This data rate, plus the necessity to be downward compatible with previous modem standards, adds complexity to the software and can require additional processor MIPS and memory size.

Features:

- The V.34+ modem standard requires higher signal-to-noise (SNR) performance from the AIC, so a higher performance sigma-delta converter is used.
- The V.34+ architecture is the same as V.32bis, but with increased memory and processor MIPS requirements.

V.34+ Modem Architecture Functional Block Diagram



TLC320AD55 Sigma-Delta Analog Interface Circuit

The TLC320AD55 is a 16-bit analog interface circuit (AIC). A sigma-delta architecture is employed to achieve high performance. This circuit provides the functionality and performance necessary to implement applications such as the V.34+ modem.

Features:

- 16-bit resolution
- Power-down mode
- Serial port interface
- Antialiasing and antiimaging filters
- 89-dB dynamic range
- 80-dB S/N ratio
- Output gain control

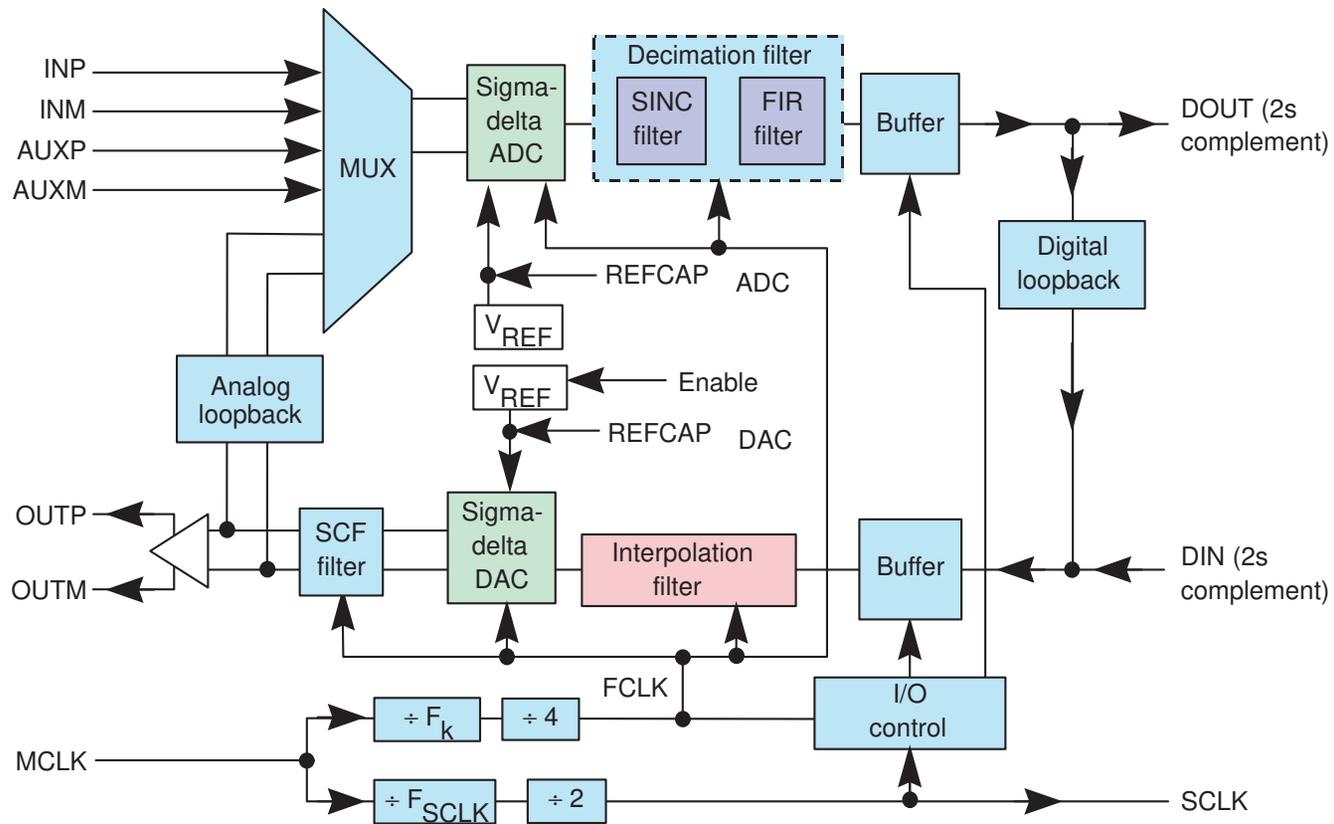
Applications:

- V.34+ modems
- DSP analog interface
- Noise cancellation/suppression
- Speech processing
- Industrial process control

Package:

- 28-pin SOIC (DW)

TLC320AD55 (Sigma-Delta AIC) Functional Block Diagram



TLC320AD56 Sigma-Delta Analog Interface Circuit

The TLC320AD56 is a 16-bit sigma-delta analog interface circuit (AIC). It is a versatile analog front-end interface for business audio and modem applications.

Features:

- 16-bit resolution
- Power supply: Single 5-V or 5-V analog / 3-V digital
- Power-down mode to <1 mW
- Serial port interface
- 91-dB dynamic range
- 88-dB S/N+D (ADC)
- 85-dB S/N+D (DAC)
- 16-bit resolution

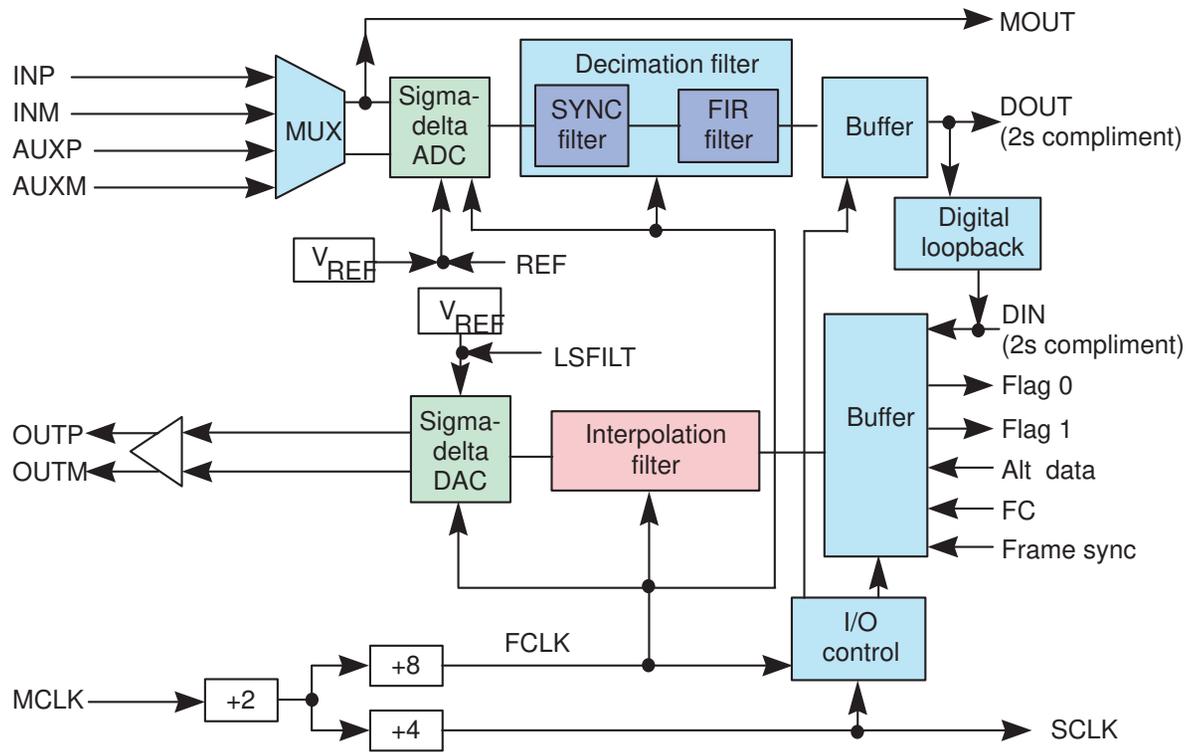
Applications:

- V.34+ modems
- DSP analog interface
- Noise cancellation
- Speech processing
- Industrial process control
- Business audio

Package:

- 28-pin PLCC
- 48-pin TQFP (PCMCIA)

TLC320AD56 Functional Block Diagram



TLC320AD57/58 Stereo Audio ADCs

The TLC320AD57 and TLC320AD58 are stereo analog-to-digital converters that use the sigma-delta architecture. These devices contain two separate converters with a common control and serial interface.

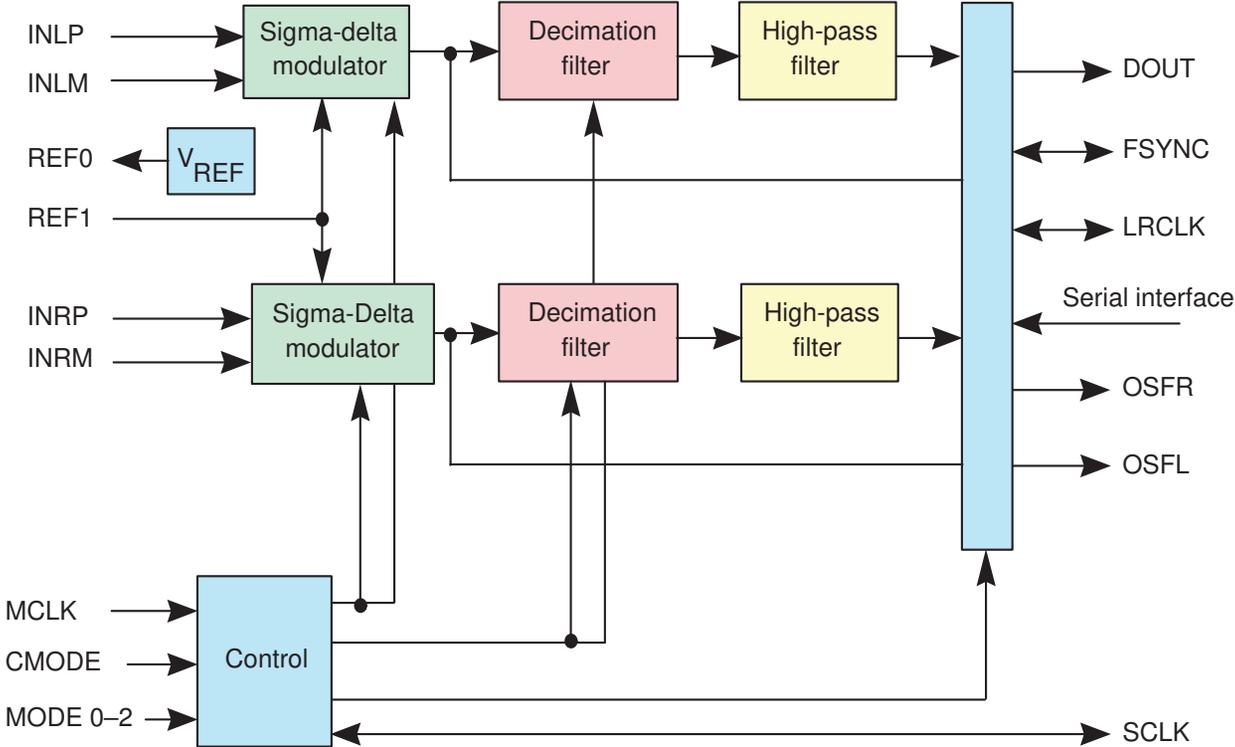
Features:

- 16-/18-bit resolution
- Power supply: single 5 V
- Power-down mode
- Serial port interface
- 95-dB dynamic range
- 93-dB S/N+D
- Sample rates to 48 kHz

Applications:

- Consumer audio
- Digital radio
- Industrial process control
- Multimedia audio
- Workstations
- DSP analog interface

TLC320AD57/58 Functional Block Diagram



TMS57014A Dual 16-/18-Bit Audio DAC

The TMS57014A is a dual DAC using sigma-delta architecture. This product features two separate DAC channels with a common serial data interface.

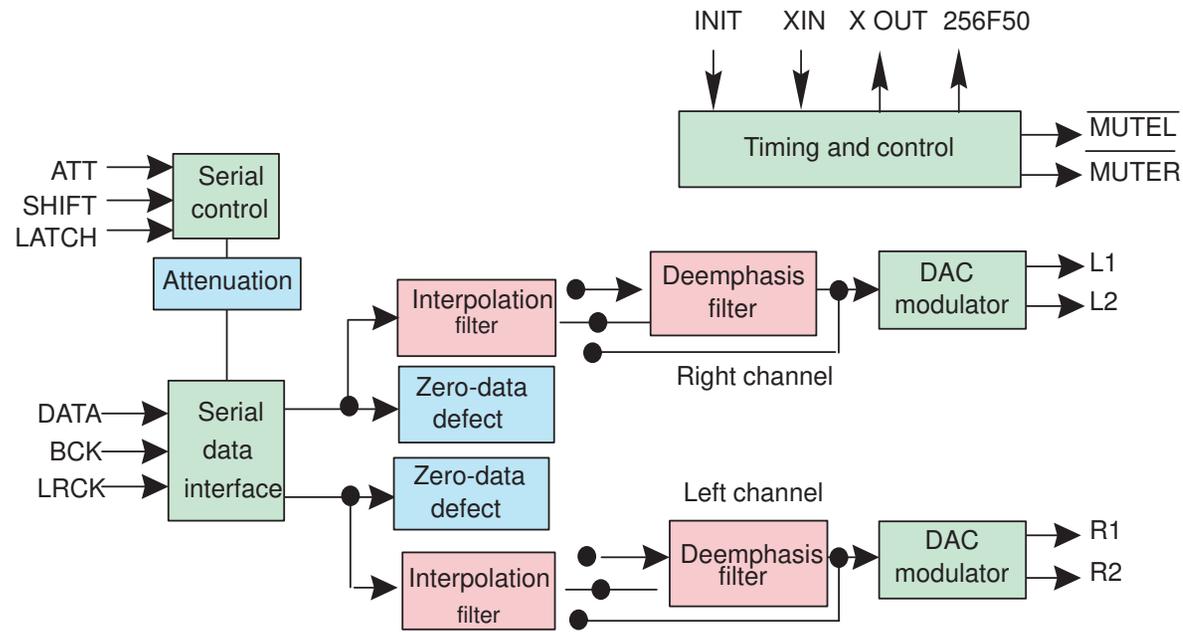
Key features:

- 18-bit resolution
- Sample rates up to 48 kHz
- Deemphasis filter for 32, 37.8, 44.1, and 48 kHz
- Digital soft mute to -60 dB
- Single 5-V DC supply
- Mute capability with zero data detect flags
- Pulse-width-modulation (PWM) output
- Serial port interface

Applications/end equipment:

- Digital audio systems
- Professional quality audio
- High-performance, audio-speed DAC
- Waveform generation
- Automated test systems

TMS57014A Dual 16-/18-Bit Audio DAC Functional Block Diagram



Development Tools and Support

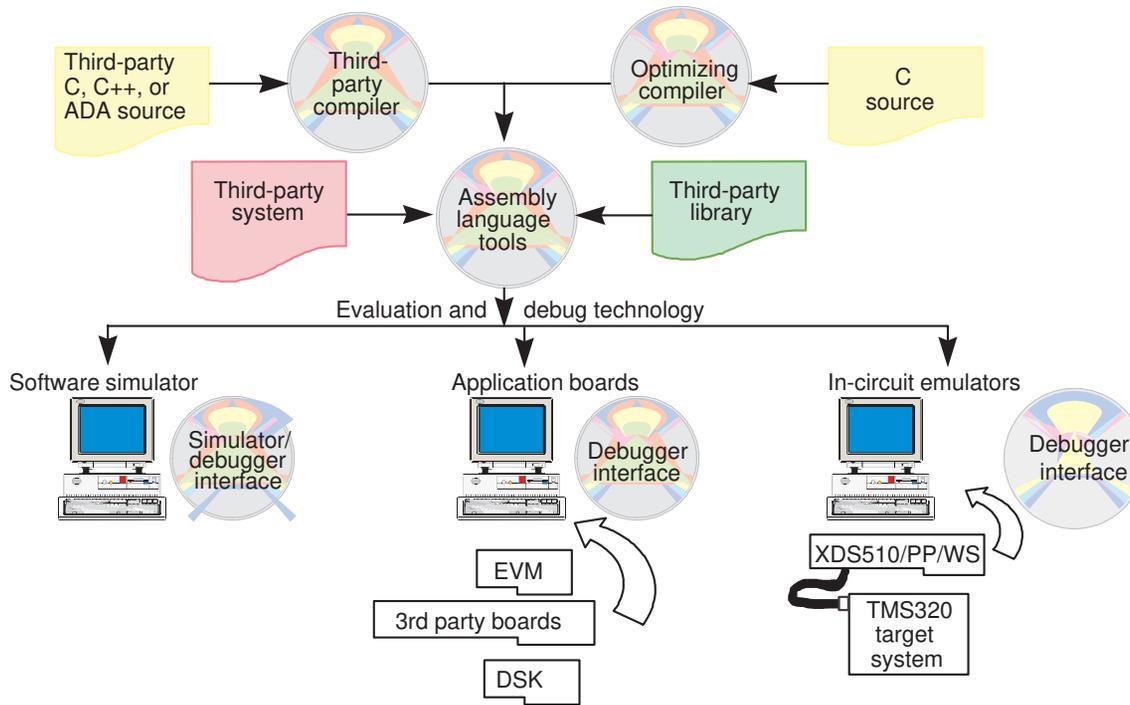
Fast time to market, increased productivity, and ease of design-in are of primary importance when developing a DSP-based system. To meet these needs, TI offers a complete suite of code-generation and debug tools as well as a broad and innovative range of third-party tools. TMS320 DSP tool support eases the design process from initial concept through integration and production, enabling customers to take full advantage of rapidly evolving DSP technologies.

TMS320 Development Tools Overview

The standard flow for development begins with code written in a high-level language (such as C) or assembly language. This code can be debugged on one of several debug platforms (simulator, emulator, etc.), all of which feature the same debugger interface.

Software and hardware can be developed in parallel by using the TMS320 compiler, assembler/linker, simulator, evaluation module (EVM), and by using the TMS320 behavioral models and emulators for hardware development.

TMS320 Development Tools Overview



TMS320 Optimizing C Compilers

TI's TMS320 C compilers translate ANSI-standard C code into TMS320 assembly language. The compilers enhance productivity by enabling customers to take advantage of the ease and speed of programming in C, while creating highly optimized code that compares favorably to hand-coded assembly. For critical DSP algorithms that demand the extreme performance of hand-coded assembly, the compiler provides a simple and accessible interface that easily enables the integration of assembly with C.

The compilers support four levels of general optimizations. You can select the level of optimization that you want to use. Additionally, each version of the compiler supports processor-specific optimizations to take advantage of the unique features of the individual DSP architectures. For example, the 'C8x compiler supports both the on-chip parallel processing PPs and the RISC-like master processor (MP), allowing for easy implementation of data and message-passing between tasks in parallel-processing systems.

The compiler package includes an ANSI-standard runtime-support library, a source interlist utility to enable customers to associate assembly language statements with the C code that produced them, and a shell program that allows customers to compile and link their programs to create executable code in one step.

TMS320 Optimizing C Compilers

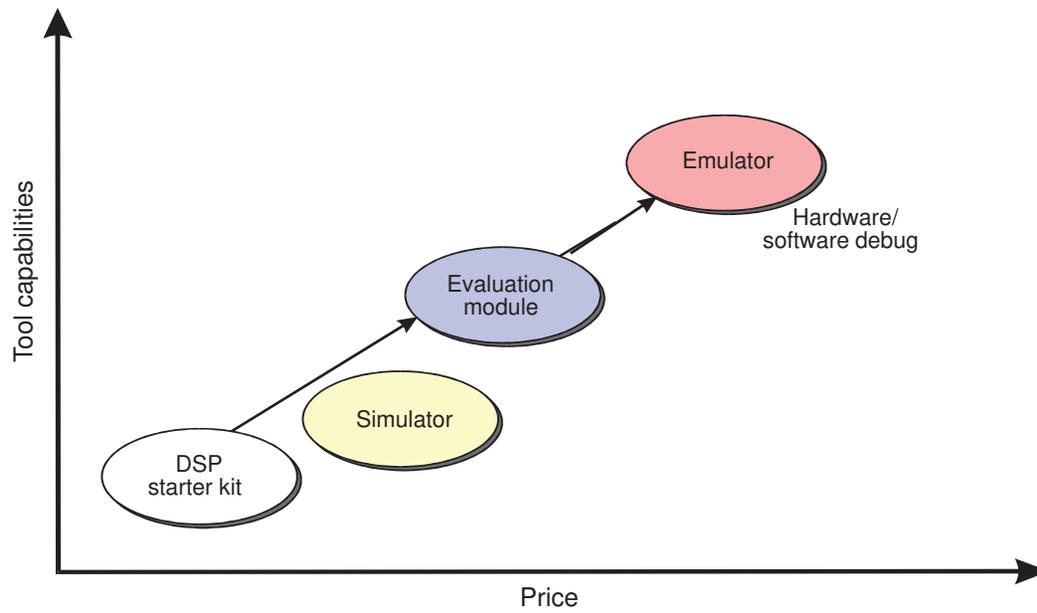
- Parallel instructions
- Autoincrement addressing
- Register tracking/targeting
- Three-operand instructions
- Delayed branches
- Jump optimizations
- Common subexpression elimination
- Algebraic reordering/stack height reduction
- Copy propagation
- Software pipelining
- Dead assignment elimination
- Loop induction variable optimizations/strength reduction
- Loop rotation
- Loop-invariant code motion
- Symbolic simplification/constant folding
- Prioritized register allocation
- Alias disambiguation
- In-line expansion of run-time support library functions
- Register variables

TMS320 Debug Tools Price/Performance Comparison

The TI DSP starter kit (DSK) is a low-cost, flexible, and easy-to-use DSP tool designed for entry-level evaluation. TMS320C3x, TMS320C5x, and TMS320C54x versions are available.

The TMS320 simulators are software programs that perform instruction-level simulation of a TMS320 device and are available for all fixed-point, floating-point, and multiprocessor DSPs. TMS320 evaluation modules (EVMs) are low-cost development systems for device evaluation, benchmarking, and system debug. EVMs are available for the TMS320C24x, 'C3x, 'C5x, and 'C54x generations. The 'C6x EVM will be available in 2Q98. The 'C5x EVM is also used for development with the 'C2xx generation. For the 'C4x family, TI offers the parallel processing development system (PPDS) to aid in system development. The extended development systems (XDS™) are powerful, full-speed emulators used for system-level integration and debug. TI provides emulators that support all TMS320 DSPs.

TMS320 Debug Tools Price/Performance Comparison Block Diagram



DSP Starter Kit (DSK)

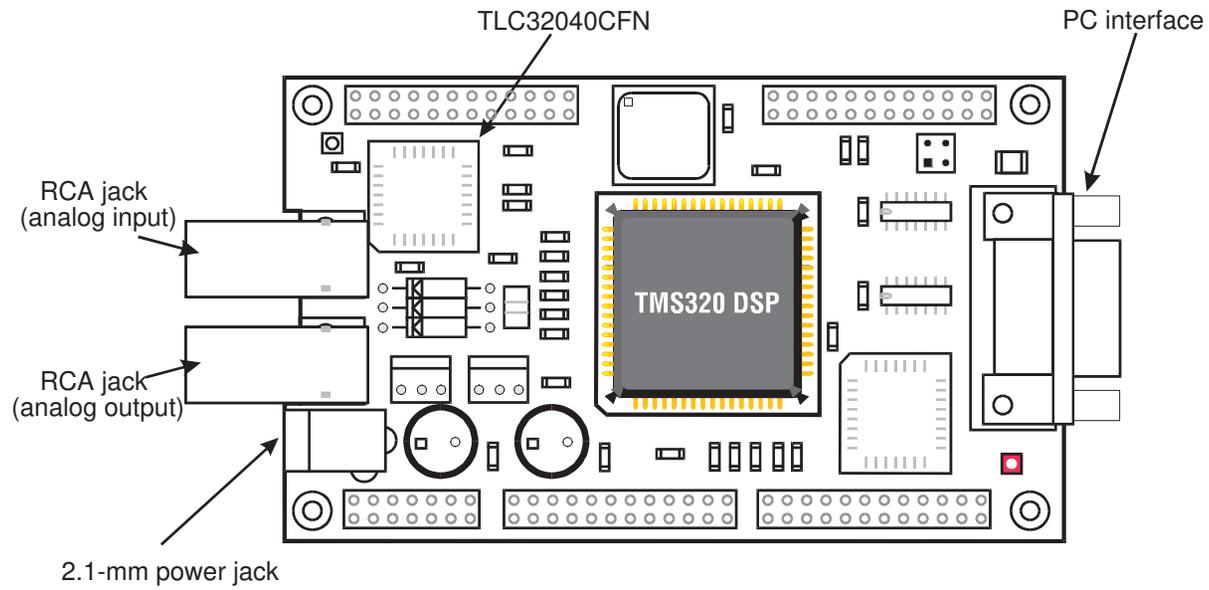
The DSP starter kit (DSK) is the ideal tool for anyone interested in evaluating a DSP platform. The TMS320C3x, TMS320C5x, or TMS320C54x DSK offers the benefits of hardware execution and software support at a low cost. The power and speed of the industry-standard TMS320 DSPs, combined with an assembler and debugger, provide a rich development environment for benchmarking and evaluating code in real time. With the analog-ready interface, you can easily benchmark and test applications such as control systems, audio, and speech processing.

All of the DSKs ('C3x, 'C5x, or 'C54x) come with a TMS320-based board, software, and documentation package. Each DSK board contains:

- An interface port for communicating with your PC
 - RS-232: 'C5x
 - Parallel: 'C3x, 'C54x
- Two standard RCA jacks providing direct connections to a microphone or speaker
- An analog interface chip
- 2K 32-bit words of on-chip RAM on the 50-MHz TMS320C3x board or 10K 16-bit words on the 40-MHz TMS320C5x board.

Also included in the kit are the DSK assembler, assembly language debugger, loader, and sample programs.

DSP Starter Kit (DSK) Diagram



TMS320 Debugger Interface

The C/assembly source debugger is the standard interface for the simulator, evaluation module, and emulator. Its friendly window-, mouse-, and menu-driven interface reduces learning time and eliminates the need to memorize complex commands.

The debugger provides complete control over program execution with features like conditional execution and single-stepping. You can set or clear a breakpoint with a click of the mouse. You can debug C, assembly, or a combination of both. These features allow you to debug your code in the same language in which it was written.

Commands can be entered in the command window or accessed through pulldown menus. Symbolic debug is supported, so structure and variable names can be used instead of addresses or data locations.

Watch and display windows allow you to easily display and edit the values of variables, arrays, structures, pointers, and registers in their natural format. Formats include floating point, integer, character, enumerated, or pointer.

The calls stack window displays function names in the order that they are called and put on the stack. A function name is removed when popped from the calls stack. This allows you to debug a program that is not executing properly because of a lack of stack space.

CPU registers can be displayed in a choice of formats and can also be edited. This feature gives a machine-level picture of chip functionality.

Memory contents can be displayed and edited. This allows you to observe the movement of data, as well as compare expected values to actual ones.

For the 'C4x, 'C5x, 'C54x, 'C6x, and 'C8x XDS510, the debugger includes a parallel debug manager for debugging multiple processors in one system.

TMS320 Debugger Interface

TMS320C80 C/Assembly Source Debugger

mpsim (MP)

Loac Break Watch Memory Color Mode Run=F5 Step=F8 Next=F10

DISASSEMBLY

02000920	00200003	bsr	TaskCreateTask
02000924	c80b8001	or.tt	0x1,r0,r25
02000928	c80b8000	or.tt	0x0,r0,r25
0200092c	08ac8000	addu	0x0,r2,r1
02000930	10746000	ld.d	r0(r1),r2
02000934	50518008	ld.d	0x8(r1),r10
02000938	60518010	ld.d	
0200093c	70518018	ld.d	

FILE: task.c

```

0367  * Allocate task descriptor an
0368  */
0369  size = (sizeof(TASK) + stackSi
0370  task = (TASK *)malloc(size);
0371  if (!task)
0372  return (0); /* failed to
0373  */
0374  * Initialize fields of task des
0375  */
0376  task->state = TASK_STAT
                    
```

CALLS

1: TaskCreateTask ()

WATCH

1: cmdBuf 0x00000001
2: i 3
3: ip 0x0200093c
4: r1 34001344

DISP: PPCMDBUF

link 0x4c454b44
flag 1581024353
function 0x7362667c
args 0x615f8594
mailbox 0xab764c5c
msgValue 1246519106
intCode 1114731852
ppNum 932222789

CPU

ip 0200093c
pc 02000940
ir 00f88000
r1 0206d1c0
r2 00000000
r3 02000558
r4 00000000
r5 00000000
r6 00000000
r7 00000000
r8 00000000
r9 00000000
r10 00000000
r11 00000000
r12 00000000
r13 00000000
r14 0206d1c0
r15 020eb088

MEMORY

020004f0 086cffe0 10598010 70598018
020004fc 00305000 800000ff 1838b000
02000508 02001814 1838b000 02001af0
02000514 1838b000 020014d8 c83b3000
02000520 02000050 c03b3000 02008278

COMMAND

```

register int stackSize;

step
whatis size
register int size;

>>>
                    
```

pull-down menus

disassembly display

C source display

interactive command entry and history window

function call traceback

natural-format data displays

scrolling data displays with on-screen, interactive editing

TMS320 Development Tool Summary

Assembler/Linker: Available for all TMS320 devices, the assemblers and linkers are code-generation tools that convert TMS320 assembly language source files into executable object code. These are included in EVMs and C compiler packages.

C compiler: Available for the 'C2xx, 'C3x, 'C4x, 'C5x, 'C54x, 'C6x, and 'C8x, the TMS320 C compiler translates ANSI-standard C language files into highly-efficient TMS320 assembly language source files. The C compiler includes an assembler/linker.

Simulator: Available for all TMS320 devices, the simulator is a software program that simulates the TMS320 microcontroller and microprocessor modes for cost-effective, non-real-time development. With the inexpensive software simulator, you can debug without target hardware. The simulator includes the high-level-language (HLL) debug interface.

Evaluation module (EVM): EVMs are PC add-in boards that include the target processor, a small amount of memory, and limited peripherals. This allows you to run code in real time and interface to an external system. The EVM includes the HLL debug interface and the assembler/linker.

Emulators (XDS™): The 'C2xx, 'C3x, 'C4x, 'C5x, 'C54x, 'C6x, and 'C8x use a scan-based technology for emulation with the XDS510PP/510WS. The emulators include the HLL debug interface.

DSP starter kit (DSK): Low-cost, simple, stand-alone application board that lets you experiment with either 'C24x, 'C3x, 'C5x, 'C54x, or 'C6x DSPs for real-time signal processing. The DSK board comes with a debugger and limited assembler.

Parallel processing development system (PPDS): The PPDS is a standalone TMS320C4x target board that allows you to develop, run, and debug a system with four 'C4x devices. For a complete system, the XDS510™ is necessary.

TMS320C2xx Development Tools

Part Number	Product Description	Host	OS
TMS320C2xx Tool Set			
Code Development Tools			
TMDS3242850-02	Assembler/linker	PC	OS/2, DOS Ext
TMDS3242855-02	C Compiler/assembler/linker	PC	OS/2, DOS Ext
TMDS3242555-08	C Compiler/assembler/linker	SPARC/HP9000	SunOS, HP-UX
Debug Tools			
TMDX324X851-02	Simulator	PC	Win, DOS
TMDX324X551-09	Simulator	SPARC	OpenWindows
TMDX324012xx	XDS510 debugger	PC	OS/2, Win, DOS
TMDX324062xx	XDS510WS debugger	SPARC	OpenWindows
TMDS00510	XDS510 board	PC (ISA bus)	N/A
Includes JTAG emulator cable			
TMDS00510WS	XDS510WS box	SPARC	OpenWindows
Includes JTAG emulator cable		N/A	N/A
TMDS3080002	JTAG emulator cable	N/A	N/A
TMDX324002xx	Emulator porting kit	PC/SPARC	N/A

- Current as of December 1997. Up-to-date version number, release date, and host/OS information is available on our web pages.
- SPARC software can run under SunOS 4.1.3 or higher or Solaris 2.x with the binary compatibility package.
- OpenWindows = OpenWindows 3.x
- Win = Win16 = MS-Windows 3.x
- HP9000 = HP9000 Series 700 running HP-UX 9.x
- DOS = MS-DOS
- DOS Ext = DOS/4GW DOS Extender
- N/A = Not applicable
- License must be signed in order to purchase the Emulator porting kit

TMS320C5x Development Tools

Part Number	Product Description	Host	OS
TMS320C5xToolset			
Code Development Tools			
TMDS3242850-02	Assembler/linker	PC	OS/2, DOS Ext
TMDS3242855-02	C Compiler/assembler/linker	PC	OS/2, DOS Ext
TMDS3242555-08	C Compiler/assembler/linker	SPARC/HP9000	SunOS, HP-UX
Debug Tools			
TMDS3245851-02	Simulator	PC	Win, DOS
TMDS3242551-09	Simulator	SPARC	OpenWindows
TMDS3240150	XDS510 debugger	PC	OS/2, Win, DOS
TMDS3240650	XDS510WS debugger	SPARC	OpenWindows
TMDS00510	XDS510 board	PC (ISA bus)	N/A
	Includes JTAG emulator cable	N/A	N/A
TMDS00510WS	XDS510WS box	SPARC	OpenWindows
	Includes JTAG emulator cable	N/A	N/A
TMDS3080002	JTAG emulator cable	N/A	N/A
TMDX3240050	Emulator porting kit	PC/SPARC	N/A
TMDS3260050	'C50 EVM	PC (ISA bus)	Win, DOS
	Includes debugger		
TMDS3200051	'C50 DSK	PC (UART)	DOS
	Includes software		

- Current as of December 1997. Up-to-date version number, release date, and host/OS information is available on our web pages.
- SPARC software can run under SunOS 4.1.3 or higher or Solaris 2.x with the binary compatibility package.
- OpenWindows = OpenWindows 3.x
- Win = Win16 = MS-Windows 3.x
- HP9000 = HP9000 Series 700 running HP-UX 9.x
- DOS = MS-DOS
- DOS Ext = DOS/4GW DOS Extender
- N/A = Not applicable
- License must be signed in order to purchase the Emulator porting kit

TMS320C54x Development Tools

Part Number	Product Description	Host	OS
TMS320C54x Tool Set Code Development Tools			
TMDS324L850-02	Assembler/linker	PC	OS/2, DOS Ext
TMDS324L855-02	C compiler/assembler/linker	PC	OS/2, DOS Ext
TMDS324L555-08	C compiler/assembler/linker	SPARC	SunOS
Debug Tools			
TMDS324L851-02	Simulator	PC	Win, DOS
TMDS324L551-09	Simulator	SPARC	OpenWindows
TMDS32401L0	XDS510 debugger	PC	OS/2, Win, DOS
TMDS32406L0	XDS510WS debugger	SPARC	OpenWindows
TMDS00510	XDS510 board	PC (ISA bus)	N/A
Includes JTAG emulator cable		N/A	N/A
TMDS00510WS	XDS510WS box	SPARC	OpenWindows
Includes JTAG emulator cable		N/A	N/A
TMDS3080002	JTAG emulator cable	N/A	N/A
TMDX32400L0	Emulator porting kit	PC/SPARC	N/A
TMDX3260051	EVM	PC (ISA bus)	Win, DOS
Includes debugger			

- Current as of December 1997. Up-to-date version number, release date, and host/OS information is available on our web pages.
- SPARC software can run under SunOS 4.1.3 or higher or Solaris 2.x with the binary compatibility package
- OpenWindows = OpenWindows 3.x
- Win = Win16 = MS-Windows 3.x
- DOS = MS-DOS
- DOS Ext = DOS/4GW DOS Extender
- N/A = Not applicable
- License must be signed in order to purchase the Emulator Porting Kit

TMS320C3x Development Tools

Part Number	Product Description	Host	OS
TMS320C3x Tool Set Code Development Tools			
TMDS3243850-02	Assembler/Linker	PC	OS/2, DOS Ext
TMDS3243855-02	C Compiler/Assembler/Linker	PC	OS/2, DOS Ext
TMDS3243555-08	C Compiler/Assembler/Linker	SPARC	SunOS
Debug Tools			
TMDS3243851-02	Simulator	PC	Win, DOS
TMDS3243551-09	Simulator	SPARC	OpenWindows
TMDS3240130	XDS510 debugger	PC	Win, DOS
TMDS3240630	XDS510WS debugger	SPARC	OpenWindows
TMDS00510M	XDS510 board Includes MPSD emulator cable	PC (ISA bus)	N/A
TMDS00510WSM	XDS510WS box Includes MPSD emulator cable	SPARC	OpenWindows
TMDS3080004	MPSD emulator cable	N/A	N/A
TMDX3240030	Emulator porting kit	PC/SPARC	N/A
TMDS3260030	'C30 EVM Includes debugger	PC (ISA bus)	Win, DOS
TMDS3200031	'C31 DSK Includes software	PC (parallel port)	DOS

- Current as of April 1996. Up-to-date version number, release date, and host/OS information is available on our web pages.
- SPARC software can run under SunOS 4.1.3 or higher or Solaris 2.x with the binary compatibility package
- OpenWindows = OpenWindows 3.x
- Win = Win16 = MS-Windows 3.x
- DOS = MS-DOS
- DOS Ext = DOS/4GW DOS Extender
- N/A = Not applicable
- License must be signed in order to purchase the Emulator Porting Kit

TMS320C4x Development Tools

Part Number	Product Description	Host	OS
TMS320C4x Tool Set Code Development Tools			
TMDS3243850-02	Assembler/Linker	PC	OS/2, DOS Ext
TMDS3243855-02	C Compiler/Assembler/Linker	PC	OS/2, DOS Ext
TMDS3243555-08	C Compiler/Assembler/Linker	SPARC	SunOS
Debug Tools			
TMDS3244851-02	Simulator	PC	Win, DOS
TMDS3244551-09	Simulator	SPARC	OpenWindows
TMDS3240140	XDS510 debugger	PC	OS/2, Win, DOS
TMDS3240640	XDS510WS debugger	SPARC	OpenWindows
TMDS00510	XDS510 board	PC (ISA bus)	N/A
	Includes JTAG emulator cable	N/A	N/A
TMDS00510WS	XDS510WS box	SPARC	OpenWindows
	Includes JTAG emulator cable	N/A	N/A
TMDX3261040	PPDS board	N/A	N/A
TMDS3080002	JTAG emulator cable	N/A	N/A
TMDX3240040	Emulator porting kit	PC/SPARC	N/A

- Current as of December 1997. Up-to-date version number, release date, and host/OS information is available on our web pages.
- SPARC software can run under SunOS 4.1.3 or higher or Solaris 2.x with the binary compatibility package
- OpenWindows = OpenWindows 3.x
- Win = Win16 = MS-Windows 3.x
- DOS = MS-DOS
- DOS Ext = DOS/4GW DOS Extender
- N/A = Not applicable
- License must be signed in order to purchase the Emulator porting kit

TMS320C6x Development Tools

Part Number	Product Description	Host	OS
TMS320C6x Tool Set Code Development Tools			
TMDX3246555-07	C compiler/assembler/linker	PC	Win32
TMDX3246855-07	C compiler/assembler/linker	SPARC	SunOS 4.1x Solaris 2.x
Debug Tools			
TMDX3246851-07	Simulator	PC	Win32
TMDX3246551-07	Simulator	SPARC	SunOS 4.1x Solaris 2.x
TMDX324016X-07	C source debug S/W	PC	Win32
TMDX324066X-07	C source debug S/W	SPARC	SunOS 4.1x Solaris 2.x
TMDX326106201	Test & evaluation board	Stand alone unit	HPUX 10.2

- Up-to-date version number, release date, and host/OS information is available on our web pages.
- X window system or Open Windows required with SunOS and Solaris for the simulator software.
- Win32 = Windows NT and Windows 95

TMS320C8x Development Tools

Part Number	Product Description	Host	OS
TMS320C8x Tool Set Code Development Tools			
TMDX324855-67	Software toolkit C compiler/assembler/linker and simulator	SPARC	SunOS
TMDX324885-07	Software toolkit C compiler/assembler/linker and simulator	PC	Windows NT/95
Debug Tools			
TMDX3240680	XDS510WS Debugger	SPARC	SunOS
TMDX3240180	XDS510 Debugger	PC	Windows NT/95
TMDS00510	XDS510 Board Includes JTAG Emulator Cable	PC (ISA bus)	N/A
TMDS00510WS	XDS510WS Box Includes JTAG Emulator Cable	SPARC	OpenWindows
TMDS3080002	JTAG Emulator Cable	N/A	N/A
TMDX3240080	Emulator Porting Kit	SPARC/PC	N/A

- Current as of December 1997. Up-to-date version number, release date, and host/OS information is available on our web pages.
- SPARC software can run under SunOS 4.1.3 or higher or Solaris 2.x with the binary compatibility package
- OpenWindows = OpenWindows 3.x
- DOS = MS-DOS
- N/A = Not applicable
- License must be signed in order to purchase the Emulator porting kit

Further TMS320 Application Development Support

A wide variety of technical support for the TMS320 family is available throughout the design cycle.

DSP World Wide Web Site. TI DSP maintains a site on the World Wide Web at <http://www.ti.com/dsps> where users can find technical information about TI digital signal processing solutions. The data presented covers TI DSPs, linear and mixed-signal devices, development tools, and products of TMS320 third-party developers, including both hardware and software. Also available are technical resources including the On-Line DSP Lab™ and the 320 Hotline On-Line™. The On-Line DSP Lab allows TMS320 users to “test drive” DSP design tools for free, right from their PC. Currently, the lab features the 'C3x software tools and evaluation module (EVM) with debugger. The 320 Hotline On-Line is a searchable database that allows engineers to research various topics and retrieve technical answers 24 hours a day.

DSP Hotline. TI also maintains a DSP Hotline to answer specific TMS320 technical questions. Questions regarding device problems, development tools, documentation, upgrades, and new products are answered. Information and questions can also be submitted via electronic mail at the Hotline Internet address, dsph@ti.com, or via fax at (281) 274-2324.

DSP Bulletin Board Service (BBS). The TMS320 DSP bulletin board service (BBS) provides access to information about the TMS320 family. The BBS is an excellent means of communicating specification upgrades for current or new DSPs and application reports as they become available. It contains TMS320 source code from more than 2000 pages of application reports. These programs include macro definitions, FFT algorithms, filter programs, ADPCM algorithms, echo cancellation, graphic control, companding routines, and sine-wave generators, among others. The BBS can be accessed with a terminal or PC and a modem at (281) 274-2323. The files on the BBS are mirrored at an anonymous FTP site on the Internet at <ftp.ti.com>. The directory is `/mirrors/tms320bbs`.

Third-Party Support. There are over 250 third-party developers that support TMS320 digital signal processing solutions. Support products (both hardware and software) include cross-assemblers, simulators, development systems, application algorithms, logic analyzers, emulators, and much more. Consultants offer expertise in fields such as speech encoding, vector quantization, software/hardware design, and system analysis. For more information about the network of developers supporting TMS320 DSPs, see the *TMS320 Third-Party Support Reference Guide* (SPRU052) and *TMS320 Software Cooperative Resource Guide* (SPRT111), both in print and on the TI home page on the WWW.

Further TMS320 Application Development Support Resources

TI Home Page on the World Wide Web; <http://www.ti.com/dsps>

- Product information, announcements
- On-Line DSP Lab
- 320 Hotline On-Line
- On-line literature:
 - * User's guides, Application reports, Designer's notebook pages
 - * Data Sheets, *Third-Party Reference Guide*, *Software Cooperative Resource Guide*
 - * *Details on Signal Processing* Newsletter

TMS320 Bulletin Board Service: (281) 274-2323

- Application software, question/answer area
- Files are mirrored for anonymous FTP at <ftp.ti.com> in `/mirrors/tms320bbs`

TMS320 Hotline: (281) 274-2320

- On-line technical support from 8:30 am to 5:00 pm CST
- Fax questions to (281) 274-2324; e-mail: dsph@ti.com

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