

BiCMOS Bus Interface Logic

Data Book

General Information

BiCMOS Circuits

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Information contained in this databook supersedes all data for this technology published by TI in the United States of America before July 1989.

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Printed in U.S.A.

Revised July 1989

INTRODUCTION

The new BiCMOS bus interface family from Texas Instruments can reduce system power consumption by up to 25% while maintaining enhanced speed and output drive. This family's combination of bipolar and CMOS technologies permits high-speed switching and drive currents of 24- or 64 mA for commercial applications and 20 or 48 mA for military applications, which are necessary for the high-capacitive loads and backplanes found in today's systems:

The BiCMOS family of bus interface products is designated SN54/74BCT, which includes latches, buffers, drivers, and transceivers to provide pin-for-pin compatibility for easy upgrades.

Features and benefits include:

- Advanced bipolar performance—supports 25- to 30-MHz cycle times
- Ability to drive high-capacitive loads:
 - 24- or 64-mA output drive current (commercial)
 - 20- or 48-mA output drive current (military)
- Low power consumption—approximately 95% power savings over bipolar devices
- Pin-for-pin compatibility with industry-standard functions

This book provides pertinent technical information on available BCT devices. Additionally, the General Information Section contains an alphanumerical index, functional index, and other useful information.

For more information on Texas Instruments BiCMOS bus interface products, please contact your local TI field sales office or authorized distributor, or call Texas Instruments at 1-800-232-3200.



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	SN54BCT2411	SN74BCT2411	†			

[†] For more information on these devices, contact the factory.



LINE DRIVERS AND BUS TRANSCEIVERS

BUFFERS AND DRIVERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	NUMBER OF BITS	DEVICE TYPE	AVAILABLE
Noninverting	8	'757	A
Buffers, Drivers		'760	•
Inverting Buffers, Drivers	8	'756	A

25- Ω DRIVERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	NUMBER OF BITS	DEVICE TYPE	AVAILABLE
Noninverting Buffers, Drivers	8	'25757 '25760	A
Inverting Buffers, Drivers	8	'25756	A

BUFFERS AND DRIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	NUMBER OF BITS	DEVICE TYPE	AVAILABLE
Quad Buffers/ Drivers with	4	'125	•
Independent Output Controls		'126	•
Noninverting Buffers/Drivers	8	'241	•
W/Symmetrical	Ŭ	'244	•
G Inputs		'541	•
Inverting	8	'240	•
Buffers/Drivers	,	'540	•
Noninverting	10	'2827A	•
Buffers/Drivers		'29827A	•
Inverting	10	'2828A	•
Buffers/Drivers		'29828A	•

25- Ω LINE DRIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	NUMBER OF BITS	TYPE OF LOGIC	DEVICE TYPE	AVAILABLE
Buffers/Drivers		True	'25241	A
W/Symmetrical G Inputs	8	True	'25244	A
Buffers/Drivers	8	Inverting	'25240	A

SPECIAL BUFFERS/DRIVERS

DESCRIPTION	NUMBER OF BITS	TYPE OF LOGIC	DEVICE TYPE	AVAILABLE
Buffers/Drivers with Parity	8	Inverting	'455	A
Checker/ Generator		True	'456	A

BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

		=1/0=	DE1/10E	
DESCRIPTION	NUMBER OF BITS	OF LOGIC	DEVICE TYPE	AVAILABLE
		True	'245	•
Transceivers	8	Inverting	'620A	•
		True	'623	•
		Inverting	'640	•
		True	'543	•
		Inverting	'544	A
Bus Transceivers	8	True	'646	•
with Registers		Inverting	'648	A
		Inverting	'651	A
		True	'652	•
Bus		True	'29833	•
Transceivers	8 to 9	Inverting	'29834	•
with Parity Checker/		True	'29853	•
Generator		Inverting	'29854	•
	9	True	'29863A	•
Transceivers	-	Inverting	'29864A	•
	10	True	'29861A	•
		Inverting	'29862A	•
			'956	A
Latch	8		'957	A
Transceivers			'958	A
			'959	A

BUFFERS AND LINE DRIVERS/MOS MEMORY DRIVERS

DESCRIPTION	NUMBER OF BITS	DEVICE TYPE	AVAILABLE
		'2240	•
Bus Drivers (Series Resistors)	8	'2241	•
(Genes resistors)		'2244	•
Buffers	11	'2410	A
(Series Resistors)		'2411	A

- Denotes available product.
- ▲ Denotes planned new products. For product availability on these devices, contact the factory.



LINE DRIVERS AND BUS TRANSCEIVERS (Continued)

25- Ω BUS TRANSCEIVERS

DESCRIPTION	NUMBER OF BITS	TYPE OF LOGIC	PORT CONFIGURATION	DEVICE TYPE	AVAILABLE
Bus Transceivers	. 8	True	3-State; A = 25 Ω Line Drive	'25245	A
		Inverting	3-State; A = 25 Ω Line Drive	'25620	A
Bus Transceivers 8	8	True	$B = 3$ -State; $A = 25 \Omega$ Drive, Open-Collector	'25621	A
	Inverting	Inverting	$B = 3$ -State; $A = 25 \Omega$ Drive, Open-Collector	'25622	A
		3-State; A = 25 Ω Line Drive	'25623	A	
		Inverting	3-State; $A = 25 \Omega$ Line Drive	'25640	A
Bus Transceivers	8	True	$B=3$ -State; $A=25~\Omega$ Line Drive, Open-Collector	'25641	A
		Inverting	B = 3-State; A = 25 Ω Line Drive, Open-Collector	'25642	. 🛦

FLIP-FLOPS

FLIP-FLOPS WITH 3-STATE OUTPUTS

DESCRIPTION	NUMBER OF BITS	TYPE OF LOGIC	DEVICE TYPE	AVAILABLE
		True	'374	•
D-Type,	8	Inverting	'534	•
Edge-Triggered		Inverting	'564	A
		True	'574	A
D.T		True	'29821	•
D-Type	10	Inverting	'29822	A

LATCHES AND REGISTERS

LATCHES WITH 3-STATE OUTPUTS

DESCRIPTION	NUMBER OF BITS	TYPE OF LOGIC	DEVICE TYPE	AVAILABLE
Transparent	8	True	'373	A
rransparent	0	riue	'573	A
Transparent	8	Invorting	'533	A
Transparent	•	Inverting	'564	A
	10	True	'29841	A
		Inverting	'29842	•
Transparent	0	True	'29843	•
Transparent	9	Inverting	'29844	•
	8	True	'29845	•
	8	Inverting	'29846	•

REGISTERS

SHIFT REGISTERS

DESCRIPTION	NUMBER	MODES				DEVICE	AVAILABLE	
DESCRIPTION	OF BITS	S-	S	L	Н	TYPE	AVAILABLE	
Parallel-In Parallel-Out	8	Х	x	х	х	'299	A	
Bi-Directional		Х	Х	Х	х	'323	A	

NOTE: Modes; S-=S-R, S=S-L, L=Load, H=Hold

SIGN-PROTECTED REGISTERS

DESCRIPTION	NUMBER	MODES				DEVICE	AVAILABLE	
DESCRIPTION	OF BITS	S-	S	L	Н	TYPE	AVAILABLE	
Sign-Protected Registers	8	х		х	х	'322	A	

OTHER REGISTERS

DESCRIPTION	NUMBER OF BITS	DEVICE TYPE	AVAILABLE
Pipeline Register		'819	A -/
Diagnostic/ Pipeline Register	8	'29818	A
	9	'29823	•
Danistana	9	'29824	A
Registers	8	'29825	A
		'29826	A

- Denotes available product.
- ▲ Denotes planned new products. For product availability on these devices, contact the factory.



INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

Ci Input capacitance

The internal capacitance at an input of the device.

Co **Output capacitance**

The internal capacitance at an output of the device.

C_{pd} Power dissipation capacitance

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $PD = C_{pd} VCC^2 f + ICC VCC$

fmax Maximum clock frequency

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

ICC Supply current

The current into* the V_{CC} supply terminal of an integrated circuit.

ΙН High-level input current

The current into* an input when a high-level voltage is applied to that input.

lu Low-level input current

The current into* an input when a low-level voltage is applied to that input.

High-level output current IOH

The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

Low-level output current loi

The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

IOZ Off-state (high-impedance-state) output current (of a three-state output)

The current flowing into* an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output.

ta Access time

The time interval between the application of a specified input pulse and the availability of valid signals at an output.

^{*}Current out of a terminal is given as a negative value.



tdis Disable time (of a three-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ} . Open-collector outputs will change only if they are low at the time of disabling so $t_{dis} = t_{PLH}$.

ten Enable time (of a three-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: In the case of memories, this is the access time from an enable input (e.g., \overline{G}). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL} . Open-collector outputs will change only if they are responding to data that would cause the output to go low so, for them, $t_{en} = t_{PHL}$.

th Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

- NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
 - 2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

tod Propagation delay time

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ($t_{pd} = t_{PHL}$ or t_{PLH}).

tphi Propagation delay time, high-to-low level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

tpHZ Disable time (of a three-state output) from high level

The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

tpl H Propagation delay time, low-to-high-level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

tp17 Disable time (of a three-state output) from low level

The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

tpzH Enable time (of a three-state output) to high level

The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.



tpzL Enable time (of a three-state output) to low level)

The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

tsu Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

- NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
 - 2. The setup time may have a negative value in which the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

Pulse duration (width) tw

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

High-level input voltage ٧щ

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

VIL Low-level input voltage

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

VOH High-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

VOL Low-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.



The following symbols are used in function tables on TI data sheets:

H = high level (steady state)

L = low level (steady state)

transition from low to high level

= transition from high to low level

→ = value/level or resulting value/level is routed to indicated destination

= value/level is re-entered

X = irrelevant (any input, including transitions)

Z = off (high-impedance) state of a 3-state-output

a..h = the level of steady-state inputs at inputs A through H respectively

Q₀ = level of Q before the indicated steady-state input conditions were established

 $\overline{\mathbb{Q}}_0$ = complement of \mathbb{Q}_0 or level of $\overline{\mathbb{Q}}$ before the indicated steady-state input conditions were

established

 Q_n = level of Q before the most recent active transition indicated by \downarrow or \uparrow

= one low-level pulse

TOGGLE = each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with \uparrow and/or \downarrow , this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q₀, or \overline{Q}_0), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, \int or \int , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

		TAE	

	INPUTS								OUT	PUTS			
CLEAR	МО	MODE CLOCK SERIAL PARALLEL		PARALLEL			QA	QB	QC	QD			
OLLA!!	S1	S0	OLOGIK	LEFT	RIGHT	Α	В	С	D	ΨД	чв	ur)	ч _D
L	x	X	х	×	Х	х	х	Х	х	L	L	L	L
н	X	Χ	L	X	X	х	Х	Х	Χ	Q _{A0}	Q_{B0}	Q _{C0}	Q_{D0}
н	Н	Н	1	X	X	а	b	С	d	а	b	С	d
Н	L	Н	1 ↑	X	Н	Х	X	Х	X	н	Q_{An}	Q_{Bn}	Q_{Cn}
н	L	Н	1	X	L	X	X	Х	Х	L	Q_{An}	Q_{Bn}	QCn
н	Н	L	1	н	X	X	X	X	X	QBn	Q_{Cn}	Q_{Dn}	Н
Н	Н	L	↑	L	X	X	Х	Х	Х	QBn	Q_{Cn}	Q_{Dn}	L
Н	L	L	х	X	X	X	Х	Χ	Χ	Q _{A0}	Q _{B0}	Q _{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output QA, data entered at B will be at QB, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at QA is now at QB, the previous levels of QB and QC are now at QC and QD respectively, and the data previously at QD is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is not at Q_A , the previous levels of Q_C and Q_D are now at Q_B and Q_C , respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

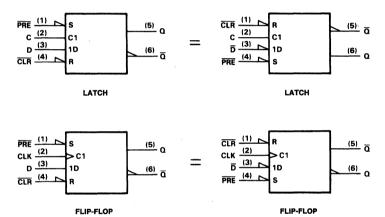
The truth table functional tests do not reflect all possible combinations or sequential modes.

D flip-flop and latch signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called \overline{Q} and those producing complementary data are called $\overline{\overline{Q}}$. An input that causes a \overline{Q} output to go high or a $\overline{\overline{Q}}$ output to go low is called Preset (PRE). An input that causes a $\overline{\overline{Q}}$ output to go high or a \overline{Q} output to go low is called Clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active-low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits \overline{D} and Q.

In some applications, it may be advantageous to redesignate the data input from D to \overline{D} or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown in parenthesis.



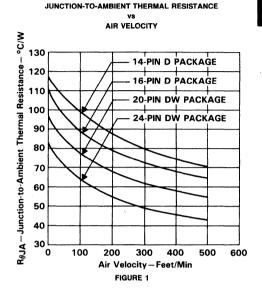
The figures show that when Q and \overline{Q} exchange names, the Preset and Clear pins also exchange names. The polarity indicators \triangleright on \overline{PRE} and \overline{CLR} remain, as these inputs are still active-low, but the presence or absence of the polarity indicator changes at D (or \overline{D}), Q, and \overline{Q} . Pin 5 (Q or \overline{Q}) is still in phase with the data input (D or \overline{D}); their active levels change together.

In digital system design, consideration must be given to thermal management of components. The small size of the "small outline" package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the BiCMOS family. In general, the junction temperature for any device can be calculated using Equation 1.

Typical junction temperature can be calculated using Equation 1 directly with typical values of I_{CC} taken from the data sheets and $V_{CC}=5$ volts. To calculate maximum junction temperature, it is necessary to take into account the spread of I_{CC} values for a population.

Maximum junction temperature for all 54BCT parts can be calculated using Equation 1 with I_{CC} being the maximum value specified on the data sheet and $V_{CC}=5.5$ volts. In fact, I_{CC} for Series 54 devices at the temperature extremes of -55° C to 125° C will be higher than for a Series 74 device at the temperature extremes of 0° C to 70° C. This is reflected in the limits specified for 74BCT devices, which are less than those specified for 54BCT devices. The BCT family



data sheets give a single maximum value for ICC. If that value is used to calculate maximum junction temperature for series 74 devices, an unrealistically high value will result. Instead, Equation 2 can be used. This uses the factor 1.31 to scale the typical value of ICC up to a practical maximum value for process variations and thermal effects.

$$T_{J} = R_{\theta JA} (V_{CC} \bullet I_{CC} + N \bullet I_{OL} \bullet V_{OL}) + T_{A}$$
(1)

where

T_{.1} = virtual junction temperature

 $R_{\theta,IA}$ = thermal resistance, junction to ambient air

VCC = supply voltage (5 V for typical, 5.5 V for maximum)

ICC = supply current

N = the number of outputs

IOL = the low-level output current

VOL = the low-level output voltage

TA = the ambient air temperature

$$TJ_{max} = R_{\theta JA} (5.5 \bullet 1.31 \bullet I_{CCtyp} + N \bullet I_{OL} \bullet V_{OL}) + T_{A}$$
 (2)





General Information

BiCMOS Circuits

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Mechanical Data

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BiCMOS Circuits Released Products





SN54BCT125, SN54BCT126 SN74BCT125, SN74BCT126

QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS D3133. SEPTEMBER 1988 REVISED MAY 1989

- State of the Art BiCMOS Design Significantly Reduces ICCZ
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015
- Package Options Include Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These bus buffers feature independent line drivers with three-state outputs. Each 'BCT125 output is disabled when the associated \overline{G} is high, and each 'BCT126 output is disabled when the associated G is low.

The SN54BCT125 and SN54BCT126 are characterized for operation over the full military temperature range of -55° C to 125 $^{\circ}$ C. The SN74BCT125 and SN74BCT126 are characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.

FUNCTION TABLES

'BCT125

(=::-:-;					
INP	UTS	OUTPUT			
G	A	Υ			
L	Н	н			
L	L	L			
Н	Х	Z			

'BCT126 (EACH BUFFER)

(EACH BUFFER)							
INP	UTS	OUTPUT					
G	Α	Y					
Н	Н	н					
Н	L	L					
L	Х	Z					

H = high level, L = low level, X = irrelevant

logic symbols‡

	'Β	CT125	5	
1G (1)	EN	D	∇	(3) 1Y
2G (4) 2A (5)				(6) 2Y
1G (1) (2) (2) (3) (4) (4) (5) (7) (7) (7) (7) (7) (7) (7) (7) (7) (7				(8) 3Y
4G (13) 4A (12)				(11) 4Y

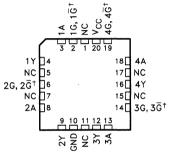
³A (9) 3A (72)

SN54BCT125, SN54BCT126 ... J PACKAGE SN74BCT125, SN74BCT126 ... N PACKAGE (TOP VIEW)

1G, 1G [†] □	∪14 V _{CC}
1 A 🔲 2	13 4G, 4G†
1 Y 🗖 3	12 🗍 4A
2G, 2Ḡ [†] □ 4	11 🛚 4Y
2A 🗌 5	10 🔲 3G, 3І
2Y 🛮 6	9 🗌 3A
GND 🗆 7	8 3Y

† G on 'BCT125; G on 'BCT126

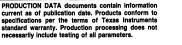
SN54BCT125, SN54BCT126 ... FK PACKAGE (TOP VIEW)



† G on 'BCT125; G on 'BCT126 NC—No internal connection

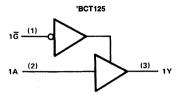
	'E	3CT126	6	
1G (1)	EN	\triangleright	∇	(3) 1Y
1A (2) 2G (4) 2A (5)	}			(6) 2Y
3G (10)	├			(8) 3Y
3A (3)	├-			(11)
4G (12)	<u> </u>			44

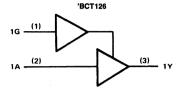
[‡] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for J and N packages.

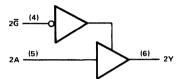


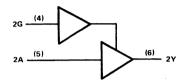


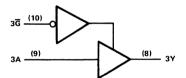
logic diagrams (positive logic)

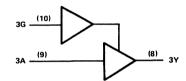


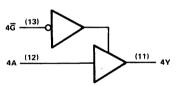


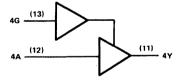












Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, VCC	0.5 V to 7 V
Input voltage (see Note 1)	
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to V _C C
Current into any output in the low state: SN54BCT125, SN54BCT126	96 mA
SN74BCT125, SN74BCT126	128 mA
Operating free-air temperature range: SN54BCT125, SN54BCT126	-55°C to 125°C
SN74BCT125, SN74BCT126	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.



SN54BCT125, SN54BCT126 SN74BCT125, SN74BCT126 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

recommended operating conditions

			SN54BCT125 SN54BCT126			SN74BCT125 SN74BCT126		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIН	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.8			0.8	٧
lк	Input clamp current	:		-18			-18	mA
ЮН	High-level output current			-12			-15	mA
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		SI	N54BCT12	:5	12	174BCT12	5	UNIT		
r Allame I Ell	'	FEST CONDITIONS	MIN	TYP	MAX	MIN	TYP†	MAX	0	
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V	
		IOH = -3 mA	2.4	3.3		2.4	3.3			
Voн	V _{CC} = 4.5 V	I _{OH} = -12 mA	2	3.2					٧	
		IOH = -15 mA				2	3.1			
VOL	V _{CC} = 4.5 V	IOL = 48 mA		0.38	0.55				V	
*OL	1.00	IOL = 64 mA					0.42	0.55	·	
11	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1			0.1	mA	
lН	$V_{CC} = 5.5 V,$	V _I = 2.7 V			35			25	μΑ	
ΊL	$V_{CC} = 5.5 V,$	V _I = 0.5 V			-20			-20	μΑ	
IOZH	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			50			50	μΑ	
IOZL	$V_{CC} = 5.5 V,$	$V_{O} = 0.5 V$			-50			-50	μΑ	
los‡	$V_{CC} = 5.5 V,$	V _O = 0	-100		- 225	-100		225	mA	
Іссн				19	- 31		19	31		
ICCL	$V_{CC} = 5.5 V,$	Outputs open		46	49		46	49	mA	
ICCZ				6	12		6	12		
Ci	$V_{CC} = 5 V$,	V _I = 2.5 V or 0.5 V		4			4		рF	
Co	V _{CC} = 5 V,	V _O = 2.5 V or 0.5 V		9			9		<u>.</u>	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.



^{*} Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		SI	154BCT12	:6	SN	174BCT12	6	UNIT		
I AIIAMETEIT		TEST CONDITIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	Oldi I	
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V	
		IOH = −3 mA	2.4	3.3		2.4	3.3			
VoH	$V_{CC} = 4.5 V$	$I_{OH} = -12 \text{ mA}$	2	3.2					٧	
		IOH = -15 mA				2	3.1		l	
VOL	V _{CC} = 4.5 V	IOL = 48 mA		0.38	0.55				v	
.05	100	IOL = 64 mA					0.42	0.55	•	
Ц	$V_{CC} = 0 V$	V _I = 7 V			0.1			0.1	mA	
۱н	$V_{CC} = 5.5 V,$	V _I = 2.7 V			35			25	μΑ	
liL.	$V_{CC} = 5.5 V,$	V _I = 0.5 V			-20			-20	μΑ	
lozh	$V_{CC} = 5.5 V,$	V _O = 2.7 V			50			50	μΑ	
lozL	$V_{CC} = 5.5 V,$	V _O = 0.5 V			-50			-50	μΑ	
los‡	$V_{CC} = 5.5 V,$	V _O = 0	-100		-225	. —100		-225	mA	
ICCH				21	33		21	33		
ICCL	$V_{CC} = 5.5 V,$	Outputs open		35	51		35	51	mA	
ICCZ				5	8		5	8		
Ci	$V_{CC} = 5 V$	V _I = 2.5 V or 0.5 V		4			4		pF	
Co	$V_{CC} = 5 V$,	V _O = 2.5 V or 0.5 V		9			9		ρ.	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN54BCT125, SN54BCT126 SN74BCT125, SN74BCT126 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

'BCT125 switching characteristics (see Figure 1)

PARAMETER	EDOM TO		C _L R1 R2	$V_{CC} = 5 V$, $C_{L} = 50 pF$, R1 = 500 Ω, R2 = 500 Ω, $T_{A} = 25^{\circ}C$		V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX [†]					
			'BCT125		ì	SN54BCT125		SN74BCT125		_]	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
tPLH	Α	Y	1.6	3.5	5.2	1.6	6	1.6	5.7	ns	
tPHL	_ ^	,	2.7	5	6.9	2.7	8	2.7	7.7	110	
tPZH	G	Y	3.4	6.7	9	3.4	11.1	3.4	10.3	ns	
tPZL		•	5	8.2	10.4	5	12.8	5	11.7		
tpHZ	G	Y	3	5.8	7.4	3	9.4	3	8.9	ns	
tPLZ	_	,	2.8	5.5	7.3	2.8	9.9	2.8	8.6		

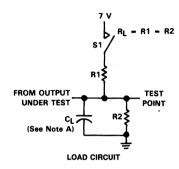
'BCT126 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2	CC = 5 V = 50 pF = 500 Ω = 500 Ω A = 25°C	=, 1, 1,		V _{CC} = 4.5 C _L = 9 R1 = 9 R2 = 9 T _A = MIN	50 pF, 500 Ω, 500 Ω,		UNIT
			'BCT126			SN54	BCT126	SN74BCT126		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	Α	v	1.5	3.6	4.9	1.5	5.6	1.5	5.4	ns
tPHL	l	·	2.7	5.3	6.9	2.7	7.7	2.7	7.4	
tPZH	G	Y	2.6	4.8	6.4	2.6	7.2	2.6	7	ns
tPZL]		3.7	6.4	8.3	3.7	10.5	3.7	10	
tPHZ	G	Y	3.2	6.6	8.2	3.2	9.6	3.2	9.1	ns
tPLZ			3.4	6.5	8	3.4	12.3	3.4	10.7	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

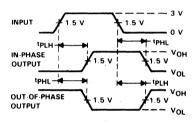


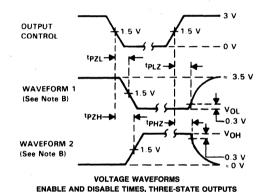
PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
t _{PHZ}	Open
tPLZ	Closed

SWITCH POSITION TABLE





VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES NOTES: A. C. includes probe and iig capacitance.

- B. Input pulses are supplied by generators having the following characteristics: PRR \geq 10 MHz, $Z_0 = 50 \Omega$, $t_f = 2.5$ ns, $t_f = 2.5$ ns,
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

SN54BCT240, SN74BCT240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D3057, OCTOBER 1987-REVISED OCTOBER 1988

- State of the Art BiCMOS Design Significantly Reduces ICCZ
- Comparable Speed and Improved Power Performance Relative to 54F/74F240
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C. Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT241 and 'BCT244, these devices provide a choice of selected combinations of inverting and non-inverting outputs, symmetrical \overline{G} (active-low output control) inputs, and complementary G and \overline{G} inputs. These devices feature high fan-out and improved fan-in.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

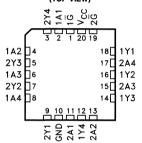
FUNCTION TABLE (EACH BUFFER)

INP	UTS	OUTPUT
Ğ	A	Y
L	н	L
L	L	н
Н	Х	Z

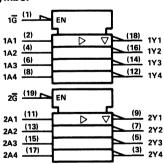
SN54BCT240 ... J PACKAGE SN74BCT240 ... DW OR N PACKAGE (TOP VIEW)

1 G 🔲 1	U20 V _{CC}
1A1 2	19 2 Š
2Y4 🛚 3	18 1Y1
1A2 🛮 4	17 2A4
2Y3 🛮 5	16 1Y2
1 A 3 🔲 6	15 2A3
2Y2 🔲 7	14 🗍 1Y3
1A4 🗌 8	13 2A2
2Y1 🛮 9	12 1Y4
GND 10	11 2A1

SN54BCT240 ... FK PACKAGE (TOP VIEW)



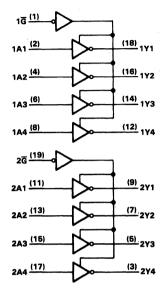
logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, VCC	. $-0.5 V$ to $7 V$
Input voltage (see Note 1)	. -0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to VCC
Input clamp current	30 mA
Current into any output in the low state: SN54BCT240	96 mA
SN74BCT240	128 mA
Operating free-air temperature range: SN54BCT240	-55°C to 125°C
SN74BCT240	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	,	SN	SN54BCT240			SN74BCT240			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4:5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.8			0.8	V	
lκ	Input clamp current			-18			-18	mA	
ЮН	High-level output current			-12			15	mA	
lOL :	Low-level output current			48			64	mA	
TA	Operating free-air temperature	-55	***************************************	125	0		70	°C	



NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

SN54BCT240, SN74BCT240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		SI	154BCT24	0	SI	174BCT24	0	UNIT	
· AIIAME I EN		TEST CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP	MAX	0
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	٧
		IOH = -3 mA	2.4	3.3		2.4	3.3		
Voн	$V_{CC} = 4.5 V$	I _{OH} = -12 mA	2	3.2					V
		I _{OH} = -15 mA				2	3.1		
VOL	V _{CC} = 4.5 V	I _{OL} = 48 mA		0.38	0.55				V
·OL	100	IOL = 64 mA					0.42	0.55	
Ŋ.	$V_{CC} = 5.5 V$	V _I = 5.5 V			0.1			0.1	mA
ΉΗ	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
¹IL	$V_{CC} = 5.5 V$,	V _I = 0.5 V			-1			-1	mA
lozh	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			50			50	μΑ
lozl	$V_{CC} = 5.5 V,$	$V_0 = 0.5 V$			-50			-50	μΑ
los‡	$V_{CC} = 5.5 V$	V _O = 0	-100		-225	-100		-225	mA
ГССН				19	31		19	31	
ICCL	$V_{CC} = 5.5 V,$	Outputs open		46	71		46	71	mA
Iccz				6	9		6	9	
Ci	$V_{CC} = 5 V$,	V _I = 2.5 V or 0.5 V		6			6		pF
Co	$V_{CC} = 5 V$,	$V_{O} = 2.5 \text{V or } 0.5 \text{V}$		11			11		pF

 $[\]overline{\dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

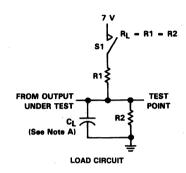
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2	CC = 5 V, = 50 pF = 500 Ω = 500 Ω A = 25°C	,		V _{CC} = 4.5 C _L = 9 R1 = 9 R2 = 9 T _A = MIN	50 pF, 500 Ω, 500 Ω,		UNIT
			'BCT240		SN54BCT240		SN74BCT240			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	Α	Y	0.5	3.3	4.8	0.5	6.4	0.5	5.6	ns
tPHL	^	i i	0.4	1.8	3.5	0.4	4.5	0.4	4	
^t PZH	G	Y	1	6.4	7.9	1	9.2	1	8.8	ns
tPZL]	· '	1	7.5	9.4	1	10.8	1	10.5	
tPHZ	G	Y	1	6	6.8	1	8.5	1	8.1	ns
tPLZ		·	1	6.7	8.1	1	10.6	1	9.5	



[‡] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

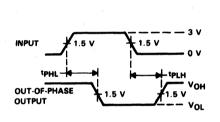


TEST \$1 tpLH Open tpHL Open tpZH Open tpZL Closed tpHZ Open

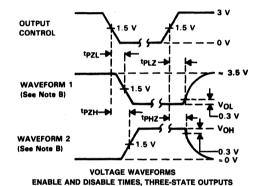
tPLZ

Closed

SWITCH POSITION TABLE



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



NOTES: A. CL includes probe and jig capacitance.

- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f = 2.5$ ns, $t_f = 2.5$ ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

SN54BCT241, SN74BCT241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D3057, OCTOBER 1987-REVISED OCTOBER 1988

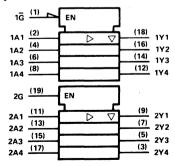
- State of the Art BiCMOS Design Significantly Reduces ICCZ
- Comparable Speed and Improved Power Performance Relative to '54F/74F241
- ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT240 and 'BCT244, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{\mathbb{G}}$ (active-low output control) inputs, and complementary \mathbb{G} and $\overline{\mathbb{G}}$ inputs.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

logic symbol[†]

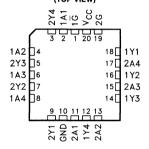


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54BCT241 ... J PACKAGE SN74BCT241 ... DW OR N PACKAGE (TOP VIEW)

•			
1 G [1	U 20] v _{cc}
1A1 [2	19] 2G
2Y4 🗌	3	18] 1Y1
1A2 🗌	4	17] 2A4
2Y3 🗌	5	16] 1Y2
1A3 🗌	6	15] 2A3
2Y2 🗌	7	14] 1Y3
1A4 🗌	8	13] 2A2
2Y1 🗌	9	12] 1Y4
GND 🗌	10	11] 2A1

SN54BCT241 ... FK PACKAGE (TOP VIEW)



FUNCTION TABLES

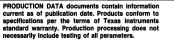
(EACH BUFFER IN FIRST SET)

INPUTS		OUTPUT
1G 1A		1Y
L	Н	н
L	L	L
н	Х	Z

(EACH BUFFER IN

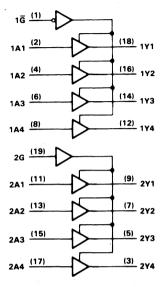
SECOND SET)					
INPUTS		OUTPUT			
2G	2A	2Y			
Н	Н	н			
Н	L	L			
L	Х	z			

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, VCC	. −0.5 V to 7 V
Input voltage (see Note 1)	. −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to V _{CC}
Input clamp current	−30 mA
Current into any output in the low state: SN54BCT241	96 mA
SN74BCT241	128 mA
Operating free-air temperature range: SN54BCT241	-55°C to 125°C
SN74BCT241	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54BCT241				SN74BCT241			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧	
VIH	High-level input voltage	2			2			٧	
VIL	Low-level input voltage			0.8			0.8	٧	
İΙΚ	Input clamp current			- 18			-18	mA	
ЮН	High-level output current			-12			-15	mA	
lOL	Low-level output current			48			64	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	



NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.

SN54BCT241, SN74BCT241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

ΡΔΙ	RAMETER	TES	ST CONDITIONS	SI	N54BCT24	11	SI	174BCT24	1	UNIT
			51 GONDITIONS	MIN	MIN TYP [†] MAX MIN TYP [†] M			MAX		
VIK		$V_{CC} = 4.5 V,$	lj = -18 mA			-1.2			-1.2	٧
			IOH = −3 mA	2.4	3.3		2.4	3.3		
Vон		$V_{CC} = 4.5 V$	IOH = -12 mA	2	3.2					٧
			IOH = -15 mA				2	3.1		
VOL		V _{CC} = 4.5 V	I _{OL} = 48 mA		0.38	0.55				V
·OL		100	IOL = 64 mA					0.42	0.55	•
lį		$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1			0.1	mA
ΊΗ		$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
IIL	1G or 2G	V _{CC} = 5.5 V, \	/ _I = 0.5 V			-1			-1	mA
'IL	Any A Input	V _{CC} = 5.5 V, \	/ _I = 0.5 V			-1.6			-1.6	1117 (
lozh		$V_{CC} = 5.5 V,$	V _O = 2.7 V			50			50	μΑ
lozL		$V_{CC} = 5.5 V,$	V _O = 0.5 V			-50			-50	μΑ
los‡		$V_{CC} = 5.5 V,$	V _O = 0	-100		-225	-100		-225	mA
ICCH		$V_{CC} = 5.5 V$	Outputs high		23	43		23	43	mA
ICCL		Outputs open	Outputs low		53	85		53	85	mA
Iccz		Caspata open	Outputs disabled		4	10		4	10	mA
Ci		$V_{CC} = 5 V, V_I$	= 2.5 V or 0.5 V		6			6		pF
Co		$V_{CC} = 5 V, V_{C}$) = 2.5 V or 0.5 V		: 11			11		pF

switching characteristics (see Figure 1)

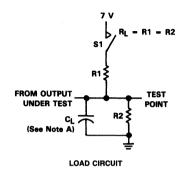
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_{A} = 25^{\circ}C$				V _{CC} = 4.5 C _L = 9 R1 = 9 R2 = 9 T _A = MIN	50 pF, 500 Ω, 500 Ω,		UNIT
			,	'BCT241		SN54	BCT241	SN74E	BCT241	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	Α	Y	0.5	2.5	4.5	0.5	5.2	0.5	4.9	ns
tPHL		·	1	3	5.4	1	6.3	1	5.9	
tPZH	G or G	Y	1	5.7	7.8	1	9.1	1	8.7	ns
tPZL	u 0. u	·	1	5.2	8.6	1	10	1	9.4	
tPHZ	G or \overline{G}	Y	1	5.8	6.8	1	8.4	1	8.1	ns
t _{PLZ}		·	1	7	8.1	1	11	1	9.9	

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



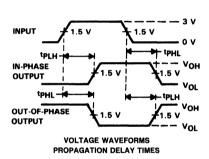
All typical values are at V_{CC} = 5 V, T_A = 25°C.

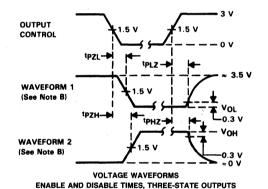
 Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



SWITCH POSITION TABLE

TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed





NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All Input pulses are supplied by the generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

SN54BCT244, SN74BCT244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D3057, OCTOBER 1987—REVISED OCTOBER 1988

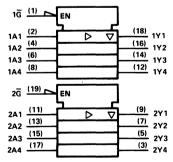
- 3-State Outputs Drive Bus Lines or Buffer **Memory Address Registers**
- P-N-P Inputs Reduce DC Loading
- State of the Art BiCMOS Design Significantly Reduces ICC7
- Comparable Speed and Improved Power Performance Relative to 54F/74F244
- ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015
- Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT240 and 'BCT241, these devices provide the choice of selected combinations of inverting outputs, symmetrical G (active-low output control) inputs, and complementary G and G inputs.

The SN54BCT244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT244 characterized for operation from 0°C to 70°C.

logic symbol†

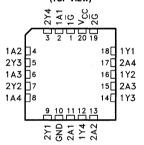


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54BCT244 ... J PACKAGE SN74BCT244 ... DW OR N PACKAGE (TOP VIEW)

1 G [1	U 20	□vcc
1A1 [2	19] 2Ğ
2Y4 [3	18	1Y1
1A2 [4	17	2A4
2Y3 [5	16	1Y2
1 A 3 [6	15	2A3
2Y2 [7	14	1Y3
1A4 [8	13	2A2
2Y1 [9	12	1Y4
GND [10	11] 2A1

SN54BCT244 ... JK PACKAGE (TOP VIEW)

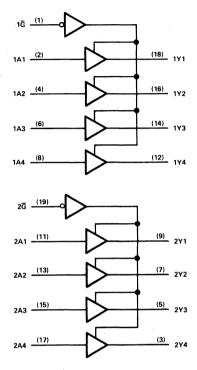


FUNCTION TABLE

OUTPUT					
1 G , 2 G	A	Y			
Н	х	z			
L	L	L			
L	н	Н			



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	
Voltage applied to any output in the disabled or power-off state	
Voltage applied to any output in the high state	-0.5 V to V _{CC}
Current into any output in the low state: SN54BCT244	96 mA
SN74BCT244	128 mA
Operating free-air temperature range: SN54BCT244	-55°C to 125°C
SN74BCT244	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN54BCT244, SN74BCT244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54BCT244			SI	SN74BCT244			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.8			0.8	٧	
ΊΚ	Input clamp current			-18			18	mA	
ЮН	High-level output current			-12			-15	mA	
lOL	Low-level output current			48			64	mA	
TA	Operating free-air temperature	-55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	S	SN54BCT244 SN74BCT244 MIN TYP [†] MAX MIN TYP [†] MAX					UNIT
170000000000000000000000000000000000000	1	1201 00110110110	MAX	MAX MIN TYP† MA					
VIK	$V_{CC} = 4.5 V$,	l₁ = −18 mA			-1.2			-1.2	٧
		IOH = -3 mA	2.4	3.3		2.4	3.3		
VOH	$V_{CC} = 4.5 V$	$I_{OH} = -12 \text{ mA}$	2	3.2					٧
		IOH = -15 mA				2	3.1		
VOL	V _{CC} = 4.5 V	IOL = 48 mA		0.38	0.55				V
1 .05	1.00	IOL = 64 mA					0.42	0.55	·
lį	$V_{CC} = 5.5 V$,	V _I = 5.5 V			0.1			0.1	mA
۱н	$V_{CC} = 5.5 V,$	$V_{ } = 2.7 V$			20			20	μΑ
IIL	$V_{CC} = 5.5 V,$	V _I = 0.5 V			-1			-1	mA
lozh	$V_{CC} = 5.5 V,$	V _O = 2.7 V			50			50	μΑ
lozl	$V_{CC} = 5.5 V,$	$V_0 = 0.5 V$			-50			-50	μΑ
los‡	$V_{CC} = 5.5 V,$	VO = 0	-100		-225	-100		-225	mA
ICCH		Outputs high		23	40		23	40	mA
ICCL	V _{CC} = 5.5 V	Outputs low		53	80		53	80	mA
ICCZ	1.00 0.0 1	Outputs disabled		4	10		4	10	mA

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

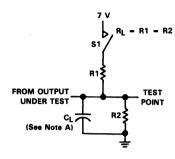
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2	C = 5 V, = 50 pF = 500 Ω = 500 Ω = 25°C	,		V _{CC} = 4.5 C _L = 5 R1 = 5 R2 = 6 T _A = MIN	50 pF, 500 Ω, 500 Ω,		UNIT
			. ,	'BCT244			IBCT244	SN74E	BCT244	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	А	Y	1.2	2.5	4.4	0.9	5.3	0.7	5	ns
tPHL]	·	1.7	3.2	5	1.4	6	1.4	5.5	
tPZH	G	Y	2	5.7	7.8	2	9	2	8.7	ns
tPZL		,	2	5.9	8.1	2	9.4	2	8.9	
t _{PHZ}	G	Υ	2	5.4	6.7	2	8	2	7.7	ns
tPLZ			2	6.1	7.6	. 2	9.8	2	8.9	

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



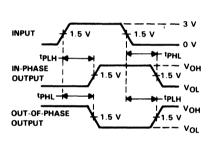
^{*} Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



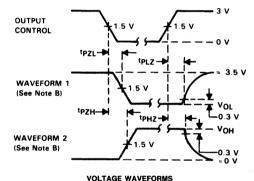
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
1231	31
tPLH	Open
tPHL	Open
^t PZH	Open
^t PZL	Closed
^t PHZ	Òpen
tPLZ	Closed



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All Input pulses are supplied by the generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS



SN54BCT245, SN74BCT245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3057, SEPTEMBER 1988—REVISED APRIL 1989

- **BiCMOS Design Substantially Reduces** Standby Current
- 3-State Outputs Drive Bus Lines Directly
- ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015
- Comparable Speed and Improved Power Performance Relative to SN54F245, SN74F245
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. Implementing the control function minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input (G) can disable the device so that the buses are effectively isolated.

The SN54BCT245 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT245 is characterized for operation from 0°C to 70°C.

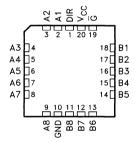
FUNCTION TABLE

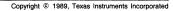
ENABLE G	CONTROL	OPERATION
L	L	B data to A bus
L	н	A data to B bus
Н	X	Isolation

SN54BCT245 ... J PACKAGE SN74BCT245 ... DW OR N PACKAGE (TOP VIEW)

DIR L	1	O 20	Ц	V_{CC}
A1 [2	19		Ğ
A2 [3	18		В1
A3 [4	17	П	В2
A4 [5	16	р	В3
A5 🗌	6	15		В4
A6 🗌	7	14		В5
A7 🗌	8	13		В6
A8 [9	12		В7
GND [10	11	р	B8

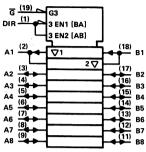
SN54BCT245 ... FK PACKAGE (TOP VIEW)







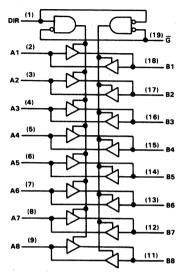
logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	−0.5 V to 7 V
Input voltage (see Note 1)	−0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	
Voltage applied to any output in the high state	-0.5 V to VCC
Current into any output in the low state: SN54BCT245	96 mA
SN74BCT245	128 mA
Operating free-air temperature range: SN54BCT245	-55°C to 125°C
SN74BCT245	0°C to 70°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SI	N54BCT24	5	AS	174BCT24	5	UNIT
1			MIN	NOM	MAX	MIN	NOM	MAX	J
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			٧
VIL	Low-level input voltage				0.8			0.8	٧
ЧK	Input clamp current				-18			-18	mA
ЮН	High-level output current	A1-A8			-3			-3	mA
1.011		B1-B8			-12			-15	mA
loL	Low-level output current	A1-A8			20			24	mA
1.05		B1-B8			48			64	mA
TA	Operating free-air temperature)	-55		125	0		70	°C



NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

SN54BCT245, SN74BCT245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5.5 V (unless otherwise noted)

PAR	RAMETER	TE	ST CONDITIONS	SI	N54BCT24	15	SI	174BCT24	5	UNIT
	IAME I EII	,-	OT CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	ONI
VIK		$V_{CC} = 4.5 V,$	I _{IK} = -18 mA			-1.2			-1.2	V
	Any A		$I_{OH} = -1 \text{ mA}$	2.5	3.4		2.5	3.4		
	/		IOH = -3 mA	2.4	3.3		2.4	3.3		
VOH		$V_{CC} = 4.5 V$	IOH = -3 mA	2.4	3.3		2.4	3.3		V
	Any B	Any B	IOH = -12 mA	2	3.2					
		$I_{OH} = -15 \text{mA}$				2	3.1			
	Any A		I _{OL} = 20 mA		0.3	0.5				
VOL	'"', '	$V_{CC} = 4.5 \text{ V}$	I _{OL} = 24 mA					0.35	0.5	v
·OL	VOL Any B	1.00	I _{OL} = 48 mA		0.38	0.55				,
	/, 5		I _{OL} = 64 mA					0.42	0.55	
tı‡	A and B	$V_{CC} = 5.5 V$	V _I = 5.5 V			1			1	mA
-1	DIR and G	$V_{CC} = 5.5 V$	V _I = 5.5 V			0.1			0.1	
l _H ‡	A and B	$V_{CC} = 5.5 \text{ V},$	Vı = 27V			70			70	μΑ
1111	DIR and G	1 100 010 1,	-1			20			20	٠,
IIL	A and B	$V_{CC} = 5.5 V_{c}$	$V_1 = 0.5 \text{V}$			-0.65			-0.65	mA
-112	DIR and G	1 100 010 1,	.,			-1.2			-1.2	
los§	Any A	$V_{CC} = 5.5 V,$	Vo = 0	-60		-150	-60		- 150	mA
.03	Any B	100 010 1,	.0 0	-100		-225	-100		-225	
ІССН		$V_{CC} = 5.5 V,$	See Note 2		36	57		36	57	
ICCL		$V_{CC} = 5.5 V,$	See Note 2		57	90		57	90	mA
Iccz		V _{CC} = 5.5 V			10	15		10	15	
Cin	G and DIR				7			7		
CIO	A to B	$V_{CC} = 5.5 V,$	$V_{I} = 2.5 \text{ V or } 0.5 \text{ V}$		9			9		pF
CIO	B to A				12			12		

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25^{\circ}\text{C}$.

switching characteristics (see Figure 1)

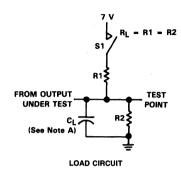
PARAMETER	FROM (INPUT)	то (оитрит)	C _L R1 R2 T,	CC = 5 V, = 50 pF = 500 Ω = 500 Ω A = 25°C	, ,	SN5/	V _{CC} = 4.5 C _L = 5 R1 = 5 R2 = 5 T _A = MIN	50 pF, 500 Ω, 500 Ω, I to MAX	BCT245	UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	A or B	B or A	1	4.4	6	1	7.2	1	7	ns
tPHL	1 70.5	BOIX	1.5	4.8	6.6	1.5	7.6	1.5	7	
tPZH	G	A or B	1.5	8	9.4	1.5	11.2	1.5	10.9	ns
tPZL	1 ~	/ / / /	1.5	8	10.2	1.5	11.8	1.5	11.6	
tPHZ	G	A or B	1.5	5.8	8.3	1.5	9.7	1.5	9.3	ns
tPLZ	1	7.515	1.5	5.1	7.8	1.5	9.6	1.5	9.1	

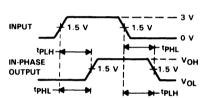


[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: ICCH and ICCL are measured in the A to B mode.



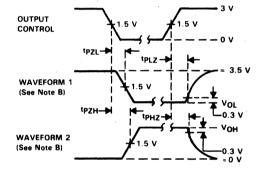


OUTPUT

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

SWITCH POSITION TABLE

TEST	S1
tPLH	Open
tPHL	Open
^t PZH	Open
tPZL	Closed
^t PHZ	Open
^t PLZ	Closed



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

OUT-OF-PHASE

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

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- C. All Input pulses are supplied by the generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS



SN54BCT373, SN74BCT373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D3145, SEPTEMBER 1988-REVISED OCTOBER 1988

- 8-Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- State of the Art BiCMOS Design Significantly Reduces ICC
- Comparable Speed and Improved Power Performance Relative to 54F/74F373
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic Ceramic 300-mil DIPs

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'BCT373 are transparent D-type latches. While the enable (C) is high, the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output-control (\overline{OC}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface components.

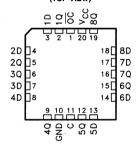
The output control (\overline{OC}) does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54BCT373 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT373 is characterized for operation from 0°C to 70°C.

SN54BCT373 ... J PACKAGE SN74BCT373 ... DW OR N PACKAGE (TOP VIEW)

U20∏ V_{CC} oc ⊓₁ 1Q ∏2 19 8Q 1 D 🗆 3 18 8D 2D 🗆 4 17 T 7D 2Q ∏5 16 7 7 Q 30 ∏6 15 60 3D ∏7 14 \ 6D 4D 🗆 8 13 7 5 D 40 ∏9 12 7 50 GND ∏10 11∏ C

SN54BCT373 ... FK PACKAGE (TOP VIEW)



FUNCTION TABLE (each latch)

	INPUTS		OUTPUT
<u>oc</u>	ENABLE C	D	Q
L	. H	Н	Ι
L	н	L	L
L	L	Х	Q ₀
Н	X	X	Z

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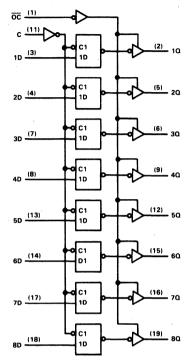
logic symbol[†]

OC (1)	·				
c (11)	EN C1				
1D (3)	10	D	솬	(2)	- 1Q
2D (4)			_	(5)	- 2Q
3D (7)	 			(6)	- 3Q
4D (8)	<u> </u>		-	(9)	- 40
5D (13)	├		[(12)	- 5Q
6D (14)	 		—[(15)	- 6Q
7D (17)	 		\dashv	(16)	- 7Q
8D (18)	┝		\dashv	(19)	- 8Q

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, VCC	-0.5 V to 7 V
Input voltage (see Note 1)	-0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 7 V
Voltage applied to any output in the high state	-0.5 V to VCC
Input clamp current	
Current into any output in the low state: SN54BCT373	96 mA
SN74BCT373	128 mA
Operating free-air temperature range: SN54BCT373	-55°C to 125°C
SN74BCT373	0°C to 70°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.

SN54BCT373, SN74BCT373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54BCT373			SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	J
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.8			0.8	٧
١ĸ	Input clamp current			-18			-18	mA
Юн	High-level output current			-12			-15	mA
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN	154BCT37	3	SN	74BCT37	'3	UNIT
, Allameter	1201 CONDITIONS				TYP	MAX	MIN	TYP	MAX	0.11.1
VIK	$V_{CC} = 4.5 V,$	$l_{\parallel} = -18 \text{ mA}$				-1.2			-1.2	V
			IOH = -3 mA	2.4	3.3		2.4	3.3		
Voн	V _{CC} = 4.5 V		IOH = -12 mA	2	3.2					V
			IOH = -15 mA				2	3.1		
VOL	V _{CC} = 4.5 V		IOL = 48 mA		0.38	0.55				V
- 02	100		IOL = 64 mA				,	0.42	0.55	
lozh	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$				50			50	μΑ
IOZL	$V_{CC} = 5.5 V,$	$V_0 = 0.5 V$				-50			-50	μΑ
Ц	$V_{CC} = 5.5 V,$	V _I = 5.5 V				0.4			0.4	mA
ЧΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V				20			20	μΑ
IIL	$V_{CC} = 5.5 V,$	V _I = 0.5 V				-0.6			-0.6	mA
los‡	$V_{CC} = 5.5 V,$	VO = 0		-100		-225	-100		-225	mA
ICCL	$V_{CC} = 5.5 V$				37	60		37	60	mA
ICCH	$V_{CC} = 5.5 V$				2	5		2	5	mA
Iccz	$V_{CC} = 5.5V$				5	8		5	8	mA
Ci	$V_{CC} = 5 V$,	V _I = 2.5 V or 0.5 V			6			6		pF
Co .	$V_{CC} = 5 V$,	$V_{O} = 2.5 \text{V} \text{or} 0.5 \text{V}$			11	-		11		pF

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25°C.

timing requirements

		V _{CC} =				to 5.5 V, to MAX§		UNIT
		'BCT:	'BCT373		CT373	SN74BCT373		0
ì		MIN	MAX	MIN	MAX	MIN	MAX	
tsu	Setup time, Data before enable C ↓	2		2		2		ns
th	Hold time, Data after enable C↓	5.5		5.5		5.5		ns
tw	Pulse duration, Enable C high	7.5		7.5		7.5		ns

[§] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.



[‡] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

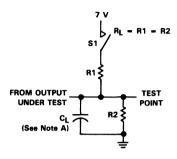
SN54BCT373, SN74BCT373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)			V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C				50 pF, 500 Ω, 500 Ω,	•	UNIT	
	1.			'ВСТ373		SN54I	BCT373	SN74BCT373			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
tPLH	D.	Any Q	2	5.9	7.7	1.5	10.1	2	9.3	ns	
tPHL	D	Any Q	2	6.7	8.5	1	10.3	1.5	9.5	ns	
tPLH .	С	Any Q	2	6.2	8.2	2	10.1	2	9.3	ns	
tPHL	С	Any Q	2	5.9	7.8	2	9.2	2	8.8	ns	
^t PZH	<u>oc</u>	Any Q	1	7.8	9.6	1	12.3	1	11.8	ns	
tPZL	ŌC	Any Q	1	8.2	10.2	1	12.5	1	12	ns	
tPHZ	ŌC	Any Q	1	4.9	6.6	1	7.4	1	7	ns	
tPLZ	OC.	Any Q	1	5	6.7	1	8.1	1	7.4	ns	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

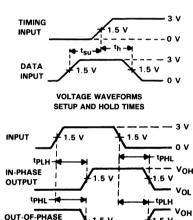




SWITCH POSITION TABLE

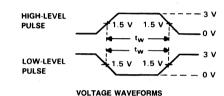
TEST	S1
^t PLH	Open
tPHL	Open
^t PZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed

LOAD CIRCUIT 1 ALL OUTPUTS EXCEPT FOR ERROR FLAG

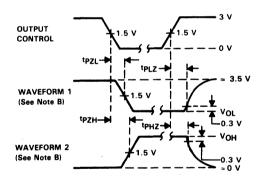


VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES



PULSE DURATIONS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C. includes probe and jig capacitance.

OUTPUT

- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f = 2.5$ ns, $t_f = 2.5$ ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
- Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS



SN54BCT374, SN74BCT374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D3130, SEPTEMBER 1988-REVISED DECEMBER 1988

- 8 D-Type Flip-Flops in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- State of the Art BiCMOS Design Significantly Reduces ICC
- Comparable Speed and Improved Power Performance Relative to 54F/74F374
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 3000-mil DIPs

description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

SN54BCT374 ... J PACKAGE SN74BCT374 ... DW OR N PACKAGE (TOP VIEW)

oc [1	∪20] V _{CC}
1Q [2	19 🗌 8Q
1 D [3	18 🗍 8D
2D [4	17 🗍 7 D
2Q [5	16 🗌 7 Q
3Q [6	15 🗌 6Q
3D [7	14 🗌 6D
4D [8	13 5D
4Q [9	12 5Q
GND [10	11 CLK

FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
oc	CLK	D	. Q
L	1	Н	н
L	↑	L	L
L	L	Х	QO
· L ·	Н	Х	QO
L	1	Х	QO QO XO Z
Н	X	Х	Z

The eight flip-flops of the 'BCT374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic levels that were set up at the D inputs.

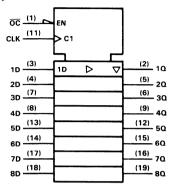
A buffered output-control (\overline{OC}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control (\overline{OC}) does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54BCT374 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74BCT374 is characterized for operation from 0°C to 70°C.



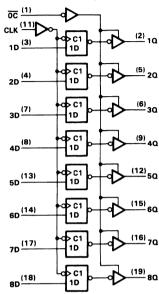
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, or N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, VCC	. −0.5 V to 7 V
Input voltage (see Note 1)	. −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to VCC
Input clamp current	30 mA
Current into any output in the low state: SN54BCT374	96 mA
SN74BCT374	128 mA
Operating free-air temperature range: SN54BCT374	-55°C to 125°C
SN74BCT374	0°C to 70°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.



SN54BCT374, SN74BCT374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54BCT374			AS	UNIT			
	·	MIN	NOM	MAX	MIN	NOM	MAX	0	
VCC	Supply Voltage	4.5	5	5.5	4.5	5	5.5	٧	
VIH	High-level input voltage	2			2			٧	
VIL	Low-level input voltage			0.8			0.8	٧	
ΙΚ	Input clamp current			-18			-18	mA	
ЮН	High-level output current			-12			-15	mA	
lOL	Low-level output current			48			64	mA	
TA	Operating free-air temperature	-55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIO	ONS	SI	154BCT37	4	AS .	174BCT37	4	UNIT
		. LOT COMBITIO		MIN	TYP	MAX	MIN	TYP [†]	MAX	0
VIK	$V_{CC} = 4.5 V$	I _I = -18 mA				-1.2			-1.2	٧
			IOH = -3 mA	2.4	3.3		2.4	3.3		
Voн	$V_{CC} = 4.5 V$		IOH = -12 mA	2	3.2					٧
			$I_{OH} = -15 \text{mA}$				2	3.1		
VOL	V _{CC} = 4.5 V		$I_{OL} = 48 \text{ mA}$		0.38	0.55				V
01	100		$I_{OL} = 64 \text{ mA}$					0.42	0.55	-
^l ozh	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$				50			50	μΑ
IOZL	$V_{CC} = 5.5 V,$	$V_0 = 0.5 V$				-50			-50	μΑ
lj	$V_{CC} = 5.5 V$,	$V_I = 5.5 V$				0.4			0.4	mA
Ī	$V_{CC} = 5.5 V$,	$V_1 = 2.7 V$				20			20	μΑ
늰	$V_{CC} = 5.5 V,$	$V_{ } = 0.5 V$				-0.6			-0.6	mA
los‡	$V_{CC} = 5.5 V,$	VO = 0		-100		-225	-100		-225	- mA
ICCL	$V_{CC} = 5.5 V$				37	60		37	60	mA
ICCH	$V_{CC} = 5.5 V$				2	5		2	5	mA
Iccz	$V_{CC} = 5.5 V$				5	8		5	8	mA
Ci	$V_{CC} = 5 V$,	$V_{ } = 2.5 \text{V or } 0$).5 V		6			6		pF _
Co	$V_{CC} = 5 V$,	$V_0 = 2.5 V or$	0.5 V		10			10		pF

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25°C.

timing requirements

		V _{CC} = T _A =				V to 5.5 V, to MAX§	,	UNIT
		'ВСТ	374	SN54B0	CT374	SN74B0	CT374	
	,	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		70		70		70	MHz
t _{su}	Setup time, Data before CLK↑	6.5		6.5		6.5		ns
th	Hold time, Data before CLK↑	0		0		0		ns
tw	Pulse duration, CLK high	7		8		7		ns

[§] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.



^{*} Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

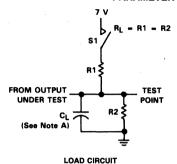
SN54BCT374, SN74BCT374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	1	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}C$			UNIT			
						SN54	3CT374	SN74E	SN74BCT374	
			MIN	TYP	MAX	MiN	MAX	MIN	MAX	
fmax			70			70		70		MHz
tPLH	CLK	Q	2	7.2	9.1	2	11.6	2	10.6	ns
tPHL	1 52		2	7.1	8.8	2	10.6	2	10	1.0
tPZH	ŌC	Q	1	8.3	10.1	1	12:7	1	12.3	ns
tPZL	1	_	1	8.6	10.6	1	13	1	12.7	
tPHZ	ŌC	Q	1	4.7	6.3	1	7.1	1	6.8	ns
tPLZ]		1	4.8	6.3	1	7.5	1	6.8	

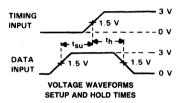
[†] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

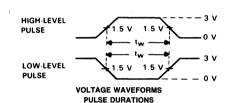


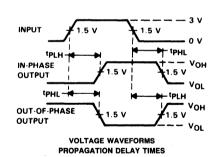


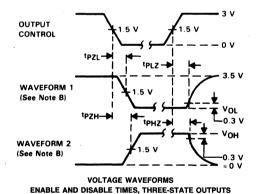
SWITCH POSITION TABLE

TEST	S1
tPLH	Open
tPHL .	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed









NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS



SN54BCT540, SN74BCT540 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D3125, JULY 1988

- State of the Art BiCMOS Design Significantly Reduces ICCZ
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These octal buffers and line drivers are designed to have the performance of the popular SN54BCT240/SN74BCT240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR gate so that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

The SN54BCT540 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74BCT540 is characterized for operation from 0°C to 70°C.

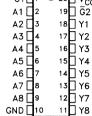
FUNCTION TABLE

	ı	INPUTS	OUTPUT	
	G1	G2	Α	Y
i	L	L	L	Н
	L	L	Н	L
	н	X	Х	z
	х	Н	Х	z

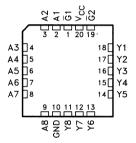
Z = High Impedance

SN54BCT540 ... J PACKAGE SN74BCT540 ... DW OR N PACKAGE

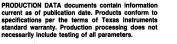
(**TOP VIEW**)



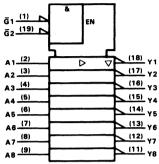
SN54BCT540 ... FK PACKAGE (TOP VIEW)



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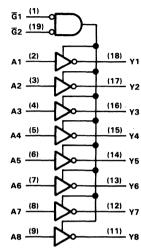


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	
Input voltage	
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to V _C C
Current into any output in the low state: SN54BCT540	96 mA
SN74BCT540	128 mA
Operating free-air temperature range: SN54BCT540	-55°C to 125°C
SN74BCT540	0°C to 70°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SI	SN54BCT540			SN74BCT540			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧	
VIH	High-level input voltage	2			2			٧	
VIL	Low-level input voltage			0.8			0.8	٧	
ΊΚ	Input clamp current			-18			-18	mA	
ЮН	High-level output current			-12			15	mA	
lOL	Low-level output current			48			64	mA	
TA	Operating free-air temperature	-55		125	0		70	°C	



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	т	EST CONDITIO	NS†	SI	154BCT54	0	SN74BCT540			UNIT
. Anameten	•	LOT CONDITIO	MIN	TYP [‡]	MAX	MIN.	TYP‡	MAX	Oilli	
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA				-1.2			-1.2	٧
			IOH = -3 mA	2.4	3.3		2.4	3.3		
VOH VCC = 4.5	V _{CC} = 4.5 V	CC = 4.5 V	IOH = -12 mA	2	3.2					l v
			IOH = -15 mA				2	3.1		
VOL	$V_{CC} = 4.5 V$		IOL = 48 mA		0.38	0.55				V
·OL	100		IOL = 64 mA					0.42	0.55	·
lozh	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$				50			50	μΑ
lozL	$V_{CC} = 5.5 V$	$V_0 = 0.5 V$				-50			-50	μΑ
lį .	$V_{CC} = 5.5 V,$	V _I = 5.5 V				0.1			0.1	mA
lін	$V_{CC} = 5.5 V_1$	$V_1 = 2.7 V$				20			20	μΑ
li <u>L</u>	$V_{CC} = 5.5 V,$	$V_1 = 0.5 V$				-0.6			-0.6	mA
los§	$V_{CC} = 5.5 V,$	VO = 0		-100		-225	-100		-225	mA
ICCL	$V_{CC} = 5.5 V$				45	71		. 45	71	mA
ICCH	V _{CC} = 5.5 V				20	30		20	30	mA
lccz	V _{CC} = 5.5 V				3	6		3	6	mA
Ci	$V_{CC} = 5 V$,	$V_1 = 2.5 \text{V or } 0$	0.5 V		6			5		pF
Co	V _C C = 5 V,	$V_{I} = 2.5 \text{V or } 0$).5 V		10			10		ρ.

[†] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

switching characteristics

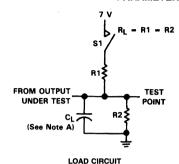
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}C$		TO R2 = 500 Ω ,				UNIT	
-			,	'BCT540		SN54BCT540 S		SN7	4BCT540	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	Α	Y	2.5	4.1	5.8	1.9	7.2	2	6.9	ns
tPHL	Α	Y	0.6	1.9	3.5	0.3	4.5	0.3	4	ns
^t PZH	G	Y	4.8	6.8	8.9	4.1	10.4	4.1	10.1	ns
tPZL	Ğ	Y	6	8	10	5.3	11.8	5.3	11.3	ns
tPHZ	Ğ	Y	3.5	5.7	7.8	2.7	9.4	2.7	9	ns
tPLZ	G	Y	3.8	5.5	7.4	3.5	8.9	3.5	8.5	ns

[†] For conditions specified as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.



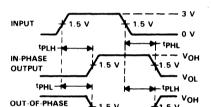
[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

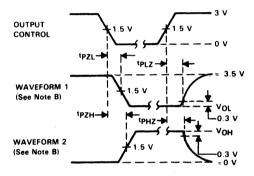


TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed

SWITCH POSITION TABLE



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.

OUTPUT

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by the generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - FIGURE 1. SWITCHING CHARACTERISTICS

SN54BCT541, SN74BCT541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D3126, JULY 1988

- State of the Art BiCMOS Design Significantly Reduces ICCZ
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These octal buffers and line drivers are designed to have the performance of the popular SN54BCT240/SN74BCT240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board lavout.

The three-state control gate is a 2-input NOR gate so that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

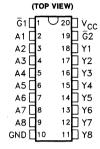
The SN54BCT541 is characterized for operation over the full military temperature range of —55°C to 125°C. The SN74BCT541 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

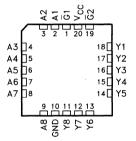
(INPUTS	OUTPUT	
Ğ1	Ğ2	A	Y
L	L	٦	L
L	L	Н	н
н	X	Х	Z
X	н	Х	z

Z = High Impedance

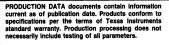
SN54BCT541 ... J PACKAGE SN74BCT541 ... DW OR N PACKAGE



SN54BCT541 ... FK PACKAGE (TOP VIEW)



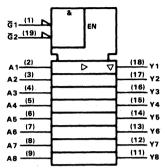
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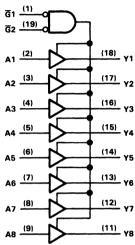
SN54BCT541, SN74BCT541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, VCC	0.5 V to 7 V
Input voltage (see Note 1)	. -0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to V _C C
Current into any output in the low state: SN54BCT541	96 mA
SN74BCT541	128 mA
Operating free-air temperature range: SN54BCT541	-55°C to 125°C
SN74BCT541	0°C to 70°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied, Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54			SN74BCT541			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	0
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.8			0.8	٧
ΊΚ	Input clamp current			-18			-18	·mA
ЮН	High-level output current			-12			-15	mA
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	0		70	· °C



NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	1	EST CONDITIO	SI	SN54BCT541			174BCT54	1	UNIT	
TATIONIE I ETT	•	LOT GONDING	MIN	TYP‡	MAX	MIN	TYP‡	MAX	0,	
ViK	$V_{CC} = 4.5 V$	$I_{\parallel} = -18 \text{mA}$				-1.2			-1.2	V
			IOH = -3 mA	2.4	3.3		2.4	3.3		
VOH VC	V _{CC} = 4.5 V		IOH = -12 mA	2	3.2					٧
			IOH = -15 mA				2	3.1		
VOL	V _{CC} = 4.5 V		IOL = 48 mA		0.38	0.55				٧
·OL	.00		IOL = 64 mA					0.42	0.55	
lozh	$V_{CC} = 5.5 V$	$V_0 = 2.7 V$				50			50	μΑ
IOZL	V _C C = 5.5 V,	$V_{O} = 0.5 V$				-50			-50	μΑ
lj.	VCC = 5.5 V,	V _I = 7 V				0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V				20			20	μΑ
ηL	$V_{CC} = 5.5 V$	$V_1 = 0.5 V$				-0.6			-0.6	mA
los§	$V_{CC} = 5.5 V,$	V _O = 0		-100		-225	-100		-225	mA
ICCL	VCC = 5.5 V				47	72		47	72	mA
ІССН	V _{CC} = 5.5 V				27	40		27	40	mA
Iccz	V _{CC} = 5.5 V				5	7		5	7	mA
Ci	V _{CC} = 5 V,	V _I = 2.5 V or 0).5 V		5			5		pF
Co	V _{CC} = 5 V,	V _I = 2.5 V or 0).5 V		10			10		۳.

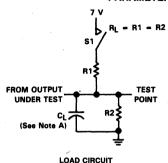
[†] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_{A} = 25^{\circ}\text{C}$			$\label{eq:VCC} \begin{array}{ll} \textbf{V}_{\text{CC}} = \textbf{4.5 V to 5.5 V,} \\ \textbf{C}_{\text{L}} = \textbf{50 pr,} \\ \textbf{R1} = \textbf{500 } \Omega, \\ \textbf{R2} = \textbf{500 } \Omega, \\ \textbf{T}_{\text{A}} = \textbf{MIN to MAX}^{\dagger} \end{array}$				UNIT
				'BCT541		SN54BCT541		SN74	SN74BCT541	
	1		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	Α	Y	2.1	3.7	5.3	1.7	6.3	1.7	6	ns
tPHL	Α	Y	3.7	5.5	7.5	3.2	8.7	3.4	8.2	ns
^t PZH	Ğ	Y	5.3	7.2	9.3	4.4	11	4.6	10.7	ns
tPZL	Ğ	Y	6	8	10.4	5.4	12.4	5.4	11.5	ns
t _{PHZ}	Ğ	Y	3.5	5.6	7.6	3	9.1	3	8.6	ns
tPLZ	Ğ	Y	3.4	5.2	7.2	3	9.4	3	8.6	ns

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

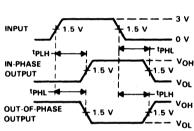


TEST	S1
tPLH	Open
t _{PHL}	Open
tPZH	Open
tPZL.	Closed
t _{PHZ}	Open

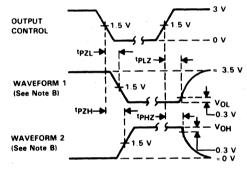
Closed

tPLZ

SWITCH POSITION TABLE



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
- Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by the generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.

FIGURE 1. SWITCHING CHARACTERISTICS

SN54BCT543, SN74BCT543 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

D3199, NOVEMBER 1988

- 3-State True Outputs
- Back-to-Back Registers for Storage
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Standard Plastic and Ceramic 300-mil DIPs

description

The 'BCT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable (LEAB or LEBA) and Output Enable (GAB or GBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B Enable (CEAB) input must be low in order to enter data from A or to output data from B. Having CEAB low and LEAB low makes the A-to-B latches transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and GAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the CEBA, LEBA, and GBA inputs.

The SN54BCT543 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT543 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

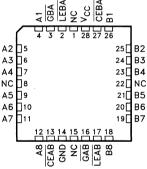
	INP	UTS		OUTPUTS	LATCH STATUS
GAB	CEAB	LEAB	DATA	B1 THRU B8	A TO B [†]
Н	Х	Х	Х	Z	OUTPUTS DISABLED
L	Н	L	L	z	OUTPUTS DISABLED
L	Н	L	Н	Z	DATA LATCHED
L	L	Н	Н	L	DATA LATCHED‡
L	L	Н	Н	Н	
L	L	L	L	L	TRANSPARENT
L	L	L	Н.	Н	

[†] A-to-B data flow is shown: B-to-A flow control is the same except uses CEBA, LEBA, and GBA.

SN54BCT543 ... JT PACKAGE SN74BCT543 ... DW OR NT PACKAGE (TOP VIEW)

LEBA [Įı .	U 24	□ v _{cc}
GBA	2	23	CEBA
A1 [3	22] B1
A2 [4	21] B2
A3 [5	20	_ B3
A4 [6	19	□B4
A5 [7	18] B5
A6 [8	17	□ B6
A7 [9	16] B7
A8 [10	15	□ B8
CEAB	11	14	LEAB
GND [12	13	GAB

SN54BCT543 ... FK PACKAGE (TOP VIEW)



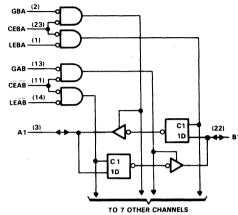
NC-No internal connection

[‡] Data present before low-to-high transition of LEAB.

SN54BCT543, SN74BCT543 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

logic symbol† GBA 1EN3 (23)CEBA (1) LEBA 1C5 (13)GAB 2EN4 CEAB (11) G2 (14)LEAB (22) 5D 4 V (20) (17)

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, VCC	-0.5 V to 7 V
Input voltage (I/O ports) (see Note 1)	-0.5 V to 5.5 V
Input voltage (Excluding I/O ports) (see Note 1)	-0.5 V to 7 V
Voltage applied to any output in the high state	-0.5 V to VCC
Input clamp current	−30 mA
Current into any output in the low state: SN54BCT543	96 mA
SN74BCT543	128 mA
Operating free-air temperature range: SN54BCT543	-55°C to 125°C
SN74BCT543	0°C to 70°C
Storage temperature range	-65°C to 150°C

^{\$} Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions

		SI	SN54BCT543		SN74BCT543			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	ONL
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.8			0.8	٧
ΊΚ	Input clamp current			-18			-18	mA
ЮН	High-level output current			-12			-15	mA
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	0		70	ů

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SI	154BCT5	13	SN74BCT543			UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	ONIT
VIK		$V_{CC} = 4.5 \text{ V}, I_{\parallel} = -18 \text{ mA}$				-1.2			-1.2	٧
			IOH = -3 mA	2.4	3.3		2.4	3.3		
۷он		V _{CC} = 4.5 V	$I_{OH} = -12 mA$	2	3.2					٧
			$I_{OH} = -15 \text{mA}$				2	3.1		
VOL		V _{CC} = 4.5 V	$I_{OL} = 48 \text{ mA}$		0.38	0.55				v
10L 4.5 V		100	$I_{OL} = 64 \text{ mA}$					0.42	0.55	
lį		$V_{CC} = 5.5 V, V_{I} = 5.5 V$				0.4			0.4	mA
IIH	Control inputs	V _{CC} = 5.5 V, V _I = 2.7 V				20			20	μΑ
	A and B					70			70	
I _{IL} §	Control inputs	$V_{CC} = 5.5 V, V_{I} = 0.5 V$				-0.6			-0.6	mA
	A and B					-0.65			-0.65	
los‡		$V_{CC} = 5.5 V, V_{O} = 0$		-100		-225	-100		-225	mA
ICCL		V _{CC} = 5.5 V			45	71		45	71	mA
ICCH		V _{CC} = 5.5 V			5	8		5	8	mA
ICCZ		V _{CC} = 5.5 V			9	15		5	15	mA
Ci	Control inputs	V _{CC} = 5 V, V _I = 2.5 V or 0.5	٧		6			6		pF
Cio	A and B	$V_{CC} = 5 \text{ V}, V_{I} = 2.5 \text{ V or } 0.5$	٧		16			16		pF

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25°C.

[‡] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

 $[\]mbox{\$}$ For I/O ports, the parameters $\mbox{I}_{\mbox{\scriptsize IH}}$ and $\mbox{I}_{\mbox{\scriptsize IL}}$ include the off-state output current.

SN54BCT543, SN74BCT543 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

timing requirements

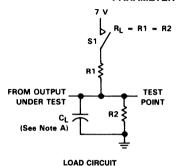
		V _{CC} =				V to 5.5 V TO MAX [†]	1	UNIT
		'BCT	'BCT543		SN54BCT543		SN74BCT543	
		MIN	MAX	MIN	MAX	MIN	MAX	
tsu	Setup time, data before latch enable ↑	4.5		4.5		4.5		ns
th	Hold time, data after latch enable ↑	1.5		1.5		1.5		ns
tw	Pulse duration, latch enable low	7		7		7		ns

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}\text{C}$			C _L = 1 R1 = 1 R2 = 1	500 Ω,	•	ŲŅIT	
			,	'BCT543 SN54BCT543		SN74BCT543				
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	i
tPLH	A or B	B or A	2	5.7	7.5	2	9.9	2	8.8	ns
tPHL		2 0.7.	2	6.3	8.2	2	` 9.7	2	9.6	
tpLH	TE	A or B	2	8.2	10.3	2	13.9	2	12.9	ns
tPHL			2	8.5	10.6	2	13.2	2	12.7	
^t PZH	G	A or B	1	6.8	8.6	1	11.4	1	10.7	ns
tPZL t		7.0.5	1	8.7	10.8	1	12.8	1	12.3	
tPHZ	G	A or B	1	5.5	7.2	1	8.8	1	8.1	ns
tPLZ		7.0.2	1	4.7	6.4	1	8.1	1	7.2	
tPZH	CE	A or B	1	7.6	9.8	1	12.8	1	12	ns
^t PZL			1	9.5	11.6	1	13.8	1	13.5] "
tPHZ	CE	A or B	1	5.8	7.5	1	9.3	1	8.5	ns
tPLZ		7.312	1	4.8	6.7	1	8.4	1	7.6	

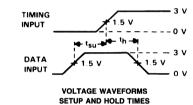
[†] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

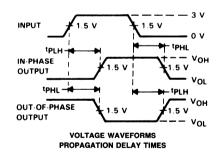


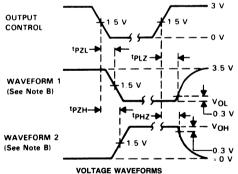


SWITCH POSITION TABLE

TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed







ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f = 2.5$ ns, $t_f = 2.5$ ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS



SN54BCT534, SN74BCT534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D3322, AUGUST 1989

- 8 D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving Inverting Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- State of the Art BiCMOS Design Significantly Reduces ICC7
- Functionally Equivalent to 54F534 and 74F534
- ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015
- Power-Up High-Impedance State
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

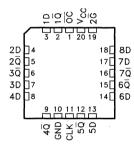
description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

SN54BCT534 ... J PACKAGE SN74BCT534 ... DW OR N PACKAGE (TOP VIEW)

oc [1	U 20	þ	٧cc
1Q [2	19		8Q
1 D [3	18		8D
2D [4	17		7D
2Q [5	16		7Q
3Q [6	15		6Q
3D [7	14		6D
4D [8	13		5D
4Q [9	12		5Q
GND [10	11		CLK

SN54BCT534 ... FK PACKAGE (TOP VIEW)



The eight flip-flops of the 'BCT534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the $\overline{\mathbb{Q}}$ outputs will be set to the complement of the logic levels that were set up at the D inputs.

A buffered output-control (\overline{OC}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control (\overline{OC}) does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54BCT534 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74BCT534 is characterized for operation from 0°C to 70°C.

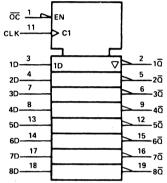


SN54BCT534, SN74BCT534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

FUNCTION TABLE (each flip-flop)

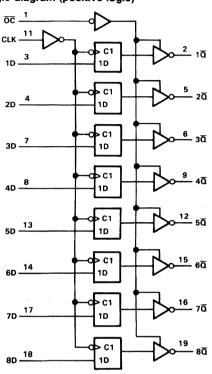
	INPUTS	OUTPUTS	
ŌĊ	CLK	D	ā
L	1	Н	L
L	1	L	н
L	L	X	Q ₀
Н	X	Х	Z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, VCC:	0.5 V to 7 V
Input voltage, V _I (see Note 1)	0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	0.5 V to 5.5 V
Voltage applied to any output in the high state	−0.5 V to V _C C
Input clamp current	−30 mA
Current into any output in the low state: SN54BCT534	96 mA
SN74BCT534	128 mA
Operating free-air temperature range: SN54BCT534	55°C to 125°C
SN74BCT534	0°C to 70°C
Storage temperature range	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



SN54BCT534, SN74BCT534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54BCT534			SN74BCT534			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	J
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage	1		0.8			0.8	٧
lik	Input clamp current			-18			-18	mA
ЮН	High-level output current			-12			-15	mA
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIO	SN54BCT534			SN74BCT534			UNIT	
1 ANAMETER	TEST CONDITIO	MIN	TYP†	MAX	MIN	TYP†	MAX	Oiti	
VIK	$V_{CC} = 4.5 \text{ V}, I_{I} = -18 \text{ mA}$				-1.2			-1.2	٧
		IOH = -3 mA	2.4	3.3		2.4	3.3		
VOH	V _{CC} = 4.5 V	IOH = -12 mA	2	3.2					V
		IOH = -15 mA				2	3.1		
VOL	V _{CC} = 4.5 V	IOL = 48 mA		0.38	0.55				٧
	100 110 1	IOL = 64 mA					0.42	0.55	
IOZH	$V_{CC} = 5.5 \text{ V}, V_{O} = 2.7 \text{ V}$				50			50	μΑ
IOZL	$V_{CC} = 5.5 \text{ V}, V_{O} = 0.5 \text{ V}$				-50			-50	μΑ
11	V _{CC} = 5.5 V, V _I = 5.5 V				0.4			0.4	mA
ΊΗ	$V_{CC} = 5.5 V, V_I = 2.7 V$				20			20	μΑ
ΊL	$V_{CC} = 5.5 \text{ V}, V_{I} = 0.5 \text{ V}$				-0.6			-0.6	mA
los‡	$V_{CC} = 5.5 \text{ V}, V_{O} = 0$		-100		-225	-100		-225	mA
ICCL	$V_{CC} = 5.5 \text{ V}, V_{O} = 0$			38	55		38	. 55	mA
ICCH	$V_{CC} = 5.5 V, V_{O} = 0$,		5	8		5	8	mA
lccz	$V_{CC} = 5.5 \text{ V}, V_{O} = 0$			4.5	7		4.5	7	mA
Ci	V _I = V _{CC} or GND, V _{CC} = 5 V			6			6		pF
Co	$V_O = V_{CC}$ or GND, $V_{CC} = 5$ V			10			10		. pF

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25°C.



[‡] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

SN54BCT534, SN74BCT534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

timing requirements

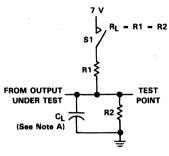
				V _{CC} = 5V, T _A = 25°C 'BCT534		V _{CC} = 4.5 V to 5.5 V, T _A = MIN to MAX [†]				
			'ВСТ			CT534	SN74BCT534		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency		0	77	0	.77	0	77	MHz	
t _{su}	Setup time, before enable CLK ↑	Data high	6		6		6		ns	
·su		Data low	9.5		9.5		9.5			
th	Hold time after CLK ↑	Data high	0		0		0		ns	
นา	Hold time after OLK	Data low	1		1		1		115	
+	Pulse duration	CLK high	6		6		6		ne	
tw	ruise duration	CLK low	7		7		7		ns	

switching characteristics (see Figure 1)

PARAMETER FROM TO (OUTPUT)		$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}\text{C}$			V	UNIT				
			,	BCT534		SN54B	CT534	SN74B	CT534	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax			77			77		77		MHz
tPLH	CLK	ō	3.3	6.7	9.6	3.3	12.8	3.3	11.4	ns
tPHL]		3.5	6.2	8.8	3.5	11	3.5	10	
tPZH	ōc	Q	3.9	7.6	10.3	3.9	13.1	3.9	12.5	ns
tPZL	7		4.6	8.2	11.1	4.6	13.7	4.6	13.3	
tPHZ	ōc	Q	2.6	4.7	6.7	2.6	8	2.6	7.4	ns
tPLZ	1 "		1.8	4.1	6.1	1.8	7.8	1.8	6.9	

[†] For conditions as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

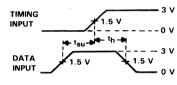




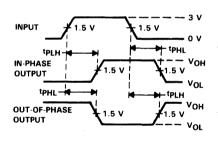
SWITCH POSITION TABLE

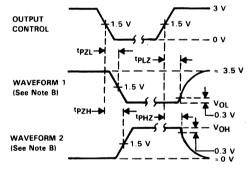
TEST	S1
tPLH .	Open
tPHL	Open
^t PZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed

LOAD CIRCUIT



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES





VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C. includes probe and jig capacitance.

- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0=50~\Omega$, $t_f=2.5$ ns, $t_f=2.5$ ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS



SN54BCT620A, SN74BCT620A OCTAL BUS TRANSCEIVERS

D3196. SEPTEMBER 1987—REVISED NOVEMBER 1988

- State of the Art BiCMOS Design Significantly Reduces ICCZ
- P-N-P Inputs Reduce DC Loading
- Functionally Equivalent to 54F620 and 74F620
- ESD Protection Exceeds 2000 V per MIL-STD-833C Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

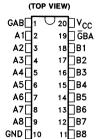
These octal bus transceivers are designed for asynchronous two-way communications between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs (GBA and GAB).

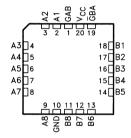
The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the octal bus transceivers the capability to store data by simultaneous activation of GBA and GAB. Each output reinforces its input in this transceiver configuration. When both enable inputs are activated and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

The SN54BCT620A is characterized for operation over the full military temperature range of -55° C to 125 $^{\circ}$ C. The SN74BCT620A is characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.

SN54BCT620A ... J PACKAGE SN74BCT620A ... DW OR N PACKAGE



SN54BCT620A ... FK PACKAGE (TOP VIEW)

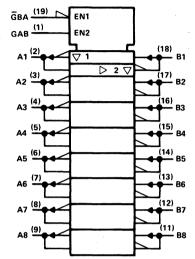


FUNCTION TABLE

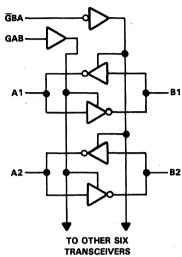
ENABLE	ENABLE INPUTS					
ĞВА	GAB	BCT620A				
L	L	B data to A bus				
Н	Н	Ā data to B bus				
Н	L	Isolation				
L	Н	B data to A bus				
L	Н	Ā data to B bus				

Texas VI

logic symbol†



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, VCC	. −0.5 V to 7 V
Input voltage (see Note 1): Control inputs	. −0.5 V to 7 V
I/O ports	-0.5 V to 5.5 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to V _C C
Input clamp current	−30 mA
Current into any output in the low state: SN54BCT620A	96 mA
SN74BCT620A	128 mA
Operating free-air temperature range: SN54BCT620A	-55°C to 125°C
SN74BCT620A	0°C to 70°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions

			SN	SN54BCT620A		SN74BCT620A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	0
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			٧
VIL	Low-level input voltage				0.8			0.8	٧
lik	Input clamp current				-18			-18	mA
ЮН	High-level output current	Any A			-3			-3	mA
.011	. ng. rever carpat carrent	Any B			-12			- 15	mA
lOL	Low-level output current	Any A			20			24	mA
.OL	2011 10101 0414 04110111	Any B			48			64	mA
TA	Operating free-air temperature		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TES	SN	54BCT62	DA	SN	74BCT620	DA	UNIT	
			ST CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP†	MAX	
VIK		$V_{CC} = 4.5 V$	$I_{\parallel} = -18 \text{ mA}$			-1.2			-1.2	٧
	Any A	V _{CC} = 4.5 V	IOH = -1 mA	2.5	3.4		2.5	3.4		٧
1			IOH = -3 mA	2.4	3.3		2.4	3.3		٧
Vон			IOH = -3 mA	2.4	3.3		2.4	3.3		٧
ŀ	Any B	$V_{CC} = 4.5 V$	IOH = -12 mA	2	3.2					٧
l			IOH = -15 mA				2	3.1		٧
	Any A	V _{CC} = 4.5 V	I _{OL} = 20 mA		0.3	0.5				٧
VOL	797.	100	$I_{OL} = 24 \text{ mA}$					0.35	0.5	٧
, OL	Any B	V _{CC} = 4.5 V	I _{OL} = 48 mA		0.38	0.55				V
	79	100	IOL = 64 mA					0.42	0.55	٧
11	A and B	$V_{CC} = 5.5 V,$	V _I = 5.5 V		,	1.0			1.0	mA
["	GAB or GBA	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1			0.1	mΑ
liH‡	A and B	$V_{CC} = 5.5 V,$	V _I = 2.7 V			70			70	μΑ
	GAB or GBA	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
I _{IL} ‡	A and B	$V_{CC} = 5.5 V,$	$V_{I} = 0.5 V$			-0.65			-0.65	mA
	GAB or GBA	$V_{CC} = 5.5 V,$	$V_{ } = 0.5 V$			-0.60			-0.60	mA
los§	Any A	$V_{CC} = 5.5 V,$	$V_O = 0$	-60		-150	-60		- 150	mA
.03	Any B	$V_{CC} = 5.5 V,$	$V_O = 0$	-100		-225	-100		-225	mA
ІССН		$V_{CC} = 5.5 V,$	See Note 2		23	37		23	37	mA
ICCL		$V_{CC} = 5.5 V,$	See Note 2		53	84		53	84	mA
Iccz		V _{CC} = 5.5 V			4	10		4	10	mA
Ci	GAB or GBA	$V_{CC} = 5 V$,	V _I = 2.5 V or 0.5 V		5			5		pF
Cio	Α	Vcc = 5 V	V _I = 2.5 V or 0.5 V		9			9		pF
	В	1.50 5.,	., 2.5 . 5. 5.5 .		12			12		<u></u>

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

NOTE 2: ICCH and ICCL are measured in the A to B mode.



For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

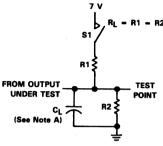
[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

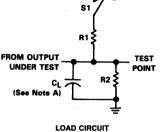
switching characteristics (see Figure 1)

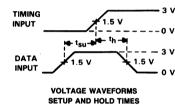
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2 T,	C = 5 V, = 50 pF, = 500 Ω = 500 Ω A = 25°C	, , ,	QNE4	V _{CC} = 4.5 C _L = 9 R1 = 5 R2 = 5 T _A = MIN	50 pF, 500 Ω, 500 Ω, to MAX [†]	CT620A	UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tpLH	Α	В	0.6	3.4	5.2	0.6	6.2	0.6	5.8	ns
tPHL	J	0.1	1.9	3.4	0.1	3.7	0.1 ′	3.6		
tPLH	В	Α	0.9	4.1	6	0.9	7.2	0.9	6.9	ns
tPHL			0.1	2	3.7	0.1	4	0.1	3.9	
tPZH	ĞВА	Α	3.5	7.2	9.2	3.5	10.9	3.5	10.6	ns
tPZL			3.7	7.6	9.9	3.7	11.5	3.7	11.1	
tPHZ	ĞВА	Α	3.1	5.3	8.6	3.1	10.8	3.1	10	ns
tPLZ	 ,	, ,	1.3	4.4	6.9	1.3	8.3	1.3	7.8	
^t PZH	GAB	В	2	5.3	6.7	2	7.9	2	7.4	ns
tPZL	J., 10		2.9	6.1	8.1	2.9	9.2	2.9	9	
tPHZ	GAB	В	2.1	5.2	7	2.1	8.5	2.1	8.1	ns
tPLZ	L		0.1	3.7	5.3	0.1	6	0.1	5.9	

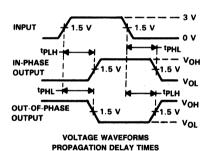
[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.





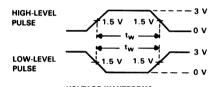




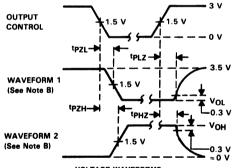


SWITCH POSITION TABLE

TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed







VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS



SN54BCT623, SN74BCT623 OCTAL BUS TRANSCEIVERS

D3057, SEPTEMBER 1988-REVISED NOVEMBER 1988

- State of the Art BiCMOS Design Significantly Reduces ICCZ
- Functionally Equivalent to SN54F623 and SN74F623
- ESD Protection Exceeds 2000 V per MIL-STD-833C Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil **DIPs**
- **Dependable Texas Instruments Quality and** Reliability

description

These octal bus transceivers are designed for asynchronous two-way communications between data buses. The control function implementation allows for maximum flexibility in timina.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs (GBA and GAB).

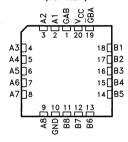
The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the octal bus transceivers the capability to store data by simultaneous activation of GBA and GAB. Each output reinforces its input in this transceiver configuration. When both enable inputs are activated and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

The SN54BCT623 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT623 is characterized for operation from 0°C to 70°C.

SN54BCT623 ... J PACKAGE SN74BCT623 ... DW OR N PACKAGE (TOP VIEW)

GAB[1	O 20	□vcc
A1[2	19	∏ĞBA
A2[3	18]B1
A3[4	17]B2
A4[5	16	_B3
A5[6	15	_B4
A6[7	14	_B5
A7[8	13	_B6
_8A	9	12	_B7
GND [10	11	_B8

SN54BCT623 ... FK PACKAGE (TOP VIEW)

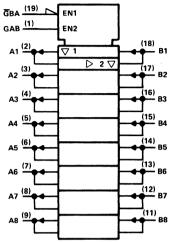


FUNCTION TABLE

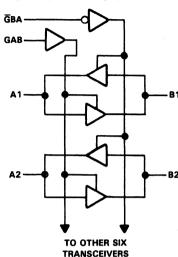
ENABLE	INPUTS	OPERATION
ĞВА	GAB	OFERATION
L	L	B data to A bus
Н	Н	A data to B bus
Н	L	Isolation
L	Н	B data to A bus
L	Н	A data to B bus



logic symbol[†]



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, VCC	-0.5	V to 7 V
Input voltage (see Note 1): Control inputs	-0.5°	V to 7 V
I/O ports	$-0.5\mathrm{V}$	to 5.5 V
Voltage applied to any output in the disabled or power-off state	$-0.5\mathrm{V}$	to 5.5 V
Voltage applied to any output in the high state	−0.5 V	to VCC
Input clamp current		-30 mA
Current into any output in the low state: SN54BCT623		96 mA
SN74BCT623		128 mA
Operating free-air temperature range: SN54BCT623	-55°C t	o 125°C
SN74BCT623	0℃	to 70°C
Storage temperature range	-65°C t	o 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions

			SI	154BCT62	:3	SN74BCT623			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	0
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧	
VIH	High-level input voltage		2			2			٧
VIL	Low-level input voltage			. 0.8			0.8	٧	
ΊK	Input clamp current				-18			-18	mA
ЮН	High-level output current	Any A			-3			-3	mA
ЮП	riigir iovor output ourroint	Any B			-12			-15	1111
lOL `	Low-level output current	Any A			20			24	- mA
·OL	2511 1515. Galpat Garrett	Any B			48			64	
TA	Operating free-air temperatur	e	-55	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P	ARAMETER	TEQ.	CONDITIONS	SI	N54BCT62	23	AS	UNIT		
		123	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	٧
	Any A	V _{CC} = 4.5 V	IOH = -1 mA	2.5	3.4		2.5	3.4		
	7,7.	1,00	IOH = -3 mA	2.4	3.3		2.4	3.3		
Vон			IOH = -3 mA	2.4	3.3		2.4	3.3		٧
	Any B	V _{CC} = 4.5 V	IOH = -12 mA	2	3.2					
			IOH = -15 mA	T			2	3.1		
	Any A Vcc =	V _{CC} = 4.5 V	IOL = 20 mA	1	0.3	0.5				
VOL	7, 7.	V _{CC} = 4.5 V	IOL = 24 mA					0.35	0.5	v
·OL	Any B		IOL = 48 mA		0.38	0.55				
	, -	100	IOL = 64 mA					0.42	0.55	
4	A and B	$V_{CC} = 5.5 V,$	V _I = 5.5 V			1			1	mA
1	GAB and GBA	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1			0.1	
liH‡	A and B	$V_{CC} = 5.5 V,$	V _I = 2.7 V			70			70	μΑ
.111	GAB and GBA	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	,
IIL‡	A and B	$V_{CC} = 5.5 V,$	V _I = 0.5 V			-0.65			-0.65	mA
·1L	GAB and GBA	$V_{CC} = 5.5 V,$	V _I = 0.5 V			-0.6			-0.6	
los	Any A	$V_{CC} = 5.5 V$,	NO = 0	-60		-150	-60		-150	mA
.03	Any B	$V_{CC} = 5.5 V$,	VO = 0	-100		-225	-100		-225	
ICCH		$V_{CC} = 5.5 V,$	See Note 2		33	53		33	53	mA
ICCL		$V_{CC} = 5.5 V$,	See Note 2		58	92		58	92	mA
ICCZ		$V_{CC} = 5.5 V$,		6	11		6	11	mA
Cin	GAB and GBA	$V_{CC} = 5 V$,	V _j = 2.5 V or 0.5 V		5			5		pF
Cio	Α	$V_{CC} = 5 V$,	V _I = 2.5 V or 0.5 V		9			9		pF
Cio	В	$V_{CC} = 5 V$,	V _I = 2.5 V or 0.5 V		12			12		pF

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25°C.

NOTE 2: ICCH and ICCL are measured in the A-to-B mode.



[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

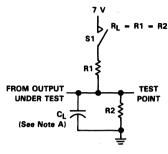
[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			ONE	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX [†] SN54BCT623 SN74BCT623				
			MIN	BCT623 TYP	MAX	MIN	MAX	MIN	MAX		
tPLH	Α	В	0.5	3.1	4.7	0.5	5.3	0.5	5.2	ns	
^t PHL	^		1.7	4.9	6.9	1.7	7.6	1.7	7.4	1115	
^t PLH	В	Α	0.9	4.1	5.9	0.9	6.8	0.9	6.7	ns	
tPHL.		^	1.8	5.3	7.6	1.8	8.3	1.8	8		
tPZH	Gва	Α	3.1	6.8	9.1	3.1	10.7	3.1	10.6	ns	
tPZL.		.,	3.3	7.2	9.6	3.3	11.3	3.3	10.7		
tPHZ	ĞВА	Α .	1.9	6.1	8.3	1.9	10.6	1.9	9.8	ns	
tPLZ		.,	1.1	4.6	7	1.1	8.1	1.1	7.8		
^t PZH	GAB	В	2	5	6.8	2	7.8	2	7.6	ns	
tPZL			2.7	6.2	8	2.7	9.3	2.7	8.9		
t _{PHZ}	GAB	В	1.1	4.6	6.5	1.1	8	1.1	7.7	ns	
t _{PLZ}		_	0.3	3.2	6.3	0.3	7.2	0.3	7.1		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

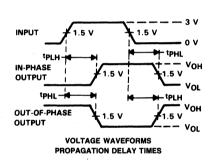


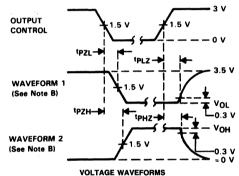


SWITCH POSITION TABLE

TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
t _{PHZ}	Open
tPLZ	Closed

LOAD CIRCUIT





ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

SN54BCT640, SN74BCT640 OCTAL BUS TRANSCEIVERS

D3057, SEPTEMBER 1988-REVISED FEBRUARY 1989

- BiCMOS Process with TTL Inputs and Outputs
- BiCMOS Design Substantially Reduces Standby Current
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs to Reduce DC Loading Effects
- Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

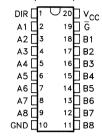
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input $(\overline{\mathbf{G}})$ can be used to disable the device so the buses are effectively isolated.

The SN54BCT640 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN54BCT640 is characterized for operation from 0°C to 70°C.

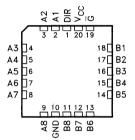
FUNCTION TABLE

	ITROL PUTS	OPERATION
G	DIR	
L	L	B data to A bus
L	Н	Ā data to B bus
н	Х	Isolation

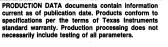
SN54BCT640 ... J PACKAGE SN74BCT640 ... DW OR N PACKAGE (TOP VIEW)



SN54BCT640 ... FK PACKAGE (TOP VIEW)

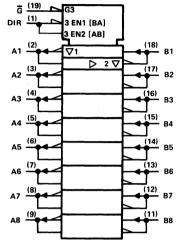


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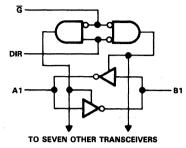




logic symbol†



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, VCC	−0.5 V to 7 V
Input voltage (see Note 1)	−0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	−0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to VCC
Input clamp current	−30 mA
Current into any output in the low state: SN54BCT640	96 mA
SN74BCT640	128 mA
Operating free-air temperature range: SN54BCT640	-55°C to 125°C
SN74BCT640	0°C to 70°C
Storage temperature range	-65°C to 150°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SI	154BCT64	10	SN	174BCT64	0	UNIT
Į					MAX	MIN	NOM	MAX	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage		2			2			٧
VIL	Low-level input voltage	,		0.8			0.8	٧	
ΙK	Input clamp current				18			-18	mA
ЮН	High-level output current	A1-A8			-3			-3	mA
.011	g ioto. oatpat oao	B1-B8			- 12			-15	
lOL	Low-level output current	A1-A8			20		***************************************	24	mA
.OL	20W 10VOI Output GuiToIII	B1-B8			48			64	
TA	Operating free-air temperatur	9	-55		125	0		70	°C



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P/	RAMETER	т	EST CONDITIONS	S	N54BCT6	40	SI	UNIT		
		•	MIN TY			MAX	MIN	TYP†	MAX	0.4
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	٧
	Any A	V _{CC} = 4.5 V	$I_{OH} = -1 \text{ mA}$	2.5	3.4		2.5	3.4		
	/, / .	100	IOH = -3 mA	2.4	3.3		2.4	3.3		
Vон			IOH = -3 mA	2.4	3.3		2.4	3.3		V
	Any B	V _{CC} = 4.5 V	I _{OH} = -12 mA	2	3.2					
			$I_{OH} = -15 \text{mA}$				2	3.1		
	Any A	V _{CC} = 4.5 V	I _{OL} = 20 mA		0.3	0.5				
VOL	/ " " " " " " " " " " " " " " " " " " "	100	I _{OL} = 24 mA					0.35	0.5	v
•OL	Any B	V _{CC} = 4.5 V	I _{OL} = 48 mA		0.38	0.55				
	/, 5	100 4.00	IOL = 64 mA					0.42	0.55	
lį	Control inputs	$V_{CC} = 5.5 V,$	V _I = 5.5 V			1.0			1.0	mA
-1	A or B ports	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1			0.1	
liH‡	Control inputs	$V_{CC} = 5.5 V,$	V _I = 2.7 V			70			70	μΑ
art.	A or B ports	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	,,,,,
IIL‡	Control inputs	$V_{CC} = 5.5 V,$	V _I = 0.5 V		-	-1.2			-1.2	mA
dE.	A or B ports	$V_{CC} = 5.5 V,$	V _I = 0.5 V			-0.60			-0.60	1117
los§	Any A	$V_{CC} = 5.5 V,$	VO = 0	-60		-150	-60		-150	mA
.03	Any B	$V_{CC} = 5.5 V,$	V _O = 0	-100		-225	100		-225	
ІССН		$V_{CC} = 5.5 V,$	See Note 1		23	37		23	41	mA
ICCL		$V_{CC} = 5.5 V,$	See Note 1		53	84		53	94	mA
lccz		$V_{CC} = 5.5 V$			4	10		4	11	mA

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25°C.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_{A} = 25^{\circ}C$				V _{CC} = 4.5 C _L = 5 R1 = 5 R2 = 5 T _A = MIN	50 pF, 500 Ω, 500 Ω,		UNIT
			,	BCT640		SN54	BCT640	SN74E	BCT640	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	A or B	B or A	0.5	3.6	5.6	0.5	7	0.5	6.5	ns
tPHL	1	50.7	0.5	1.9	3.4	0.5	3.8	0.5	3.7	
tPZH	G	A or B	2.6	6.4	8.9	2.6	10.5	2.6	10.2	ns
tPZL	1	1 710.5	3.5	6.9	9.5	3.5	12.3	3.5	10.7	
tPHZ	G	A or B	1.4	5	7.9	1.4	12.2	1.4	10.2	ns
^t PLZ			1.5	4.3	6.8	1.5	8.3	1.5	7.8	

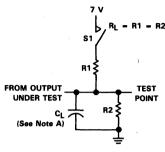
[¶] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

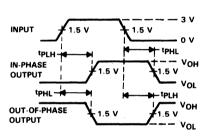
NOTE 1: ICCH and ICCL are measured in the A to B mode.



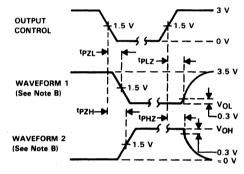
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
tPLH .	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open .
t _{PLZ}	Closed



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by the generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

AUGUST 1989

- State of the Art BiCMOS Design Significantly Reduces ICCZ
- Dependable Texas Instruments Quality and Reliability
- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

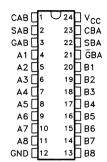
description

These devices consist of bus transceivers circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and GBA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the transceivers and registers.

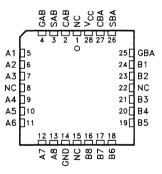
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The SN54BCT652 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT652 is characterized for operation from 0°C to 70°C.

SN54BCT652 ... JT PACKAGE SN74BCT652 ... DW OR NT PACKAGE (TOP VIEW)



SN54BCT652 ... FK PACKAGE (TOP VIEW)





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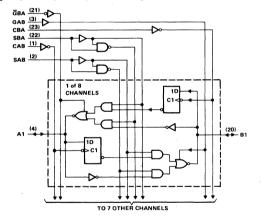
FUNCTION TABLE

		INP	UTS			DAT	A I/O	OPERATION OR FUNCTION
GAB	ĞBA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
XHLLLHHH	HHHHXLLLHHL	H or L + or L X X X H or L	H or L H or L X H or L X H or L	X X X X X X H H	X X X L H X X H	Input Input Input Input Unspecified‡ Output Output Output Input Output	Input Unspecified† Output Input Input Input Output Output	Isolation Store A and B Data Store A, Hold B Store A, Hold B Store A in both registers Hold A, Store B Store B in both registers Real-Time B Data to A Bus Stored B Data to A Bus Stored A Data to B Bus

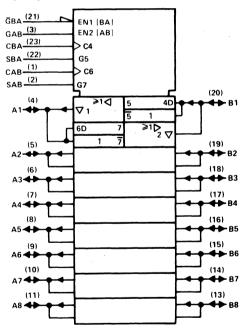
[‡] The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input function are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock i.

Select control = H: clocks must be staggered in order to load both registers.

logic diagram (positive logic)



logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



f Select control = L: clocks can occur simultaneously.

Pin numbers shown are for JT, DW, or NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	
Input voltage (I/O ports)	
Input voltage (Excluding I/O ports)	
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	0.5 V to VCC
Current into any output in the low state: SN54BCT652	96 mA
SN74BCT652	128 mA
Operating free-air temperature range: SN54BCT652	-55°C to 125°C
SN74BCT652	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54BCT652			SN74BCT652			UNIT
		MIN	MOM	MAX	MIN	NOM	MAX	UNII
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.8			0.8	V
lк	Input clamp current			-18			-18	mA
ЮН	High-level output current			-12			-15	mA
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	0		70	°C



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETER	TEGT GOVERNITION	No	SI	54BCT6	52	SN.	174BCT6	52		
PA	RAMETER	TEST CONDITIO	NS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
VIK		$V_{CC} = 4.5 \text{ V, I}_{I} = -18 \text{ mA}$				-1.2			-1.2	V	
			IOH = -3 mA	2.4	3.3		2.4	3.3			
VOH		V _{CC} = 4.5 V	IOH = -12 mA	2	3.2					V.	
			$I_{OH} = -15 \text{mA}$				2	3.1			
VOL		V _{CC} = 4.5 V	I _{OL} = 48 mA		0.38	0.55				>	
VOL		VCC - 4:5 V	IOL = 64 mA					0.42	0.55		
lj.	Control Inputs	$V_{CC} = 5.5 \text{ V}, V_{I} = 5.5 \text{ V}$				1			1	mA	
"	A or B	$V_{CC} = 5.5 \text{ V}, V_{I} = 5.5 \text{ V}$				1			1	111/	
liH‡	Control Inputs	$V_{CC} = 5.5 V, V_{I} = 2.7 V$				20			20		
	A or B	$V_{CC} = 5.5 \text{ V}, V_1 = 2.7 \text{ V}$				70			70	μΑ	
կլ‡	Control Inputs	$V_{CC} = 5.5 \text{ V}, V_{I} = 0.5 \text{ V}$				-1			-1	mA	
	A or B	$V_{CC} = 5.5 \text{ V}, V_{I} = 0.5 \text{ V}$				-1			-1		
los§		$V_{CC} = 5.5 \text{ V}, V_{O} = 0 \text{ V}$		-100		-225	-100		-225	mA	
ICCL		$V_{CC} = 5.5 \text{ V}, V_{I} = \text{GND}$			43	69		43	69	mA	
Іссн		$V_{CC} = 5.5 \text{ V}, V_{I} = 4.5 \text{ V}$			6	10		6	10	mA	
Iccz		$V_{CC} = 5.5 \text{ V}, V_{\parallel} = \text{GND}$			10	17		10	17	mA	
CI		$V_{CC} = 5 \text{ V}, V_{I} = 2.5 \text{ V or } 0.5 \text{ V}$			6			6		pF	
Clo		$V_{CC} = 5 \text{ V}, V_{\parallel} = 2.5 \text{ V or } 0.5 \text{ V}$			14			14		pF	

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25°C.

timing requirements

			VCC TA =	V _{CC} = 4.5 V to 5.5 V, T _A = MIN to MAX [†]				UNIT	
			'BCT652		SN54BCT652		SN74BCT652		UNII
			MIN	MAX	MIN	MAX	MIN	MAX	1
fclock	Clock frequency		0	77	0	77	0	77	MHz
	Dula - dunatian	CBA or CAB high	6.5		6.5		6.5		ns
t _W	Pulse duration	CBA or CAB low	6.5		6.5		6.5		
t _{su}	Setup time, before CAB ↑ or CBA ↑	A or B	5		5		5		ns
th	Hold time, after CAB↑ or CBA↑	A or B	1		1		1		ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operation Conditions.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

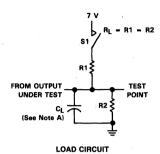
[§] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 V$, $C_{L} = 50 pF$, $R_{L} = 500 Ω$, $R_{L} = 500 Ω$, $R_{L} = 25^{\circ}C$				V _{CC} = 4.5 C _L = R1 = R2 = T _A = MIN 3CT652	50 pF, 500 Ω, 500 Ω, I to MAX [†]		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax	<u> </u>		77			77		77		MHz
tPLH	СВА	_	2.6	6.9	8.9	2.6	11.6	2.6	10.5	
tPHL	CBA	Α	2.8	6.8	8.8	2.8	10.7	2.8	9.9	ns
tPLH	CAB	В	2.6	6.9	8.9	2.6	11.6	2.6	10.5	
tPHL	CAB	Р	2.8	6.8	8.8	2.8	10.7	2.8	9.9	ns
tPLH	Α	В	1.7	5.8	7.5	1.7	10.3	1.7	8.9	
tPHL		В	2.4	6.5	8.2	2.4	10	2.4	9.8	ns
tPLH	В		1.7	5.8	7.5	1.7	10.3	1.7	8.9	
tPHL	1	Α	2.4	6.5	8.2	2.4	10	2.4	9.8	ns
tPLH	SBA‡		3.5	8.8	10.8	3.5	14.2	3.5	13.1	
tPHL	(with B high)	A	2.4	5.9	7.7	2.4	9.1	2.4	8.5	ns
tPLH	SBA‡	Α	3	7.6	9.7	3	12.4	3	11.3	
tPHL	(with B low)	^	3.8	8.3	10.4	3.8	12.9	3.8	12.5	ns
tPLH	SAB‡	В	3.5	8.8	10.8	3.5	14.2	3.5	13.1	
tPHL	(with A high)	P	2.4	5.9	7.7	2.4	9.1	2.4	8.5	ns
tPLH	SAB‡	В	3	7.6	9.7	3	12.4	3	11.3	
tPHL	(with A low)	P	3.8	8.3	10.4	3.8	12.9	3.8	12.5	ns
tPZH	GBA	Α	2.5	7.2	8.9	2.5	11.2	2.5	10.6	
†PZL	1 GBA	A	3.2	8.1	10.1	3.2	12.6	3.2	12	ns
tPHZ	GBA	_	2.8	6.7	8.8	2.8	10.9	2.8	10	
†PLZ	1 GBA	A	2.4	6.3	8.4	2.4	10.5	2.4	9.5	ns
^t PZH	GAB	В	1.5	5.4	7.1	1.5	8.7	1.5	8.1	
tPZL	1 GAB	P P	2.3	6.2	8.1	2.3	9.9	2.3	9.3	ns
tPHZ	GAR	В	3.5	8.2	10	3.5	12.2	3.5	11.6	200
tPLZ	GAB		2.8	7.2	9.5	2.8	12	2.8	11.3	ns

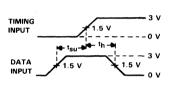
[†] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

[‡] These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

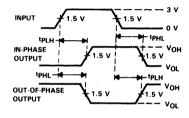


SWITCH POSITION TABLE

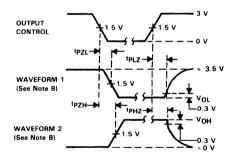
TEST	S1
tPLH	Open
tPHL	Open
^t PZH	Open
tPZL	Closed
t _{PHZ}	Open
^t PLZ	Closed



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0=50~\Omega$, $t_f=2.5$ ns, $t_f=2.5$ ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS



SN54BCT760, SN74BCT760 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

D3301, JULY 1989

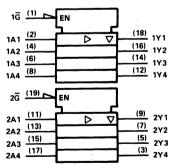
- Open-Collector Version of 'BCT244
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015
- Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT756 and 'BCT757, these devices provide the choice of selected combinations of inverting outputs, symmetrical \overline{G} (active-low output control) inputs, and complementary G and \overline{G} inputs.

The SN54BCT760 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT760 is characterized for operation from 0°C to 70°C.

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

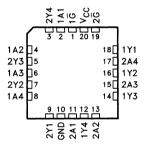
SN54BCT760 ... J PACKAGE SN74BCT760 ... DW OR N PACKAGE

(TOP VIEW)

1	O 20	П	V_{CC}
2	19		2Ğ
3	18	ם	1Y1
4	17		2A4
5	16		1Y2
6	15		2A3
7	14		1Y3
8	13		2A2
9	12		1Y4
10	11		2A1
	3 4 5 6 7 8	3 18 4 17 5 16 6 15 7 14 8 13 9 12	3 18 4 17 5 16 7 14 7 8 13 7 9 12 7

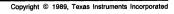
SN54BCT760 ... JK PACKAGE

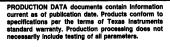
(TOP VIEW)



FUNCTION TABLE

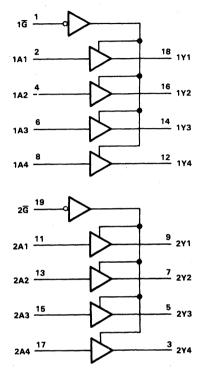
OUTPUT CONTROL G	DATA INPUT A	О UТР ИТ Ү
н	х	z
L	L	L
L	н	н







logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	0.5 V to 7 V
Input voltage, V _I (see Note 1)	0.5 V to 7 V
Input current, I	-30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	0.5 V to VCC
Current into any output in the low state: SN54BCT760	96 mA
SN74BCT760	128 mA
Operating free-air temperature range: SN54BCT760	-55°C to 125°C
SN74BCT760	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



NOTE 1: The negative input voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT760			SN74BCT760			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	J
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.8			0.8	٧
ΊΚ	Input clamp current			18			-18	mA
VOH	High-level output voltage			5.5	:		5.5	٧
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SI	154BCT76	0	SI	174BCT76	0	UNIT
PARAMETER		IESI CONDITIO	in 5	MIN	TYP†	MAX	MIN	TYP [†]	MAX	UNII
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA				-1.2			-1.2	٧
ЮН	$V_{CC} = 4.5 V,$	$V_{OH} = 5.5 V$				0.1			0.1	mA
VOL	$V_{CC} = 4.5 V,$	$I_{OL} = 48 \text{ mA}$			0.38	0.55				_ v
VOL	$V_{CC} = 4.5 V,$	IOL = 64 mA					0	0.42	0.55	
lı .	$V_{CC} = 5.5 V,$	$V_{ } = 5.5 V$				0.1			0.1	mA
lн	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$				20			20	μΑ
IIL	$V_{CC} = 5.5 V,$	$V_{I} = 0.5 V$				-1			-1	mA
Icc	V _{CC} = 5.5 V,	Outputs open	Outputs high		21	33		21	33	^
100	VCC = 5.5 V,	Outputs open	Outputs low		48	76		48	76	μΑ
Ci	$V_{CC} = 5 V$,	$V_{I} = 2.5 V or 0$.5 V		6			6		pF
Co	$V_{CC} = 5 V$,	$V_1 = 2.5 V or 0$.5 V		10			10		pF

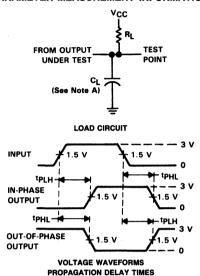
[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

'BCT760 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R _L	V _{CC} = 5 V, C _L = 50 pF, R _L = 500 Ω, T _A = 25°C			$egin{array}{ll} V_{CC} = 4.5 \ V \ to 5.5 \ V, \\ C_L = 50 \ pF, \\ R_L = 500 \ \Omega, \\ T_A = MIN \ to \ MAX^{\ddagger} \end{array}$				
			,	BCT760		SN54	4BCT760	SN74B	CT760		
	1		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _{PLH}	Any A	v	6.3	8	9.5	6.3	. 11.1	6.3	10	ns	
tPHL	1 71117	'	2.1	4.3	6.5	2.1	7.7	2.1	7.2	.,,5	
tPLH	Any G	· ·	8.6	13	15.2	8.6	18.7	8.6	17.5	ns	
tPHL	1 / " " "	'	3.2	6.2	8.9	3.2	10.4	3.2	9.9		

[‡] For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.





NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O}=50~\Omega$, $t_{r}\leq$ 2.5 ns, $t_{f}\leq$ 2.5 ns.

C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

SN54BCT2240, SN74BCT2240 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

D3057, SEPTEMBER 1988—REVISED JULY 1989

- BiCMOS Design Substantially Reduces Standby Current
- Output Ports have Equivalent 33-Ω Series Resistors so No External Resistors are Required
- ESD Protection Exceeds 2000 V, MIL-STD-883C, Method 3015
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

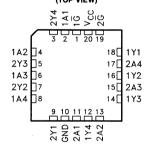
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT2241 and 'BCT2244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical \overline{G} (active-low output control) inputs, and complementary G and \overline{G} inputs. These devices feature high fan-out and improved fan-in.

The SN54BCT2240 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT2240 is characterized for operation from 0°C to 70°C.

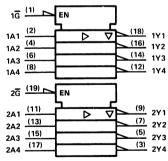
SN54BCT2240 ... J PACKAGE SN74BCT2240 ... DW OR N PACKAGE (TOP VIEW)

20 V_{CC} 1G F 1A1 [19 7 2 G 2Y4 [18 1Y1 1 A 2 □ 4 17 7 2 4 2Y3 🗆 5 16 1Y2 1A3 15 2A3 2Y2 7 14 T 1 Y 3 1 A 4 Π 8 13 7 2A2 2Y1 🗖 12 1Y4 GND [72A1

SN54BCT2240 ... FK PACKAGE (TOP VIEW)



logic symbol†

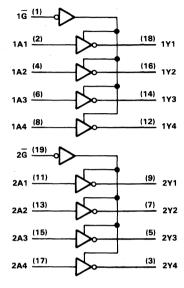


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

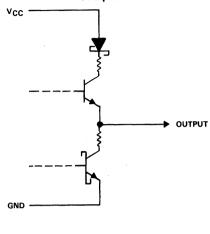


SN54BCT2240, SN74BCT2240 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

logic diagram (positive logic)



schematic of each output



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, VCC	−0.5 V to 7 V
Input voltage (see Note 1)	-0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	−0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to VCC
Input clamp current	−30 mA
Current into any output in the low state: SN54BCT2240	96 mA
SN74BCT2240	128 mA
Operating free-air temperature range: SN54BCT2240	-55°C to 125°C
SN74BCT2240	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54BCT2240			SN	UNIT			
		MIN	NOM	MAX	MIN	NOM	MAX	0	
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧	
VIH	High-level input voltage	2			2			٧	
VIL	Low-level input voltage			0.8			0.8	٧	
ΊK	Input clamp current			-18			-18	mA	
ЮН	High-level output current			-12			-12	mA	
IOL	Low-level output current			12			12	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	



NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.

SN54BCT2240, SN74BCT2240 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	18	154BCT22	40	SN	UNIT		
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	O.U.
VIK	$V_{CC} = 4.5 V,$	$I_{OH} = -18 \text{ mA}$			-1.2			-1.2	٧
Voн	V _{CC} = 4.5 V	IOH = -1 mA	2.4	3.3		2.4	3.3		V
	100	I _{OH} = -12 mA	2	3.2		2	3.2		
VOL	V _{CC} = 4.5 V	IOL = 1 mA		0.15	0.5		0.15	0.5	V
.02	100	I _{OL} = 12 mA		0.35	0.8		0.35	0.8	
lj	$V_{CC} = 5.5 V,$	$V_I = 5.5 V$			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
IL	$V_{CC} = 5.5 V$,	V _I = 0.5 V			-1			-1	mA
lozh	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			50			50	μΑ
IOZL	$V_{CC} = 5.5 V,$	$V_{O} = 0.5 V$			-50			50	μΑ
los‡	$V_{CC} = 5.5 V,$	V _O = 0	-100		-225	-100		-225	mA
ICCH				19	32		19	32	
ICCL	$V_{CC} = 5.5 V,$	Outputs open		46	76		46	76	mA
Iccz	1	-		6	8		6	8	

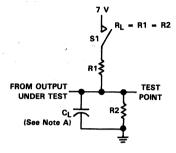
[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _i R:	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_{A} = 25^{\circ}C$			$V_{CC}=4.5$ V to 5.5 V, $C_L=50$ pF, $R1=500$ Ω , $R2=500$ Ω , $T_{A}=MIN$ to MAX				
			,	'BCT2240		SN54BCT2240		SN74BCT2240			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
tPLH	Α	Y	0.5	3.4	4.8	0.5	6.3	0.5	5.7	ns	
t _{PHL}	,,	·	0.5	2.8	4	0.5	4.6	0.5	4.4		
tPZH	G ·	Y	2.6	6.2	8.2	2.6	10.1	2.6	9.3	ns	
tPZL		, i	4.3	8.8	10.9	4.3	12.9	4.3	12.4		
tPHZ	G	Y	2	5.3	7.1	2	9.2	2	8.7	ns	
tPLZ		,	2.2	6.7	8.5	2.2	12.2	2.2	10.6		



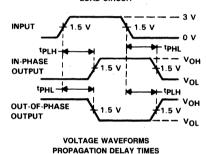
[‡] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

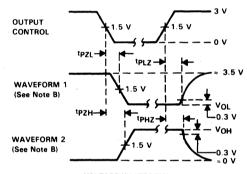


SWITCH POSITION TABLE

TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed

LOAD CIRCUIT





VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by the generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega,~t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

SN54BCT2241, SN74BCT2241 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

D3057, SEPTEMBER 1988-REVISED MAY 1989

- BiCMOS Design Substantially Reduces Standby Current
- Output Ports have Equivalent 33-Ω Series Resistors so No External Resistors are Required
- ESD Protection Exceeds 2000 V
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

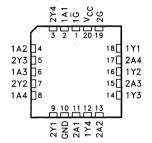
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT2240 and 'BCT2244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical \overline{G} (active-low output control) inputs, and complementary G and \overline{G} inputs. These devices feature high fan-out and improved fan-in.

The SN54BCT2241 is characterized for operation over the full military temperature range of -55° C to 125 $^{\circ}$ C. The SN74BCT2241 is characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.

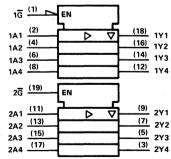
SN54BCT2241 ... J PACKAGE SN74BCT2241 ... DW OR N PACKAGE

(TOP VIEW) 1G 🗆 1 A 1 ∏2 19 7 2G 2Y4 T3 18∏ 1Y1 1A2 Π 4 17 2A4 2Y3 🗆 5 16 1Y2 15 2A3 1A3 ∏6 2Y2 | 7 14 1 1 Y 3 1А4 Пв 13 2A2 2Y1 [12 1Y4 GND T10 11 D 2A1

SN54BCT2241 ... FK PACKAGE (TOP VIEW)



logic symbol†

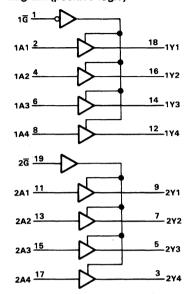


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

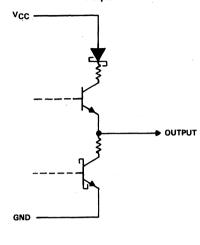


SN54BCT2241, SN74BCT2241 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

logic diagram (positive logic)



schematic of each output



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, VCC	0.5 V to 7 V
Input voltage	−0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to VCC
Operating free-air temperature ranges: SN54BCT2241	-55°C to 125°C
SN74BCT2241	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN	SN	UNIT				
		MIN	NOM	MAX	MIN	NOM	MAX	J
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.8			0.8	٧
ΊΚ	Input clamp current			-18			-18	mA
ЮН	High-level output current			-12			-12	mA
lOL	Low-level output current			12			12	mA
TA	Operating free-air temperature	-55		125	0		70	٠c



SN54BCT2241, SN74BCT2241 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		SN	SN54BCT2241			SN74BCT2241			
		TEST CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	$I_{OH} = -18 \text{ mA}$			-1.2			-1.2	V
Voh	V _{CC} = 4.5 V	IOH = −1 mA	2.4	3.3		2.4	3.3		V
*CC 4.5 *	$I_{OH} = -12 \text{ mA}$	2	3.2					•	
VOL	V _{CC} = 4.5 V	IOL = -12 mA		0.38	0.55				V
100	IOL = 12 mA					0.42	0.55	•	
l _l	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
lıL.	$V_{CC} = 5.5 V,$	V _I = 0.5 V			-1			-1	mA
lozh	$V_{CC} = 5.5 V,$	V _O = 2.7 V			50			50	μΑ
lozL	$V_{CC} = 5.5 V,$	V _O = 0.5 V			50			-50	μΑ
los‡	$V_{CC} = 5.5 V,$	V _O = 0	-100		-225	-100		-225	mA
ІССН				23	37		23	37	
ICCL ICCL	$V_{CC} = 5.5 V,$	Outputs open		37	76		37	76	mA
ICCZ				6	9		6	9	

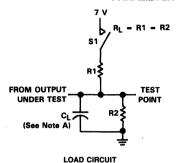
 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25°C.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}\text{C}$			$V_{CC}=4.5$ V to 5.5 V, $C_L=50$ pF, R1 = 500 Ω , R2 = 500 Ω , $T_A=MIN$ to MAX				
,			'[3CT2241		SN54E	BCT2241	SN74B	CT2241		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
tPLH	A	Y	1.1	3	4.4	1.1	5.1	1.1	4.9	ns	
tPHL	1 ``	·	2.9	4.9	6.6	2.9	7.2	2.9	6.9		
^t PZH	G or \overline{G}	Υ	2.7	6	7.8	2.7	9.4	2.7	8.9	ns	
tPZL	1	,	4.1	7.7	9.4	4.1	10.9	4.1	10.3		
tPHZ	G or \overline{G}	Υ	2.5	5.2	7.2	2.5	9.7	2.5	8.7	ns	
tPLZ]	'	3.2	7.1	9.5	3.2	12.9	3.2	11.3	.,.	

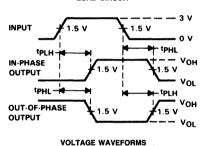


[‡] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

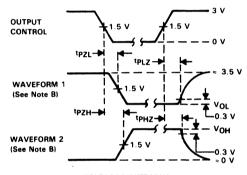


TEST S1

TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed



PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES. THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by the generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

SN54BCT2244, SN74BCT2244 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

D3057, SEPTEMBER 1988-REVISED AUGUST 1989

- BiCMOS Design Substantially Reduces Standby Current
- Output Ports have Equivalent 33-Ω Series Resistors so No External Resistors are Required
- ESD Protection Exceeds 2000 V, MIL-STD-883C, Method 3015
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT2240 and 'BCT2241, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{\mathbf{G}}$ (active-low input control) inputs, and complementary \mathbf{G} and $\overline{\mathbf{G}}$ inputs. These devices feature high fan-out and improved fan-in.

The SN54BCT2244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT2244 is characterized for operation from 0°C to 70°C.

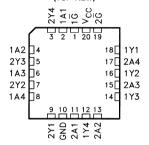
FUNCTION TABLE (each buffer)

INP	UTS	OUTPUT
G	A	Y
Н	Х	Z
L	L	L
L	Н	н

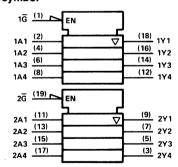
SN54BCT2244 ... J PACKAGE SN74BCT2244 ... DW OR N PACKAGE

(TOP VIEW)		
1 G [1	∪20 V _{CC}
1A1 [2	19∏ 2Ġ
2Y4 🗌	3	18 1Y1
1 A 2 🗌	4	17 2A4
2Y3 🗌	5	16 1Y2
1 A 3 🗌	6	15 2A3
2Y2 🗌	7	14 🛮 1Y3
1A4 🗌	8	13 2A2
2Y1 [9	12 1Y4
GND [10	11 2A1

SN54BCT2244 ... FK PACKAGE (TOP VIEW)



logic symbol†

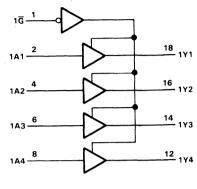


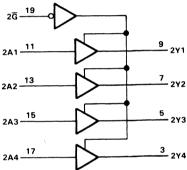
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



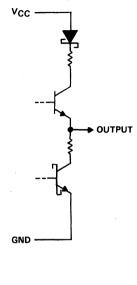
SN54BCT2244, SN74BCT2244 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

logic diagram (positive logic)





schematic of each output



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, VCC	. −0.5 V to 7 V
Input voltage (see Note 1)	. −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to V _C C
Input clamp current	−30 mA
Current into any output in the low state: SN54BCT2244	96 mA
SN74BCT2244	128 mA
Operating free-air temperature range: SN54BCT2244	-55°C to 125°C
SN74BCT2244	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.



SN54BCT2244, SN74BCT2244 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

3		SN54BCT2244 SN74BCT2244			UNIT			
		MIN	NOM	MAX	MIN	NOM	MAX	0
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
lικ	Input clamp current			-18			-18	mA
ЮН	High-level output current			-12			-12	mA
lOL	Low-level output current			12			12	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN	I54BCT22	44	SN	74BCT22	44	UNIT
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	0
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	٧
Voн	V _{CC} = 4.5 V	I _{OH} = −1 mA	2.4			2.4			V
10,1	.00	IOH = -12 mA	2			2			·
VOL	V _{CC} = 4.5 V	I _{OL} = 1 mA		0.15	0.5		0.15	0.5	V
102	100	I _{OL} = 12 mA		0.35	0.8		0.35	0.8	
11	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1			0.1	mA
ΙΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
ΊL	$V_{CC} = 5.5 V$	V _I = 0.5 V			-1			-1	mA
lozh	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			50			50	μΑ
lOZL	$V_{CC} = 5.5 V,$	$V_{O} = 0.5 V$			-50			-50	μΑ
los‡	$V_{CC} = 5.5 V$	V _O = 0	-100		-225	-100		- 225	mA
ICCH				23	37		23	37	
CCL	$V_{CC} = 5.5 V,$	Outputs open		53	77		53	77	mA
Iccz				6.5	10		6.5	10	
Ci	$V_{CC} = 5 V$,	V _I = 2.5 V or 0.5 V		6			6		pF
Co	$V_{CC} = 5 V$,	V _O = 2.5V or 0.5 V		11			11		Ρ.

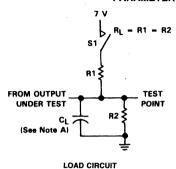
[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _I R:	CC = 5 V L = 50 pl I = 500 (2 = 500 (A = 25°C	=, l, l,		V _{CC} = 4.5 C _L = R1 = 1 R2 = 1 T _A = MII	50 pF, 500 Ω, 500 Ω,		UNIT
			,	BCT2244		SN54	BCT2244	SN74	BCT2244	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	Α	Y	0.5	3	4.4	0.5	5.2	0.5	4.9	ns
tPHL	, ,	·	1.6	4.6	6.3	1.6	7.1	1.6	6.7	
tPZH	G	Υ	2.4	6.1	7.7	2.4	9.1	2.4	8.7	ns
^t PZL	_	,	3.9	7.6	9.4	3.9	10.8	3.9	10.4	
tPHZ	G	Y	1.7	5.2	6.9	1.7	8.1	1.7	7.8	ns
tPLZ	1	, i	2.8	6.5	8.3	2.8	10.9	2.8	9.8]



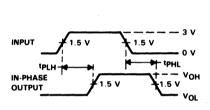
[‡] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

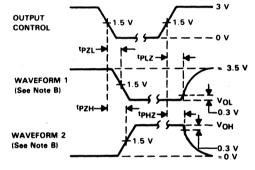


SWITCH PUSHTON	I I ABLE

TEST	S1
tPLH	Open
t _{PHL}	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by the generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

SN74BCT2827A, SN74BCT2828A 10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE OUTPUTS

D2977, APRIL 1987-REVISED AUGUST 1989

BiCMOS Design Substantially Reduces Standby Current

- 25-Ω Series Resistors at Outputs Significantly Reduce Overshoot and Undershoot
- Specifically Designed to Drive MOS DRAMs
- 3-State Outputs
- Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)
- Power-Up High-Impedance State
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic DIPs

description

These 10-bit buffers and bus drivers are specifically designed to drive the capacitive input characteristics of MOS DRAMs. They provide high-performance bus interface for wide data paths or buses carrying parity.

The three-state control gate is a 2-input positive NOR gate so if either \$\overline{G}\$1 or \$\overline{G}\$2 is high, all 10 outputs are in the high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down.

The SN74BCT2827A provides true data and the SN74BCT2828A provides inverted data at the outputs.

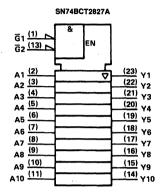
These devices are characterized for operation from 0°C to 70°C.

OW OR NT PACKAGE (TOP VIEW) G1 1 24 V_C A1 2 23 Y1

GIL	ľ	\cup	24	μ	v _{CC}
A1 []2		23	П	Y1
A2 [3		22		Y2
A3 [4		21		Y3
A4 [5		20		Y4
A5 [6		19		Y5
A6 [7		18		Y6
A7 [8		17		Y7
A8 [9		16		Y8
A9 [10		15		Y9
A10[11		14		Y10
GND [12		13		G2

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logic symbols†

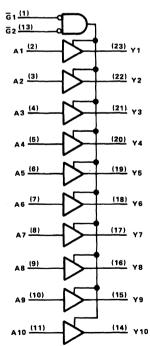


A3 (4) (21) Y3 A4 (5) (20) Y4 A5 (6) (19) Y5 A6 (7) (18) A7 (8) (17) Y7 A8 (9) (16) Y8		SN74B	CT2828A	١	
A2 (3) (22) Y2 A3 (4) (21) Y3 A4 (5) (20) Y4 A5 (6) (19) Y5 A6 (7) (18) Y6 A7 (8) (17) Y7 A8 (9) (16) Y8	$\overline{G}_1 \xrightarrow{(1)}$ $\overline{G}_2 \xrightarrow{(13)}$	&	EN		
A10 (11) (14) Y10	A2 (3) A3 (4) A4 (5) A5 (6) A6 (7) A7 (8) A8 (9) A9 (10)			(22) (21) (20) (19) (18) (17) (16) (15)	Y2 Y3 Y4 Y5 Y6 Y7

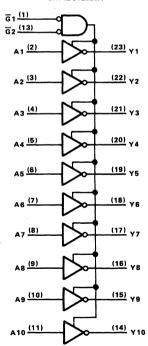
[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

SN74BCT2827A



SN74BCT2828A





SN74BCT2827A 10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		. 7V
Input voltage		
Voltage applied to a disabled 3-state output		5.5 V
Operating free-air temperature range	0°C to	70°C
Storage temperature range	-65°C to	150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	٧
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	٧
ЮН	High-level output current			-1	mA
lOL	Low-level output current			12	mA
TA	Operating free-air temperature	0		. 70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
VIL	$V_{CC} = 4.5 V,$	$I_{\parallel} = -18 \text{ mA}$			-1.2	٧
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	IOH = −1 mA	V _{CC} -2			٧
VOL	$V_{CC} = 4.5 V_{r}$	I _{OL} = 1 mA		0.15	0.5	V
100	$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.35	0.8	·
IOZH	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			20	μΑ
IOZL	$V_{CC} = 5.5 V,$	$V_{O} = 0.4 \text{ V}$			-20	μΑ
loL	$V_{CC} = 4.5 V,$	$V_O = 2 V$	50			mA
ЮН	$V_{CC} = 4.5 V$,	$V_0 = 2 V$	-35			mA
l ₁	$V_{CC} = 5.5 V$	V _I = 7 V			0.1	mA
IH	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20	μΑ
IIL	V _{CC} = 5.5 V,	$V_{ } = 0.4 \text{ V}$			-0.2	mA
10‡	$V_{CC} = 5.5 V,$	$V_{O} = 2.25 \text{ V}$	-30		-112	mA
ICCL	V _{CC} = 5.5 V,	Outputs open		28	40	mA
lccz	V _{CC} = 5.5 V,	Outputs open		4.5	8	

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5$ V, $T_{A} = 25$ °C.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2	CC = 5 V, = 50 pF, = 500 Ω = 500 Ω A = 25°C	,	C _L = R1 = R2 =	5 V to 5.5 V, 50 pF, 500 Ω, 500 Ω, IN to MAX	UNIT
			MIN	TYP	MAX	MIN	MAX	
tPLH	Α	Y		4	6	2	7	ns
tPHL				6	8	2	9	
tPZH	G	Y		8	10	4	13	ns
tPZL				11	14	6	17	
tPHZ	G	Y		8	12	4	15	ns
tPLZ	_	·		7	11	3	13	



[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		7 V
Input voltage		
Voltage applied to a disabled 3-state output	8	5.5 V
Operating free-air temperature range		
Storage temperature range	-65°C to 19	50°C

recommended operating conditions

	,	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	٧
VIH	High-level input voltage	2			٧
VIL	Low-level input voltage			0.8	٧
ЮН	High-level output current			-1	mA
lol	Low-level output current			12	mA
TA	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vik	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	IOH = -1 mA	V _{CC} -2			٧
VOL	$V_{CC} = 4.5 V$	IOL = 1 mA		0.15	0.5	v
•OL	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.35	0.8	. •
lozh	$V_{CC} = 5.5 V$,	V _O = 2.7 V			20	μΑ
lozL	$V_{CC} = 5.5 V$,	V _O = 0.4 V			-20	μΑ
lOL	$V_{CC} = 4.5 V,$	V _O = 2 V	50			mA
ЮН	$V_{CC} = 4.5 V,$	V _O = 2 V	-35			mA
lj .	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1	mA
ЧН	V _C C = 5.5 V,	V _I = 2.7 V			20	μΑ
liL .	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.2	mA
10‡	$V_{CC} = 5.5 V,$	V _O = 2.25 V	-30		-112	mA
ICCL	VCC = 5.5 V,	Outputs open		28	40	mA
ICCZ	$V_{CC} = 5.5 V$,	Outputs open		3.5	6	

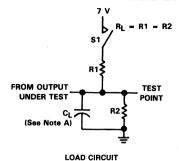
[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _I R·	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C		CL = R1 = R2 =	5 V to 5.5 V, 50 pF, 500 Ω, 500 Ω, N to MAX	UNIT
		,	MIN	TYP	MAX	MIN	MAX	
tPLH	Α	Υ		5	7	2	. 8	ns
t _{PHL}		·		5	7	2	8	
t _{PZH}	G	Y		8	11	4	12	ns
tPZL	-		,	10	14	6	16	
t _{PHZ}	G	Y		10	14	4	16	ns
tPLZ				8	12	3	14	



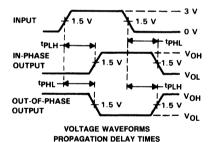
[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

PARAMETER MEASUREMENT INFORMATION



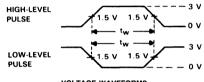
TIMING 11.5 V 1.5
INPUT

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

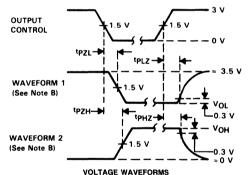


SWITCH POSITION TABLE

TEST	S1
t _{PLH}	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed



VOLTAGE WAVEFORMS PULSE DURATIONS



ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z₀ = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1. SWITCHING CHARACTERISTICS



SN74BCT29827A, SN74BCT29828A 10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

D2977 APRIL 1987—REVISED JULY 1989

- BiCMOS Design Substantially Reduces Standby Current
- Functionally Equivalent to Am29827, Am29828, SN74ALS29827, and SN74ALS29828
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce DC Loading
- Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)
- Power-Up High-Impedance State
- Package Options Include Plastic and Ceramic DIPs
- BiCMOS Process with TTL Inputs and Outputs
- Dependable Texas Instruments Quality and Reliability

description

These 10-bit buffers and bus drivers provide high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input positive NOR gate so if either \$\overline{G}\$1 or \$\overline{G}\$2 is high, all 10 outputs are in the high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down.

The SN74BCT29827A provides true data and the SN74BCT29828A provides inverted data at the outputs.

The SN74BCT29827A and SN74BCT29828A are characterized for operation from 0°C to 70°C.

(TOP VIEW) 24 V_{CC} A1 🗖 2 23 Y1 A2 ∏3 22 Y2 A3 []4 21 Y3 A4 ∏5 20 NY4 19 Y5 A5 ∏6 A6 ∏7 18 Y6 ∆7 П8 17 Y Y7 АВ П9 16 Y8 15 Y9 A9 ∏10

14 TY10

A10 ∏11

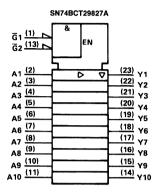
GND ∏12

DW OR NT PACKAGE

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



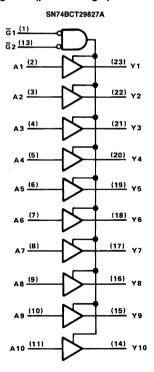
logic symbols†



SN74BCT29828A									
$\overline{G}_1 \frac{(1)}{G_2} \nearrow$	&	EN							
A1 (2) (3) (4) (5) (6) (6) (7) (8) (8) (9) (10)		> √	(23) (22) (21) (20) (19) (18) (17) (16) (15)	Y2 Y3 Y4 Y5 Y6 Y7 Y8					
A10 (11)			(14)	Y 10					

[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



SN74BCT29828A G1 (1) G2 (13) (23) Y1 A1 (2) (22) Y2 A2 (3) (21) Y3 A3 (4) (<u>20)</u> Y4 A4 (5) (19) Y5 (18) Y6 (17) Y7 A7 (8) (16) Y8 (15) Y9 A9 (10) (14) Y10



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}		. 7V
Input voltage (all inputs and I/O ports)		5.5 V
Operating free-air temperature range	0°C to	70°C
Storage temperature range	-65°C to	150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	٧
VIH	High-level input voltage	2			٧
VIL	Low-level input voltage			0.8	V
ЮН	High-level output current			-24	mA
IOL	Low-level output current			48	mÁ
TA	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	MIN	TYP‡	MAX	UNIT
VIK	V _{CC} = MIN,	$I_{\parallel} = -18 \text{ mA}$			-1.2	٧
Voн	V _{CC} = MIN	$I_{OH} = -15 \text{ mA}$	2.4			V
	100	I _{OH} = -24 mA	2			•
VOL	$V_{CC} = MIN,$	$I_{OL} = 48 \text{ mA}$		0.35	0.5	٧
lozh	$V_{CC} = MAX,$	$V_O = 2.7 V$			20	μΑ
lozl	$V_{CC} = MAX,$	$V_{O} = 0.4 \text{ V}$			-20	μΑ
lj	$V_{CC} = MAX,$	V _I = 5.5 V			0.1	mA
IH	$V_{CC} = MAX,$	$V_{ } = 2.7 V$			20	μΑ
IJĹ	$V_{CC} = MAX,$	V _I = 0.4 V			-0.2	mA
los§	$V_{CC} = MAX,$	$V_{O} = 0$	-75		-250	mA
ICCL	$V_{CC} = MAX,$	Outputs open		28	40	mA
Iccz	$V_{CC} = MAX,$	Outputs open		3.5	6	mA

[†] For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$\begin{array}{cccccccccccccccccccccccccccccccccccc$		50 pF, 500 Ω, 500 Ω,	UNIT		
			MIN	TYP	MAX	MIN	MAX	
tPLH	Α	Y	1	3.5	6	1	7	ns
tPHL	,,		1	5	7	· 1	9	
tPZH	G	Υ	2	7	10	2	12	ns
tPZL		·	2	10	13	2	15	
t _{PHZ}	G	Υ	2	. 7	10	2	12	ns
t _{PLZ}	-		2	7	10	2	12	



[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time and duration of the short circuit should not exceed 1 second.

SN74BCT29828A 10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	7 V
Input voltage (all inputs and I/O ports)	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	65°C to 150°C

recommended operating conditions

	•	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	٧
VIH	High-level input voltage	2			٧
VIL	Low-level input voltage			0.8	٧
ЮН	High-level output current			-24	mA
lOL	Low-level output current			48	mA
TA	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP [‡]	MAX	UNIT
VIK	V _{CC} = MIN,	$I_{\parallel} = -18 \text{ mA}$			-1.2	٧
Voн	V _{CC} = MIN	$I_{OH} = -15 \text{mA}$	2.4			V
-011	100	$I_{OH} = -24 \text{mA}$	2			
VOL	V _{CC} = MIN,	$I_{OL} = 48 \text{mA}$		0.35	0.5	٧
lozh	$V_{CC} = MAX$,	$V_{O} = 2.7 \text{ V}$			20	μΑ
lozL	$V_{CC} = MAX,$	$V_O = 0.4 V$			-20	μΑ
11	$V_{CC} = MAX,$	$V_{I} = 5.5 V$			0.1	mA
ΊΗ	$V_{CC} = MAX,$	$V_{\parallel} = 2.7 \text{ V}$			20	μΑ
ΙΙL	$V_{CC} = MAX,$	$V_{\parallel} = 0.4 \text{ V}$			-0.2	mA
los§	$V_{CC} = MAX,$	$V_O = 0$	-75		-250	mA
ICCL	$V_{CC} = MAX,$	Outputs open		28	40	mA
Iccz	$V_{CC} = MAX,$	Outputs open		3.5	6.5	mA

[†] For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

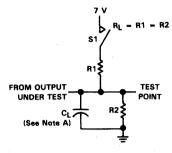
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _I R1 R2	CC = 5 V, CC = 50 pF $CC = 500 \Omega$ $CC = 500 \Omega$ $CC = 500 \Omega$ $CC = 500 \Omega$, ,	CL = R1 = R2 =	5 V to 5.5 V, 50 pF, 500 Ω , 500 Ω , IN to MAX	UNIT
		}	MIN	TYP	MAX	MIN	MAX	
tPLH	Α	Y	1	3.5	6	1	7	ns
tPHL			1	3.5	6	1	7	
^t PZH	. <u>G</u>	Y	2	7	9	2	11	ns
[†] PZL			2	9	13	2	15	
^t PHZ	G	Y	2	6	9	2	10	ns
[†] PLZ			2	6	10	2	11	



[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time and duration of the short circuit should not exceed 1 second.

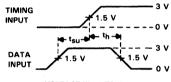
PARAMETER MEASUREMENT INFORMATION



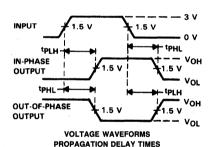
SWITCH POSITION TABLE

TEST	S1			
tPLH	Open			
tPHL	Open			
tPZH	Open			
tPZL	Closed			
tPHZ	Open			
tPLZ	Closed			



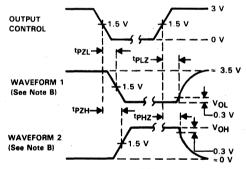


VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



HIGH-LEVEL PULSE 1.5 V 1.5 V 0 V 1.5 V 1.5 V 1.5 V 1.5 V 0 V

VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.

FIGURE 1. SWITCHING CHARACTERISTICS

SN74BCT29833, SN74BCT29834 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

D3031, SEPTEMBER 1987-REVISED JULY 1989

- BiCMOS Process with TTL Inputs and Outputs
- BiCMOS Design Reduces Standby Current
- Flow-Through Pinout (All Inputs on Opposite Side from Outputs)
- Functionally Equivalent to AMD Am29833, Am29834, 'ALS29833, and 'ALS29834
- High-Speed Bus Transceivers with Parity Generator/Checker
- Parity Error Flag with Open-Collector Output
- Has a Register for Storage of the Parity Error Flag
- Choice of True ('BCT29833) or Inverting ('BCT29834) Logic
- Package Options Include Plastic "Small Outline" Package and Standard Plastic 300-mil DIPs

description

The SN74BCT29833 and SN74BCT29834 are 8-bit to 9-bit parity transceivers designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the $\overline{\text{ERR}}$ output will indicate whether or not an error in the B data has occurred. The output enable inputs $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd output (PARITY) and monitors the parity of the I/O ports with an open-collector parity error flag (ERR). ERR is clocked into the register on the rising edge of the CLK input. The error flag register is cleared with a low pulse on the CLR input. When both OEA and OEB are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The SN74BCT29833 and SN74BCT29834 are characterized for operation from 0°C to 70°C.

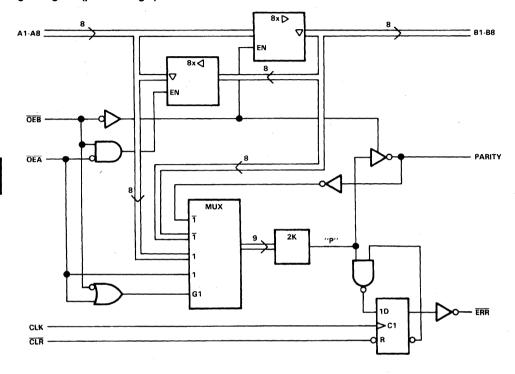
SN74BCT' ... DW OR NT PACKAGE (TOP VIEW)

OEA [1	U24] v _{cc}
A1 🗆 2	23] B1
A2 🛚 3	22] B2
A3 🛮 4	21	B3
A4 ∏5	20] B4
A5 ∏6	19] B5
A6 □ 7	18] B6
A7 🗌 8	17] B7
A8 ∏9	16] B8
ERR []1	0 15] PARITY
CLR [1	1 14	OEB
GND 1	2 13] CLK

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logic diagram (positive logic)



FUNCTION TABLE

			INPUTS				OU	TPUT & I/O		
OEB	OEA	CLR	CLK	Ai Σ of H's	Bi [†] Σ of H's	Α	В	PARITY	ERR‡	FUNCTION
L	Н	х	х	Odd Even	NA	NA	Α	L H	NA	A Data to B Bus and Generate Parity
н	L	Н	1	NA	Odd Even	В	NA	NA	H L	B Data to A Bus and Check Parity
X	Х	L	Х	Х	X	X	NA	NA	Н	Clear Error Flag Register
н	Н	ILI	No↑ No↑	X X Odd Even	х	Z	z	Z	NC H H L	Isolation [§]
L	L	х	х	Odd Even	NA	NA	Α	H L	NA	A Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care

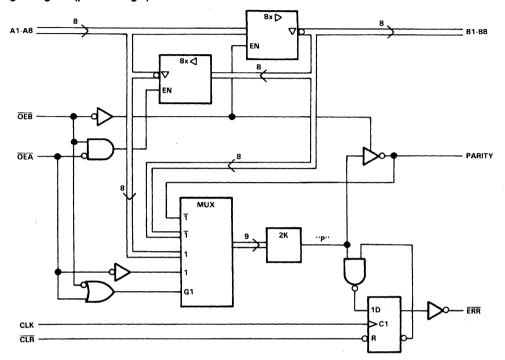
†Summation of high-level inputs includes PARITY along with Bi inputs.

‡Output states shown assume the ERR output was previously high.

§In this mode, the ERR output, when clocked, shows inverted parity of the A bus.



logic diagram (positive logic)



FUNCTION TABLE

			INPUTS				OU	TPUT & I/O		
OEB	OEA	CLR	CLK	Ai Σ of H's	Bi [†] Σ of L's	А	В	PARITY	ERR‡	FUNCTION
L	н	х	х	Odd Even	NA	. NA	Ā	H L	NA	Ā Data to B Bus and Generate Parity
н	L	н	1	NA	Odd Even	B	NA	NA	H	B Data to A Bus and Check Parity
Х	Х	L	Х	Х	Х	Х	NA	NA	Н	Clear Error Flag Register
Н	н	H L H	No ↑ No ↑	X X Odd Even	х	Z	Z	Z	NC H L H	Isolation [§]
L	L	х	х	Odd Even	NA	NA	Ā	L H	NA	A Data to B Bus and Generate Inverted Parity

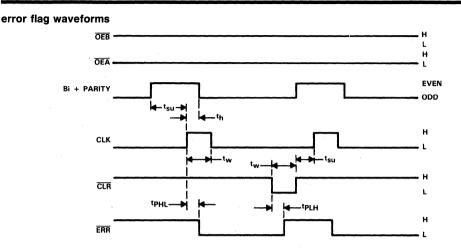
NA = Not applicable, NC = No change, X = Don't care



[†]Summation of low-level inputs includes PARITY along with Bi inputs.

[‡]Output states shown assume the ERR output was previously high.

[§]In this mode, the ERR output, when clocked, shows noninverted parity of the A bus.



ERROR FLAG FUNCTION TABLE

INP	UTS	INTERNAL TO DEVICE	OUTPUT PRE-STATE OUTPUT		FUNCTION
CLR	CLK	POINT "P"	ERR _{n-1}	ERR	
H H H	†	H X L	H L X	H L L	SAMPLE
L	Х	×	×	Н	CLEAR

ERR_{n-1} represents the state of the ERR output before any changes at CLR, CLK, or point "P".

SN74BCT29833, SN74BCT29834 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	٧
Input voltage	٧
Voltage applied to a disabled I/O port	V
Operating free-air temperature range	
Storage temperature range – 65°C to 150°	°C

recommended operating conditions

				MIN	NOM	MAX	UNIT	
Vcc	Supply voltage			4.5	5	5.5	٧	
VIH	High-level input voltage	-		2			V	
VIL	Low-level input voltage					0.8	V	
Vон						2.4	V	
ЮН	High-level output current					-24	mA	
lOL	Low-level output current					48	mA	
		CLK high		10				
tw	Pulse duration	CLK low		10			ns	
		CLR low		10				
t _{su}	Setup time before CLK ↑	Bi and PARITY		12			ns	
'Su	Comp and Soloio Sait	CLR inactive		12			1	
th	Hold time, Bi and PARITY after CLK ↑			0			ns	
TA	Operating free-air temperature			0		.70	°C	

electrical characteristics over recommended operating free-air temperature and supply voltage range (unless otherwise noted)

1	PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	$I_{\parallel} = -18 \text{mA}$			-1.2	٧
Vон	All inputs/outputs	V _{CC} = 4.5 V	IOH = -15 mA	2.4			V
exce	except ERR	100	IOH = -24 mA	2			
ЮН	ERR	$V_{CC} = 4.5 V$	$V_{OH} = 2.4 \text{ V}$			20	μΑ
VOL		$V_{CC} = 4.5 V,$	$I_{OL} = 48 \text{ mA}$		0.35	0.5	V
ij		$V_{CC} = 5.5 V,$	$V_{ } = 5.5 V$			0.1	mA
I _{IH} ‡		$V_{CC} = 5.5 V$,	V _I = 2.7 V			20	μΑ
I _{IL} ‡	Data	$V_{CC} = 5.5 V_1$	V _I = 0.4 V			-0.2	mA
·IL.	Control	100 0.0 1,	1 0			-0.75	
los§		$V_{CC} = 5.5 V,$	$V_O = 0$	-75		-250	mA
ICCL		$V_{CC} = 5.5 V,$	All Outputs Open		55	80	mA
ICCZ		100 3.5 1,	, iii Galpato Opon		30	45	

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25°C.



[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed 1 second.

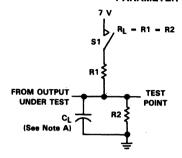
SN74BCT29833 switching characteristics (see Figure 1)

PARAMETER			$\begin{array}{c} \text{VCC} = 5 \text{ V,} \\ \text{C}_{L} = 50 \text{ pF,} \\ \text{R1} = 500 \ \Omega, \\ \text{R2} = 500 \ \Omega, \\ \text{TA} = 25^{\circ}\text{C} \end{array}$			V _{CC} = 4 C _L R1 = R2 = T _A = I	UNIT	
			MIN	TYP	MAX	MIN	MAX	
tPLH .	A or B	B or A	1	5	7	1	8	ns
tPHL			1.5	5	8	1.5	10	
tPLH	Α	PARITY	1.5	7	9	1.5	11	ns
tPHL telephone			1.5	10	13	1.5	15	
tpzH	OEA or OEB	A or B	2	11	15	2	19	ns
tPZL	02.10.022		2	13	17	2	21	1 "
tPHZ	OEA or OEB	A or B	2	8	11	2	15	ns
tPLZ	020.022	7.0.2	2	10	14	2	17	1 "
t _{PHL}	CLK	ERR	1.5	7	10	1.5	12	ns
tPLH	CLR	ERR	1.5	13	. 17	1.5	20	ns
t _{PLH}	ŌĒĀ	PARITY	1.5	10	13	1.5	15	ns
t _{PHL}	J	IAIIII	1.5	10	13	1.5	15	

SN74BCT29834 switching characteristics (see Figure 1)

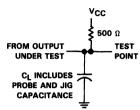
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C Fi	VCC = 5 \ CL = 50 pl R1 = 500 s R2 = 500 s TA = 25°C	F, D, D,	CL : R1 : R2 : T _A = I	1.5 V to 5.5 V, = 50 pF, = 500 Ω, = 500 Ω, MIN to MAX	UNIT
	 		MIN	TYP 5	MAX 7	MIN 1	MAX 8	
tPLH ·	A or B	B or A						ns
tPHL			1.5	4	6	1.5	7	
tPLH telephone	_ A	PARITY	1.5	10	13	1.5	15	ns
tPHL			1.5	8	10	1.5	15	
^t PZH	OEA or OEB	A or B	2	11	15	2	19	ns
tPZL		7.075	2	15	19	2	21	
tPHZ	OEA or OEB	A or B	2	8	11	2	15	ns
tPLZ	7 02/10/025	7.0.2	2	13	17	2	21	"
tPHL	CLK	ERR	1.5	7	10	1.5	12	ns
tPLH	CLR	ERR	1.5	13	17	1.5	18	ns
tPLH	ŌĒĀ	PARITY	1.5	10	13	1.5	15	ns
tPHL	7 55,	railli	1.5	10	13	1.5	15	

PARAMETER MEASUREMENT INFORMATION

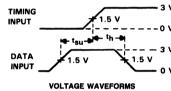


SWITCH POSITION TABLE

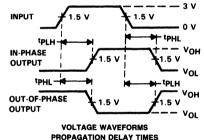
TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
^t PHZ	Open
tPLZ	Closed



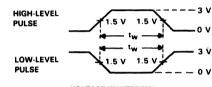
LOAD CIRCUIT 1 ALL OUTPUTS EXCEPT FOR ERROR FLAG



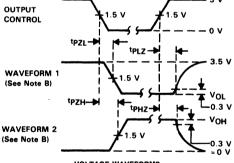
SETUP AND HOLD TIMES



LOAD CIRCUIT 2 ERROR FLAG OUTPUT



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.

FIGURE 1



SN74BCT29843, SN74BCT29844 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D3180, FEBRUARY 1989—REVISED JULY 1989

- BiCMOS Process with CMOS Inputs and TTL Outputs Substantially Reduces Standby Current
- Input Has 50-kΩ Pullup Resistor
- Bus-Structured Pinout
- Functionally Equivalent to AMD Am29843A, Am29844A, 'ALS29843, and 'ALS29844
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs to Reduce DC Loading Effects
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

These 9-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

SN74BCT29843 ... DW OR NT PACKAGE (TOP VIEW)

OC [1D [2D [1 C 2 3	24 23 22] V _{CC}] 10] 20
3D 🗌	4	21	30
4D 🗌	5	20	40
5D 🗌	6	19	5Q
6D 🗆	7	18] 6Q
70 🗌	8	17	7Q
8D 🗌	9	16	98
9D 🗌	10	15	9Q
CLR [11	14	PRE
GND [12	13	1c

SN74BCT29844 ... DW OR NT PACKAGE (TOP VIEW)

oc [ſι	U 24	□vcc
1D [2	23	10
2D 🗌	3	22] 2Q
3D [4	21] 3Q
4D [5	20] 4Q
5D [6	19	□ 5Ω
6D 🗆	7	18	□ 6α
7D [8	17] 7Q
8D 🗌	9	16	□ 80
9D 🗀	10	15	30
CLR [11	14	PRE
GND [12	13] c

The nine latches are transparent D-type. The 'BCT29843 has noninverting data (D) inputs. The 'BCT29844 has inverting D inputs.

A buffered output control (\overline{OC}) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control (OC) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

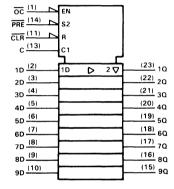
The SN74BCT29843 and SN74BCT29844 are characterized for operation from 0°C to 70°C.



BCT29843 FUNCTION TABLE

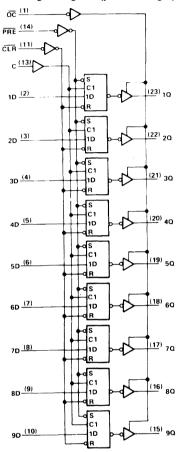
	OUTPUT				
PRE	CLR	ŌC	D	Q	
L	X	L	X	×	Н
н	L	L	X	×	L
Н	Н	L	Н	L	L
Н	Н	L	Н	н	н
н	Н	L	L	x	Q_0
Х	Х	Н	Х	x	Z

'BCT29843 logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'BCT29843 logic diagram (positive logic)

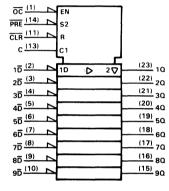




'BCT29844 FUNCTION TABLE

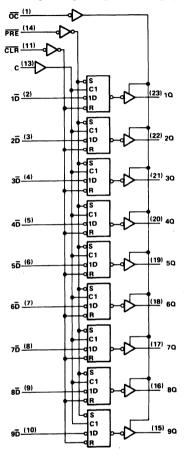
	INPUTS								
PRE	CLR	oc	С	D	Q.				
L	Х	L	Х	×	Н				
Н	L	L	Х	x	L				
Н	Н	L	Н	L	н				
Н	Н	L	н	н	L				
Н	н	L	L	x	Q ₀ Z				
Х	X	н	X	х	Z				

'BCT29844 logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'BCT29844 logic diagram (positive logic)



SN74BCT29843, SN74BCT29844 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	Supply voltage, VCC	. 7	٧
	Input voltage	. 7	٧
,	Voltage applied to a disabled 3-state output	5.5	٧
-	Operating free-air temperature range	70° د	С
	Storage temperature range65°C to	150°	С

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5		5.5	V
VIH	High-level input voltage		2			٧
VIL	Low-level input voltage				0.8	٧
ЮН	High-level output current				-24	mA
lOL	Low-level output current				48	mA
	PRE low	7				
tw	Pulse duration	CLR low	5			ns
		C high	4			
tsu	Setup time, before enable C 1	Data	1.5			ns
·su		PRE or CLR inactive state	2			
th	Hold time, data after enable C \		3.5			ns
TA	Operating free-air temperature		0		70	°C



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
VIĶ	$V_{CC} = 4.5 V$,	$I_{\parallel} = -18 \text{ mA}$			-1.2	٧
Vон	$V_{CC} = 4.5 V,$	$I_{OH} = -15 \text{mA}$	2.4	3.2		٧
	$V_{CC} = 4.5 V,$	$I_{OH} = -24 \text{ mA}$	2			
VOL	$V_{CC} = 4.5 V$,	$I_{OL} = 48 \text{ mA}$		0.35	0.5	٧
lozh	$V_{CC} = 5.5 V,$	$V_O = 2.7 V$			20	μΑ
lozl	$V_{CC} = 5.5 V,$	$V_O = 0.4 V$			-20	μΑ
. 11	$V_{CC} = 5.5 V,$	$V_{I} = 5.5 V$			0.1	mA
Ιн	$V_{CC} = 5.5 V,$	$V_{l} = 2.7 V$	-10		-75	μΑ
ΙΙL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.2	mA
los‡	$V_{CC} = 5.5 V$,	$V_O = 0$	-75		-275	mA
		Outputs high		3	7	
Icc	V _{CC} = 5.5 V	Outputs low		24	35	mA
		Outputs disabled		3	7	

 $[\]uparrow$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	C _L R1 R2 T,	CC = 5 V, = 50 pF = 500 Ω = 500 Ω A = 25°C	, ,	C _L = R1 = R2 = T _A = 0	.5 V to 5.5 V, = 50 pF, = 500 Ω, = 500 Ω, °C to 70°C	UNIT
			MIN	TYP	MAX	MIN	MAX	
tPLH tPLH	D	Any Q	1.5	4.5	7	1.5	8	ns
tpHL			1.5	5.7	8	1.5	9	
t _{PLH}	С	Any Q	1.5	6	8	1.5	10	ns
t _{PHL}		, -	1.5	6	8	1.5	10	
t _{PLH}	PRE	Any Q	1.5	6	10	1.5	12	ns
t _{PHL}		', =	1.5	6	10	1.5	12	
tPLH	CLR	Any Q	1.5	6	10	1.5	12	ns
tPHL] 02	/, 🔾	1.5	6	10	1.5	12	1
^t PZH	<u>oc</u>	OC Any Q		10	13	2	15	ns
tPZL .]	, ~	2	10	13	2	15]
tPHZ	ōc	Any Q	2	5	7	2	8	ns
t _{PLZ}	1	/, &	2	5	7	2	8	



[‡] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	$I_{j} = -18 \text{ mA}$			-1.2	V
Voн	$V_{CC} = 4.5 V,$	$I_{OH} = -15 \text{mA}$	2.4	3.2		V
-011	$V_{CC} = 4.5 V,$	$I_{OH} = -24 \text{ mA}$	2			·
VOL	$V_{CC} = 4.5 V,$	$I_{OL} = 48 \text{ mA}$		0.35	0.5	V
IOZH	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			20	μΑ
IOZL	$V_{CC} = 5.5 V,$	$V_O = 0.4 V$			-20	μΑ
lj .	$V_{CC} = 5.5 V,$	$V_{ } = 5.5 \text{ V}$			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	$V_{I} = 2.7 V$	-10		-75	μΑ
IIL	$V_{CC} = 5.5 V,$	$V_{ } = 0.4 \text{ V}$			-0.2	mA
los‡	$V_{CC} = 5.5 V,$	$V_O = 0$	-75		-275	mA
		Outputs high		3	7	
Icc	V _{CC} = 5.5 V	Outputs low		24	35	mA
		Outputs disabled		3	7	

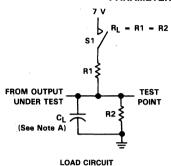
[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2	CC = 5 V, = 50 pF = 500 Ω $CC = 500 \Omega$ A = 25°C	, ,	C _L = R1 =	V to 5.5 V, 50 pF, 500 Ω, 500 Ω, C to 70°C	UNIT
			MIN	TYP	MAX	MIN	MAX	
tPLH	D	Any Q	1.5	5.7	8	1.5	9	ns
tPHL		7, 0	1.5	4.5	7	1.5	8	
^t PLH	С	Any Q	1.5	6	8	1.5	10	ns
t _{PHL}		7, 2	1.5	6	8	1.5	10	
tPLH	PRE	Any Q	1.5	6	11	1.5	12	ns
t _{PHL}		/ly G	1.5	6	11	1.5	12	
t _{PLH}	CLR	Any Q	1.5	6	11	1.5	12	ns
tPHL		/, 🖫	1.5	6	11	1.5	12	τ
^t PZH	OC OC	Any Q	2	10	13	2	15	ns
t _{PZL}		,, G	2	10	13	2	15	
t _{PHZ}	OC OC	Any Q	2	5	7	2	8	ns
tPLZ		', &	2	5	7	2	8	



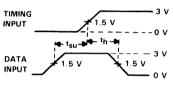
F Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

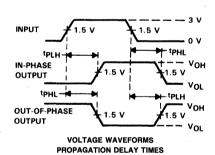


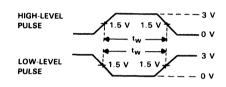
SWITCH POSITION TABLE

TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed

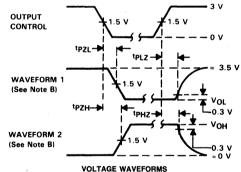


VOLTAGE WAVEFORMS SETUP AND HOLD TIMES





VOLTAGE WAVEFORMS PULSE DURATIONS



ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0=50~\Omega$, $t_f\leq$ 2.5 ns, $t_f\leq$ 2.5 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS



SN74BCT29845, SN74BCT29846 8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D3248, JULY 1989

- BiCMOS Process with CMOS Inputs and TTL Outputs Substantially Reduces Standby Current
- Input Has 50-kΩ Pullup Resistor
- Bus-Structured Pinout
- Functionally Equivalent to AMD Am29845, Am29846. 'ALS29845. and 'ALS29846
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State
- Buffered Control Inputs to Reduce DC Loading Effects
- Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type. The 'BCT29845 has noninverting data (D) inputs. The 'BCT29846 has inverting $\overline{\mathbb{D}}$ inputs. Since $\overline{\mathbb{CLR}}$ and $\overline{\mathbb{PRE}}$ are independent of the clock, taking the $\overline{\mathbb{CLR}}$ input low will cause the eight Q outputs to go low. Taking the $\overline{\mathbb{PRE}}$ input low will cause the eight Q outputs to go high. When both $\overline{\mathbb{PRE}}$ and $\overline{\mathbb{CLR}}$ are taken low, the outputs will follow the preset condition.

SN74BCT29845 ... DW OR NT PACKAGE (TOP VIEW)

OC1 [1	U 24	□ v _{cc}
0C2 [2	23	OC3
1 D 🗌	3	22] 1Q
2D 🗌	4	21] 2Q
3D 🗌	5	20] 3Q
4D 🗌	6	19] 4Q
5D 🗌	7	18] 5Q
6D 🗌	8	17] 6Q
7D 🗌	9	16] 7Q
8D [10	15] 8Q
CLR	11	14	PRE
GND [12	13	Пс

SN74BCT29846 ... DW OR NT PACKAGE (TOP VIEW)

0C1 [1	O 24	□ v _{cc}
OC2	2	23	□ oc₃
1 D [3	22] 1Q
2Ď [4	21] 2Q
3Ď [5	20] 3Q
4Ď [6	19] 4Q
5Ď [7	18] 5Q
6Ď [8	17] 6Q
7Ď [9	16] 7Q
8Ď [10	15] 8Q
CLR	11	14	PRE
GND [12	13] c

The buffered output control inputs ($\overline{OC1}$, $\overline{OC2}$, and $\overline{OC3}$) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without

need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74BCT29845 and SN74BCT29846 are characterized for operation from 0°C to 70°C.

Texas Instruments

'BCT29845

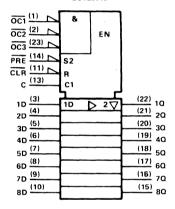
		OUTPUT							
PRE	CLR	ŌC1	OC2	OC3	С	D	Q		
L	Х	L.	L	L	х	Χ	Н		
н	L	L	L	L	Х	Χ	L		
н	Н	L	L	L	Н	L	L		
н	Н	L	L	L	Н	Н	н		
н	Н	L	L	L	L	Х	Q_0		
×	X	X	Х	Н	Х	Х	Z		
×	X	X	Н	X	Χ	Х	Z		
×	X	н	Х	X	Χ	Х	Z		

'BCT29846

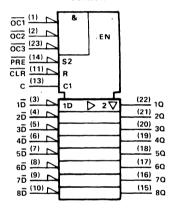
	OUTPUT						
PRE	CLR	OC1	OC2	OC3	c	D	Q
L	Х	L	L	L	Х	Х	Н
н	L	L	L	L	Х	X	L
н	Н	L	L	L	Н	L	н
Н	Н	L	L	L	Н	н	L
Н	Н	L	L	L	L	Х	Q_0
×	X	X	X	н	Χ	Х	Z
×	X	X	Н	X	Х	Х	Z
X	X	Н	Х	Х	X	Х	Z

logic symbols[†]

'BCT29845



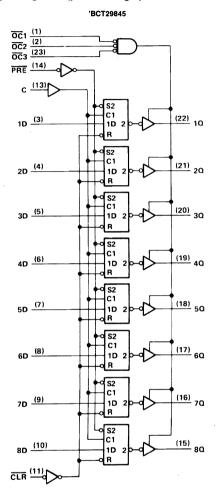
'BCT29846

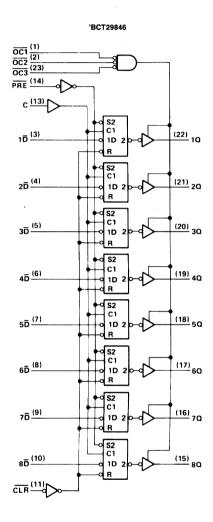


[†] These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

BiCMOS Circuits

logic diagrams (positive logic)







SN74BCT29845, SN74BCT29846 8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range	. −0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5		5.5	٧
VIH	High-level input voltage		. 2			٧
VIL	Low-level input voltage				0.8	٧
ЮН	High-level output current				-24	mA
loL	Low-level output current				48	mA
		PRE low	7			,
$t_{\mathbf{W}}$	Pulse duration	CLR low	5			ns
		C high	4			
t _{su}	Setup time, before enable C \(\bigcup \)	Data	1.5			ns
-Su		PRE or CLR, inactive state	2			
th	Hold time, data after enable C↓		3.5			ns
TA	Operating free-air temperature		. 0		70	ŝ



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 V$	$I_{\parallel} = -18 \text{ mA}$			-1.2	٧
Voн	$V_{CC} = 4.5 V$	IOH = -15 mA	2.4	3.2		V
-011	$V_{CC} = 4.5 V,$	$I_{OH} = -24 \text{mA}$	2			
VOL	$V_{CC} = 4.5 V_{r}$	I _{OL} = 48 mA		0.35	0.5	٧
lozн	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			20	μΑ
lozL	$V_{CC} = 5.5 V$,	$V_{O} = 0.4 \text{ V}$			-20	μΑ
l _l	$V_{CC} = 5.5 V$,	$V_1 = 5.5 V$			0.1	mA
ίн	$V_{CC} = 5.5 V,$	V _I = 2.7 V	-10		-75	μΑ
11L	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.2	mA
los‡	$V_{CC} = 5.5 V,$	$V_O = 0$	-75		-275	mA
		Outputs high		3	7	
ICC	$V_{CC} = 5.5 V$	Outputs low		24	35	mA
		Outputs disabled		3	7	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$\begin{array}{c} \text{VCC} = 5 \text{ V,} \\ \text{CL} = 50 \text{ pF,} \\ \text{R1} = 500 \ \Omega, \\ \text{R2} = 500 \ \Omega, \\ \text{TA} = 25^{\circ}\text{C} \\ \\ \text{MIN} \qquad \text{TYP} \qquad \text{MAX} \\ \end{array}$		C _L = R1 = R2 =	.5 V to 5.5 V, = 50 pF, = 500 Ω, = 500 Ω, O'C to 70°C	UNIT	
tPLH	D	A=::0	1.5	4.5	7	1.5	8	ns
tPHL		Any Q	1.5	5.7	8	1.5	9	ris
tPLH	С	C Any Q		6	8	1.5	10	ns
tPHL		7.iiy G	1.5	6	8	1.5	10	110
tPLH t	PRE	Any Q	1.5	6	11	1.5	12	ns
t _{PHL}		7, C	1.5	6	11	1.5	12	
tPLH tPLH	CLR	Any Q	1.5	6	11	1.5	12	ns
tPHL	J	, -	1.5	6	11	1.5	12	
^t PZH	ŌC	Any Q	2	10	13	2	15	ns
t _{PZL}		, -	2	10	13	2	15	
tPHZ	ŌC	OC Any Q		5	7	2	8	ns
tPLZ		,	2	5	7	2	8	



^{*} Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

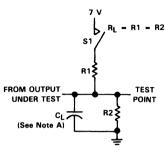
PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
ViK	$V_{CC} = 4.5 V,$	$I_{\rm I} = -18$ mA			-1.2	٧
Voн	$V_{CC} = 4.5 V,$	$I_{OH} = -15 \text{mA}$	2.4	3.2		٧
-011	$V_{CC} = 4.5 V,$	$I_{OH} = -24 \text{mA}$	2			
VOL	$V_{CC} = 4.5 V,$	$I_{OL} = 48 \text{ mA}$		0.35	0.5	٧
lozh	$V_{CC} = 5.5 V,$	$V_O = 2.7 V$			20	μΑ
lozL	$V_{CC} = 5.5 V,$	$V_O = 0.4 V$			-20	μΑ
l _l	$V_{CC} = 5.5 V,$	$V_{ } = 5.5 \text{ V}$			0.1	mA
JIH	$V_{CC} = 5.5 V,$	$V_{\parallel}=2.7\mathrm{V}$	-10		-75	μΑ
IIL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.2	mA
los‡	$V_{CC} = 5.5 V,$	$V_{O} = 0$	-75		-275	mA
lcc		Outputs high		3	7	
	$V_{CC} = 5.5 V$	Outputs low		24	35	mA
		Outputs disabled		3	7	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER	FROM (INPUT)			V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C		CL R1 R2	4.5 V to 5.5 V, = 50 pF, = 500 Ω, = 500 Ω, 0°C to 70°C	UNIT
			MIN	TYP	MAX	MIN	MAX	
tPLH	D	Any Q	1.5	5.7	8	1.5	9	ns
tPHL]		1.5	4.5	7	1.5	8	
tPLH	С	Any Q	1.5	6	8	1.5	10	ns
tPHL temperature	_	, _	1.5	6	8	1.5	10	
tPLH	PRE	Any Q	1.5	6	11	1.5	12	ns
tPHL the transfer of the trans		[1.5	6	11	1.5	12	
tPLH	CLR	Any Q	1.5	6	11	1.5	12	ns
tPHL]	, _	1.5	6	11	1.5	12	
tPZH	ŌĊ	Any Q	2	10	13	2	15	ns
tPZL		Ally G		10	13	2	15	
t _{PHZ}	ŌĊ	Any Q	2	6	8	2	<u>,</u> 10	ns
tPLZ		, 🔾	2	6	8	2	10	

[‡] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

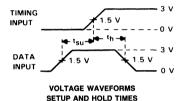
PARAMETER MEASUREMENT INFORMATION

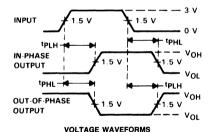


LOAD CIRCUIT

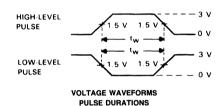
SWITCH POSITION TABLE

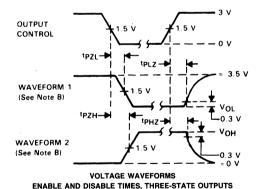
TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed





PROPAGATION DELAY TIMES





NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C, All input pulses are supplied by the generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f \leq 2.5$ ns. $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS



BiCMOS Design Reduces Standby Current

- Flow-Through Pinout (All Inputs on Opposite Side from Outputs)
- Functionally Equivalent to AMD Am29853 and Am29854
- **High-Speed Bus Transceivers with Parity** Generator/Checker
- Parity Error Flag with Open-Collector Output
- Choice of True ('BCT29853) or Inverting ('BCT29854) Logic
- Has a Latch for Storage of the Parity Error Flag
- Package Options Include Plastic "Small Outline" Package, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

The SN74BCT29853 and SN74BCT29854 are 8-bit to 9-bit parity transceivers designed for two-way communication between data buses. When data is transmitted from the A to B bus, a parity bit is generated. When data is transmitted from the B to A bus with its corresponding parity bit, the ERR output will indicate whether or not an error in the B data has occurred. The output enable inputs OEA and OEB can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd output (PARITY), and monitors the parity of the I/O ports with an open-collector parity error flag (ERR). ERR can be either passed, sampled, stored, or cleared from the latch using the LE and CLR control inputs. When both OEA and OEB are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The SN74BCT29853 and SN74BCT29854 are characterized for operation from 0°C to 70°C.

SN74BCT' ... DW OR NT PACKAGE (TOP VIEW)

OEA [1 0	24] v _{cc}
A1 [2	23	B1
A2 [3	22] B2
A3 [4	21] B3
A4 [5	20] B4
A5 [6	19] B5
A6 [7	18] B6
A7 [8	17	B7
A8 [9	16] B8
ERR [10	15	PARITY
CLR	11	14	OEB
GND	112	13	LE

BiCMOS Circuits

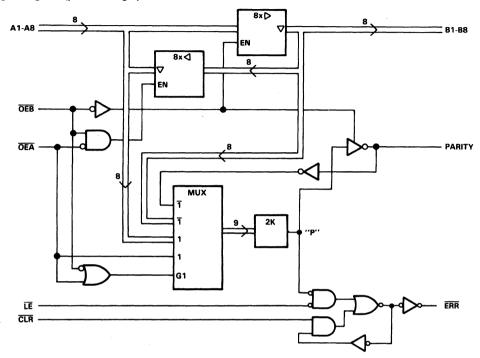
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not

necessarily include testing of all parameters.



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logic diagram (positive logic)



FUNCTION TABLE

INPUTS						OUTPUT & I/O				
ŌĒB	OEA	CLR	LE	Ai Σ of H's	Bi [†] Σ of H's	A	В	PARITY	ERR‡	FUNCTION
L	н	х	х	Odd Even	NA	NA	А	L H	NA	A Data to B Bus and Generate Parity
Н	L	х	L	NA	Odd Even	В	NA	NA	H	B Data to A Bus and Check Parity
Н	L	Н	Н	NA	Х	Х	NA	NA	N-1	Store Error Flag
Х	Х	L	Н	Х	X	X	NA	NA	Н	Clear Error Flag Register
Н	н	H	HHLL	X X L Odd H Even	х	z	z	Z	NC H H L	Isolation [§] (Parity Check)
L	L	Х	×	Odd Even	NA	NA	Α	H	NA	A Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care

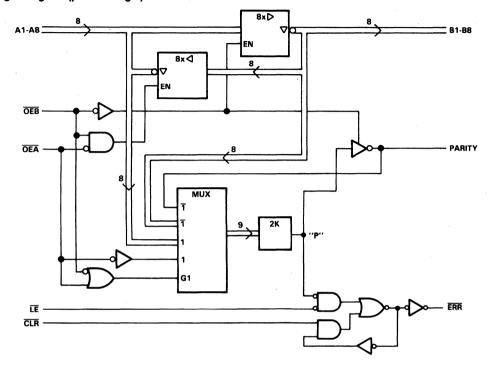


[†]Summation of high-level inputs includes PARITY along with Bi inputs.

[‡]Output states shown assume the ERR output was previously high.

[§]In this mode the ERR output, when enabled, shows inverted parity of the A bus.

logic diagram (positive logic)



FUNCTION TABLE

	INPUTS					OUTPUT & I/O				
ŌĒB	ŌĒĀ	CLR	LE	Ai Σ of H's	Bi [†] Σ of L's	А	В	PARITY	ERR‡	FUNCTION
L	н	х	х	Odd Even	NA	NA	Ā	· L	NA	Ā Data to B Bus and Generate Parity
Н	L	х	L	NA	Odd Even	B	NA	NA	H	B Data to A Bus and Check Parity
Н	L	Н	Н	NA	Х	X	NA	NA	N-1	Store Error Flag
X	Х	L	Н	×	Х	Х	NA	NA	Н	Clear Error Flag Register
н	н	H K X	HLL	X X L Odd H Even	x	z	z	z	NC H L H	Isolation [§]
Ł	L	х	×	Odd Even	NA	NA	Ā	L H	NA	Ā Data to B Bus and Generate Inverted Parity

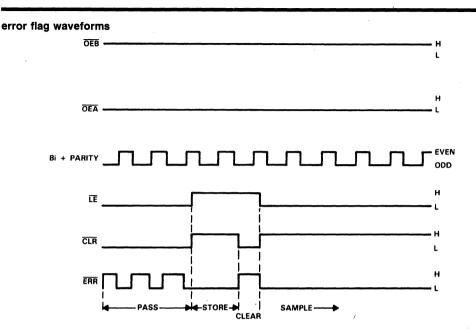
NA = Not applicable, NC = No change, X = Don't care



[†]Summation of low-level inputs includes PARITY along with Bi inputs.

[‡]Output states shown assume the ERR output was previously high.

[§]In this mode the ERR output, when enabled, shows noninverted parity of the A bus.



ERROR FLAG FUNCTION TABLE

INF	PUTS	INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION
LE	CLR	POINT "P"	ERR _{n-1} †	ERR	
L	L	ΞĻ	х	L H	PASS
L	н	L X H	X L H	LLH	SAMPLE
Н	L	Х	Х	Н	CLEAR
Н	Н	Х	L H	L H	STORE

[†]ERR_{n-1} represents the state of the ERR output before any changes at CLR, LE or point P.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Voltage applied to a disabled I/O port	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

				MIN	NOM	MAX	UNIT	
VCC	Supply voltage			4.5	5	5.5	٧	
VIH	High-level input voltage			2			٧	
VIL	Low-level input voltage					0.8	٧	
Vон	High-level output voltage, ERR					2.4	٧	
ЮН	High-level output current					-24	mA	
lOL	Low-level output current					48	mA	
tw	Pulse duration	LE low		10			ns	
·w		CLR low		10			110	
t _{su}	Setup time before LE ↓	Bi and PARITY		12			ns	
th	Hold time, Bi and PARITY after LE↓			3			ns	
TA	Operating free-air temperature			0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIK		$V_{CC} = 4.5 V$	$I_{\parallel} = -18 \text{ mA}$			-1.2	٧
VOH	All inputs/outputs	V _{CC} = 4.5 V	$I_{OH} = -15 \text{mA}$	2.4			٧
	except ERR	•	IOH = -24 mA	2			
ЮН	ERR	$V_{CC} = 4.5 V,$	$V_{OH} = 2.4 V$			20	μΑ
VOL		$V_{CC} = 4.5 V,$	IOL = 48 mA		0.35	0.5	٧
l _l		$V_{CC} = 5.5 V,$	$V_{ } = 5.5 V$			0.1	mA
l _{IH} ‡		$V_{CC} = 5.5 V,$	V _I = 2.7 V			20	μΑ
IIL‡	Data	$V_{CC} = 5.5 V_{r}$	$V_1 = 0.4 \text{ V}$			-0.2	mA
"IL.	Control	1 100 0.0 1,	• • • • • • • • • • • • • • • • • • • •			-0.75	
los§		$V_{CC} = 5.5 V,$	VO = 0	-75		-250	mA
ICCL		$V_{CC} = 5.5 V_{r}$	All outputs open	-	55	80	mA
Iccz		1 .00 0.0 1,	, iii saipats spot		30	45	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] These parameters include off-state output current for I/O ports only.

[§] Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed 1 second.

SN74BCT29853 switching characteristics (see Figure 1)

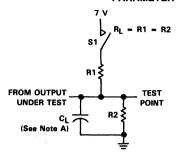
PARAMETER	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$, ,	CL R1 R2	4.5 V to 5.5 V, = 50 pF, = 500 Ω, = 500 Ω, MIN to MAX	UNIT		
tPLH			1	5	7	1	10	
tPHL	A or B	B or A	1	5	7	1	10	ns
tPLH	Α	PARITY	1.5	10	13	1.5	15	ns
t _{PHL}	^	178811	1.5	10	13	1.5	15	1 '''
tPZH	OEA or OEB	A or B	2	13	16	2	20	ns
tPZL	02/10/022		2	13	16	2	20	,,,
t _{PHZ}	OEA or OEB	A or B	2	13	16	2	20	ns
tPLZ			2	13	16	2	20	
tPHL	Œ	ERR	1.5	5	7	1.5	9	ns
tPLH	CLR	ERR	1.5	11	14	1.5	15	ns
tPLH	ŌĒĀ	PARITY	1.5	10	13	1.5	15	ns
tPHL	2271		1.5	10	13	1.5	15]
tPLH .	Bi/PARITY	ERR	1.5	17	22	1.5	24	ns
t _{PHL}		=:	1.5	10	13	1.5	16	

SN74BCT29854 switching characteristics (see Figure 1)

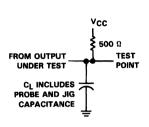
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _i R:	CC = 5 V L = 50 pF $1 = 500 \Omega$ $2 = 500 \Omega$ $A = 25^{\circ}C$ TYP	, ,	C _L R1 R2	4.5 V to 5.5 V, $= 50 \text{ pF,}$ $= 500 \Omega,$ $= 500 \Omega,$ $= 500 \Omega,$ MIN to MAX	UNIT
tPLH	A or B	B or A	1	5	7	1	8	ns
tPHL	AOIB	BOIA	1	5	7	1	8	1 115
tPLH	А	PARITY	1.5	10	13	1.5	15	ns
tPHL			1.5	10	13	1.5	15]
^t PZH	OEA or OEB	or OEB A or B	2	12	15	2	17	ns
tpZL	7	7, 0, 5	2	13	16	2	19	
^t PHZ	OEA or OEB	DEB A or B	2	8	11	2	15	ns
tPLZ			2	10	14	2	17	
t _{PHL}	ĪĒ	ERR	1.5	5	7	1.5	9	ns
tPLH	CLR	ERR	1.5	11	13	1.5	15	ns
tPLH	ŌĒĀ	PARITY	1.5	10	13	1.5	15	ns
tpHL]	1,4411	1.5	10	13	1.5	16]
^t PLH	Bi/PARITY	ERR	1.5	15	18	1.5	20	ns
tPHL]		1.5	10	13	1.5	15]



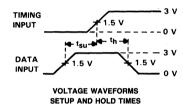
PARAMETER MEASUREMENT INFORMATION

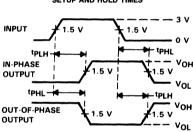


SWITCH PO	SITION TABL
TEST	S 1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed



LOAD CIRCUIT 1 ALL OUTPUTS EXCEPT FOR ERROR FLAG

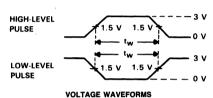




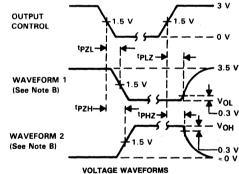
VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES

LOAD CIRCUIT 2 ERROR FLAG OUTPUT



PULSE DURATIONS



ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1



SN74BCT29861A, SN74BCT29862A 10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3161, NOVEMBER 1988-REVISED JULY 1989

- BiCMOS Design Substantially Reduces Standby Current
- Functionally Equivalent to Am29861A, Am29862A, 'ALS29861, and 'ALS29862
- Choice of True ('BCT29861A) or Inverting ('BCT29862A) Logic
- Power-Up High-Impedance State
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 10-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs ($\overline{G}BA$ and $\overline{G}AB$).

The outputs are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down.

The SN74BCT29861A and SN74BCT29862A are characterized for operation from 0°C to 70° C.

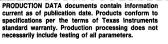
FUNCTION TABLE

INP	UTS	OPERATION			
GAB	GВА	'BCT29861A	'BCT29862A		
L	Н	A to B	Ā to B		
Н	L	B to A	B̄ to A		
Н	Н	Isolation	Isolation		
L	L	Latch A and B	Latch A and B		
		(A = B)	$(A = \overline{B})$		

DW OR NT PACKAGE (TOP VIEW)

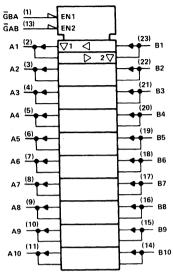
ĞBA [1	U 24	$\square \vee_{cc}$
A1 [2	23	_ B1
A2 🗌	3	22	☐ B2
A3 [4	21	_ B3
A4 🗌	5	20	□ B4
A5 🗌	6	19	☐ B5
A6 🗌	7	18	☐ B6
A7 🗌	8	17	□ B7
A8 🗌	9	16	☐ B8
A9 🗌	10	15	☐ B9
A10 🗌	11	14	☐B10
GND [12	13	☐ ĞAE

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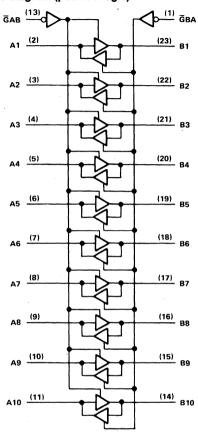


logic symbol[†]



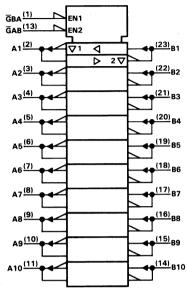
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



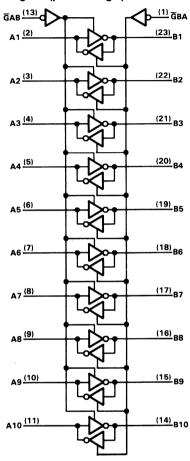


logic symbol[†]



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage (all inputs and I/O ports)	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	٧
VIH	High-level input voltage	2			٧
ViL	Low-level input voltage			0.8	٧
ЮН	High-level output current			-24	mA
lOL	Low-level output current			48	mA
TA	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER		TEST CO	NDITIONS	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	$I_{\parallel} = -18 \text{ mA}$				-1.2	٧
VOH		$V_{CC} = 4.5 V$	IOH = -15 mA		2.4			٧
*On		1.00	IOH = -24 mA		2			
VOL		$V_{CC} = 4.5 V,$	IOL = 48 mA			0.35	0.5	٧
II .		$V_{CC} = 5.5 V$,	$V_{ } = 5.5 \text{ V}$				0.1	mA
ήн	Control inputs	$V_{CC} = 5.5 V,$	Vı = 27V				20	μΑ
יורו	A or B port‡	100 0.0 1,	·1 ·				20	,
կլ_	Control inputs	$V_{CC} = 5.5 V_{r}$	VI = 0.4 V				-0.2	mA
·1L	A or B port‡	100 515 1,	.,				-0.2	
IO(off)§		$V_{CC} = 0$,	V _O = 2.9 V				0.1	mA
los¶		$V_{CC} = 5.5 V,$	V _O = 0		-75		-250	mA
			· · · · · · · · · · · · · · · · · · ·	Outputs high		18	30	
ICC	$V_{CC} = 5.5 V$		Outputs low		30	45	mA	
				Outputs disabled		6.5	12	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the offstate output current.

[§] IO(off) = Power-off bus leakage current.

Not more than one output should be shorted at a time and duration of the short circuit should not exceed 1 second.

SN74BCT29861A, SN74BCT29862A 10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

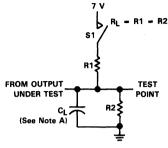
SN74BCT29861A switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C ₁ R1 R2	CC = 5 V, = 50 pF I = 500 Ω Ω = 500 Ω A = 25°C	, ,	C _L = R1 = R2 =	5 V to 5.5 V, 50 pF, 500 Ω, 500 Ω, C to 70°C	UNIT
			MIN	TYP	MAX	MIN	MAX	
tPLH .	A or B	B or A	1.5	5	7	1	8	ns
tPHL ten	L		1.5	5	7	1	8	
^t PZH	GAB or GBA	A or B	2	7	10	2	11	ns
^t PZL]		2	9	12	2	13	
^t PHZ	GAB or GBA	A or B	2	6	9	2	10	ns
tPLZ]		2	6	9	2	10]

SN74BCT29862A switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	G F	$f_{CC} = 5 \text{ N}$ $f_{CC} = 50 \text{ pl}$ $f_{CC} = 500 \text{ s}$	F, n, n,	C _L R1 R2 T _A =	4.5 V to 5.5 V, = 50 pF, = 500 Ω , = 500 Ω , 0°C to 70°C	UNIT
			MIN	TYP	MAX	MiN	MAX	ļ
tPLH_	A or B	B or A	1.5	5	8	1	9	ns
tPHL			1.5	5	7	1	8	
^t PZH	GAB or GBA	A or B	2	7	10	2	11	ns
^t PZL	aris or asr.	7.0.2	2	9	12	2	13	
tPHZ	GAB or GBA	A or B	2	6	9	2	10	ns
tPLZ	22 3r db/(7.015	2	6	9	2	10]

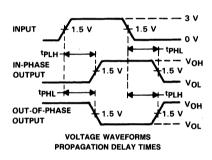
PARAMETER MEASUREMENT INFORMATION

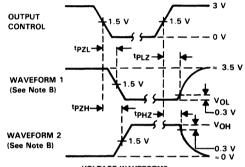


LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
tPLH	Open
t _{PHL}	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed





VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by the generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.

FIGURE 1. SWITCHING CHARACTERISTICS

SN74BCT29863A, SN74BCT29864A 9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3162, NOVEMBER 1988-REVISED FEBRUARY 1989

- BiCMOS Design Substantially Reduces Standby Current
- Functionally Equivalent to Am29863A, Am29864A, 'ALS29863, and 'ALS29864
- Choice of True ('BCT29863A) or Inverting ('BCT29864A) Logic
- Power-Up High-Impedance State
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 9-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs (GBA1, GBA2, GAB1, and GAB2).

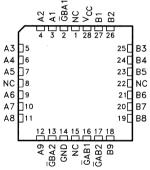
The outputs are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down.

The SN74BCT29863A and SN74BCT29864A are characterized for operation from 0°C to 70°C.

DW OR NT PACKAGE (TOP VIEW)

ĞΒA1 [1	U 24	□ v _{cc}
A1 [2	23	□ B1
A2 🗌	3	22	☐ B2
A3 [4	21] B3
A4 🗌	5	20	□ B4
A5 [6	19] B5
A6 🗌	7	18]в6
A7 🗌	8	17	□ B7
A8 [9	16	_ B8
A9 🗌	10	15] B9
GBA2 □	11	14	☐ ĞAB2
GND [12	13	☐ ĞAB1

FN PACKAGE (TOP VIEW)



NC-No internal connection

FUNCTION TABLE

	ENABLE	INPUTS		OPERATION			
GAB1	GAB2	GBA1	GBA2	'BCT29863A	'BCT29864A		
L	L	L	L	Latch A and B	Latch A and B		
L	L	Н	Х	A to B	A to B		
L	L	X	Н	AIUB	A 10 B		
н	x	L	L	B to A	B to Ā		
X	н	L	L	BIOA	BIOA		
н	X	н	х				
н	X	X	н	lastation	laslation		
x	н	X	н	Isolation	Isolation		
×	н	н	X				

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

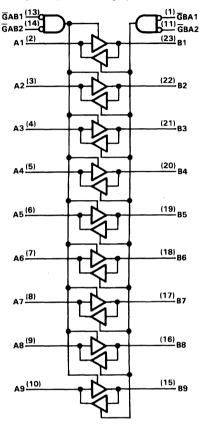


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logic symbol[†] GBA1 (1) GBA2 (11) EN1 GAB1 (13) EN2 GAB2 (14) (23)_{B1} A1 (2) ব 2 🗸 (22) B2 A2(3) (21)_{B3} A3 (4) (20)_{B4} A4 (5) (<u>19)</u> _{B5} A5 (6) (18)_{B6} A6 (7) (17)_{B7} A7 (8) (16)_{B8} A8⁽⁹⁾ (<u>15)</u> _{B9} A9⁽¹⁰⁾

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



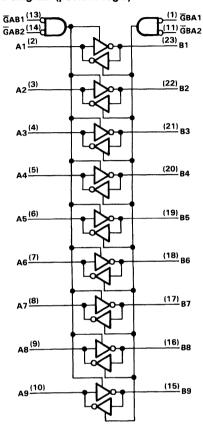


SN74BCT29864A 9-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

logic symbol[†] GBA1 (1) GBA2(11) EN1 GBA2 GAB1 (13) GAB2 (14) & EN2 (23) B1 A1 (2) ব 20 (<u>22)</u> B2 A2(3) (<u>21)</u> B3 A3(4) A4⁽⁵⁾ (20) B4 (19)_{B5} A5 (6) A6 (7) (18) B6 (17) B7 A7⁽⁸⁾ A8(9) (16) B8 (15) B9 A9(10)

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SN74BCT29863A, SN74BCT29864A 9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage (all inputs and I/O ports)	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	٧
VIH	High-level input voltage	2			٧
VIL	Low-level input voltage			0.8	٧
ЮН	High-level output current			-24	mA
lOL	Low-level output current			48	mA ·
TA	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		TEST CO	NDITIONS	MIN	TYP†	MAX	UNIT	
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA				-1.2	٧	
Vон		V _{CC} = 4.5 V	IOH = -15 mA		2.4			V	
•011		100	IOH = -24 mA		2				
VOL		$V_{CC} = 4.5 V,$	$I_{OL} = 48 \text{ mA}$			0.35	0.5	V	
lj.		$V_{CC} = 5.5 V,$	$V_{CC} = 5.5 V, V_I = 5.5 V$				0.1	mA	
ΊΗ	Control inputs	$V_{CC} = 5.5 V_{r}$	Vı = 2.7 V				20	μΑ	
1111	A or B port‡	1,000 0.0 1,	•1 = •				20	,	
l _{IL}	Control inputs	$V_{CC} = 5.5 V,$	VI = 0.4 V				-0.2	mA	
11.	A or B port‡	100 00 1,	.,				-0.2		
IO(off) [§]		$V_{CC} = 0$,	V _O = 2.9 V				0.1	mA	
los¶		$V_{CC} = 5.5 V,$	$5 \text{ V}, \text{V}_{\text{O}} = 0$		-75		-250	mA	
				Outputs high		18	30		
ICC		$V_{CC} = 5.5 V$		Outputs low		30	45	mA	
				Outputs disabled		6.5	12		

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] IO(off) = Power-off bus leakage current.

Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

SN74BCT29863A, SN74BCT29864A 9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SN74BCT29863A switching characteristics

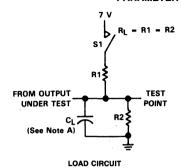
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2	CC = 5 V, = 50 pF = 500 Ω = 500 Ω A = 25°C	, ,	C _L R1 R2	4.5 V to 5.5 V, = 50 pF, = 500 Ω , = 500 Ω , 0°C to 70°C	UNIT
			MIN	TYP	MAX	MIN	MAX	
tPLH	A or B	B or A	1	5	7	1	8	ns
tPHL the transfer of the trans			1	5	7	1	8	
^t PZH	GAB or GBA	A or B	2	7	10	2	11	ns
tPZL			2	9	12	2	13	
tPHZ	GAB or GBA	A or B	2	6	9	2	10	ns
tPLZ] 3. 0	,	2	6	9	2	10	"

SN74BCT29864A switching characteristics

PARAMETER	FROM (INPUT)	1		CC = 5 V, = 50 pF = 500 Ω = 500 Ω A = 25°C	, ,	C _L R1 = R2 =	3.5 V to 5.5 V, = 50 pF, = 500 Ω, = 500 Ω, 0°C to 70°C	UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	1	5	8	1	9	ns
t _{PHL}	,,,,,		1	5	7	1	8	
^t PZH	GAB or GBA	A or B	2	7	10	2	11	ns
t _{PZL}			2	9	12	2	13	
^t PHZ	GAB or GBA	A or B	2	6	9	2	10	ns
†PLZ			2	6	9	2	10	

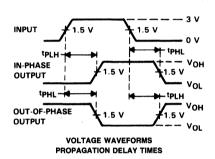


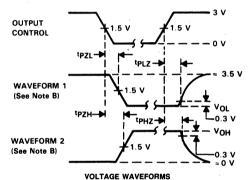
PARAMETER MEASUREMENT INFORMATION



SWITCH POSITION TABLE

TEST	S 1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed





ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by the generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.

FIGURE 1. SWITCHING CHARACTERISTICS

BiCMOS Circuits Preliminary Data Sheets





SN64BCT540 OCTAL BUFFER AND LINE DRIVER WITH 3-STATE OUTPUTS

D3253, FEBRUARY 1989

- State of the Art BiCMOS Design Significantly Reduces ICCZ
- 3-State Inverting Outputs Drive Bus Lines or Buffer Memory Address Registers
- High-Impedance State During Power Up and Power Down
- P-N-P Inputs Reduce D-C Loading
- Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

This octal buffer and line driver is designed to have the performance of the popular SN64BCT240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR gate so that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

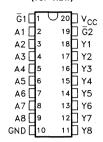
The SN64BCT540 is characterized for operation from -40° C to 85°C.

FUNCTION TABLE

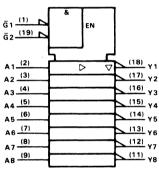
	INPUTS		OUTPUT
G1	G2	Α	Y
L	L	L	н
L	L	н	L
Н	X	X	z
×	Н	Х	Z

Z = High Impedance

SN64BCT540 ... DW OR N PACKAGE



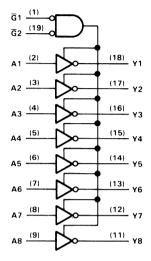
logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, VCC	. −0.5 V to 7 V
Input voltage	0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to V _C C
Current into any output in the low state	128 mA
Operating free-air temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	٧
VIH	High-level input voltage	2			٧
VIL	Low-level input voltage			0.8	٧
ΊΚ	Input clamp current			-18	mA
ЮН	High-level output current			-15	mA
lOL	Low-level output current			64	mA
TA	Operating free-air temperature	-40		85	°C



SN64BCT540 OCTAL BUFFER AND LINE DRIVER WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]					TYP [‡]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	$I_{\rm J}=-18~{\rm mA}$					-1.2	٧
Voн	V _{CC} = 4.5 V			IOH = -3 mA	2.4	3.3		v
·On	100			$I_{OH} = -15 \text{mA}$	2	3.1		1
VOL	$V_{CC} = 4.5 V$	CC = 4.5 V				0.42	0.55	٧
lozh	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	$V_0 = 2.7 V$					50	μΑ
^I OZL	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	$V_0 = 0.5 V$					-50	μΑ
loz	G at 0.8 V,		$V_{CC} = 0$ to 2.	V _{CC} = 0 to 2.35 V (power up)			± 50	μΑ
.02	$V_0 = 2.7 \text{ V or } 0.5 \text{ V}$	/	$V_{CC} = 2 V to$	0 (power down)	Ī		±50	
ij	$V_{CC} = 5.5 V,$	V _I = 7 V					0.1	mA
lΗ	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$					20	μΑ
IJĽ	$V_{CC} = 5.5 V,$	$V_{J} = 0.5 V$					-0.6	mA
los [§]	$V_{CC} = 5.5 V,$	$V_O = 0$			-100		-225	mA
ICCL	$V_{CC} = 5.5 V$					45	71	mA
ССН	$V_{CC} = 5.5 V$	5 V				20	30	mA
lccz	V _{CC} = 5.5 V					3	6	mA
Ci	$V_{CC} = 5 V$,	$V_{ } = 2.5 \text{V or } 0$	0.5 V			5		pF
Co	$V_{CC} = 5 V$	$V_{ } = 2.5 \text{V or } 0$	0.5 V			. 10		["

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	F	V _{CC} = 5 \ C _L = 50 p R1 = 500 s R2 = 500 s T _A = 25°C	F, Ω, Ω,	$\begin{array}{l} \text{VCC} = 4.5 \text{ V to } 5.5 \text{ V,} \\ \text{C}_L = 50 \text{ pF,} \\ \text{R1} = 500 \Omega, \\ \text{R2} = 500 \Omega, \\ \text{T}_A = \text{MIN to MAX}^\dagger \end{array}$		UNIT
			MIN	TYP	MAX	MIN	MAX	}
tPLH	A	Y	2.5	4.1	5.8	1.9	7.2	ns
t _{PHL}	, ,	· '	0.6	1.9	3.5	0.3	4.5]
tPZH	G	Y	4.8	6.8	8.9	4.1	10.4	ns
tPZL		·	6	8	10	5.3	11.8	
tPHZ	G	Y	3.5	5.7	7.8	2.7	9.4	ns
tPLZ] ~	,	3.8	5.5	7.4	3.5	8.9]

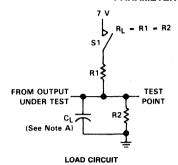
[†] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.



[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

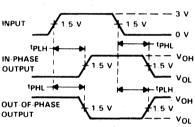
PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH	Open
toui	Open

SWITCH POSITION TABLE

TEST	51	
tPLH	Open	
tPHL	Open	
tPZH	Open	
tPZL	Closed	
tPHZ	Open	
tPLZ	Closed	





OUTPUT CONTROL tPZL-WAVEFORM 1 (See Note B) VOL tPZH-0.3 V ¹PHZ-▶ ۷он **WAVEFORM 2** (See Note B) 0.3 V

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by the generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega, t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement,

FIGURE 1. SWITCHING CHARACTERISTICS

SN54BCT544, SN74BCT544 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

D3317, NOVEMBER 1988

- 3-State True Outputs
- Back-to-Back Registers for Storage
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Standard Plastic and Ceramic 300-mil DIPs

description

The 'BCT544 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable (LEAB or LEBA) and Output Enable (GAB or GBA) inputs are provided for each register to permit independent control in either direction of data flow. For the SN54BCT544 and SN74BCT544 respectively, the A outputs are characterized to sink 20 or 24 mA while the B outputs are characterized for 48 or 64 mA. The 'BCT544 inverts data in both directions.

The A-to-B Enable (CEAB) input must be low in order to enter data from A or to output data from B. Having CEAB low and LEAB low makes the A-to-B latches transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and GAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the CEBA, LEBA, and GBA inputs.

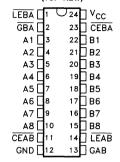
The SN54BCT544 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT544 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

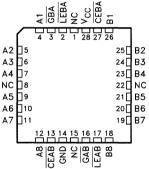
INPUTS		OUTPUT BUFFERS		
CEAB	LEAB	GAB	A to B [†]	B1 THRU B8
Н	Х	Х	Storing	High Z
х	н		Storing	
Х		Н		High Z
L	L	L	Transparent	Current A Data
L	Н	L	Storing	Previous‡ A Data

[†] A-to-B data flow is shown: B-to-A flow control is the same except uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{GBA}}$.

SN54BCT544 ... JT PACKAGE SN74BCT544 ... DW OR NT PACKAGE (TOP VIEW)



SN54BCT544 ... FK PACKAGE (TOP VIEW)



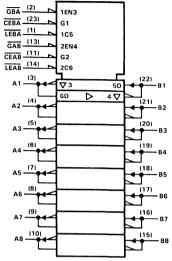
NC-No internal connection



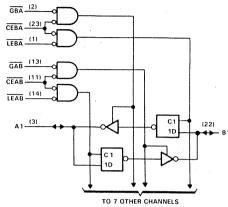
[‡] Before low-to-high transition of LEAB.

SN54BCT544, SN74BCT544 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

logic symbol†



logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	−0.5 V to 7 V
Input voltage, (see Note 1)	−0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to VCC
Input clamp current	−30 mA
Current into any output in the low state: SN54BCT544	96 mA
SN74BCT544	128 mA
Operating free-air temperature range: SN54BCT544	-55°C to 125°C
SN74BCT544	0°C to 70°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions

		SI	SN54BCT544			SN74BCT544		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.8			0.8	٧
ΊΚ	Input clamp current			-18			18	mA
ЮН	High-level output current			-12			-15	mA
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SI	SN54BCT544			SN74BCT544			
PANAMETEN			MIN	TYP [†]	MAX	MIN	TYP	MAX	UNIT	
ViK	$V_{CC} = 4.5 \text{ V}, I_{I} = -18 \text{ mA}$				-1.2			-1.2	٧	
		IOH = -3 mA	2.4	3.3		2.4	3.3			
VOH	$V_{CC} = 4.5 V$	IOH = -12 mA	2	3.2					V	
		IOH = -15 mA				2	3.1			
Voн	V _{CC} = 4.5 V	IOH = 48 mA		0.38	0.55				V 55	
. VOH	VCC = 4.5 V	IOL = 64 mA					0.42	0.55		
lozh	$V_{CC} = 5.5 V, V_{O} = 2.7 V$				50			50	μΑ	
IOZL	$V_{CC} = 5.5 V, V_{O} = 0.5 V$				-50			-50	μΑ	
l _l	$V_{CC} = 5.5 V, V_I = 7 V$				0.6			0.6	mA	
ΊΗ	$V_{CC} = 5.5 V, V_{I} = 2.7 V$				20		2200	20	μΑ	
IIL	$V_{CC} = 5.5 V, V_{I} = 0.5 V$				-0.6			-0.6	mA	
los‡	$V_{CC} = 5.5 V, V_{O} = 0$		-100		-225	-100		-225	mA	
ICCL	V _{CC} = 5.5 V								mA	
ССН	V _{CC} = 5.5 V								mA	
ICCZ	V _{CC} = 5.5 V								mA	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.



[‡] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

SN54BCT544, SN74BCT544 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

timing requirements

	VCC = 5 V, VCC = 4.5 V to 5.5 V TA = 25°C TA = MIN to MAX		to MAX†		UNIT				
1			'BCT	544 SN54BCT544 SN74BCT544		CT544	, 5		
l			MIN	MAX	MIN	MAX	MIN	MAX	
tsu	Setup time, data before latch enable	High or low							ns
th	Hold time, data after latch enable	High or low							ns

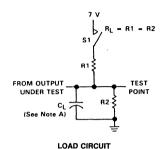
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}\text{C}$		$\begin{array}{lll} \text{CL} = 50 \text{ pF,} & \text{CL} = 50 \text{ pF,} \\ \text{R1} = 500 \ \Omega, & \text{R1} = 500 \ \Omega, \\ \text{R2} = 500 \ \Omega, & \text{R2} = 500 \ \Omega, \\ \text{TA} = 25^{\circ}\text{C} & \text{TA} = \text{MIN to MAX}^{\circ} \end{array}$		$C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}C$		R1 = 500 Ω , R2 = 500 Ω ,				
				'BCT544		44 SN54BCT544		SN74BCT544					
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	1			
^t PLH	A or B	BorA								ns			
tPHL													
tPLH	LEBA	Α								ns			
tPHL													
tPLH	LEAB	В								ns			
tPHL													
^t PZH	G or CE	A or B								ns			
^t PZL													
t _{PHZ}	G or CE	A or B								ns			
tPLZ	G OI OL									<u> </u>			

[†] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

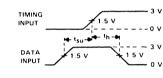


PARAMETER MEASUREMENT INFORMATION

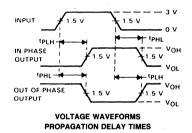


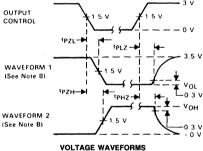
SWITCH POSITION TABLE

TEST	S1
t _{PLH}	Open
tPHL	Open
tPZH	Open
tpzL	Closed
tPHZ	Open
t _{PLZ}	Closed



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES





ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by the generators having the following characteristics: PRR \leq 10 MHz, $Z_{\Omega}=50~\Omega$, $t_{f}\leq2.5$ ns, $t_{f}\leq2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS



SN54BCT756, SN74BCT756 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

JULY 1989

- Open-Collector Version of BCT240
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-833C Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

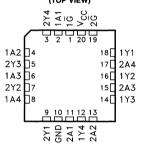
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for 3-state overlap protection. Taken together with the BCT757 and the BCT760, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{\bf G}$ (active-low input control) inputs, and complimentary $\bf G$ and $\overline{\bf G}$ inputs.

The SN54BCT756 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT756 is characterized for operation from 0°C to 70°C.

SN54BCT756 ... J PACKAGE SN74BCT756 ... DW OR N PACKAGE (TOP VIEW)

1Ğ 🏻	1 0	20] v _{cc}
1A1 🗌	2	19] 2Ğ
2Y4 🗌	3	18] 1Y1
1A2 🗌	4	17] 2A4
2Y3 🗌	5	16] 1Y2
1A3 🗌	6	15	2A3
2Y2 🗌	7	14] 1Y3
1A4 🗌	8	13] 2A2
2Y1 🗌	9	12] 1Y4
GND 🗌	10	11	2A1

SN54BCT756 ... FK PACKAGE (TOP VIEW)

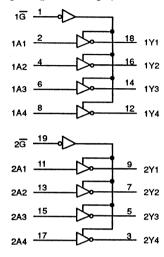


FUNCTION TABLE

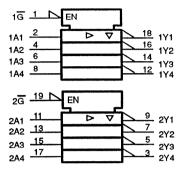
OUTPUT CONTROL				
1G, 2G	A	Υ		
L	Н	L		
L	L	Н		
н	X	z		



logic diagram (positive logic)



logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

	0.5141. 314
Supply voltage, VCC	-0.5 V to / V
Input voltage, V _I (see Note 1)	. −0.5 V to 7 V
Input current, I ₁	-30 mA to 5 mA
Voltage applied to any output in the high state	-0.5 V to 5.5 V
Current into any output in the low state: SN54BCT756	96 mA
SN74BCT756	128 mA
Operating free-air temperature range: SN54BCT756	-55°C to 125°C
SN74BCT756	0°C to 70°C
Storage temperature range	-55°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage ratings may be exceeded if the input clamp current rating is observed.



SN54BCT756, SN74BCT756 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

		SN54BCT756			SN	UNIT			
	·	MIN	NOM	MAX	MIN	NOM	MAX	J	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧	
VIH	High-level input voltage	2			2			٧	
VIL	Low-level input voltage			0.8			0.8	٧	
ΊΚ	Input clamp current			-18			-18	mA	
Vон	High-level output voltage			5.5			5.5	٧	
loL	Low-level output current			48			64	mA	
TA	Operating free-air temperature	-55		125	, 0		70	ŝ	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIO	SI	154BCT75	6	AS	UNIT				
PARAMETER	TEST CONDITIO	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT		
VIK	$V_{CC} = 4.5 \text{ V}, I_{I} = -18 \text{ mA}$				-1.2			-1.2	٧	
lОН	$V_{CC} = 4.5 V$, $V_{OH} = 5.5 V$				0.1			0.1	mA	
VOL	$V_{CC} = 4.5 V$, $I_{OL} = 48 \text{mA}$			0.38	0.55				V	
· OL	$V_{CC} = 4.5 \text{V}, I_{OL} = 64 \text{mA}$						0.42	0.55		
ſΙ	$V_{CC} = 5.5 V, V_{I} = 5.5 V$				0.1			0.1	mA	
lіН	$V_{CC} = 5.5 V, V_{I} = 2.7 V$				20			20	μΑ	
ΙΙL	$V_{CC} = 5.5 V, V_I = 0.5 V$				-1	1		-1	mA	
ICC	V _{CC} = 5.5 V, Outputs open	Outputs high		21	33		21	33	μΑ	
.00	100 010 1, 044410 04011	Outputs low		48	76		48	76	<i> </i>	
Ci	$V_{CC} = 5 \text{ V}, V_{I} = 2.5 \text{ V or } 0.5 \text{ V}$			6			6		pF	
Co	$V_{CC} = 5 \text{ V}, V_{I} = 2.5 \text{ V or } 0.5 \text{ V}$			10			10		pF	

 $[\]dagger$ All typical values are at $V_{CC} = 5$ V, $T_A = 25$ °C.

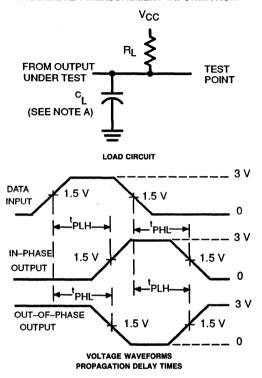
'BCT756 switching characteristics (see Figure 1)

PARAMETER	AMETER FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25^{\circ}\text{C}$			RL =	5 V to 5.5 V 50 pF, 500 Ω, N to MAX [‡]		UNIT		
			'BCT756			SN54BCT756		SN74BCT756			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	1	
tPLH	Any A	Υ		8						ns	
tPHL],			4.3							
^t PLH	Any G	Y		13						ns	
tpHI	7tily G	'		6.2]	

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.



PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

SN54BCT8244, SN74BCT8244 SCAN TEST DEVICE WITH OCTAL BUFFER

AUGUST 1989

- Device is a member of Texas Instruments SCOPE™ Family of Testability Products
- **Octal Test Integrated Circuit**
- Compatible with the Proposed IEEE P1149.1 Serial Test Bus
- Functionally Equivalent to 54/74F244 and 54/74BCT244 in the Normal Function Mode
- Implements Optional "Test Reset" Signal on TAP by Recognizing a Double-High on TMS
- **Test Operation Synchronous to Test** Access Port (TAP)
- 16 Test Instructions-Conforms to the Proposed JTAG Boundary Scan—Provides Data Compression of Inputs—Provides Pseudo-Random Pattern Generation from Outputs-Output Toggle Boundary Mode-**Outputs to High Impedance State Mode**
- Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300 mil DIPs

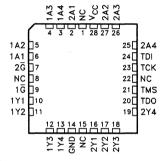
description

The SN54BCT8244 and SN74BCT8244 are members of Texas Instruments SCOPETM testability IC family. This family of components blend test circuitry with standard logic functions to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire Test Access Port (TAP) interface.

SN54BCT8244 ... JT PACKAGE SN74BCT8244 ... DW OR NT PACKAGE (TOP VIEW)

1 G 🗆	1	U 24] 2Ğ
1Y1 🛚	2	23]1A1
1 Y 2 🗌	3	22]1A2
1Y3 🗌	4	21]1A3
1Y4 🗌	5	20] 1A4
GND [6	19	2A1
2Y1[7	18	□ v _{cc}
2Y2 🗌	8	17	2A2
2Y3 🗌	9	16] 2A3
2Y4 🗌	10	15] 2A4
TDO [11	14] TDI
TMS 🗌	12	13] тск

SN54BCT8244 ... FK PACKAGE (TOP VIEW)

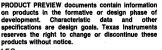


In normal mode these devices are functionally equivalent to the SN54/74F244 and SN54/74BCT244 octal buffers. In normal mode the test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE octal buffers.

In test mode the normal operation of the SCOPE octal buffer is inhibited and the test circuitry is enabled to observe and control the device's I/O boundary. When enabled, the test circuitry can perform boundary scan test operations as described in the proposed JTAG/P1149.1 specification. Additionally, the test circuitry can perform other testing functions such as: parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

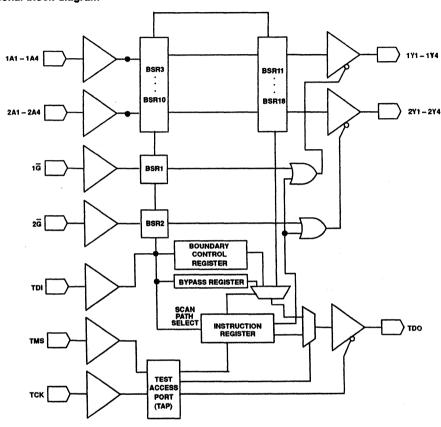
The SN54BCT8244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT8244 is characterized for operation from 0°C to 70°C.

SCOPETM is a trademark of Texas Instruments Incorporated.





functional block diagram



FUNCTION TABLE

OUTPUT CONTROL	DATA INPUT	OUTPUT								
1 G , 2 G	A	Y								
н	x	Z								
L	L	L								
L	н	н								



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, VCC	-0.5 V to 7 V
Input voltage	-0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to VCC
Current into any output in the low state: SN54BCT8244	96 mA
SN74BCT8244	128 mA
Operating free-air temperature range: SN54BCT8244	-55°C to 125°C
SN74BCT8244	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			AS.	SN54BCT8244			SN74BCT8244		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage		2		5.5	2		5.5	٧
VIHH	Double high-level input voltage	TMS	10.25	10.50	10.75	10.25	10.50	10.75	V
VIL	Low-level input voltage				0.8			0.8	٧
ЧK	Input clamp current				-18			-18	mA
ЮН	High-level output current				-12			-15	mA
lOL	Low-level output current				48			64	mA
TA	Operating free-air temperature		-55		125	0		. 70	°C



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT8244			SN74BCT8244			UNIT	
			MIN	TYP†	MAX	MIN	TYP	MAX	וואט	
VIK	$V_{CC} = 4.5 \text{ V}, \text{ I}_{I} = -18 \text{ mA}$					-1.2			-1.2	٧
VOH	$V_{CC} = 4.5 \text{V}, \ I_{OH} = -3 \text{mA}$			2.4	3.3		2.4	3.3		٧
	$V_{CC} = 4.5 \text{ V}, \ I_{OH} = -12 \text{ mA}$			2	3.2					٧
	$V_{CC} = 4.5 \text{ V}, I_{OH} = -15 \text{ mA}$						2	3.1		٧
VOL	V _{CC} = 4.5 V, I _{OL} = 48 mA				0.38	0.55				٧
	$V_{CC} = 4.5 \text{ V}, I_{OL} = 64 \text{ mA}$							0.42	0.55	٧
11	V _{CC} = 5.5 V, V _I = 5.5V					0.1			0.1	mA
liн	V _{CC} = 5.5 V, V _I = 2.7 V					20			20	μΑ
инн	TMS	$V_{CC} = 5.5V,$	V _I = 10.50 V			1			1	mA
ΊL	$V_{CC} = 5.5 \text{ V}, V_{I} = 0.5 \text{ V}$					-1			-1	mA
lozh	$V_{CC} = 5.5 \text{ V}, \ V_{O} = 2.7 \text{ V}$					50			50	μΑ
lozL	$V_{CC} = 5.5 \text{ V}, \ V_{O} = 0.5 \text{ V}$				-	-50			-50	μΑ
los‡	V _{CC} = 5.5 V, V _O = 0			-100		-225	-100		-225	mA
Icc	V _{CC} = 5.5 V, Outputs open	Outputs high			5.5			5.5		mA
		Outputs low			52			52		mA
		Outputs disabled			2.3			2.3		mA
Ci	V _{CC} = 5.0 V, V _I = 2.5 V or 0.5 V									pF
Co	V _{CC} = 5.0 V, V _O = 2.5 V or 0.5 V									pF

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



^{*} Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

'BCT8244 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_{A} = 25^{\circ}\text{C}$		V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω , R2 = 500 Ω , T _A = MIN to MAX [†]					
			'i	BCT8244	ļ.	SN54	BCT8244	SN74B	CT8244	}
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	ļ
fmax	TCK			20						MHz
^t PLH	ANY A	Υ		5.9						ns
tPHL ·	ANY A	Y		6.5						ns
^t PLH	TCK↓	Y		11.5						ns
tPHL	TCK↓	Y		11						ns
tPLH	TCK ↓	TDO		9.8						ns
tPHL	TCK.↓	TDO		9.7						ns
tPZH	ANY G	Y		5.5						ns
tPZH	TCK↓	Υ		13						ns
tPZH	TCK↓	TDO		8						ns
tPZL	ANY G	Υ		7.7						ns
tPZL	TCK↓	Y		14						ns
tPZL	TCK↓	TDO		9.2						ns
t _{PHZ}	ANY G	Y		7						ns
tPHZ	TCK↓	Y		13						ns
tPHZ	TCK↓	TDO		7						ns
tPLZ	ANY G	Y		6.7						ns
t _{PLZ}	TCK↓	Y		13						ns
tPLZ	TCK↓	TDO		7.8						ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions. NOTE 1: See General Information for load circuits and waveforms.

timing requirements (see Note 1)

			V _{CC} = 5 \ T _A = 25°		,	V _{CC} = 4.5 T _A = MIN			UNIT
			'BCT8244	ı	SN54B	CT8244	SN74B	CT8244	UNIT
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	1
fclock	TCK	0							MHz
t _w	Pulse duration TCK high or low								ns
t _{su}	Setup time, TMS before TCK ↑	9							ns
t _{su}	Setup time, TDI before TCK ↑	9							ns
t _{su}	Setup time, Any A before TCK ↑	9							ns
t _{su}	Setup time, Any G before TCK ↑	9							ns
th	Hold time, TMS after TCK↑	5							ns
^t h	Hold time, TDI after TCK ↑	5							ns
th	Hold time, Any A after TCK ↑	5							ns
th	Hold time, Any G after TCK ↑	5							ns
t _{pu}	Wait time, power-up to TCK ↑	100							ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions. NOTE 1: See General Information for load circuits and waveforms.



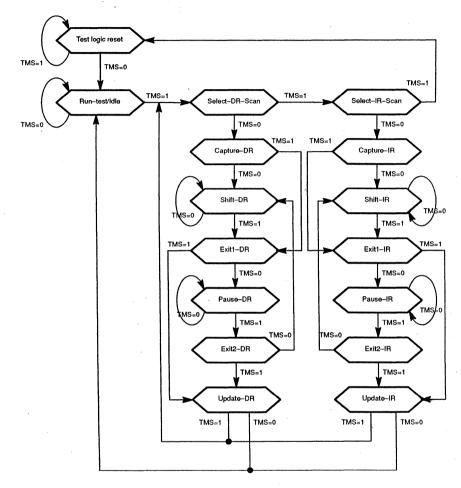


FIGURE 1. TAP STATE DIAGRAM

functional description

JTAG test information is conveyed by means of a 4-wire test bus. Test commands, test data, circuit state control instructions and synchronous control signals are all passed along the 4-wire bus. The function of the TAP is to extract the state control information and synchronous control signals from the 4-wire test bus, and generate the appropriate on-chip control signals for the JTAG test structures on the device. To accomplish this, the TAP cell monitors two signals from the 4-wire test bus—TCK (the JTAG Test Clock) and TMS (the JTAG Test Mode Select line). The functional block diagram on page 2 illustrates the JTAG 4-wire test bus and boundary scan architecture, and the relationship between the TAP cell, the 4-wire bus, and the various boundary scan test elements.

architectural elements

boundary scan register BSR0-BSR17

The boundary scan register contains eighteen (18) bits—one for each functional input or output pin of the device. FIGURE 2 illustrates the order of bits in the boundary scan register scan path. The boundary scan registers allow for board interconnect testing, defining conditions at the device logic periphery, and sampling data on the functional input or output pins without disturbing normal device operations.

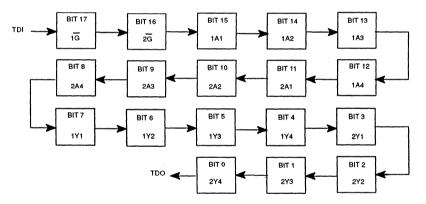


FIGURE 2. BOUNDARY SCAN REGISTER ORDER OF SCAN

bypass register

The bypass register contains one (1) bit for use when the device is in the bypass scan mode as defined in TABLE 3. FIGURE 3 illustrates the flow through the bypass register. This register provides a short one bit scan path through the device rather than scanning through the eighteen bit boundary scan register path. This is especially useful for decreasing test access times to a particular device on a board with several JTAG compatible devices which are not required for a specific test.

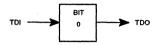


FIGURE 3. BYPASS REGISTER ORDER OF SCAN

test data register

The test data register contains two (2) bits used to control test operations occurring at the boundary. FIGURE 4 illustrates the order of bits in the test data register scan path.

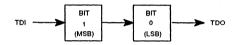


FIGURE 4. TEST DATA REGISTER ORDER OF SCAN

In addition to the boundary test instructions shown in TABLE 3, additional test operations shown in TABLE 1 can be performed when the run test opcode is installed in the instruction register. These test operations include: pseudo-random pattern generation (PRPG) and parallel signature analysis (PSA) as shown in TABLE 1 when the run test opcode is installed in the instruction register.

TABLE 1. RUN TEST OPCODES

OPCODE MSB → LSB	TEST
00	SAMPLE INPUTS/TOGGLE OUTPUTS
01	PRPG/16-BIT MODE
10	PSA/16-BIT MODE
11	SIMULTANEOUS PRPG AND PSA/8 BIT MODE



SN54BCT8244, SN74BCT8244 SCAN TEST DEVICE WITH OCTAL BUFFER

example

In order to implement the sample inputs/toggle outputs opcode from TABLE 1, a series of operations must be performed. Refer to FIGURE 1 to trace these operations through the TAP state diagram. The select-IR path is used to shift opcodes into the instruction register. The select-DR path is used to shift data into the boundary scan register or bypass register, or to shift opcodes into the test data register. To shift data or opcodes into the registers, after entering the appropriate shift-DR or shift-IR state TMS must be held low for enough TCK pulses to shift the correct number of bits into the registers.

First, the boundary read opcode (test or normal mode) must be loaded into the instruction register using the select-IR scan path, then the boundary scan registers may be initialized using the select-DR scan path. Load the test data register scan opcode (test or normal mode) into the instruction register using the select-IR scan path, then the sample inputs/toggle outputs opcode (00) may be entered into the test data register using the select-DR-scan path. Finally, the boundary run test opcode (test or normal mode) must be entered into the instruction register using the select-IR scan path. Exiting the select-IR-scan path to the run-test/idle state starts the outputs togaling. As long as the device remains in the run-test/idle state, each TCK pulse will cause the device's function outputs to toggle to the opposite state.

tap bits

Tap bit settings used for PSA and PRPG test operations are shown in TABLE 2. The use of these tap bits as well as the shift operations necessary to perform 8-bit and 16-bit PSA and PRPG test operations is described in FIGURE 5 through FIGURE 7.

TABLE 2. TAP BIT SETTINGS FOR PSA AND PRPG TEST OPERATIONS

OPERATION	MODE	TAP BITS A \rightarrow Y
PSA	8-BIT	1A2, 1A3, 1A4, 2A4
PSA	16-BIT	2A3, 1Y1, 1Y4, 2Y4
PRPG	8-BIT	1Y2, 1Y3, 1Y4, 2Y4
PRPG	16-BIT	2A3, 1Y1, 1Y4, 2Y4

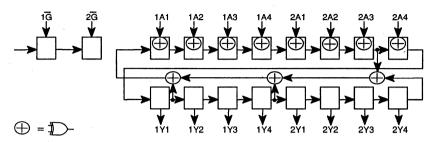


FIGURE 5. 16 BIT PSA CONFIGURATION DURING RUN TEST/IDLE STATE

A PSA operation on the 8 data inputs proceeds as the 8 data outputs are held static.

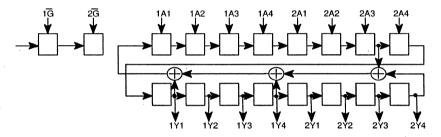


FIGURE 6. 16 BIT PRPG CONFIGURATION DURING RUN TEST/IDLE STATE

A PRPG operation from the 8 data outputs proceeds while the 8 data inputs are ignored.

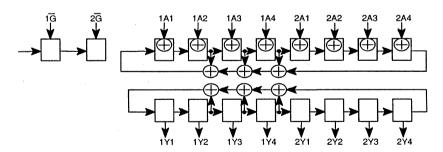


FIGURE 7. 8 BIT PSA AND PRPG CONFIGURATION DURING RUN TEST/IDLE STATE

Simultaneously, an 8 bit PSA operation proceeds on the 8 data inputs, while an 8 bit PRPG operation proceeds from the 8 data outputs.



SN54BCT8244, SN74BCT8244 SCAN TEST DEVICE WITH OCTAL BUFFER

instruction register

The test device instruction register is 8 bits in length. When in the Shift-IR state, data can be scanned into the register from the most significant bit (MSB) to the least significant bit (LSB) as shown in FIGURE 8. The instruction register controls the internal device structures and test operations according to the opcodes listed in TABLE 3.

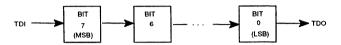


FIGURE 8. INSTRUCTION REGISTER ORDER OF SCAN

instruction set

The 'BCT8244 uses the 8-bit serial instruction register as its instruction input. TABLE 3 summarizes the 8-bit opcodes and corresponding tests.

TABLE 3. OPCODES (see Note 1)

OPCODE BIT 7-BIT 0 MSB-LSB	FUNCTION
X0000000	BOUNDARY SCAN
X0000001	ID REGISTER SCAN
X0000010	SAMPLE BOUNDARY
X0000011	BOUNDARY SCAN
X0000100	BYPASS SCAN MODE
X0000101	BYPASS SCAN MODE
X0000110	CONTROL BOUNDARY TO HIGH IMPEDANCE
X0000111	CONTROL BOUNDARY TO 1/0
X0001000	BYPASS SCAN MODE
X0001001 .	BOUNDARY RUN TEST/TEST MODE
X0001010	BOUNDARY READ/NORMAL MODE
X0001011	BOUNDARY READ/TEST MODE
X0001100	BOUNDARY SELF TEST/NORMAL MODE
X0001101	BOUNDARY TOGGLE OUTPUTS/TEST MODE
X0001110	TEST DATA REGISTER SCAN/NORMAL MODE
X0001111	TEST DATA REGISTER SCAN/TEST MODE
ALL OTHER	BYPASS SCAN MODE

X = Parity Bit (Even Parity)

NOTE 1: If Bit 4 through Bit 6 are all 0, then Bit 0 through Bit 3 are decoded as shown in TABLE 3.



SN54BCT8244, SN74BCT8244 SCAN TEST DEVICE WITH OCTAL BUFFER

The test functions which are identified in TABLE 3 and performed by the test integrated circuits are defined as follows:

boundary scan

A boundary scan of the boundary scan register is performed according to the methodology designated by the proposed JTAG or the proposed IEEE P1149.1 specifications. This instruction performs a combination of sample boundary and control boundary to 1/0 tests as specified below.

ID register scan

The test circuit is placed in the bypass mode as defined by JTAG in the absence of an ID Register. A logic 0 is loaded into the bypass register before scanning.

sample boundary

Data appearing at the device's function inputs and outputs is sampled and scanned out the TDO pin. This operation is performed in a functional mode without disturbing normal device operations.

control boundary to high impedance

The device's function outputs are placed in the high impedance state. The bypass register is selected in the scan path. Function inputs remain operational.

control boundary to 1/0

Function inputs and outputs are controlled by the boundary register. The bypass register is selected in the scan path.

boundary run test

Test operations controlled by the test data register are performed while the device is in the idle mode. Operations performed in this mode include the following:

parallel signature analysis of inputs

Data appearing on the device's data inputs is compressed by a parallel signature analysis (PSA) operation with fixed tap bits. Data shall be compressed into sixteen bits. The initial seed value for the PSA operation should be scanned into the boundary scan register prior to performing the test operation.



pseudo-random pattern generation from outputs

A pseudo-random data pattern (PRPG) is output from the outputs of the test device. The initial seed value for the PRPG should be scanned into the data register prior to performing the test operation.

simultaneous PSA and PRPG

An 8 Bit PSA of inputs and an 8 Bit PRPG from outputs is performed simultaneously as specified above.

sample inputs/toggle outputs

The devices inputs are sampled on successive rising edges of TCK, while the device's function output pins are toggled simultaneously on successive falling edges of TCK while the device is in the idle mode. This test is intended to be used for parametric testing and pattern generation purposes. The initial pattern should be scanned into the boundary scan register prior to performing the test operation.

boundary read (test mode and normal mode)

Data is scanned in and out of the boundary scan register without first preloading the boundary condition. This function is particularly useful after a PSA operation—the results can be scanned out for review by the test controller.

test data register scan (test mode and normal mode)

The test data register is selected for scan access.

boundary self test

The boundary scan register is preloaded with the inverted contents of the latch memory elements of each boundary scan register bit. The boundary scan register is then scanned out. Prior to performing this test known data should be scanned into the boundary scan register.

boundary toggle outputs

The device's function output pins are toggled simultaneously on successive TCK clock inputs. This test is intended to be used for parametric testing and pattern generation purposes. The initial pattern should be scanned into the data register prior to performing the test operation.

bypass scan mode

The bypass register is selected in the scan path and the device is placed in the normal mode.



MAY 1989

- Device is a member of Texas Instruments SCOPETM Family of Testability Products
- Octal Test Integrated Circuit
- Compatible with the Proposed IEEE P1149.1 Serial Test Bus
- Functionally Equivalent to 54/74F245 and 54/74BCT245 in the Normal Function Mode
- Implements Optional "Test Reset" Signal on TAP by Recognizing a Double-High on TMS Pin
- Test Operation Synchronous to Test Access Port (TAP)
- 16 Test Instructions—Conforms to the Proposed JTAG Boundary Scan—Provides Data Compression of Inputs—Provides Pseudo-Random Pattern Generation from Outputs—Output Toggle Boundary Mode— Outputs to High Impedance State Mode
- Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300 mil DIPs

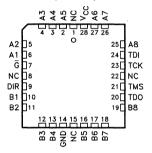
SN54BCT8245 ... JT PACKAGE SN74BCT8245 ... DW OR NT PACKAGE

(TOP VIEW) DIR [в1 Г 23 A1 В2 П 22 A2 взГ 21 A3 в4 П 20 A4 GND ∏6 19 A5 B5 🗖 7 18 V_{CC} в6 Пв 17 🛮 A6 В7 П9 16 A7 B8 ∏10 15 A8 TDO []11 14 TDI

SN54BCT8245 ... FK PACKAGE (TOP VIEW)

13 TCK

TMS 12



description

The SN54BCT8245 and SN74BCT8245 are members of Texas Instruments SCOPE™ testability IC family. This family of components blend test circuitry with standard logic functions to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire Test Access Port (TAP) interface. In normal mode these devices are functionally equivalent to the SN54/74F245 and SN54/74BCT245 octal transceivers. In normal mode the test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE octal buffers.

In test mode the normal operation of the SCOPE octal buffer is inhibited and the test circuitry is enabled to observe and control the device's I/O boundary. When enabled, the test circuitry can perform boundary scan test operations as described in the proposed JTAG/P1149.1 specification. Additionally, the test circuitry can perform other testing functions such as: parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54BCT8245 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74BCT8245 is characterized for operation from 0°C to 70°C.

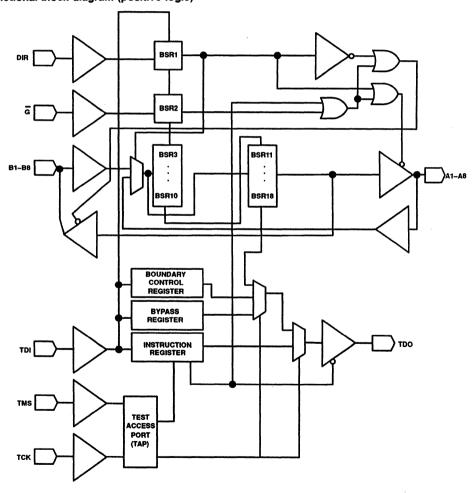
SCOPETM is a trademark of Texas Instruments Incorporated.



NORMAL MODE FUNCTION TABLE

ENABLE G	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	х	Isolation

functional block diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC}	-0.5	V to 7 V
Input voltage	-0.5	V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V	to 5.5 V
Voltage applied to any output in the high state	-0.5 V	to VCC
Current into any output in the low state: SN54BCT8245 (A1 thru A8)		40 mA
SN54BCT8245 (B1 thru B8)		96 mA
SN74BCT8245 (A1 thru A8)		
SN74BCT8245 (B1 thru B8)		128 mA
Operating free-air temperature range: SN54BCT8245	-55°C t	o 125°C
SN74BCT8245	0°C	to 70°C
Storage temperature range	-65°C t	o 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			SN	54BCT82	45	SN	74BCT82	45	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage		2		5.5	2		5.5	٧
VIHH	Double high-level input voltage	TMS	10.25	10.50	10.75	10.25	10.50	10.75	٧
VIL	Low-level input voltage				0.8			0.8	V
lik	Input clamp current				-18			-18	mA
lou	High-level output current	A1 thru A8			-3			-3	mA
ЮН	riigii-level output current	B1 thru B8			-12			-15	111/
1	I am laval autout autout	A1 thru A8			20			24	mA
IOL	Low-level output current	B1 thru B8			48			64	11114
TA	Operating free-air temperature	\ \	-55		125	0		70	°C



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DAE	RAMETER	TEST CONDITIONS	SN	54BCT82	45	SN74BCT8245			UNIT		
PAF	AMEIER	TEST CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII		
٧ıĸ		$V_{CC} = 4.5 \text{ V}, I_{I} = -18 \text{ mA}$				-1.2			-1.2	٧	
	Any output	$V_{CC} = 4.75 \text{ V}, I_{OH} = -1 \text{ mA to } -3 \text{ mA}$	4				2.7				
	Δ1 thru Δ8	V _{CC} = 4.5 V	IOH = -1 mA	2.5	3.4		2.5	3.4			
۷он	AT UIIU AO	VCC - 4:5 V	IOH = -3 mA	2.4	3.3		2.4	3.3		V	
- 011	B1 thru B9	V _{CC} = 4.5 V	IOH = -12 mA	2	3.2						
	טו וווע טט	VCC - 4:5 V	IOH = -15 mA				2	3.1			
	A1 thru A8	Voc = 45V	$I_{OL} = 20 \text{ mA}$		0.3	0.5					
VOL	A1 thru A8 V _{CC} = 4.5 V		IOL = 24 mA	1				0.35	0.5	_v	
·OL	R1 thru R9	V _{CC} = 4.5 V	$I_{OL} = 48 \text{ mA}$		0.38	0.55				'	
	טו וווע טט	VCC - 4:5 V	$I_{OL} = 64 \text{ mA}$					0.42	0.55		
l.	DIR and G	V _{CC} = 5.5 V	V _I = 7 V			0.1			0.1	mA	
lj .	A and B	V _{CC} = 5.5 V	V _I = 5.5 V			1			1	IIIA	
lн	A and B	$V_{CC} = 5.5 V, V_{I} = 2.7 V$				70			70	μΑ	
чH	other	$V_{CC} = 5.5 V, V_{I} = 2.7 V$				20			20	μΛ	
Ιнн	TMS	$V_{CC} = 5.5 \text{ V}, V_I = 10.50 \text{ V}$				1			1	mA	
Ιμ	A and B	$V_{CC} = 5.5 V, V_I = 0.5 V$				-0.65			-0.65	mA	
IIL.	other	$V_{CC} = 5.5 V, V_{I} = 0.5 V$				-1.2			-1.2	шА	
los‡	A1 thru A8	$V_{CC} = 5.5 V, V_{O} = 0$		-60		- 150	-60		- 150	mA	
105.	B1 thru B8	$V_{CC} = 5.5 V V_{O} = 0$		-100		-225	-100		-225	ш	
			Outputs high		5.5			5.5			
ICC		V _{CC} = 5.5 V, Outputs open	Outputs low		52 53		52		mA		
			Outputs disabled		2.3			2.3			
Ci		$V_{CC} = 5.0 \text{ V}, V_{I} = 2.5 \text{ V or } 0.5 \text{ V}$								pF	
Cio		$V_{CC} = 5.0 \text{ V}, V_{O} = 2.5 \text{ V or } 0.5 \text{ V}$								pF	

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25°C.



[‡] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

timing requirements (see Note 1)

			/ _{CC} = 5 V, T _A = 25°C			V _{CC} = 4.5 V T _A = MIN			UNIT
			'BCT8245		SN54BC	T8245	SN74BC	T8245	UNII
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fclock	TCK	0							MHz
t _W	Pulse duration TCK high or low								ns
t _{su}	Setup time, TMS before TCK ↑	9							ns
t _{su}	Setup time, TDI before TCK ↑	9							ns
t _{su}	Setup time, Any A or B before TCK ↑	9							ns
t _{su}	Setup time, G before TCK↑	9							ns
th	Hold time, TMS after TCK ↑	1							ns
th	Hold time, TDI after TCK ↑	1							ns
th	Hold time, Any A or B after TCK ↑	1							ns
th	Hold time, G after TCK ↑	1							ns
t _{pu}	Wait time, power-up to TCK ↑	100							ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions. NOTE 1: See General Information for load circuits and waveforms.



'BCT8245 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C		SN54BC	UNIT						
			MIN	TYP	MAX	MIN	MAX	SN74BC MIN	MAX			
fmax	TCK	L		20						MHz		
tPLH	A or B	B or A		5.9						ns		
tPHL	7,015	2017		6.5						"		
tPLH	TCK↓	A or B		11.5						ns		
tPHL		7.0.2		11]		
^t PLH	TCK↓	TDO		9.8						ns		
tPHL				9.7						,,,		
^t PZH	G	A or B		6.2						ns		
tPZL				13								
^t PZH	TCK↓	A or B		8						ns		
tPZL				7.7								
tPZH	TCK↓	TDO		14						ns		
tPZL	•			9.2								
^t PHZ	G	A or B		7.5						ns		
^t PLZ				13								
tPHZ	TCK↓	A or B		7						ns		
tPLZ	•			6.7								
tPHZ	TCK↓	TDO		13						ns		
tPLZ .				7.8								

[†] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions. NOTE 1: See General Information for load circuits and waveforms.



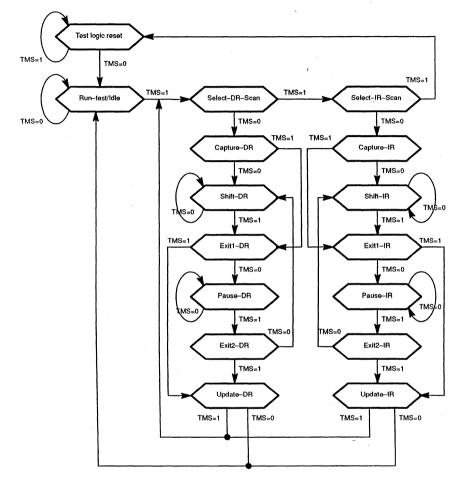


FIGURE 1. TAP STATE DIAGRAM

functional description

JTAG test information is conveyed by means of a 4-wire test bus. Test commands, test data, circuit state control instructions and synchronous control signals are all passed along the 4-wire bus. The function of the TAP is to extract the state control information and synchronous control signals from the 4-wire test bus, and generate the appropriate on-chip control signals for the JTAG test structures on the device. To accomplish this, the TAP cell monitors two signals from the 4-wire test bus—TCK (the JTAG Test Clock) and TMS (the JTAG Test Mode Select line). The functional block diagram on page 2 illustrates the JTAG 4-wire test bus and boundary scan architecture, and the relationship between the TAP cell, the 4-wire bus, and the various boundary scan test elements.

architectural elements

boundary scan register BSR0-BSR17

The boundary scan register contains eighteen (18) bits—one for each functional input or output pin of the device. FIGURE 2 illustrates the order of bits in the boundary scan register scan path. The boundary scan registers allow for board interconnect testing, defining conditions at the device logic periphery, and sampling data on the functional input or output pins without disturbing normal device operations.

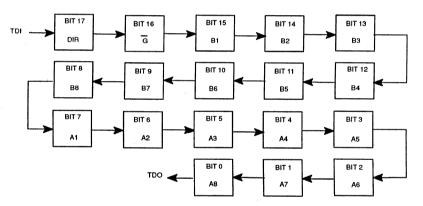


FIGURE 2. BOUNDARY SCAN REGISTER ORDER OF SCAN

bypass register

The bypass register contains one (1) bit for use when the device is in the bypass scan mode as defined in TABLE 3. FIGURE 3 illustrates the flow through the bypass register. This register provides a short one bit scan path through the device rather than scanning through the eighteen bit boundary scan register path. This is especially useful for decreasing test access times to a particular device on a board with several JTAG compatible devices which are not required for a specific test.

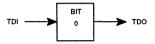


FIGURE 3. BYPASS REGISTER ORDER OF SCAN

test data register

The test data register contains two (2) bits used to control test operations occurring at the boundary. FIGURE 4 illustrates the order of bits in the test data register scan path.

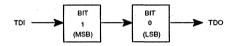


FIGURE 4. TEST DATA REGISTER ORDER OF SCAN

In addition to the boundary test instructions shown in TABLE 3, additional test operations shown in TABLE 1 can be performed when the run test opcode is installed in the instruction register. These test operations include: pseudo-random pattern generation (PRPG) and parallel signature analysis (PSA) as shown in TABLE 1 when the run test opcode is installed in the instruction register.

TABLE 1. RUN TEST OPCODES

OPCODE MSB → LSB	TEST
00	SAMPLE INPUTS/TOGGLE OUTPUTS
01	PRPG/16 BIT MODE
10	PSA/16 BIT MODE
11	SIMULTANEOUS PRPG AND PSA/8 BIT MODE



example

In order to implement the sample inputs/toggle outputs opcode from TABLE 1, a series of operations must be performed. Refer to FIGURE 1 to trace these operations through the TAP state diagram. The select-IR path is used to shift opcodes into the instruction register. The select-DR path is used to shift data into the boundary scan register or bypass register, or to shift opcodes into the test data register. To shift data or opcodes into the registers, after entering the appropriate shift-DR or shift-IR state TMS must be held low for enough TCK pulses to shift the correct number of bits into the registers.

First, the boundary read opcode (test or normal mode) must be loaded into the instruction register using the select-IR scan path, then the boundary scan registers may be initialized using the select-DR scan path. Load the test data register scan opcode (test or normal mode) into the instruction register using the select-IR scan path. then the sample inputs/toggle outputs opcode (00) may be entered into the test data register using the select-DR-scan path. Finally, the boundary run test opcode (test or normal mode) must be entered into the instruction register using the select-IR scan path. Exiting the select-IR-scan path to the run-test/idle state starts the outputs toggling. As long as the device remains in the run-test/idle state, each TCK pulse will cause the device's function outputs to toggle to the opposite state.

tap bits

Tap bit settings used for PSA and PRPG test operations are shown in TABLE 2. The use of these tap bits as well as the shift operations necessary to perform 8-bit and 16-bit PSA and PRPG test operations is described in FIGURE 5 through FIGURE 7.

TABLE 2. TAP BIT SETTINGS FOR PSA AND PRPG TEST OPERATIONS

OPERATION	MODE	TAP BITS A → Y
PSA	8-BIT	B2, B3, B4, B8
PSA	16-BIT	B7, A1, A4, A8
DDDC	8-BIT	A2, A3, A4, A8
PRPG	16-BIT	B7, A1, A4, A8



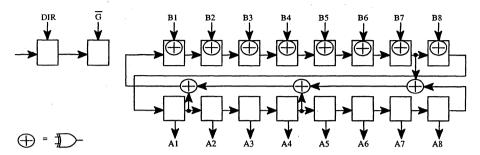


FIGURE 5. 16-BIT PSA CONFIGURATION DURING RUN TEST/IDLE STATE

A PSA operation on the 8 data inputs proceeds as the 8 data outputs are held static.

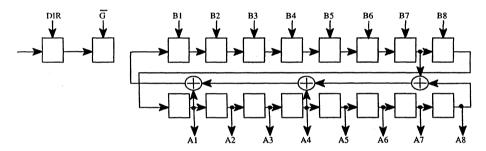


FIGURE 6. 16-BIT PRPG CONFIGURATION DURING RUN TEST/IDLE STATE

A PRPG operation from the 8 data outputs proceeds while the 8 data inputs are ignored.

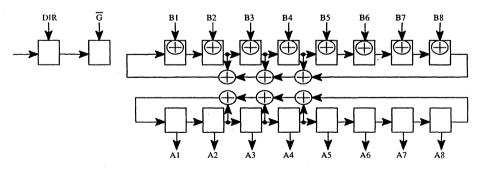


FIGURE 7. 8-BIT PSA AND PRPG CONFIGURATION DURING RUN TEST/IDLE STATE

Simultaneously, an 8-bit PSA operation proceeds on the 8 data inputs, while an 8-bit PRPG operation proceeds from the 8 data outputs.



instruction register

The test device instruction register is 8 bits in length. When in the Shift-IR state, data can be scanned into the register from the most significant bit (MSB) to the least significant bit (LSB) as shown in FIGURE 8. The instruction register controls the internal device structures and test operations according to the opcodes listed in TABLE 3.

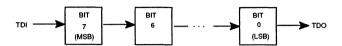


FIGURE 8. INSTRUCTION REGISTER ORDER OF SCAN

instruction set

The 'BCT8245 uses the 8-bit serial instruction register as its instruction input. TABLE 3 summarizes the 8-bit opcodes and corresponding tests.

TABLE 3. OPCODES (see Note 1)

OPCODE BIT 7-BIT 0 MSB-LSB	FUNCTION
X0000000	BOUNDARY SCAN
X000001	ID REGISTER SCAN
X0000010	SAMPLE BOUNDARY
X0000011	BOUNDARY SCAN
X0000100	BYPASS SCAN MODE
X0000101	BYPASS SCAN MODE
X0000110	CONTROL BOUNDARY TO HIGH IMPEDANCE
X0000111	CONTROL BOUNDARY TO 1/0
X0001000	BYPASS SCAN MODE
X0001001	BOUNDARY RUN TEST/TEST MODE
X0001010	BOUNDARY READ/NORMAL MODE
X0001011	BOUNDARY READ/TEST MODE
X0001100	BOUNDARY SELF TEST/NORMAL MODE
X0001101	BOUNDARY TOGGLE OUTPUTS/TEST MODE
X0001110	TEST DATA REGISTER SCAN/NORMAL MODE
X0001111	TEST DATA REGISTER SCAN/TEST MODE
ALL OTHER	BYPASS SCAN MODE

X = Parity Bit (Even Parity)

NOTE 1: If Bit 4 through Bit 6 are all 0, then Bit 0 through Bit 3 are decoded as shown in TABLE 3.



The test functions which are identified in TABLE 3 and performed by the test integrated circuits are defined as follows:

boundary scan

A boundary scan of the boundary scan register is performed according to the methodology designated by the proposed JTAG or the proposed IEEE P1149.1 specifications. This instruction performs a combination of sample boundary and control boundary to 1/0 tests as specified below.

ID register scan

The test circuit is placed in the bypass mode as defined by JTAG in the absence of an ID Register. A logic 0 is loaded into the bypass register before scanning.

sample boundary

Data appearing at the device's function inputs and outputs is sampled and scanned out the TDO pin. This operation is performed in a functional mode without disturbing normal device operations.

control boundary to high impedance

The device's function outputs are placed in the high impedance state. The bypass register is selected in the scan path. Function inputs remain operational.

control boundary to 1/0

Function inputs and outputs are controlled by the boundary register. The bypass register is selected in the scan path.

boundary run test

Test operations controlled by the test data register are performed while the device is in the idle mode. Operations performed in this mode include the following:

parallel signature analysis of inputs

Data appearing on the device's data inputs is compressed by a parallel signature analysis (PSA) operation with fixed tap bits. Data shall be compressed into sixteen bits. The initial seed value for the PSA operation should be scanned into the boundary scan register prior to performing the test operation.

pseudo-random pattern generation from outputs

A pseudo-random data pattern (PRPG) is output from the outputs of the test device. The initial seed value for the PRPG should be scanned into the data register prior to performing the test operation.

simultaneous PSA and PRPG

An 8-Bit PSA of inputs and an 8-Bit PRPG from outputs is performed simultaneously as specified above.

sample inputs/toggle outputs

The devices inputs are sampled on successive rising edges of TCK, while the device's function output pins are toggled simultaneously on successive falling edges of TCK while the device is in the idle mode. This test is intended to be used for parametric testing and pattern generation purposes. The initial pattern should be scanned into the boundary scan register prior to performing the test operation.



boundary read (test mode and normal mode)

Data is scanned in and out of the boundary scan register without first preloading the boundary condition. This function is particularly useful after a PSA operation—the results can be scanned out for review by the test controller.

test data register scan (test mode and normal mode)

The test data register is selected for scan access.

boundary self test

The boundary scan register is preloaded with the inverted contents of the latch memory elements of each boundary scan register bit. The boundary scan register is then scanned out. Prior to performing this test known data should be scanned into the boundary scan register.

boundary toggle outputs

The device's function output pins are toggled simultaneously on successive TCK clock inputs. This test is intended to be used for parametric testing and pattern generation purposes. The initial pattern should be scanned into the data register prior to performing the test operation.

bypass scan mode

The bypass register is selected in the scan path and the device is placed in the normal mode.



SN74BCT29821, SN74BCT29822 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D3125, FEBRUARY 1989-REVISED JULY 1989

- BiCMOS Process with CMOS Inputs and TTL Outputs Substantially Reduces Standby Current
- Input has 50-kΩ Pullup Resistor
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State
- Buffered Control Inputs to Reduce DC Loading Effects
- Functionally Equivalent to Am29821A, Am29822A, SN74ALS29821, and SN74ALS29822
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

These 10-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs on the 'BCT29821 will be true, and on the 'BCT29822 will be complementary to the data input.

A buffered output-control (OC) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a highimpedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74BCT' family is characterized for operation from 0°C to 70°C.

SN74BCT29821 ... DW OR NT PACKAGE (TOP VIEW)

OC 🔲 1	O 24	$\square \vee_{cc}$
1 D 🔲 2	23]1Q
2D 🛮 3	22] 2Q
3D 🛮 ₄	21] 3Q
4D 🛮 5	20] 4Q
5D ∏ 6	19] 5Q
6D 🔲 7	18] 6Q
7D 🗌 8	17] 7Q
8D 🛮 9	16] 8Q
9D [[10	15] 9Q
10D 🗆 1	1 14]10Q
GND T1:	2 13	CLK

SN74BCT29822 ... DW OR NT PACKAGE (TOP VIEW)

oc 🗆	1	U 24	\square \lor cc
1 D 🗌	2	23]1Q
2D 🗌	3	22] 2Q
3D 🗌	4	21] 3Q
4Ū 🗌	5	20] 4Q
5D 🗌	6	19] 5Q
6D 🗌	7	18] 6Q
7Ē 🗌	8	17] 7Q
8D 🗌	9	16] 8Q
9D 🗌	10	15] 9Q
10D 🗌	11	14] 10Q
GND 🗌	12	13	□ cĽĸ

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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SN74BCT29821 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

FUNCTION TABLE (EACH FLIP-FLOP) 'BCT29821

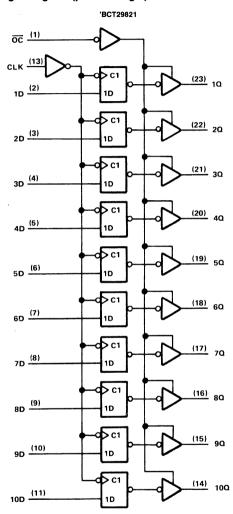
	INPUTS		OUTPUT
ÖC	CLK	D	Q
L	1	Н	н
L	1	L	L
L	L	X	Q ₀
Н	X	X	z

'BCT29821

logic symbol†

(1), \overline{oc} (13) CLK C1 (2) (23)1D 10 1D Δ (3) (22)2D - 20 (4) (21) 3D 30 (5) (20) 4D 40 (6) (19) 5D -5Q (7) (18) 6D 60 (17) (8) 7D 7Q (16) (9) 8D - 8Q (10) (15) 9D - 9Q (14) (11) 10D 10Q

logic diagram (positive logic)





[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE (EACH FLIP-FLOP) 'BCT29822

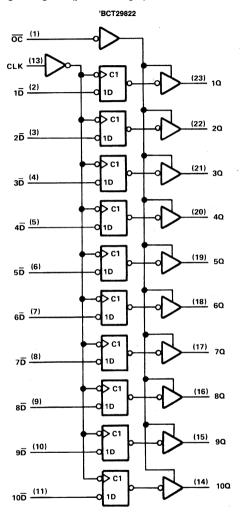
	INPUTS		OUTPUT
<u>oc</u>	CLK	D	Q
L	1	Н	L
L	↑	L	н
L	L	X	Q ₀
' Н	Х	Х	z

logic symbol[†]

'BCT29822

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		7 V
Input voltage		. 7 V
Voltage applied to a disabled 3-state output		5.5 V
Operating free-air temperature range	. 0°C to	70°C
Storage temperature range	-65°C to	150°C



SN74BCT29821 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

recommended operating conditions

		_	MIN	NOM	MAX	UNIT	
VCC	Supply voltage		4.5	5	5.5	V	
VIH	High-level input voltage		2			V	
VIL	Low-level input voltage				0.8	V	
ЮН	High-level output current				-24	mA .	
IOL	Low-level output current				48	mA	
tw	Pulse duration	CLK high	7			ns	
, w	· diss duration	CLK low	 7				
t _{su}	Setup time, data before CLK 1		7			ns	
th	Hold time, data after CLK↑		1			ns	
TA	Operating free-air temperature		0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 \text{ V, I}_{I} = -18 \text{ mA}$				-1.2	V
Voн	$V_{CC} = 4.5 \text{ V}, I_{OH} = -15 \text{ mA}$		2.4	3.3		V
•011	$V_{CC} = 4.5 \text{ V}, I_{OH} = -24 \text{ mA}$		2			
VOL	V _{CC} = 4.5 V, I _{OL} = 48 mA	$V_{CC} = 4.5 \text{ V}, I_{OL} = 48 \text{ mA}$				٧
lozh	$V_{CC} = 5.5 \text{ V}, V_{O} = 2.4 \text{ V}$				20	μΑ
IOZL	$V_{CC} = 5.5 \text{ V}, V_{O} = 0.4 \text{ V}$				-20	μΑ
lį	V _{CC} = 5.5 V, V _I = 7 V				0.1	mA
lін	$V_{CC} = 5.5 \text{ V}, V_{I} = 2.7 \text{ V}$	·	-10		-75	μΑ
IIL	$V_{CC} = 5.5 \text{ V}, V_{I} = 0.4 \text{ V}$				-0.2	mA
los‡	$V_{CC} = 5.5 \text{ V}, V_{O} = 0$		-75		-250	mA
ICC		Outputs high		6	- 10	
	V _{CC} = 5.5 V	Outputs low		25	35	mA
		Outputs disabled		2	6	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _I R1 R2	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ R1 = 500 Ω, R2 = 500 Ω, $T_A = 25^{\circ}\text{C}$		C _L = R1 = R2 =	5 V to 5.5 V, 50 pF, 500 Ω, 500 Ω, C to 70°C	UNIT
			MIN	TYP	MAX	MIN	MAX	
tPLH	CLK	Any Q	1.5	7.5	10	1.5	12	ns
tPHL		/, ~	1.5	6.5	9	1.5	10	
tPZH	ŌC	Any Q	2	7.5	10	2	12	ns
tPZL		/, ~	2	9	12	2	13	
tPHZ	ŌC	Any Q	2	5	7	2	8	ns
tPLZ		,	2	5	7	2	8	



^{*} Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

recommended operating conditions

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	٧
VIH	High-level input voltage		 2			٧
VIL	Low-level input voltage				0.8	٧
ЮН	High-level output current				-24	mA
lOL	Low-level output current				48	mA
tw	Pulse duration	CLK high				ns
·w	r diso daration	CLK low		***************************************		113
tsu	Setup time, data before CL	K↑				ns
th	Hold time, data after CLK 1					ns
TA	Operating free-air temperat	ure	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIK	$V_{CC} = 4.5 \text{ V, I}_{I} = -18 \text{ mA}$				-1.2	٧
Voн	$V_{CC} = 4.5 \text{ V, I}_{OH} = -15 \text{ mA}$		2.4	3.3		V
	$V_{CC} = 4.5 \text{V}, \text{IOH} = -24 \text{mA}$		2			
VOL	$V_{CC} = 4.5 \text{ V}, I_{OL} = 48 \text{ mA}$			0.35	0.5	٧
lozh	$V_{CC} = 5.5 \text{ V}, V_{O} = 2.4 \text{ V}$				20	μΑ
lozL	$V_{CC} = 5.5 \text{ V}, V_{O} = 0.4 \text{ V}$				-20	μΑ
lı	V _{CC} = 5.5 V, V _I = 7 V				0.1	mA
ήн	V _{CC} = 5.5 V, V _I = 2.7 V		-10		-75	μΑ
ΊL	V _{CC} = 5.5 V, V _I = 0.4 V				-0.2	mA
los‡	$V_{CC} = 5.5 \text{ V}, V_{O} = 0$		-75		-250	mA
	,	Outputs high		6		
ICC	$V_{CC} = 5.5 V$	Outputs low		25		mA
		Outputs disabled		2		

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _I R: R:	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_{A} = 25^{\circ}\text{C}$		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 0^{\circ}\text{C to } 70^{\circ}\text{C}$		UNIT
			MIN	TYP	MAX	MiN	MAX	
tPLH .	CLK	Any Q		7.5				ns
tPHL]	1, _		6.5				
tPZH	<u>oc</u>	Any Q		7.5				ns
tPZL:	1	7.1.7		9				
^t PHZ	ŌC	Any Q		5				ns
tPLZ		/, =		5				

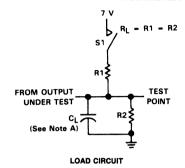


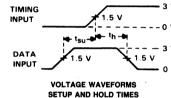
[‡] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

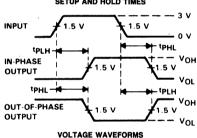
3 V

SN74BCT29821, SN74BCT29822 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



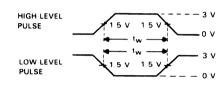




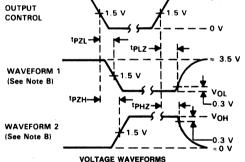
PROPAGATION DELAY TIMES

SWITCH POSITION TABLE

TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed







ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by the generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.

FIGURE 1. SWITCHING CHARACTERISTICS



SN74BCT29823, SN74BCT29824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D3181, NOVEMBER 1988-REVISED JULY 1989

- **BiCMOS Process with TTL Inputs and Outputs**
- **BiCMOS Design Substantially Reduces** Standby Current
- Functionally Equivalent to AMD Am29823. Am29824, 'ALS29823, and 'ALS29824
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with **Parity**
- Power-Up High-Impedance State
- Buffered Control Inputs to Reduce DC Loading Effects
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

These 9-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working reaisters.

With the clock enable (CLKEN) low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high will disable the clock buffer, thus latching the outputs. The 'BCT29823 has noninverting D inputs and the 'BCT29824 has inverting D inputs. Taking the CLR input low causes the nine Q outputs to go low independently of the clock.

SN74BCT29823 ... DW OR NT PACKAGE (TOP VIEW)

ōc [1	24] v _{cc}
1 D 🗌	2	23]1Q
2D [3	22] 2Q
3D 🗌	4	21] 3Q
4D 🗌	5	20] 4Q
5D 🗌	6	19] 5Q
6D 🗌	7	18] 6Q
7D 🗌	8	17] 7Q
8Ď [9	16] 8Q
9D 🗌	10	15] 9Q
CLR [11	14	CLKEN
GND [12	13] CLK

SN74BCT29824 ... DW OR NT PACKAGE (TOP VIEW)

OC [1	U24		Vcc
1 D [2	23	b	1Q
2Ō 🗌	3	22		2Q
3D 🗌	4	21		3Q
4D [5	20		4Q
5D [6	19		5Q
6D 🗆	7	18		6Q .
7Ō [8	17		7Q
8Ū 🗌	9	16	Р	8Q
9D 🗌	10	15	þ	9Q
CLR [11	14		CLKEN
GND [12	13		CLK

A buffered output-control input (\overline{OC}) can be used to place the nine outputs in either normal logic state (high or low level) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powereddown. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The highimpedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops.

Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74BCT29823 and SN74BCT29824 are characterized for operation from 0° to 70°C.

information on new products in the sampling or preproduction phase of development. Characteristic ita and other specifications are subject to change

documents



ADVANCE

without notice.

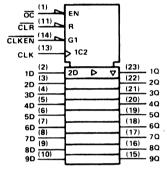
INFORMATION

SN74BCT29823 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

FUNCTION TABLE

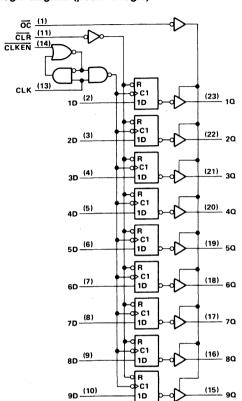
		INPUTS			OUTPUT
<u>oc</u>	CLR	CLKEN	CLK	D	œ
L	L	Х	х	Х	L
L	Н	L	1	н	н
L	н	L	1	L	L
L	Н	н	Х	X	Q ₀
н	Х	X	Х	Х	z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

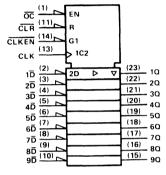




FUNCTION TABLE

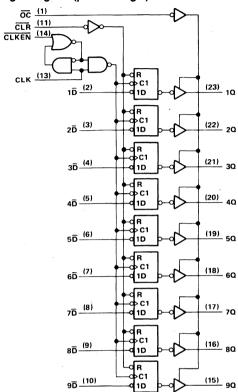
	OUTPUT				
ŌC	CLR	CLKEN	CLK	D	Q
L	L	Х	Х	Х	L
L	H	L	1	Н	L
L	Н	L	1	L	н
L	Н	н	X	X	Q ₀
Н	X	X	X	Χ	Z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SN74BCT29823, SN74BCT29824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

nerwise noted)
7 V
7 V
5.5 V
0°C to 70°C
−65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	V
VIH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	٧
ЮН	High-level output current				-24	mA
JOL	Low-level output current				48	mA
t _w	w Pulse duration	CLR low	6			ns
·w	r alos daration	CLK high or low	7	7		
		CLR inactive	2			
t _{su}	Setup time before CLK ↑	Data	7			l ns
•su	Cottap time Soloro CERT	CLKEN high	6			
		CLKEN low	8			
th	Hold time	CLKEN	0			ns
411		Data	1			'''
TA	Operating free-air temperature		0		70	°C



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V$	$I_{\text{I}} = -18 \text{ mA}$			-1.2	V
Voн	$V_{CC} = 4.5 V$	$I_{OH} = -15 \text{mA}$	2.4	3.2		V
011	$V_{CC} = 4.5 V$	$I_{OH} = -24 \text{ mA}$	2			·
VOL	$V_{CC} = 4.5 V$	$I_{OL} = 48 \text{ mA}$		0.35	0.5	٧
lozh	$V_{CC} = 5.5 V$	$V_O = 2.7 V$			20	μΑ
lozl	$V_{CC} = 5.5 V$	$V_O = 0.4 V$			-20	μΑ
l _l .	$V_{CC} = 5.5 V$	$V_{ } = 5.5 V$			0.1	mA
lн	$V_{CC} = 5.5 V$	$V_{\parallel} = 2.7 V$	-10		-75	μΑ
ΙΙL	$V_{CC} = 5.5 V$	$V_{ } = 0.4 \text{ V}$			-0.2	mA
los‡	$V_{CC} = 5.5 V$,	$V_O = 0$	-75		-250	mA
		Outputs high		6	10	
Icc	V _{CC} = 5.5 V	Outputs low		25	35	mA
		Outputs disabled		2	6	

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25°C.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2	$V_{CC} = 5 V,$ $C_{L} = 50 pF,$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_{A} = 25^{\circ}C$		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ R1 = 500 Ω, R2 = 500 Ω, $T_A = 0^{\circ}\text{C to } 70^{\circ}\text{C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	CLK	Any Q	1.5	7.5	10	1.5	12	ns
†PHL		7 my G	1.5	6.5	9	1.5	10	1
tPHL	CLR	Any Q	1.5	7.5	10	1.5	12	ns
^t PZH	ŌC	Any Q	2	7.5	10	2	12	ns
tPZL	00	/, G	2	9	12	2	13] '''
tPHZ	ōc	Any Q	2	5	7	2	8	ns
tPLZ	1	,, Q	2	5	7	2	8]



[‡] Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

SN74BCT29824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 V$	I _I = -18 mA			-1.2	V
VOH	$V_{CC} = 4.5 V,$	I _{OH} = -15 mA	2.4	3.2		V
1011	$V_{CC} = 4.5 V,$	IOH = -24 mA	2			•
VOL	$V_{CC} = 4.5 V,$	$I_{OL} = 48 \text{ mA}$		0.35	0.5	٧
lozh	$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			20	μΑ
IOZL	$V_{CC} = 5.5 V$,	$V_O = 0.4 V$			-20	μΑ
l _l	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1	mA
ήн	$V_{CC} = 5.5 V,$	$V_I = 2.7 V$	-10		-75	μΑ
IIL	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.2	mA
los‡	$V_{CC} = 5.5 V$	$V_O = 0$	-75		-250	mA
		Outputs high		6		
ICC	V _{CC} = 5.5 V	Outputs low		25		mA
		Outputs disabled		2		

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _I R1	$\begin{array}{c} \text{V}_{\text{CC}} = 5 \text{ V,} \\ \text{C}_{\text{L}} = 50 \text{ pF,} \\ \text{R1} = 500 \ \Omega, \\ \text{R2} = 500 \ \Omega, \\ \text{T}_{\text{A}} = 25^{\circ}\text{C} \\ \text{MIN} \qquad \text{TYP} \qquad \text{MAX} \end{array}$		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 0^{\circ}\text{C to } 70^{\circ}\text{C}$ MIN MAX		UNIT	
tPLH	CLK	Any Q		7.5				ns	
tPHL				6.5					
tPHL	CLR	Any Q		7.5				ns	
^t PZH	ōc	Any Q		7.5				ns	
tPZL				9]	
tPHZ	ŌC	Any Q		5				ns	
tPLZ				5					

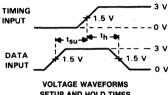


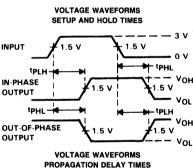
[‡] Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

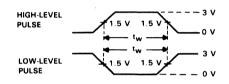
PARAMETER MEASUREMENT INFORMATION 7 V RL = R1 = R2 SWITCH TEST UNDER TEST UNDER TEST POINT TOTAL TIMING TEST TOTAL T

SWITCH POSITION TABLE

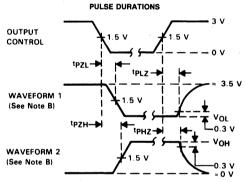
TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed







VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C. includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by the generators having the following characteristics: PRR \leq 10 MHz, $Z_0=50~\Omega,~t_f\leq$ 2.5 ns. $t_f\leq$ 2.5 ns.

FIGURE 1. SWITCHING CHARACTERISTICS



SN74BCT29841, SN74BCT29842 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D3226, MARCH 1989 - REVISED JULY 1989

- **BiCMOS Process with CMOS Inputs and** TTL Outputs Substantially Reduces Standby Current
- 3-State Buffer-Type Outputs Drive Bus **Lines Directly**
- **Bus-Structured Pinout**
- Input Has 50-kΩ Pullup Resistor
- **Provide Extra Bus Driving Latches** Necessary for Wider Address/Data Paths or **Buses with Parity**
- Buffered Control Inputs to Reduce DC Loading
- Power-Up High-Impedance State
- Functionally Equivalent to Am29841A. Am29842A, SN74ALS29841, and SN74ALS29842
- Package Options include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

These 10-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type. The 'BCT29841 has noninverting data (D) inputs. The 'BCT29842 has inverting \overline{D} inputs.

SN74BCT29841 ... DW OR NT PACKAGE (TOP VIEW)

ōc□	1	U 24	□v _{cc}
1D[2	23]1Q
2D[3	22]2Q
3D[4	21]3Q
4D[5	20	□4Q
5D[6	19]5Q
6D[7	18]6Q
7D[8	17]7Q
8D[9	16]8Q
9D[10	15]9Q
10D[11	14]10Q
GND□	12	13	Пс

SN74BCT29842 ... DW OR NT PACKAGE (TOP VIEW)

oc_	1	U 24	□v _{cc}
1 D 🗆	2	23]1Q
2D	3	22]2Q
3D[4	21]3Q
4D[5	20]4Q
5D[6	19]5Q
6D 🗌	7	18]6Q
7D[8	17]7Q
8D	9	16]8Q
9D 🗌	10	15]9Q
10D[11	14]10Q
CND	12	1.3	Пс

A buffered output control (\overline{OC}) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powereddown. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The highimpedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN74BCT29841 and SN74BCT29842 are characterized for operation from 0°C to 70°C.

SN74BCT29841, SN74BCT29842 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'BCT29841 logic symbol[†]

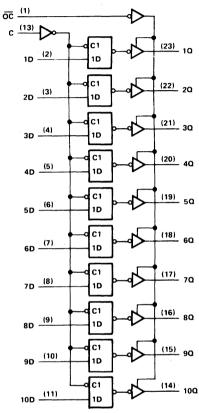
== (1) ~		
OC	EN	
C (13)	C1	
(2)	ے ۔۔۔۔۔۔ د	(23)
1D (2)	1D D 🔻	10
2D (3)		(22) 20
(A)		(21)
3D (5)		(20)
40		40
5D (6)		(19) 5Q
(7)		(18)
6D		6U
7D (8)		(17) 70
(9)		(16) 8Q
8D (10)		(15)
9D		9u
10D (11)		(14) 100

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE 'BCT29841

II	INPUTS		OUTPUT
<u>oc</u>	С	D	Q
L	Н	Н	н
L	Н	L	L
L	L	X	Q_0
н	Х	Х	Z

'BCT29841 logic diagram (positive logic)





'BCT29842 logic symbol[†]

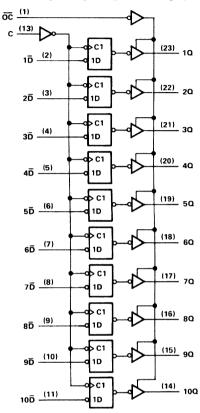
OC (1) EN C1 10 D D V 10 D D D D D D D D D D D D D D D D D D	(23) 1Q (22) 2Q (21) 3Q (20) 4Q (19) 5Q (18) 6Q (17) 7Q (16) 8Q
8Ē (9)	(16) 8Q
9Ē (10)	(15) 9Q
10Ē (11)	(14) 10Q

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE 'BCT29842

	NPUTS	OUTPUT	
ŌĊ	С	D	Q
L	Н	Н	L
L	Н	L	н
L	L	Х	Q ₀
Н	X	X	z

'BCT29842 logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		7 V
Input voltage		. 5.5 V
Voltage applied to a disabled 3-state output	t	. 5.5 V
Operating free-air temperature range		C to 70°C
Storage temperature range	−65°C	to 150°C



SN74BCT29841 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	٧
VIH	High-level input voltage	- 2			٧
VIL	Low-level input voltage			0.8	٧
ЮН	High-level output current			-24	mA
loL	Low-level output current			48	mA
t _W	Pulse duration, enable C high	4			ns
t _{su}	Setup time, data before enable C ↓	1.5			ns
th	Hold time, data after enable C ↓	3.5			ns
TA	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			1.2	٧
Voн	V _{CC} = 4.5 V	$I_{OH} = -15 \text{ mA}$	2.4			<
-011	100	$I_{OH} = -24 \text{ mA}$	2			·
VOL	$V_{CC} = 4.5 V$	$I_{OL} = 48 \text{ mA}$		0.35	0.5	٧
lozh	$V_{CC} = 5.5 V,$	$V_0 = 2.7 \text{ V}$			20	μΑ
lozL	$V_{CC} = 5.5 V,$	$V_O = 0.4 V$			-20	μΑ
li .	$V_{CC} = 5.5 V,$	$V_{I} = 5.5 V$			0.1	mA
ΙΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V	-10		-75	μΑ
IIL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.2	mA
los‡	$V_{CC} = 5.5 V,$	$V_O = 0$	-75		-275	mA
		Outputs high		3	7	mA
Icc	$V_{CC} = 5.5 V$	Outputs low		24	35	mA
		Outputs disabled		3	7	mA

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25°C.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}C$		C _L R1 R2	4.5 V to 5.5 V, = 50 pF, = 500 Ω, = 500 Ω, 0°C to 70°C	UNIT	
	-		MIN	TYP	MAX	MIN	MAX	Ì
tPLH	D	Q	1.5	4.5	. 7	1.5	8	ns
t _{PHL}	7 -	_	1.5	5.7	8	1.5	9] ""
^t PLH	С	Q	1.5	6	8	1.5	10	ns
^t PHL	7 ~		1.5	6	8	1.5	10]
^t PZH	oc	Q	2	10	. 13	2	15	ns
tPZL tpzL			2	10	13	2	15]
^t PHZ	ŌC	Q	2	5	7	2	8	ns
t _{PLZ}		N -	2	5	7	2	8	



[‡] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

SN74BCT29842 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	٧
VIH	High-level input voltage	2			٧
VIL	Low-level input voltage			0.8	٧
ЮН	High-level output current			-24	mA
lOL	Low-level output current			48	mA
t _W	Pulse duration, enable C high	4			ns
t _{su}	Setup time, data before enable C ↓	1.5			ns
th	Hold time, data after enable C ↓	3.5		VI. (1)	ns
TA	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vik	$V_{CC} = 4.5 V$,	$I_{\parallel} = -18 \text{ mA}$			-1.2	٧
VOH	V _{CC} = 4.5 V	$I_{OH} = -15 \text{mA}$	2.4			٧
		$I_{OH} = -24 \text{ mA}$	2			
VOL	$V_{CC} = 4.5 V,$	IOL = 48 mA		0.35	0.5	٧
IOZH	$V_{CC} = 5.5 V,$	$V_{O} = 2.7 \text{ V}$			20	μΑ
IOZL	$V_{CC} = 5.5 V,$	$V_{O} = 0.4 \text{ V}$			-20	μΑ
II.	$V_{CC} = 5.5 V,$	$V_{ } = 5.5 \text{ V}$			0.1	mA
łн	$V_{CC} = 5.5 V,$	V _I = 2.7 V	-10		-75	mA
IIL	$V_{CC} = 5.5 V,$	$V_{ } = 0.4 \text{ V}$			-0.2	mA
los‡	$V_{CC} = 5.5 V,$	$V_O = 0$	-75		-275	mA
lcc	V _{CC} = 5.5 V	Outputs high		3	7	mA
		Outputs low		24	35	mA
		Outputs disabled		3	7	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

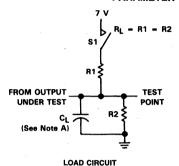
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$\begin{array}{c} {\rm V_{CC}} = 5 \; {\rm V,} \\ {\rm C_L} = 50 \; {\rm pF,} \\ {\rm R1} = 500 \; \Omega, \\ {\rm R2} = 500 \; \Omega, \\ {\rm T_A} = 25^{\circ} {\rm C} \end{array}$			$\begin{array}{c} \text{V}_{\text{CC}} = 4.5 \ \text{V to } 5.5 \ \text{V}, \\ \text{C}_{\text{L}} = 50 \ \text{pF}, \\ \text{R1} = 500 \ \Omega, \\ \text{R2} = 500 \ \Omega, \\ \text{T}_{\text{A}} = 0 ^{\circ}\text{C to } 70 ^{\circ}\text{C} \\ \end{array}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
tPLH	D	Q	1.5	5.7	8	1.5	9	ns
tPHL]	_ "	1.5	4.5	7	1.5	8] "
tPLH	С	Q	1.5	6	8	1.5	10	ns
^t PHL]	Ĭ ŭ	1.5	6	8	1.5	10]
^t PZH	oc	Q	2	10	13	2	15	ns
tPZL		.	2	10	13	2	15] ""
tPHZ	ŌC	Q	2	5	7	2	8	ns
tPLZ]		2	5	7	2	8	



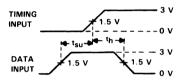
^{*} Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

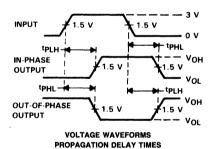


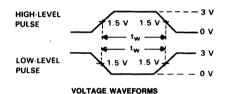
SWITCH POSITION TABLE

TEST	S1
t _{PLH}	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed

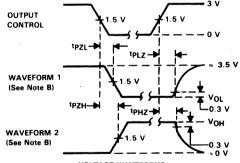


VOLTAGE WAVEFORMS SETUP AND HOLD TIMES





PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES. THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns,
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS



General Information 1

BICMOS Circuits 2

Mechanical Data

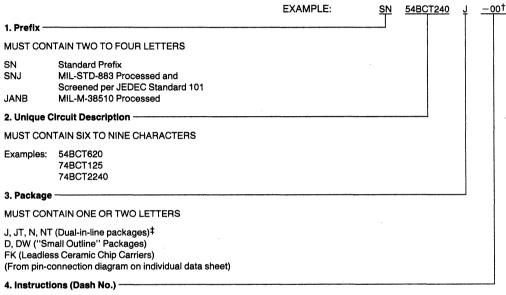
2

Contents

	rage
Ordering Instructions	3-3
Package Data	3-4

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.



MUST CONTAIN TWO NUMBERS

- -00 No special instructions
- 10 Solder-dipped leads (N and NT packages only)
- † For tape and reel information contact the factory.
- ‡ These circuits in dual-in-line packages are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method that will best suit your particular needs.

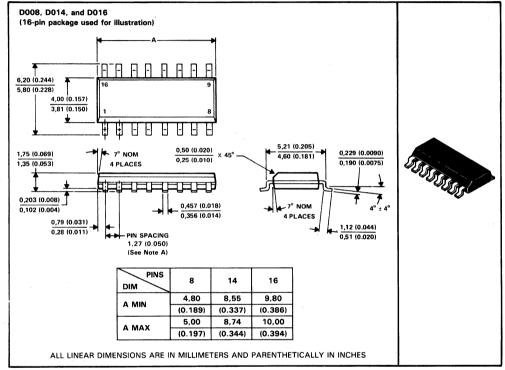
Dual-in-line (J, JT, N, NT)

- -Slide Magazines
- —A-Channel Plastic Tubing
- -Barnes Carrier (N only)
- -Sectioned Cardboard Box
- -Individual Plastic Box



D008, D014, and D016 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



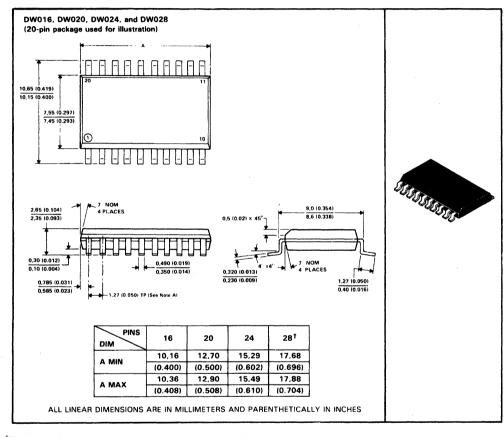
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.

- B. Body dimensions do not include mold flash or protrusion.
- C. Mold flash or protrusion shall not exceed 0.15 (0.006).
- D. Lead tips to be planar within $\pm 0,051$ (0.002) exclusive of solder.



DW016, DW020, DW024, and DW028 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



[†]The 28-pin package drawing is presently classified as Advance Information.

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.

- B. Body dimensions do not include mold flash or protrusion.
- C. Mold flash or protrusion shall not exceed 0,15 (0.006).
- D. Lead tips to be planar within ± 0.051 (0.002) exclusive of solder.

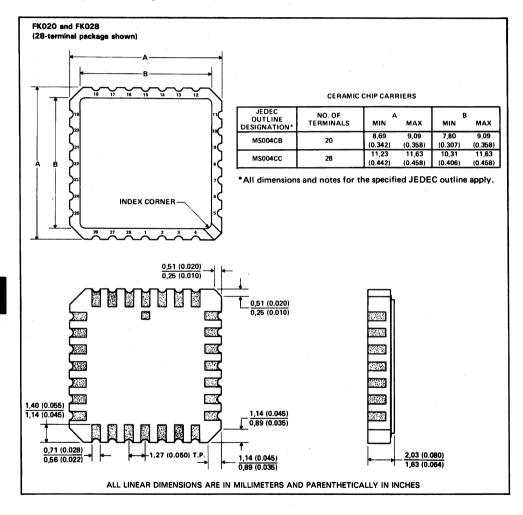


Mechanical Data

FK020 and FK028 ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

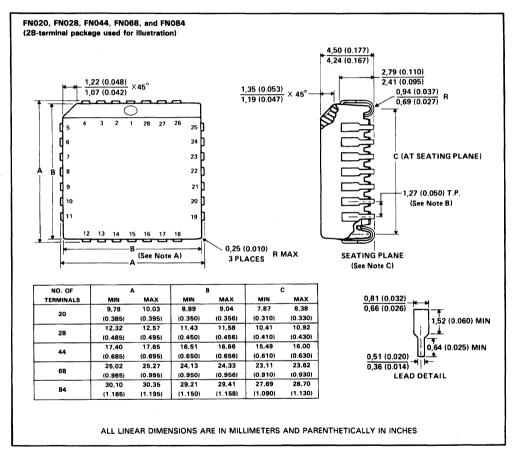
FK package terminal assignments conform to JEDEC Standards 1 and 2.





FN020, FN028, FN044, FN068, and FN084 plastic chip carrier packages

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in highhumidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.

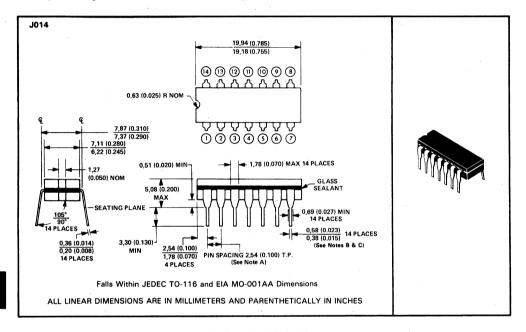
B. Location of each pin is within 0.127 (0.005) of true position with respect to center pin on each side.

C. The lead contact points are planar within 0,10 (0.004).



J014 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

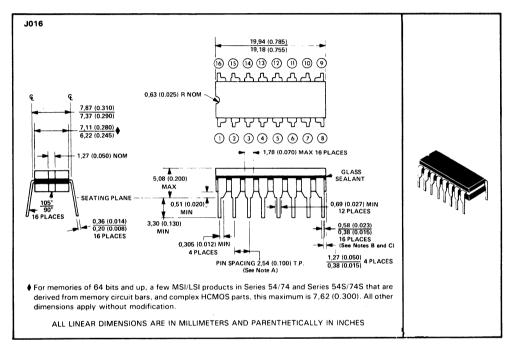


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

J016 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

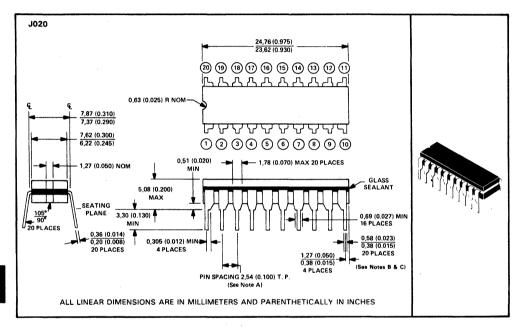


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

J020 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

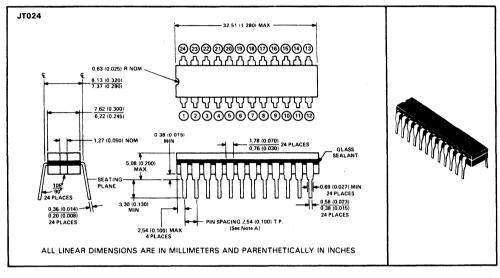


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

JT024 ceramic dual-in-line package

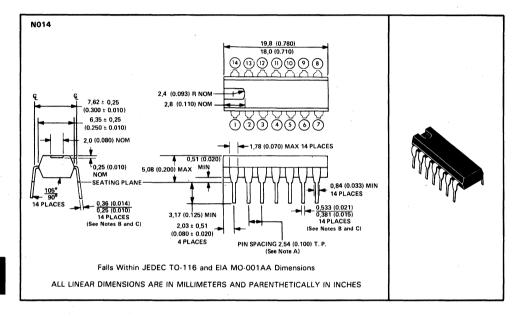
This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldering assembly.



NOTE: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

N014 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

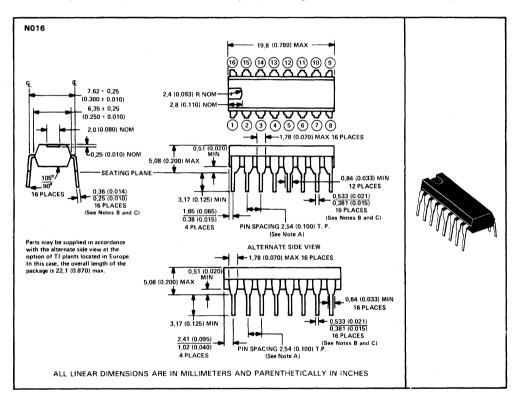


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

N016 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



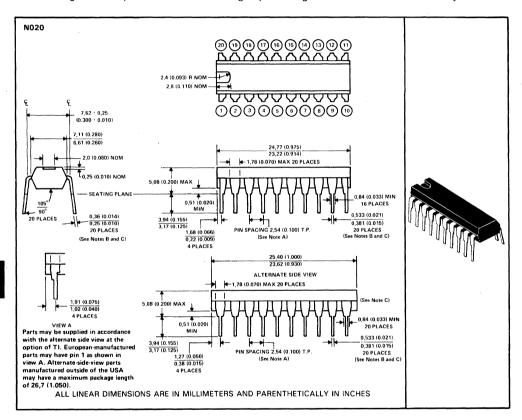
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.



N020 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

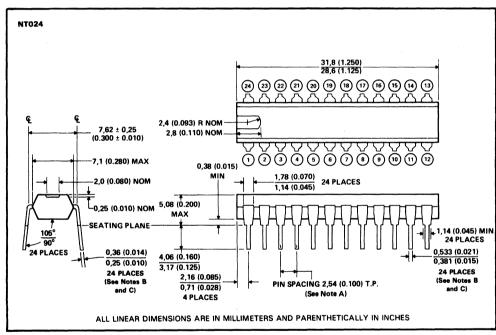
- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.



NT024 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.



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