TOSHIBA AMERICA INC.

MOS MEMORY PRODUCTS

DATA BOOK '83-4

TOSHIBA AMERICA, INC.

TOSHIBA

MOS MEMORY PRODUCTS

DATA BOOK

TOSHIBA

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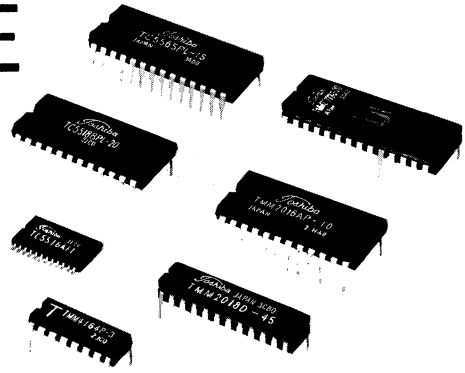
*: PRELIMINARY

MEMORY PRODUCT GUIDE



1. Dynamic RAM

Capacity	Device Number	Organization	Process	Access Time Max. (ns)		Cycle Time Min. (ns)	Power Supplies (V)	Power Dissipation Max. (mW)		Pins	Alternate Source
				t_{RAC}	t_{CAC}			Active	Standby		
16K Bit	TMM416P–2	16,384 x 1	NMOS	150	100	320	+5	462	20	16	MK4116–2
	TMM416P–3			200	135	375	–5				MK4116–3
	TMM416P–4			250	165	410	+12				MK4116–4
64K Bit	TMM4164P–2	65,536 x 1	NMOS	120	80	260	+5	275	27.5	16	—
	TMM4164P–3			150	100	260					
	TMM4164P–4			200	135	330					
	TMM4164AP–12			120	60	220	+5	275	22	16	—
	TMM4164AP–15			150	75	260					
	TMM4164AP–20			200	100	330					
256K Bit *	TMM41256C–12	262,144 x 1	NMOS	120	60	220	+5	330	27.5	16	—
*	TMM41256C–15			150	75	260		275			

Note; TMM41256C : Page Mode Parts

2. Static RAM

Capacity	Device Number	Organization	Process	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supplies (V)	Power Dissipation Max. (mW)		Pins	Alternate Source
							Active	Standby		
4K Bit	TMM314AP–1	1,024 x 4	NMOS	200	200	+5	550	—	18	i2114–2
	TMM314AP–3			300	300					i2114–3
	TMM314AP			450	450					i2114
	TMM314APL–1			200	200		385	—		i2114L–2
	TMM314APL–3			300	300					i2114L–3
	TMM314APL			450	450					i2114L
	TMM2114AP–12	1,024 x 4	NMOS	120	120	+5	330	—	18	i2114A
	TMM2114AP–15			150	150					
	TMM315D–1	4,096 x 1	NMOS	55	55	+5	990	165	18	i2147–3
	TMM315D			70	70		880	110		
16K Bit	TMM2016P/D–1	2,048 x 8	NMOS	100	100	+5	660	83	24	(HM6116)
	TMM2016P/D			150	150		550	83		
	TMM2016P/D–2			200	200		770	165		
	TMM2016AP–90	2,048 x 8	NMOS	90	90	+5	440	38.5	24	(HM6116)
	TMM2016AP–10			100	100		358			
	TMM2016AP–12			120	120		358			
	TMM2016AP–15			150	150		358			
*	TMM2015AP–90	2,048 x 8	NMOS	90	90	+5	440	38.5	24	—
*	TMM2015AP–10			100	100		358			
*	TMM2015AP–12			120	120		358			
*	TMM2015AP–15			150	150		358			
	TMM2018D–45	2,048 x 8	NMOS	45	45	+5	788	105	24	—
	TMM2018D–55			55	55					

Note; Package TMM2016AP 0.6 inch width DIP
TMM2015AP: 0.3 inch width DIP
TMM2018D: 0.3 inch width DIP

Note; Package Material P: Plastic C: Ceramic D: Cerdip F: Plastic Flat
*Preliminary: These are target specifications and are subject to change without notice.

3. CMOS Static RAM

Capacity	Device Number	Organization	Process	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supplies (V)	Power Dissipation Max. (mW)		Pins	Alternate Source
							Active	Standby		
1 K Bit	TC5501P	256 x 4	CMOS	450	450	+5	83	0.055	22	i5101L–1
	TC5501 P–1			650	650					i5101L
4K Bit	TC5047AP–1	1,024 x 4	CMOS	550	650	+5	110	0.11	20	μPD445
	TC5047AP–2			800	1000					
	TC5504AP/AD–2	4,096 x 1	CMOS	200	300	+5	27.5	0.11	18	(HM6504)
	TC5504AP/AD–3			300	420					
	TC5504APL/ADL–2			200	300		27.5	0.005		
	TC5504APL/ADL–3			300	420					
	TC5514AP/AD–2	1.024 x 4	CMOS	200	200	+5	27.5	0.11	18	(HM6514)
	TC5514AP/AD–3			300	300					
	TC5514APL/ADL–2			200	200		27.5	0.005		
	TC5514APL/ADL–3			300	300					
	TC5513AP/AD–20	1,024 x 4	CMOS	200	200	+5	27.5	0.11	18	
	TC5513APL/ADL–20			200	200			0.005		
	TC5514P	1.024 x 4	CMOS	450	450	+5	138	0.11	18	
	TC5514P–1			650	650		110			
16K Bit	TC5516AP/AD/AF–2	2,048 x 8	CMOS	200	200	+5	385	0.165	24	–
	TC5516AP/AD/AF			250	250					
	TC5516APL/ADL/AFL–2			200	200		385	0.005		
	TC5516APL/ADL/AFL			250	250					
	TC5517AP/AD/AF–2	2,048 x 8	CMOS	200	200	+5	385	0.165	24	(TMM2016) (HM6116L)
	TC5517AP/AD/AF			250	250					
	TC5517APL/ADL/AFL–2			200	200		385	0.005		
	TC5517APL/ADL/AFL			250	250					
	TC5517BP/BD/BF–20	2,048 x 8	CMOS	200	200	+5	55	0.165	24	(TMM2016) (HM6116L)
	TC5517BPL/BDL/BFL–20			200	200			0.005		
	TC5518BP/BD/BF –20	2,048 x 8	CMOS	200	200	+5	55	0.165	24	–
	TC5518BPL/BDL/BFL–20			200	200			0.005		
64K Bit	* TC5564P–10	8,192 x 8	CMOS	100	100	+5	55	0.11	28	–
	* TC5564P–15			150	150					
	* TC5564PL–10			100	100			0.005		
	* TC5564PL–15			150	150					
	TC5565P–12	8,192 x 8	CMOS/ NMOS	120	120	+5	55	5.5	28	–
	TC5565P–15			150	150					
	TC5565PL–12			120	120			0.55		
	TC5565PL–15			150	150					

Note Package Material P: Plastic C: Ceramic D: Cerdip F: Plastic Flat
*Preliminary: These are target specifications and are subject to change without notice.

4. Erasable Programmable ROM

Capacity	Device Number	Organization	Process	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supplies (V)	Power Dissipation Max. (mW)		Pins	Alternate Source
							Active	Standby		
64K Bit	TMM2764D-2	8,192 x 8	NMOS	200	200	+5	630	184	28	i2764
	TMM2764D			250	250					
	TMM2764DI-2			200	200		683	210		—
	TMM2764DI			250	250					
128K Bit	TMM27128D-20	16,384 x 8	NMOS	200	200	+5	630	184	28	i27128
	TMM27128D-25			250	250					

Note; TMM2764DI/DI-2: (Operating temperature range: −40°C ~ 85°C)

5 Mask Programmable ROM

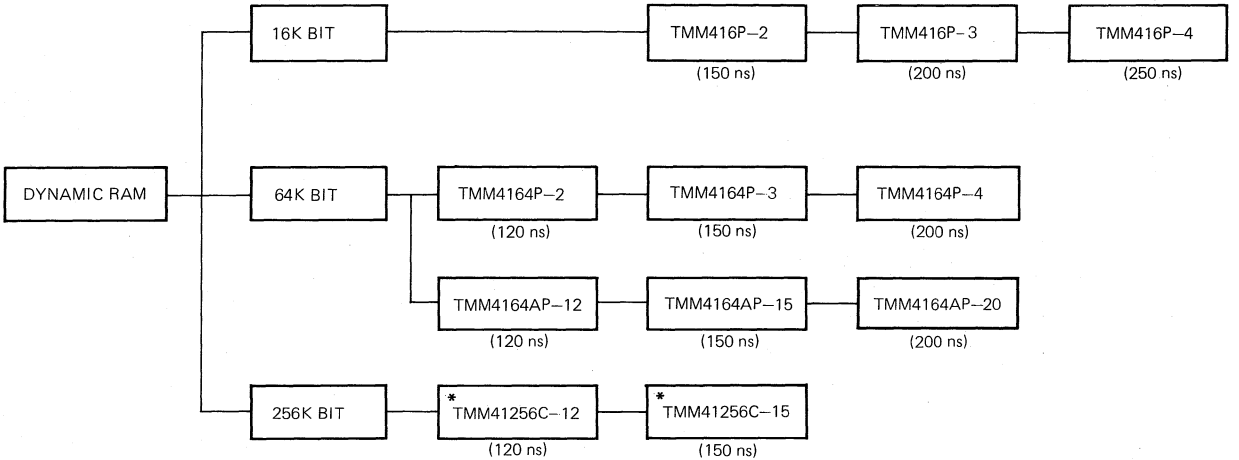
Capacity	Device Nnumber	Organization	Process	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supplies (V)	Power Dissipation Max. (mW)		Pins	Alternate Source
							Active	Standby		
16K Bit	TMM334P	2,048 x 8	NMOS	450	450	+5	440	—	24	i2316E
32K Bit	TMM333P	4,096 x 8	NMOS	450	450	+5	525		24	TMS4732
	TMM2332P			350	350		550	83	24	i2332
64K Bit	TMM2364P	8,192 x 8	NMOS	250	350	+5	220	83	28	i2364
	TMM2365P			200	200		550	138	28	(i2364)
	TMM2366P			200	200		550	138	24	MK36000
128K Bit *	TMM23128P	16,384 x 8	NMOS	200	200	+5	440	110	28	—
256K Bit	TMM23256P	32,768 x 8	NMOS	150	230	+5	220	55	28	—

6. CMOS Mask Programmable ROM

Capacity	Device Number	Organization	Process	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supplies (V)	Power Dissipation Max. (mW)		Pins	Alternate Source
							Active	Standby		
32K Bit	TC5332P	4,096 x 8	CMOS	450	450	+5	39	0.11	24	TMM2332
	TC5333P			450	540					(TMM2332)
	TC5334P			450	450					TMM333
	TC5335P			450	540					(TMM333)
*	TC5364P	8,192 x 8	CMOS	250	350	+5	39	0.11	28	TMM2364
64K Bit *	TC5365P			250	250				28	TMM2365
*	TC5366P			250	250				24	TMM2366
256K Bit *	TC53256P	32,768 x 8	CMOS	350	450	+5	83	0.11	28	(TMM23256)

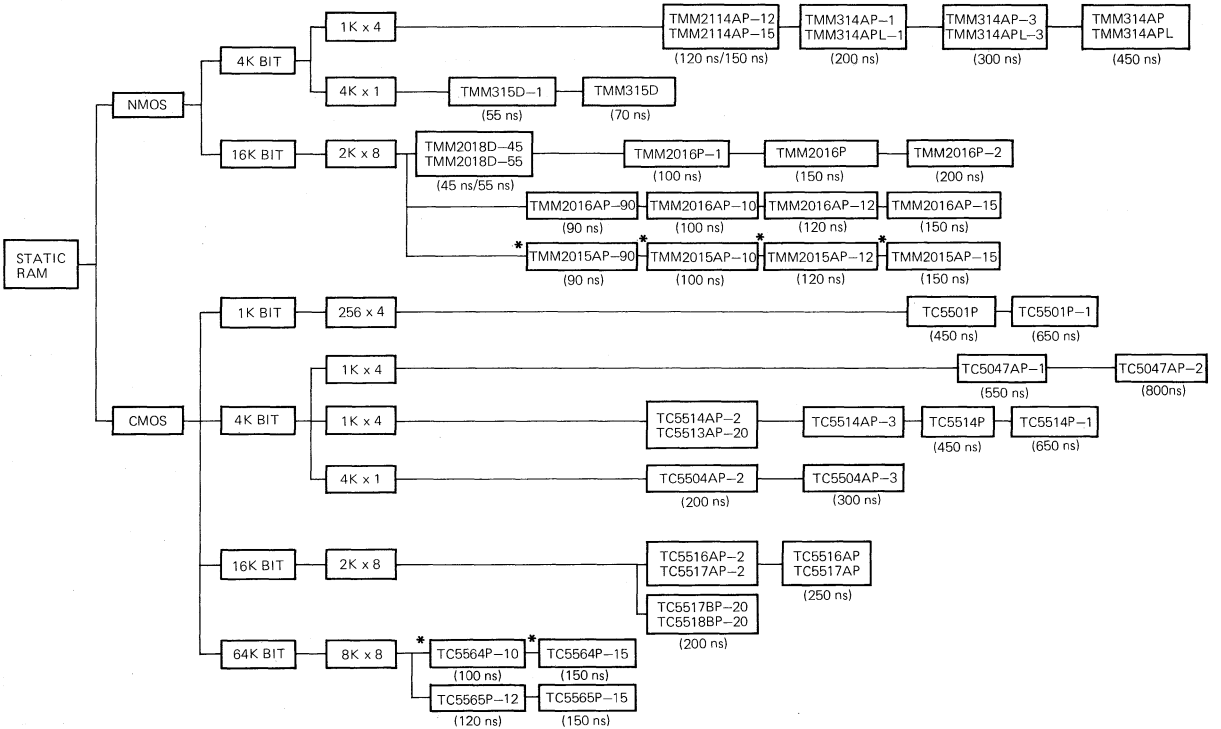
Note Package Material P: Plastic C: Ceramic D: Cerdip F: Plastic Flat
*Preliminary: These are tartet specifications and are subject to change without notice.

TOSHIBA DYNAMIC RAM



*: PRELIMINARY

TOSHIBA STATIC RAM (NMOS STATIC RAM, CMOS STATIC RAM)



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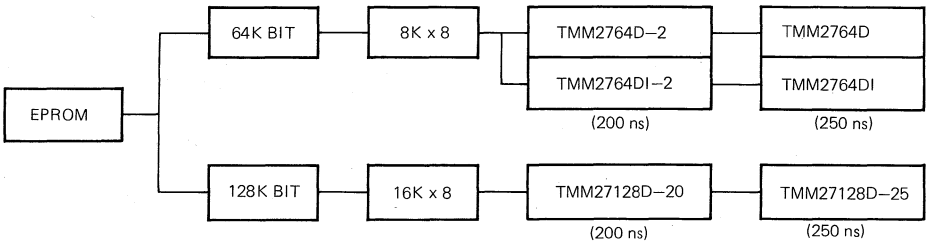
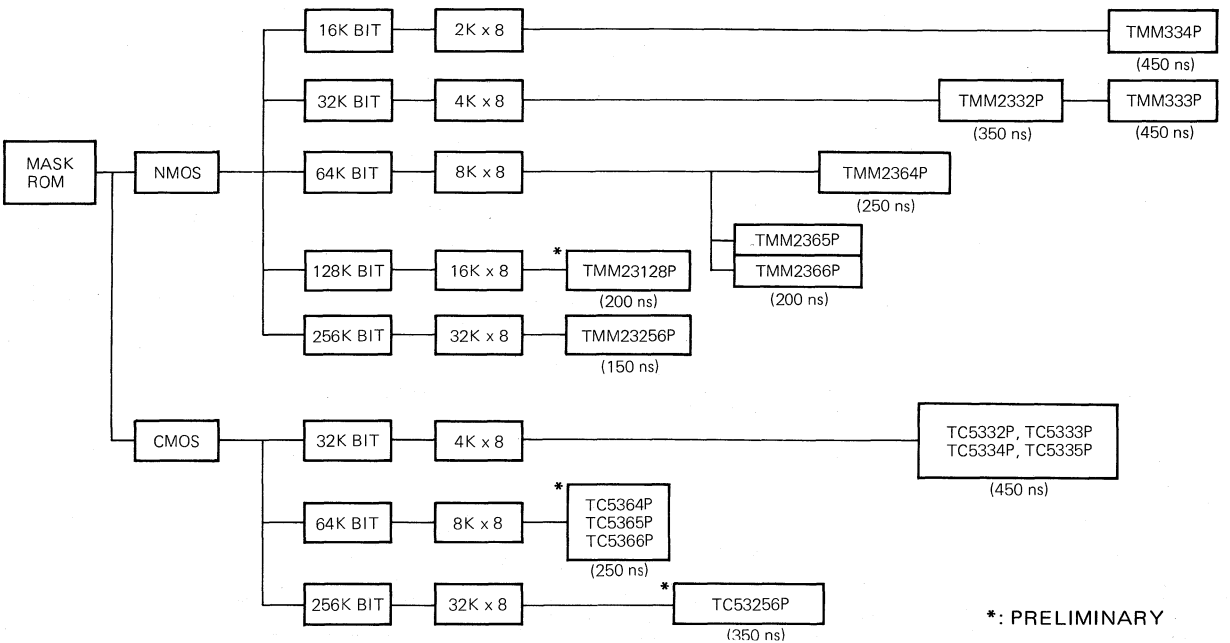
TOSHIBA

TOSHIBA EPROM



DI version: Operating Temperature = –40 ~ 85°C

TOSHIBA MASK ROM (NMOS MASK ROM, CMOS MASK ROM)



*: PRELIMINARY

MEMORY SELECTION GUIDE 1.

Note; *: Preliminary

ACCESS TIME (ns)	1K Bit	4K Bit	16K Bit	32K Bit	64K Bit	128K Bit	256K Bit
800		TC5047AP–2					
700							
600	TC5501 P	TC5514P–1					
500		TC5047AP–1					
400	TC5501P	TMM314AP TC5514P	TMM334P	TC5332P TC5333P TC5334P TC5335P TMM333P			
300				TMM2332P			*TC53256P
200		TMM314AP–3 TC5514AP–3 TC5504AP–3	TC5516AP TC5517AP TMM416P–4		TMM2764D TMM2364P *TC5364P *TC5365P *TC5366P	TMM27128D–25	
100		TMM314AP–1 TC5514AP–2 TC5513AP–20	TMM2016P–2 TCC5517AP–2 TMM416P–3 *TC5517BP–20 TC5516AP–2 *TC5518BP–20		TMM4164P–4 TMM2764D–2 TMM2365P TMM2366P TMM4164AP–20	TMM27128D–20 *TMM23128P	
0		TMM2114AP–12 TMM2114AP–15	TMM2016P *TMM2015AP–12 TMM2016AP–12 *TMM2015AP–15 TMM2016AP–15 TMM416P–2		TMM4164P–2/3 TMM4164AP-12/15 *TC5564P–15 TC5565P-12/15	TMM23256P	*TMM41256C–12 *TMM41256C–15
		TMM315D TMM315D–1	TMM2016P–1 *TMM2015AP–10 TMM2016AP–10 *TMM2015AP–90 TMM2016AP–90 TMM2018D–55		*TC5564P–10		
			TMM2018D–45				

MEMORY SELECTION GUIDE (2)

Memory	Type	Memory Capacity						
		1K Bit	4K Bit	16K Bit	32K Bit	64K Bit	128K Bit	256K Bit
RAM	Dynamic RAM			TMM416P		TMM4164P TMM4164AP		*TMM41256C
	Nch Static RAM		TMM314AP TMM2114AP TMM315D	TMM2016P TMM2016AP *TMM2015AP TMM2018D				
	CMOS Static RAM	TC5501P	TC5047AP TC5514P TC5514AP TC5513AP	TC5517AP/AF TC5516AP/AF *TC5517BP/BF *TC5518BP/BF		*TC5564P TC5565P		
ROM	EPROM					TMM2764D TMM2764DI	TMM27128D	
	Nch MASK ROM			TMM334P	TMM333P TMM2332P	TMM2364P TMM2365P TMM2366P	*TMM23128P	TMM23256P
	CMOS MASK ROM				TC5332P TC5333P TC5334P TC5335P	*TC5364P *TC5365P *TC5366P		*TC53256P

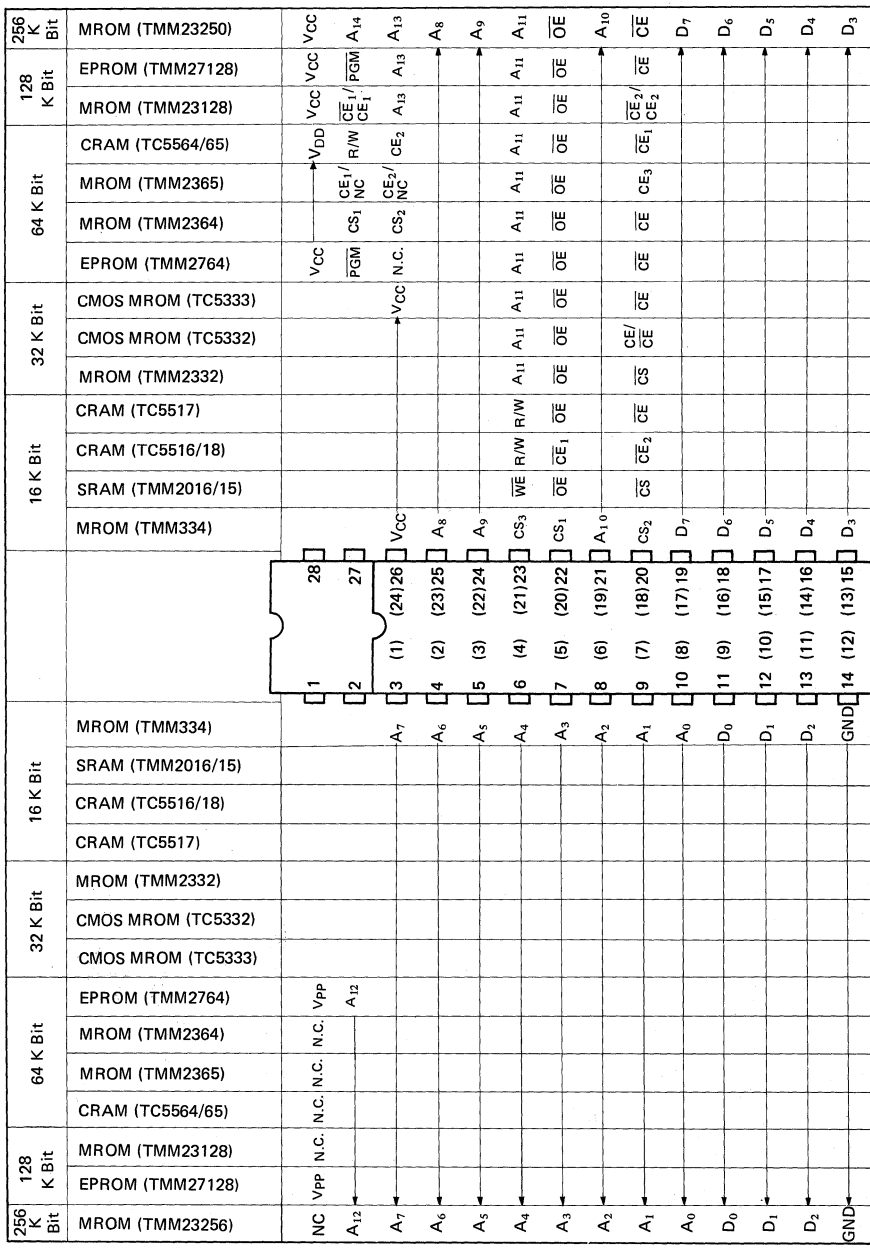
*PRELIMINARY

MEMORY SELECTION GUIDE (3)

Word \ Bit	1	4	8
256		TC5501P	
1,024		TMM314AP TMM2114AP TC5047AP TC5514P TC5514AP TC5513AP	
2,048			TMM2016P TMM2016AP *TMM2015AP TMM2018D TC5516AP/AF TC5517AP/AF *TC5517BP/BF *TC5518BP/BF TMM334P
4,096	TMM315D TC5504AP		TMM2332P TMM333P TC5332P TC5333P TC5334P TC5335P
8,192			*TC5564P TC5565P *TC5364P TMM2364P *TC5365P TMM2365P *TC5365P TMM2366P TMM2764D
16,384	TMM416P		TMM27128D *TMM23128P
32,768			TMM23256P *TC53256P
65,536	TMM4164P TMM4164AP		
262,144	*TMM41256C		

*PRELIMINARY

TOSHIBA BYTE-WIDE MEMORY PIN OUT (CURRENT AND FUTURE DEVICES)



CROSS REFERENCE

1. 16 K Bit Dynamic RAM

Access Tim	150 ns	200 ns	250 ns
Toshiba	**TMM416P–2**	**TMM416P–3**	**TMM416P–4**
Fairchild	F16K–2	F16K–3	F16K4
Fujitsu	MB8116H	MB8116E	MB8116N
Hitachi	HM4716A–2	HM4716A–3	HM4716A–4
Intel	2117–2	2117–3	2117–4
Intersil		IM7116–3	IM7116–4
Mitsubishi	M5K4116–2	M5K4116–3	M5K4116–4
Mostek	MK4116–2	MK4116–3	MK4116–4
Motorola	MCM4116C–2	MCM4116C–3	MCM4116C–4
National Semi.	NM5290–2	MM5290–3	
NEC	μPD416C/D–3	μPD416C/D–2	μPD416C/D–1
TI	TMS4116–15	TMS4116–20	TMS4116–25

2. 64K Bit Dynamic RAM.

	120 ns	150 ns	200 ns
Toshiba	**TMM4164P–2**	**TMM4164P–3**	**TMM4164P–4**
Fujitsu		MB8264–15	MB8264–20
Hitachi		HM4864–2	HM4864–3
Intel		2164–15	2164–20
Mitsubishi		M5K4164N-15	M5K4164N–20
Motorola		MCM6665–15	MCM6665–20
NEC		μPD4164–3	μPD4164–2
OKI	MSM3764–12	MSM3764–15	MSM3764–20
TI		TMS4164–15	TMS4164–20

3. 4K Bit Static RAM

	1,024 x 4			4,096 x 1	
Access Time	**200 ns**	**300 ns**	**450 ns**	**55 ns**	**70 ns**
Toshiba	**TMM314AP-1/APL-1**	**TMM314AP-3/APL-3**	**TMM314AP/APL**	**TMM315D–1**	**TMM315D**
AND	Am9114EPC	Am9114CPC	Am9114BPC		
AMI	S2114-2	S2114-3			S2147
Fujitsu	MB8114EL	MB8114NL		MB8147H	MB8147E
Hitachi	HM472114AP-2	HM472114AP-3	HM472114AP-4	HM6147-3	HM6147
Intel	2114-2/L2	2114-3/L3	2114/L	2147-3	2147
Intersil	IM7114-2/L2		IM7114L		
Mitsubishi	M5L2114LP, S-2	M5L2114LP, S-3	M5L2114LP, S		
Motorola	MCM2114-20	MCM2114-30	MCM2114-45	MCM2147-55	MCM2147-70
National	MM2114-2/–2L	MM2114-3/–3L	MM2114/–L	MM2147-3	MM2147
NEC	μPD2114LC/D-3	μPD2114LC/D-1	μPD2114LC/D	μPD2147D-3	μPD2147D-2
SYNERTEK					SY2147
TI	TMS4045-20		TMS4045-45	TMS2147-5	TMS2147-7

4. 1K/4K Bit CMOS RAM

	1 K Bit	4 K Bit		
	256 x 4	1,024 x 4	1,024 x 4	4,096 x 1
Toshiba	**TC5501P**	**TC5047AP**	**TC5514P TC5514AP/TC5513AP**	**TC5504P TC5504AP**
Fujitsu			MB8414	MB8404
Harris	HM6501		HM6514	HM6504
Hitachi	HM435101		HM4334	HM4315
Intel	i5101L			
Intersil			IM6514	IM6504
Mitsubishi	M5L5101P-1		M58981S-45	
NEC	μPD5101	μPD445	μPD444	
Oki			MSM5114	MSM5104
RCA			MWS5114	

5. 16 K Bit NMOS/CMOS Static RAM

	16 K Bit			
	NMOS	CMOS		
Toshiba	**TMM2016P TMM2016AP**	**TC5516AP**	**TC5517AP/BP**	**TC5518BP**
Fujitsu	MB8128	MB8417	TM8416	MB8418
Hitachi	(HM6116)		(HM6116)	(HM6117)
Mitsubishi	M58725			
NEC	μPD4016	μPD447	μPD446	μPD449
OKI	MSM2128	MSM5127	MSM5128	MSM5129

6. ROM (EPROM & MROM)

	EPROM	MROM			
	64 K Bit	32 K Bit		64 K Bit	
Toshiba	**TMM2764D**	**TMM333P TC5334P TC5335P**	**TMM2332P TC5332P TC5333P**	**TMM2364P TMM2365P**	**TMM2366P**
Fujitsu	MB2764	MB8332	MB8333		MB8364
Hitachi	HN482764	HM46332P			HN48364
Intel	i2764		i2332	i2364	
Mitsubishi		M58333	M58735		M58334
Mostak		MK32000		MK37000	MK36000
Motorola					
NEC		μPD2332			μPD2364
Oki	MSM2764AS				
TI		TMS4732			TM54764

Dynamic Random Access Memories

16384 WORD x 1 BIT DYNAMIC RAM

N CHANNEL SILICON GATE MOS

TMM416P-2, TMM416P-3, TMM416P-4

DESCRIPTION

The TMM416P is a 16,384 words by 1 bit MOS random access memory circuit fabricated with TOSHIBA's double poly N-channel silicon gate process for high performance and high functional density.

The TMM416P uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation. Multiplexed address inputs permit the TMM416P to be packaged in a standard 16 pin plastic DIP. This package size provides high system bit densities and is compatible with widely available automatic testing and insertion equipment.

FEATURES

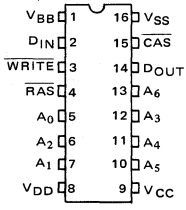
- 16,384 words by 1 bit organization
- Fast access time and cycle time

DEVICE	t_{RAC}	t_{RC}
TMM416P-2	150 ns	320 ns
TMM416P-3	200 ns	375 ns
TMM416P-4	250 ns	410 ns

- Industry standard 16 pin plastic DIP
- Standard ± 10% power supply (+12V, ± 5V)
- Lower power: 462mW operating (max.)
  20mW standby (max.)
- Output unlatched at cycle end allows two-dimensional chip select
- Common I/O capability using "Early Write" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- All inputs and output TTL compatible
- 128 refresh cycles / 2 msec
- Compatible with MK4116

PIN CONNECTIONS

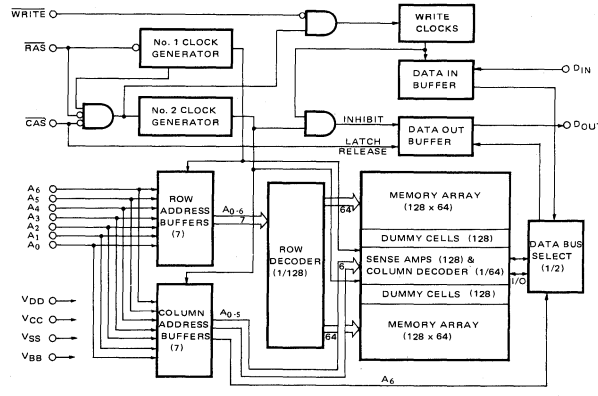
(TOP VIEW)



PIN NAMES

A_0-A_6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{BB}	Power (−5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

RATING	VALUE	UNITS	NOTES
Voltage on any pin relative to V_{BB}	−0.5 ~ +20	V	1
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS}	−1.0 ~ +15	V	1
V_{BB}-V_{SS} (V_{DD}-V_{SS} > OV)	0	V	1
Operating temperature	0 ~ 70	°C	1
Storage temperature	−55 ~ 150	°C	1
Soldering temperature · Time	260 · 10	°C · sec	1
Power dissipation	600	mW	1
Short circuit output current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 ~ 70°C) (Note 2)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	V	3
V_{CC}		4.5	5.0	5.5	V	3,4
V_{SS}		0	0	0	V	3
V_{BB}		−4.5	−5.0	−5.5	V	3
V_{IHC}	Input High Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7		7.0	V	3
V_{IH}	Input High Voltage, except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7.0	V	3
V_{IL}	Input Low Voltage, all inputs	−1.0		0.8	V	3

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 12.0V ± 10%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%, Ta = 0°C ~ 70°C) (Note 2)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES
I_{DD1}	OPERATING CURRENT		35	mA	5
I_{CC1}	Average power supply operating current				6
I_{BB1}	($\overline{RAS}$, $\overline{CAS}$ cycling : t_{RC} = minimum value)		200	μA	
I_{DD2}	STANDBY CURRENT		1.5	mA	
I_{CC2}	Power supply standby current	−10	10	μA	
I_{BB2}	($\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance)		100	μA	
I_{DD3}	REFRESH CURRENT		27	mA	5
I_{CC3}	Average power supply current, refresh mode.	−10	10	μA	
I_{BB3}	($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC} : t_{RC} = minimum value)		200	μA	
I_{DD4}	PAGE MODE CURRENT		27	mA	5
I_{CC4}	Average power supply current, page mode operation				6
I_{BB4}	($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling : t_{PC} = minimum value)		200	μA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input leakage current, any input (V_{BB} = −5V OV ≤ V_{IN} ≤ +7.0V, all other pins not under test = OV)	−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, OV ≤ V_{OUT} ≤ +5.5V)	−10	10	μA	
V_{OH}	OUTPUT LEVELS Output "H" level voltage (I_{OUT} = −5mA)	2.4		V	4
V_{OL}	OUTPUT LEVELS Output "L" level voltage (I_{OUT} = 4.2mA)		0.4	V	4

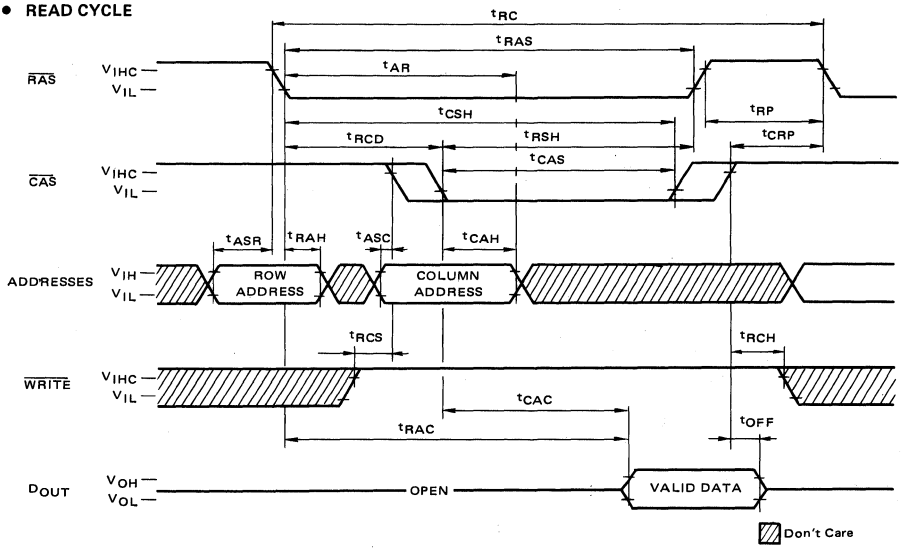
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%, V_{SS} = OV, V_{BB} = −5.0V ± 10%, Ta = 0°C ~ 70°C) (NOTES 2, 7, 8, 10)

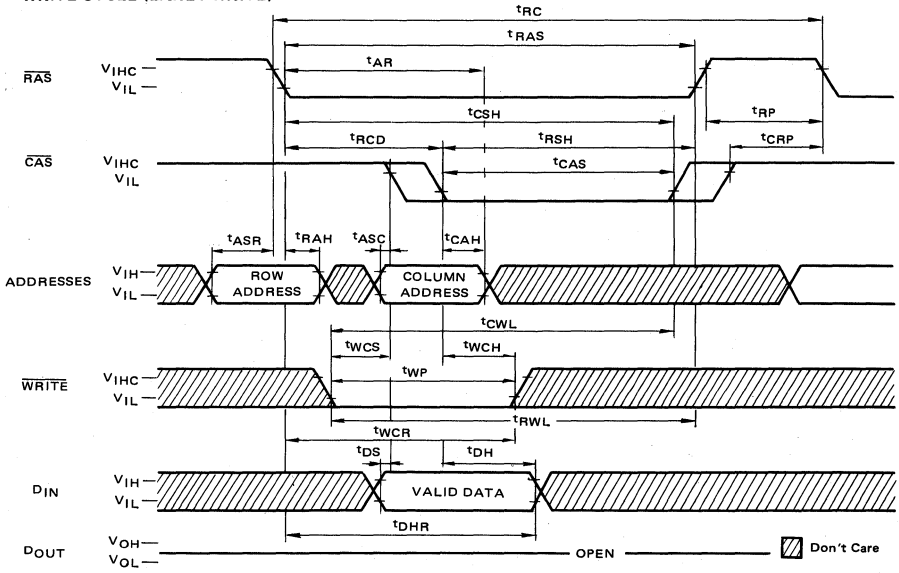
SYMBOL	PARAMETER	TMM416P-2		TMM416P-3		TMM416P-4		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random read or write cycle time	320		375		410		ns	9
t_{RWC}	Read-write cycle time	320		375		425		ns	9
t_{RMW}	Read-modify-write cycle time	320		405		500		ns	9
t_{PC}	Page mode cycle time	170		225		275		ns	
t_{RAC}	Access time from $\overline{RAS}$		150		200		250	ns	11, 13
t_{CAC}	Access time from $\overline{CAS}$		100		135		165	ns	12, 13
t_{OFF}	Output buffer turn-off delay	0	40	0	50	0	60	ns	14
t_T	Transition time (rise and fall)	3	35	3	50	3	50	ns	10
t_{RP}	$\overline{RAS}$ precharge time	100		120		150		ns	
t_{RAS}	$\overline{RAS}$ pulse width	150	32,000	200	32,000	250	32,000	ns	
t_{RSH}	$\overline{RAS}$ hold time	100		135		165		ns	
t_{CSH}	$\overline{CAS}$ hold time	150		200		250		ns	
t_{CAS}	$\overline{CAS}$ pulse width	100	10,000	135	10,000	165	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	20	50	25	65	35	85	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	−20		−20		−20		ns	
t_{ASR}	Row Address set-up time	0		0		0		ns	
t_{RAH}	Row Address hold time	20		25		35		ns	
t_{ASC}	Column Address set-up time	−10		−10		−10		ns	
t_{CAH}	Column Address hold time	45		55		75		ns	
t_{AR}	Column Address hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	45		55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write command pulse width	45		55		75		ns	
t_{RWL}	Write command to $\overline{RAS}$ lead time	50		70		85		ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	50		70		85		ns	
t_{DS}	Data-in set-up time	0		0		0		ns	16
t_{DH}	Data-in hold time	45		55		75		ns	16
t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CP}	$\overline{CAS}$ precharge time (for page-mode cycle only)	60		80		100		ns	
t_{REF}	Refresh period		2		2		2	ms	
t_{WCS}	$\overline{WRITE}$ command set-up time	−20		−20		−20		ns	17
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		80		90		ns	17
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	110		145		175		ns	17

TIMING WAVEFORMS

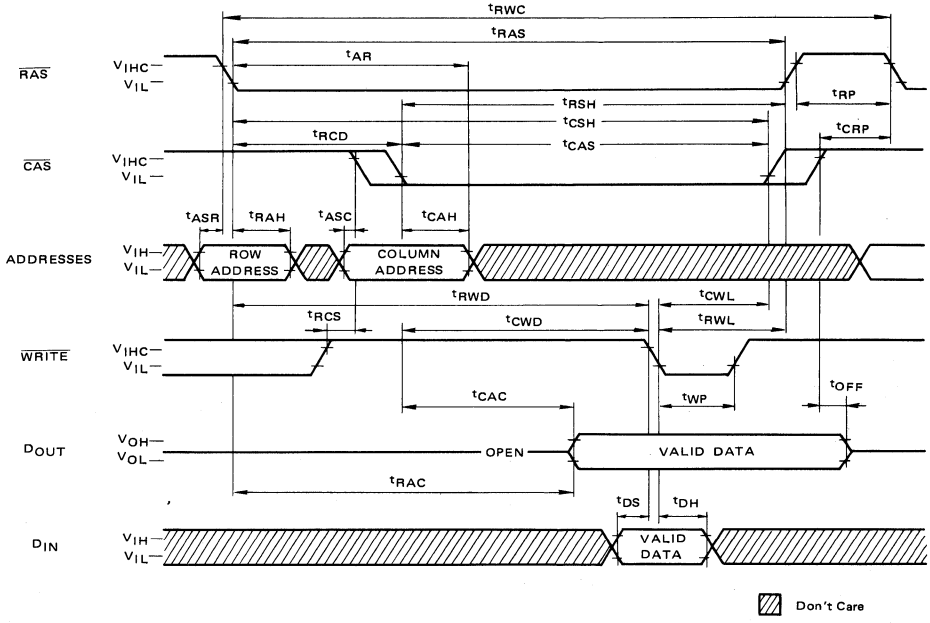
- **READ CYCLE**



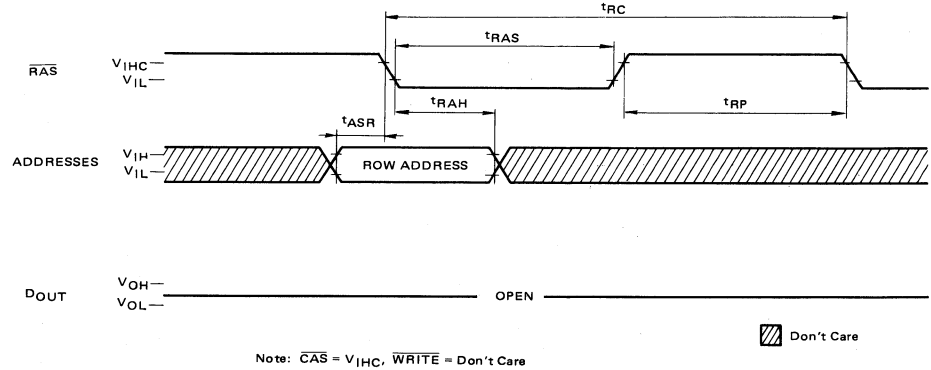
- **WRITE CYCLE (EARLY WRITE)**



- **READ-WRITE/READ-MODIFY-WRITE CYCLE**

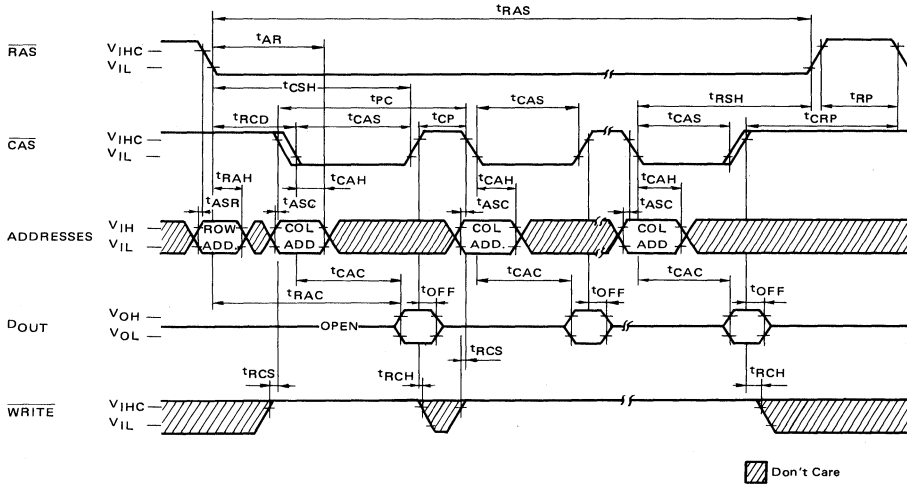


- **"RAS-ONLY" REFRESH CYCLE**

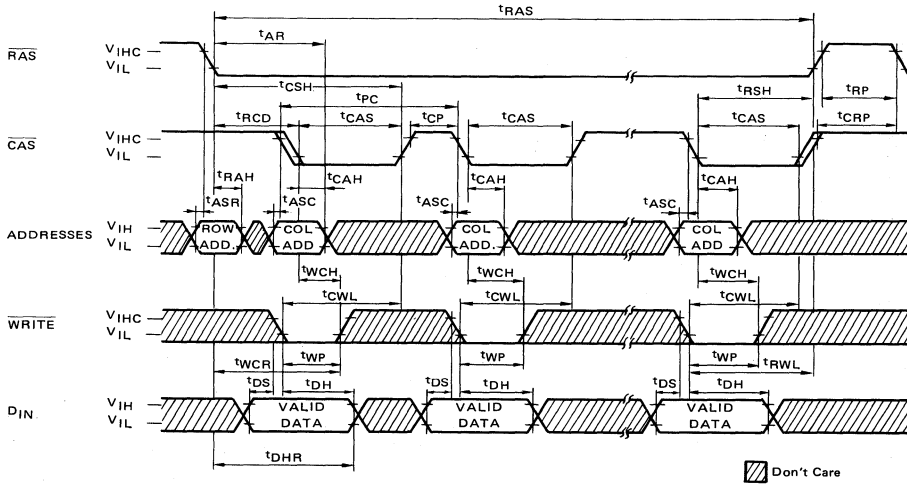


Note: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care

- **PAGE MODE READ CYCLE**



- **PAGE MODE WRITE CYCLE**



CAPACITANCE

(V_{DD} = 12.0V ± 10%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%, f = 1MHz, Ta = 0°C ~ 70°C)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
Ci_1	Input Capacitance (A_0-A_6), D_{IN}	4	5	pF
Ci_2	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF
C_O	Output Capacitance (D_{OUT})	5	7	pF

POWER DERATING CHARACTERISTICS

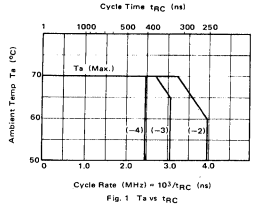


Fig. 1 Ta vs t_{RC}

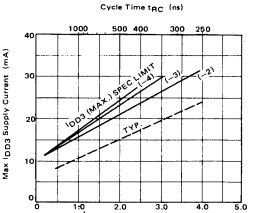


Fig. 3 t_{RC} vs I_{DD3}

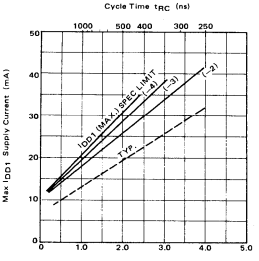


Fig. 2 t_{RC} vs I_{DD1}

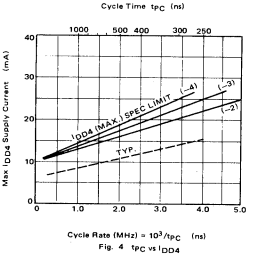


Fig. 4 t_{PC} vs I_{DD4}

NOTES

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. T_a is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min.). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met. See Fig. 1 for derating curve.
3. All voltages are referenced to V_{SS}.
4. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min.) specification is not guaranteed in this mode.
5. I_{DD1}, I_{DD3} and I_{DD4} depend on cycle rate. See figures 2, 3 and 4 for I_{DD} limits at other cycle rates.
6. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance to data out. At all other times I_{CC} consists of leakage currents only.
7. After the application of supply voltages or after extended periods of bias (greater than t_{REF}: 2ms) without clocks, the device must perform about eight initialization cycles prior to normal operation.
8. AC measurements assume t_T = 5ns.
9. The specifications for t_{RC} (min.), t_{RMW} (min.) and t_{RWC} (min.) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_a ≤ 70°C) is assured.
10. V_{IHC} (min.) or V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
11. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
12. Assumes that $t_{RCD} \geq t_{RCD}$ (max.)
13. Measured with a load equivalent to 2 TTL loads and 100pF.
14. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
16. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
17. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only.

    If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle:

    If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

APPLICATION INFORMATION

ADDRESSING

The 14 address bits required to decode 1 of the 16,384 cell locations within the TMM416P are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM416P is the high impedance (open-circuit) state. That is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until $\overline{CAS}$ is taken to the precharge (logic 1) state, whether or not $\overline{RAS}$ goes into precharge.

If the cycle in progress is an "early-write" cycle ($\overline{WRITE}$ active before $\overline{CAS}$ goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the D_{OUT} pin simply by controlling the placement of $\overline{WRITE}$ command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

PAGE MODE OPERATION

The "Page-Mode" feature of the TMM416P allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by

strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{DD3} specification.

POWER CONSIDERATIONS

Most of the circuitry used in the TMM416P is dynamic and most of the power drawn is the result of an address strobe edge. (refer to the TMM416P current waveforms in Fig. 5) In system applications requiring lower power dissipation, the operating frequency (cycle rate) of the TMM416P can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the I_{DD1} (max.) spec limit curve illustrated in Fig. 2.

It is possible to operate certain versions of the TMM416P family (–2 and 3 speed selections for example) at frequencies higher than specified, provided all AC operating parameters are met. Operation at shorter cycle times ($< t_{RC}$ min.) results in higher power dissipation and, therefore, a reduction in ambient temperature is required. Refer to Fig. 1 for derating curve.

POWER UP

The TMM416P requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, TOSHIBA recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

TYPICAL CURRENT WAVEFORMS

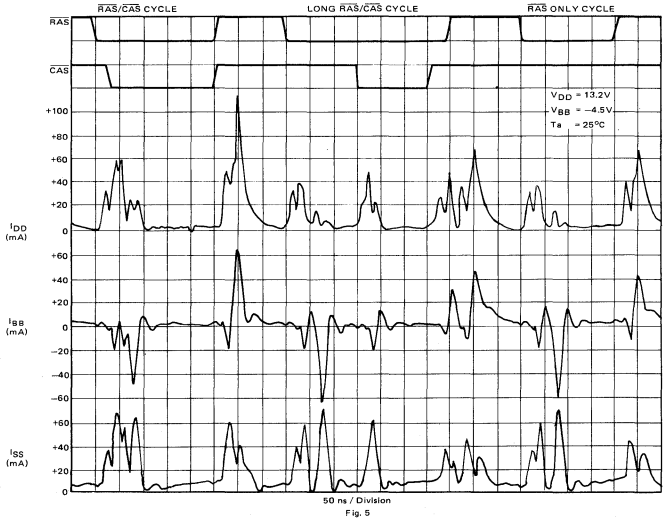
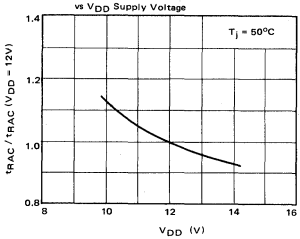


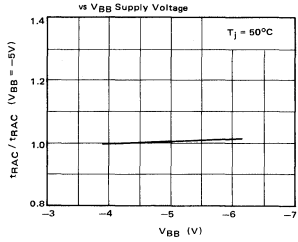
Fig. 5

TYPICAL CHARACTERISTICS

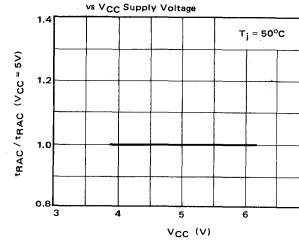
Normalized Access Time t_{RAC} vs V_{DD} Supply Voltage



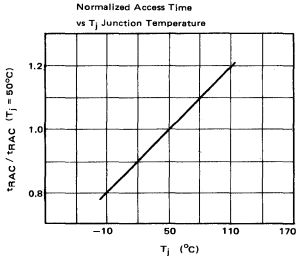
Normalized Access Time t_{RAC} vs V_{BB} Supply Voltage



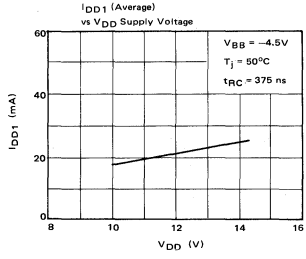
Normalized Access Time t_{RAC} vs V_{CC} Supply Voltage



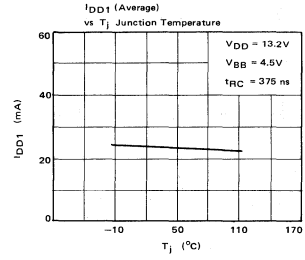
Normalized Access Time vs T_j Junction Temperature



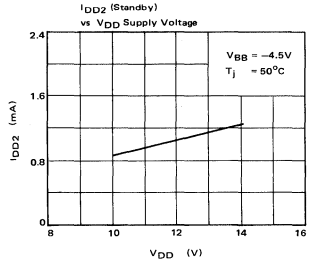
I_{DD1} (Average) vs V_{DD} Supply Voltage



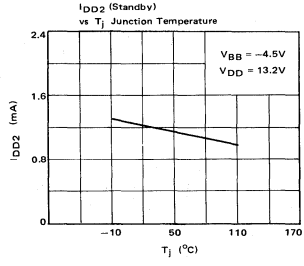
I_{DD1} (Average) vs T_j Junction Temperature



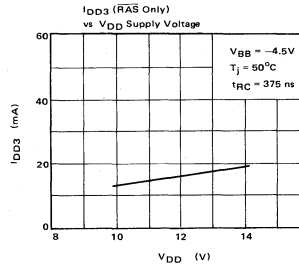
I_{DD2} (Standby) vs V_{DD} Supply Voltage



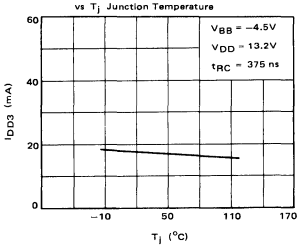
I_{DD2} (Standby) vs T_j Junction Temperature



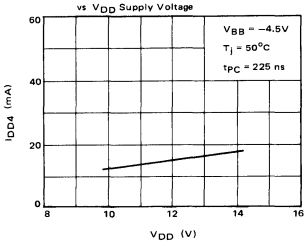
I_{DD3} ($\overline{RAS}$ Only) vs V_{DD} Supply Voltage



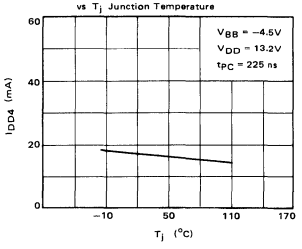
I_{DD3} ($\overline{RAS}$ Only)
vs T_j Junction Temperature



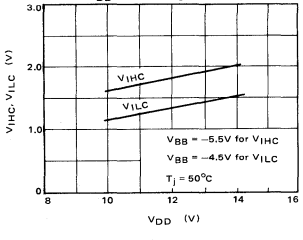
I_{DD4} (Page Mode)
vs V_{DD} Supply Voltage



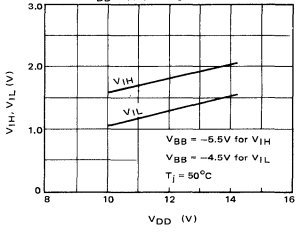
I_{DD4} (Page Mode)
vs T_j Junction Temperature



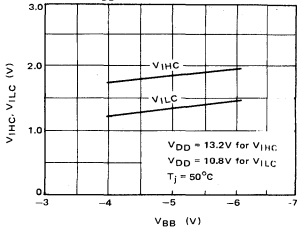
V_{IHC}, V_{ILC} Input Levels
vs V_{DD} Supply Voltage



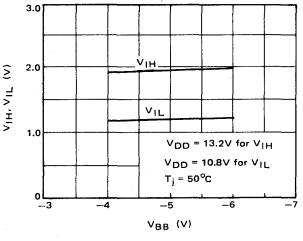
V_{IH}, V_{IL} Input Levels
vs V_{DD} Supply Voltage



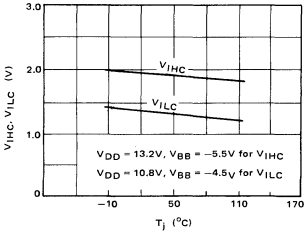
V_{IHC}, V_{ILC} Input Levels
vs V_{BB} Supply Voltage



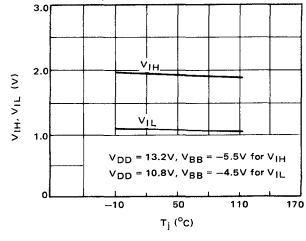
V_{IH}, V_{IL} Input Levels
vs V_{BB} Supply Voltage



V_{IHC}, V_{ILC} Input Levels
vs T_j Junction Temperature

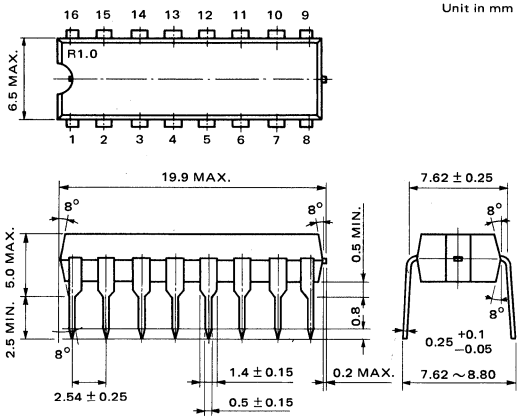


V_{IH}, V_{IL} Input Levels
vs T_j Junction Temperature



OUTLINE DRAWING

Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No. 1 and No. 16 leads.

65,536 WORD X 1 BIT DYNAMIC RAM

N-CHANNEL SILICON GATE MOS

TMM4164P-2, TMM4164P-3 TMM4164P-4

DESCRIPTION

The TMM4164P is the new generation dynamic RAM organized 65,536 words by 1 bit, it is successor to the industry standard TMM416P.

The TMM4164P utilizes TOSHIBA's double poly N-channel Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TMM4164P to be packaged in a standard 16 pin plastic DIP. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include single power supply of 5V ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

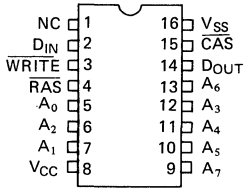
FEATURES

- 65,536 words by 1 bit organization
- Fast access time and cycle time

DEVICE	t_{RAC}	t_{RC}
TMM4164P-2	120 ns	260 ns
TMM4164P-3	150 ns	260 ns
TMM4164P-4	200 ns	330 ns

- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Low power; 275mW operating (MAX.)
  27.5mW standby (MAX.)
- Industry standard 16 pin plastic DIP
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh and Page Mode capability
- All inputs and output TTL compatible
- 128 refresh cycles/2ms

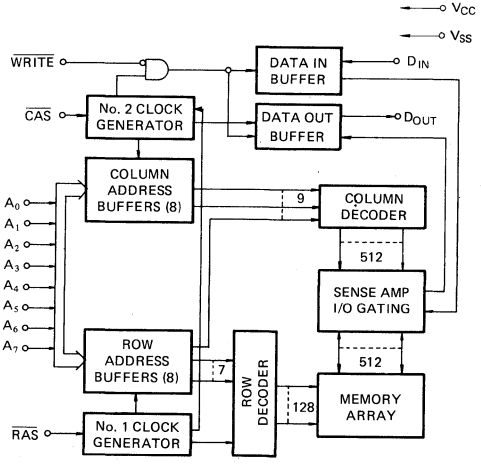
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_7$	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
NC	No – Connection
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	−55 ~ 150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4		6.5	V	2
V_{IL}	Input Low Voltage	−1.0		0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)			50	mA	3,4
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = V_{IH}, D_{OUT} = High Impedance)			5	mA	
I_{CC3}	REFRESH CURRENT Average Power Supply Current, Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)			40	mA	3
I_{CC4}	PAGE MODE CURRENT Average Power Supply Current, Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling: t_{PC} = t_{PC} MIN.)			40	mA	3, 4
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (OV ≦ V_{IN} ≦ 6.5V All Other Pins Not Under Test = 0V)	−10		10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, OV ≦ V_{OUT} ≦ +5.5V)	−10		10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −5mA)	2.4			V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)			0.4	V	

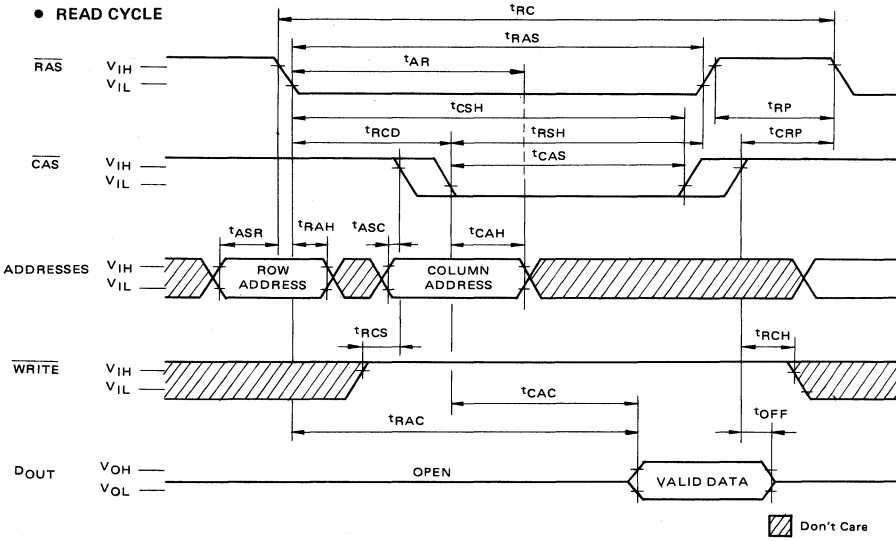
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 5, 6, 7)

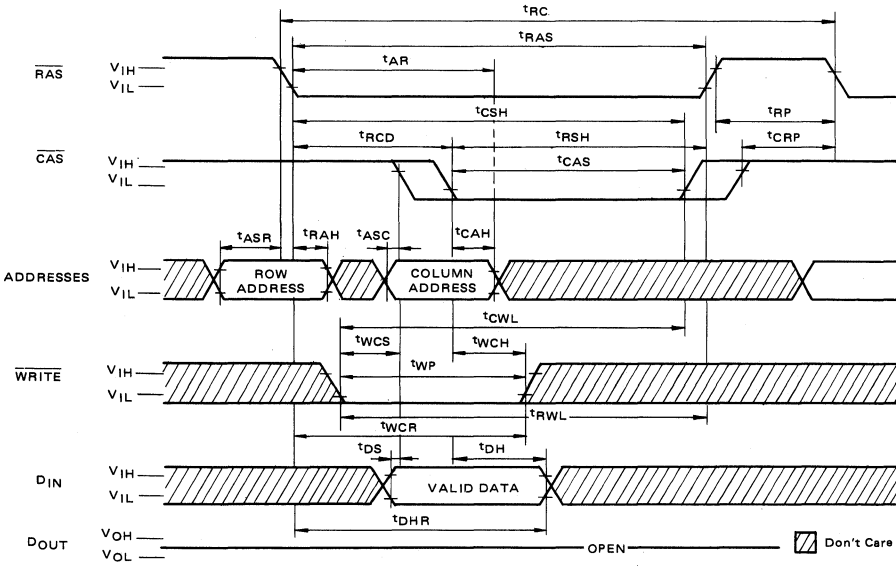
SYMBOL	PARAMETER	TMM4164P-2		TMM4164P-3		TMM4164P-4		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random read or write cycle time	260		260		330		ns	
t_{RWC}	Read-write cycle time	260		270		335		ns	
t_{RMW}	Read-modify-write cycle time	265		310		390		ns	
t_{PC}	Page mode cycle time	140		170		225		ns	
t_{RAC}	Access time from $\overline{RAS}$		120		150		200	ns	8, 10
t_{CAC}	Access time from $\overline{CAS}$		80		100		135	ns	9, 10
t_{OFF}	Output buffer turn-off delay	0	35	0	40	0	50	ns	11
t_T	Transition time (rise and fall)	3	35	3	35	3	50	ns	6
t_{RP}	$\overline{RAS}$ precharge time	90		100		120		ns	
t_{RAS}	$\overline{RAS}$ pulse width	120	10,000	150	10,000	200	10,000	ns	
t_{RSH}	$\overline{RAS}$ hold time	80		100		135		ns	
t_{CSH}	$\overline{CAS}$ hold time	120		150		200		ns	
t_{CAS}	$\overline{CAS}$ pulse width	80	10,000	100	10,000	135	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	25	40	25	50	30	65	ns	12
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	0		0		0		ns	
t_{ASR}	Row Address set-up time	0		0		0		ns	
t_{RAH}	Row Address hold time	15		15		20		ns	
t_{ASC}	Column Address set-up time	0		0		0		ns	
t_{CAH}	Column Address hold time	40		45		55		ns	
t_{AR}	Column Address hold time referenced to $\overline{RAS}$	80		95		120		ns	
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	40		45		55		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	80		95		120		ns	
t_{WP}	Write command pulse width	40		45		55		ns	
t_{RWL}	Write command to $\overline{RAS}$ lead time	40		45		55		ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	40		45		55		ns	
t_{DS}	Data-in set-up time	0		0		0		ns	13
t_{DH}	Data-in hold time	40		45		55		ns	13
t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	80		95		120		ns	
t_{CP}	$\overline{CAS}$ precharge time (for page-mode cycle only)	50		60		80		ns	
t_{REF}	Refresh period		2		2		2	ms	
t_{WCS}	Write command set-up time	−10		−10		−10		ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	50		60		80		ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	90		110		145		ns	14

TIMING WAVEFORMS

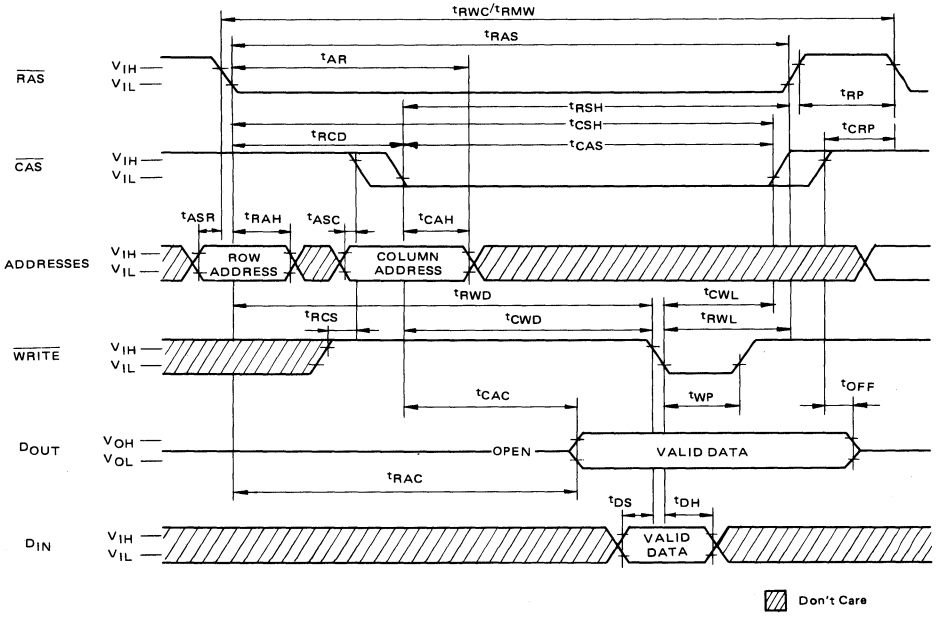
- READ CYCLE



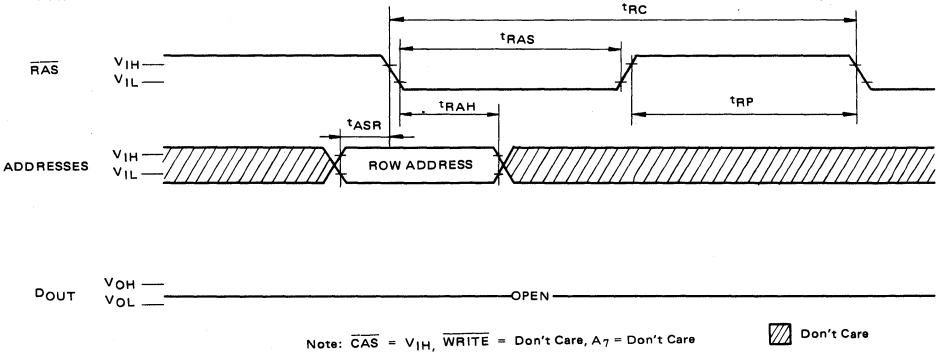
- WRITE CYCLE (EARLY WRITE)



- **READ-WRITE/READ-MODIFY-WRITE CYCLE**

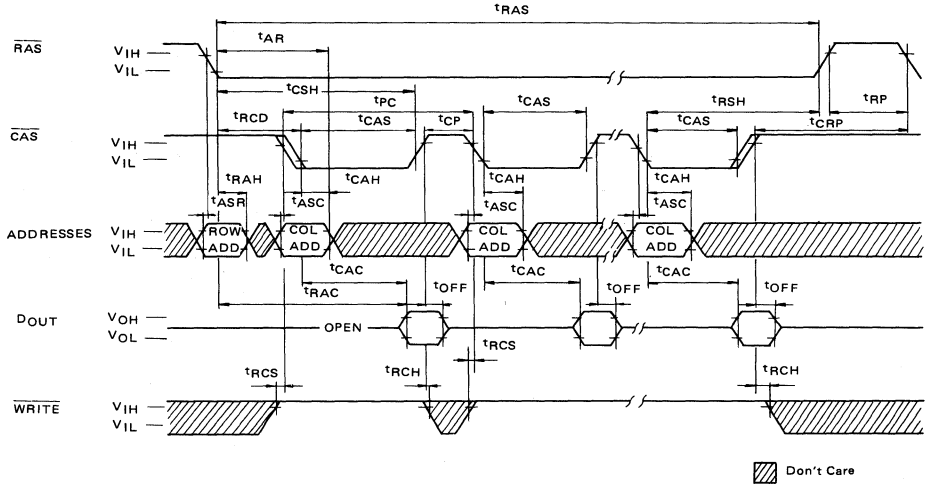


- **"$\overline{\text{RAS}}$-ONLY" REFRESH CYCLE**

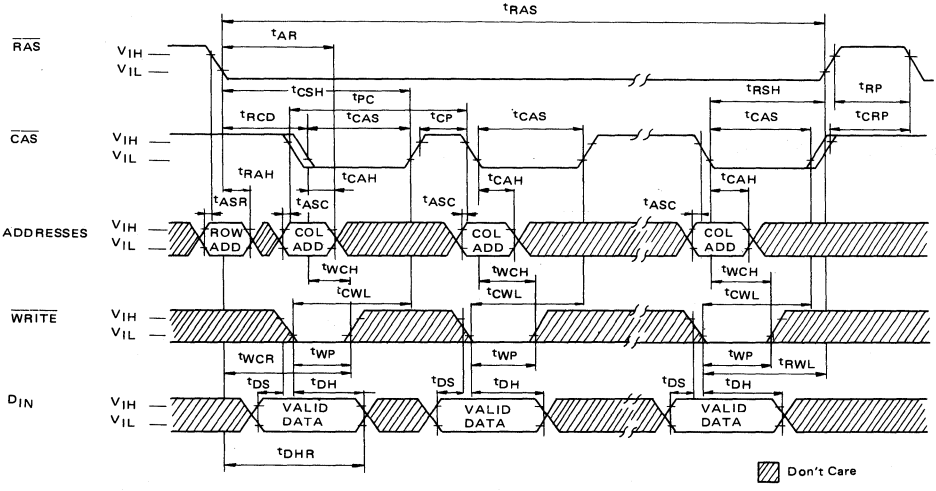


Note: $\overline{\text{CAS}}$ = V_{IH}, $\overline{\text{WRITE}}$ = Don't Care, A_7 = Don't Care

- **PAGE MODE READ CYCLE**



- **PAGE MODE WRITE CYCLE**



CAPACITANCE

(V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
C_{I1}	Input Capacitance ($A_0 \sim A_7$, D_{IN})		4	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)		8	10	pF
C_O	Output Capacitance (D_{OUT})		5	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8$\overline{RAS}$ cycles before proper device operation is achieved.
6. AC measurements assume t_T = 5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
14. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle:
    If $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{RWD} \geqq t_{RWD}$ (min.), the cycle is read-write cycle or read-modify-cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TMM4164P are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 8 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM4164P is the high impedance (open circuit) state. That is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

PAGE MODE

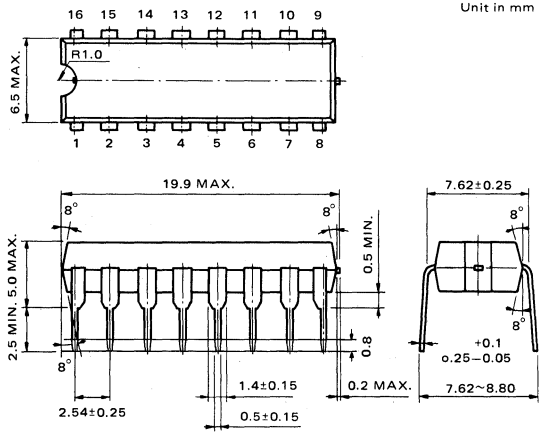
The "Page-Mode" feature of the TMM4164P allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page-Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row address ($A_0 \sim A_6$) within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 16 leads.
All dimensions are in millimeters.

65,536 WORD X 1 BIT DYNAMIC RAM

N-CHANNEL SILICON GATE MOS

TMM4164AP-12
TMM4164AP-15
TMM4164AP-20

*** This is advance information and specifications are subject to change without notice.**

DESCRIPTION

The TMM4164AP is the high speed, low power dynamic RAM organized 65,536 words by 1 bit, it is successor to the industry standard TMM4164P.

The TMM4164AP utilizes TOSHIBA's double poly N-channel Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TMM4164AP to be packaged in a standard 16 pin plastic DIP. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include single power supply of 5V ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

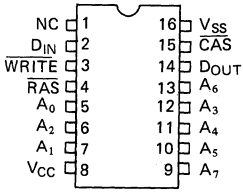
FEATURES

- 65,536 words by 1 bit organization
- Fast access time and cycle time

DEVICE	t_{RAC}	t_{CAC}	t_{RC}
TMM4164AP-12	120 ns	60 ns	220 ns
TMM4164AP-15	150 ns	75 ns	260 ns
TMM4164AP-20	200 ns	100 ns	330 ns

- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Low power; 275mW operating (MAX.)
  22mW standby (MAX.)
- Industry standard 16 pin plastic DIP
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh and Page Mode capability
- All inputs and output TTL compatible
- 128 refresh cycles/2ms

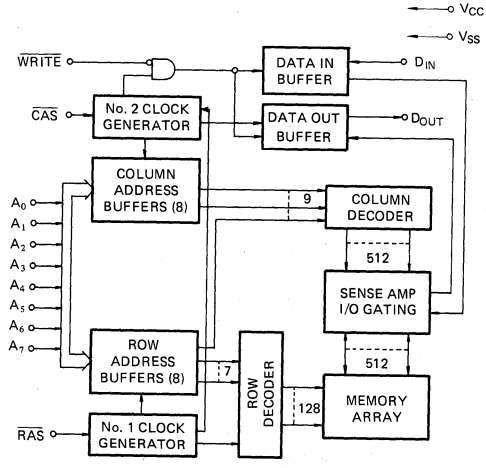
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_7$	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
NC	No – Connection
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	−55 ~ 150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4		6.5	V	2
V_{IL}	Input Low Voltage	−1.0		0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)			50	mA	3,4
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = V_{IH}, D_{OUT} = High Impedance)			4	mA	
I_{CC3}	REFRESH CURRENT Average Power Supply Current, Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)			40	mA	3
I_{CC4}	PAGE MODE CURRENT Average Power Supply Current, Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling: t_{PC} = t_{PC} MIN.)			40	mA	3, 4
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)	−10		10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ +5.5V)	−10		10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −5mA)	2.4			V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)			0.4	V	

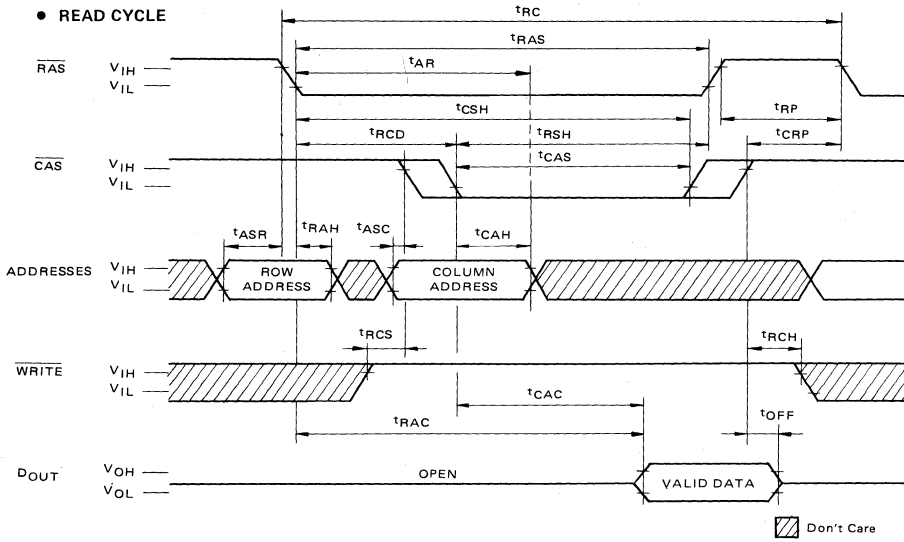
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 5, 6, 7)

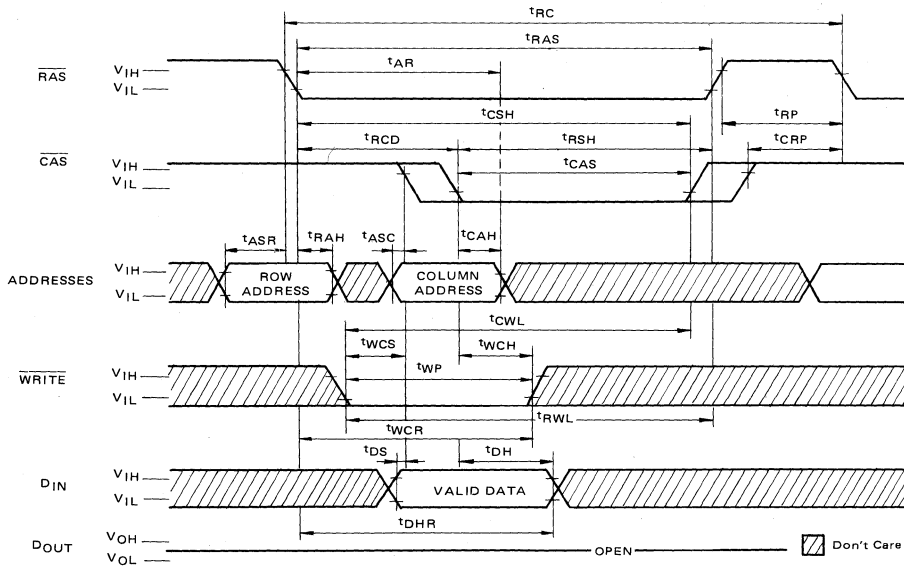
SYMBOL	PARAMETER	TMM4164AP-12		TMM4164AP-15		TMM4164AP-20		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	220		260		330		ns	
t_{RWC}	Read-Write Cycle Time	240		285		350		ns	
t_{RMW}	Read-Modify-Write Cycle Time	260		310		390		ns	
t_{PC}	Page Mode Cycle Time	120		145		190		ns	
t_{RAC}	Access Time from $\overline{RAS}$		120		150		200	ns	8, 10
t_{CAC}	Access Time from $\overline{CAS}$		60		75		100	ns	9, 10
t_{OFF}	Output Buffer Turn-Off Delay	0	35	0	40	0	50	ns	11
t_T	Transition Time (Rise and Fall)	3	35	3	35	3	50	ns	6
t_{RP}	$\overline{RAS}$ Precharge Time	90		100		120		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	120	10,000	150	10,000	200	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	60		75		100		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	120		150		200		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	75	10,000	100	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	30	100	ns	12
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		ns	
t_{ASR}	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	15		15		20		ns	
t_{ASC}	Column Address Set-Up Time	0		0		0		ns	
t_{CAH}	Column Address Hold Time	35		45		55		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	95		120		155		ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{WCH}	Write Command Hold Time	35		45		55		ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		120		155		ns	
t_{WP}	Write Command Pulse Width	35		45		55		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	35		45		55		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	35		45		55		ns	
t_{DS}	Data-In Set-Up Time	0		0		0		ns	13
t_{DH}	Data-In Hold Time	35		45		55		ns	13
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	95		120		155		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (for Page Mode Cycle Only)	50		60		80		ns	
t_{REF}	Refresh Period		2		2		2	ms	
t_{WCS}	Write Command Set-Up Time	−10		−10		−10		ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	40		50		60		ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	100		125		160		ns	14

TIMING WAVEFORMS

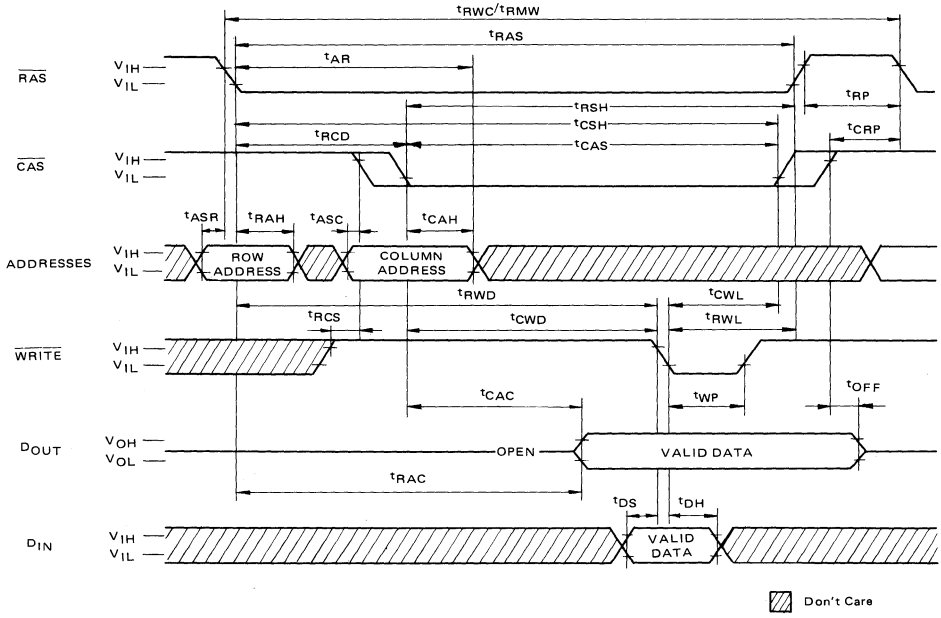
- READ CYCLE



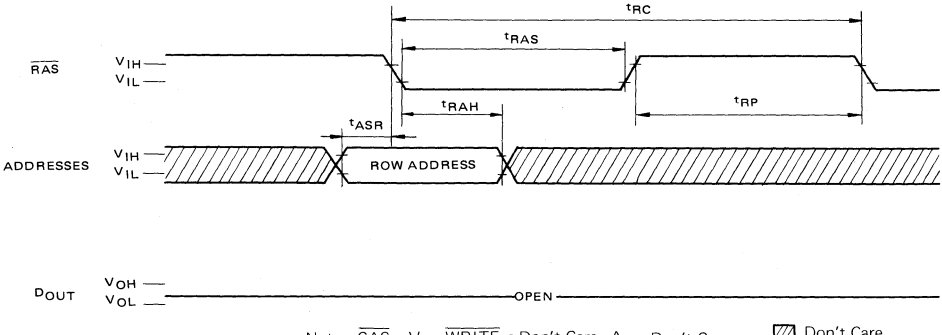
- WRITE CYCLE (EARLY WRITE)



- **READ-WRITE/READ-MODIFY-WRITE CYCLE**

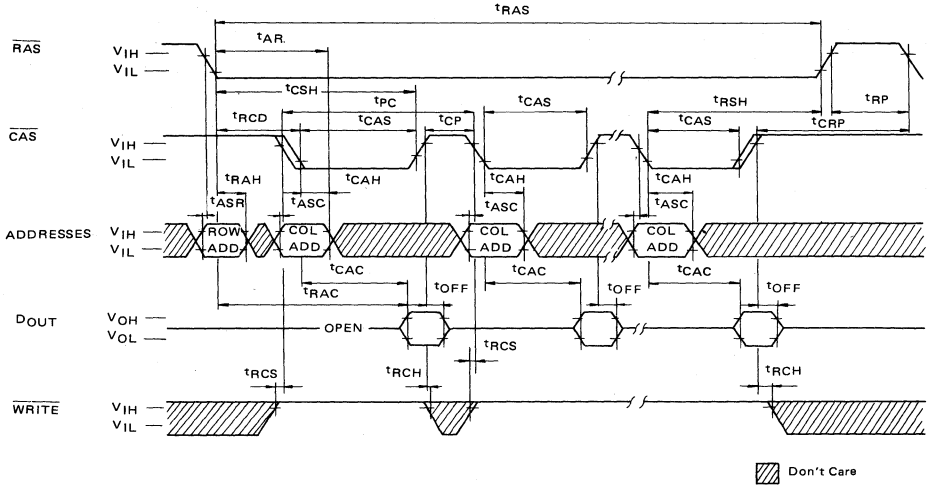


- **"$\overline{\text{RAS}}$-ONLY" REFRESH CYCLE**

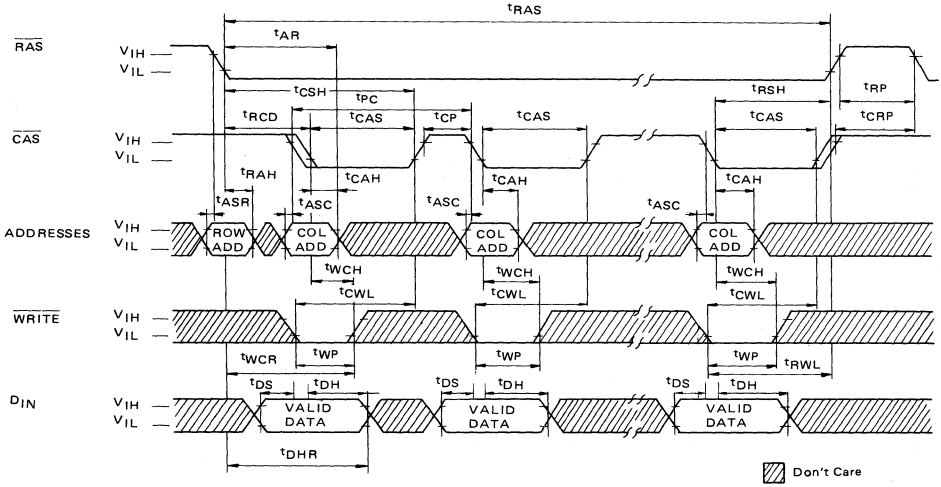


Note: $\overline{\text{CAS}} = V_{IH}$, $\overline{\text{WRITE}}$ = Don't Care, A_7 = Don't Care Don't Care

- **PAGE MODE READ CYCLE**



- **PAGE MODE WRITE CYCLE**



CAPACITANCE

(V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
C_{I1}	Input Capacitance ($A_0 \sim A_7$, D_{IN})		4	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)		8	10	pF
C_O	Output Capacitance (D_{OUT})		5	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
6. AC measurements assume t_T = 5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
14. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle:
    If $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{RWD} \geqq t_{RWD}$ (min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TMM4164AP are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 8 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM4164AP is the high impedance (open circuit) state. That is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

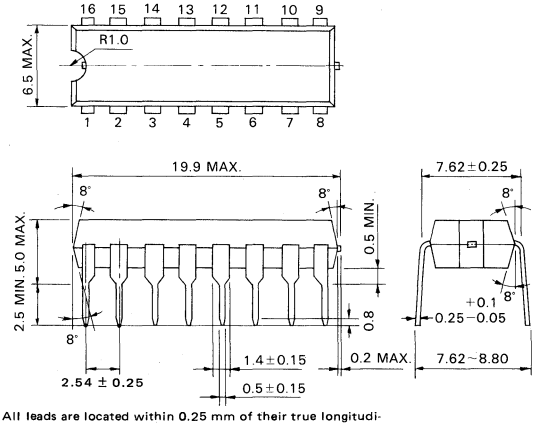
PAGE MODE

The "Page-Mode" feature of the TMM4164AP allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page-Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row address ($A_0 \sim A_6$) within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

OUTLINE DRAWINGS



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 16 leads.
All dimensions are in millimeters.

TOSHIBA MOS MEMORY PRODUCTS

262,144 WORD X 1 BIT DYNAMIC RAM

N-CHANNEL SILICON GATE MOS

TMM41256C-12
TMM41256C-15

*** This is advance information and specifications are subject to change without notice.**

DESCRIPTION

The TMM41256C is the new generation dynamic RAM organized 262,144 words by 1 bit, it is successor to the industry standard TMM4164P.

The TMM41256C utilizes TOSHIBA's N-channel Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TMM-41256C to be packaged in a standard 16 pin ceramic DIP. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include single power supply of 5V ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

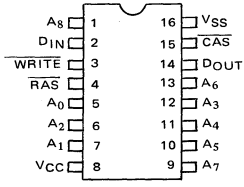
FEATURES

- 262,144 words by 1 bit organization
- Fast access time and cycle time

DEVICE	t_{RAC}	t_{CAC}	t_{RC}
TMM41256C-12	120 ns	60 ns	220 ns
TMM41256C-15	150 ns	75 ns	260 ns

- Single power supply of 5V ±10% with a built-in V_{BB} generator
- Low Power:
  330mW Operating (MAX.) (TMM41256C-12)
  275mW Operating (MAX.) (TMM41256C-15)
  27.5mW Standby (Max.)
- Industry standard 16 pin ceramic DIP
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh, Hidden refresh, and Page Mode capability.
- All inputs and output TTL compatible
- 256 refresh cycles/4ms

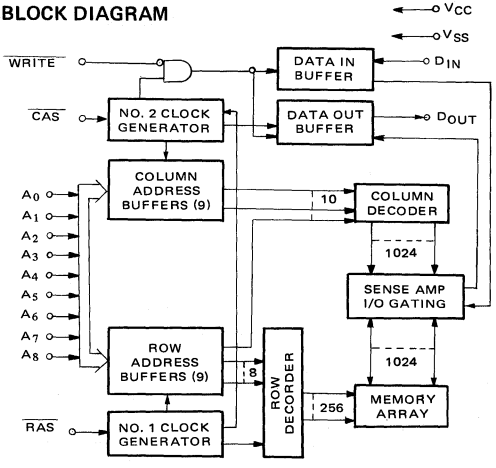
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_8$	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	−55 ~ 150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	1	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4		6.5	V	2
V_{IL}	Input Low Voltage	−1.0		0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TMM41256C-12		60	mA	3, 4
		TMM41256C-15		50		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})			5	mA	
I_{CC3}	REFRESH CURRENT Average Power Supply Current, Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} MIN.)	TMM41256C-12		45	mA	3
		TMM41256C-15		40		
I_{CC4}	PAGE MODE CURRENT Average Power Supply Current, Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling : t_{PC} = t_{PC} MIN.)	TMM41256C-12		45	mA	3, 4
		TMM41256C-15		40		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = OV)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, OV ≦ V_{OUT} ≦ +5.5V)		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −5mA)		2.4		V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)			0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ±10%, Ta = 0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41256C-12		TMM41256C-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	220	–	260	–	ns	
t_{RWC}	Read-Write Cycle Time	240	–	285	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	260	–	310	–	ns	
t_{PC}	Page Mode Cycle Time	120	–	145	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	120	–	150	ns	8, 10
t_{CAC}	Access Time from $\overline{CAS}$	–	60	–	75	ns	9, 10
t_{OFF}	Output Buffer Turn-Off Delay	0	35	0	40	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	6
t_{RP}	$\overline{RAS}$ Precharge Time	90	–	100	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	120	10,000	150	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	60	–	75	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	120	–	150	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	75	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	ns	13
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0	–	0	–	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	25	–	25	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (for Page Mode Cycle Only)	50	–	60	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	15	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	35	–	45	–	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	95	–	120	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	–	0	–	ns	12
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	15	–	20	–	ns	12
t_{WCH}	Write Command Hold Time	35	–	45	–	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95	–	120	–	ns	
t_{WP}	Write Command Pulse Width	35	–	45	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	35	–	45	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	35	–	45	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	0	–	ns	14
t_{DH}	Data-In Hold Time	35	–	45	–	ns	14
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	95	–	120	–	ns	
t_{REF}	Refresh Period	–	4	–	4	ms	
t_{WCS}	Write Command Set-Up Time	−10	–	−10	–	ns	15
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	40	–	50	–	ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	100	–	125	–	ns	15

CAPACITANCE

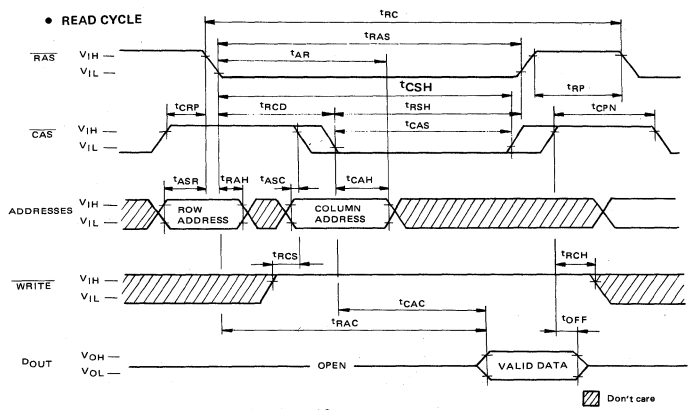
(V_{CC} = 5V ±10%, f = 1MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance ($A_0 \sim A_8$, D_{IN})		6	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)		7	pF
C_O	Output Capacitance (D_{OUT})		7	pF

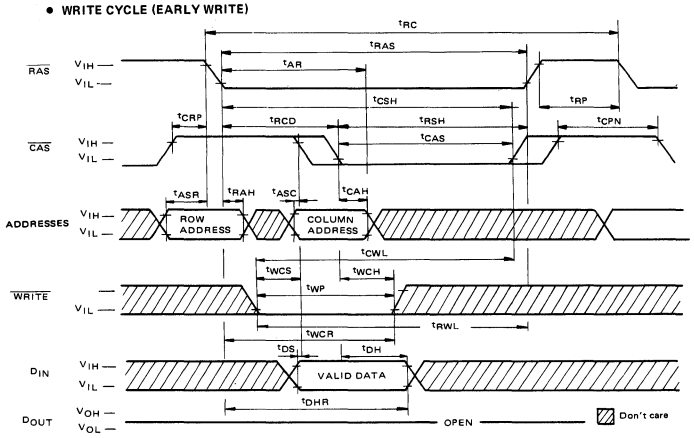
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
6. AC measurements assume t_T = 5 ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.)
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
15. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{RWD} \geqq t_{RWD}$ (min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

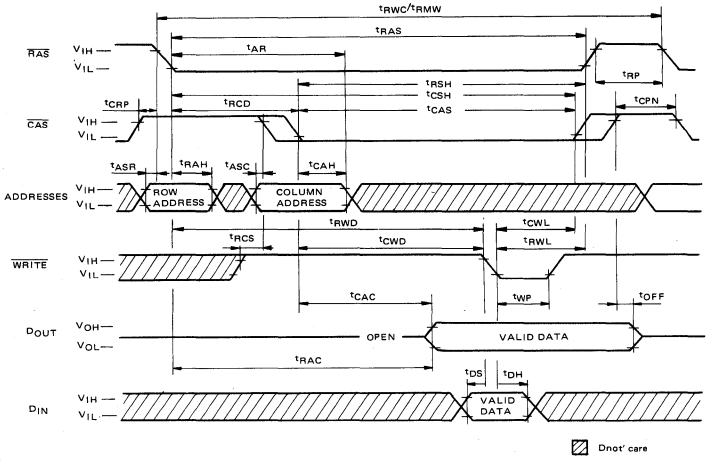
TIMING WAVEFORMS



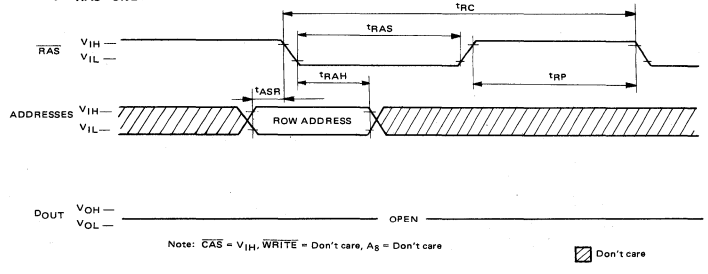
● WRITE CYCLE (EARLY WRITE)



●READ-WRITE/READ-MODIFY-WRITE CYCLE

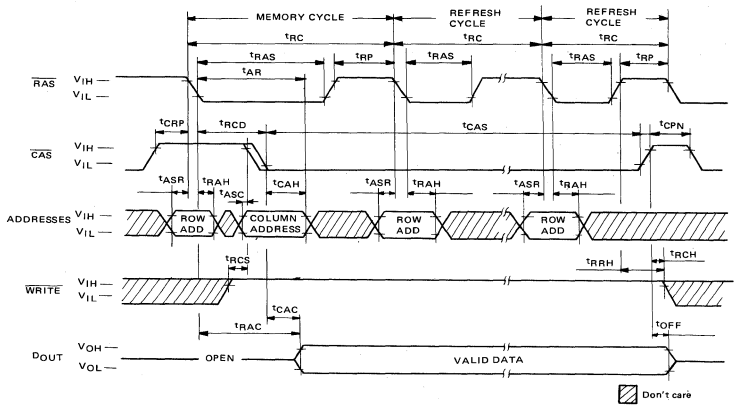


● "$\overline{RAS}$ - ONLY" REFRESH CYCLE

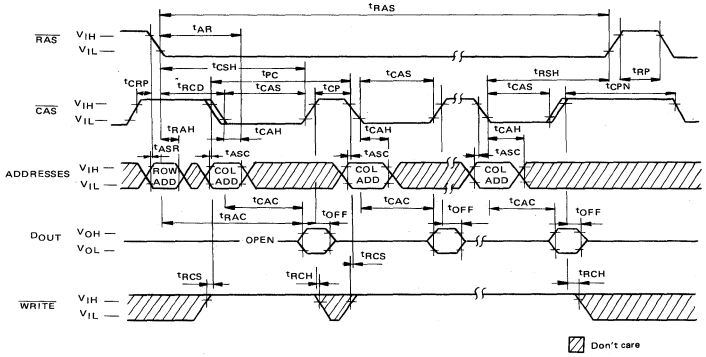


Note: $\overline{CAS}$ = V_{IH}, $\overline{WRITE}$ = Don't care, A_8 = Don't care

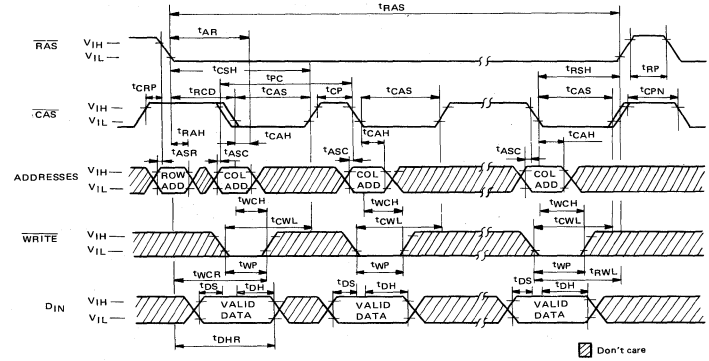
- **HIDDEN REFRESH CYCLE**



- **PAGE MODE READ CYCLE**



- **PAGE MODE WRITE CYCLE**



APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41256C are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited unitl the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM41256C is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

PAGE MODE

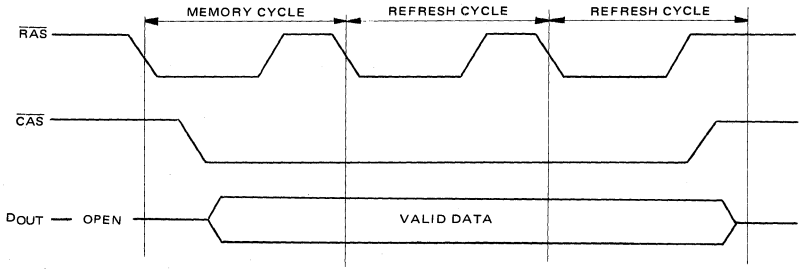
The "Page-Mode" feature of the TMM41256C allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

REFERSH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address ($A_0 \sim A_7$) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this funciton is most easily accomplished with "$\overline{RAS}$ - only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

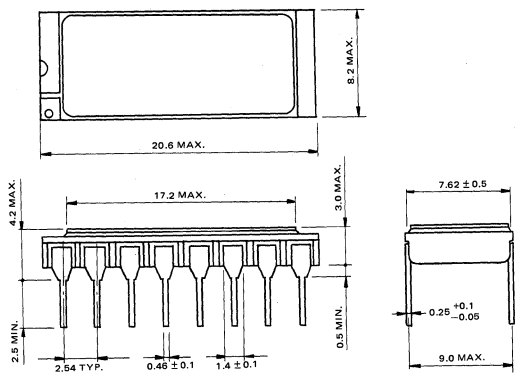
HIDDEN REFRESH

An optional feature of the TMM41256C is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a "$\overline{RAS}$ - only" refresh cycle, but with $\overline{CAS}$ held low (see Figure below).



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

OUTLINE DRAWINGS



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 16 leads. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without noitce, to change said circuitry.

Static Random Access Memories

TOSHIBA MOS MEMORY PRODUCTS

1024 WORD x 4 BIT STATIC RAM

N CHANNEL SILICON GATE DEPLETION LOAD

TMM314AP TMM314APL
TMM314AP-1 TMM314APL-1
TMM314AP-3 TMM314APL-3

DESCRIPTION

TMM314AP family is 1024 word x 4 bit high speed read write memories operated with 5 V single power supply. The memories with 6 Tr. cells are static in operation and require no clocks or refresh period and suitable for use in microprocessor application systems where high performance, low cost, simple interfacing are important design objectives.

TMM314AP family is able to be connected to TTL directly and to drive 1 STTL or 5 LSTTLS.

TMM314AP family is fabricated with N channel silicon gate depletion load type MOS technology by ion implantation for fast speed, stable performance and reliability.

The chip is moulded in the standard 18 pin plastic package of 0.3 inch width for low cost and high density assembly.

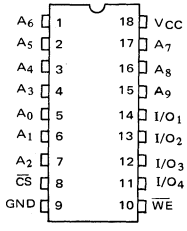
FEATURES

- Fully decoded 1024 word x 4 bit organization
- Static operation – No clocks or refresh period
- Single 5V supply voltage – V_{CC} = 5V ± 10%
- Easy memory expansion – $\overline{CS}$ input
- Three state output – Wired OR tie capability
- Inputs and outputs directly TTL compatible
- Data input/output terminal is common
- Input protected – All inputs have protection against static charge
- 2114 Type Pin compatible
- Low Power dissipation and Access time

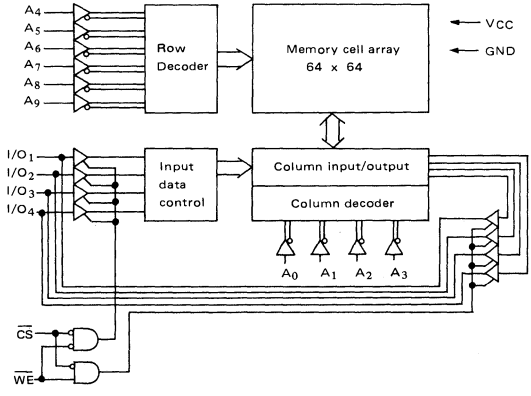
Power and Access time (maximum value)

	Access time	Power
TMM314AP-1	200 ns	550 mW
TMM314AP-3	300 ns	550 mW
TMM314AP	450 ns	550 mW
TMM314APL-1	200 ns	385 mW
TMM314APL-3	300 ns	385 mW
TMM314APL	450 ns	385 mW

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_3$	Column Address Inputs
$A_4 \sim A_9$	Row Address Inputs
$I/O_1 \sim I/O_4$	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
V_{CC}	Supply Voltage
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Supply Voltage	−0.5 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	−0.5 ~ 7.0	V
T_{OPR}	Operating Temperature	0 ~ 70	°C
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C . sec
P_D	Power dissipation (Ta = 70°C)	850	mW

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	–	2.0	–	V_{CC}	V
V_{IL}	Input Low Voltage	–	−0.5	–	0.8	V
V_{CC}	Supply Voltage	–	4.5	5	5.5	V

DC CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.*	MAX.	UNIT
I_{IH}	Input High Current	V_{IN} = 5.50 V		–	–	10	μA
I_{IL}	Input Low Current	V_{IN} = 0 V		–	–	−10	μA
V_{OH}	Output High Voltage	I_{SOURCE} = −1.0 mA		2.4	2.8	–	V
V_{OL}	Output Low Voltage	I_{SINK} = 2.1 mA		–	0.15	0.4	V
I_{OH}	Output High Current	V_{OUT} = 2.4 V		−1.0	−5.5	–	mA
I_{OL}	Output Low Current	V_{OUT} = 0.4 V		2.1	6.5	–	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 0.4 V ~ V_{CC}		–	–	±10	μA
I_{CC1}	Supply Current	TMM314A PL/PL-1/PL-3 I_{OUT} = 0 mA	25°C	–	50	64	mA
			0°C	–	–	70	
I_{CC2}	Supply Current	TMM314A P/P-1/P-3 I_{OUT} = 0 mA	25°C	–	70	90	mA
			0°C	–	–	100	

* Ta = 25°C, V_{CC} = 5V

AC CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, C_L = 100pF, t_r, t_f ≦ 10 ns)

READ CYCLE

SYMBOL	PARAMETER	TMM314AP-1/APL-1		TMM314AP-3/APL-3		TMM314AP/APL		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	200	–	300	–	450	–	ns
t_{ACC}	Access Time	–	200	–	300	–	450	ns
t_{CO}	Chip Select Time	–	70	–	100	–	100	ns
t_{CX}	Output Active from $\overline{CS}$	20	–	20	–	20	–	ns
t_{OD}	Chip Deselect Time	0	40	0	80	0	100	ns
t_{OH}	Output Hold from Address Change	20	–	20	–	20	–	ns

WRITE CYCLE

SYMBOL	PARAMETER	TMM314AP-1/APL-1		TMM314AP-3/APL-3		TMM314AP/APL		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	200	–	300	–	450	–	ns
t_{WP}	Write Pulse Width	120	–	150	–	200	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	ns
t_{ODW}	Output High Z from $\overline{WE}$	0	40	0	80	0	100	ns
t_{DS}	Data Setup Time	120	–	150	–	200	–	ns
t_{DH}	Data Hold Tome	0	–	0	–	0	–	ns
t_{AW}	Address to Write Setup Time	30	–	30	–	30	–	ns

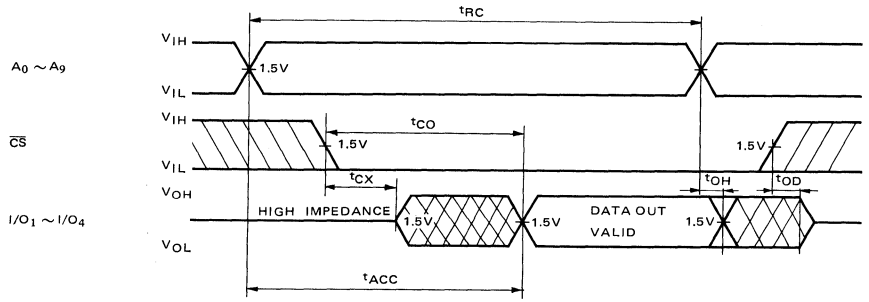
CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = AC Ground	–	–	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = AC Ground	–	–	5	pF

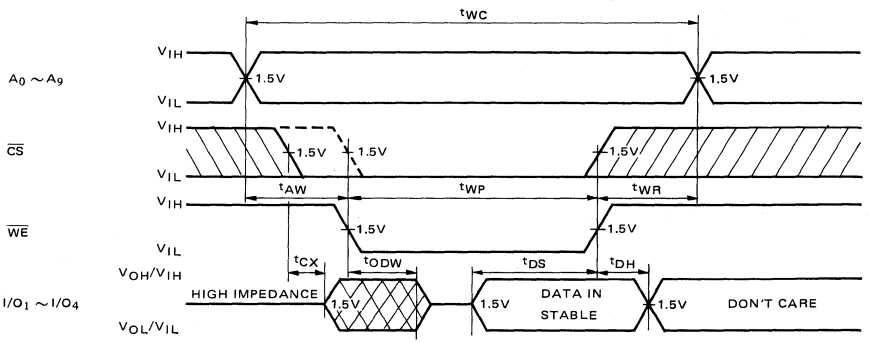
Note: This parameter is periodically sampled and not 100% tested.

TIMING WAVEFORMS

READ CYCLE



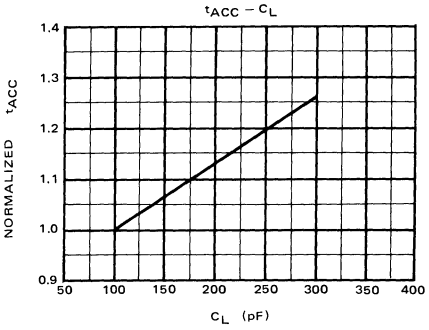
WRITE CYCLE

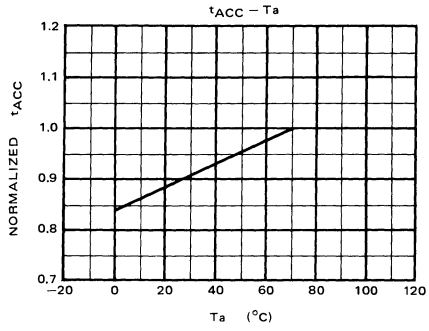


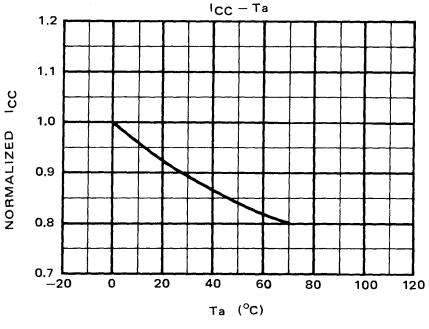
Note 1 : $\overline{WE}$ is high for a READ CYCLE.

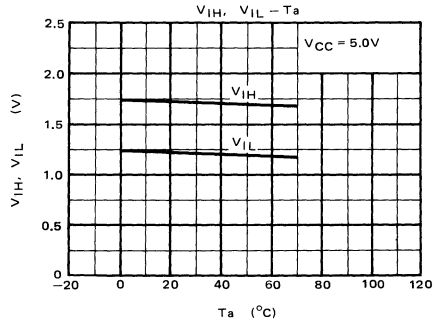
2 ; t_{WP} is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

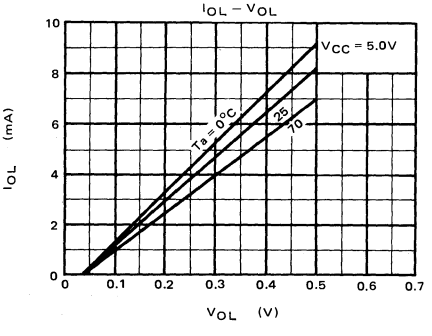
TYPICAL CHARACTERISTICS

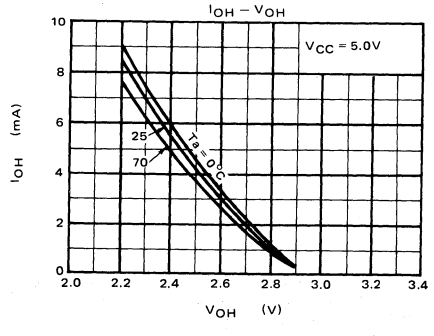




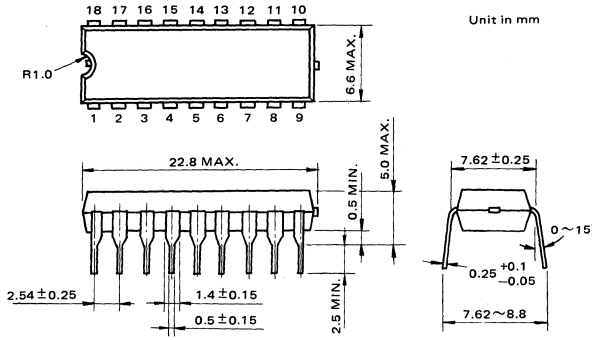








OUTLINE DRAWINGS



Notes: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 18 leads.

TOSHIBA MOS MEMORY PRODUCTS

1024 WORD x 4 BIT STATIC RAM

TMM2114AP-12
TMM2114AP-15

DESCRIPTION

The TMM2114AP is a 4,096 bits static random access memory organized as 1024 words by 4 bits and operates from a single 5V power supply. Toshiba's high performance device technology provides both high speed and low power features with maximum operating current of 60mA and maximum access time of 120ns/150ns. The memories with 6Tr. cells are fully static in operation and require no clocks or refresh periods. Therefore the TMM2114AP is most suitable for use in microcomputer peripheral memory where high performance, lower cost, simple interfacing are required.

The TMM2114AP is fabricated with N channel silicon gate depletion load type MOS technology by ion implantation for high speed, high performance and high reliability.

The chip is moulded in the standard 18 pin plastic package with 0.3 inch width.

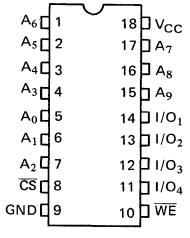
FEATURES

- 1024 Word x 4 Bit organization
- Fully static operation
- Single 5V supply voltage
- All inputs and outputs: Directly TTL compatible
- Three state output: Wired OR capability
- Common data inputs and outputs
- 2114A type pin compatible
- Fast Access time and Low Operating Current (Max.)

	TMM2114AP-12	TMM2114AP-15
$t_{ACC(ns)}$	120	150
$I_{CC(mA)}$	60	60

- Input protected: All inputs have protection against static charge.

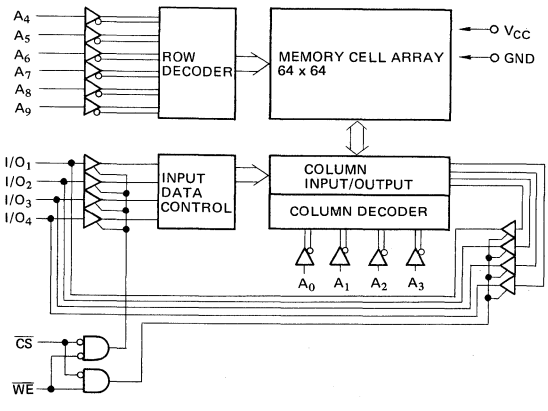
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_3$	Column Address Inputs
$A_4 \sim A_9$	Row Address Inputs
$I/O_1 \sim I/O_4$	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
V_{CC}	Supply Voltage
GND	Ground

BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	MODE
H	*	*	High Impedance	Non-decode
L	H	*	Data Output	Read
L	L	H/L	Data Input	Write

* L or H

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Supply Voltage	−0.5 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	−0.5 ~ 7.0	V
T_{OPR}	Operating Temperature	0 ~ 70	°C
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
P_D	Power Dissipation (Ta = 70°C)	850	mW

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	–	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5	–	0.8	V
V_{CC}	Supply Voltage	4.5	5	5.5	V

DC CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.*	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0V ~ 5.5V	−10	–	10	μA
V_{OH}	Output High Voltage	I_{SOURCE} = −1.0mA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{SINK} = 2.1mA	–	–	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 0.0V ~ 5.5V	−10	–	10	μA
I_{CC}	Supply Current	I_{OUT} = 0mA	–	–	60	mA

* Ta = 25°C, V_{CC} = 5V

AC CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, 1-TTL Gate & C_L = 100pF, t_r, t_f ≦ 10 ns)

READ CYCLE

SYMBOL	PARAMETER	TMM2114AP-12			TMM2114AP-15			UNIT
		MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
t_{RC}	Read Cycle Time	120	–	–	150	–	–	ns
t_{ACC}	Access Time	–	–	120	–	–	150	ns
t_{CO}	Chip Select Time	–	–	70	–	–	70	ns
t_{CX}	Output Active from $\overline{CS}$	10	–	–	10	–	–	ns
t_{OD}	Deselect Time	0	–	35	0	–	40	ns
t_{OH}	Output Hold From Address Change	20	–	–	20	–	–	ns

* Ta = 25°C, V_{CC} = 5V

WRITE CYCLE

SYMBOL	PARAMETER	TMM2114AP-12			TMM2114AP-15			UNIT
		MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
t_{WC}	Write Cycle Time	120	–	–	150	–	–	ns
t_{WP}	Write Pulse Width	70	–	–	90	–	–	ns
t_{WR}	Write Recovery Time	0	–	–	0	–	–	ns
t_{ODW}	Output High Z From $\overline{WE}$	0	–	35	0	–	40	ns
t_{DS}	Data Setup Time	70	–	–	90	–	–	ns
t_{DH}	Data Hold Time	0	–	–	0	–	–	ns
t_{AW}	Address to Write Setup Time	0	–	–	0	–	–	ns

* Ta = 25°C, V_{CC} = 5V

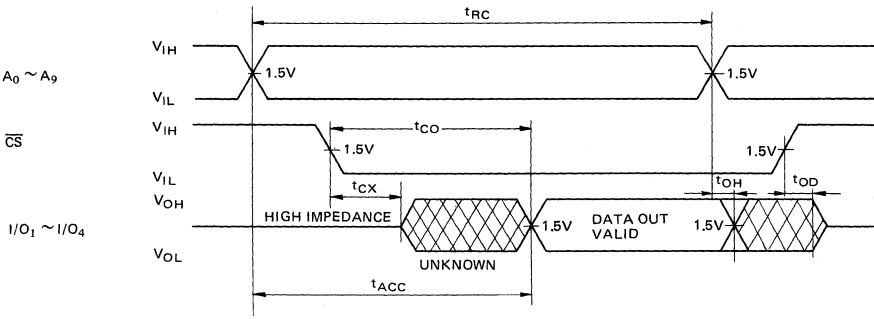
CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = AC Ground	–	–	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = AC Ground	–	–	10	pF

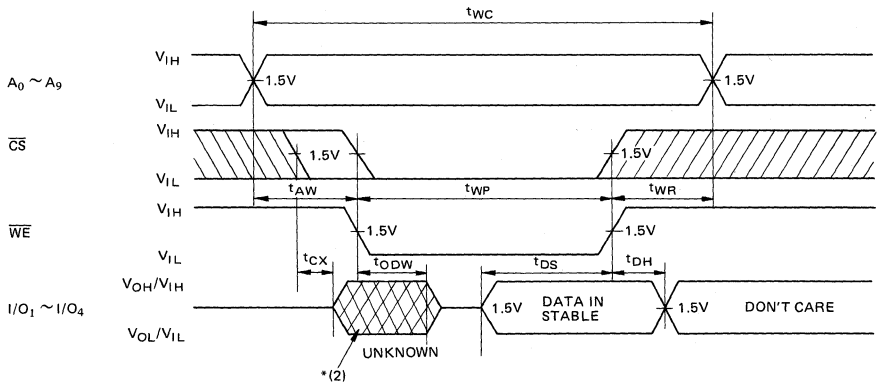
Note: This parameter is periodically sampled and not 100% tested.

TIMING WAVEFORMS

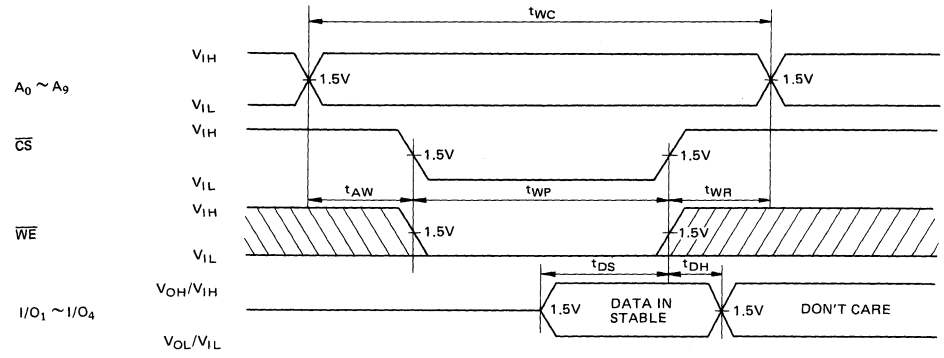
- **READ CYCLE**



- **WRITE CYCLE [1] *(1)**



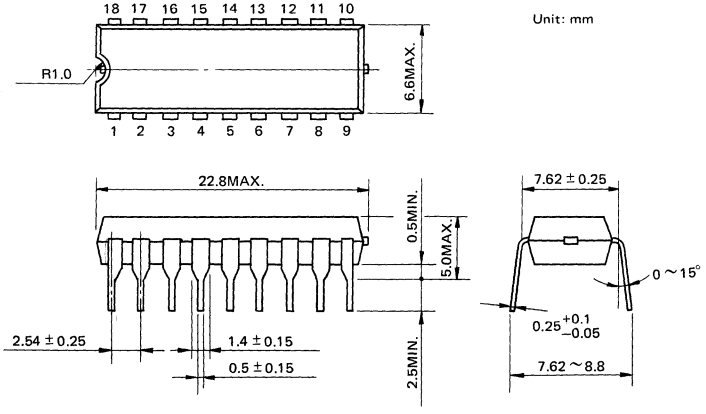
- **WRITE CYCLE [2] *(1)**



Note *(1): A write occurs during the overlap of a low $\overline{CS}$ and low $\overline{WE}$.
And twp is specified as the logical 'AND' of $\overline{CS}$ and $\overline{WE}$.

*(2): If the $\overline{CS}$ low transition occurs simultaneously with or latter from $\overline{WE}$ low transition, the output buffers remain in a high impedance state in this period.

OUTLINE DRAWINGS



Note: All dimensions are in millimeters. Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads.

TOSHIBA MOS MEMORY PRODUCTS

4096 WORD x 1 BIT STATIC RAM

N CHANNEL SILICON GATE DEPLETION LOAD

TMM315D
TMM315D-1

DESCRIPTION

TMM315D/TMM315D-1 are 4096 word x 1 bit read write memories operated with 5V single power supply. The memories are static in operation and require no clocks or refresh period. This device has two types in data access - address access and chip select access which are equal and very high speed. When $\overline{CS}$ goes high, this device is deselected and changes into the low power standby mode automatically, and keep its state during the period that $\overline{CS}$ is high. Accordingly, this device is suitable for use in larger memory system which the majority of devices are deselected, and is suitable for use in cache memory required very high speed. TMM315D/TMM315D-1 are directly TTL compatible and its output can drive the TTL up to 5. TMM315D/TMM315D-1 are fabricated with N-channel silicon gate depletion load type technology for stable and high performance. The chip is mounted in the standard 18 pin package of 0.3 inch width for low cost purpose.

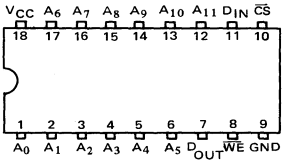
FEATURES

- Fully decoded 4096 word x 1 bit organization
- Static operation – No clocks
- 5V single power supply
- Easy memory expansion – $\overline{CS}$ input
- Standby feature – $\overline{CS} = V_{IH}$
- I/O separate
- Three state output
- Directly TTL compatible
- Current and Access time (Maximum value)

PARAMETER	TMM315D-1	TMM315D
Active Current (Max.)	180 mA	160 mA
Standby Current (Max.)	30 mA	20 mA
Address Access time	55 ns	70 ns
Chip select Access time	55 ns	70 ns

- Pin to pin compatible – i2147/i2147-3
- Inputs protected – All inputs have protection against static charge.

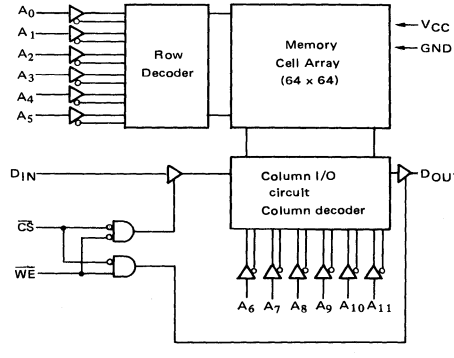
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_5$	Row Address inputs
$A_6 \sim A_{11}$	Column Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select input
$\overline{WE}$	Write enable input
V_{CC}/GND	Power supply

BLOCK DIAGRAM



OPERATION MODE

$\overline{CS}$	$\overline{WE}$	Output	Power	Mode
H	*	High-Impedance	Standby	Deselected
L	H	Data out	Active	Read
L	L	High-Impedance	Active	Write

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power supply voltage	−1.5 ~ 7.0	V
$V_{IN, OUT}$	Input and output voltage	−1.5 ~ 7.0	V
T_{opr}	Operating temperature	0 ~ 70	°C
T_{strg}	Storage temperature	−55 ~ 150	°C
T_{solder}	Soldering temperature · time	260 · 10	°C · sec
P_D	Power dissipation (Ta = 70°C)	1.0	W
I_{out}	DC output current	20	mA

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input high voltage	—	2.0	—	6.0	V
V_{IL}	Input low voltage	—	−1.0	—	0.8	V
V_{CC}	Power supply voltage	—	4.5	5.0	5.5	V

DC and OPERATING CHARACTERISTICS

Ta = 0 ~ 70°C, V_{CC} = 5.0V± 10%,unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{OH}	Output high voltage	Isource = −4.0 mA		2.4	—	—	V
V_{OL}	Output low voltage	Isink = 8 mA		—	—	0.4	V
I_{OH}	Output high current	V_{OH} = 2.4V		−4.0	—	—	mA
I_{OL}	Output low current	V_{OL} = 0.4V		8.0	—	—	mA
I_{LI}	Input leakage current	V_{IN} = 0 ~ V_{CC}		—	±0.01	±10	μA
I_{LO}	Output leakage current	V_{OUT} = 0 ~ 4.5V $\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL}		—	±0.1	±50	μA
I_{CC}	Operating current	$\overline{CS}$ = V_{IL} output open	TMM315D	—	—	160	mA
			TMM315D-1	—	—	180	mA
I_{SB}	Standby current	$\overline{CS}$ = V_{IH} output open	TMM315D	—	—	20	mA
			TMM315D-1	—	—	30	mA
I_{SBP}	Peak power on current	$\overline{CS}$ = V_{IH} during power on	TMM315D	—	—	50	mA
			TMM315D-1	—	—	70	mA

* Typical values are at V_{CC} = 5.0V, Ta = 25°C.

A.C. CHARACTERISTICS

Ta = 0 ~ 70°C, V_{CC} = 5V± 10%, unless otherwise noted.

- **READ CYCLE**

SYMBOL	PARAMETER	TMM315D-1		TMM315D		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read cycle time	55	–	70	–	ns
t_{ACC}	Address access time	–	55	–	70	ns
t_{CO_1}	Chip select access time 1	–	55	–	70	ns
t_{CO_2}	Chip select access time 2	–	65	–	80	ns
t_{OH}	Output hold from address change	5	–	5	–	ns
t_{LZ}	Chip selection to output in low Z	10	–	10	–	ns
t_{HZ}	Chip deselection to output in high Z	0	40	0	40	ns
t_{PU}	Chip selection to power up time	0	–	0	–	ns
t_{PD}	Chip deselection to power down time	–	30	–	30	ns

- **WRITE CYCLE**

SYMBOL	PARAMETER	TMM315D-1		TMM315D		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write cycle time	55	–	70	–	ns
t_{CW}	Chip selection to end of write	45	–	55	–	ns
t_{AW}	Address valid to end of write	45	–	55	–	ns
t_{AS}	Address set up time	0	–	0	–	ns
t_{WP}	Write pulse width	35	–	40	–	ns
t_{WR}	Write recovery time	10	–	15	–	ns
t_{DS}	Data set up time	25	–	30	–	ns
t_{DH}	Data hold time	10	–	10	–	ns
t_{ODW}	Write enable to output in high Z	0	30	0	35	ns
t_{WO}	Output active from end of write	0	–	0	–	ns

- **AC TEST CONDITIONS**

Input pulse levels	0 ~ 3.5V
Input rise and fall times	10 ns
Input and output timing reference levels	1.5V
Output load	See Fig. 1

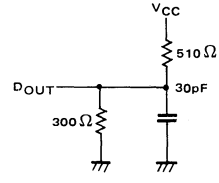


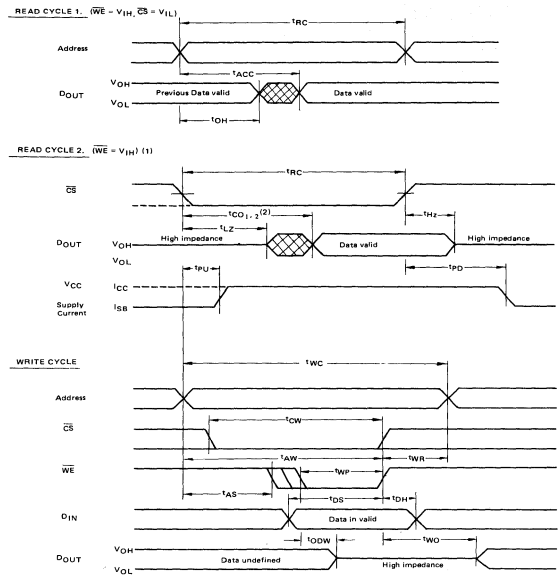
Fig. 1 Output load

CAPACITANCE (Ta = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAX.	UNIT
C_{IN}	Input capacitance	5	pF
C_{OUT}	Output capacitance	7	pF

This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS

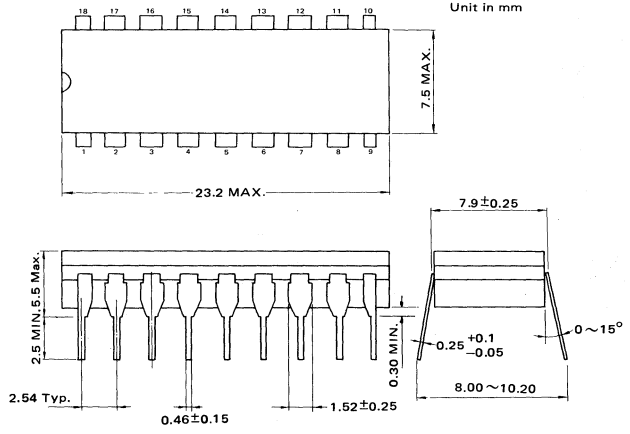


Note: (1) Addresses are to valid prior to or coincident with $\overline{CS}$ transition low.

(2) t_{CO1}: Chip is deselected for a time that is greater than 55 ns prior to selection.
t_{CO2}: Chip is deselected for a time that is less than 55 ns prior to selection.

OUTLINE DRAWINGS

Unit in mm



Note: 1. Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 18 leads.
2. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCTS

2048 WORD X 8 BIT STATIC RAM

N CHANNEL SILICON GATE DEPLETION LOAD

TMM2016P/D
TMM2016P-1/D-1
TMM2016P-2/D-2

DESCRIPTION

The TMM2016P/D is a 16384-bit static random access memory organized as 2048-words by 8-bits and operates from a single 5V power supply. Common 8-bit input/output, output enable ($\overline{OE}$) and pin-compatibility with 2716 type EPROM (TMM323D) allow a wide application in microprocessor peripheral memory.

In memory expansion, low power application is possible by using the chip select input ($\overline{CS}$). When $\overline{CS}$ is in V_{IH} level, the device is in low power standby mode.

TMM2016P/D is fabricated with ion implanted N-channel silicon gate technology. This technology provides high performance and high reliability. The TMM2016P/D is offered in both standard 24 pin plastic and cerdip packages, o.6 inch in width.

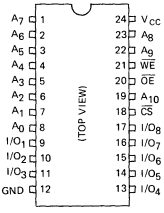
FEATURES

- Pin compatible with 2716 type EPROM
- Single 5V supply – V_{CC} = 5V ± 10%
- Access time and current

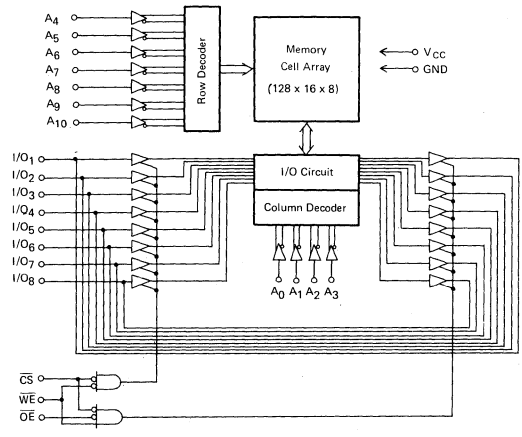
	TMM2016P/D	TMM2016P-1/D-1	TMM2016P-2/D-2
Access time (MAX.)	150 ns	100 ns	200 ns
Operating current (MAX.)	100mA	120mA	140mA
Standby current (MAX.)	15mA	15mA	30mA

- Power down feature – $\overline{CS}$
- Output buffer control – $\overline{OE}$
- Easy memory expansion – $\overline{CS}$
- Static operation – No clock or timing strobe required
- Directly TTL compatible – All inputs and outputs
- Common data input and output
- Three state outputs – Wired OR capability
- Inputs protected – All inputs have protection against static charge.

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

SYMBOL	NAME
$A_0 \sim A_3$	Column Address Inputs
$A_4 \sim A_{10}$	Row Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5 ~ 7.0	V
$V_{IN, OUT}$	Input and Output Voltage	−0.5 ~ 7.0	V
$T_{OPR.}$	Operating Temperature	0 ~ 70	°C
$T_{STG.}$	Storage Temperature	−55 ~ 150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
P_D	Power Dissipation (Ta = 70°C)	1.0	W

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage	−0.5	—	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

D.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 ~ 5.5V		—	—	±10	μA
I_{OH}	Output High Current	V_{OUT} = 2.4V		−1.0	—	—	mA
I_{OL}	Output Low Current	V_{OUT} = 0.4V		2.1	—	—	mA
V_{OH}	Output High Voltage	I_{OUT} = −1.0mA		2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA		—	—	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{CC}		—	—	±10	μA
*I_{SBP}	Peak Power-on Current	$\overline{CS}$ = V_{CC} I_{OUT} = 0mA during power on	TMM2016P/P-1/D/D-1	—	—	30	mA
			TMM2016P-2/D-2	—	—	45	mA
I_{SB}	Standby Current	$\overline{CS}$ = V_{IH} I_{OUT} = 0mA	TMM2016P/P-1/D/D-1	—	—	15	mA
			TMM2016P-2/D-2	—	—	30	mA
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL} I_{OUT} = 0mA	TMM2016P/D	—	—	100	mA
			TMM2016P-1/D-1	—	—	120	mA
			TMM2016P-2/D-2	—	—	140	mA

*Note: I_{CC} exceeds I_{SB} maximum during power on. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.

* CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = A.C. Ground	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = A.C. Ground	10	pF

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TMM2016P/D		TMM2016P-1/D-1		TMM2016P-2/D-2		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	150	–	100	–	200	–	ns
t_{ACC}	Address Access Time	–	150	–	100	–	200	ns
t_{CO}	Chip Select Access Time	–	150	–	100	–	200	ns
t_{OE}	Output Enable Time	–	55	–	35	–	55	ns
t_{OH}	Output Hold Time from Address Change	10	–	10	–	10	-	ns
t_{CLZ}	Output in Low-Z from $\overline{CS}$	10	–	10	–	10	-	ns
t_{CHZ}	Output in High-Z from $\overline{CS}$	–	55	–	40	–	55	ns
t_{OLZ}	Output in Low-Z from $\overline{OE}$	5	–	5	–	5	–	ns
t_{OHZ}	Output in High-Z from $\overline{OE}$	–	50	–	35	–	50	ns
t_{PU}	Chip Selection to Power up Time	0	–	0	–	0	-	ns
t_{PD}	Chip Deselection to Power down Time	–	60	–	50	–	60	ns

WRITE CYCLE

SYMBOL	PARAMETER	TMM2016P/D		TMM2016P-1/D1		TMM2016P-2/D-2		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	150	–	100	–	200	–	ns
t_{CW}	Chip Selection to End of Write	120	–	90	–	150	–	ns
t_{AS}	Address Set up Time	20	–	20	–	20	–	ns
t_{WP}	Write Pulse Width	100	–	70	–	120	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	ns
t_{DS}	Data Set up Time	60	–	40	–	60	–	ns
t_{DH}	Data Hold Time	15	–	10	–	15	–	ns
t_{WLZ}	Output in Low-Z from $\overline{WE}$	5	–	5	–	5	–	ns
t_{WHZ}	Output in High-Z from $\overline{WE}$	–	50	–	35	–	50	ns

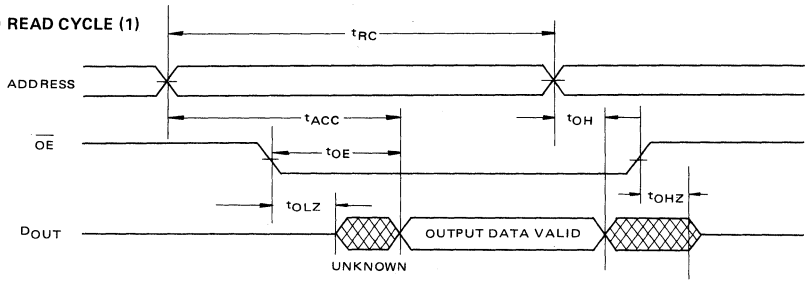
A.C. TEST CONDITIONS

Input Pulse Levels	0 ~ 3.5 V
Input Rise and Fall Times	10ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Note

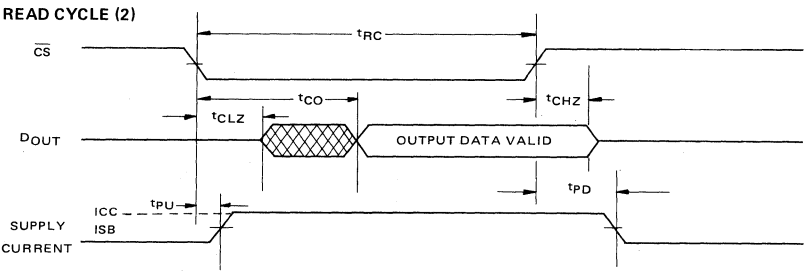
Note: Output Load – 1 TTL Gate and C_L = 100pF
(Including scope and jig)

TIMING WAVEFORMS

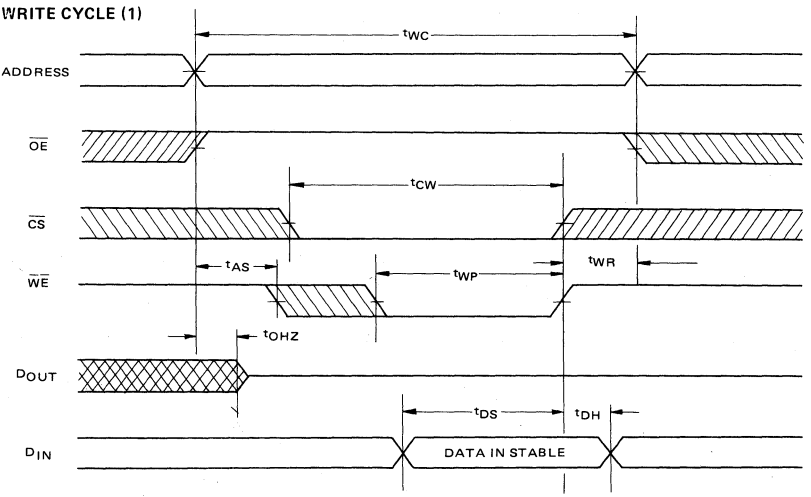
(A) READ CYCLE (1)



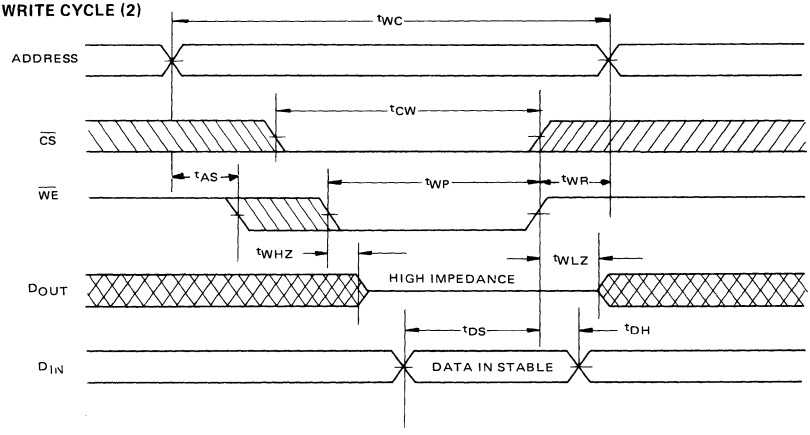
(B) READ CYCLE (2)



(C) WRITE CYCLE (1)



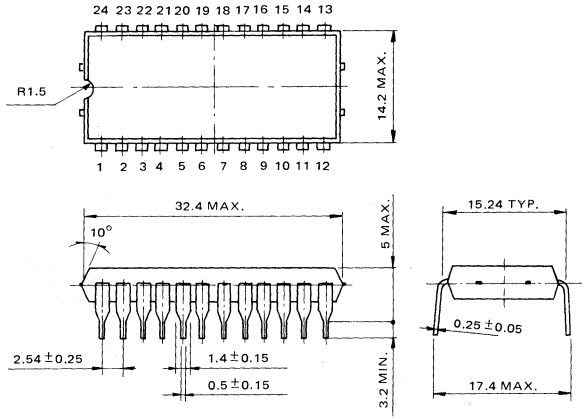
(D) WRITE CYCLE (2)



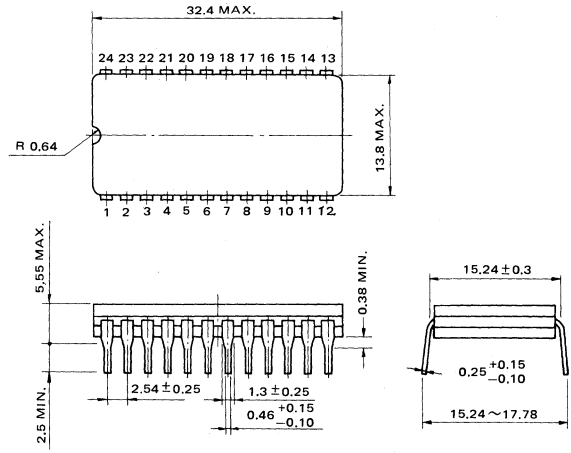
* Note: READ CYCLE (1) — $\overline{WE}$ is high for Read Cycle.
Device is continuously selected, $\overline{CS} = V_{IL}$.
READ CYCLE (2) — All addresses are valid prior to or coincident with $\overline{CS}$ transition low.
$\overline{WE}$ is high for Read Cycle. $\overline{OE} = V_{IL}$.
WRITE CYCLE (2) — $\overline{OE} = V_{IL}$.

OUTLINE DRAWINGS

- **Plastic package**



- **Cerdip package**



Note: Each lead pitch is 2.54 mm All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 24 leads.
All dimensions are in millimeters

PRELIMINARY

Characteristics are subject to change without notice.

TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD x 8 BIT STATIC RAM **TMM2016AP-90 TMM2016AP-12**
TMM2016AP-10 TMM2016AP-15

DESCRIPTION

The TMM2016AP is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns/120ns/150ns and maximum operating current of 80mA/65mA/65mA/65mA. When $\overline{CS}$ is a logical high, the device is placed in a low power standby mode in which maximum standby current is 7mA. Thus the TMM2016AP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2016AP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

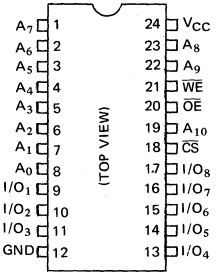
FEATURES

- Access Time and Current

Parameter / Part Number	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2016AP-90	90ns	80mA	7mA
TMM2016AP-10	100ns	65mA	7mA
TMM2016AP-12	120ns	65mA	7mA
TMM2016AP-15	150ns	65mA	7mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: $\overline{CS}$
- Output Buffer Control: $\overline{OE}$
- Three Stage Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs protected: All inputs have prtoection against static charge.

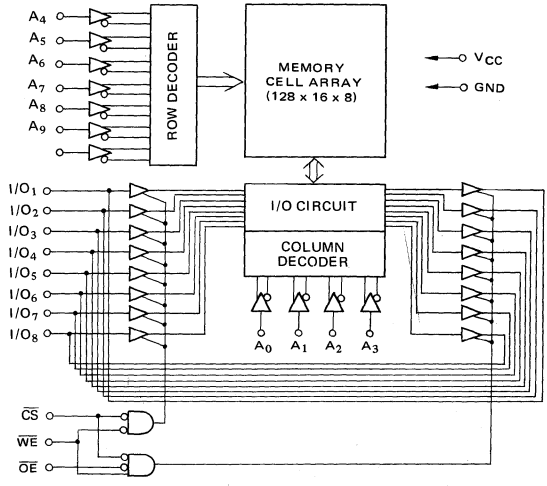
PIN CONNECTION



PIN NAMES

SYMBOL	NAME
$A_0 \sim A_3$	Column Address Inputs
$A_4 \sim A_{10}$	Row Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input/Output Voltage	−0.5 ~ 7.0	V
$T_{opr.}$	Operating Temperature	0 ~ 70	°C
$T_{stg.}$	Storage Temperature	−55 ~ 150	°C
T_{solder}	Soldering Temperature • Time	260 • 10	°C • sec
P_D	Power Dissipation (Ta = 70°C)	1.0	W

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	–	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5	–	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

D.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0V ~ 5.5V	−10	–	10	μA
V_{OH}	Output High Voltage	I_{OUT} = −1.0mA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA	–	–	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0V ~ 5.5V	−10	–	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS}$ = V_{CC}, I_{OUT} = 0mA	–	–	30	mA
I_{SB}	Standby Current	$\overline{CS}$ = V_{IH}, I_{OUT} = 0mA	–	–	7	mA
I_{CC1}	Operating Current TMM2016AP-10/-12/-15	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA	–	–	65	mA
I_{CC2}	Operating Current TMM2016AP-90	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA	–	–	80	mA

CAPACITANCE* (Ta = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = A.C. Ground	5	pF
C_{OUT}	Output Capacitance	V_{IN} = A.C. Ground	10	pF

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TMM2016AP-90		TMM2016AP-10		TMM2016AP-12		TMM2016AP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	90	–	100	–	120	–	150	–	ns
t_{ACC}	Address Access Time	–	90	–	100	–	120	–	150	ns
t_{CO}	Chip Select Access Time	–	90	–	100	–	120	–	150	ns
t_{OE}	Output Enable Time	–	35	–	35	–	50	–	55	ns
t_{OH}	Output Data Hold Time from Address Change	10	–	10	–	10	–	10	–	ns
t_{CLZ}	Output in Low-Z from $\overline{CS}$	10	–	10	–	10	–	10	–	ns
t_{CHZ}	Output in High-Z from $\overline{CS}$	–	40	–	40	–	40	–	55	ns
t_{OLZ}	Output in Low-Z from $\overline{OE}$	5	–	5	–	5	–	5	–	ns
t_{OHZ}	Output in High-Z from $\overline{OE}$	–	35	–	35	–	35	–	50	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselection to Power Down Time	–	50	–	50	–	60	–	60	ns

WRITE CYCLE

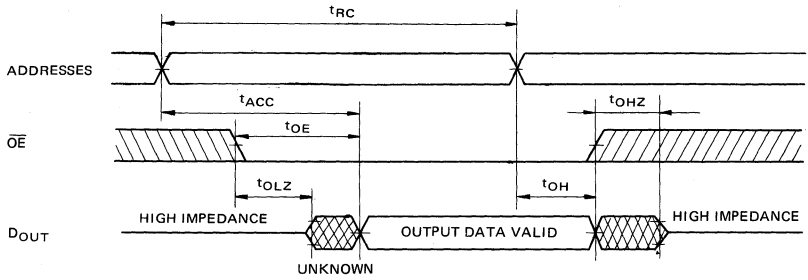
SYMBOL	PARAMETER	TMM2016AP-90		TMM2016AP-10		TMM2016AP-12		TMM2016AP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	90	–	100	–	120	–	150	–	ns
t_{CW}	Chip Selection to End of Write	70	–	80	–	100	–	120	–	ns
t_{AS}	Address Set up Time	20	–	20	–	20	–	20	–	ns
t_{WP}	Write Pulse Width	60	–	70	–	85	–	100	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{DS}	Data Set up Time	35	–	40	–	50	–	60	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns
t_{WLZ}	Output in Low-Z from $\overline{WE}$	5	–	5	–	5	–	5	–	ns
t_{WHZ}	Output in High-Z from $\overline{WE}$	–	25	–	30	–	35	–	50	ns

A.C. TEST CONDITIONS

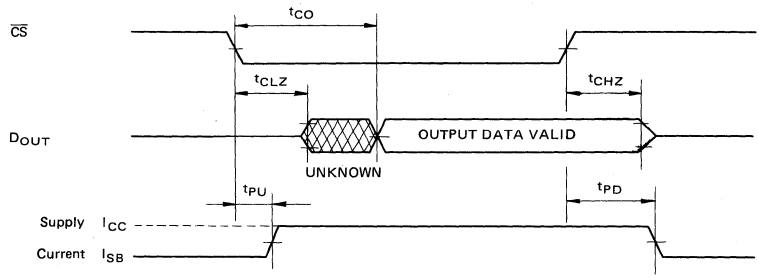
Input Pulse Levels	$0 \sim 3.5V$
Input Rise and Fall Time	10 ns
Input and Output Reference Levels	1.5V
Output Load	1 TTL Gate & $C_L = 100pF$

TIMING WAVEFORMS

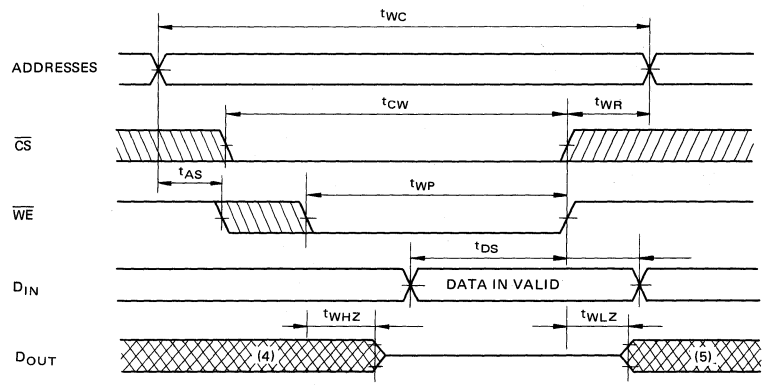
(A) READ CYCLE [1] (1)



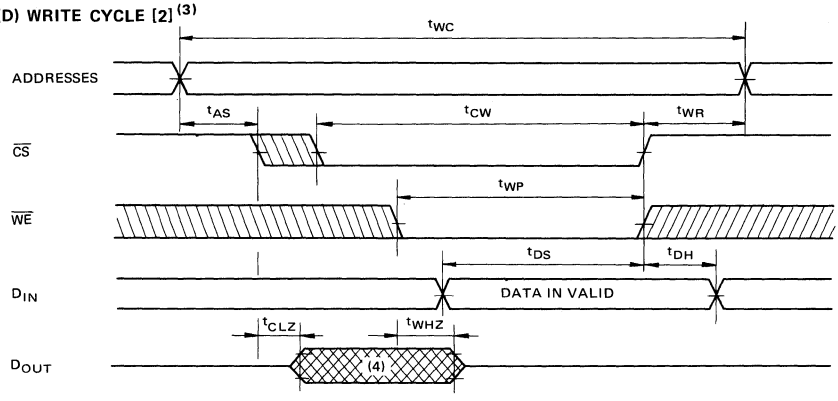
(B) READ CYCLE [2] (1)(2)



(C) WRITE CYCLE [1] (3)



(D) WRITE CYCLE [2] (3)



Note: (1) The $\overline{WE}$ is high for read cycle.
Device is continuously selected, $\overline{CS}$ = V_{IL} in read cycle [1].

(2) All address are valid perior to or simultaneously with $\overline{CS}$ transistions.

(3) A write occurs during the overlap of low $\overline{CS}$ and low $\overline{WE}$.
The t_{CW} is specified as the time from the chip selection to end of write in write cycle, and the t_{WP} is specified as the overlap time of low $\overline{CS}$ and low $\overline{WE}$.
$\overline{OE}$ is allowed to be low or high level in write cycle.
If the $\overline{OE}$ is high, the output buffers remain in a high impedance state in this period.

(4) If the $\overline{CS}$ low transistion occurs simultaneously with or latter to the $\overline{WE}$ low transition, the output buffers remain in a high impedance state in this period.

(5) If the $\overline{CS}$ high transition occurs simultaneously with $\overline{WE}$ high transition, the output buffers remain in a high impedance state in this period.

These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) t_{CLZ}, t_{OLZ}, t_{WLZ} ..... Output Enable Time
(B) t_{CHZ}, t_{OHZ}, t_{WHZ} ..... Output Disable Time

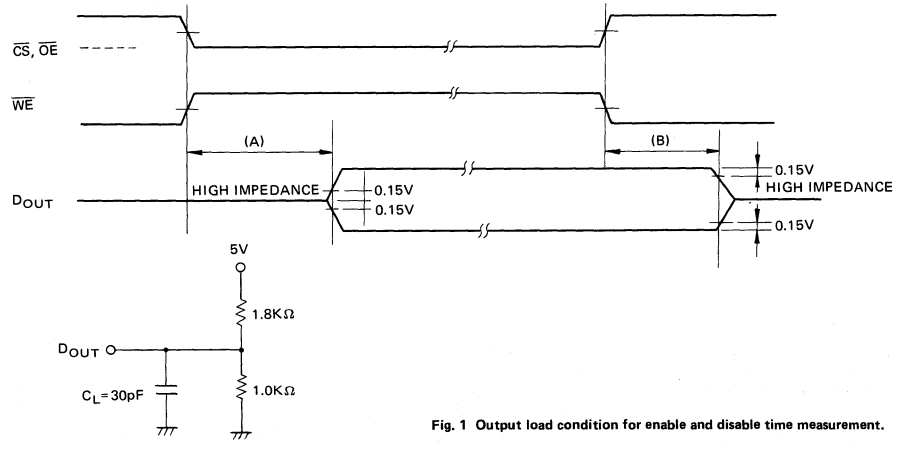
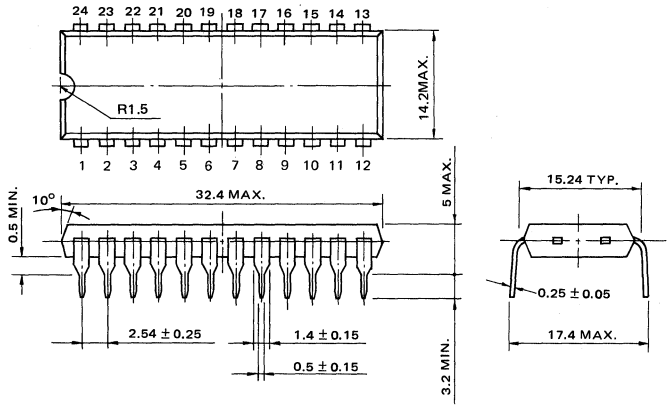


Fig. 1 Output load condition for enable and disable time measurement.

OUTLINE DRAWINGS

Unit: mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 24 leads.

TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD x 8 BIT STATIC RAM **TMM2015AP-90 TMM2015AP-12 TMM2015AP-10 TMM2015AP-15**

DESCRIPTION

The TMM2015AP is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns/120ns/150ns and maximum operating current of 80mA/65mA/65mA/65mA. When $\overline{CS}$ is a logical high, the device is placed in a low power standby mode in which maximum standby current is 7mA. Thus the TMM2015AP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2015AP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

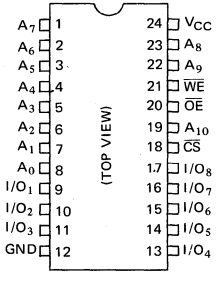
FEATURES

- Access Time and Current

Parameter / Part Number	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2015AP-90	90ns	80mA	7mA
TMM2015AP-10	100ns	65mA	7mA
TMM2015AP-12	120ns	65mA	7mA
TMM2015AP-15	150ns	65mA	7mA

- High Density Assembly Capability:
  0.3 inch package
  (24 pins plastic DIP)
- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: $\overline{CS}$
- Output Buffer Control: $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs protected: All inputs have protection against static charge.

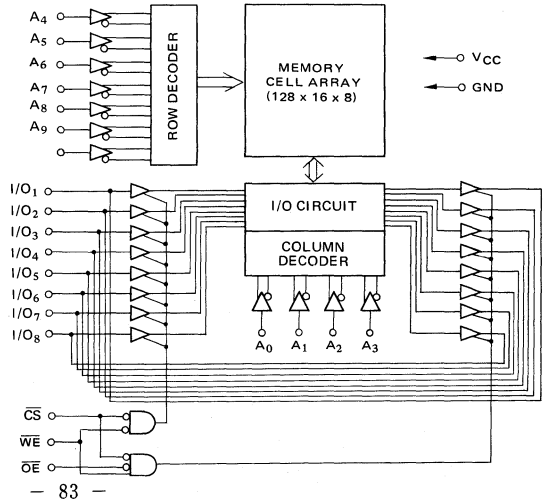
PIN CONNECTION



PIN NAMES

SYMBOL	NAME
$A_0 \sim A_3$	Column Address Inputs
$A_4 \sim A_{10}$	Row Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input/Output Voltage	−0.5 ~ 7.0	V
$T_{opr.}$	Operating Temperature	0 ~ 70	°C
$T_{stg.}$	Storage Temperature	−55 ~ 150	°C
T_{solder}	Soldering Temperature • Time	260 • 10	°C • sec
P_D	Power Dissipation (Ta = 70°C)	0.7	W

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	–	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5	–	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

D.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0V ~ 5.5V	−10	–	10	μA
V_{OH}	Output High Voltage	I_{OUT} = −1.0mA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA	–	–	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0V ~ 5.5V	−10	–	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS}$ = V_{CC}, I_{OUT} = 0mA	–	–	30	mA
I_{SB}	Standby Current	$\overline{CS}$ = V_{IH}, I_{OUT} = 0mA	–	–	7	mA
I_{CC1}	Operating Current TMM2015AP-10/-12/-15	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA	–	–	65	mA
I_{CC2}	Operating Current TMM2015AP-90	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA	–	–	80	mA

CAPACITANCE* (Ta = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = A.C. Ground	5	pF
C_{OUT}	Output Capacitance	V_{IN} = A.C. Ground	10	pF

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TMM2015AP-90		TMM2015AP-10		TMM2015AP-12		TMM2015AP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	90	–	100	–	120	–	150	–	ns
t_{ACC}	Address Access Time	–	90	–	100	–	120	–	150	ns
t_{CO}	Chip Select Access Time	–	90	–	100	–	120	–	150	ns
t_{OE}	Output Enable Time	–	35	–	35	–	50	–	55	ns
t_{OH}	Output Data Hold Time from Address Change	10	–	10	–	10	–	10	–	ns
t_{CLZ}	Output in Low-Z from $\overline{CS}$	10	–	10	–	10	–	10	–	ns
t_{CHZ}	Output in High-Z from $\overline{CS}$	–	40	–	40	–	40	–	55	ns
t_{OLZ}	Output in Low-Z from $\overline{OE}$	5	–	5	–	5	–	5	–	ns
t_{OHZ}	Output in High-Z from $\overline{OE}$	–	35	–	35	–	35	–	50	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselection to Power Down Time	–	50	–	50	–	60	–	60	ns

WRITE CYCLE

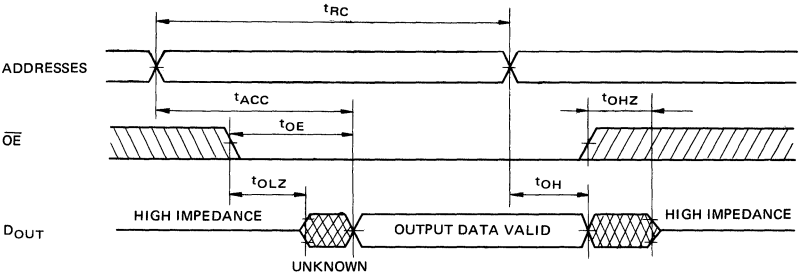
SYMBOL	PARAMETER	TMM2015AP-90		TMM2015AP-10		TMM2015AP-12		TMM2015AP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	90	–	100	–	120	–	150	–	ns
t_{CW}	Chip Selection to End of Write	70	–	80	–	100	–	120	–	ns
t_{AS}	Address Set up Time	20	–	20	–	20	–	20	–	ns
t_{WP}	Write Pulse Width	60	–	70	–	85	–	100	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{DS}	Data Set up Time	35	–	40	–	50	–	60	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns
t_{WLZ}	Output in Low-Z from $\overline{WE}$	5	–	5	–	5	–	5	–	ns
t_{WHZ}	Output in High-Z from $\overline{WE}$	–	25	–	30	–	35	–	50	ns

A.C. TEST CONDITIONS

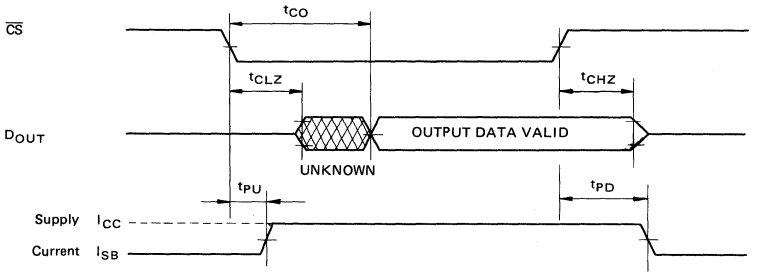
Input Pulse Levels	$0 \sim 3.5V$
Input Rise and Fall Time	10 ns
Input and Output Reference Levels	1.5V
Output Load	1 TTL Gate & $C_L = 100pF$

TIMING WAVEFORMS

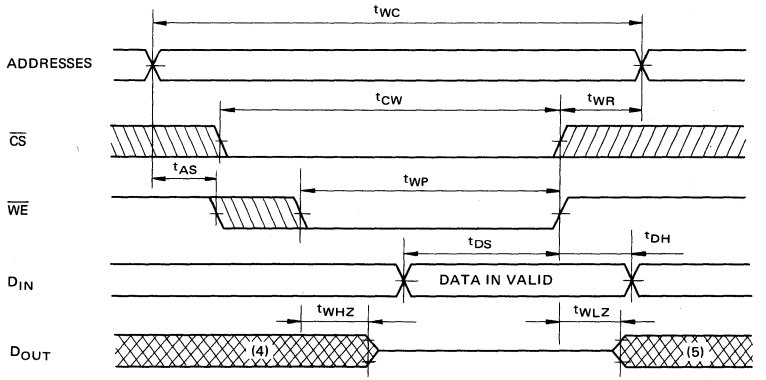
(A) READ CYCLE [1] (1)



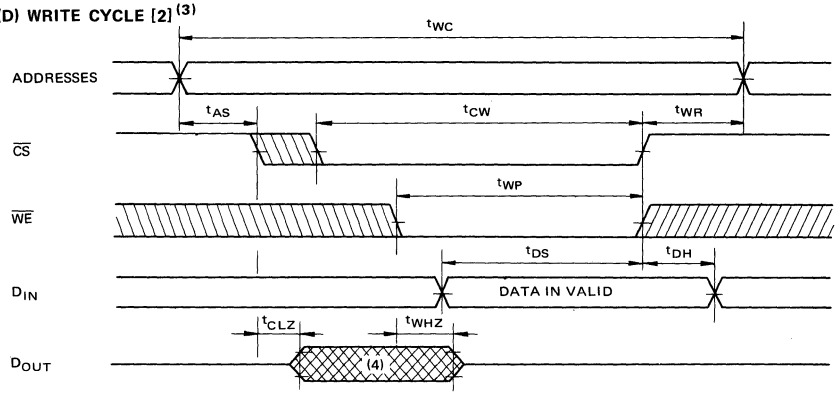
(B) READ CYCLE [2] (1) (2)



(C) WRITE CYCLE [1] (3)



(D) WRITE CYCLE [2] (3)



Note: (1) The $\overline{WE}$ is high for read cycle.
Device is continuously selected, $\overline{CS} = V_{IL}$ in read cycle [1].

(2) All addresses are valid prior to or simultaneously with $\overline{CS}$ transitions.

(3) A write occurs during the overlap of low $\overline{CS}$ and low $\overline{WE}$.
The t_{CW} is specified as the time from the chip selection to end of write in write cycle, and the t_{WP} is specified as the overlap time of low $\overline{CS}$ and low $\overline{WE}$.
$\overline{OE}$ is allowed to be low or high level in write cycle.
If the $\overline{OE}$ is high, the output buffers remain in a high impedance state in this period.

(4) If the $\overline{CS}$ low transition occurs simultaneously with or latter to the $\overline{WE}$ low transition, the output buffers remain in a high impedance state in this period.

(5) If the $\overline{CS}$ high transition occurs simultaneously with $\overline{WE}$ high transition, the output buffers remain in a high impedance state in this period.

These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) t_{CLZ}, t_{OLZ}, t_{WLZ} ..... Output Enable Time
(B) t_{CHZ}, t_{OHZ}, t_{WHZ} ..... Output Disable Time

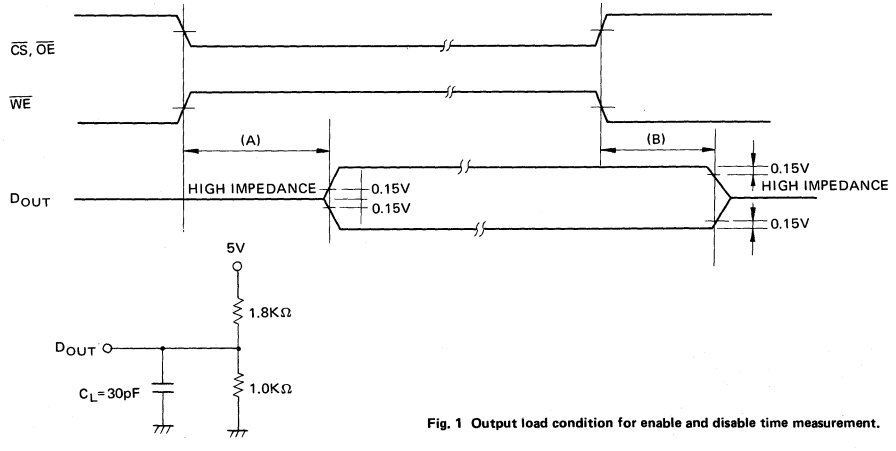
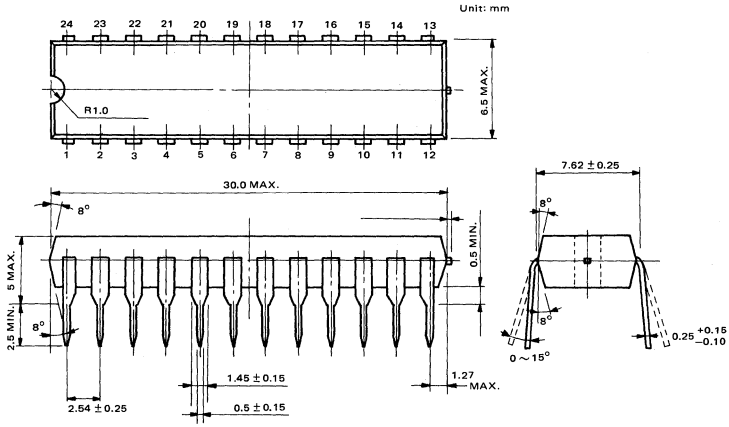


Fig. 1 Output load condition for enable and disable time measurement.

OUTLINE DRAWINGS



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 24 leads.

TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD x 8 BIT STATIC RAM

N-CHANNEL SILICON GATE MOS PROCESS

TMM2018D-45
TMM2018D-55

DESCRIPTION

The TMM2018D is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 45ns/55ns and maximum operating current of 150mA. When $\overline{CS}$ goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA.

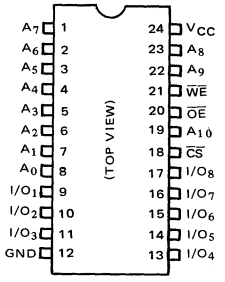
Thus the TMM2018D is most suitable for use in cache memory and high speed storage. The TMM-2018D is offered in 24 pin standard cerdip package with 0.3 inch width for high density assembly.

The TMM2018D is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

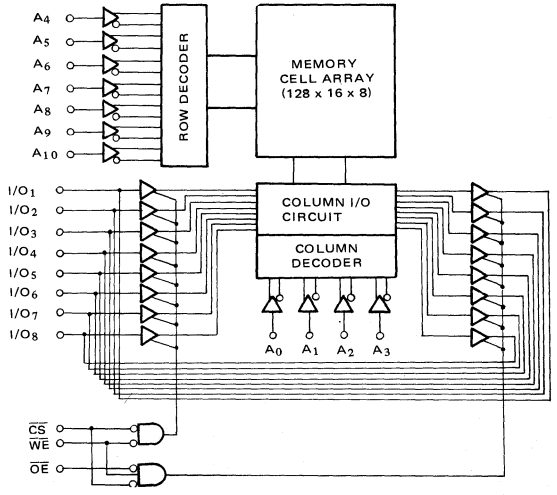
FEATURES

- Fast access time
  t_{ACC} = 45 ns : TMM2018D-45
  t_{ACC} = 55 ns : TMM2018D-55
- Low power dissipation
  I_{CC} = 150mA
  I_{SB} = 20mA
- Single 5V power supply
- Fully static operation
- All inputs and outputs
  Directly TTL compatible
- Power down feature: $\overline{CS}$ = V_{IH}
- Output buffer control: $\overline{OE}$
- Three state outputs
- Inputs protected: All inputs have protection against static charge.
- Package: 24 pin standard cerdip package, 0.3 inch width

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{10}$	Address Inputs
$I/O_1 \sim I/O_8$	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enalbe Input
V_{CC}	Power (+5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−3.5 ~ 7.0	V
V_{IN}	Input Voltage	−3.5 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	−3.5 ~ 7.0	V
T_{opr}	Operating Temperature	0 ~ 70	°C
T_{strg}	Storage Temperature	−55 ~ 150	°C
T_{solder}	Soldering Temperature · Time	260 · 10	°C · sec
P_D	Power Dissipation	0.9	W
I_{OUT}	D.C. Output Current	20	mA

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	–	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage	−3.0	–	0.8	V
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V

D.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ±5%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Current	V_{IN} = 0 ~ V_{CC}	–	±10	μA
V_{OH}	Output High Voltage	I_{OH} = −4.0mA	2.4	–	V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA	–	0.4	V
I_{LO}	Output Leakage Current	V_{OUT} = 0 ~ V_{CC} $\overline{CS}$ = V_{IH}	–	±50	μA
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}	–	150	mA
I_{SB}	Standby Current	$\overline{CS}$ = V_{IH}	–	20	mA
I_{SBP}	Peak Power-on Current	$\overline{CS}$ = V_{CC}, V_{CC} = 0 ~ 5.5V	–	40	mA

CAPACITANCE* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = OV	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = OV	10	

*Note: This parameter is periodically sampled and is not 100% tested.;

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ±5%)

Read Cycle

SYMBOL	PARAMETER	TMM2018D-45		TMM2018D-55		UNIT
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	45		55		ns
t_{ACC}	Address Access Time		45		55	
t_{CO}	Chip Select Access Time		45		55	
t_{OE}	Output Enable to Output Valid		20		25	
t_{CLZ}	Chip Selection to Output in Low-Z	5		5		
t_{CHZ}	Chip Deselection to Output in High-Z	0	20	0	20	
t_{OLZ}	Output Enable to Output in Low-Z	0		0		
t_{OHZ}	Output Disable to Output in High-Z	0	15	0	20	
t_{OH}	Output Data Hold Time	5		5		
t_{PU}	Chip selection to Power Up Time	0		0		
t_{PD}	Chip Deselection to Power Down Time		30		30	

Write Cycle

SYMBOL	PARAMETER	TMM2018D-45		TMM2018D-55		UNIT
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	45		55		ns
t_{CW}	Chip Selection to End of Write	40		50		
t_{AS}	Address Set up Time	0		0		
t_{WP}	Write Pulse Width	35		40		
t_{WR}	Write Recovery Time	0		0		
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	0		0		
t_{WHZ}	$\overline{WE}$ to Output in High-Z	0	15	0	20	
t_{DS}	Data Set up Time	20		20		
t_{DH}	Data Hold Time	0		0		

A.C. TEST CONDITIONS

Input Pulse Levels	0 ~ 3.5V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

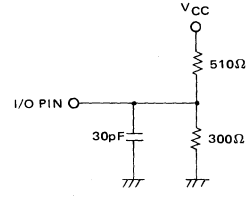
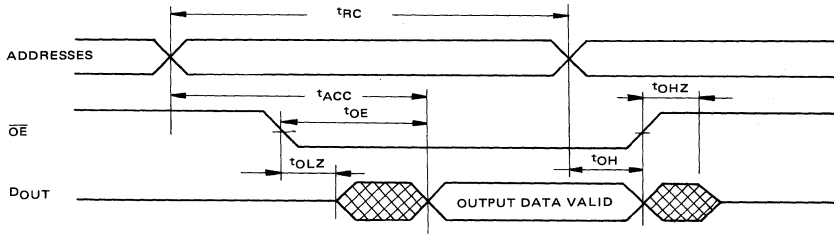


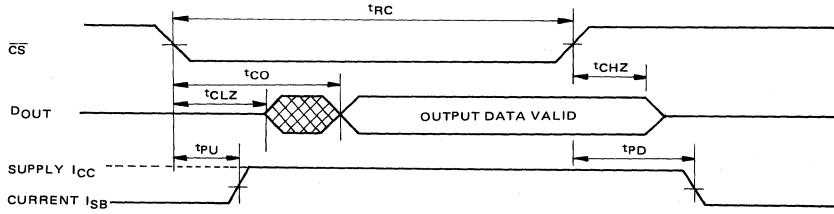
Fig. 1 Output Load

TIMING WAVEFORMS

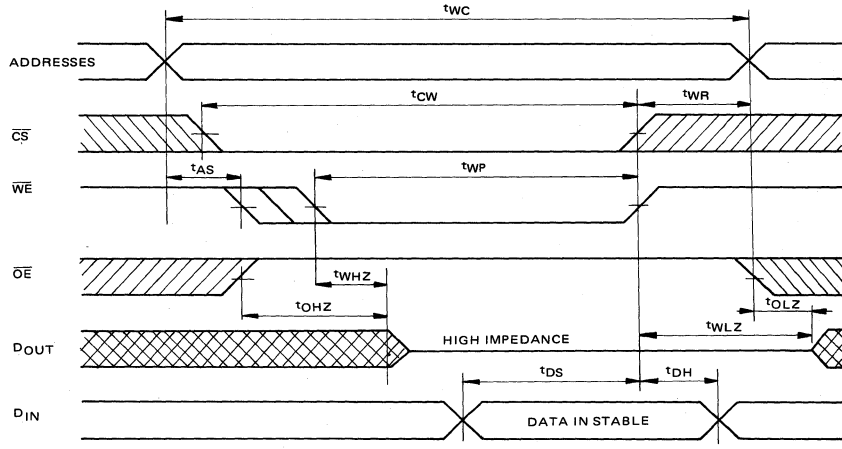
Read Cycle 1. ($\overline{WE}$ = V_{IH}, $\overline{CS}$ = V_{IL})



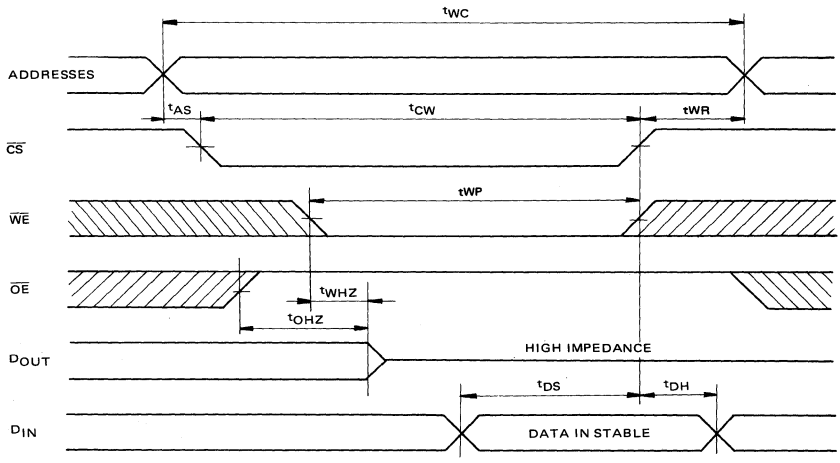
Read Cycle 2. ($\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL})



Write Cycle 1.



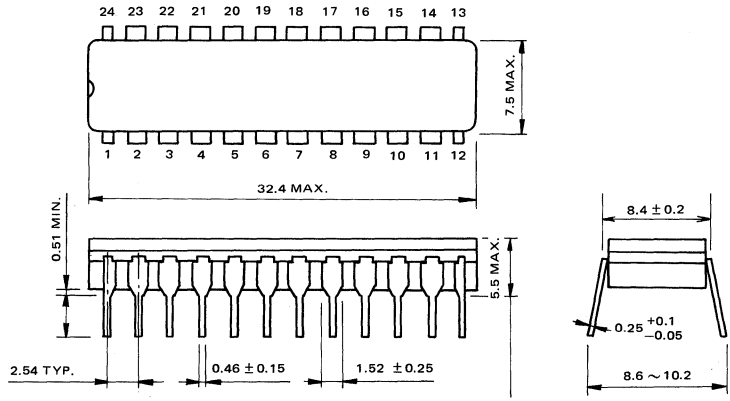
Write Cycle 2.



Note:
1. In read cycle 2, all addresses are valid prior to or coincident with $\overline{CS}$ transition low.
2. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
3. During the period of selected state ($\overline{CS}$ = V_{IL}), all address inputs must not be in a high impedance state.

OUTLINE DRAWINGS

Unit in mm

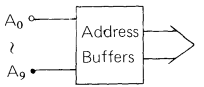
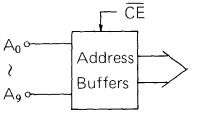


Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No. 1 and No. 24 leads.

CMOS Static Random Access Memories

4 KBit CMOS STATIC RAM COMPARISON TABLE

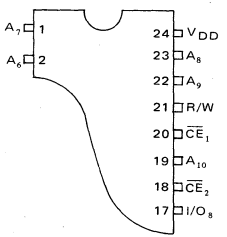
1K x 4 CMOS STATIC RAM

	Device Number	TC5514AP					TC5513AP				
	Pin Name / Mode	$\overline{CE}$	R/W	Addresses	$I/O_{1\sim4}$	Power	$\overline{CE}$	R/W	Addresses	$I/O_{1\sim4}$	Power
OPERATION MODE	WRITE	L	L	Valid	D_{IN}	I_{DDO}	L	L	Valid	D_{IN}	I_{DDO}
	READ	L	H	Valid	D_{OUT}	I_{DDO}	L	H	Valid	D_{OUT}	I_{DDO}
	STANDBY	H	*	Fixed 'H' or 'L'	High-Z	I_{DDS}	H	*	*	High-Z	I_{DDS}
		H	*	Transition	High-Z	I_{DDO}					
Difference in control function		All address input circuits are not controlled by $\overline{CE}$.  Once address transition occur, the device is activated independent of $\overline{CE}$ input levels.					All address input circuits are controlled by $\overline{CE}$.  Only when address transition occur under the condition of $\overline{CE}$ = L, the device is activated.				
Difference in access time from address and chip enable		Address Access time				200 ns	Address Access time				200 ns
		Chip Enable Access time				70 ns	Chip Enable Access time				200 ns

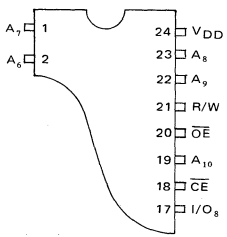
16KBit CMOS STATIC RAM COMPARISON TABLE

PIN CONFIGURATION

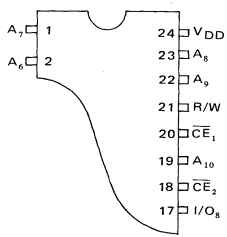
TC5516AP



TC5517AP
TC5517BP



TC5518BP



OPERATION MODE

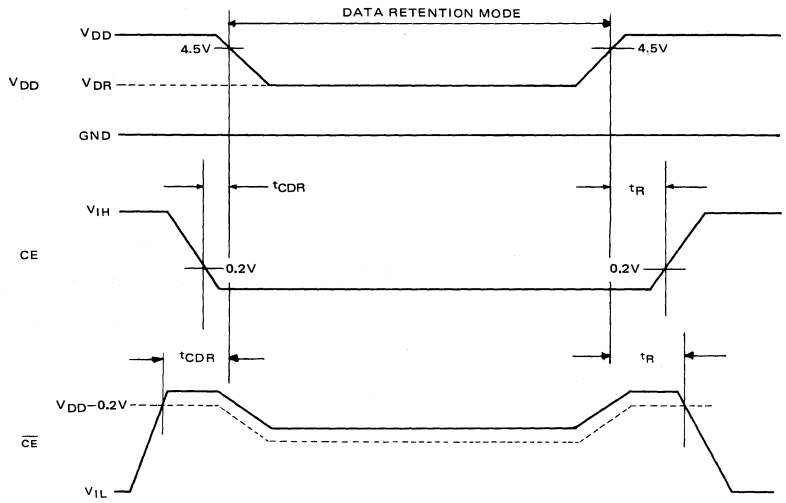
Device Number	TC5516AP						TC5517AP TC5517BP						TC5518BP					
Pin No. / Mode / Name	18	20	21	1~8, 22 23, 19	9~11 13~17	Power	18	20	21	1~8, 22 23, 19	9~11 13~17	Power	18	20	21	1~8, 22 23, 19	9~11 13~17	Power
	$\overline{CE}_2$	$\overline{CE}_1$	R/W	A_0~A_{10}	$I/O_{1\sim8}$		$\overline{CE}$	$\overline{OE}$	R/W	A_0~A_{10}	$I/O_{1\sim8}$		$\overline{CE}_2$	$\overline{CE}_1$	R/W	A_0~A_{10}	$I/O_{1\sim8}$	
WRITE	L	L	L	Valid	D_{IN}	I_{DDO}	L	*	L	Valid	D_{IN}	I_{DDO}	L	L	L	Valid	D_{IN}	I_{DDO}
READ	L	L	H	Valid	D_{OUT}	I_{DDO}	L	L	H	Valid	D_{OUT}	I_{DDO}	L	L	H	Valid	D_{OUT}	I_{DDO}
STANDBY 1	L	H	*	*	High-Z	I_{DDO}							*	H	*	*	High-Z	I_{DDS}
STANDBY 2	H	*	*	*	High-Z	I_{DDS}	H	*	*	*	High-Z	I_{DDS}	H	*	*	*	High-Z	I_{DDS}
OUTPUT DESELECT							L	H	*	*	High-Z	I_{DDO}						

DATA RETENTION CHARACTERISTICS (Ta = -30 ~ 85°)

SYMBOL	PARAMETER	CONDITIONS	Min.	Max.	UNIT
V_{DR}	Data Retention Voltage	$0V \leqq CE \leqq 0.2V$ or $V_{DD}-0.2V \leqq CE \leqq V_{DD}$ *(3)	2.0	5.5	V
I_{DDS}	Data Retention Current		–	Note (1)	μA
t_{CDR}	Chip Deselection to Data Retention Time		0	–	μS
t_R	Recovery Time		t_{RC} Note(2)	–	μS

Note (1) : Refer to I_{DDS} specification in individual data sheet.
(2) : Read cycle time.

TIMING CHART



Note (3) : For 16K Bit CMOS RAM, $V_{DD}-0.5V \leqq \overline{CE} \leqq V_{DD}$
Details are specified in TC5516/17/18 data sheets.

256 WORD x 4 BIT CMOS RAM

TC5501P/-1
TC5501D/-1

DESCRIPTION

The TC5501P/D is a fully static read write memory organized as 256 words by 4 bits using CMOS technology. Because of ultra low power dissipation, the TC5501P/D can be used as battery operated portable memory system and also as a nonvolatile memory with battery back up. The TC5501P/D operates from a single 5V power supply with a static operation, so that the no refresh periods are required. This simplifies the power supply circuit design.

The three state outputs simplify the memory expansion making the TC5501P/D suitable for use in a microprocessor peripheral memory. Since the minimum data retention voltage is 2V, the battery back up system needs only simple circuit. By using Toshiba's original C²MOS technology, the device circuitry is not only simplified but wide operating margin and noise margin are also realized.

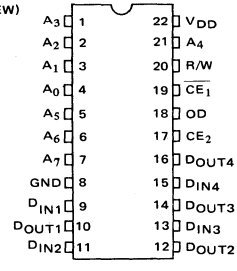
The TC5501P/D is offered in standard 22 pin plastic and cerdip packages, 0.4 inch in width.

FEATURES

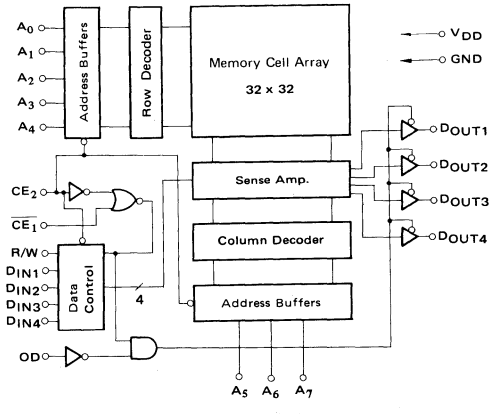
- Low Power Dissipation
  - 55μW (MAX.) STANDBY
  - 83mW (MAX.) OPERATING
- Single 5V Power Supply
- Data Retention Voltage 2V to 5.5V
- Package
  - Plastic DIP : TC5501P
  - Cerdip DIP : TC5501D
- Fully static operation
- Three State Output
- Input/output, TTL Compatible
- Access Time
  TC5501P/D ; $t_{ACC} \leqq 450$ns (MAX.)
  TC5501P-1/D-1; $t_{ACC} \leqq 650$ns (MAX.)

PIN CONNECTION

(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_7$	Address Inputs
R/W	Read Write Input
$\overline{CE_1}$, CE_2	Chip Enable Inputs
$D_{IN1 \sim 4}$	Data Inputs
$D_{OUT1 \sim 4}$	Data Outputs
OD	Output Disable Input
V_{DD}/GND	Power Supply Terminals

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3 ~ V_{DD} + 0.3	V
V_{OUT}	Output Voltage	0 ~ V_{DD}	V
P_D	Power Dissipation (Ta = 85°C)	800	mW
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{OPR}	Operating Temperature	−30 ~ 85	°C

DC RECOMMENDED OPERATING CONDITION

SYMBOL	PARAMETER	MIN	TYP.	MAX.	UNITS
V_{DD}	Power Supply Voltage	4.5	–	5.5	V
V_{IH}	Input High Level Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Level Voltage	−0.3	–	0.65	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

DC CHARACTERISTICS (Ta = −30 ~ 85°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP(1)	MAX.	UNITS
I_{IN}	Input Current	$0 \leqq V_{IN} \leqq V_{DD}$	–	±0.05	±1.0	μA
I_{DDS}	Standby Current	V_{DD} = 2.0V to 5.5V CE_2 = 0.2V, Output open	–	0.2	10	μA
I_{DDO}	Operating Current	V_{DD} = 5.5V, t_{CYC} = 1μs	–	6.2	15	mA
I_{LO}	Output Leakage Current	$0 \leqq V_{OUT} \leqq V_{DD}$	–	±0.05	±1.0	μA
I_{OH}	Output High Current	V_{DD} = 4.5V, V_{OH} = 2.4V	−1.0	−2.0	–	mA
I_{OL}	Output Low Current	V_{DD} = 4.5V, V_{OL} = 0.4V	2.0	3.0	–	mA

Note (1) Ta = 25°C V_{DD} = 5V

CAPACITANCE (2) (Ta = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1MHz	–	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1MHz	–	7	15	pF

Note (2) This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS

- **READ CYCLE**

SYMBOL	PARAMETER	TC5501P/D		TC5501P-1/D-1		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	450	–	650	–	ns
t_{ACC}	Address Access Time	–	450	–	650	ns
t_{ACC1}	$\overline{CE}_1$ Access Time	–	400	–	600	ns
t_{ACC2}	CE_2 Access Time	–	500	–	700	ns
t_{ODO}	OD Access Time	–	250	–	350	ns
t_{COE}	Output Enable Time	0	–	0	–	ns
t_{DIS}	Output Disable Time	0	130	0	150	ns
t_{OH}	Output Data Hold Time	0	–	0	–	ns

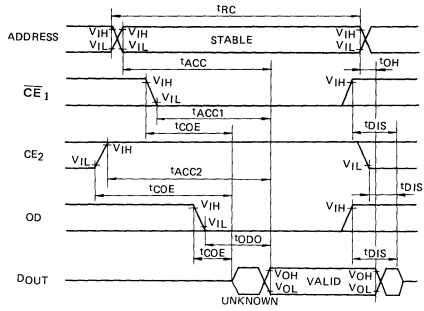
- **WRITE CYCLE**

SYMBOL	PARAMETER	TC5501P/D		TC5501P-1/D-1		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	450	–	650	–	ns
t_{AW}	Address Setup Time	130	–	150	–	ns
t_{CW}	CE_2 Setup Time	130	–	150	–	ns
t_{WP}	Write Pulse Width	250	–	400	–	ns
t_{DS}	Data Setup Time	250	–	400	–	ns
t_{DH}	Data Hold Time	50	–	100	–	ns
t_{WR}	Write Recovery Time	50	–	50	–	ns

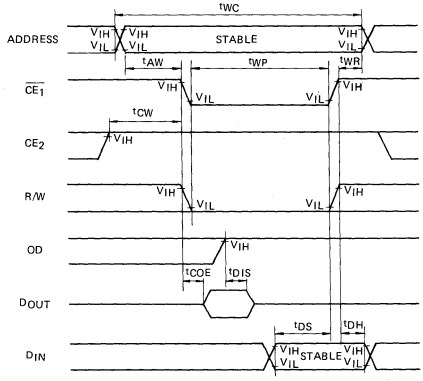
A.C. TEST CONDITIONS

- Output Load : 100 pF + 1 TTL Gate
- Input Pulse Levels : 0.45V, 2.4V
- Timing Measurement Reference Levels
  - Input : 0.65V, 2.2V
  - Output : 0.65V, 2.2V
- Input Pulse Rise and Fall Times : 10ns

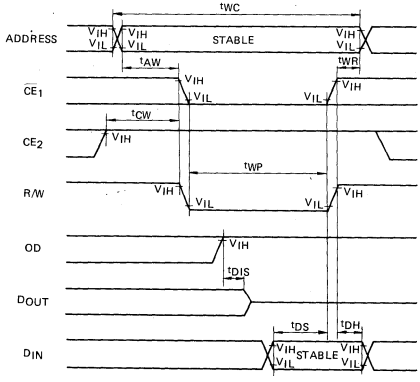
Read Cycle



Write Cycle 1

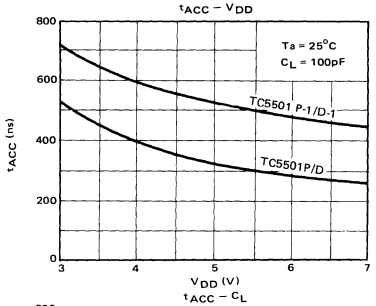


Write Cycle 2

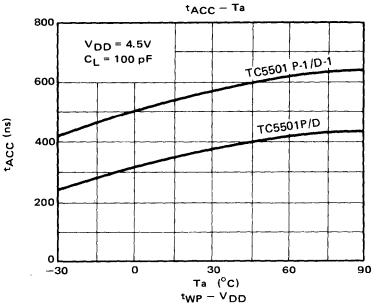


TYPICAL CHARACTERISTICS

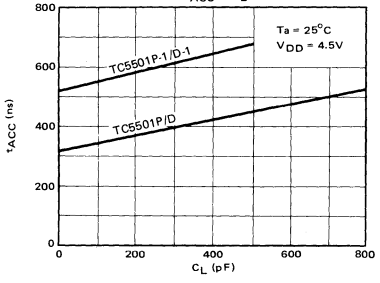
t_{ACC} – V_{DD}



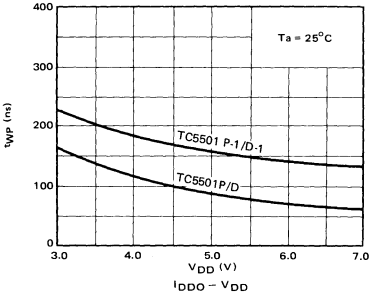
t_{ACC} – Ta



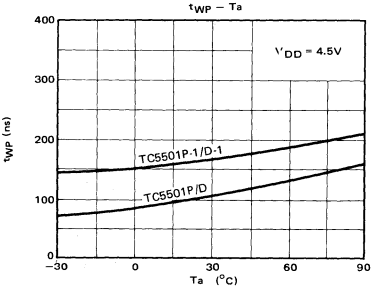
t_{ACC} – C_L



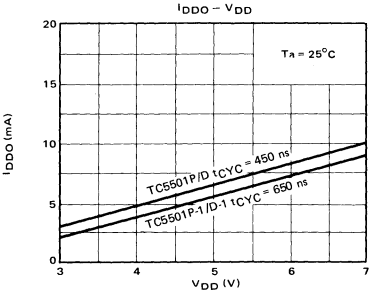
t_{WP} – V_{DD}



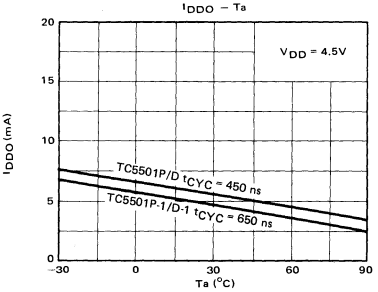
t_{WP} – Ta



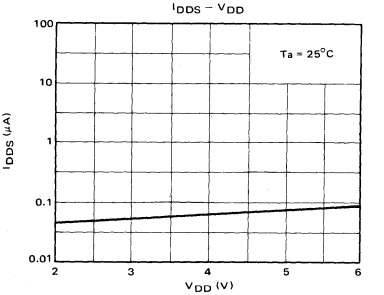
I_{DDO} – V_{DD}



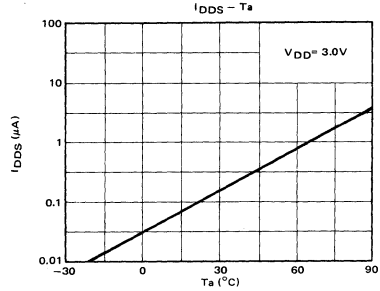
I_{DDO} – Ta



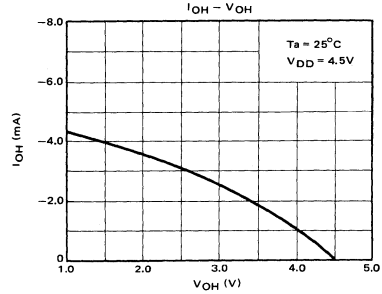
I_{DDS} – V_{DD}



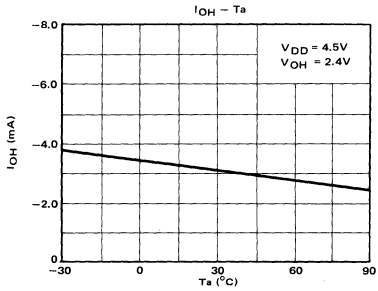
I_{DDS} – Ta



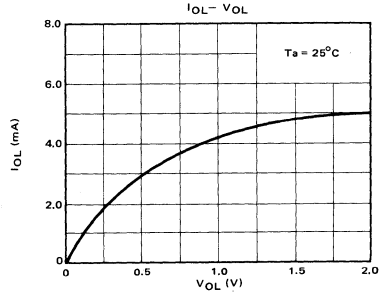
I_{OH} – V_{OH}



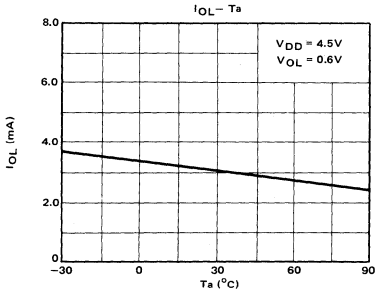
I_{OH} – Ta



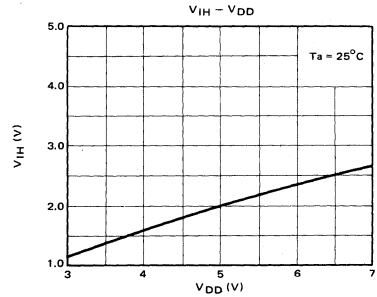
I_{OL} – V_{OL}



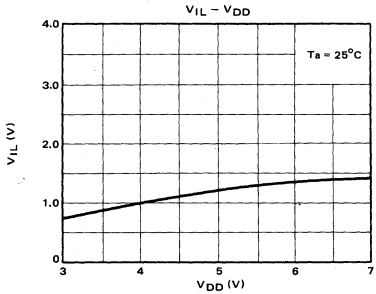
I_{OL} – Ta



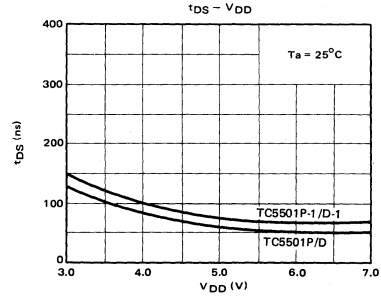
V_{IH} – V_{DD}



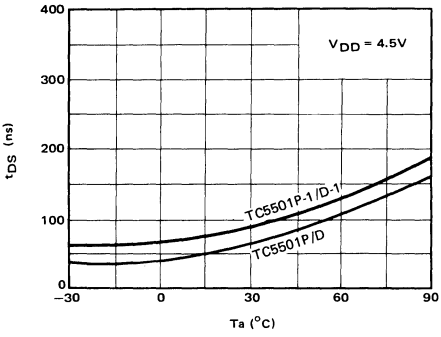
V_{IL} – V_{DD}



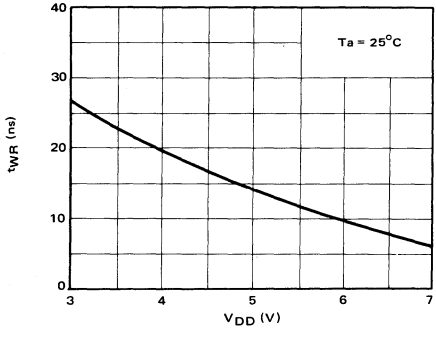
t_{DS} – V_{DD}



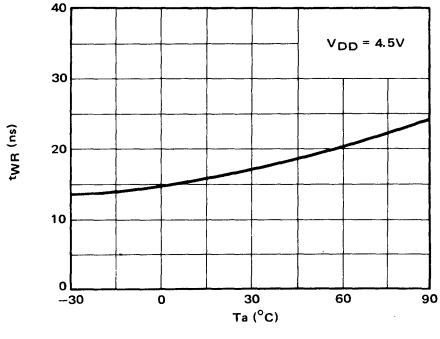
t_{DS} – Ta



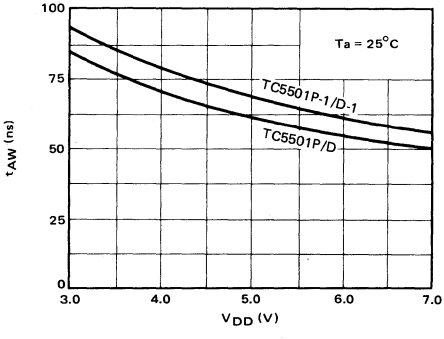
t_{WR} – V_{DD}



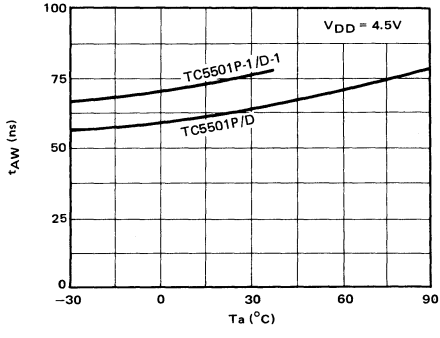
t_{WR} – Ta



t_{AW} – V_{DD}



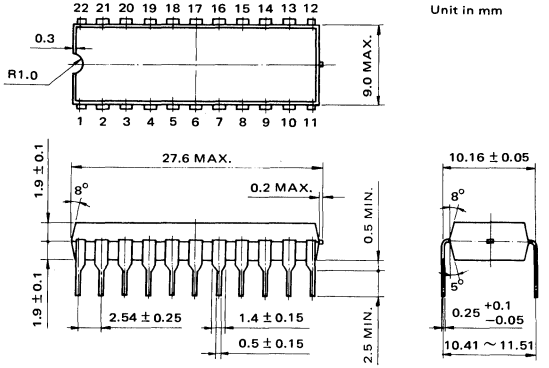
t_{AW} – Ta



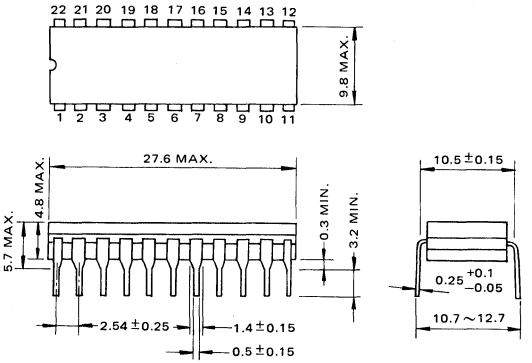
OUTLINE DRAWINGS

PLASTIC PACKAGE

Unit in mm



CERDIP PACKAGE



Notes: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 22 leads.

TOSHIBA MOS MEMORY PRODUCTS

1024 WORD X 4BIT CMOS RAM

SILICON GATE CMOS

TC5047AP-1
TC5047AP-2

DESCRIPTION

The TC5047AP is a static read write memory organized as 1024 words by 4 bits using CMOS technology. Because of ultra low power dissipation, the TC5047AP can be used as battery operated portable memory system and also as a nonvolatile memory with battery back up. The TC5047AP operates from a single 5V power supply with a static operation, so that the no refresh periods are required. This simplifies the power supply circuit design.

The three state outputs simplify the memory expansion making the TC5047AP suitable for use in a microprocessor peripheral memory. Since the minimum data retention voltage is 2V, the battery back up system needs only simple circuit. By using Toshiba's original C^2MOS technology, the device circuitry is not only simplified but wide operating margin and noise margin are also realized.

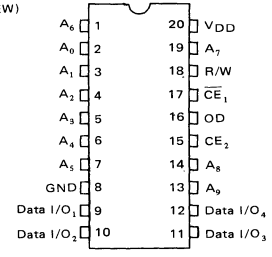
The TC5047AP family is moulded in a dual-in-line 20 pin plastic package, 0.4 inch in width.

FEATURES

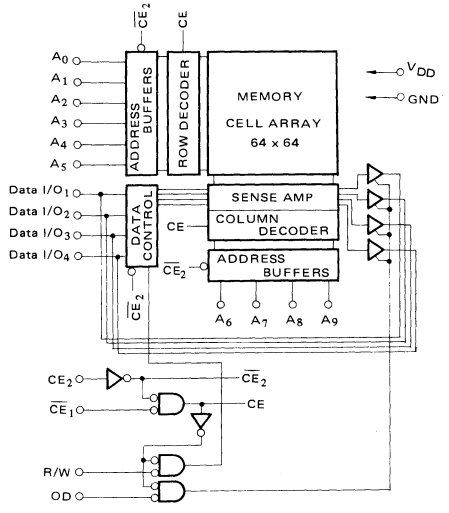
- Low Power Dissipation
  110 μW (MAX.) STANDBY
  110mW (MAX.) OPERATING
- Single 5V Power Supply
- Data Retention Voltage; 2.0~5.5V
- 20 PIN Plastic Package
- Static Operation
- Three State Outputs
- Input/Output; TTL Compatible
- Access Time
  TC5047AP-1; $t_{ACC} \leqq 550$ns (MAX.)
  TC5047AP-2; $t_{ACC} \leqq 800$ns (MAX.)

PIN CONNECTION

(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_9$	Address Inputs
R/W	Read Write Input
$\overline{CE}_1$, CE_2	Chip Enable inputs
Data $I/O_{1\sim4}$	Data Input/Output
OD	Output Disable Input
V_{DD}/GND	Power Supply Terminals

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	$-0.3 \sim 7.0$	V
V_{IN}	Input Voltage	$-0.3 \sim V_{DD} + 0.3$	V
V_{OUT}	Output Voltage	$0 \sim V_{DD}$	V
P_D	Power Dissipation (Ta = 85°C)	700	mW
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{STG}	Storage Temperature	$-55 \sim 150$	°C
T_{OPR}	Operating Temperature	$-30 \sim 85$	°C

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Level Voltage	$V_{DD}-1.5$	–	$V_{DD}+0.3$	V
V_{IL}	Input Low Level Voltage	−0.3	–	0.6	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

DC CHARACTERISTICS (Ta = −30 ~ 85° C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP. (1)	MAX.	UNIT
I_{IN}	Input Current	$0V \leqq V_{IN} \leqq V_{DD}$	0	±0.05	±1.0	μA
I_{DDS}	Standby Current	V_{DD} = 2 ~ 5.5V CE_2 = 0.2V, Output Open	0	0.2	20	μA
I_{DDO}	Operating Current	V_{DD}=5.5V, t_{CYC}=1μs	0	10	20	mA
I_{LO}	Output Leakage Current	$0V \leqq V_{OUT} \leqq V_{DD}$	0	±0.1	±5.0	μA
I_{OH}	Output High Current	V_{DD}=4.5V, V_{OH} = 2.4V	−1.0	−2.0	–	mA
I_{OL}	Output Low Current	V_{DD} = 4.5V, V_{OL} = 0.4V	1.6	2.0	–	mA
C_i (2)	Input Capacitance	f = 1MHz	–	5	10	pF
C_O (2)	Output Capacitance	f = 1MHz	–	7	15	pF

Note (1) Ta = 25° C, V_{DD} = 5V
Note (2) This parameter is periodically sampled and is not 100% tested.

A.C. RECOMMENDED OPERATING CONDITIONS

- **TC5047AP-1**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_{RC}	Read Cycle Time	V_{DD} = 4.5 ~ 5.5V C_L = 100 pF V_{IH} = V_{DD} − 1.5V ~ V_{DD} + 0.3V V_{IL} = −0.3 ~ 0.6V Ta = −30 ~ 85°C	650	–	ns
t_{WC}	Write Cycle Time		650	–	ns
t_{CES}	CE Setup Time		20(3)	–	ns
t_{CEH}	CE Hold Time		20(3)	–	ns
t_{PC}	Precharge Time		100	–	ns
$t_{\overline{CE}}$	$\overline{CE}$ Pulse Width		550	–	ns
t_{WP}	Write Pulse Width		300	–	ns
t_{DS}	Data Setup Time		300	–	ns
t_{DH}	Data Hold Time		0	–	ns
t_{CW}	Write Setup Time		350	–	ns
t_{RS}	Read Setup Time		0	–	ns
t_{RH}	Read Hold Time		0	–	ns

Note (3) $t_{CES} + t_{CEH} \geqq 100$ ns

- **TC5047AP-2**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	V_{DD} = 4.5 ~ 5.5V C_L = 100 pF V_{IH} = V_{DD} − 1.5V ~ V_{DD} + 0.3V V_{IL} = −0.3 ~ 0.6V Ta = −30 ~ 85°C	1000	–	ns
t_{WC}	Write Cycle Time		1000	–	ns
t_{CES}	CE Setup Time		20(4)	–	ns
t_{CEH}	CE Hold Time		20(4)	–	ns
t_{PC}	Precharge Time		200	–	ns
$t_{\overline{CE}}$	$\overline{CE}$ Pulse Width		800	–	ns
t_{WP}	Write Pulse Width		500	–	ns
t_{DS}	Data Setup Time		500	–	ns
t_{DH}	Data Hold Time		0	–	ns
t_{CW}	Write Setup Time		550	–	ns
t_{RS}	Read Setup Time		0	–	ns
t_{RH}	Read Hold Time		0	–	ns

Note (4) $t_{CES} + t_{CEH} \geqq 200$ ns.

A.C. CHARACTERISTICS (Ta = −30~85°C)

- **TC5047AP-1**

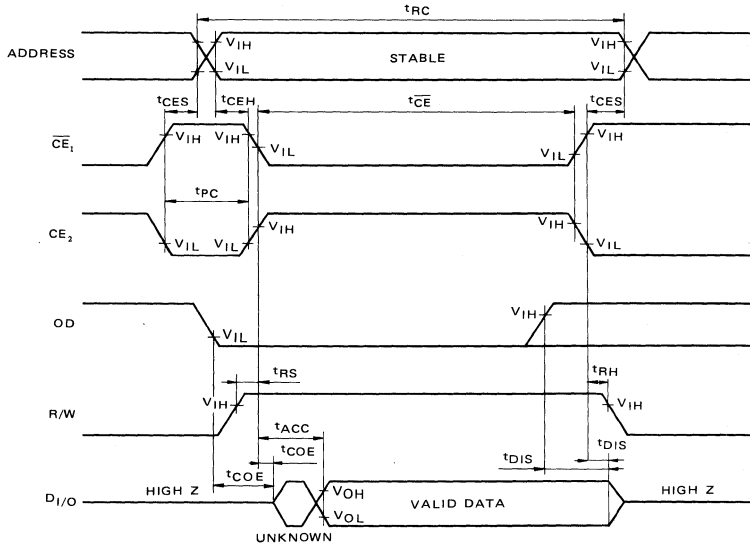
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{ACC}	Access Time	V_{DD} = 4.5 ~ 5.5V	–	–	550	ns
t_{DIS}	Output Disable Time	C_L = 100 pF	–	–	100	ns
t_{COE}	Output Enable Time	V_{OH} =2.4V, V_{OL}=0.6V	–	100	–	ns

- **TC5047AP-2**

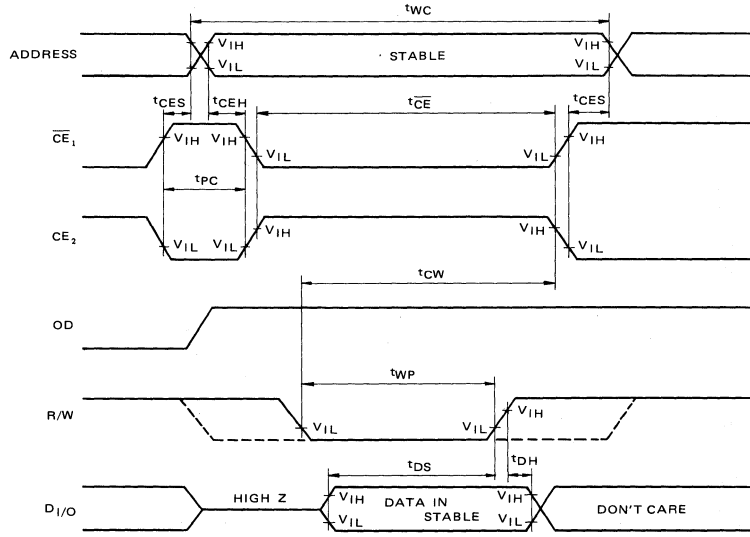
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{ACC}	Access Time	V_{DD} = 4.5 ~ 5.5V	–	–	800	ns
t_{DIS}	Output Disable Time	C_L = 100 pF	–	–	200	ns
t_{COE}	Output Enable Time	V_{OH} =2.4V, V_{OL} = 0.6V	–	200	–	ns

TIMING WAVEFORMS

- **Read Cycle**

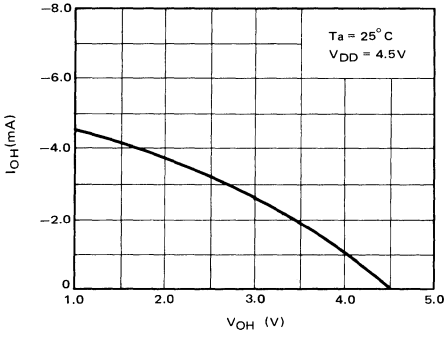


- **Write Cycle**

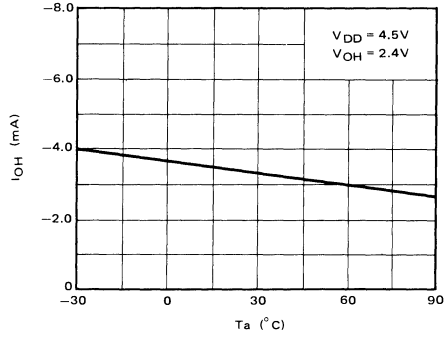


TYPICAL CHARACTERISTICS

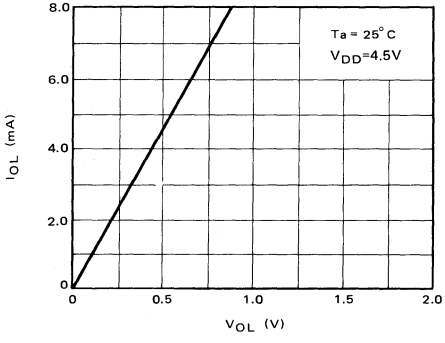
$V_{OH} - I_{OH}$



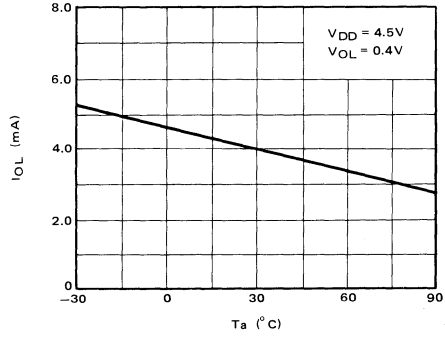
$I_{OH} - Ta$



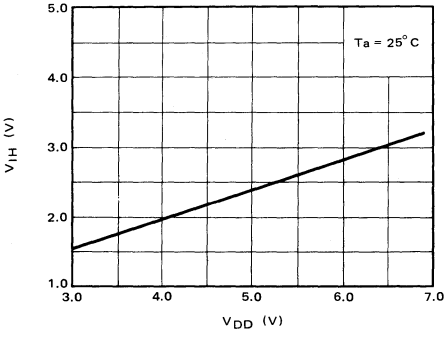
$I_{OL} - V_{OL}$



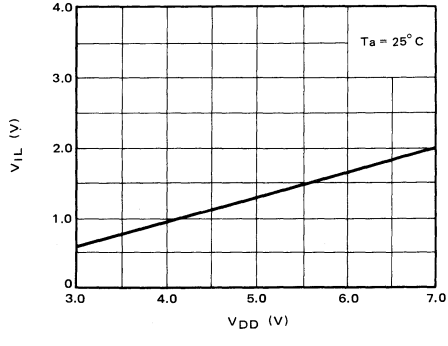
$I_{OL} - Ta$



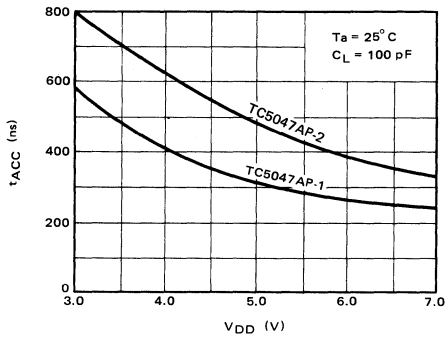
$V_{IH} - V_{DD}$



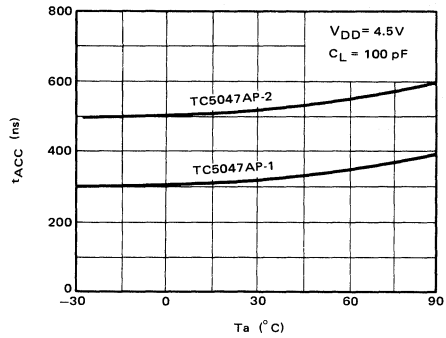
$V_{IL} - V_{DD}$



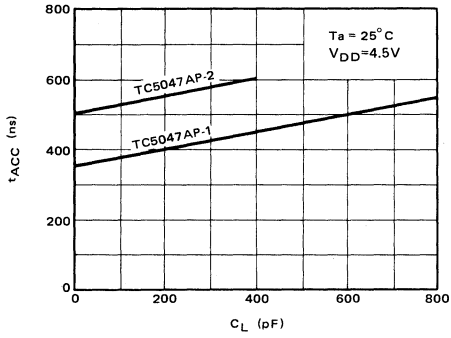
$t_{ACC} - V_{DD}$



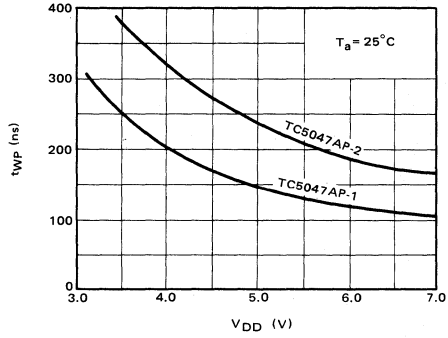
$t_{ACC} - T_a$



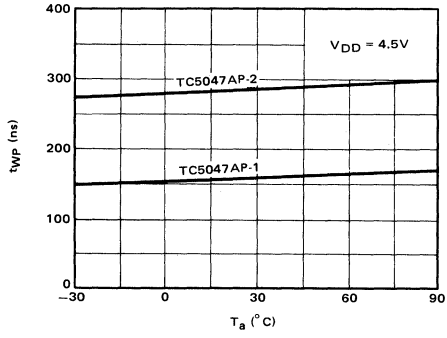
$t_{ACC} - C_L$



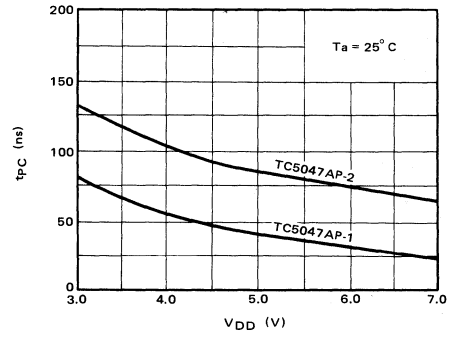
$t_{WP} - V_{DD}$



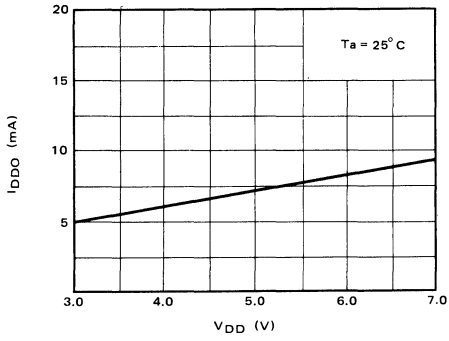
$t_{WP} - T_a$



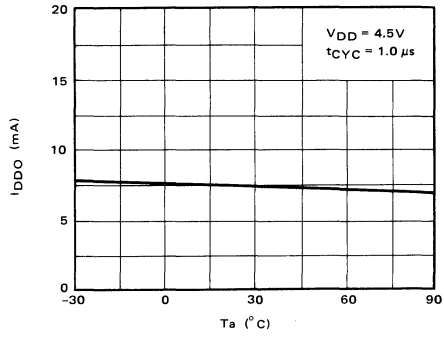
$t_{PC} - V_{DD}$



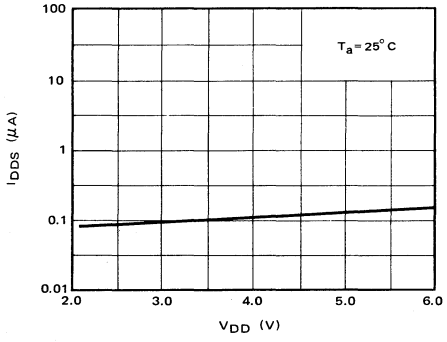
$I_{DDO} - V_{DD}$



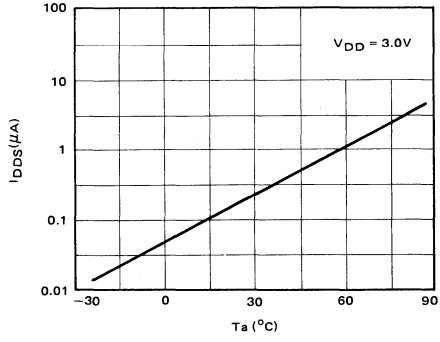
$I_{DDO} - T_a$



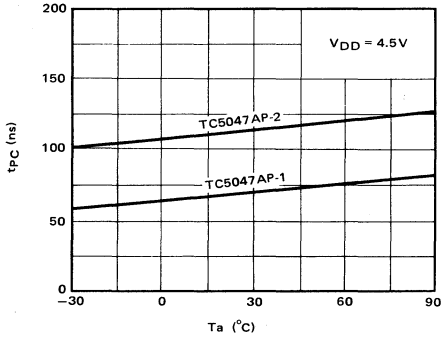
$I_{DDS} - V_{DD}$



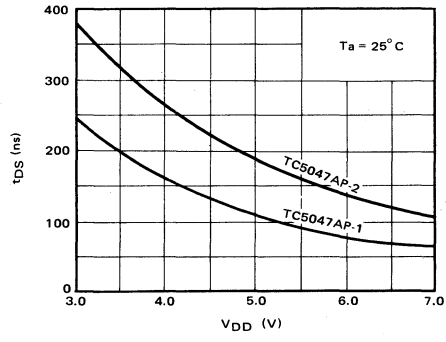
$I_{DDS} - T_a$

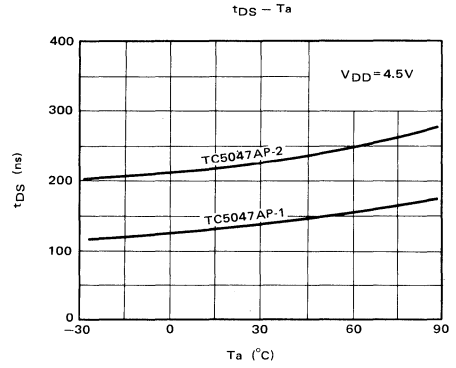


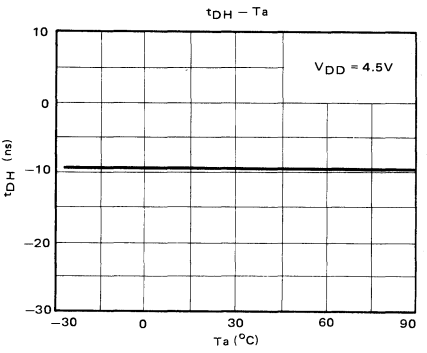
$t_{PC} - T_a$



$t_{DS} - V_{DD}$

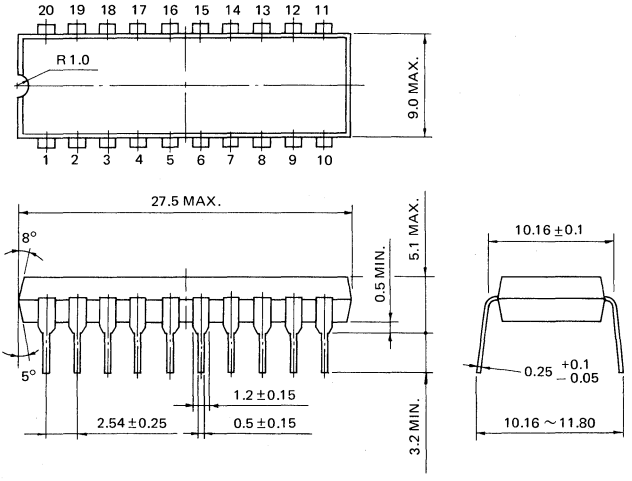






OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 20 leads.

Distributed by

4096 WORD x 1 BIT CMOS STATIC RAM

SILICON GATE CMOS

TC5504AP-2/-3, TC5504APL-2/-3
TC5504AD-2/-3, TC5504ADL-2/-3

DESCRIPTION

The TC5504AP/AD is a 4,096 bit high speed and low power static random access memory organized as 4,096 words by 1 bit using CMOS technology, and operates from a single 5-volt supply.

On chip latches are provided for addresses, data input and output, and read write control allowing efficient interfacing with microprocessor systems.

The TC5504AP/AD is a fully CMOS RAM, therefore it is suited for use in low power applications where battery operation and battery back up for non-volatility are required. Furthermore the TC5504APL/ADL guaranteed a standby current equal to or less than 1μA at 60°C ambient temperature.

The TC5504AP/AD is guaranteed for data retention at a power supply as low as 2 volts. The TC5504AP/AD is directly TTL compatible in all inputs and output.

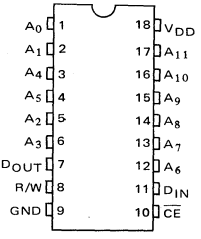
The TC5504AP/AD is offered in both standard 18 pin plastic and cerdip packages, 0.3 inch in width.

FEATURES

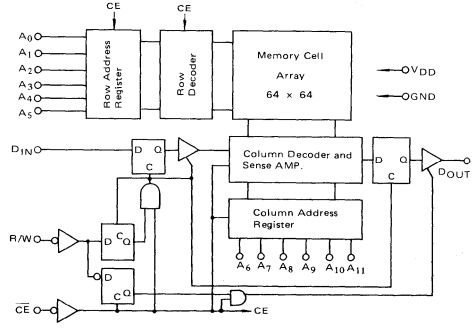
- Standby Current
  0.2μA (Max.) at Ta = 25°C
  1.0μA (Max.) at Ta = 60°C : TC5504APL/ADL
  20μA (Max.) : TC5504AP/AD
- Low Power Dissipation : 15mW (Typ.) operating
- Single 5V Power Supply : 5V ± 10%
- Data Retention Supply Voltage : 2 ~ 5.5V
- All Inputs and Output : Directly TTL Compatible
- Access Time
  200ns (Max.): TC5504AP/APL/AD/ADL-2
  300ns (Max.) : TC5504AP/APL/AD/ADL-3
- Static Operation
- On Chip Address Register
- Three State Output
- Package
  Plastic DIP : TC5504AP/APL
  Cerdip DIP : TC5504AD/ADL

PIN CONNECTION

(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{11}$	Address Inputs
R/W	Read Write Control Input
$\overline{CE}$	Chip Enable Input
D_{IN}	Data Input
D_{OUT}	Data Output
V_{DD}	Power
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM		RATING	UNIT
V_{DD}	Power Supply Voltage		−0.3 ~ 7.0	V
V_{IN}	Input Voltage		−0.3 ~ 7.0	V
V_{OUT}	Output Voltage		0 ~ V_{DD}	V
P_D	Power Dissipation (Ta = 85°C)	TC5504AP/APL	550	mW
		TC5504AD/ADL	800	mW
T_{SOLDER}	Soldering Temperature · Time		260 · 10	°C · sec
T_{STG}	Storage Temperature		−55 ~ 150	°C
T_{OPR}	Operating Temperature		−30 ~ 85	°C

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

D.C. CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = −30°C to 85°C, unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.(1)	MAX.	UNIT
I_{IL}	Input Leakage Current	0V ≦ V_{IN} ≦ V_{DD}			–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{DD} − 0.2V, 0V ≦ V_{OUT} ≦ V_{DD}			–	–	±5.0	μA
I_{OH}	Output High Level Current	V_{OH} = 2.4V			−1.0	–	–	mA
I_{OL}	Output Low Level Current	V_{OL} = 0.4V			2.0	–	–	mA
I_{DDS}	Standby Current	V_{DD} = 2V ~ 5.5V, $\overline{CE}$ = V_{DD} − 0.2V, other inputs = 0.2V or V_{DD} − 0.2V	TC5504APL	Ta = 25°C	–	–	0.2	μA
			TC5504ADL	Ta = 60°C	–	–	1.0	
			TC5504AP TC5504AD		–	0.05	20	μA
I_{DDO1}	Operating Current	t_{cycle} = 1μS, I_{OUT} = 0mA			–	–	10.0	mA
I_{DDO2}		t_{cycle} = 1μS, V_{IH} = V_{DD}, V_{IL} = 0V, I_{OUT} = 0mA			–	3.0	5.0	mA

Note (1) V_{DD} = 5V, Ta = 25°C

CAPACITANCE(2) (Ta = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1MHz	–	4	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1MHz	–	5	10	pF

Note (2): This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = –30°C to 85°C, unless otherwise noted)

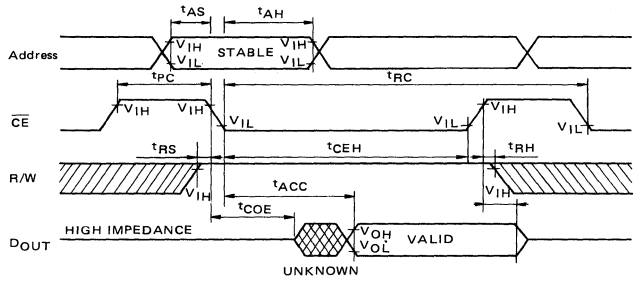
SYMBOL	PARAMETER	TC5504AP-2/APL-2 TC5504AD-2/ADL-2		TC5504AP-3/APL-3 TC5504AD-3/ADL-3		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	300	–	420	–	ns
t_{WC}	Write Cycle Time	300	–	420	–	ns
t_{RMWC}	Read Modify Write Cycle Time	390	–	580	–	ns
t_{AS}	Address Setup Time	5	–	5	–	ns
t_{AH}	Address Hold Time	60	–	80	–	ns
t_{PC}	Precharge Time	80	–	100	–	ns
t_{CEH}	Chip Enable Hold Time	200	–	300	–	ns
t_{ACC}	Access Time	–	200	–	300	ns
t_{OD}	Output Disable Time	–	70	–	100	ns
t_{COE}	Output Enable Time	0	–	0	–	ns
t_{RS}	Read Setup Time	0	–	0	–	ns
t_{RH}	Read Hold Time	0	–	0	–	ns
t_{WS}	Write Setup Time	0	–	0	–	ns
t_{WH}	Write Hold Time	60	–	80	–	ns
t_{DS}	Data Setup Time	5	–	5	–	ns
t_{DH}	Data Hold Time	60	–	80	–	ns
t_{WCH}	Write Enable to $\overline{CE}$ Hold Time	80	–	150	–	ns
t_{MD}	Modify Time	0	–	0	–	ns

A.C. TEST CONDITIONS

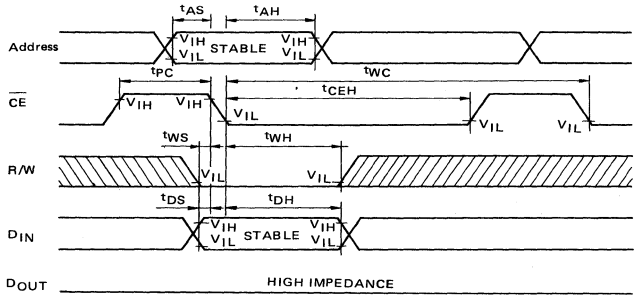
Output Load : 100pF + 1TTL Gate
Input Pulse Levels : 0.6 ~ 2.4V
Timing Measurement Reference Levels
Input : 0.8V and 2.2V
Output : 0.8V and 2.2V
Input Pulse Rise and Fall Times : 10 ns

TIMING WAVEFORMS

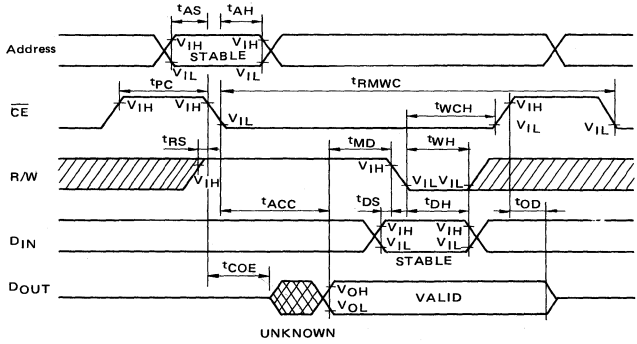
- **READ CYCLE**



- **WRITE CYCLE**

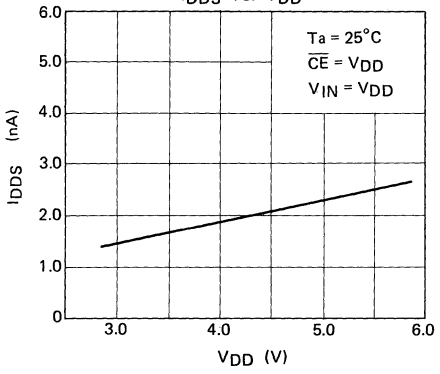


- **READ MODIFY WRITE CYCLE**

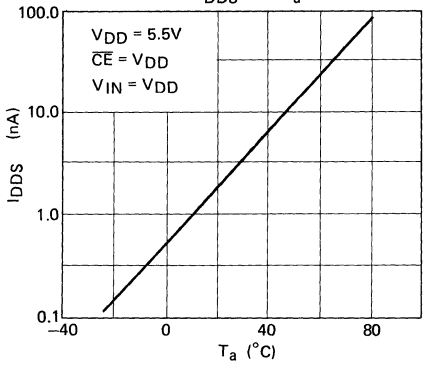


TYPICAL CHARACTERISTICS

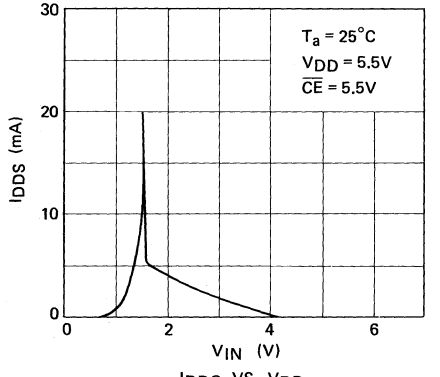
I_{DDS} VS. V_{DD}



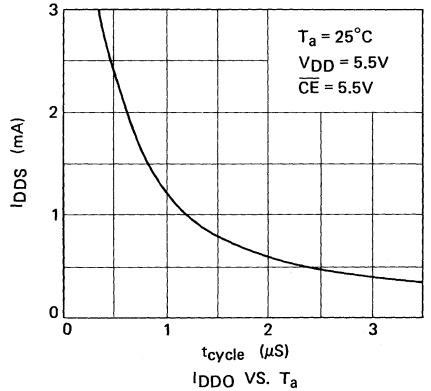
I_{DDS} VS. T_a



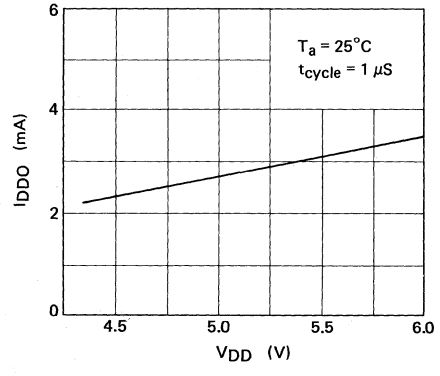
I_{DDS} VS. V_{IN}



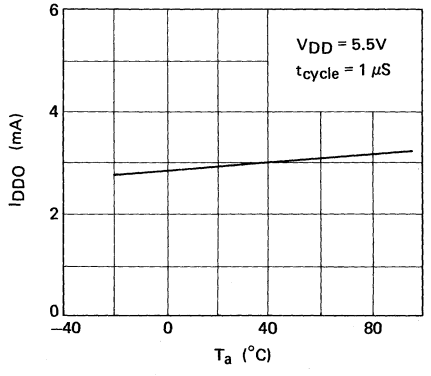
I_{DDS} VS. t_{cycle}



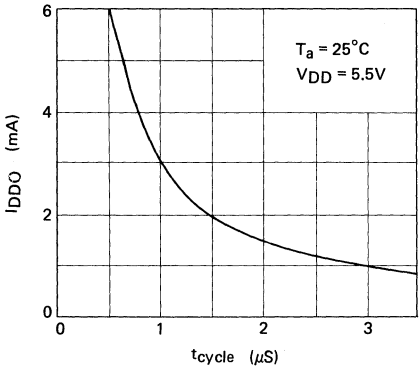
I_{DDO} VS. V_{DD}



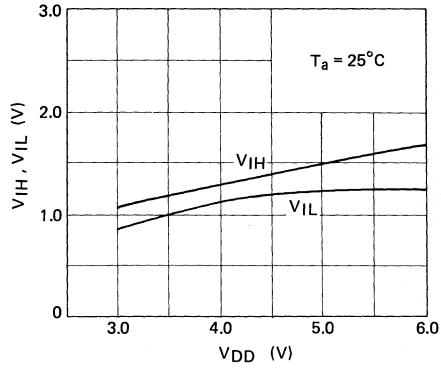
I_{DDO} VS. T_a



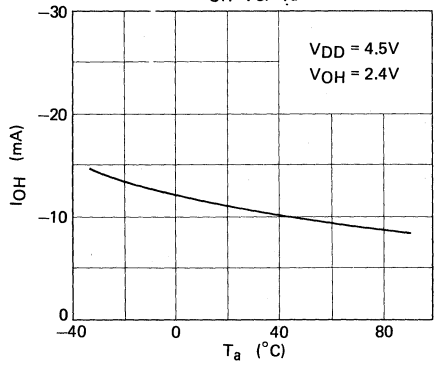
I_{DDO} VS. t_{cycle}



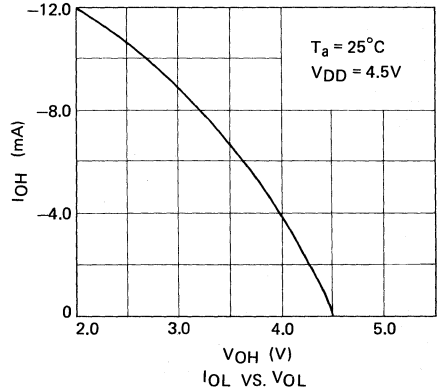
V_{IH}, V_{IL} VS. V_{DD}



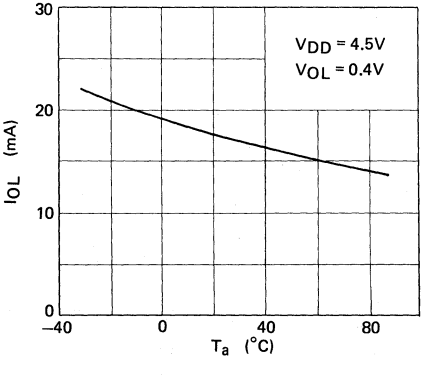
I_{OH} VS. T_a



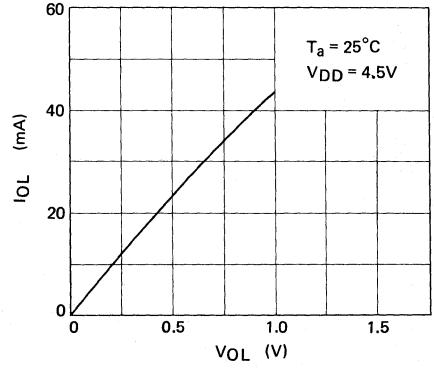
I_{OH} VS. V_{OH}



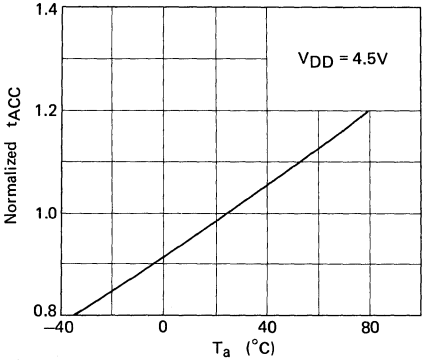
I_{OL} VS. T_a



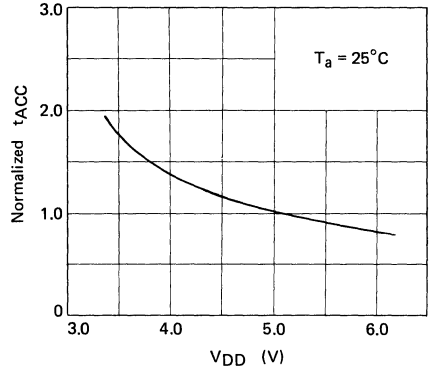
I_{OL} VS. V_{OL}



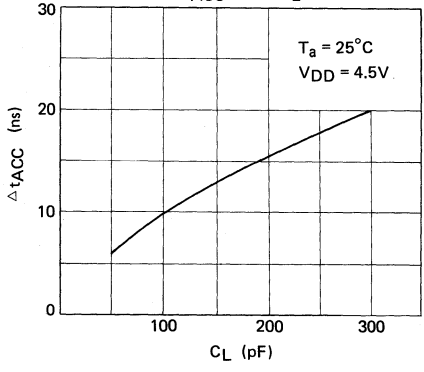
Normalized t_{ACC} VS. T_a



Normalized t_{ACC} VS. V_{DD}

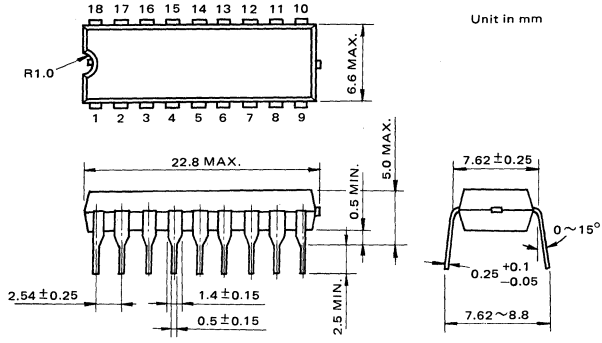


$\triangle t_{ACC}$ VS. C_L

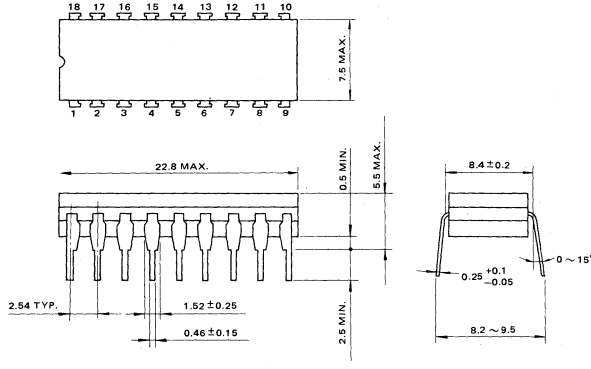


OUTLINE DRAWINGS

- PLASTIC PACKAGE



- CERDIP PACKAGE



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25mm of their longitudinal position with respect to No. 1 and No. 18 leads.
All dimensions are in millimeters.

1024 WORD x 4 BIT CMOS STATIC RAM

SILICON GATE CMOS

TC5513AP-20/TC5513APL-20
TC5513AD-20/TC5513ADL-20

DESCRIPTION

The TC5513AP/AD is a 4,096-bit high speed static random access memory organized as 1,024 words by 4 bits and operates form a single 5-volt supply.

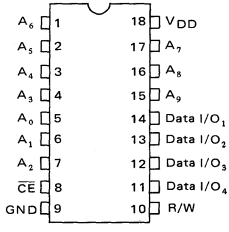
The TC5513AP/AD is a fully CMOS RAM and is therefore suited for use in low power applications where battery operation and/or battery back up for nonvolatility are required. The TC5513AP/AD is guaranteed for data retention at power supply voltages as low as 2.0 volt. All inputs and outputs are TTL compatible.

The TC5513AP/AD is packaged in a standard 18-pin dual-in-line plastic and cerdip package, 0.3 inch width.

FEATURES

- Low Power Dissipation
  27.5m W/MHz (MAX.) : Operating
- Standby Current
  0.2μA (MAX.) at Ta = 25°C
  1.0μA (MAX.) at Ta = 60°C
  } TC5513APL/ADL-20
  20 μA (MAX.) TC5513AP/AD-20
- Fast Access Time
  t_{ACC} : 200ns (MAX.)
- Single 5V Power Supply
- Data Retention Supply Voltage
  2V to 5.5V
- Fully Static Operation
- On-chip Address Transition Detector
- Three State Outputs
- Inputs and outputs Directly TTL compatible
- Package
- Plastic DIP: TC5513AP-20/APL-20
  Cerdip DIP: TC5513AD-20/ADL-20

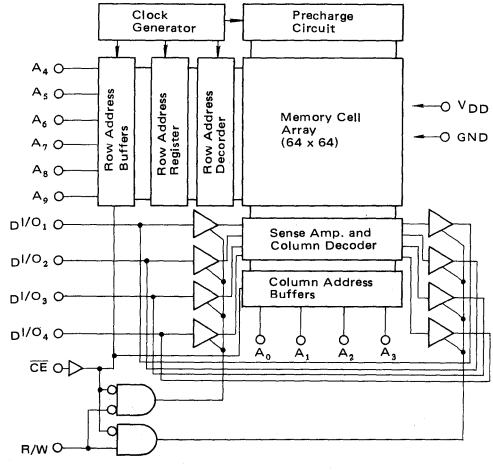
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_9$	Address Inputs
R/W	Read Write Input
$\overline{CE}$	Chip Enable Input
Data $I/O_{1\sim4}$	Data Input/Output
V_{DD}/GND	Power Supply Terminals

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM		RATING	UNIT
V_{DD}	Power Supply Voltage		−0.3 ~ 7.0	V
V_{IN}	Input Voltage		−0.3 ~ 7.0	V
$V_{I/O}$	I/O Voltage		−0.3 ~ V_{DD} +0.5	V
P_D	Power Dissipation (Ta = 85°C)	TC5513AP/APL	550	mW
		TC5513AD/ADL	800	mW
T_{SOLDER}	Soldering Temperature • Time		260 • 10	°C • sec
T_{STG}	Storage Temperature		−55 ~ 150	°C
T_{OPR}	Operating Temperature		−30 ~ 85	°C

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Level Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Level Voltage	−0.3	–	0.8	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

D.C. CHARACTERISTICS (Ta = −30°C ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.[1]	MAX.	UNIT
I_{IL}	Input Leakage Current	$0V \leqq V_{IN} \leqq V_{DD}$		–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$, $0V \leqq V_{I/O} \leqq V_{DD}$		–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		−1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		2.0	–	–	mA
I_{DDS}	Standby Current	V_{DD} = 2V ~ 5.5V, $\overline{CE} \geqq V_{DD}$ −0.2V	TC5513APL-20 Ta=25°C	–	–	0.2	μA
			TC5513ADL-20 Ta=60°C	–	–	1.0	μA
			TC5513AP-20, TC5513AD-20	–	0.05	20	μA
I_{DD01}	Operating Current	t_{cycle} = 1μs, I_{OUT} = 0mA		–	5.0	9.0	mA
I_{DD02}		t_{cycle} = 1μs, $V_{IH} = V_{DD}$, V_{IL} = 0V, I_{OUT} = 0mA		–	3.0	5.0	mA

Note (1): V_{DD} = 5V, Ta = 25°C

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	4	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	–	5	10	pF

Note (2): This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = -30 ~ 85°C)

- **READ CYCLE**

SYMBOL	PARAMETER	TC5513AP-20/APL-20 TC5513AD-20/ADL-20		UNIT
		MIN.	MAX.	
t_{RC}	Read Cycle Time	200	–	ns
t_{ACC}	Access Time	–	200	ns
t_{CO}	$\overline{CE}$ Access Time	–	200	ns
t_{OH}	Output Data Hold Time	15	–	ns
t_{DIS}	Output Disable Time	–	60	ns
t_{COE}	Output Enable Time	5	–	ns

- **WRITE CYCLE**

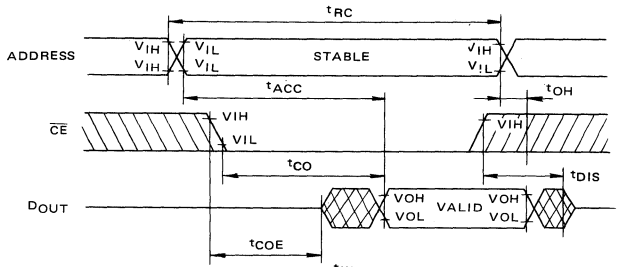
SYMBOL	PARAMETER	TC5513AP-20/APL-20 TC5513AD-20/ADL-20		UNIT
		MIN.	MAX.	
t_{WC}	Write Cycle Time	200	–	ns
t_{AW}	Address Setup Time	0	–	ns
t_{WP}	Write Pulse Width	120	–	ns
t_{DS}	Data Setup Time	120	–	ns
t_{DH}	Data Hold Time	0	–	ns
t_{WR}	Write Recovery Time	0	–	ns

A.C. TEST CONDITIONS

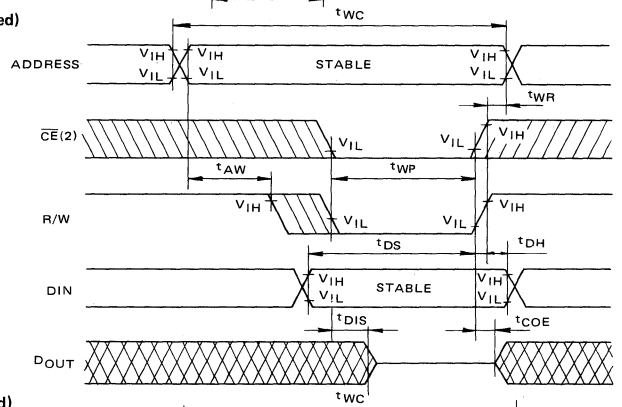
- Output Load : 100pF + 1 TTL Gate
- Input Pulse Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels
  - Input : 0.8V, 2.2V
  - Output : 0.8V, 2.2V
- Input Pulse Rise and Fall Times : 10ns

TIMING WAVEFORMS

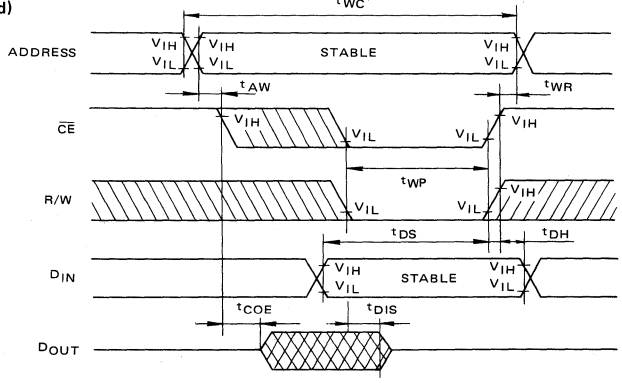
- **Read Cycle (1)**



- **Write Cycle 1 (R/W Controlled)**

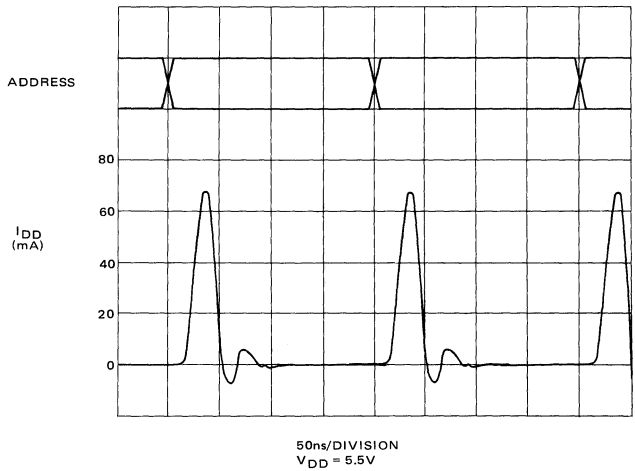


- **Write Cycle 2 ($\overline{CE}$ Controlled)**



Notes: (1) R/W is high for a Read Cycle.
(2) If the $\overline{CE}$ low transition occurs simultaneously with the R/W low transition, the output buffers remain in high impedance state.

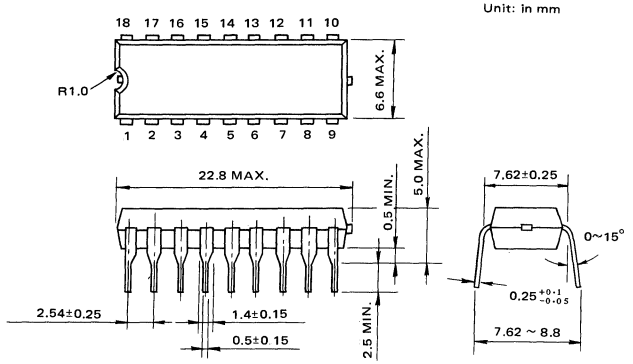
TYPICAL CURRENT WAVEFORM



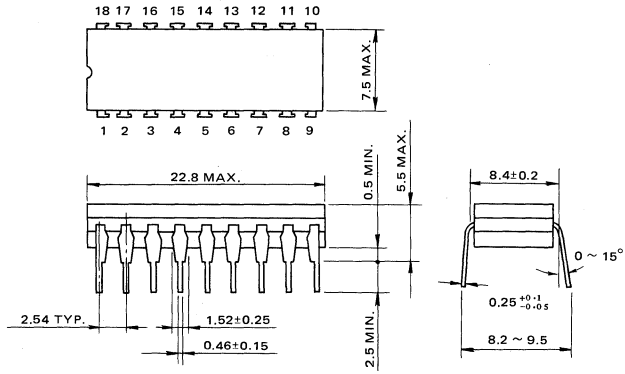
OUTLINE DRAWINGS

- **PLASTIC PACKAGE**

Unit: in mm



- **CERDIP PACKAGE**



Notes: (1) Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No. 1 and No. 18 leads. All dimensions are in millimeters.

TOSHIBA MOS MEMORY PRODUCTS

1024 WORD X 4 BIT CMOS STATIC RAM

SILICON GATE CMOS

TC5514AP-2/-3, TC5514APL-2/-3
TC5514AD-2/-3, TC5514ADL-2/-3

DESCRIPTION

The TC5514AP/AD is a 4,096 bit high speed and low power static random access memory organized as 1,024 words by 4 bits using CMOS technology, and operates from a single 5-volt supply.

The TC5514AP/AD is compatible with the industry produced NMOS 2114 type 4KRAM, yet offers a more than 90% reduction in power of their NMOS equivalents.

The TC5514AP/AD is a fully CMOS RAM, therefore it is suited for use in low power applications where battery operation and battery back up for nonvolatility are required. Furthermore the TC5514APL/ADL guaranteed a standby current equal to or less than 1μA at 60°C ambient temperature is available.

The TC5514AP/AD is guaranteed for data retention at a power supply as low as 2 volts. The TC5514AP/AD is directly TTL compatible in all inputs and outputs.

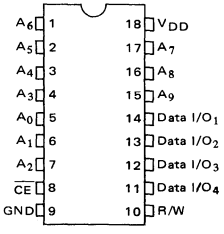
The TC5514AP/AD is offered in both standard 18 pin plastic and cerdip packages, 0.3 inchs in width.

FEATURES

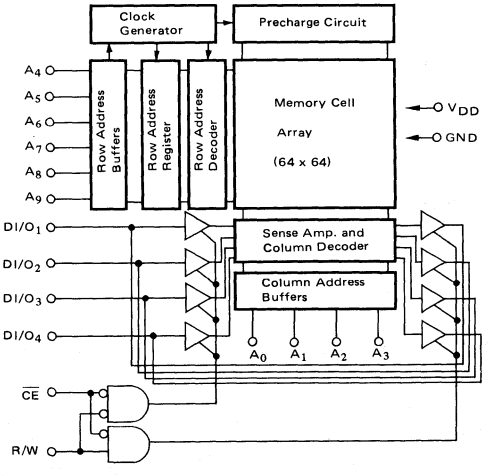
- Standby Current
  0.2μA (Max.) at Ta=25°C
  1.0μA (Max.) at Ta=60°C } : TC5514APL/ADL
  20μA (Max.) : TC5514AP/AD
- Low Power Dissipation : 15mW (Typ.) operating
- Single 5-volt Supply : 5V ± 10%
- Data Retention Supply Voltage : 2 ~ 5.5V
- Three State Outputs
- All Inputs and Outputs : Directly TTL Compatible
- Access Time
  200ns (Max.) : TC5514AP/APL/AD/ADL-2
  300ns (Max.) : TC5514AP/APL/AD/ADL-3
- Fully Static Operation
- On-chip Address Transition Detector
- Fully Compatible with TMM314AP Family (Nch 2114 type 4KRAM)
- Package
  Plastic DIP : TC5514AP/APL
  Cerdip DIP : TC5514AD/ADL

PIN CONNECTION

(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_9$	Address Inputs
R/W	Read Write Control Input
$\overline{CE}$	Chip Enable Input
Data $I/O_{1 \sim 4}$	Data Input/Output
V_{DD}/GND	Power Supply Terminals

MAXIMUM RATINGS

SYMBOL	ITEM		RATING	UNIT
V_{DD}	Power Supply Voltage		−0.3 ~ 7.0	V
V_{IN}	Input Voltage		−0.3 ~ 7.0	V
$V_{I/O}$	I/O Voltage		0 ~ V_{DD}	V
P_D	Power Dissipation (Ta = 85°C)	TC5514AP/APL	550	mW
		TC5514AD/ADL	800	mW
T_{SOLDER}	Soldering Temperature · Time		260 · 10	°C · sec
T_{STG}	Storage Temperature		−55 ~ 150	°C
T_{OPR}	Operating Temperature		−30 ~ 85	°C

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Level Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Level Voltage	−0.3	–	0.8	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

D.C. CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = −30 ~ 85°C unless otherwise noted.)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP. (1)	MAX.	UNIT
I_{IL}	Input Leakage Current	$0V \leqq V_{IN} \leqq V_{DD}$			–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$, $0V \leqq V_{I/O} \leqq V_{DD}$			–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.0	–	–	mA
I_{DDS}	Standby Current	V_{DD} = 2V ~ 5.5V, All Inputs = 0.2V or V_{DD} − 0.2V	TC5514APL	Ta = 25°C	–	–	0.2	μA
			TC5514ADL	Ta = 60°C	–	–	1.0	μA
			TC5514AP TC5514AD		–	0.05	20	μA
I_{DDO1}	Operating Current	t_{cycle} = 1μs, I_{OUT} = 0mA			–	5.0	9.0	mA
I_{DDO2}		t_{cycle} = 1μs, $V_{IH} = V_{DD}$, V_{IL} = 0V, I_{OUT} = 0mA			–	3.0	5.0	

Note (1): V_{DD} = 5V, Ta = 25°C

CAPACITANCE(2) (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	4	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	–	5	10	pF

Note (2): This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = –30 ~ 85°C)

- **READ CYCLE**

SYMBOL	PARAMETER	TC5514AP-2/APL-2 TC5514AD-2/ADL-2		TC5514AP-3/APL-3 TC5514AD-3/ADL-3		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	200	–	300	–	ns
t_{ACC}	Access Time	–	200	–	300	ns
t_{CO}	$\overline{CE}$ Access Time	–	70	–	100	ns
t_{OH}	Output Data Hold Time	15	–	20	–	ns
t_{DIS}	Output Disable Time	–	60	–	80	ns
t_{COE}	Output Enable Time	5	–	5	–	ns

- **WRITE CYCLE**

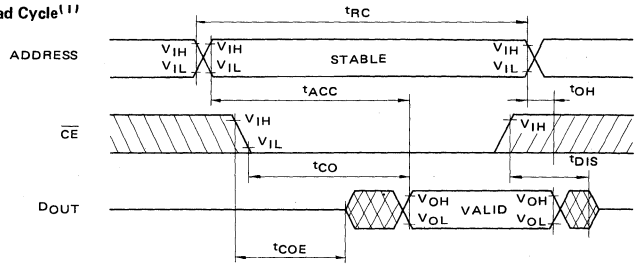
SYMBOL	PARAMETER	TC5514AP-2/APL-2 TC5514AD-2/ADL-2		TC5514AP-3/APL-3 TC5514AD-3/ADL-3		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	200	–	300	–	ns
t_{AW}	Address Setup Time	0	–	0	–	ns
t_{WP}	Write Pulse Width	120	–	150	–	ns
t_{DS}	Data Setup Time	120	–	150	–	ns
t_{DH}	Data Hold Time	0	–	0	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	ns

A.C. TEST CONDITIONS

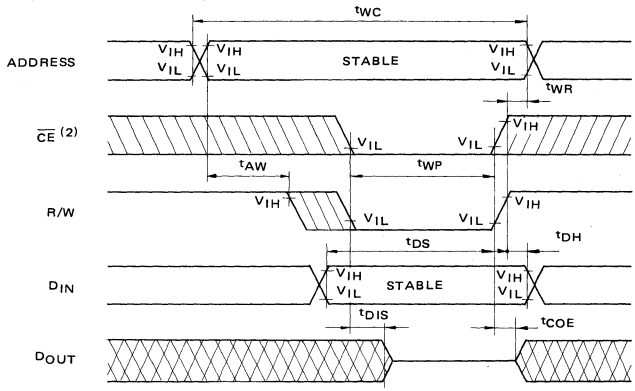
- Output Load : 100 pF + 1 TTL Gate
- Input Pulse Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels
  - Input : 0.8V, 2.2V
  - Output : 0.8V, 2.2V
- Input Pulse Rise and Fall Times : 10 ns

TIMING WAVEFORMS

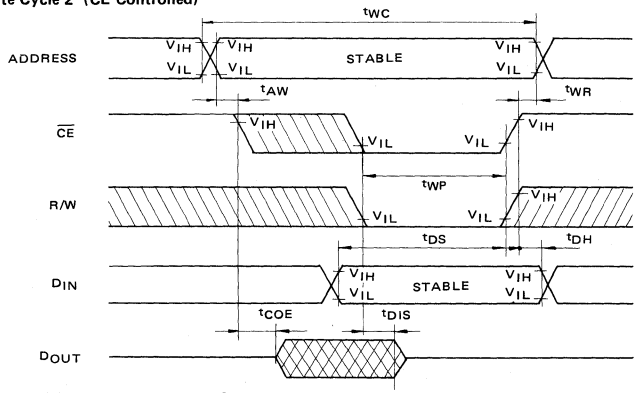
- **Read Cycle**(1)



- **Write Cycle 1 (R/W Controlled)**

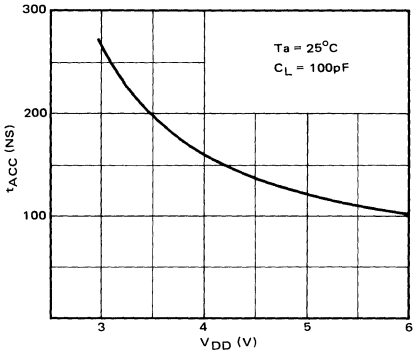


- **Write Cycle 2 (CE Controlled)**

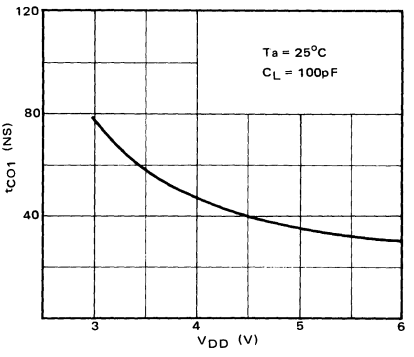


Notes: (1) R/W is high for a Read Cycle.
(2) If the CE low transition occurs simultaneously with the R/W low transition, the output buffers remain in a high impedance state.

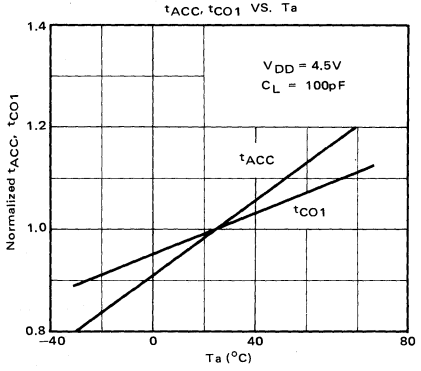
t_{ACC} VS. V_{DD}



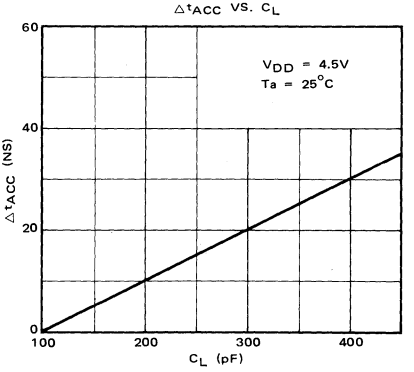
t_{CO1} VS. V_{DD}



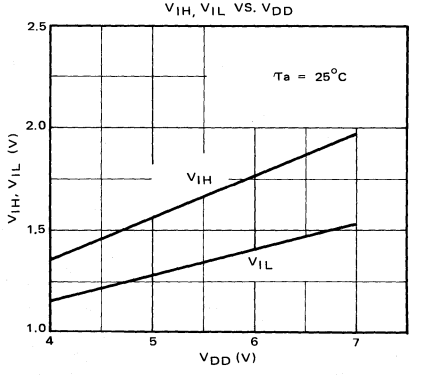
t_{ACC}, t_{CO1} VS. Ta



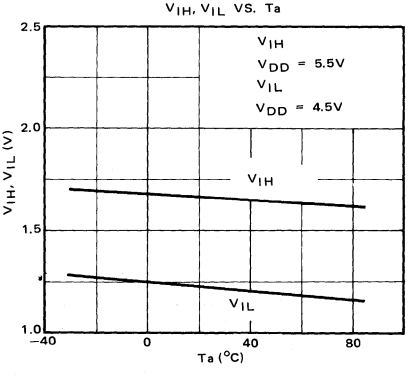
$\triangle t_{ACC}$ VS. C_L



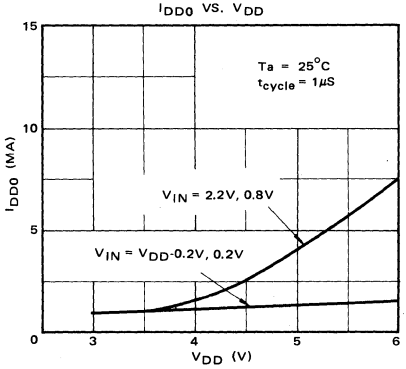
V_{IH}, V_{IL} VS. V_{DD}



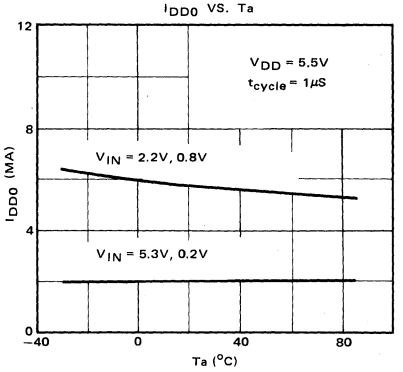
V_{IH}, V_{IL} VS. Ta



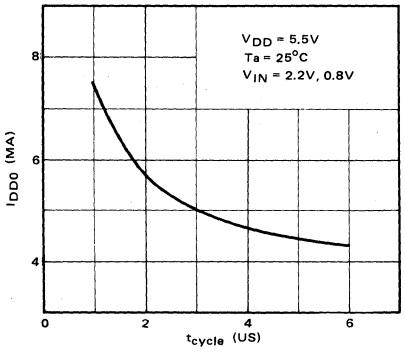
I_{DD0} VS. V_{DD}



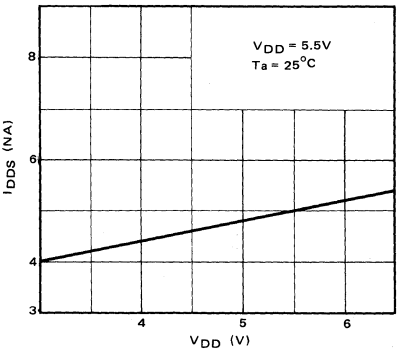
I_{DD0} VS. Ta



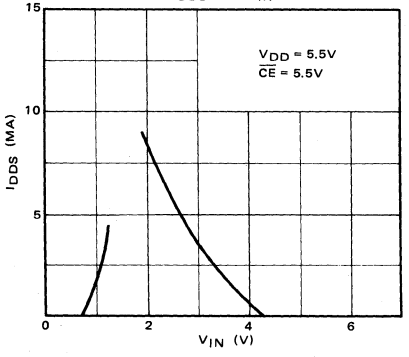
I_{DD0} VS. t_{cycle}



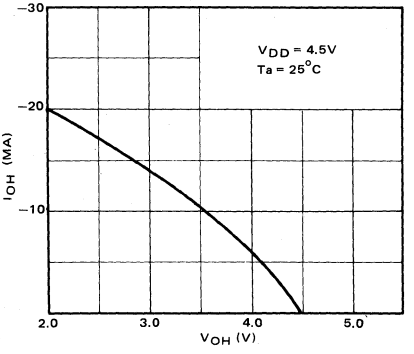
I_{DDS} VS. V_{DD}

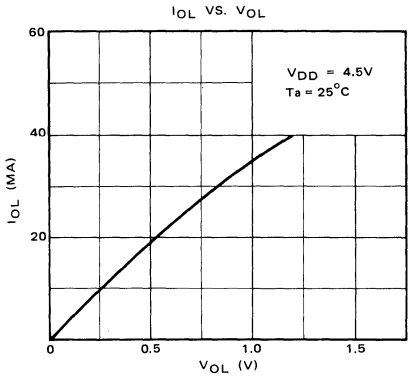


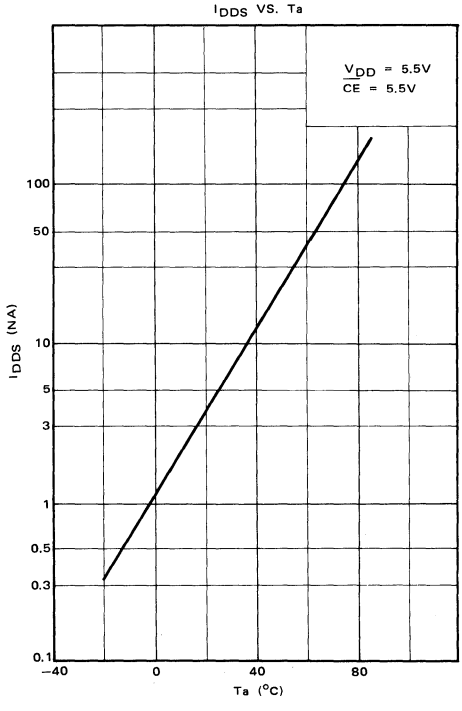
I_{DDS} VS. V_{IN}



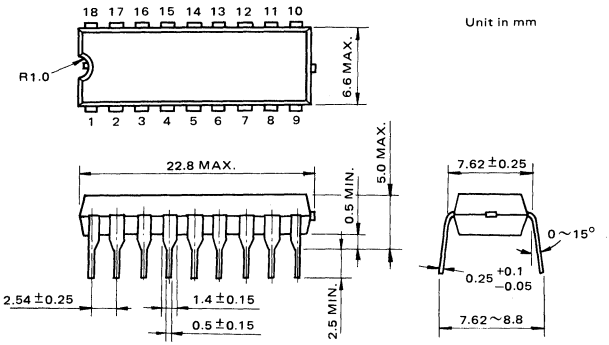
I_{OH} VS. V_{OH}



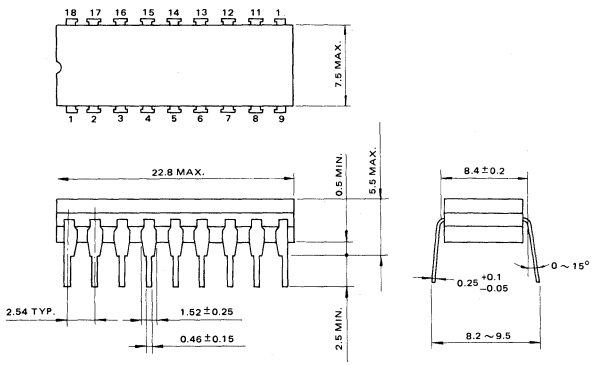

I_{OL} VS. V_{OL}
V_{DD} = 4.5V
Ta = 25°C
I_{OL} (MA)
60
40
20
0
0.5
1.0
1.5
V_{OL} (V)


I_{DDS} VS. Ta
V_{DD} = 5.5V
$\overline{CE}$ = 5.5V
I_{DDS} (NA)
100
50
10
5
3
1
0.5
0.3
0.1
−40
0
40
80
Ta (°C)

- PLASTIC PACKAGE



- CERDIP PACKAGE



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25mm of their longitudinal position with respect to No. 1 and No. 18 leads.
All dimensions are in millimeters.

1024 WORD X 4 BIT CMOS RAM

SILICON GATE CMOS

TC5514P
TC5514P-1

DESCRIPTION

The TC5514P is a full static read write memory organized as 1024 words by 4 bits using CMOS technology. Because of ultra low power dissipation, the TC5514P can be used as battery operated portable memory system and also as a nonvolatile memory with battery back up. The TC5514P operates from a single 5V power supply with a static operation, so that the no refresh periods are required. This simplifies the power supply circuit design.

The three state outputs simplify the memory expansion making the TC5514P suitable for use in a microprocessor peripheral memory. Since the minimum data retention voltage is 2V, the battery back up system needs only simple circuit. By using Toshiba's original C²MOS technology, the device circuitry is not only simplified but wide operating margin and noise margin are also realized.

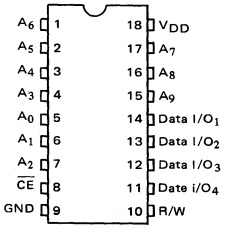
The TC5514P family is moulded in a dual-in-line 18-pin plastic package, 0.3 inch in width.

FEATURES

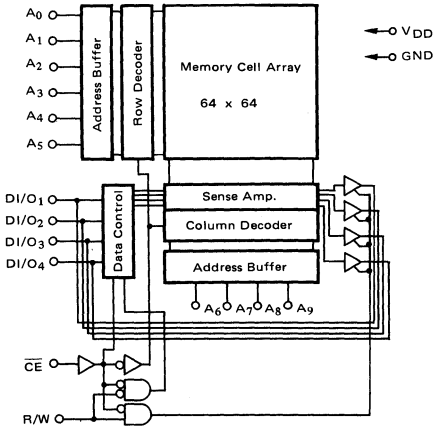
- Low Power Dissipation
  110 μW (MAX.) STAND BY
  110mW (MAX.) OPERATING; TC5514P-1
  138mW (MAX.) OPERATING; TC5514P
- Data Retention Voltage 2V to 5.5V
- Single 5V Power Supply
- 18 PIN Plastic Package
- Full Static Operation
- Three State Outputs
- Input/Output TTL Compatible
- Access Time
  TC5514P ; t_{ACC} = 450ns (MAX.)
  TC5514P-1; t_{ACC} = 650ns (MAX.)

PIN CONNECTION

(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_9$	Address Inputs
R/W	Read Write Input
$\overline{CE}$	Chip Enable Input
Data $I/O_1 \sim 4$	Data Input/Output
V_{DD}/GND	Power Supply Terminal

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3~V_{DD} +0.3	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation (Ta = 85°C)	550	mW
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	−30~85	°C

D.C. RECOMMENDED OPERATING CONDITION

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Level Voltage	2.2	–	V_{DD} +0.3	V
V_{IL}	Input Low Level Voltage	−0.3	–	0.65	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

D.C. CHARACTERISTICS (Ta = −30 ~ 85°C)

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP. (1)	MAX.	UNIT
I_{IN}	Input Current	$0 \leqq V_{IN} \leqq V_{DD}$		–	±0.05	±1.0	μA
I_{DDS}	Standby Current	V_{DD} = 2V to 5.5V $\overline{CE}$ = V_{DD} −0.2V; Output Open Other Inputs = 0.2V or V_{DD} −0.2V		–	0.2	20	μA
I_{DDO}	Operating Current	V_{DD} = 5.5V, t_{CYC} = 1 μS Output Open	TC5514P	–	13	25	mA
			TC5514P-1	–	10	20	mA
I_{LO}	Output Leakage Current	$0 \leqq V_{OUT} \leqq V_{DD}$		–	±0.05	±1.0	μA
I_{OH}	Output High Current	V_{DD} = 4.5V, V_{OH} = 2.4V		−1.0	−2.0	–	mA
I_{OL}	Output Low Current	V_{DD} = 4.5V, V_{OL} = 0.4V		2.0	3.0	–	mA
C_i (2)	Input Capacitance	f = 1MHz		–	5	10	pF
C_o (2)	Output Capacitance	f = 1MHz		–	7	15	pF

Note (1) Ta = 25°C V_{DD} = 5V

(2) This parameter is periodically sampled and is not 100% tested.

A.C. RECOMMENDED OPERATING CONDITION

TC5514P

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	V_{DD} = 4.5 ~ 5.5V C_L = 100pF + 1 TTL Gate V_{IH} = 2.2 ~ V_{DD} + 0.3V V_{IL} = –0.3 ~ 0.65V Ta = –30 ~ 85°C	450	–	ns
t_{WC}	Write Cycle Time		450	–	ns
t_{WP}	Write Pulse Width		350	–	ns
t_{DS}	Data Setup Time		200	–	ns
t_{DH}	Data Hold Time		0	–	ns
t_{WR}	Write Recovery Time		0	–	ns
t_{AW}	Address Setup Time		30	–	ns
t_{OH}	Output Data Hold Time		30	–	ns

TC5514P-1

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	V_{DD} = 4.5 ~ 5.5V C_L = 100pF + 1 TTL Gate V_{IH} = 2.2 ~ V_{DD} + 0.3V V_{IL} = –0.3 ~ 0.65V Ta = –30 ~ 85°C	650	–	ns
t_{WC}	Write Cycle Time		650	–	ns
t_{WP}	Write Pulse Width		350	–	ns
t_{DS}	Data Setup Time		200	–	ns
t_{DH}	Data Hold Time		0	–	ns
t_{WR}	Write Recovery Time		0	–	ns
t_{AW}	Address Setup Time		50	–	ns
t_{OH}	Output Data Hold Time		30	–	ns

A.C. CHARACTERISTICS (Ta = −30 ~ 85°C)

TC5514P

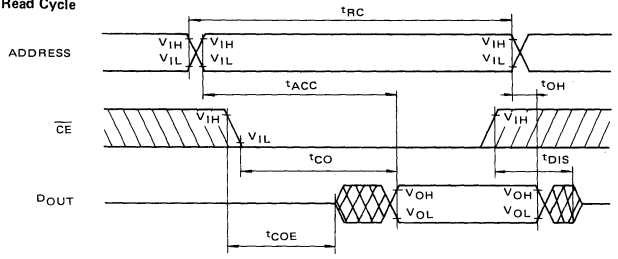
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{ACC}	Access Time	V_{DD} = 4.5 ~ 5.5V C_L = 100 pF V_{OH} = 2.2V, V_{OL} = 0.65V	–	–	450	ns
t_{CO}	$\overline{CE}$ Access Time		–	–	450	ns
t_{DIS}	Output Disable Time		–	–	150	ns
t_{COE}	Output Enable Time		20	150	–	ns

TC5514P-1

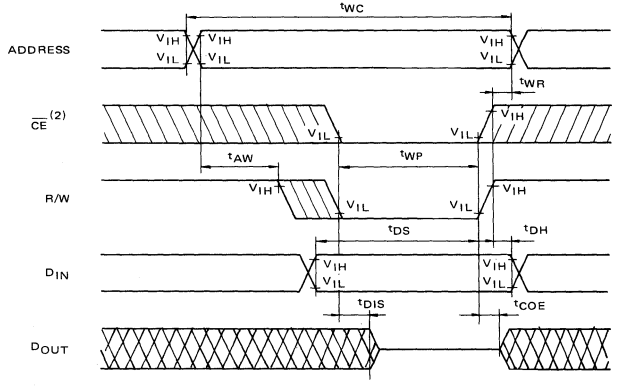
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{ACC}	Access Time	V_{DD} = 4.5 ~ 5.5V C_L = 100 pF V_{OH} = 2.2V, V_{OL} = 0.65V	–	–	650	ns
t_{CO}	$\overline{CE}$ Access Time		–	–	650	ns
t_{DIS}	Output Disable Time		–	–	150	ns
t_{COE}	Output Enable Time		20	150	–	ns

TIMING WAVEFORMS

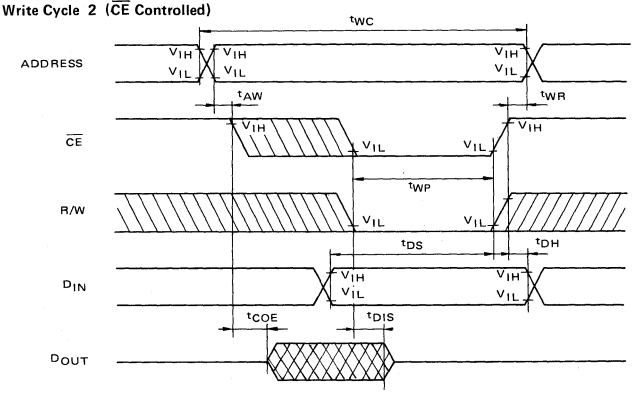
- **Read Cycle** (1)



- **Write Cycle 1 (R/W Controlled)**



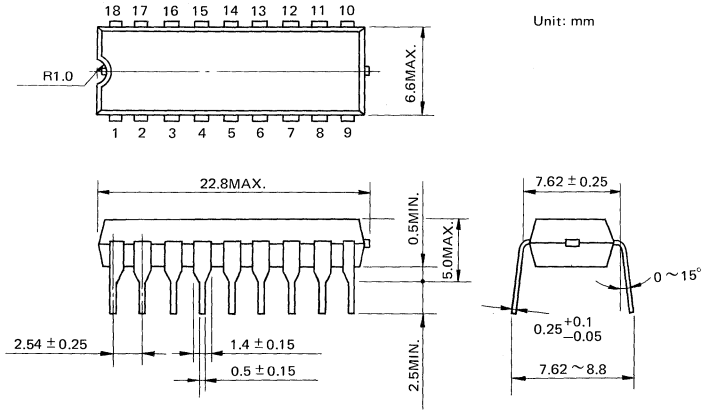
- **Write Cycle 2 ($\overline{CE}$ Controlled)**



Notes: (1) R/W is high for a Read Cycle.

(2) If the $\overline{CE}$ low transition occurs simultaneously with the R/W low transition, the output buffers remain in a high impedance state.

OUTLINE DRAWINGS



Unit: mm

Note: All dimensions are in millimeters. Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads.

2048 WORD x 8 BIT CMOS STATIC RAM

SILICON GATE CMOS

TC5516AP/-2, TC5516APL/-2
TC5516AD/-2, TC5516ADL/-2
TC5516AF/-2, TC5516AFL/-2

DESCRIPTION

The TC5516AP/AD/AF is a 16384-bit static random access memory organized as 2048 words by 8 bit using CMOS technology, and operates from a single 5 volt supply.

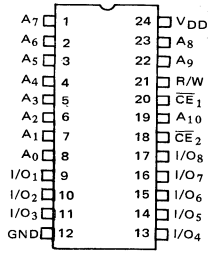
The TC5516AP/AD/AF is featured by two chip enable inputs, that is, $\overline{CE}_1$ for fast memory access and $\overline{CE}_2$ for a minimum standby current mode, and is suited for low power application where battery operation or battery back up for nonvolatility are required. Furthermore the TC5516APL/ADL/AFL guaranteed a standby current equal to or less than 1μA at 60°C ambient temperature is avialable.

The TC5516AP/AD is also featured by pin compatibility with 2716 type EPROM. This means that the TC5516AP/AD and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM obtained as a result allows the wide application in microcomputer system.

FEATURES

- Standby Current
  - 0.2μA (Max.) at Ta = 25°C } TC5516APL/
  - 1.0μA (Max.) at Ta = 60°C } ADL/AFL
  - 1.0μA (Max.) at Ta = 25°C } TC5516AP/
  - 5.0μA (Max.) at Ta = 60°C } AD/AF
- Low Power Dissipation : 200mW (Typ.) Operating
- Single 5V Power Supply : 5V ± 10%
- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Fully Static Operation
- Access Time
  - 250ns (Max.): TC5516AP/APL/AD/ADL/AF/AFL
  - 200ns (Max.): TC5516AP-2/APL-2/AD-2/ADL-2 AF-2/AFL-2
- Two Chip Enable ($\overline{CE}_1$, $\overline{CE}_2$) for Simple Memory Expansion and Battery Back Up.
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package
  - Plastic DIP : TC5516AP/APL
  - Cerdip DIP : TC5516AD/ADL
  - Plastic FP : TC5516AF/AFL

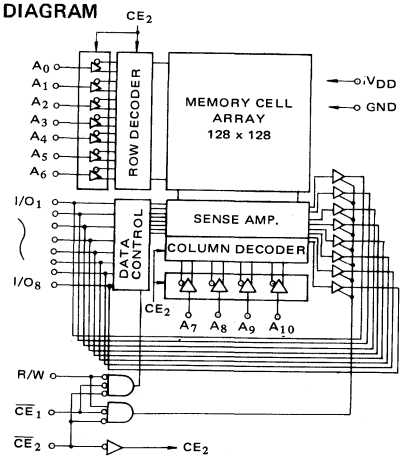
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_{10}$	Address Inputs
R/W	Read/Write Control Input
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enable Inputs
$I/O_1 \sim I/O_8$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	−0.3V ~ 7.0V
V_{IN}	Input Voltage	−0.3V ~ V_{DD} + 0.3
$V_{I/O}$	Input/Output Voltage	−0.3V ~ V_{DD} + 0.3
P_D	Power Dissipation (Ta = 85°C)	0.8W (0.45W)*
T_{STG}	Storage Temperature	−55°C ~ 150°C
T_{OPR}	Operating Temperature	−30°C ~ 85°C
T_{SOLDER}	Soldering Temperature · Time	260°C · 10 sec

*Plastic FP

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = −30°C ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

D.C. CHARACTERISTICS (Ta = −30°C ~ 85°C, V_{DD} = 5V ±10%)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$0 \leqq V_{IN} \leqq V_{DD}$			–	–	±1.0	μA
I_{LO}	I/O Leakage Current	$\overline{CE}_2 = V_{IH}$, $OV \leqq V_{I/O} \leqq V_{DD}$			–	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−1.0	−2.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.0	3.0	–	mA
I_{DDS1}	Standby Current	$\overline{CE}_2$ = 2.2V			–	1.0	3.0	mA
I_{DDS2}		$\overline{CE}_2 = V_{DD}$ −0.5V	TC5516APL/ ADL/AFL	Ta = 25°C	–	–	0.2	μA
				Ta = 60°C	–	–	1.0	
		V_{DD} = 2 ~ 5.5V	TC5516AP/ AD/AF	Ta = 25°C	–	0.05	1.0	
				Ta = 60°C	–	–	5.0	
				Ta = 85°C	–	–	30	
I_{DDO1}	Operating Current	$\overline{CE}_2$ = OV, $V_{IN} = V_{IH}/V_{IL}$, I_{OUT} = 0mA			–	40	70	mA
I_{DDO2}		$\overline{CE}_2$ = OV, $V_{IN} = V_{DD}$/GND, I_{OUT} = 0mA			–	30	55	

Note: Typical values are at Ta = 25°C, V_{DD} = 5V.

CAPACITANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	–	5	10	pF
$C_{I/O}$	Input/Output Capacitance	–	5	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = −30 ~ 85°C, V_{DD} = 5V ±10%)

- **Read Cycle**

SYMBOL	PARAMETER	TC5516AP-2/APL-2 TC5516AD-2/ADL-2 TC5516AF-2/AFL-2		TC5516AP/APL TC5516AD/ADL TC5516AF/AFL		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	200	–	250	–	ns
t_{ACC}	Access Time	–	200	–	250	ns
t_{CO1}	$\overline{CE}_1$ to Output Valid	–	100	–	100	ns
t_{CO2}	$\overline{CE}_2$ to Output Valid	–	200	–	250	ns
t_{COE}	$\overline{CE}_1$ or $\overline{CE}_2$ to Output Active	10	–	10	–	ns
t_{OD}	Output High-Z form Deselection	–	80	–	80	ns
t_{OH}	Output Hold from Address Change	10	–	10	–	ns

- **Write Cycle**

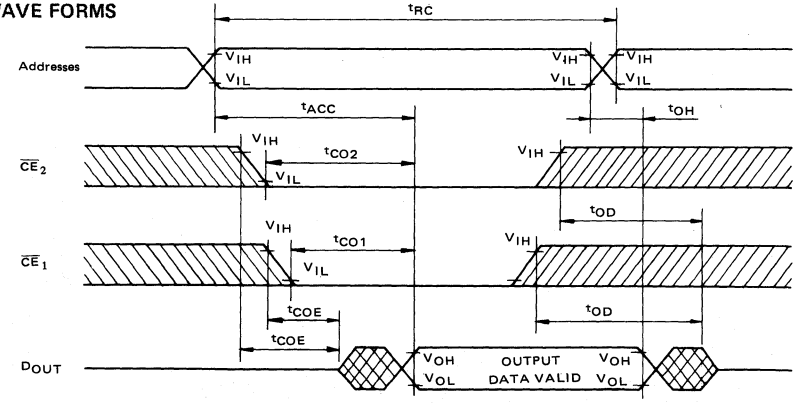
SYMBOL	PARAMETER	TC5516AP-2/APL-2 TC5516AD-2/ADL-2 TC5516AF-2/AFL-2		TC5516AP/APL TC5516AD/ADL TC5516AF/AFL		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	200	–	250	–	ns
t_{WP}	Write Pulse Width	160	–	200	–	ns
t_{AW}	Addresss Set Up Time	0	–	0	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	ns
t_{ODW}	Output High-Z from R/W	–	80	–	80	ns
t_{OEW}	Output Active from R/W	10	–	10	–	ns
t_{DS}	Data Set Up Time	80	–	120	–	ns
t_{DH}	Data Hold Time	0	–	0	–	ns

A.C. TEST CONDITIONS

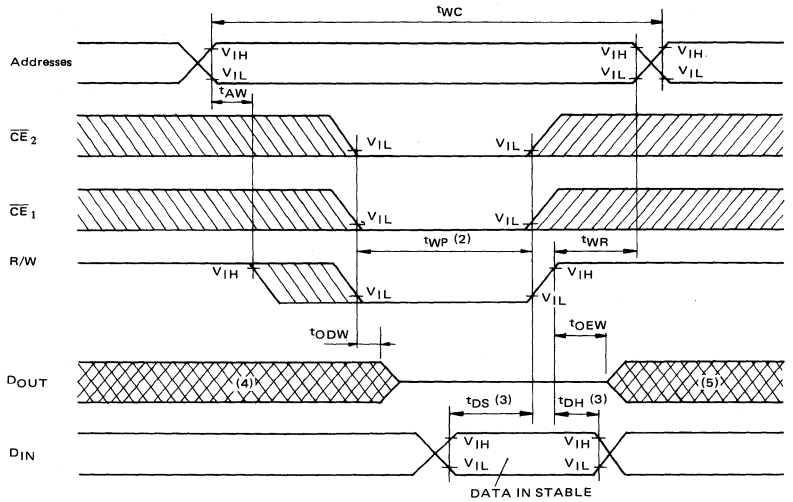
Output Load : 100 pF + ITTL Gate
Input Pulse Levels : 0.6V, 2.4V
Timing Measurement Reference Levels
Input : 0.8V and 2.2V
Output : 0.8V and 2.2V
Input Pulse Rise and Fall Times : 10ns

TIMING WAVE FORMS

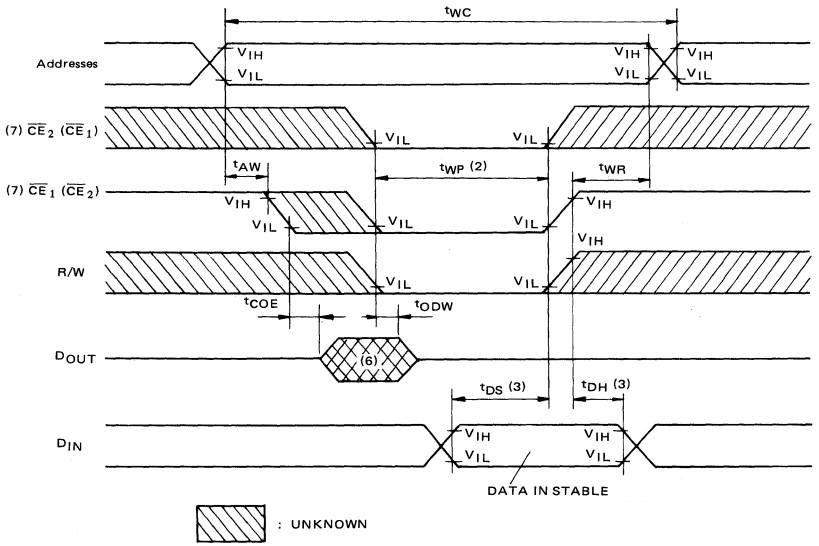
- **Read Cycle**



- **Write Cycle 1**



- **Write Cycle 2**

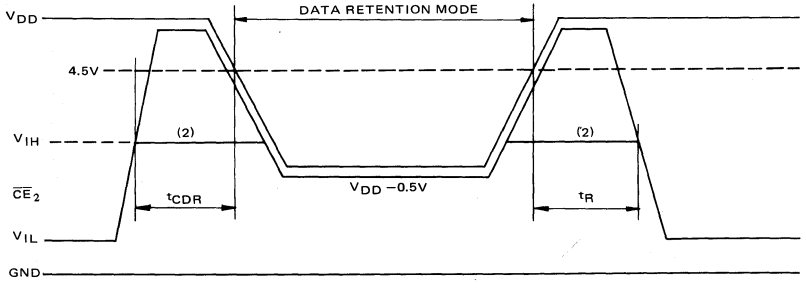


NOTE: (1) R/W is high for a Read Cycle.
(2) t_{WP} is specified as the logical "AND" of $\overline{CE}_1$, $\overline{CE}_2$ and R/W.
t_{WP} is measured from the latter of $\overline{CE}_1$, $\overline{CE}_2$ or R/W going low to the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or R/W going high.
(3) t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or R/W going high.
(4) If the $\overline{CE}_1$, or $\overline{CE}_2$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(5) If the $\overline{CE}_1$ or $\overline{CE}_2$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(6) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE}_1$ or $\overline{CE}_2$ low transition, the output buffers remain in a high impedance state in this period.
(7) A write occurs during the overlap of a low $\overline{CE}_1$, low $\overline{CE}_2$ and low R/W. In write cycle 2, write is controlled by either $\overline{CE}_1$ or $\overline{CE}_2$.

DATA RETENTION CHARACTERISTICS (Ta = −30 ~ 85°C)

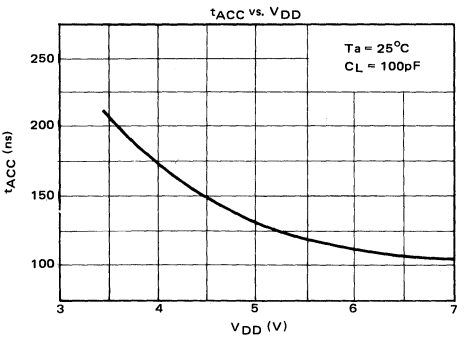
SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DR}	Data Retention Power Supply Voltage			2.0	—	5.5	V
I_{DDS}	Standby Current	TC5516APL/ ADL/AFL	Ta = 25°C	—	—	0.2	μA
			Ta = 60°C	—	—	1.0	
		TC5516AP/ AD/AF	Ta = 25°C	—	0.05	1.0	
			Ta = 60°C	—	—	5.0	
			Ta = 85°C	—	—	30	
t_{CDR}	From Chip Deselection to Data Retention Mode			0	—	—	μs
t_R	Recover Time			t_{RC} (1)	—	—	μs

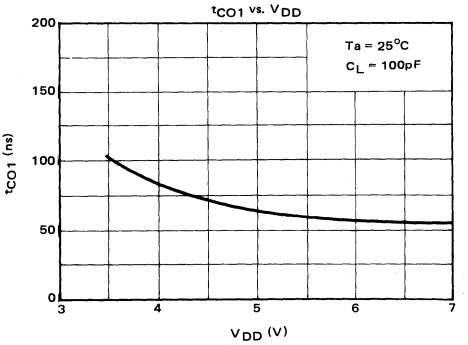
Note (1) t_{RC} : Read Cycle Time.

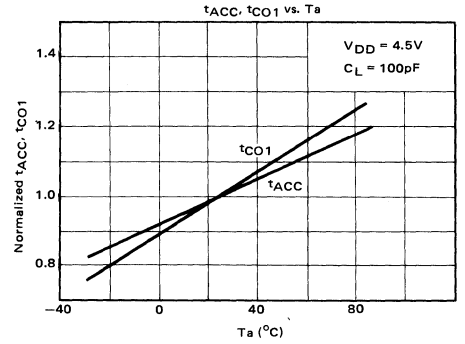


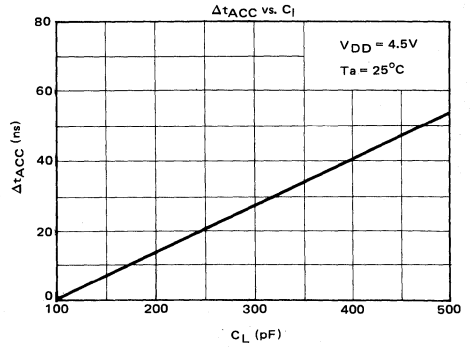
Note: (2) If the V_{IH} level of $\overline{CE}_2$ is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{SSD1} current flows. (Refer to D.C. CHARACTERISTICS or TYPICAL CHARACTERISTIC FIGURES.)

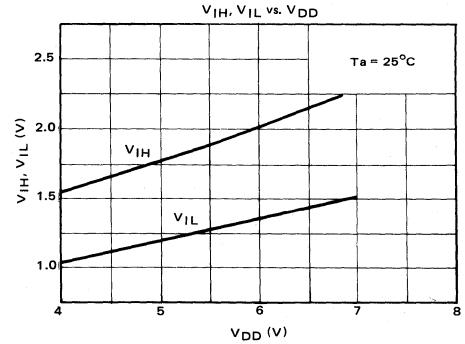
TYPICAL CHARACTERISTICS

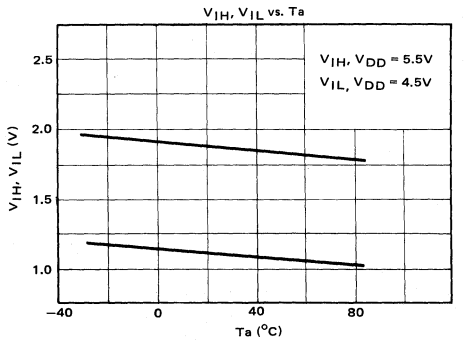




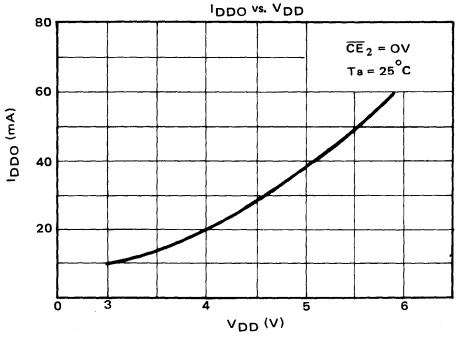




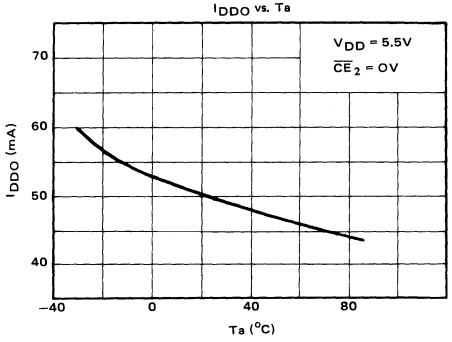




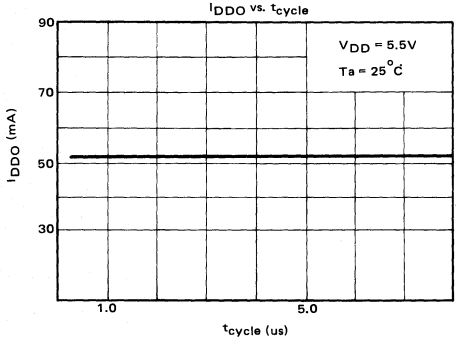
I_{DDO} vs. V_{DD}



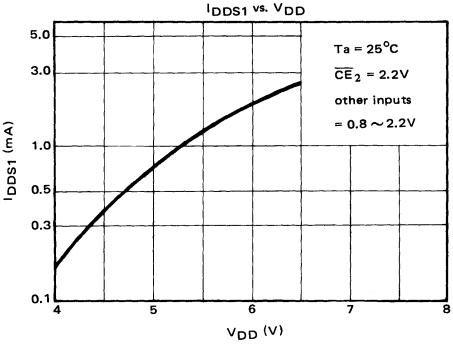
I_{DDO} vs. Ta



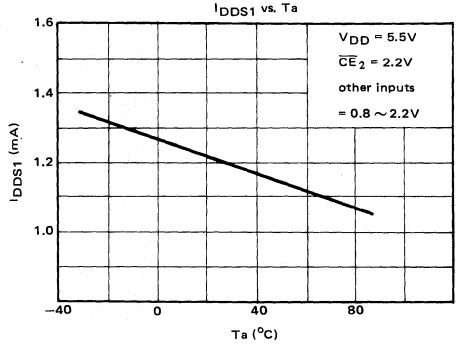
I_{DDO} vs. t_{cycle}



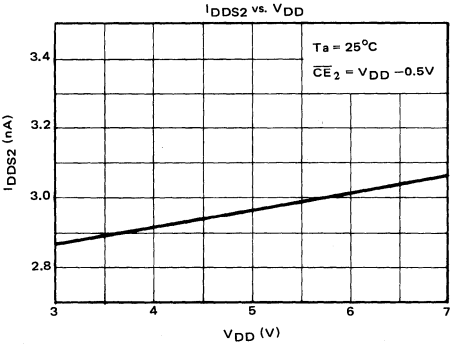
I_{DDS1} vs. V_{DD}

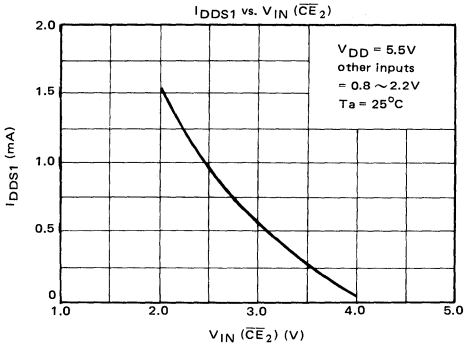


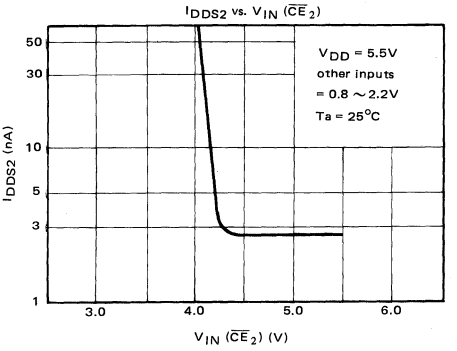
I_{DDS1} vs. Ta

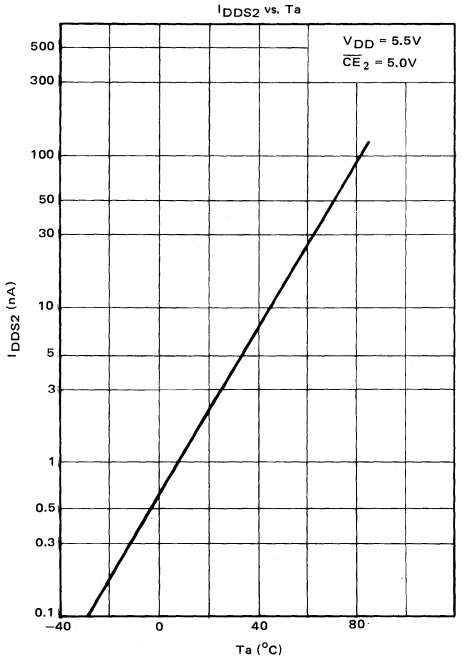


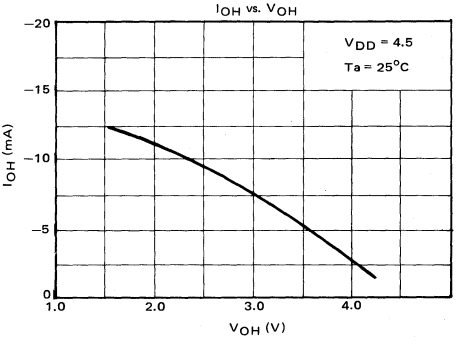
I_{DDS2} vs. V_{DD}

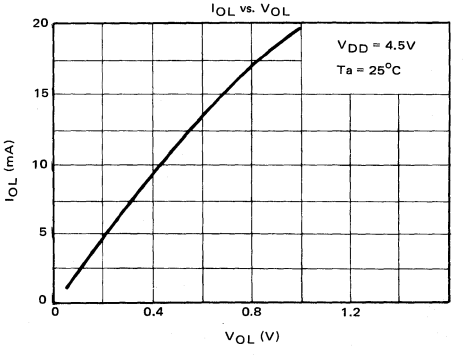



I_{DDS1} vs. V_{IN} ($\overline{CE}_2$)
V_{DD} = 5.5V
other inputs
= 0.8 ~ 2.2V
Ta = 25°C
I_{DDS1} (mA)
2.0
1.5
1.0
0.5
0
1.0
2.0
3.0
4.0
5.0
V_{IN} ($\overline{CE}_2$) (V)


I_{DDS2} vs. V_{IN} ($\overline{CE}_2$)
V_{DD} = 5.5V
other inputs
= 0.8 ~ 2.2V
Ta = 25°C
I_{DDS2} (nA)
50
30
10
5
3
1
3.0
4.0
5.0
6.0
V_{IN} ($\overline{CE}_2$) (V)

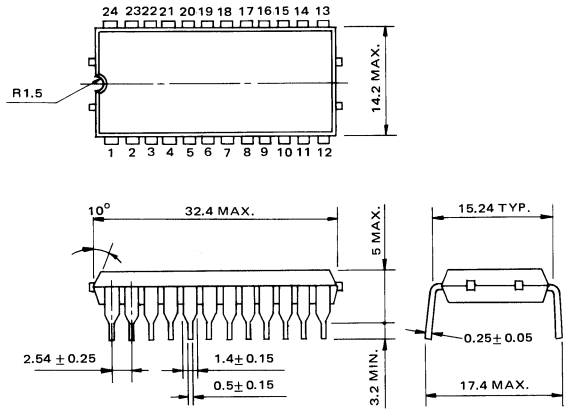

I_{DDS2} vs. Ta
V_{DD} = 5.5V
$\overline{CE}_2$ = 5.0V
I_{DDS2} (nA)
500
300
100
50
30
10
5
3
1
0.5
0.3
0.1
−40
0
40
80
Ta (°C)


I_{OH} vs. V_{OH}
V_{DD} = 4.5
Ta = 25°C
I_{OH} (mA)
−20
−15
−10
−5
0
1.0
2.0
3.0
4.0
V_{OH} (V)

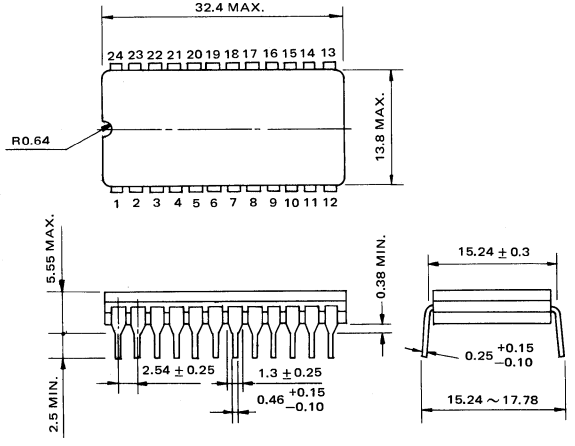

I_{OL} vs. V_{OL}
V_{DD} = 4.5V
Ta = 25°C
I_{OL} (mA)
20
15
10
5
0
0
0.4
0.8
1.2
V_{OL} (V)

OUTLINE DRAWINGS

- **Plastic DIP**

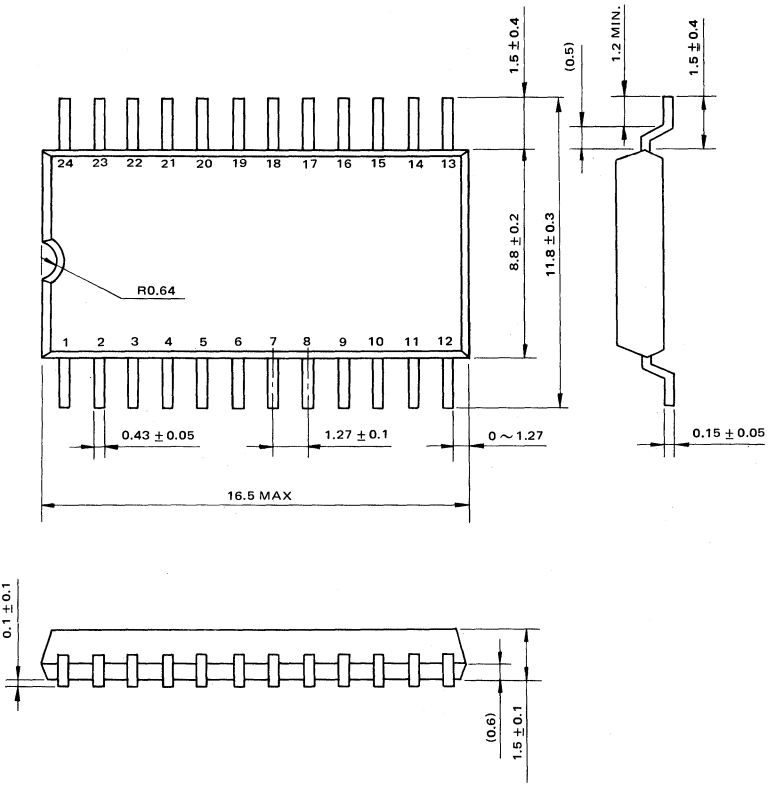


- **Cerdip DIP**



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 24 leads. All dimensions are in millimeters.

- **Plastic FP**



Note: Each lead pitch is 1.27mm.
All leads are located within 0.1mm of their true longitudinal position with respect to No. 1 and No. 24 leads.

PACKAGE INFORMATION FOR FLAT PACKAGE

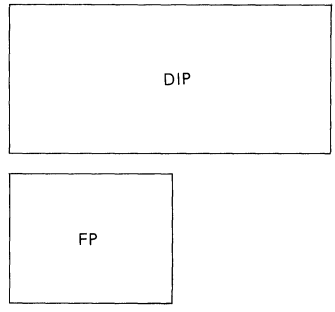
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit : mm

	Flat package	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	1.6	5

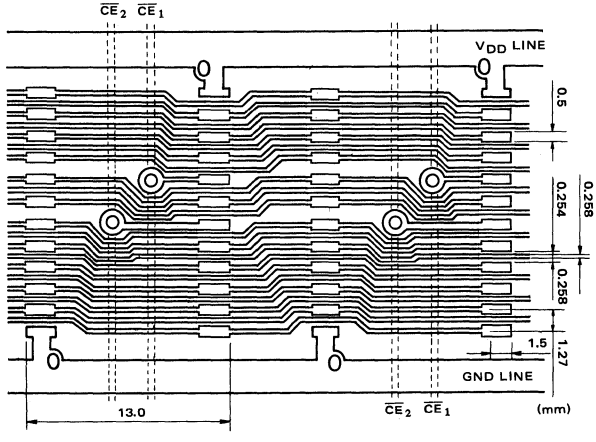
2. Comparison in occupied space.



3. Advantage of this package

- Small dimensions
- Capability of High Density Assembly
- Capability of thin Assembly — Capability of Assembly on both side of PC board.

4. PC pattern layout example



2048 WORD x 8 BIT CMOS STATIC RAM

SILICON GATE CMOS

TC5517AP/-2, TC5517APL/-2
TC5517AD/-2, TC5517ADL/-2
TC5517AF/-2, TC5517AFL/-2

DESCRIPTION

The TC5517AP/AD/AF is a 16384-bit static random access memory organized as 2048 words by 8 bits using CMOS technology, and operates from a single 5 volt supply.

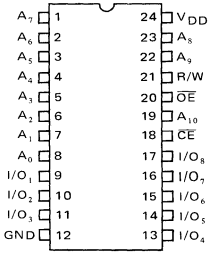
The TC5517AP/AD/AF is featured by output enable and chip enable inputs, that is, $\overline{OE}$ for fast memory access and $\overline{CE}$ for a minimum standby current mode, and is suited for low power application where battery operation or battery back up for non-volatility are required. Furthermore the TC5517APL/ADL/AFL guaranteed a standby current equal to or less than 1μA at 60°C ambient temperature is available.

The TC5517AP/AD is also featured by pin compatibility with 2716 type EPROM. This means that the TC5517AP/AD and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM obtained as a result allows the wide application in microcomputer system.

FEATURES

- Standby Current
  - 0.2μA (Max.) at Ta = 25°C } TC5517APL/
  - 1.0μA (Max.) at Ta = 60°C } ADL/AFL
  - 1.0μA (Max.) at Ta = 25°C } TC5517AP/
  - 5.0μA (Max.) at Ta = 60°C } AD/AF
- Low Power Dissipation : 200mW (Typ.) operating
- Single 5V Power Supply : 5V ± 10%
- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Fully Static Operation
- Access Time
  - 250ns (Max.) : TC5517AP/APL/AD/ADL/AF/AFL
  - 200ns (Max.) : TC5517AP-2/APL-2/AD-2/ADL-2/AF-2/AFL-2
- Two Control Input ($\overline{CE}$, $\overline{OE}$)
- Pin Compatible with Nch Static RAM TMM2016P
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package
  - Plastic DIP : TC5517AP/APL
  - Cerdip DIP : TC5517AD/ADL
  - Plastic FP : TC5517AF/AFL

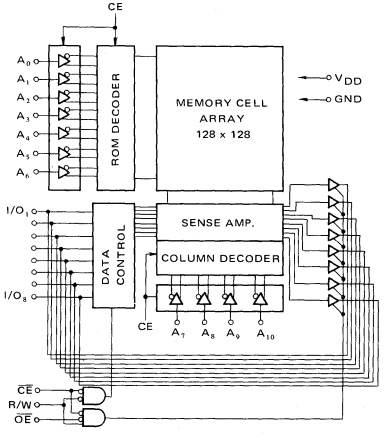
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_{10}$	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	-0.3V ~ 7.0V
V_{IN}	Input Voltage	-0.3V ~ V_{DD}+0.3V
$V_{I/O}$	Input/Output Voltage	-0.3V ~ V_{DD}+0.3V
P_D	Power Dissipation (Ta = 85°C)	0.8W (0.45W)*
T_{STG}	Storage Temperature	-55°C ~ 150°C
T_{OPR}	Operating Temperature	-30°C ~ 85°C
T_{SOLDER}	Soldering Temperature • Time	260°C • 10 sec.

*Plastic FP

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = -30°C ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	–	0.8	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

D.C. CHARACTERISTICS (Ta = -30°C ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$0 \leqq V_{IN} \leqq V_{DD}$			–	–	±1.0	μA
I_{LO}	I/O Leakage Current	$\overline{CE} = V_{IH}$, $0V \leqq V_{I/O} \leqq V_{DD}$			–	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	-2.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.0	3.0	–	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = 2.2V			–	1.0	3.0	mA
I_{DDS2}		$\overline{CE} = V_{DD}$ - 0.5V V_{DD} = 2 ~ 5.5V	TC5517APL/ ADL/AFL	Ta = 25°C	–	–	0.2	μA
				Ta = 60°C	–	–	1.0	
			TC5517AP/ AD/AF	Ta = 25°C	–	0.05	1.0	
				Ta = 60°C	–	–	5.0	
				Ta = 85°C	–	–	30	
I_{DDO1}	Operating Current	$\overline{CE}$ = 0V, $V_{IN} = V_{IH}/V_{IL}$, I_{OUT} = 0mA			–	40	70	mA
I_{DDO2}		$\overline{CE}$ = 0V, $V_{IN} = V_{DD}$/GND, I_{OUT} = 0mA			–	30	55	

Note : Typical values are at Ta = 25°C, V_{DD} = 5V.

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	–	5	10	pF
$C_{I/O}$	Input/Output Capacitance	–	5	10	pF

Note : This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = -30 ~ 85°C, V_{DD} = 5V ± 10%)

- **Read Cycle**

SYMBOL	PARAMETER	TC5517AP-2/APL-2 TC5517AD-2/ADL-2 TC5517AF-2/AFL-2		TC5517AP/APL TC5517AD/ADL TC5517AF/AFL		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	200	–	250	–	ns
t_{ACC}	Access Time	–	200	–	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	–	100	–	100	ns
t_{CO}	$\overline{CE}$ to Output Valid	–	200	–	250	ns
t_{COE}	$\overline{OE}$ or $\overline{CE}$ to Output Active	10	–	10	–	ns
t_{OD}	Output High-Z from Deselection	–	80	–	80	ns
t_{OH}	Output Hold from Address Change	10	–	10	–	ns

- **Write Cycle**

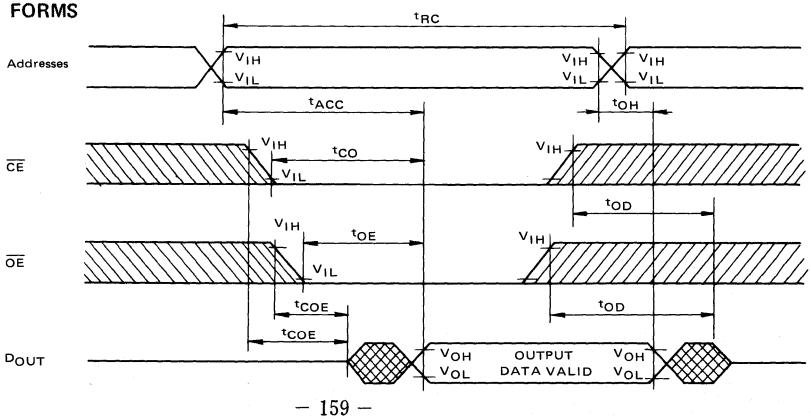
SYMBOL	PARAMETER	TC5517AP-2/APL-2 TC5517AD-2/ADL-2 TC5517AF-2/AFL-2		TC5517AP/APL TC5517AD/ADL TC5517AF/AFL		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	200	–	250	–	ns
t_{WP}	Write Pulse Width	160	–	200	–	ns
t_{AW}	Address Set Up Time	0	–	0	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	ns
t_{ODW}	Output High-Z from R/W	–	80	–	80	ns
t_{OEW}	Output Active from R/W	10	–	10	–	ns
t_{DS}	Data Set Up Time	80	–	120	–	ns
t_{DH}	Data Hold Time	0	–	0	–	ns

A.C. TEST CONDITIONS

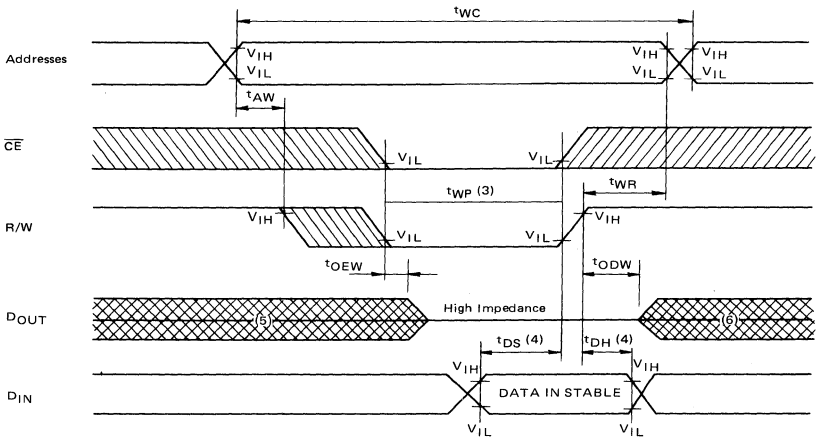
Output Load : 100pF + 1TTL Gate
Input Pulse Levels : 0.6V, 2.4V
Timing Measurement Reference Levels
Input : 0.8V and 2.2V
Output : 0.8V and 2.2V
Input Pulse Rise and Fall Times : 10ns

TIMING WAVE FORMS

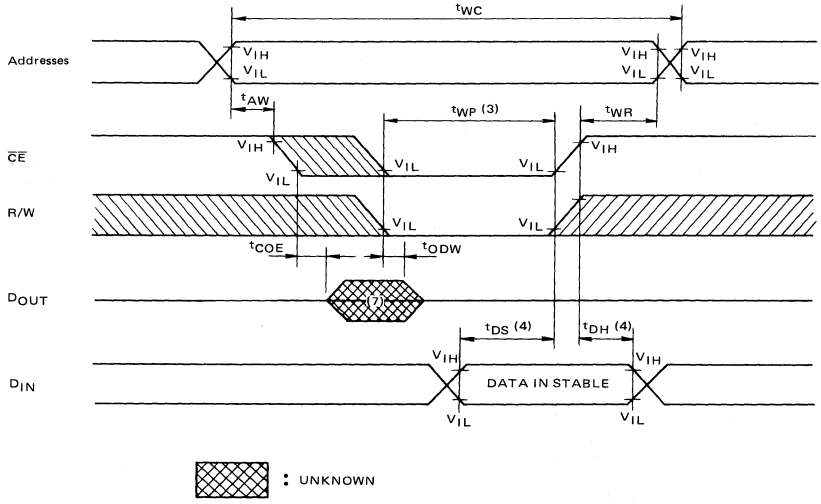
- **Read Cycle (1)**



- **Write Cycle 1 (1)**



- **Write Cycle 2 (2)**

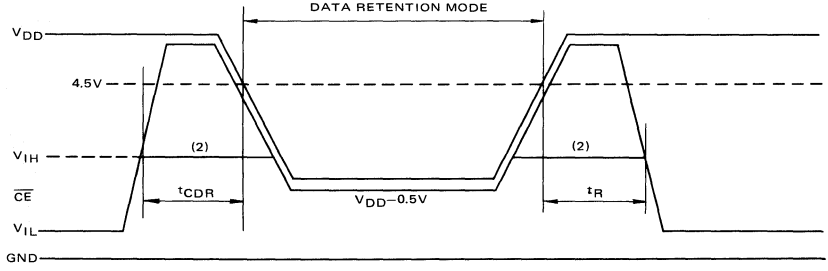


NOTE: (1) R/W is high for a Read Cycle.
(2) $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
(3) t_{WP} is specified as the logical "AND" of $\overline{CE}$ and R/W.
t_{WP} is measured from the latter of $\overline{CE}$ of R/W going low to the earlier of $\overline{CE}$ or R/W going high.
(4) t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ of R/W going high.
(5) If the $\overline{CE}$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(6) If the $\overline{CE}$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(7) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.

DATA RETENTION CHARACTERISTICS (Ta = -30 ~ 85°C)

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DR}	Data Retention Power Supply Voltage			2.0	–	5.5	V
I_{DDS2}	Standby Current	TC5517APL/ ADL/AFL	Ta = 25°C	–	–	0.2	μA
			Ta = 60°C	–	–	1.0	
		TC5517AP/ AD/AF	Ta = 25°	–	0.05	1.0	
			Ta = 60°C	–	–	5.0	
			Ta = 85°C	–	–	30	
t_{CDR}	From Chip Deselection to Data Retention Mode			0	–	–	μs
t_R	Recovery Time			t_{RC}(1)	–	–	μs

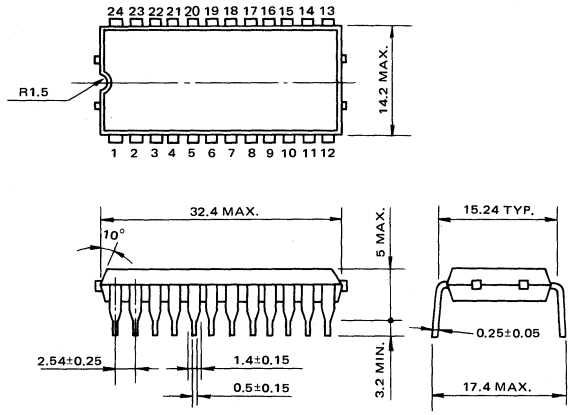
Note (1) t_{RC} : Read Cycle Time



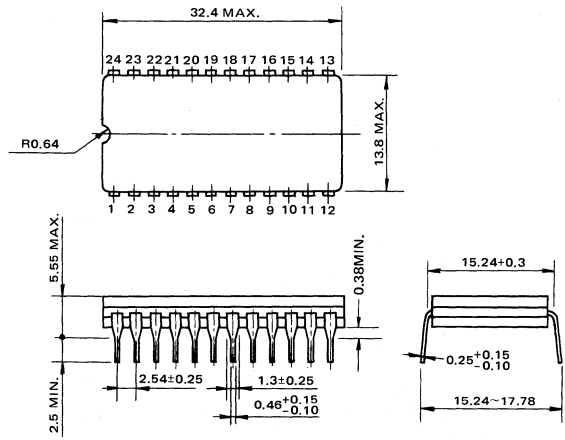
Note (2) If the V_{IH} level of $\overline{CE}$ is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{DDS1} current flows.

OUTLINE DRAWINGS

- **Plastic DIP**

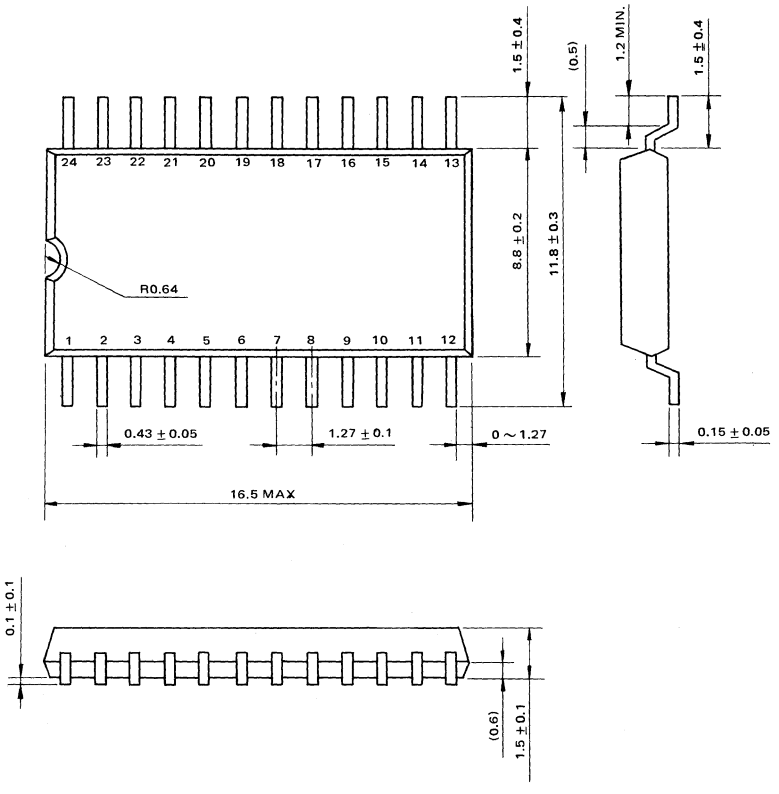


- **Cerdip DIP**



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 24 leads. All dimensions are in millimeters.

- **Plastic FP**



Note: Each lead pitch is 1.27 mm.
All leads are located within 0.1 mm of their true longitudinal position with respect to No. 1 and No. 24 leads.

PACKAGE INFORMATION FOR FLAT PACKAGE

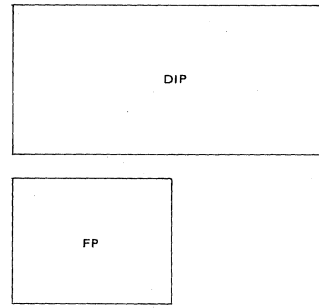
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit: mm

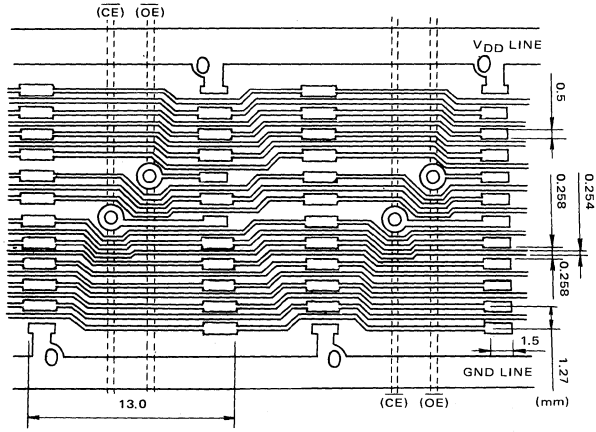
	Flat package	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	1.6	5

2. Comparison in occupied space



3. Advantage of this package
   Small dimensions
   Capability of High Density Assembly
   Capability of thin Assembly——Capability of Assembly on both side of PC board.

4. PC pattern layout example



2048 WORD x 8 BIT CMOS STATIC RAM

SILICON GATE CMOS

TC5517BP-20, TC5517BPL-20
TC5517BD-20, TC5517BDL-20
TC5517BF-20, TC5517BFL-20

DESCRIPTION

The TC5517BP/BD/BF is a 16384-bit high speed and low power fully static random access memory organized as 2048 words by 8 bits using CMOS technology, and operates from a single 5 volt supply.

The TC5517BP/BD/BF has a output enable input ($\overline{OE}$) for fast memory access and output control and chip enable input ($\overline{CE}$) which is used for device selection and can be used in order to achieve the minimum standby current mode easily for battery back up.

Also the high speed and low power characteristics which maximum access time is 200ns and maximum operating current is 5mA/MHz are achieved.

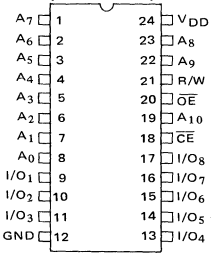
Thus the TC5517BP/BD/BF is most suitable for use in low power applications where battery operation or battery back up for nonvolatility are required. Furthermore the TC5517BPL/BDL/BFL guaranteed a standby current equal to or less than 1μA at 60°C ambient temperature available.

And the TC5517BP/BD/BF is pin compatible with 2716 type EPROM. This means that the TC5517BP/BD/BF and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM allows the wide application in microcomputer system.

FEATURES

- Low Power Dissipation
  27.5mW/MHz (Max.) Operating
- Standby Current
  0.2μA (Max.) at Ta = 25°C } TC5517BPL/
  1.0μA (Max.) at Ta = 60°C } BDL/BFL-20
  1.0μA (Max.) at Ta = 25°C } TC5517BP/BD/
  5.0μA (Max.) at Ta = 60°C } BF-20
- Single 5V Power Supply : 5V±10%
- Data Retention Supply Voltage 2.0 ~ 5.5V
- Fully Static Operation
- Fast Access Time
  t_{ACC} = 200ns (Max.)
  t_{OE} = 70ns (Max.)
- Output Buffer Control : $\overline{OE}$
- On-chip Address Transition Detector
- All inputs and outputs Directly TTL Compatible
- Three State Outputs
- Package
  Plastic DIP : TC5517BP/BPL
  Cerdip DIP : TC5517BD/BDL
  Plastic FP : TC5517BF/BFL

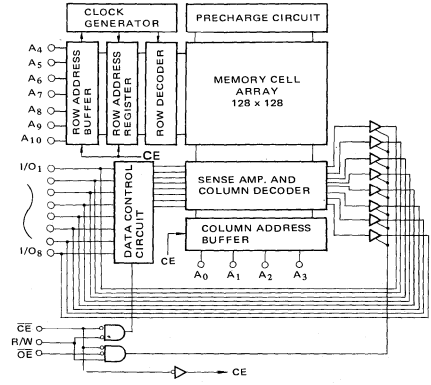
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_{10}$	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{CE}$	$\overline{OE}$	R/W	$A_0 \sim A_{10}$	$I/O_1 \sim _8$	POWER
Read	L	L	H	Stable	Data Out	I_{DDO}
Write	L	*	L	Stable	Data In	I_{DDO}
Output Deselect	*	H	*	*	High Impedance	I_{DDO}
**Standby	H	*	*	*	High Impedance	I_{DDS}

Note: *: H or L **: Data Retention Mode

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	−0.3V ~ 7.0V
V_{IN}	Input Voltage	−0.3V ~ V_{DD} + 0.3V
$V_{I/O}$	Input/Output Voltage	−0.3V ~ V_{DD} + 0.3V
P_D	Power Dissipation (Ta = 85°C)	0.8W (0.45W) *
T_{STG}	Storage Temperature	−55°C ~ 150°C
T_{OPR}	Operating Temperature	−30°C ~ 85°C
T_{SOLDER}	Soldering Temperature · Time	260 °C · 10 sec.

* Plastic FP = 0.45W

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = −30°C ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

D.C. CHARACTERISTICS (Ta = −30°C ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$0 \leqq V_{IN} \leqq V_{DD}$			–	–	±1.0	μA
I_{LO}	I/O Leakage Current	$\overline{CE} = V_{IH}$, $0V \leqq V_{I/O} \leqq V_{DD}$			–	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−1.0	−2.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.0	3.0	–	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = 2.2V			–	1.0	3.0	mA
I_{DDS2}		$\overline{CE} \geqq V_{DD}$ −0.5V V_{DD} = 2 ~ 5.5V	TC5517BPL /BDL/BFL-20	Ta=25°C	–	–	0.2	μA
				Ta=60°C	–	–	1.0	
			TC5517BP/ BD/BF-20	Ta=25°C	–	0.05	1.0	
				Ta=60°C	–	–	5.0	
				Ta=85°C	–	–	30	
I_{DDO1}	Operating Current	t_{cycle} = 200ns $\overline{CE}$ = OV, I_{OUT} = 0mA	$V_{IN} = V_{IH}/V_{IL}$		–	–	30	mA
I_{DDO2}			$V_{IN} = V_{DD}$/GND		–	–	25	
I_{DDO3}		$t_{cycle} \geqq 1\mu s$ $\overline{CE}$ = OV, I_{OUT} = 0mA	$V_{IN} = V_{IH}/V_{IL}$		–	–	10	
I_{DDO4}			$V_{IN} = V_{DD}$/GND		–	–	5	

Note: Typical Values are at Ta = 25°C, V_{DD} = 5V.

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMTER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	–	5	10	pF
$C_{I/O}$	Input/Output Capacitance	–	5	10	pF

Note: This paramter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = −30 ~ 85°C, V_{DD} = 5V ± 10%)

- **Read Cycle**

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	200	–	ns
t_{ACC}	Access Time	–	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	–	70	ns
t_{CO}	$\overline{CE}$ to Output Valid	–	200	ns
t_{COE}	$\overline{OE}$ or $\overline{CE}$ to Output Active	10	–	ns
t_{OD}	Output High-Z from Deselection	–	60	ns
t_{OH}	Output Hold from Address Change	10	–	ns

- **Write Cycle**

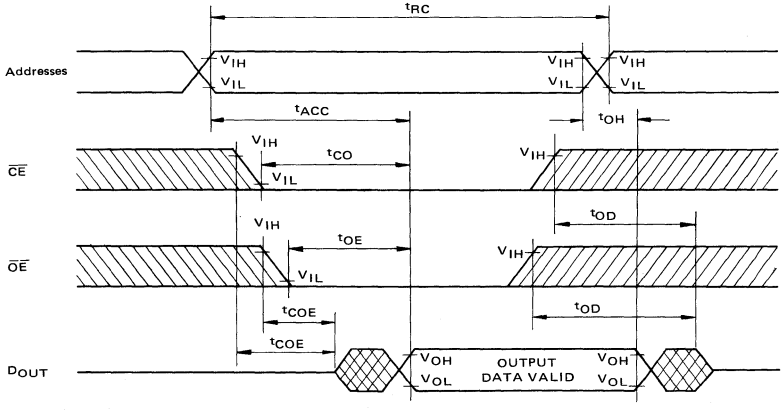
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	200	–	ns
t_{WP}	Write Pulse Width	150	–	ns
t_{AW}	Address Set up Time	0	–	ns
t_{WR}	Write Recovery Time	0	–	ns
t_{ODW}	Output High-Z from R/W	–	60	ns
t_{OEW}	Output Active from R/W	10	–	ns
t_{DS}	Data Set up time	90	–	ns
t_{DH}	Data Hold Time	0	–	ns

A.C. TEST CONDITIONS

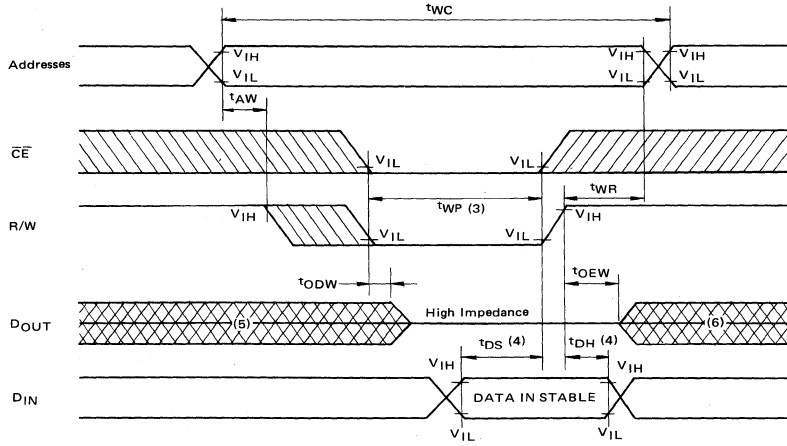
Output Load : 100pF + 1TTL Gate
Input Pulse Levels : 0.6V, 2.4V
Timing Measurement Reference Levels
Input : 0.8V and 2.2V
Output : 0.8V and 2.2V
Input Pulse Rise and Fall Times : 10ns

TIMING WAVEFORMS

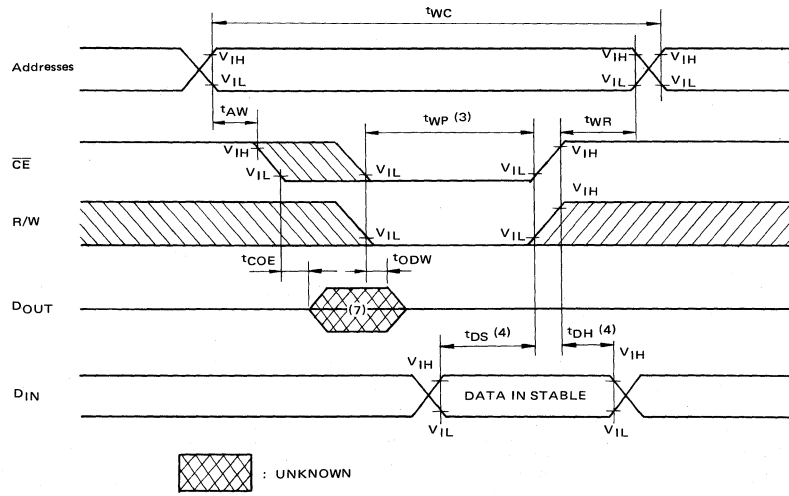
- **Read Cycle (1)**



- **Write Cycle 1 (2)**



- **Write Cycle 2 (2)**

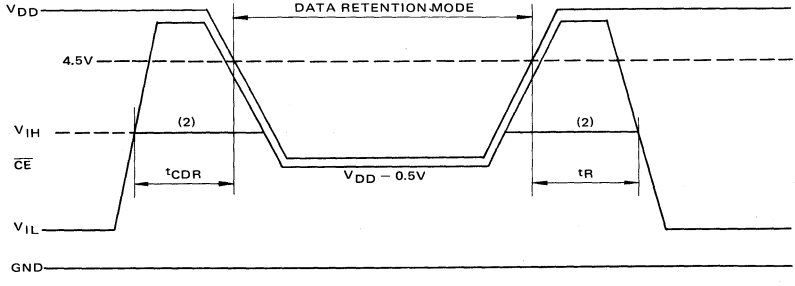


Note: (1) R/W is high for a Read Cycle.
(2) $\overline{OE}$ = V_{IH} or V_{IL}. If, $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
(3) t_{WP} is specified as the logical "AND" of $\overline{CE}$ and R/W.
t_{WP} is measured from the latter of $\overline{CE}$ or R/W going low to the earlier of $\overline{CE}$ or R/W going high.
(4) t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or R/W going high.
(5) If the $\overline{CE}$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(6) If the $\overline{CE}$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(7) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.

DATA RETENTION CHARACTERISTICS (Ta = −30 ~ 85°C)

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DR}	Data Retention Power Supply Voltage			2.0	–	5.5	V
I_{DDS2}	Standby Current	TC5517BPL/ BDL/BFL-20	Ta=25°C	–	–	0.2	μA
			Ta=60°C	–	–	1.0	
		TC5517BP/ BD/BF-20	Ta=25°C	–	0.05	1.0	
			Ta=60°C	–	–	5.0	
			Ta=85°C	–	–	30	
t_{CDR}	From Chip Deselection to Data Retention Mode			0	–	–	μs
t_R	Recovery Time			t_{RC}(1)	–	–	μs

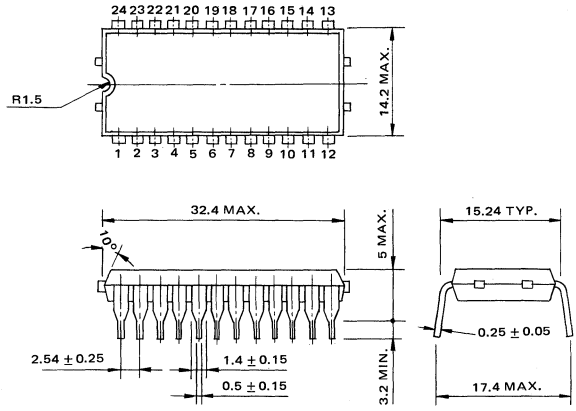
Note (1) t_{RC} : Read Cycle Time



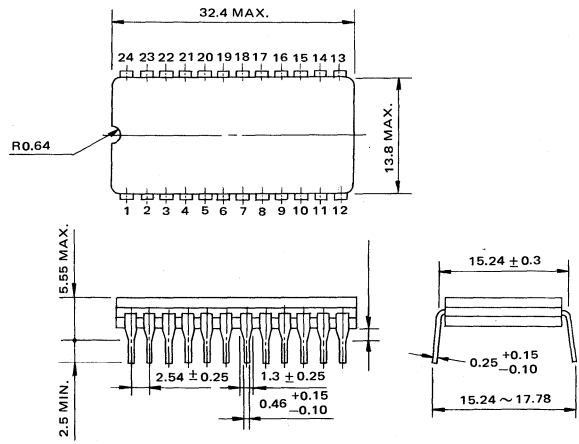
Note (2) If the V_{IH} level of $\overline{CE}$ is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{DDS1} current flows.

OUTLINE DRAWINGS

- Plastic DIP



- Cerdip DIP



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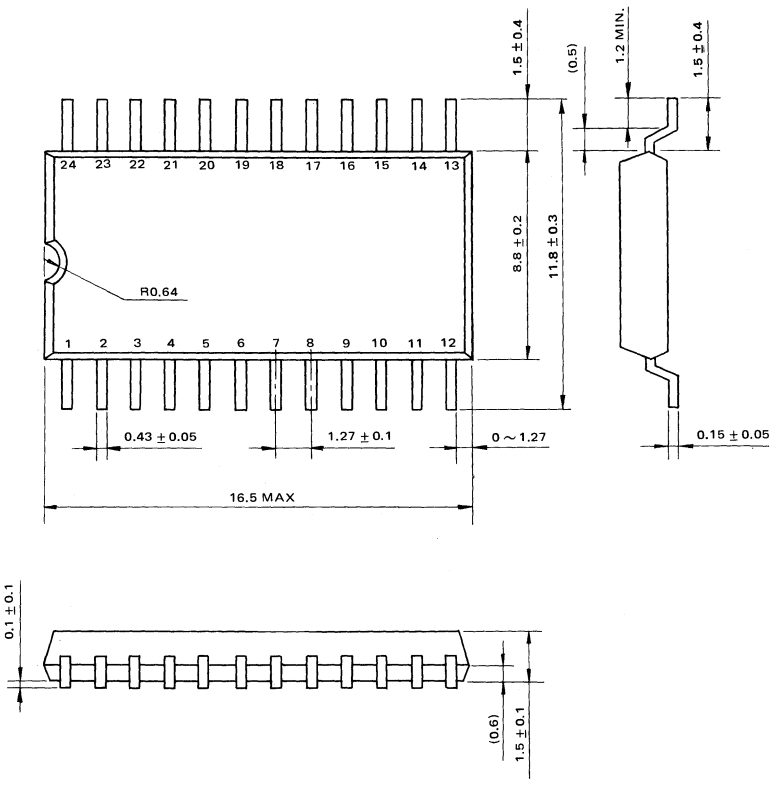

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PACKAGE INFORMATION FOR FLAT PACKAGE

This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit :mm

	Flat package	Standard package
Length	16.5	32.4
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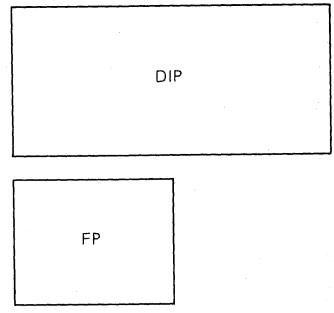
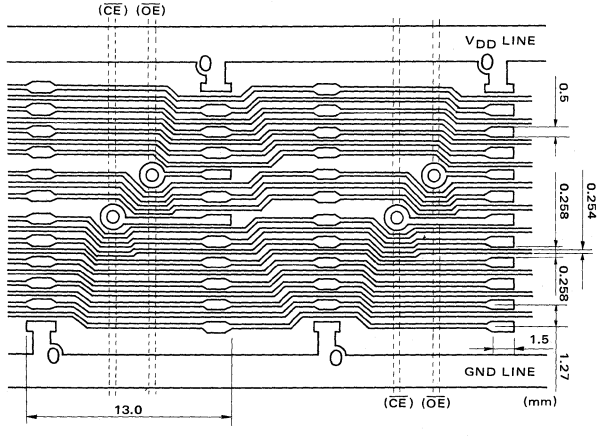


3. Advantage of this package
   Small dimensions
   Capability of High Density Assembly
   Capability of thin Assembly —— Capability of Assembly on both side of PC board.

4. PC pattern layout example



Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCTS

2048 WORD x 8 BIT CMOS STATIC RAM

SILICON GATE CMOS

TC5518BP-20, TC5518BPL-20
TC5518BD-20, TC5518BDL-20
TC5518BF-20, TC5518BFL-20

DESCRIPTION

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Thus the TC5518BP/BD/BF is most suitable for use in low power applications where battery operation or battery back up for nonvolatility are required. Furthermore the TC5518BPL/ BDL/BFL guaranteed a standby current equal to or less than 1μA at 60°C ambient temperature available.

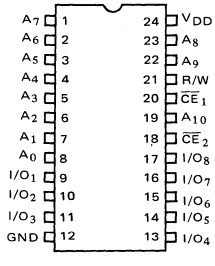
And the TC5518BP/BD/BF is pin compatible with 2716 type EPROM. This means that the TC5518BP/ BD/BF and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM allows the wide application in microcomputer system.

FEATURES

- Low Power Dissipation
  27.5mW/MHz (Max.) Operating
- Standby Current
  0.2μA (Max.) at Ta = 25°C } TC5518BPL/
  1.0μA (Max.) at Ta = 60°C } BDL/BFL-20
  1.0μA (Max.) at Ta = 25°C } TC5518BP/BD/
  5.0μA (Max.) at Ta = 60°C } BF-20
- Single 5V Power Supply: 5V±10%
- Data Retention Supply Voltage
  2.0 ~ 5.5V
- Fully Static Operation
- Fast Access Time
  t_{ACC} = 200ns (Max.)
- Two Chip Enables ($\overline{CE}_1$, $\overline{CE}_2$) for Simple Memory Expansion and Battery Back Up
- On-chip Address Transition Detector
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package
  Plastic DIP : TC5518BP/BPL
  Cerdip DIP : TC5518BD/BDL
  Platic FP : TC5518BF/BFL

PIN CONNECTION

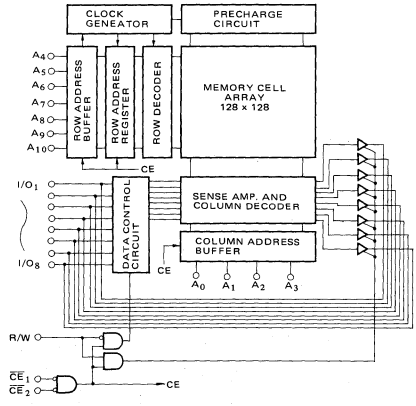
(Top VIEW)



PIN NAMES

$A_0 \sim A_{10}$	Address Inputs
R/W	Read/Write Control Input
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enable Inputs
$I/O_1 \sim I/O_8$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{CE}_2$	$\overline{CE}_1$	R/W	$A_0 \sim A_{10}$	$I/O_1 \sim _8$	POWER
Read	L	L	H	Stable	Data Out	I_{DDO}
Write	L	L	L	Stable	Data In	I_{DDO}
** Standby 1	*	H	*	*	High Impedance	I_{DDS}
** Standby 2	H	*	*	*	High Impedance	I_{DDS}

Note; *: H or L **: Data Retention Mode

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	−0.3V ~ 7.0V
V_{IN}	Input Voltage	−0.3V ~ V_{DD}+0.3V
$V_{I/O}$	Input/Output Voltage	−0.3V ~ V_{DD}+0.3V
P_D	Power Dissipation (Ta = 85°C)	0.8W (0.45W)*
T_{STG}	Storage Temperature	−55°C ~ 150°C
T_{OPR}	Operating Temperature	−30°C ~ 85°C
T_{SOLDER}	Soldering Temperature · Time	260°C · 10 sec

*: Plastic FP = 0.45W

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = −30°C ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

D.C. CHARACTERISTICS (Ta = −30°C ~ 85°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$0 \leqq V_{IN} \leqq V_{DD}$			–	–	±1.0	μA
I_{LO}	I/O Leakage Current	$\overline{CE}_2 = V_{IH}$, $OV \leqq V_{I/O} \leqq V_{DD}$			–	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−1.0	−2.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.0	3.0	–	mA
I_{DDS1}	Standby Current	$\overline{CE}_2$ = 2.2V or $\overline{CE}_1$ = 2.2V			–	1.0	3.0	mA
I_{DDS2}		$\overline{CE}_2 \geqq V_{DD}$ −0.5V or $\overline{CE}_1 \leqq V_{DD}$ −0.5V, V_{DD} = 2 ~ 5.5V	TC5518BPL /BDL/BFL-20	Ta=25°C	–	–	0.2	mA
				Ta=60°C	–	–	1.0	μA
			TC5518BP/ BD/BF-20	Ta=25°C	–	0.05	1.0	
				Ta=60°C	–	–	5.0	
				Ta=85°C	–	–	30	
I_{DDO1}	Operating Current	t_{cycle} = 200ns, $\overline{CE}_1$ =	$V_{IN} = V_{IH}/V_{IL}$		–	–	30	mA
I_{DDO2}		$\overline{CE}_2$ = OV, I_{OUT} = 0mA	$V_{IN} = V_{DD}/GND$		–	–	25	
I_{DDO3}		t_{cycle} = 1μs, $\overline{CE}_1$ =	$V_{IN} = V_{IH}/V_{IL}$		–	–	10	
I_{DDO4}		$\overline{CE}_2$ = OV, I_{OUT} = 0mA	$V_{IN} = V_{DD}/GND$		–	–	5	

Note: Typical Values are at Ta = 25°C, V_{DD} = 5V

CAPACITANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	–	5	10	pF
$C_{I/O}$	Input/Output Capacitance	–	5	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = –30 ~ 85°C, V_{DD} = 5V ± 10%)

Read Cycle

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{RC}	Read Cycle Time	200	–	–	ns
t_{ACC}	Access Time	–	–	200	ns
t_{CO1}	$\overline{CE}_1$ to Output Valid	–	–	200	ns
t_{CO2}	$\overline{CE}_2$ to Output Valid	–	–	200	ns
t_{COE}	$\overline{CE}_1$ or $\overline{CE}_2$ to Output Active	10	–	–	ns
t_{OD}	Output High-Z from Deselection	–	–	60	ns
t_{OH}	Output Hold from Address Change	20	–	–	ns

Write Cycle

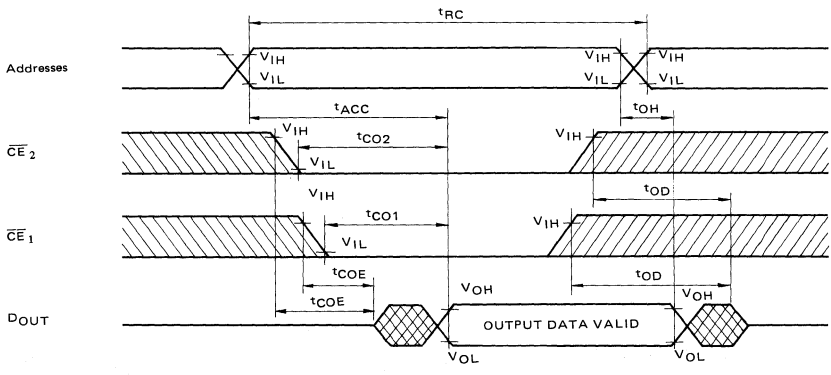
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{WC}	Write Cycle Time	200	–	–	ns
t_{WP}	Write Pulse Width	150	–	–	ns
t_{AW}	Address Set up Time	0	–	–	ns
t_{WR}	Write Recover Time	0	–	–	ns
t_{ODW}	Output High-Z from R/W	–	–	60	ns
t_{OEW}	Output Active from R/W	10	–	–	ns
t_{DS}	Data Set up Time	90	–	–	ns
t_{DH}	Data Hold Time	0	–	–	ns

A.C. TEST CONDITIONS

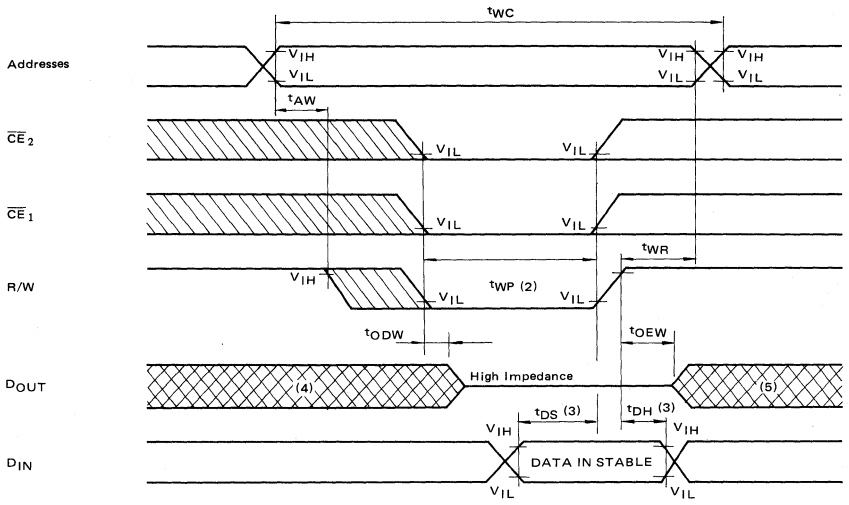
Output Load : 100pF + 1TTL Gate
Input Pulse Levels : 0.6V, 2.4V
Timing Mesurement Reference Levels
Input : 0.8V and 2.2V
Output : 0.8V and 2.2V
Input Pulse Rise and Fall Times : 10 ns

TIMING WAVEFORMS

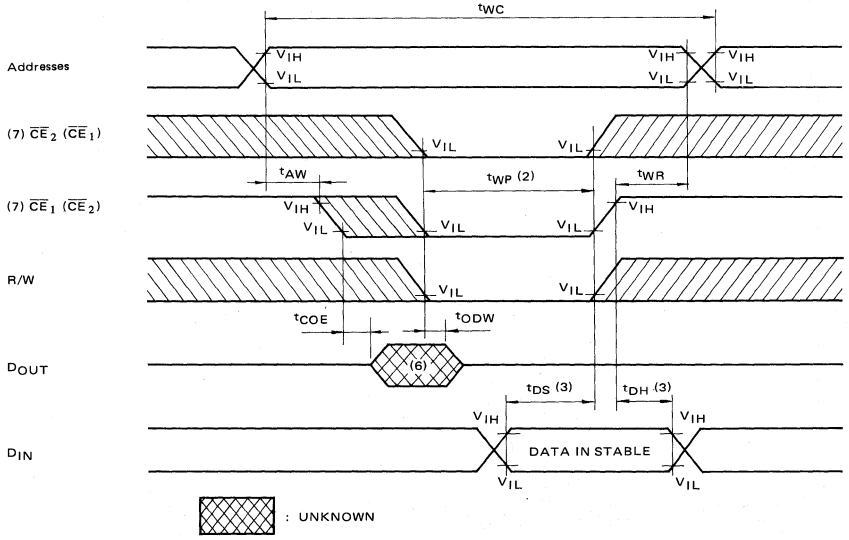
Read Cycle (1)



Write Cycle 1.



Write Cycle 2.



Note: (1) R/W is high for a Read Cycle.

(2) t_{WP} is specified as the logical "AND" or $\overline{CE}1$, $\overline{CE}2$ and R/W.
t_{WP} is measured from the latter of $\overline{CE}1$, $\overline{CE}2$ or R/W going low to the earlier of $\overline{CE}1$, $\overline{CE}2$ or R/W going high.

(3) t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}1$, $\overline{CE}2$ or R/W going high.

(4) If the $\overline{CE}1$, or $\overline{CE}2$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.

(5) If the $\overline{CE}1$ or $\overline{CE}2$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.

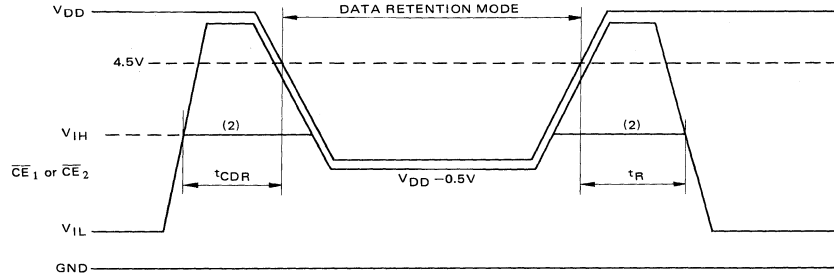
(6) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE}1$ or $\overline{CE}2$ low transition, the output buffers remain in a high impedance state in this period.

(7) A write occurs during the overlap of a low $\overline{CE}1$, low $\overline{CE}2$ and low R/W.
In write cycle 2, write is controlled by either $\overline{CE}1$ or $\overline{CE}2$.

DATA RETENSION CHARACTERISTICS (Ta = –30 ~ 85°C)

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DR}	Data Retention Power Supply Voltage			2.0	–	5.5	V
I_{DDS2}	Standby Current	TC5518BPL/ BDL/BFL-20	Ta = 25°C	–	–	0.2	μA
			Ta = 60°C	–	–	1.0	
		TC5518BP/ BD/BF-20	Ta = 25°C	–	0.05	1.0	
			Ta = 60°C	–	–	5.0	
			Ta = 85°C	–	–	30	
t_{CDR}	From Chip Deselection to Data Retention Mode			0	–	–	μs
t_R	Recover Time			t_{RC}(1)	–	–	μs

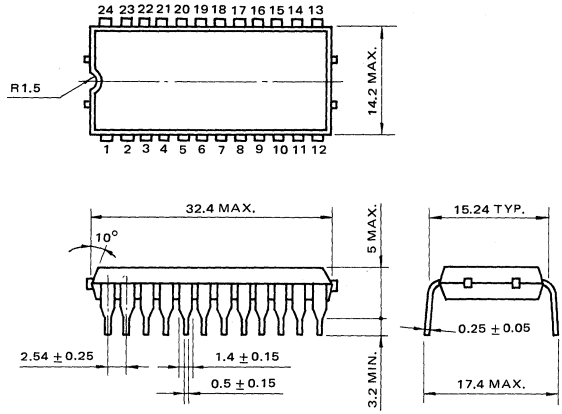
Note (1) t_{RC} : Read Cycle Time



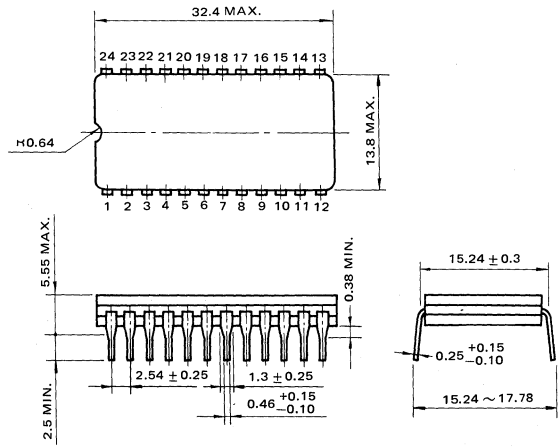
Note (2) if the V_{IH} level of $\overline{CE}_2$ ($\overline{CE}_1$) is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{DDS1} current flows.

OUTLINE DRAWINGS

- **Plastic DIP**

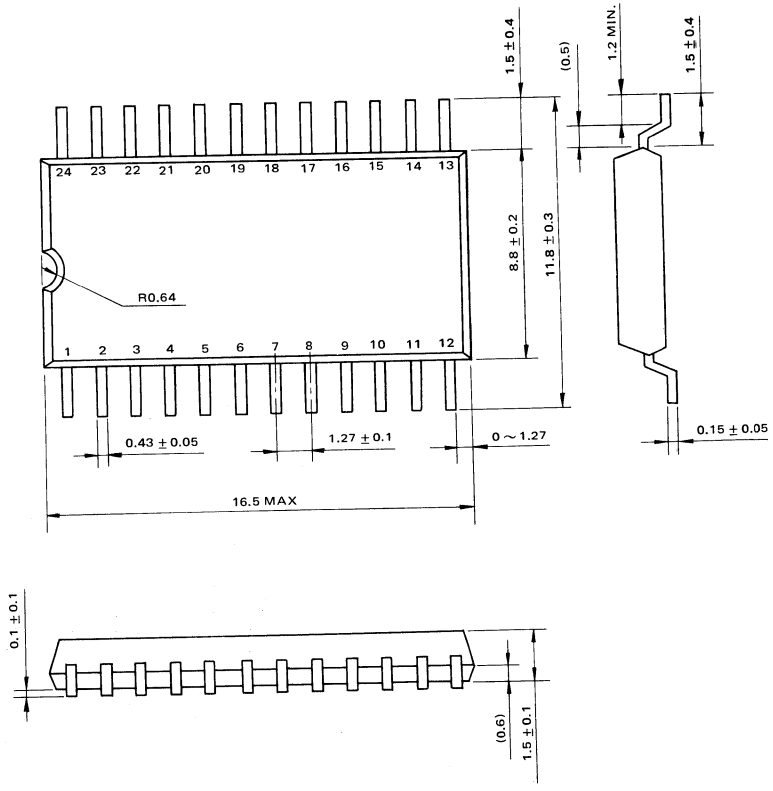


- **Cerdip DIP**



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudianl position with respect to No. 1 and No.24 leads. All dimensions are in millimeters.

- **Plastic FP**



Note: Each lead pitch is 1.27mm.
All leads are located within 0.1mm of their true longitudinal position with respect to No. 1 and No. 24 leads.

PACKAGE INFORMATION FOR FLAT PACKAGE

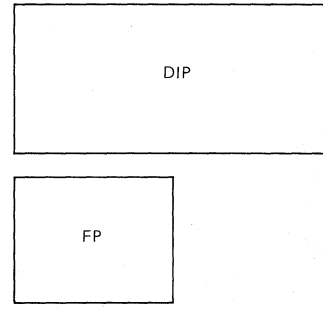
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit : mm

	Flat package	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	1.6	5

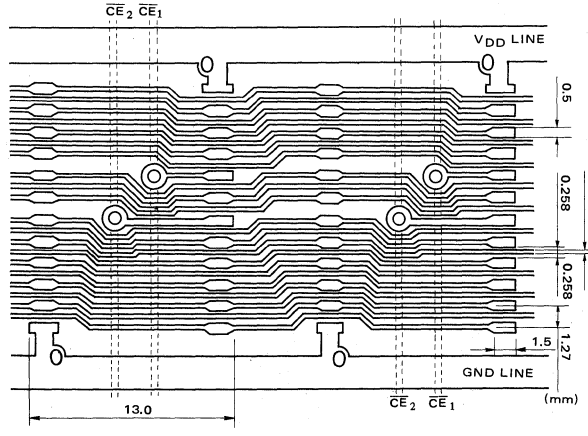
2. Comparison in occupied space



3. Advantage of this package

Small dimensions
Capability of High Density Assembly
Capability of thin Assembly — Capability of Assembly on both side of PC board.

4. PC pattern layout example



Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

Distributed by

8192 WORD x 8 BIT CMOS RAM

SILICON GATE CMOS

TC5564P-10/P-15
TC5564PL-10/PL-15

DESCRIPTION

The TC5564P is a 65,536-bit high speed static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5-volt supply.

The TC5564P features output enable and chip enable inputs, that is, $\overline{OE}$ for fast memory access and $\overline{CE}_1$, CE_2 for a minimum standby current mode. So it is suited for a high speed, and low power applications where battery operation and/or battery back up for nonvolatility are required. The TC5564P is guaranteed for voltage as low as 2.0 volt. Furthermore the TC5564PL is guranteed a standby current equal to or less than 1 μA at Ta = 60°C ambient temperature available.

The TC5564P also features pincompatibility with the 64K bit EPROM (TMM2764D). This means that the TC5564P and EPROM can be interchanged in the same socket, and flexibility in the definition of the quantity of RAM versus EPROM obtained as a result allows the wide application in microcomputer system.

The TC5564P is moulded in a dual-in-line 28 pin standard plastic package, 0.6 inch width.

FEATURES

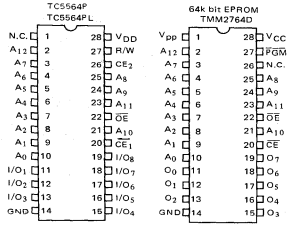
- Low Standby Current
  - 0.2μA (Max.) at Ta = 25°C } TC5564PL-10
  - 1.0μA (Max.) at Ta = 60°C } TC5564PL-15
  - 20 μA (Max.) at Ta = 85°C } TC5564P-10 / TC5564P-15
- Low Power Dissipation
  - 27.5mW/MHz (Max.) Operating
- 5V Single Power Supply
- 8,192 Word x 8 Bit
- Fully Static Operation
- Data Retention Supply Voltage: 2.0 ~ 5.5V

- Access Time

	TC5564P-10 TC5564PL-10	TC5564P-15 TC5564PL-15
Address Access Time (Max.)	100 ns	150 ns
$\overline{CE}_1$ Access Time (Max.)	100 ns	150 ns
CE_2 Access Time (Max.)	100 ns	150 ns
Output Enable Time (Max.)	50 ns	70 ns

- Directly TTL Compatible:
  - All Inputs and Outpus
- Stndard 28 Pin DIP
- Pin Compatible with 2764 type EPROM

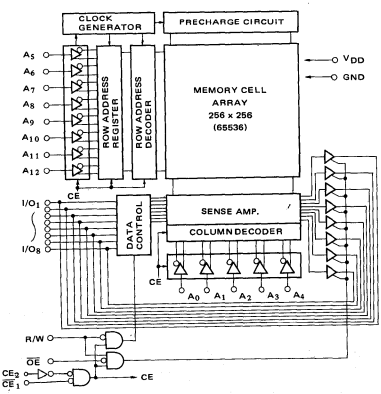
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_{12}$	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}_1$, CE_2	Chip Enable Inputs
$I/O_1 \sim I/O_8$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

Operation Mode	$\overline{CE}_1$	CE_2	$\overline{OE}$	R/W	$I/O_1 \sim I/O_8$	Power
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	*	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	$-0.3 \sim 7.0$	V
V_{IN}	Input Voltage	$-2.0 \sim 7.0$	V
$V_{I/O}$	Input and Output Voltage	$-0.5 \sim V_{DD} + 0.5$	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature	260 · 10	°C · sec
T_{strg}	Storage Temperature	$-55 \sim 150$	°C
$T_{opr.}$	Operating Temperature	$-30 \sim 85$	°C

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} +0.3	V
V_{IL}	Input Low Voltage	−0.5	–	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	V

D.C. and OPERATING CHARACTERISTICS (Ta = −30 ~ 85°C, V_{DD} = 5V ±10% Unless otherwise noted)

SYMBOL		PARAMETER		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$		–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		−1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		4.0	–	–	mA
I_{LO}	Output Leakage Current	$\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$ or R/W = V_{IL} or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$		–	–	±1.0	μA
I_{DDO1}	Operating Current	$\overline{CE}_1 = V_{IL}$ and $CE_2 = V_{IH}$ Other Input = V_{IH}/V_{IL}	t_{cycle} = 1 μs	–	–	10	mA
			t_{cycle} = 100ns	–	–	45	
I_{DDO2}	Operating Current	$\overline{CE}_1$ = 0.2V and $CE_2 = V_{DD} - 0.2V$ Other Input = $V_{DD} - 0.2V/0.2V$	t_{cycle} = 1μs	–	–	5	mA
			t_{cycle} = 100ns	–	–	40	
I_{DDS1}	Standby Current	$\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$		–	–	2	mA
I_{DDS2}	Standby Current	$\overline{CE}_1 = V_{DD} - 0.2V$ or CE_2 = 0.2V V_{DD} = 2.0 ~ 5.5V	TC5564PL-10 Ta = 25°C	–	–	0.2	μA
			TC5564PL-15 Ta = 60°C	–	–	1.0	
			TC5564P-10/TC5564P-15	–	–	20	

Note: In standby mode with $\overline{CE}_1 \geqq V_{DD} - 0.2V$, these specification limits are guaranteed under the condition of $CE_2 \geqq V_{DD} - 0.2V$ or $CE_2 \leqq 0.2V$.

CAPACITANCE (Ta = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note: This prameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = −30 ~ 85°C, V_{DD} = 5V ± 10%)

Read Cycle

SYMBOL	PARAMETER	CONDITIONS	TC5564P-10/PL-10		TC5564P-15/PL-15		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	V_{IN} = 2.4V/0.6V	100	—	150	—	ns
t_{ACC}	Address AccessTime	V_{IH} = 2.2V	—	100	—	150	ns
t_{CO1}	$\overline{CE}_1$ Access Time	V_{IL} = 0.8V	—	100	—	150	ns
t_{CO2}	CE_2 Access Time	t_r, $t_f \leqq$ 5ns	—	100	—	150	ns
t_{OE}	Output Enable to Output in Valid	V_{OH} = 2.2V V_{OL} = 0.8V Output Load: C_L (100pF) and 1-TTL Gate	—	50	—	70	ns
t_{COE}	Chip Enable ($\overline{CE}_1$, CE_2) to Output in Low-Z		10	—	10	—	ns
t_{OEE}	Output Enable to Output in Low-Z		5	—	5	—	ns
t_{OD}	Chip Enable ($\overline{CE}_1$, CE_2) to Output in High-Z		—	50	—	70	ns
t_{ODO}	Output Enable to Output in High-Z		—	40	—	60	ns
t_{OH}	Output Data Hold Time		30	—	30	—	ns

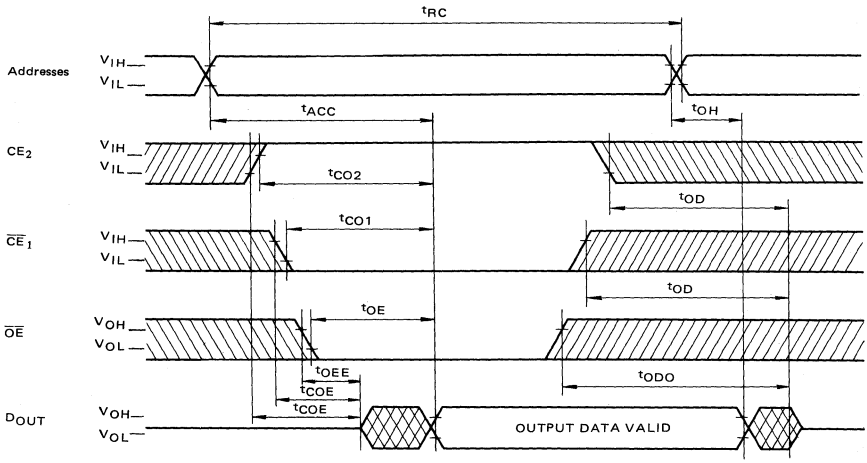
Write Cycle

SYMBOL	PARAMETER	CONDITIONS	TC5564P/PL		TC5564P-1/PL-1		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	V_{IN} = 2.4V/0.6V	100	—	150	—	ns
t_{WP}	Write Pulse Width	V_{IH} = 2.2V	70	—	100	—	ns
t_{CW}	Chip Selection to End of Write	V_{IL} = 0.8V t_r, $t_f \leqq$ 5ns	90	—	120	—	ns
t_{AW}	Address Set up Time		0	—	0	—	ns
t_{WR}	Write Recovery Time		0	—	0	—	ns
t_{ODW}	R/W to Output High-Z		—	50	—	70	ns
t_{OEW}	R/W to Output Low-Z		10	—	10	—	ns
t_{DS}	Data Set up Time		40	—	60	—	ns
t_{DH}	Data Hold Time		0	—	0	—	ns

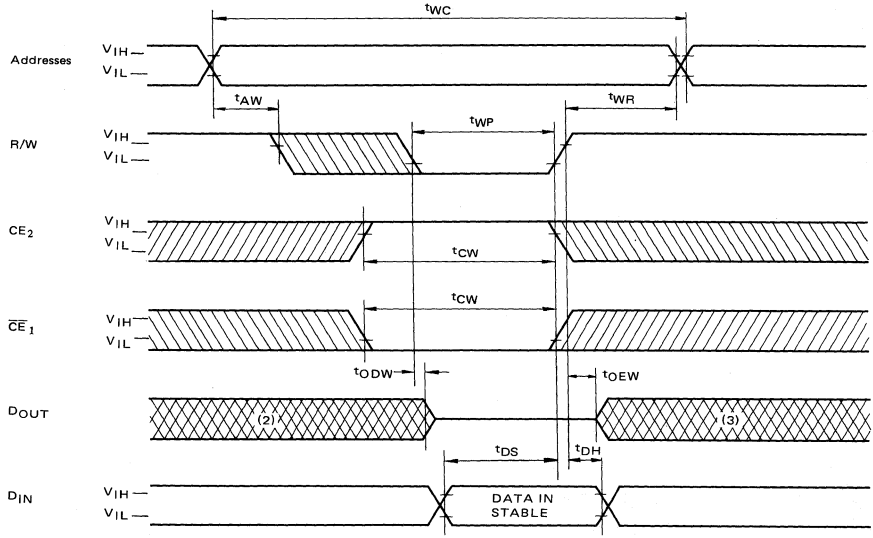
Note: Input Pulse Levels = V_{IN}
Timing Measurement Reference Levels = V_{IH}, V_{IL}

TIMING WAVEFORMS

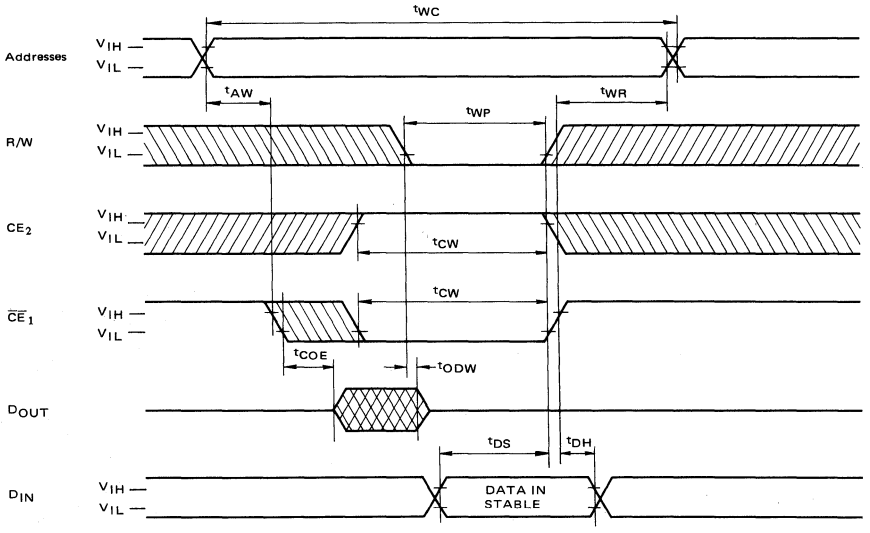
READ CYCLE (1)



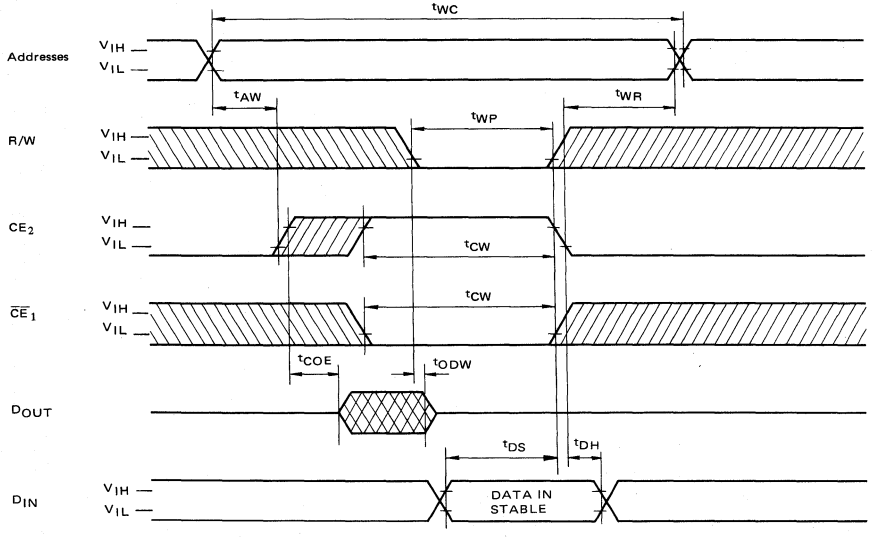
WRITE CYCLE 1 (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE}_1$ Controlled Write)



WRITE CYCLE 3 (4) (CE_2 Controlled Write)



NOTE:

(1) R/W is High for Read Cycle.

(2) Assuming that $\overline{CE}_1$ Low transition or CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

(3) Assuming that $\overline{CE}_1$ High transition or CE_2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.

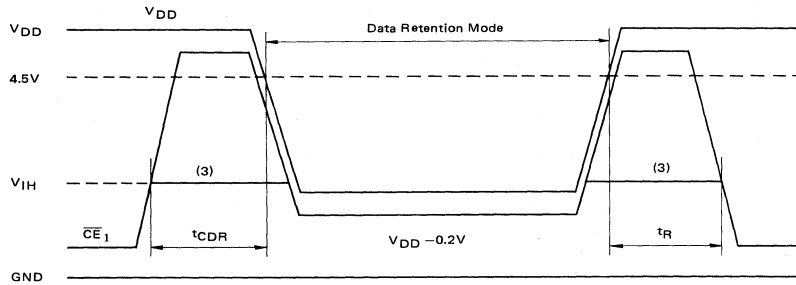
(4) Assuming that $\overline{OE}$ is High for Write cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta = –30 ~ 85°C)

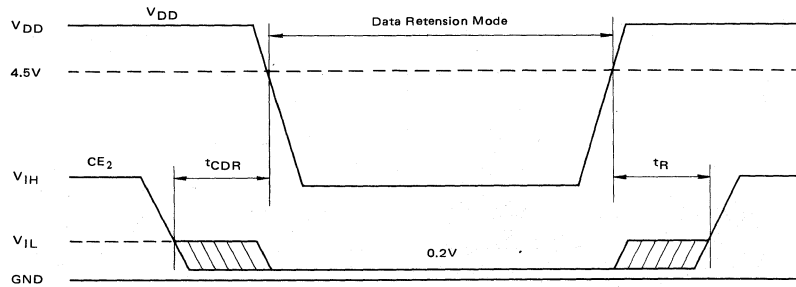
SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage			2.0	–	5.5	V
I_{DDS2}	Standby Current	TC5564PL-10, PL-15	Ta = 25°C	–	–	0.2	μA
			Ta = 60°C	–	–	1.0	μA
		TC5564P-10, P-15		–	–	20	μA
t_{CDR}	Chip Deselection to Data Retention Mode			0	–	–	μS
t_R	Recovery Time			t_{RC}	–	–	μS

Note (1) t_{RC} : Read cycle time $\overline{CE}_1$ Controlled Data Retention Mode (2)

$\overline{CE}_1$ Controlled Data Retention Mode (2)



CE_2 Controlled Data Retention Mode (4)



NOTE:

(2) In $\overline{CE}_1$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$ or $CE_2 \geqq V_{DD} - 0.2V$.

(3) If the V_{IH} of $\overline{CE}_1$ is 2.2V in operation, during the period that the V_{DD} Voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

(4) In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$.

DEVICE INFORMATION

The TC5564P is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows after only row address change, as is shown in the following figure.

This peak current may induce the noise on V_{DD}/GND line. Thus the use of about 0.1μF decoupling capacitor every device is recommended to eliminate such noise.

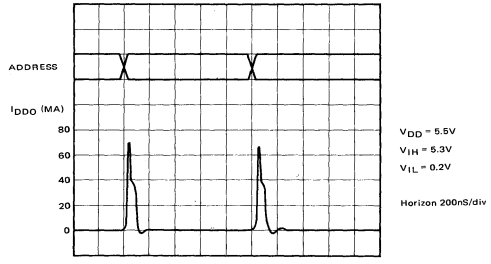
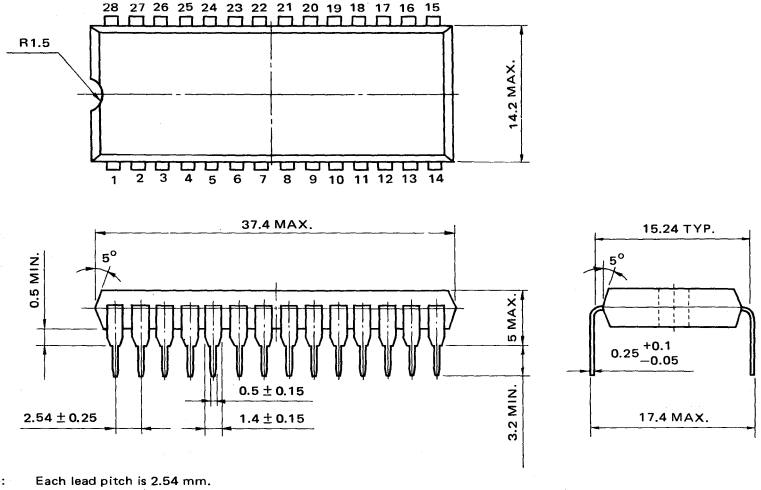


Fig. TYPICAL CURRENT WAVE FORMS

OUTLINE DRAWINGS

Unit : mm



Note: Each lead pitch is 2.54 mm.
All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

8,192 WORD X 8 BIT CMOS STATIC RAM

SILICON GATE CMOS

TC5565P-12/P-15
TC5565PL-12/PL-15

DESCRIPTION

The TC5565P is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provides both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 120ns/150ns.

When CE_2 is a logical low or $\overline{CE}_1$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC5565P has three control inputs. Two chip enables ($\overline{CE}_1$, CE_2) allow for device selection and data retention control and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5565P is suitable for use in various microprocessor application systems where high speed, low power and battery back up are required.

The TC5565P also features pin compatibility with the 64K bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

The TC5565P is offered in a dual-in-line 28 pin standard plastic package.

FEATURES

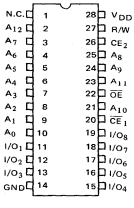
- Low Power Dissipation
  27.5mW/MHz (Max.) Operating
- Standby Current
  100μA (Max.) : TC5565PL-12, PL-15
  1mA(Max.) : TC5565P-12, P-15
- 5V Single Power Supply
- Power Down Features: CE_2, $\overline{CE}_1$
- Fully Static Operation
- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Access Time

	TC5565P-12 TC5565PL-12	TC5565P-15 TC5565PL-15
Address Access Time (MAX.)	120 ns	150 ns
$\overline{CE}_1$ Access Time (MAX.)	120 ns	150 ns
CE_2 Access Time (MAX.)	120 ns	150 ns
Output Enable Time (MAX.)	60 ns	70 ns

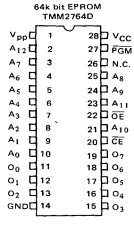
- Directly TTL Compatible: All Inputs and Outputs
- Standard 28 Pin DIP
- Pin Compatible with 2764 type EPROM

PIN CONNECTION (TOP View)

TC5565P



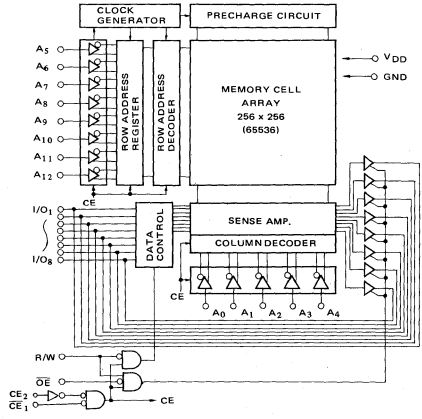
64k bit EPROM
TMM2764D



PIN NAMES

$A_0 \sim A_{12}$	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}_1$, CE_2	Chip Enable Inputs
$I/O_1 \sim I/O_8$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

Operation Mode	$\overline{CE}_1$	CE_2	$\overline{OE}$	R/W	$I/O_1 \sim I/O_8$	Power
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	*	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	$-0.3 \sim 7.0$	V
V_{IN}	Input Voltage	$-2.0 \sim 7.0$	V
$V_{I/O}$	Input and Output Voltage	$-0.5 \sim V_{DD} +0.5$	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature	260·10	°C · sec
T_{strg}	Storage Temperature	$-55 \sim 150$	°C
$T_{opr.}$	Operating Temperature	$0 \sim 70$	°C

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} +0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0 ~ 70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$			–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			4.0	–	–	mA
I_{LO}	Output Leakage Current	$\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$ or R/W = V_{IL} or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$			–	–	±1.0	μA
I_{DDO1}	Operating Current	V_{DD} = 5.5V, $\overline{CE}_1 = V_{IL}$ $CE_2 = V_{IH}$	t_{cycle} = 1μs		–	–	10	mA
		Other Input = V_{IH}/V_{IL}	t_{cycle} = 100ns		–	–	45	mA
I_{DDO2}	Operating Current	V_{DD} = 5.5V $\overline{CE}_1$ = 0.2V, $CE_2 = V_{DD} -0.2V$ Other Input = V_{IH}/V_{IL}	t_{cycle} = 1μs		–	–	5	mA
			t_{cycle} =100ns		–	–	40	mA
I_{DDS1}	Standby Current	$\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$			–	–	3	mA
*I_{DDS2}	Standby Current	$\overline{CE}_1 = V_{DD} -0.2V$ or $CE_2 = 0.2V$ V_{DD} = 2.0 ~ 5.5V		TC5565PL	–	2	100	μA
				TC5565P		–	1.0	mA

Note: In standby mode with $\overline{CE}_1 \geqq V_{DD} -0.2V$, these specification limits are guaranteed under the condition of $CE_2 \geqq V_{DD} -0.2V$ or $CE_2 \leqq 0.2V$.

CAPACITANCE (Ta = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{DD} = 5V ±10%)

Read Cycle

SYMBOL	PARAMETER	CONDITIONS	TC5565P-12/PL-12		TC5565P-15/PL-15		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	V_{IN} = 2.4V/0.6V	120	–	150	–	ns
t_{ACC}	Address Access Time	V_{IH} = 2.2V	–	120	–	150	ns
t_{CO1}	$\overline{CE}_1$ Access Time	V_{IL} = 0.8V	–	120	–	150	ns
t_{CO2}	CE_2 Access Time	t_r, $t_f \leqq$ 5ns	–	120	–	150	ns
t_{OE}	Output Enable to Output in Valid	V_{OH} = 2.2V V_{OL} = 0.8V	–	60	–	70	ns
t_{COE}	Chip Enable ($\overline{CE}_1$, CE_2) to Output in Low-Z	Output Load: C_L (100pF) and 1-TTL Gate	10	–	10	–	ns
t_{OEE}	Output Enable to Output Low-Z		5	–	5	–	ns
t_{OD}	Chip Enable ($\overline{CE}_1$, CE_2) to Output in High-Z		–	60	–	70	ns
t_{ODO}	Output Enable to Output in High-Z		–	50	–	60	ns
t_{OH}	Output Data Hold Time		20	–	20	–	ns

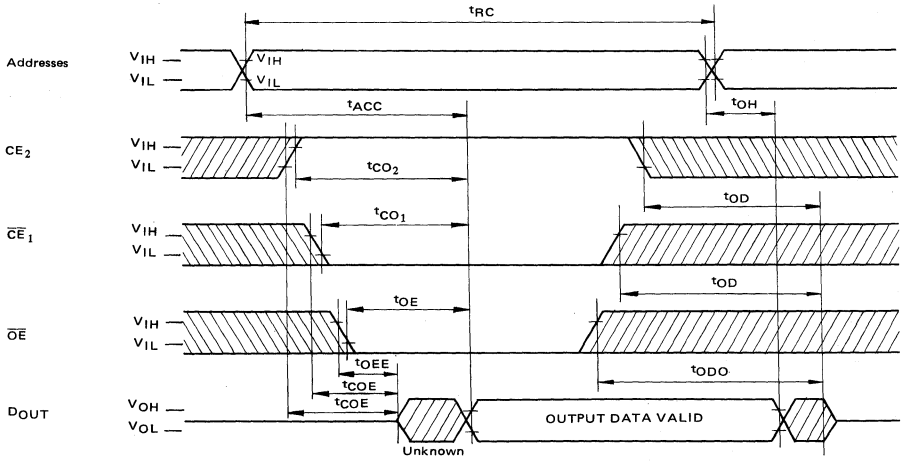
Write Cycle

SYMBOL	PARAMETER	CONDITIONS	TC5565P-12/PL-12		TC5565P-15/PL-15		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	V_{IN} = 2.4V/0.6V	120	–	150	–	ns
t_{WP}	Write Pulse Width	V_{IH} = 2.2V	80	–	100	–	ns
t_{CW}	Chip Selection to End of Write	V_{IL} = 0.8V t_r, $t_f \leqq$ 5 ns	100	–	120	–	ns
t_{AS}	Address Set up Time		0	–	0	–	ns
t_{WR}	Write Recovery Time		0	–	0	–	ns
t_{WRI}	Write Recovery Time ($\overline{CE}_1$, $\overline{CE}_2$)		10	–	10	–	ns
t_{ODW}	R/W to Output High-Z		–	50	–	70	ns
t_{OEW}	R/W to Output Low-Z		10	–	10	–	ns
t_{DS}	Data Set up Time		50	–	60	–	ns
t_{DH}	Data Hold Time		0	–	0	–	ns
t_{DHI}	Data Hold Time ($\overline{CE}_1$, $\overline{CE}_2$)		10	–	10	–	ns

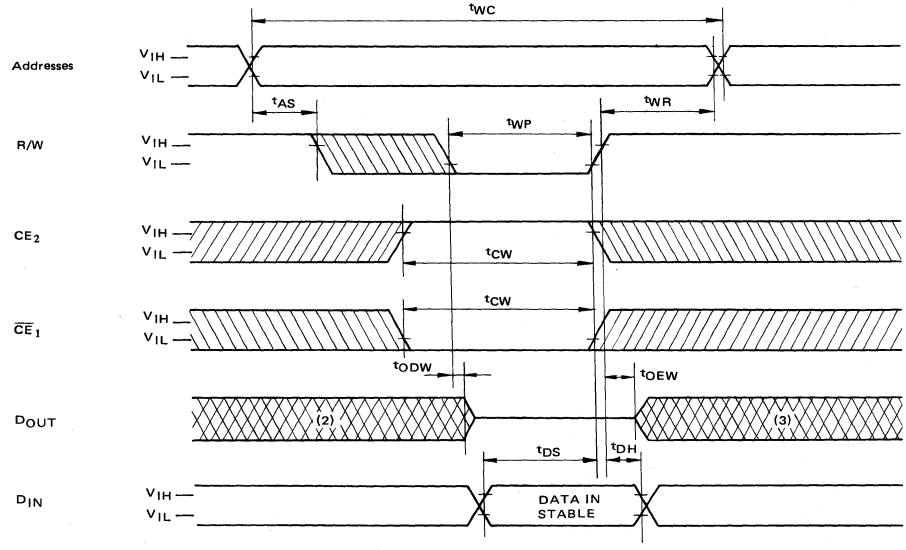
Note: Input pulse levels = V_{IN}
Timing Measurement Reference levels = V_{IH}, V_{IL}

TIMING WAVEFORMS

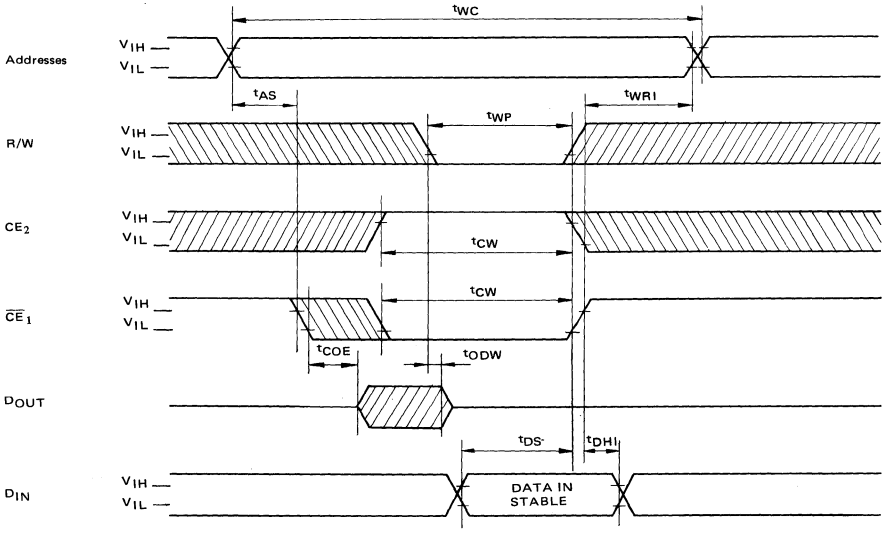
• READ CYCLE (1)



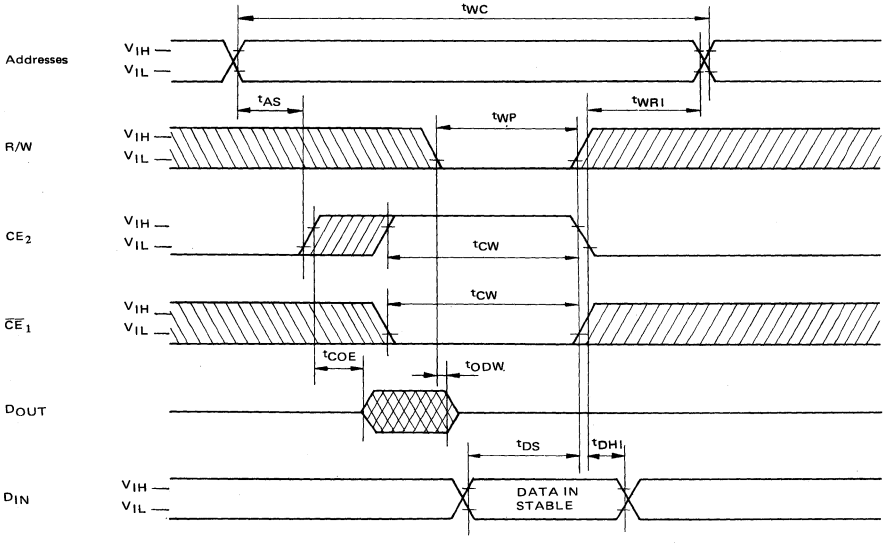
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE}_1$ Controlled Write)



WRITE CYCLE 3 (4) (CE_2 Controlled Write)



NOTE:

(1) R/W is High for Read Cycle.

(2) Assuming that $\overline{CE}_1$ Low transition of CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

(3) Assuming that $\overline{CE}_1$ High transition or CE_2 Low transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.

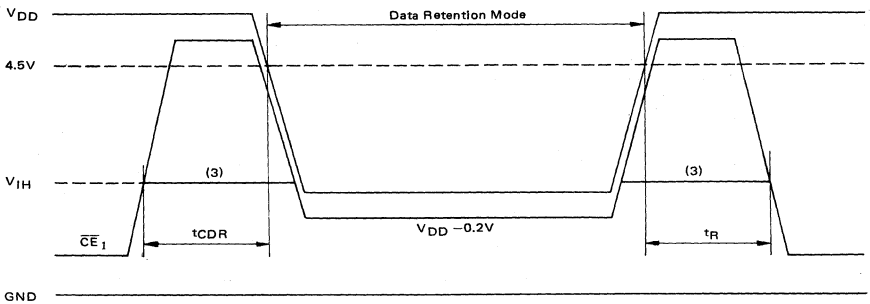
(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70°C)

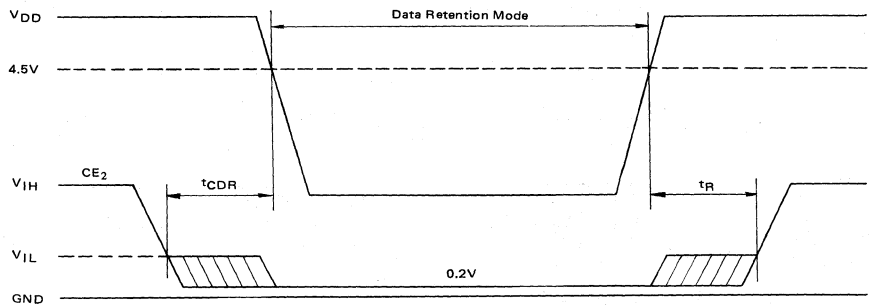
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Stand by Supply Current	TC5565PL-12, PL-15	–	–	100	μA
		TC5565P-12, P-15	–	–	1.0	mA
t_{CDR}	Chip Deselection to Data Retention Mode		0	–	–	μs
t_R	Recovery Time		t_{RC}(1)	–	–	μs

Note (1): Read cycle time

● **$\overline{CE}_1$ Controlled Data Retention Mode (2)**



● **CE_2 Controlled Data Retention Mode (4)**



NOTE:

(2) In $\overline{CE}_1$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$ or $CE_2 \geqq V_{DD} - 0.2V$.

(3) If the V_{IH} of $\overline{CE}_1$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

(4) In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$.

DEVICE INFORMATION

The TC5565P is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows after only row address change, as is shown in the following figure.

This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF decoupling capacitor every device is recommended to eliminate such noise.

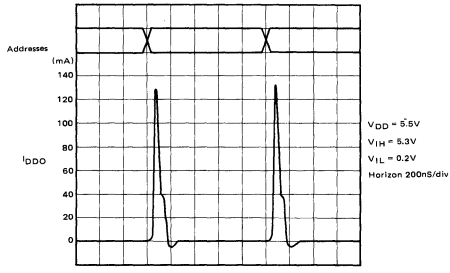
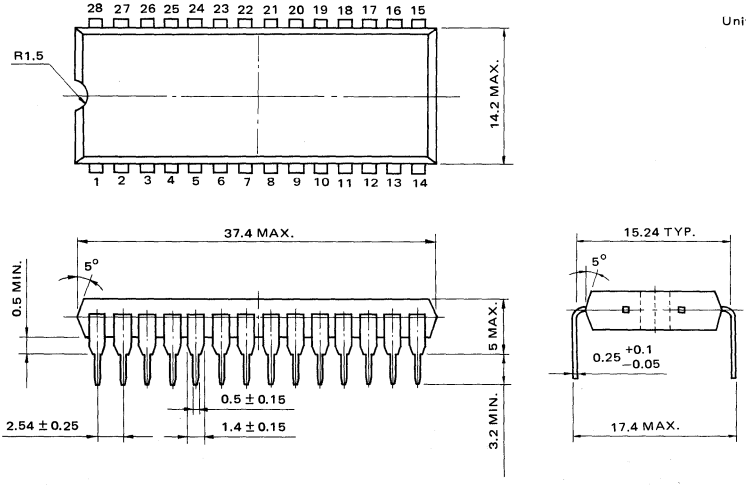


Fig. TYPICAL CURRENT WAVE FORMS

OUTLINE DRAWINGS

Unit : mm



Note: Each lead pitch is 2.54 mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

rasable/Programmable Read Only Memory

8,192 WORD x 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

N-CHANNEL SILICON STACKED GATE MOS

TMM2764D
TMM2764D-2

DESCRIPTION

The TMM2764D is a 8192 word x 8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM2764D's access time is 200 ns, and the TMM2764D operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. The maximum active current is 120mA and the maximum standby current is 35mA.

For program operation, the programming is achieved by applying a 50ms active TTL low program pulse to the $\overline{PGM}$ input, and it is possible to program sequentially individually., or at random.

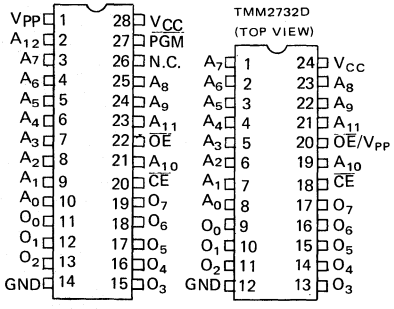
The TMM2764D is fabricated with the N-channel silicon double layer gate MOS technology and is packaged in a standard 28 pin dual in line cerdip package.

FEATURES

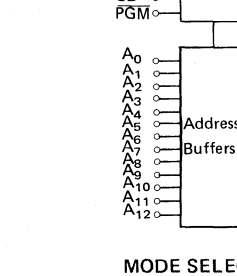
- Single 5-volt power supply
- Fast access time : TMM2764D 250 ns
  TMM2764D-2 200 ns
- Power dissipation :
  120 mA (active current) Max.
  35 mA (standby current) Max.
- Low power standby mode : $\overline{CE}$
- Output buffer control : $\overline{OE}$
- Fully static operation
- Programs with one 50 ms pulse
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i2764 and ROM TMM2364P

PIN CONNECTION

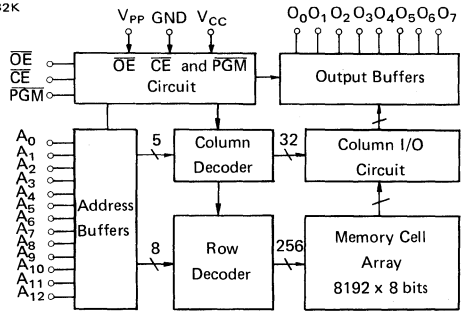
(TOP VIEW) Lower 24 pins compatible with 32K bit EPROM TMM2732D



TMM2732D (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{12}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
N.C.	No Connection
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

Mode \ Pin	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13,15~19)	Power
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H		5V	High Impedance	
Standby	*	H	*		5V	High Impedance	Standby
Program	L	L	*	21V	5V	Data in	Active
Program Inhibit	*	H	*		5V	High Impedance	
	H	L	H		5V	High Impedance	
Program Verify	H	L	L		5V	Data Out	

Note: * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6 ~ 7.0	V
V_{PP}	Program Supply Voltage	−0.6 ~ 22.0	V
V_{IN}	Input Voltage	−0.6 ~ 7.0	V
V_{OUT}	Output Voltage	−0.6 ~ 7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
$T_{STRG.}$	Storage Temperature	−65 ~ 125	°C
$T_{OPR.}$	Operating Temperature	0 ~ 70	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	–	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	–	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC} + 0.6	V

D.C. and OPERATING CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 5\%$ Unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	–	–	± 10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE} = V_{IH}$	–	–	35	mA
I_{CC2}	Supply Current (Active)	$\overline{CE} = V_{IL}$	–	–	120	mA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu A$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$	–	–	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = 0 \sim V_{CC} + 0.6$	–	–	± 10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4 \sim V_{CC}$	–	–	± 10	μA

A.C. CHARACTERISTICS

Ta = 0 ~ 70°C, V_{CC} = 5V ± 5%, V_{PP} = 2.0V ~ V_{CC} + 0.6V, Unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	TMM2764D-2		TMM2764D		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	200	–	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	200	–	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	70	–	100	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	$\overline{OE}$ = $\overline{CE}$ = V_{IL}	–	70	–	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	60	0	90	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	$\overline{OE}$ = $\overline{CE}$ = V_{IL}	0	60	0	90	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	–	–	–	ns

A.C. Test Conditions

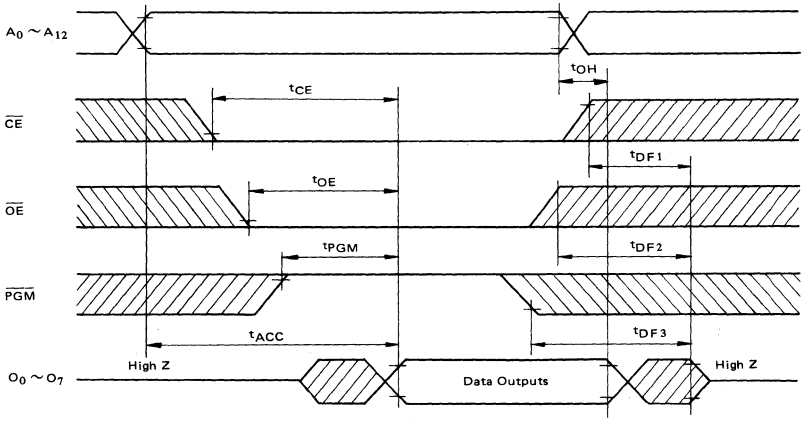
- Output Load : 1 TTL Gate and C_L = 100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.8V to 2.2V
- Timing Measurement Reference Level : Inputs 1V and 2V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	–	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage	–0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.0	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D.C. and OPERATING CHARACTERISTICS

($Ta = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	–	–	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu A$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	120	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 21.5V$	–	–	30	mA

A.C. PROGRAMMING CHARACTERISTICS

($Ta = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$)

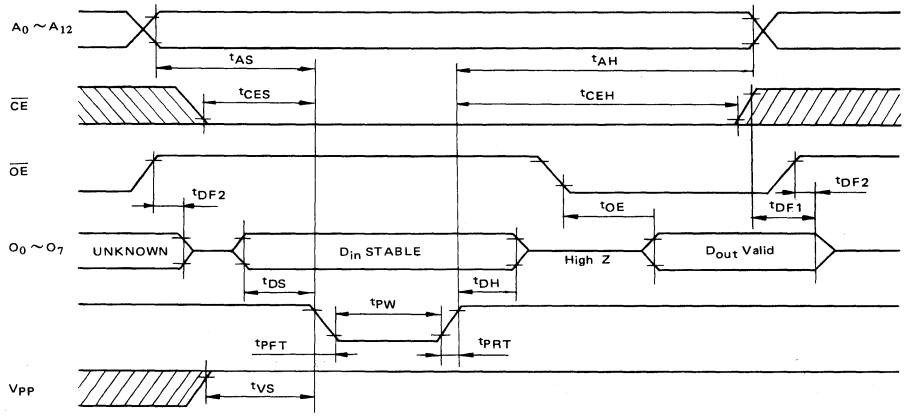
SYMBOL	PARAMETER	CONDITIONS	MIN.	Typ.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	μs
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{PS}	$\overline{PGM}$ Setup Time	–	2	–	–	μs
t_{PH}	$\overline{PGM}$ Hold Time	–	2	–	–	μs
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	μs
t_{VS}	V_{PP} Setup Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	$\overline{PGM} = \overline{CE} = V_{IL}$	45	50	55	ms
t_{CP}	Program Recovery Time	–	0	–	–	μs
t_{PRT}	Program Pulse Rise Time	–	5	–	–	ns
t_{PFT}	Program Pulse Fall Time	–	5	–	–	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	–	–	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	–	–	–	100	ns
t_{DF1}	$\overline{CE}$ to Output in High Z	$\overline{OE} = V_{IL}$	–	–	90	ns
t_{DF2}	$\overline{OE}$ to Output in High Z	$\overline{CE} = V_{IL}$	–	–	90	ns

A.C. Test Conditions

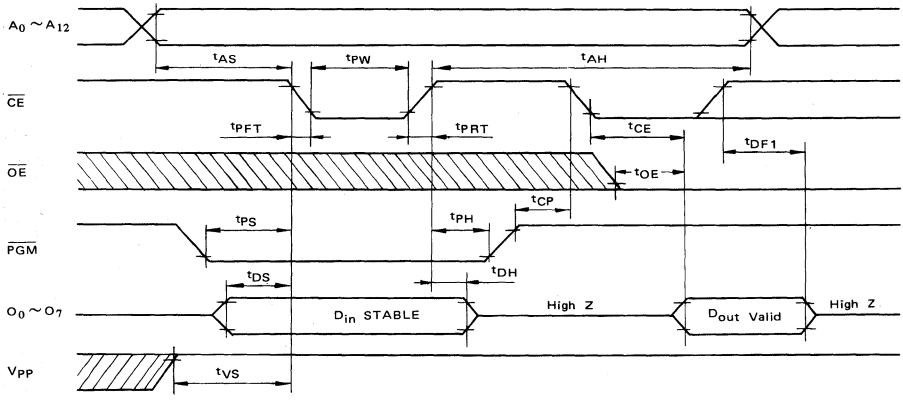
- Output Load : 1TTL Gate and C_L (100 pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.8 ~ 2.2V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

PROGRAM OPERATION 1. (V_{PP} = 21V ± 0.5V)



PROGRAM OPERATION 2. (V_{PP} = 21V ± 0.5V)



Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP} = 21V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the over-shoot voltage of its pulse should not be exceeded 22V.

ERASURE CHARACTERISTICS

The TMM2764D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (Ultraviolet light intensity [w/cm²] x exposure time [sec.]) for erasure should be a minimum of 15 [W. sec/cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1 cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [μw/cm²] x (20 x 60) [sec] ≅ 15 [w. sec/cm²].)

The TMM2764D's erasure begins to occur when exposed to light with wavelength shorter than 4000 Å. The sunlight and the fluorescent lamps will include 3000 ~ 4000 Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TMM2764D's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs. In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	Power
READ OPERATION (Ta = 0 ~ 70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta = 25±5°C)	Program	L	L	*	21V	5V	Data In	Active
	Program	*	H	*			High Impedance	Active
	Inhibit	H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TMM2764D has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}$ = $\overline{OE}$ = V_{IL} and $\overline{PGM}$ = V_{IH}, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}$ = $\overline{OE}$ = V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, the outputs will be in a high impedance state. So two or more TMM2764D can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM2764D has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a TTL high level to the $\overline{CE}$ input, the TMM2764D is placed in the standby mode which reduce the operating current from 120mA to 35mA, and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM2764D are in the "1" state which is erased state.

Therefore the program operation is to introduce "0s" data into the desired bit locations by electrically programming.

The TMM2764D is set up in the program operation mode when applied the program voltage (+21V) to the V_{PP} terminal under $\overline{CE}$ = $\overline{PGM}$ = $\overline{OE}$ = V_{IH}.

The program operation occurs during the overlap of the $\overline{CE}$ low and the $\overline{PGM}$ low. Then the programming is achieved by applying a 50ms (t_{PW}) active low program pulse to the $\overline{CE}$ or the $\overline{PGM}$ input after the addresses and data are stable.

This program pulse should be a single pulse with 50ms pulse width per address word, and its maximum value is 55ms.

The levels required for all inputs are TTL.

The TMM2764D can be programmed any location at anytime — either individually, sequentially, or at random.

The TMM2764D should not be programmed with D.C. signal applied to both $\overline{CE}$ and $\overline{PGM}$ inputs.

PROGRAM VERIFY MODE

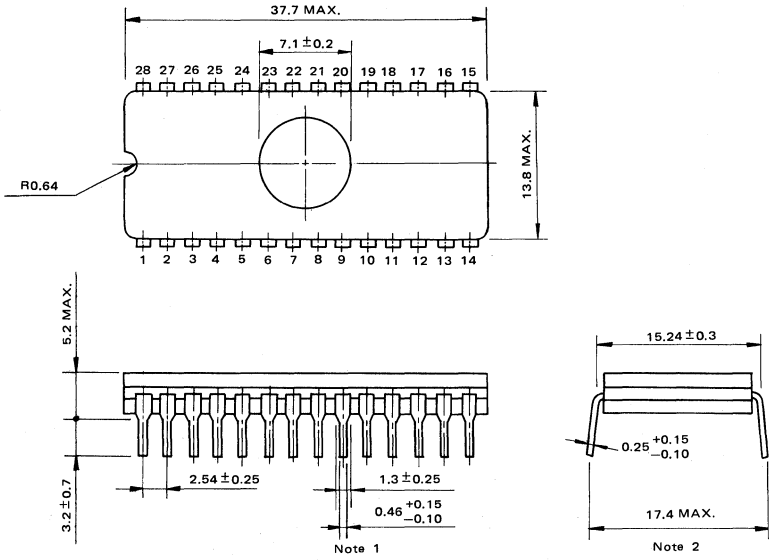
The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM2764D from being programmed. Programming of two or more TMM2764Ds in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

OUTLINE DRAWINGS



Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No. 28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

8,192 WORD x 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

N-CHANNEL SILICON STACKED GATE MOS

TMM2764DI
TMM2764DI-2

DESCRIPTION

The TMM2764DI is a 8192 word x 8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM2764DI's access time is 200 ns, and the TMM2764DI operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. The maximum active current is 130 mA and the maximum standby current is 40mA.

For program operation, the programming is achieved by applying a 50ms active TTL low program pulse to the $\overline{PGM}$ input, and it is possible to program sequentially individually, or at random.

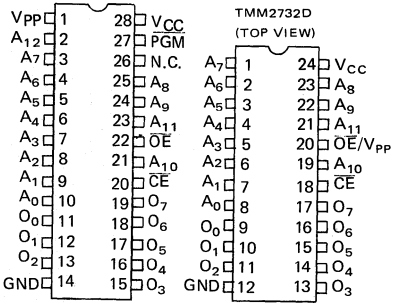
The TMM2764DI is fabricated with the N-channel silicon double layer gate MOS technology and is packaged in a standard 28 pin dual in line cerdip package.

FEATURES

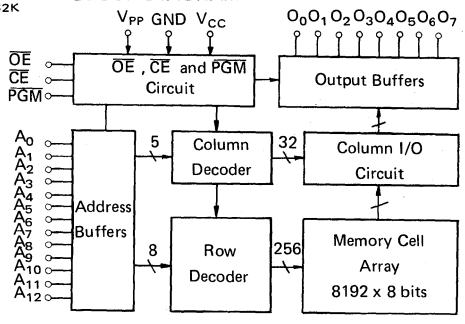
- Wide operating temperature Range −40~85°C
- Single 5-volt power supply
- Fast access time : TMM2764DI 250 ns
  TMM2764DI-2 200 ns
- Power dissipation :
  130 mA (active current) Max.
  40 mA (standby current) Max.
- Low power standby mode : $\overline{CE}$
- Output buffer control : $\overline{OE}$
- Fully static operation
- Programs with one 50 ms pulse
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i2764 and ROM TMM2364P

PIN CONNECTION

(TOP VIEW) Lower 24 pins compatible with 32K bit EPROM TMM2732D



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{12}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
N.C.	No Connection
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

Mode \ Pin	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13,15~19)	Power
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H		5V	High Impedance	
Standby	*	H	*		5V	High Impedance	Standby
Program	L	L	*	21V	5V	Data in	Active
Program Inhibit	*	H	*		5V	High Impedance	
	H	L	H		5V	High Impedance	
Program Verify	H	L	L		5V	Data Out	

Note: * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6 ~ 7.0	V
V_{PP}	Program Supply Voltage	−0.6 ~ 22.0	V
V_{IN}	Input Voltage	−0.6 ~ 7.0	V
V_{OUT}	Output Voltage	−0.6 ~ 7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
$T_{STRG.}$	Storage Temperature	−65 ~ 125	°C
$T_{OPR.}$	Operating Temperature	−40 ~ 85	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	–	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.2	V_{CC}	V_{CC} + 0.6	V

D.C. and OPERATING CHARACTERISTICS

($Ta = -40 \sim 85°C$, $V_{CC} = 5V \pm 5\%$ Unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	–	–	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE} = V_{IH}$	–	–	40	mA
I_{CC2}	Supply Current (Active)	$\overline{CE} = V_{IL}$	–	–	130	mA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu A$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$	–	–	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = 0 \sim V_{CC} + 0.6$	–	–	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4 \sim V_{CC}$	–	–	±10	μA

A.C. CHARACTERISTICS

Ta = −40 ~ 85°C, V_{CC} = 5V±5%, V_{PP} = 2.2V ~ V_{CC} + 0.6V, Unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	TMM2764DI-2		TMM2764DI		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	200	–	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	200	–	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	70	–	100	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	$\overline{OE}$ = $\overline{CE}$ = V_{IL}	–	70	–	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	60	0	90	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	$\overline{OE}$ = $\overline{CE}$ = V_{IL}	0	60	0	90	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	–	0	–	ns

A.C. Test Conditions

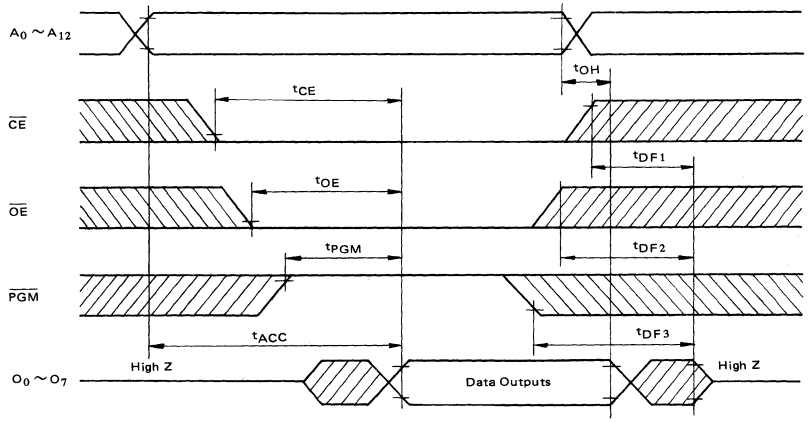
- Output Load : 1 TTL Gate and C_L = 100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.6V to 2.4V
- Timing Measurement Reference Level : Inputs 1V and 2V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.0	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D.C. and OPERATING CHARACTERISTICS

($Ta = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	–	–	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu A$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	130	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 21.5V$	–	–	30	mA

A.C. PROGRAMMING CHARACTERISTICS

($Ta = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$)

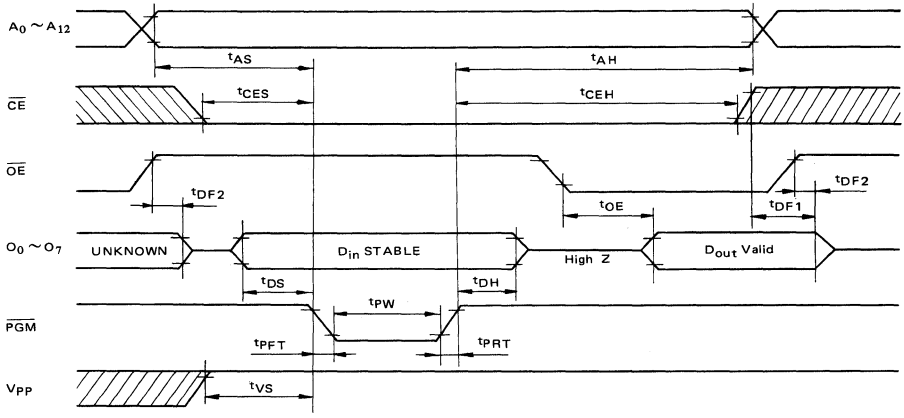
SYMBOL	PARAMETER	CONDITIONS	MIN.	Typ.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	μs
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{PS}	$\overline{PGM}$ Setup Time	–	2	–	–	μs
t_{PH}	$\overline{PGM}$ Hold Time	–	2	–	–	μs
t_{VS}	V_{PP} Setup Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	$\overline{PGM} = \overline{CE} = V_{IL}$	45	50	55	ms
t_{CP}	Program Recovery Time	–	0	–	–	μs
t_{PRT}	Program Pulse Rise Time	–	5	–	–	ns
t_{PFT}	Program Pulse Fall Time	–	5	–	–	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	–	–	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	–	–	–	100	ns
t_{DF1}	$\overline{CE}$ to Output in High Z	$\overline{OE} = V_{IL}$	–	–	90	ns
t_{DF2}	$\overline{OE}$ to Output in High Z	$\overline{CE} = V_{IL}$	–	–	90	ns

A.C. Test Conditions

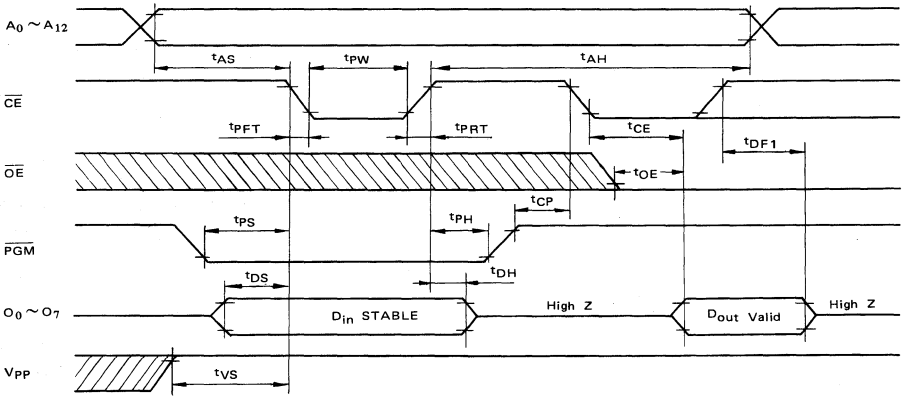
- Output Load : 1TTL Gate and C_L (100 pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.6 ~ 2.4V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

PROGRAM OPERATION 1. (V_{PP} = 21V ± 0.5V)



PROGRAM OPERATION 2. (V_{PP} = 21V ± 0.5V)



Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP} = 21V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the over-shoot voltage of its pulse should not be exceeded 22V.

ERASURE CHARACTERISTICS

The TMM2764DI's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (Ultraviolet light intensity [w/cm²] x exposure time [sec.]) for erasure should be a minimum of 15 [W. sec/cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1 cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] x (20 x 60) [sec] ≅ 15 [w. sec/cm²].)

The TMM2764DI's erasure begins to occur when exposed to light with wavelength shorter than 4000 Å. The sunlight and the fluorescent lamps will include 3000 ~ 4000 Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TMM2764DI's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs. In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11 ~ 13, 15 ~ 19)	Power
READ OPERATION (Ta = −40~85°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impednace	Standby
PROGRAM OPERATION (Ta = 25 ±5°C)	Program	L	L	*	21V	5V	Data In	Active
	Program Inhibit	*	H	*			High Impednace	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TMM2764DI has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}$ = $\overline{OE}$ = V_{IL} and $\overline{PGM}$ = V_{IH}, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}$ = $\overline{OE}$ = V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more TMM2764DI can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM2764DI has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a TTL high level to the $\overline{CE}$ input; the TMM2764DI is placed in the standby mode which reduce the operating current from 130mA to 40mA, and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM2764DI are in the "1" state which is erased state.

Therefore the program operation is to introduce "0s" data into the desired bit locations by electrically programming.

The TMM2764DI is set up in the program operation mode when applied the program voltage (+21V) to the V_{PP} terminal under $\overline{CE} = \overline{PGM} = \overline{OE} = V_{IH}$.

The program operation occurs during the overlap of the $\overline{CE}$ low and the $\overline{PGM}$ low. Then the programming is achieved by applying a 50ms (t_{PW}) active low program pulse to the $\overline{CE}$ or the $\overline{PGM}$ input after the addresses and data are stable.

This program pulse should be a single pulse with 50ms pulse width per address word, and its maximum value is 55ms.

The levels required for all inputs are TTL.

The TMM2764DI can be programmed any location at anytime — either individually, sequentially, or at random.

The TMM2764DI should not be programmed with D.C. signal applied to both $\overline{CE}$ and $\overline{PGM}$ inputs.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

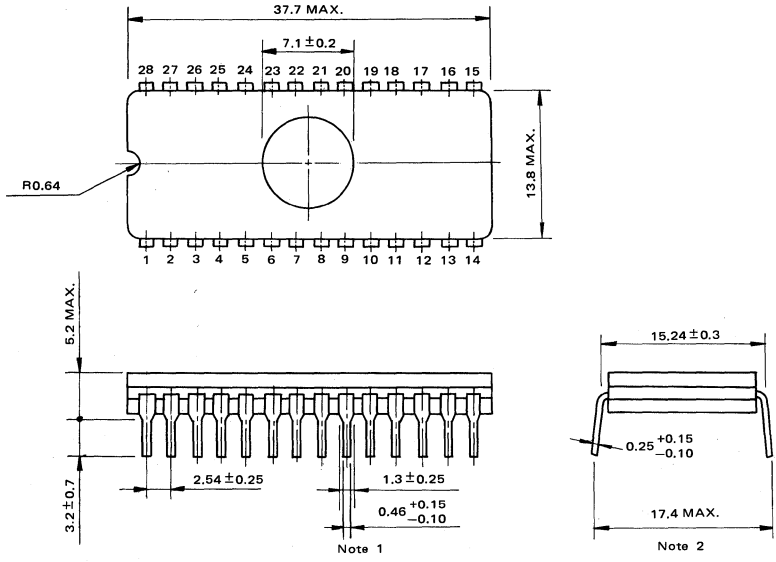
The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM2764DI from being programmed. Programming of two or more TMM2764DIs in parallel with different data is easily accomplished.

That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

OUTLINE DRAWINGS



Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No. 28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

Distributed by

16384 WORD x 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

TMM27128D-20
TMM27128D-25

DESCRIPTION

The TMM27128D is a 16384 word x 8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM 27128D's access time is 200 ns, and the TMM27128D operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. The maximum active current is 120 mA and the maximum standby current is 35mA.

For program operation, the programming is achieved by applying a 50 ms active TTL low program pulse to the $\overline{PGM}$ input, and it is possible to program sequentially, individually, or at random.

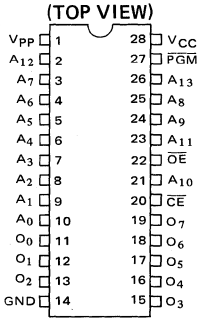
The TMM27128D is fabricated with the N-channel silicon double layer gate MOS technology and is packaged in a standard 28 pin dual in line cerdip package.

FEATURES

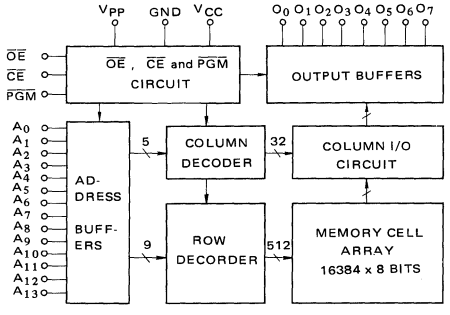
- Single 5-volt power supply
- Fast access time: TMM27128D-25 250 ns
  TMM27128D-20 200 ns
- Power dissipation:
  120 mA (active current) Max.
  35 mA (standby current) Max.
- Low power standby mode: $\overline{CE}$
- Output buffer control: $\overline{OE}$
- Fully static operation
- Programs with one 50 ms pulse
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i27128

PIN CONNECTION

(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{13}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

Mode \ Pin	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	Power
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H		5V	High Impedance	
Standby	*	H	*		5V	High Impedance	Standby
Program	L	L	*	21V	5V	Data In	Active
Program Inhibit	*	H	*		5V	High Impedance	
	H	L	H		5V	High Impedance	
Program Verify	H	L	L		5V	Data Out	

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6 ~ 7.0	V
V_{PP}	Program Supply Voltage	−0.6 ~ 22.0	V
V_{IN}	Input Voltage	−0.6 ~ 7.0	V
V_{OUT}	Output Voltage	−0.6 ~ 7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
$T_{STRG.}$	Storage Temperature	−65 ~ 125	°C
$T_{OPR.}$	Operating Temperature	0 ~ 70	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	–	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	–	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC} + 0.6	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ±5% Unless otherwise noted)

SYMBOL	PARAMTER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN} = 0 ~ V_{CC}	–	–	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$ = V_{IH}	–	–	35	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$ = V_{IL}	–	–	120	mA
V_{OH}	Output High Voltage	I_{OH} = −400μA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	–	–	0.4	V
I_{PP1}	V_{PP} Current	V_{PP} = 0 ~ V_{CC} + 0.6	–	–	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4 ~ V_{CC}	–	–	±10	μA

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ±5%, V_{PP} = 2.0V ~ V_{CC} + 0.6V, Unless otherwise noted)

SYMBOL	PARAMTER	CONDITIONS	TMM27128D-20		TM27128D-25		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	200	–	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	200	–	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	70	–	100	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	$\overline{OE}$ = $\overline{CE}$ = V_{IL}	–	70	–	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	60	0	90	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	$\overline{OE}$ = $\overline{CE}$ = V_{IL}	0	60	0	90	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	ns

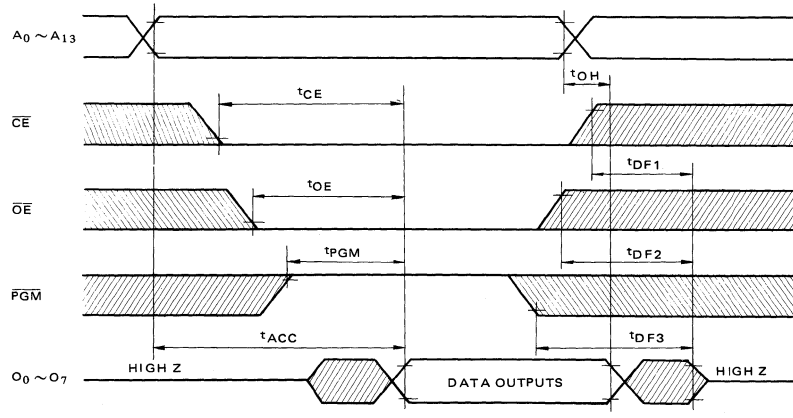
- **AC Test Conditions**
- Output Load: 1 TTL Gate and C_L = 100pF
- Input Pulse Rise and Fall Times: 10 ns Max.
- Input Pulse Levels: 0.8V to 2.2V
- Timing Measurement Reference Level: Inputs 1V and 2V, Outputs 0.8V and 2.0V

CAPACITIANCE * (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = OV	–	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = OV	–	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	–	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage	–0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.0	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D.C. and OPERATING CHARACTERISTICS (Ta = 25 ± 5°C, V_{CC} = 5V ± 5%, V_{PP} = 21V ± 0.5V)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN} = 0 ~ V_{CC}	–	–	±10	μA
V_{OH}	Output High Voltage	I_{OH} = –400μA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	120	mA
I_{PP2}	V_{PP} Supply Current	V_{PP} = 21.5V	–	–	30	mA

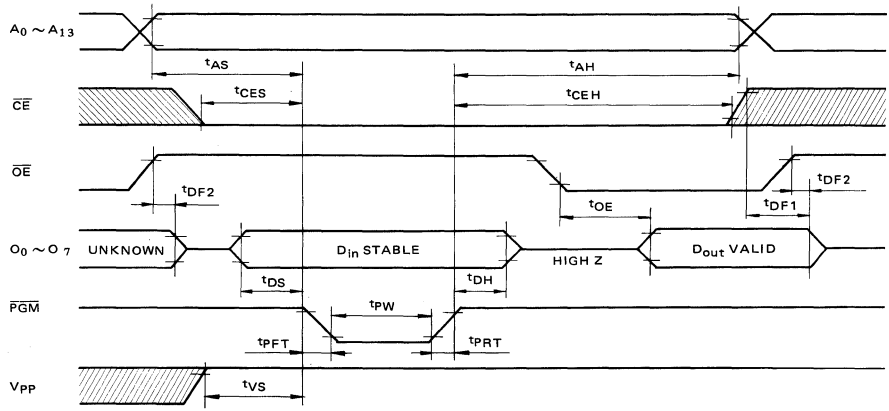
A.C. PROGRAMMING CHARACTERISTICS (Ta = 25 ± 5°C, V_{CC} = 5V ± 5%, V_{PP} = 21V ± 0.5V)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	μs
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{PS}	$\overline{PGM}$ Setup Time	–	2	–	–	μs
t_{PH}	$\overline{PGM}$ Hold Time	–	2	–	–	μs
t_{VS}	V_{PP} Setup Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	$\overline{PGM}$ = $\overline{CE}$ = V_{IL}	45	50	55	ms
t_{CP}	Program Recovery Time	–	0	–	–	μs
t_{PRT}	Program Pulse Rise Time	–	5	–	–	ns
t_{PFT}	Program Pulse Fall Time	–	5	–	–	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	–	–	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	–	–	–	100	ns
t_{DF1}	$\overline{CE}$ to Output in High Z	$\overline{OE}$ = V_{IL}	–	–	90	ns
t_{DF2}	$\overline{OE}$ to Output in High Z	$\overline{CE}$ = V_{IL}	–	–	90	ns

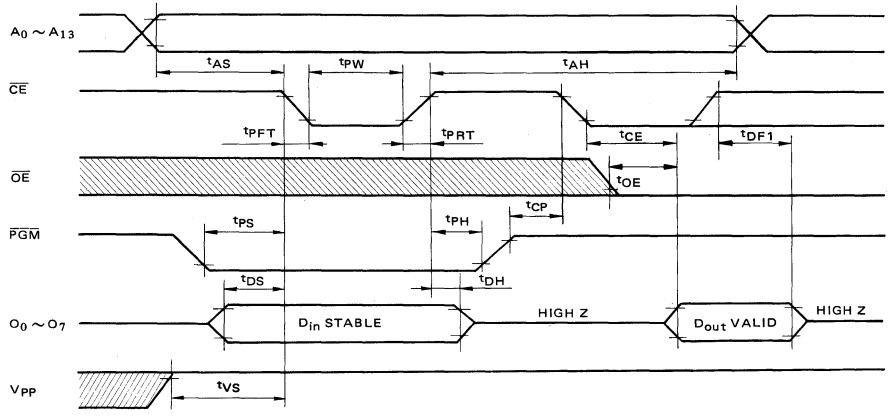
- **A.C. Test Conditions**
- Output Load: 1TTL Gate and C_L (100 pF)
- Input Pulse Rise and Fall Times: 10 ns Max.
- Input Pulse Levels: 0.8 ~ 2.2V
- Timing Measurement Reference Level: Input 1V and 2V; Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

PROGRAM OPERATION 1. (V_{PP} = 21V ± 0.5V)



PROGRAM OPERATION 2. (V_{PP} = 21V ± 0.5V)



Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP} = 21V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the over-shoot voltage of its pulse should not be exceeded 22V.

ERASURE CHARACTERISTICS

The TMM27128D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537 Å (Angstroms) to the chip through the transparent window. Then integrated dose (Ultraviolet light intensity [w/cm^2] x exposure time [sec.]) for erasure should be a minimum of 15 [W. sec/cm^2].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1 cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm^2] x (20 x 60) [sec] ≅ 15 [w.sec/cm^2].)

The TMM27128D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000 ~ 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals — Toshiba EPROM Protect Seal AC901 — are available.

OPERATION INFORMATION

The TMM27128D's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs. In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11 ~ 13, 15 ~ 19)	Power
READ OPERATION (Ta = 0 ~ 70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta = 25 ± 5°C)	Program	L	L	*	21V	5V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
	Program Inhibit	H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note: H; V_{IH}, L; V_{IL}, *V_{IH} or V_{IL}

READ MODE

The TMM27128D has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The Output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}$ = $\overline{OE}$ = V_{IL} and $\overline{PGM}$ = V_{IH}, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}$ = $\overline{OE}$ = V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, the outputs will be in a high impedance state. So two or more TMM27128D can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27128D has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a TTL high level to the $\overline{CE}$ input, the TMM27128D is placed in the standby mode which reduce the operating current from 120mA to 35mA, and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and $\overline{PGM}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27128D are in the "1" state which is erased state.

Therefore the program operation is to introduce "Os" data into the desired bit locations by electrically programming.

The TMM27128D is set up in the program operation mode when applied the program voltage (+21V) to the V_{PP} terminal under $\overline{CE}$ = $\overline{PGM}$ = $\overline{OE}$ = V_{IH}.

The program operation occurs during the overlap of the $\overline{CE}$ low and the $\overline{PGM}$ low. Then the programming is achieved by applying a 50ms (tpw) active low program pulse to the $\overline{CE}$ or the $\overline{PGM}$ input after the addresses and data are stable.

This program pulse should be a single pulse with 50ms pulse width per address word, and its maximum value is 55ms.

The levels required for all input are TTL. The TMM27128D can be programmed any location at anytime — either individually, sequentially, or at random.

The TMM27128D should not be programmed with D.C. signal applied to both $\overline{CE}$ and $\overline{PGM}$ inputs.

PROGRAM VERIFY MODE

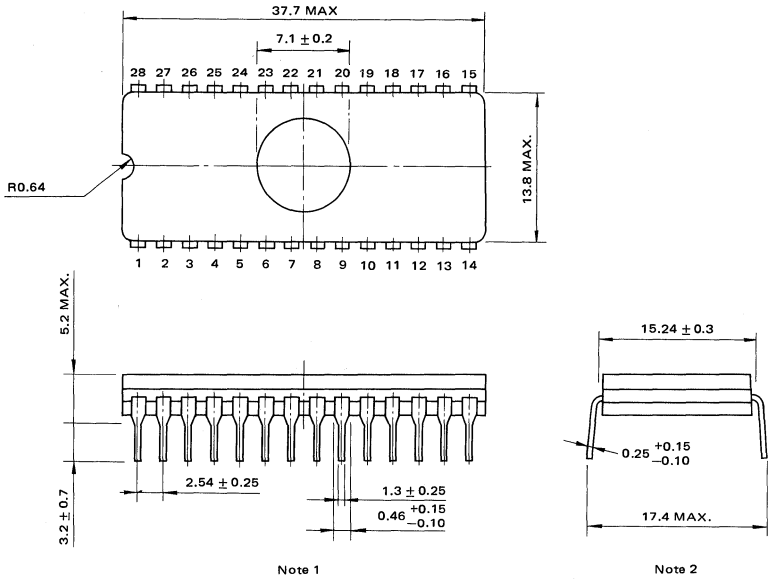
The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM27128D from being programmed. Programming of two or more TMM27128Ds in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

OUTLINE DRAWINGS



Note 1 Note 2

Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No. 28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

Mask Programmable Read Only Memories

2048 WORD x 8 BIT MASK ROM

N CHANNEL SILICON GATE DEPLETION LOAD

TMM334P

DESCRIPTION

TMM334P is a 16,384 bits read only memory organized as 2048 words by 8 bits and is compatible with i2716 type (16K EPROM). It is suitable for use in programming of production apparatus used micro processor because of its low cost per bit.

TMM334P's mask making is carried out by computer using punched paper tape data of customer and then sample manufacturing will start. Then for customer, 16384 bits memory data and three chip select input active logic are programmable.

Therefore TMM334P manufacturing procedure goes through three steps before mass production. First step is a acceptance of customer's punched paper tape data. Second step is a presentation of programmed sample (Engineering Sample) for customers. Third step is a verification of Engineering Sample by customers. Sample verification is most important and Toshiba will enter into mass production after above three steps are concluded. Then Toshiba will adopt a established on-line system and so can respond to a customer's needs quickly and can maintain a stable delivery.

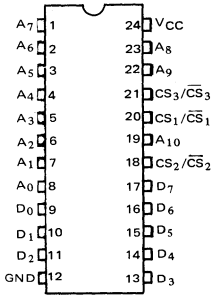
TMM334P is fabricated with ion implanted N-channel silicon gate technology. This technology allows a production of high performance. TMM334P is moulded in a 24 pin standard plastic package.

FEATURES

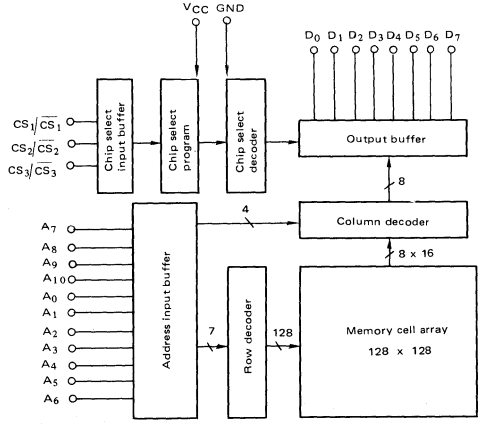
- Single 5V supply voltage; V_{CC} = 5V ± 10%
- Access time; t_{ACC} = 450 ns. (Max.)
- Directly TTL compatible; All inputs and outputs
- Programmable chip select inputs; CS1, CS2, CS3 Easy memory expansion
- Three state output; OR tie capability
- Static operation; No clocks are required.
- Input protected; All inputs have protection against static charge
- Pin to pin compatible; TMM323C, i2316E, i2716

PIN CONNECTION

(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_6$	Row address inputs
$A_7 \sim A_{10}$	Column address inputs
$D_0 \sim D_7$	Data outputs
$CS_1/\overline{CS_1} \sim CS_3/\overline{CS_3}$	Chip select inputs
VCC	V_{CC} Power Supply Voltage
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power supply voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input and output voltage	−0.5 ~ 7.0	V
T_{opr}	Operating temperature	0 ~ 70	°C
T_{stg}	Storage temperature	−55 ~ 150	°C
T_{SOLDER}	Soldering temperature · time	260 · 10	°C · sec
P_D	Power Dissipation (Ta = 70°C)	1.0	W

D.C. OPERATING CONDITION

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input high voltage	–	2.0	–	V_{CC} + 1	V
V_{IL}	Input low voltage	–	−0.5	–	0.8	V
V_{CC}	Power supply voltage	–	4.5	–	5.5	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0°C ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IH}	Input high current	$V_{IN} = V_{CC}$	–	0.01	10	μA
I_{IL}	Input low current	V_{IN} = GND	–	−0.01	−10	μA
V_{OH}	Output high voltage	I_{SOURCE} = −0.4mA	2.4	3.0	–	V
V_{OL}	Output low voltage	I_{SINK} = 2.1mA	–	0.2	0.4	V
I_{OH}	Output high current	V_{OUT} = 2.4V	−0.4	−3.0	–	mA
I_{OL}	Output low current	V_{OUT} = 0.4V	2.1	5.0	–	mA
I_{LO}	Output leakage current	$\overline{CS}$ = 0.8V, $\overline{CS}$ = 2.0V V_{OUT} = 0.4V to V_{CC}	–	±0.01	± 10	μA
I_{CC}	Supply current	I_{OUT} = 0mA	–	40	80	mA

* Ta = 25°C, V_{CC} = 5V

A.C. CHARACTERISTICS ($Ta = 0°C \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 100pF$, $t_r, t_f = 20ns$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.*	MAX.	UNIT
t_{ACC}	Access time	$t_{AC} \leqq 100ns$	–	270	450	ns
t_{CO}	Output delay time from chip select	$t_{AC} \geqq t_{ACC}$	–	80	120	ns
t_{OD}	Output deselect time	$R_L = 100\Omega$	0	70	100	ns
t_{RC}	Read cycle time	–	450	–	–	ns

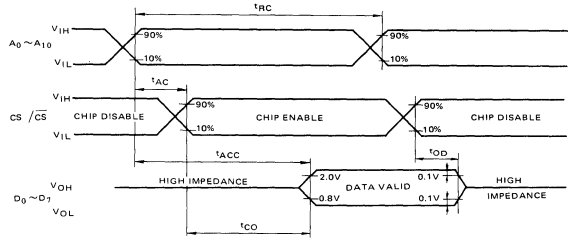
* Ta = 25°C, V_{CC} = 5V

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input capacitance	V_{IN} = A. C. GND	–	4	10	pF
C_{OUT}	Output capacitance	V_{OUT} = A. C. GND	–	8	15	pF

Note: This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



PAPER TAPE FORMAT

Punched paper tape data must be a positive logic and use a 7 to 8 bit ASCII code.
Format 1 (including Data and Check sum every word).

NULL	Take NULL more than fifty characters.
▼TMM334P - XXXX▼	Contents in single quotation mark (▼. . .▼) indicates a comment and XXXX is a user's number.
CR LF	CR and LF indicate carriage return and line feed respectively.
▼MSB = D_7▼	Specify MSB pin. (D_7 or D_0)
CR LF	
N8;	N8 indicates a 8-bit mask pattern. Semicolon (;) indicates a punctuation of data.
CR LF	
Ruuu0; X07P3; . . . . ; XF1P5;	R indicates an absolute address. Enter the address by decimal code every eight words.
CR LF	
. . . .	X indicates hexadecimal code. So enter the data represented by hexadecimal code every word after X.
CR LF	P indicates a check sum of its word. So enter a sum of one's number in a word by decimal code after P.
R2040; X01P1; . . . ; X3AP4;	Data modification: Enter the modified address before the End mark and then enter the data following above procedure independently or serialy. Modification can be allowed from 0 address to 2047 address.
CR LF	
(CS_1 = 0)	Customers can program the active logic of three chip select inputs independently. Specify the active logic of chip select input in the brackets. The example is shown in Figure. In this example, chip is active under the condition that CS1 = '0' and CS2 = '1' and CS3 = '0'.
CR LF	
(CS_2 = 1)	
CR LF	
(CS_3 = 0)	
CR LF	
$	$ Indicates an End mark .
CR LF	
NULL	Take NULL more then fifty characters.

Format 2 (including Data only every word)

```
NULL
▼TMM334P - XXXX▼
CR LF
▼MSB = D7 ▼
CR LF
N8;
CR LF
Ruuu0; X075A . . . 3BF1;
CR LF
.
.
.
R2032; XBCAE . . . 0085;
CR LF
(CS1 = 0)
CR LF
(CS2 = 0)
CR LF
(CS3 = 0)
CR LF
$
CR LF
NULL
```

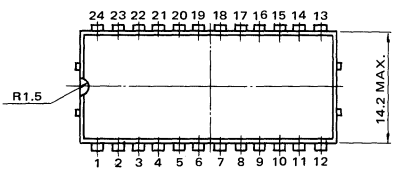
R indicates an absolute address. Enter the address by decimal code every sixteen words.

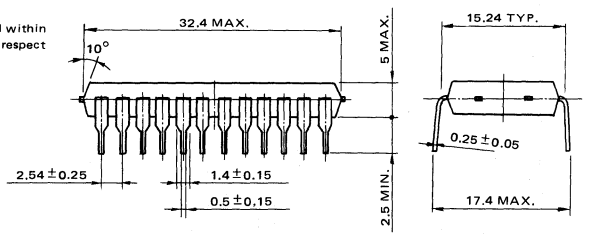
X indicates a hexadecimal code and so enter the data of sixteen words continuously after X.

Data modification: This procedure is following to Format 1. Otherwise specified in Format 1.

Format 1 and Format-2 are Toshiba preferred Format.
The other acceptable Format is Intel BNPF Format.

OUTLINE DRAWINGS





Note: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 24 leads.
All dimensions are in millimeters.

4096 WORD x 8 BIT MASK ROM

N CHANNEL SILICON GATE DEPLETION LOAD

TMM333P

DESCRIPTION

The TMM333P is a 32,768 bits read only memory organized as 4,096 words by 8 bits. It is suitable for use in programming of production apparatus used micro processor because of its low cost per bit.

The TMM333P's mask making is carried out by computer using punched paper tape data of customer and then sample manufacturing will start. Then for customer, 32,768 bits memory data and two chip select input active logic are programmable.

Therefore the TMM333P manufacturing procedure goes through three steps before mass production. First step is a acceptance of customer's punched paper tape data. Second step is a presentation of programmed sample (Engineering Sample) for customers. Third step is a verification of Engineering Sample by customers. Sample verification is most important and Toshiba will enter into mass production after above three steps are concluded. Then Toshiba will adopt a established on-line system and so can respond to a customer's needs quickly and can maintain a stable delivery.

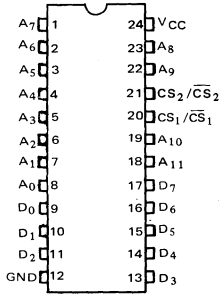
The TMM333P is fabricated with ion implanted N-channel silicon gate technology. This technology allows a production of high performance. The TMM 333P is moulded in a 24 pin standard plastic package.

FEATURES

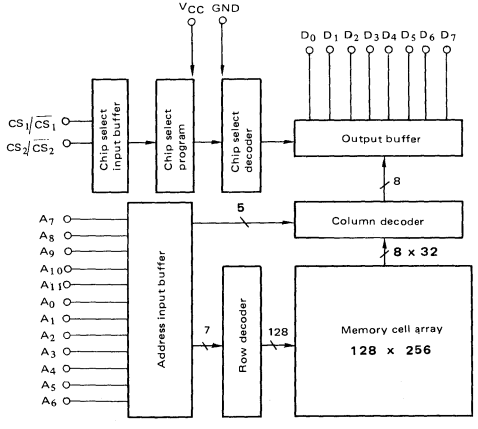
- Single 5V supply voltage; V_{CC} = 5V ± 5%
- Access time; t_{ACC} = 450 ns. (Max.)
- Directly TTL compatible; All inputs and outputs
- Programmable chip select inputs; CS1, CS2, Easy memory expansion
- Three state outputs; OR tie capability
- Static operation; No clocks are required.
- Input protected; All inputs have protection against static charge
- Pin to pin compatible; TMS4732

PIN CONNECTION

(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_6$	Row address inputs
$A_7 \sim A_{11}$	Column address inputs
$D_0 \sim D_7$	Data outputs
$CS_1/\overline{CS_1}$; $CS_2/\overline{CS_2}$	Chip select inputs
VCC	Power supply terminal
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power supply voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input and output voltage	−0.5 ~ 7.0	V
T_{opr}	Operating temperature	0 ~ 70	°C
T_{stg}	Storage temperature	−55 ~ 150	°C
T_{SOLDER}	Soldering temperature · time	260 · 10	°C · sec
P_D	Power Dissipation (Ta = 70°C)	1.0	W

D.C. OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input high voltage	–	2.0	–	V_{CC} + 1	V
V_{IL}	Input low voltage	–	−0.5	–	0.8	V
V_{CC}	Power supply voltage	–	4.75	5.0	5.25	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0°C ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IH}	Input high current	$V_{IN} = V_{CC}$	–	0.01	10	μA
I_{IL}	Input low current	V_{IN} = GND	–	−0.01	−10	μA
V_{OH}	Output high voltage	I_{SOURCE} = −0.4mA	2.4	3.0	–	V
V_{OL}	Output low voltage	I_{SINK} = 2.1mA	–	0.2	0.4	V
I_{OH}	Output high current	V_{OUT} = 2.4V	−0.4	−3.0	–	mA
I_{OL}	Output low current	V_{OUT} = 0.4V	2.1	5.0	–	mA
I_{LO}	Output leakage current	$\overline{CS}$ = 0.8V, $\overline{CS}$ = 2.0V V_{OUT} = 0.4V to V_{CC}	–	±0.01	±10	μA
I_{CC}	Supply current	I_{OUT} = 0mA	–	60	100	mA

* Ta = 25°C, V_{CC} = 5V

A.C. CHARACTERISTICS (Ta = 0°C ~ 70°C, V_{CC} = 5V ± 5%, C_L = 100pF, t_r, t_f = 20ns)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.*	MAX.	UNIT
t_{ACC}	Access time	$t_{AC} \leqq$ 100ns	–	300	450	ns
t_{CO}	Output delay time from chip select	$t_{AC} \geqq t_{ACC}$	–	120	200	ns
t_{OD}	Output deselect time	–	0	100	150	ns
t_{RC}	Read cycle time	–	450	–	–	ns

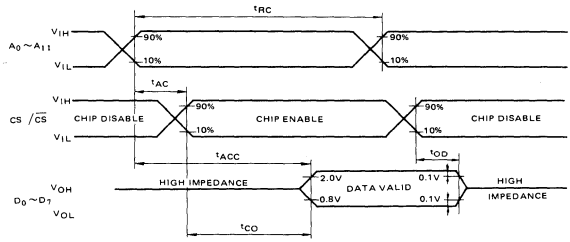
* Ta = 25°C, V_{CC} = 5V

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input capacitance	V_{IN} = A. C. GND	–	4	10	pF
C_{OUT}	Output capacitance	V_{OUT} = A. C. GND	–	8	15	pF

Note: This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



PAPER TAPE FORMAT

Punched paper tape data must be a positive logic and use a 7 to 8 bit ASCII code.
Format 1 (including Data and Check sum every word).

NULL	Take NULL more than fifty characters.
▼ TMM333P - XXXX ▼	Contents in single quotation mark (▼. . .▼) indicates a comment and XXXX is a user's number.
CR LF	CR and LF indicate carriage return and line feed respectively.
▼ MSB = D_7 ▼	Specify MSB pin. (D_7 or D_0)
CR LF	
N8;	N8 indicates a 8-bit mask pattern.
CR LF	Semicolon (;) indicates a punctuation of data.
Ruuu0; X07P3; . . . . ; XF1P5;	R indicates an absolute address. Enter the address by decimal code every eight words.
CR LF	X indicates hexadecimal code. So enter the data represented by hexadecimal code every word after X.
. . . . .	P indicates a check sum of its word. So enter a sum of one's number in a word by decimal code after P.
CR LF	
R4088; X01P1; . . . ; X3AP4;	Data modification: Enter the modified address before the End mark and then enter the data following above procedure independently or serialy. Modification can be allowed from 0 address to 4095 address.
CR LF	
(CS_1 = 0)	Customers can program the active logic of two chip select inputs independently. Specify the active logic of chip select input in the brackets. The example is shown in Figure. In this example, chip is active under the condition that CS1 = '0' and CS2 = '1'.
CR LF	
(CS_2 = 1)	
CR LF	
$	$ Indicates an End mark .
CR LF	
NULL	Take NULL more then fifty characters.

Format 2 (including Data only every word)

NULL

▼TMM333P - XXXX▼

CR LF

▼MSB = D_7 ▼

CR LF

N8;

CR LF

Ruuu0; X075A . . . 3BF1;

CR LF

.
.
.

R4080; XBCAE . . . 0085;

CR LF

(CS_1 = 0)

CR LF

(CS_2 = 0)

CR LF

$

CR LF

NULL

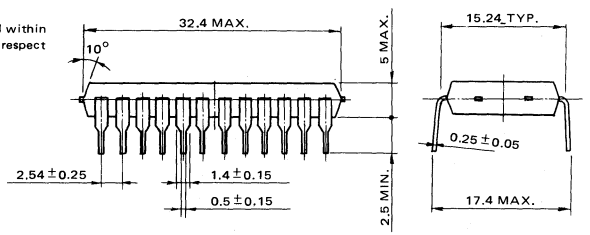
R indicates an absolute address. Enter the address by decimal code every sixteen words.

X indicates a hexadecimal code and so enter the data of sixteen words continuously after X.

Data modification: This procedure is following to Format 1. Otherwise specified in Format 1.

Format 1 and Format 2 are Toshiba preferred Format.
The other acceptable Format is Intel BNPF Format.

OUTLINE DRAWINGS



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 24 leads.
All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

4,096 WORD X 8 BIT MASK ROM

N-CHANNEL SILICON GATE

TMM2332P

DESCRIPTION

The TMM2332P is a 32768-bit read only memory organized as 4096 words by 8 bits with a low bit cost, thus being most suitable for use in programming of production apparatus using microprocessor.

The TMM2332P features an automatic power down mode. When deselected by Chip Select (CS/$\overline{CS}$), the device is in low power (I_{SB}=15mA MAX.) standby mode. This device feature results in system power saving in larger systems, where the majority of devices are deselected.

The TMM2332P is fabricated with ion implanted N-channel silicon gate technology. This technology allows a production of high performance.

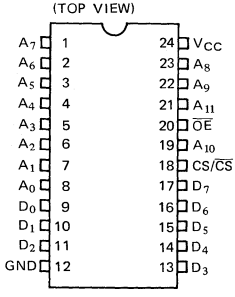
The TMM2332P is moulded in a 24-pin standard plastic package.

FEATURES

- Single 5V-Power Supply
- Fast Access Time: 350ns (MAX.)
- Low Power Dissipation
  Operating Current = 100mA (MAX.)
  Standby Current = 15mA (MAX.)
- Power Down Feature: CS / $\overline{CS}$
- Programmable Chip Select: CS / $\overline{CS}$
- Output Buffer Control : $\overline{OE}$
- Easy memory Expansion : CS / $\overline{CS}$
- Static Operation
- Pin Compatible with 2732 Type EPROM and i2332
- All Inputs and Outputs:
  Directly TTL Compatible
- Three State Outputs: Wired OR Capability.
- Inputs Protected: All inputs have protection against static charge.

PIN CONNECTION

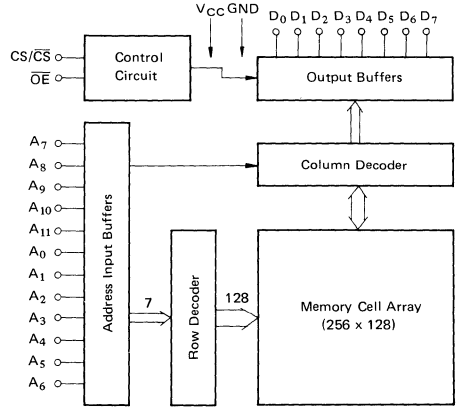
(TOP VIEW)



PIN NAMES

A_0~A_{11}	Address Inputs
D_0~D_7	Data Outputs
CS/$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-0.5 ~ 7.0	V
V_{OUT}	Output Voltage	-0.5 ~ 7.0	V
T_{OPR}	Operating Temperature	0 ~ 70	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{SOLDER}	Soldering Temperature•Time	260 • 10	°C•Sec
P_D	Power Dissipation (Ta = 70°C)	1.0	W

D.C. OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	–	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.5	–	0.8	V
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V

D.C. CHARACTERISTICS (V_{CC} = 5V±10%, T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 ~ V_{CC}	–	±0.02	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	-0.4	-2.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	4.0	–	mA
I_{LO}	Output Leakage Current	$\overline{OE}$ = V_{IH} or $\overline{CS}$ = V_{IH} V_{OUT} = 0.4V ~ V_{CC}	–	±0.05	±10	μA
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL} or CS = V_{IH}	–	–	100	mA
I_{SB}	Standby Current	$\overline{CS}$ = V_{IH} or CS = V_{IL}	–	–	15	mA

CAPACITANCE (T_a = 0 ~ 70°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	8	15	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{RC}	Read Cycle Time	350	–	–	ns
t_{ACC}	Access Time	–	–	350	ns
t_{CO}	Chip Selection to Output Valid	–	–	350	ns
t_{OO}	$\overline{OE}$ to Output Valid	–	–	120	ns
t_{ODC}	Chip Deselection to Output in High-Z	–	–	100	ns
t_{ODO}	$\overline{OE}$ to Output in High-Z	–	–	100	ns
t_{PU}	Chip Selection to Power Up Time	0	–	–	ns
t_{PD}	Chip Deselection to Power Down Time	–	–	100	ns

A.C. TEST CONDITIONS

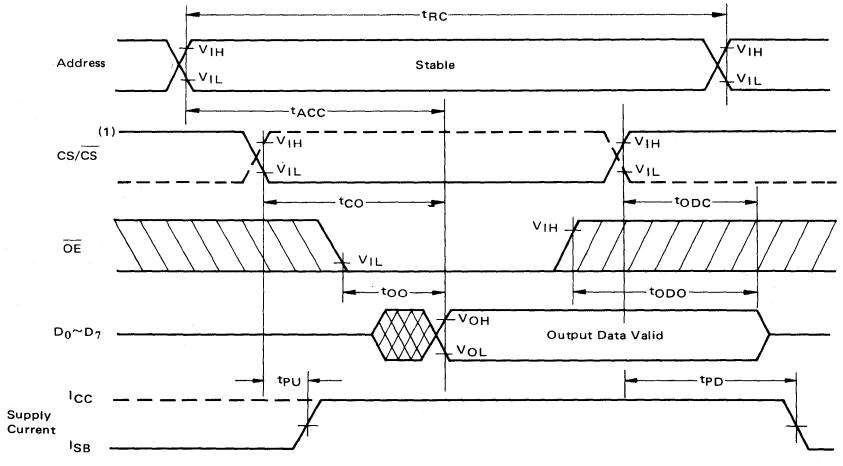
Input Rise and Fall Times ; 20ns

Timing Measurement Reference Levels ; Input : 0.8V and 2.0V

Output: 0.8V and 2.0V

Output Load; 1-TTL Gate and C_L = 100pF

A.C. TIMING WAVEFORMS

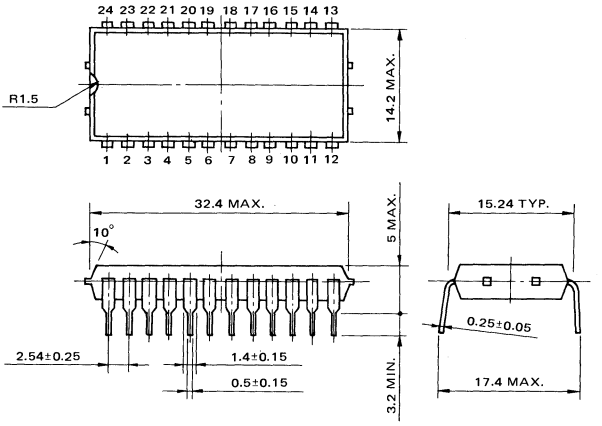


Note: (1) CS and $\overline{CS}$ waveforms are shown by dotted line and straight line respectively.

ACCEPTABLE FORMAT

Toshiba can accept programming and masking information for TMM2332P in the form of punched paper tape with Intel BNPF format or master devices (EPROM).

OUTLINE DRAWINGS



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm longitudinal position with respect to No. 1 and No. 24 leads.
All dimensions are in millimeters.

64K BIT (8K WORD X 8 BIT) MASK ROM

N CHANNEL SILICON GATE

TMM2364P

DESCRIPTION

The TMM2364P is a 65536 bit read only memory organized as 8192 words by 8 bits with a low bit cost, thus being most suitable for use in programming of production apparatus using micro-processor.

Consisting of static memory cells and clocked peripheral circuitry, the TMM2364P provides a high speed and low power dissipation (access time 250ns, operating current 40mA).

The TMM2364P also features an automatic stand-by power mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced from 40mA to 15mA. Output Enable ($\overline{OE}$) is effective in preventing data confliction on a common bus line.

The TMM2364P uses the address latch system that the falling edge of $\overline{CE}$ latches all inputs except for $\overline{OE}$, thus can be easily connected to a system where address and data buses are commonly used.

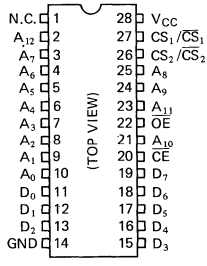
The TMM2364P is fabricated with ion implanted N-channel silicon gate technology. This technology allows a production of high performance.

The TMM2364P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

FEATURES

- Single 5V ± 10% power Supply
- Access Time: 250ns max.
- Low Power Dissipation
  - Average Current: 40mA max.
  - Standby Current: 15mA max.
- Input and Output: TTL Compatible
- Three State Outputs: Wired OR Capability
- Edge Enabled Operation: $\overline{CE}$
- Output Buffer Control: $\overline{OE}$
- Programmable Chip Select: CS_1, CS_2 Easy Memory Expansion
- Pin Compatible with i2364
- Inputs protected: All inputs have protection against static charge.

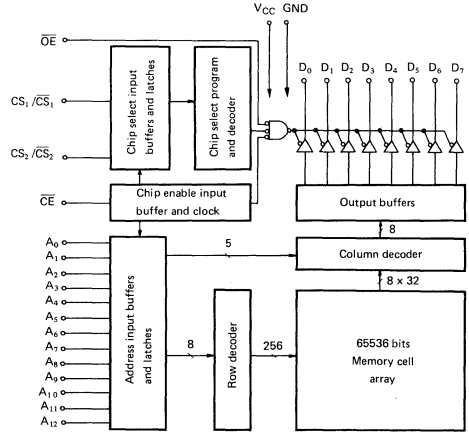
PIN CONNECTION



PIN NAMES

$A_0 \sim A_{12}$	Address inputs
$D_0 \sim D_7$	Data outputs
$CS/\overline{CS}$	Chip select inputs
$\overline{OE}$	Output enable inpu
$\overline{CE}$	Chip enable input
N.C.	No connection
V_{CC}	Power supply terminal
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input and Output Voltage	−0.5 ~ 7.0	V
T_{OPR}	Operating Temperature	0 ~ 70	°C
T_{STRG}	Storage Temperature	−55 ~ 150	°C
T_{SD}	Soldering Temperature · Time	260 · 10	°C · sec
P_D	Power Dissipation (Ta = 70°C)	1.0	W

D.C. OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	—	2.2	—	V_{CC} + 1	V
V_{IL}	Input Low Voltage	—	−0.5	—	0.8	V
V_{CC}	Power Supply Voltage	—	4.5	5.0	5.5	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
I_{IH}	Input High Current	V_{IN} = 5.5V		—	0.05	10	μA
I_{IL}	Input Low Current	V_{IN} = GND		—	−0.05	−10	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA		2.4	3.3	—	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA		—	0.3	0.4	V
I_{LOH}	Output Leakage Current	V_{OUT} = 5.5V	$\overline{CE}$ = 2.2V or	—	0.05	10	μA
I_{LOL}		V_{OUT} = 0.4V	$\overline{OE}$ = 2.2V	—	−0.1	−20	μA
I_{CC1}	Standby Current	$\overline{CE}$ = 2.2V		—	8	15	mA
I_{CC2}	Average Current	t_{CYC} = 350ns, I_{OUT} = 0mA		—	20	40	mA

* Typical values are at Ta = 25°C and V_{CC} = 5V.

A.C. CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{CE}	$\overline{CE}$ pulse width	–	250	–	–	ns
t_{AS}	Address Setup Time	–	0	–	–	ns
t_{AH}	Address Hold Time	–	50	–	–	ns
t_{ACC}	Access Time	–	–	150	250	ns
t_{OO}	Output Delay Time from $\overline{OE}$	–	–	50	120	ns
t_{OD}	Output Turn off Delay	–	–	40	70	ns
t_{CC}	$\overline{CE}$ off Time	–	90	–	–	ns
t_{CYC}	Cycle Time	$t_{AS} = 0ns$, $t_r, t_f = 5ns$	350	–	–	ns

* Typical values are at $Ta = 25°C$ and $V_{CC} = 5V$.

A.C. TEST CONDITIONS

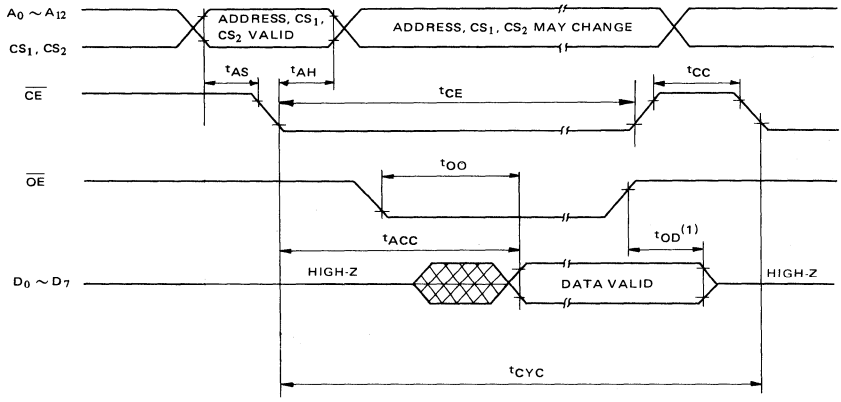
- Output Load: ITTL Gate + 100pF
- Input Rise and Fall Times (10% ~ 90%): 5ns
- Input Pulse Levels: 0.8 ~ 2.4V
- Timing Measurement Reference Levels: Input; 1V and 2.2V
  Output; 0.8V and 2.0V

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = A.C. GND	–	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = A.C. GND	–	8	15	pF

Note: This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



Note (1) t_{OD} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

OPERATION MODE

$\overline{CE}$	CS_1, CS_2, Address	$\overline{OE}$	OUTPUT	MODE
H	(1)	(1)	High Z	Standby
⌐	Valid	(1)	High Z	Latch
L	(2)	L	Data out	Read

Note (1) Don't care
(2) CS_1, CS_2, Address may change after t_{AH}.

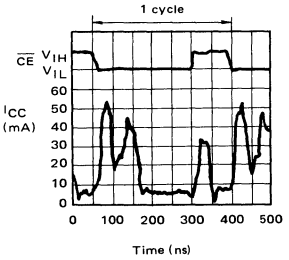
APPLICATION INFORMATION

1. POWER SUPPLY DECOUPLING

The operating current I_{CC} waveforms for TMM2364P are shown in Fig. 1, 2.

The TMM2364P is a clocked device, so the transient current peaks are produced on the $\overline{CE}$ transition and $\overline{CE}$ active level.

The I_{CC} current transients require adequate decoupling of V_{CC} power supply.



Fgi. 1 I_{CC} vs time (CS: Select)

2. POWER ON

The TMM2364P requires initialization prior to normal operation. Two initialization methods are as follows:

(1) A minimum 100 μs time delay is required after the application of V_{CC} (+5V) before proper device operation is achieved. And during this period, $\overline{CE}$ must be at V_{IH} level.

(2) A minimum 100 μs time delay is required after the application of V_{CC} (5V), and then a minimum of one initialization cycle must be performed before proper device operation is acheived.

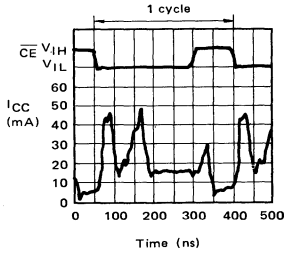


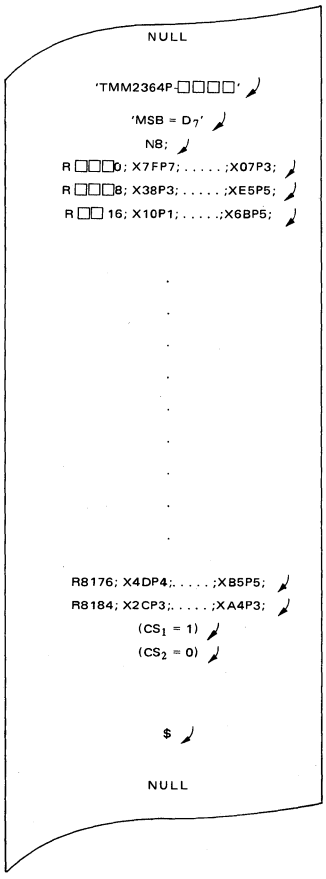
Fig. 2 I_{CC} vs time (CS: Deselect)

Initialization cycle: An initialization cycle is one Chip Enable clock cycle from the first down edge of the $\overline{CE}$ till the next down edge.

TOSHIBA PAPER TAPE FORMAT

Use 7 or 8-bit (even parity) ASCII code paper Tape for ROM data input.
Two acceptable formats which are described in section A and B are available.

A. Format 1 (when a check sum per word is used)



Preceding the first data field and following the last data field there must be a leader/trailer length of at least 50 null characters.

Contents in a single quotation mark (, ... ,) signify a comment and □ □ □ □ indicates a four-digit user pattern number.

↵ indicates carriage return and line feed.

Specify the most significant bit (MSB) of the device outputs (D_7 or D_0)

N8 indicates that the mask pattern is an 8-bit pattern.

Semicolon (;) signifies a punctuation of data.

R signifies an address. Enter the address with the four decimal digits every 8-words after the character R.

X signifies a hexadecimal digit.
Enter the data with the two hexadecimal digits every word after the character X.

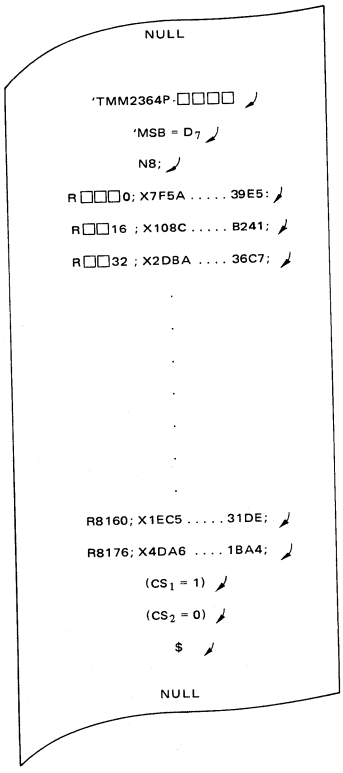
P signifies the check sum per word.
Enter the sum of 1 in a one word decimal after the character P.

* Data Modification
Modifying single and continuous word data can be carried out by specifying the modifying addresses and inputting the data following the above procedure before the end symbol.
Modification can be allowed from 0 to 8191 addresses.

Specify the active logic of chip selects (CS_1 and CS_2) in the parentheses respectively.
Enter "1" and "0" when active at high and low levels, respectively.
An example is shown in the left figure.
In this example, the device is selected under the condition that CS_1 and CS_2 are at high and low levels, respectively.

$ signifies the End symbol.

B. Format 2 (When a check sum per word is not used)



R signifies an address.
Enter the address with the four decimal digits every sixteen words after the character R.

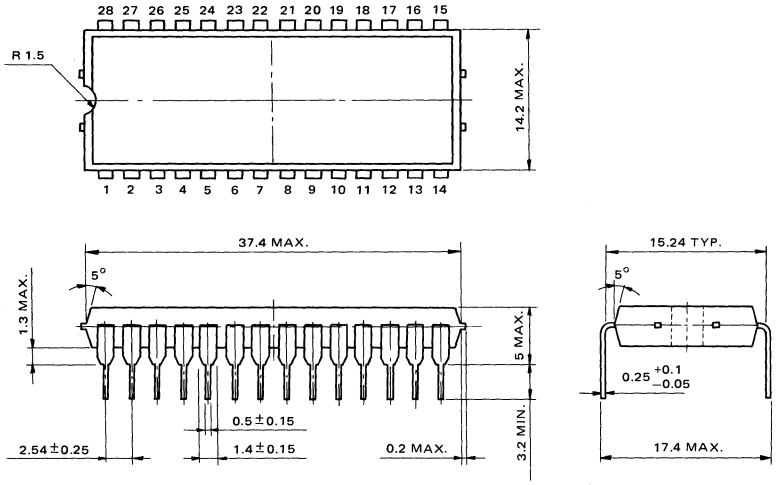
X signifies a hexadecimal digit.
Enter the data of sixteen words continuously after the character X.

Otherwise specified in Format 1.

In addition, Toshiba can also accept programming and masking information for TMM2364P in the form of punched paper tape with Intel BNPF format or master devices (EPROMs).

OUTLINE DRAWINGS

Unit: mm



Note: Each lead pitch is 2.54 mm.
All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

64K BIT (8K WORD x 8BIT) MASK ROM

N-CHANNEL SILICON GATE

TMM2365P

DESCRIPTION

The TMM2365P is a 65536 bit fully static read only memory organized as 8192 words by 8 bits with a low bit cost, thus being most suitable for use in programming of production apparatus using microprocessor.

The TMM2365P is fully compatible with a 64 K bits EPROM TMM2764D, so completely replace EPROM socket.

The TMM2365P also features an automatic standby power mode. When deselected by Chip Enable ($CE_{1\sim3}/\overline{CE_{1\sim3}}$), the operating current is reduced from 100mA (MAX) to 25mA(MAX). Output Enable ($\overline{OE}$) is effective in preventing data confliction of a common bus line.

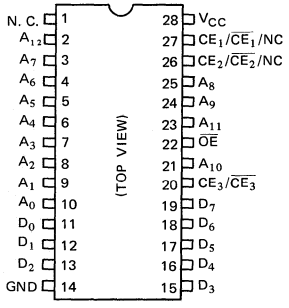
The TMM2365P is fabricated with ion implanted N-channel silicon gate technology. This technology allows a production of high performance.

The TMM2365P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

FEATURES

- Single 5V power Supply
- Access Time: 200ns max.
- Power Dissipation
  - Average Current: 100mA max.
  - Standby Current: 25mA max.
- Input and Output: TTL Compatible
- Three State Outputs: Wired OR Capability
- Output Buffer Control: $\overline{OE}$
- Programmable Chip Enable: $CE_1/\overline{CE_1}$, $CE_2/\overline{CE_2}$ $CE_3/\overline{CE_3}$
  - Easy Memory Expansion
- Compatible with 64K EPROM TMM2764D

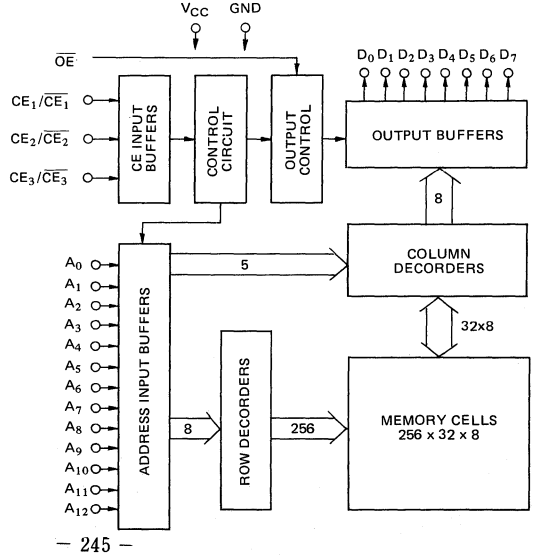
PIN CONNECTION



PIN NAMES

$A_0 \sim A_{12}$	Address inputs
$D_0 \sim D_7$	Data outputs
$\overline{OE}$	Output enable input
$CE_1/\overline{CE_1}$, $CE_2/\overline{CE_2}$, $CE_3/\overline{CE_3}$	Chip enable inputs
N. C.	No connection
V_{CC}	Power supply terminal
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input and Output Voltage	−0.5 ~ 7.0	V
T_{OPR}	Operating Temperature	0 ~ 70	°C
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{SD}	Soldering Temperature • Time	260 • 10	°C • sec
P_D	Power Dissipation (Ta = 70°C)	1.0	W

D.C. OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	–	2.0	–	V_{CC}+1	V
V_{IL}	Input Low Voltage	–	−0.5	–	0.8	V
V_{CC}	Power Supply Voltage	–	4.5	5.0	5.5	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IH}	Input High Current	V_{IN} = 5.5V	–	10	μA
I_{IL}	Input Low Current	V_{IN} = GND	–	−10	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA	2.4	–	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA	–	0.4	V
I_{LO}	Output Leakage Current	$0V \leqq V_{OUT} \leqq Vcc$	−10	10	μA
I_{CC1}	Standby Current	$\overline{CE}$ = 2.0V, CE = 0.8V	–	25	mA
I_{CC2}	Average Current	t_{CYC}=200nS, I_{OUT}=0mA	–	100	mA

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Access Time	–	200	ns
t_{CE}	Output Delay Time from CE/$\overline{CE}$	–	200	ns
t_{OE}	Output Delay Time from $\overline{OE}$	–	70	ns
t_{OD}	Output Turn off Delay	–	60	ns
t_{CYC}	Cycle Time	200	–	ns

A.C. TEST CONDITIONS

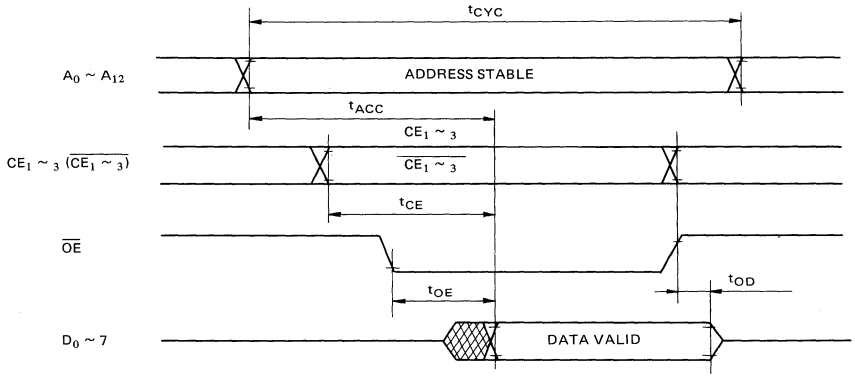
- Output Load : 1TTL Gate + 100pF
- Input Rise and Fall Times (10% ~ 90%) : 5 ns
- Input Pulse Levels : 0.8 ~ 2.2V
- Timing Measurement Reference Levels :
  Input ; 1V and 2.0V
  Output; 0.8V and 2.0V

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = A.C. GND	–	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = A.C. GND	–	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS

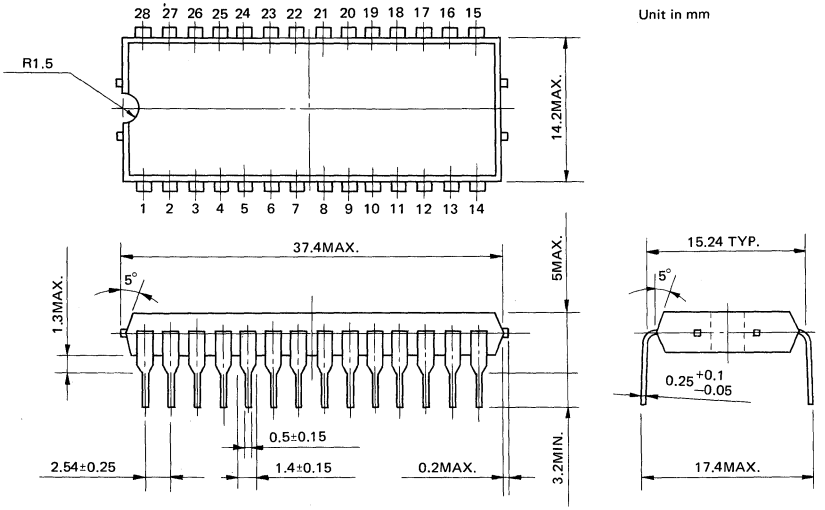


Note: t_{OD} is specified from $\overline{OE}$ or CE/$\overline{CE}$, whichever occurs first.

POWER ON

The TMM2365 has self substrate-bias generator internally. So a minimum 100μs time delay is required after the application of V_{CC} (4.5 ~ 5.5V) before proper device operation is achieved.

OUTLINE DRAWINGS



Unit in mm

Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No. 28 leads

TOSHIBA MOS MEMORY PRODUCTS

64K BIT (8K WORD x 8 BIT) MASK ROM

N-CHANNEL SILICON GATE MOS

TMM2366P

DESCRIPTION

The TMM2366P is a 65536 bit fully static read only memory organized as 8192 words by 8 bits with a low bit cost, thus being most suitable for use in programming of production apparatus using microprocessor.

The TMM2366P also features an automatic standby power mode. When deselected by Chip Enable (CE/$\overline{CE}$), the operating current is reduced from 100mA (MAX) to 25mA (MAX).

The TMM2366P is fabricated with ion implanted N-channel silicon gate technology.

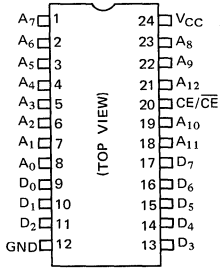
This technology allows a production of high performance.

The TMM2366P is moulded in a 24 pin standard plastic package, 0.6 inch in width.

FEATURES

- Single 5V power Supply
- Access Time: 200ns max.
- Power Dissipation
  Average Current: 100mA max.
  Standby Current: 25mA max.
- Input and Output: TTL Compatible
- Three State Outputs: Wired OR Capability
- Programmable Chip Enable: CE/$\overline{CE}$
- Compatible with TMS4764

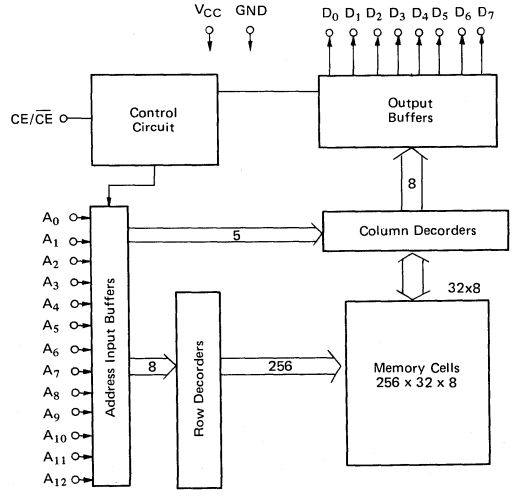
PIN CONNECTION



PIN NAMES

$A_0 \sim A_{12}$	Address inputs
$D_0 \sim D_7$	Data outputs
CE/$\overline{CE}$	Chip enable input
V_{CC}	Power supply terminal
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input and Output Voltage	−0.5 ~ 7.0	V
T_{OPR}	Operating Temperature	0 ~ 70	°C
T_{STRG}	Storage Temperature	−55 ~ 150	°C
T_{SD}	Soldering Temperature Time	260 • 10	°C • sec
P_D	Power Dissipation (Ta = 70°C)	1.0	W

D.C. OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	–	2.0	–	V_{CC}+1	V
V_{IL}	Input Low Voltage	–	−0.5	–	0.8	V
V_{CC}	Power Supply Voltage	–	4.5	5.0	5.5	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IH}	Input High Current	V_{IN} = 5.5V	–	10	μA
I_{IL}	Input Low Current	V_{IN} = GND	–	−10	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA	2.4	–	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA	–	0.4	V
I_{LO}	Output Leakage Current	$OV \leqq V_{OUT} \leqq V_{CC}$	−10	10	μA
I_{CC1}	Standby Current	$\overline{CE}$ = 2.0V, CE = 0.8V	–	25	mA
I_{CC2}	Average Current	t_{CYC} = 200ns, I_{OUT} = 0mA	–	100	mA

A.C. CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Access Time	–	200	ns
t_{CE}	Output Delay Time from CE/$\overline{CE}$	–	200	ns
t_{OD}	Output Turn off Delay	–	60	ns
t_{CYC}	Cycle Time	200	–	ns

A.C. TEST CONDITIONS

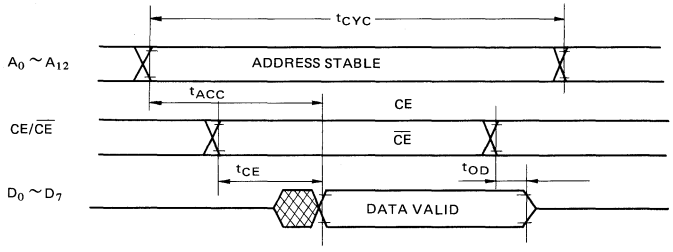
- Output Load : 1TTL Gate + 100pF
- Input Rise and Fall Times (10% ~ 90%) : 5 ns
- Input Pulse Levels : 0.8 ~ 2.2V
- Timing Measurement Reference Levels : Input; 1V and 2.0V
  Output; 0.8V and 2.0V

CAPACITANCE ($Ta = 25°C$, $f = 1MHz$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitnace	V_{IN} = A.C. GND	–	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = A.C. GND	–	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

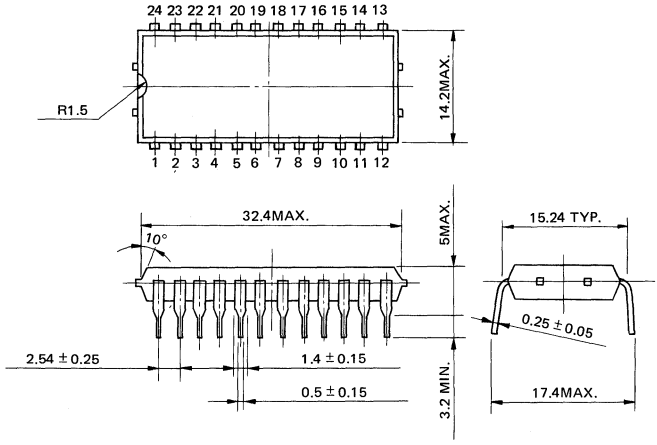
TIMING WAVEFORMS



POWER ON

The TMM2366 has a self substrate-bias generator internaly. So a minimum 100 μs time delay is required after the application of V_{CC} (4.5 ~ 5.5V) before proper device operation is achieved.

OUTLINE DRAWING



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm longituidnal position with respect to No. 1 and No. 24 leads.
All dimensions are in millimeters.

Distributed by

16,384 Word x 8 Bit Mask ROM

N-CHANNEL SILICON GATE MOS

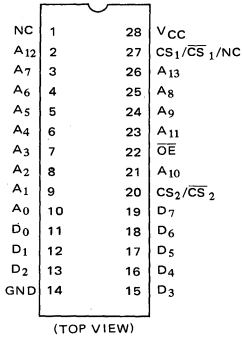
TMM23128P

PRELIMINARY

FEATURES

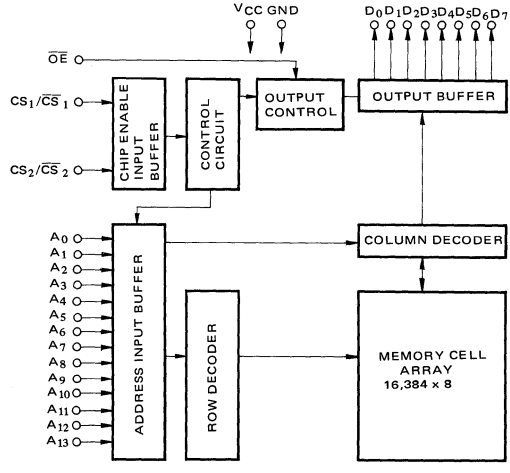
- Fully Static Operation
- 16,384 word x 8 bit Structure
- Single 5V Power Supply
- t_{ACC} = 200 ns max.
- T_{opr} = 0 ~ 70°C
- I_{CC} ope = 80 mA max.
- I_{CC} sby = 20 mA max.
- Input and Output: TTL Compatible
- Three State Outputs
- Programmable Chip Select
- Pin compatible with EPROM TMM27128
- 28 pin 600 mil. Width DIP Plastic Package

PIN CONNECTION



(TOP VIEW)

BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{13}$	Address Inputs
$D_0 \sim D_7$	Data Outputs
$CS_1 \sim {}_2/\overline{CS}_1 \sim {}_2$	Chip Select Inputs
$\overline{OE}$	Output Enable Input
N.C.	No Connection
V_{CC}	5 V Power Supply
GND	Ground

TMM23256P 256K BIT (32K WORD x 8 BIT) MASK ROM

N-CHANNEL SILICON GATE

TMM23256P

DESCRIPTION

The TMM23256P is a 262,144 bit read only memory organized as 32,768 words by 8 bits with a low bit cost, thus being most suitable for use in character generator.

Consisting of static memory cells and clocked peripheral circuitry, the TMM23256P provides a high speed and low power dissipation (access time 150ns, operating current 40mA).

The TMM23256P also features an automatic stand-by power mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced from 40mA to 10mA. Output Enable ($\overline{OE}$) is effective in preventing data confliction on a common bys line.

The TMM23256P uses the address latch system that the falling edge of $\overline{CE}$ latches all inputs except for $\overline{OE}$, thus can be easily connected to a system where address and data buses are commonly used.

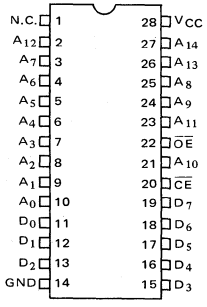
The TMM23256P is fabricated with ion implanted N-channel silicon gate technology. This technology allows a production on high performance.

The TMM23256P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

FEATURES

- Single 5V Power Supply
- Fast Access Time : 150ns (Max.)
- Low Power Dissipation
  - Average Current : 40mA (Max.)
  - Standby Current : 10mA (Max.)
- Inputs protected : All Inputs have Protection Against Static Charge
- Edge Enabled Operation : $\overline{CE}$
- Output Buffer Control : $\overline{OE}$
- Input and Output : TTL Compatible
- Three State Outputs : Wired OR Capability
- 28 pin Standard Plastic DIP

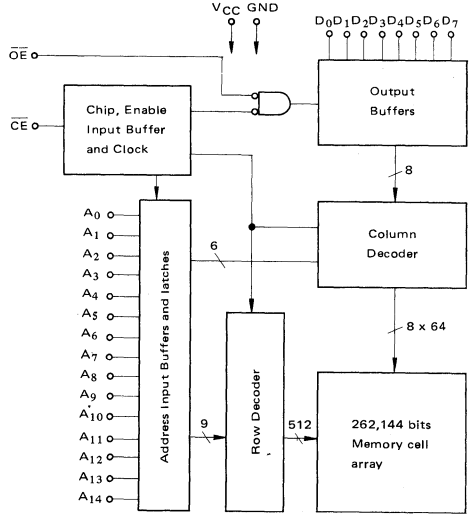
PIN CONNECTION



PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$D_0 \sim D_7$	Data Outputs
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
N.C.	No Connection
V_{CC}	Power Supply Terminal
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input and Output Voltage	−0.5 ~ 7.0	V
T_{OPR}	Operating Temperature	0 ~ 70	°C
T_{STRG}	Storage Temperature	−55 ~ 150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
P_D	Power Dissipation (Ta = 70°C)	1.0	W

D.C. OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	—	2.2	—	V_{CC} + 1	V
V_{IL}	Input Low Voltage	—	−0.5	—	0.8	V
V_{CC}	Power Supply Voltage	—	4.5	5.0	5.5	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
I_{IH}	Input High Current	V_{IN} = 5.5V		—	0.05	10	μA
I_{IL}	Input Low Current	V_{IN} = GND		—	−0.05	−10	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA		2.4	3.3	—	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA		—	0.3	0.4	V
I_{LOH}	Output Leakage Current	V_{OUT} = 5.5V	$\overline{CE}$ = 2.2V or	—	0.05	10	μA
I_{LOL}		V_{OUT} = 0.4V	$\overline{OE}$ = 2.2V	—	−0.1	−20	μA
I_{CC1}	Standby Current	$\overline{CE}$ = 2.2V		—	—	10	mA
I_{CC2}	Average Current	t_{CYC} = 230ns, I_{OUT} = 0mA		—	—	40	mA

• Typical values are at Ta = 25°C and V_{CC} = 5V.

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = A.C. GND	—	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = A.C. GND	—	8	15	pF

Note : This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%)

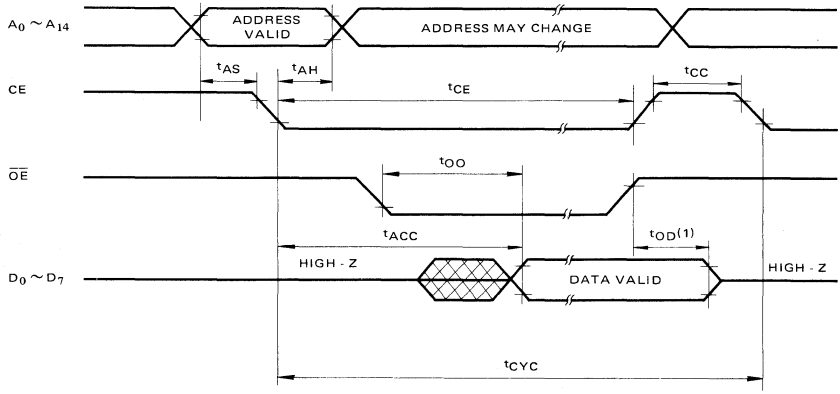
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{CE}	$\overline{CE}$ pulse width	–	150	–	–	ns
t_{AS}	Address Setup Time	–	0	–	–	ns
t_{AH}	Address Hold Time	–	30	–	–	ns
t_{ACC}	Access Time	–	–	–	150	ns
t_{OO}	Output Delay Time form $\overline{OE}$	–	–	–	70	ns
t_{OD}	Output Turn off Delay	–	–	–	70	ns
t_{CC}	$\overline{CE}$ off Time	–	70	–	–	ns
t_{CYC}	Cycle Time	t_{AS} = 0ns, t_r, t_f = 5ns	230	–	–	ns

- Typical values are at Ta = 25°C and V_{CC} = 5V.

A.C. TEST CONDITIONS

- Output Load : 1TTL Gate + 100pF
- Input Rise and Fall Times (10% ~ 90%) : 5ns
- Input Pulse Levels : 0.8 ~ 2.4V
- Timing Measurement Reference Levels : Input ; 1V and 2.2V
  Output ; 0.8V and 2.0V

TIMING WAVEFORMS



Note (1) t_{OD} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

OPERATION INFORMATION

The TMM23256P has two control functions.

The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The falling edge of the $\overline{CE}$ will activate the device and latch the addresses. The output enable ($\overline{OE}$) control the output buffers, independent of device selection. Assuming that $\overline{OE}$ = V_{IL}, the output data is valid at the outputs after t_{ACC} (150ns) from the falling edge of the $\overline{CE}$.

The operation modes of the TMM23256P are listed in the following table.

MODE	$\overline{CE}$	ADDRESS	$\overline{OE}$	OUTPUT	POWER
Standby	H	*	*	High Impedance	Standby
Latch	⊓_	Valid	*	High Impedance	–
Read	L	**	L	Data Out	Active
Output Deselect	L	*	H	High Impedance	Active

Note * : Don't care

** : Address may change after t_{AH}.

APPLICATION INFORMATION

1. POWER SUPPLY DECOUPLING

The operating current I_{CC} waveforms for TMM 23256P are shown in Fig. 1, 2.

The TMM23256P is a clocked device, so the transient current peaks are produced on the $\overline{CE}$ transition and $\overline{CE}$ active level.

The I_{CC} current transients require adequate decoupling of V_{CC} power supply.

2. POWER ON

The TMM23256P requires initialization prior to normal operation. Two initialization methods are as follows:

(1) A minimum 100μs time delay is required after the application of V_{CC} (+5V) before proper device operation is achieved. And during this period, $\overline{CE}$ must be at V_{IH} level.

(2) A minimum 100μs time delay is required after the application of V_{CC} (5V), and then a minimum of one initialization cycle must be performed before proper device operation is acheived.

Initialization cycle : An initialization cycle is one Chip Enable clock cycle from the first down edge of the $\overline{CE}$ till the next down edge.

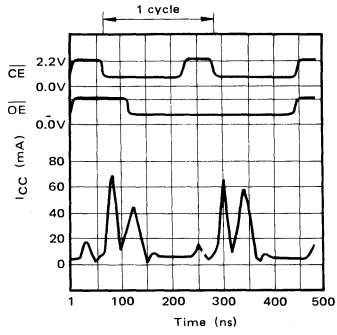


Fig. 1 I_{CC} vs. Time (1)

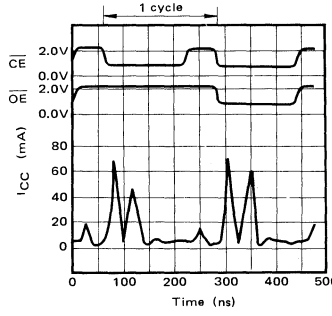
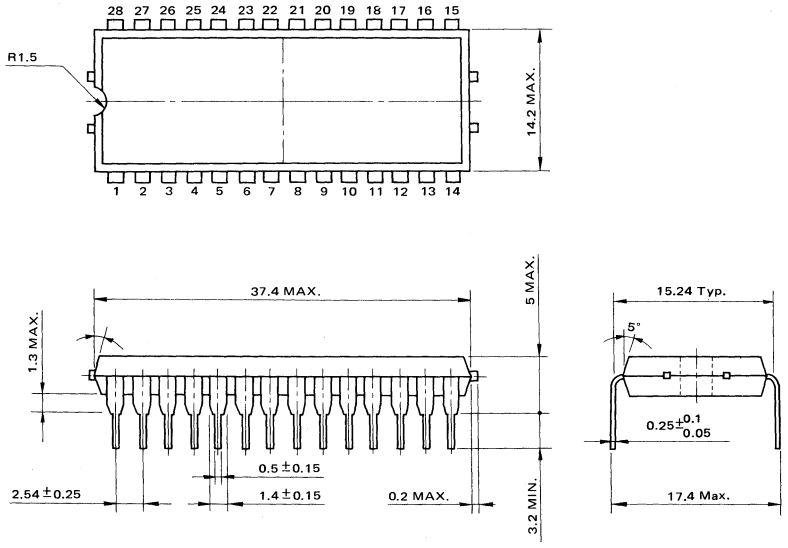


Fig. 2 I_{CC} vs. Time (2)

OUTLINE DRAWINGS

Unit : mm

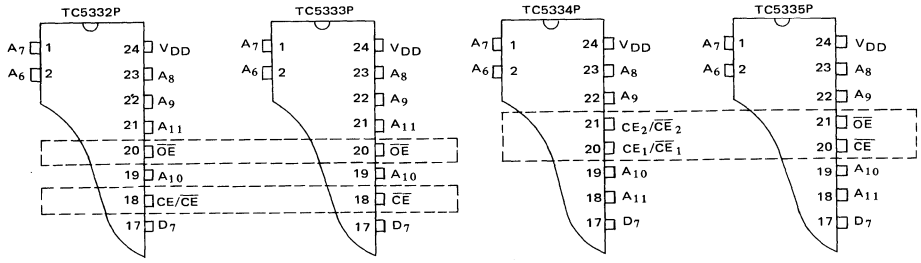


Note: Each lead pitch is 2.54 mm.
All leads are located within 0.25 mm of their true lingitudinal position with respect to No. 1 and No. 28 leads.

MOS Mask Programble Read Only Memory

32 K Bit CMOS MASK ROM COMPARISON TABLE

PIN CONFIGURATION



Operation Mode Table

Pin Name / Number	TC5332P CE/CE (18)	TC5332P OE (20)	TC5332P Addresses	TC5332P Outputs	TC5332P Power	TC5333P CE (18)	TC5333P OE (20)	TC5333P Addresses	TC5333P Outputs	TC5333P Power
Address Latch						↓	*	Valid	High-Z	–
Read	H/L	L	Valid	Dout	Active	L	L	*	Dout	Active
Standby	L/H	*	*	High-Z	Standby	H	*	*	High-Z	Standby
Output Deselect	H/L	H	*	High-Z	Active	L	H	*	High-Z	Active
Operation Mode	Fully Static Operation (Asynchronous Type)					Address Latched Operation (Synchornous Type)				

Pin Name / Number	TC5334P CE1/CE1 (20)	TC5334P CE2/CE2 (21)	TC5334P Addresses	TC5334P Outputs	TC5334P Power	TC5335P CE (20)	TC5335P OE (21)	TC5335P Addresses	TC5335P Outputs	TC5335P Power
Addresses Latch						↓	*	Valid	High-Z	–
Read	H/L	H/L	Valid	Dout	Active	L	L	*	Dout	Active
Standby 1	L/H	*	*	High-Z	Standby	H	*	*	High-Z	Standby
Standby 2	*	L/H	*	High-Z	Standby					
Output Deselect						L	H	*	High-Z	Active
Operation Mode	Fully Static Operation (Asynchronous Type)					Address Latched Operation (Synchronous Type)				

4K WORD x 8 BIT CMOS MASK ROM

SILICON GATE CMOS

TC5332P

DESCRIPTION

The TC5332P is a 32,768 bit low power read only memory organized as 4,096 words by 8 bits using CMOS technology, and operates from a single 5V supply.

The TC5332P has a programmable chip enable input ($CE/\overline{CE}$) for device selection and a output enable input ($\overline{OE}$) for fast access and output control. The maximum access times from address and chip enable are both 450 ns.

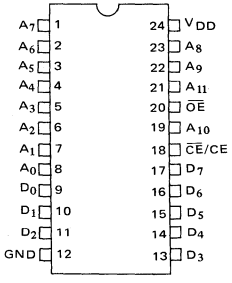
The TC5332P is pin compatible with the industry produced NMOS ROM TMM2332P, yet offers a more than 90% reduction in power of their NMOS equivalent. The TC5332P's maximum operating and standby current is 7mA and 20μA, respectively. Thus the TC5332P is most suitable for use in low power applications such as battery operated system.

The TC5332P is molded in a 24 pin standard plastic package.

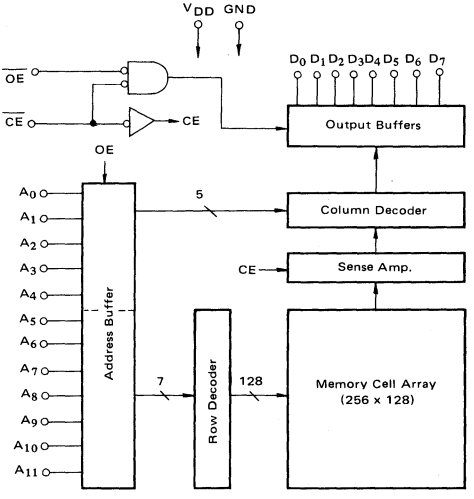
FEATURES

- Access Time: 450ns
- Low Power Dissipation
  I_{DDO} = 7mA (Max.) : Operating
  I_{DDS} = 20μA (Max.) : Standby
- All Inputs and Outputs: TTL Compatible
- Three state outputs
- Fully Static Operation
- Two Control Functions: $\overline{CE}/CE$, $\overline{OE}$
- Programmable Chip Enable: $\overline{CE}/CE$
- Output Control: $\overline{OE}$
- Pin Compatible with TMM2332P and TMM2732D
- Standard 24 pin Plastic Package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{11}$	ADDRESS INPUTS
$D_0 \sim D_7$	DATA OUTPUTS
$CE/\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
V_{DD}	POWER (+5V)
GND	GROUND

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	-0.3V ~ 7.0V
V_{IN}	Input Voltage	-0.3V ~ 7.0V
V_{OUT}	Input/Output Voltage	0V ~ V_{DD}
P_D	Power Dissipation (Ta = 85°C)	0.8W
T_{STG}	Storage Temperature	-55°C ~ 150°C
T_{OPR}	Operating Temperature	-40°C ~ 85°C
T_{SOLDER}	Soldering Temperature • Time	260°C ~ 10 sec

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = -40°C ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	–	0.8	V

D.C. CHARACTERISTICS (Ta = -40°C ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Load Current	$0 \leqq V_{IN} \leqq V_{DD}$	–	–	±1.0	μA
I_{LO}	Output Leakage Current	CE = V_{IL} ($\overline{CE}$ = V_{IH}), $0V \leqq V_{out} \leqq V_{DD}$	–	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	-1.0	-4.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	4.0	–	mA
I_{DDS1}	Standby Supply Current	CE = 0.8V ($\overline{CE}$ = 2.2V)	–	0.5	2.0	mA
I_{DDS2}		CE = 0.2V ($\overline{CE}$ = V_{DD} – 0.2V)	–	0.05	20	μA
I_{DDO1}	Operating Supply Current	CE = V_{IH} ($\overline{CE}$ = V_{IL}), t_{cyc} = 1μs, V_{IN} = V_{IH}/V_{IL}, I_{out} = 0mA	–	6.0	10.0	mA
I_{DDO2}		CE = V_{DD} ($\overline{CE}$ = 0V), t_{cyc} = 1μs, V_{IN} = V_{DD}/GND, I_{out} = 0mA	–	4.0	7.0	mA

Note: Typical values are at Ta = 25°C, V_{DD} = 5V.

CAPACITANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	–	5	10	pF
C_{out}	Output Capacitance	–	5	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

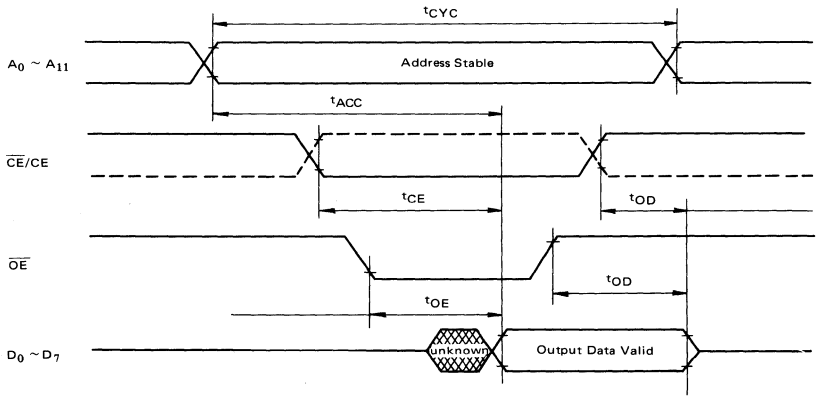
A.C. CHARACTERISTICS (Ta = -40 ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{ACC}	Address Access Time	–	–	450	ns
t_{CE}	Chip Enable Access Time	–	–	450	ns
t_{OE}	Output Enable Access Time	–	–	150	ns
t_{OD}	Output Desable Time	–	–	100	ns
t_{CYC}	Cycle Time	450	–	–	ns

A.C. TEST CONDITIONS

- Output Load : 100pF + 1TTL Gate
- Input Pulse Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels
  - Input : 0.8V and 2.2V
  - Output : 0.8V and 2.2V
- Input Pulse Rise and Fall Times : 10ns

TIMING WAVEFORMS

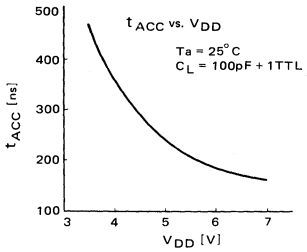


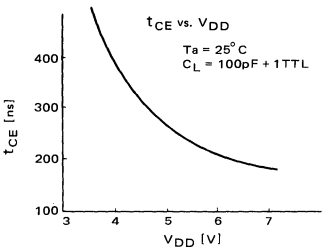
OPERATION MODE

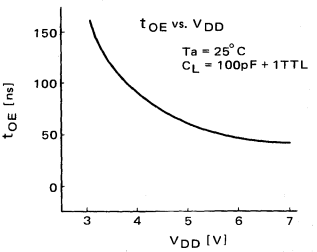
MODE	CE/$\overline{CE}$	$\overline{OE}$	ADDRESS	OUTPUTS
Read	H (L)	L	Valid	Data out
Standby	L (H)	*	*	High Z

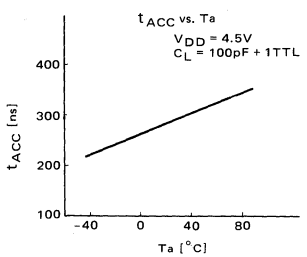
* : Don't care

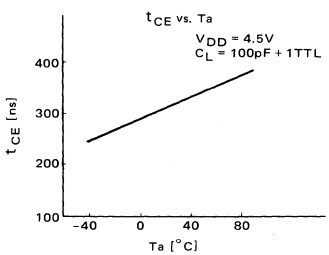
TYPICAL CHARACTERISTICS

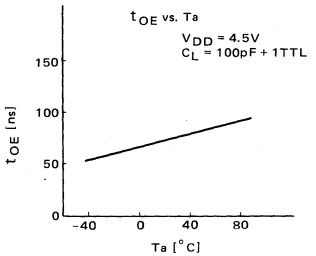


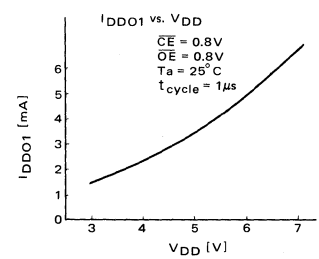


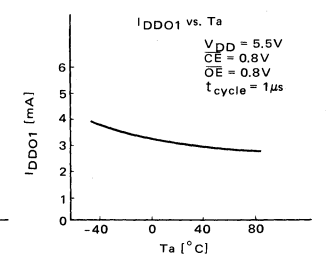


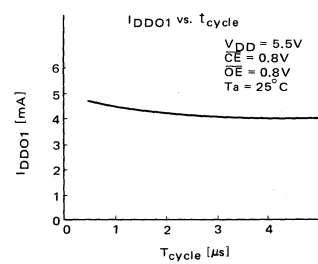


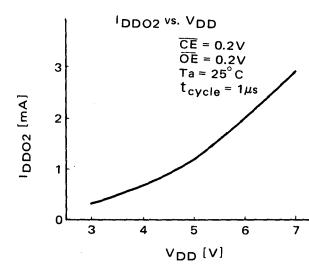


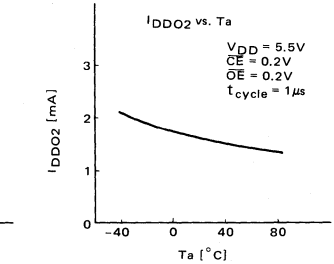


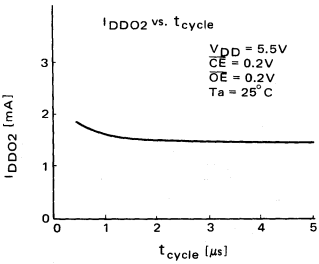


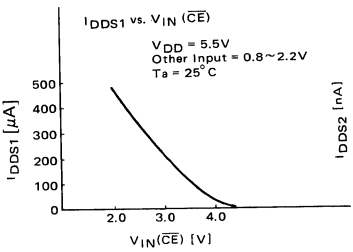


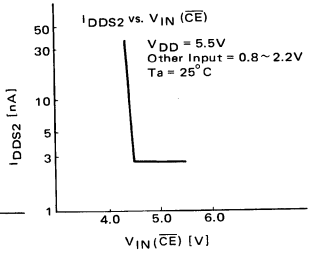


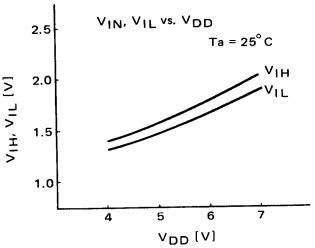


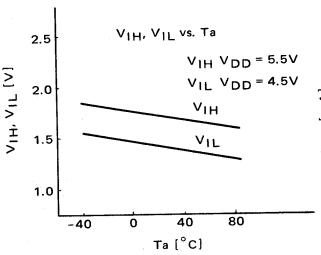


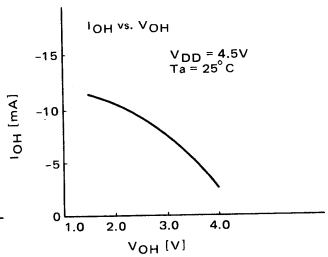


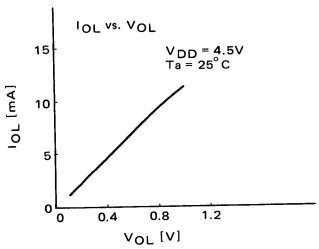

I_{DDS1} vs. V_{IN} ($\overline{CE}$)
V_{DD} = 5.5V
Other Input = 0.8~2.2V
Ta = 25°C
I_{DDS1} [μA]
500
400
300
200
100
0
2.0
3.0
4.0
V_{IN}($\overline{CE}$) [V]

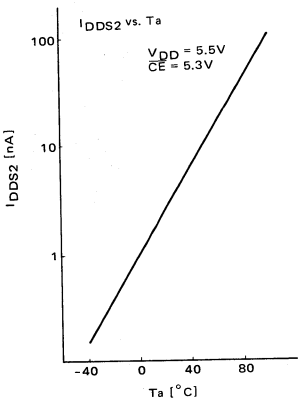

I_{DDS2} vs. V_{IN} ($\overline{CE}$)
V_{DD} = 5.5V
Other Input = 0.8~2.2V
Ta = 25°C
I_{DDS2} [nA]
50
30
10
5
3
1
4.0
5.0
6.0
V_{IN}($\overline{CE}$) [V]


V_{IN}, V_{IL} vs. V_{DD}
Ta = 25°C
V_{IH}
V_{IL}
V_{IH}, V_{IL} [V]
2.5
2.0
1.5
1.0
4
5
6
7
V_{DD} [V]


V_{IH}, V_{IL} vs. Ta
V_{IH} V_{DD} = 5.5V
V_{IL} V_{DD} = 4.5V
V_{IH}
V_{IL}
V_{IH}, V_{IL} [V]
2.5
2.0
1.5
1.0
-40
0
40
80
Ta [°C]


I_{OH} vs. V_{OH}
V_{DD} = 4.5V
Ta = 25°C
I_{OH} [mA]
-15
-10
-5
0
1.0
2.0
3.0
4.0
V_{OH} [V]

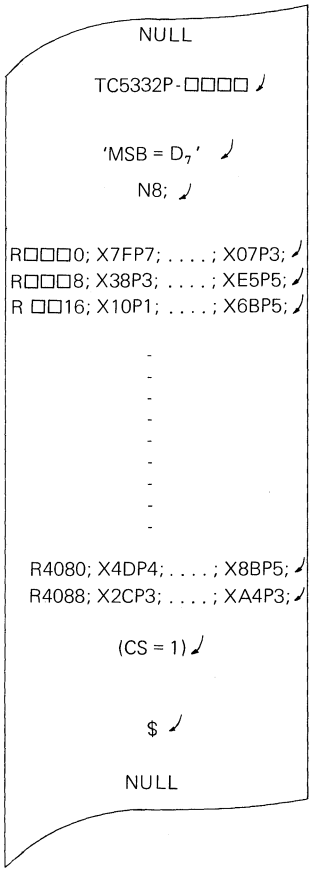

I_{OL} vs. V_{OL}
V_{DD} = 4.5V
Ta = 25°C
I_{OL} [mA]
15
10
5
0
0
0.4
0.8
1.2
V_{OL} [V]


I_{DDS2} vs. Ta
V_{DD} = 5.5V
$\overline{CE}$ = 5.3V
I_{DDS2} [nA]
100
10
1
-40
0
40
80
Ta [°C]

TOSHIBA PAPER TAPE FORMAT

Use 7 or 8-bit (even parity) ASCII code paper tape for ROM data input. Two acceptable formats which are described in section A and B are available.

A. Format 1 (when a check sum per word is used)



Preceding the first data field and following the last data field there must be a leader/trailer length of a least 50 null characters.

Contents in a single quotation mark (, ... ,) signify a comment and □ □ □ □ indicates a four-digit user pattern number.

↵ indicates carriage return and line feed.

Specify the most significant bit (MSB) of the device outputs (D_7 or D_0) N8 indicates that the mask pattern is an 8-bit pattern.

Semicolon (;) signifies a punctuation of data.

R signifies an address. Enter the address with the four decimal digits every 8-words after the character R.

X signifies a hexadecimal digit.
Enter the data with the two hexadecimal digits every word after the character X.

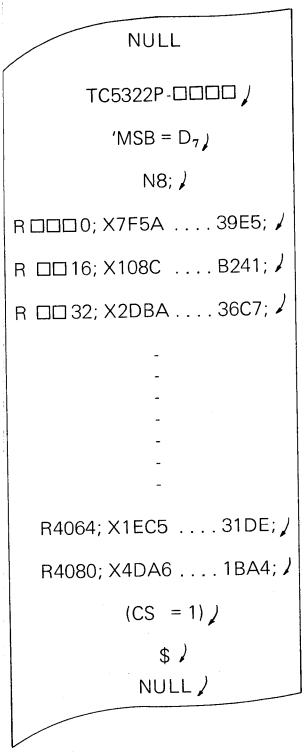
P signifies the check sum per word.
Enter the sum of 1 in a one word decimal after the character P.

* Data Modification
Modifying single and continuous word data can be carried out by specifying the modifying addresses and inputting the data following the above procedure before the end symbol.
Modification can be allowed from 0 to 4095 addresses.

Specify the active logic of chip enable $\overline{CE}$/CE (18PIN) in the parentheses. Enter CS = 1 and CS = 0 when active logic of chip enable is at high and low levels, respectively.
An example is shown in the left figure.
In this example the device is selected under the condition that $\overline{CE}$/CE is at high level.

$ signifies the End symbol.

B. Format 2 (When a check sum per word is not used)



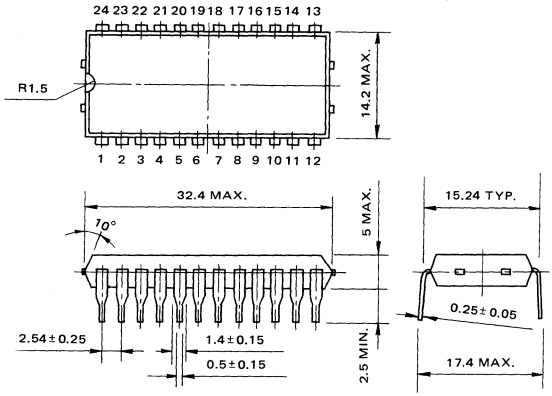
R signifies an address.
Enter the address with the four decimal digits every sixteen words after the character R.

X signifies a hexadecimal digit.
Enter the data of sixteen words continuously after the character X.

Otherwise specified in Format 1.

In addition, Toshiba can also accept programming and masking information for TC5332P in the form of punched paper tape with Intel BNPF format or master devices (EPROMs).

OUTLINE DRAWINGS



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 24 leads. All dimensions are in millimeters.

4,096 WORD X 8 BIT CMOS MASK ROM

SILICON GATE CMOS

TC5333P

DESCRIPTION

The TC5333P is a 32,768 bit low power read only memory organized as 4,096 words by 8 bits using CMOS technology, and operates from a single 5V supply.

The TC5333P has a chip enable input ($\overline{CE}$) for device selection and a output enable input ($\overline{OE}$) for fast memory access and output control. And the TC5333Puses the address latch system that the falling edge of $\overline{CE}$ latches all inputs except for $\overline{OE}$, thus can be connected to a system where address and data buses are commonly used. The maximum access time from chip enable is 450 ns.

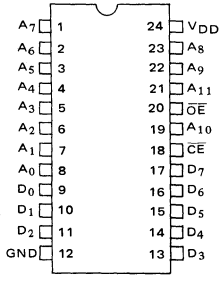
The TC5333P is pin compatible with the industry produced NMOS ROM TMM2332P, yet offers a more than 90% reduction in power of their NMOS equivalent. The TC5333P's maximum operating and standby current is 7 mA and 20 μA, respectively. Thus the TC5333P is most suitable for use in low power applications such as battery operated system.

The TC5333P is moulded in a 24 pin standard plastic package.

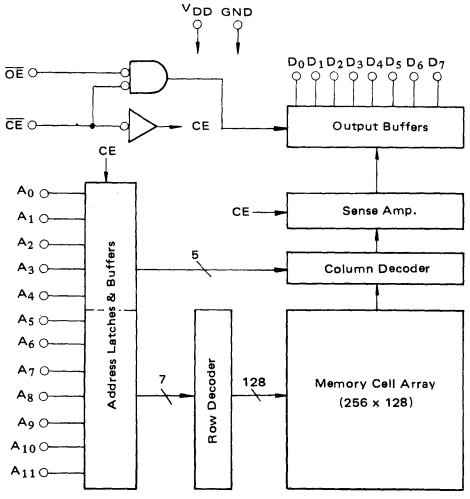
FEATURES

- Access Time: 450 ns
- Low Power Dissipation
  I_{DDO} = 7mA (Max.) : Operating
  I_{DDS} = 20μA (Max.) : Standby
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- Two Control Functions: $\overline{CE}$, $\overline{OE}$
- Address Latches: $\overline{CE}$
- Output Control: $\overline{OE}$
- Pin Compatible with TMM2332P and TMM2732D
- Standard 24 pin Plastic Package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 - A_{11}$	Address Inputs
$D_0 - D_7$	Data Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	−0.3V ~ 7.0V
V_{IN}	Input Voltage	−0.3V ~ 7.0V
V_{OUT}	Output Voltage	OV ~ V_{DD}
P_D	Power Dissipation (Ta = 85°C)	0.8W
T_{STG}	Storage Temperature	−55°C ~ 150°C
T_{OPR}	Operating Temperature	−40°C ~ 85°C
T_{SOLDER}	Soldering Temperature · Time	260°C · 10 sec

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = −40°C ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V

D.C. CHARACTERISTICS (Ta = −40°C ~ 85°C, V_{DD} = 5V ±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Load Current	$0 \leqq V_{IN} \leqq V_{DD}$	–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH}, OV ≦ V_{out} ≦ V_{DD}	–	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	−4.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	4.0	–	mA
I_{DDS1}	Standby Supply Current	$\overline{CE}$ = 2.2V other inputs = V_{IH} or V_{IL}	–	2.0	5.0	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} −0.2V other inputs = 0.2V or V_{DD} −0.2V	–	0.05	20	μA
I_{DDO1}	Operating Supply Current	$\overline{CE}$ = V_{IL}, t_{cyc} = 1 μs, V_{IN} = V_{IH}/V_{IL}, I_{out} = 0mA	–	6.0	10.0	mA
I_{DDO2}		$\overline{CE}$ = OV, t_{cyc} = 1μs, V_{IN} = V_{DD}/GND, I_{out} = 0mA	–	4.0	7.0	mA

Note: Typical values are at Ta = 25°C, V_{DD} = 5V.

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	–	5	10	pF
C_{OUT}	Output Capacitance	–	5	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

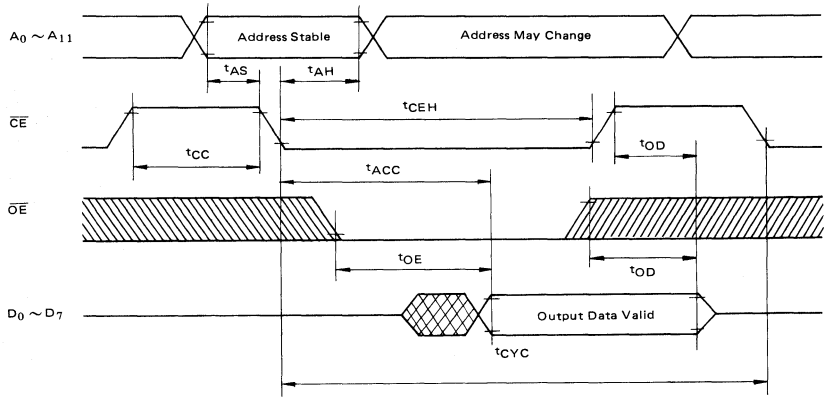
A.C. CHARACTERISTICS ($Ta = -40 \sim 85°C$ $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{ACC}	Chip Enable Access Time	–	–	450	ns
t_{OE}	Output Enable Access Time	–	–	150	ns
t_{AS}	Address Setup Time	30	–	–	ns
t_{AH}	Address Hold Time	30	–	–	ns
t_{CC}	$\overline{CE}$ OFF time	70	–	–	ns
t_{CEH}	Chip Enable Hold Time	450	–	–	ns
t_{OD}	Output Desable Time	–	–	100	ns
t_{CYC}	Cycle Time	540	–	–	ns

A.C. TEST CONDITIONS

- Output Load : 100pF + 1TTL Gate
- Input Pulse Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels
  - Input : 0.8V and 2.2V
  - Output : 0.8V and 2.2V
- Input Pulse Rise and Fall Times : 10 ns

TIMING WAVEFORMS



OPERATION MODE

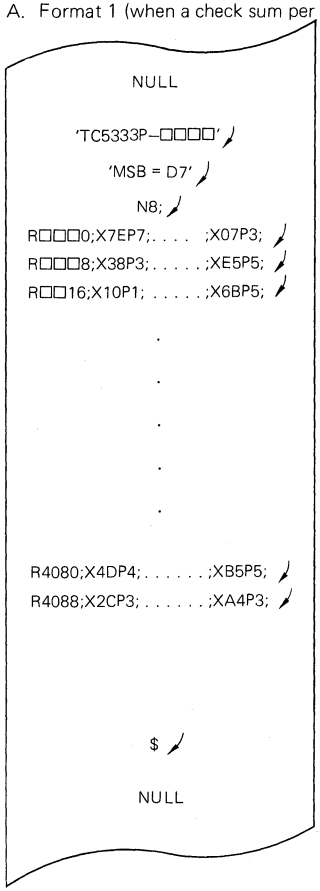
MODE	$\overline{CE}$	$\overline{OE}$	ADDRESS	OUTPUTS
Read	L	L	*	Data out
Standby	H	*	*	High Z
Address Latch	↓	*	Valid	High Z

* : Don't care.

TOSHIBA PAPER TAPE FORMAT

Use 7 or 8-bit (even parity) ASCII code paper tape for ROM data input.
Two acceptable formats which are described in section A and B are available.

A. Format 1 (when a check sum per word is used)

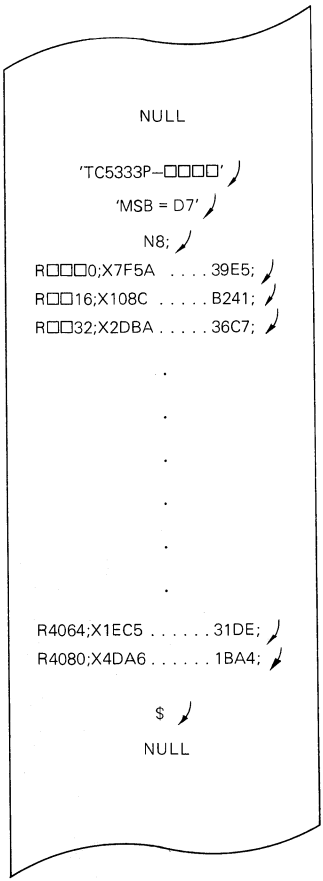


Preceding the first data field and follwing the last data field there must be a leader/trailer length of at least 50 null characters.
Contents in a single quotation mark (' . . . . . ') signify a comment and □□□□ indicates a four-digit user pattern number.
↵ indicates carriage return and line feed.
Specify,the most significant bit (MSB) of the device outputs (D_7 or D_0)
N8 indicates that the mask pattern is an 8-bit pattern.
Semicolon (;) signifies a punctuation of data.
R signifies an address. Enter the address with the four decimal digits every 8-words after the character R.
X signifies a hexadecimal digit.
Enter the data with the two hexadecimal digits every word after the character X.
P. signifies the check sum per word.
Enter the sum of 1 in a one word decimal after the character P.

* Data Modification
Modifying single and continuous word data can be carried out by specifying the modifying addresses and inputting data following the above procedure before the end symbol.
Modification can be allowed from 0 to 4095 addresses.

$ signifies the End symbol.

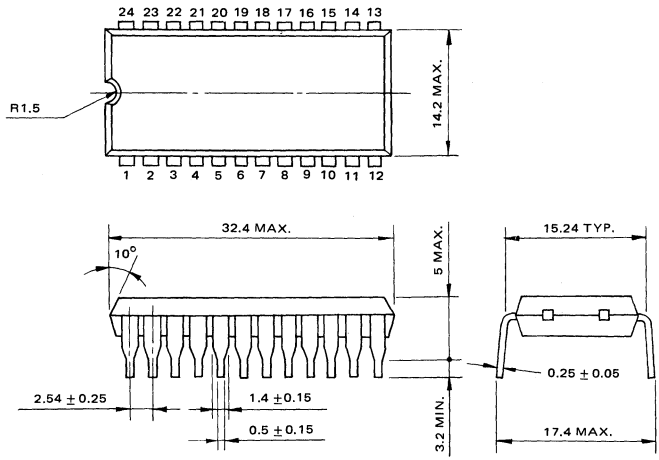
B. Format 2 (when a check sum per word fis not used)



R signifies an address.
Enter the address with the four decimal digits every sixteen words after the character R.
X signifies a hexadecimal digit.
Enter the data of sixteen words continuously after the character X.
Otherwise specified in Format 1.

In addition, Toshiba can also accept programming and masking information for TC5333P in the form of punched paper tape with Intel BNPF format or master devices (EPROMs).

OUTLINE DRAWINGS



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 24 leads.
All dimensions are in millimeters.

4,096 WORD x 8 BIT CMOS MASK ROM

SILICON GATE CMOS

TC5334P

DESCRIPTION

The TC5334P is a 32,768 bit low power read only memory organized as 4,096 words by 8 bits using CMOS technology, and operates from a single 5V supply.

The TC5334P has two programmable chip enable inputs ($\overline{CE}_1/CE_1$ and $\overline{CE}_2/CE_2$) for device selection. The maximum access times from address and chip enable are both 450 ns.

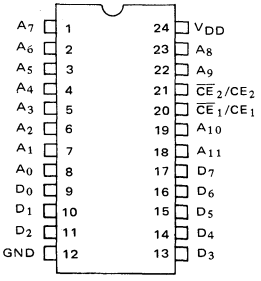
The TC5334P is pin compatible with the industry produced NMOS ROM TMM333P, yet offers a more than 90% reduction in power of their NMOS equivalent. The TC5334P's maximum operating and standby current is 7mA and 20μA, respectively. Thus the TC5334P is most suitable for use in low power applications such as battery operated system.

The TC5334P is molded in a 24 pin standard plastic package.

FEATURES

- Access Time: 450 ns
- Low Power Dissipation
  I_{DDO} = 7 mA (Max.) : Operating
  I_{DDS} = 20μA (Max.) : Standby
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- Fully Static Operation
- Two Programmable Chip Enables: $\overline{CE}_1/CE_1$, $\overline{CE}_2/CE_2$
- Pin Compatible with TMM333P
- Standard 24 pin Plastic Package

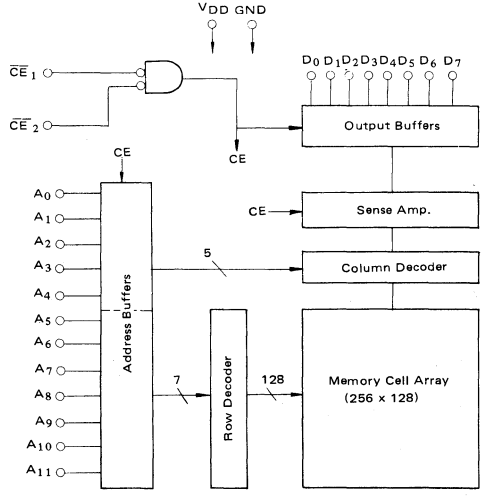
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 - A_{11}$	Address Inputs
$D_0 - D_7$	Data Outputs
$\overline{CE}_1/CE_1$ $\overline{CE}_2/CE_2$	Chip Enable Inputs
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	−0.3V ~ 7.0V
V_{IN}	Input Voltage	−0.3V ~ 7.0V
V_{OUT}	Output Voltage	0V ~ V_{DD}
P_D	Power Dissipation (Ta = 85°C)	0.8W
T_{STG}	Storage Temperature	−55°C ~ 150°C
T_{OPR}	Operating Temperature	−40°C ~ 85°C
T_{SOLDER}	Soldering Temperature · Time	260°C · 10 sec

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = −40°C ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V

D.C. CHARACTERISTICS (Ta = −40°C ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Load Current	$0 \leqq V_{IN} \leqq V_{DD}$	–	–	±1.0	μA
I_{LO}	Output Leakage Current	$CE = V_{IL}$ ($\overline{CE} = V_{IH}$), $0V \leqq V_{out} \leqq V_{DD}$	–	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	−4.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	4.0	–	mA
I_{DDS1}	Standby Supply Current	CE_1 = 0.8V or CE_2 = 0.8V ($\overline{CE}_1$ = 2.2V or $\overline{CE}_2$ = 2.2V)	–	0.5	5.0	mA
I_{DDS2}		CE_1 = 0.2V or CE_2 = 0.2V ($\overline{CE}_1 = V_{DD}$ −0.2V or $\overline{CE}_2 = V_{DD}$ −0.2V)	–	0.05	20	μA
I_{DDO1}	Operating Supply Current	$CE_1 = CE_2 = V_{IH}$ ($\overline{CE}_1 = \overline{CE}_2 = V_{IL}$) t_{CYC} = 1μs $V_{IN} = V_{IH}/V_{IL}$ I_{out} = 0mA	–	6.0	10.0	mA
I_{DDO2}		$CE_1 = CE_2 = V_{DD}$ ($\overline{CE}_1 = \overline{CE}_2$ = 0V) t_{CYC} = 1μs $V_{IN} = V_{DD}$/GND I_{out} = 0mA	–	4.0	7.0	mA

Note: Typical values are at Ta = 25°C, V_{DD} = 5V.

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	–	5	10	pF
C_{OUT}	Output Capacitance	–	5	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

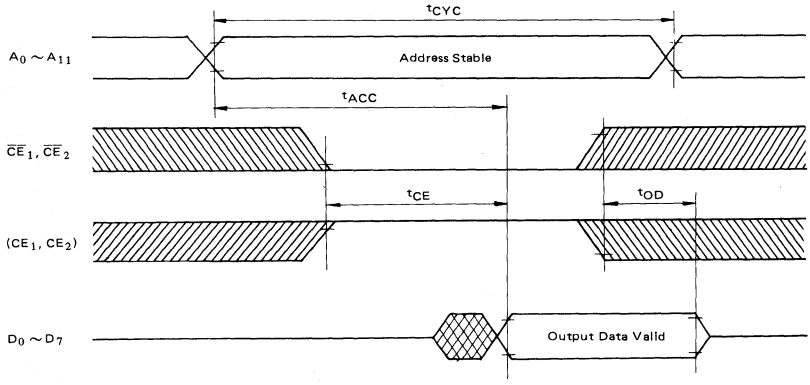
A.C. CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 5V ±10%)

SYMBOL	PARAMTER	MIN.	TYP.	MAX	UNIT
t_{ACC}	Address Access Time	—	—	450	ns
t_{CE}	Chip Enable Access Time	—	—	450	ns
t_{OD}	Out put Desable Time	—	—	100	ns
t_{CYC}	Cycle Time	450	—	—	ns

A.C. TEST CONDITIONS

- Output Load : 100pF + 1TTL Gate
- Input Pulse Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels
  Input : 0.8V and 2.2V
  Output : 0.8V and 2.2V
- Input Pulse Rise and Fall Times : 10 ns

TIMING WAVEFORMS



OPERATION MODE

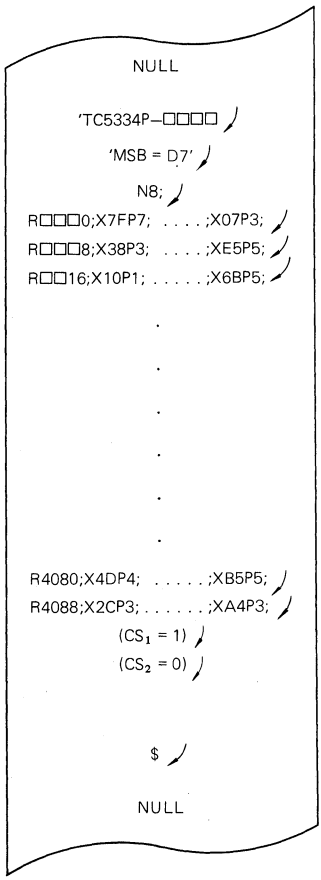
MODE	CE_1 ($\overline{CE}_1$)	CE_2 ($\overline{CE}_2$)	ADDRESS	OUTPUTS
Read	H(L)	H(L)	Valid	Data out
Standby	L(H)	*(*)	*	High Z
	*(*)	L(H)	*	High Z

* Don't care

TOSHIBA PAPER TAPE FORMAT

Use 7 or 8-bit (even parity) ASCII code paper tape for ROM data input.
Two acceptable formats which are described in section A and B are available.

A. Format 1 (when a check sum per word is used)



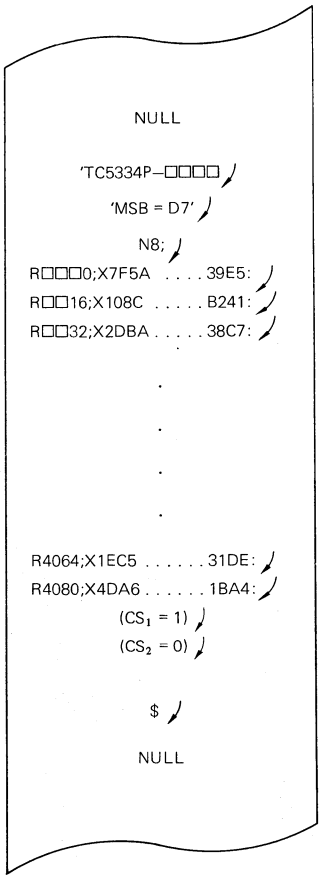
Preceding the first data field and following the last data field there must be a leader/trailer length of at least 50 null characters.
Contents in a single quotation mark ('. . . . . ') signify a comment and □□□□ indicates a four-digit user pattern number
↙ indicates carriage return and line feed.
Specify the most significant bit (MSB) of the device outputs (D_7 or D_0)
N8 indicates that the mask pattern is an 8-bit pattern.
Semicolon(;) signifies a punctuation of data.
R signifies an address. Enter the address with the four decimal digits every 8-words after the character R.
X signifies a hexadecimal digit.
Enter the data with the two hexadecimal digits every word after the character X.
P signifies the check sum per word.
Enter the sum of 1 in a one word decimal after the character P.

* Data Modification
Modifying single and continuous word data can be carried out by specifying the modifying addresses and inputting data following the above procedure before the end symbol.
Modification can be allowed from 0 to 4095 addresses.

Specify the active logic of chip enables $\overline{CE}_1/CE_1$ (20 PIN) and $\overline{CE}_2/CE_2$ (21 PIN) in the parentheses respectively.
Enter CS1 = 1 or CS1 = 0 when active logic of $\overline{CE}_1/CE_1$ is at high or low levels, respectively.
Enter CS2 = 1 or CS2 = 0 when active logic of $\overline{CE}_2/CE_2$ is at high or low levels, respectively.
An example is shown in the left figure.
In this example, the device is selected under the condition that $\overline{CE}_1/CE_1$ and $\overline{CE}_2/CE_2$ are at high and low levels, respectively.

$ signifies the End symbol.

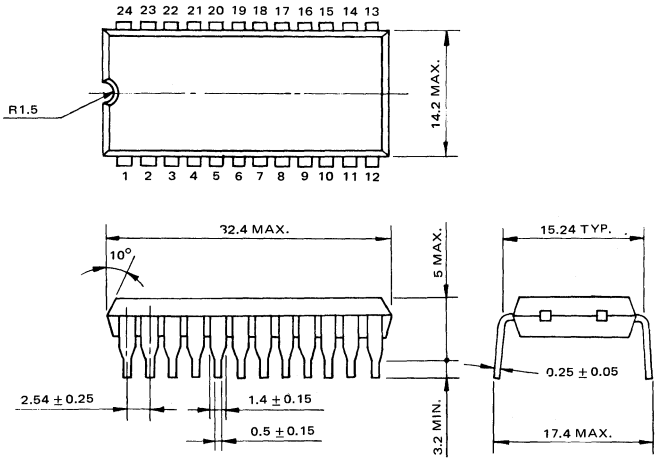
B. Format 2 (when a check sum per word is not used)



R signifies an address.
Enter the address with the four decimal digits every sixteen words after the character R.
X signifies a hexadecimal digit.
Enter the data of sixteen words continuously after the character X.
Otherwise specified in Format 1

In additon, Toshiba can also accept programming and masking information for TC5334P in the form of punched paper tape with Intel BNPF format or master devices (EPROMs).

OUTLINE DRAWINGS



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 24 leads. All dimensions are in millimeters.

TOSHIBA MOS MEMORY PRODUCTS

4,096 WORD x 8 BIT CMOS MASK ROM

SILICON GATE CMOS

TC5335P

DESCRIPTION

The TC5335P is a 32,768 bit low power read only memory organized as 4,096 words by 8 bits using CMOS technology, and operates from a single 5V supply.

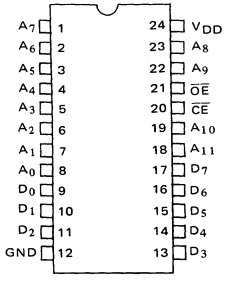
The TC5335P has a chip enable input ($\overline{CE}$) for device selection and a output enable input ($\overline{OE}$) for fast memory access and output control. And the TC5335P uses the address latch system that the falling edge of $\overline{CE}$ latches all inputs except for $\overline{OE}$, thus can be connected to a system where address and data buses are commonly used. The maximum access time from chip enable is 450 ns. The TC 5335P is pin compatible with the industry produced NMOS ROM TMM333P, yet offers a more than 90% reduction in power of their NMOS equivalent. The TMM5335P's maximum operating and standby current is 7 mA and 20 μA, respectively. Thus the TC5335P is most suitable for use in low power applications such as battery operated system.

The TC5335P is moulded in a 24 pin standard plastic package.

FEATURES

- Access Time: 450 ns
- Low Power Dissipation
  I_{DDO} = 7 mA (Max.) : Operating
  I_{DDS} = 20μA (Max.) : Standby
- All Inputs and Outputs: TTL Compatible
- Three state outputs
- Two Control Functions: $\overline{CE}$, $\overline{OE}$
- Address Latches: $\overline{CE}$
- Output Control: $\overline{OE}$
- Pin Compatible with TMM333P
- Standard 24 pin Plastic Package

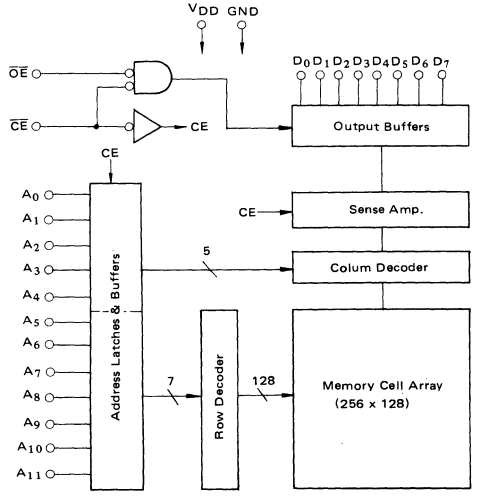
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 - A_{11}$	Address Inputs
$D_0 - D_7$	Data Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	−0.3V ~ 7.0V
V_{IN}	Input Voltage	−0.3V ~ 7.0V
V_{OUT}	Output Voltage	0V ~ V_{DD}
P_D	Power Dissipation (Ta = 85°C)	0.8W
T_{STG}	Storage Temperature	−55°C ~ 150°C
T_{OPR}	Operating Temperature	−40°C ~ 85°C
T_{SOLDER}	Soldering Temperature · Time	260°C · 10 sec

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = −40°C ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V

D.C. CHARACTERISTICS (Ta = −40°C ~ 85°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Load Current	$0 \leqq V_{IN} \leqq V_{DD}$	–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$, $0V \leqq V_{out} \leqq V_{DD}$	–	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	−4.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	4.0	–	mA
I_{DDS1}	Standby Supply Current	$\overline{CE}$ = 2.2V other inputs = V_{IH} or V_{IL}	–	2.0	5.0	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ other inputs = 0.2V or V_{DD} −0.2V	–	0.05	20	μA
I_{DDO1}	Operating Supply Current	$\overline{CE} = V_{IL}$, t_{cyc} = 1μs, $V_{IN} = V_{IH}/V_{IL}$, Iout = 0mA	–	6.0	10.0	mA
I_{DDO2}		$\overline{CE}$ = 0V, t_{cyc} = 1 μs, $V_{IN} = V_{DD}$/GND, I_{out} = 0mA	–	4.0	7.0	mA

Note: Typical values are at Ta = 25°C, V_{DD} = 5V

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	–	5	10	pF
C_{OUT}	Output Capacitance	–	5	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

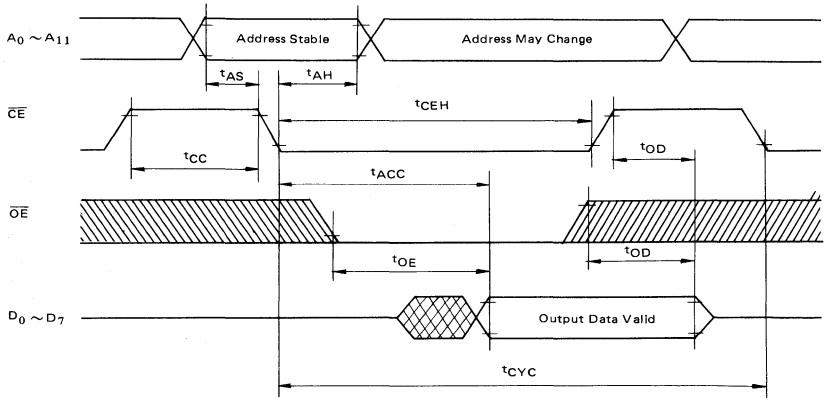
A.C. CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 5V ±10%)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{ACC}	Chip Enable Access Time	—	—	450	ns
t_{OE}	Output Enable Access Time	—	—	150	ns
t_{AS}	Address Setup Time	30	—	—	ns
t_{AH}	Address Hold Time	30	—	—	ns
t_{CC}	$\overline{CE}$ OFF time	70	—	—	ns
t_{CEH}	Chip Enable Hold Time	450	—	—	ns
t_{OD}	Output Desable Time	—	—	100	ns
t_{CYC}	Cycle Time	540	—	—	ns

A.C. TEST CONDITIONS

- Output Load : 100pF + 1TTL Gate
- Input Pulse Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels
  - Input : 0.8V and 2.2V
  - Output : 0.8V and 2.2V
- Input Pulse Rise and Fall Times : 10 ns

TIMING WAVEFORMS



OPERATION MODE

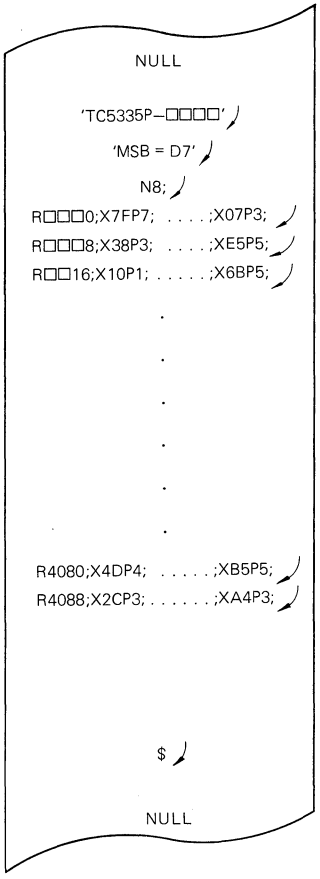
MODE	$\overline{CE}$	$\overline{OE}$	ADDRESS	OUTPUTS
Read	L	L	*	Data out
Standby	H	*	*	High Z
Address Latch	⌐↓	*	Valid	High Z

* : Don't care.

TOSHIBA PAPER TAPE FORMAT

Use 7 or 8-bit (even parity) ASCII code paper tape for ROM data input.
Two acceptable formats which are described in section A and B are available.

A. Format 1 (when a check sum per word is used)

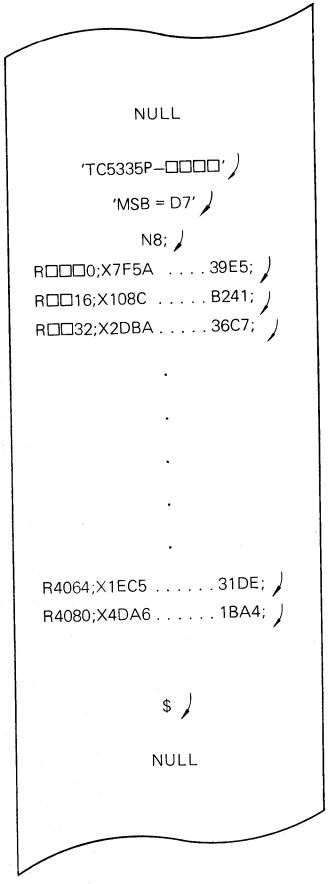


Preceding the first data field and following the last data field there must be a leader /trailer length of at least 50 null characters.
Contents in a single quotation mark (' . . . . . ') signify a comment and □□□□ indicates a four-digit user pattern number.
↵ indicates carriage return and line feed.
Specify the most significant bit (MSB) of the device outputs (D_7 or D_0)
N8 indicates that the mask pattern is an 8-bit pattern.
Semicolon (;) signifies a punctuation of data.
R signifies an address. Enter the address with the four decimal digits every 8-words after the character R.
X signifies a hexadecimal digit.
Enter the data with the two hexadecimal digits every word after the character X.
P signifies the check sum per word.
Enter the sum of 1 in a one word decimal after the character P.

* Data Modification
Modifying single and continuous word data can be carried out by specifying the modifying addresses and inputting the data following the above procedure before the end symbol.
Modification can be allowed from 0 to 4095 addresses.

$ signifies the End symbol.

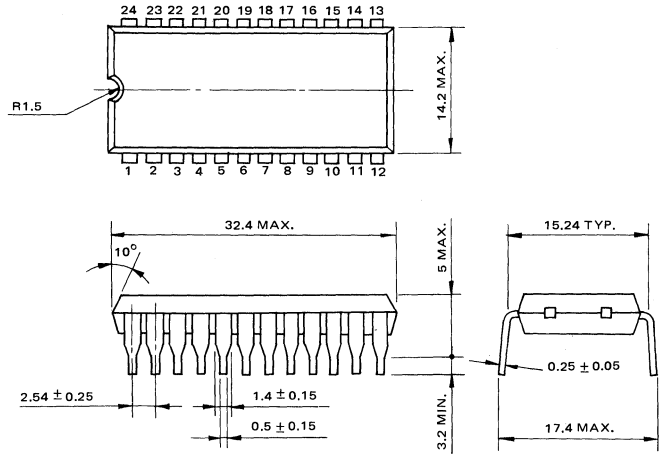
B. Format 2 (when a check sum per word is not used)



R signifies an address.
Enter the address with the four decimal digits every sixteen words after the character R.
X signifies a hexadecimal digit.
Enter the data of sixteen words continuously after the character X.
Otherwise specified in Format 1.

In addition, Toshiba can also accept programming and masking information for TC5335P in the form of punched paper tape with Intel BNPF format or master devices (EPROMs).

OUTLINE DRAWINGS



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 24 leads. All dimensions are in millimeters.

TOSHIBA MOS MEMORY PRODUCTS

TC5364P 64K BIT (8K WORD x 8 BIT) CMOS MASK ROM

SILICON GATE CMOS

TC5364P

PRELIMINARY

DESCRIPTION

The TC5364P is a 65,536 bit read only memory organized as 8,192 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor and character generator. The TC5364P using CMOS technology is most suitable for low power applications such as battery operated system.

The TC5364P is asynchronous type ROM which is consisting of address latch circuit, static memory cells and clocked peripheral circuitry. The falling edge of $\overline{CE}_3$ (or rising edge of CE_3) latches all inputs except for $\overline{OE}$ and PD/$\overline{PD}$.

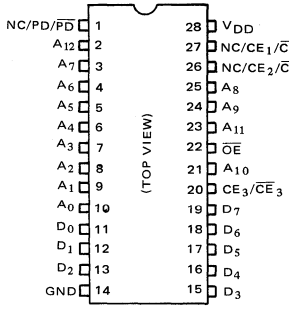
The TC5364P has a PD/$\overline{PD}$ (optional) input for device power saving, and also has three programmable chip enable inputs ($CE_1 \sim 3/\overline{CE}_1 \sim 3$) and one output enable input ($\overline{OE}$) for fast memory access and output control.

The TC5364P is moulded in a 28 pin standard plastic package.

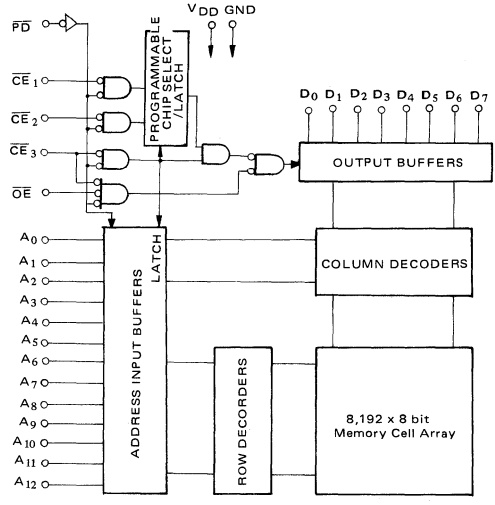
FEATURES

- Single Power Supply: 5V
- Access Time: 250 ns
- Low Power Dissipation
  - Operating Current: 7mA (Max.)
  - Standby Current: 20μA (Max.)
- Wide Operating Temperature Range: $-40 \sim 85°C$
- Pin Compatible with 64K EPROM TMM2764 and NMOS ROM TMM2364/2365
- Edge Enable Operation: $CE_3/\overline{CE}_3$
- Address Latch Type
- Programmable Power Saving Input PD/$\overline{PD}$/NC
- Programmable Chip Select: CE_1, CE_2, CE_3, Easy Memory Expansion
- All Inputs and Outputs: TTL Compatible
- Three State Outputs

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{12}$	Address inputs
$D_0 \sim D_7$	Data outputs
$CE_1 \sim CE_3$	Chip enable inputs
P_D	Power down input
$\overline{OE}$	Output enable input
NC	No connection
V_{DD}	Power Supply
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}	Input Voltage	−0.5 ~ 7.0	V
V_{OUT}	Output Voltage	0 ~ V_{DD}	V
P_D	Power Dissipation	1.0	W
T_{opr}	Operating Temperature	−40 ~ 85	°C
T_{stg}	Storage Temperature	−55 ~ 150	°C
T_{SOLDR}	Soldering Temperature · Time	260 · 10	°C · sec

D.C. OPERATING CONDITIONS (Ta = −40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
I_{IN}	Input Leakage Current	$OV \leqq V_{IN} \leqq V_{DD}$	–	±1.0	μA
I_{LO}	Output Leakage Current	$OV \leqq V_{OUT} \leqq V_{DD}$	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	–	mA
I_{DDO1}	Operating Current	(CE, V_{IH}) = 2.2V ($\overline{CE}$, V_{IL}) = 0.8V t_{CYC} = 1μs	–	10	mA
I_{DDO2}		(CE, V_{IH}) = V_{DD} −0.2V ($\overline{CE}$, V_{IL}) = 0.2V t_{CYC} = 1μs	–	7	mA
I_{DDS1}	Standby Current	($\overline{CE}$, V_{IH}) = 2.2V CE = 0.8V (CE, V_{IL}) = 0.8V $\overline{CE}$ = 2.2V Output = OPEN	–	5	mA
I_{DDS2}		(CE) = 0.2V, ($\overline{CE}$) = V_{DD} −0.2V V_{IN} = 0.2V or V_{DD} −0.2V Output = OPEN	–	20	μA

CAPACITANCE* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = OV	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = OV	10	pF

*This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = 40 ~ 85°C, V_{DD} = 5V ± 10%)

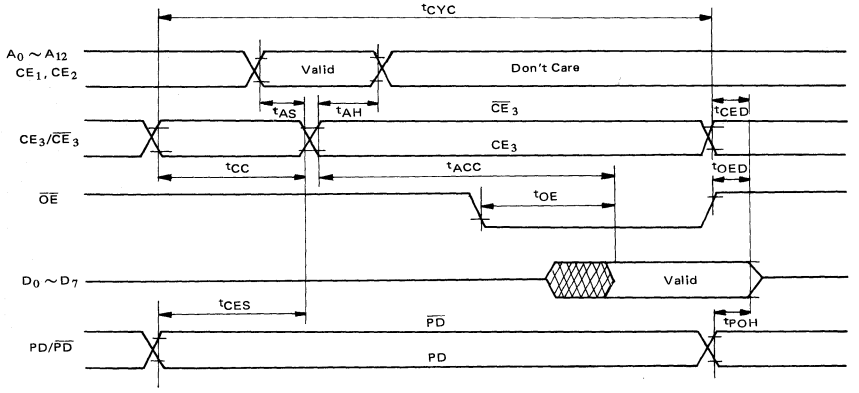
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Chip Enable Access Time	–	250	ns
t_{OE}	Output Enable Access Time	–	100	ns
t_{AS}	Address Set up Time	0	–	ns
t_{AH}	Address Hold Time	50	–	ns
t_{CC}	Chip Enable Off Time	90	–	ns
t_{CES}	Chip Enable Setup Time from PD	90	–	ns
t_{OED}	Output Disable Time from OE	–	90	ns
t_{CED}	Output Disable Time from CE	–	90	ns
t_{POH}	Output Hold Time from PD	–	90	ns
t_{CYC}	Cycle Time	350	–	ns

Note 1: Assumes than $\overline{OE}$ delay time to $CE_3/\overline{CE}_3 \geqq t_{ACC} - t_{OE}$

A.C. TEST CONDITIONS

- Output Load: 100pF + 1 TTL Gate
- Input Levels: V_{IL} = 0.6V, V_{IH} = 2.4V
- Timing Measurement Rference Levels
  - Input: 0.8V, 2.2V
  - Output: 0.8V, 2.2V
- Input Rise and Fall Time: 5 ns

TIMING WAVE FORMS



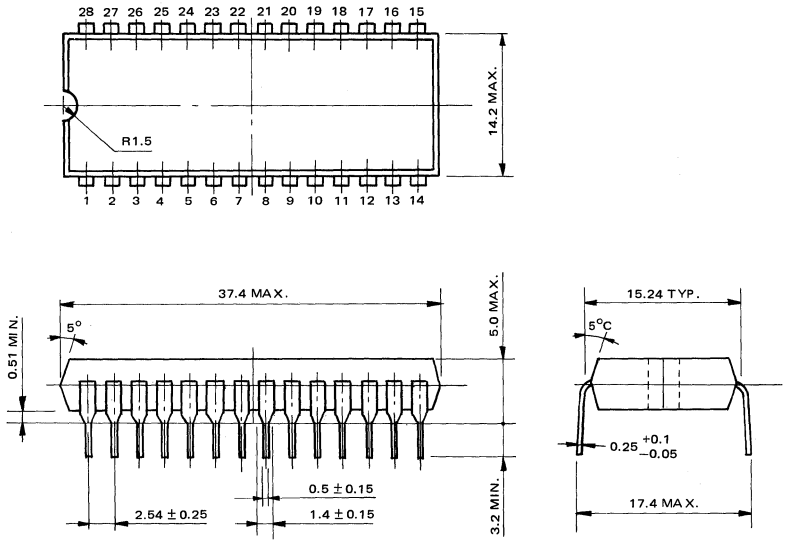
OPERATION MODE

MODE	PD ($\overline{PD}$)	CE_1 ($\overline{CE}_1$)	CE_2 ($\overline{CE}_2$)	CE_3 ($\overline{CE}_3$)	OE	Outputs
Read	L(H)	H(L)	H(L)	H (L)	L	Valid
Output Deselect	H(L)	*	*	*	*	High-Z
	*	L(H)	*	*	*	
	*	*	L(H)	*	*	
	*	*	*	L(H)	*	
	*	*	*	*	H	

Note: H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

OUTLINE DRAWING

Unit: mm



Note: Each lead pitch is 2.54 mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

TC5365P 64K BIT (8K WORD X 8 BIT) CMOS MASK ROM

TC5365P

SILICON GATE CMOS

DESCRIPTION

The TC5365P is a 65,536 bit read only memory organized as 8,192 words by 8 bits with a low bit cost, thus being suitable for use in program memory for microprocessor and character generator.

The TC5365P using CMOS technology is most suitable for low power applications such as battery operated system.

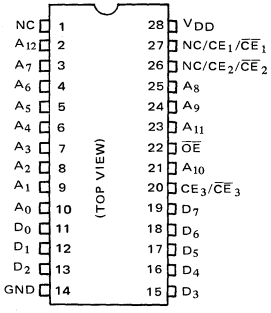
The TC5365P is an asynchronous type ROM which has three programmable chip enable inputs ($CE_1 \sim CE_3/\overline{CE}_1 \sim \overline{CE}_3$), and one output enable input ($\overline{OE}$) for fast memory access and output control.

The TC5365P is moulded in a 28 pin standard plastic package.

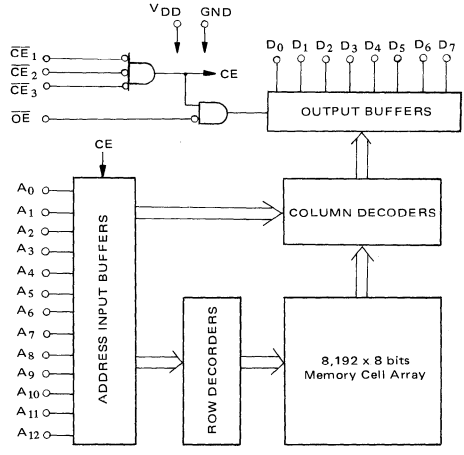
FEATURES

- Single Power Supply: 5V
- Low Power Dissipation
  - Operating Current: 7mA (Max.)
  - Standby Current: 20μA (Max.)
- Compatible with 64K EPROM TMM2764 and 64K NMOS ROM TMM2365P.
- Fully Static Operation
- Programmable chip select: CE_1, CE_2, CE_3 Easy Memory Expansion
- All Inputs and Outputs: TTL-Compatible
- Three State Outputs

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{12}$	Address inputs
$D_0 \sim D_7$	Data outputs
$CE_1 \sim CE_3$	Chip enable inputs
$\overline{OE}$	Output enable inputs
NC	No connection
V_{DD}	Power Supply
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}	Input Voltage	−0.5 ~ 7.0	V
V_{OUT}	Output Voltage	0 ~ V_{DD}	V
P_D	Power Dissipation	1.0	W
T_{opr}	Operating Temperature	−40 ~ 85	°C
T_{stg}	Storage Temperature	−55 ~ 150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

D.C. OPERATING CONDITIONS (Ta = −40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 5V ±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IN}	Input Leakage Current	$OV \leqq V_{IN} \leqq V_{DD}$	–	±1.0	μA
I_{LO}	Output Leakage Current	$OV \leqq V_{OUT} \leqq V_{DD}$	–	±0.5	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	–	mA
I_{DDO1}	Operating Current	$(\overline{CE}, V_{IH})$ = 2.2V $(\overline{CE}, V_{IL})$ = 0.8V t_{CYC} = 1 μs	–	10	mA
I_{DDO2}		$(\overline{CE}, V_{IH}) = V_{DD} - 0.2V$ $(\overline{CE}, V_{IL})$ = 0.2V t_{CYC} = 1 μs	–	7	mA
I_{DDS1}	Standby Current	$(\overline{CE}, V_{IH})$ = 2.2V (CE, V_{IL}) = 0.8V Output = OPEN	–	2	mA
I_{DDS2}		$(CE) = 0.2V, (\overline{CE}) = V_{DD} - 0.2V$ V_{IN} = OV ~ V_{DD} Output = OPEN	–	20	μA

CAPACITANCE* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = OV	8	pF
C_{OUT}	Output Capacitanc	V_{OUT} = OV	10	pF

*This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 5V ±10%)

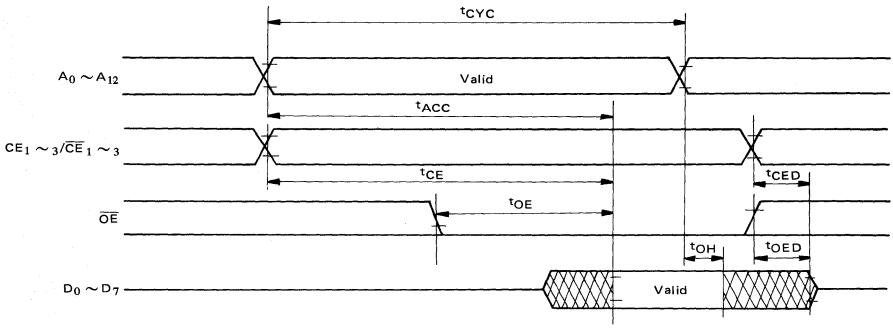
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Access Time	—	250	ns
t_{CE}	Chip Enable Access Time	—	250	ns
t_{OE}	Output Enable Access Time	—	100	ns
t_{CED}	Output Disable Time from CE/$\overline{CE}$	0	90	ns
t_{OED}	Output Disable Time from $\overline{OE}$	0	90	ns
t_{OH}	Output Hold Time	0	—	ns
t_{CYC}	Cycle Time	250	—	ns

Note 1: Assumes that $\overline{OE}$ delay time to $CE_1 \sim CE_3/\overline{CE}_1 \sim \overline{CE}_3 \geqq t_{ACC} - t_{OE}$

A.C. TEST CONDITIONS

- Output Load: 100 pF + 1TTL
- Input Levels: VIL = 0.6V, V_{IH} = 2.4V
- Timing Measurement Reference Levels
  - Input: 0.8V, 2.2V
  - Output: 0.8V, 2.2V
- Input Rise and Fall time: 5 ns

TIMING WAVE FORMS



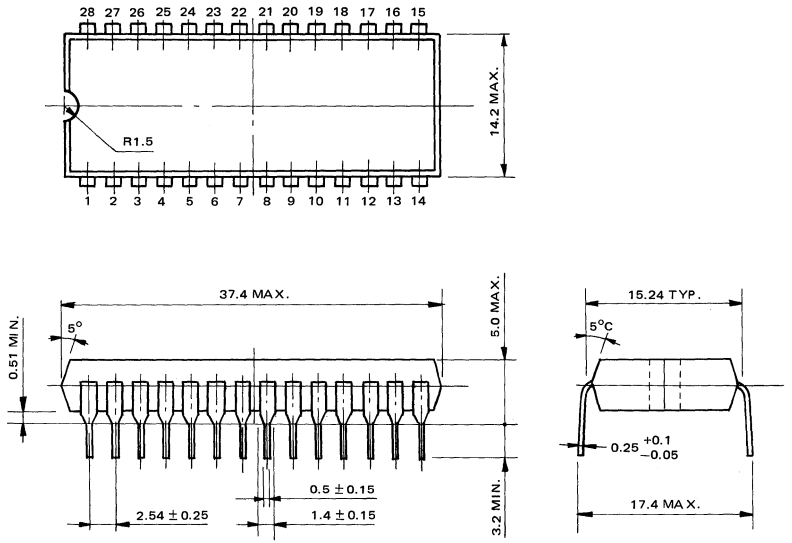
OPERATION MODE

MODE	CE_1 ($\overline{CE}_1$)	CE_2 ($\overline{CE}_2$)	CE_3 ($\overline{CE}_3$)	$\overline{OE}$	Outputs
Read	H(L)	H(L)	H(L)	L	Valid
Output Deselect	L(H)	*	*	*	High-Z
	*	L(H)	*	*	
	*	*	L(H)	*	
	*	*	*	H	

Note: H: V_{IL}, L: V_{IL}, *: V_{IH} or V_{IL}

OUTLINE DRAWING

Unit: mm



Note: Each lead pitch is 2.54 mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

TOSHIBA MOS MEMORY PRODUCTS

TC5366P 64K BIT (8K WORD x 8 BIT) CMOS MASK ROM

TC5366P

SILICON GATE CMOS

PRELIMINARY

DESCRIPTION

The TC5366P is a 65,536 bit read only memory organized as 8,192 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor and character generator.

The TC5366P using CMOS technology is most suitable for low power applications such as battery operated system.

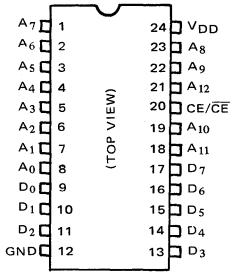
The TC5366P is an asynchronous type ROM and has a programmable chip enable input for device selection and device power saving.

The TC5366P is moulded in a 24 pin standard plastic package.

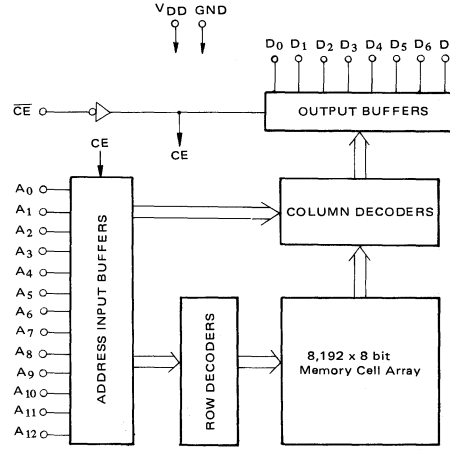
FEATURES

- Single Power Supply: 5V
- Access Time: 250 ns
- Low Power Dissipation
  - Operating Current: 7mA (Max.)
  - Standby Current: 20μ A (Max.)
- Fully Static Operation
- Programmable Chip Enable: CE/$\overline{CE}$
- All Inputs and Outputs: TTL Compatible
- Three State Outputs

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{12}$	Address inputs
$D_0 \sim D_7$	Data outputs
CE/$\overline{CE}$	Chip enable inputs
V_{DD}	Power supply
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}	Input Voltage	−0.5 ~ 7.0	V
V_{OUT}	Output Voltage	0 ~ V_{DD}	V
P_D	Power Dissipation	1.0	W
T_{opr}	Operating Temperature	−40 ~ 85	°C
T_{stg}	Storage Temperature	−55 ~ 150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

D.C. OPERATING CONDITIONS (Ta = −40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 5V ±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IN}	Input Leakage Current	$OV \leqq V_{IN} \leqq V_{DD}$	–	±1.0	μA
I_{LO}	Output Leakage Current	$OV \leqq V_{OUT} \leqq V_{DD}$	–	±0.5	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	–	mA
I_{DDO1}	Operating Current	(CE, V_{IH}) = 2.2V ($\overline{CE}$, V_{IL}) = 0.8V t_{CYC} = 1μs	–	10	mA
I_{DDO2}		(CE, V_{IH}) = V_{DD} −0.2V ($\overline{CE}$, V_{IL}) = 0.2V t_{CYC} = 1μs	–	7	mA
I_{DDS1}	Standby Current	($\overline{CE}$, V_{IH}) = 2.2V (CE, V_{IL}) = 0.8V Output = OPEN	–	2	mA
I_{DDS2}		(CE) = 0.2V, ($\overline{CE}$) = V_{DD} −0.2V V_{IN} = OV ~ V_{DD} Output = OPEN	–	20	μA

CAPACITANCE* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = OV	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = OV	10	pF

*This parameter is periodically sampled and is not 100% tested.

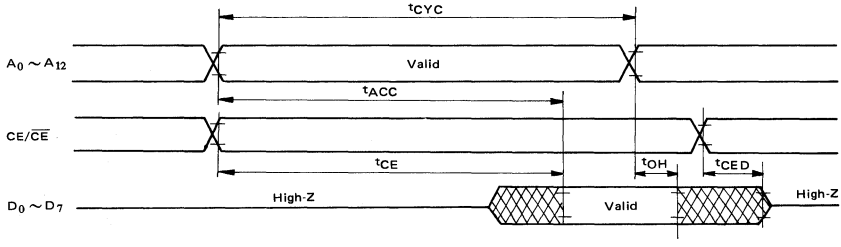
A.C. CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 5V ±10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Access Time	–	250	ns
t_{CE}	Chip Enable Access Time	–	250	ns
t_{CED}	Output Disable Time from CE	0	90	ns
t_{OH}	Output Hold Time	0	–	ns
t_{CYC}	Cycle Time	250	–	ns

A.C. TEST CONDITIONS

- Output Load: 100pF + 1 TTL
- Input Levels: V_{IL} = 0.6V, V_{IH} = 2.4V
- Timing Measurement Reference Levels
  - Input: 0.8V, 2.2V
  - Output: 0.8V, 2.2V
- Input Rise and Fall Time: 5ns

TIMING WAVE FORMS

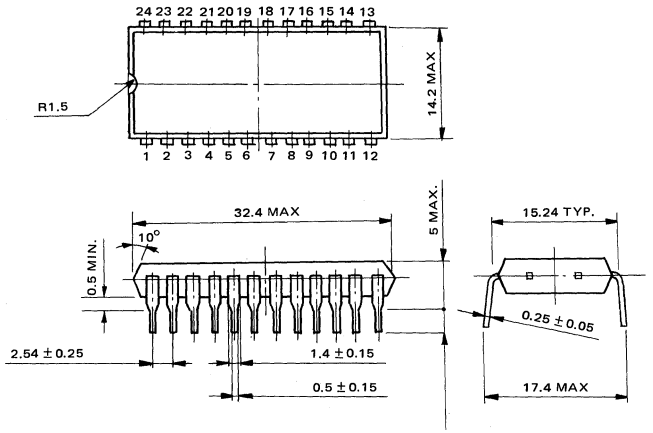


OPERATION MODE

MODE	CE ($\overline{CE}$)	Output
Read	H(L)	Valid
Output Deselect	L(H)	High-Z

Note: H: V_{IH}, L: V_{IL}

OUTLINE DRAWINGS



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25mm longitudinal position with respect to No. 1 and 24 leads.
All dimensions are in millimeters.

TC53256P 256K BIT (32K WORD x 8 BIT) CMOS MASK ROM

TC53256P

SILICON GATE CMOS

PRELIMINARY

DESCRIPTION

The TC53256P is a 262,144 bit read only memory organized as 32,768 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor and character generator. The TC53256P using CMOS technology is most suitable for low power applications such as battery operated system.

The TC53256P is a synchronous type ROM which is consisting of address latch circuit, static memory cells and clocked peripheral circuitry. The $\overline{CE}$ falling edge latches all inputs except for CS/$\overline{CS}$ and $\overline{OE}$.

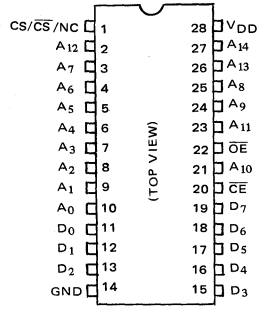
The TC53256P has a programmable chip select input (CS/$\overline{CS}$, optional) for device power saving, one chip enable input ($\overline{CE}$) for device selection, and one output enable input ($\overline{OE}$) for fast memory access and output control.

The TC53256P is moulded in a 28 pin standard plastic package.

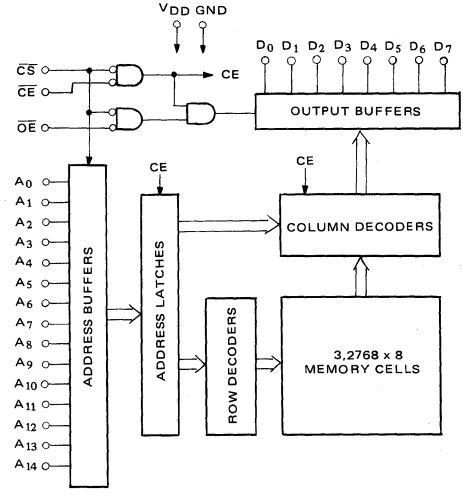
FEATURES

- Single 5V Power Supply: 5V
- Access Time: 350 ns (Max.)
- Power Dissipation
  - Operating Current: 15mA (Max.)
  - Standby Current: 20μA (Max.)
- Pin Compatible with 256K NMOS ROM TMM23256P
- Edge Enable Operation: $\overline{CE}$
- Address Latch Type
- Programmable Chip Select Input: CS/$\overline{CS}$/NC
- All Inputs and Outputs: TTL Compatible
- Three State Outputs: Wired OR capability

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{14}$	Address inputs
$D_0 \sim D_7$	Data outputs
CS/$\overline{CS}$	Chip select input
NC	No conection
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
V_{DD}	Power supply
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	$-0.5 \sim 7.0$	V
V_{IN}	Input Voltage	$-0.5 \sim V_{DD} + 0.5$	V
V_{OUT}	Output Voltage	$0 \sim V_{DD}$	V
PD	Power Dissipation	0.8	W
T_{stg}	Storage Temperature	$-55 \sim 150$	°C
T_{opr}	Operating Temperature	$-40 \sim 85$	°C
T_{sld}	Soldering Temperature · Time	260 · 10	°C · sec

D.C. OPERATING CONDITIONS (Ta = −40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CS} = V_{IL}$ ($CS = V_{IH}$) or $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = OV \sim V_{DD}$	–	±1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	−1.0	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	–	2.0	mA
I_{DDS}	Standby Current	$\overline{CS} = OV$ ($\overline{CS} = V_{DD}$) or $\overline{CE} = V_{DD}$ and $V_{IN} = OV$ (V_{DD})	–	20	μA
I_{DDO1}	Operating Current	$V_{IN} = V_{IH}/V_{IL}$, $t_{cycle} = 1\mu s$	–	25	mA
I_{DDO2}		$V_{IN} = V_{DD}/OV$, $t_{cycle} = 1\mu s$	–	15	mA

CAPACITANCE* (f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	–	10	pF
C_{OUT}	Output Capacitance	–	10	pF

*This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS

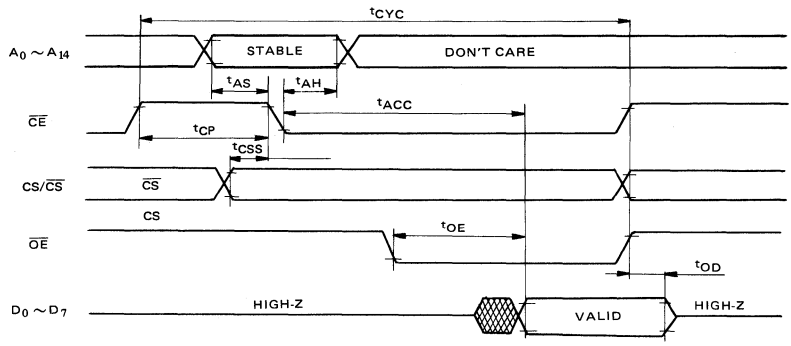
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	450	–	ns
t_{ACC}	Chip Enable Access Time	–	350	ns
t_{OE}	Output Enable Access Time	–	120	ns
t_{OD}	Output Disable Time	0	100	ns
t_{CP}	Precharge Time	90	–	ns
t_{AS}	Address Set-up Time	50	–	ns
t_{AH}	Address Hold Time	50	–	ns
t_{CSS}	Chip Select Set-up Time	50	–	ns

Note 1: Assumes that $\overline{OE}$ delay time to $\overline{CE} \geqq t_{ACC} - t_{OE}$
Note 2: T_{OD} is specified from $\overline{CE}$, $\overline{OE}$ or CS/$\overline{CS}$ trailing edge, whichever occurs first.

AC TEST CONDITIONS

- Output Load: 100pF + 1TTL
- Input Levels: 0.6V, 2.4V
- Timing Measurement Reference Levels
  - Input: 0.8V, 2.2V
  - Output: 0.8V, 2.2V
- Input Rise and Fall Time: 5 ns

TIMING WAVEFORMS



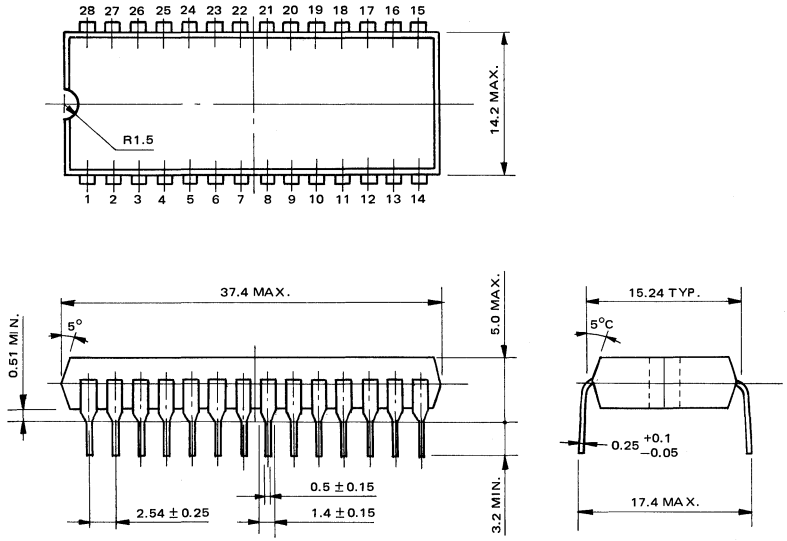
OPERATION MODE

MODE	CS ($\overline{CS}$)	$\overline{CE}$	$\overline{OE}$	$A_0 \sim _{14}$	Outputs
Read	H(L)	L(⌐‾)	L	Valid	Data out
Output Deselect	L(H)	*	*	*	High Z
	*	H	*	*	
	*	*	H	*	

Note: H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

OUTLINE DRAWING

Unit: mm



Note: Each lead pitch is 2.54 mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

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