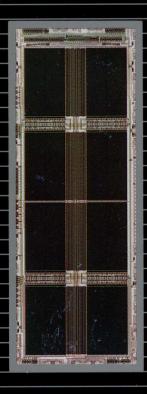
TOSHIBA



NON-VOLATILE MEMORY 1990

TOSHIBA

NON-VOLATILE MEMORY 1990

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1. EPROM/HIGH SPEED EPROM

CAPACITY	PART NUMBER	ORGANIZATION	ACCESS TIME (ns)	POWER SUPPLY (V)	OPERATING TEMPERATURE (*C)	POWER DISSIP	ATION max (mW) STANDBY	PIN COUNT	PACKAGE DPFJ	PACKAGE WIDTH (inch)
	TC57256AD-12		120		0 ~ 70	450				
i	TC57256AD-15	1	150	5V±5%	- 40 ~ 85	158	0.525			
	TC57256AD-120	1 1	120					İ		
256K	TC57256AD-150	3216x8	150	5V <u>+</u> 10%	0~70	165	0.550	28		0.6
l	TC57256AD-20	1 1	200		-40 ~ 85	158	0.525	ĺ		
	TC57H256D-70		70	5V±5%	0	263	0.525	1		
	TC57H256D-85	1	85	5V±10%	0 ~ 70	275	0.550			
	TC57512AD-15	2114.2	150		-40 ~ 85	4		28	=	0.6
512K	TC57512AD-20	64Kx8	200	5V±5%		158	0.525	25	-	u.o
	TC571000AD-12		120	5V±5%		158	0.525			
	TC571000AD-150]	150	5V±10%	0~70	165	0.550			
	TC571001AD-12		120	5V±5%	0 /0	158	0.525			
İ	TC571001AD-150	128Kx8	150	5V+10%		165	0.550			
	TC57H1000AD-85		85	-			32	-	0.6	
	TC57H1000AD-100	1	100		0 ~ 70					
	TC57H1001AD-85]	85	5V±10%		220	0.550			
1M	TC57H1001AD-100		100							
	TC571024D-15		150	514.50	0 ~ 70	210	0.525		10	
	TC571024D-20]	200 5V±5%	-40 ~ 85	210 0.525					
	TC571024D-200]	200	5V±10%		220	0.550		•	
	TC57H1024D-85]	85	5V+5%		210	0.525	40	-	
	TC57H1024D-10	64Kx16	100	37 13%		210	0.525	40		0.6
	TC57H1024D-100	1	100	5V±10%	0~70	220	0.550			
	TC57H1025AD-55]	55			315	52.5			
	TC57H1026D-45	1	45	5V±5%		368	52.5			
	TC57H1026D-35]	35						-	
	TC574000D-12		120	5V±5%		315	0.525			
	TC574000D-120]	120		0 ~ 70	330	0.550			
	TC574000D-150	512Kx8	150	E14.100		330	0.550	32		
	TC574000DI-150]	150	5V±10%	- 40 ~ 85	me	0.550			0.6
4M	TC574000DI-200		200		65	275	0.550			0.6
	TC574200D-120		120						=	
	TC574200D-150	256Kx16/512Kx8	150	5V±10%	0 ~ 70	330	0.550	40		
	TC574200D-200	1	200						=	

D = CERAMIC DIP, P = PLASTIC DIP, F = PLASTIC FLAT PACKAGE (SOP), J = PLASTIC SOJ

2. OTP/HIGH SPEED OTP

CAPACITY	PART NUMBER	ORGANIZATION	ACCESS TIME (ns)	POWER SUPPLY (V)	OPERATING TEMPERATURE (*C)	POWER DISSIF	ATION max (mW) STANDBY	PIN COUNT	PACKAGE D P F J	PACKAGE WIDTH (inch)
256K	TC54256AP/AF-20	32Kx8	200	5V <u>+</u> 5%	-40 ~ 85	158	0.525	28		0.6 (P) 0.45 (F)
512K	TC54512AP/AF-15	64Kx8	150	5V+5%	-40 ~ 85	158	0.525	28		0.6 (P)
3124	TC54512AP/AF-20	040.00	200	1			5,020	_		0.45 (F)
	TC541000J-15		150		0~70				-	
	TC541001J-15		150	150 200 200 5V+5%	0 70		0.525	28		0.4
j	TC541000J-20]	200		-40 ~ 85					0.4
	TC541001J-20	128Kx8	200			158			•	
1M	TC541000P/F-15		150		0 ~ 70					
	TC541001P/F-15]	150							0.6 (P)
	TC541000P/F-20		200	1	-40 ~ 85				==	0.525 (F)
	TC541001P/F-20		200		-40 &					
ļ	TC54H1024P/F-85	64Kx16	85	EV. EW	0 ~ 70	210	0,525	40		0.6 (P)
	TC54H1024P/F-10	DHAXIO	100	5V±5%	0 70	210	0.525	40		0.525 (F)
	TC544000P/F-12		120	5V±5%		315	0.525	32		0.6 (P)
4M	TC544000P/F-120	512Kx8	100	74.404	0~70	220	0.550	22		0.525 (F)
	TC544000P/F-150		120	5V±10%		330	0.550	32		

D = CERAMIC DIP, P = PLASTIC DIP, F = PLASTIC FLAT PACKAGE (SOP), J = PLASTIC SOJ

3. MROM/HIGH SPEED MROM

CARACITY	DADT NI HADED	OOCANIZATION	ACCESS	POWER	OPERATING	POWER DISSIP	ATION max (mW)	PIN	PACKAGE	PACKAGE
CAPACITY	PART NUMBER	ORGANIZATION	TIME (ns)	SUPPLY (V)	TEMPERATURE (°C)	ACTIVE	STANDBY	COUNT	DPFJ	WIDTH (inch)
	TC531000CP/CF-12		120			220				0.6 (P)
	TC531000CP/CF	128Kx8	150	5V+10%	-40 ~ 70	193		28	• •	0.525 (F)
1M	TC531001CP/CF-12		120			220	0.11			
	TC531001CP/CF		150			193				
	TC531024P/F-12		120	5V <u>+</u> 5%	0 ~ 70	220 193		40		
	TC531024P/F-15	64Kx16	150	5V+10%	0 - 70					
	TC534000P/F		200	5V <u>+</u> 5%	-40 ~ 70					0.6 (P)
414	TC534000P/F	512Kx8	250		-40 ~ 85	165	0.11	32		0.525 (F)
••••	TC534000AP/AF		150	5V <u>+</u> 10%		220	•		••	
	TC534200P/F	256Kx16/512Kx8	150		0~70	275		40	• •	
8M	TC538200P/F	512Kx16/1Mx8	200	5V+10%	0 ~ 70	275	0.55	42P 44F		0.6 (P) 0.6 (F)
16M	TC5316200P/F	1Mx16/2Mx8	200	5V <u>+</u> 10%	0 ~ 70	275	0.55	42P 44F		0.6 (P) 0.6 (F)

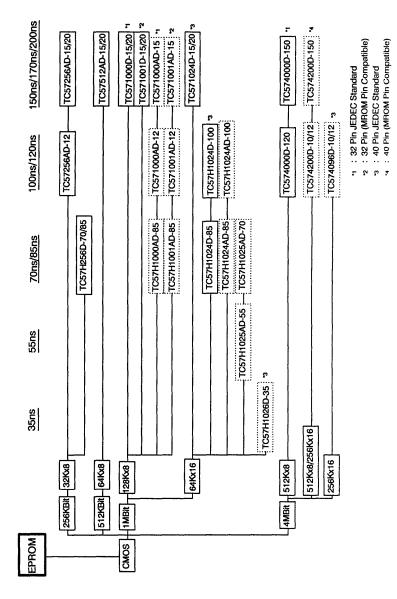
D = CERAMIC DIP, P = PLASTIC DIP, F = PLASTIC FLAT PACKAGE (SOP), J = PLASTIC SOJ

4. FLASH E2PROM

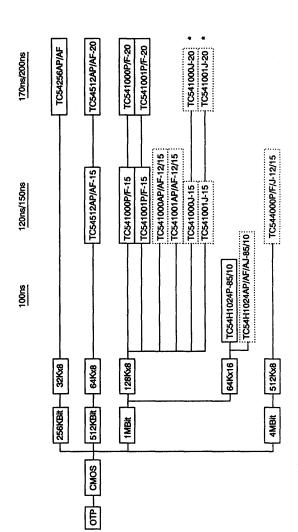
CAPACITY PART NUMBER		ORGANIZATION	ACCESS POWER		OPERATING	POWER DISSIPATION max (mW)		PIN	PACKAGE	PACKAGE
			TIME (ns)	SUPPLY (V)	TEMPERATURE (°C)	ACTIVE	STANDBY	COUNT	DPFJ	WIDTH (inch)
	TC58257AP/AF-17LV		170						==	0.6 (P)
256K	TC58257AP/AF-20LV	32Kx8	200	5V <u>+</u> 10%	- 10 ~ 70	165	0.55	28		0.45 (F)
	TC58257AP/AF-25LV		250]						
1M	TC58F1000P/F/J-15	128Kx8	150	5V+10%	0 ~ 70	165	0.55	32	===	0.6 (P) 0.525 (F)
	TC58F1000P/F/J-20	200		0,0		"			0.4 (J)	

 $[\]label{eq:decomposition} D = \text{CERAMIC DIP, } P = \text{PLASTIC DIP, } F = \text{PLASTIC FLAT PACKAGE (SOP), } J = \text{PLASTIC SOJ}$

TOSHIBA EPROM/HIGH SPEED EPROM

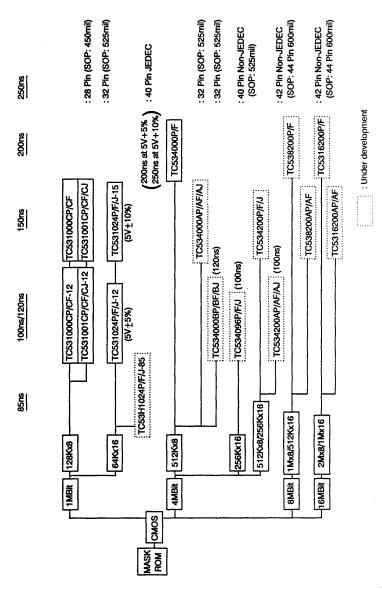


TOSHIBA OTP/HIGH SPEED OTP

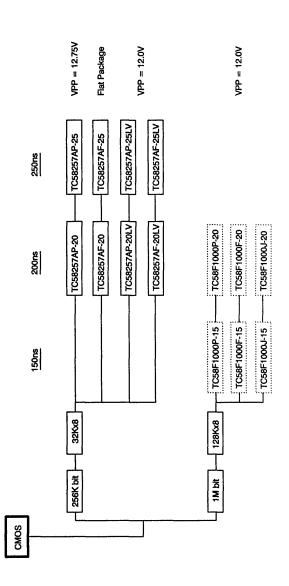


* : 400mil 32pin SOJ

TOSHIBA MASK ROM/HIGH SPEED MASK ROM



FLASH E2PROM



1. EPROM

ORGANIZATION	32Kx8	64Kx8	128Kx8	128K/8	64Kx16
PACKAGE WIDTH	0.6 in CERDIP	0.6 in CERDIP	0.6 in CERDIP	0.6 in CERDIP	0.6 in CERDIP
TOSHIBA	TC57256AD	TC57512AD	TC571000AD	TC571001AD	TC571024D
AMD	AM27C256	AM27C512	AM27C010		AM27C1024
FWITSU	MBM27C256A	MBM27C512	MBM27C1001	MBM27C1000	MBM27C1024
HITACHI	HN27C256		HN27C101	HN27C301	HN27C1024
INTEL	27C256		27C010		27C210
MITSUBISHI	M5M27C256	M5M27C512A	M5M27C101	M5M27C100	M5M27C102
NEC	uPD27C256A	uPD27C512	uPD27C1001	uPD27C1000	uPD27C1024
OIG	MSM27256				
TI	TMS27C256	TMS27C512	TMS27C010		TMS27C210

ORGANIZATION	512Kx8	512Kx8	512Kx8/256Kx16
PACKAGE WIDTH	0.6 in CERDIP	0.6 in CERDIP	0.6 in CERDIP
TOSHIBA	TC574000D	TC574000DI	TC574200D
AMD			
FWITSU	MBM27C4000/1		MBM27C4096
HITACHI			
INTEL			27C240
MITSUBISHI			
NEC	uPD27C4001		
OIQ			
Π			

2. HIGH SPEED EPROM

ORGANIZATION	32Kx8	128Kx8	64Kx16	64l0x16	64l0x16
PACKAGE WIDTH	0.6 in CERDIP	0.6 in CERDIP	0.6 in CERDIP	0.6 in CERDIP	0.6 in CERDIP
TOSHIBA	TC57H256D	TC57H1000/1AD	TC57H1024D	TC57H1025AD	TC57H1026D
HITACHI	HN27C256H		HN27C1024H		

3. OTP

ORGANIZATION	32	Kra .	. 64	oar Deriver	128Kx8		
PACKAGE WIDTH	0.6 in DIP	0.45 in SOP	0.6 in DIP	0.45 in SOP	0.6 in DIP	0.525 in SOP	
TOSHIBA	TC54256AP	TC54256AF	TC54512AP	TC54512AF	TC541000P	TC541000F	
AMD	AM27C256		AM27C512		AM27C010		
FUJITSU							
HITACHI		HN27C256FP			HN27C101P	HN27C101FP	
INTEL	27C256				27C010		
MITSUBISHI	M5M27C256P	M5M27C256FP	M5M27C512AP	M5M27C512AFP	M5M27C101P	M5M27C101FP	
NEC							
OKI I							
n and	TMS27PC256						

DESCRIPTION	128	Kx8	512	:Ka
PACKAGE WIDTH	0.6 in DIP	0.525 in SOP	0.6 in DIP	0.525 In SOP
TOSHIBA	TC541001P	TC541001F	TC544000P	TC544000F
AMD				
FWITSU				
HITACHI	HN27C301P	HN27C301FP		
INTEL				
MITSUBISHI	M5M27C100P	M5M27C100FP		
NEC				
ОКІ				
n.				

4. HIGH SPEED OTP

ORGANIZATION		
PACKAGE WIDTH	0.6 In DIP	0.525 in SOP
TOSHIBA	TC54H1024P	TC54H1024F
AMD		
FUJITSU		
HITACHI	HN27C1024HG	
INTEL		
MITSUBISHI		
NEC -		***************************************
OKI		
Π		

5. MASK ROM

ORGANIZATION	128	IKv8	128Kx8		
PACKAGE WIDTH	0.6 in DIP	0.45 in SOP	0.6 in DIP	0.525 in SOP	
TOSHIBA	TC531000CP	TC531000CF	TC531001CP	TC531001CF	
FWITSU	MB831000				
HITACHI	HN62321/31P	HN62321/31F	HN62321A/31AP	HN62321A/31AF	
MITSUBISHI	M5M231000P				
NEC	uPD23C1000C	uPD23C1000G	uPD23C1001EC		
ON	MSM531000RS				
SHARP	LH531000				
SONY	CXK381000P				

ORGANIZATION	64Kx16	64Kx16	512Kx8/256Kx16	
PACKAGE WIDTH	0.6 in DIP	0.6 in DIP	0.6 in DIP	0.525 in SOP
TOSHIBA	TC531024P	TC53H1024P	TC534200P	TC534200F
FWITSU			MB834100	
HITACHI			HN62404P	
MITSUBISHI			M5M23C400P	
NEC	uPD23C1024EP			
ОКІ				
SHARP			LH534000	
SONY				

5. MASK ROM

ORGANIZATION	1Mx8/512Kx16		2Mx6/	Mic18	
PACKAGE WIDTH	0.6 in DIP	0.6 in SOP	0.6 in DIP	0.6 in SOP	
TOSHIBA	TC538200P	TC538200F	TC5316200P	TC5316200F	
FLUITSU					
HITACHI	HN62801P	HN62801F	HN621601P	HN621601F	
MITSUBISH	M5M23C800P	M5M23C800FP	M5M231600P	M5M231600FP	
NEC	uPD23C8000C	uPD23C8000G	uPD23C1600C	uPD23C1600G	
OX					
SHARP	LH538100	LH538100	LH531601	LH531601	
SOMY					

ORGANIZATION	512	Kx8
PACKAGE WIDTH	0.6 in DIP	0.525 in SOP
TOSHIBA	TC534000AP	TC534000AF
FUJITSU	MB834000	MB834000
HITACHI	HN62401P	HN62401F
MITSUBISH	M5M23C400P	M5M217C400FP
NEG	uPD23C4000C	uPD23C4000G
ОКІ		
SHARP	LH534100	LH534100
SONY		

6. FLASH E2PROM

ORGANIZATION	33	2Kx8		1281648	A STATE OF
PACKAGE WIDTH	0.6 in DIP	0,45 in SOP	0.6 in DIP	0.525 in SOP	0.4 in SOJ
TOSHIBA	TC58257AP	TC58257AF	TC58F1000P	TC58F1000F	TC58F1000J
INTEL	27/28F256		28F010		
SEEQ			48C1024		



		·	
	e.		
			-

32,768 WORD x 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC57256AD is a 32,768 word \times 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57256AD's access time is 120ns, and the TC57256AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the CE input. Advanced CMOS technology reduces the maximum active current to 30mA/8.3MHz and standby current to $100\mu\text{A}$. For program operation, the programming is achieved by using the high speed programming mode. TC57256AD is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

FEATURES

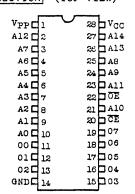
 Peripheral circuit: CMOS Memory cell : N-MOS

	-12	-120	-150
VCC	5V±5%	5V	±10%
tACC	120ns	120ns	150ns

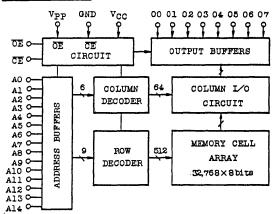
· Single 5V power supply

- Full static operation
- · High speed programming mode
- · Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, TMM27256AD and TC57256D
- · Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ∿A14	Address Inputs
00 ∿ 07	Outputs(Inputs)
ĈĒ	Chip Enable Input
ŌĒ	Output Enable Input
V _{PP}	Program Supply Voltage
Vcc	VCC Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE	ČE (20)	OE (22)	VPP (1)	V _{CC} (28)	00 ~ 07 (11 ~ 13,15 ~ 19)	POWER
Read	L	L			Data Out	Active
Output Deselect	*	H	5V	5V	High Impedance	ACCIVE
Standby	Н	*			High Impedance	Standby
Program	L	Н	12.5V	(L)	Data In	
Program Inhibit	Н	H	2)	2)	High Impedance	Active
Program Verify	*	L			Data Out	

* H or L 1); HIGH SPEED PROGRAM MODE I, 2): HIGH SPEED PROGRAM MODE II

TC57256AD-12, TC57256AD-120 TC57256AD-150

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
v _{CC}	V _{CC} Power Supply Voltage	-0.6 ∿7.0	v
Vpp	Program Supply Voltage	-0.6 ∿14.0	v
VIN	Input Voltage	-0.6 ∿7.0	v
V _{I/O}	Input/Output Voltage	-0.6 ~ V _{CC} +0.5	v
P_{D}	Power Dissipation	1.5	W
TSOLDER	Soldering Temperature . Time	260 • 10	°C • sec
TSTG	Storage Temperature	-65 ~125	°C
T _{OPR}	Operating Temperature	0 ∿ 70	°C

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57256AD-12	TC57256AD-120/150
Ta	Operating Temperature	0 ∿ 70°C	0 ∿ 70°C
VCC	V _{CC} Power Supply Voltage	5V±5%	5V±10%
V _{PP}	V _{PP} Power Supply Voltage	V _{CC} -0.6V ∿V _{CC} +0.6V	V _{CC} -0.6V ~ V _{CC} +0.6V

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDIT	ION	MIN.	TYP.	MAX.	UNIT
ILI	Input Current	V _{IN} =0 ~ V _C	C	-	-	±10	μA
ILO	Output Leakage Current	V _{OUT} =0.4	~ v _{CC}	-	- 4	±10	μA
I _{CC01}	0	CE=0V	f=8.3MHz		-	30	mA
I _{CCO2}	Operating Current	I _{OUT} =OmA f=1MHz -	-	15			
Iccs1	Standby Current	<u>CE</u> =VIH		-	-	1	mA
I _{CCS2}	Scandby Current	CE=V _{CC} -0.	2V	-	-	100	μA
VIH	Input High Voltage	-		2.2	-	V _{CC} +0.3	V
VIL	Output Low Voltage	-		-0.3	-	0.8	v
v _{он}	Output High Voltage	I _{OH} =-400μ	I _{OH} =-400μA			•	v
V _{OL}	Output Low Voltage	I _{OL} =2.1mA		-	-	0.4	v
I _{PP1}	V _{PP} Current	V _{PP} =V _{CC} -0.	6 ~ V _{CC} +0.6	-	-	±10	μA

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	TC57256A	D-120/12	TC5725	UNIT	
SIMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	MIN.	MAX.	IUNII
tACC	Address Access Time	CE=OE=VIL	-	120	-	150	ns
t _{CE}	CE to Output Valid	OE=VIL	-	120	-	150	ns
t _{OE}	OE to Output Valid	CE=VIL	-	60	-	70	ns
t _{DF1}	CE to Output in High-Z	OE=VIL	0	50	0	60	ns
t _{DF2}	OE to Output in High-Z	CE=VIL	0	50	0	60	ns
t _{OH}	Output Data Hold Time	CE=OE=VIL	0	-	0	-	ns

A.C. TEST CONDITIONS

• Output Load : 1 TTL Gate and C_L =100pF

• Input Pulse Rise and Fall Times : 10ns Max. • Input Pulse Levels : $0.45 \text{V} \sim 2.4 \text{V}$

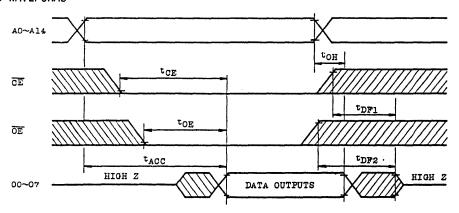
• Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CIN	Input Capacitance	v _{IN} =0v	-	4	6	pF
COUT	Output Capacitance	V _{OUT} =0V	-	8	12	pF

^{*} This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



TC57256AD-12, TC57256AD-120 TC57256AD-150

HIGH SPEED PROGRAM MODE I

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	Vcc+1.0	v
VIL	Input Low Voltage	-0.3		0.8	V
VCC	V _{CC} Power Supply Voltage	5.75	6.0	6.25	V
v_{PP}	Vpp Power Supply Voltage	12.0	12.5	13.0	V

D.C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

			-			
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ILI	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	±10	μA
VOH	Output High Voltage	I _{OH} =-400μA	2.4	-	-	V
VOL	Output Low Voltage	IOL=2.1mA	-	-	0.4	V
ICC	VCC Supply Current	-		-	30	mA
I _{PP2}	Vpp Supply Current	Vpp=13.0V	-	-	50	mA
V _{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, VCC=6V±0.25V, Vpp=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	-	-	μs·
t _{AH}	Address Hold Time	-	2	-	-	με
t _{CES}	CE Setup Time	-	0		-	ns
^t CEH	CE Hold Time	-	0	-	-	ns
toes	OE Setup Time	-	2	•	-	μs
t _{DS}	Data Setup Time	-	2	-	-	μs
tDH	Data Hold Time	-	2	-	-	μs
typs	Vpp Setup Time	-	2	-	-	μѕ
tvcs	V _{CC} Setup Time	-	2	-	-	μs
t _{PW}	Initial Program Pulse Width	CE=V _{IL} , OE=V _{IH}	0.95	1	1.05	ms
topw	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
^t OE	OE to Output Valid	CE=VIH	-	_	100	ns
t _{DFP}	OE to Output in High-Z	CE=V _{IH}	-	-	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L(100 pF)$

• Input Pulse Rise and Fall Times : 10ns Max. • Input Pulse Levels : 0.45V ~ 2.4V

• Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overpgoram pulse may vary as a function of the counter value X.

HIGH SPEED PROGRAM OPERATION II

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
v_{IH}	Input High Voltage	2.2	-	V _{CC} +1.0	V
VIL	Input Low Voltage	-0.3	-	0.8	V
v _{cc}	V _{CC} Power Supply Voltage	6.00	6.25	6.50	v
v_{PP}	Vpp Power Supply Voltage	12.50	12.75	13.00	v

D.C. AND OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	±10	μA
VOH	Output High Voltage	I _{OH} =-400μA	2.4	_	-	v
VOL	Output Low Voltage	I _{OL} =2.1mA	-		0.4	V
Icc	V _{CC} Supply Current	-	-	-	30	mA
I _{PP2}	Vpp Supply Current	V _{PP} =13.0V	-	-	50	mA
V _{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tAS	Address Setup Time	-	2	-	-	μs
t _{AH}	Address Hold Time	-	2	-	-	μs
tCES	CE Setup Time	_	0	-	-	ns
^t CEH	CE Hold Time	-	0	-	-	ns
tDS	Data Setup Time	-	2	-	-	μs
t _{DH}	Data Hold Time	-	2	-	-	με
t _{VPS}	Vpp Setup Time	-	2	-	-	μs
tvcs	V _{CC} Setup Time	-	2	-	-	μs
t _{PW}	Program Pulse Width	CE=VIL, OE=VIH	0.095	0.1	0.105	ms
toE	OE to Output Valid	CE=VIH	-	-	100	ns
tDFP	OE to Output in High-Z	CE=V _{IH}	-	-	90	ns

A.C. TEST CONDITIONS

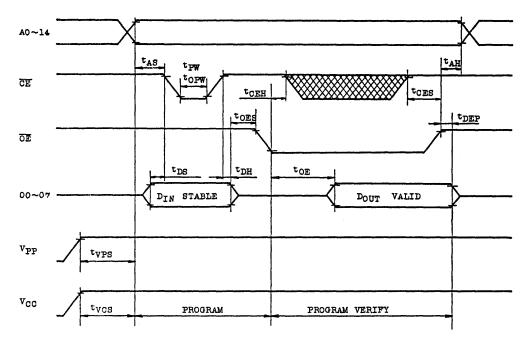
• Output Load : 1 TTL Gate and $C_L(100 \mathrm{pF})$

• Input Pulse Rise and Fall Time : 10ns Max. • Input Pulse Levels : 0.45V to 2.4V

• Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM MODE I (v_{CC} =6v±0.25v, v_{PP} =12.5v±0.5v)
HIGH SPEED PROGRAM MODE II (v_{CC} =6.25v±0.25v, v_{PP} =12.75v±0.25v)



Note 1. V_{CC} must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.

- 2. Removing the device from socket and setting the device in socket with $V_{\rm pp}$ =12.5V (12.75V) may cause permanent damage to the device.
- 3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57256AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537A°(Angstroms) to the chip through the transparent window.

The integrated dose (ultraviolet light intensity [w/cm²] x exposure time [sec.]) for erasure should be a minimum of 15 [w • sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of lcm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [μ w/cm²] will reduce the exposure time to about 20 minutes. (In the case, the integrated dose is 12000 [μ w/cm²] x (20 x 60) [sec] = 15 [w • sec/cm²].)

OPERATION INFORMATION

The TC57256AD's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

PIN NAMES (NUMBER) MODE			ŌĒ (22)	V _{PP} (1)	V _{CC} (28)	00 ∿ 07 (11 ∿13, 15 ∿ 19)	POWER
0 - 1 0	Read	L	L			Data Out	Active
Read Operation (Ta=0 ∿ 70°C)	Output Deselect	*	н	5V 5V	5V	High Impedance	
(1a=0 % /0 C)	Standby	н	*	1 [High Impedance	Standby
Program Occupation	Program	L	H	1) 12.5V	1)	Data In	
Program Operation (Ta=25±5°C)	Program Inhibit	H	Н	2)	6V 2)	High Impedance	Active
(14-23-3 0)	Program Verify	*	L	12.750		Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}, 1); HIGH SPEED PROGRAM MODE II

READ MODE

The TC57256AD has two control functions. The chip enable (CE) controls the operation power and should be used for device selection.

The output enable (OE) controls the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=VIL$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{\text{CE=V}_{IL}}$ and all addresses are valid, the output data is valid at the outputs after toe from the falling edge of $\overline{\text{OE}}$.

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}}=\text{V}_{\text{IH}}$ or $\overline{\text{OE}}=\text{V}_{\text{IH}}$, the outputs will be in a high impedance state. So two or more TC57256AD's can be connected together on a common bus line. When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

TC57256AD-12, TC57256AD-120 TC57256AD-150

STANDBY MODE

The TC57256AD has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC57256AD is placed in the standby mode which reduces the operating current to $100\mu\text{A}$ by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57256AD are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The TC57256AD is in the programming mode when the Vpp input is at 12.5V and $\overline{\text{CE}}$ is at TTL-Low under $\overline{\text{OE}}$ =VIH.

The TC57256AD can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{\text{OE}}$ at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V or +12.75V) is applied to Vpp terminal, a high level $\overline{\text{CE}}$ input inhibits the TC57256AD from being programmed. Programming of two or more TC57256AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{\text{CE}}$ and $\overline{\text{OE}}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{\text{CE}}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE I

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage ($\pm 12.5V$) is applied to the V_{PP} terminal with $V_{CC}=6V$.

The programming is achieved by applying a single TTL low level lms pulse to the CE input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied. When programming has been completed, the data in all addresses should be verified with VCC=Vpp=5V.

HIGH SPEED PROGRAM MODE II

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with V_{CC} =6.25V.

The programming is achieved by applying a single TTL low level 0.1ms pulse the CE input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

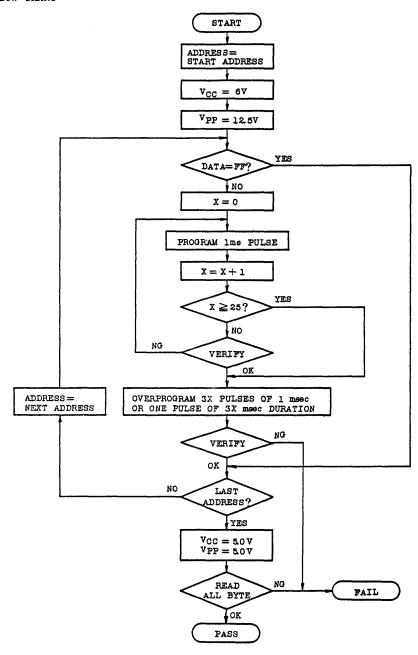
If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{\rm CC} = V_{\rm PP} = 5V$.

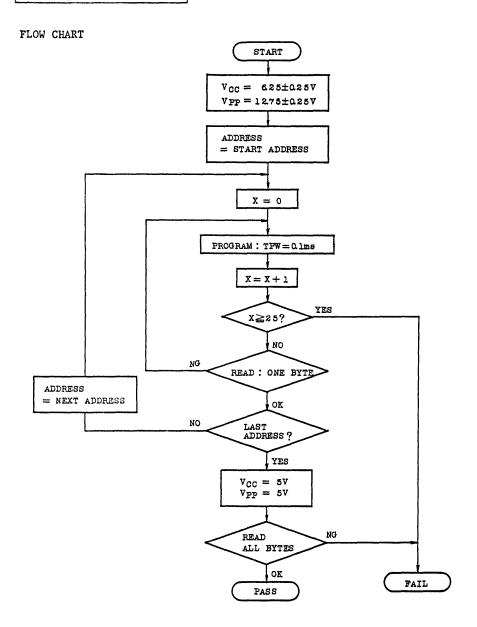


HIGH SPEED PROGRAM MODE I

FLOW CHART



HIGH SPEED PROGRAM MODE II



TC57256AD-12, TC57256AD-120 TC57256AD-150

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57256AD which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC57256AD by using this mode before program operation and automatically set program voltage $(V_{\rm PP})$ and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH} . These two codes possess an odd parity with the parity bit of MSB (07). The following table shows electric signature of TD57256AD.

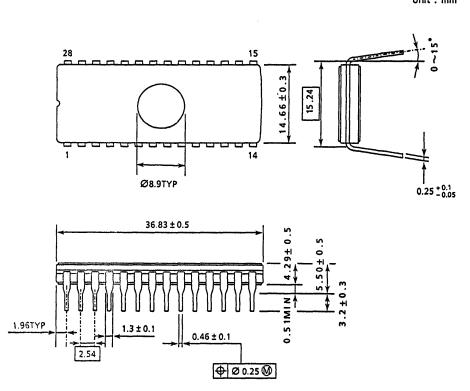
PINS SIGNATURE	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacture Code	VIL	1	0	0	1	1	0	0	0	98
Device Code	VIH	1	1	0	0	0	1	0	0	C4

Notes: A9=12V±0.5V

A1 ~ A8, A10 ~ A14, CE, OE=VIL

OUTLINE DRAWINGS WDIP28-G-600

Unit : mm



32,768 WORD x 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

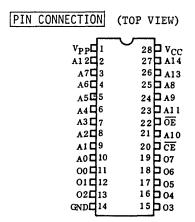
PRELIMINARY

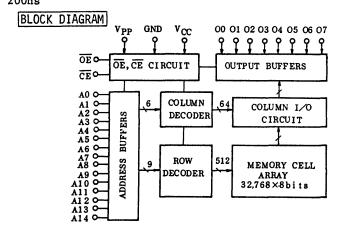
DESCRIPTION

The TC57256AD is a 32,768 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57256AD's access time is 150ns, and the TC57256AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{\text{CE}}$ input. Advanced CMOS technology reduces the maximum active current to 30mA/6.7MHz and standby current to $100\mu\text{A}$. For program operation, the programming is achieved by using the high speed programming mode. TC57256AD is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

FEATURES

- Peripheral circuit: CMOS Memory cell : N-MOS
- Low power dissipation Active: 30mA/6.7MHz Standby: 100uA
- Fast access time: TC57256AD-15 150ns TC57256AD-20 200ns
- Single 5V power supply
- · Fully static operation
- · High speed programming mode
- · Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, TMM27256AD and TC57256D
- Standard 28 pin DIP cerdip package





PIN NAMES

A0 ~ A14	Address Inputs
00 ∿ 07	Outputs (Inputs)
CE	Chip Enable Input
ŌĒ	Output Enable Input
Vpp	Program Supply Voltage
- VCC	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

PIN		ŌĒ	Vpp	VCC		POWER
MODE	(20)	(22)	(1)	(20)	$(11 \sim 13, 15 \sim 19)$	
Read	L	L			Data Out	Active
Output Deselect	*	H	50	5V	High Impedance	VCTIA
Standby	H	*			High Impedance	Standby
Program	L	H			Data In	
Program Inhibit	H	H	12.5V	6V	High Impedance	Active
Program Verify	*	L			Data Out	

* H or L

TC57256AD-15 TC57256AD-20

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
v _{cc}	Power Supply Voltage	-0.6 ∿ 7.0	v
V _{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
v _{IN}	Input Voltage	-0.6 ∿ 7.0	v
V _{I/O}	Input/Output Voltage	-0.6 ∿ V _{CC} +0.5	v
PD	Power Dissipation	1.5	W
TSOLDER	Soldering Temperature . Time	260 • 10	°C • sec
TSTRG	Storage Temperature	-65 ∿ 125	°C
TOPR	Operating Temperature	-40 ∿ 85	°C

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	_	V _{CC} +0.3	
VIL	Input Low Voltage	-0.3	-	0.8	
v _{cc}	V _{CC} Power Supply Voltage	4.75	5.00	5.25	V
V _{PP}	Vpp Power Supply Voltage	V _{CC} -0.6	v _{CC}	Vcc+0.6	

DC and OPERATING CHARACTERISTICS (Ta=-40 \sim 85°C, V_{CC}=5V±5%)

SYMBOL	PARAMETER	TEST CON	TEST CONDITION		TYP.	MAX.	UNIT
I _{LI}	Input Current	$\Lambda^{IN=0\Lambda} \sim \Lambda^{C}$	V _{IN} =0V ∿ V _{CC}		-	±10	μA
I _{CC01}		CE=0V		-	-	30	mA
I _{CCO2}	Operating Current	I _{OUT} =OmA	f=1MHz	-	-	10	шл
^I ccs1		CE=VIH		-	-	1	mA
I _{CCS2}	Standby Current	CE=V _{CC} -0.2	v	-	-	100	μA
v _{он}	Output High Voltage	I _{OH} =-400μA		2.4	-	-	٧
v _{OL}	Output Low Voltage	I _{OL} =2.1mA		-	-	0.4	V
I _{PP1}	VCC Current	VPP=VCC±0.	V _{PP} =V _{CC} ±0.6V		-	±10	μŅ
ILO	Output Leakage Current	V _{OUT} =0.4V ~ V _{CC}		-		±10	μA

AC CHARACTERISTICS (Ta=-40 \sim 85°C, V_{CC} =5V±5%, V_{PP} = V_{CC} ±0.6V)

CIRCROT	DADAMETER	THE CONTRACT	TC57256AD-15		TC57256AD-20		UNIT
SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	MIN.	MAX.	ONII
tACC	Address Access Time	CE=OE=VIL	-	150	-	200	
tCE	CE to Output Valid	OE=V _{IL}	-	150	-	200	
tOE	OE to Output Valid	CE=VIL	-	70	-	70	
t _{DF1}	CE to Output in High-Z	OE=VIL	0	60	0	60	ns
t _{DF2}	OE to Output in High-Z	CE=VIL	0	60	0	60	!
tOH	Output Data Hold Time	CE=OE=VIL	0	-	0	_	

AC TEST CONDITIONS

· Output Load

: 1 TTL Gate and C_L=100pF

• Input Pulse Rise and Fall Times

: 10ns Max.

• Input Pulse Levels

: 0.45V ~ 2.4V

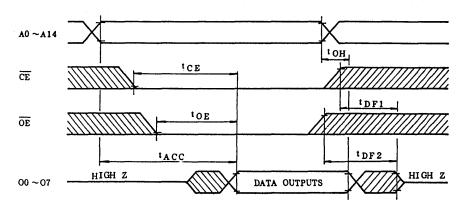
• Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CIN	Input Capacitance	V _{IN} =0V	-	4	6	pF
COUT	Output Capacitance	V _{OUT=} 0V	-	8	12	pF

^{*} This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	V _{CC} +1.0	
,V _{IL}	Input Low Voltage	-0.3	_	0.8	1 .,
v _{CC}	V _{CC} Power Supply Voltage	5.75	6.0	6.25	1 '
V _{PP}	V _{PP} Power Supply Voltage	12.0	12.5	13.0	1

DC and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0 ∿ V _{CC}	-	-	±10	μА
VOH	Output High Voltage	I _{OH} =-400µA	2.4	-	_	v
VOL	Output Low Voltage	I _{OL=2.1mA}	-	-	0.4	v
ICC	VCC Supply Current	-	-	-	30	mA
I _{PP2}	Vpp Supply Current	VPP=13.0V	-	-	50	mA
V _{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	v

AC PROGRAMMING CHARACTERISTICS (Ta=25 \pm 5°C, V_{CC}=6V \pm 0.25V, V_{PP}=12.5V \pm 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	-	-	μs
tAH	Address Hold Time	-	2	-	-	μS
t _{CES}	CE Setup Time	-	0	-	-	ns
t _{CEH}	CE Hold Time	_	0	-	-	ns
t _{OES}	OE Setup Time	-	2	-	-	μs
t _{DS}	Data Setup Time	-	2	-	-	μs
tDH	Data Hold Time	_	2	-	-	μs
typs	VPP Setup Time	_	2	-	-	μs
tvcs	VCC Setup Time	-	2	-	_	μs
t _{PW}	Initial Program Pulse Width	CE=V _{IL} , OE=V _{IH}	0.95	1	1.05	ms
tOPW	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t _{OE}	OE to Output Valid	CE=V _{IH}	-	-	150	ns
tDFP	OE to Output in High-Z	CE=V _{IH}	-	-	130	ns

AC TEST CONDITIONS

• Output Load : 1 TTL Gate and CL (100pF)

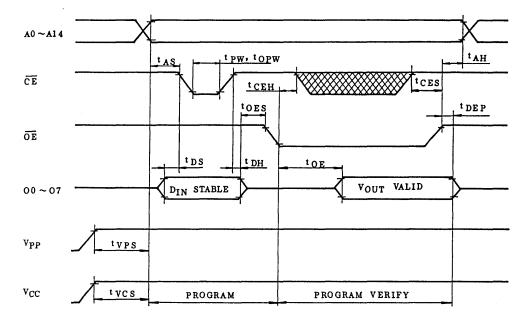
• Input Pulse Rise and Fall Times : 10ns Max. • Input Pulse Levels : $0.45 \text{V} \sim 2.4 \text{V}$

• Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

 $(V_{CC}=6V\pm0.25V, V_{PP}=12.5V\pm0.5V)$



- Note 1. V_{CC} must be applied simultaneously or before $V_{\mbox{\footnotesize{PP}}}$ and cut off simultaneously or after $V_{\mbox{\footnotesize{PP}}}$.
 - 2. Removing the device from socket and setting the device in socket with $V_{\rm PP}$ =12.5V may cause permanent damage to the device.
 - 3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57256AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537A°(Angstroms) to the chip through the transparent window.

The integrated dose (ultraviolet light intensity $[w/cm^2]$ x exposure time [sec.]) for erasure should be a minimum of 15 $[w \cdot sec/cm^2]$.

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 $[\mu w/cm^2]$ will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 $[\mu w/cm^2]$ x (20 x 60) $[sec] = 15 [w \cdot sec/cm^2]$.)

The TC57256AD's erasure begins to occur when exposed to light with wavelength shorter than 4000A. The sunlight and the fluorescent lamps will include $3000 \sim 4000$ A° wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC57256AD's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE	PIN NAMES (NUMBER)	CE (20)	ŌE (22)	V _{PP} (1)	V _{CC} (28)	00 \(^0.07\) (11 \(^1.013\), 15 \(^1.019\)	POWER	
	Read	L	L	(1)	5V 5V	Data Out	Active	
Read Operation	Output Deselect	*	H	5V		High Impedance	ACLIVE	
(Ta=-40 ∿ 85°C)	Standby	H	*			High Impedance	Standby	
Program Operation	Program	L	H			Data In		
(Ta=25±5°C)	Program Inhibit	Н	Н	12.5V	6V	High Impedance	Active	
	Program Verify	*	L			Data Out		

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC57256AD has two control functions. The chip enable $(\overline{\text{CE}})$ controls the operation power and should be used for device selection.

The output enable (\overline{OE}) control the output buffers, independent of device selection. Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{\text{CE}}\text{=V}_{\text{IL}}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}}=\text{V}_{\text{IH}}$ or $\overline{\text{OE}}=\text{V}_{\text{IH}}$, the outputs will be in a high impedance state. So two or more TC57256AD's can be connected together on a common bus line. When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57256AD has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC57256AD is placed in the standby mode which reduce the operating current to $100\mu\text{A}$ by applying MOS-high level (VCC) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57256AD are in the "l" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The TC57256AD is in the programming mode when the Vpp input is at 12.5V and CE is at TTL-Low under $\overline{\text{OE}}\text{=VIH}$.

The TC57256AD can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly porgrammed on the programmed bits.

The verify is accomplished with \overline{OE} at V_{TI} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage ($\pm 12.5V$) is applied to Vpp terminal, a high level $\overline{\text{CE}}$ input inhibits the TC57256AD from being programmed. Programming of two or more TC57256AD's in parallel with different data is easily ac-

rogramming of two or more TC5/256AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{\text{CE}}$ and $\overline{\text{OE}}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{\text{CE}}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

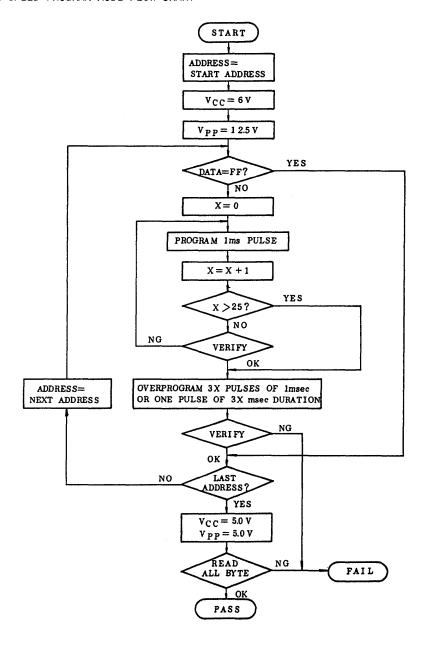
The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with $V_{CC}=6V$.

The programming is achieved by applying a single TTL low level lms pulse to the $\overline{\text{CE}}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of lms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times)

After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied. When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57256AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC57256AD by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest. of address lines is set to $V_{\rm IL}$ in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to $V_{\rm IH}$. These two codes possess an odd parity with the parity bit of MSB (07).

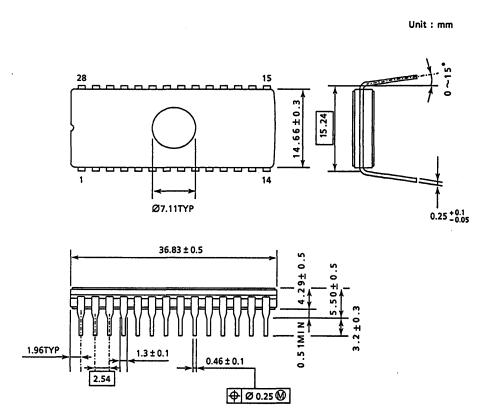
The following table shows electric signature of TC57256AD.

PINS	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacture Code	VIL	1	0	0	1	1	0	0	0	98
Device Code	VIH	1	1.	0	0	0	1	0	0	C4

Notes: A9=12V±0.5V

A1 \sim A8, A10 \sim A14, \overline{CE} , \overline{OE} = V_{IL}

OUTLINE DRAWINGS WDIP28-G-600A



65,536 WORDS x 8 BITS CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC57512AD is a 65,536 word \times 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57512AD's access time is 150ns/200ns, and the TC57512AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{\text{CE}}$ input. Advanced CMOS technology reduces the maximum active current to 30mA/6.7MHz and standby current to 100 μ A. For program operation, the programming is achieved by using the high speed programming mode. TC57512AD is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

FEATURES

- Peripheral circuit: CMOS Memory cell : N-MOS
- Fast access time: TC57512AD-15 150ns TC57512AD-20 200ns
- Low power dissipation Active : 30mA/6.7MHz Standby: 100µA

PIN	CONNECTI	ON	(TOI	VIEW)
	A15 [1 A12 [2	\neg	28	l V _{CC}
	A12 🗖 2		27	VCC
	A7 🗖 3		26	A13
	A6 🗖 4		25	l a8

лоц4	∞µ ws
A5 🗖 5	24 🗖 A9
A4 □ 6	23 🗖 A1 1
A3 🗖 7	22 □ 0E ∕ V P I
A2 🗆 8	21 🗖 A1 0
A1 🗗 9	20 🗖 CE
A0 🗖 10	19 🗖 07
00 ⊏ 11	18 🗖 06
01 🗖 12	17 🗖 05
02 🗖 13	16 🗖 04

15 03

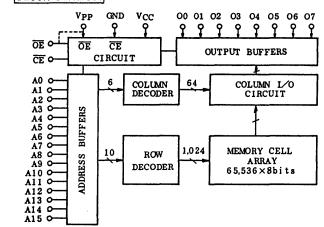
PIN NAMES

GND d 14

LTIA MALIT	:의
A0 ~ A15	Address Inputs
00 ∿ 07	Outputs (Inputs)
ĈĒ	Chip Enable Input
ŌĒ/V _{PP}	Output Program Enable Supply Input Voltage
v _{CC}	Power Supply Voltage (+5V)
GND	Ground

- Full static operation
- · High speed programming mode I, II
- · Inputs and outputs TTL compatible
- · Standard 28 pin DIP cerdip package

BLOCK DIAGRAM



MODE SELECTION

MODE	ČE (20)	OE/V _{PP} (22)	V _{CC} (28)	00 \(07 \) (11 \(\) 13,15 \(\) 19)	POWER
	(20)	(22)	(20)		
Read	L	L		Data Out	A - 4
Output Deselect	*	H	5V	High Impedance	Active
Standby	H	*		High Impedance	Standby
Program	L	v_{PP}	6V ¹)	Data In	
Program Inhibit	Н	v_{PP}	2)	High Impedance	Active
Program Verify	L	L	6.25V	Data Out	

- *: H or L
- 1): HIGH SPEED PROGRAMMING MODE I
- 2): HIGH SPEED PROGRAMMING MODE II

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
v _{cc}	V _{CC} Power Supply Voltage	-0.6 ~ 7.0	V
V _{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V _{IN}	Input Voltage	-0.6 ~ 7.0	٧
V _{I/O}	Input/Output Voltage	-0.6 ∿ V _{CC} +0.5	٧
PD	Power Dissipation	1.5	W
TSOLDER	Soldering Temperature • Time	260 • 10	°C•sec
TSTG	Storage Temperature	-65 ∿ 125	°C
T _{OPR}	Operating Temperature	-40 ∿ 85	°C

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57512AD-15/TC57512AD-20
Ta	Operating Temperature	-40 ∿ 85°C
VCC	V _{CC} Power Supply Voltage	5V±5%

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDI	TION	MIN.	TYP.	MAX.	UNIT
ILI	Input Current	$V_{\rm IN}=0 \sim V_{\rm CO}$	$V_{IN}=0 \sim V_{CC}$		-	±10	μА
ILO	Output Leakage Current	V _{OUT} =0.4 ∿	v _{CC}	-	_	±10	μА
I _{CC01}		CE=0V	CE=0V f=6.7MHz		-	30	mA
I _{CCO2}	Operating Current	I _{OUT} =OmA	f=1MHz	-	-	15	ша
I _{CCS1}	0. 11 0	CE=VIH		-	-	1	mA
I _{CCS2}	Standby Current	CE=V _{CC} -0.2	CE=V _{CC} -0.2V		-	100	μA
VIH	Input High Voltage	-		2.2	-	V _{CC} +0.3	V
VIL	Output Low Voltage	-		-0.3	-	0.8	V
v _{он}	Output High Voltage	I _{OH} =-400μA		2.4	-	-	V
V _{OL}	Output Low Voltage	I _{OL} =2.1mA		-	-	0.4	V
Ippl	V _{PP} Current	V _{PP} =0 ~ V _C (;+0.6	-	-	±10	μA

A.C. CHARACTERISTICS

arn/nor	DADAMETED	TEST CONDITION	TC5751	.2AD-15	TC575	UNIT	
SYMBOL	SYMBOL PARAMETER TEST CO		MIN.	MAX.	MIN.	MAX.	UNII
tACC	Address Access Time	CE=OE=VIL	-	150	-	200	ns
tCE	CE to Output Valid	<u>OE</u> =VIL	-	150	-	200	ns
toE	OE to Output Valid	CE=V _{IL}	-	70	-	70	ns
t _{DF1}	CE to Output in High-Z	OE=V _{IL}	0	60	0	60	ns
t _{DF2}	OE to Output in High-Z	CE=VIL	0	60	0	60	ns
t _{OH}	Output Data Hold Time	CE=OE=V _{IL}	0	-	0	 -	ns

A.C. TEST CONDITIONS

• Output Load

: 1 TTL Gate and CL=100pF

• Input Pulse Rise and Fall Times

: 10ns Max.

· Input Pulse Levels

: 0.45V ~ 2.4V

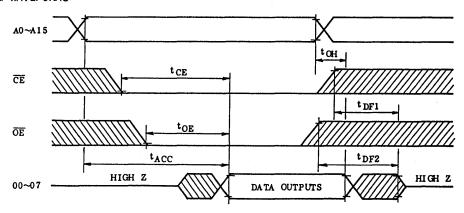
• Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C _{IN1}	Input Capacitance	v _{in} =ov	-	4	6	pF
C _{IN2}	OE/Vpp Input Capacitnace	V _{IN} =0V	_	50	60	pF
COUT	Output Capacitance	V _{OUT} =0V	-	8	12	pF

 $[\]mbox{\scriptsize {\tt \#}}$ This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



HIGH SPEED PROGRAM MODE I

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	V _{CC} +1.0	V
V _{IL}	Input Low Voltage	-0.3	-	0.8	V
V _{CC}	V _{CC} Power Supply Voltage	5.75	6.0	6.25	V
V _{PP}	V _{PP} Power Supply Voltage	12.0	12.5	13.0	v

DC and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

		(, ·(c)		, 11		
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	±10	μA
v _{OH}	Output High Voltage	I _{OH} =-400μA	2.4	T -	 	V
V _{OL}	Output Low Voltage	I _{OL} =2.1mA	-	 	0.4	V
I _{CC}	V _{CC} Supply Current	-	-	-	30	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} =13.0V	-	-	50	mA

AC PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tAS	Address Setup Time	-	2	_	-	μs
^t AH	Address Hold Time	-	2	_	-	μs
tOES	\overline{OE}/V_{PP} Setup Time	-	2	-	_	μs
t _{OEH}	$\overline{\text{OE}}/\text{V}_{ ext{PP}}$ Hold Time	-	2	_	-	μs
tPRT	$\overline{ ext{OE}}/ ext{V}_{ ext{PP}}$ Pulse Rise Time	-	50	-	-	ns
t _{DS}	Data Setup Time	460	2	***	-	μs
t _{DH}	Data Hold Time	-	2	-	-	μs
t _{VR}	OE/V _{PP} Recovery Time		2	-	-	μs
tvcs	V _{CC} Setup Time	-	2	-	-	μs
t _{PW}	Initial Program Pulse Width	CE=V _{IL} , OE/V _{PP} =V _{PP}	0.95	1.0	1.05	ms
tOPW	Overprogram Pulse Width	Note 1	2.85	3.0	78.75	ms
t _{DV}	Data Valid from CE	OE/VPP=VIL	-	-	1	μs
t _{DF}	CE to Output in High-Z	OE/VPP=VIL	-	-	130	ns

AC TEST CONDITIONS

• Output Load : 1 TTL Gate and C_L (100pF)

Input Pulse Rise and Fall Times
 Input Pulse Levels
 : 10ns Max.
 : 0.45V ~ 2.4V

• Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value $X_{\:\raisebox{1pt}{\text{\circle*{1.5}}}}$

HIGH SPEED PROGRAM MODE II

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	V _{CC} +1.0	V
VIL	Input Low Voltage	-0.3	-	0.8	V
v _{CC}	V _{CC} Power Supply Voltage	6.0	6.25	6.5	V
Vpp	Vpp Power Supply Voltage	12.5	12.75	13.0	V

DC and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)

					-	
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ILI	Input Current	V _{IN} =0 ∿ V _{CC}	-	-	±10	μA
V _{OH}	Output High Voltage	I _{OH} =-400μA	2.4	-	_	v
VOL	Output Low Voltage	I _{OL} =2.1mA	-	_	0.4	v
ICC	V _{CC} Supply Current	-	-	-	30	mA.
I _{PP2}	Vpp Supply Current	V _{PP} =13.0V	-	-	50	mA.

AC PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tAS	Address Setup Time	-	2	-	-	μs
tAH	Address Hold Time	-	2	-	-	μs
toes	OE/V _{PP} Setup Time	-	2	-	-	μs
^t OEH	OE/Vpp Hold Time	-	2	-	-	μs
tPRI	OE/V _{PP} Pulse Rise Time	-	50	-	-	ns
tDS	Data Setup Time	-	2	-	-	μs
t DH	Data Hold Time	-	2	-	-	μs
tvR	OE/V _{PP} Recovery Time	•	2	-	-	μs
tvcs	V _{CC} Setup Time	-	2	-	-	μѕ
^t PW	Program Pulse Width	CE=VIL, OE/Vpp=Vpp	0.095	0.1	0.105	ms
tDV	Data Valid from CE	OE/V _{PP} =V _{IL}	-	-	1	μs
t _{DF}	CE to Output in High-Z	ŌĒ/V _{PP} =V _{IL}		-	130	ns

AC TEST CONDITIONS

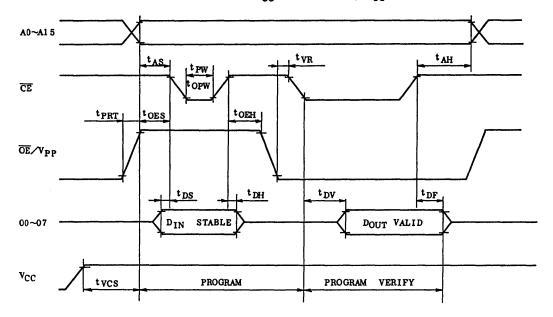
• Output Load : 1 TTL Gate and CL (100pF)

• Input Pulse Rise and Fall Times : 10ns Max. • Input Pulse Levels : $0.45 \text{V} \sim 2.4 \text{V}$

• Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAMMING MODE I ($V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$) HIGH SPEED PROGRAMMING MODE II ($V_{CC}=6.25V\pm0.25V$, $V_{PP}=12.75V\pm0.25V$)



Note 1. V_{CC} must be applied simultaneously or before $V_{\mbox{\footnotesize{pp}}}$ and cut off simultaneously or after $V_{\mbox{\footnotesize{pp}}}$.

- Removing the device from socket and setting the device in socket with Vpp=12.5±0.5V or Vpp=12.75±0.25V may cause permanent damage to the device.
- 3. The Vpp supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the Vpp terminal. When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57512AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. The integrated dose (ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²]. When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μ w/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [μ w/cm²] × (20 × 60) [sec] \cong 15 [w·sec/cm²].) The TC57512AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000 \sim 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC57512AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

	IN NAMES (NUMBER)	CE	ŌĒ	VPP	V _{CC}	00 ∿ 07	POWER
MODE		(20)	(22)	(1)	(28)	(11 ∿ 13, 15 ∿ 19)	
Bood Operation	Read	L	L			Data Out	
	Output Deselect	*	H	5V	5V	High Impedance	Active
(Ta=-40 ∿ 85°C)	Standby	Н	*			High Impedance	Standby
Program Operation	Program	L	Н	12.5V ¹⁾	6V ¹)	Data In	
	Program Inhibit	Н	H	1	21	High Impedance	Active
(Ta=25±5°C)	Program Verify	*	L	12.75V ²⁾	6.25V	Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}, 1); HIGH SPEED PROGRAM MODE I

READ MODE

The TC57512AD has two control functions. The chip enable (\overline{CE}) controls the operation power and should be used for device selection. The output enable (\overline{OE}) control the output buffers, independent of device selection. Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The \overline{CE} to output valid (t_{CE}) is equal to the address access time (t_{ACC}) . Assuming that $\overline{CE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after toe from the falling edge of \overline{OE} .

TC57512AD-15 TC57512AD-20

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TC57512AD's can be connected together on a common bus line. When \overline{CE} is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57512AD has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC57512AD is placed in the standby mode which reduce the operating current to 100µA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57512AD are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC57512AD is in the programming mode when the $\overline{\text{OE}}/\text{Vpp}$ input is at 12.5V or 12.75V and $\overline{\text{CE}}$ is at TTL-Low level. The TC57512AD can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{\text{OE}}/\text{Vpp}$ at V_{IL} and $\overline{\text{CE}}$ at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V or +12.75V) is applied to V_{pp} terminal, a high level \overline{CE} input inhibits the TC57512AD from being programmed. Programming of two or more TC57512AD's in parallel with different data is easily accomplished. That is, all inputs except for \overline{CE} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE I

This high speed programming mode I is performed at $V_{CC}=6.0V$ and $\overline{\rm OE}/V_{\rm PP}=12.5V$. The programming is achieved by applying a single TTL low level lms pulse to the $\overline{\rm CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of lms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with pulse width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{\rm CC}$ =5V.

HIGH SPEED PROGRAM MODE II

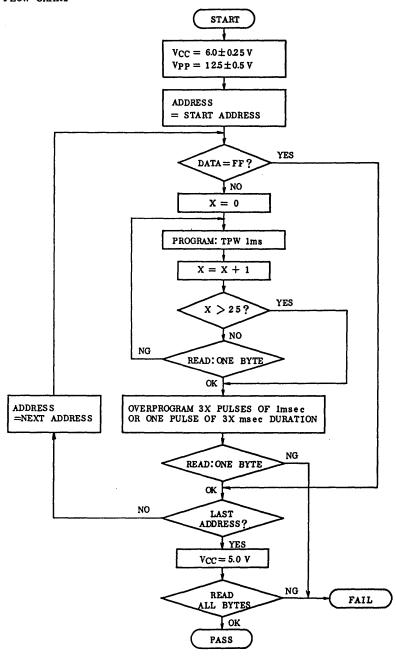
The program time can be greatly decreased by using this high speed programming mode II. This high speed programming mode II is performed at $V_{CC}=6.25V$ and $\overline{OE}/Vpp=12.75V$. The programming is achieved by applying a single TTL low level 0.1ms pulse to the \overline{CE} input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{\rm CC}$ =5V.

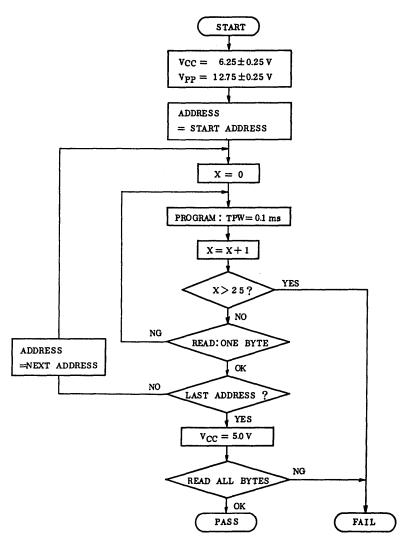
HIGH SPEED PROGRAM MODE I





HIGH SPEED PROGRAM MODE II

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57512AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC57512AD by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to $V_{\rm IL}$ in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to $V_{\rm IH}$. These two codes possess an odd parity with the parity bit of MSB (07). The following table shows electric signature of TC57512AD.

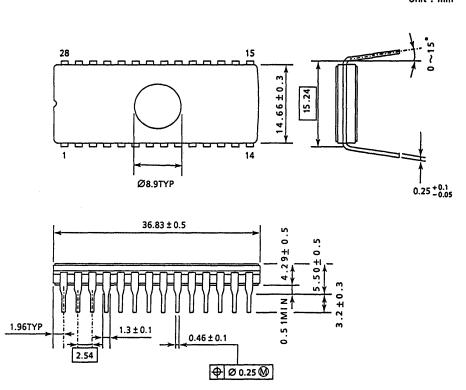
PINS	A0	07	06	05	04	03	02	01	00	HEX.
SIGNATURE	(10)	(19)	(18)	(17)	(16)	(15)	(13)	(12)	(11)	DATA
Manufacture Code	VIL	1	0	0	1	1	0	0	0	98
Device Code	VIH	1	0	0	0	0	1	0	1	85

Notes: A9=12V±0.5V

A1 \sim A8, A10 \sim A15, \overline{CE} , \overline{OE} = V_{TL}

OUTLINE DRAWINGS WDIP28-G-600

Unit: mm





131,072 WORD×8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC571000AD/TC571001AD is a 131,072 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory.

The TC571000AD is JEDEC standard pin configuration and the TC571001AD is compatible with 28 pin 1M bit Mask ROM. Both products are packed in 32 pin standard cerdip package.

The TC571000AD/TC571001AD is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 30mA/8.3MHz and access time of 120ns/150ns.

The programming times of the TC571000AD/TC571001AD except overhead times of EPROM programmer is only 14 seconds by using the high speed programming algoritim.

FEATURES

Peripheral circuit : CMOS
 Memory cell : N-MOS

• Access time

	- 12	- 150
Vcc	5V ± 5%	5V ± 10%
†ACC	120ns	150ns

• Low power dissipation
Active : S0mA/8.3MHz

Standby: 100µA

• Wide operating temperature range : 0~70°C

• Single 5V power supply

• Full static operation

• High speed programming operation : tpw 0.1ms

• Input and output TTL compatible

• JEDEC standard 32 pin : TC571000AD

• 1M MROM compatible : TC571001AD

• Standard 32 pin DIP cerdip package

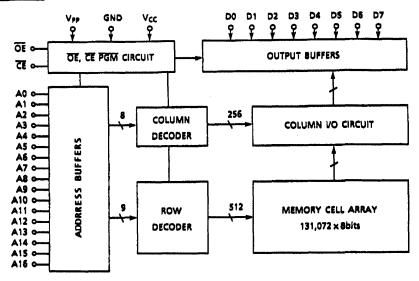
PIN CONNECTION (TOP VIEW)

Vpp	d · ·	32] Vcc	Vpp	d 1	¥ 32 Vcc		(Refe	rence)
A16	d 2	31 PGN		2	31) PG	₩,		
A15	₫ 3	30 NC	A15	1 3	300 NC	A15 [1	28] V _{CC}
A12	4	29DA14	A12	d 4	29 A14	L A12 [2	27[]A14
A7	₫ 5	28) A13	A7]	5	28 A13	A7 [3	26] A13
A6	d 6	27 A8	A6	6	27 A8	A6 [4	25] A8
A5	0 7	26] A9	A5 (d 7	26] A9	A5 [5	24] A9
A4	d a	25 A11	A4	8 1	25 A11	ı A4 ₫	6	23]A11
A3	(9	24) OE	A3	d 9	24] A16	; A3 [7	22]A16
A2	[10	23] A10	A2	10	23 A10) A2 [8	21]A10
A1	d 11	22] CE	A1	11	22) CE	A1 [9	20] [[
A0	d 12	2107	A0 1	12	21007	A0 [10	19] D7
D0	[13	20] D6	D0 [13	20] D6	D0 [11	18) D6
D1	[14	19) DS	D1 [14	19D D5	D1 [12	17] 05
D2	15	18] D4	D2 [15	180 04	D2 [13	16 <u>1</u> 3 D4
GND	16	<u>17</u> 1 D3	GND [16	<u>17</u> 103	GND [14	15) 03
	TC5710	OOAD		TC57	1001AD	1	M M	osk ROM

PIN NAMES

A0~A15	Address Inputs
D0~D7	Outputs (inputs)
CE.	Chip Enable Input
OE	Output Enable Input
PGM	Program Control Input
Vcc	V _{CC} Supply Voltage
Vpp	Program Supply Voltage
GND	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE	PGM	CE	QE	Vpp	Vcc	D0~D7	Power	
Read	Н	L	L			Data Out	Active	
Output Deselect	•	•	Н	5∨	5∨	High Impedance		
Standby	٠	н	•			High Impedance	Standby	
Program	L	L	н			Data In		
December to bible	•	Н	•	42.554	6.25V	High Impedance	Active	
Program Inhibit	н	L	н	12.75∨	0.230	High Impedance		
Program Verify	н	L	L			Data Out		

[.] H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	TINU
Vcc	V _{CC} Power Supply Voltage	- 0.6~7.0	V
Vpp	Program Supply Voltage	-0.6~14.0	V
VIN	Input Voltage	- 0.6~7.0	V
Vvo	Input/Output Voltage	- 0.6~V _{CC} + 0.5	V
PD	Power Dissipation	1.5	W
TSOLDER	Soldering Temperature Time	260 • 10	*C · sec
TSTRG	Storage Temperature	- 65~125	•c
TOPR	Operating Temperature	0~70	•c

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL		TC571000AD	/1001AD - 12	TC571000AD / 100	UNIT	
	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNII
ViH	Input High Voltage	2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	٧
V _{IL}	Input Low Voitage	- 0.3	0.8	- 0.3	0.8	٧
Vcc	V _{CC} Power Supply Voltage	4.75	5.25	4.50	5.50	٧
Vpp	V _{PP} Power Supply Voltage	V _{CC} - 0.6	V _{CC} + 0.6	V _{CC} = 0.6	V _{CC} + 0.6	٧

DC AND OPERATING CHARACTERISTICS (Ta=0~70°C)

SYMBOL	PARAMETER	TEST CONDITION V _{IN} = 0~V _{CC}		MIN.	TYP.	MAX.	UNIT
1 _{LI}	input Current			Current VIN = 0~VCC -	-	-	± 10
lcco1	Operating Current	Œ=0V f=8.3MHz		-	-	30	mA
lccoz	Operating Current	I _{OUT} = 0mA	f= 1MHz	-	_	10	
Iccs1	Standby Current	CE=V _{IH} CE=V _{CC} -0.2V		-	-	1	mA
Iccs2	Standby Current			-	-	100	μА
VoH	Output High Voltage	i _{OH} = -400µA		2.4	-	-	٧
VoL	Output Low Voltage	I _{OL} = 2.1mA		-	-	0.4	٧
lpp1	V _{PP} Current	Vpp = Vcc ± 0.6V		-	-	± 10	μА
ILO	Output Leakage Current	V _{OUT} = 0.4V~V _{CC}		-	-	10	μΑ

AC CHARACTERISTICS ($Ta=0\sim70^{\circ}C$, $V_{PP}=V_{CC}\pm0.6V$)

SIMBOL	PARAMETER	TC571000AD	/1001AD - 12	TC571000AD/10		
	PARAIVIETER	MIN.	MAX.	MIN.	MAX.	UNIT
tACC	Address Access Time	-	120	-	150	ns
^t CE	CE to Output Valid		120	-	150	ns
^t OE	OE to Output Valid	-	60	_	70	ns
tpgM	PGM to Output Valid	_	60	_	70	NS
t _{DF1}	CE to Output in High-Z	0	50	0	60	ns
t _{DF2}	OE to Output in High-Z	0	50	0	60	ns
[†] DF3	PGM to Output in High-Z	0	50	0	60	ns
[‡] ОН	Output Data Hold Time	0	_	0	-	ns

TC571000AD/TC571001AD-12 are satisfied with the specification of TC571000AD/TC571001AD-150.

AC TEST CONDITIONS

• Output Load

: 1 TTL Gate and CL=100pF

• Input Pulse Rise and Fall Times

: 10ns Max.

• Input Pulse Levels

: 0.45V~2.4V

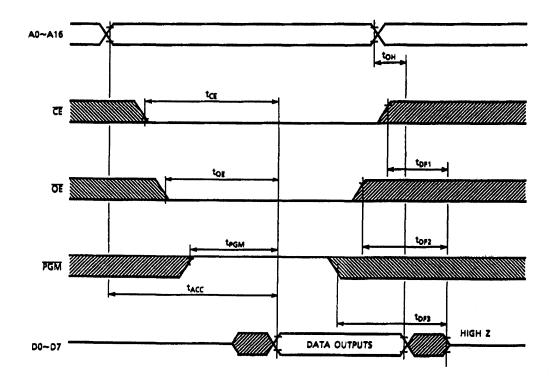
• Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CiN	input Capacitance	V _{IN} = 0V	-	4	9	P.
C _{OUT}	Output Capacitance	V _{OUT} = 0V	-	10	12	

^{*} This parameter is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	Vcc + 1.0	٧
VIL	Input Low Voltage	-0.3	-	0.8	٧
Vcc	V _{CC} Power Supply Voltage	6.00	6.25	6.50	٧
Vpp	V _{PP} Power Supply Voltage	12.50	12.75	13.00	٧

DC AND OPERATING CHARACTERISTICS ($T_2 = 25 \pm 5^{\circ}\text{C}$, $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	דואט
lu	Input Current	VIN = 0~VCC	-	-	± 10	ДA
VoH	Output High Voltage	l _{OH} = - 400μA	2.4	-	-	٧
Vol	Output Low Voltage	l _{OL} = 2.1mA	-	-	0.4	٧
lcc	V _{CC} Supply Current	_	-	-	30	mA
lpp2	V _{PP} Supply Current	Vpp = 13.0V	-	-	50	mA

AC PROGRAMMING CHARACTERISTICS ($T_8 = 25 \pm 5^{\circ}$ C, $V_{CC} = 6.25 V \pm 0.25 V$, $V_{PP} = 12.75 V \pm 0.25 V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tas	Address Setup Time	-	2	•	-	hz
t _{AH}	Address Hold Time	-	2	-	-	μι
tces	CE Setup Time	-	2	-	-	με
[‡] CEH	CE Hold Time	•	2	-	-	μs
tos	Data Set up Time	-	2	-	-	μι
t _{DH}	Data Hold Time	-	2	-	-	μs
tvs	V _{PP} Set up Time	-	2	-	-	μs
tpw	Program Pulse Width	-	0.095	0.1	0.105	ms
^t OE	OE to Output Valid	-	•	-	100	ns
tor2	OE to Output in High-Z	CE . VIL	-	•	90	ns

AC TEST CONDITIONS

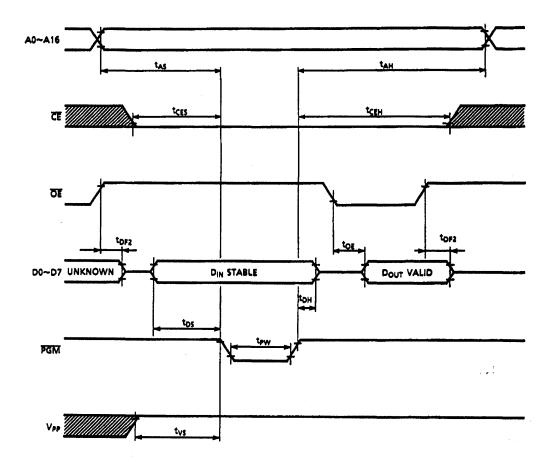
• Output Load : 1 TTL Gate and CL (100pF)

Input Pulse Rise and Fall Time : 10ns Max.
 Input Pulse Levels : 0.45V~2.4V

• Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



- Note 1. VCC must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.
 - 2. Removing the device from socket and setting the device in socket with VPP=12.75V may cause permanent damage to the device.
 - 3. The Vpp supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the Vpp terminal. When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC571000AD / TC571001AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

The integrated dose (ultraviolet light intensity $[w/cm^2]\times exposure$ time [sec.]) for erasure should be a minimum of 15 $[w\cdot sec/cm^2]$.

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of lcm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [μ w/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000[μ w/cm²]× (20×60) [sec.] \simeq 15 [w·sac/cm²].)

The TC571000AD / TC571001AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC571000AD/TC571001AD's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE	PIN	PGM	CE	ŌĒ	Vpp	Vcc	D0~D7	POWER	
Read	Read	H	L	L			Data Out	Active	
Operation	Output Deselet	*		Н	5∨	5V	High impedance	ACTIVE	
(Ta = 0~70°C)	Standby	•	H	10			High Impedance	Standby	
Program	Program	L	L	X	12.75V 6.25V			Data in	
Operation	Program Inhibit	•	H	*		6 351/	High Impedance	Active	
(Ta = 25 ± 5°C)	Program innight	Н	L	н		12.75	6.254	High Impedance	ACTIVE
	Program Verify	н	L	L	<u> </u>		Data Out		

Note: H; VIH, L: VIL, *: VIH or VIL

READ MODE

The TC571000AD/TC571001AD has three control functions. The chip enable (CE) controls the operation power and should be used for device selection. The output enable (OE) and the program control (FGM) control the output buffers independent of device selection.

Assuming that $\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}$ and $\overline{\text{PGM}} = V_{\text{IH}}$, the output data will be valid at the output after address access time from stabilizing of all addresses. The CE to output valid (top) is equal to the address access time (tacc).

Assuming that $\overline{CE}=V_{IL}$, $\overline{FGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after tog from the falling edge of \overline{OE} . And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after trom from the rising edge of \overline{FGM} .

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line. When \overline{CE} is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC571000AD/TC571001AD has a low power standby mode controlled by the CE signal. By applying a high level to the CE input, the TC571000AD/TC571001AD is placed in the standby mode which reduce the operating current to 100µA by applying MOS-high level (VCC) and then the outputs are in a high impedance state, independent of the OE inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC571000AD/TC571001AD is in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The levels required for all inputs are TTL.

The TC571000AD / TC571001AD can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with \overline{OE} and \overline{CE} at V_{IL} and \overline{PGM} at V_{IH} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to Vpp terminal, a high level $\overline{\text{CE}}$ or $\overline{\text{PGM}}$ input inhibits the TC571000AD/TC571001AD from being programmed.

Programming of two or more EPROM's in inputs except for CE or PGM may be commonly connected, and a TTL low level program pulse is applied to the CE and PGM of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

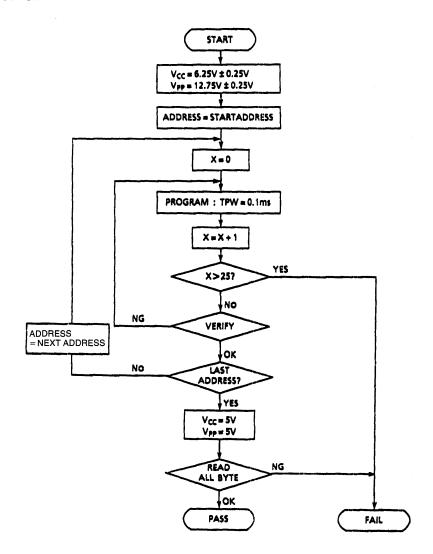
The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the Vpp terminal with $V_{CC}=6.25\text{V}$ and $\overline{PGM}=V_{IH}$.

The programming is achieved by applying a single TTL low level 0.1ms pulse the FGM input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC571000AD / TC571001AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC571000AD / TC571001AD by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{II}, in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{II}.

These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC571000AD/TC571001AD.

SIGNATURE	PINS	AO	D7	D6	D 5	D4	D3	D2	D1	D0	HEX Data
Manufacture C	ode	VIL	1	0	Ö	1	1	0	0	0	98
Davids Cada	TC571000AD		1	0	0	0	0	1	1 "	0	86
Device Code	TC571001AD	V _{IH}	0	0	0	0	0	1	1	1	07

Notes: A9=12V±0.5V

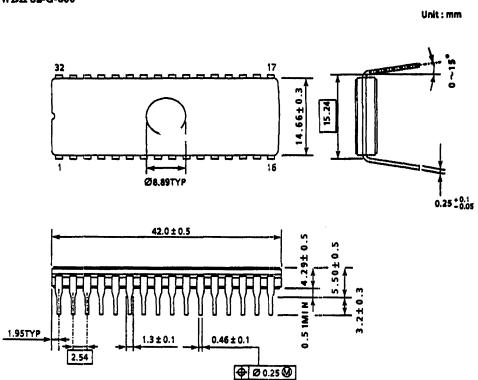
A1~A8, A0~A16, \overline{CE} , $\overline{OE} = V_{IL}$

POM = VIH

OUTLINE DRAWINGS

• Cerdip DIP

WDIP32-G-600



1 MEGA BIT (65,536 WORD x 16 BIT) CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC571024D is a 65,536 word $\times 16$ bit CMOS ultraviolet light erasable and electrically programmable read only memory.

The TC571024D is JEDEC standard pin configuration. This product is packaged in 40 pin standard cerdip package.

TC571024D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and lowpower features with a maximum operating current of 40mA/6.7MHz and access time of 150ns/200ns.

The programming times of the TC571024D except overhead times of EPROM programmer is only 7 seconds by using the high speed programming algorithm.

FEATURES

• Peripheral circuit: CMOS

Memory cell

: N-MOS

· Fast access time

	TC571024D-15	TC571024D-20	TC571024D-200
Ta	0 ∿ 70°C	~40 ∿	85°C
v_{cc}	5V±	:5%	5V±10%
^t ACC	150ns	20)Ons

· Low power dissipation

Active: 40mA/6.7MHz Standby: 100µA

- · Single 5V power supply
- · Full static operation
- High speed programming operation:
 tpw 0.1ms
- · Input and output TTL compatible
- JEDEC standard 40 pin: TC571024D
- · Standard 40 pin DIP cerdip package

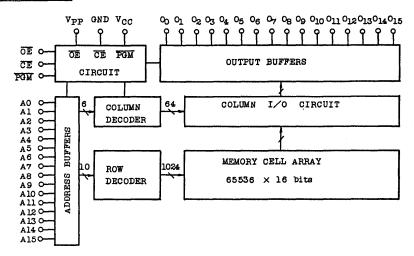
PIN CONNECTION (TOP VIEW)

			•	
1000 F	Γ.	$\neg \checkmark$		L,,,
VPP [T -	_	40	$P^{v_{\infty}}$
CE [2		39	POM
D15 🗀			38	Ьи. с.
D14 C	4		37	A15
D13	1		36	JA14
DIS [6		35	IA13
D11 🗀	7		34	TA12
D10 🗖	8		33	All
D9	9		32	J A10
D8 🗖	10		31] A9
Vss C			30	⊐Vss
D7 🗀	12		29	JAB
D6 🗖	13		28] A7
D5 🗀	14		27]A6
D4 🗀	15			J A5
D3 🗖			25]A4
D2 🗆			24	3 A3
D1 🗖	18		23	SA
Do 🗖	19		22]Al
OE 🗖	20		21	DA
,				

PIN NAMES

A0 ~ A15	Address Inputs
DO ∿ D15	Outputs (Inputs)
CE	Chip Enable Input
ŌĒ	Output Enable Input
PGM	Program Control Input
v _{cc}	VCC Supply Voltage
V _{PP}	Program Supply Voltage
VSS	Ground
N.C.	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE	CE	ŌĒ	P GM	v _{PP}	VCC	D ₀ ∿ D ₁₅	POWER
Read	L	L	H			Data Out	Active
Output Deselect	*	H	*	5v	5V	High Impedance	ACCIVE
Standby	Н	*	*			High Impedance	Standby
Program	L	*	L			Data In	
Program Inhibit	Н	*	*	12.750	6 25V	High Impedance	Active
110gram tillitote	L	Н	Н]	0.25	might impedance	ACCIVE
Program Verify	L	L	Н			Data Out	,

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
VCC	V _{CC} Power Supply Voltage	-0.6 ∿ 7.0	v
V _{PP}	Program Supply Voltage	-0.6 ∿ 14.0	. V
VIN	Input Voltage	-0.6 ∿ 7.0	٧
VIN (A9)	Input Voltage (A9)	-0.6 ∿ 13.5	V
VI/O	Input/Output Voltage	-0.6 ∿ Vcc+0.5	v
P _D	Power Dissipation	1.5	W
TSOLDER	Soldering Temperature Time	260 • 10	°C•sec
T _{STRG}	Storage Temperature	-65 ∿ 125	°C
TOPR	Operating Temperature	-40 ∿ 85	°C

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC571024D-15	TC571024D-20	TC571024D-200
Ta	Ambient Temperature	0 ∿ 70°C	-4	0 ∿ 85°C
V _{CC}	V _{CC} Power Supply Voltage	5V	'±5%	5V±10%
V _{PP}	V _{PP} Power Supply Voltage	V _{CC} -0.6	V ~ V _{CC} +0.6V	$V_{CC}-0.6V \sim V_{CC}+0.6V$

D.C. and OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	TEST	TEST CONDITION		TYP.	MAX.	UNIT
ILI	Input Current	$V_{IN}=0 \sim V_{CC}$		-	-	±10	μA
I _{CCO1}	Onestine Correct	CE=0V	t _{cycle} =150ns	-	-	40	mA
I _{CCO2}	Operating Current	I _{OUT} =OmA	t _{cycle} =1µs	-	-	20	ша
I _{CCS1}	Standby Current	CE=VIH		-	-	1	mA
I _{CCS2}	Standby Current	CE=V _{CC} -0.	2V	-	-	100	μA
VIH	Input High Voltage		-	2.2	-	V _{CC} +0.3	v
v_{IL}	Input Low Voltage		-	-0.3	-	0.8	V
voH	Output High Voltage	I _{OH} =-400μ	A	2.4	-	-	V
v _{OL}	Output Low Voltage	I _{OL} =2.1mA		-	-	0.4	V
I _{PP1}	Vpp Current	V _{PP} =V _{CC} ±0	.6V	-	-	±10	μA
ILO	Output Leakage Current	V _{OUT} =0.4V	~ V _{CC}	-	-	±10	μA

A.C. CHARACTERISTICS (VPP=VCC±0.6V)

CVMDOT	DADAMETER	TC5710	24D-15	TC571024	D-200/-20 MAX. 200 200 70 60	TC571024D-200/-20	
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT	
tACC	Address Access Time	-	150	-	200		
t _{CE}	CE to Output Valid	_	150	-	200		
t _{OE}	OE to Output Valid	-	70	_	70		
t _{DF1}	CE to Output in High-Z	0	60	0	60	ns	
tDF2	OE to Output in High-Z	0	60	0	60		
tOH	Output Data Hold Time	0	-	0	-		

A.C. TEST CONDITIONS

Output Load : 1 TTL Gate and C_L =100pF

Input Pulse Rise and Fall Times : 10ns Max.

Input Pulse Levels : 0.45V to 2.4V

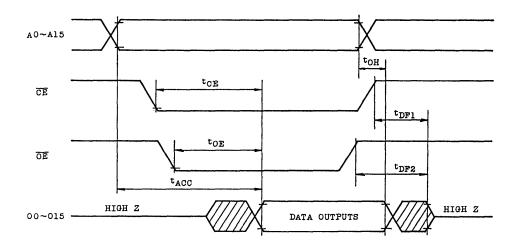
Timing Measurement Reference Level: Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CIN	Input Capacitance	V _{IN} =OV	-	6	10	_
COUT	Output Capacitance	V _{OUT} =0V	-	10	12	pF

^{*} This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	V _{CC} +0.3	
VIL	Input Low Voltage	-0.3	_	0.8] "
v _{cc}	V _{CC} Power Supply Voltage	6.00	6.25	6.50]
VPP	Vpp Power Supply Voltage	12.50	12.75	13.00	

D.C. AND OPERATING CHARACTERISTICS (Ta=25±5°C, VCC=6.25±0.25V, VPP=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	VIN=0 ~ VCC	-	-	±10	μА
v _{OH}	Output High Voltage	I _{OH} =-400μA	2.4	-	_	v
v_{OL}	Output Low Voltage	I _{OL} =2.1mA	-	-	0.4	v
I _{CC}	V _{CC} Supply Current	_	-	-	40	mA
I _{PP2}	Vpp Supply Current	V _{PP} =13.0V	-	-	100	mA

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, VCC=6.25±0.25V, Vpp=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tAS	Address Setup Time	-	2	-	-	μs
^t AH	Address Hold Time	-	2	_	-	μs
tCES	CE Setup Time	-	2	-	-	μѕ
t CEH	CE Hold Time	-	2	-	_	μs
t _{DS}	Data Setup Time	-	2	-	-	μs
t _{DH}	Data Hold Time	-	2	-	-	μs
tVS	Vpp Setup Time	-	2	-	_	μs
TPW	Program Pulse Width	-	0.095	0.1	0.105	ms
^t OE	OE to Output Valid		-	-	500	ns
t _{DF2}	OE to Output in High-Z	ÖE=VIL	-	-	150	ns
toes	OE Setup Time	-	2.0	_	-	μѕ

A.C. TEST CONDITIONS

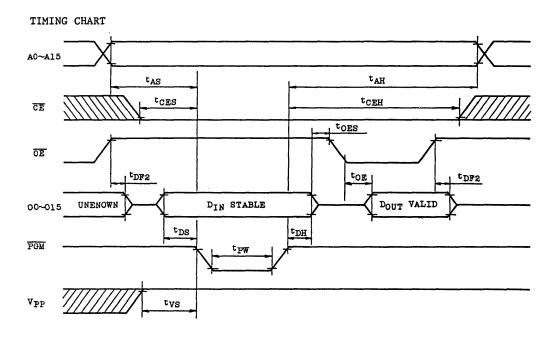
- Output Load : 1 TTL Gate and $C_{\rm L}$ (100pF)

• Input Pulse Rise and Fall Time : 10ns Max.

• Input Pulse Levels : 0.45V and 2.4V

• Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION



Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

- 2. Removing the device from socket and setting the device in socket with Vpp=12.75V may cause permanent damage to the device.
- 3. The Vpp supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the Vpp terminal. When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC571024D erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. The integrated dose (Ultraviolet light intensity $[W/cm^2] \times exposure time [sec.]$) for erasure should be a minimum of 15 $[W.•sec/cm^2]$.

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of lcm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 $[\mu W/cm^2]$ will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 $[\mu W/cm^2] \times (20 \times 60)$ [sec] =15 $[W \cdot sec/cm^2]$.) The TC571024D erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000 \sim 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TC571024D six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

	PIN	CE	ŌĒ	PGM	V _{PP}	v _{cc}	DO ∿ D15	POWER
READ	Read	L	L	Н			Data Out	Active
OPERATION	Output Deselect	*	Н	*	5V	50	High Impedance	ACLIVE
	Standby	Н	*	*			High Impedance	Standby
PROGRAM	Program	L	*	L			Data In	
OPERATION	Program Inhibit	Н	*	*	12.75V	6.25V	Ndah Tanadanaa	Active
(Ta=25±5°C)	riogram innibit	L	Н	Н	12./50	0.234	High Impedance	Accive
	Program Verify	L	L	H			Data Out	

Note: H; V_{IH} , L; V_{IL} , *; V_{IH} or V_{IL}

TC571024D-15, TC571024D-200 TC571024D-20

READ MODE

The TC571024D has three control functions. The chip enable ($\overline{\text{CE}}$) controls the operation power and should be used for device selection.

The output enable (\overline{OE}) control the output buffers, independent of device selection. Assuming in that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{\text{CE}}=\text{V}_{\text{IL}}$, $\overline{\text{PGM}}=\text{V}_{\text{IH}}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}}=\text{V}_{\text{IH}}$ or $\overline{\text{OE}}=\text{V}_{\text{IH}}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line. When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC571024D has a low power standby mode controlled by the CE signal.

By applying a high level to the $\overline{\text{CE}}$ input, the TC571024D is placed in the standby mode which reduce the operating current to 100 μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC571024D are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC571024D can be programmed any location at anytime—either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{\text{OE}}$ and $\overline{\text{CE}}$ at V_{TI} and $\overline{\text{PGM}}$ at V_{TH} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{pp} terminal, a high level \overline{CE} or \overline{PGM} input inhibits the TC571024D from being programmed. Programming of two or more EPROMS in parallel with different data is easily accomplished. That is, all inputs except for \overline{CE} or \overline{PGM} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} and \overline{PGM} of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

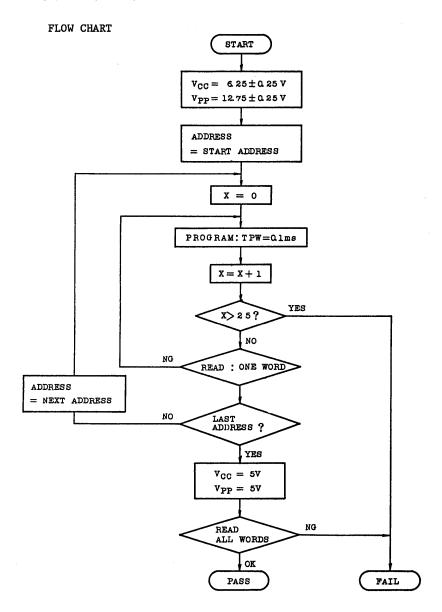
The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with V_{CC} =6.25V and \overline{PGM} = V_{TH} .

The programming is achieved by applying a single TTL low level 0.1 ms pulse the PGM input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{\rm pp}=5V$.

HIGH SPEED PROGRAM OPERATION



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC571024D which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC571024D by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to $V_{\rm IL}$ in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to $V_{\rm IH}$. These two codes possess an odd parity with the parity bit of (07). The following table shows electric signature of TC571024D.

PINS SIGNATURE	A ₀	015	014	013	012	011	010	و٥	08	07	06	05	04	03	02	01	00	HEX. DATA
Manufacture Code	VIL	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	VIH	*	*	*	*	*	*	*	*	0	0	0	0	1	0	0	0	**08

Notes: A9=12V±0.5V, A1 ∿A8, A10 ∿A15, CE, OE=VIL, PGM=VIH

*: Don't Care

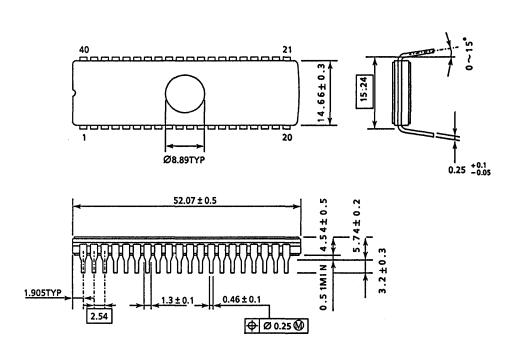
D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
v_{ID}	A9 Auto Select Voltage	11.5	12.0	12.5	v

TC571024D-15, TC571024D-200 TC571024D-20

OUTLINE DRAWINGS WDIP40-G-600

単位:mm



524,288 WORD × 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC574000D is a 524,288 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC574000D's access time is 120ns, and the TC574000D operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the $\overline{\text{CE}}$ input.

Advanced CMOS technology reduces the maximum active current to 60mA / 8.3MHz and standby current to 100µA. For program operation, the programming is achieved by using the high speed programming mode. TC574000D is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

FEATURES

• Peripheral circuit

: CMOS

Memory cell

: N-MOS

• Access time

	- 12	- 120	- 150
V _{CC}	5V ± 5%	5V ±	10%
Temp		0°C~70°C	
t _{ACC}	120)ns	150ns

• Low power dissipation

Active: 60mA/8.3MHz

Standby: $100\mu A (Ta = 70^{\circ}C)$

- High speed programming operation
- Single 5V power supply
- Full static operation
- Input and output TTL compatible
- JEDEC standard 32 pin
- Standard 32 pin DIP cerdip package

PIN CONNECTION	(TOP VIEW)

V _{PP} A16 A15 A12 A7 A6 A5 A4 A3 A2 A1 A0 D0	1 2 3 4 5 6 6 7 8 9 10 11 12	32] V _{cc} 31] A18 30] A17 29] A14 28] A13 27] A8 26] A9 25] A11 24] OE 23] A10 22] CE 21] D7 20] D6
A0	12	21 07
D0 D1 D2	U13 U14 U15	19 D5
GND	16	17 03

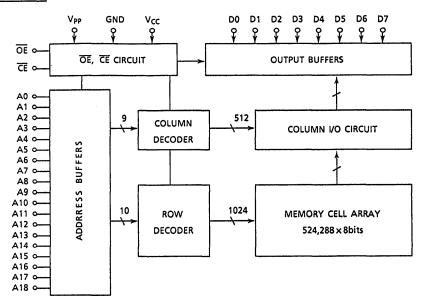
TC574000D

PIN NAMES

A0~A18	Address Inputs
D0~D7	Outputs (Inputs)
CE	Chip Enable Input
ŌĒ	Output Enable Input
Vcc	V _{CC} Supply Voltage
V _{PP}	Program Supply Voltage
GND	Ground

TC574000D-12, TC574000D-120 TC574000D-150

BLOCK DIAGRAM



MODE SELECTION

MODE	CE	ŌĒ	V _{PP}	Vcc	D0~D7	Power	
Read	L	L			Data Out	Active	
Output Deselect	* H		5V	5V	High Impedance	Active	
Standby	Н	*			High Impedance	Standby	
Program	L	н			Data In		
Program Inhibit	Н	Н	12.50V	6.25V	High Impedance	Active	
Program Verify	+ .	L			Data Out	7	

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	- 0.6~7.0	V
V _{PP}	Program Supply Voltage	-0.6~14.0	V
V _{IN} Input Voltage		- 0.6~7.0	٧
V _{IN} (A9)	Input Voltage (A9)	-0.6~13.5	V
V _{I/O}	Input/Output Voltage	-0.6~V _{CC} +0.5	V
P _D	Power Dissipation	1.5	w
T _{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T _{strg}	Storage Temperature	- 65~125	°C
Topr	Operating Temperature	0~70	•€

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC574000D - 12	TC574000D - 120 / 150
V _{IH}	Input High Voltage	2.2V~V _{CC} + 0.3V	2.2V~V _{CC} +0.3V
V _{IL}	Input Low Voltage	-0.3V~0.8V	0.3V~0.8V
Vcc	V _{CC} Power Supply Voltage	5V ± 5%	5V ± 10%
V _{PP}	V _{PP} Power Supply Voltage	V _{CC} - 0.6V~V _{CC} + 0.6V	V _{CC} - 0.6V~V _{CC} + 0.6V

DC AND OPERATING CHARACTERISTICS (Ta=0~70°C)

SIMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
ILI	Input Current	V _{IN} = 0~V _{CC}		-	-	± 10	μА
1		CE = V _{IL}	f = 8.3MHz	-	-	60	
lcco1	Operating Current		f = 6.7MHz	-	-	50	mA
I _{CCO2}		I _{OUT} = 0mA	f = 1MHz	-	-	15	
I _{CCS1}	C. 11 C.	CE = V _{IH}		-	-	1	mA
I _{CCS2}	Standby Current	$\overline{CE} = V_{CC} - 0.$	2V	_	_	100	μА
V _{OH}	Output High Voltage	l _{OH} = - 400μ	A	2.4	-	-	V
VoL	Output Low Voltage	I _{OL} = 2.1mA		-	-	0.4	V
I _{PP1}	V _{PP} Current	V _{PP} = V _{CC} ± 0.6V		-	-	± 10	μА
I _{LO}	Output Leakage Current	V _{OUT} = 0.4V~V _{CC}		-	_	± 10	μА

AC CHARACTERISTICS ($Ta=0\sim70^{\circ}C$, $V_{PP}=V_{CC}\pm0.6V$)

SIMBOL	PARAMETER	TEST CONDITION	TC574000	D - 12/120	TC57400	0D - 150	UNIT
SIIVIBOL	PARAIVIETER	TEST CONDITION	MIN.	MAX.	MIN.	MAX.	UNII
t _{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	_	120	_	150	ns
t _{CE}	CE to Output Valid	OE = V _{IL}	-	120	_	150	ns
t _{OE}	OE to Output Valid	CE = V _{IL}	_	60	_	70	ns
t _{DF1}	CE to Output in High-Z	OE = V _{IL}	0	50	0	60	ns
t _{DF2}	OE to Output in High-Z	CE = VIL	0	50	0	60	ns
t _{ОН}	Output Data Hold Time	CE = OE = V _{IL}	0	-	0		ns

AC TEST CONDITIONS

• Output Load : 1 TTL Gate and C_L=100pF

Input Pulse Rise and Fall Times : 10ns Max.
Input Pulse Levels : 0.45V~2.4V

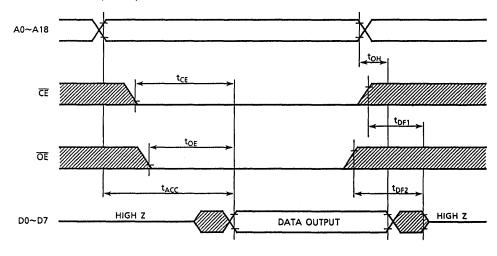
• Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	-	9	PF
Cout	Output Capacitance	V _{OUT} = 0V	-	13	FF

^{*}This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	V _{CC} + 1.0	٧
V _{IL}	Input Low Voltage	- 0.3	-	0.8	V
V _{CC}	V _{CC} Power Supply Voltage	6.00	6.25	6.50	V
V _{PP}	V _{PP} Power Supply Voltage	12.20	12.50	12.80	V

DC AND OPERATING CHARACTERISTICS (Ta=25±5°C,V_{CC}=6.25V±0.25V,Vpp=12.50V±0.30V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
lu	Input Current	V _{IN} = 0~V _{CC}		_	± 10	μА
V _{OH}	Output High Voltage	I _{OH} = -400μA	2.4	-	-	٧
V _{OL}	Output Low Voltage	1 _{OL} = 2.1mA	-	-	0.4	٧
lcc	V _{CC} Supply Current	-	-	-	30	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} = 12.8V	-	-	50	mA

AC PROGRAMMING CHARACTERISTICS ($Ta = 25 \pm 5^{\circ}C$, $V_{CC} = 6.25 V \pm 0.25 V$, $V_{PP} = 12.50 V \pm 0.30 V$)

SYMBOL	PAŔAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	-	-	μs
t _{AH}	Address Hold Time	-	2	-	-	μs
t _{CES}	CE Setup Time	-	0		-	μs
t _{CEH}	CE Hold Time	-	0	-	-	μs
t _{OES}	ŌĒ Set up Time	-	2		-	μs
t _{DS}	Data Set up Time	-	2	_	_	μs
t _{DH}	Data Hold Time	-	2	-	-	μs
t _{VPS}	V _{PP} Set up Time	-	2	_	_	μς
t _{VCS}	V _{CC} Set up Time	_	2	-	_	μς
t _{PW}	Program Pulse Width	$\overline{CE} = V_{IL}, \ \overline{OE} = V_{IH}$	45	50	55	μs
t _{OE}	OE to Output Valid	CE = VIH	-	-	100	ns
t _{DFP}	OE to Output in High-Z	CE = VIH	_	-	90	ns

AC TEST CONDITIONS

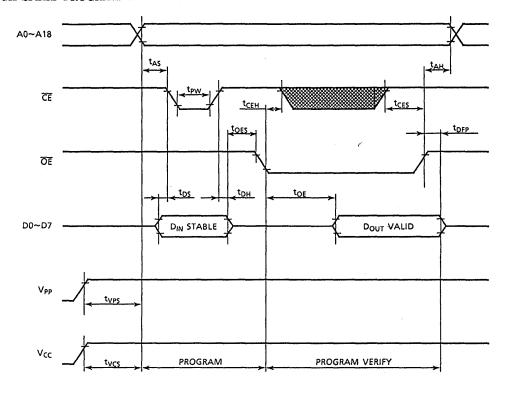
• Output Load : 1 TTL Gate and C_L (100pF)

Input Pulse Rise and Fall Time : 10ns Max.
 Input Pulse Levels : 0.45V~2.4V

Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



Note 1. VCC must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.

- 2. Removing the device from socket and setting the device in socket with VPP=12.50V may cause permanent damage to the device.
- 3. The VPP supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the VPP terminal. When the switching pulse voltage is applied to the VPP terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC574000D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

The integrated dose (ultraviolet light intensity $[w/cm^2] \times exposure$ time [sec.]) for erasure should be a minimum of 15 $[w \cdot sec/cm^2]$.

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of lcm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [μ w/cm²] will reduce the exposure time to about 20 minutes. (In this case, the intergrated dose is 12000[μ w/cm²]×(20×60) [sec.] \approx 15 [$w \cdot sec/cm²$].)

The TC574000D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC902-are available.

OPERATION INFORMATION

The TC574000D's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE	PIN NAMES (NUMBER)	CE (22)	OE (24)	V _{PP} (1)	V _{CC} (32)	D0~D7 (13~15, 17~21)	POWER
Read	Read	L	L			Data Out	Activo
Operation	Output Deselet	*	Н	5∨	5∨	High Impedance	Active
(Ta = 0~70°C)	Standby	н	*]		High Impedance	Standby
Program	Program	L	н			Data In	
Operation	Program Inhibit	н	н	12.50V	6.25V	High Impedance	Active
$(Ta = 25 \pm 5^{\circ}C)$	Program Verify	. *	L			Data Out	

Note: H; VIH, L: VIL, *: VIH or VIL

READ MODE

The TC574000D has two control functions. The chip enable ($\overline{\text{CE}}$) controls the operation power and should be used for device selection. The output enable ($\overline{\text{OE}}$) controls the output buffers, independent of device selection. Assuming that $\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of \overline{OE} .

TC574000D-12, TC574000D-120 TC574000D-150

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TC574000D's can be connected together on a common bus line. When \overline{CE} is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC574000D has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC574000D is placed in the standby mode which reduces the operating current to 100 μ A by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC574000D are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC574000D is in the programming mode when the Vpp input is at 12.50V and $\overline{\text{CE}}$ is at Low under $\overline{\text{OE}} = V_{\text{IH}}$.

The TC574000D can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with \overline{OE} at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.50V) is applied to Vpp terminal, a high level $\overline{\text{CE}}$ and $\overline{\text{OE}}$ input inhibits the TC574000D from being programmed.

Programming of two or more TC574000D's in parallel with different data is easily accomplished. That is, all inputs except for \overline{CE} and \overline{OE} may be commonly connected, and a low level program pulse is applied to the \overline{CE} of the desired device only and high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

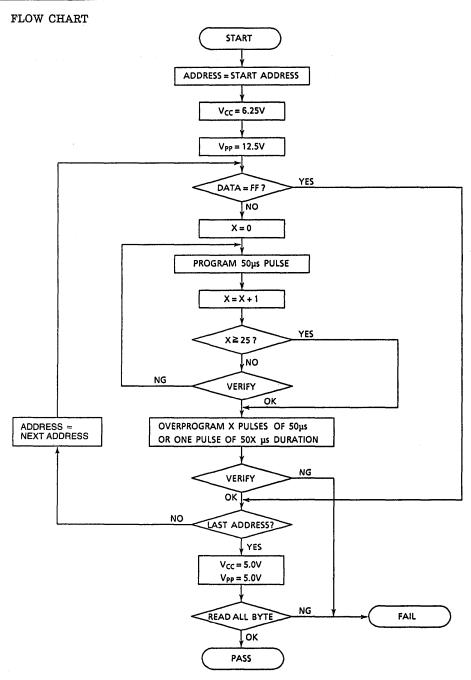
The device is set up in the high speed programming mode when the programming voltage (+12.50V) is applied to the Vpp terminal with $V_{CC}=6.25\text{V}$.

The programming is achieved by applying a single low level 50µs pulse to the $\overline{\text{CE}}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 50µs is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 1 time more than that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

HIGH SPEED PROGRAM MODE



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC574000D which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC574000D by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to $V_{\rm IL}$ in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to $V_{\rm IH}$.

These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC574000D.

PINS	Α0	D7	D6	D5	D4	D3	D2	D1	D0	HEX. DATA
Manufacture Code	ViL	1	0	0	1	1	0	0	0	98
Device Code	V _{IH}	1	0	0	0	1	1	0	0	8C

Notes: $A9 = 12V \pm 0.5V$

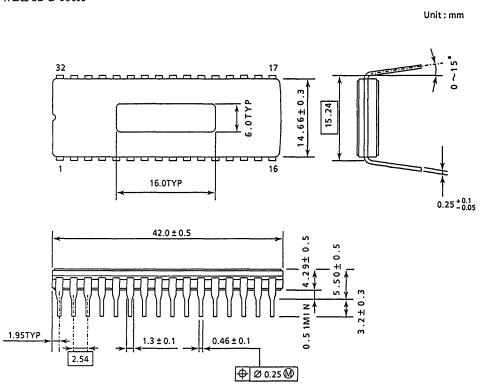
A1~A8, A10~A18, \overline{CE} , $\overline{OE} = V_{IL}$

TC574000D-12, TC574000D-120 TC574000D-150

OUTLINE DRAWINGS

• Cerdip DIP

WDIP32-G-600A



524,288 WORD×8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC574000DI is a 524,288 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC574000DI's access time is 150ns, and the TC574000DI operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the $\overline{\text{CE}}$ input.

Advanced CMOS technology reduces the maximum active current to 50mA/6.7MHz and standby current to 100µA. For program operation, the programming is achieved by using the high speed programming mode. TC574000DI is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

FEATURES

• Peripheral circuit

: CMOS : N-MOS

Memory cell
• Access time

	- 150 - 200			
Vcc	5V ± 10%			
Temp	- 40-	-85°C		
tacc	150ns	200ns		

Low power dissipation

Active: 50mA/6.7MHz Standby: 100µA (Ta=85°C)

- High speed programming operation
- Single 5V power supply
- Full static operation
- Input and output TTL compatible
- JEDEC standard 32 pin
- Standard 32 pin DIP cerdip package

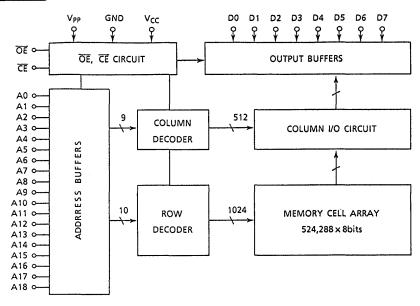
PIN CONNECTION (TOP VIEW)

V _{PP} A16 A15 A12 A7 A6 A5 A4 A3 A2	1 2 3 1 4 5 6 6 7 0 8 9 10	32] 31] 30] 29] 28] 27] 26] 25] 24] 23]	V _{CC} A18 A17 A14 A13 A8 A9 A11 ŌE A10
	3.		
	_1		
A3	Q9	г	ŌĒ
A2	[]10	23	
A1	011	22]	
A0	12	21]	D7
D0	[] 13	20]	D6
D1	[]14	19]	D5
D2	15	18	D4
GND	16	17	D3
_		 	

PIN NAMES

A0~A18	Address Inputs
D0~D7	Outputs (Inputs)
CE	Chip Enable Input
ŌĒ	Output Enable Input
V _{CC}	V _{CC} Supply Voltage
V _{PP}	Program Supply Voltage
GND	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE	CE	ŌĒ	V _{PP}	Vcc	D0~D7	Power
Read	L	L			Data Out	Active
Output Deselect	*	Н	5∨	5V	High Impedance	Active
Standby	Н	*			High Impedance	Standby
Program	L	н			Data In	
Program Inhibit	Н	н	12.50V	6.25V	High Impedance	Active
Program Verify	*	L	1		Data Out	1

^{*:} H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	- 0.6~7.0	V
V _{PP}	Program Supply Voltage	-0.6~14.0	V
V _{IN}	Input Voltage	-0.6~7.0	V
V _{I/O}	input/Output Voltage	-0.6~V _{CC} +0.5	V
PD	Power Dissipation	1.5	w
T _{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T _{strg}	Storage Temperature	- 65~125	°C
Topr	Operating Temperature	- 40~85	°C

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	_	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	-0.3	_	0.8	٧
Vcc	V _{CC} Power Supply Voltage	4.50	5.00	5.50	٧
Vpp	V _{PP} Power Supply Voltage	V _{CC} -0.6	Vcc	V _{CC} + 0.6	٧

DC AND OPERATING CHARACTERISTICS (Ta = -40~85°C)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
ILI	Input Current	V _{IN} = 0~V _{CC}			-	± 10	μА
lcco1	Operating Current	CE = V _{IL}	f = 6.7MHz	-	_	50	mA
I _{CCO2}	Operating Current	I _{OUT} = 0mA	f = 1MHz		_	15	IIIA
I _{CCS1}	Standby Current	CE = V _{IH}		_	_	1	mA
I _{CCS2}	Standby Current	$\overline{CE} = V_{CC} - 0$.2V	-	-	100	μА
Voh	Output High Voltage	I _{OH} = 400μA		2.4	_	_	V
Vol	Output Low Voltage	l _{OL} = 2.1mA		_	_	0.4	٧
Ipp1	V _{PP} Current	$V_{PP} = V_{CC} \pm 0.6V$		_	_	± 10	μА
ILO	Output Leakage Current	V _{OUT} = 0.4V~V _{CC}		_	_	10	μA

AC CHARACTERISTICS ($Ta = -40 \sim 85$ °C, $V_{PP} = V_{CC} \pm 0.6V$)

SIMBOL	PARAMETER	TEST CONDITION	TC574000DI 150		TC57400	UNIT	
31111000	PANAIVIETER	TEST CONDITION	MIN.	MAX.	MIN.	MAX.	UNIT
t _{ACC}	Address Access Time	CE = OE = V _{IL}	-	150	_	200	ns
t _{CE}	CE to Output Valid	OE = V _{IL}	_	150	_	200	ns
toE	OE to Output Valid	CE = V _{IL}	-	70	-	70	ns
t _{DF1}	CE to Output in High-Z	OE = V _{IL}	0	60	0	60	ns
t _{DF2}	OE to Output in High-Z	CE = V _{IL}	0	60	0	60	ns
tон	Output Data Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0	-	0	_	ns

AC TEST CONDITIONS

• Output Load : 1 TTL Gate and C_L=100pF

• Input Pulse Rise and Fall Times : 10ns Max. • Input Pulse Levels : 0.45V~2.4V

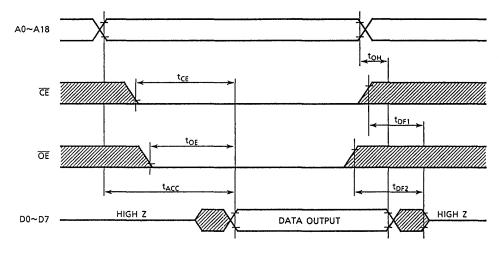
• Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	-	9	PF
C _{OUT}	Output Capacitance	out Capacitance V _{OUT} = 0V		13	rr

^{*} This parameter is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} + 1.0	٧
V _{IL}	Input Low Voltage	- 0.3	-	0.8	V
V _{CC}	V _{CC} Power Supply Voltage	6.00	6.25	6.50	٧
V _{PP}	V _{PP} Power Supply Voltage	12.20	12.50	12.80	V

DC AND OPERATING CHARACTERISTICS (Ta=25 $\pm 5^{\circ}\text{C}, \text{V}_{\text{CC}} = 6.25\text{V} \pm 0.25\text{V}, \text{Vpp} = 12.50\text{V} \pm 0.30\text{V})$

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
lu	Input Current	V _{IN} = 0~V _{CC}	-	-	± 10	μА
V _{OH}	Output High Voltage	I _{OH} = - 400μA	2.4	-	-	٧
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	-	-	0.4	٧
lcc	V _{CC} Supply Current	-	-	-	30	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} = 12.8V	-	-	50	mA
V _{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

AC PROGRAMMING CHARACTERISTICS ($Ta = 25 \pm 5^{\circ}C$, $V_{CC} = 6.25V \pm 0.25V$, $V_{PP} = 12.50V \pm 0.30V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	_	-	μs
t _{AH}	Address Hold Time	-	2	-	-	μs
t _{CES}	CE Setup Time	-	0	_	-	μs
t _{CEH}	CE Hold Time	-	0	-	-	μs
toes	OE Set up Time	-	2		-	μs
t _{DS}	Data Set up Time	-	2	-	-	μs
t _{DH}	Data Hold Time	-	2	-	-	μs
t _{VPS}	V _{PP} Set up Time	-	2	-	_	μs
t _{VCS}	V _{CC} Set up Time	-	2		_	μs
t _{PW}	Program Pulse Width	CE = VIL, OE = VIH	45	50	55	μs
t _{OE}	OE to Output Valid	CE = V _{IH}	-	-	100	ns
t _{DFP}	OE to Output in High-Z	CE = V _{IH}	-	-	90	ns

AC TEST CONDITIONS

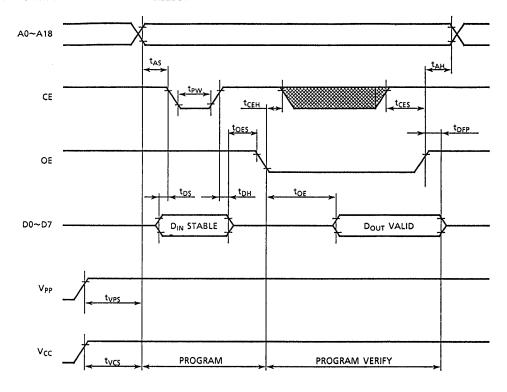
• Output Load : 1 TTL Gate and C_L (100pF)

Input Pulse Rise and Fall Time : 10ns Max.
Input Pulse Levels : 0.45V~2.4V

• Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



Note 1. VCC must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.

- 2. Removing the device from socket and setting the device in socket with VPP=12.50V may cause permanent damage to the device.
- 3. The VPP supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the VPP terminal. When the switching pulse voltage is applied to the VPP terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC574000DI's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

The integrated dose (ultraviolet light intensity $[w/cm^2] \times exposure$ time [sec.]) for erasure should be a minimum of 15 $[w \cdot sec/cm^2]$.

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of lcm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [μ w/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is $1200\varnothing[\mu$ w/cm²]× (20×60) [sec.] \approx 15 [w·sec/cm²].)

The TC574000DI's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended perioded periods of time, the opaque seals-Toshiba EPROM Protect Seal AC902-are available.

OPERATION INFORMATION

The TC574000DI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE	PIN NAMES (NUMBER)	CE (22)	OE (24)	V _{PP} (1)	V _{CC} (32)	D0~D7 (13~15, 17~21)	POWER
Read	Read	L	L			Data Out	Active
Operation	Output Deselet	*	Н	5∨	5V	High Impedance	Active
(Ta = - 40~85°C)	Standby	Н	*			High Impedance	Standby
Program	Program	L	Н			Data In	
Operation	Program Inhibit	Н	Н	12.50V	6.25V	High Impedance	Active
$(Ta = 25 \pm 5^{\circ}C)$	Program Verify	*	L]		Data Out	

Note : H ; V_{IH} , L : V_{IL} , * : V_{IH} or V_{IL}

READ MODE

The TC574000DI has two control functions. The chip enable (\overline{CE}) controls the operation power and should be used for device selection. The output enable (\overline{OE}) control the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The \overline{CE} to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of \overline{OE} .

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more TC574000DI's can be connected together on a common bus line. When \overline{CE} is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC574000DI has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC574000DI is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC574000DI are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC574000DI is in the programming mode when the Vpp input is at 12.50V and \overline{CE} is at Low under $\overline{OE} = V_{IH}$.

The TC574000DI can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with \overline{OE} at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.50V) is applied to Vpp terminal, a high level $\overline{\text{CE}}$ and $\overline{\text{OE}}$ input inhibits the TC574000DI from being programmed.

Programming of two or more TC574000DI's in parallel with different data is easily accomplished. That is, all inputs except for \overline{CE} and \overline{OE} may be commonly connected, and a low level program pulse is applied to the \overline{CE} of the desired device only and high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

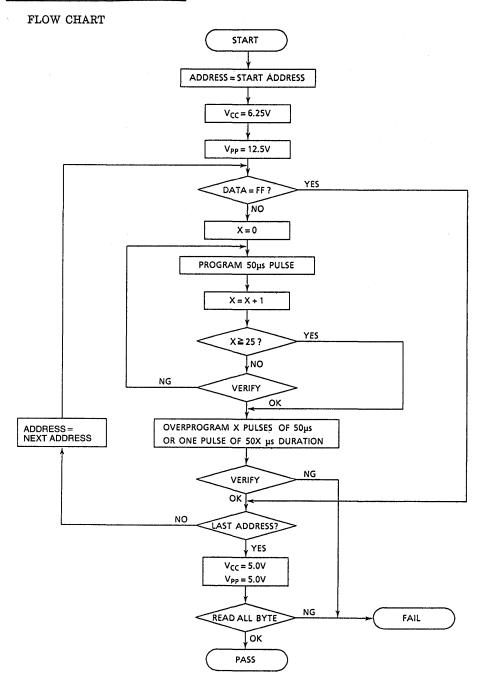
The device is set up is the high speed programming mode when the programming voltage (+12.50V) is applied to the Vpp terminal with $V_{CC}=6.25V$.

The programming is achieved by applying a single low level 50µs pulse to the $\overline{\text{CE}}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of lms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 1 time more than that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC574000DI which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC574000DI by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to $V_{\rm IL}$ in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to $V_{\rm IH}$.

These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC574000DI.

PINS	Α0	D7	D6	D5	D4	D3	D2	D1	D0	HEX. DATA
Manufacture Code	V _{IL}	1	0	0	1	1	0	0	0	98
Device Code	V _{IH}	1	0	0	0	1	1	0	0	8C

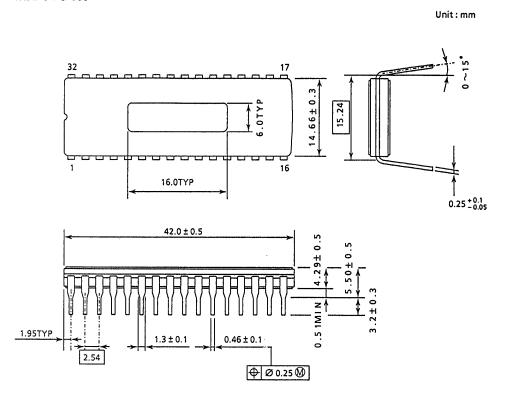
Notes: $A9 = 12V \pm 0.5V$

A1~A8, A0~A18, \overline{CE} , $\overline{OE} = V_{IL}$

OUTLINE DRAWINGS

• Cerdip DIP

WDIP32-G-600



4MEGA BIT (262,144 WORD × 16BIT / 524,288 WORD × 8BIT)
CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

: 100uA

DESCRIPTION

The TC574200D is a 4,194,304 bit CMOS ultraviolet light erasable and electrically programmable read only memory. It is organized as 256K words of 16 bit or 512K words of 8 bit. The TC574200D is compatible with 40 pin 4M bit Mask ROM. This product is packed in 40 pin standard cerdip package. The TC574200D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with access time of 120ns/150ns / 200ns and a maximum operating current of 60mA / 8.3MHz. The programming time of the TC574200D except overhead times of EPROM programmer is only 28 seconds by using the high speed programming algorithm.

FEATURES

Peripheral circuit : CMOS
 Memory cell : NMOS

Fast access time

 $(V_{CC}=5V\pm10\%, Ta=0\sim70^{\circ}C)$

TC574200D - 120 : 120ns

TC574200D - 150 : 150ns TC574200D - 200 : 200ns

Single 5V power supply

Low power dissipation

Standby

Full static operation

Input and output TTL compatible

• Three state output

High speed programming operation: tpw 50µs
 4M MROM compatible pinout: TC534200P

• Standard 40 pin DIP cerdip package

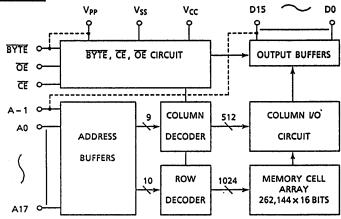
PIN CONNECTION

	(TOP VIEW)	(Reference)	
A17	40 A8 39 A9 38 A10 37 A11 36 A12 35 A13 34 A14 33 A15 32 A16	TOP VIEW) A17 A7 A6 A5 A4 A3 A2 A1 A1 A2 A1 A2 A1 A2 A1 A2 A3 A2 A3 A2 A3 A4 A4 A4 A4 A4 A5 A4 A4 A5 A6 A7 A7 A7 A8 (Reference) 1 40 2 39 3 38 4 37 5 36 6 35 7 34 8 33 9 32	A8 A9 A10 A11 A12 A13 A14 A15 A16	
CE 10 V ₃₅ 11 OE 12 DO 13 D8 14 D1 15 D9 16 D2 17 D10 18 D3 19 D11 20	31 BYTE 30 Vss 29 D15 / 28 D7 27 D14 26 D6 25 D13 24 D5 23 D12 22 D4 21 Vsc	V ₅₅ C A - 1 OE C D8 C D1 C D9 C D10 C D10 C	10 31 11 30 12 29 13 28 14 27 15 26 16 25 17 24 18 23 19 22 20 21	□ BYTE □ Vss □ D15/A-1 □ D7 □ D14 □ D6 □ D13 □ D5 □ D12 □ D4
TC5742000		D11 🗀	20 21 4M Mask ROM TC534200P	J⊒ v _{cc}

PIN NAMES

A0~A17	Address Input
D0~D14	Output (Input)
ČĒ	Chip Enable Input
OE	Output Enable Input
D15/A-1	Output (Input)
D13/A-1	/ Address Input
BYTE / VPP	Word, Byte select Input
DTIE/VPP	/Program Supply Voltage
Vcc	V _{CC} Supply Voltage
Vss	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE	CE	ŌĒ	BYTE /Vpp	Vcc	D0~D7	D8~D14	D15 /A-1	Power		
Read (16 Bit)	٦	L	Н		Dat	a Out				
Read (Lower 8 Bit)	L	L	L		Data Out High Impedance (Lower 8 Bit)		L			
Read (Upper 8 Bit)	L	L	Ļ	Data Out High Impedance 50 (Upper 8 Bit)		. []	Data Out High Impedance		Н	Active
Output Deselect	eselect L H	н.		High Impedance						
Output Deserect		c	L		High Impedance *					
Standby	н		Н		Hig	h Impedance		Canadha		
Standby			L		High Impedance *			Standby		
Program	L	Н			Data In					
Program Inhibit	н	Н	12.5V	6.25V	High Impedance			Active		
Program Verify	*	L			Dat	a Out				

Note: $H = V_{IH}$, $L = V_{IL}$, $\star = V_{IH}$ or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
Vcc	V _{CC} Power Supply Voltage	- 0.6~7.0	v
V _{PP}	Program Supply Voltage	-0.6~14.0	V
V _{IN} Input Voltage		- 0.6~7.0	V
V _{IN} (A9)	Input Voltage (A9)	- 0.6~13.5	v
V _{1/0}	Input/Output Voltage	− 0.6~V _{CC} + 0.5	v
P _D	Power Dissipation	1.5	w
TSOLDER	Soldering Temperature · Time	260-10	°C · sec
T _{STRG}	Storage Temperature	65~150	•c
TOPR	Operating Temperature	0~70	•c

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	- 0.3	-	0.8	v
Vcc	V _{CC} Power Supply Voltage	4.50	5.00	5.50	v

D.C. AND OPERATING CHARACTERISTICS ($Ta = 0 \sim 70^{\circ}C$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ILI	Input Current	V _{IN} = 0V~V _{CC}	-	_	± 10	μА
I _{CCO1}		CE = 0V lout = 0mA f = 8.3MHz	-	_	60	mA
lcco2	Operating Current	CE = 0V I _{OUT} = 0mA f = 1MHz	-	-	30	mA
I _{CCS1}		CE = V _{IH}	-	-	1	mA
I _{CCS2}	Standby Current	CE = V _{CC} - 0.2V	-	-	100	μА
Voн	Output High Voltage	I _{OH} = - 400µA	2.4	-	_	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	-	-	0.4	٧
I _{PP1}	V _{PP} Current	V _{PP} = 0V~V _{CC} + 0.6V	_	_	± 10	μА
ILO	Output Leakage Current	V _{OUT} = 0.4V~V _{CC}	-	-	± 10	μА

A.C. CHARACTERISTICS ($Ta = 0 \sim 70$ °C)

SYMBOL	PARAMETER	_	120	150		- 200		UNIT
3 TIVIBUL	PARAIVIETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNII
t _{ACC}	Address Access Time	-	120	-	150	-	200	ns
t _{CE}	CE to Output Valid	-	120	-	150	-	200	ns
t _{OE}	OE to Output Valid	-	60	-	70	-	70	ns
t _{DF1}	CE to Output in High Impedance	0	50	0	60	0	60	ns
t _{DF2}	OE to Output in High Impedance	0	50	0	60	0	60	ns
t _{OH}	Output Data Hold Time	0	-	0	-	0	-	ns
t _{BT}	BYTE to Output Valid	_	120	-	150	-	200	ns
t _{BTD}	BYTE to Output in High Impedance	_	50	-	60		60	ns

· A.C. TEST CONDITIONS

· Output Load : 1 TTL Gate and CL = 100PF

Input Pulse Rise and Fall Time : 10ns Max
 Input Pulse Levels : 0.45V and 2.4V

• Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

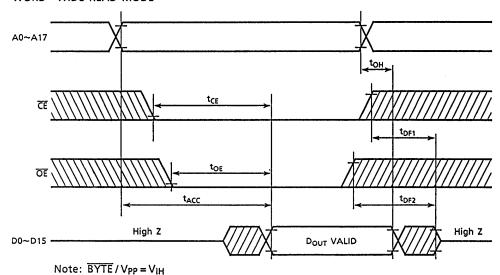
CAPACITANCE * (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CINI	Input Capacitance	V _{IN} = 0V	-	6	10	pF
C _{IN2}	Input Capacitance (BYTE/V _{PP})	V _{IN} = 0V	-	50	60	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	-	10	12	PF

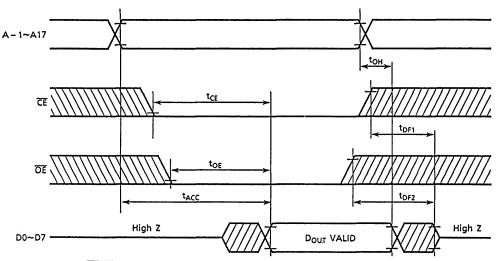
^{*} This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS

WORD - WIDE READ MODE



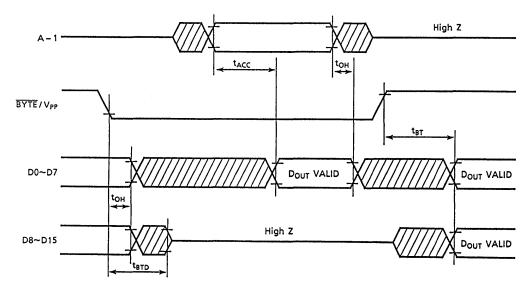




Note: $\overline{BYTE}/V_{PP} = V_{IL}$

BYTE TRANSITION

A0~A17



Note: \overline{CE} , $\overline{OE} = V_{IL}$

HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	V _{CC} + 1.0	٧
V _{IL}	Input Low Voltage	- 0.3	-	0.8	>
Vcc	V _{CC} Power Supply Voltage	6.00	6.25	6.50	٧
V _{PP}	V _{PP} Power Supply Voltage	12.20	12.50	12.80	V

D.C. AND OPERATING CHARACTERISTICS ($Ta = 25 \pm 5^{\circ}C$, $V_{CC} = 6.25 \pm 0.25V$, $V_{PP} = 12.50 \pm 0.30V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
1 _{LI}	Input Current	V _{IN} = 0V~V _{CC}	-	-	± 10	μА
VoH	Output High Voltage	I _{OH} = - 400μA	2.4	-	-	V
VoL	Output Low Voltage	I _{OL} = 2.1mA	-	-	0.4	V
lcc	V _{CC} Supply Current	-	-	-	40	mA
lpp2	V _{PP} Supply Current	V _{PP} = 12.8V	-	-	100	mA

A.C. PROGRAMMING CHARACTERISTICS ($Ta = 25 \pm 5^{\circ}C$, $V_{CC} = 6.25 \pm 0.25V$, $V_{PP} = 12.50 \pm 0.30V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tas	Address Setup Time	-	2	_	-	μs
t _{AH}	Address Hold Time	-	2	-	_	μs
t _{CES}	CE Setup Time	-	0	-	-	μs
t _{CEH}	CE Hold Time	-	0	-	-	μs
toes	OE Setup Time	-	2	-	_	μs
t _{D\$}	Data Setup Time	-	2	-	-	μs
t _{DH}	Data Hold Time	-	2	-	-	μs
t _{VPS}	V _{PP} Setup Time	-	2	-	-	μs
t _{VCS}	V _{CC} Setup Time	-	2	-	-	μs
t _{PW}	Program Pulse Width	-	45	50	55	μs
t _{OPW}	Overprogram Pulse Width	Note 1	45	50	55	μs
t _{OE}	OE to Output Valid	CE = VIH	-	-	100	ns
t _{DFP}	OE to Output in High Impedance	CE = V _{IH}	-	-	90	ns

· A.C. TEST CONDITIONS

· Output Load

: 1 TTL Gate and CL = 100PF

· Input Pulse Rise and Fall Time

: 10ns Max

· Input Pulse Levels

: 0.45V and 2.4V

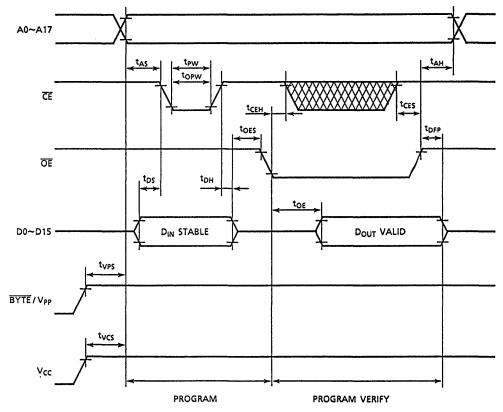
· Timing Measurement Reference Level

: Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: topw depends on the program pulse width which is required in the initial program.

TIMING WAVEFORMS

HIGH SPEED PROGRAM OPERATION



- Note: 1. VCC must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.
 - 2. Removing the device from socket and setting the device in socket with $V_{\rm PP} = 12.50 V$ may cause permanent damage to the device.
 - 3. The Vpp supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the Vpp terminal. When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC574200D-120, TC574200D-150 TC574200D-200

ERASURE CHARACTERISTICS

The TC574200D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. The integrated dose (ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W·sec/cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a $12000 \, [\mu W/cm^2]$ will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is $12000 \, [\mu W/cm^2] \times (20 \times 60) \, [sec] = 15 \, [W\cdot sec/cm^2]$.)

The TC574200D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals—Toshiba EPROM Protect Seal AC902—are available.

OPERATION INFORMATION

The TC574200D's eight operation mode are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE	CE	ŌĒ	BYTE /Vpp	Vcc	D0~D7	D8~D14	D15 /A-1	Power		
Read (16 Bit)	L	L	Н		Data Out					
Read (Lower 8 Bit)	L	L	L		Data Out (Lower 8 Bit)	High Impedance	L			
Read (Upper 8 Bit)	L	L	L	5V	Data Out (Upper 8 Bit)	High Impedance	Н	Active		
Output Deselect		н	Н		Hig	h Impedance				
Output Deselect	_	П	٦		Hig	h Impedance	*			
Standby	ndby H *		1,, 1		н		High Impedance			Canadha
			L		Hig	*	Standby			
Program	L	н			Dat	ta In				
Program Inhibit	Н	Н	12.5V	6.25V	High Impedance			Active		
Program Verify	*	L			Data Out					

Note: $H = V_{IH}$, $L = V_{IL}$, $\star = V_{IH}$ or V_{IL}

READ MODE

The TC574200D has the \overline{BYTE}/V_{PP} terminal that selects word-wide output and byte-wide output. When \overline{BYTE}/V_{PP} is set to V_{IH} , the word-wide output is selected, and D15/A-1 pin is used for D15 data output.

When $\overline{\text{BYTE}}/\text{Vpp}$ is set to V_{IL} , the byte-wide output is selected, and D15/A-1 pin is used for A-1 address input. When A-1 is set to V_{IL} in this condition, the data output is selected lower 8 bits of the 16 bit data which has been programmed. When A-1 is set to V_{IH} , the data output is selected upper 8 bits.

The TC574200D has two control function. The chip enable (\overline{CE}) controls the operation power and should be used for device selection. The output enable (\overline{OE}) controls the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The \overline{CE} to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{CE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of \overline{OE} .

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more TC574200D's can be connected together on a common bus line. When \overline{CE} is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC574200D has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC574200D is placed in the standby mode which reduces the operating current to 100 μ A by applying MOS-high level (VCC) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

TC574200D-120, TC574200D-150 TC574200D-200

PROGRAM MODE

Initially, when recieved by customers, all bits of the TC574200D are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit location by electrically programming. The TC574200D is in the programming mode when the Vpp input is at 12.50V and \overline{CE} is at TTL-Low under \overline{OE} =V_{IH}. Data to be programmed must be applied 16 bits in parallel to the data pins.

The TC574200D can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with \overline{OE} at V_{IL} . The programmed data should be compared with the original word-wide (16 bit) data.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (12.50V) is applied to Vpp terminal, a high level $\overline{\text{CE}}$ input inhibits the TC574200D from being programmed. Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{\text{CE}}$ and $\overline{\text{OE}}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{\text{CE}}$ of the desired device only and TTL high level signal is applied to the other devices.

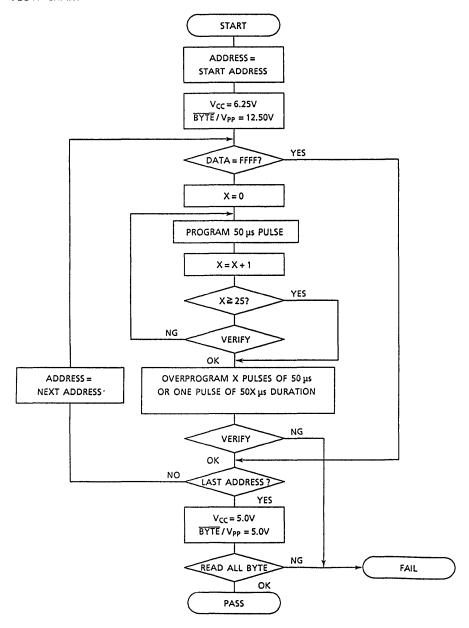
HIGH SPEED PROGRAM MODE

The device is set up the high speed programming mode when the programming voltage (12.50V) is applied to the Vpp terminal with V_{CC}=6.25V. The programming is achieved by applying a single TTL low level 50µs pulse to the $\overline{\text{CE}}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 50µs is applied and then the programmed data is verified. This should be repeated until the program operates correctly(max. 25 times).

After correctly programming the selected address, the overprogram pulse of same length that needed for initial programming should be applied. When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



TC574200D-120, TC574200D-150 TC574200D-200

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC574200D which identifies its manufacturer and device type. The programming equipment may read out manufacturer code and device code from TC574200D by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC574200D.

PINS	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX DATA
Manufacturer Code	VIL	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	VIH	*	*	*	*	*	*	*	*	1	0	0	0	1	1	1	1	**8F

Note: A1 - A8, A10 - A17, CE, OE = VIL

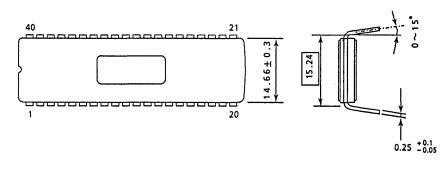
BYTE / VPP = V_{IH}
* Don't care

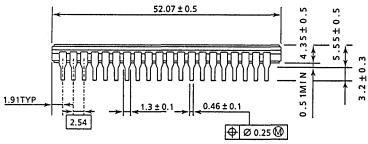
D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{CC}	V _{CC} Power Supply Voltage	4.50	5.00	5.50	٧
V _{ID}	A9 Auto Select Voltage	11.50	12.00	12.50	٧

OUTLINE DRAWINGS

Unit in mm





				· -
				-

,			

32,768 WORD x 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC57H256D is a 32,768 word x 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57H256D's access time is 70ns, and the TC57H256D operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{\text{CE}}$ input. Advanced CMOS technology reduces the maximum active current to 50mA/14.2MHz and standby current to $100\mu\text{A}$. For program operation, the programming is achieved by using the high speed programming mode. For program operation, the programming is achieved by using high speed programming mode. TC57H256D is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

FEATURES

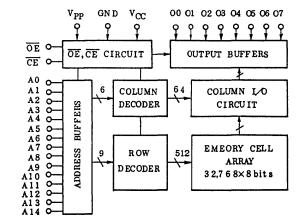
- Peripheral circuit: CMOS
- Memory cell : N-MOS

	-70	-85
V _{CC}	5V±5%	5V±10%
tACC	70ns	85ns

· Single 5V power supply

- · Full static operation
- · High speed programming mode
- · Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, TMM27256AD and TC57256AD
- · Standard 28 pin DIP cerdip package

BLOCK DIAGRAM



PIN CONNECTION (TOP VIEW)

V _{PP}	1	28	⊨ v _{DD}
A12	2	27	□ A14
A7 🗆	3	26	DA13
A6 🗆	4	25	DA8
A5 🗆	5	24	D A9
A4 🗆	6	23	DAll
A3 🗆	7	22	DOE
A2 🗆	8	21	DA10
A1 🗆	9	20	DCE
A0 🗆	10	19	07
00 🗖	11	18	D 06
01 🗖	12	17	D 05
O2 🗆	13	16	□ 04
GND	14	15	роз

PIN NAMES

A0 ~ A14	Address Inputs
00 ∿ 07	Outputs (Inputs)
CE	Chip Enable Input
ŌĒ	Output Enable Input
Vpp	Program Supply Voltage
vcc	V _{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE	ČE (20)	ÖE (22)	VPP (1)	V _C C (28)	00 ∿ 07 (11∿13, 15∿19)	POWER		
Read	L	L			Data Out	A - 4-2		
Output Deselect	*	Н	5V	5V	High Impedance	Active		
Standby	H	*			High Impedance	Standby		
Program	L	H	125V ¹⁾	6 V	Data In			
Program Inhibit	Н	Н	2)	2)	High Impedance	Active		
Program Verify	*	L	12.75 V	6.25V	Data Out			
* H or L 1): H								

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
v _{CC}	VCC Power Supply Voltage	-0.6 ~ 7.0	V
V _{PP}	Program Supply Voltage	-0.6 ∿14.0	V
VIN	Input Voltage	-0.6 ~ 7.0	v
V _I /0	Input/Output Voltage	-0.6 ~ V _{CC} +0.5	V
PD	Power Dissipation	1.5	W
TSOLDER	Soldering Temperature Time	260 - 10	°C · sec
tSTG	Storage Temperature	-65 ~125	°C
tOPR	Operating Temperature	0 ~70	°C

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57H256D-70	TC57H256D-85
Ta	Operating Temperature	0 ∿ 70°C	0 ∿ 70°C
VCC	V _{CC} Power Supply Voltage	5V±5%	5V±10%
V _{PP}	Vpp Power Supply Voltage	V _{CC} -0.6V ~ V _{CC} +0.6V	V _{CC} -0.6V ~ V _{CC} +0.6V

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDI	TION	NIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0 ~VCC	;	-	-	±10	μA
ILO	Output Leakage Current	V _{OUT} =0.4 ∿	V _{CC}	-	-	±10	μА
I _{CC01}	0	Œ=0V	f=14.2MHz	-	-	50	
I _{CCO2}	Operating Current	02-01	f=1MHz	1	-	20	mA
I _{CCS1}	Standby Current	CE=VIH	-	-	1	mA	
I _{CCS2}	Standby Current	CE=V _{CC} -0.2	:v	-	-	100	μА
v_{IH}	Input High Voltage	-		2.2	-	V _{CC} +0.3	v
VIL	Output Low Voltage	-		-0.3	-	0.8	V
v _{oh}	Output High Voltage	I _{OH} =0400μA		2.4	-	-	V
VOL	Output Low Voltage	I _{OL} =2.1mA		-	-	0.4	v
I _{PP1}	Vpp Current	V _{PP} =V _{CC} -0.	6 ~ V _{CC} +0.6	-	-	±10	μA

A.C. CHARACTERISTICS

arninor.	DAD AMERICA	meam compressor	TC57H256D-70		TC57H2	256D-85	UNIT
SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	MIN.	MAX.	ONLI
tACC	Address Access Time	CE=OE=V _{IL}	-	70	-	85	ns
tCE	CE to Output Valid	OE=V _{IL}	-	70	-	85	ns
tOE	OE to Output Valid	CE=V _{IL}	-	40	-	45	ns
t _{DF1}	CE to Output in High-Z	OE=V _{IL}	0	30	0	30	ns
t _{DF2}	OE to Output in High-Z	CE=VIL	0	30	0	30	ns
tOH	Output Data Hold Time	CE=OE=VIL	5	-	5	-	ns

A.C. TEST CONDITIONS

· Output Load

: 1 TTL Gate and C_L =100pF

 $\boldsymbol{\cdot}$ Input Pulse Rise and Fall Times

: 10ns Max.

· Input Pulse Levels

: 0.45V ~ 2.4V

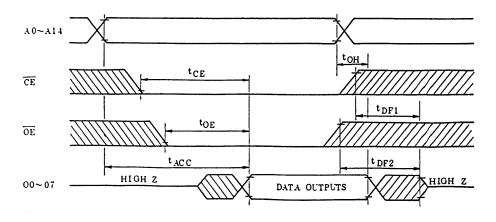
• Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CIN	Input Capacitance	Λ ^{IN} =0Λ	-	4	6	pF
COUT	Qutput Capacitance	V _{OUT} =0V	-	8	12	pF

st This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



HIGH SPEED PROGRAM MODE I

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	_	V _{CC} +1.0	v
VIL	Input Low Voltage	-0.3	-	0.8	V
vcc	V _{CC} Power Supply Voltage	5.75	6.0	6, 25	v
V _{PP}	Vpp Power Supply Voltage	12.0	12.5	13.0	V

D.C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ILI	Input Current	V _{IN} =0 ∿V _{CC}	-	-	±10	μA
v _{OH}	Output High Voltage	I _{OH} =400μA	2.4	-	-	V
VOL	Output Low Voltage	I _{OL} =2.1mA	_	-	0.4	V
ICC	VCC Supply Current	-	_	-	40	mA
I _{PP2}	Vpp Supply Current	V _{PP} =13.0V	_	-	50	πA

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP	MAX.	UNIT
tAS	Address Setup Time	-	2	-	-	μs
tAH	Address Hold Time	-	2	_	-	μs
^t CES	CE Setup Time	-	0	-	-	μs
t CEH	CE Hold Time	-	0	-	-	μs
tOES	OE Setup Time	-	2	-	: -	μs
t _{DS}	Date Setup Time	-	2	_	-	μs
t _{DH}	Data Hold Time	_	2	-	-	μs
tVPS	V _{PP} Setup Time	_	2	-	-	μs
tVCS	V _{CC} Setup Time	-	2	-	-	μs
t _{PW}	Initial Program Pulse Width	CE=V _{IL} , OE=V _{IH}	0.95	1	1.05	ms
tOPW	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t _{OE}	OE to Output Valid	CE=VIH	-	-	100	ns
tDFP	OE to Output in High-Z	CE=VIH	-	-	90	ns

A.C. TEST CONDITIONS

• Output Load : 1 TTL Gate and CL(100pF)

• Input Pulse Rise and Fall Times : 10ns Max. • Input Pulse Levels : $0.45 \text{V} \sim 2.4 \text{V}$

· Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

HIGH SPEED PROGRAM OPERATION II

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	V _{CC} +1.0	V
VIL	Input Low Voltage	-0.3	_	0.8	v
v _{CC}	V _{CC} Power Supply Voltage	6.00	6.25	6.50	V
V _{PP}	Vpp Power Supply Voltage	12.50	12.75	13.00	v

D.C. AND OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ILI	Input Current	$V_{IN}=0 \sim V_{CC}$	_	-	±10	μA
v _{OH}	Output High Voltage	I _{OH} =-400μA	2.4	-	-	v
V _{OL}	Output Low Voltage	I _{OL} =2.1mA	-	-	0.4	V
ICC	VCC Supply Current	-	-	-	40	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} =13.0V	_	_	50	mA

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	-	_	μs
t _{AH}	Address Hold Time	-	2	_	_	μs
tCES	CE Setup Time	-	0	-	_	ns
^t CEH	CE Hold Time	-	0	-	_	ns
t _{DS}	Data Setup Time	-	2	-	_	μS
t _{DH}	Data Hold Time	-	2	-	-	μs
tVPS	V _{PP} Setup Time	-	2	-	-	μs
t _{VCS}	V _{CC} Setup Time	-	2	-	-	μs
tPW	Program Pulse Width	CE=VIL, OE=VIH	0.095	0.1	0.105	ms
^t OE	OE to Output Valid	CE=VIH	/-	-	100	ns
t _{DFP}	OE to Output in High-Z	CE=VIH	-	-	90	ns

A.C. TEST CONDITIONS

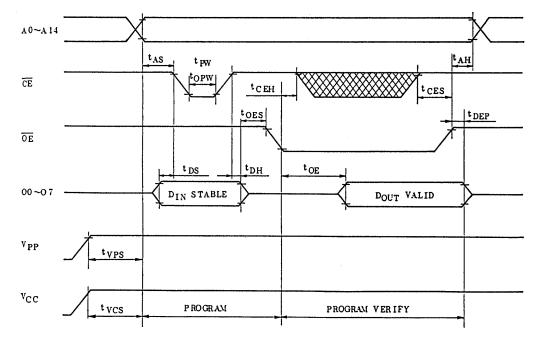
• Output Load : 1 TTL Gate and $C_L(100pF)$

Input Pulse Rise and Fall Time : 10ns Max.
Input Pulse Levels : 0.45V to 2.4V

• Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM MODE I ($v_{CC}=6v\pm0.25v$, $v_{PP}=12.5v\pm0.5v$) HIGH SPEED PROGRAM MODE II ($v_{CC}=6.25v\pm0.25v$, $v_{PP}=12.5v\pm0.5v$)



- Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
 - 2. Removing the device from socket and setting the device in socket with $V_{\rm PP}$ =12.5V(12.75V) may cause permanent damage to the device.
 - 3. The V_{pp} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{pp} terminal. When the switching pulse voltage is applied to the V_{pp} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57H256D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

The integrated dose (ultraviolet light intensity $[w/cm^2]$ 4×1 exposure time [sec.]) for erasure should be a minimum of 15 $[w\cdot sec/cm^2]$.

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μ w/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [μ w/cm²] × (20 × 60) [sec] \cong 15 [ω ·sec/cm²].)

The TC57H256D's erasure begins to occur when exposed to light with wavelength shorter than 4000\AA . The sunlight and the fluorescent lamps will include $3000 \sim 4000\text{\AA}$ wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC57H256D's six operation modes are listed in the following table. Mode selection can be achived by applying TTL level signal to all inputs.

MODE	'IN NAMES (NUMBER)	Œ (20)	OE (22)	V _{PP} (1)	V _{CC} (28)		00 ~07 √13, 15 ~19)	POWER
Read Operation	Read	L	L			Data	Out	A = # d = 1
(Ta=0 ∿ 70°C)	Output Deselect	*	н	5v	5v	High	Impedance	Active
	Standby	н	*] [High	Impedance	Standby
D	Program	L	Н	1)		Data	In	
Program Operation (Ta=25±5°C)	Program Inhibit	Н	Н	12.50	6V 2)	High	Impedance	Active
(14 2323 0)	Program Verify	*	L	12.75V		Data	Out	

Note: H; V_{IH} ; L; V_{IL} ; *; V_{IH} or V_{IL} ,

1): HIGH SPEED PROGRAM MODE I, 2): HIGH SPEED PROGRAM MODE II

READ MODE

The TC57H256D has two control functions. The chip enable $(\overline{\text{CE}})$ controls the operation power and should be used for device selection.

The output enable (\overline{OE}) control the output buffers, independent of device selection. Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{\text{CE}}=V_{\text{IL}}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}}=\text{V}_{\text{IH}}$ or $\overline{\text{OE}}=\text{V}_{\text{IH}}$, the outputs will be in a high impedance state. So two or more TC57H256D's can be connected together on a common bus line. When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

TC57H256D-70 TC57H256D-85

STANDBY MODE

The TC57H256D has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC57H256D is placed in the standby mode which reduce the operating current to 100µA by applying MOS-high level (VCC) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57H256D are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The TC57H256D is in the programming mode when the Vpp input is at 12.5V and $\overline{\text{CE}}$ is at TTL-Low under $\overline{\text{OE}}$ =VIH.

The TC57H256D can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with \overline{OE} at V_{TI} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage ($\pm 12.5V$ or $\pm 12.75V$) is applied to Vpp terminal, a high level \overline{CE} input inhibits the TC57H256D from being programmed. Programming of two or more TC57H256D's in parallel with different data is easily accomplished. That is, all inputs except for \overline{CE} and \overline{OE} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE I

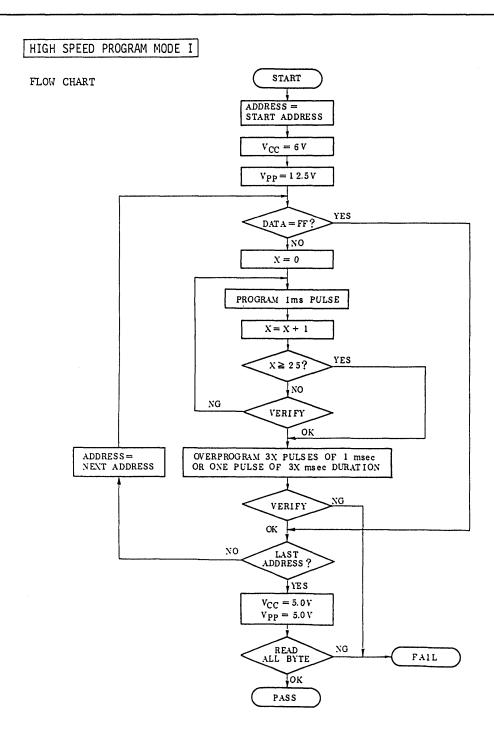
The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming

voltage (+12.5V) is applied to the V_{pp} terminal with $V_{CC}=6V$.

The programming is achieved by applying a single TTL low level lms pulse to the CE input after addresses and data are stable. Then the programmed data is verified by using Progam Verify Mode.

If the programmed data is not correct, another program pulse of lms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied. When programming has been completed, the data in all addresses should be verified with $V_{\rm CC}=V_{\rm PP}=5V$.



TC57H256D-70 TC57H256D-85

HIGH SPEED PROGRAM MODE II

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the $V_{\rm PP}$ terminal with $V_{\rm CC}$ =6.25V.

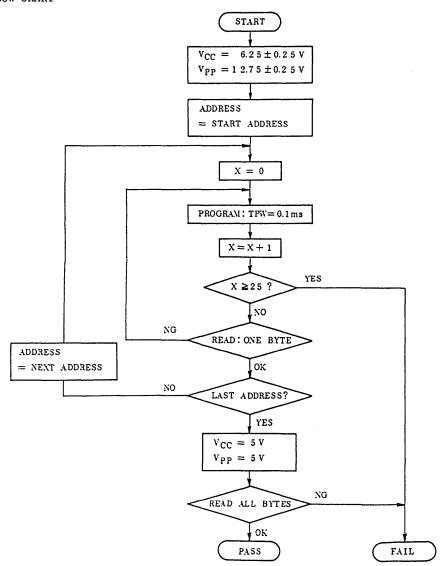
The programming is achieved by applying a single TTL low level 0.1ms pulse the CE input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{\rm CC} = V_{\rm PP} = 5V$.

HIGH SPEED PROGRAM MODE II

FLOW CHART



TC57H256D-70 TC57H256D-85

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57H256D which identifies its manufacturer and device type.

The programming equipment may read out manufacturer coce and device code from TC57H256D by using this mode before program operation and automatically set program voltage ($V_{\rm PP}$) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to $V_{\rm IL}$ in read operation. Data output in this con-

dition is manufacturer code. Device code is identified when address AO is set to V_{IH} . These two codes possess an odd parity with the parity bit of MSB (O7). The following table shows electric signature of TC57H256D.

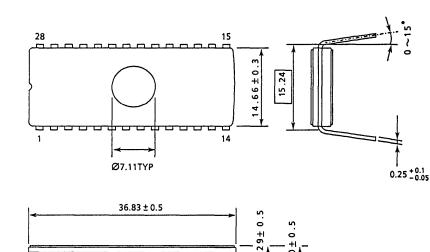
PINS	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacture Code	VIL	1	0	0	1	1	0	0	0	98
Device Code	VIH	0	1	0	0	0	1	0	1	45

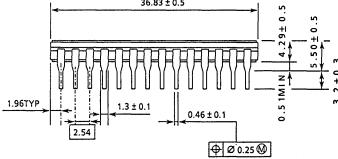
Notes: $A9=12V\pm0.5V$

Al \sim A8, AlO \sim A14, $\overline{\text{CE}}$, $\overline{\text{OE}}$ =V_{IL}

OUTLINE DRAWINGS WDIP28-G-600A

Unit: mm





	4		
•			
			-

131,072 WORD × 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC57H1000AD/TC57H1001AD is a 131,072 word \times 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory.

The TC57H1000AD is JEDEC standard pin configuration and the TC57H1001AD is compatible with 28 pin 1M bit Mask ROM. Both products are packed in 32 pin standard cerdip package.

The TC57H1000AD/TC57H1001AD is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 40mA/11.8MHz and access time of 85ns/100ns.

The programming times of the TC57H1000AD / TC57H1001AD except overhead times of EPROM programmer is only 14 seconds by using the high speed programming algoritim.

FEATURES

• Peripheral circuit

: CMOS

Memory cell

: N-MOS

• Access time

	- 85	- 100					
t _{ACC}	85ns	100ns					
Vcc	5V ±	10%					

• Low power dissipation

Active: 40mA/11.8MHzStandby: $100\mu\text{A}$ (Ta = 70°C) Wide operating temperature range: 0~70°C

• Single 5V power supply

• Full static operation

• High speed programming operation: tpw 0.1ms

Input and output TTL compatible

JEDEC standard 32 pin : TC57H1000AD
1M MROM compatible : TC57H1001AD

• Standard 32 pin DIP cerdip package

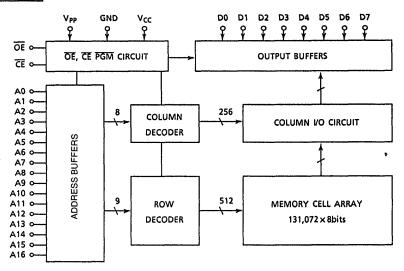
PIN CONNECTION (TOP VIEW)

		\neg		ſ		٠		1					
V _{PP} [1 1	32 V _{CC}	V_{PP}		1		32	þνcc			(Ref	erence	?)
A16 [2	31) PGM	ŌĒ	þ	2		31) PGM					l
A15 [3	30) NC	A15	þ	3		30	Jис	A15		1	28] V _{CC}
A12 [4	29] A14	A12	d	4		29	DA14	A12		2	27	DA14
A7 (5	28] A13	Α7	d	5		28	1A13	Α7	ζ	3	26	A13
A6 [6	27] A8	A6	q	6		27	18A	A6		4	25] A8
A5 [7	26] A9	A5	Д	7		26	A9	A5		5	24	A9
A4 [8	25] A11	A4	р	8		25	A11	A4		6	23]A11
A3 [9	24] OE	А3	d	9		24	A16	A3		7	22	A16
A2 [10	23] A10	A2	П	10		23	A10	A2	C	8	21]A10
A1 [11	22) CE	A1	d	11		22	CĒ	A1		9	20) CE
A0 [12	2107	A0	Д	12		21	D7	A0		10	19	D7
D0 [13	20] D6	D0	d	13		20	D6	D0		11	18] D6
D1 [14	19] D5	D1	d	14		19	D5	D1	С	12	17] D5
D2 [15	18] D4	D2	q	15		18	D4	D2	þ	13	16] D4
GND [16	17] D3	GND	þ	16		17	D3	GND	q	.14	15] D3
TC57H1000AD			TC57H1001AD							(1M Mask ROM)			

PIN NAMES

A0~A16	Address Inputs						
D0~D7	Outputs (inputs)						
CĒ	Chip Enable Input						
ŌĒ	Output Enable Input						
PGM	Program Control Input						
Vcc	V _{CC} Supply Voltage						
V _{PP}	Program Supply Voltage						
GND	Ground						
NC	No Connection						

BLOCK DIAGRAM



MODE SELECTION

MODE	PGM	CE	ŌĒ	Vpp	Vcc	D0~D7	Power	
Read	Н	L	L			Data Out	A -41	
Output Deselect	•	*	н	5V	5V	High Impedance	Active	
Standby	*	н	*			High Impedance	Standby	
Program	L	L	н			Data In	Active	
D	*	н	*	42.751	6.0514	High Impedance		
Program Inhibit	Н	L	н	12.75V	6.25V	High Impedance		
Program Verify	н	L	L			Data Out	7	

^{* :} H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT			
Vcc	V _{CC} Power Supply Voltage	-0.6~7.0				
Vpp	Program Supply Voltage	-0.6~14.0 V				
VIN	Input Voltage	-0.6~7.0 V				
V _{I/O}	Input/Output Voltage	-0.6~V _{CC} +0.5	V			
PD	Power Dissipation	1.5	w			
TSOLDER	Soldering Temperature Time	260 · 10	°C · sec			
TSTRG	Storage Temperature	- 65~125				
TOPR	Operating Temperature	0~70	°C			

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

	0.0.445770	TC57H1000AD / 10	UNIT	
SYMBOL	PARAMETER	MIN.	MAX.	UNII
ViH	Input High Voltage	2.2	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	- 0.3	0.8	٧
Vcc	V _{CC} Power Supply Voltage	4.50	5.50	V
V _{PP}	V _{PP} Power Supply Voltage	V _{CC} - 0.6	V _{CC} + 0.6	V

DC AND OPERATING CHARACTERISTICS (Ta=0~70°C)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} = 0~V _{CC}		_	-	± 10	μА
lcco1	Otion Comment	CE = OV	f = 11.8MHz	_	-	40	mA
lcco2	Operating Current	I _{OUT} = 0mA	f = 1MHz		-	15	l IIIA
lccs1	Standby Current	CE = VIH		_	_	1	mA
I _{CCS2}	Standby Current	<u>CE</u> = V _{CC} − 0	.2V	_	_	100	μА
VoH	Output High Voltage	I _{OH} = - 400 ₁	μΑ	2.4	_	- ,	٧
Vol	Output Low Voltage	I _{OL} = 2.1mA		-	-	0.4	٧
l _{PP1}	V _{PP} Current	V _{PP} = V _{CC} ± 0.6V		-	_	± 10	μΑ
ILO	Output Leakage Current	V _{OUT} = 0.4V~V _{CC}			_	10	μΑ

AC CHARACTERISTICS ($Ta=0\sim70^{\circ}C$, $V_{PP}=V_{CC}\pm0.6V$)

CINADOL	DADAMETER	TC57H1000AI	D/ 1001AD - 85	TC57H1000AD	/1001AD-100	UNIT
SIMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	וואט
t _{ACC}	Address Access Time	-	85	-	100	ns
t _{CE}	CE to Output Valid	-	85	-	100	ns
t _{OE}	OE to Output Valid	-	45	-	50	ns
t _{PGM}	PGM to Output Valid	-	45	_	50	ns
t _{DF1}	CE to Output in High-Z	0	30	0	40	ns
t _{DF2}	OE to Output in High-Z	0	30	0	40	ns
t _{DF3}	PGM to Output in High-Z	0	30	0	40	ns
t _{OH}	Output Data Hold Time	0		0	-	ns

AC TEST CONDITIONS

• Output Load : 1 TTL Gate and C_L=100pF

Input Pulse Rise and Fall Times : 10ns Max.
 Input Pulse Levels : 0.45V~2.4V

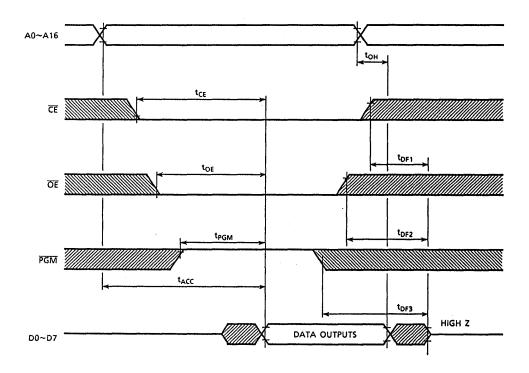
• Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	-	4	9	D.
C _{OUT}	Output Capacitance	V _{OUT} = 0V	-	10	12	r.

^{*}This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} + 1.0	٧
V _{IL}	input Low Voltage	- 0.3	-	0.8	٧
Vcc	V _{CC} V _{CC} Power Supply Voltage		6.25	6.50	٧
V _{PP}	V _{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC AND OPERATING CHARACTERISTICS ($Ta = 25 \pm 5^{\circ}C$, $V_{CC} = 6.25V \pm 0.25V$, $V_{PP} = 12.75V \pm 0.25V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
l _{Ll}	Input Current	V _{IN} = 0~V _{CC}	-	~	± 10	μΑ
V _{OH}	Output High Voltage	I _{OH} = - 400μA	2.4	-	-	>
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	-	-	0.4	>
Icc	V _{CC} Supply Current	-	-	-	30	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} = 13.0V	-	-	50	mA

AC PROGRAMMING CHARACTERISTICS ($Ta = 25 \pm 5^{\circ}C$, $V_{CC} = 6.25V \pm 0.25V$, $V_{PP} = 12.75V \pm 0.25V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	-	-	μς
t _{AH}	Address Hold Time		2	-	-	μs
t _{CES}	CE Setup Time	-	2	-	_	μς
t _{CEH}	CE Hold Time	-	2	-	-	μs
t _{DS}	Data Set up Time	-	2	-	-	μς
t _{DH}	Data Hold Time	-	2	•	-	μς
t _{VS}	V _{PP} Set up Time	-	2	-	-	μs
tpW	Program Pulse Width	-	0.095	0.1	0.105	ms
t _{OE}	OE to Output Valid	-	-	-	100	ns
t _{DF2}	OE to Output in High-Z	<u>CE</u> = VII	-	-	90	ns

AC TEST CONDITIONS

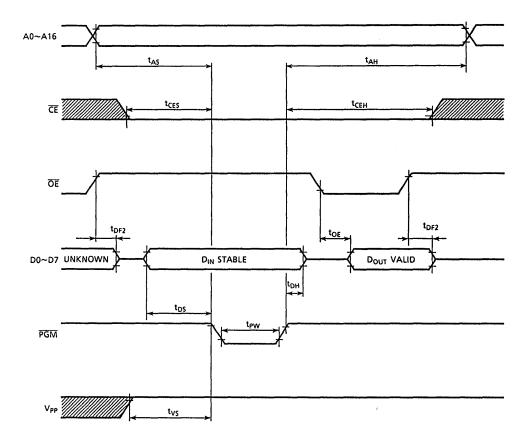
• Output Load : 1 TTL Gate and C_L (100pF)

Input Pulse Rise and Fall Time : 10ns Max.
 Input Pulse Levels : 0.45V~2.4V

• Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .

- 2. Removing the device from socket and setting the device in socket with VPP=12.75V may cause permanent damage to the device.
- 3. The Vpp supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the Vpp terminal. When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57H1000AD / TC57H1001AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

The integrated dose (ultraviolet light intensity $[w/cm^2] \times exposure$ time [sec.]) for erasure should be a minimum of 15 $[w \cdot sec/cm^2]$.

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of lcm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [μ w/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000[μ w/cm²]× (20×60) [sec.] \approx 15 [ν sec/cm²].)

The TC57H1000AD / TC57H1001AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC57H1000AD/TC57H1001AD's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE	PIN	PGM	CE	ŌĒ	V _{PP}	V _{CC}	D0~D7	POWER	
Read	Read	н	L	L			Data Out	Active	
Operation	Output Deselet	*	*	Н	5∨	5∨	High Impedance		
$(Ta = 0 \sim 70^{\circ}C)$	Standby	*	Н	*]		High Impedance	Standby	
Program	Program	L	L	н			Data In	Active	
Operation	Program Inhibit	*	Н	*	12.75V	6.25V	High Impedance		
(Ta = 25 ± 5°C)		н	L	Н	12.75	6.25V	High Impedance		
	Program Verify	Н	L	L	1 [Data Out		

Note: H; VIH, L: VIL, *: VIH or VIL

READ MODE

The TC57H1000AD/TC57H1001AD has three control functions. The chip enable $(\overline{\text{CE}})$ controls the operation power and should be used for device selection. The output enable $(\overline{\text{OE}})$ and the program control $(\overline{\text{PGM}})$ control the output buffers independent of device selection.

Assuming in that $\overline{CE} = \overline{OE} = V_{IL}$ and $\overline{PGM} = V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses. The CE to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of \overline{OE} . And assuming that $\overline{CE} = \overline{OE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of \overline{PGM} .

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line. When \overline{CE} is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57H1000AD/TC57H1001AD has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC57H1000AD/TC57H1001AD is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57H1000AD/TC57H1001AD is in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The levels required for all inputs are TTL.

The TC57H1000AD / TC57H1001AD can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with \overline{OE} and \overline{CE} at V_{IL} and \overline{PGM} at V_{IH} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to Vpp terminal, a high level $\overline{\text{CE}}$ or $\overline{\text{PGM}}$ input inhibits the TC57H1000AD/TC57H1001AD from being programmed.

Programming of two or more EPROM's in inputs except for \overline{CE} or \overline{PGM} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} and \overline{PGM} of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

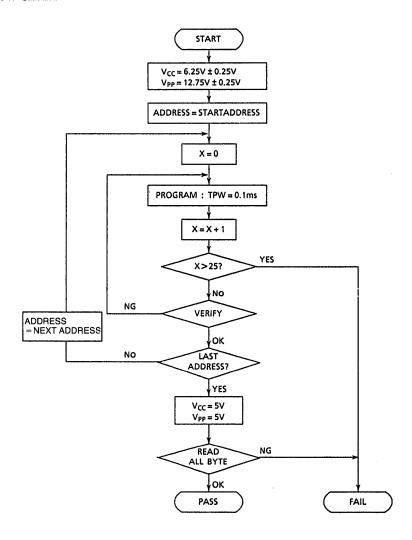
The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the Vpp terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{IH}$.

The programming is achieved by applying a single TTL low level 0.1ms pulse the \overline{PGM} input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

HIGH SPEED PROGRAM MODE

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57H1000AD/TC57H1001AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC57H1000AD/TC57H1001AD by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH} .

These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC57H1000AD/TC57H1001AD.

	SIGNATURE	PINS	Α0	D7	D6	D5	D4	D3	D2	D1	D0	HEX Data
	Manufacture C	ode	VIL	1	0	0	1	1	0	0	0	98
ľ		TC57H1000AD		1	0	0	0	0	1	1	0	86
	Device Code	TC57H1001AD	V _{IH}	o	0	0	0	0	1	1	1	07

Notes: A9 = 12V ± 0.5V

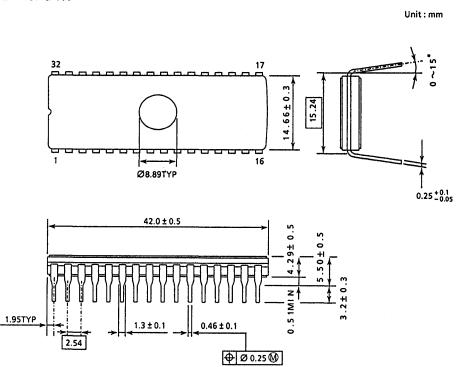
A1~A8, A0~A16, \overline{CE} , $\overline{OE} = V_{IL}$

 $\overline{PGM} = V_{1H}$

OUTLINE DRAWINGS

• Cerdip DIP

WDIP32-G-600



PRELIMINARY

1 MEGA BIT (65,536 WORD \times 16 BIT) CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC57Hl024D is a 65,536 word × 16 bit CMOS ultraviolet light erasable and electrically programmable read only memory. The TC57Hl024D is JEDEC standard pin configuration. This product is packed in 40 pin standard cerdip package.

TC57Hl024D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 40mA/lMHz and access time of 85ns/100ns.

The programming times of the TC57Hl024D except overhead times of EPROM programmer is only 7 seconds by using the high speed programming algorithm.

FEATURES

Peripheral circuit : CMOS
 Memory cell : N-MOS

• Fast access time

TC57Hl024D-85 : 85ns TC57Hl024D-10/100 : 100ns

• Low power dissipation

Active : 40mA/lMHz Standby : 100µA • Single 5V power supply

• Full static operation

• High speed programming operation: tpw 0.1ms

• Input and output TTL compatible

• JEDEC standard 40 pin : TC57Hl024D

• Standard 40 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)

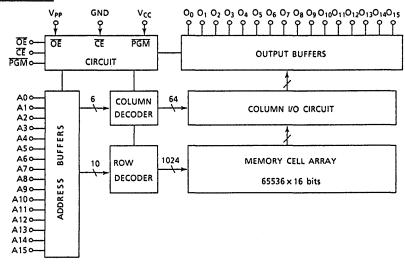
V _{PP} []1	40) V _{CC}
रहं 🛮 2	39 [PGM
D15 🛛 3	38 NC
D14 🛮 4	37 A15
D13 🛭 5	36 A14
D12 🛛 6	35 A13
D11 🛛 7	34) A12
D10 🛛 8	33 A11
D9 □ 9	32 A10
D8 🛘 10	31 A9
v _{ss} □11	30 D Vss
D7 🛘 12	29] A8
D6 🛚 13	28 D A7
D5 🛘 14	27 A6
D4 🛘 15	26 A5
D3 🛛 16	25 A4
D2 [17	24 🖰 A3
D1 🛘 18	23 D A2
DO 🛘 19	22 A1
○E [20	21 A0
L	

PIN NAMES

A0~A15	Address Inputs
D0~D15	Outputs (Inputs)
CE	Chip Enable Input
ŌĒ	Output Enable Input
PGM	Program Control Input
Vcc	V _{CC} Supply Voltage
Vpp	Program Supply Voltage
V _{SS}	Ground
NC	No Connection

TC57H1024D-85, TC57H1024D-10 TC57H1024D-100

BLOCK DIAGRAM



MODE SELECTION

MODE	PIN CE	OE	PGM	V _{PP}	Vcc	D0~D15	Power		
Read	Ĺ	L	Н			Data Out	Active		
Output Deselect	*	н	*	5V	5V	Himb Income de ann	Active		
Standby	н	*	*		l	High Impedance	Standby		
Program	L	н	L			Data In			
Program Inhibit	н	*	*]		Uish Impadance			
	Ļ	н	н	12.75V	6.25V	High Impedance	Active		
Program Verify	L	L	н]		Data Out]		

^{*} H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
Vcc	V _{CC} Power Supply Voltage	- 0.6~7.0	٧
V _{PP}	Program Supply Voltage	- 0.6~14.0	V
V _{IN}	Input Voltage	- 0.6~7.0	V
V _{IN} (A9)	Input Voltage (A9)	- 0.6~13.5	٧
V _{1/0}	input/Output Voltage	- 0.6~V _{CC} + 0.5	V
PD	Power Dissipation	1.5	w
TSOLDER	Soldering Temperature Time	260 · 10	°C · sec
T _{strg}	Storage Temperature	- 65~125	° C
Topr	Operating Temperature	0~70	•c

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57H1024D-85/10	TC57H1024D-100				
Ta	Ambient Temperature	0~70°C					
Vcc	V _{CC} Power Supply Voltage	5V ± 5%	5V ± 10%				
Vpp	V _{PP} Power Supply Voltage	0V~V _{CC}	+ 0.6V				

DC AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ILI	Input Current	V _{IN} = 0~V _{CC}		-	± 10	μА
lcco	Operating Current	CE = 0V I _{OUT} = 0mA t _{cycle} = 1μs	-	-	40	mA
I _{CCS1}	Standby Current	CE = V _{IH}	-	-	1	mA
I _{CCS2}	Standby Corrent	$\overline{CE} = V_{CC} - 0.2V$	-	-	100	μА
V _{IH}	Input High Voltage		2.2	-	V _{CC} + 0.3	٧
VIL	Input Low Voltage		- 0.3	-	0.8	٧
VoH	Output High Voltage	I _{OH} = -400 ₁ 1A	2.4	-	-	٧
Vol	Output Low Voltage	I _{OL} = 2.1mA	-	-	0.4	ν
I _{PP1}	V _{PP} Current	$V_{PP} = V_{CC} \pm 0.6V$	-	-	± 10	μА
lLO	Ouptut Leakage Current	V _{OUT} = 0.4V~V _{CC}	-	-	± 10	μΑ

AC CHARACTERISTICS ($V_{PP} = 0V \sim V_{CC} + 0.6V$)

SYMBOL	PARAMETER	TC57H1	024D-85	TC57H102	4D-10/100	UNIT
STIVIBUL	PARAIVIETER	MIN.	MAX.	MIN.	MAX.	UNII
t _{ACC}	Address Access Time		85	-	100	
tce	CE to Output Valid	_	85	_	100	
t _{OE}	OE to Output Valid		45	-	50	
t _{DF1}	CE to Output in High-Z	-	* 30	-	50	ns
t _{DF2}	OE to Output in High-Z	-	30	-	50	1
tон	Output Data Hold Time	5	l -	10	_	

TC57H1024D-85 is satisfied with the specification of TC57H1024D-100.

AC TEST CONDITIONS

Ouput Load : 1 TTL Gate and C_L=100pF

Input Pulse Rise and Fall Times : 10ns Max.
Input Pulse Levels : 0.45V to 2.4V

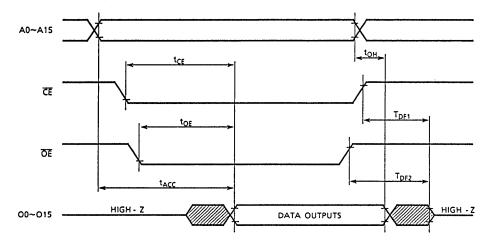
Timing Measurement Reference Levels: Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

CAPACITANCE *(Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	-	6	10	_
Cout	Output Capacitance	V _{OUT} = 0V	-	10	12	pr

^{*} This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} + 0.3	V
VIL	Input Low Voltage	- 0.3	-	0.8	V
Vcc	V _{CC} Power Supply Voltage	6.00	6.25	6.50	V
Vpp	V _{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC AND OPERATING CHARACTERISTICS(Ta = 25 ± 5 °C, V_{CC} = 6.25V ± 0.25 V, V_{PP} = 12.75V ± 0.25 V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ILI	Input Current	V _{IN} = 0~V _{CC}	£	-	± 10	μΑ
Voh	Output High Voltage	i _{OH} = -400μA	2.4	-	-	٧
VoL	Output Low Voltage	I _{OL} = 2.1mA	-	-	0.4	٧
Icc	V _{CC} Supply Current	-	-	-	50	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} = 13.0V	_	-	100	mA

AC PROGRAMMING CHARACTERISTICS(Ta=25 \pm 5°C, V_{CC}=6.25V \pm 0.25V, V_{PP}=12.75V \pm 0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tas	Address Setup Time	-	2	-	-	μs
t _{AH}	Address Hold Time		2	-	-	μs
t _{CES}	CE Setup Time		2	-	-	μs
t _{CEH}	ČĒ Hold Time	-	2	-	-	μs
t _{D\$}	Data Setup Time	-	2	-	-	μs
^t DH	Data Hold Time	-	2	_	-	μs
tvs	V _{PP} Setup Time	-	2	-	T -	μs
tpW	Program Pulse Width		0.095	0.1	0.105	ms
toE	OE to Output Valid	-	-	-	500	ns
t _{DF2}	OE to Output in High-Z	ČĒ = V _{IL}	-	-	150	ns
toes	ŌĒ Setup Time	-	2	_	_	μs

AC TEST CONDITIONS

• Output Load

: 1 TTL Gate and C_L (100pF)

• Input Pulse Rise and Fall Times

: 10ns Max.

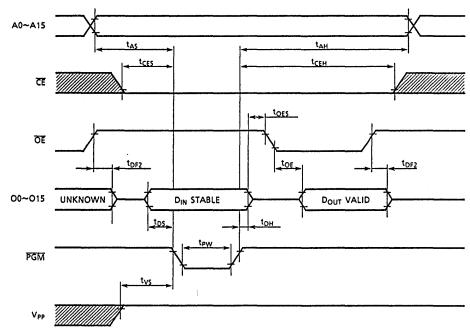
• Input Pulse Levels

: 0.45V and 2.4V

Timing Measurement Reference Levels: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



Note:

- 1. VCC must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.
 - 2. Removing the device from socket and setting the device in socket with V_{PP} = 12.75V may cause permanent damage to the device.
- 3. The Vpp supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the Vpp terminal.
 When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its

pulse should not be exceeded 14V.

TC57H1024D-85, TC57H1024D-10 TC57H1024D-100

ERASURE CHARACTERISTICS

The TC57H1024D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. The integrated dose (Ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W·sec./cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 $[\mu W/cm^2]$ will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 $[\mu W/cm^2] \times (20 \times 60)$ [sec] $\approx 15 [W \cdot sec./cm^2]$.)

The TC57H1024D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TC57H1024D's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN	CĒ	ŌĒ	PGM	V _{PP}	Vcc	D0~D15	Power	
READ OPERATION	Read		L	L	Н			Data Out	Active	
	Output Deselect		*	Н	*	5∨	5V	High Impodence		
	Standby		Н	*	*]		High Impedance	Standby	
	Program		L	н	L			Data In		
PROGRAM OPERATION	December Inhibit		Н	*	*			High Impadance		
(Ta = 25 ± 5°C)	Program Inhibit		L	н	Н	12.75∨	6.25∨	High Impedance	Active	
	Program Verify		L	L	н			Data Out	7	

Note: H; VIH, L: VIL, *: VIII or VIL

TC57H1024D-85, TC57H1024D-10 TC57H1024D-100

READ MODE

The TC57H1024D has three control functions. The chip enable (CE) controls the operation power and should be used for device selection.

The output enable (\overline{OE}) controls the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$ and $\overline{PGM} = V_{III}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The CE to output valid (tCE) is equal to the address access time (tACC).

Assuming that $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$ and all addresses are valid, the output data is valid at the outputs after toe from the falling edge of \overline{OE} .

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{III}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line.

When CE is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57H1024D has a low power standby mode controlled by the $\overline{\text{CE}}$ signal.

By applying a high level to the \overline{CE} input, the TC57H1024D is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (VCC) and then the outputs are in a high impedance state, independent of the \overline{OE} inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57H1024D are in the "1" state which is erased state.

Therefore the program operation is to introduce "Ø" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC57H1024D can be programmed any location at anytime -- either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with OE and CE at VII, and PGM at VIH.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to Vpp terminal, a high level \overline{CE} or \overline{PGM} input inhibits the TC57H1024D from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for \overline{CE} or \overline{PGM} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} and \overline{PGM} of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the Vpp terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{IH}$.

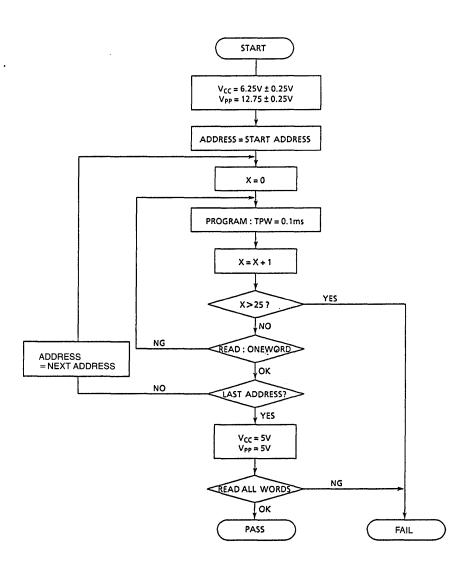
The programming is achieved by applying a single TTL low level 0.1ms pulse the \overline{PGM} input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{\text{CC}} = V_{\text{PP}} = 5V$.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57H1024D which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from TC57H1024D by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to $V_{\rm IL}$ in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to $V_{\rm IH}$.

These two codes possess an odd parity with the parity bit of (O7).

The following table shows electric signature of TC57H1024D.

PINS	A ₀	015	014	013	012	011	010	Og	08	07	06	Ο ₅	04	Ο3	O2	01	00	HEX DATA
Manufacturer Code	V _{IL}	*		*	*	*	*	•	*	1	0	0	1	1	0	0	0	**98
Device Code	V _{IH}			*	*	*		*	*	1	0	0	0	1	0	0	1	**89

Notes: $A9 = 12V \pm 0.5V$, $A_1 - A_8$, $A_{10} - A_{15}$, \overline{CE} , $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$

*: Don't care

DC AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	TINU
V _{ID}	A ₉ Auto Select Voltage	11.5	12.0	12.5	٧

TC57H1024D-85, TC57H1024D-10 TC57H1024D-100

OUTLINE DRAWINGS

• Cerdip DIP

WDIP40-G-600A

Unit: mm

1 MEGA BIT (65,536 WORD x 16 BIT) HIGH SPEED CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC57Hl025AD is a 65,536 word \times 16 bit high speed CMOS ultraviolet light erasable and electrically programmable read only memory. The TC57Hl025AD is JEDEC standard pin configuration. This product is packed in 40 pin standard cerdip package.

TC57Hl025AD is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 60mA/lMHz and access time of 55ns.

The programming time of the TC57Hl025AD except overhead times of EPROM programmer is only 7 seconds by using the high speed programming algorithm.

FEATURES

• Peripheral circuit

: CMOS : NMOS

Memory cell

Fast access time

TC57H1025AD-55 : 55ns

Low power dissipation
 Active : 60mA/IMHz

Standby: 10mA

• Single 5V power supply

• Full static operation

• High speed programming operation: tpw 0.1ms

• Input and output TTL compatible

• JEDEC standard 40 pin

• Standard 40 pin DIP cerdip package

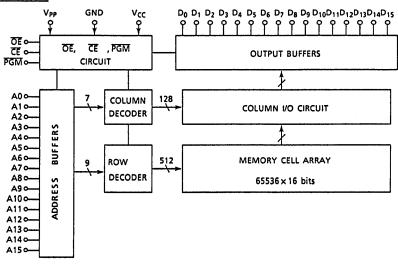
PIN CONNECTION (TOP VIEW)

V _{PP} []1	40] Vcc
₹ 12	39 FGM
D15 🛛 3	38 NC
D14 4	37 A15
D13 🛭 5	36 A14
D12 [6	35 A13
D11 [7	34] A12
D10 [8	33 A11
D9 🗓 9	32 A10
D8 🛘 10	31 A9
V ₅₅ []11	30] V _{ss}
D7 []12	29∏ ∧8
D6 🛚 13	28 A7
D5 🗓 14	27 A6
D4 🛮 15	26] A5
D3 🛛 16	25 A4
D2 []17	24[] A3
D1 []18	23] A2
00 🛮 19	22 A1
<u> </u>	21 D A0
ا	

PIN NAMES

A0~A15	Address Inputs •
D0~D15	Outputs (inputs)
CE .	Chip Enable Input
ŌĒ	Output Enable Input
PGM	Program Control Input
Vcc	V _{CC} Supply Voltage
V _{PP}	Program Supply Voltage
Vss	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE	PIN CE	OE	PGM	Vpp	Vcc	D0~D15	Power
Read	L	L.	Н			Data Out	A 441a
Output Deselect		н	*	" JV JV		Active	
Standby	Н	н • •		*		High Impedance	Standby
Program	L	Н	L]		Data In	
Program Inhibit	Н	*	*]		Ulah Impadaga	
	L	н	н	12.75V 6.25		High Impedance	Active
Program Verify	L	L	н] .	-	Data Out	1

^{*} H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
Vcc	V _{CC} Power Supply Voltage	- 0.6~7.0	٧
Vpp	Program Supply Voltage	-0.6~14.0	٧
V _{IN}	Input Voltage	- 0.6~7.0	٧
V _{IN} (A9)	input Voltage (A9)	- 0.6~13.5	٧
V _{VO}	Input/Output Voltage	-0.6~V _{CC} +0.5	٧
PD	Power Dissipation	1.5	W
TSOLDER	Soldering Temperature · Time	260 · 10	°C · sec
T _{strg}	Storage Temperature	- 65~125	° C
Topr	Operating Temperature	0~70	•c

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57H1025AD-55
Ta	Ambient Temperature	0~70°C
Vcc	V _{CC} Power Supply Voltage	5V ± 5%
Vpp	V _{PP} Power Supply Voltage	0V~V _{CC} + 0.6V

DC AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
1 _{Ll}	Input Current	V _{IN} = 0~V _{CC}	-	-	± 10	μА
lcco	Operating Current	ČE = 0V I _{OUT} = 0mA t _{cycle} = 1μs	_	-	60	mA
I _{CCS1}	Standby Current	CE = V _{IH}	-	-	12	mA
I _{CC\$2}	Standby Current	<u>CE</u> = V _{CC} − 0.2V	-	-	10	mA
VIH	Input High Voltage		2.2	_	V _{CC} + 0.3	V
VIL	Input Low Voltage		- 0.3	-	0.8	٧
Voн	Output High Voltage	I _{OH} = -4.0mA	2.4	_	-	٧
VOL	Output Low Voltage	I _{OL} = 8.0mA	-	-	0.4	٧
IPP1	V _{PP} Current	$V_{PP} = V_{CC} + 0.6V$	-	-	± 10	μΑ
lo	Output Leakage Current	V _{OUT} = 0.4V~V _{CC}	-	-	± 10	μA

AC CHARACTERISTICS (VPP=0V~VCC+0.6V)

SYMBOL	PARAMETER	TC57H1	TC57H1025AD-55		
STIVIBOL	PARAIVIETER	MIN.	MAX.	UNIT	
t _{ACC}	Address Access Time	-	55		
t _{CE}	CE to Output Valid	-	55		
toE	OE to Output Valid	_	30	ns	
t _{DF1}	CE to Output in High-Z	_	25		
t _{DF2}	OE to Output in High-Z	_	25]	
tон	Output Data Hold Time	0	-		

AC TEST CONDITIONS

Output Load

: See Fig.1

• Input Pulse Rise and Fall Times

: 5ns Max.

• Input Pulse Levels

: 0V to 3V

• Timing Measurement Reference Levels : Inputs 1.5V Outputs 1.5V

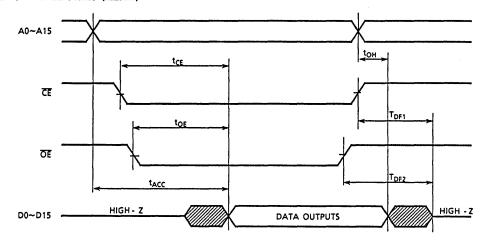
Fig.1 OUTPUT LOAD

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CIN	Input Capacitance	V _{IN} = 0V	_	6	10	
C _{OUT}	Output Capacitance	V _{OUT} = 0V	-	10	12	Pr

^{*} This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} + 0.3	٧
VIL	Input Low Voltage	- 0.3	-	0.8	v
Vcc	V _{CC} Power Supply Voltage	6.00	6.25	6.50	V
Vpp	V _{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC AND OPERATING CHARACTERISTICS(Ta=25 \pm 5°C,V_{CC}=6.25V \pm 0.25V, V_{PP}=12.75V \pm 0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ارر	input Current	V _{IN} = 0~V _{CC}	-	-	± 10	μА
V _{OH}	Output High Voltage	I _{OH} = - 4.0mA	2.4	-	-	٧
Vol	Output Low Voltage	I _{OL} = 8.0mA	-	-	0.4	V
lcc	V _{CC} Supply Current	_	-	-	50	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} = 13.0V	-	-	100	mA

AC PROGRAMMING CHARACTERISTICS(Ta=25 \pm 5°C, V_{CC}=6.25V \pm 0.25V, V_{PP}=12.75V \pm 0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	-	_	μs
t _{AH}	Address Hold Time	-	2	-	-	μs
t _{CES}	CE Setup Time	-	2	-	_	μs
t _{CEH}	CE Hold Time	_	2	_	_	μs
t _{D\$}	Data Setup Time	-	2	-	-	μs
t _{DH}	Data Hold Time		2	-	-	μs
t _{VS}	V _{PP} Setup Time	_	2	-	_	μs
tpW	Program Pulse Width	-	0.095	0.1	0.105	ms
toE	OE to Output Valid	-	-	-	500	ns
t _{DF2}	OE to Output in High-Z	Œ = V _{IL}	-	_	150	ns
toes	OE Setup Time	-	2	-	_	μs

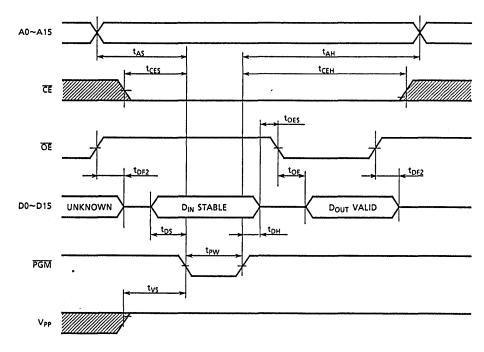
ACTEST CONDITION

Output Load : See Fig.1
 Input Pulse Rise and Fall Times : 5ns Max.
 Input Pulse Levels : 0V to 3V

• Timing Measurement Reference Levels : Inputs 1.5V Outputs 1.5V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



- Note: 1. VCC must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.
 - 2. Removing the device from socket and setting the device in socket with VPP=12.75V may cause permanent damage to the device.
 - 3. The VPP supply voltage is permitted up to 14V for program operation. Voltages greater than should not be applied to the VPP terminal.

When the switching pulse voltage is applied to the VPP terminal, the overshoot voltage of its 14V should not be applied to the VPP terminal.

ERASURE CHARACTERISTICS

The TC57H1025AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. The integrated dose (Ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W·sec./cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μ W/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μ W/cm²] × (20 × 60) [sec]=15[W·sec./cm²].)

The TC57H1025AD's erasure begins to occur when exposed to light with wavelength shorter than 4000\AA . Sunlight and fluorescent lamps include $3000{\sim}4000\text{\AA}$ wavelength components. Therefore components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TC57H1025AD's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN	ζĒ	ŌĒ	PGM	V _{PP}	Vcc	D0~D15	Power	
READ OPERATION (Ta = 0~70°C)	Read		٦	L	н			Data Out	Active	
	Output Deselect		*	н	*	5V 5V		High Impedance	Active	
	Standby		Н	*	*			nigh impedance	Standby	
PROGRAM OPERATION (Ta = 25 ± 5°C)	Program		L	H,	L			Data in		
	Program Inhibit		Н	*	*		6.25V	High Impedance	Active	
			L	н	н	12.75V		High Impedance	Active	
	Program Verify		L	L	Н			Data Out]	

Note : H ; V_{IH} , L : V_{IL} , * : V_{IH} or V_{IL}

READ MODE

The TC57H1025AD has three control functions. The chip enable (CE) controls the operation power and should be used for device selection.

The output enable (\overline{OE}) controls the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$ and $\overline{PGM} = V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{\text{CE}}$ to output valid (tCE) is equal to the address access time (tACC).

Assuming that $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of \overline{OE} .

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{III}$ or $\overline{OE} = V_{III}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line.

When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57H1025AD has a low power standby mode controlled by the CE signal.

By applying a high level to the \overline{CE} input, the TC57H1025AD is placed in the standby mode which reduces the operating current to 10mA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the \overline{OE} inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57H1025AD are in the "1" state which is erased state.

Therefore the 'rogram operation is to introduce "0s" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC57H1025AD can be programmed any location at anytime -- either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with OE and CE at VIL and PGM at VIH.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to Vpp terminal, a high level $\overline{\text{CE}}$ or $\overline{\text{PGM}}$ input inhibits the TC57H1025AD from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for \overline{CE} or \overline{PGM} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} and \overline{PGM} of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with V_{CC} =6.25V and \overline{PGM} = V_{IH} .

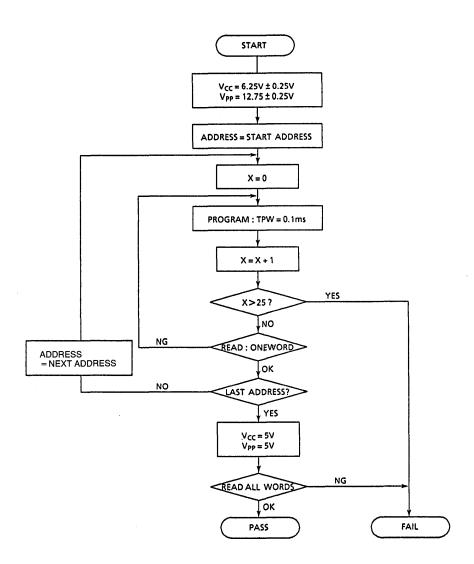
The programming is achieved by applying a single TTL low level 0.1ms pulse the \overline{PGM} input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57H1025AD which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from TC57H1025AD by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to $V_{\rm IL}$ in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to $V_{\rm IH}$.

These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC57H1025AD.

PINS	A ₀	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D9	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	HEX DATA
Manufacturer Code	V _{IL}	*	•	*	ā. #	٠	•	*	٠	1	0	0	1	1	0	0	0	**98
Device Code	ViH	*	*	*	*	٠	*	*	*	1	0	0	0	1	0	0	1	**89

Note: $A9 = 12V \pm 0.5V$, $A_1 - A_8$, $A_{10} - A_{15}$, $\overline{CE}_{i'}$ $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$

*: Don't care

OUTLINE DRAWINGS

• Cerdip DIP
WDIP40-G-600A

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Unit: mm

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1 MEGA BIT (65,536 WORD×16 BIT) HIGH SPEED CMOS U.V. ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The TC57H1026D is a 65,536 word \times 16 bit high speed CMOS ultraviolet light erasable and electrically programmable read only memory. The TC57H1026D is JEDEC standard pin configuration. This product is packed in 40 pin standard cerdip package.

TC57Hl026D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 70mA/lMHz and access time of 35ns.

The programming times of the TC57Hl026D except overhead times of EPROM programmer is only 7 seconds by using the high speed programming algorithm.

FEATURES

Peripheral circuit : CMOS
 Memory cell : NMOS

• Fast access time

TC57Hl026D-35 : 35ns

Low power dissipation

Active : 70mA/lMHz Standby : 10mA • Single 5V power supply

• Full static operation

• High speed programming operation: tpw 0.1ms

• Input and output TTL compatible

• JEDEC standard 40 pin

• Standard 40 pin DIP cerdip package

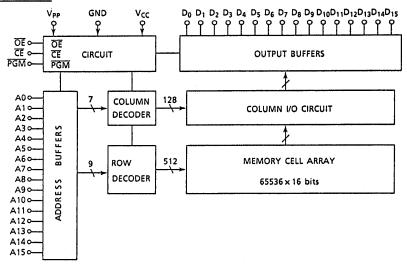
PIN CONNECTION (TOP VIEW)

		~	1
Vpp	[]1	40] v _{cc}
CE		39	PGM
D15	Дз	38	D NC
D14	[]4	37	A15
D13]5	36	A14
D12	<u>]</u> 6	35	A13
D11	[]6 []7	34	
D10	₫8	33	D A11
D9	9	32	
D8	10		A9
Vss	911		V _{ss}
D7	[]12		A8
D6]13		A7
D5	14		A6
D4	15		A5
D3	16	25	
D2	17		A3
D1	18		AZ
00	119		AI
<u>DE</u>	20		A0
OE.	ت ا		,v

PIN NAMES

A0~A15	Address Inputs
D0~D15	Outputs (Inputs)
CE	Chip Enable Input
ŌĒ	Output Enable Input
PGM	Program Control Input
Vcc	V _{CC} Supply Voltage
V _{PP}	Program Supply Voltage
V _{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE	N CE	OE	PGM	V _{PP}	Vcc	D0~D15	Power
Read	L	L	н			Data Out	Active
Output Deselect	*	Н	*	5∨	5V	High Impedance	Active
Standby	н	*	*			High Impedance	Standby
Program	L	Н	L			Data In	
	н	*	*]		High brands	Active
Program Inhibit	L	Н	н	12.75V	75V 6.25V High Impedance		Active
Program Verify	L	L	н			Data Out	
Blank Check One	L	Lis	нн			Data Out One (FFFF)	
Blank Check Zero	L	Н	нн	5∨	5V	Data Out Zero (0000)	Active

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	- 0.6~7.0	٧
Vpp	Program Supply Voltage	- 0.6~14.0	٧
V _{IN}	Input Voltage	- 0.6~7.0	v
V _{IN} (A9)	input Voltage (A9)	- 0.6~13.5	٧
V _{I/O}	Input/Output Voltage	- 0.6~V _{CC} + 0.5	٧
PD	Power Dissipation	1.5	w
TSOLDER	Soldering Temperature Time	260 · 10	°C · sec
T _{strg}	Storage Temperature	- 65~125	• c
Topr	Operating Temperature	0~70	° C

* H or L

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC57H10246D-35, 45
Ta	Ambient Temperature	0~70°C
Vcc	V _{CC} Power Supply Voltage	5V ± 5%
V _P p	V _{PP} Power Supply Voltage	V _{CC} - 0.6v~V _{CC} + 0.6V

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CO	MIN.	TYP.	MAX.	UNIT	
lu	Input Current	V _{IN} = 0~V ₀	V _{IN} = 0~V _{CC}			± 10	μА
lcco	Operating Current	CE = 0V I _{OUT} = 0mA	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		-	70	mA
I _{CCS1}	Standby Current	CE = VIH	-	-	12	mA	
1 _{CCS2}	Standby Current	CE = V _{CC} -	-	-	10	mA	
VIH	Input High Voltage	_	_	2.2	-	V _{CC} + 0.3	V
VIL	Input Low Voltage	_	_	- 0.3	-	0.8	V
VoH	Output High Voltage	I _{OH} = -4.0	mĄ	2.4	-	-	V
V _{OL}	Output Low Voltage	I _{OL} = 8.0	I _{OL} = 8.0mA		-	0.4	٧
I _{PP1}	V _{PP} Current	Vpp = Vcc	$V_{PP} = V_{CC} \pm 0.6V$		-	± 10	μА
l _{LO}	Ouptut Leakage Current	V _{OUT} = 0.4			± 10	μΑ	

AC CHARACTERISTICS ($V_{PP} = V_{CC} - 0.6v \sim V_{CC} + 0.6V$)

C) (1 4 D O)		TC57H	1026D-35	TC57H	1026D-45	ļ <u>-</u>
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT
t _{ACC}	Address Access Time	-	35	-	45	
t _{CE}	CE to Output Valid	-	35	-	45	
t _{OE}	OE to Output Valid	-	20	-	. 20	ns
tDF1	CE to Output in High-Z	0	20	0	20] "
t _{DF2}	OE to Output in High-Z	0	20	0	20]
tон	Output Data Hold Time	0	-	0	-	1

AC TEST CONDITIONS

• Output Load : See Fig. 1

• Input Pulse Rise and Fall Time : 5ns Max.

Input Pulse Levels : 0V to 3V
 Timing Measurement Reference Level : Inputs 1.5V Outputs 1.5V

480Ω 30pF ₹ 255Ω

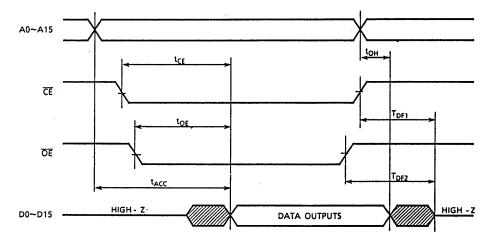
Fig. 1 OUTPUT LOAD

CAPACITANCE *(Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT	
C _{IN}	Input Capacitance	V _{IN} = 0V	-	10	_	
C _{OUT}	Output Capacitance	V _{OUT} = 0V	-	12	př	

^{*} This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	3.0	-	V _{CC} + 0.3	٧
V _{IL}	Input Low Voltage	- 0.3	-	0.6	٧
Vcc	V _{CC} Power Supply Voltage	6.00	6.25	6.50	v
Vpp	V _{PP} Power Supply Voltage	12.50	12.75	13.00	٧

DC PROGRAMMING CHARACTERISTICS(Ta = 25 ± 5 °C,V_{CC} = 6.25V ±0.25 V, V_{PP} = 12.75V ±0.25 V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ILI	Input Current	V _{IN} = 0~V _{CC}	-	-	± 10	μА
VoH	Output High Voltage	I _{OH} = -4.0mA	2.4	-	-	V
VoL	Output Low Voltage	I _{OL} = 8.0mA	_	_	0.4	V
Icc	V _{CC} Supply Current	-	-	_	50	mA
Ipp2	V _{PP} Supply Current	V _{PP} = 13.0V	-	-	100	mA

AC PROGRAMMING CHARACTERISTICS (Ta = $25 \pm 5^{\circ}$ C, $V_{CC} = 6.25 V^{\circ}0.25 V$, $V_{PP} = 12.75 V \pm 0.25 V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tas	Address Hold Time	-	2	-	-	μs
t _{AH}	Address Hold Time	-	2	-	-	μs
t _{CES}	CE Setup Time	-	2	-	_	μς
t _{CEH}	CE Hold Time	-	2	_	-	μs
tos	Data Setup Time	-	2	-	-	μs
t _{DH}	Data Hold Time	-	2	-	-	μς
tvs	V _{PP} Setup Time	-	2	-	-	μs
tpw	Program Pulse Width	-	0.095	0.1	0.105	ms
toE	OE to Output Valid	-	-	-	500	ns
t _{DF2}	OE to Output in High-Z	CE = V _{IL}	-	-	150	ns
toes	OE Setup Time	-	2	_	_	μς

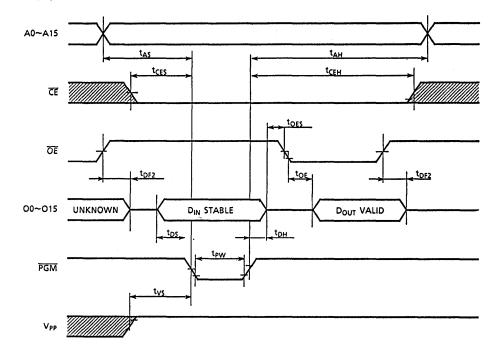
AC TEST CONDITIONS

Output Load : See Fig. 1
 Input Pulse Rise and Fall Time : 5ns Max.
 Input Pulse Levels : 0V and 3V

• Timing Measurement Reference Level: Input 1.5V, Ouptut 1.5V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



- Note: 1. VCC must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.
 - 2. Removing the device from socket and setting the device in socket with VPP=12.75V may cause permanent damage to the device.
 - 3. The VPP supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the VPP terminal. When the switching pulse voltage is applied to the VPP terminal, the overshoot voltage of its

pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57H1026D erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. The integrated dose (Ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W·sec./cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [µW/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [µW/cm²] × (20 × 60) [sec]≈15 [W·sec./cm²].)

The TC57II1026D erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seal - Toshiba EPROM Protect Seal AC902 - is available.

OPERATION INFORMATION

The TC57H1026D' eight operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN	CE	ŌĒ	PGM	V _{PP}	Vcc	D0~D15	Power	
READ	Read		L	L	н			Data Out	Active	
OPERATION	Output Deselet		*	Н		5∨	5∨	High Impodunce	Active	
(Ta = 0~70°C)	Standby		н	*	*			High Impedance	Standby	
	Program		L	Н	L			Data In		
PROGRAM OPERATION			н	*	*	l		lünk lannadanaa	A adding	
(Ta = 25 ± 5°C)	Program Inhibit		L	н	Н	12.750 6.250		High Impedance	Active	
(10-25250)	Program Verify		L	L	н	1		Data Out		
Blank Check	Blank Check One		L	L	нн			Data Out One	.,	
OPEREATION	Blank Check Zero		L	Н	нн	5v	5v	Data Out Zero	Active	

Note : II ; V_{III} , L : V_{IL} , * : V_{III} or V_{IL} IIII ; $12V \pm 0.5V$

TC57H1026D-35 TC57H1026D-45

READ MODE

The TC57H1026D has three control functions. The chip enable ($\overline{\text{CE}}$) controls the operation power and should be used for device selection.

The output enable (\overline{OE}) control the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{1L}$ and $\overline{PGM} = V_{1H}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The \overline{CE} to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{III}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of \overline{OE} .

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{III}$ or $\overline{OE} = V_{III}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line.

When CE is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57H1026D has a low power standby mode controlled by the CE signal.

By applying a high level to the \overline{CE} input, the TC57H1026D is placed in the standby mode which reduce the operating current to 10mA by applying MOS-high level (VCC) and then the outsuts are in a high impedance state, independent of the \overline{OE} inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57H1026D are in the "1" state which is erased state.

Therefore the program operation is to introduce "0'S" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC57H1026D can be programmed any location at anytime -- either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with OE and CE at VIL and PGM at VIII.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to Vpp terminal, a high level \overline{CE} or \overline{PGM} input inhibits the TC57H1026D from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for \overline{CE} or \overline{PGM} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} and \overline{PGM} of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the Vpp terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{HI}$.

The programming is achieved by applying a single TTL low level 0.1ms pulse the \overline{PGM} input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct; another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{\rm PP} = 5 \, V$.

BLANK CHECK MODE

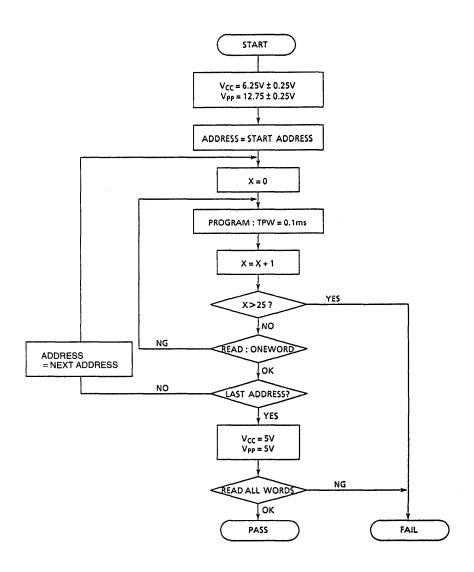
In the erase state a device contains neither a one nor a zero, because of the differential memory cell. The erase state of this device is verified by using the two blank check modes.

BLANK CHECK ZERO mode, which is to check that one side of the differential memory cell is "1" data, is accomplished with $\overline{OE} = \overline{CE} = V_{IL}$ and $\overline{PGM} = 12V$.

BLANK CHECK ONE mode, which is to check that the other side of the differential memory cell is "0" data, is accomplished with $\overline{OE} = V_{III}$, $\overline{CE} = V_{IL}$ and $\overline{PGM} = 12V$.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57H1026D which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from TC57H1026D by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH} .

These two codes possess an odd parity with the parity bit of (D7).

The following table shows electric signature of TC57H1026D.

PINS S!GNATURE	A ₀	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D9	D ₈	D ₇	D ₆	D ₅	D4	D ₃	D ₂	Dı	D ₀	HEX DATA
Manufacturer Code	V _{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V _{IH}		•	*	٠	٠	*	*	*	1	0	0	0	1	0	0	1	**C7

Note: $A9 = 12V \pm 0.5V$, $A_1 - A_8$, $A_{10} - A_{15}$, \overline{CE} , $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$

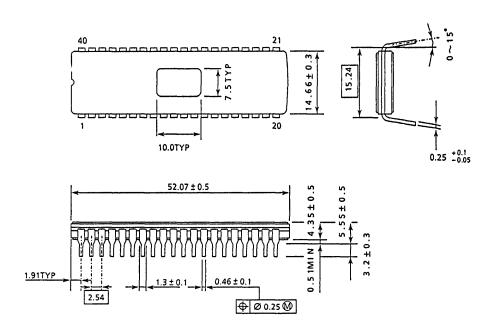
*: Don't care

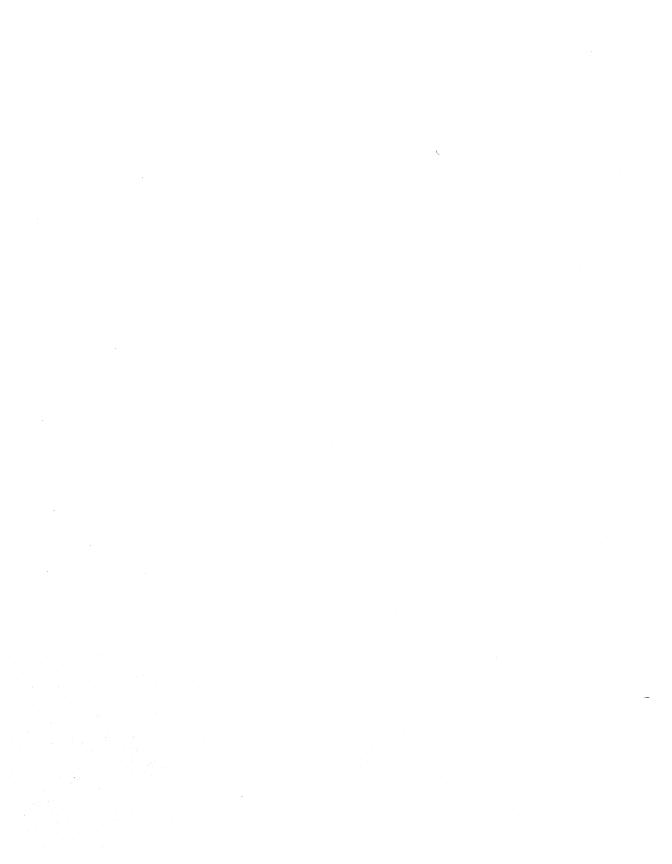
OUTLINE DRAWINGS

• Cerdip DIP

WDIP40-G-600A

Unit: mm





32,768 WORD imes 8 BIT CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC54256AP/AF is a 32,768 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic package. The TC54256AP/AF's access time is 200ns and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TC57256AD's. Once programmed, the TC54256AP/AF cannot be erased because of using plastic DIP without transparent window.

FEATURES

- Peripheral circuit: CMOS Memory cell : N-MOS
- Low power dissipation Active: 30mA/6.7MHz Standby: 100uA
- · Fast access time: 200ns
- Single 5V power supply
- · Full static operation
- · High speed programming mode

· Inputs and outputs TTL compatible

BLOCK DIAGRAM

- Pin compatible with ROM TC53257P, TMM23256P, EPROM TMM27256D/AD, TC57256D/AD, One time PROM TMM24256P/AP and TC54256P
- · Standard 28 pin DIP plastic package: TC54256AP
- Plastic Flat Package : TC54256AF

08°{ 08°	V _{PP} OE a	nd Ö		/cc	000	OUTPU	03 04 0 0 JT BUI	O5 FFER	۲
A0 0 A1 0 A2 0 A3 0 A4 0 A5 0	BUFFERS	6_	COL		64	C	DLUMN CIRC		
A60 A70 A80 A90 A110 A120 A130 A140	ADDRESS B	9,	PCC		512		MORY ARRA ,768×	Y	_

PIN CONNECTION (TOP VIEW) V_{PP} C|1 28 🗖 V C C A12 2 27 A14 A7 🗖 3 26 A13 A6 🛮 4 25 A8 A5 🗖 5 24 A A 9 A4 0 6 23 A11 A3 07 22 DE 21 A10 8 D SA A1 49 20 D CE 19 07 A0 10 00 디끄 18 06 01 412 17 05 02 🗖 13 16 04 GND 🗖 14 15 03

PIN NAMES

1 211 13/3/1	
A0 ~ A14	Address Inputs
00 ∿ 07	Outputs (Inputs)
ĈĒ	Chip Enable Input
ŌĒ	Output Enable Input
V _{PP}	Program Supply Voltage
VCC	V _{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

PIN	CE	ŌĒ	VPP	VCC	00 ∿ 07	POWER
MODE	(20)	(22)	(1)	(28)	$(11 \sim 13, 15 \sim 19)$	LOWER
Read	L	L			Data Out	Active
Output Deselect	*	Н	5V	50	High Impedance	ACLIVE
Standby	H	*			High Impedance	Standby
Program	L	H			Data In	
Program Inhibit	H	H	12.5V	6V	High Impedance	Active
Program Verify	*	L			Data Out	

*: H or L

TC54256AP/AF

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
VCC	VCC Power Supply Voltage	-0.6 ∿ 7.0	v
V _{PP}	Program Supply Voltage	-0.6 ∿ 14.0	v
VIN	Input Voltage	-0.6 ∿ 7.0	v
V _I /O	Input/Output Voltage	-0.6 ~ V _{CC} +0.5	v
PD	Power Dissipation	1.5	W
TSOLDER	Soldering Temperature Time	260 • 10	°C · sec
TSTRG	Storage Temperature	-65 ∿ 125	°c
TOPR	Operating Temperature	-40 ∿ 85	°c

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	V _{CC} +0.3	
v _{IL}	Input Low Voltage	-0.3	-	0.8	
v _{cc}	V _{CC} Power Supply Voltage	4.75	5.00	5.25	V
V _{PP}	Vpp Power Supply Voltage	V _{CC} -0.6	VCC	V _{CC} +0.6	

D.C. and OPERATING CHARACTERISTICS ($Ta=-40 \sim 85$ °C, $VCC=5V\pm5\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	VIN=OV ~ VC	$V_{IN}=0V \sim V_{CC}$		-	±10	μA
Iccol			f=6.7MHz	-	- ,	30	4
I _{CCO2}	Operating Current	ČE=0V	f=lMHz	-	-	10	mA
I _{CCS1}	Ch 11 . C	Œ=V _{IH} Œ=V _{CC} -0.2V		449	-	1	mA
I _{CCS2}	Standby Current			_	-	100	μA
v _{OH}	Output High Voltage	I _{OH} =-400µA		2.4	-	-	v
V _{OL}	Output Low Voltage	I _{OL} =2.1mA		_	-	0.4	V
I _{PP1}	Vpp Current	V _{PP} =V _{CC} ±0.6V			-	±10	μА
ILO	Output Leakage Current	V _{OUT} =0.4V ∿ V _{CC}		••		±10	μA

A.C. 0	CHARACTERISTICS	$(Ta=-40 \sim 85^{\circ}C,$	$V_{CC}=5V\pm5\%$	$V_{PP}=V_{CC}\pm0.6V$
--------	-----------------	-----------------------------	-------------------	------------------------

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
tACC	Address Access Time	CE=OE=VIL	-	200	
t _{CE}	CE to Output Valid	ŌĒ=V _{IL}	-	200	1
t _{OE}	OE to Output Valid	CE=V _{IL}	-	70	
t _{DF1}	CE to Output in High-Z	ŌĒ=V _{IL}	0	60	ns
t _{DF2}	OE to Output in High-Z	CE=V _{IL}	0	60	1
t _{OH}	Output Data in Hold Time	CE=OE=V _{IL}	0	-	

A.C. TEST CONDITIONS

· Output Load

: 1 TTL Gate and C_L =100pF

· Input Pulse Rise and Fall Times

: 10ns Max.

• Input Pulse Levels

: 0.45V ~ 2.4V

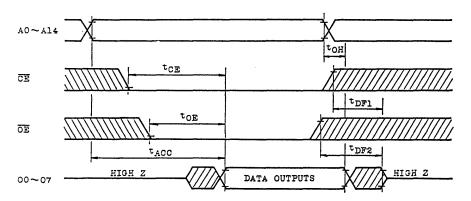
· Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CIN	Input Capacitance	v _{IN} =0v	-	4	6	n.P
C _{OUT}	Output Capacitance	V _{OUT} =0V	-	8	12	PF

^{*} This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



TC54256AP/AF

PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	V _{CC} +1.0	
AIT	Input Low Voltage	-0.3	-	0.8	7 ,,
Vcc	V _{CC} Power Supply Voltage	5.75	6.0	6.25	7 °
V _{PP}	V _{PP} Power Supply Voltage	12.0	12.5	13.0	1

D.C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	T -	-	±10	μA
v _{OH}	Output High Voltage	I _{OH} =-400μA	2.4	-	-	V
VOL	Output Low Voltage	I _{OL} =2.1mA	_	-	0.4	V
¹cc	V _{CC} Supply Current	-	-	-	40	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} =13.0V	-	-	50	mA
V _{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, VCC=6V±0.25V, VPP=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	-		μs
t _{AH}	Address Hold Time	-	2	-	-	μs
tCES	CE Setup Time	-	0		-	ns
t _{CEH}	CE Hold Time	-	0	_		ns
toes	OE Setup Time	-	2	-	-	μs
tDS	Data Setup Time	-	2	-	-	μs
t _{DH}	Data Hold Time	-	2	-	-	μS
t _{VPS}	V _{PP} Setup Time	-	2	-	-	μS
tvcs	V _{CC} Setup Time	-	2	-	-	μs
t _{PW}	Initial Program Pulse Width	CE=VIL, OE=VIH	0.95	1	1.05	ms
t _{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t _{OE}	OE to Output Valid	CE=V _{IH}	-	-	150	ns
t _{DFP}	OE to Output in High-Z	CE=VIH	-	-	130	ns

A.C. TEST CONDITIONS

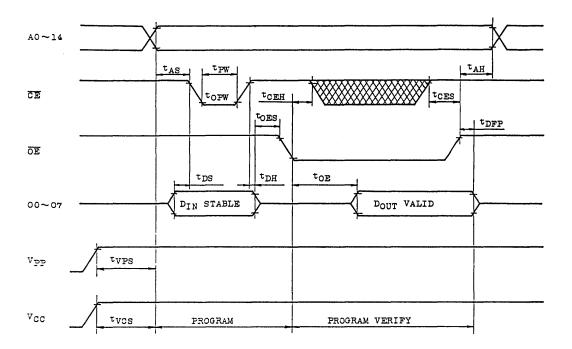
 \cdot Output Load : 1 TTL Gate and CL (100pF)

• Input Pulse Rise and Fall Times : 10ns Max. • Input Pulse Levels : $0.45 \text{V} \sim 2.4 \text{V}$

· Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM) $(v_{CC} = 6v \pm 0.25v, v_{PP} = 12.5v \pm 0.5v)$



- Note 1. $V_{\mbox{CC}}$ must be applied simultaneously or before $V_{\mbox{PP}}$ and cut off simultaneously or after $V_{\mbox{PP}}$.
 - 2. Removing the device from socket and setting the device in socket with $V_{\rm PP}$ =12.5V may cause permanent damage to the device.
 - 3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

TC54256AP/AF

OPERATION INFORMATION

The TC54256AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE	PIN NAMES (NUMBER)	CE (20)	ŌĒ (22)	V _{PP} (1)	V _{CC} (28)	00 ∿ 07 (11 ∿ 13, 15 ∿ 19)	POWER	
Road Operation	Read	L	L			Data Out	Active	
Read Operation (Ta=-40 ∿ 85°C)	Output Deselect	*	Н	5V	5V	High Impedance	ACCIVE	
,	Standby	Н	*			High Impedance	Standby	
Program Operation	Program	L	Н			Data In		
(Ta=25±5°C)	Program Inhibit	Н	Н	12.5V	12.5V 6V	High Impedance	Active	
,	Program Verify	*	L			Data Out		

Note: H; V_{TH}, L; V_{TL}, *; V_{TH} or V_{TL}

READ MODE

The TC54256AP/AF has two control functions. The chip enable $(\overline{\text{CE}})$ controls the operation power and should be used for device selection. The output enable $(\overline{\text{OE}})$ controls the output buffers, independent of device selection. Assuming that $\overline{\text{CE}}=\overline{\text{OE}}=\text{V}_{\text{IL}}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{\text{CE}}=\text{V}_{\text{IL}}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}}=\text{V}_{\text{IH}}$ or $\overline{\text{OE}}=\text{V}_{\text{IH}}$, the outputs will be in a high impedance state. So two or more TC54256AP/AF's can be connected together on a common bus line. When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC54256AP/AF has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC54256AP/AF is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (VCC) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC54256AP/AF are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The TC54256AP/AF is in the programming mode when the Vpp input is at 12.5V and $\overline{\text{CE}}$ is at TTL-Low level under $\overline{\text{OE}}$ =V_{TH}.

The TC54256AP/AF can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with \overline{OE} at V_{TL} and \overline{CE} at V_{TH} or V_{TL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to Vpp terminal, a TTL high level \overline{CE} input inhibits the TC54256AP/AF from being programmed. Programming of two or more TC54256AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for \overline{CE} and \overline{OE} may be commonly connected, and a TTL Low level program pulse is applied to the \overline{CE} of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

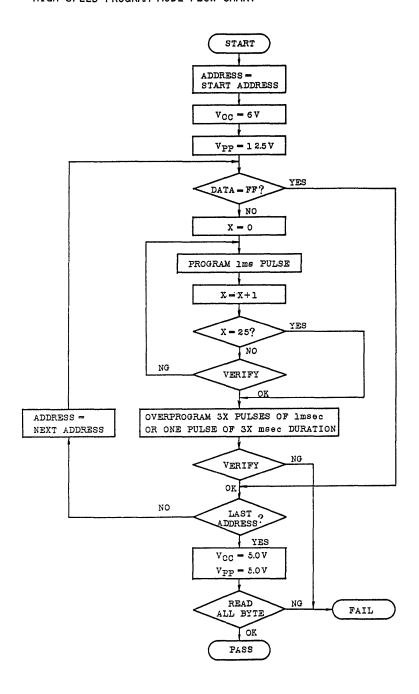
The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the Vpp terminal with Vcc=6V.

The programming is achieved by applying a single TTL low level lms pulse to the $\overline{\text{CE}}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of lms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied. When programming has been completed, the data in all addresses should be verified with $V_{\rm CC}=V_{\rm PP}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC54256AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC54256AP/AF by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

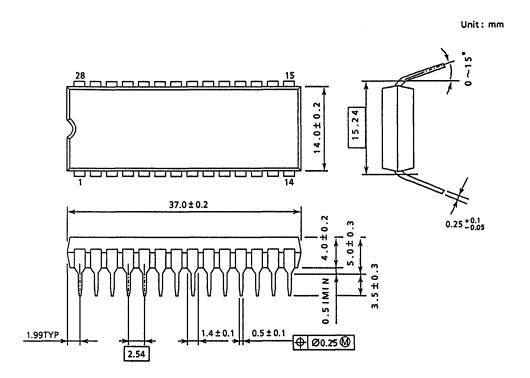
Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to $V_{\rm IL}$ in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to $V_{\rm IH}$. These two codes possess an odd parity with the parity bit of MSB (07). The following table shows electric signature of TC54256AP/AF.

PIN	1 ' '	07	06	05	04	03	02	01	00	HEX.
SIGNATURE	(10)	(19)	(18)	(17)	(16)	(15)	(13)	(12)	(11)	DATA
Manufacture Cod	le VIL	1	0	0	1	1	0	0	0	98
Device Code	VIH	1	1	0	0	0	1	0	0	C4

Notes: A9=12V±0.5V

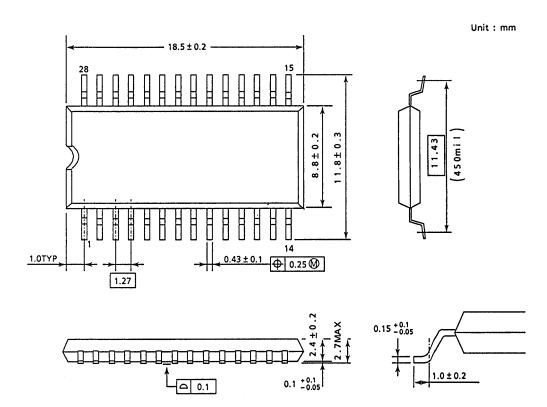
A1 \sim A8, A10 \sim A14, \overline{CE} , \overline{OE} = V_{TL}

OUTLINE DRAWINGS DIP28-P-600



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS SOP28-P-450



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

65,536 WORDS x 8 BITS CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC54512AP/AF is a 65,536 word \times 8 bit CMOS one time programmable read only memory, and molded in a 28 pin plastic package. For read operation, the TC54512AP/AF's access time is 150ns/200ns, and the TC54512AP/AF operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{\text{CE}}$ input. Advanced CMOS technology reduces the maximum active current to 30mA/5.9MHz and standby current to 100 μ A. The electrical characteristics and programming method are the same as U.V. EPROM TC57512AD's. Once programmed, the TC54512AP/AF cannot be erased because of using plastic DIP without transparent window.

FEATURES

- Peripheral circuit: CMOS Memory cell : N-MOS
- Fast access time: TC54512AP/AF-15 150ns TC54512AP/AF-20 200ns
- Low power dissipation Active : 30mA/5.9MHz Standby: 100µA
- · Full static operation

•	High	speed	programming	mode	I.	I
	6	ppeca	51021 ammiting	mouc	~,	-

- Inputs and outputs TTL compatible
- Standard 28 pin DIP plastic package: TC54512AP
 28 pin plastic Flat Package : TC54512AF

PIN	CON	٧E	CTION	(T	OP	VIEW)
					1	
	A15		1	28	Þ	v_{cc}
	A12		2	27	þ	A14
	A7		3	26	Þ	A13
	A6		4	25	Þ	A8
	A 5		5	24	Þ	A9
	A4		6	23	Þ	A11
	A3		7	22	Þ	ŌĒ∕V _{PP}
	A2		8	21	þ	A10
	Al		9	20	Ь	CE
	A0		10	19	Ь	07
	00		11	18	Ь	06
	01		12	17	Ь	O5
	02		13	16	Þ	04
	GND	d	14	15	Þ	03
					,	

V _{PP} GND V _{CC} OE OE, CE CIRCUIT	00 01 02 03 04 05 06 07
A0 0 0 6 COLUMN DECODE A1 0 DECODE A1 0 DECODE A1 1 0 DECO	CIRCUIT V 1.024 ME MORY CELL ARRAY

PIN NAMES

TIN WAILS								
A0 ∿ A15	Address Inputs							
00 ∿ 07	Outputs (Inputs)							
CE	Chip Enable Input							
OE/V _{PP}	Output Program Enable Supply Input Voltage							
v _{CC}	Power Supply Voltage (+5V)							
GND	Ground							

MODE SELECTION					
PIN	CE	OE/Vpp		00 ∿ 07	POWER
MODE	(20)	(22)	(28)	$(11 \lor 13, 15 \lor 19)$	1001
Read	L	L		Data Out	Active
Output Deselect	*	H	5V	High Impedance	ACLIVE
Standby	H	*		High Impedance	Standby
Program	L	Vpp	6v ¹)	Data In	
Program Inhibit	H	VPP	2)	High Impedance	Active
Program Verify	L	L	6.25V	Data Out	

*: H or L 1): HIGH SPEED PROGRAMMING MODE I

2): HIGH SPEED PROGRAMMING MODE II

MODE SELECTION

TC54512AP-15, TC54512AP-20 TC54512AF-15, TC54512AF-20

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
[∇] CC	V _{CC} Power Supply Voltage	-0.6 ~7.0	v
VPP	Program Supply Voltage	-0.6 ∿14.0	v
VIN	Input Voltage	-0.6 ~7.0	v
V _{I/0}	Input/Output Voltage	-0.6 ~ V _{CC} +0.5	v
PD	Power Dissipation	1.5	W
TSOLDER	Soldering Temperature Time	260 - 10	°C·sec
TSTG	Storage Temperature	-65 ∿125	°c
TOPR	Operating Temperature	-40 ∿85	°c

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC54512AP/AF-15/TC54512AP/AF-20
Ta	Operating Temperature	-40 ∿ 85°C
v _{CC}	V _{CC} Power Supply Voltage	5V±5%

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDI	TION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0 ~ V _C	V _{IN} =0 ∿ V _{CC}		-	±10	μA
ILO	Output Leakage Current	V _{OUT} =0.4 Λ	V _{OUT} =0.4 ∿V _{CC}		-	±10	μA
ICC01	Onematine Comment	CE=0V	f=5.9MHz	-	-	30	mA
I _{CC02}	Operating Current	I _{OUT} =0mA	f=1MHz	-	-	15	1 11125
1 _{CCS1}	Standby Current	CE=VIH		-	-	1	mA
I _{CCS2}		CE=V _{CC} -0.2	2 v	-	-	·100	μA
v _{IH}	Input High Voltage	-		2.2	-	V _{CC} +0.3	٧
VIL	Input Low Voltage	-		-0.3	-	0.8	v
v _{oh}	Output High Voltage	I _{OH} =-400μA		2.4	-	-	V
v _{OL}	Output Low Voltage	I _{OL} =2.1mA		-	-	0.4	V
I _{PPI}	V _{PP} Current	V _{PP} =0 ∿V _C	₂ +0.6	-	-	±10	μA

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	TC54512AP/AF-15		TC54512AP/AF-20		IINTT
SIMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	MIN.	MAX.	UNII
tACC	Address Access Time	CE=OE=VIL	-	150	ı	200	ns
t _{CE}	CE to Output Valid	OE=VIL	-	150	-	200	ns
t _{OE}	OE to Output Valid	CE=VIL	-	70	-	70	ns
tDF1	CE to Output in High-Z	OE=VIL	0	60	0	60	ns
t _{DF2}	OE to Output in High-Z	CE=VIL	0	60	0	60	ns
^t OH	Output Data Hold Time	CE=OE=VIL	0	-	0	-	ns

A.C. TEST CONDITIONS

Output Load

: 1 TTL Gate and C_L =100pF

Input Pulse Rise and Fall Times

: 10ns Max.

Input Pulse Levels

: 0.45V ~ 2.4V

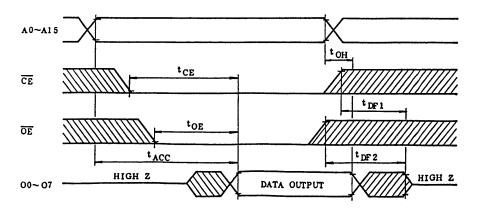
Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C _{IN1}	Input Capacitance	V _{IN=OV}	-	4	6	pF
C _{IN2}	OE/Vpp Input Capacitance	v _{IN} =0v	_	50	60	pF
COUT	Output Capacitance	V _{OUT} =V	-	8	12	pF

^{*} This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



TC54512AP-15, TC54512AP-20 TC54512AF-15, TC54512AF-20

HIGH SPEED PROGRAM MODE I

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
v _{IH}	Input High Voltage	2.2	-	Vcc+1.0	V
VIL	Input Low Voltage	-0.3	-	0.8	V
v _{cc}	VCC Power Supply Voltage	5.75	6.0	6.25	V
V _{PP}	Vpp Power Supply Voltage	12.0	12.5	13.0	v

DC and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ILI	Input Current	V _{IN} =0 ~V _{CC}	-		±10	μA
v _{oh}	Output High Voltage	I _{OH} =-400μA	2.4	-	-	V
v _{OL}	Output Low Voltage	I _{OL} =2.1mA	-	-	0.4	V
ICC	V _{CC} Supply Current	-	-	-	30	mA
I _{PP2}	Vpp Supply Current	Vpp=13.0V	-	-	50	mA.

AC PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
^t AS	Address Setup Time	-	2	_	-	μs
t _{AH}	Address Hold Time	-	2	_	-	μs
tOES	OE/V _{PP} Setup Time	-	2		_	μs
^t OEH	OE/V _{PP} Hold Time	-	2	_	-	μs
tPRT	OE/V _{PP} Pulse Rise Time	-	50	_	-	ns
tDS	Data Setup Time	-	2	_	-	μs
t _{DH}	Data Hold Time	-	2	_	-	μs
tVR	OE/Vpp Recovery Time	-	2	-	-	μs
tvcs	V _{CC} Setup Time	-	2	-	-	μs
t _{PW}	Initial Program Pulse Width	CE=VIL, OE/VPP=VPP	0.95	1.0	1.05	ms
tOPW	Overprogram Pulse Width	Note 1	2.85	3.0	78.75	ms
tDV	Data Valid from $\overline{\text{CE}}$	ŌE/Vpp=VIL	-	-	1	μs
t _{DF}	CE to Output in High-Z	OE/Vpp=VIL	_	_	130	ns

AC TEST CONDITIONS

• Output Load : 1 TTL Gate and C_L (100pF)

• Input Pulse Rise and Fall Times : 10ns Max. • Input Pulse Levels : 0.45V ∿ 2.4V

• Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

HIGH SPEED PROGRAM MODE II

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	V _{CC} +1.0	v
VIL	Input Low Voltage	-0.3	-	0.8	v
v _{CC}	V _{CC} Power Supply Voltage	6.0	6.25	6.5	v
V _{PP}	Vpp Power Supply Voltage	12.5	12.75	13.0	V

DC and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25v±0.25v, V_{PP}=12.75v±0.25v)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0 ~V _{CC}	-	-	±10	μA
v _{OH}	Output High Voltage	V _{OH} =-400μ A	2.4	-	-	v
V _{OL}	Output Low Voltage	I _{OL} =2.1mA	-	-	0.4	v
ICC	V _{CC} Supply Current	_	-	-	30	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} =13.0V	-	-	50	m.A.

AC PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)

SYMBOL	PAPAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	-	-	μs
t _{AH}	Address Hold Time	•	2		-	μs
toES	OE/Vpp Setup Time	-	2	-	_	μs
^t OEH	OE/V _{PP} Hold Time	-	2	-	_	μs
tPRI	\overline{OE}/Vpp Pulse Rise Time	-	50	-	-	ns
tDS	Data Setup Time	-	2		-	μs
t _{DH}	Data Hold Time	-	2	•	-	μs
t _{VR}	OE/Vpp Recovery Time	-	2	-	-	μs
tvcs	V _{CC} Setup Time	-	2	-	-	μs
tPW	Program Pulse Width	CE=VIL, OE/Vpp=Vpp	0.095	0.1	0.105	ms
t _{DV}	Data Valid from CE	OE/V _{PP} =V _{IL}	-	-	1	μs
tDF	CE to Output in High-Z	OE/VPP=VIL	-	_	130	ns

AC TEST CONDITIONS

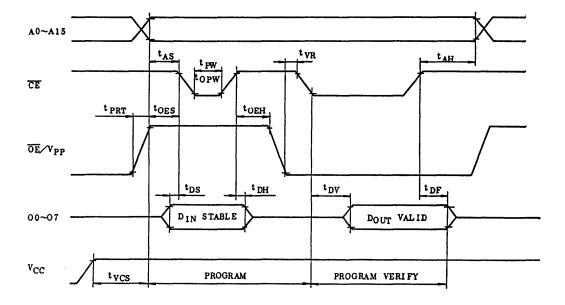
• Output Load : 1 TTL Gate and C_L (100pF)

• Input Pulse Rise and Fall Times : 10ns Max. • Input Pulse Levels : $0.45 \text{V} \sim 2.4 \text{V}$

Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAMMING MODE I (V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)
HIGH SPEED PROGRAMMING MODE II (V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)



- Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
 - 2. Removing the device from socket and setting the device in socket with $V_{\rm PP}=12.5\pm0.5V$ or $V_{\rm PP}=12.75\pm0.25V$ may cause permanent damage to the device.
 - 3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC54512AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE	N NAMES (NUMBER)	CE (20)	(22)	V _{PP} (1)	VCC (28)	00 ∿07 (11 ∿13, 15 ∿19)	POWER	
Part Ot	Read	L	L			Data Out		
Read Operation	Output Deselect	*	н	5v	5V	High Impedance	Active	
(Ta=-40 ∿85°C)	Standby	н	*	1		High Impedance	Standby	
Program Operation	Program	L	Н			Data In		
(Ta=25±5°C)	Program Inhibit	H	H	12.5V ¹⁾	6V ¹⁾	High Impedance	Active	
(1d-2)±) ()	Program Verify	*	L	12.75v ²⁾	6.25V	Data Out		

Note: H; V_{IH} , L; V_{IL} , *: V_{IH} or V_{IL} , 2); HIGH SPEED PROGRAM MODE II

READ MODE

The TC54512AP/AF has two control functions. The chip enable ($\overline{\text{CE}}$) controls the operation power and should be used for device selection. The output enable ($\overline{\text{OE}}$) control the output buffers, independent of device selection. Assuming that $\overline{\text{CE}}=\overline{\text{OE}}=\text{V}_{\text{IL}}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{\text{CE}}=\text{V}_{\text{IL}}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

TC54512AP-15, TC54512AP-20 TC54512AF-15, TC54512AF-20

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TC54512AP/AF's can be connected together on a common bus line. When \overline{CE} is decode for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC54512AP/AF has a low power standby mode controlled by the CE signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC54512AP/AF is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (VCC) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC54512AP/AF are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC54512AP/AF is in the programming mode when the $\overline{\text{OE}}/\text{Vpp}$ input is at 12.5V or 12.75V and $\overline{\text{CE}}$ is at TTL-Low level. The TC54512AP/AF can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{\text{OE}}/\text{Vpp}$ at V_{IL} and $\overline{\text{CE}}$ at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V or +12.75V) is applied to Vpp terminal, a high level $\overline{\text{CE}}$ input inhibits the TC54512AP/AF from being programmed. Programming of two or more TC54512AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for CE may be commonly connected, and a TTL low level program pulse is applied to the $\overline{\text{CE}}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE I

This high speed programming mode I is performed at $V_{CC}=6.0V$ and $\overline{\rm OE}/V_{PP}=12.5V$. The programming is achieved by applying a single TTL low level lms pulse to the $\overline{\rm CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of lms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with 3 times that needed for initial programming is applied.

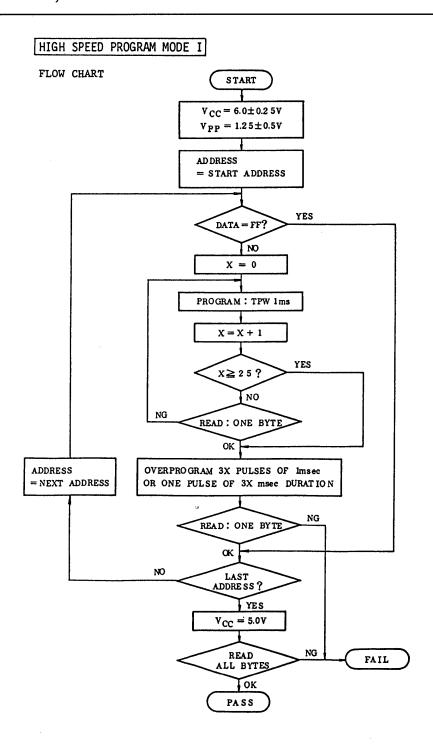
When programming has been completed, the data in all addresses should be verified with $V_{\rm CC}=5V$.

HIGH SPEED PROGRAM MODE II

The program time can be greatly decreased by using this high speed programming mode II. This high speed programming mode II is performed at $V_{CC}=6.25V$ and $\overline{OE}/V_{PP}=12.75V$. The programming is achieved by applying a single TTL low level 0.1ms pulse to the \overline{CE} input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

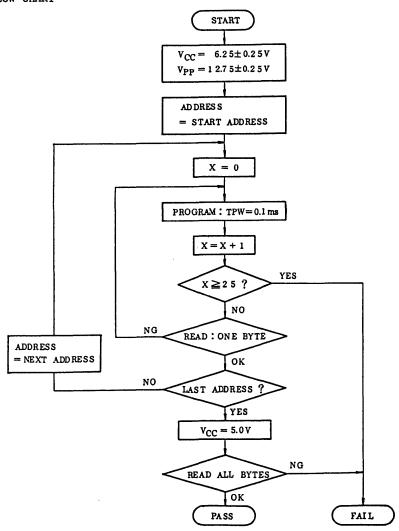
If the programmed data is not correct, another program pulse of 0.1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{CC}=5V$.



HIGH SPEED PROGRAM MODE II

FLOW CHART



TC54512AP-15, TC54512AP-20 TC54512AF-15, TC54512AF-20

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC54512AP/AF which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC54512AP/AF by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to $V_{\rm IL}$ in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to $V_{\rm IH}$. These two codes possess an odd parity with the parity bit of MSB (07). The following table shows electric signature of TC54512AP/AF.

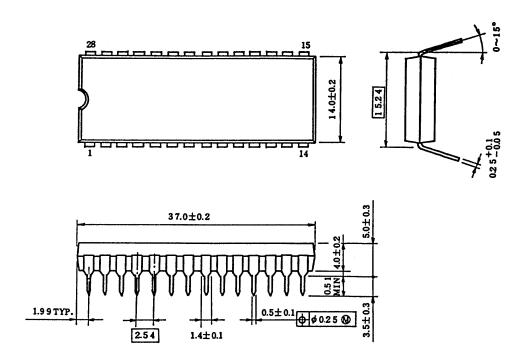
PINS SIGNATURE	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacture Code	VIL	1	0	0	1	1	0	0	0	98
Device Code	v _{IH}	1	0	0	0	0	1	0	1	85

Notes: A9=12V±0.5V

A1 \sim A8, A10 \sim A15, \overline{CE} , \overline{OE} = V_{IL}

OUTLINE DRAWINGS (TC54512AP) DIP28-P-600

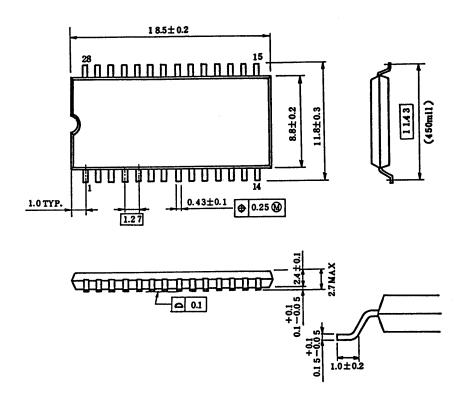
Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS (TC54512AF) SOP28-P-450

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

131,072 WORD x 8 BIT CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC541000J/TC541001J is a 131,072 word × 8 bit one time programmable read only memory, and molded in a 32 pin plastic package.

The TC541000J/TC541001J's access time is 150ns/200ns and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TC571000D/TC571001D's. Once programmed, the TC541000J/TC541001J cannot be erased because of using plastic package without transparent window.

FEATURES

• Peripheral circuit: CMOS

Memory cell

: N-MOS

· Access Time

	-15	-20
Temp	0~70°C	-40~85°C
TACC	150ns	200ns

· Low power dissipation

Active: 30mA/6.7MHzStandby: $100\mu A$ (Ta=85°C)

- Single 5V power supply
- · Full static operation
- · High speed programming operation: tpw 0.1ms
- · Input and output TTL compatible
- · Standard 32 pin DIP plastic package

PIN CONNECTION (TOP VIEW)

V _{PP} t	$_{1}$. \bigcirc	32	P <u>vcc</u>	V _{PP} [, 0	32	vcc
A16 [31	PGM	OE C			PGM
A1 5 🕻	3	30	DNC	A1 5 [3	30	PNC
A12[4	29	DA14	A12[4	29	DA14
A7 [5	28	DA13	A7 [5	28	1A13
A6 [6	27	JA8	A6 [6	27	8A¢
A5 [7	26	JA9	A5 [7	26	PA9
A4 [JA11	A4 [8	25	DA11
A3 [9	24	JOE	A3E	9	24	JA16
A2[1A10	A2[10	23	JA10
A1 [11	22	DCE	Ald	11	22	DCE
VO C	12	21	D7	AOD	12	21	D7
D0 d	13	20	D6	DO C	13	20	1 D6
DIQ	14	19	D5	D1 d	14	19	D5
D2 (D14	D21	15	18	D4
GNDd	16	17	1D3	GNDI	16	17	D3
1	C5410	ooj		:	C5410	01J	

	(Refer	en	e)
A15 C A12 C A7 C A6 C A3 C A1 C A0 C D0 C	1 2 3 4 5 6 7 8 9 10 11 12	28 27 26 25 24 23 22 21 20 19 18	PVCC HA14 HA13 HA8 HA9 HA11 HA16 HA10 HA10 HA10 HA10 HA10
GND	<u> </u>	_	роз
. 1 N	/ MASK	RC	M .

(1M MASK ROM TC531000P

PIN NAMES

A0~A16	Address Inputs
D0∿D7	Outputs (Inputs)
CE	Chip Enable Input
ŌĒ	Output Enable Input
PGM	Program Control Input
v _{CC}	V _{CC} Supply Voltage
V _{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	V _{CC} +0.3	
VIL	Input Low Voltage	-0.3	-	0.8	7
V _{CC}	VCC Power Supply Voltage	4.75	5.00	5.25	7 °
Vpp	VPP Power Supply Voltage	V _{CC} -0.6	VCC	V _{CC} +0.6	

DC and OPERATING CHARACTERISTICS (Ta=-40 $^{\circ}$ 85 $^{\circ}$ C, V_{CC} =5 $V\pm5\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0 ~ V _{CC}		-	-	±10	μA
ICC01	0	CE =0V	f=6.7MHz	-	-	30	mA.
I _{CCO2}	Operating Current	I _{OUT} =OmA	f=1MHz	_	-	10	
ICCS1	Ch 11 C	CE=VIH		-	-	1	mA
I _{CCS2}	Standby Current	CE=V _{CC} -0.	2V	-	-	100	μA
VOH	Output High Voltage	I _{OH} =-400μ	A	2.4	-	-	V
VOL	Output Low Voltage	I _{OL} =2.1mA		_	-	0.4	v
IPP1	V _{PP} Current	V _{PP} =V _{CC} ±0.6V		-	-	±10	μA
ILO	Output Leakage Current	V _{OUT} =0.4V ∿ V _{CC}		-	-	±10	μА

 $Ta=0 \sim 70^{\circ}C$ for TC541000 J/TC541001 J-15

AC CHARACTERISTICS (Ta=-40 \sim 85°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

SYMBOL	PARAMETER	TC541000		TC54100	0 <i>3</i> /1001 <i>3</i> 20	UNIT
	* *************************************	MIN.	MAX.	MIN.	MAX.	01111
tACC	Address Access Time	-	150	-	200	
tCE	CE to Output Vaild	-	150	-	200	
toE	OE to Output Vaild	_	70	_	70	
t_{PGM}	PGM to Output Vaild	_	70	-	70	ns
t _{DF1}	CE to Output in High-Z	0	60	0	60	
tDF2	OE to Output in High-Z	0	60	0	60	
t _{DF3}	PGM to Output in High-Z	0	60	0	60	
tон	Output Data Hold Time	0	-	0	_	

 $Ta = 0 \sim 70^{\circ}C$ for TC541000J/TC541001J-15

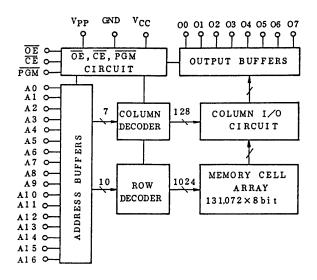
AC TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L =100pF

• Input Pulse Rise and Fall Time : 10ns Max. • Input Pulse Levels : 0.45V to 2.4V

• Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

BLOCK DIAGRAM



MODE SELECTION

MODE	PGM	CE	ŌĒ	v _{PP}	v _{CC}	00 ∿ 07	POWER
Read	Н	L	L			Data Out	Active
Output Deselect	*	*	Н	5V	5V	High Impedance	ACCIVE
Standby	*	Н	*	i		High Impedance	Standby
Program	L	L	Н			Data In	
Program Inhibit	*	н	*	12.750	6.25V	High Impedance	1
riogram innibit	Н	L	Н	12.75	0.23	High Impedance	Active
Program Verify	H	L	L			Data Out]

^{*:} H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
VCC	VCC Power Supply Voltage	-0.6 ∿ 7.0	v
VPP	Program Supply Voltage	-0.6 ∿ 14.0	v
VIN	Input Voltage	-0.6 ~ 7.0	v
V _I /O	Input/Output Voltage	-0.6 ~ V _{CC} +0.5	v
PD	Power Dissipation	1.0	W
TSOLDER	Soldering Temperature . Time	260 • 10	°C•sec
TSTRG	Storage Temperature	-65 ∿ 125	°C
TOPR	Operating Temperature	-40 ∿ 85	°C

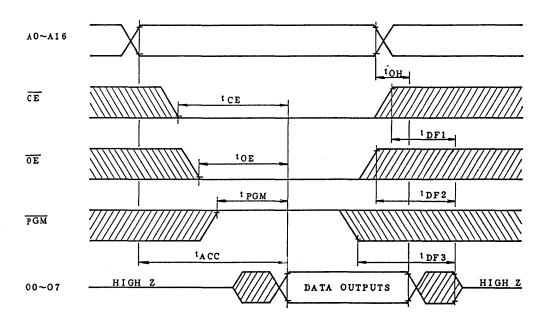
TC541000J-15, TC541000J-20 TC541001J-15, TC541001J-20

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CIN	Input Capacitance	V _{IN} =OV	-	4	8	рF
C _{OUT}	Output Capacitance	V _{OUT} =0V	-	10	12	PΓ

^{*} This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	V _{CC} +1.0	
VIL	Input Low Voltage	-0.3	-	0.8	**
v _{CC}	V _{CC} Power Supply Voltage	6.00	6.25	6.50	V
V _{PP}	Vpp Power Supply Voltage	12.50	12.75	13.00	

DC AND OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ILI	Input Current	V _{IN} =0 ~ V _{CC}	-	-	±10	μA
V _{OH}	Output High Voltage	I _{OH} =-400μA	2.4	-	-	v
V _{OL}	Output Low Voltage	I _{OL} =2.1mA	-	-	0.4	V
ICC	V _{CC} Supply Current	-	-	-	30	mA
Ipp2	VPP Supply Current	V _{PP} =13.0V	_	-	50	mA

AC PROGRAMMING CHARACTERISTICS (Ta=25 \pm 5°C, V_{CC} =6.25 \pm 0.25V, V_{PP} =12.75 \pm 0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	-	-	μs
tAH	Address Hold Time	-	2	_	_	μs
t _{CES}	CE Setup Time	-	2	-	-	μs
^t CEH	CE Hold Time	-	2	-	-	μs:
t _{DS}	Data Setup Time	-	2	-	-	μs
t _{DH}	Data Hold Time	-	2	-	-	μs
t _{VS}	Vpp Setup Time	-	2	-	-	μs
t _{PW}	Program Pulse Width	-	0.095	0.1	0.105	ms
tOE	OE to Output Valid	-	-	-	100	ns
t _{DF2}	OE to Output in High-Z	CE=VIL	-	-	90	ns

AC TEST CONDITIONS

• Output Load : 1 TTL Gate and C_L (100pF)

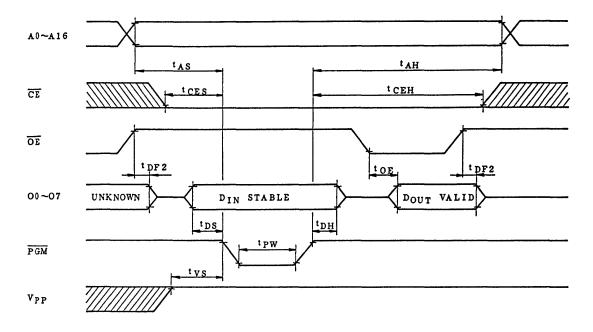
• Input Pulse Rise and Fall Time : 10ns Max.

• Input Pulse Levels : 0.45V and 2.4V

• Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

- 2. Removing the device from socket and setting the device in socket with Vpp=12.75V may cause permanent damage to the device.
- 3. The Vpp supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the Vpp terminal. When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC541000J/TC541001J's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

	PINS	PGM	CE	ŌĒ	v _{PP}	v _{cc}	00 ∿ 07	POWER
READ OPERATION (Ta=-40 ~ 85°C)	Read	н	L	L			Data Out	Active
	Output Deselect	*	*	H	5V	5V	High Impedance	
	Standby	*	Н	*	1		High Impedance	Standby
PROGRAM	Program	L	L	Н			Data In	
OPERATION	Danasaa Tabibis	*	H	*			High Impedance	
(Ta=25±5°C)	Program Inhibit	Н	L	Н	12.75V	6.25V	High Impedance	Active
	Program Verify	Н	L	L			Data Out	

Note: H; V_{IH} , L; V_{IL} , *; V_{IH} or V_{IL} $Ta=0 \sim 70$ °C for TC541000J/TC574001J-15

READ MODE

The TC541000J/TC541001J has three control functions. The chip enable (\overline{CE}) controls the operation power and should be used for device selection.

The output enable (\overline{OE}) and the program control (\overline{PGM}) control the output buffers, independent of device selection.

Assuming in that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{\text{CE}}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{\text{CE}}=\text{V}_{\text{IL}}$, $\overline{\text{PGM}}=\text{V}_{\text{IH}}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{\text{OE}}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of \overline{PGM} .

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}}=V_{\text{IH}}$ or $\overline{\text{OE}}=V_{\text{IH}}$, the outputs will be in a high impedance state.

So two or more ROMs can be connected together on a common bus line.

When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

TC541000J-15, TC541000J-20 TC541001J-15, TC541001J-20

STANDBY MODE

The TC541000J/TC541001J has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC541000J/TC541001J is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (VCC) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC541000J/TC541001J are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC541000J/TC541001J can be programmed any location at anytime ----- either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{\text{OE}}$ and $\overline{\text{CE}}$ at V_{TL} and PGM at V_{TH} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level \overline{CE} or \overline{PGM} input inhibits the TC541000J/TC541001J from being programmed. Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for \overline{CE} or \overline{PGM} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} and \overline{PGM} of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

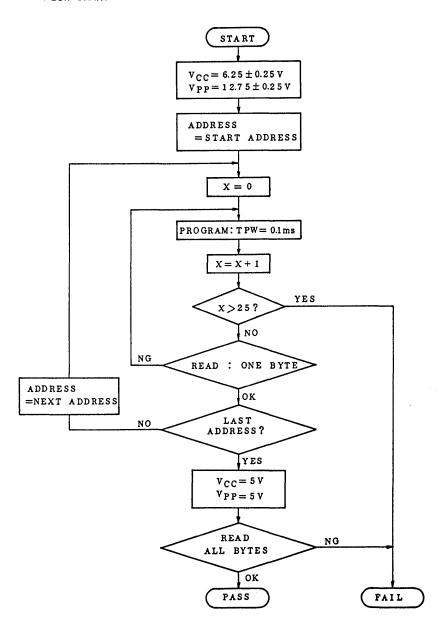
The device is set up in the high speed programming mode when the programming voltage ($\pm 12.75V$) is applied to the Vpp terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{TH}$.

The programming is achieved by applying a single TTL low level 0.lms pulse the \overline{PGM} input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{\rm CC} = V_{\rm PP} = 5V$.

HIGH SPEED PROGRAM OPERATION FLOW CHART



C541000J-15, TC541000J-20 C541001J-15, TC541001J-20

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC541000J/TC541001J which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC541000J/TC541001J by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to $V_{\rm IL}$ in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to $V_{\rm IH}$. These two codes possess an odd parity with the parity bit of MSB (07). The following table shows electric signature of TC541000J/TC541001J.

SIGNATURE	PINS	A0	07	06	05	04	03	02	01	00	HEX DATA
Manufacture Co	VIL	1	0	0	1	1	0	0	0	98	
D	TC541000J	37	1	0	0	0	0	1	1	0	86
Device Code	TC541001J	VIH	0	0	0	0	0	1	1	1	07

Notes: $A9=12V\pm0.5V$

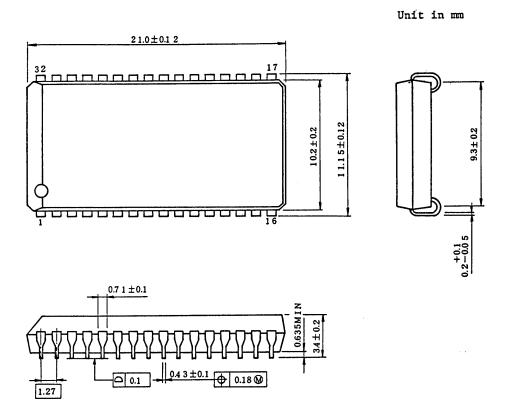
A1 \sim A8, A10 \sim A16, \overline{CE} , \overline{OE} = V_{TL}

PGM=V_{IH}

OUTLINE DRAWINGS

(S0J32-P-400)

Plastic SOJ



Note: Each lead pitch is $1.27 \, \mathrm{mm}$.

All dimensions are in millimeters.

131,072 WORD x 8 BIT CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC541000P/F and TC541001P/F are a 131,072 word x 8 bit one time programmable read only memory and molded in a 32 pin plastic package.

The TC541000P/F and TC541001P/F's access time are 150ns/200ns and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TC571000D/TC571001D's. Once programmed, the TC541000P/F and TC541001P/F cannot be erased because of using plastic package without transparent window.

FEATURES

Peripheral circuit : CMOS
 Memory cell : N-MOS

• Access Time

	15	- 20
Temp	0~70°C	- 40~85℃
tacc	150ns	200ns

• Low power dissipation

Active : 30mA/6.7MHz Standby : 100µA • Single 5V power supply

• Full static operation

• High speed programming operation : tpw 0.1ms

• Input and output TTL compatible

JEDEC standard 32 pin : TC541000P/F
1M MROM compatible : TC541001P/F

• Standard 32 pin DIP plastic package: TC541000P/TC541001P

• S32Pin Plastic Flat Package: TC541000F/TC541001F

PIN CONNECTION (TOP VIEW)

	~			$\overline{}$			
V _{PP} [1	32	V _{CC} V _{PP}	[1	32]] V _{CC}		(D - (
A16 [2	31]	PGM ŌĒ	d 2	31] PGM		(Refere	nce)
A15 [3	30	NC A15	[3	30] NC	A15	d 1	28] V _{CC}
A12 [4	29]	A14 A12	d 4	29] A14	A12	[2	27] A14
A7 [5	28].	A13 A7	d 5	28]A13	Α7	[3	26] A13
A6 [6	27].	A8 A6	[6	27] A8	Α6	[4	25]] A8
A5 [7	26]	A9 A5	d 7	26] A9	A5	d 5	24 A9
A4 [8	25]	A11 A4	8	25]A11	A4	[6	23]A11
A3 [9	24]	ŌĒ A3	d 9	24] A16	Α3	[7	22]] A 16
A2 [10	23].	A10 A2	[10	23] A10	A2	[8	21 A10
A1 [11	22]	ČË A1	d 11	22] CE	A1	[9	20] ČĒ
A0 [12	21	D7 A0	[12	21 07	A0	[10	19] D7
D0 [13	20	D6 D0	[13	20] D6	D0	[11	18] D6
D1 [14	19	D5 D1	d 14	19D5	D1	[12	17] D5
D2 [15	18	D4 D2	[15	18] D4	D2	[13	16] D4
GND (16	17	D3 GND	16	17] D3	GND	[14	15] 03
TC54	11000P/F	,	TC541	001P/F	(IM M	

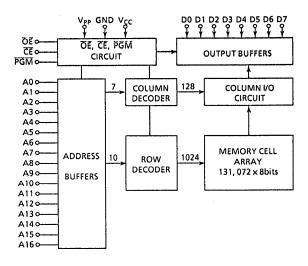
PIN NAMES

A0~A16	Address Inputs
D0~D7	Outputs (Inputs)
ČĒ	Chip Enable Input
ŌĒ	Output Enable Input
PĞM	Program Control Input
Vcc	V _{CC} Supply Voltage
V _{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

TC531000P

TC541000P/F-15, TC541000P/F-20 TC541001P/F-15, TC541001P/F-20

BLOCK DIAGRAM



MODE SELECTION

MODE	N PGM	ζĒ	ŌĒ	V _{PP}	V _{CC}	D0~D7	Power	
Read	н	L	L			Data Out		
Output Deselect	•	*	н	5V 5	5V	High Impedance	Active	
Standby	* Н *		High Impedance	Standby				
Program	L	L	н			Data In		
B			*	12.75V	6.25V	High Impedance	Active	
Program Inhibit	н	L	н	12.73	ÿ.25 V	High Impedance		
Program Verify	н	L	L			Data Out		

^{*} II or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	- 0.6~7.0	V
V _{PP}	Program Supply Voltage	-0.6~14.0	v
V _{IN}	Input Voltage	- 0.6~7.0	v
V _{I/O}	Input/Output Voltage	- 0.6~V _{CC} + 0.5	v
PD	Power Dissipation	1.0	w
T _{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T _{STRG}	Storage Temperature	- 65~125	•€
TOPR	Operating Temperature	- 40~85	°c

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	TINU
V _{IH}	Input High Voltage	2.2	_	V _{CC} + 0.3	٧
VIL	Input Low Voltage	- 0.3	-	0.8	٧
V _{CC}	V _{CC} Power Supply Voltage	4.75	5.00	5.25	>
V _{PP}	V _{PP} Power Supply Voltage	V _{CC} - 0.6V	V _{CC}	V _{CC} ~ 0.6	٧

D.C. AND OPERATING CHARACTERISTICS (Ta = $-40 \sim 85\%$, $V_{CC} = 5V \pm 5\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
lεi	Input Current	V _{IN} = 0~V _{CC}		-	-	± 10	μΑ
lcco1		ČĒ = 0V	f = 6.7 _{MHz}	-	-	30	mA
l _{CCO2}	Operating Current	I _{OUT} = 0mA	f = 1 _{MHz}	-	-	10	mA
I _{CCS1}		ČĒ = VIH		-	-	1	mA
I _{CCS2}	Standby Current	ĈĒ = V _{CC} - 0.2	2V	-	_	100	μA
V _{OH}	Output High Voltage	I _{OH} = - 400μ	Δ	2.4	_	-	V
Vol	Output Low Voltage	I _{OL} = 2.1mA		_	_	€0.4	V
l _{PP1}	V _{PP} Current	$V_{PP} = V_{CC} \pm 0.6V$		_		± 10	μΑ
ILO	Output Leakage Current	V _{OUT} = 0.4V~	-V _{CC}	_	-	± 10	μА

 $Ta = 0 \sim 70^{\circ}C$ for TC541000P/F/TC541001P/F - 15

A.C. CHARACTERISTICS (Ta = $-40 \sim 85^{\circ}$ C, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC} \pm 0.6V$)

		TC541000P - 157		TC541000P - 207	UNIT	
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	
t _{ACC}	Address Access Time	-	150	-	200	ns
t _{CE}	ČĒ to Output Valid	-	150	_	200	ns
t _{Oξ}	ŌË to Output Valid	-	70	-	70	ns
t _{PGM}	PGM to Output Valid		70	-	70	ns
t _{DF1}	CE to Output in High-Z	0	60	0	60	ns
t _{DF2}	OE to Output in High-Z	0	60	0	60	ns
t _{DF3}	PGM to Output in High-Z	0	60	0	60	ns
ton	Output Data Hold Time	0	_	0	-	ns

 $Ta = 0 \sim 70^{\circ}C$ for TC541000P/F/TC541001P/F - 15

A.C. TEST CONDITIONS

Output Load
 : 1 TTL Gate and C_L=100pF

Input Pulse Rise and Fall Time
 Input Pulse Levels
 10ns Max.
 0.45V to 2.4V

Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

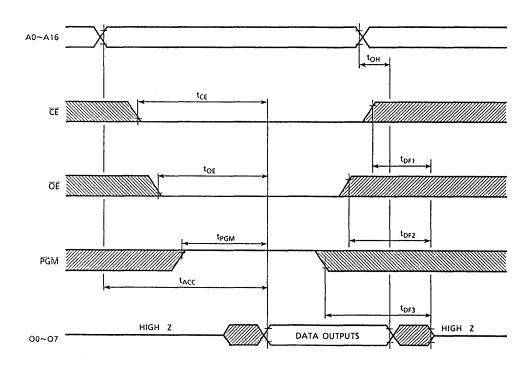
TC541000P/F-15, TC541000P/F-20 TC541001P/F-15, TC541001P/F-20

CAPACITANCE* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	-	4	8	рF
Cout	Output Capacitance	V _{OUT} = 0V	_	10	12	pF

This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} + 1.0	V
VIL	Input Low Voltage	- 0.3	-	0.8	٧
V _{CC}	V _{CC} Power Supply Voltage	6.00	6.25	6.50	٧
V _{PP}	V _{PP} Power Supply Voltage	12.50	12.75	13.00	V

D.C. AND OPERATING CHARACTERISTICS ($Ta = 25 \pm 5^{\circ}C$, $V_{CC} = 6.25 \pm 0.25V$, $V_{PP} = 12.75 \pm 0.25V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
lu	Input Current	V _{IN} = 0~V _{CC}	-	-	± 10	μА
V _{OH}	Output High Voltage	I _{OH} = - 400μA	2.4	-	_	V
VOL	Output Low Voltage	l _{OL} = 2.1mA	-	-	0.4	V
lcc	V _{CC} Supply Current	-		-	30	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} = 13.0V	-	-	50	mA

A.C. PROGRAMMING CHARACTERISTICS (Ta = $25 \pm 5^{\circ}$ C, $V_{CC} = 6.25 \pm 0.25$ V, $V_{PP} = 12.75 \pm 0.25$ V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	_	-	μs
t _{AH}	Address Hold Time	-	2	-	_	μs
t _{CES}	CE Setup Time	-	2	-	-	μς
t _{CEH}	CE Hold Time	-	2	-	-	μs
t _{DS}	Data Setup Time	-	2	-	-	μs
t _{DH}	Data Hold Time	_	2	_	-	μs
t _{VS}	V _{PP} Setup Time	-	2	-	-	μς
t _{PVV}	Program Pulse Width	-	0.095	0.1	0.105	ms
toe	ÖE to Output Valid	-	-	-	100	ns
t _{DF2}	OĒ to Output in High-Z	CE = VIL	-	_	90	ns

A.C. TEST CONDITIONS

Output Load

: 1 TTL Gate and C_L (100pF)

• Input Pulse Rise and Fall Time

: 10ns Max.

• Input Pulse Levels

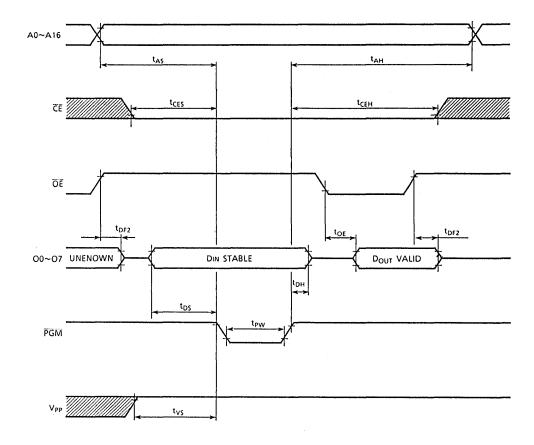
: 0.45V and 2.4V

• Timing Measurement Reference Level

: Input 0.8V and 2.2V, Output 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



Note: 1. VCC must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.

- 2. Removing the device from socket and setting the device in socket with Vpp=12.75V may cause permanent damage to the device.
- 3. The VPP supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the VPP terminal. When the switching pulse voltage is applied to the VPP terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC541000P/F/TC541001P/F's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

		PGM	CE	ŌĒ	V _{PP}	V _{cc}	00~07	Power	
READ	Read	н	L	L			Data Out		
OPERATION	Output Deselect	*	*	Н	5∨	5∨	High Impedance	Active	
	Standby	*	н	*			High Impedance	Standby	
PROGRAM	Program	L	L)	н			Data In		
OPERATION		*	Η	*			High Impedance		
	Program Inhibit	н	L	н	12.75V 6.25V	6.25V	6.250	High Impedance	Active
(Ta = 25 ± 5°C)	Program Verify	н	L	L			Data Out		

Note: H; VIII, L; VIII, *; VIII or VIII.

READ MODE

The TC541000P/F/TC541001P/F has three control functions. The chip enable (\overline{CE}) controls the operation power and should be used for device selection.

The output enable (\overline{OE}) and the program control (\overline{PGM}) control the output buffers independent of device selection.

Assuming in that $\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$ and $\overline{\text{PGM}} = V_{III}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{\text{CE}}$ to output valid (tce) is equal to the address access time (tacc).

Assuming that $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{III}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of \overline{OE} .

And assuming that $\overline{CE} = \overline{OE} = V_{1L}$, and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of \overline{PGM} .

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{III}$ or $\overline{OE} = V_{III}$, the outputs will be in a high impedance state.

So two or more ROMs can be connected together on a common bus line.

When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

TC541000P/F-15, TC541000P/F-20 TC541001P/F-15, TC541001P/F-20

STANDBY MODE

The TC541000P/F/TC541001P/F has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC541000P/F/TC541001P/F is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC541000P/F/TC541001P/F are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC541000P/F/TC541001P/F can be programmed any location at anytime - either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with \overline{OE} and \overline{CE} at V_{IL} and \overline{PGM} at V_{III} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to Vpp terminal, a high level $\overline{\text{CE}}$ or $\overline{\text{PGM}}$ input inhibits the TC541000P/F/TC541001P/F from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for \overline{CE} or \overline{PGM} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} and \overline{PGM} of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with $V_{CC}=6.25V$ and $\overline{PGM}=V_{III}$.

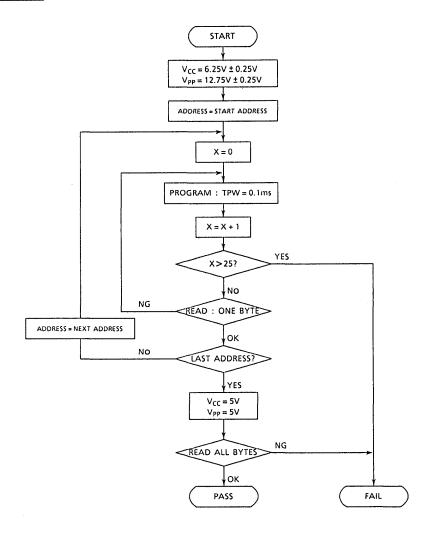
The programming is achieved by applying a single TTL low level 0.1ms pulse the <u>PGM</u> input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{\rm CC} = V_{\rm PP} = 5V$.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



TC541000P/F-15, TC541000P/F-20 TC541001P/F-15, TC541001P/F-20

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC541000P/F/TC541001P/F which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC541000P/F/TC541001P/F by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH} . These two codes possess an odd parity with the parity bit of MSB (07).

The following table shows electric signature of TC541000P/F/TC541001P/F.

SIGNATURE	PINS	Α0	07	06	O5	04	О3	O2	01	00	HEX. DATA
Manufacture Code		V _{IL}	1	0	0	1	1	0	0	0	98
TC541000P/F			1	0	0	0	0	1	1	0	86
Device Code	TC541001P/F	V _{IH}	0	0	0	0	0	1	1 .	., 1	07

Notes: $A9 = 12V \pm 0.5V$

A1~A8, A10~A16, \overline{CE} , $\overline{OE} = V_{1L}$

 $\overline{PGM} = V_{III}$

Unit: mm

OUTLINE DRAWINGS

• Plastic DIP

DIP32-P-600

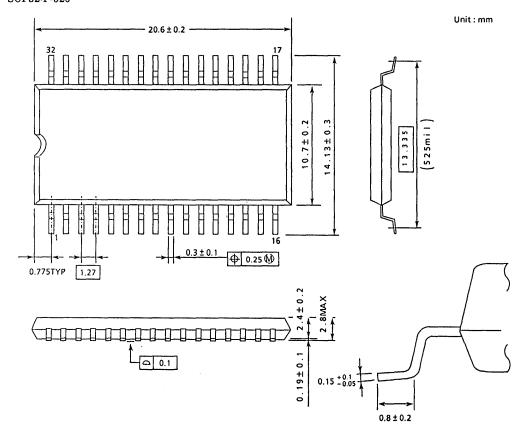
Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm

TC541000P/F-15, TC541000P/F-20 TC541001P/F-15, TC541001P/F-20

OUTLINE DRAWINGS

• Plastic SOP

SOP32-P-525



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm

524,288 WORD x 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC544000P/F is a 524,288 word × 8 bit one time programmable read only memory, and molded in a 32 pin plastic package. The access time of TC544000P/F is 120ns/150ns and has low power standby mode which reduces the power dissipation without increasing access time.

The electrical characteristics and programming method are the same as U.V. EPROM TC574000D's once programmed, the TC544000P/F cannot be erased because of using plastic DIP without transparent window.

FEATURES

• Peripheral circuit

: CMOS

Memory cell

: N-MOS

• Access time

	- 12	- 120	- 150
Vcc	5∨ ± 5%	5∨ ±	10%
Temp		0°C~70°C	
t _{ACC}	120	150ns	

• Low power dissipation

Active: 60mA/8.3MHz Standby: 100µA (Ta=70°C)

- High speed programming operation
- Single 5V power supply
- Full static operation
- Input and output TTL compatible
- JEDEC standard 32 pin
- Standard 32 pin DIP plastic package: TC544000P

32 pin plastic Flat Package: TC544000F

PIN CONNECTION (TOP VIEW)

V _{PP} A16 A15 A12 A7 A6 A5 A4 A3 A2 A1 A0 D0 D1 D2	1 2 3 4 5 6 6 7 8 9 10 11 11 12 13 14 15	3 3 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	0 9 1 8	Vcc A18 A17 A14 A13 A8 A9 A11 OE D7 D6 D5 D4
	7		8[]	D4 D3

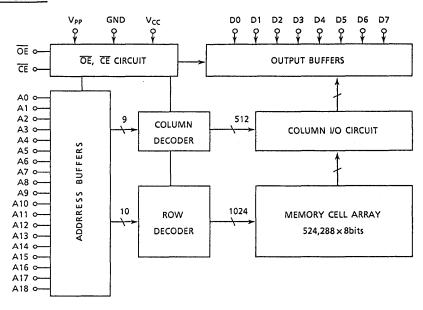
TC544000P/F

PIN NAMES

A0~A18	Address Inputs
D0~D7	Outputs (Inputs)
CE	Chip Enable Input
ŌĒ	Output Enable Input
V _{CC}	V _{CC} Supply Voltage
V _{PP}	Program Supply Voltage
GND	Ground

TC544000P/F-12, TC544000P/F-120 TC544000P/F-150

BLOCK DIAGRAM



MODE SELECTION

MODE	CE	ŌĒ	V _{PP}	Vcc	D0~D7	Power
Read	L	L			Data Out	Active
Output Deselect	*	Н	5V	5V	High Impedance	Active
Standby	н	*			High Impedance	Standby
Program	L	н			Data in	
Program Inhibit	н	Н	12.50V 6.25V		High Impedance	Active
Program Verify	*	L			Data Out	

^{*:} H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	- 0.6~7.0	V
V _{PP}	Program Supply Voltage	-0.6~14.0	٧
ViN	Input Voltage	- 0.6~7.0	V
V _{IN} (A9)	Input Voltage (A9)	-0.6~13.5	٧
V _{I/O}	Input/Output Voltage	-0.6~V _{CC} +0.5	٧
PD	Power Dissipation	1.5	w
T _{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T _{strg}	Storage Temperature	- 65~125	°C
Topr	Operating Temperature	0~70	°C

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC544000P/F - 12	TC544000P/F-120/-150
VIH	Input High Voltage	2.2V~V _{CC} + 0.3V	2.2V~V _{CC} + 0.3V
VIL	Input Low Voltage	-0.3V~0.8V	0.3V~0.8V
Vcc	V _{CC} Power Supply Voltage	5V ± 5%	5V ± 10%
Vpp	V _{PP} Power Supply Voltage	V _{CC} - 0.6V~V _{CC} + 0.6V	V _{CC} - 0.6V~V _{CC} + 0.6V

DC AND OPERATING CHARACTERISTICS ($Ta=0\sim70^{\circ}C$)

SIMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT	
lu	Input Current	V _{IN} = 0~V _{CC}		-	_	± 10	μА	
,	CCO1 Operating Current	CE = V _{IL}	f = 8.3MHz	-	-	60		
ICCO1		l _{OUT} = 0mA	f = 6.7MHz	-	-	50	mA	
I _{CCO2}			f = 1MHz	-	_	15		
I _{CCS1}	CE = V _{IH}			-	_	11	mA	
l _{CCS2}	Standby Current	CE = V _{CC} - 0.2V		-	_	100	μΑ	
VoH	Output High Voltage	l _{OH} = - 400μA		2.4	-	-	V	
Vol	Output Low Voltage	I _{OL} = 2.1mA		-	-	0.4	V	
I _{PP1}	V _{PP} Current	V _{PP} = V _{CC} ± 0.6V		-	-	± 10	μΑ	
I _{LO}	Output Leakage Current	V _{OUT} = 0.4V~V _{CC}		-	_	± 10	μA	

AC CHARACTERISTICS (Ta=0~70°C, VPP=VCC±0.6V)

SIMBOL	PARAMETER	TEST CONDITION	TC544000P/	F - 12/ - 120	TC544000P/F - 150		UNIT
			MIN.	MAX.	MIN.	MAX.	UNII
t _{ACC}	Address Access Time	CE = OE = V _{IL}	_	120	-	150	ns
t _{CE}	CE to Output Valid	ŌĒ = V _{IL}	_	120	_	150	ns
toE	OE to Output Valid	CE = V _{IL}	_	60	_	70	ns
t _{DF1}	CE to Output in High-Z	OE = V _{IL}	0	50	0	60	ns
t _{DF2}	OE to Output in High-Z	CE = V _{IL}	0	50	0	60	ns
tон	Output Data Hold Time	CE = OE = V _{IL}	0	-	0		ns

AC TEST CONDITIONS

• Output Load : 1 TTL Gate and C_L=100pF

Input Pulse Rise and Fall Times : 10ns Max.
 Input Pulse Levels : 0.45V~2.4V

• Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

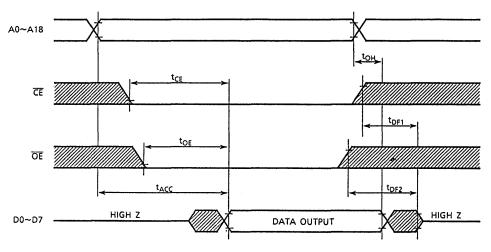
TC544000P/F-12, TC544000P/F-120 TC544000P/F-150

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	-	9	PF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	-	13] "

^{*}This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} + 1.0	V
V _{IL}	Input Low Voltage	- 0.3	-	0.8	٧
V _{CC}	V _{CC} Power Supply Voltage	6.00	6.25	6.50	V
V _{PP}	V _{PP} Power Supply Voltage	12.20	12.50	12.80	٧

DC AND OPERATING CHARACTERISTICS (Ta = $25\pm5^{\circ}$ C, V_{CC} = 6.25V ±0.25 V, V_{pp} = 12.50V ±0.30 V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
l _{Li}	I _{LI} Input Current V _I		-	-	± 10	μА	
V _{OH}	Output High Voltage	l _{OH} = - 400μA	2.4	-	-	٧	
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	-	- -	0.4	V	
lcc	V _{CC} Supply Current	-	-	-	30	mA	
I _{PP2}	V _{PP} Supply Current	V _{PP} = 12.8V	-	_	50	mA	

AC PROGRAMMING CHARACTERISTICS (Ta=25±5°C, $V_{CC}=6.25V\pm0.25V$, $V_{PP}=12.50V\pm0.30V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	¢Δ4X.	UNIT
t _{AS}	Address Setup Time	-	2	-	-	μs
t _{AH}	Address Hold Time	_	2	-	_	μs
t _{CES}	CE Setup Time	-	0	_	_	μs
t _{CEH}	CE Hold Time	-	0	-	_	μs
toes	OE Set up Time	-	2		-	μs
t _{DS}	Data Set up Time	_	2	-	-	μς
t _{DH}	Data Hold Time	_	2	-	-	μs
t _{VPS}	V _{PP} Set up Time	-	2	-	-	μs
t _{VCS}	V _{CC} Set up Time	-	2	-	-	μs
tpW	Program Pulse Width	$\overline{CE} = V_{1L}, \ \overline{OE} = V_{1H}$	45	50	55	μς
t _{OE}	OE to Output Valid	CE = V _{IH}	-	_	100	ns
t _{DFP}	OE to Output in High-Z	CE = V _{IH}	-	-	90	ns

AC TEST CONDITIONS

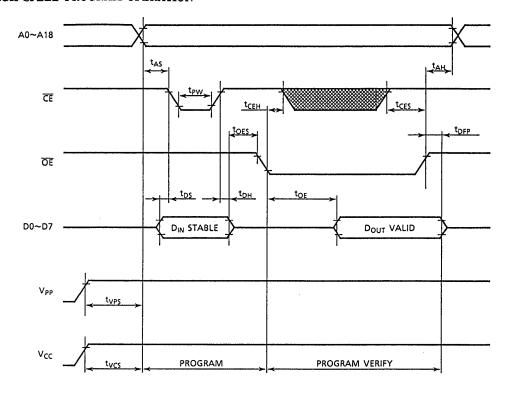
• Output Load : 1 TTL Gate and C_L (100pF)

Input Pulse Rise and Fall Time : 10ns Max.
 Input Pulse Levels : 0.45V~2.4V

• Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAM OPERATION



- Note 1. V_{CC} must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.
 - 2. Removing the device from socket and setting the device in socket with VPP=12.50V may cause permanent damage to the device.
 - 3. The VPP supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the VPP terminal. When the switching pulse voltage is applied to the VPP terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC544000P/F's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE	PIN NAMES (NUMBER)	CE (22)	OE (24)	V _{PP} (1)	V _{CC} (32)	D0~D7 (13~15, 17~21)	POWER	
Read	Read	L	L			Data Out	A -+i	
Operation	Output Deselet	*	Н	5V	5V	High Impedance	Active	
(Ta = 0~70°C)	Standby	н	*			High Impedance	Standby	
Program	Program	L	Н			Data In		
Operation (Ta = 25 ± 5°C)	Program Inhibit	Н	Н	12.50V	6.25V	High Impedance	Active	
	Program Verify	*	L	1		Data Out		

Note : H ; V_{IH} , L : V_{IL} , * : V_{IH} or V_{IL}

READ MODE

The TC544000P/F has two control functions. The chip enable (\overline{CE}) controls the operation power and should be used for device selection. The output enable (\overline{OE}) controls the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The \overline{CE} to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of \overline{OE} .

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more TC544000P/F's can be connected together on a common bus line. When \overline{CE} is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC544000P/F has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC544000P/F is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ inputs.

TC544000P/F-12, TC544000P/F-120 TC544000P/F-150

PROGRAM MODE

Initially, when received by customers, all bits of the TC544000P/F are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC544000P/F is in the programming mode when the V_{PP} input is at 12.50V and \overline{CE} is at Low under $\overline{OE}=V_{IH}$.

The TC544000P/F can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with \overline{OE} at V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.50V) is applied to Vpp terminal, a high level $\overline{\text{CE}}$ and $\overline{\text{OE}}$ input inhibits the TC544000P/F from being programmed.

Programming of two or more TC544000P / F's in parallel with different data is easily accomplished. That is, all inputs except for \overline{CE} and \overline{OE} may be commonly connected, and a low level program pulse is applied to the \overline{CE} of the desired device only and high level signal is applied to the other devices.

HIGH SPEED PROGRAM MODE

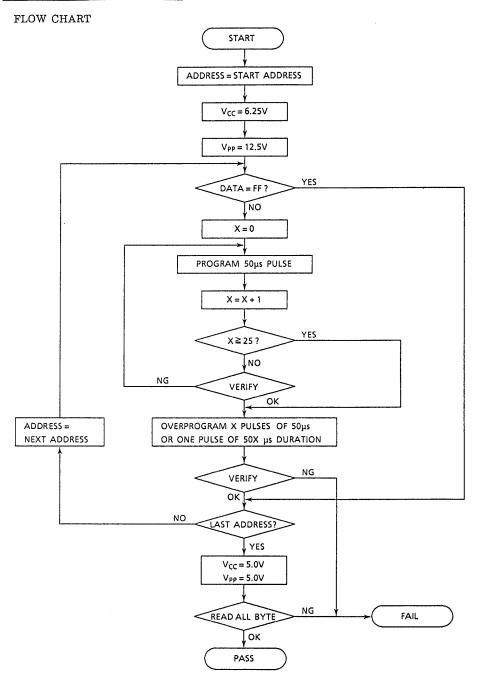
The device is set up in the high speed programming mode when the programming voltage (+12.50V) is applied to the Vpp terminal with $V_{CC}=6.25V$.

The programming is achieved by applying a single low level 50µs pulse to the $\overline{\text{CE}}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 50µs is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 1 time more than that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

HIGH SPEED PROGRAM MODE



TC544000P/F-12, TC544000P/F-120 TC544000P/F-150

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC544000P/F which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC544000P/F by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to $V_{\rm IL}$ in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to $V_{\rm IH}$.

These two codes possess an odd parity with the parity bit of MSB (D7).

The following table shows electric signature of TC544000P/F.

PINS SIGNATURE	Α0	D7	D6	D5	D4	D3	D2	D1	D0	HEX. DATA
Manufacture Code	VIL	1	0	0	1	1	0	0	0	98
Device Code	V _{IH}	1	0	0	0	1	1	0	0	8C

Notes: $A9 = 12V \pm 0.5V$

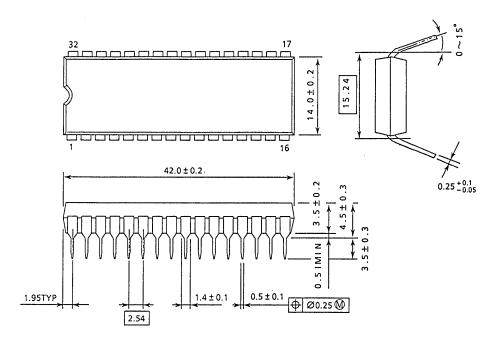
A1~A8, A10~A18, \overline{CE} , $\overline{OE} = V_{IL}$

OUTLINE DRAWINGS

• Plastic DIP

DIP32-P-600

Unit: mm



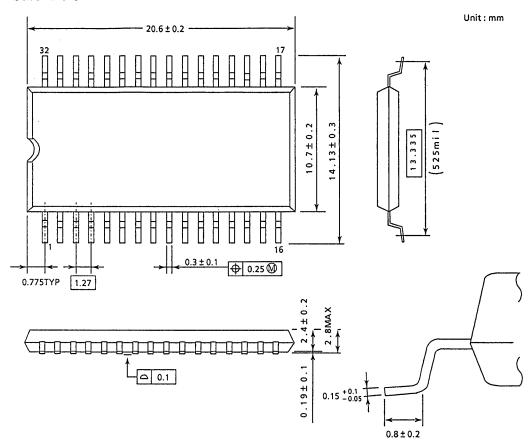
Note: Package width and length do not include mold protrusion, allowable mode protrusion is 0.15mm.

TC544000P/F-12, TC544000P/F-120 TC544000P/F-150

OUTLINE DRAWINGS

• Plastic SOP

SOP32-P-525



Note: Package width and length do not include mold protrusion, allowable mode protrusion is 0.15mm.

			_
•			

1 MEGA BIT (65,536 WORD × 16 BIT) CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

DESCRIPTION

The TC54Hl024P/F is a 65,536 word \times 16 bit one time programmable read only memory, and molded in a 40 pin plastic package.

TC54Hl024P/F is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 40mA/1MHz.

The electrical characteristics and programming method are the same as U.V.EPROM TC57Hl024D. Once programmed, the TC54Hl024P/F cannot be erased because of using plastic package without transparent window.

FEATURES

Peripheral circuit : CMOS
 Memory cell : N-MOS

• Fast access time

TC54Hl024P/F-85 : 85ns TC54Hl024P/F-10 : 100ns

• Low power dissipation Active : 40mA/1MHz

Standby: 100µA

• Single 5V power supply

• Full static operation

• High speed programming operation: tpw 0.1ms

• Input and output TTL compatible

• JEDEC standard 40 pin

• TC54Hl024P: standard 40pin plastic package

• TC54Hl024F: 40pin plastic package

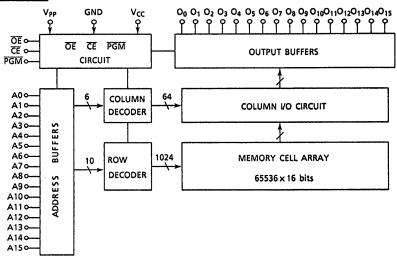
PIN CONNECTION (TOP VIEW)

			1	
V_{PP}	Ţ١	40		v_{cc}
CE	[] ₂	39	μ	PGM
D15	[]3	38	ы	NC
D14	[]4	37	μ	A15
D13	[]5	36	þ	A14
D12	Q6	35	Þ	A13
D11	Q ₇	34	þ	A12
D10	[]8	33	þ	A11
D9	[]9	32	þ	A10
D8	[]10	31	þ	A9
Vss	[11	30	þ	Vss
D7	[]12	29	þ	A8
D6	[] 13	28	þ	Α7
D5	[]14	27	þ	A6
D4	[] 15	26	b	A5
D3	1 16	25	b	A4
D2	J17	24	b	A3
D1	[]18	23	þ	A2
DO	19	22	b	A1
ŌĒ	20	21	b	A0
	1		Ľ	

PIN NAMES

A0~A15	Address Inputs
D0~D15	Outputs (Inputs)
CE	Chip Enable Input
ŌĒ	Output Enable Input
PGM	Program Control Input
Vcc	V _{CC} Supply Voltage
V _{PP}	Program Supply Voltage
Vss	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

PIN	CE	ŌĒ	PGM	V _{PP}	Vcc	D0~D15	Power
Read	L	Ĺ	н			Data Out	Active
Output Deselect	*	н	*	5∨	5V	Mah Impedance	Active
Standby	н	*	*			High Impedance	Standby
Program	L	*	L			Data In	
Program Inhibit	н	*	*]		High Impedance	Active
	L	н	н	12.75V	6.25V	righ impedance	Active
Program Verify	L	L	Н			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	- 0.6~7.0	٧
Vpp	Program Supply Voltage	- 0.6~14.0	٧
VIN	Input Voltage	- 0.6~7.0	٧
V _{IN} (A9)	Input Voltage (A9)	- 0.6~13.5	٧
V _{I/O}	Input/Output Voltage	- 0.6~V _{CC} + 0.5	٧
PD	Power Dissipation	1.5	W
TSOLDER	Soldering Temperature Time	260 · 10	°C · sec
' T _{strg}	Storage Temperature	- 65~125	° C
Topr	Operating Temperature	0~70	° C

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC54H1024P/F-85/10
Ta	Ambient Temperature	0~70°C
Vcc	V _{CC} Power Supply Voltage	5V ± 5%
V _{PP}	V _{PP} Power Supply Voltage	0V~V _{CC} + 0.6V

DC and OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
ILI	Input Current	V _{IN} = 0~V _{CC}	V _{IN} = 0~V _{CC}		•	± 10	μА
Icco	Operating Current	CE = 0V I _{OUT} = 0mA	t _{cycle} = 1µs	-	-	40	mA
I _{CCS1}	Standby Current	CE = VIH	CE = V _{IH}		-	1	mA
I _{CCS2}	Standby Current	$\overline{CE} = V_{CC} - 0.2V$		-		100	μА
V _{IH}	Input High Voltage			2.2	-	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	-	_	- 0.3	-	0.8	V
VoH	Output High Voltage	I _{OH} = -400μA		2.4	-	-	V
VOL	Output Low Voltage	I _{OL} = 2.1mA		-	-	0.4	V
l _{PP1}	V _{PP} Current	$V_{PP} = V_{CC} \pm 0.6V$		-	-	± 10	μА
lLO	Ouptut Leakage Current	V _{OUT} = 0.4V~V _{CC}		-	-	± 10	μА

AC CHARACTERISTICS (VPP=0V~VCC+0.6V)

SYMBOL	PARAMETER	TC54H10)24P/F-85	TC54H1024P/F-10		TINU
31 MBOL	PARAIVIETER	MIN.	MAX.	MIN.	MAX.	UNII
t _{ACC}	Address Access Time	-	85	-	100	
t _{CE}	CE to Output Valid	-	85	_	100	
t _{OE}	OE to Output Valid	0	45	-	50]
t _{DF1}	CE to Output in High-Z	0	30	0	50	ns
t _{DF2}	OE to Output in High-Z	0	30	0	50	
tон	Output Data Hold Time	5	_	10	50	

AC TEST CONDITIONS

Ouput Load

: 1 TTL Gate and $C_L=100pF$

Input Pulse Rise and Fall Time

: 10ns Max.

Input Pulse Levels

: 0.45V to 2.4V

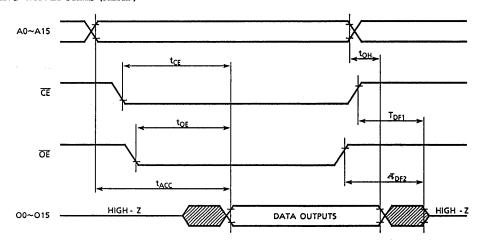
Timing Measurement Reference Level: Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	-	6	10	
C _{OUT}	Output Capacitance	V _{OUT} = 0V	-	10	12	рř

^{*} This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	V _{CC} + 0.3	٧
VIL	Input Low Voltage	- 0.3	-	0.8	٧
Vcc	V _{CC} Power Supply Voltage	6.00	6.25	6.50	٧
Vpp	V _{PP} Power Supply Voltage	12.50	12.75	13.00	V

DC AND OPERATING CHARACTERISTICS($T_a = 25 \pm 5^{\circ}\text{C}$, $VCC = 6.25 \text{V} \pm 0.25 \text{V}$, $VPP = 12.75 \text{V} \pm 0.25 \text{V}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ILI	Input Current	V _{IN} = 0~V _{CC}	-	-	± 10	μА
V _{OH}	Output High Voltage	I _{OH} = -400μA	2.4	-	-	v
VOL	Output Low Voltage	I _{OL} = 2.1mA	-	-	0.4	٧
Icc	V _{CC} Supply Current	-	-	-	50	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} = 13.0V		-	100	mA

AC PROGRAMMING CHARACTERISTICS (Ta = $25 \pm 5^{\circ}$ C, VCC = 6.25V ± 0.25 V, VPP = 12.75V ± 0.25 V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	_	-	μς
t _{AH}	Address Hold Time	-	2	-	-	μs
t _{CES}	CE Setup Time	-	2	-	_	μs
t _{CEH}	CE Hold Time	_	2	_	-	μs
t _{DS}	Data Setup Time	-	2	-	_	μς
t _{DH}	Data Hold Time	-	2	-		μς
t _{VS}	V _{PP} Setup Time	-	2	_	-	μs
t _{PW}	Program Pulse Width	-	0.095	0.1	0.105	ms
t _{OE}	OE to Output Valid	-	-	-	500	ns
t _{DF2}	OE to Output in High-Z	CE = V _{IL}	-	-	150	ns
toes	OE Setup Time		2	-	_	μs

AC TEST CONDITIONS

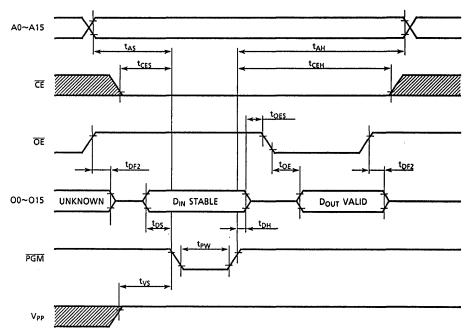
• Output Load : 1 TTL Gate and C_L (100pF)

Input Pulse Rise and Fall Time : 10ns Max.
 Input Pulse Levels : 0.45V and 2.4V

• Timing Measurement Reference Level: Input 0.8V and 2.2V, Ouptut 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



Note

- 1. VCC must be applied simultaneously or before Vpp and cut off simultaneously or after Vpp.
- 2. Removing the device from socket and setting the device in socket with $V_{PP}=12.75V$ may cause permanent damage to the device.
- The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.
 - When the switching pulse voltage is applied to the $V_{\rm PP}$ terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC54H1024P/F's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN	CĒ	ŌĒ	PGM	V _{PP}	V _{CC}	D0~D15	Power	
READ OPERATION	Read		L	L	Н			Data Out	Active	
	Output Deselet		*	Н	*	5∨	5V	5∨	Ulah impadansa	Active
	Standby		Н	*	*			High Impedance	Standby	
	Program		L	*	L			Data In		
PROGRAM OPERATION (Ta = 25 ± 5°C)	Brogram Inhihit		Н	*	*	12.75V 6.25V				
	Program Inhibit		L	Н	н		/50 6.250	High Impedance	Active	
	Program Verify		L	L	Н			Data Out		

Note : H ; V_{IH} , L : V_{IL} , * : V_{IH} or V_{IL}

READ MODE

The TC54H1024P/F has three control functions. The chip enable (\overline{CE}) controls the operation power and should be used for device selection.

The output enable (\overline{OE}) control the output buffers, independent of device selection. Assuming in that $\overline{CE} = \overline{OE} = V_{IL}$ and $\overline{PGM} = V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The \overline{CE} to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of \overline{OE} .

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line.

When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC54H1024P/F has a low power standby mode controlled by the CE signal.

By applying a high level to the $\overline{\text{CE}}$ input, the TC54H1024P/F is placed in the standby mode which reduce the operating current to 100 μ A by applying MOS-high level (V_{CC}) and then the oututts are in a high impedance state, independent of the $\overline{\text{OE}}$ inputs.

TC54H1024P/F-85 TC54H1024P/F-10

PROGRAM MODE

Initially, when received by customers, all bits of the TC54H1024P/F are in the "1" state which is erased state.

Therefore the program operation is to introduce O'S data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC54H1024P/F can be programmed any location at anytime -- either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with \overline{OE} and \overline{CE} at V_{IL} and \overline{PGM} at V_{IH} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to Vpp terminal, a high level $\overline{\text{CE}}$ or $\overline{\text{PGM}}$ input inhibits the TC54H1024P/F from being programmed.

Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for \overline{CE} or \overline{PGM} may be commonly connected, and a \overline{TTL} low level program pulse is applied to the \overline{CE} and \overline{PGM} of the desired device only and \overline{TTL} high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

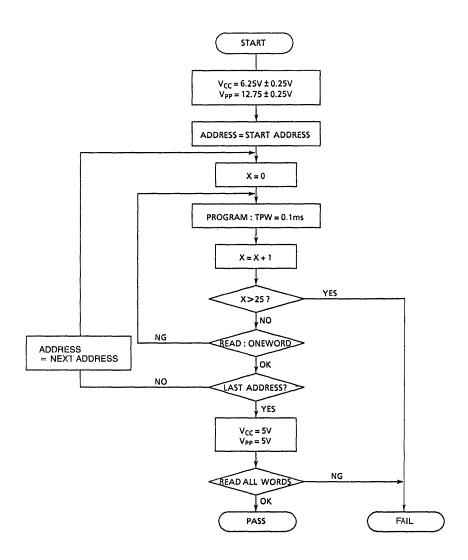
The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the Vpp terminal with $V_{CC}=6.25\text{V}$ and $\overline{PGM}=V_{IH}$.

The programming is achieved by applying a single TTL low level 0.1ms pulse the PGM input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated unitly the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{\rm CC} = V_{\rm PP} = 5V$.

HIGH SPEED PROGRAM OPERATION FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC54H1024P/F which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC54H1024P/F by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH} .

These two codes possess an odd parity with the parity bit of (07).

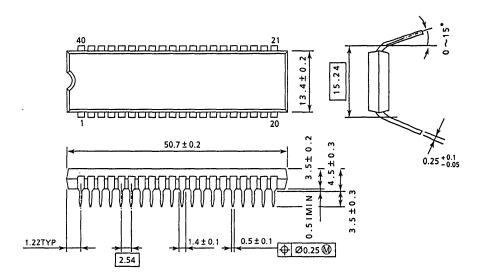
The following table shows electric signature of TC54H1024P/F.

SIGNATURE	A ₀	015	014	013	012	011	010	Og	Ов	07	06	O ₅	04	O ₃	O2	01	00	HEX DATA
Manufacturer Code	V _{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0.	0	**98
Device Code	V _{IH}	*	٠	٠,	*	*	٠	*	*	1	0	0	0	1	0	0	1	**89

Notes: $A9 = 12V \pm 0.5V$, $A_1 - A_8$, $A_{10} - A_{15}$, \overline{CE} , $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$

OUTLINE DRAWINGS DIP40-P-600

Unit: mm



			-





1M BIT (128K WORD x 8 BIT) CMOS MASK ROM SILICON GATE CMOS

DESCRIPTION

The TC531000CP/CF is a 1,048,576 bits read only memory organized as 131,072 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor, especially character generator. The TC531000CP/CF using CMOS technology is most suitable for low power applications where battery operation are required. The TC531000CP/CF has one chip enable input CE/CE, programmable for device selection.

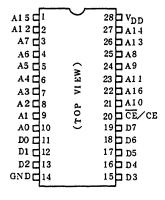
FEATURES

TC531000CP/CF		120ns Version	150ns Version
Access Time	(max.)	120ns	150ns
Power Dissipation Operation Current	(max.)	4 Om.A	35mA
Power Dissipation Standby Current	(max.)	20μA	20μΑ

- · Single 5V Power Supply
- All Inputs and Outputs: TTL Compatible
- · Three State Outputs
- · Fully Static Operation
- · Programmable Chip Enable
- · Package

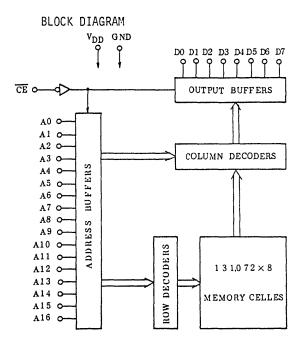
Plastic DIP: TC531000CP Plastic FP: TC531000CF

PIN CONNECTION



PIN NAMES

A0 ~ A16	Address Inputs
D0 ∿ D7	Data Outputs
CE/CE	Chip Enable Input
VDD	Power Supply
GND	Ground



TC531000CP-12, TC531000CP TC531000CF-12, TC531000CF

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ∿.7.0	
VIN	Input Voltage	-0.5 ∿ V _{DD}	v
VOUT	Output Voltage	o ∿ V _{DD}	7
PD	Power Dissipation	1.0/0.6 *	W
TSTG	Storage Temperature	- 55 [∿] 150	- °c
TOPR	Operating Temperature	-40 ~ 70	
TSOLDER	Soldering Temperature • Time	260 · 10	°C•sec

Note: * Plastic FP

DC OPERATING CONDITIONS (Ta=-40 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
v_{DD}	Power Supply Voltage	4.5	5.0	.5.5	
VIH	Input High Voltage	2.2	-	V _{DD} +0.3	V
VIL	Input Low Voltage	-0.3	-	0.8	

DC and OPERATING CHARACTERISTICS (Ta=-40 $^{\circ}$ 70 °C, V_{DD} =5V±10%)

SYMBOL	PARAMETER	CONDITIO	ons	MIN.	MAX.	UNIT
IIL	Input Leakage Current	$V_{IN}=0 \sim V_{DD}$		-	±1.0	
ILO	Output Leakage Current	CE=VIH, VOUT=0 ~ VI	-	±5.0	μA	
IOH	Output High Current	V _{OH} =2.4V	-1.0	-		
IOL	Output Low Current	V _{OL} =0.4V	3.2	-	mΑ	
I _{DDS1}	Standby Current	CE=0.8V (CE=2.2V)	_	2		
IDDS2	Standby Current	CE=0.2V (CE=VDD-0	.2V)	-	20	μA
I _{DDO1}		V _{IN} =V _{IH} /V _{IL}	t _{cycle} =120ns	-	50	
±DD01	Onemating Comment	I _{OUT} =0mA	t _{cycle} =150ns	-	45	mA
Tabaa	Operating Current	$v_{IN} = v_{DD} - 0.2 \text{V} / 0.2 \text{V}$	t _{cycle} =120ns	-	40	III.
I _{DDO2}		I _{OUT} =0mA	t _{cycle} =150ns	-	35	

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
CIN	Input Capacitance	f=1MHz, Ta=25°C	-	10	рF
COUT	Output Capacitance	f=1MHz, Ta=25°C	-	10	pτ

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS ($V_{DD}=5V\pm10\%$, Ta=-40 $\sim70^{\circ}$ C)

SYMBOL	PARAMETER	120ns	Version	150ns	UNIT	
		MIN.	MAX.	MIN.	MAX.	
^t cycle	Cycle Time	120	-	150	-	
^t ACC	Access Time	-	120	-	150	7
^t CE	Chip Enable Access Time	-	120	-	150	ns
tCED	Output Disable Time	-	50	-	50	7
t _{OH}	Output Hold Time	5	-	5	_	

AC TEST CONDITION

· Output Load_

: 100pF + 1TTL

· Input Levels

: 0.6V, 2.4V

· Timing Measurement Reference Levels

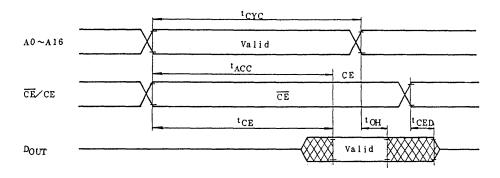
Input: 0.8V, 2.2V

Output: 0.8V, 2.0V

· Input Rise and Fall Time

: 5ns

TIMING WAVEFORMS



OPERATING MODE

MODE	CE(CE)	A0 ∿ 16	Outputs	Power
Read	L(H)	Valid	Data Out	Operating
Standby	H(L)	*	High-Z	Standby

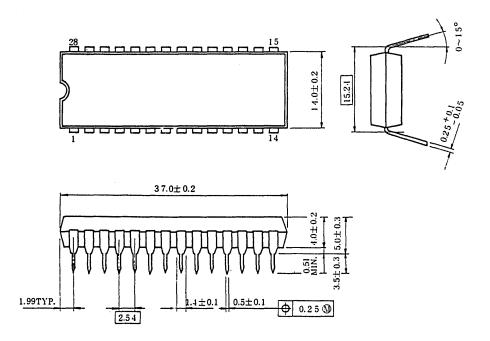
H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

TC531000CP-12, TC531000CP TC531000CF-12, TC531000CF

OUTLINE DRAWINGS

Plastic DIP (DIP28-P-600)

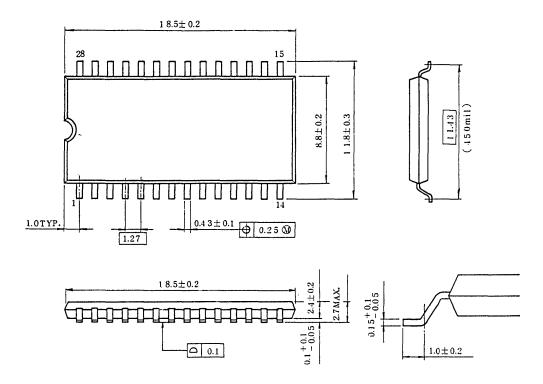
Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

Plastic FP (SOP28-P-450)

unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is $0.15\,\mathrm{mm}$.

IM BIT (128K WORD x 8 BIT) CMOS MASK ROM SILICON GATE CMOS

DESCRIPTION

The TC531001CP/CF is a 1,048,576 bits read only memory organized as 131,072 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor, and data memory, especially character generator. The TC531001CP/CF using CMOS technology is most suitable for low power applications where battery operations are required.

The TC531001CP/CF has one chip enable input $\overline{\text{CE}}$ for device selection.

FEATURES

TC531001CP/CF		120ns Version	150ns Version
Access Time	(max.)	120ns	150ns
Power Dissipation Operating Current	(max.)	40mA	35mA
Power Dissipation Standby Current	(max.)	20μΑ	20µA

- Single 5V Power Supply
- · All Inputs and Outputs: TTL Compatible
- · Three State Outputs
- Fully Static Operation
- Package Plastic DIP: TC531001CP

Plastic FP: TC531001CF

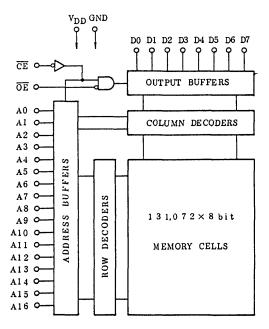
PIN CONNECTION

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иcd	1		32	$\vdash v_{DD}$
A16	2		31	DN.C.
A1 5 🗖	3		30	, c.
A12	4		29	□ A1 4
A7 🗖	5		28	□ A13
A6 🗖	6	$\widehat{}$	27	□ A8
A5 🗆	7	2	26	□ A 9
A4 🗖	8	^	25	DAII
A3 🗖	9	(TOP VIEW)	24	DOE
A2 🗖	10	0.1	23	A10
AID	11	\sim	22	D CE
A0 🗖	12		21	D D7
D0 🗖	13		20	□ D6
DI口	14		19	⊐ D5
D2口	15		18	D D4
GND	16		17	D D3
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PIN NAMES

A0 ~ A16	Address Inputs	
DO ∿ D7	Data Outputs	
ŌĒ	Output Enable Input	
ČĒ	Chip Enable Input	
v_{DD}	Power Supply	
GND	Ground	
N.C.	No Connection	

BLOCK DIAGRAM



TC531001CP-12, TC531001CP TC531001CF-12, TC531001CF

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
VDD	Power Supply Voltage	-0.5 ~ 7.0	v
VIN	Input Voltage	-0.5 ∿ V _{DD}	v
VOUT Output Voltage		0 ∿ V _{DD}	
PD	Power Dissipation	1.0/0.6 *	W
T _{STG} Storage Temperature		-55 ^ 150	°C
T _{OPR} Operating Temperature		-40 ∿ 70	°C
T _{SOLDER} Soldering Temperature Time		260 · 10	°C•sec

Note: * Plastic FP

DC OPERATING CONDITIONS (Ta=-40 \sim 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
ADD	Power Supply Voltage	4.5	5.0	5.5	
VIH	Input High Voltage	2.2	-	V _{DD} +0.3	v
VIL	Input Low Voltage	-0.3	-	0.8	

DC and OPERATING CHARACTERISTICS (Ta=-40 \sim 70°C, V_{DD} =5V±10%)

SYMBOL	PARAMETER	CONDITION		MIN.	MAX.	UNIT
IIL	Input Leakage Current	$V_{IN}=0 \sim V_{DD}$		-	±1.0	μA
I _{LO}	Output Leakage Current	CE=V _{IH} , V _{OUT} =OV ~ V _D	D	-	±5.0	μA
IOH	Output High Current	V _{OH} =2.4V		-1.0	-	mA
IOL	Output Low Current	V _{OL} =0.4V		3.2	-	mA
I _{DDS1}	Standby Current	<u>CE</u> =2.2V		-	2	mA
I _{DDS2}	Standby Current	<u>CE</u> =V _{DD} -0.2V		-	200	μA
I _{DDO1}		V _{IN} =V _{IH} /V _{IL}	t _{cycle} =120ns	-	50	
10001		I _{OUT} =0mA	t _{cycle} =150ns	-	45	
Operating Current		V _{IN} =V _{DD} -0.2V/0.2V	t _{cycle} =120ns	-	40	mA
I _{DDO2}		I _{OUT} =OmA	t _{cycle} =150ns	-	35	

CAPACITANCE

SYMBOL	PARAMETER CONDITIONS		MIN.	MAX.	UNIT
CIN	Input Capacitance	f=1MHz, Ta=25°C	-	10	pF
C _{OUT}	Output Capacitance	f=1MHz, Ta=25°C	-	10] pr

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS (Ta=-40 \sim 70°C, V_{DD} =5V±10%)

CYNTROL	PARAMETER	120ns	Version	150ns	Version	IIII m
SYMBOL PARAMETER		MIN.	MAX.	MIN.	MAX.	UNIT
t _{cycle}	Cycle Time	120	_	150	-	
t _{ACC}	Access Time	-	120	-	150	
^t CE	Chip Enable Access Time	-	120	-	150	
tOE	Output Enable Access Time	-	70	-	70	ns
^t CED	Output Disable Time from CE	-	50	-	50	
tOED	Output Disable Time from OE	-	50	-	50	
tOH	Output Hold Time	5	-	5	_	

AC TEST CONDITIONS

• Output Load : 100pF + 1TTL

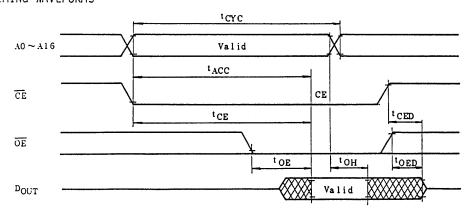
• Input Levels : 0.6V, 2.4V

· Timing Measurement Reference Levels Input: 0.8V, 2.2V

Output: 0.8V, 2.0V

• Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



OPERATION MODE

MODE	ĈĒ	ŌĒ	A0 ∿ 16	Outputs	Power
Read	L	L	Valid	Data Out	Operating
Standby	Н	*	*	High-Z	Standby
Output Deselect	L	Н	it	High-Z	Operating

 $H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}$

TC531001CP-12, TC531001CP TC531001CF-12, TC531001CF

OUTLINE DRAWINGS

Plastic DIP (DIP32-P-600)

Unit in mm

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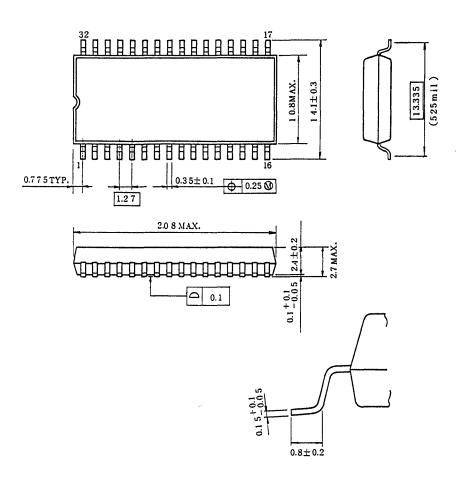
1.4±0.1

1.4±

Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

Plastic FP (SOP32-P-525)

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

1M BIT (65,536 WORD x 16 BIT) CMOS MASK ROM

DESCRIPTION

The TC531024P/F is a 1,048,576 bits read only memory organized as 65,536 words by 16 bits.

The TC531024P/F is fabricated using Toshiba's advanced CMOS technology which provides the high speed and low power features with access time of 120ns/150ns, an operation current of 40mA at 8.3MHz and a standby current of $20\mu A$.

The TC531024P/F is packaged in a standard 600mil 40pin DIP, or 525mil 40pin SOP.

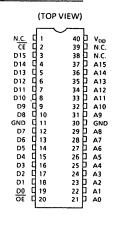
FEATURES

TC531024P/F	- 12 ⁻	- 15
Power Supply	5V ± 5%	5V ± 10%
Access Time (Max.)	120ns	150ns
Power Dissipation : Operating Current (Max.)	40mA	35mA
Power Dissipation : Standby Current (Max.)	20μΑ	20μΑ

- Single 5V Power Supply
- Fully Static Operation
- All Input and Output: TTL Compatible
- · Three State Output
- 40pin 600mil width Plastic DIP
- 40pin 525mil width Plastic SOP

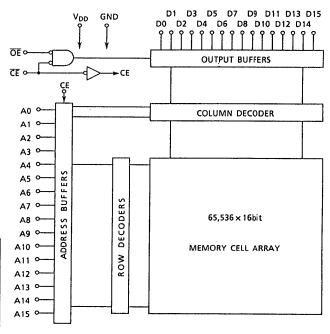
PIN CONNECTION

BLOCK DIAGRAM



PIN NAMES

	
A0~A15	Address inputs
D0~D15	Data Outputs
ŌĒ	Output Enable Input
ČĒ	Chip Enable Input
V _{DD}	Power Supply
GND	Ground
N.C.	No Connection



TC531024P-12, TC531024P-15 TC531024F-12, TC531024F-15

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	- 0.5~7.0	V
VIN	Input Voltäge	- 0.5~V _{DD}	V
V _{OUT}	Output Voltage	0~V _{DD}	v
P _D	Power Dissipation	1.0/0.6*	w
T _{STG}	Storage Temperature	- 55~150	•℃
T _{OPR}	Operating Temperature	0~70	°C
T _{SOLDER}	Soldering Temperature - Time	260 10	°C · sec

Note: * Plastic FP.

D.C. OPERATING CONDITIONS (Ta = $0\sim70^{\circ}$ C)

SYMBOL	PARAMETER		MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.5	٧
VIH	Input High Voltage	2.2	V _{DD} + 0.3	٧
V _{IL}	Input Low Voltage	- 0.3	0.8	٧

D.C. OPERATING CHARACTERISTICS (Ta = $0 \sim 70$ °C, $V_{DD} = 5V \pm 10$ %)

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
l _{IL}	Input Leakage Current	0V≤V _{IN} ≤V _{DD}	0∨≤∨ _{IN} ≤∨ _{DD}		± 1.0	
lo	Output Leakage Current	0V≤V _{OUT} ≤V _{DD}	0V≤V _{OUT} ≤V _{DD}		± 5.0	μΑ
Іон	Output High Current	V _{OH} = 2.4V	V _{OH} = 2.4V		-	
lor	Output Low Current	V _{OL} = 0.4V		3.2	-	mA
I _{DDS1}	Canada Comana	$\overline{CE} = 2.2V$ $\overline{CE} = V_{DD} - 0.2V$		_	2.0	
IDDS2	Standby Current			-	20	μА
1		CE = VIL, VIN = VIH / VIL	t _{cycle} = 120ns	-	50	
DDO1	Operating Current	I _{OUT} = 0mA	t _{cycle} = 150ns	-	45	
I _{DDO2}		$\overline{CE} = 0.2V$, $V_{IN} = V_{DD} - 0.2V / 0.2V$	t _{cycle} = 120ns	-	40	mA
		I _{OUT} = 0mA	t _{cycle} = 150ns	-	35	

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	f = 1MHz , Ta = 25°C	-	10	pF
C _{OUT}	Output Capacitance	f = 1MHz , Ta = 25°C	-	10	pF

Note: This Parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = 0° C \sim 70°C)

SYMBOL	DARAMETER	V _{DD} = 5V ± 5%		V _{DD} = 5V ± 10%		LINUT
	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT
t _{ACC}	Access Time	_	120	_	150	ns
t _{CE}	Chip Enable Access Time	-	120	-	150	ns
t _{OE}	Output Enable Access Time	-	70	-	70	ns
t _{CED}	Output Disable Time from CE	0	60	0	60	ns
t _{OED}	Output Disable Time from $\overline{\sf OE}$	0	60	0	60	ns
t _{OH}	Output Hold Time	5	-	5	_	ns
t _{CYC}	Cycle Time	120	_	150	-	ns

A.C. TEST CONDITIONS

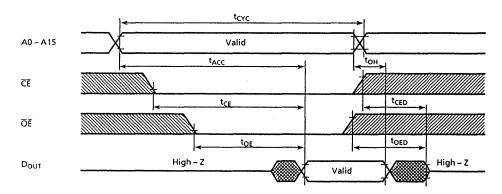
Output Load : 100pF + 1TTL

Input Levels : 0.6V / 2.4V
Timing Measurement Reference Levels Input : 0.8V / 2.2V

Output: 0.8V / 2.0V

Input Rise and Fall Time (10%~90%) : 5ns

TIMING WAVEFORMS



OPERATION MODE

MODE	CE	ŌĒ	A0~A15	Outputs	Power
Read	L	L	Valid	Data Out	Operating
Standby	н	*	*	High-Z	Standby
Output Deselect	L	н	*	High-Z	Operating

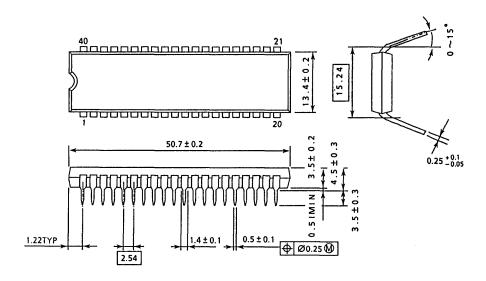
H: VIH L: VIL *: VIH or VIL

TC531024P-12, TC531024P-15 TC531024F-12, TC531024F-15

OUTLINE DRAWINGS

Plastic DIP (DIP40-P-600)

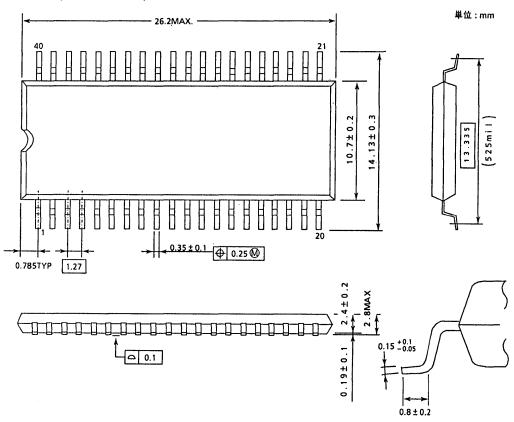
単位:mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

Plastic FP (SOP40-P-525)



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

			-

4M BIT (512K WORD × 8 BIT) CMOS MASK ROM

DESCRIPTION

The TC534000P/F is a 4,194,304 bits read only memory organized as 524,288words by 8bits.

The TC534000P/F is fabricated using Toshiba's advanced CMOS technology which provides the high speed and low power features with access time of 200ns/250ns, an operation current of 30mA at 5MHz and a standby current of 20µA.

The TC534000P/F has one programmable chip enable input CE/CE for device selection.

The TC534000P/F is packaged in a standard 600mil 32pin DIP or 525mil 32pin SOP.

FEATURES

• Single 5V Power Supply

• Access Time: 250ns (Max.) VDD=5V±10%

: 200ns (Max.) $V_{DD} = 5V \pm 5\%$

• Power Dissipation

Operating Current: 30mA (Max.)

Standby Current : 20µA (Max.)

• All Inputs and Outputs: TTL Compatible

Three State Outputs

Fully Static Operation

• Programmable Chip Enable

Package Plastic DIP: TC534000P

Plastic FP: TC534000F

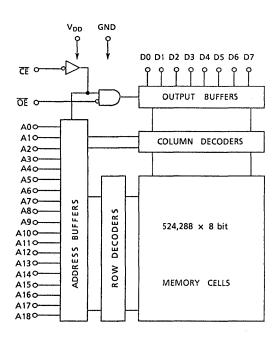
PIN CONNECTION

A1 0 11 22 0 CE/CE A0 0 12 21 0 D7 D0 0 13 20 0 D6 D1 0 14 19 0 D5 D2 0 15 18 0 D4 GND 0 16 19 0 D3	A3 A2 A1 A0 D0 D1 D2	[] 13 [] 14 [] 15	20 D D6 19 D D5 18 D D4
--	--	-------------------------	-------------------------------

PIN NAMES

A0~A18	Address inputs
D0~D7	Data Outputs
ŌĒ	Output Enable Input
CE/CE	Chip Enable Input
V _{DD}	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



TC534000P/F

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	- 0.5~7.0	v
V _{IN}	Input Voltage	- 0.5~V _{DD}	v
Vout	Output Voltage	0~V _{DD}	v
P _D	Power Dissipation	1.0/0.6*	w
TstG	Storage Temperature	- 55~150	° C
T _{OPR}	Operating Temperature	- 40~85	° C
TSOLDER	Soldering Temperature - Time	260 · 10	*C · sec

Note: * Plastic FP.

D.C. OPERATING CONDITIONS (Ta = $-40 \sim 85$ °C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.5	v
VIH	Input High Voltage	2.2	V _{DD} + 0.3	>
V _{IL}	Input Low Voltage	- 0.3	0.8	V

D.C. and OPERATING CHARACTERISTICS ($V_{DD} = 5V \pm 10\%$, $Ta = -40 \sim 85^{\circ}C$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
l _{IL}	Input Leakage Current	V _{IN} = 0~V _{DD}	_	± 1.0	μΑ
ło	Output Leakage Current	CE=VIH, VOUT=0~VDD	_	± 5.0	μΑ
Юн	Output High Current	V _{OH} =2.4V	- 1.0	-	mA
loL	Output Low Current	V _{OL} =0.4V	2.0	-	mA
I _{DDS1}	- Standby Current	Œ=V _{IH}	_	2	mA
I _{DDS2}	Standby Content	$\overline{CE} = V_{DD}$ and $V_{IN} = 0V (V_{DD})$	-	20	μΑ
l _{DDO1}	Operating Current	V _{IN} = V _{IH} / V _{IL} , t _{cycle} = 250ns	-	40	mA
IDDO2	Operating Otherit	V _{IN} = V _{DD} / 0V , t _{cycle} = 250ns	_	30	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	f=1MHz , Ta=25°C	-	8	рF
C _{OUT}	Output Capacitance	f=1MHz, Ta=25°C	-	10	pF

Note: This Parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS

CVAADO	YMBOL PARAMETER		Ta = -40~85°C, V _{DD} = 5V ± 10%		Ta = -40~70°C, V _{DD} = 5V ± 5%	
STIVIBUL	PARAIVIETER	MIN.	MAX.	MIN.	MAX.	UNIT
t _{ACC}	Access Time	-	250	-	200	ns
t _{CE}	Chip Enable Access Time	-	250	-	200	ns
t _{OE}	Output Enable Access Time	-	70	_	70	ns
t _{CED}	Output Disable Time from CE	0	70	0	70	ns
t _{OED}	Output Disable Time from OE	0	70	0	70	ns
tон	Output Hold Time	10	-	10	_	ns
tcyc	Cycle Time	250	_	200	_	ns

A.C. TEST CONDITIONS

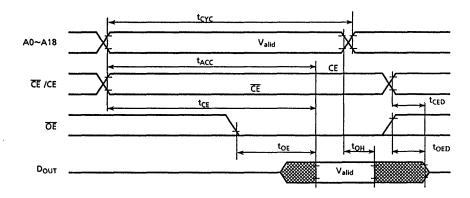
Output Load : 100pF + 1TTL

 $\begin{tabular}{ll} Input Levels & : 0.6V \ , 2.4V \\ Timing Measurement Reference Levels & Input & : 0.8V \ , 2.2V \\ \end{tabular}$

Output: 0.8V, 2.0V

Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



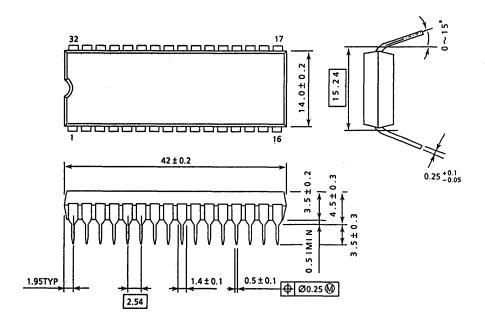
OPERATION MODE

MODĘ	ČĒ (CE)	ŌĒ	A0~A18	Outputs	Power
Read	L(H)	L	Valid	Data Out	Operating
Standby	H(L)	*	*	High-Z	Standby
Output Deselect	L(H)	Н	*	High-Z	Operating

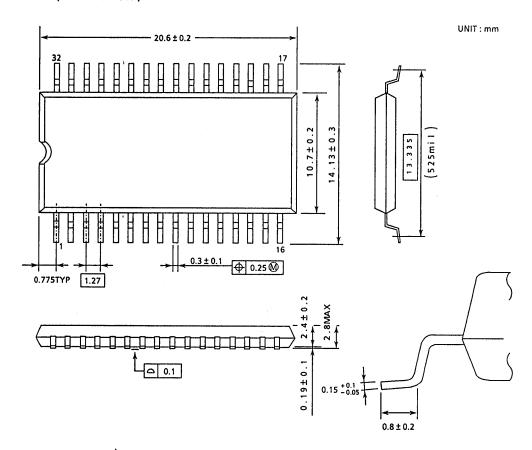
H: VIH L: VIL *: VIH or VIL

OUTLINE DRAWINGS
Plastic DIP (DIP32 - P - 600)

UNIT: mm



OUTLINE DRAWINGS
Plastic FP (SOP32 - P - 525)



			-
	•		
		•	

4M BIT (256K WORD x 16 BIT/512K WORD x 8BIT) CMOS MASK ROM

PRELIMINARY

DESCRIPTION

The TC534200P/F is a 4,194,304 bits read only memory organized as 262,144 words by 16 bits when BYTE is logical high, and is organized as 524,288 words by 8 bits when BYTE is logical low.

The TC534200P/F is most suitable for in program memory of 16 bits microprocessor, data memory, and character generator. The TC534200P/F has a programmable chip enable input CE/\overline{CE} for device selection.

The TC534200P/F is packaged in a standard 600mil 40pin DIP, or 525mil 40 pin SOP.

FEATURES

Single 5V Power Supply

• Access Time: 150ns (Max.)

• Power Dissipation

Operating Current: 50mA (Max.)

Standby Current : 20µA (Max.)

Fully Static Operation

• All Inputs and Outputs: TTL Compatible

• Three State Outputs

Programmable Chip Enable

• 40pin 600mil width Plastic DIP

• 40pin 525mil width Plastic SOP

PIN CONNECTION (TOP VIEW)

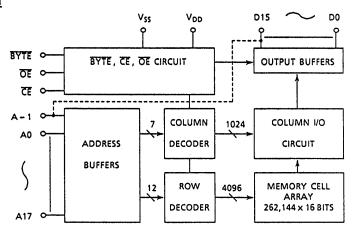
	
A17 [] 1	40 🗖 A8
A7 🗆 2	39 🗖 A9
A6 🖸 3	38 🗖 A10
A5 🗆 4	37 🗖 A11
A4 🗖 5	36 🗖 A12
A3 🗆 6	35 🗖 A13
A2 🔲 7	34 🗖 A14
A1 ☐ 8	33 🗖 A15
A0 🗖 9	32 🗖 A16
CE/CE ☐ 10	31 D BYTE
GND ☐ 11	30 🗖 GND
죤口 12	29 🗀 D15 / A – 1
DO 🗖 13	28 🗀 D7
D8 🗖 14	27 🗖 D14
D1 🔲 15	26 🗖 D6
D9 🗖 16	25 🗖 D13
D2 🗖 17	24 🗖 D5
D10 🗖 18	23 🗖 D12
D3 🗖 19	22 🗖 D4
D11 🔲 20	21 🗆 VDD
	

PIN NAMES

A0~A17	Address inputs
D0~D14	Data Outputs
CE/CE	Chip Enable Input
ŌĒ	Output Enable Input
D15/A-1	Data Output Address Input
BYTE	Word, Byte selection Input
V _{DD}	Power Supply
GND	Ground

TC534200P/F

BLOCK DIAGRAM



MODE SELECTION

MODE	CE (CE)	ŌĒ	BYTE	D0 – D7	D8 - D14	D15/A-1	
Read (16 Bit)	L (H)	Ļ	н	Data Out			
Read (8 Bit)	L (H)	L	L	Data Out (Lower 8bit)	High Impedance	L	
Read (8 Bit)	L (H)	L	L	Data Out (Upper 8bit)	High Impedance	н	
Output Deselect	L (H)	н	*	High Impedance			
Standby	H (L)	*	*	High Impedance			

 $H:V_{IH}\ L:V_{IL}\ *:V_{IH}\ or\ V_{IL}$

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	- 0.5~7.0	v
VIN	Input Voltage	-0.5~V _{DD}	v
Vout	Output Voltage	0~V _{DD}	V
P _D	Power Dissipation	1.0/0.6*	w
T _{STG}	Storage Temperature	- 55~150	°C
TOPR	Operating Temperature	- 40~85	°C
TSOLDER	Soldering Temperature • Time	260 · 10	°C · sec

^{*} SOP

D.C. OPERATING CONDITIONS (Ta = $0\sim70^{\circ}$ C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	٧
V _{IH}	Input High Voltage	2.2	-	V _{DD} + 0.3	٧
V _{IL}	Input Low Voltage	- 0.3	-	0.8	v

D.C. and OPERATING CHARACTERISTICS ($Ta = 0 \sim 70$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
l _{IL}	Input Leakage Current	V _{IN} = 0~V _{DD}	_	± 1.0	μА
I _{LO}	Output Leakage Current	V _{OUT} = 0~V _{DD}	-	± 5.0	μΑ
Гон	Output High Current	V _{OH} =2.4V	- 1.0	_	mA
l _{OL}	Output Low Current	V _{OL} = 0.4V	2.0	-	mA
loosi	- Standby Current	ČE=V _{IH}	-	2	mA
I _{DDS2}	Standby Current	<u>CE</u> =V _{DO} − 0.2V	_	20	μΑ
I _{DDO1}	Operating Current	$V_{IN} = V_{IH} / V_{IL}$, $t_{cycle} = 150 ns$		60	mA
10002	Operating outlett	$V_{IN} = V_{DD} - 0.2V / 0.2V t_{cycle} = 150 ns$	-	50	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
CiN	Input Capacitance	f = 1MHz , Ta = 25°C	-	10	рF
C _{OUT}	Output Capacitance	f = 1MHz , Ta = 25°C	T -	10	pF

Note : This Parameter is periodically sampled and is not 100% tested.

TC534200P/F

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
tcyc	Cycle Time	150	-	ns
t _{ACC}	Address Access Time	-	150	ns
t _{CE}	Chip Enable Access Time	-	150	ns
t _{BT}	BYTE Access Time	-	150	ns
t _{OE}	Output Enable Access Time	-	70	ns
t _{CED}	Output Disable Time from CE	-	60	ns
^t OED	Output Disable Time from OE	_	60	ns
t _{8TO}	Output Disable Time from BYTE	-	60	ns
^t он	Output Hold Time	5	_	ns

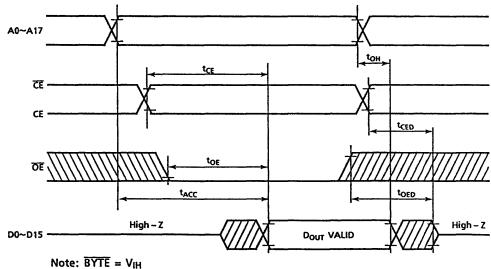
A.C. TEST CONDITIONS

Output Load : 100pF + 1TTL : 0.6V , 2.4V Input Levels Input : 0.8V , 2.2V Timing Measurement Reference Levels Output: 0.8V, 2.0V

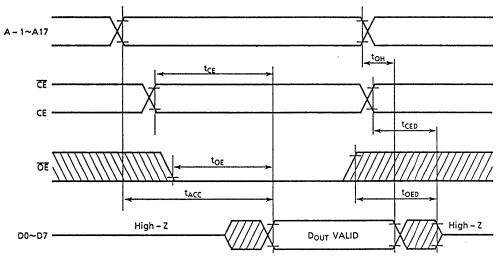
Input Rise and Fall Time : 5ns

TIMING WAVEFORMS

WORD - WIDE READ MODE



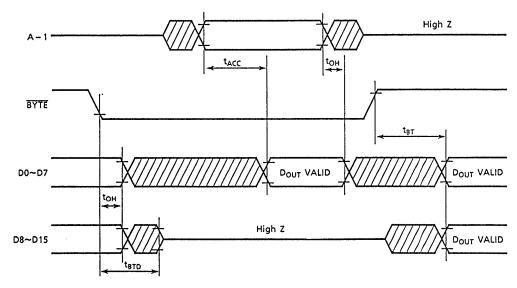




Note: $\overline{BYTE} = V_{1L}$

BYTE TRANSITION

A0~A17



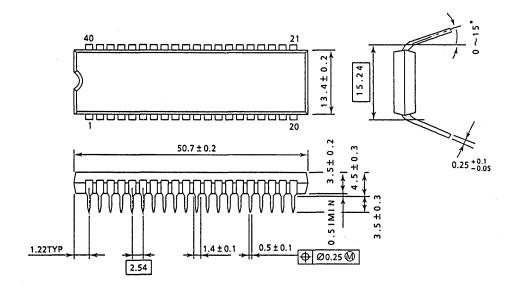
Note: \overline{CE} , $\overline{OE} = V_{IL}$

OUTLINE DRAWINGS

• Plastic DIP

DIP40-P-600

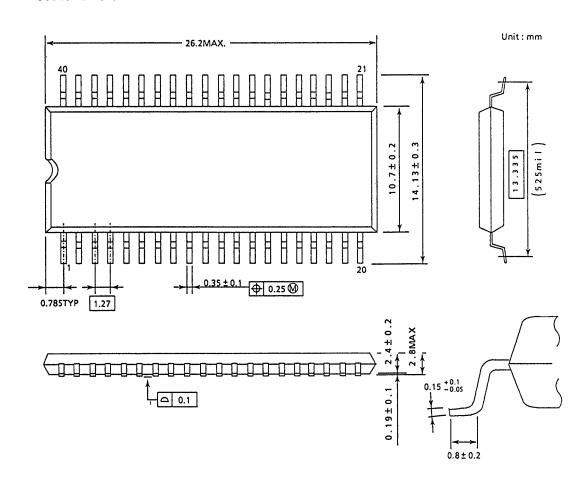
Unit:mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

• Plastic SOP SOP40-P-525



8M BIT (512K WORD \times 16 BIT/1M WORD \times 8BIT) CMOS MASK ROM

PRELIMINARY

DESCRIPTION

The TC538200P/F is a 8,388,608 bits read only memory organized as 524,288 words by 16 bits when BYTE is logical high, and is organized as 1,048,576 words by 8 bits when BYTE is logical low.

The TC538200P/F is most suitable for the program memory, data memory, and character generator.

The TC538200P/F has a programmable chip enable input CE/CE for device selection.

The TC538200P/F is packaged in a standard 600mil 42pin DIP, or 600mil 44 pin SOP.

FEATURES

• Single 5V Power Supply

Access Time : 200ns (Max.)

• Power Dissipation

Operating Current
Standby Current

Fully Static Operation

: 50mA (Max.)

: 100µA (Max.)

• All Inputs and Outputs: TTL Compatible

• Three State Outputs

• Programmable Chip Enable

42pin 600mil width Plastic DIP

• 44pin 600mil width Plastic SOP

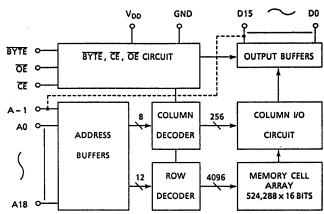
PIN CONNECTION (TOP VIEW)

		N.C. 🛚 1	✓ 44 □ N.C.
A18 🗓 1	✓ 42 D N.C.	A18 🗓 2	43 🕽 N.C.
A17 🛛 2	41 D A8	A17 [] 3	42 D A8
A7 [] 3	40 D A9	A7 [] 4	41 A9
A6 []4	39 D A10	A6 [] 5	40 D A10
A5 0 5	38 D A11	A5 [] 6	39 A11
			E
			38 A12
A3 🛚 7	36 🖟 A13	A3 🛭 8	37 [] A13
A2 []8	35 🖟 A14	A2 🛛 9	36 🛘 A14
A1 []9	34 🛮 A15	A1 [] 10	35 🛭 A15
A0 🗓 10	33 🕽 A16	A0 [11	34 D A16
CE/CE 0 11	32 BYTE	CE/CE 1 12	
GND 0 12	31 D GND	GND 0 13	
ŌĒ	30 D D15/A-1	OE 114	
		_	E
D8 🛭 15	28 D14	D8 🗓 16	
D1 🖟 16	27 🛭 D6	D1 🛘 17	28 🗓 D6
D9 🛭 17	26 D13	D9 🛚 18	27 D D13
D2 🗓 18	25 🗓 D5	D2 🗓 19	26 D5
D10 🗓 19	24 D D12	D10 1 20	
D3 0 20	23 D4	D3 Q 21	24 D4
D11 421	E	D11 22	
211 421	22 V _{DD}	V11 422	23 D V _{DD}
TC538	200P	TC	538200F

PIN NAMES

A0~A18	Address inputs
D0~D14	Data Outputs
CE/CE	Chip Enable Input
ŌĒ	Output Enable Input
D15/A-1	Data Output/Address Input
BYTE	Word, Byte selection Input
V _{DD}	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE	Œ (CE)	ŌĒ	BYTE	D0 - D7	D8 - D14	D15/A-1	Power
Read (16 Bit)	L (H)	L	н	Data Out		Active	
Read (8 Bit)	L (H)	L	L	Data Out (Lower 8bit)	High Impedance	L	Active
Read (8 Bit)	L (H)	L	L	Data Out (Upper 8bit)	High Impedance	н	Active
Output Deselect	L (H)	н	*	High Impedance			Active
Standby	н (L)	*	*	High Impedance		Standby	

 $H:V_{IH}\ L:V_{IL}\ \ ^{*}:V_{IH}\ or\ V_{IL}$

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	- 0.5~7.0	V
V _{IN}	Input Voltage	- 0.5~V _{DD}	v
V _{OUT}	Output Voltage	0~V _{DD}	V
PD	Power Dissipation	1.0/0.6*	w
T _{STG}	Storage Temperature	- 55~150	•c
T _{OPR}	Operating Temperature	0~70	° C
TSOLDER	Soldering Temperature • Time	260 · 10	*C · sec

^{*} SOP

D.C. OPERATING CONDITIONS (Ta = $0 \sim 70$ °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	٧
V _{IH}	Input High Voltage	2.2	-	V _{DD} + 0.3	٧
V _{IL}	Input Low Voltage	- 0.3	-	0.8	٧

D.C. and OPERATING CHARACTERISTICS ($Ta = 0 \sim 70$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
l _{IL}	Input Leakage Current	V _{IN} = 0~V _{DD}	-	± 1.0	μА
اده	Output Leakage Current	V _{OUT} = 0~V _{DD}		± 5.0	μА
Іон	Output High Current	V _{OH} =2.4V	- 1.0	-	mA
lor	Output Low Current	V _{OL} = 0.4V	2.0	-	mA
I _{DDS1}	- Standby Current	Œ=V _{IH}	-	2	. mA
l _{DDS2}	Standby Current	<u>CE</u> = V _{DD} − 0.2V	-	100	μА
l _{DDO1}	Operating Current	$V_{IN} = V_{IH} / V_{IL}$, $t_{cycle} = 200$ ns	-	60	mA
IDDO2	Operating Current	$V_{IN} = V_{DD} - 0.2 \text{V} / 0.2 \text{V}, t_{cycle} = 200 \text{ns}$	-	50	mA

CAPACITANCE f = 1MHz, Ta = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	TINU
C _{IN}	Input Capacitance	V _{IN} = 0V	•	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	•	12	pF

Note: This Parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($Ta = 0 \sim 70^{\circ}\text{C,V}_{DD} = 5\text{V} \pm 10\%$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
tcyc	Cycle Time	200	-	ns
†ACC	Address Access Time	_	200	ns
t _Œ	Chip Enable Access Time	-	200	ns
t _{ST}	BYTE Access Time	-	200	ns
t _{OE}	Output Enable Access Time	-	70	ns
t _{CED}	Output Disable Time from CE	_	60	ns
t _{OED}	Output Disable Time from OE	_	60	ns
t _{STD}	Output Disable Time from BYTE		60	ns
t _{ОН}	Output Hold Time	5	_	ns

: 100pF + 1TTL

A.C. TEST CONDITIONS

Output Load

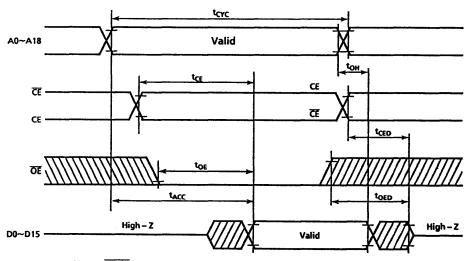
Input Levels : 0.6V , 2.4V Timing Measurement Reference Levels Input : 0.8V , 2.2V

Output: 0.8V, 2.0V

Input Rise and Fall Time : 5ns

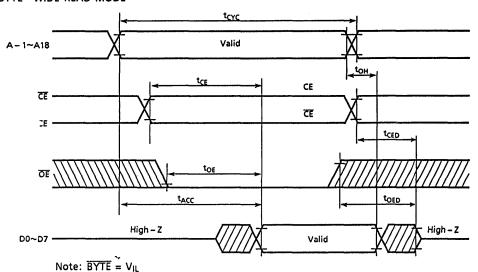
TIMING WAVEFORMS

WORD - WIDE READ MODE



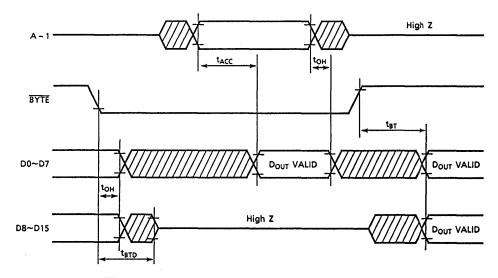
Note: BYTE = VIH

BYTE-WIDE READ MODE



BYTE TRANSITION

A0~A18



Note: $CE(\overline{CE}) = V_{IH}(V_{IL})$, $\overline{OE} = V_{IL}$

OUTLINE DRAWINGS

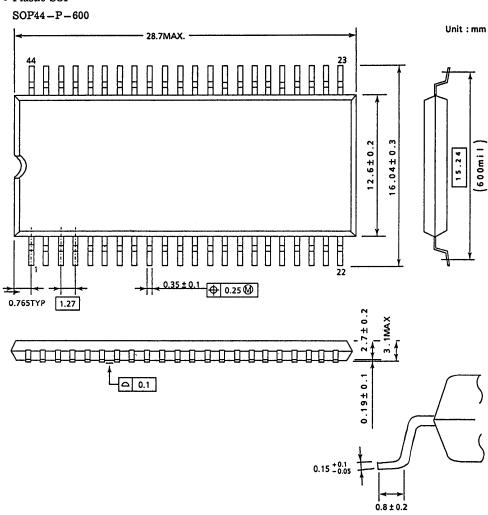
• Plastic DIP

DIP42-P-600

Unit:mm

OUTLINE DRAWINGS

• Plastic SOP



			-

16M BIT (1M WORD × 16 BIT/2M WORD × 8BIT) CMOS MASK ROM

PRELIMINARY

DESCRIPTION

The TC5316200P/F is a 16,777,216 bits read only memory organized as 1,048,576 words by 16 bits when $\overline{\text{BYTE}}$ is logical high, and is organized as 2,097,152 words by 8 bits when $\overline{\text{BYTE}}$ is logical low.

The TC5316200P/F is most suitable for the program memory, data memory, and character generator. The TC5316200P/F has a programmable chip enable input CE/\overline{CE} for device selection.

The TC5316200P/F is packaged in a standard 600mil 42pin DIP, or 600mil 44 pin SOP.

FEATURES

Single 5V Power Supply

Access Time : 200ns (Max.)

• Power Dissipation

Operating Current : 50mA (Max.)

Standby Current :

: 100µA (Max.)

All Inputs and Outputs: TTL Compatible

Three State Outputs

• Programmable Chip Enable

• 42pin 600mil width Plastic DIP

• 44pin 600mil width Plastic SOP

Fully Static Operation

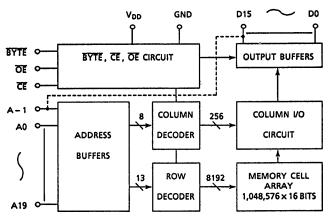
PIN CONNECTION (TOP VIEW)

A18 []	42 A19	N.C. [1 A18 [2	44 N.C. 43 A19
A17 42	41 🗓 A8	A17 🗓 3	42 🕽 A8
A7 [] 3	40 🛘 A9	A7 🛛 4	41 🗓 A9
A6 🛚 4	39 🛭 A10	A6 🛚 5	40 D A10
A5 🗓 5	38 A11	A5 []6	39 A11
A4 [6	37 D A12	A4 [7	38 D A12
A3 [7	36 D A13	A3 [8	37 D A13
A2 [] 8	35 D A14	A2 []9	36 D A14
A1 09	34 D A15	A1 010	35 D A15
A0 [] 10	33 D A16	A0 [] 11	34 D A16
CE/CE 11	32 BYTE	CE/CE 12	33 D BYTE
GND 112	31 D GND	GND 13	32 D GND
OE () 13	30 D15/A-1	OE 1 14	31 D D15/A-1
DO 114	29 0 07	DO [] 15	
	E		E
		D8 4 16	29 D14
	27 D D6	D1 17	28 🏻 D6
D9 🗓 17	26 U D13	D9 🗓 18	27 🗓 D13
D2 🛚 18	25 🛭 D5	D2 🗓 19	26 🛭 D5
D10 🗓 19	24 🛭 D12	D10 🗓 20	25 🛛 D12
D3 🗓 20	23 🖟 D4	D3 🗓 21	24 🗍 D4
D11 [21	22] V _{DD}	D11 [22	23 J V _{DD}
TC5316	200P	TC531	16200F

PIN NAMES

A0~A19	Address inputs
D0~D14	Data Outputs
CE/CE	Chip Enable Input
ŌĒ	Output Enable Input
D15/A-1	Data Output/Address Input
BYTE	Word, Byte selection Input
V _{DD}	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE	Œ (CE)	ŌĒ	BYTE	D0 - D7	D8 - D14	D15/A-1	Power
Read (16 Bit)	L (H)	L	н		Data Out		Active
Read (8 Bit)	L (H)	L	L	Data Out (Lower 8bit)	High Impedance	L	Active
Read (8 Bit)	L (H)	L	L	Data Out (Upper 8bit)	High Impedance	Н	Active
Output Deselect	L (H)	н	*	High Impedance		Active	
Standby	H (L)	*	*	High Impedance		Standby	

 $H:V_{IH} \ L:V_{IL} \ *:V_{IH} \ or \ V_{IL}$

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	- 0.5~7.0	V
V _{IN}	Input Voltage	-0.5~V _{DD}	V
V _{OUT}	Output Voltage	0~V _{DD}	٧
PD	Power Dissipation	1.0/0.6*	w
T _{STG}	Storage Temperature	- 55~150	• c
TOPR	Operating Temperature	0~70	• c
TSOLDER	Soldering Temperature · Time	260 · 10	°C · sec

^{*} SOP

D.C. OPERATING CONDITIONS (Ta = $0 \sim 70$ °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	٧
V _{IH}	Input High Voltage	2.2	-	V _{DD} + 0.3	>
VIL	Input Low Voltage	-0.3	-	0.8	v

D.C. and OPERATING CHARACTERISTICS ($Ta = 0 \sim 70^{\circ}C$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0~V _{DD}	-	± 1.0	μА
l _{LO}	Output Leakage Current	V _{OUT} = 0~V _{DD}	-	± 5.0	μА
loh	Output High Current	V _{OH} =2.4V	- 1.0	-	mA
IOL	Output Low Current	V _{OL} =0.4V	2.0	_	mA
I _{DD\$1}	Standby Current	<u>CE</u> =V _{IH}	-	2	mA
I _{DDS2}	Standby Current	<u>CE</u> =V _{DD} − 0.2V	-	100	μА
l _{DDO1}	On a setting Coursest	$V_{iN} = V_{iH} / V_{iL}$, $t_{cycle} = 200$ ns		60	mA
I _{DDO2}	Operating Current	$V_{IN} = V_{DD} - 0.2V / 0.2V_{cycle} = 200$ ns	-	50	mA

CAPACITANCE f = 1MHz, Ta = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
CiN	Input Capacitance	V _{IN} = 0V	-	10	рF
Cout	Output Capacitance	V _{OUT} = 0V	-	12	pF

Note: This Parameter is periodically sampled and is not 100% tested.

TC5316200P/F

A.C. CHARACTERISTICS (Ta = $0\sim70^{\circ}$ C, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
tcyc	Cycle Time	200	-	NS
tACC	Address Access Time	-	200	ns
t _{CE}	Chip Enable Access Time	-	200	ns
t _{at}	BYTE Access Time	_	200	ns
[‡] OE	Output Enable Access Time	_	70	ns
†CED	Output Disable Time from CE	-	60	ns
^t OED	Output Disable Time from OE	-	60	ns
t _{BTD}	Output Disable Time from BYTE	-	60	ns
t _{ОН}	Output Hold Time	5	_	ns

A.C. TEST CONDITIONS

Output Load

Input Levels

Timing Measurement Reference Levels

: 100pF + 1TTL

: 0.6V , 2.4V Input : 0.8V , 2.2V

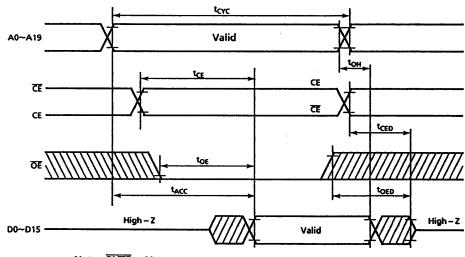
Output: 0.8V, 2.0V

: 5ns

TIMING WAVEFORMS

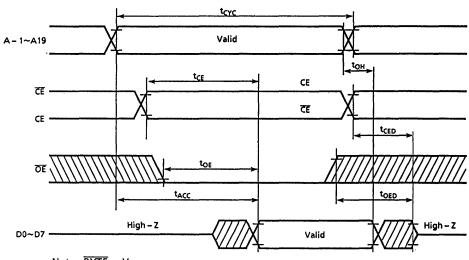
WORD-WIDE READ MODE

Input Rise and Fall Time



Note: BYTE = VIH

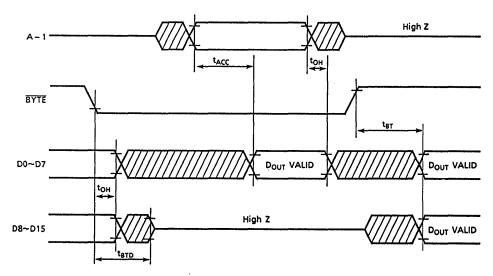
BYTE-WIDE READ MODE



Note: $\overline{BYTE} = V_{1L}$

BYTE TRANSITION



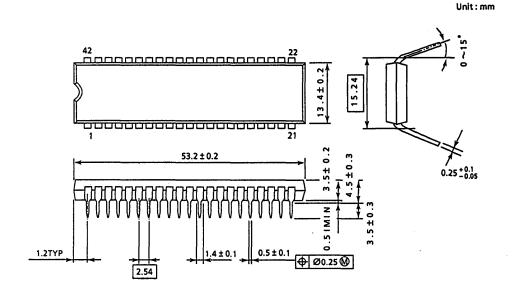


Note: $CE(\overline{CE}) = V_{IH}(V_{IL})$, $\overline{OE} = V_{IL}$

OUTLINE DRAWINGS

• Plastic DIP

DIP42-P-600.



OUTLINE DRAWINGS

• Plastic SOP SOP44-P-600 Unit:mm 28.7MAX. 12.6 ± 0.2 15.24 (600mil) **⊕** 0.25 0.765TYP 1.27 0.19 ± 0.1 **△** 0.1

Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

0.8 ± 0.2

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			-
•			

4M BIT (512K WORD × 8 BIT) CMOS MASK ROM

PRELIMINARY

DESCRIPTION

The TC534000AP/AF is a 4,194,304 bits read only memory organized as 524,288words by 8bits. The TC534000AP/AF is fabricated using Toshiba's advanced CMOS technology which provides the high speed and low power features with access time of 150ns, an operation current of 40mA at 6.7MHz and a standby current of 20µA.

The TC534000AP/AF has one programmable chip enable input CE/CE for device selection. The TC534000AP/AF is packaged in a standard 600mil 32pin DIP or 525mil 32pin SOP.

FEATURES

Single 5V Power Supply

Access Time: 150ns (Max.) V_{DD}=5V±10%

• Power Dissipation

Operating Current: 40mA (Max.)

Standby Current : 20µA (Max.)

• All Inputs and Outputs: TTL Compatible

• Three State Outputs

• Fully Static Operation

• Programmable Chip Enable

Package Plastic DIP: TC534000AP
 Plastic FP: TC534000AF

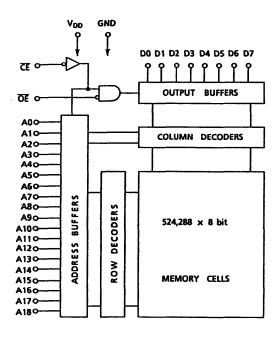
PIN CONNECTION

	- 1		_		7	
N.C.	d	1	\smile	32	þ	V _{DD}
A16	d	2		31		A18
A15	d	3		30	b	A17
A12	d	4		29	b	A14
A7	d	5		28	b	A13
A6	d	6		27	b	A8
A5		7		26		A9
A4	d	8				A11
A3	q	9		24	00000	ŌĒ
A2	þ	10		23	þ	A10
A1	q	11		22	þ	CE/CE
A0	q	12		21	Þ	D7
D0	þ	13		20	þ	.D6
D1	q	14		19	þ	D5
D2	Q	15		18	þ	D4
GND	þ	16		19	þ	D3
	L				ı	-

PIN NAMES

A0~A18	Address inputs
D0~D7	Data Outputs
OE .	Output Enable Input
CE/CE	Chip Enable Input
V _{DD}	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



TC534000AP/AF

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	- 0.5~7.0	٧
V _{IN}	Input Voltage	- 0.5~V _{DD}	٧
Vout	Output Voltage	0~V _{DD}	V
Po	Power Dissipation	1.0/0.6*	w
T _{STG}	Storage Temperature	55~150	•c
TOPR	Operating Temperature	0~70	•c
TSOLDER	Soldering Temperature - Time	260 · 10	°C · sec

Note: * Plastic FP.

D.C. OPERATING CONDITIONS (Ta = $0 \sim 70$ °C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.5	v
V _{IH}	Input High Voltage	2.2	V _{DD} + 0.3	>
V _{IL}	Input Low Voltage	- 0.3	0.8	V

D.C. and OPERATING CHARACTERISTICS ($V_{DD} = 5V \pm 10\%$, $Ta = 0 \sim 70^{\circ}C$)

SYMBOL	PARAMETER	CONDITIONS	CONDITIONS MIN.		UNIT
1 _{IL}	Input Leakage Current	V _{IN} = 0~V _{DD}	-	± 1.0	μΑ
lo	Output Leakage Current	CE=VIH, VOUT=0~VDD	-	± 5.0	μΑ
Гон	Output High Current	V _{OH} =2.4V	- 1.0	-	mA
lor	Output Low Current	V _{OL} =0.4V	2.0	-	mA
loosi	Standby Current	CE=V _{IH}	-	2	mA
I _{DD\$2}	Standay Carrent	$\overline{CE} = V_{DD}$ and $V_{IN} = OV(V_{DD})$	_	20	μА
l _{DDO1}	Operating Current	$V_{IN} = V_{IH} / V_{IL}$, $t_{cycle} = 150 ns$		50	mA
IDDO2	Operating outlett	$V_{IN} = V_{DD}/0V$, $t_{cycle} = 150$ ns	_	40	mA

CAPACITANCE

SYMBOL PARAMETER		CONDITIONS	MIN.	MAX.	UNIT	
C _{IN}	Input Capacitance	f = 1MHz , Ta = 25°C	-	10	рF	
C _{OUT}	Output Capacitance	f = 1MHz , Ta = 25°C	-	10	pF	

Note: This Parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t _{ACC}	Access Time	-	150	ns
t _{CE}	Chip Enable Access Time	-	150	ns
t _{OE}	Output Enable Access Time	_	70	ns
t _{CED}	Output Disable Time from CE	0	60	ns
t _{OED}	Output Disable Time from OE	0	60	ns
t _{он}	Output Hold Time	10	-	ns
t _{CYC}	Cycle Time	150	_	ns

A.C. TEST CONDITIONS

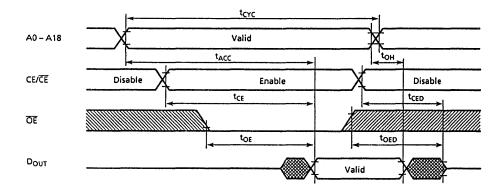
Output Load : 100pF + 1TTL

Input Levels : 0.6V , 2.4V

Timing Measurement Reference Levels Input : 0.8V, 2.2V Output : 0.8V, 2.0V

Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



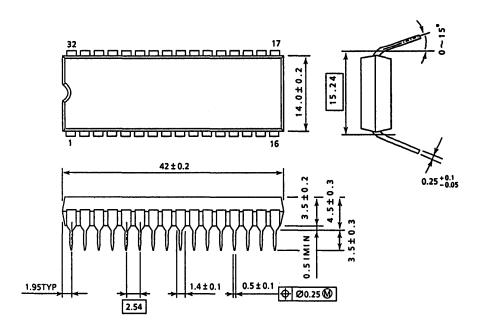
OPERATION MODE

MODE	CE (CE)	ŌĒ	A0~A18	Outputs	Power
Read	L(H)	L	Valid	Data Out	Operating
Standby	H(L)	*	*	High-Z	Standby
Output Deselect	L(H)	н	*	High-Z	Operating

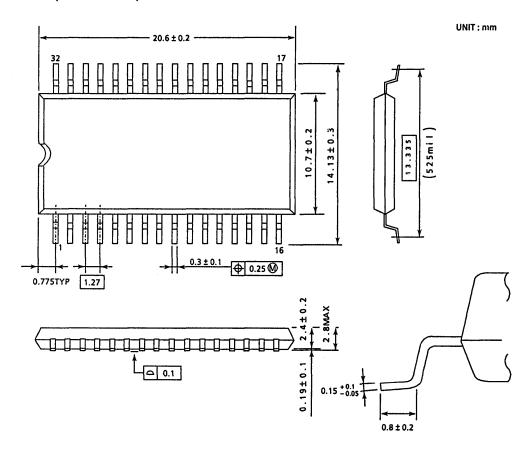
H: VIH L: VIL *: VIH or VIL

OUTLINE DRAWINGS
Plastic DIP (DIP32 - P - 600)

UNIT: mm



OUTLINE DRAWINGS
Plastic FP (SOP32 - P - 525)



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TC53H1024P-85

TARGET

1M BIT (64K WORD x 16 BIT) HIGH-SPEED CMOS MASK ROM SILICON GATE CMOS

DESCRIPTION

The TC53H1024P is a high-speed 1,048,576 bits read only memory organized as 65,536 words by 16 bits with a low bit cost, thus being suitable for use in program memory of microprocessors.

The TC53H1024P is molded in a 40 pin standard plastic package, 0.6 inch in width.

FEATURES

TC53H1024P	-85
Access Time (max)	85ns
Power Dissipation Operation Current (max)	60mA
Power Dissipation Standby Current (max)	100uA

- All Inputs and Outputs: TTL Compatible
- · Three State Outputs
- · Fully Static Operation
- Pin Compatible with 1M High-Speed EPROM TC57H1024D
- Package

Plastic DIP: TC53H1024P

· Single 5V Power Supply

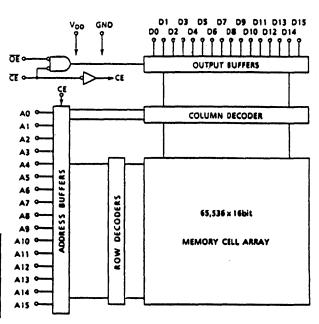
PIN CONNECTION



PIN NAMES

A0-A15	Address inputs
D0~D15	Data Outputs
ŌΕ	Output Enable Input
35	Chip Enable Input
Vop	Power Supply
GND	Graund
N.C.	No Connection

BLOCK DIAGRAM



			f .	
			· 1	
				-

TC58257AP/AF 32,768 WORD x 8 BIT ELECTRICALLY CHIP ERASABLE AND PROGRAMMABLE READ ONLY

PRELIMINARY

DESCRIPTION

TC58257AP/AF is a 32,768 word × 8 bit electrically chip erasable and programmable read only memory, and molded in a 28 pin plastic package. The TC58257AP/AF's access time is 170ns/200ns/250ns, and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics are the same as U.V.EPROM TC57256AD's. For program operation, the programming is achieved by using the high speed programming mode. The TC58257AP/AF has an electrically chip erasing mode which can erase whole bits at the same time.

FEATURES

 Peripheral circuit: CMOS Memory cell : NMOS

• Fast access time: TC58257AP/AF-17LV 170ns TC58257AP/AF-20LV 200ns

TC58257AP/AF-25LV 250ns

 Low power dissipation Active: 30mA/5.9MHz

Standby: 100µA

· Full static operation

· High speed programming mode

· Electrically chip erasing mode

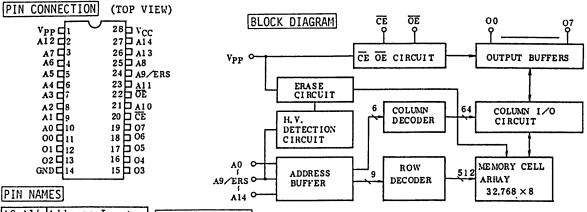
· Inputs and outputs TTL compatibility

 Pin compatible with MASK ROM TC53257P, TMM23256P, EPROM TMM27256D/AD, and TC57256D/AD, one time PROM TMM24256P/AP/AF and TC54256P/AP/AF

· Standard 28 pin DIP

plastic package : TC58257AP

• Plastic Flat package: TC58257AF



A0~A14	Address Inputs
00 ∿ 07	Output (Input)
ČĒ	Chip Enable Input
ŌĒ	Output Enable Input
A9/ERS	Address And Erase Control Input
V _{PP}	Program And Erase Power Supply Voltage
Vcc	VCC Power Supply Voltage
GND	Ground

MODE SELECTION								
Pin	CE	ŌĒ	А9	VPP	Vсс	A0∿A8 (10∿14)	00 ∿ 07	Power
Read	L	L	311			**	Data Output	Active
Output Deselect	*	Н	×	5V	50	*	High Impedance	
Standby	Н	*	*	<u> </u>		**	High Impedance	Standby
Program	L	Н	*			×	Data Input	!
Program Inhibit	н	*	яt	12V	5V	*	High Impedance	Active
Program Verify	L	L	*	l		*	Data Out	
Chip Erase	L	Н	12V	1 2 V	50	3%	Don't Care	
Chip Erase Inhibit	H	*	120	124	٥,	*	High Impedance	Active
*: VIH or VIL								

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
VCC	V _{CC} Power Supply Voltage	-0.6 ~ 7.0	v
V _{PP}	Program Supply Voltage	-0.6 ~ 14.0	v
VIN	Input Voltage	-0.6 ~ 7.0	v
V _{I/O}	Input/Output Voltage	-0.6 ∿ V _{CC} +0.5	v
PD	Power Dissipation	1.5	W
TSOLDER	Soldering Temperature • Time	260 • 10	°C • sec
TSTG	Storage Temperature	-65 ∿ 125	°C
TOPR	Operating Temperature	-10 ~ 70	°C
NEW	Erase Write Endurance	100	Cycles

READ OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	V _{CC} +0.3	V
VIL	Input Low Voltage	-0.3	-	0.8	V
VCC	V _{CC} Power Supply Voltage	4.50	5.00	5.50	٧
V _{PP}	VPP Power Supply Voltage	V _{CC} -0.6	V _{CC}	V _{CC+0.6}	v

DC AND OPERATING CHARACTERISTICS (Ta=-10 ~ 70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
ILI	Input Current	$V_{IN}=0 \sim V$	cc ·	-	-	±10	μA
I _{CC01}	Operating Current	CE-OV	f=5.9MHz	-	_	30	
I _{CC02}	operating current		f=1MHz	-	-	10	mA
I _{CCS1}	Chandha Canana	CE=VIH		-	-	1	mA
I _{CCS2}	Standby Current	CE=V _{CC} -().2V	-	-	100	μА
v _{OH}	Output High Voltage	I _{OH} =-400μA		2.4	-	-	v
VOL	Output Low Voltage	I _{OL} =2.ln	nA	-	-	0.4	v
I _{PP1}	VPP Current	V _{PP} =V _{CC} -0.6~V _{CC} +0.6		-	-	±10	μA
Ī _{LO}	Output Leakage Current	V _{OUT} =0.4 ∿ V _{CC}		-	-	- ±10	μА

AC CHARACTERISTICS $(Ta=-10 \sim 70^{\circ}C, V_{CC}=5V\pm10\%, V_{PP}=V_{CC}\pm0.6V)$

arn			-17		-20		-	IINIT TO	
SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT
tACC	Address Access Time	CE=OE=VIL	-	170	-	200	_	250	ns
t _{CE}	CE to Output Valid	ŌĒ=V _{IL}	-	170	-	200	-	250	ns
t _{OE}	OE to Output Valid	CE=VIL	-	70	-	70	-	100	ns
t _{DF1}	CE to Output in High-Z	OE=VIL	0	60	0	60	0	90	ns
t _{DF2}	OE to Output in High-Z	CE=V _{IL}	0	60	0	60	0	90	ns
tOH	Output Data Hold Time	CE=OE=VIL	0	-	0	1	0	-	ns

AC TEST CONDITIONS

· Output Load

1 TTL Gate and C_L=100pF

· Input Pulse Rise and Fall Times · Input Pulse Levels

: 10ns Max. : 0.45V ~ 2.4V

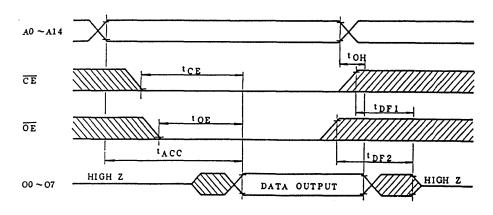
Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CIN	Input Capacitance	V _{IN} =OV	-	4	6	pF
COUT	Output Capacitance	V _{OUT} =0V	-	8	12	pF

This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	V _{CC} +1.0	V
VIL	Input Low Voltage	-0.3	-	0.8	V
v _{cc}	VCC Power Supply Voltage	4.5	5.0	5.5	V
V _{PP}	VPP Power Supply Voltage	11.5	12.0	12.5	V

DC AND OPERATING CHARACTERISTICS (Ta=-10 \sim 70°C, V_{CC} =5.0V±10%, V_{PP} =12.0V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ILI	Input Current	V _{IN} =0 ~ V _{CC}	-	-	10	μA
VOH	Output High Voltage	I _{OH} =-400μA	2.4	-	-	v
VOL	Output Low Voltage	I _{OL} =2.lmA	-	-	0.4	v
ICC	VCC Supply Current	-	-	-	40	mA
I _{PP2}	VPP Supply Current	VPP=13.0V	_	-	50	mA

AC PROGRAMMING CHARACTERISTICS (Ta=-10 ~ 70°C, V_{CC}=5.0V±10%, V_{PP}=12.0V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	-	2	-	-	μs
t _{AH}	Address Hold Time	-	2	-	-	μS
tCES	CE Setup Time	-	2	-	-	μs
tCEH	CE Hold Time	-	2	-	-	μs
toES	$\overline{\text{OE}}$ Setup Time	-	2	-	-	μs
t _{OEH}	OE Hold Time	-	2	-	-	μs
tDS	Data Setup Time	-	2	-	_	μs
^t DH	Data Hold Time	-	2	-	-	μs
tvs	V _{PP} Setup Time	-	2		-	μs
tPW	Initial Program Pulse Width	CE=VIL, OE=VIH	0.95	1.0	1.05	ms
t _{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
tDV	CE to Output Valid	ŌĒ=V _{IL}	-	-	1	μs
t _{DF1}	CE to Output in High-Z	ŌĒ=V _{IL}	-	_	150	ns

AC TEST CONDITIONS

• Output Load : 1 TTL Gate and $C_{\rm L}$ (100pF)

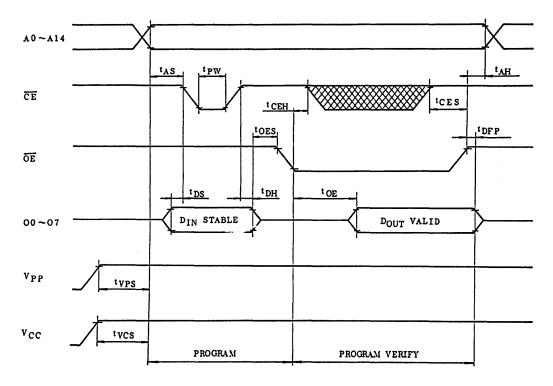
Input Pulse Rise and Fall Times : 10ns Max.
 Input Pulse Levels : 0.45V \(\cdot 2.4V \)

• Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value \mathbf{X} .

TIMING WAVEFORMS (PROGRAM)

 $(V_{CC}=5.0V\pm10\%, V_{PP}=12.0V\pm0.5V)$



- Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
 - 2. Removing the device from socket and setting the device in socket with $V_{\rm PP}$ =12.0V may cause permanent damage to the device.
 - 3. The Vpp supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{pp} terminal. When the switching pulse voltage is applied to the V_{pp} terminal, the overshoot voltage of its pulse should not exceed 14V.

ERASE OPERATION

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.2	-	V _{CC} +1.0	v
VIL	Input Low Voltage	-0.3	-	0.8	V
v _{CC}	VCC Power Supply Voltage	4.5	5.0	5.5	v
VPP	Vpp Power Supply Voltage	11.5	12.0	12.5	V
VIHH	Input High Voltage	11.5	12.0	12.5	v

DC AND OPERATING CHARACTERISTICS (Ta=-10 \sim 70°C, V_{CC} =5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ILI	Input Current	V _{IN} =0 ~ V _{CC}	-	-	±10	μA
I _{LIE}	A9/ERS Input Current	A9/ERS=0 ~ V _{IHH}	-	-	±100	μA
ICC	V _{CC} Supply Current	-	_	-	40	mA
I _{PP2}	Vpp Supply Current	V _{PP} =12.5V	-	,	50	mA

AC ERASING CHARACTERISTICS (Ta=-10 \sim 70°C, V_{CC} =5V±10%, V_{PP} =12.0V±0.5V)

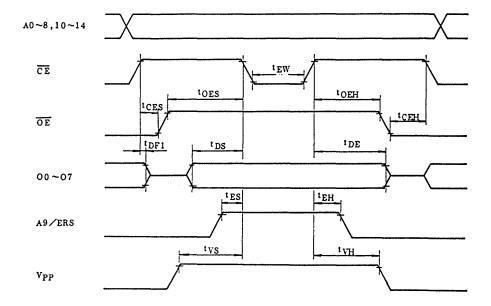
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tCES	CE Setup Time	-	2	-	-	μs
t _{CEH}	CE Hold Time	-	2	-	-	μs
tOES	$\overline{\text{OE}}$ Setup Time	-	2	-	-	μs
tOEH	OE Hold Time	-	500	-	-	μs
t _{DS}	Data Setup Time	-	2	-	-	μs
^t DH	Data Hold Time	-	500	_	_	μs
tvs	VPP Setup Time	_	2	_	-	μs
t _{VH}	VPP Hold Time	-	500	-	-	μs
t _{ES}	A9/ERS Setup Time	-	2	-	•	рs
tEH	A9/ERS Hold Time	-	2	-	•	μѕ
t _{EW}	Erase Pulse Width	CE=VIL, OE=VIH, A9=VIHH	1950	2000	2050	ms
t _{DF1}	CE to Output in High-Z	OE=VIL	-	-	150	ns

Input Pulse Rise and Fall Time: 10ns Max.

Input Pulse Levels : 0.45V \(2.4V \)

TIMING WAVEFORMS (ERASE)

 $(V_{CC}=5V\pm10\%, V_{PP}=12.0V\pm0.5V)$



- Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
 - 2. Removing the device from socket and setting the device in socket with $V_{\rm PP}{=}12.0V$ may cause permanent damage to the device.
 - 3. The Vpp supply voltage is permitted up to 14V for erase operation. So the voltage over 14V should not be applied to the Vpp terminal. When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its pulse should not exceed 14V.

Read	Pin	CE	ŌĒ	А9	VPP	vcc	00 ∿ 07	Power	
_	Read	L	L	*			Data Out	Active	
Read Operation	Output Deselect	*	н	*	5V	5V	High Impedance	Active	
Operation	Standby	н	*	*	1		High Impedance	Standby	
	Program	L	Н	*			Data In	Active	
Program	Program Inhibit	Н	*	*	12V	5V	High Impedance		
Operation	Program Verify	L	L	*]		Data Out		
Erase	Erase	L	Н	1017	1011	F.,	Don't Care		
Operation	Erase Inhibit	Н	3°C	12V	12V	5V	High Impedance	Active	

Note: H; VIH, L; VIL, *; VIH or VIL

READ MODE

The TC58257AP/AF has two control functions. The chip enable (\overline{CE}) controls the operat power and should be used for device selection. The output enable (\overline{OE}) controls the output buffers, independent of device selection. Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The \overline{CE} to output valid (t_{CE}) is equal to the address access time (t_{ACC}) . Assuming that $\overline{CE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of \overline{OE} .

OUTPUT DESELECT MODE

Assuming that $\overline{\text{CE}}=\text{V}_{\text{IH}}$ or $\overline{\text{OE}}=\text{V}_{\text{IH}}$, the outputs will be in a high impedance state. So two or more TC58257AP/AF's can be connected together on a common bus line. When $\overline{\text{CE}}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC58257AP/AF has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC58257AP/AF is placed in the standby mode which reduce the operating current to $100\mu\text{A}$ by applying MOS-high level (VCC) and then the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC58257AP/AF are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC58257AP/AF is in the programming mode when the Vpp input is at 12V and $\overline{\text{CE}}$ is at TTL-Low under $\overline{\text{OE}}$ =VIH. The TC58257AP/AF can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check if desired data is correctly programmed on the programmed bits. The verify is accomplished with \overline{OE} at V_{TL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.0V) is applied to V_{PP} terminal, a high level \overline{CE} input inhibits the TC58257AP/AF from being programmed. Programming of two or more TC58257AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for \overline{CE} may be commonly connected, and a TTL low level program pulse is applied to the \overline{CE} of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage ($\pm 12.0V$) is applied to the Vpp terminal with Vcc=5.0V. The programming is achieved by applying a single TTL low level $\pm 100\mu$ s pulse to the $\overline{\text{CE}}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of $\pm 100\mu$ s is applied and then the programmed data is verified. The should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{\rm CC} = V_{\rm PP} = 5V$.

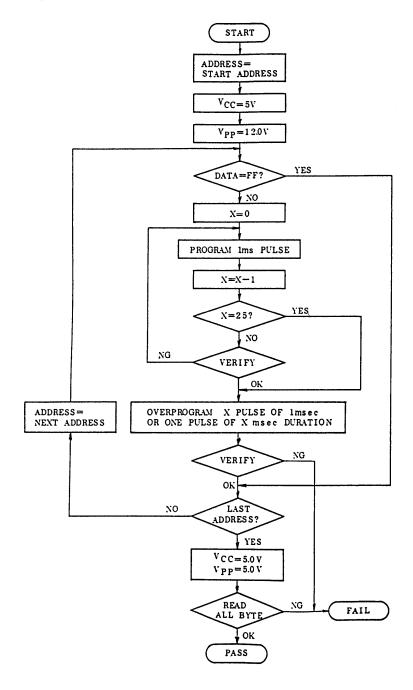
CHIP ERASE MODE

The TC58257AP/AF is in chip erase mode when the Vpp input is 12.0V and $\overline{\text{CE}}$ is at TTL-Low level under the condition of A9=12V, $\overline{\text{OE}}$ =V_{IH}. The chip erase pulse width is only 1 sec. Once chip is erased, all bits of the device are in "1" state.

ERASE INHIBIT

Under the condition that the erase voltage (12.0V) is applied to Vpp terminal and 12V is to A9 input, TTL-High level $\overline{\text{CE}}$ input inhibits the TC58257AP/AF from being erased.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TC58257AP/AF which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from TC58257AP/AF by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to $V_{\rm IL}$ in read operation. Data output in this condition is the manufacturer code. Device code is identified when address A0 is set to

 V_{IH} . These two codes possess an odd parity with the parity bit of MSB (07). The following table shows the electric signature of TC58257AP/AF.

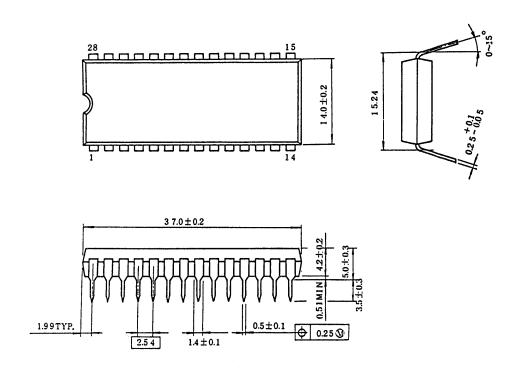
PINS	A0	07	06	05	04	03	02	01	00	HEX.
SIGNATURE	(10)	(19)	(18)	(17)	(16)	(15)	(13)	(12)	(11)	DATA
Manufacture Code	VIL	1	0	0	1	1	0	0	0	98
Device Code	VIH	0	0	1	0	0	1	0	1	25

Notes: A9=12V±0.5V

A1 \sim A8, A10 \sim A14, \overline{CE} , \overline{OE} = V_{IL}

OUTLINE DRAWINGS (TC58257AP)

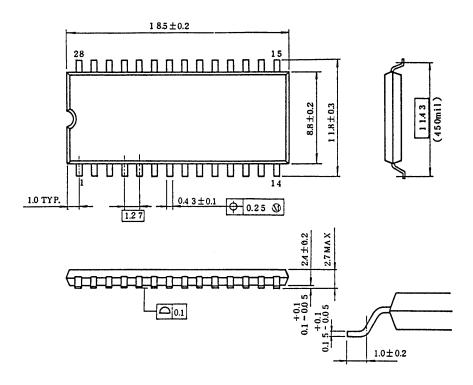
Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS (TC58257AF)

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

TC58F1000P/F/J 131,072WORD x 8BIT CMOS FLASH E² PROM

DESCRIPTION

The TC58F1000P/F/J is a 1,048,576 bits, Flash Electrically Erasable and Programmable Read Only Memory (FE²PROM) organized as 131,072 words by 8 bits. The TC58F1000P/F/J is fabricated by using advanced CMOS technology which provides the high speed and low power features with access times of 150ns/200ns, an operating current of 30mA at 6.7 MHz and a standby current of 100pA.

The TC58F1000P/F/J features a command control mode and an EPROM compatible mode for programming and erasing. The command control mode is used for in-system programming controlled by the MPU timing. A specific software sequence must be executed to enable the program, program-verify, chip-erase, block-erase, erase-verify, signature read and mode reset operations. The EPROM compatible mode is used for programming and erasing with a conventional EPROM programmer. The programming time is 14-seconds and the erasing time is only 1-second. The TC58F1000P/F/J is also provided with a block-erase feature. The programming time of 1 block (4K byte) is only 0.5-second.

The TC58F1000P/F/J has a JEDEC standard pinout configuration and is packaged in either a 32-pin plastic DIP, 32-pin flat package (SOP) or 32-pin SOJ.

FEATURES

Access time : 150ns/200ns

Power dissipation

Operating : 30mA

Standby : 100µA

Erase/Write endurance

100 cycles

10,000 cycles (Option)

• High-speed programming

14 second / chip 0.5 second / block • Electrical erase mode

Chip erase 1 second
Block erase 1 second
(Block size: 4K Byte × 32 blocks)

Package options

suffix "P": 32-pin Plastic DIP

suffix "F": 32-pin Plastic flat package (SOP)

suffix "J": 32-pin Plastic SOJ

Program / Erase mode
 Command control mode
 EPROM compatible mode

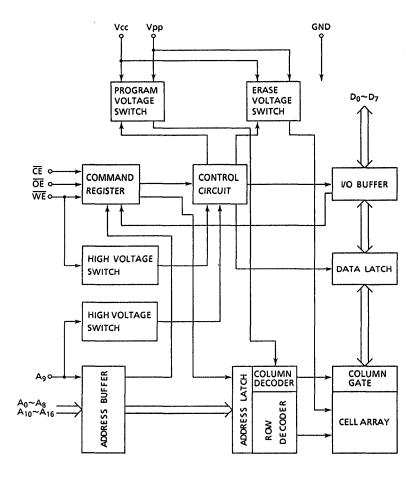
PIN CONNECTION (TOP VIEW)

Vpp	d	1	$\overline{\mathcal{C}}$	32	þ	Vcc
A16		2		31	þ	WĒ
A15	d	3		30	þ	N.C.
A12	4	4		29	þ	A14
Α7	d	5		28	þ	A13
A6	d	6		27	þ	A8
A5	9	7		26	þ	Α9
A4	þ	8		25	þ	A11
A3	þ	9		24	þ	ŌĒ
A2	þ	10				A10
Α1	d	11		22	þ	CE
A0	9	12		21	þ	D7
D0	d	13		20	þ	D6
D1	þ	14		19	þ	D5
D2	d	15		18	þ	D4
GND	þ	16		17	þ	D3

PIN NAMES

	· · · · · · · · · · · · · · · · · · ·
A0~16	Address input
D0~7	Data input/output
CE	Chip enable
ŌĒ	Output enable
WĔ	Write enable/EPROM mode switch
N.C.	NO connection
V _{PP}	Program and erase power Supply
V _{CC}	Power Supply
GND	Ground

BLOCK DIAGRAM



 $\mathcal{M}_{\mathbf{i}}$

OPERATING MODE

<Command Control Mode>

① WE Control

MODE		WE	CE	ŌĒ	V _{PP}	Vcc	D0~7	Power
	Read	Н	L	L			Data Output	
Read	Output Deselect	*	*	н	0V~V _{CC} or 12V	5V	High - Z	Active
	Standby	*	н	*	1 120	l	-	Standby
Command Input Program or Erase Program Verify or Erase Verify Signature Read		7.5	L	н			Data Input	
		н * *		*		5V	**	Active
		н	L	L	12V	5 V	Data Output	Active
		н	L	L	}		Code Output	7

Note: $*: V_{IH}$ or V_{IL} , $H: V_{IH}$, $L: V_{IL}$

**: Data Input or Data Output or High-Z

② CE Control

MODE		WE	ζĒ	ŌĒ	V _{PP}	V _{CC}	D0~7	Power
	Read	н	L	L			Data Output	
Read	Output Deselect	*	*	н	0V~V _{CC} or 12V	5∨	High - Z	Active
	Standby	*	Н	*	1 120			Standby
Command	Command Input		4	Н			Data Input	
Program or Erase Program Verify or Erase Verify Signature Read		Н	*	*	124	r.v.	**	
		н	L	L	1,2V	5V	Data Output	Active
		н	L	L			Code Output	1

Note: $*:V_{III}$ or V_{IL}

**: Data Input or High-Z

<EPROM Compatible Mode>

M	IODE	A9	WE	ĈĒ	ŌĒ	V _{PP}	V _{CC}	D0~7	Power
	Read	*	н	L	L			Data Output	
Read	Output	*	* * H 0V~VCC		0∨~∨ _{cc}			Active	
	Deselect	*	L	*	*	or 12V	5∨	High - Z]
	Standby	*	*	н	*	120			Standby
	Program	*	V _{WE}	L	н			Data Input	
Program	Program Inhibit	*	V _{WE}	н	*	12V	5∨	High – Z	Active
	Program Verify	*	V _{WL}	*	L			Data Output	
Erase	Erase	V _{ID}	VwE	L	н	12V	5V	*	Active
(Chip Erase)	Erase inhibit	V _{ID}	V _{WE}	Н	*	120	34	High Z	Active
Signature Rea	ad	V _{ID}	н	L	L	0V~V _{CC} or 12V	5∨	Code Output	Active

Note : *: V_{IH} or V_{IL} , $H:V_{IH}$, $L:V_{IL}$

 $V_{\rm ID}$, $V_{\rm WE} = 12V$

TC58F1000P/F/J-15 TC58F1000P/F/J-20

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
Vcc	Power Supply Voltage	- 0.6~7.0	V
V _{PP}	Program / Erase Supply Voltage	-0.6~14.0	٧
V _{IN}	Input Voltage	- 0.6~7.0	٧
V _{1/O}	Input/Output Voltage	- 0.6~V _{CC} + 0.5	٧
P _D	Power Dissipation	1.0/0.6*	w
TSOLDER	Soldering Temperature · Time	260-10	°C·sec
T _{STG}	Storage Temperature	- 55~150	°C
T _{OPR}	Operating Temperature	0~70	°C
N _{EW}	Erase Write Endurance	100 / 10000**	Cycle
V _{ID} /V _{WE}	Input Voltage (A9/WE)	-0.6~13.5	v

Note: * Plastic FP & Plastic SOJ

** 10000 cycle is optional

D.C. RECOMMENDED OPERATING CONDITION ($Ta = 0 \sim 70^{\circ}C$)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
V _{CC}	Vcc Power Supply Voltage	4.5	5.5	
V _{IH}	Input high Voltage	2.2	V _{CC} + 0.3	
V _{IL}	Input Low Voltage	- 0.3	0.8	
V _{ID}	A9 Pin Identifier Mode Voltage	11.4	12.6	l v
V _{WE}	WE Pin EPROM Command Mode Switch Voltage	11.4	12.6	
	V _{PP} Power Supply Voltage (Read Operation and Signature Read Operation)	0	12.6	
V _{PP}	V _{PP} Power Supply Voltage (Program, Erase, and Verify Operation)	11.4	12.6	

D.C. AND OPERATING CHARACTERISTICS ($Ta=0\sim70^{\circ}C$, $VCC=5.0V\pm10\%$, $VPP=12.0V\pm5\%$)

SYMBOL	PARAMETER		TEST CONDITION	MIN	MAX	UNIT
ili	Input Leakage Current		0V≦V _{IN} ≦V _{CC}	-	± 10	
lro	Output Leakage Current		0V≦ V _{OUT} ≦ V _{CC}	_	± 10	μΑ
V _{ОН}	Output High Voltage		I _{OH} = - 0.400mA	2.4	_	V
V _{OL}	Output Low Voltage		I _{OL} = + 2.10mA	-	0.4	V
l _{CC1}	Output High Voltage Output Low Voltage V _{CC} Supply Current (Read / Verify / Signature Read Operation) V _{CC} Supply Current (Program / Erase Operation) V _{CC} Standby Current (Read Operation) V _{PP} Supply Current		$V_{IN} = V_{IH} / V_{IL}$, $I_{OUT} = 0$ mA $t_{cycle} = 150$ ns	-	30	
I _{CC2}	V _{CC} Supply Current (Program / Erase Operation)		$V_{IN} = V_{IH} / V_{IL}$, $I_{OUT} = 0$ mA $t_{cycle} = 90$ µs	_	30	mA
I _{CCS1}	V _{CC} Standby Current		CE = V _{IH}	-	1	mA
Iccs2	(Program / Erase Operation) V _{CC} Standby Current		Œ = V _{CC} − 0.20V	-	100	μА
	I _{PP1} V _{PP} Supply Current (Read / Verify / Signature Read Operation)		$0V \le V_{PP} \le V_{CC} + 0.6V, V_{IN} = V_{IH} / V_{IL}$		± 10	
I _{PP1}			11.4V ≤ V _{PP} ≤ 12.6V, V _{IN} = V _{IH} / V _{IL}	- 200		μΑ
	V _{PP} Supply Current	Program	11.4V ≦ V _{PP} ≦ 12.6V	-	50	
lpp2		Erase	V _{IN} = V _{IH} / V _{IL}	-	30	mA
ماا	A9 Pin Identifier Mode Current		11.4V ≦ V _{ID} ≦ 12.6V	-	200	
IWE	WE Pin EPROM Compatible Mode Swite	h Current	11.4V ≤ V _{WE} ≤ 12.6V	-	200	μΑ

A.C. CHARACTERISTICS

1. READ OPERATION ($Ta=0~70^{\circ}C$, $V_{CC}=5.0V\pm10\%$, $V_{PP}=0V~V_{CC}$ or 12.0V $\pm5\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t _{RC}	Read Cycle Time	150/200*	-	-	
t _{ACC}	Address Access Time	-	-	150/200*	
t _{CE}	Chip Enable Access Time	-	_	150/200*	
t _{OE}	Output Enable Access Time	- 1	-	70	
t _{CEE}	Chip Enable to Output in Low-Z	0	_	_	ns
t _{OEE}	Output Enable to Output in Low-Z	0	-	-	
t _{OH}	Output Data Hold Time	0	-	- '	
t _{DF1}	Chip Enable to Output in High-Z	_	_	60	
t _{DF2}	Output Enable to Output in High-Z	_	-	60	

Note: * 150ns for TC58F1000P/F/J-15 200ns for TC58F1000P/F/J-20

A.C. TEST CONDITIONS

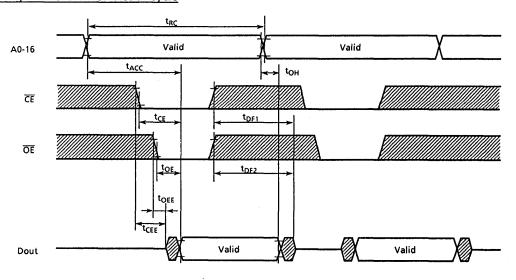
• Output Load : 1 TTL Gate and C_L (100pF)

• Input Pulse Rise and Fall Time (10%~90%) : 5ns

• Input Pulse Levels : 0.45V to 2.40V • Timing Measurement Reference Levels Input : 0.80V/2.20V

Output : 0.80V/2.00V

Timing Waveform of Read Cycle



2. COMMAND CONTROL OPERATION ($Ta=0\sim70^{\circ}C$, $V_{CC}=5.0V\pm10\%$, $V_{PP}=12.0V\pm5\%$)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t _{AS}	Address Setup time	0	-	-	
t _{AH}	Address Hold time	100	•	-	
t _{CES}	Chip Enable Setup time or Command Cycle	0	-	-	
t _{CEH}	Chip Enable Hold time or Command Cycle	10	-	-	
toes	Output Enable Setup time	0		-]
t _{OEH}	Output Enable Hold time	10	-	-	
t _{WES}	Write Enable Setup time on Command Cycle	0	_	-	
twen	Write Enable Hold time on Command Cycle	10	-	-	ns
t _{D\$}	Data Setup time	50	-	-	
t _{DH}	Data Hold time	0	_	_	
twelh	Write Enable Low Level Hold time	100	-	-]
₩ЕНН	Write Enable High Level Hold time	50	-	-	
t _{CELH}	Chip Enable Low Level Hold time	90	-	-	
t _{CEHH}	Chip Enable High Level Hold time	50	_	-	
t _{CMC}	Command Cycle time	150	-	-	
t _{PH}	Programming Hold time	90	-	150	
t _{PRV}	Program Recovery time before Program Verify	2	-	-	μs
t _{EH}	Erasing Hold time	0.9	-	1.5	8
terv	Erase Recovery time before Erase Verify	500	-	_	μs
t _{ACC}	Address Access time	_		150/200*	
t _{CE}	Chip Enable Access time	-	-	150/200*	
toE	Output Enable Access time	-	_	70	
t _{CEE}	Chip Enable to Output in Low - Z	0	_	-	
toee	Output Enable to Output in Low – Z	0	-		
t _{ОН}	Output Data Hold time	0	-	-	ns
t _{DF1}	Chip Enable to Output in High – Z	_	-	60	
t _{DF2}	Output Enable to Output in High - Z	-	-	60	
twesv	Write Enable Setup time on Verify Cycle	0	-	-	
twehv	Write Enable Hold time on Verify Cycle	0	-	-	
t _{RC}	Verify Cycle time	150/200*		-	

Note: * 150ns for TC58F1000P/F/J-15 200ns for TC58F1000P/F/J-20

A.C. TEST CONDITIONS

Output Load

: 1 TTL Gate and C_L (100pF)

• Input Pulse Rise and Fall Time (10%~90%)

: 5ns

Input Pulse LevelsTiming Measurement Reference Levels

: 0.45V to 2.40V : 0.80V/2.20V

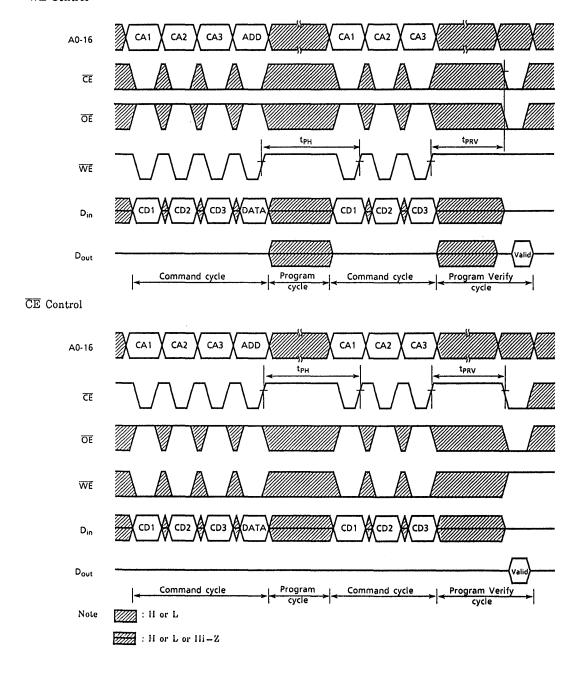
- 11111116 Mcasarement Reference Devels

Output : 0.80V/2.00V

Input

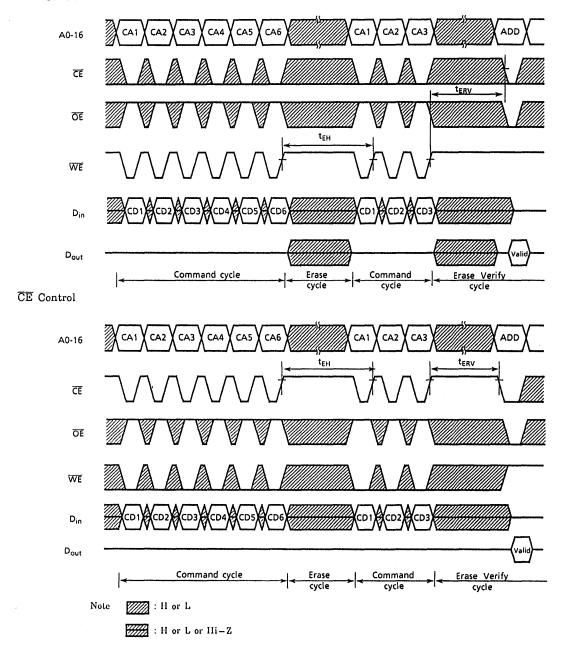
Program and Program Verify Operation

WE Control



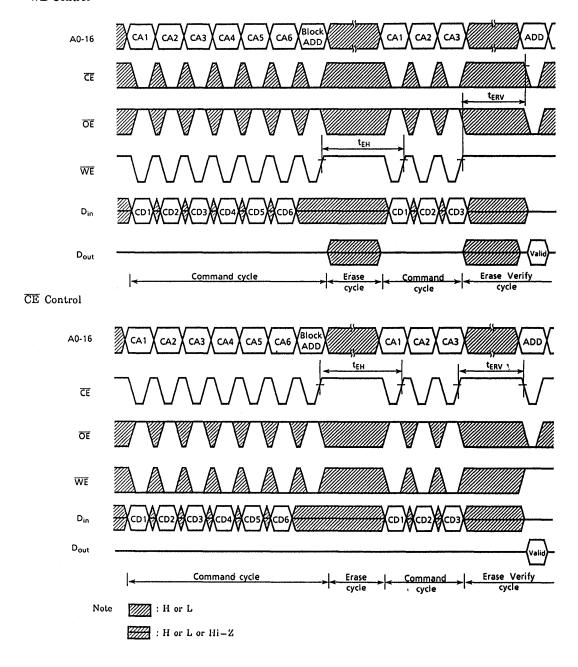
Chip Erase and Erase Verify Operation





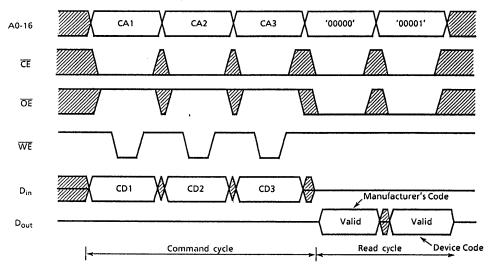
Block Erase and Erase Verify Operation

WE Control

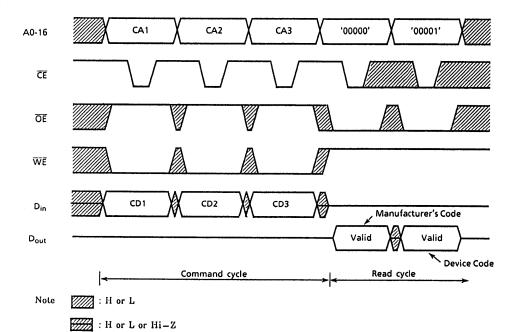


Signature Read Operation

WE Control

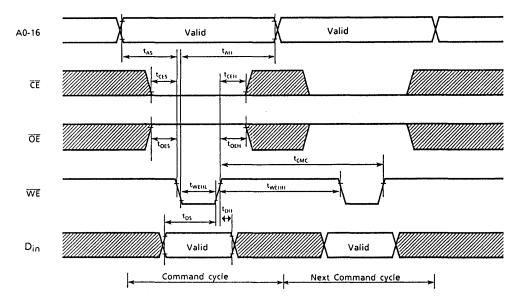


CE Control

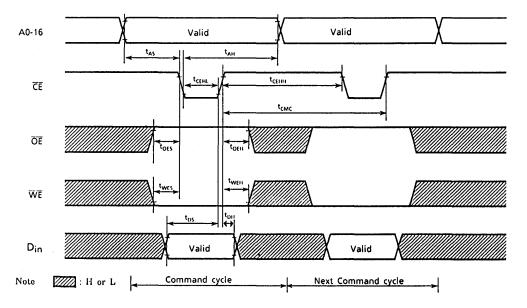


Timing Waveform of Command Cycle

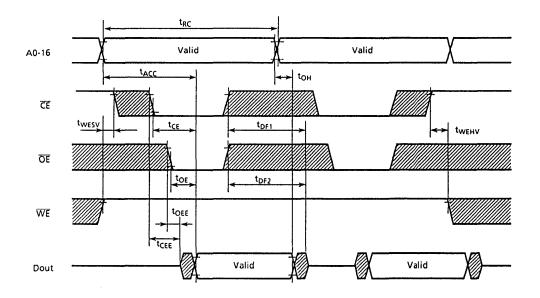
WE Control



CE Control



Timing Waveform of Verify Cycle



Note : II or L

TC58F1000P/F/J-15 TC58F1000P/F/J-20

3. EPROM COMPATIBLE OPERATION

 $(Ta=0\sim70^{\circ}C, V_{CC}=5V\pm10\%, V_{PP}=12.0V\pm5\%, V_{WE}=12.0V\pm5\%)$

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT
t _{A\$}	Address Setup time	0	-	-	ns
t _{AH}	Address Hold time	100	-	-	113
t _{WP}	Programming Pulse Width	90	120	150	μs
LOESP	Output Enable Setup time on Program Operation	2.0	-	-	
t _{D\$}	Data Setup time	50	-	_	ns
t _{DH}	Data Hold time	0	-	_	113
t _{EW}	Erasing Pulse Width	0.9	1.2	1.5	s
toese	Output Enable Setup time on Erase Operation	0	-	-	ns
toehe	Output Enable Hold time on Erase Operation	500	-	-	μs
t _{ACC}	Address Access time	_	-	150/200*	
t _{CE}	Chip Enable Access time	-	-	150 / 200*	
t _{OE}	Output Enable Access time	-	-	70	
t _{CEE}	Chip Enable to Output in Low - Z	0	-	-	
tole	Output Enable to Output in Low – Z	0	-	-	ns
t _{OH}	Output Data Hold time	0	_	-	
t _{DF1}	Chip Enable to Output in High – Z	_	-	60	
t _{DF2}	Output Enable to Output in High - Z	-	-	60	
t _{RC}	Read / Verify cycle time	150/200*	-	_	
t _{VS}	V _{PP} Setup time	2.0	-	_	μѕ
t _{A95}	V _{ID} Setup time	2.0	-	_	
twes	V _{WE} Setup time	2.0	-	_	

Note: * 150ns for TC58F1000P/F/J-15 200ns for TC58F1000P/F/J-20

A.C. TEST CONDITIONS

• Output Load : 1 TTL Gate and C_L (100pF)

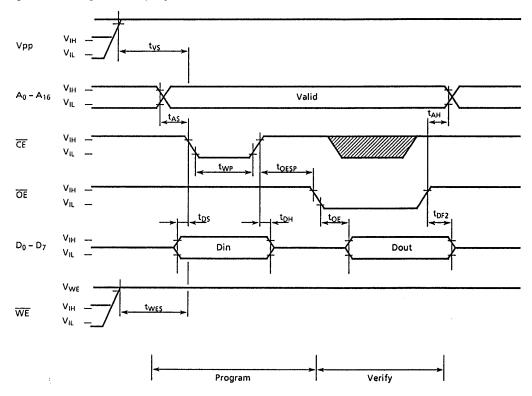
• Input Pulse Rise and Fall Time (10%~90%) : 5ns

• Input Pulse Levels : 0.45V to 2.40V • Timing Measurement Reference Levels Input : 0.80V/2.20V

Output: 0.80V/2.00V

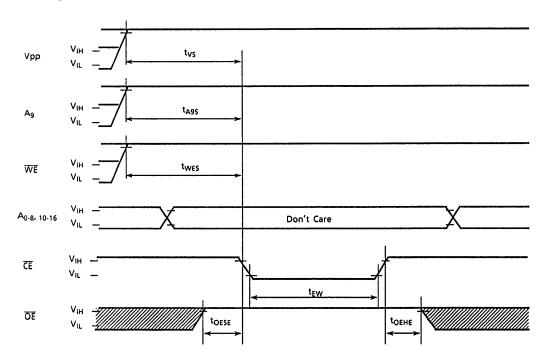
Timing Waveform of EPROM Compatible Operation

Program and Program Verify Operation



Timing Waveform of EPROM Compatible Operation

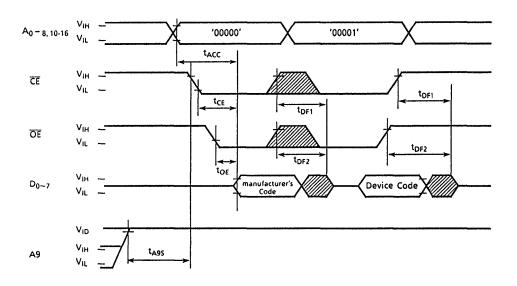
Erase Operation



Note: Din is don't care (II or L)

Timing Waveform of EPROM Compatible Operation

Signature Read Operation

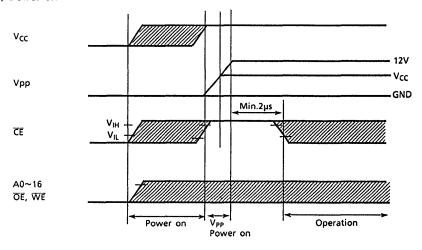


Note : $\overline{WE} = V_{IH}$, $V_{PP} = 0V \sim V_{CC}$ or 12V

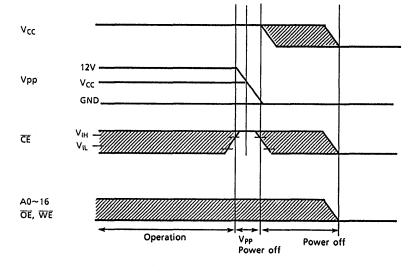
POWER ON/OFF SEQUENCE

This power on/off sequence protects against inadvertent programming or erasure. In case of power on, V_{CC} and \overline{CE} must be high level before V_{PP} becomes a high level. In case of power off, V_{CC} and \overline{CE} must remain high level until V_{PP} becomes a low level.

(1) Power on



(2) Power off



OPERATIONS

READ

The TC58F1000P/F/J has two control input pins. The chip enable (\overline{CE}) controls the operating power and should be used for device selection/deselection. The \overline{CE} access time (t_{CE}) is equal to the address access time (t_{ACC}) . The output enable (\overline{OE}) controls the output buffers. The output data is valid after a delay of t_{OE} from the falling edge of \overline{OE} .

OUTPUT DISABLE

When the OE input control is high, the outputs are placed in the high-impedance state.

STANDBY

The TC58F1000P/F/J has a low power standby mode controlled by the $\overline{\text{CE}}$ signal. By applying a high level to the $\overline{\text{CE}}$ input, the TC58F1000P/F/J is placed in the standby mode and the outputs are in the high impedance state, independent of the $\overline{\text{OE}}$ and $\overline{\text{WE}}$ inputs.

PROGRAM/PROGRAM-VERIFY/ERASE/ERASE-VERIFY/SIGNATURE READ

The TC58F1000P/F/J features a command control mode and an EPROM compatible mode. The command control mode is used to enable the program, program-verify, chip-erase, block erase, erase-verify, signature read and reset operations and the EPROM compatible mode controls the program, program-verify, chip erase and signature read operations.

1. COMMAND CONTROL MODE

The command code must be entered into the TC58F1000P/F/J before performing program, program-verify, erase (chip-erase and block-erase operations), erase-verify, signature read, reset operations.

The command control is a useful software protection method to protect from inadvertent operation. The command control mode is enabled when a high voltage (12V) is applied Vpp.

TC58F1000P/F/J has an internal command register circuit and the operation mode is defined by the command codes. The specific addresses and data presented to the TC58F1000P/F/J are latched in the command registers and the operation mode is defined. Address and data code are latched by the $\overline{\rm WE}$ signal. The address is latched at the falling edge of $\overline{\rm WE}$, and the data is latched at the rising edge of $\overline{\rm WE}$.

1) PROGRAM OPERATION

The program operation is setup by the first 3 steps of command codes and performed during the 4th step by providing the address and data to be programmed.

The command codes are as follows.

STEP (Bus Cycle) Mode		Address*	D0~7	
1	Write	5555(H) : A0~14	AA(H)	
2	Write	2AAA(H): A0~14	55(H)	
3	Write	5555(H) : A0~14	A0(H)	
4	Write	Address : A0~16	Data-in	

2) PROGRAM-VERIFY OPERATION

The program-verify operation is setup by the first 3 steps of command codes and performed during the 4th step. The program-verify address is a don't care because the address is latched during the program operation. Between the 3rd and 4th bus cycles a 2µs (minimum) program recovery delay is required.

The command codes are as follows.

STEP (Bus Cycle)	Mode	Address*	D0~7
1	Write	5555(H) : A0~14	AA(H)
2	Write	2AAA(H): A0~14	55(H)
3	Write	5555(H): A0~14	B0(H)
4	Read	Don't Care	Data-out

Note: *The addresses which are not defined in the table are "don't care."

3) ERASE OPERATION

The chip erase operation is setup and performed after 6 steps of command codes. The block erase operation is setup by 6 steps of command codes and performed after the 7th step by giving the first address of each block.

The command codes are as follows.

a) Chip erase operation

STEP (Bus Cycle)	Mode	Address*	D0~7
1	Write	5555(H): A0~14	AA(H)
2	Write	2AAA(H): A0~14	55(H)
3	Write	5555(H): A0~14	80(H)
4	Write	5555(H): A0~14	AA(H)
5	Write	2AAA(H): A0~14	55(H)
6	Write	5555(H): A0~14	10(H)

b) Block erase operation

STEP (Bus Cycle)	Mode	Address*	D0~7
1	Write	5555(H) : A0~14	AA(H)
2	Write	2AAA(H): A0~14	55(H)
3	Write	5555(H): A0~14	60(H)
4	Write	5555(H): A0~14	AA(H)
5	Write	2AAA(H): A0~14	55(H)
6	Write	5555(H) : A0~14	20(H)
7	Write	Block Add.: A12~16	Don't Care

Note: * The addresses which are not defined in the table are "don't care".

4) ERASE-VERIFY OPERATION

The erase-verify operation is setup by 3 steps of command codes and performed by presenting the erase-verify address during the 4th step. By providing the next erase-verify address during subsequent steps, additional erase verify operations can be performed. Between the 3rd and 4th steps a 500µs (minimum) erase recovery time required.

The command codes are as follows.

STEP (Bus Cycle)	Mode	Address*	D0~7
1	Write	5555(H) : A0~14	AA(H)
2	Write	2AAA(H): A0~14	55(H)
3	Write	5555(H): A0~14	D0(H)
4	Read	Address : A0~16	Data-out

5) SIGNATURE READ OPERATION

The signature-read operation is setup by 3 steps of command codes and by providing address 00000(H) to read the manufacturers code and address 00001(H) to read the device code during the 4th or 5th steps.

The command codes are as follows.

STEP (Bus Cycle)	<u>Mode</u>	Address*	<u>D0~7</u>
1	Write	5555(H): A0~14	AA(H)
2	Write	2AAA(H): A0~14	55(H)
3	Write	5555(H) : A0~14	90(H)
4	Read	0 : A0~16	Manufacturer's Code
5	Read	1 : A0~16	Device Code

Note: * The addresses which are not defined in the table are "don't care".

6) RESET

Each operation mode is cleared by the reset command and the operation mode returns to the initial state which is the read mode. The reset operation is performed by 3 steps of command codes.

The command codes are as follows.

STEP (Bus Cycle)	Mode	Address*	D0~7
1	Write	5555(H) : A0~14	AA(H)
2	Write	2AAA(H): A0~14	55(H)
-3	Write	5555(H): A0~14	F0(H)

Note: * The addresses which are not defined in the table are "don't care".

TC58F1000P/F/J-15 TC58F1000P/F/J-20

<Command Control Code Table>

				C	ommand Ste	р		
		1	2	3	4	5	6	7
	Mode	Write	Write	Write	Write			
Program	Address	5555 (A0 – 14)	2AAA (A0 – 14)	5555 (A0 – 14)	Program Add. (A0 – 16)		X	
	D0~7	AA	55	Α0	Data in			
	Mode	Write	Write	Write	Read			
Program – Verify	Address	5555 (A0 – 14)	2AAA (A0 – 14)	5555 (A0 – 14)	Don't care		X	
	D0~7	AA	55	80	Data out			
	Mode	Write	Write	Write	Read	Read		
Signature Read	Address	5555 (A0 – 14)	2AAA (A0 – 14)	5555 (A0 – 14)	00000 (A0 – 16)	00001 (A0 - 16)		
	D0~7	АА	55	90	Manu – facturer's code	Device code		

	***************************************		Command Step							
		1	2	3	4	5	6	7		
	Mode	Write	Write	Write	Write	Write	Write			
Chip Erase	Address	5555 (A0 – 14)	2AAA (A0 – 14)	5555 (A0 – 14)	5555 (A0.– 14)	2AAA (A0 – 14)	5555 (A0 – 14)	X		
	D0~7	AA	55	80	AA	55	10			
	Mode	Write	Write	Write	Write	Write	Write	Write		
Block Erase	Address	5555 (A0 – 14)	2AAA (A0 – 14)	5555 (A0 – 14)	5555 (A0 – 14)	2AAA (A0 – 14)	5555 (A0 – 14)	Block Add. (A12 – 16)		
	D0~7	AA	55	60	AA	55	20	Don't care		
	Mode	Write	Write	Write	Read					
Erase – Verify	Address	5555 (A0 – 14)	2AAA (A0 – 14)	5555 (A0 – 14)	Verify Add. (A0 – 16)		X			
	D0~7	АА	55	D0	Data out					
	Mode	Write	Write	Write						
Reset	Address	5555 (A0 – 14)	2AAA (A0 ~ 14)	5555 (A0 – 14)						
	D0~7	АА	55	FO						

Note: *The addresses which are not defined in the table are "don't care."

TC58F1000P/F/J-15 TC58F1000P/F/J-20

BLOCK ERASE MODE <Block Address Table>

Block No.	Addresss Area	Hex Adresss	A16	A15	A14	A13	A12	A11~A0
1	00000~00FFF	00XXX	0	0	0	0	0	Don't Care
2	01000~01FFF	01XXX	0	0	0	0	1	Don't Care
3	02000~02FFF	02XXX	0	0	0	1	0	Don't Care
4	03000~03FFF	03XXX	0	0	0	1	1	Don't Care
5	04000~04FFF	04XXX	0	0	1	0	0	Don't Care
6	05000~05FFF	05XXX	0	0	1	0	1	Don't Care
7	06000~06FFF	06XXX	0	0	1	1	0	Don't Care
8	07000~07FFF	07XXX	0	0	1	1	1	Don't Care
9	08000~08FFF	08XXX	0	1	0	0	0	Don't Care
10	09000~09FFF	09XXX	0	1	0	0	1	Don't Care
11	0A000~0AFFF	0AXXX	0	1	0	1	0	Don't Care
12	0B000~0BFFF	0BXXX	0	1	0	1	1	Don't Care
13	0C000~0CFFF	0CXXX	0	1	1	0	0	Don't Care
14	0D000~0DFFF	0DXXX	0	1	1	0	1	Don't Care
15	0E000~0EFFF	0EXXX	0	1	1	1	0	Don't Care
16	0F000~0FFFF	0FXXX	0	1	1	1	1	Don't Care
17	10000~10FFF	10XXX	1	0	0	0	0	Don't Care
18	11000~11FFF	11XXX	1	0	0	0	1	Don't Care
19	12000~12FFF	12XXX	1	0	0	1	0	Don't Care
20	13000~13FFF	13XXX	1	0	0	1	1	Don't Care
21	14000~14FFF	14XXX	1	0	1	0	0	Don't Care
22	15000~15FFF	15XXX	1	0	1	0	1	Don't Care
23	16000~16FFF	16XXX	1	0	1	1	0	Don't Care
24	17000~17FFF	17XXX	1	0	1	1	1	Don't Care
25	18000~18FFF	18XXX	1	1	0	0	0	Don't Care
26	19000~19FFF	19XXX	1	1	0	0	1	Don't Care
27	1A000~1AFFF	1AXXX	1	1	0	1	0	Don't Care
28	18000~1BFFF	1BXXX	1	1	0	1	1	Don't Care
29	1C000~1CFFF	1CXXX	1	1	1	0	0	Don't Care
30	1D000~1DFFF	1DXXX	1	1	1	0	1	Don't Care
31	1E000~1EFFF	1EXXX	1	1	1	1	0	Don't Care
32	1F000~1FFFF	1FXXX	1	1	1	1	1	Don't Care

2. EPROM COMPATIBLE MODE

This mode is the same as used for Toshiba's 256K FE²PROM, the TC58257A. When a high-voltage (12V) is applied to the WE pin of the TC58F1000P/F/J, the program and erase operations are enabled and can be performed by any conventional EPROM programmer.

(1) PROGRAM OPERATION

TC58F1000P/F/J is placed in the programming mode by applying a high voltage (12V) to the V_{PP} and \overline{WE} pins. During the programming cycle the addresses and input data must be held valid, the \overline{OE} signal must be held high and the \overline{CE} input must be clocked. The programming is controlled by the \overline{CE} input timing.

(2) PROGRAM-VERIFY OPERATION

The programmed data is verified with the V_{PP} and \overline{WE} pins held at high voltage (12V) level and with \overline{OE} held at V_{IL} .

(3) CHIP ERASE OPERATION

TC58F1000P/F/J is placed in the chip erase mode by applying a high voltage (12V) to the V_{PP} , \overline{WE} and A9 pins. During the chip erase cycle, addresses A0~A8 and A10~A16 are "don't care", \overline{OE} must be held high and \overline{CE} must be clocked.

(4) ELECTRIC SIGNATURE READ

With VPP held at a voltage between 0 and V_{CC}, WE held at VIH and by applying a high voltage (12V) to the A9 address input, the manufacturer's code can be read by specifying address 00000(H) and the device code can be read by specifying address 00001(H). Toshiba's manufacturer code and the TC58F1000P/F/J device code are shown in the table below.

TC58F1000P/F/J

Signature	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Manufacturer's Code	0	1	0	0	1	1	0	0	0	98
Device Code	1	0	0	1	0	0	1	1	0	26



APPLICATIONS

Toshiba's TC58F1000P/F/J Flash-EEPROM offers a cost-competitive and reliable alternative for applications which have traditionally employed the U.V. EPROM or O.T. PROM.

The Flash-EEPROM adds electrical erasure capability and eliminates the time consuming and labor intensive process of U.V. light exposure for erasing EPROMS. Furthermore, the Flash-EEPROM is electrically reprogrammable and thus eliminates the one-time programmable limitation of the O.T. PROM.

The TC58F1000P/F/J is offered in plastic DIP and surface mount packages (SOP and SOJ) which can be processed through the automated assembly line process. The electrically programmable and erasable features of the Flash-EEPROM eliminate the need for sockets both at the prototype stage and at the production stage. The major application advantages offered by the Flash-EEPROM in system design are listed below.

In-System Programming

The TC58F1000P/F/J is provided with a command control mode which makes it possible to program and erase data by using the system MPU timing. The TC58F1000P/F/J can be used for updating the system operating code or data in the system through a telecommunication line or a floppy disk interface. In this case, a 12V power supply must be available in the system.

On-Board Programming with an External Programmer

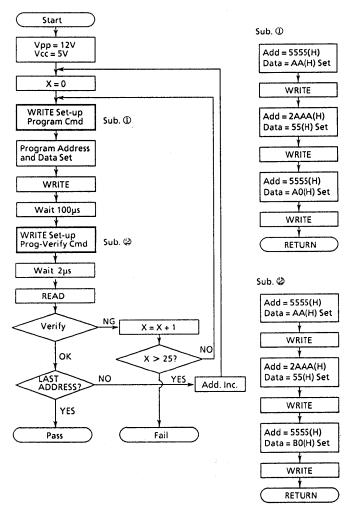
The TC58F1000P/F/J can be mounted directly onto the system board and all subsequent program and erase operations can be handled by an external PROM programmer through a connector. Since the TC58F1000P/F/J supports an EPROM compatible programming mode, a conventional PROM programmer can be used for this operation.

Card and Cartridge Applications

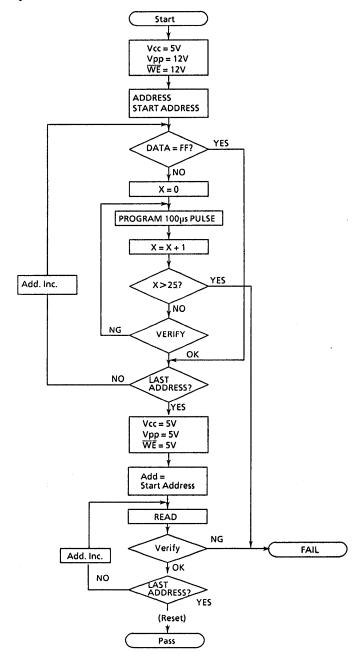
High density non-volatile memory cards and cartridges can be assembled using the SOP or SOJ surface mount version of Toshiba's TC58F1000. These cards and cartridges can be erased and reprogrammed using either the in-system programming method or an external programmer.

Program Flow Chart

① Command Control mode

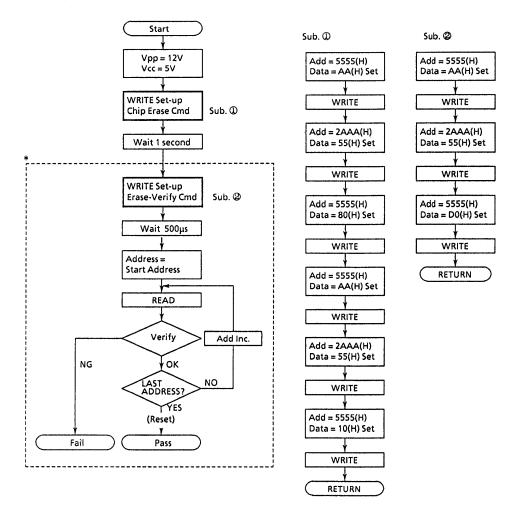


2 EPROM Compatible mode



Electrical Erase Flow Chart

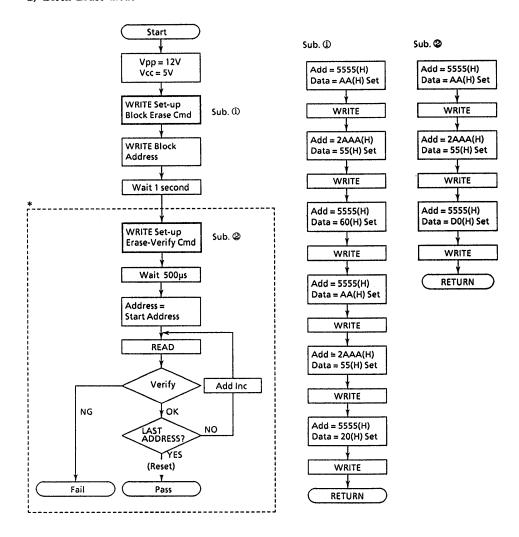
- ① Command Control mode
 - 1) Chip Erase mode



Note: *: This part is an erase verify sequence part.

It is helpful to verify the amount of erasing.

2) Block Erase mode



Note: *: This part is an erase verify sequence part.

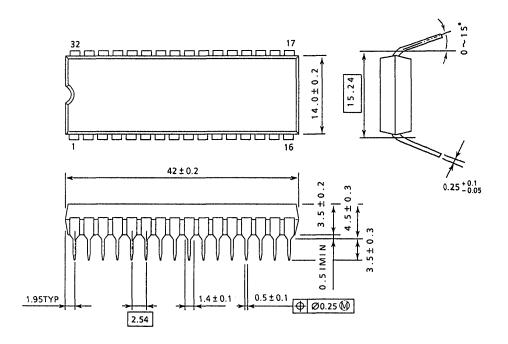
It is helpful to verify the amount of erasing.

OUTLINE DRAWINGS

• Plastic DIP

DIP32-P-600

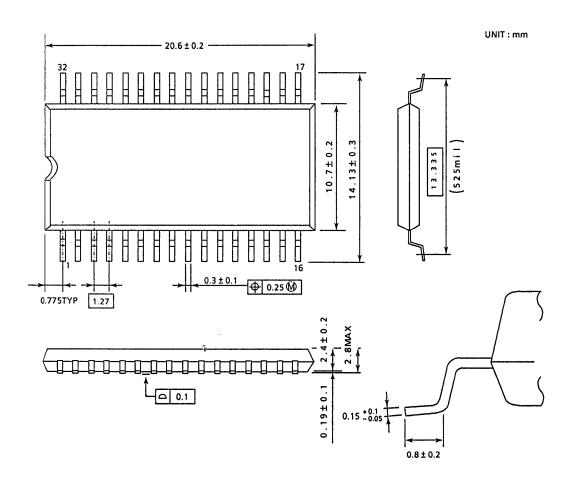
UNIT: mm



OUTLINE DRAWINGS

• Plastic SOP

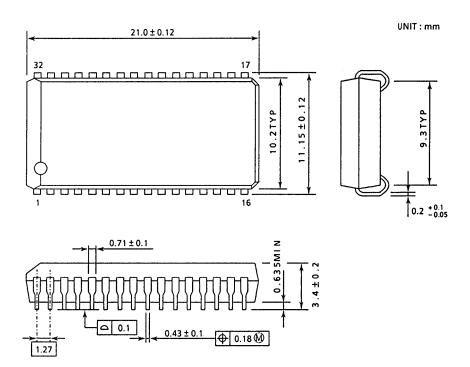
SOP32-P-525



OUTLINE DRAWINGS

• Plastic SOJ

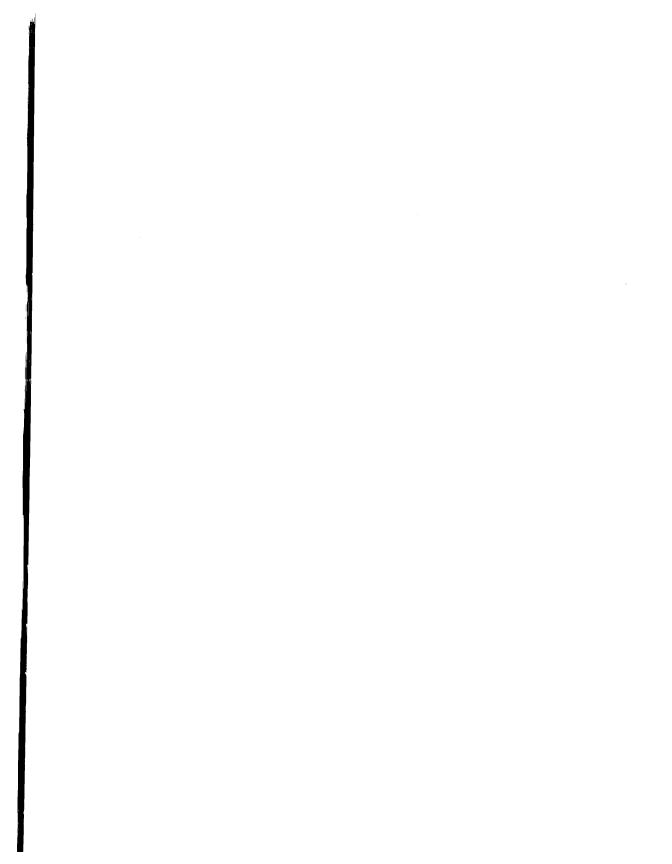
SOJ32-P-400



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