TOSHIBA

Application Specific DRAM

DATA BOOK

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Video RAM
Synchronous DRAM
Rambus™ DRAM

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TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

TOSHIBA

Application Specific DRAM
1994

Video RAM
Synchronous DRAM
Rambus™ DRAM

CONTENTS

2M VRAM CROSS REFERENCE

FUNCTION	BASIC & SPECIAL FEATURES	BASIC & SPECIAL FEATURES INCLUDING EXTENDED DATA OUT
Toshiba	TC528257	TC528267
Micron	MT42C8257	MT42C8256
NEC	μPD482234	μPD482235
Hitachi	HM538254	

Note: This cross reference has been developed based on compatibility of feature sets. We recommend system designers to check timing specifications in detail to ensure complete compatibility.

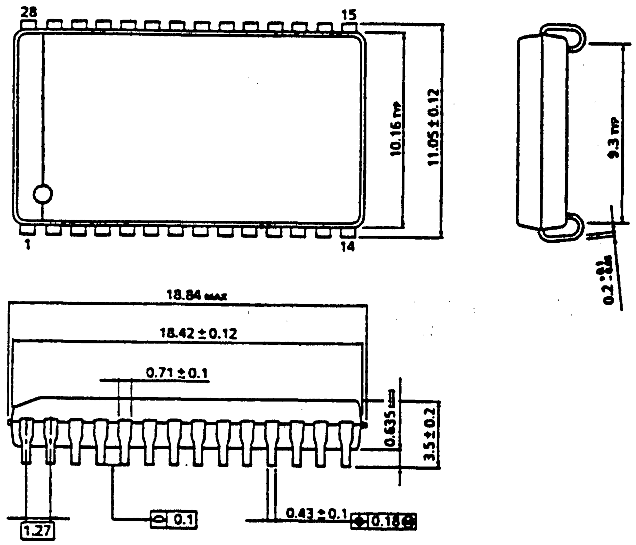
OUTLINE DRAWINGS

• Plastic SOJ

TC524258BJ

SOJ28 - P - 400

Unit in mm

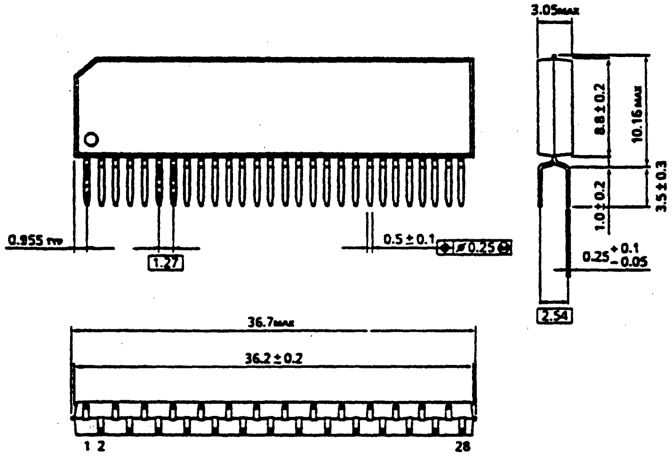


Weight : 1.13g (TYP.)

• **Plastic ZIP**

ZIP28 - P - 400

Unit in mm

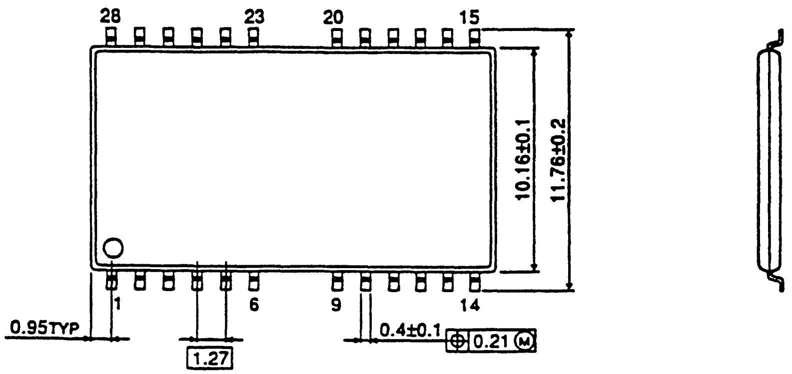


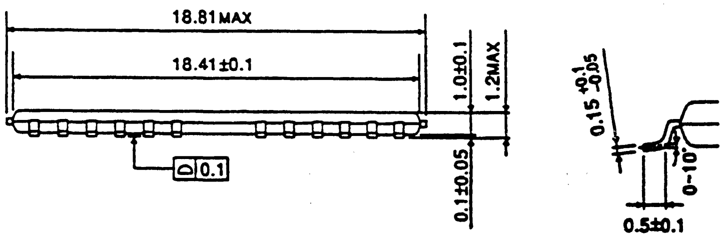
Weight : 2.01g (TYP.)

- **Plastic TSOP** **TC524258BFT**

TSOP28 - P - 400B

Unit in mm



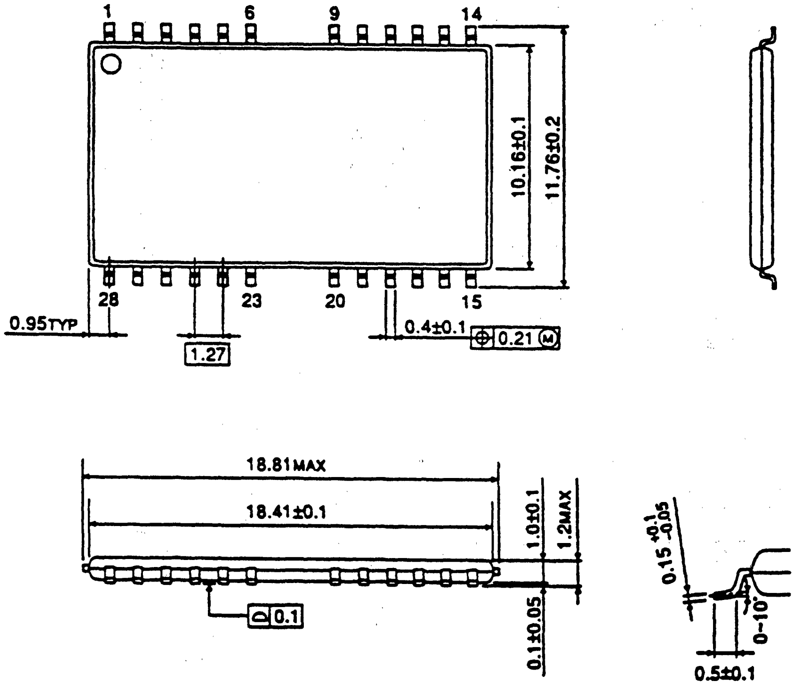


Weight : 0.53g (TYP.)

- **Plastic TSOP** **TC524258BTR**

TSOP28 - P - 400C

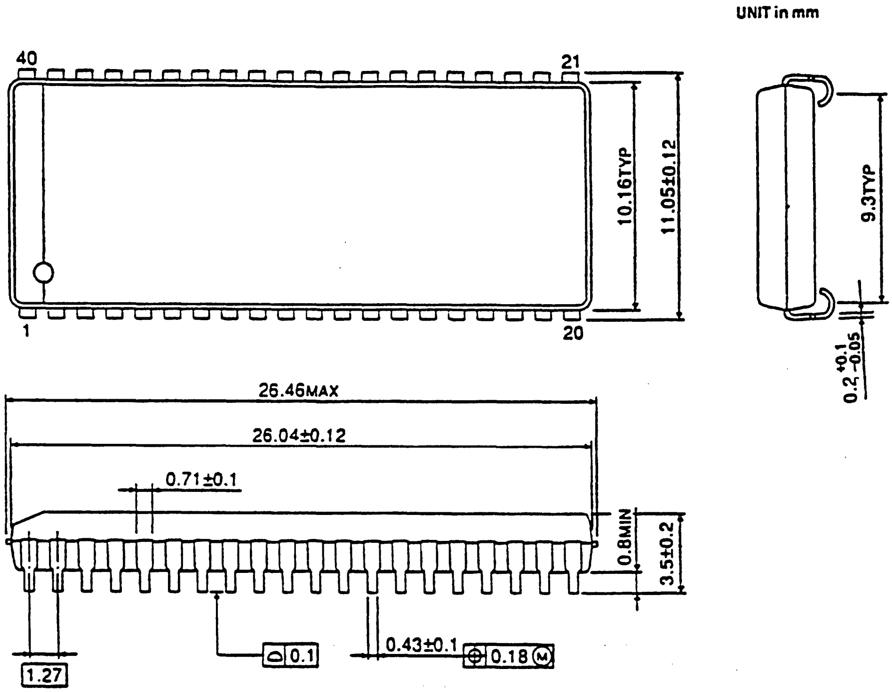
Unit in mm



Weight : 0.53g (TYP.)

- **Plastic SOJ** **TC528128BJ, TC528257J, TC528267J**

SOJ40 - P - 400

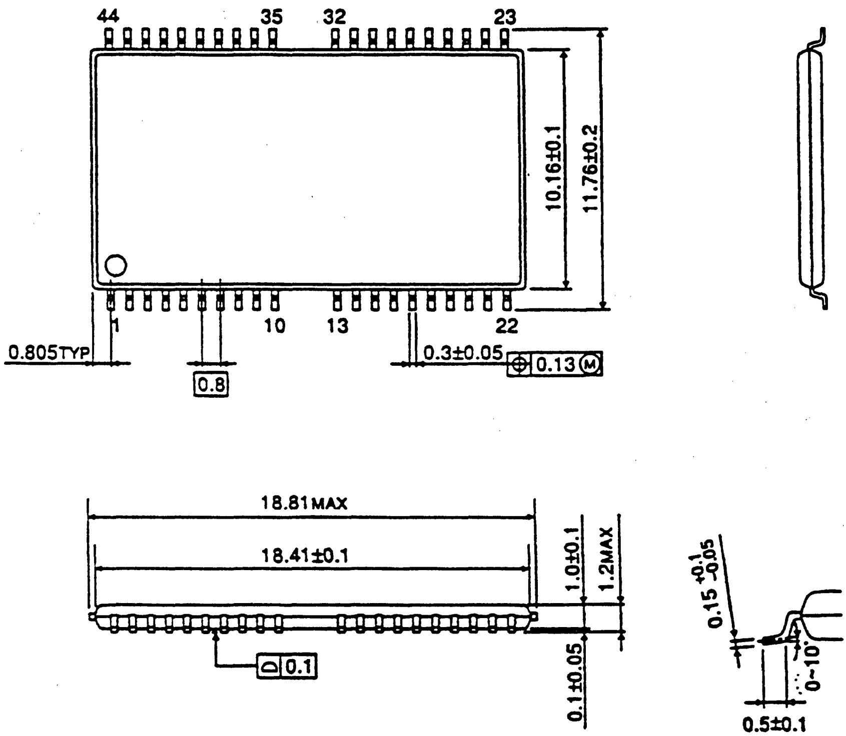


Weight : 1.55g (TYP.)

• **Plastic TSOP** **TC528128BFT, TC528257FT, TC528267FT**

TSOP44 - P - 400B

UNIT in mm

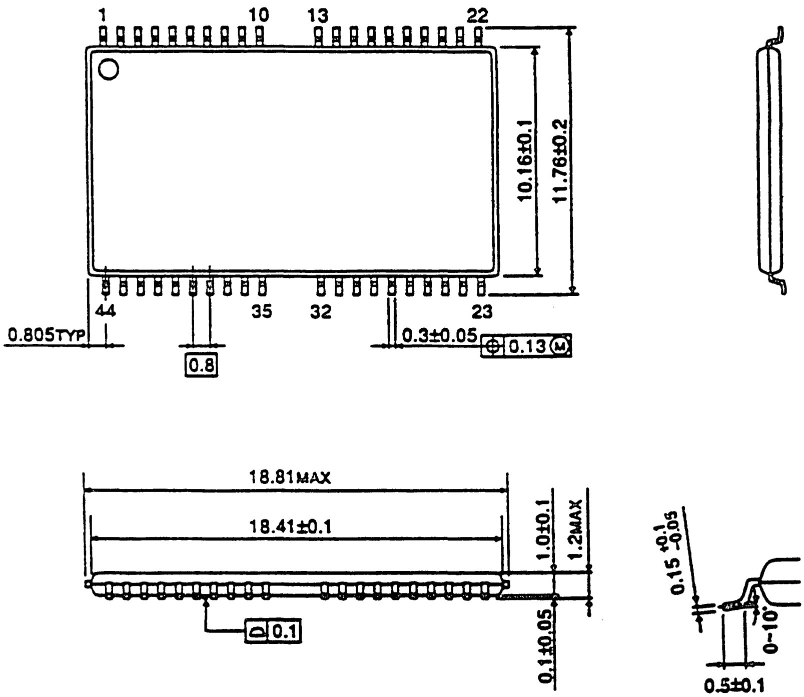


ıt : 0.48g (TYP.)

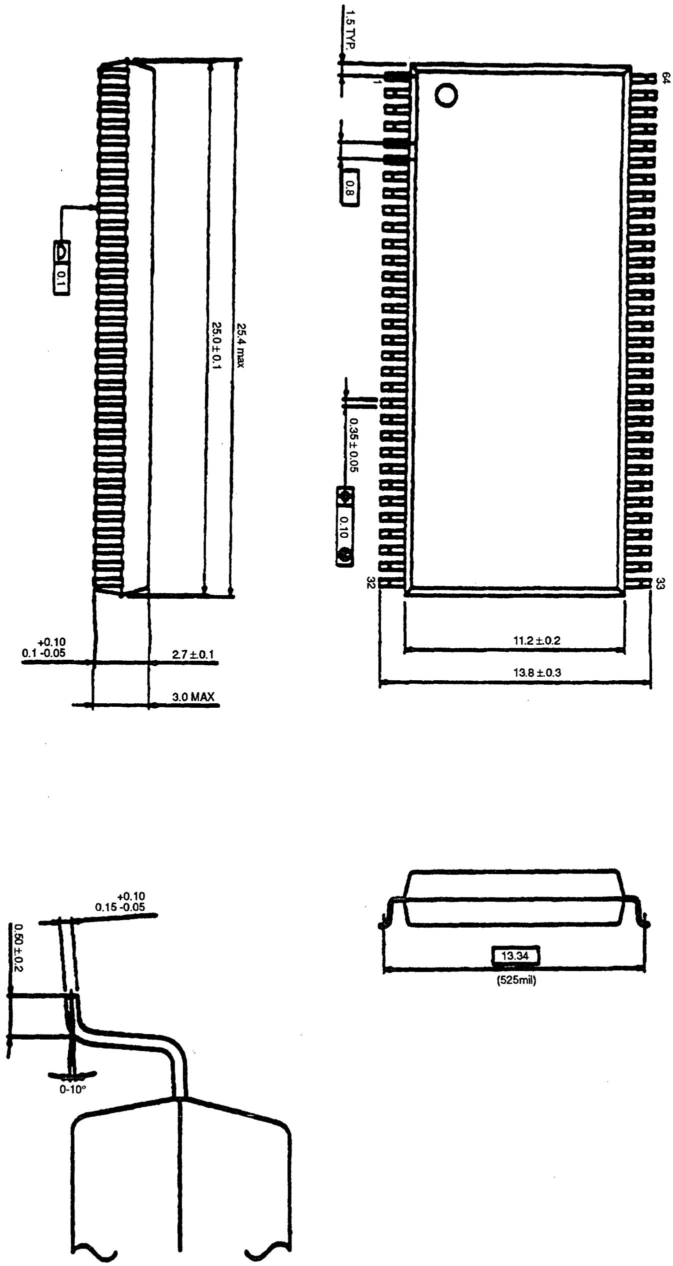
- **Plastic TSOP**

TSOP44 - P - 400C

UNIT in mm

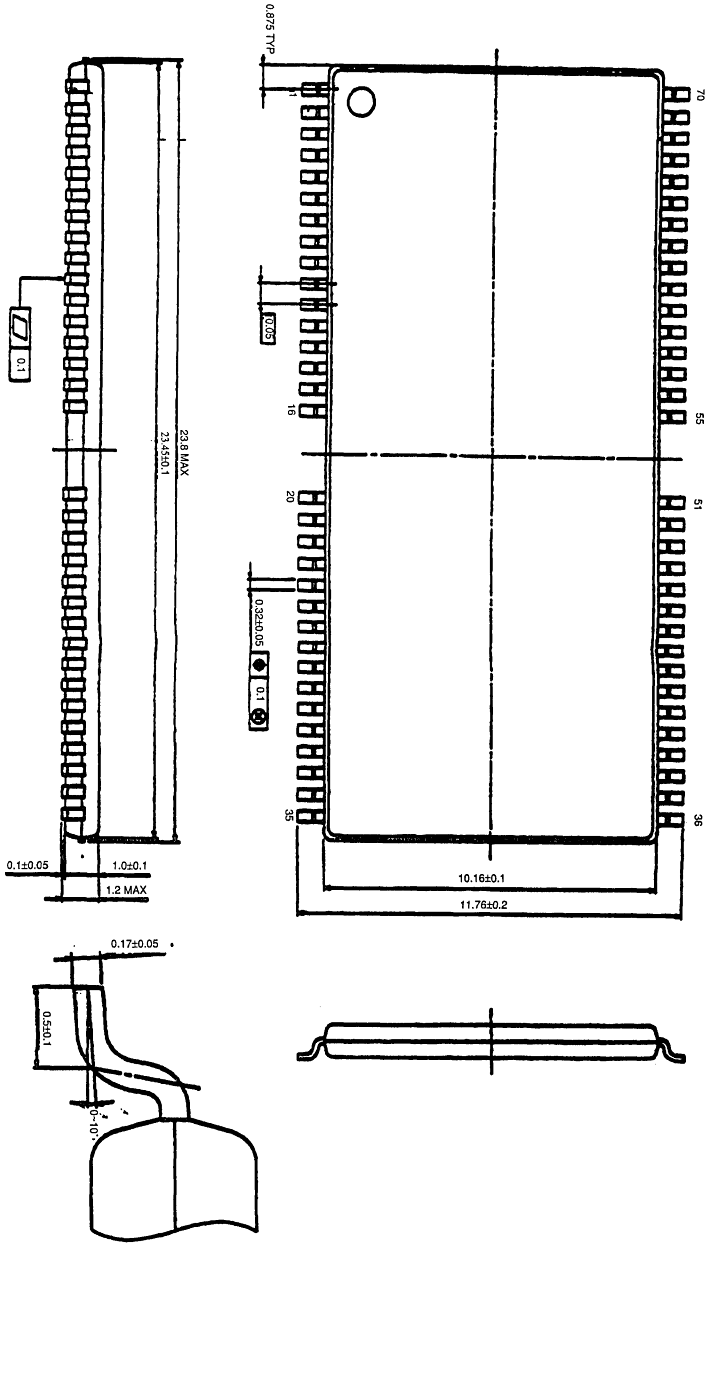


Weight : 0.48g (TYP.)


1.5 TYP.
1
64
0.8
0.1
25.0 ± 0.1
25.4 max
0.35 ± 0.05
0.10
32
33
+0.10
0.1 -0.05
2.7 ± 0.1
3.0 MAX
11.2 ± 0.2
13.8 ± 0.3
+0.10
0.15 -0.05
0.50 ± 0.2
0-10°
13.34
(525mil)

- **TSOP70-P-400**

TC524162/165FT, TC524162/165TR, TC524262/265FT, TC524262/265TR



SILICON GATE CMOS
262,144WORDS X 4BITS MULTIPORT DRAM

target spec

DESCRIPTION

The TC524258B is a CMOS multiport memory equipped with a 262,144-words by 4-bits dynamic random access memory (RAM) port and a 512-words by 4-bits static serial access memory (SAM) port. The TC524258B supports three types of operations; Random access to and from the RAM port, high speed serial access to and from the SAM port and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally. In addition to the conventional multiport video RAM operating modes, the TC524258B features the block write and flash write functions on the RAM port and a split register data transfer capability on the SAM port. The TC524258B is fabricated using Toshiba's CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

FEATURES

- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- All inputs and outputs : TTL Compatible
- Organization
  - RAM Port : 262,144words X 4bits
  - SAM Port : 512words X 4bits
- RAM Port
  - Fast Page Mode, Read - Modify - Write
  - $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh
  - $\overline{RAS}$ only Refresh, Write per Bit
  - Flash Write, Block Write
  - 512 refresh cycles / 8ms
- SAM Port
  - High Speed Serial Read / Write Capability
  - 512 Tap Locations
  - Fully Static Register
- RAM - SAM Bidirectional Transfer
  - Read / Write / Pseudo Write Transfer
  - Real Time Read Transfer
  - Split Read / Write Transfer
- Package
  - TC524258BJ : SOJ28-P-400
  - TC524258BZ : ZIP28-P-400

KEY PARAMETERS

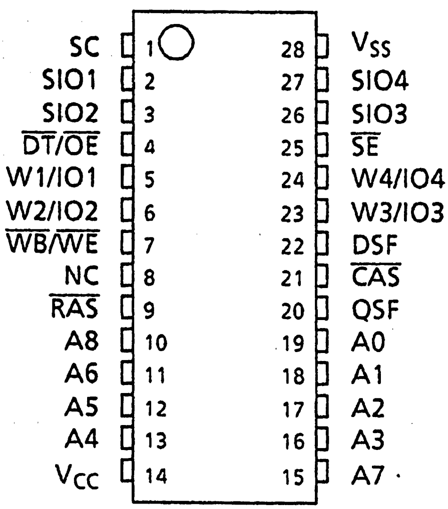
ITEM		—80	—10
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	80ns	100ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	25ns	25ns
t_{AA}	Column Address Access Time (Max.)	45ns	50ns
t_{RC}	Cycle Time (Min.)	150ns	180ns
t_{PC}	Page Mode Cycle Time (Min.)	50ns	55ns
t_{SCA}	Serial Access Time (Max.)	25ns	25ns
t_{SCC}	Serial Cycle Time (Min.)	30ns	30ns
I_{CC1}	RAM Operating Current (SAM : Standby)	85mA	70mA
I_{CC2A}	SAM Operating Current (RAM : Standby)	50mA	50mA
I_{CC2}	Standby Current	10mA	10mA

PIN NAME

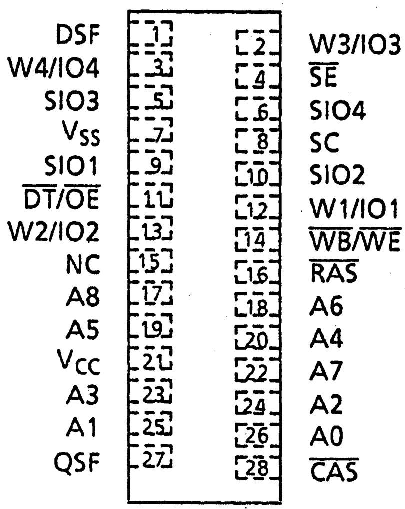
A0~A8	Address inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}/\overline{WE}$	Write per Bit/Write Enable
DSF	Special Function Control
Wl/IOl ~W4/IO4	Write Mask/Data IN, OUT
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIOl~SIO4	Serial Input/Output
QSF	Special Flag Output
V_{CC}/V_{SS}	Power (5V)/Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

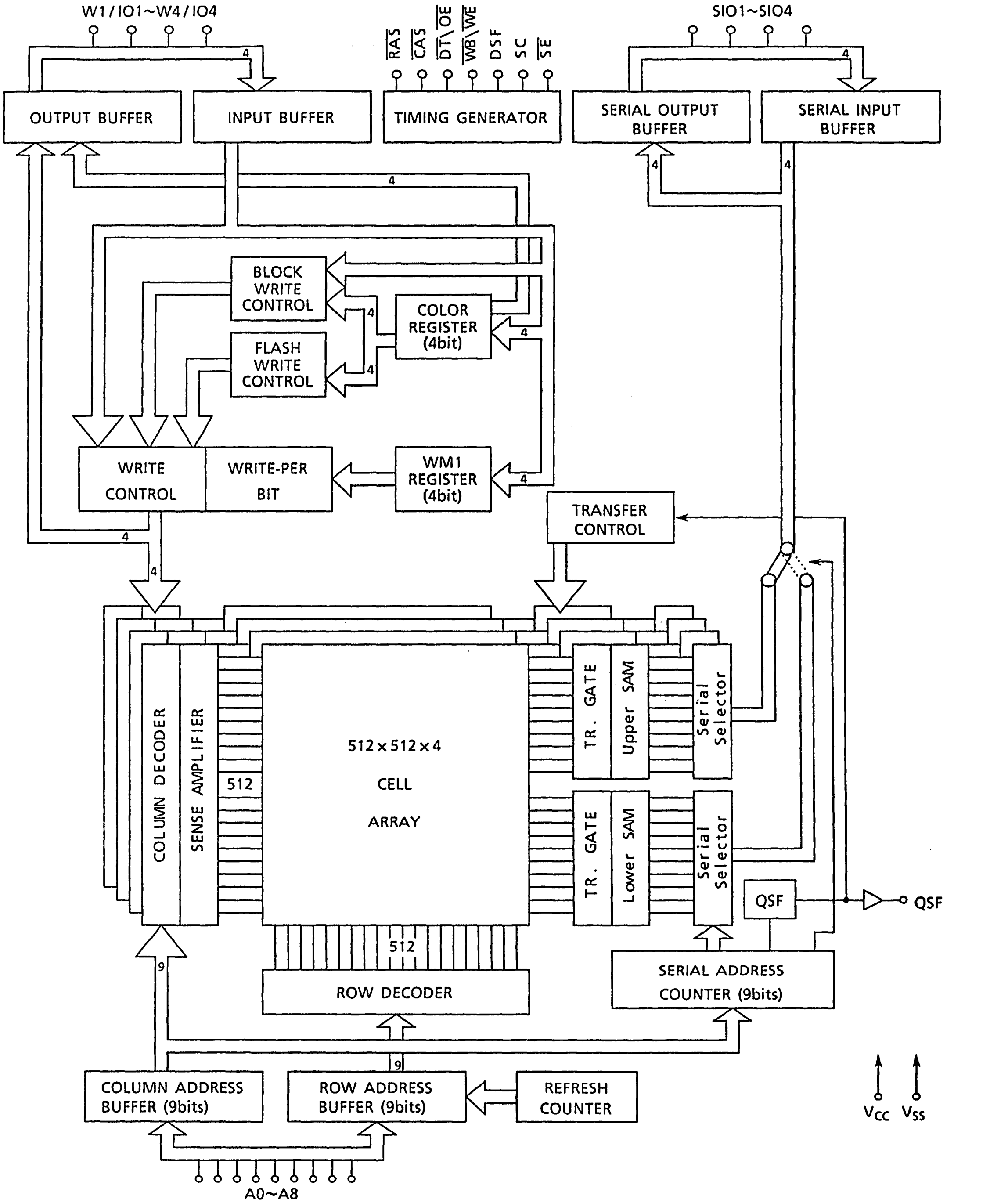
TC524258BJ



TC524258BZ



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}, V_{OUT}	Input Output Voltage	— 1.0~7.0	V	1
V_{CC}	Power Supply Voltage	— 1.0~7.0	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	— 55~150	°C	1
T_{SOLDER}	Soldering Temperature • Time	260•10	°C•sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	6.5	V	2
V_{IL}	Input Low Voltage	—1.0	—	0.8	V	2

CAPACITANCE (V_{CC} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance	—	7	pF
C_{IO}	Input/Output Capacitance	—	9	
C_O	Output Capacitance (QSF)	—	9	

Note: This parameter is periodically sampled and is not 100% tested.

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

ITEM (RAM PORT)	SAM PORT	SYMBOL	-80		-10		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
OPERATING CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC1}	—	85	—	70	mA	3, 4
	Active	I_{CC1A}	—	125	—	110	mA	3, 4
STANDBY CURRENT ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	Standby	I_{CC2}	—	10	—	10	mA	
	Active	I_{CC2A}	—	50	—	50	mA	3, 4
RAS ONLY REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	Standby	I_{CC3}	—	85	—	70	mA	3, 4
	Active	I_{CC3A}	—	125	—	110	mA	3, 4
PAGE MODE CURRENT ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{PC} = t_{RC} min.)	Standby	I_{CC4}	—	75	—	60	mA	3, 4
	Active	I_{CC4A}	—	115	—	100	mA	3, 4
CAS BEFORE RAS REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$, t_{RC} = t_{RC} min.)	Standby	I_{CC5}	—	85	—	70	mA	3, 4
	Active	I_{CC5A}	—	125	—	110	mA	3, 4
DATA TRANSFER CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC6}	—	105	—	90	mA	3, 4
	Active	I_{CC6A}	—	145	—	130	mA	3, 4
FLASH WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC7}	—	85	—	70	mA	3, 4
	Active	I_{CC7A}	—	125	—	110	mA	3, 4
BLOCK WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC8}	—	95	—	80	mA	3, 4
	Active	I_{CC8A}	—	135	—	120	mA	3, 4

ITEM	SYMBOL	MIN.	MAX	UNIT	NOTE
INPUT LEAKAGE CURRENT 0V≤V_{IN}≤6.5V, All other pins not under test=0V	$I_{I(L)}$	—10	10	μA	
OUTPUT LEAKAGE CURRENT 0V≤V_{OUT} ≤5.5V, OutputDisable	$I_{O(L)}$	—10	10	μA	
OUTPUT "H" LEVEL VOLTAGE I_{OUT} = - 2mA	V_{OH}	2.4	—	V	
OUTPUT "L" LEVEL VOLTAGE I_{OUT} = 2mA	V_{OL}	—	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes: 5, 6, 7)

SYMBOL	PARAMETER	-80		-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150		180		ns	
t_{RMW}	Read-Modify-Write Cycle Time	195		235			
t_{PC}	Fast Page Mode Cycle Time	50		55			
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	90		100			
t_{RAC}	Access Time from $\overline{RAS}$		80		100		8,14
t_{AA}	Access Time from Column Address		45		50		8,14
t_{CAC}	Access Time from $\overline{CAS}$		25		25		8,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		45		50		8,15
t_{OFF}	Output Buffer Turn-Off Delay	0	20	0	20		10
t_T	Transition Time (Rise and Fall)	3	35	3	35		7
t_{RP}	$\overline{RAS}$ Precharge Time	60		70			
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10000	100	10000		
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode Only)	80	100000	100	100000		
t_{RSH}	$\overline{RAS}$ Hold Time	25		25			
t_{CSH}	$\overline{CAS}$ Hold Time	80		100			
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10000	25	10000		
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	55	20	75		14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	50		14
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45		50			
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10			
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10			
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10			
t_{ASR}	Row Address Set-Up Time	0		0			
t_{RAH}	Row Address Hold Time	10		10			
t_{ASC}	Column Address Set-Up Time	0		0			
t_{CAH}	Column Address Hold Time	15		15			
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55		70			
t_{RCS}	Read Command Set-Up Time	0		0			
t_{RCH}	Read Command Hold Time	0		0			11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0			11
t_{WCH}	Write Command Hold Time	15		15			
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55		70			
t_{WP}	Write Command Pulse Width	15		15			
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25			
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25			

SYMBOL	PARAMETER	-80		-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{DS}	Data Set-Up Time	0		0		ns	12
t_{DH}	Data Hold Time	15		15			12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55		70			
t_{WCS}	Write Command Set-Up Time	0		0			13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100		130			13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65		80			13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45		55			13
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0			
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0			
t_{OEA}	Access Time from $\overline{OE}$		20		25		8
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	0	10	0	20		10
t_{OED}	$\overline{OE}$ to Data Delay Time	10		20			
t_{OEH}	$\overline{OE}$ Command Hold Time	10		20			
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15		15			
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0			
t_{REF}	Refresh Period		8		8	ms	
t_{WSR}	$\overline{WB}$ Set-Up Time	0		0		ns	
t_{RWH}	$\overline{WB}$ Hold Time	15		15			
t_{FSR}	DSF Set-Up Time referenced to $\overline{RAS}$	0		0			
t_{RFH}	DSF Hold Time referenced to $\overline{RAS}$ (1)	15		15			
t_{FHR}	DSF Hold Time referenced to $\overline{RAS}$ (2)	55		70			
t_{FSC}	DSF Set-Up Time referenced to $\overline{CAS}$	0		0			
t_{CFH}	DSF Hold Time referenced to $\overline{CAS}$	15		15			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0		0			
t_{MH}	Write-Per-Bit Mask Data Hold Time	15		15			
t_{THS}	$\overline{DT}$ High Set-Up Time	0		0			
t_{THH}	$\overline{DT}$ High Hold Time	15		15			
t_{TLS}	$\overline{DT}$ Low Set-Up Time	0		0			
t_{TLH}	$\overline{DT}$ Low Hold Time	15	10000	15	10000		
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	65	10000	80	10000		
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	30		30			
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	25		25			

SYMBOL	PARAMETER	-80 MIN.	-80 MAX.	-10 MIN.	-10 MAX.	UNIT	NOTE
t_{ESR}	$\overline{SE}$ Set-Up Time referenced to $\overline{RAS}$	0		0		ns	
t_{REH}	$\overline{SE}$ Hold Time referenced to $\overline{RAS}$	15		15			
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	60		70			
t_{TP}	$\overline{DT}$ Precharge Time	20		30			
t_{RSD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	80		100			
t_{ASD}	Column Address to First SC Delay Time (Read Transfer)	45		50			
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	25		25			
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		5			
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	15		15			
t_{SRS}	Last SC to $\overline{RAS}$ Set-Up Time (Serial Input)	30		30			
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	25		25			
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	50		50			
t_{SDZ}	Serial Output Buffer Turn-off Delay from $\overline{RAS}$ (Pseudo Write Transfer)	10	50	10	50		10
t_{SCC}	SC Cycle Time	30		30			
t_{SC}	SC Pulse Width (SC High Time)	10		10			
t_{SCP}	SC Precharge Time (SC Low Time)	10		10			
t_{SCA}	Access Time from SC		25		25		9
t_{SOH}	Serial Output Hold Time from SC	5		5			
t_{SDS}	Serial Input Set-Up Time	0		0			
t_{SDH}	Serial Input Hold Time	15		15			
t_{SEA}	Access Time from $\overline{SE}$		25		25		9
t_{SE}	$\overline{SE}$ Pulse Width	25		25			
t_{SEP}	$\overline{SE}$ Precharge Time	25		25			
t_{SEZ}	Serial Output Buffer Turn-off Delay from $\overline{SE}$	0	20	0	20		10
t_{SZE}	Serial Input to SE Delay Time	0		0			
t_{SZS}	Serial Input to First SC Delay Time	0		0			
t_{SWS}	Serial Write Enable Set-Up Time	0		0			
t_{SWH}	Serial Write Enable Hold Time	15		15			
t_{SWIS}	Serial Write Disable Set-Up Time	0		0			
t_{SWIH}	Serial Write Disable Hold Time	15		15			
t_{STS}	Split Transfer Set-Up Time	30		30			
t_{STH}	Split Transfer Hold Time	30		30			
t_{SQD}	SC-QSF Delay Time		25		25		
t_{TQD}	$\overline{DT}$-QSF Delay Time		25		25		
t_{CQD}	$\overline{CAS}$-QSF Delay Time		35		35		
t_{RQD}	$\overline{RAS}$-QSF Delay Time		75		90		

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltage are referenced to V_{SS}.

3. These parameters depend on cycle rate.

4. These parameters depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}/\overline{OE}$ "high") and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T = 5ns.

7. $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. RAM port outputs are measured with a load equivalent to 1 TTL load and 100pF.
D_{OUT} reference levels : V_{OH} / V_{OL} = 2.0V / 0.8V.

9. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
D_{OUT} reference levels : V_{OH} / V_{OL} = 2.0V / 0.8V.

10. $t_{OFF\ (max.)}$, $t_{OEZ\ (max.)}$, $t_{SDZ\ (max.)}$ and $t_{SEZ\ (max.)}$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must he satisfied for a read cycles.

12. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}$ / $\overline{WE}$ leading edge in $\overline{OE}$-controlled-write cycles and read-modify-write cycles.

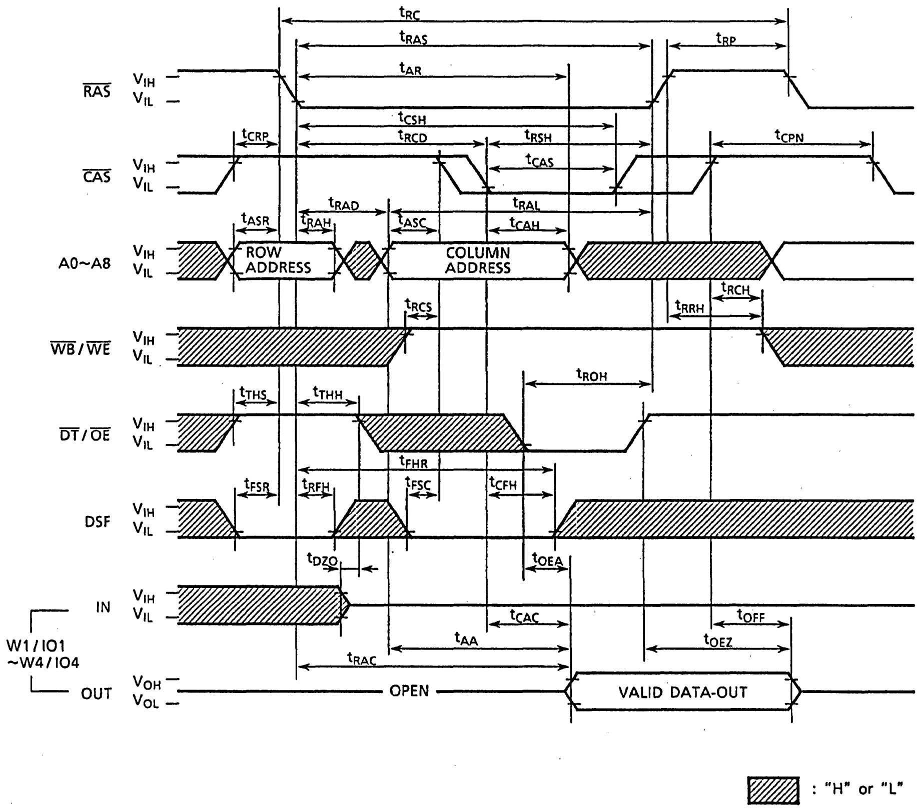
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS\ (min.)}$, the cycle is an early write cycles and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geq t_{RWD\ (min.)}$, $t_{CWD} \geq t_{CWD\ (min.)}$ and $t_{AWD} \geq t_{AWD\ (min.)}$ the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the $t_{RCD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can he met.
$t_{RCD\ (max.)}$ is specified as a reference point only : If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

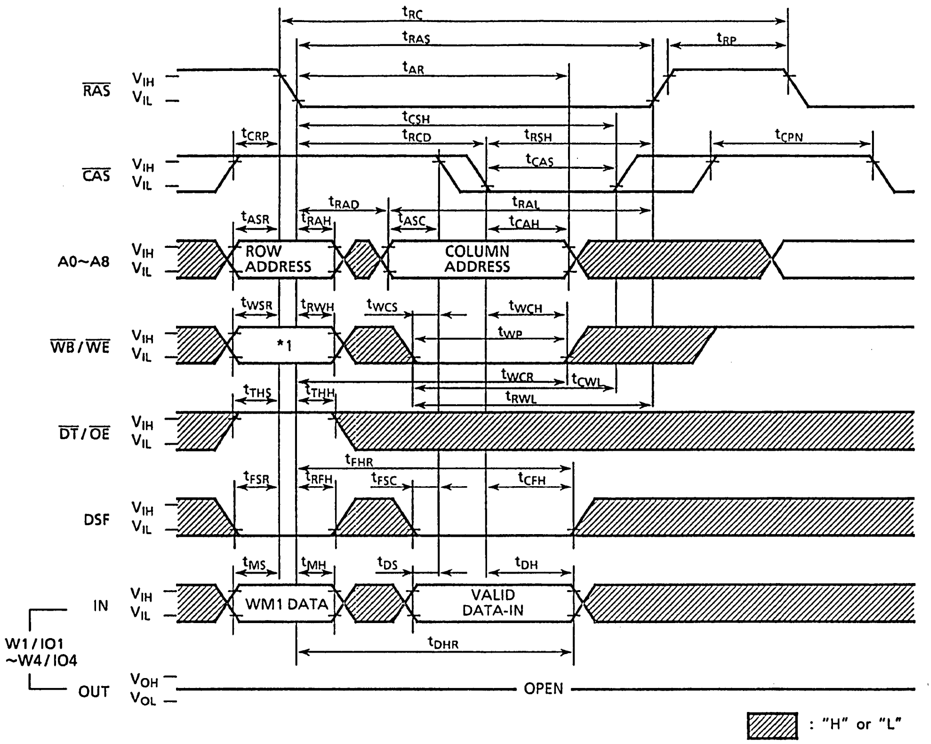
15. Operation within the $t_{RAD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

TIMING WAVEFORM

READ CYCLE



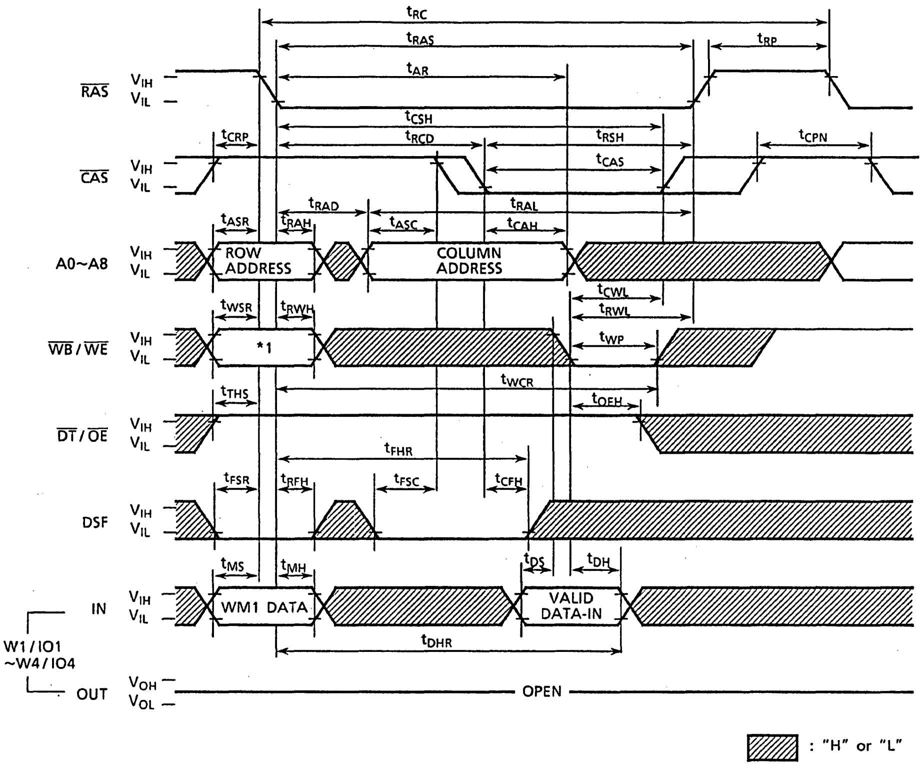
WRITE CYCLE (EARLY WRITE)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data 0: Write Disable
1: Write Enable

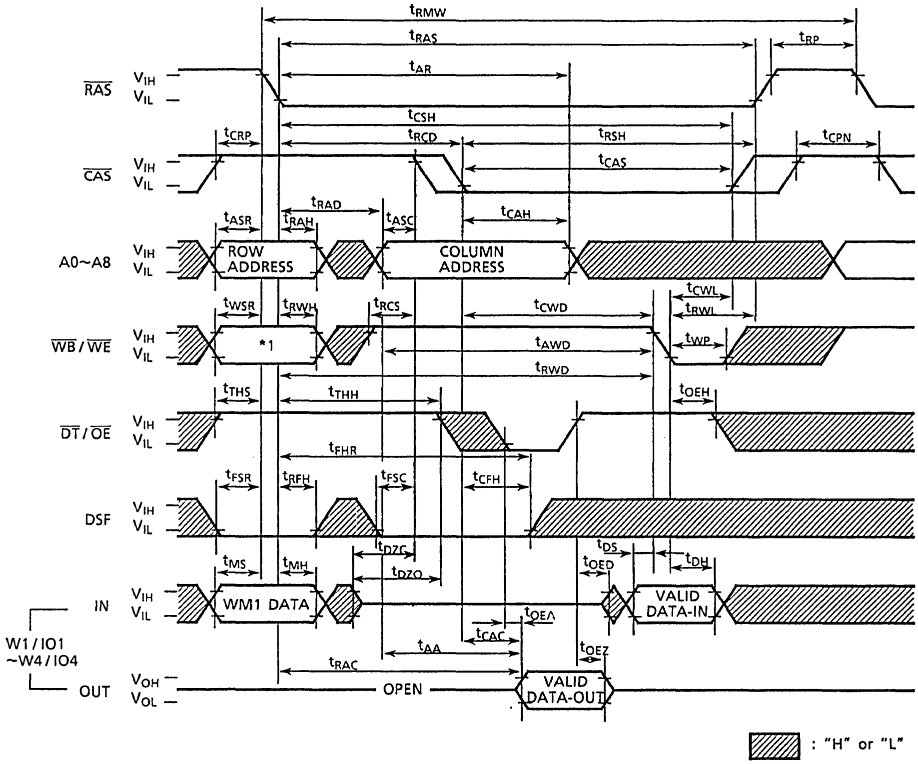
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data   0: Write Disable
            1: Write Enable

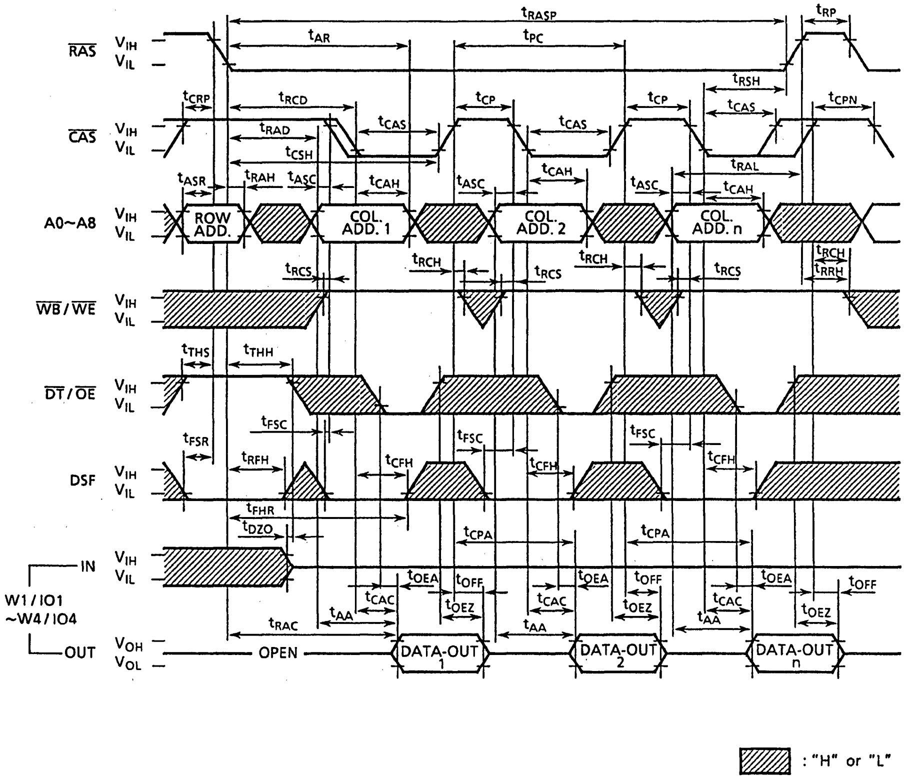
READ-MODIFY-WRITE CYCLE



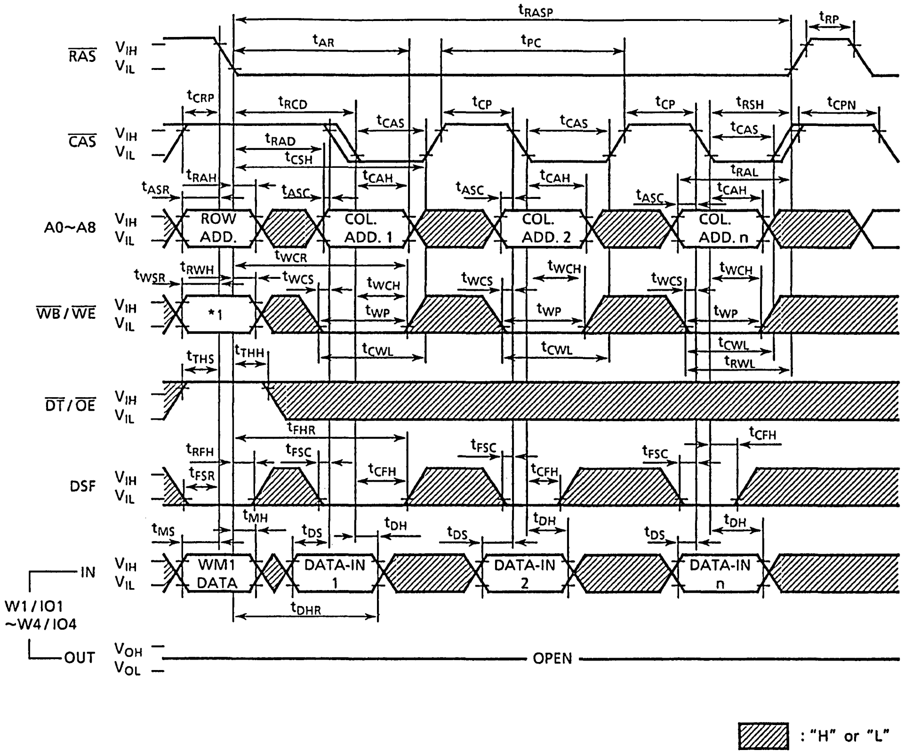
*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data 0: Write Disable
1: Write Enable

FAST PAGE MODE READ CYCLE



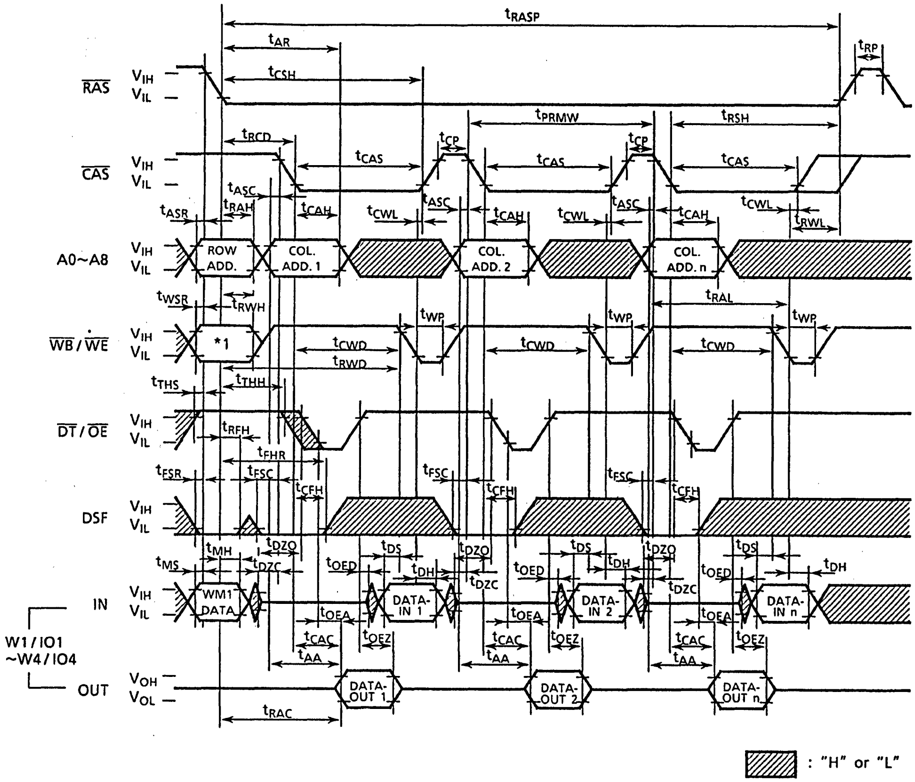
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data 0: Write Disable
1: Write Enable

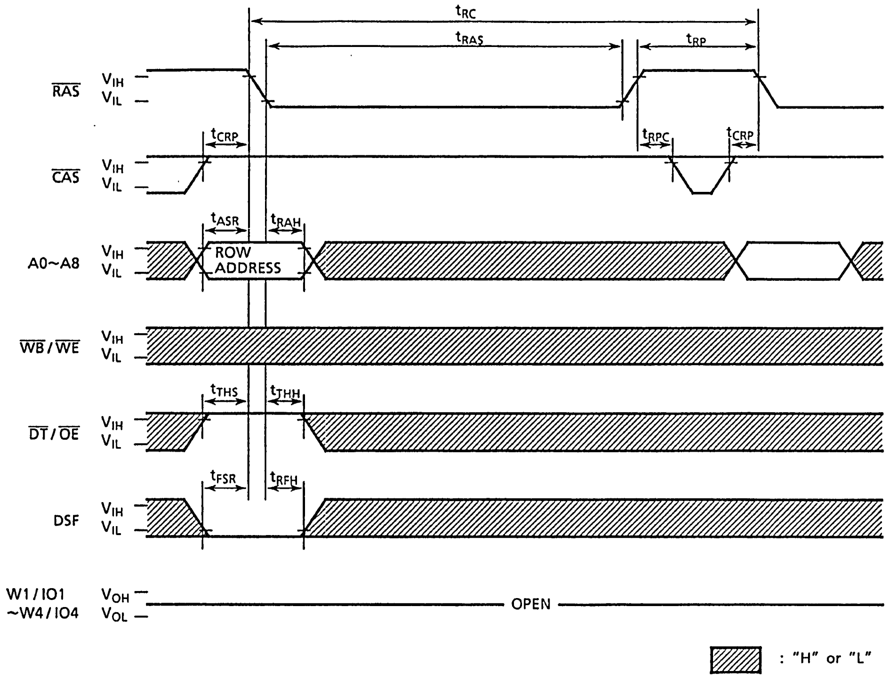
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



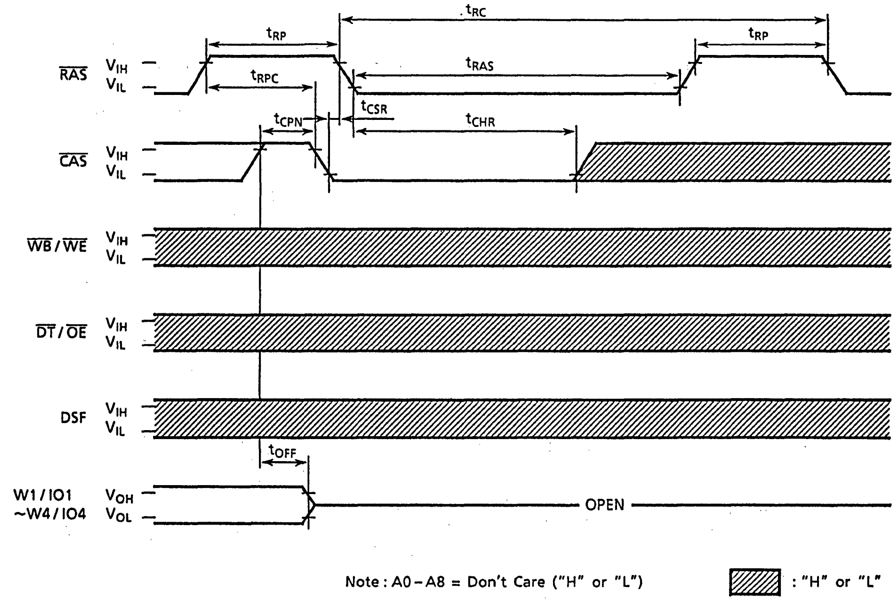
*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data 0: Write Disable
1: Write Enable

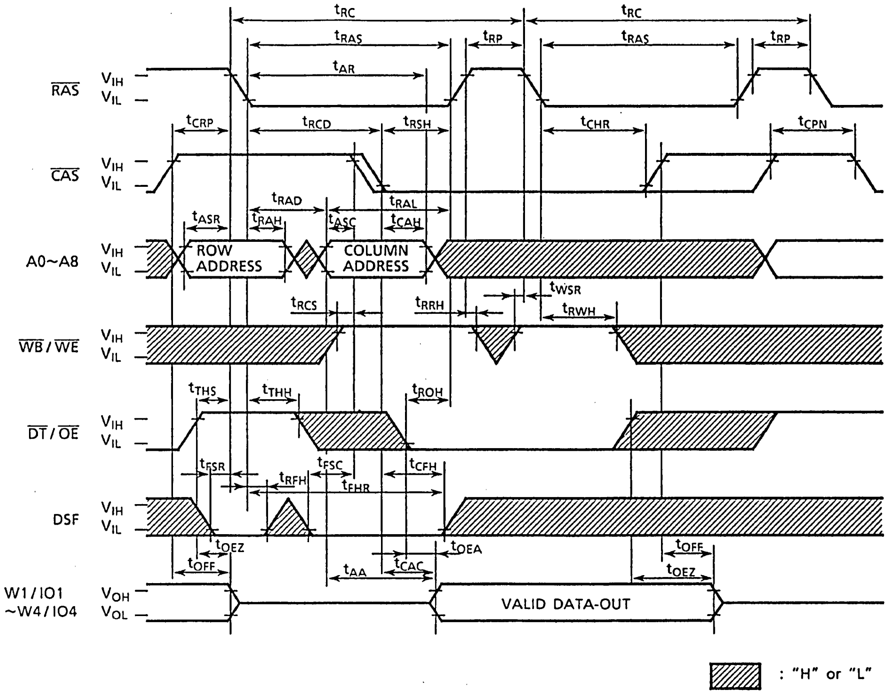
$\overline{RAS}$ ONLY REFRESH CYCLE



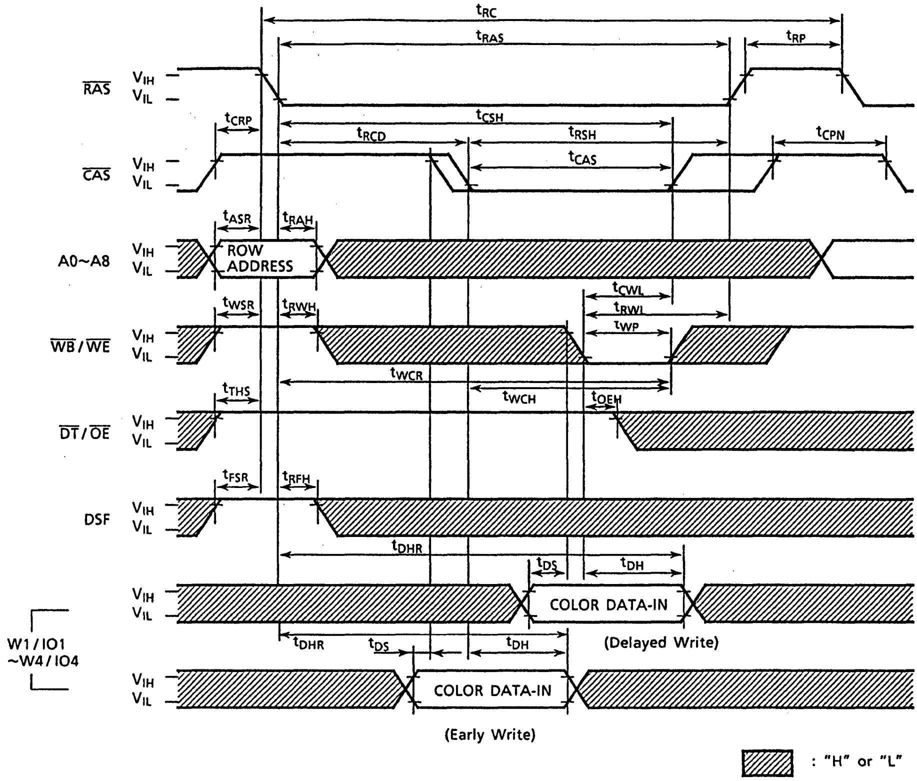
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



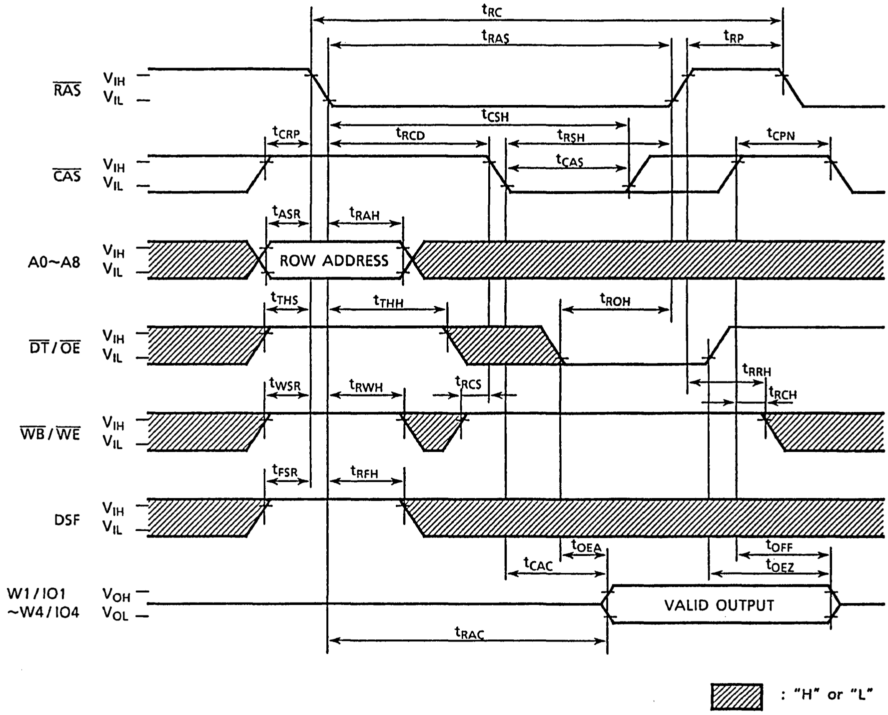
HIDDEN REFRESH CYCLE



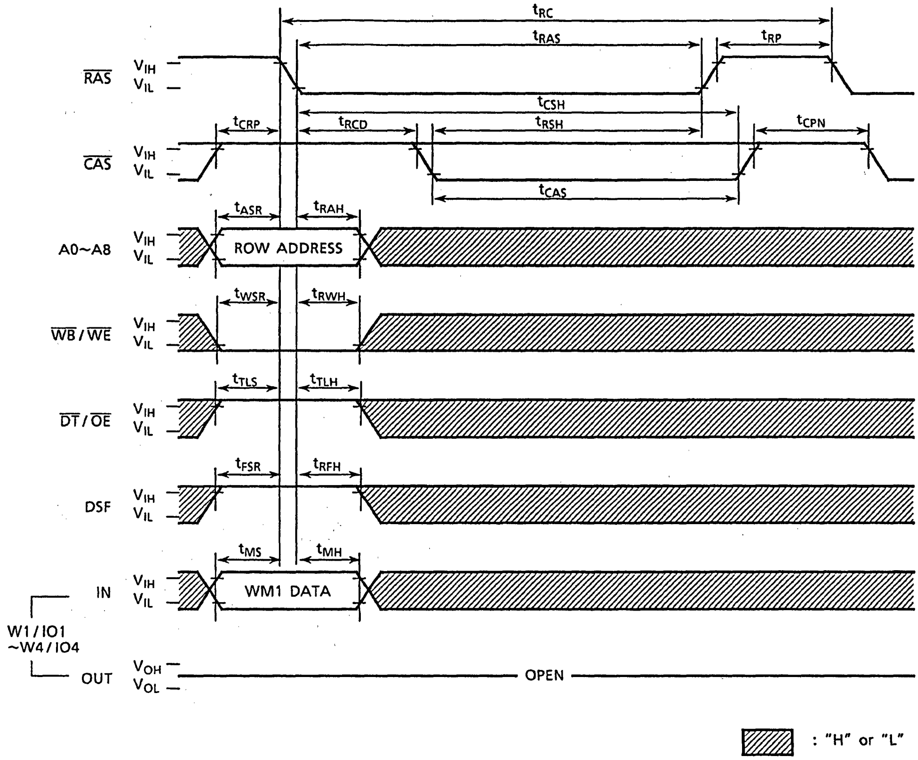
LOAD COLOR REGISTER CYCLE



READ COLOR REGISTER CYCLE

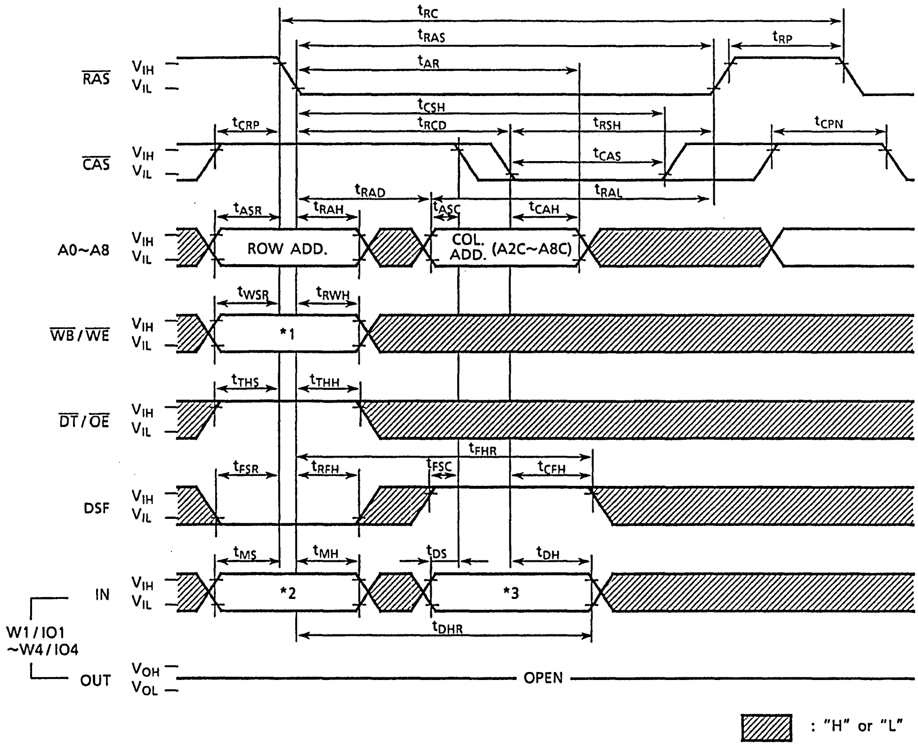


FLASH WRITE CYCLE



WM1 Data	Cycle
0	Flash Write Disable
1	Flash Write Enable

BLOCK WRITE CYCLE



*1 $\overline{WB}/\overline{WE}$	*2 W1/IO1~W4/IO4	Cycle
0	WM1 Data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

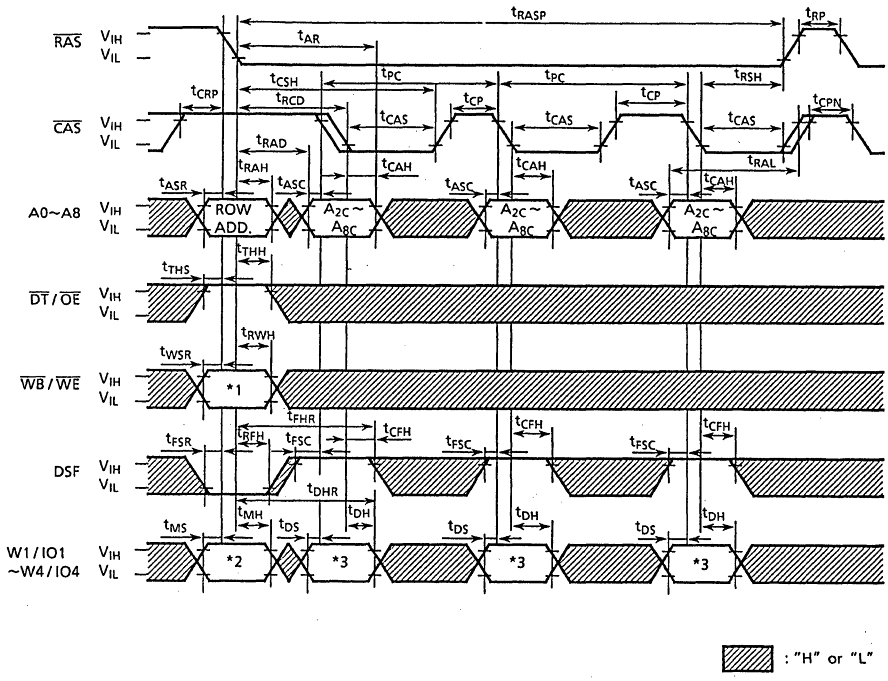
WM1 data 0: Write Disable
1: Write Enable

*3 COLUMN SELECT

W1/IO1 - Column 0 (A_{1C} = 0, A_{0C} = 0
W2/IO2 - Column 1 (A_{1C} = 0, A_{0C} = 1
W3/IO3 - Column 2 (A_{1C} = 1, A_{0C} = 0
W4/IO4 - Column 3 (A_{1C} = 1, A_{0C} = 1

Wn/IOn
=0 : Disable
=1 : Enable

PAGE MODE BLOCK WRITE CYCLE



*1 $\overline{WB}/\overline{WE}$	*2 W1/IO1~W4/IO4	Cycle
0	WM1 Data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

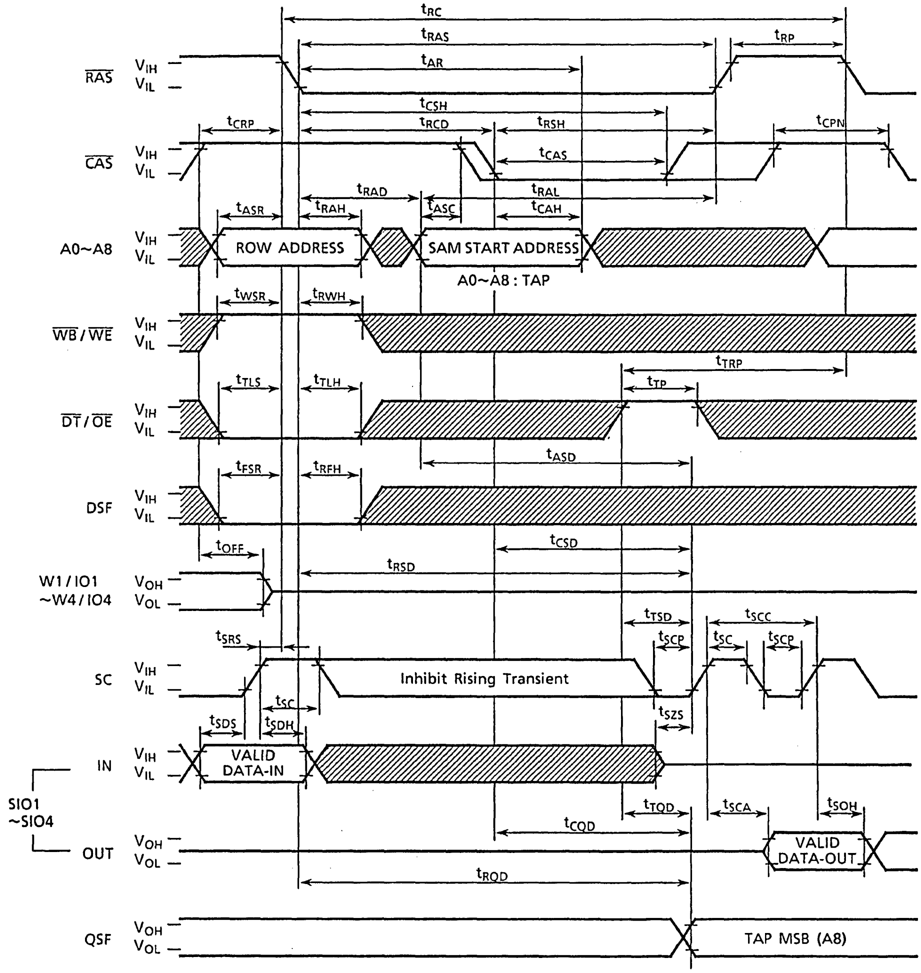
WM1 data 0: Write Disable
1: Write Enable

*3 COLUMN SELECT

W1/IO1 - Column 0 (A_{1C} = 0, A_{0C} = 0
W2/IO2 - Column 1 (A_{1C} = 0, A_{0C} = 1
W3/IO3 - Column 2 (A_{1C} = 1, A_{0C} = 0
W4/IO4 - Column 3 (A_{1C} = 1, A_{0C} = 1

Wn/IOn
=0 : Disable
=1 : Enable

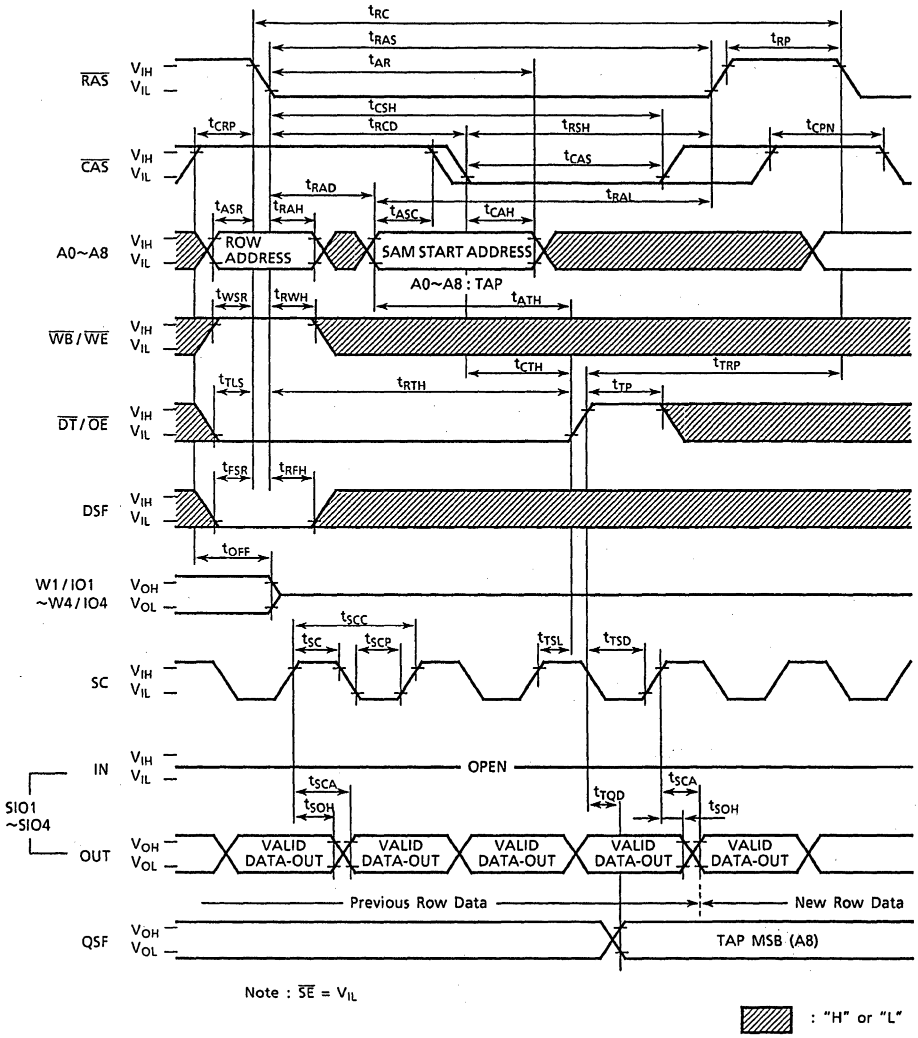
READ TRANSFER CYCLE (Previous Transfer is WRITE TRANSFER CYCLE)



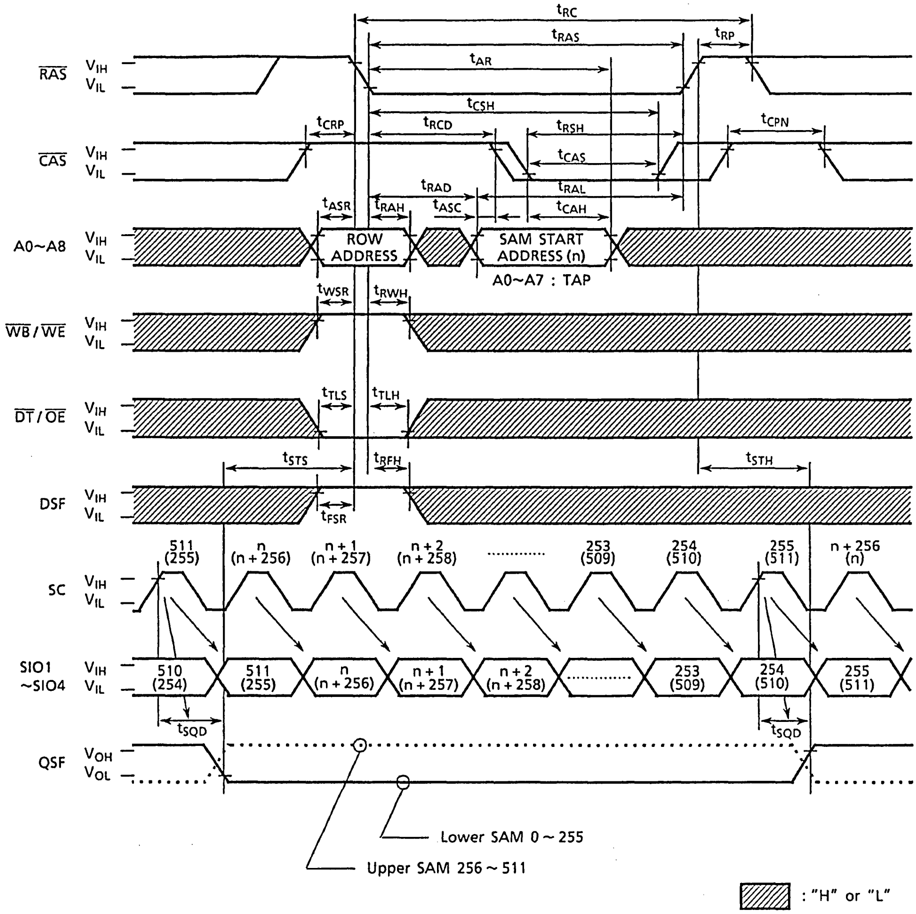
Note : $\overline{SE}$ = V_{IL}

: "H" or "L"

REAL TIME READ TRANSFER CYCLE

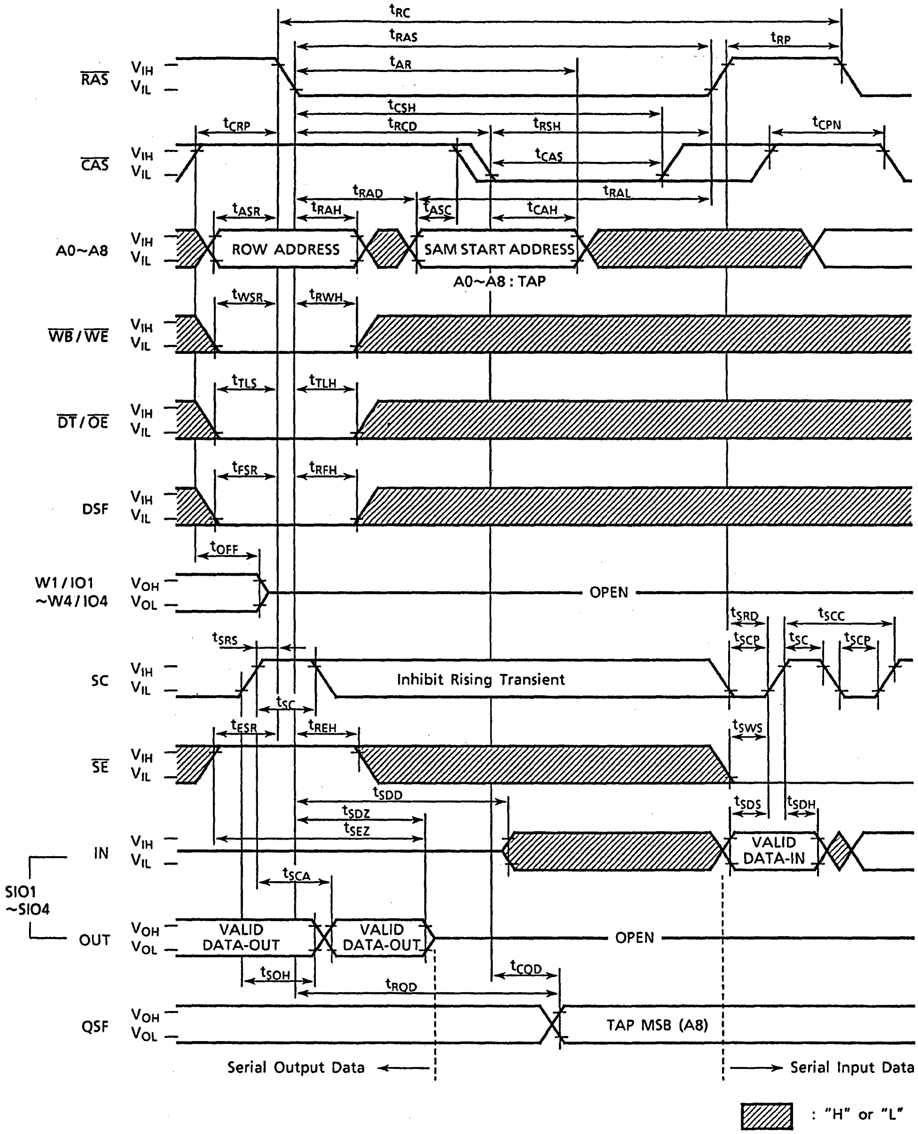


SPLIT READ TRANSFER CYCLE

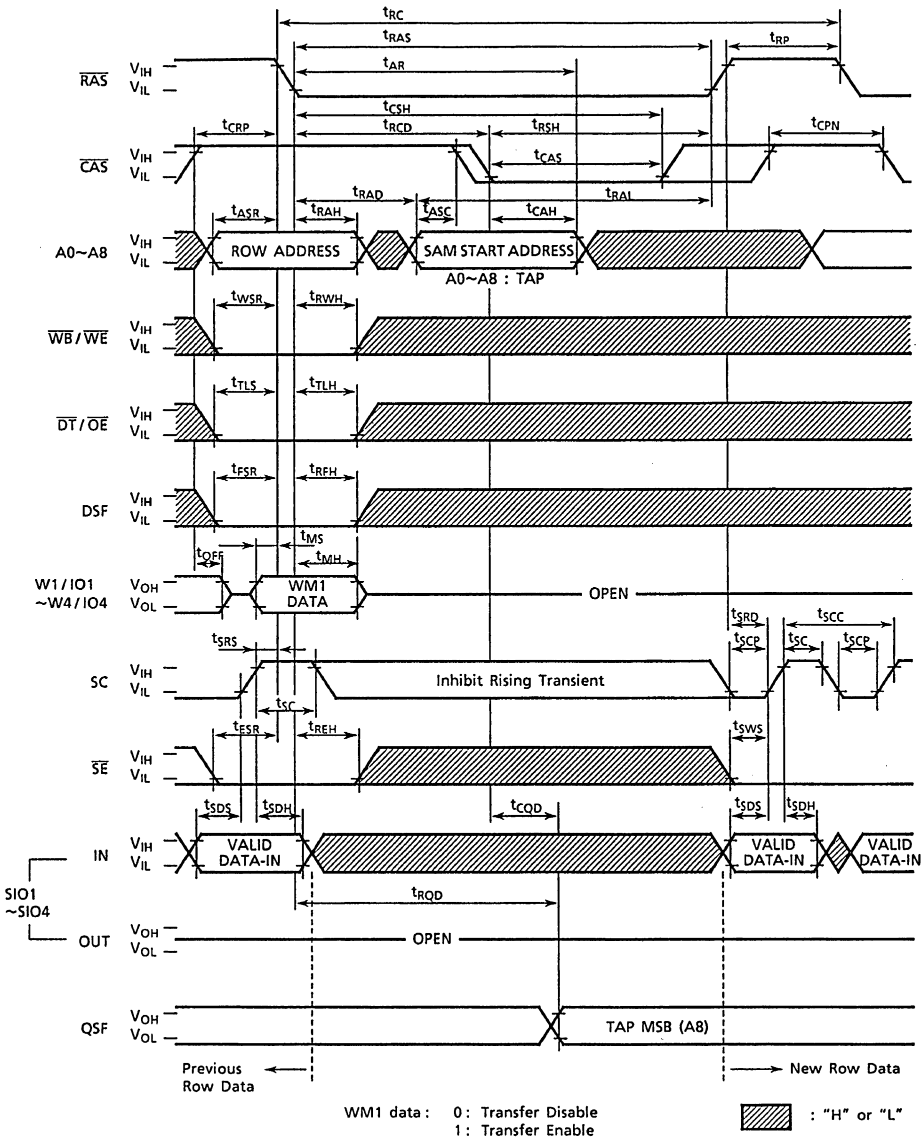


Note : $\overline{SE}$ = V_{IL}

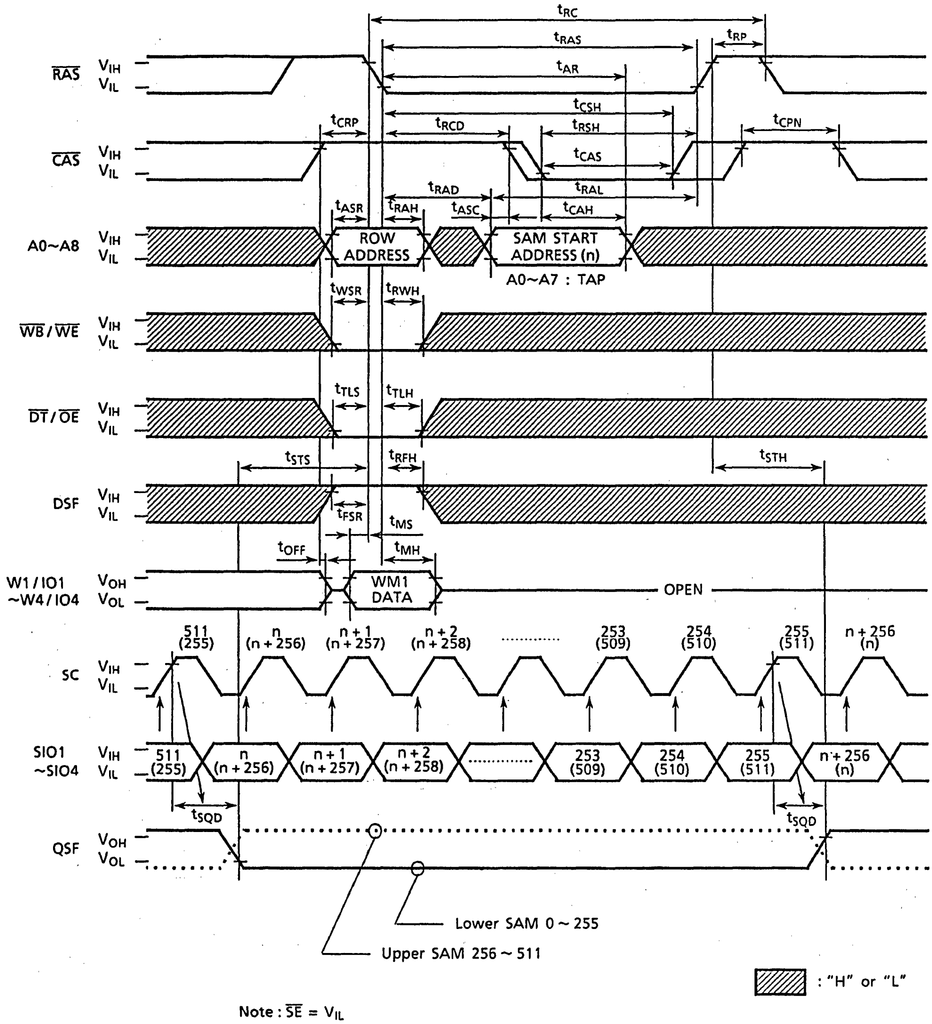
PSEUDO WRITE TRANSFER CYCLE



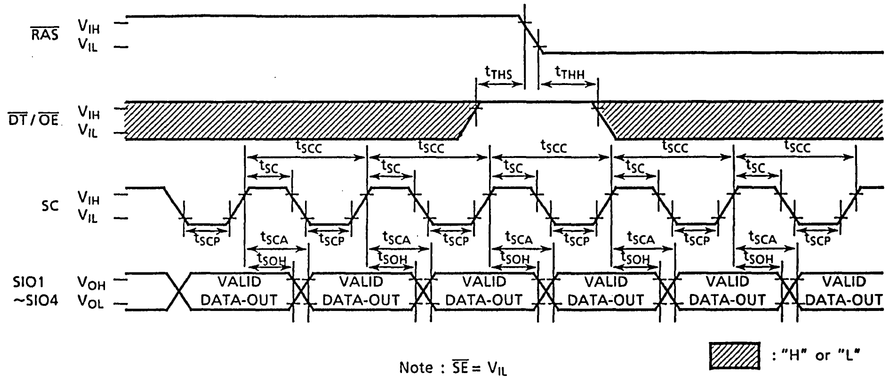
WRITE TRANSFER CYCLE



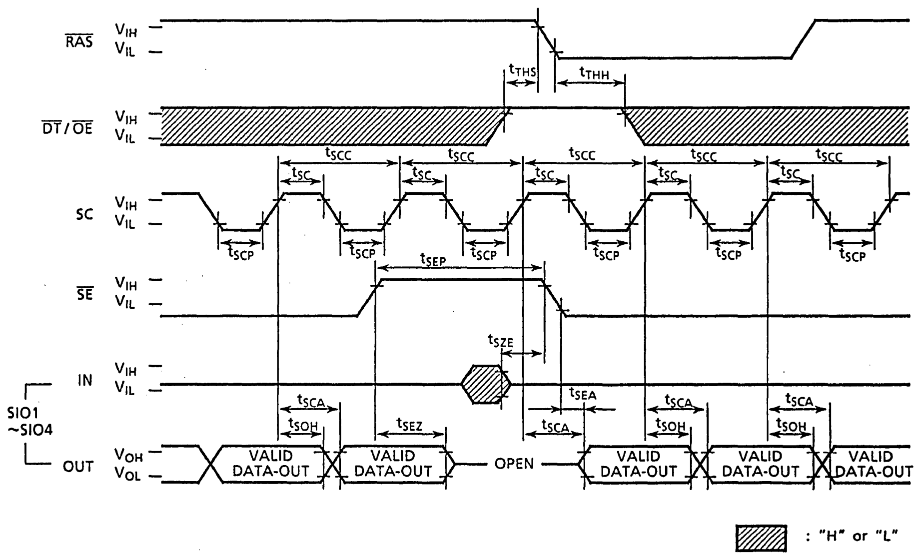
SPLIT WRITE TRANSFER CYCLE



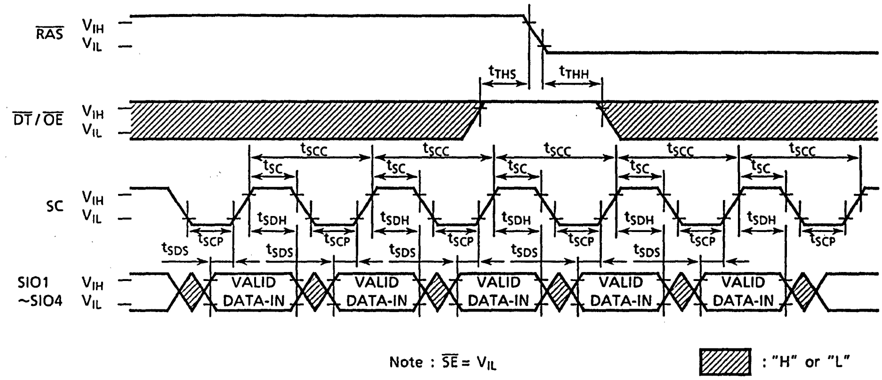
SERIAL READ CYCLE ($\overline{SE}=V_{IL}$)



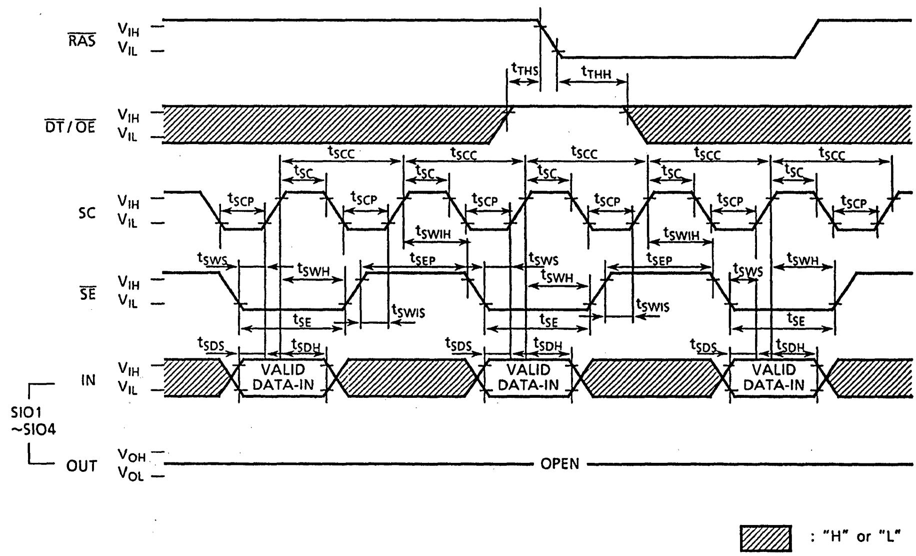
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



SERIAL WRITE CYCLE ($\overline{SE}$=V_{IL})



SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



PIN FUNCTION

ADDRESS INPUTS : $A_0 \sim A_8$

The 18 address bits required to decode 4 bits of the 1,048,576 cell locations within the dynamic RAM memory array of the TC524258B are multiplexed onto 9 address input pins (A_0~A_8). nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

ROW ADDRESS STROBE : $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$ and DSF to invoke the various random access and data transfer operating modes shown in Table 2. $\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the RAS control is held "high".

COLUMN ADDRESS STROBE : $\overline{CAS}$

$\overline{CAS}$ is the control input that latches the column address bits and the state of the special function input DSF to select, in conjunction with the $\overline{RAS}$ control, either read / write operations or the special block write feature on the RAM port when the DSF input is held "low" at the falling edge of $\overline{RAS}$. Refer to the operation truth table shown in Table 1. $\overline{CAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. $\overline{CAS}$ also acts as an output enable for the output buffers on the RAM port.

DATA TRANSFER/OUTPUT ENABLE : $\overline{DT}/\overline{OE}$

The $\overline{DT}/\overline{OE}$ input is a multifunction pin. When $\overline{DT}/\overline{OE}$ is "high" at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT}/\overline{OE}$ is used as an output enable control. When the $\overline{DT}/\overline{OE}$ is "low" at the falling edge of $\overline{RAS}$, a data transfer operation is started between the RAM port and the SAM port.

WRITE PER BIT/WRITE ENABLE : $\overline{WB}/\overline{WE}$

The $\overline{WB}/\overline{WE}$ input is also a multifunction pin. When $\overline{WB}/\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$ during RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$ during RAM port operations, the write-per-hit function is enabled. The $\overline{WB}/\overline{WE}$ input also determines the direction of data transfer between the RAM array and the serial register (SAM). When $\overline{WB}/\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer). When $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (masked-write transfer).

WRITE MASK DATA/DATA INPUT AND OUTPUT : W_1/IO_1~W_4/IO_4

When the write-per-bit function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register (WM1) at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic "1". Writing is inhibited on data lines where the write-mask data is a logic "0". The write-mask data is valid for only one cycle. Data is written into the RAM port during a write or read-modify-write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs late. During an early-write cycle, the outputs are in the high impedance state. Data is read out of the RAM port during a read or read-modify-write cycle. The output data becomes valid on the W_i/IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and column address are satisfied and will remain valid as long as $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ are kept "low". The outputs will return to the high-impedance state at the rising edge of either $\overline{CAS}$ or $\overline{DT}/\overline{OE}$, whichever occurs first.

SERIAL CLOCK : SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 9-bits serial pointer (8-bits in split register mode) which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the starting location which is determined by the column address in the read transfer cycle. When the pointer reaches the most significant address location (decimal 511), the next SC clock will place it at the least significant address location (decimal 0). The serial clock SC must he held at a constant V_{IH} or V_{IL} level during read / pseudo write / write transfer operations and should not he clocked while the SAM port is in the standby mode to prevent the SAM pointer from being incremented.

SERIAL ENABLE : $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "high".

SPECIAL FUNCTION CONTROL INPUT : DSF

The DSF input is latched at the falling edge of $\overline{RAS}$ and $\overline{CAS}$ and allows for the selection of various random port and data transfer operating modes. In addition to the conventional multiport DRAM, the special features consisting of flash write, block write, load color register and split read / write transfer can be invoked.

SPECIAL FUNCTION OUTPUT : QSF

QSF is an output signal which, during split register mode, indicates which half of the split SAM is being accessed. QSF "low" indicates that the lower split SAM (Bit 0~255) is being accessed and QSF "high" indicates that the upper split SAM (Bit 256~511) is being accessed. QSF is monitored so that after it toggles and after allowing for a delay of t_{STS}, split read / write transfer operation can be performed on the non-active split SAM.

SERIAL INPUT/OUTPUT : SIO1~SIO4

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode. During subsequent write transfer cycle, the SAM remains in the input mode.

OPERATION MODE

The RAM port and data transfer operating of the TC524258B are determined by the state of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$ and DSF at the falling edge of $\overline{RAS}$ and by the state of DSF at the falling edge of $\overline{CAS}$. The Table 1 and the Table 2 show the operation truth table and the functional truth table for a listing of all available RAM port and transfer operation, respectively.

Table 1. Operaton Truth Table

$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	DSF ($\overline{CAS}$ falling edge) 0 / DSF ($\overline{RAS}$ falling edge) 0	0 / 1	1 / 0	1 / 1
0	*	*	*	$\overline{CAS}$ before $\overline{RAS}$ Refresh			
1	0	0	0	Masked Write Transfer	Split Write Transfer with Mask	Masked Write Transfer	Split Write Transfer with Mask
1	0	0	1	Pseudo Write Transfer		Pseudo Write Transfer	
1	0	1	*	Read Transfer	Split Read Transfer	Read Transfer	Split Read Transfer
1	1	0	*	Read/Write per Bit	Masked Flash Write	Masked Block Write	Masked Flash Write
1	1	1	*	Read/Write	Load Color	Block Write	Load Color

Table 2. Functional Truth Table

Function	$\overline{RAS}$ ↓					$\overline{CAS}$ ↓	Address		W/IO			Write Mask	Register	
	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DSF	$\overline{SE}$	DSF	$\overline{RAS}$ ↓	$\overline{CAS}$ ↓	$\overline{RAS}$ ↓	$\overline{CAS}$ ↓	$\overline{CAS}$ ↓ $\overline{WE}$ ↓		WM1	Color
$\overline{CAS}$ before $\overline{RAS}$ Refresh	0	*	*	*	*	-	*	-	*	-	-	-	-	-
Masked Write Transfer	1	0	0	0	0	*	Row	TAP	WM1	*	*	WM1	Load use	-
Pseudo Write Transfer	1	0	0	0	1	*	Row	TAP	*	*	*	-	-	-
Split Write Transfer	1	0	0	1	*	*	Row	TAP	WM1	-	*	WM1	Load use	-
Read Transfer	1	0	1	0	*	*	Row	TAP	*	*	*	-	-	-
Split Read Transfer	1	0	1	1	*	*	Row	TAP	*	*	*	-	-	-
Write per Bit	1	1	0	0	*	0	Row	Column	WM1	-	DIN	WM1	Load use	-
Masked Block Write	1	1	0	0	*	1	Row	Column A2C-8C	WM1	Column Select	-	WM1	Load use	use
Masked Flash Write	1	1	0	1	*	*	Row	*	WM1	-	*	WM1	Load use	use
Read Write	1	1	1	0	*	0	Row	Column	*	-	DIN	-	-	-
Block Write	1	1	1	0	*	1	Row	Column A2C-8C	*	Column Select	-	-	-	use
Load Color	1	1	1	1	*	*	Row	*	*	-	Color	-	-	Load

* : "0" or "1" , TAP : SAM start address , : not used

If the special function control input (DSF) is in the "low" state at the falling edges of $\overline{RAS}$ and $\overline{CAS}$, only the conventional multiport DRAM operating features can be invoked: $\overline{CAS}$-before-$\overline{RAS}$ refresh, write transfer, pseudo-write transfer, read transfer and read write modes. If the DSF input is "high" at the falling edge of $\overline{RAS}$, special features such as split write transfer, split read transfer, flash write and load color register can be invoked. If the DSF input is "low" at the falling edge of $\overline{RAS}$ and "high" at the falling edge of $\overline{CAS}$, the block write special feature can be invoked.

RAM PORT OPERATION

FAST PAGE MODE CYCLE

Fast page mode allows data to be transferred into or out of multiple column locations of the same row by performing multiple $\overline{CAS}$ cycle during a single active $\overline{RAS}$ cycle. During a fast page cycle, the $\overline{RAS}$ signal may be maintained active for a period up to 100 µseconds. For the initial fast page mode access, the output data is valid after the specified access times from $\overline{RAS}$, $\overline{CAS}$, column address and $\overline{DT}/\overline{OE}$. For all subsequent fast page mode read operations, the output data is valid after the specified access times from $\overline{CAS}$, column address and $\overline{DT}/\overline{OE}$, When the write-per-bit function is enabled, the mask data latched at the falling edge of $\overline{RAS}$ is maintained throughout the fast page mode write or read-modify-write cycle.

$\overline{RAS}$-ONLY REFRESH

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-Only" cycle.

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

The TC524258BJ/BZ also offers an internal-refresh function. When $\overline{CAS}$ is held "low" for a specified period (t_{CSR}) before $\overline{RAS}$ goes "low", an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ cycle. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, $\overline{CAS}$ can remain "low" while cycling $\overline{RAS}$.

HIDDEN REFRESH

A hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh performed by holding $\overline{CAS}$ "low" from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling RAS after the specified $\overline{RAS}$-precharge period (Refer to Figure 1)

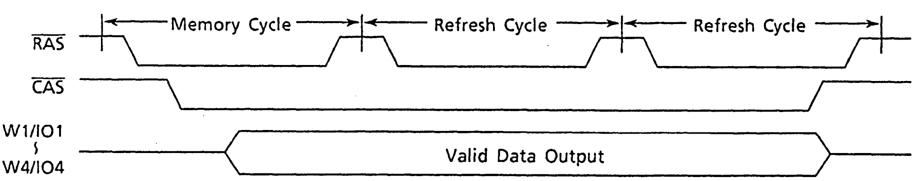


Figure 1. Hidden Refresh Cycle

WRITE-PER-BIT FUNCTION

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB}$ / $\overline{WE}$ is held "low" at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the Wi / IOi pins is latched onto the write-mask register (WM1). When a "0" is sensed on any of the Wi / IOi pins, their corresponding write circuits are disabled and new data will not be written, When a "1" is sensed on any of the Wi / IOi pins, their corresponding write circuits will remain enabled so that new data is written. The truth table of the write-per-bit function is shown in Table 3.

Table 3. Truth table for write-per-bit function

At the falling edge of $\overline{RAS}$				Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	Wi/IOi (i=1~4)	
H	H	H	*	Write Enable
H	H	L	1	Write Enable
			0	Write Mask

An example of the write-per-bit function illustrating its application to displays is shown in Figures 2 and 3.

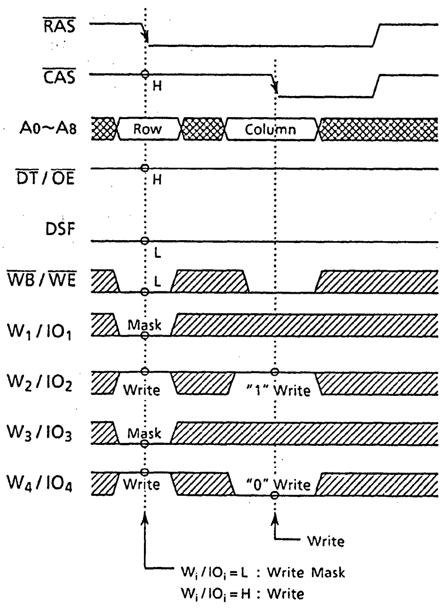


Figure 2. Write-per-bit timing cycle

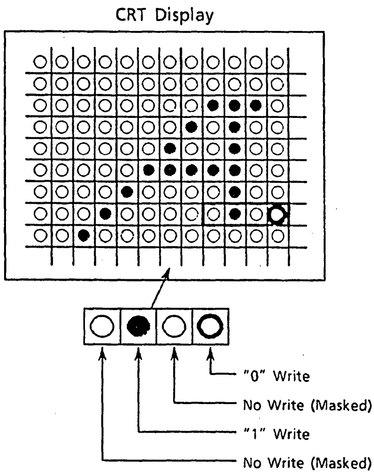


Figure 3. Corresponding bit-map

LOAD COLOR REGISTER/READ COLOR REGISTER

The TC524258B is provided with an on-chip 4-bits register (color register) for use during the flash write or block write operation. Each bit of the color register corresponds to one of the DRAM I/O blocks. The load color register cycle is initiated by holding $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and DSF "high" at the falling edge of $\overline{RAS}$. The data presented on the W_i/IO_i lines is subsequently latched into the color register at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs last. The data stored in the color register can be read out by performing a read color register cycle. This cycle is activated by holding $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and DSF "high" at the falling edge of $\overline{RAS}$ and by holding $\overline{WB}/\overline{WE}$ "high" at the falling edge of $\overline{CAS}$ and throughout the remainder of the cycle. The data in the color register becomes valid on the W_i/IO_i lines after the specified access times from $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ are satisfied. During the load/read color register cycle, valid A_0~A_8 row addresses are not required, but the memory cells on the row address latched at the falling edge of $\overline{RAS}$ are refreshed.

FLASH WRITE

Flash write is a special RAM port write operation which in a single $\overline{RAS}$ cycle, allows for the data in the color register to be written into all the memory locations of a selected row. Each bit of the color register corresponds to one of the DRAM I/O blocks and the flash write operation can be selectively controlled on an I/O basis in the same manner as the write-per-bit operation.

A flash write cycle is performed by holding $\overline{CAS}$ "high", $\overline{WB}/\overline{WE}$ "low" and DSF "high" at the falling edge of $\overline{RAS}$. The mask data must also be provided on the W_i/IO_i lines at the falling edge of $\overline{RAS}$ in order to enable the flash write operation for selected I/O blocks (Refer to Figure 4 and 5).

Flash write is most effective for fast plane clear operations in frame buffer applications. Selected planes can be cleared by performing 512 flash write cycle and by specifying a different row address location during each flash write cycle (Refer to Figure 6). Assuming a cycle time of 180ns, a plane clear operation can be completed in less than 92.2 µseconds.

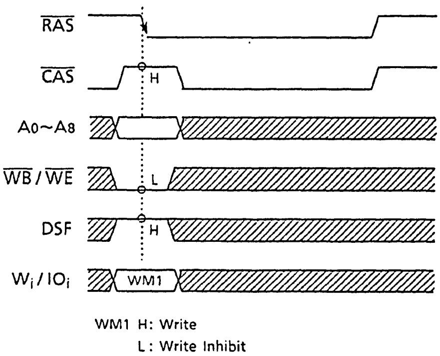


Figure 4. Flash Write Timing

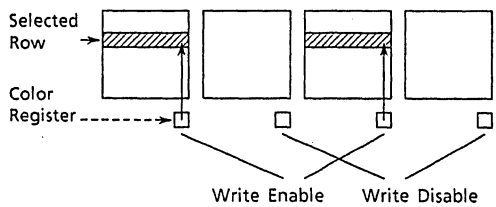


Figure 5. Flash Write

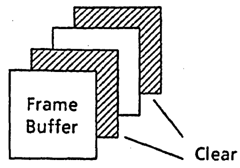


Figure 6. Plane clear application example

BLOCK WRITE

Block write is also a special RAM port write operation which, in a single $\overline{RAS}$ cycle, allows for the data in the color register to be written into 4 consecutive column address locations starting from a selected column address in a selected row. The block write operation can be selectively controlled on an I/O basis and a column mask capability is also available.

A block write cycle is performed by holding $\overline{CAS}$, $\overline{DT}/\overline{OE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$ and by holding DSF "high" at the falling edge of $\overline{CAS}$. The state of the $\overline{WB}/\overline{WE}$ input at the falling edge of $\overline{RAS}$ determines whether or not the I/O data mask is enabled ($\overline{WB}/\overline{WE}$ must be "low " to enable the I/O data mask or "high" to disable it). At the falling edge of $\overline{RAS}$, a valid row address and I/O mask data are also specified. At the falling edge of $\overline{CAS}$, the starting column address location and column mask data must be provided. During a block write cycle, the 2 least significant column address locations (A0C and A1C) are internally controlled and only the seven most significant column addresses (A2C~A8C) are latched at the falling edge of $\overline{CAS}$. (Refer to Figure 7).

An example of the block write function is shown in Figure 8 with a data mask on W_1~ /IO_1, W_4 / IO_4 and column 2. Block write is most effective for window clear and fill operation in frame buffer applications, as shown in the examples in Figure 9.

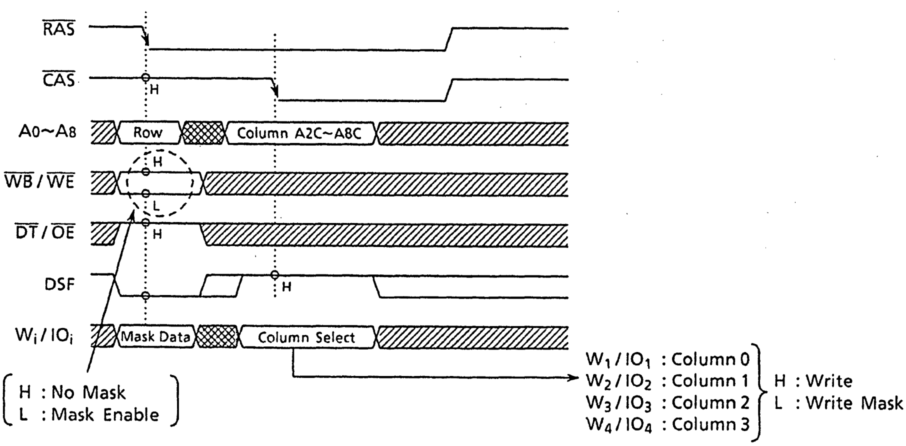


Figure 7. Block Write Timing

	Mask Data	Column Select	Color Resister Data
W_1 / IO_1	0	1	0
W_2 / IO_2	1	1	0
W_3 / IO_3	1	0	1
W_4 / IO_4	0	1	1

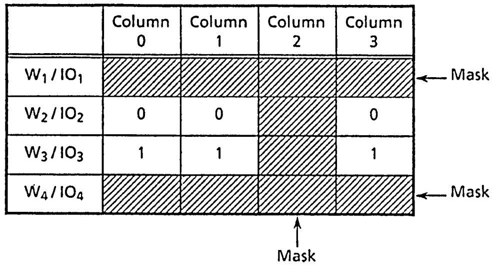


Figure 8. Example of Block Write Operation

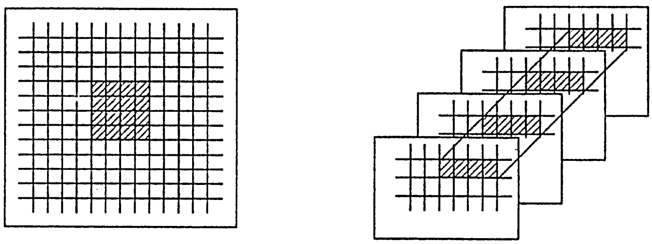


Figure 9. Examples of Block Write Application

FAST PAGE MODE BLOCK WRITE CYCLE

Fast page mode block write can be used to perform high speed clear and fill operations. The cycle is initiated by holding the DSF signal "low" at the falling edge of $\overline{RAS}$ and a fast page mode block write is performed during each subsequent $\overline{CAS}$ cycle with DSF held "high" at the falling edge of $\overline{CAS}$.

If the DSF signal is "low" at the falling edge of $\overline{CAS}$, a normal fast page mode read / write operation will occur. Therefore a combination of block write and read / write operations can be performed during a fast page mode block write cycle. Refer to the example shown in Figure 10.

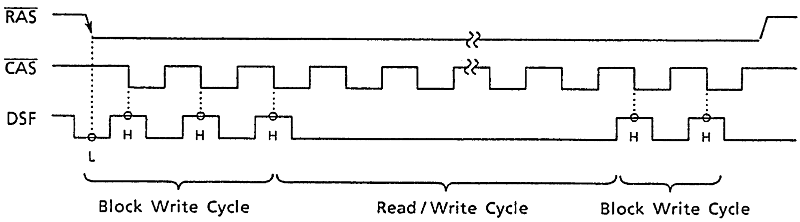


Figure 10. Fast Page Mode Block Write Cycle

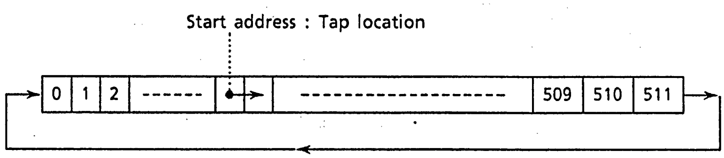
SAM PORT OPERATION

The TC524258B is provided with 512 words by 4 bits serial access memory (SAM) which can be operated in the single register mode or the split register mode.

SINGLE REGISTER MODE

When operating in the single register mode, high speed serial read or write operations can be performed through the SAM port independent of the RAM port operations, except during read / write / pseudo-write transfer cycles. The preceding transfer operation determines the direction of data flow through the SAM port. If the preceding transfer operation is a read transfer, the SAM port is in the output mode. If the preceding transfer operation is a write or pseudo write transfer, the SAM port is in the input mode. The pseudo write transfer operation only switches the SAM port from output mode to input mode; Data is not transferred from SAM to RAM.

Serial data can be read out of the SAM port after a read transfer (RAM→SAM) has been performed. The data is shifted out of the SAM port starting at any of the 512 bits locations. The TAP location corresponds to the column address selected at the falling edge of $\overline{CAS}$ during the read transfer cycle. The SAM registers are configured as circular data registers. The data is shifted out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit, as illustrated below.



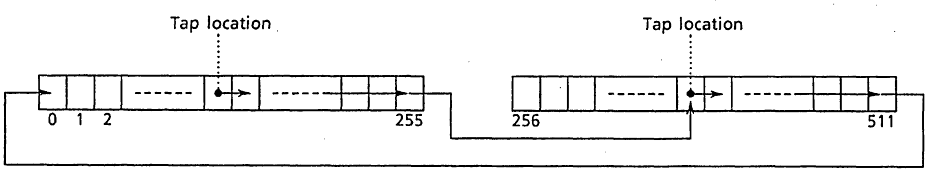
Subsequent real-time read transfer may be performed on-the-fly as many times as desired, within the refresh constraints of the DRAM array. Simultaneous serial read operation can be performed with some timing restrictions. A pseudo write transfer cycle is performed to change the SAM port from output mode to input mode in order to write data into the serial registers through the SAM port. A write transfer cycle must be used subsequently to load the SAM data into the RAM row selected by the row address at the falling edge of $\overline{RAS}$. The starting location in the SAM registers for the next serial write is selected by the column address at the falling edge of $\overline{CAS}$. The truth table for single register mode SAM operation is shown in Table 4.

Table 4. Truth Table for SAM Port Operation

SAM PORT OPERATION	$\overline{DT}/\overline{OE}$ at the falling edge of $\overline{RAS}$	SC	$\overline{SE}$	FUNCTION	Preceded by a
Serial Output Mode	H	⎍	L	Enable Serial Read	Read Transfer
			H	Disable Serial Read	
Serial Input Mode		⎍	L	Enable Serial Write	Write Transfer
			H	Disable Serial Write	
Serial Inut Mode		⎍	L	Enable Serial Write	Pseudo Write Transfer
			H	Disable Serial Write	

SPLIT REGISTER MODE

In split register mode, data can be shifted into or out of one half of the SAM while a split read or split write transfer is being performed on the other half of the SAM. A normal (Non-split) read / write / pseudo write transfer operation must precede any split read / write transfer operation. The non-split read, write and pseudo write transfer will set the SAM port into output mode or input mode. The split read and write transfers will not change the SAM port mode set by preceding normal transfer operation. RAM port operation may be performed independently except during split transfers. In the split register mode, serial data can be shifted in or out of one of the split SAM registers starting from any at the 256 tap locations, excluding the last address of each split SAM, data is shifted in or out sequentially starting from the selected tap location to the most significant bit (255 or 511) of the first split SAM and then the SAM pointer moves to the tap location selected for the second split SAM to shift data in or out sequentially starting from this tap location to the most significant bit (511 or 255) and finally wraps around to the least significant bit, as illustrated in the example below.



REFRESH

The SAM data registers are static flip-flop, therefore a refresh is not required.

DATA TRANSFER OPERATION

The TC524258B features two types of internal bidirectional data transfer capability between RAM and the SAM, as shown in Figure 11. During a normal (Non-split) transfer, 512 words by 4 bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer). During a split transfer, 256 words by 4 bits of data can be loaded from the lower / upper half of the RAM into the lower / upper half of the SAM (Split Read Transfer) or from the lower/upper half of the SAM into the lower/upper half of the RAM (Split Write Transfer). The normal transfer and split transfer modes are controlled by the DSF special function input signal

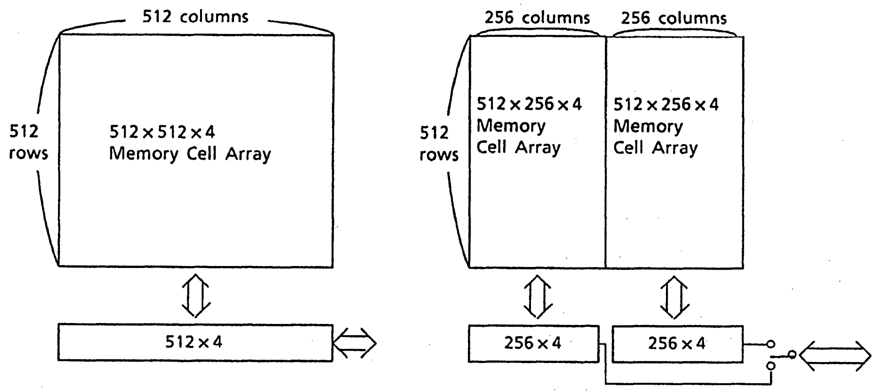


Figure 11. (a) Normal (Non-split) Transfer (b) Split Transfer

As shown in Table 5, the TC524258B supports five types of transfer operations: Read transfer, Split read transfer, Write transfor, Split write transfer and Pseudo write transfer. Data transfer operations between RAM and SAM are invoked by holding the $\overline{DT}/\overline{OE}$ signal "low" at the falling edge of $\overline{RAS}$. The type of data transfer operation is determined by the state of $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$ and DSF latched at the falling edge of $\overline{RAS}$. During normal (Non-split) data transfer operations, the SAM port is switched from input to output mode (Read transfer) or output to input mode (Write transfer / Pseudo write transfer) whereas it remains unchanged during split transfer operations (Split read or split write transfers). During a data transfer cycle, the row address A_0~A_8 select one of the 512 rows of the memory array to or from which data will be transferred and the column address A_0~A_8 select one of the tap locations in the serial register. The selected tap location is the start position in the SAM port from which the first serial data will be read out during the subsequent serial read cycle or the start position in the SAM port into which the first serial data will be written during the subsequent serial write cycle. During split data transfer cycles, the most significant column address (A8C) is controlled internally to determine which half of the serial register will be reloaded from the RAM array.

Table 5. Transfer Modes

at the falling edge of $\overline{RAS}$					Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	DSF				
H	L	H	*	L	Read Transfer	RAM → SAM	512x4	Input → Output
H	L	L	L	L	Write Transfer	SAM → RAM	512x4	Output → Input
H	L	L	H	L	Pseudo Write Transfer	—	—	Output → Input
H	L	H	*	H	Split Read Transfer	RAM → SAM	256x4	Not changed
H	L	L	*	H	Split Write Transfer	SAM → RAM	256x4	Not changed

* : "H" or "L"

READ TRANSFER CYCLE

A read transfer consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low" $\overline{WB}/\overline{WE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of $\overline{DT}/\overline{OE}$. When the transfer is completed, the SAM port is set into the output mode. In a read / real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and this data becomes valid on the SIO lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Figure 12 shows the operation block diagram for read transfer operation.

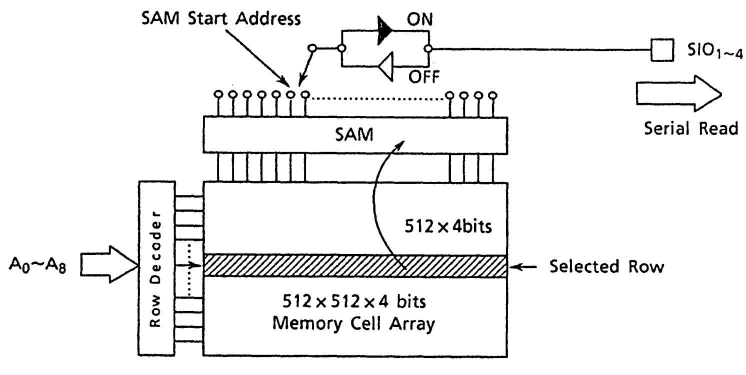


Figure 12. Block Diagram. for Read Transfer Operation

In a read transfer cycle (which is preceded by a write transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}/\overline{OE}$, as shown in Figure 13.

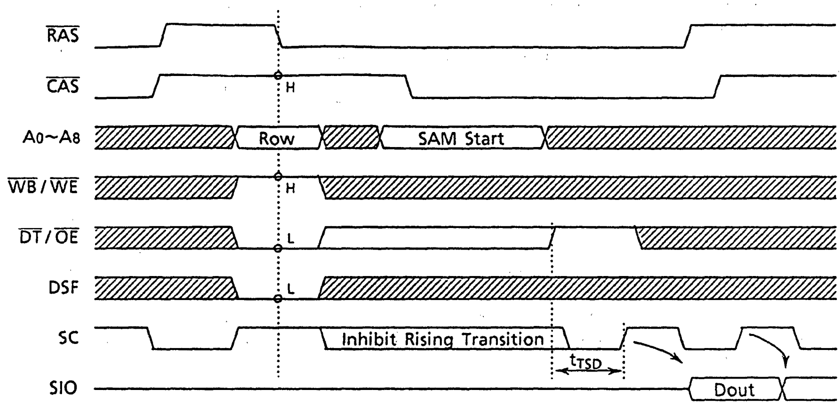


Figure 13. Read Transfer Timing

In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SIO lines until the $\overline{DT}/\overline{OE}$ signal goes "high" and the serial access time t_{SCA} for the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (t_{RTH}, t_{CTH}, and t_{TSL}/t_{TSD} must be satisfied), as shown in Figure 14.

The timing restriction t_{TSL}/ t_{TSD} are 5ns min / 15ns min. The split read transfer mode eliminates these timing restrictions.

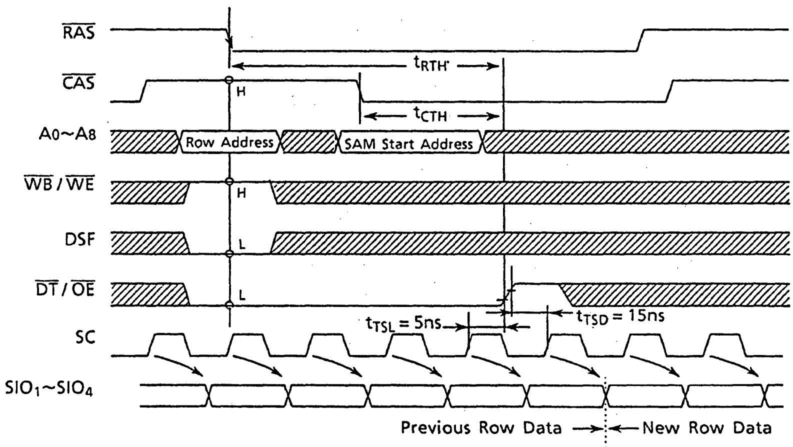


Figure 14. Real Time Read Transfer

WRITE TRANSFER CYCLE

A write transfer cycle consist of loading the content of the SAM register into a selected row of the RAM array. If the SAM data to be transferred must first be loaded through the SAM port, a pseudo write transfer operation must precede the write transfer cycles. However, if the SAM port data to be transferred into the RAM was previously loaded into the SAM via a read transfer, the SAM to RAM transfer can be executed simply by performing a write transfer directly. A write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low", $\overline{SE}$ "low" and DSF "low" at the falling edge of $\overline{RAS}$. This write transfer is selectively controlled per RAM I/O block by setting the mask data on the W_i/IO_i lines at the falling edge of $\overline{RAS}$ (same as in the write-per-bit operation). Figure 15 and 16 show the timing diagram and block diagram for write transfer operations, respectively.

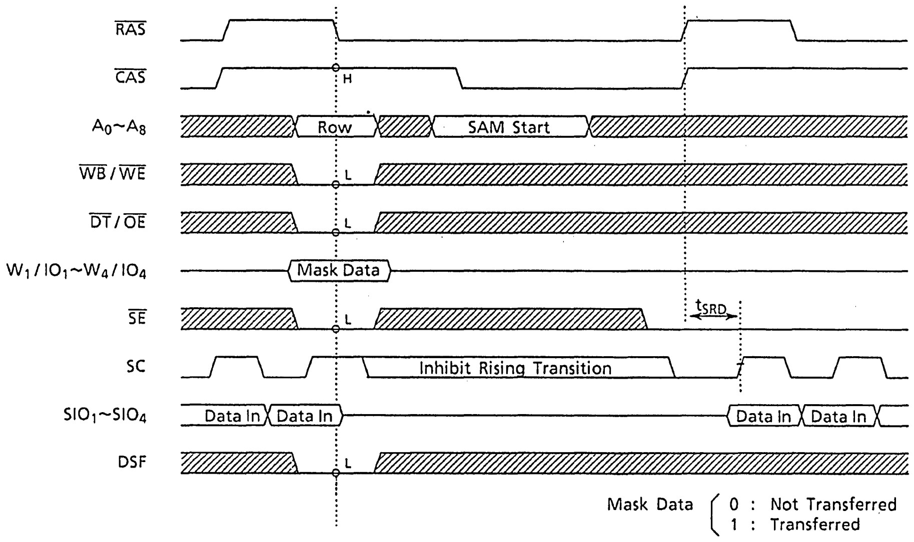


Figure 15. Write Transfer Timing

The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.

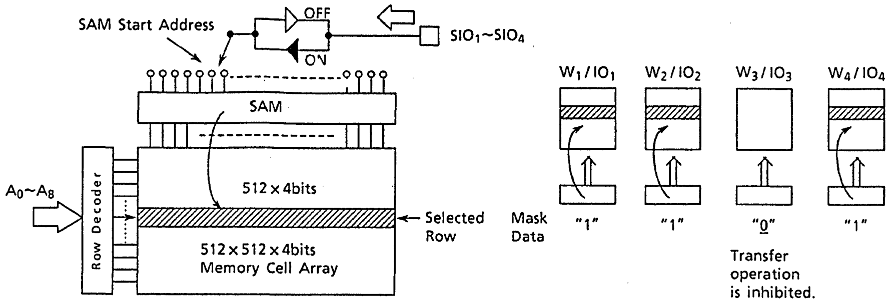


Figure 16. Block Diagram for Write Transfer Operation

When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{\text{RAS}}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{\text{RAS}}$ cycle. A rising edge of the SC Clock is only allowed after the specified delay t_{SRD} from the rising edge of $\overline{\text{RAS}}$, at which time a new row of data can be written in the serial register.

PSEUDO WRITE TRANSFER CYCLE

A pseudo write transfer cycle must be performed before loading data into the serial register after a read transfer operation has been executed. The only purpose of a pseudo write transfer is to change the SAM port mode from output mode to input mode (A data transfer from SAM to RAM does not occur). After the serial register is loaded with new data, a write transfer cycle must be performed to transfer the data from SAM to RAM. A pseudo write transfer is invoked by holding $\overline{\text{CAS}}$ "high", $\overline{\text{DT}}/\overline{\text{OE}}$ "low", $\overline{\text{WB}}/\overline{\text{WE}}$ "low", $\overline{\text{SE}}$ "high" and DSF "low" at the falling edge of $\overline{\text{RAS}}$. The timing conditions are the same as the one for the write transfer cycle except for the state of $\overline{\text{SE}}$ at the falling edge of $\overline{\text{RAS}}$.

SPLIT DATA TRANSFER AND QSF

The TC524258B features a bi-directional split data transfer capability between the RAM and the SAM. During split data transfer operation, the serial register is split into two halves which can be controlled independently. Split read or split write transfer operations can be performed to or from one half of the serial register while serial data can be shifted into or out of the other half of the serial register, as shown in Figure 17. The most significant column address location (A8C) is controlled internally to determines which half of the serial register will be reloaded from the RAM array. QSF is an output in which indicates which half of the serial register is in an active state. QSF changes state when the last SC clock is applied to active split SAM, as shown in Figure 18.

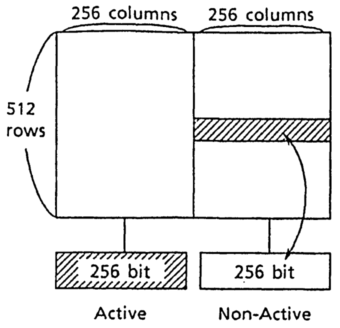


Figure 17. Split Register Mode

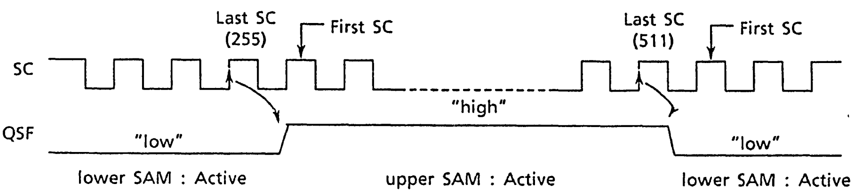


Figure 18. QSF Output State During Split Register Mode

SPLIT READ TRANSFER CYCLE

A split read transfer consists of loading 256 words by 4 bits of data from a selected row of the split RAM array into the corresponding non-active split SAM register.

Serial data can be shifted out of the other half of the split SAM register simultaneously. The block diagram and timing diagram for split read transfer mode are shown in Figure 19 and 20, respectively. During split read transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus eliminating timing restrictions as in the case of on-the-fly read transfers. A split read transfer can be performed after a delay of t_{STS}, from the change of state of the QSF output, is satisfied.

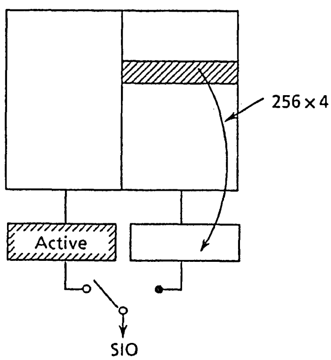


Figure 19. Block Diagram for Split Read Transfer

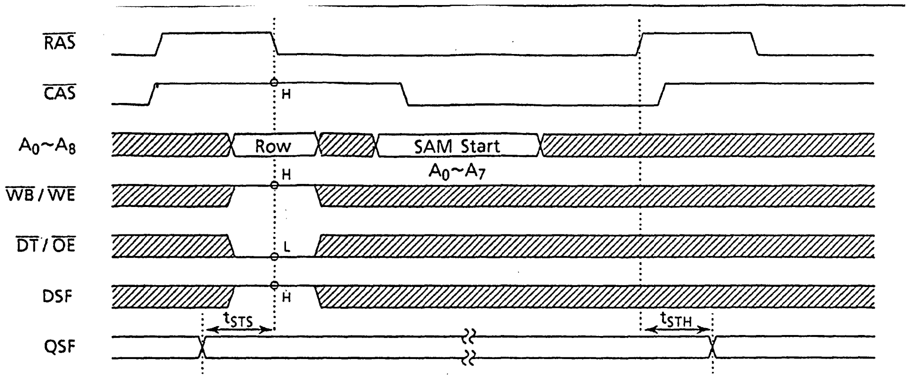


Figure 20. Timing Diagram for Split Read Transfer

A normal (Non-split) read transfer operation must precede split read transfer cycles as shown in the example in Figure 21.

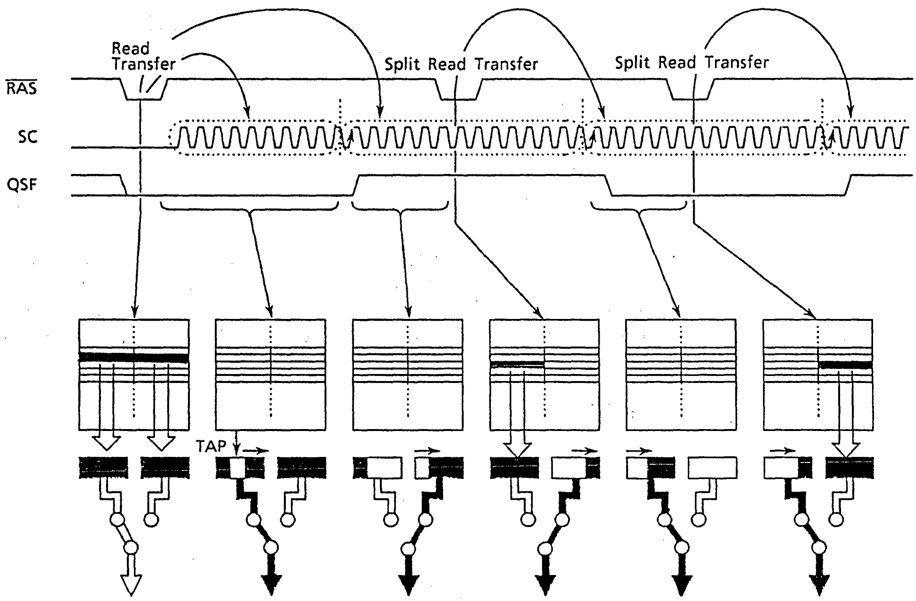


Figure 21. Example of Consecutive Read Transfer Operations

SPLIT WRITE TRANSFER CYCLE

A split write transfer consists of loading 256 words by 4 bits of data from the non-active split SAM register into a selected row of the corresponding split RAM array.

Serial data can be shifted into the other half of the split SAM register simultaneously. The block diagram and timing diagram for split write transfer mode are shown in Figure 22 and 23, respectively. During split write transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus allowing for real time transfer. A split write transfer can be performed after a delay of t_{STS}, from the change of state of the QSF output, is satisfied.

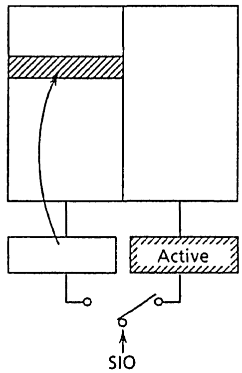


Figure 22. Block Diagram for Split Write Transfer

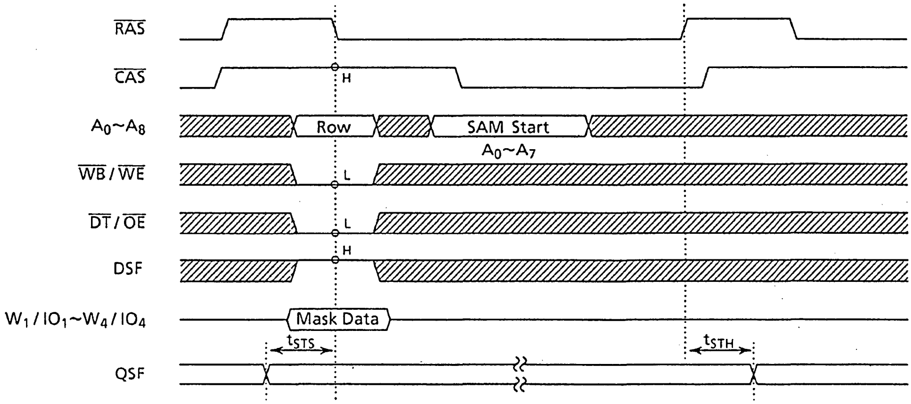


Figure 23. Timing Diagram for Split Write Transfer

A pseudo write transfer operation must precede split transfer cycles as shown in the example in Figure 24. The purpose of the pseudo write transfer operation is to switch the SAM port from output mode to input mode and to set the initial tap location prior to split write transfer operations.

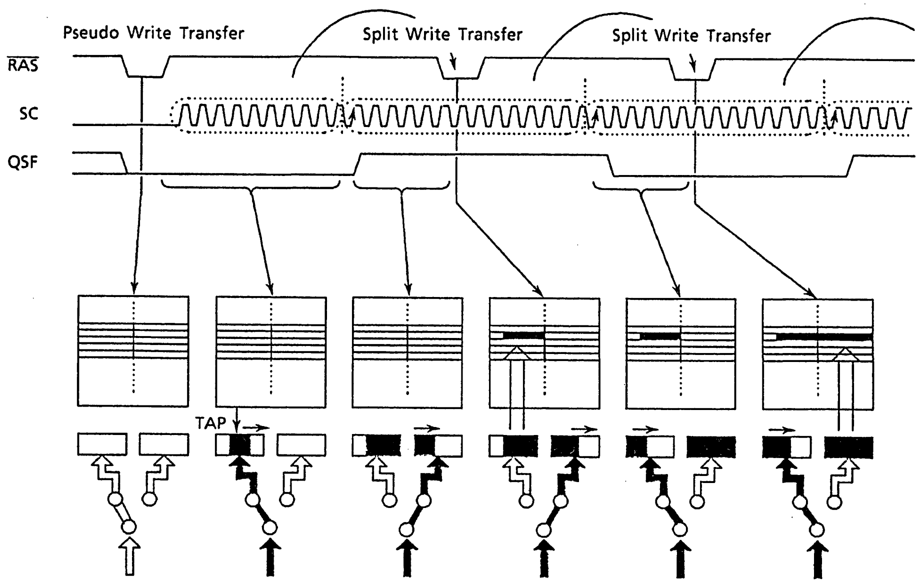


Figure 24. Example of Consecutive Write Transfer Operations

SPLIT-REGISTER OPERATION SEQUENCE (EXAMPLE)

Split read / write transfers must be preceded by a normal (Non-split) transfer such as a read, write or pseudo write transfer. Figure 25 illustrates an example of split register operation sequence after device power-up and initialization. After power-up, a minimum of 8 $\overline{RAS}$ and 8 SC clock cycles must be performed to properly initialize the device. A read transfer is then performed and the column address latched at the falling edge of $\overline{CAS}$ sets the SAM tap pointer location which up to that point was in an undefined location. Subsequently, the pointer address is incremented by cycling the serial clock SC from the starting location to the last location in the register (address 511) and wraps around to the tap location set by the split read transfer performed for the lower SAM while the upper SAM is being accessed. The SAM address is incremented as long as SC is clocked. The following split read transfer sets a new tap location in the upper split SAM register address 256 in this example and the pointer is incremented from this location by cycling the SC clock.

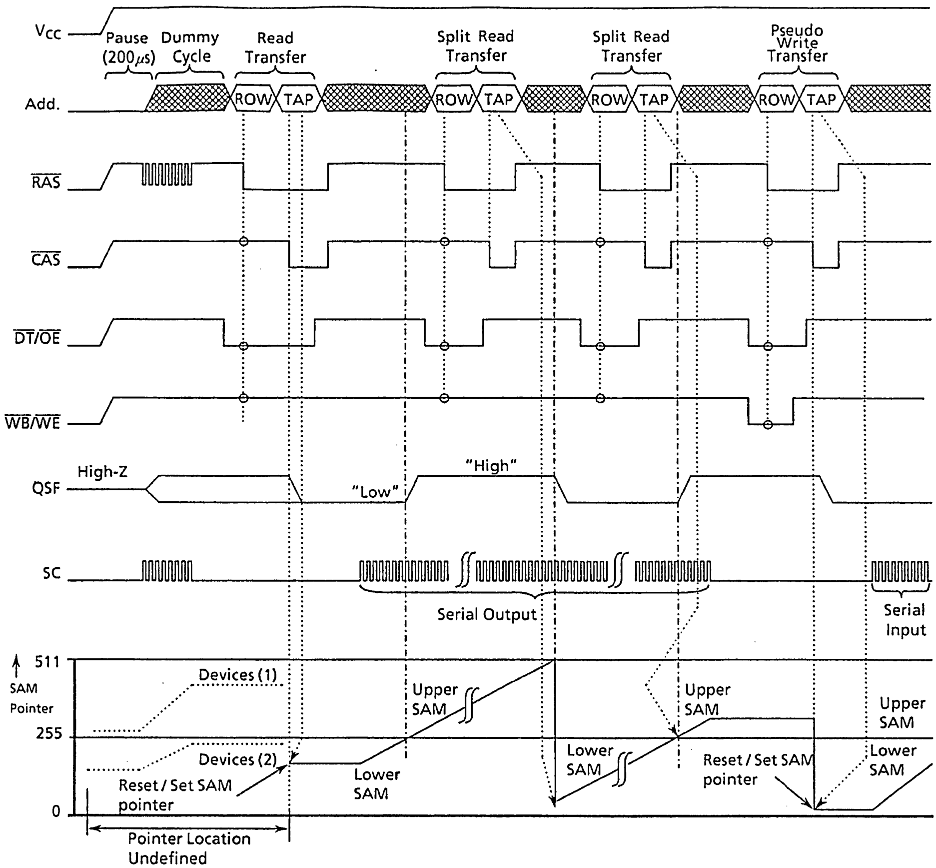
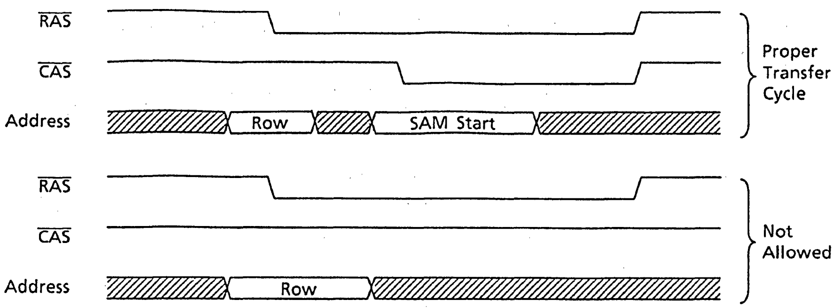


Figure 25. Example of Split SAM Register Operation Sequence

The next operation is a pseudo write transfer which switches the SAM port from output mode to input mode in preparation for either write transfers or split write transfers. The column address latched at the falling edge of $\overline{CAS}$ during the pseudo write transfer sets the serial register tap location. Serial data will be written into the SAM starting from this location.

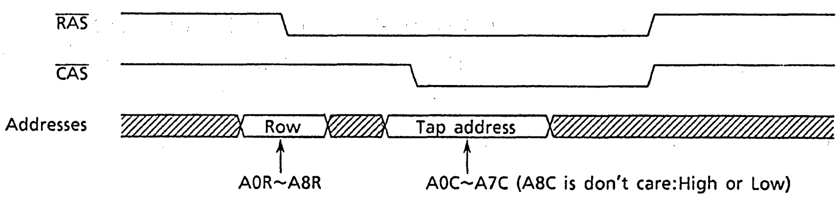
TRANSFER OPERATION WITHOUT $\overline{CAS}$

During all transfer cycles, the $\overline{CAS}$ input clock must be cycled, so that the column address are latched at the falling edge of $\overline{CAS}$, to set the SAM tap location. If $\overline{CAS}$ was maintained at a constant "high" level during a transfer cycle, the SAM pointer location would be undefined. Therefore a transfer cycle with $\overline{CAS}$ held "high" is not allowed (Refer to the illustration below).



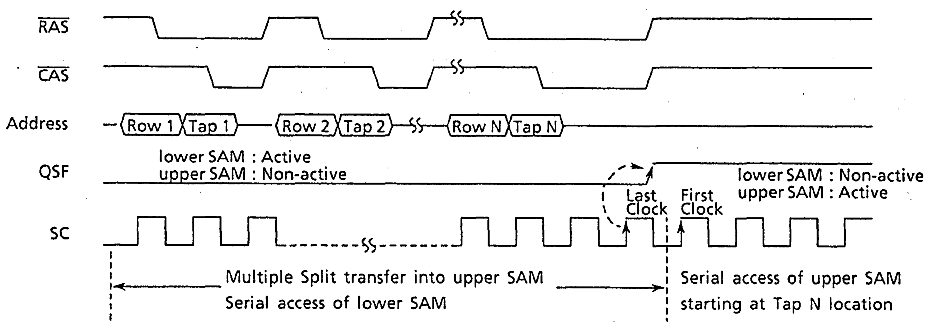
TAP LOCATION SELECTION IN SPLIT TRANSFER OPERATION

(a) In a split transfer operation, column addresses AOC through A7C must be latched at the falling edge of $\overline{CAS}$ in order to set the tap location in one of the split SAM registers. During a split transfer, column address A8C is controlled internally and therefore it is ignored internally at the falling edge of $\overline{CAS}$.



During a split transfer, it is not allowed to set the last address location (A0C~A7C=FF), in either the lower SAM or the upper SAM, as the tap location.

(b) In the case of multiple split transfers performed into the same split SAM register, the tap location specified during the last split transfer, before QSF toggles, will prevail. In the example shown below, multiple split transfers are performed into the upper SAM (Non-active) while the lower SAM (active) is being accessed at the time when QSF toggles, the first SC serial clock will start shifting serial data starting from the Tap N address location.



SPLIT READ / WRITE TRANSFER OPERATION ALLOWABLE PERIOD

Figure 26 illustrates the relationship between the serial clock SC and the special function output QSF during split read / write transfers and highlights the time periods where split transfers are allowed, relative to SC and QSF.

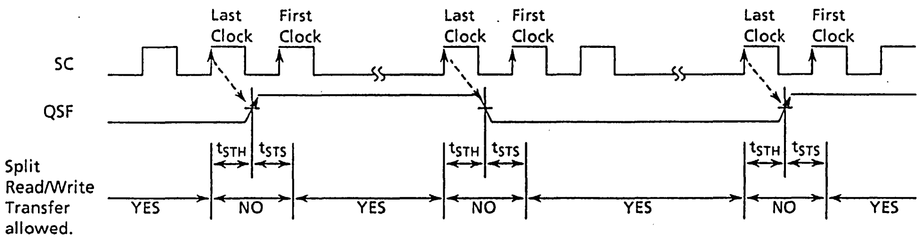
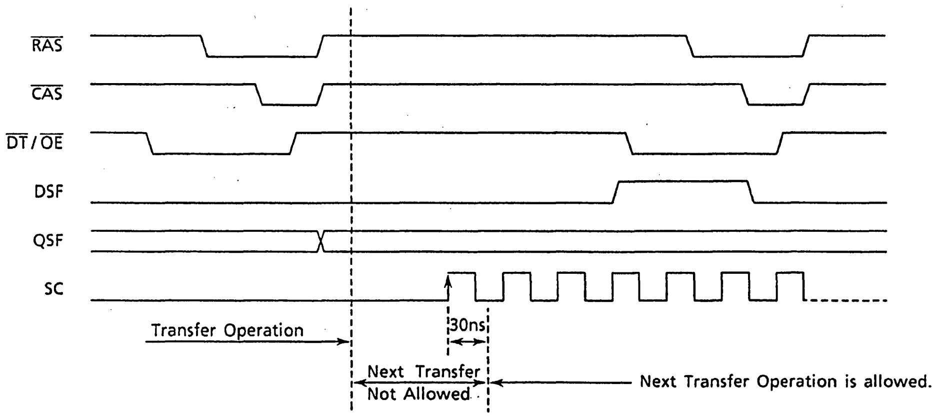


Figure 26. Split Transfer Operation Allowable Periods

As indicated in Figure 26, a split read / write transfer is not allowed during the period of $t_{STH} + t_{STS}$.

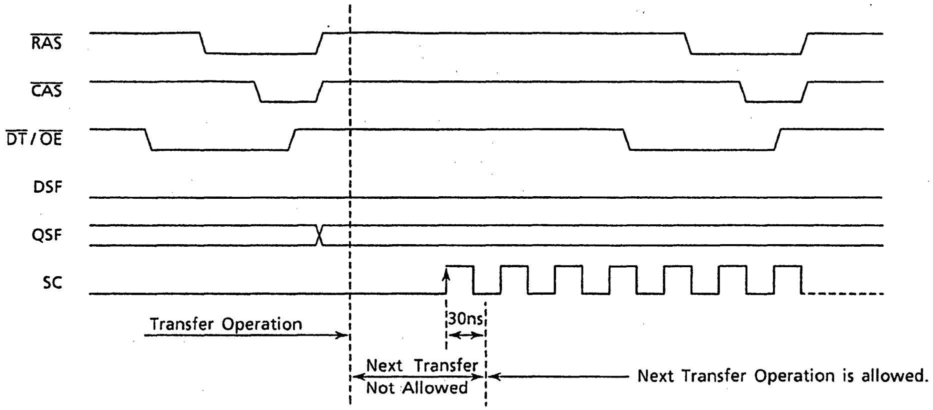
SPLIT TRANSFER CYCLE AFTER NORMAL TRANSFER CYCLE

A split transfer may be performed following a normal transfer (Read / Write / Pseudo-write transfer) provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (Refer to the illustration shown below).



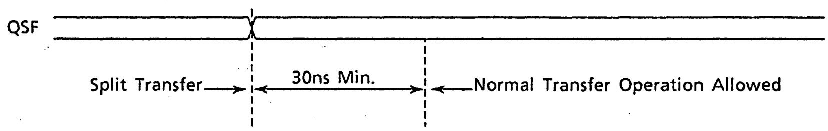
NORMAL READ TRANSFER CYCLE AFTER NORMAL READ TRANSFER CYCLE

Another read transfer may be performed following the read transfer provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (Refer to the illustration shown below).



NORMAL TRANSFER AFTER SPLIT TRANSFER

A normal transfer (read / write / pseudo write) may be performed following split transfer operation provided that a 30ns minimun delay is satisfied after the QSF signal toggles.



POWER-UP

Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them "high" before or at the same time as the V_{CC} supply is turned on. After power-up, a pause of 200, µseconds minimum is required with $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ held "high". After the pause, a minimum of 8 $\overline{RAS}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT}/\overline{OE}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.

INITIAL STATE AFTER POWER-UP

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and $\overline{WB}/\overline{WE}$ held "high", the internal state of the TC524258B is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 µseconds pause followed by a minimum of 8 $\overline{RAS}$ cycles and 8 SC cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
QSF	High-Impedance
Color Register	all "0"
WM1 Register	Write Enable
TAP pointer	Invalid

SILICON GATE CMOS
262, 144WORDS X 4BITS MULTIPORT DRAM

target spec

DESCRIPTION

The TC524259B is a CMOS multiport memory equipped with a 262,144-words by 4-bits dynamic random access memory (RAM) port and a 512-words by 4-bits static serial access memory (SAM) port. The TC524259B supports three types of operations; Random access to and from the RAM port, high speed serial access to and from the SAM port and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally. In addition to the conventional multiport video RAM operating modes, the TC524259B features the block write functions on the RAM port and a split register data transfer capability on the SAM port. The TC524259B is fabricated using Toshiba's CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

FEATURES

- Single power supply of 5V± 10% with a built in V_{BB} generator
- All inputs and outputs : TTL Compatible
- Organization
  RAM Port : 262,144wordsX4bits
  SAM Port : 512wordsX4bits
- RAM Port
  Fast Page Mode Read - Modify - Write $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh $\overline{RAS}$ only Refresh, Write per Bit 1&2 Block Write , Block Write (Mask 1&2) 512 refresh cycles / 8ms
- SAM Port
  High Speed Serial Read / Write Capability
  512 Tap Locations
  Fully Static Register
- RAM- SAM Bidirectional Transfer
  Read / Write / Pseudo Write Transfer
  Real Time Read Transfer
  Split Read Transfer
- Package
  TC524259BJ : SOJ28 - P-400
  TC524259BZ : ZIP28 - P-400

KEY PARAMETERS

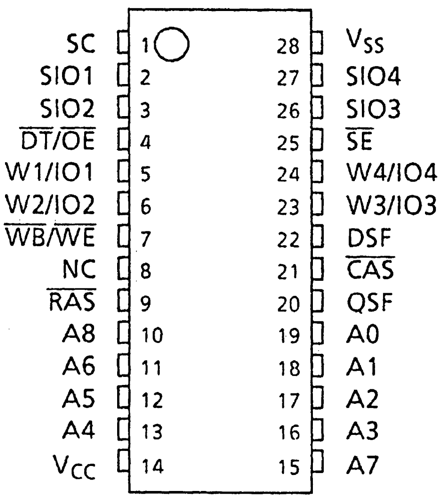
ITEM		TC524259B	
		—80	—10
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	80ns	100ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	25ns	25ns
t_{AA}	Column Address Access Time (Max.)	45ns	50ns
t_{RC}	Cycle Time (Min.)	150ns	180ns
t_{PC}	Page Mode Cycle Time (Min.)	50ns	55ns
t_{SCA}	Serial Access Time (Max.)	25ns	25ns
t_{SCC}	Serial Cycle time (Min.)	30ns	30ns
I_{CC1}	RAM Operating Current (SAM : Standby)	85mA	70mA
I_{CC2A}	SAM Operating Current (RAM : Standby)	50mA	50mA
I_{CC2}	Standby Current	10mA	10mA

PIN NAME

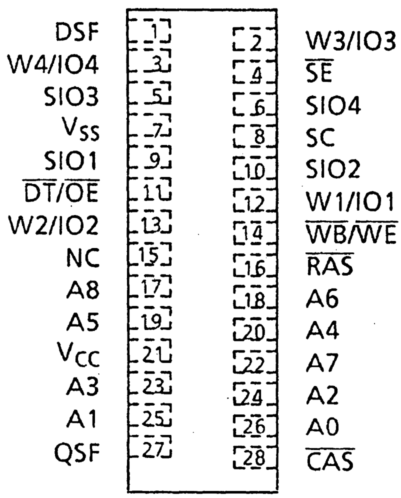
A0~A8	Address inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
DT/OE	Data Transfer/Output Enable
WB/WE	Write per Bit/Write Enable
DSF	Special Function Control
WI/IOI ~W4/IO4	Write Mask/Data IN, OUT
SC	Serial Clock
SE	Serial Enable
SIOI~SIO4	Serial Input/Output
QSF	Special Flag Output
V_{CC}/V_{SS}	Power(5V)/Ground
N.C.	No Connection

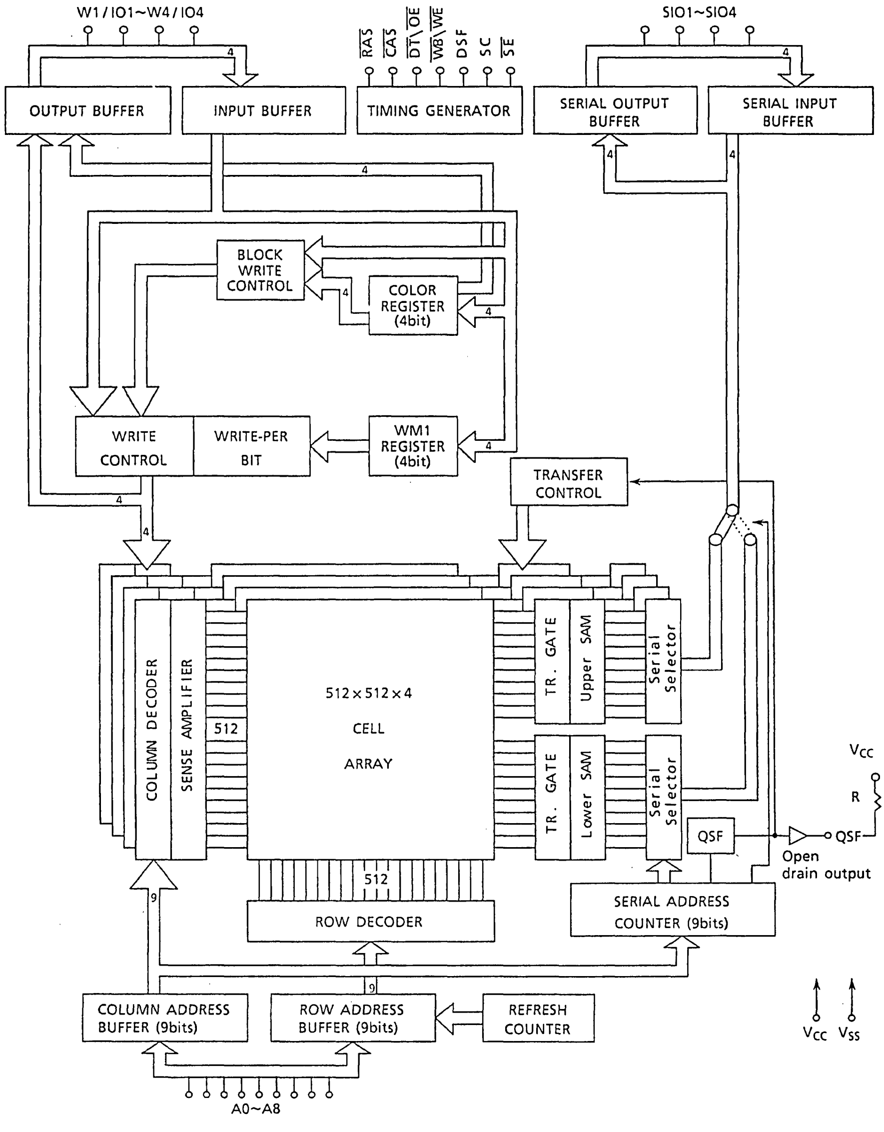
PIN CONNECTION (TOP VIEW)

TC524259BJ



TC524259BZ




W1/IO1~W4/IO4
RAS
CAS
DT\OE
WB\WE
DSF
SC
SE
SIO1~SIO4
OUTPUT BUFFER
INPUT BUFFER
TIMING GENERATOR
SERIAL OUTPUT BUFFER
SERIAL INPUT BUFFER
BLOCK WRITE CONTROL
COLOR REGISTER (4bit)
WRITE CONTROL
WRITE-PER BIT
WM1 REGISTER (4bit)
TRANSFER CONTROL
COLUMN DECODER
SENSE AMPLIFIER
512
512×512×4
CELL
ARRAY
TR. GATE
Upper SAM
Serial Selector
TR. GATE
Lower SAM
Serial Selector
QSF
Vcc
R
QSF
Open drain output
ROW DECODER
SERIAL ADDRESS COUNTER (9bits)
COLUMN ADDRESS BUFFER (9bits)
ROW ADDRESS BUFFER (9bits)
REFRESH COUNTER
Vcc
Vss
A0~A8

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}, V_{OUT}	Input Output Voltage	— 1.0~7.0	V	1
V_{CC}	Power Supply Voltage	— 1.0~7.0	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	— 55~150	°C	1
T_{SOLDER}	Soldering Temperature • Time	260•10	°C•sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	6.5	V	2
V_{IL}	Input Low Voltage	- 1.0	—	0.8	V	2

+: -1V 20ns Pulse width

CAPACITANCE (V_{CC} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_1	Input Capacitance	—	7	pF
C_{IO}	Input/Output Capacitance	—	9	
C_O	Output Capacitance (QSF)	—	9	

Note: This parameter is periodically sampled and is not 100% tested.

D.C. ELECTRICAL CHARACTERISTICS (VCC = 5V ± 10%, Ta = 0~70°C)

ITEM (RAM PORT)	SAM PORT	SYMBOL	-80		UNIT	NOTE
			MIN.	MAX.		
OPERATING CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling; $t_{RC} = t_{RC}$ min.)	Standby	I_{CC1}	—	85	mA	3, 4
	Active	I_{CC1A}	—	125		3, 4
STANDBY CURRENT $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	Standby	I_{CC2}	—	10		
	Active	I_{CC2A}	—	50		3, 4
RAS ONLY REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}; $t_{RC} = t_{RC}$ min.)	Standby	I_{CC3}	—	85		3, 4
	Active	I_{CC3A}	—	125		3, 4
PAGE MODE CURRENT ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling; $t_{PC} = t_{RC}$ min.)	Standby	I_{CC4}	—	75		3, 4
	Active	I_{CC4A}	—	115		3, 4
CAS BEFORE RAS REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$; $t_{RC} = t_{RC}$ min.)	Standby	I_{CC5}	—	85		3, 4
	Active	I_{CC5A}	—	125		3, 4
DATA TRANSFER CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling; $t_{RC} = t_{RC}$ min.)	Standby	I_{CC6}	—	105		3, 4
	Active	I_{CC6A}	—	145		3, 4
BLOCK WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling; $t_{RC} = t_{RC}$ min.)	Standby	I_{CC8}	—	95		3, 4
	Active	I_{CC8A}	—	135		3, 4

ITEM	SYMBOL	MIN.	MAX	UNIT	NOTE
INPUT LEAKAGE CURRENT 0V ≤ V_{IN} ≤ 6.5V, All other pins not under test = 0V	$I_{I(L)}$	—10	10	μA	
OUTPUT LEAKAGE CURRENT 0V ≤ V_{OUT} ≤ 5.5V, OutputDisable	$I_{O(L)}$	—10	10	μA	
OUTPUT "H" LEVEL VOLTAGE I_{OUT} = - 2mA	V_{OH}	2.4	—	V	
OUTPUT "L" LEVEL VOLTAGE I_{OUT} = 2mA	V_{OL}	—	0.4	V	
OUTPUT "L" LEVEL VOLTAGE I_{OUT} = 6mA	$V_{OL\ (QSF)}$	—	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V±10%, Ta = 0~70°C)(Notes: 5, 6, 7)

SYMBOL	PARAMETER	-80		UNIT	NOTE
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150			
t_{RMW}	Read-Modify-Write Cycle Time	195			
t_{PC}	Fast Page Mode Cycle Time	50			
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	90			
t_{RAC}	Access Time from $\overline{\text{RAS}}$		80		8,14
t_{AA}	Access Time from Column Address		45		8,14
t_{CAC}	Access Time from $\overline{\text{CAS}}$		25		8,15
t_{CPA}	Access Time from $\overline{\text{CAS}}$ Precharge		45		8,15
t_{OFF}	Output Buffer Turn-Off Delay	0	20		10
t_{T}	Transition Time (Rise and Fall)	3	35		7
t_{RP}	$\overline{\text{RAS}}$ Precharge Time	60			
t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	80	10000		
t_{RASP}	$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode Only)	80	100000		
t_{RSH}	$\overline{\text{RAS}}$ Hold Time	25			
t_{CSH}	$\overline{\text{CAS}}$ Hold Time	80			
t_{CAS}	$\overline{\text{CAS}}$ Pulse Width	25	10000		
t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	20	55		14
t_{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	15	35	ns	14
t_{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	45			
t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	10			
t_{CPN}	$\overline{\text{CAS}}$ Precharge Time	10			
t_{CP}	$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	10			
t_{ASR}	Row Address Set-Up Time	0			
t_{RAH}	Row Address Hold Time	10			
t_{ASC}	Column Address Set-Up Time	0			
t_{CAH}	Column Address Hold Time	15			
t_{AR}	Column Address Hold Time referenced to $\overline{\text{RAS}}$	55			
t_{RCS}	Read Command Set-Up Time	0			
t_{RCH}	Read Command Hold Time	0			11
t_{RRH}	Read Command Hold Time referenced to $\overline{\text{RAS}}$	0			11
t_{WCH}	Write Command Hold Time	15			
t_{WCR}	Write Command Hold Time referenced to $\overline{\text{RAS}}$	55			
t_{WP}	Write Command Pulse Width	15			
t_{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	20			
t_{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	20			

SYMBOL	PARAMETER	-80 MIN.	-80 MAX	UNIT	NOTE
t_{DS}	Data Set-Up Time	0		ns	12
t_{DH}	Data Hold Time	15			12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55			
t_{WCS}	Write Command Set-Up Time	0			13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100			13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65			13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45			13
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0			
t_{DZO}	Data to $\overline{OE}$ Delay Time	0			
t_{OEA}	Access Time from $\overline{OE}$		20		8
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	0	10		10
t_{OED}	$\overline{OE}$ to Data Delay Time	10			
t_{OEH}	$\overline{OE}$ Command Hold Time	10			
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15			
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10			
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10			
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0			
t_{REF}	Refresh Period		8	ms	
t_{WSR}	$\overline{WB}$ Set-Up Time	0		ns	
t_{RWH}	$\overline{WB}$ Hold Time	15			
t_{FSR}	DSF Set-Up Time referenced to $\overline{RAS}$	0			
t_{RFH}	DSF Hold Time referenced to $\overline{RAS}$(1)	15			
t_{FHR}	DSF Hold Time referenced to $\overline{RAS}$(2)	55			
t_{FSC}	DSF Set-Up Time referenced to $\overline{CAS}$	0			
t_{CFH}	DSF Hold Time referenced to $\overline{CAS}$	15			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0			
t_{MH}	Write-Per-Bit Mask Data Hold Time	15			
t_{THS}	$\overline{DT}$ High Set-Up Time	0			
t_{THH}	$\overline{DT}$ High Hold Time	15			
t_{TLS}	$\overline{DT}$ Low Set-Up Time	0			
t_{TLH}	$\overline{DT}$ Low Hold Time	15	10000		
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	65	10000		
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	30			
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	25			

SYMBOL	PARAMETER	-80 MIN.	-80 MAX	UNIT	NOTE
t_{ESR}	$\overline{SE}$ Set-Up Time referenced to $\overline{RAS}$	0			
t_{REH}	$\overline{SE}$ Hold Time referenced to $\overline{RAS}$	15			
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	60			
t_{TP}	$\overline{DT}$ Precharge Time	20			
t_{RSD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	80			
t_{ASP}	Column Address to First SC Delay Time (Read Transfer)	45			
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	25			
t_{TSL}	Last SC to DT Lead Time (Real Time Read Transfer)	5			
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	15		ns	
t_{SRS}	Last SC to $\overline{RAS}$ Set-Up Time (Serial Input)	30			
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	25			
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	50			
t_{SDZ}	Serial Output Buffer Turn-off Delay from $\overline{RAS}$ (Pseudo Write Transfer)	10	50		10
t_{SCC}	SC Cycle Time	30			
t_{SC}	SC Pulse Width (SC High Time)	10			
t_{SCP}	SC Precharge Time (SC Low Time)	10			
t_{SCA}	Access Time from SC		25		9
t_{SOH}	Serial Output Hold Time from SC	5		ms	
t_{SDS}	Serial Input Set-Up Time	0			
t_{SDH}	Serial Input Hold Time	15			
t_{SEA}	Access Time from $\overline{SE}$		25		9
t_{SE}	$\overline{SE}$ Pulse Width	25			
t_{SEP}	$\overline{SE}$ Precharge Time	25			
t_{SEZ}	Serial Output Buffer Turn-off Delay from $\overline{SE}$	0	20		10
t_{SZE}	Serial Input to $\overline{SC}$ Delay Time	0			
t_{SZS}	Serial Input to First SC Delay Time	0		ns	
t_{SWS}	Serial Write Enable Set-Up Time	0			
t_{SWH}	Serial Write Enable Hold Time	15			
t_{SWIS}	Serial Write Disable Set-Up Time	0			
t_{SWIH}	Serial Write Disable Hold Time	15			
t_{STS}	Split Transfer Set-Up Time	30			
t_{STH}	Split Transfer Hold Time	30			
t_{SQD}	SC-QSF Delay Time		60		16

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltage are referenced to V_{SS}.

3. These parameters depend on cycle rate.

4. These parameters depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}/\overline{OE}$ "high") and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T = 5ns.

7. $V_{IH\,(min.)}$ and $V_{IL\,(max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. RAM port outputs are measured with a load equivalent to 1 TTL load and 100pF.
   D_{OUT} reference levels : V_{OH} / V_{OL} = 2.0V / 0.8V.

9. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
   D_{OUT} reference levels : V_{OH} / V_{OL} = 2.0V / 0.8V.

10. $t_{OFF\,(max.)}$, $t_{OEZ\,(max.)}$, $t_{SDZ\,(max.)}$ and $t_{SEZ\,(max.)}$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must he satisfied for a read cycles.

12. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}$ / $\overline{WE}$ leading edge in $\overline{OE}$-controlled-write cycles and read-modify-write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS\,(min.)}$, the cycle is an early write cycles and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geq t_{RWD\,(min.)}$, $t_{CWD} \geq t_{CWD\,(min.)}$ and $t_{AWD} \geq t_{AWD\,(min.)}$ the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

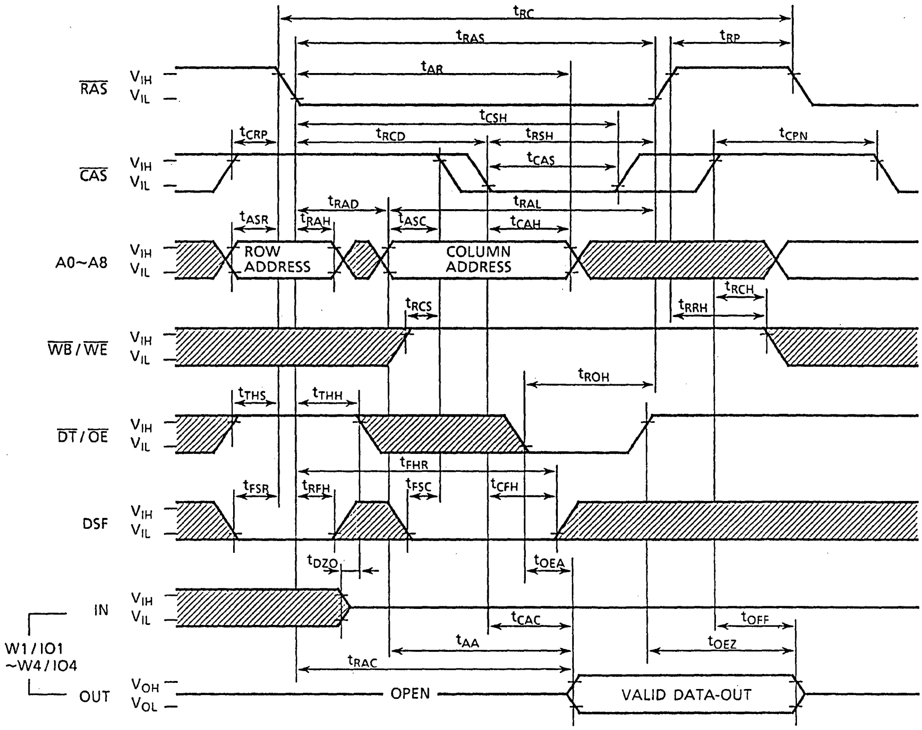
14. Operation within the $t_{RCD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can he met.
    $t_{RCD\,(max.)}$ is specified as a reference point only : If t_{RCD} is greater than the specified
    $t_{RCD\,(max.)}$ limit, then access time is controlled by t_{CAC}.

15. Operation within the $t_{RAD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can be met. $t_{RAD\,(max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\,(max.)}$ limit, then access time is controlled by t_{AA}.

16. This parameter measurement assumes Pull up resister = 820Ω.

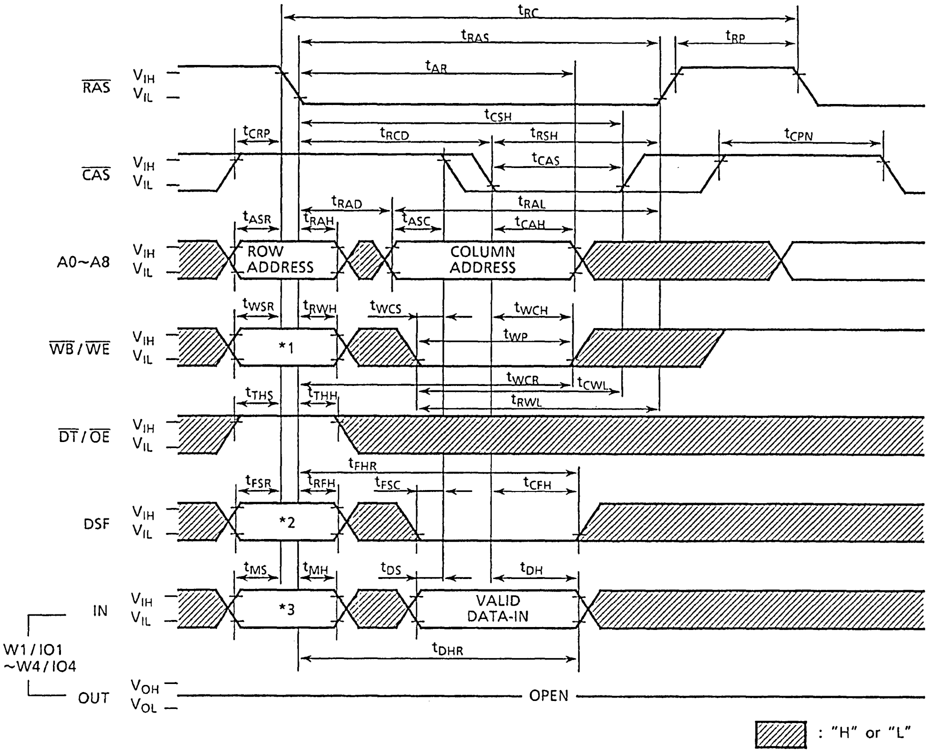
TIMING WAVEFORM

READ CYCLE



: "H" or "L"

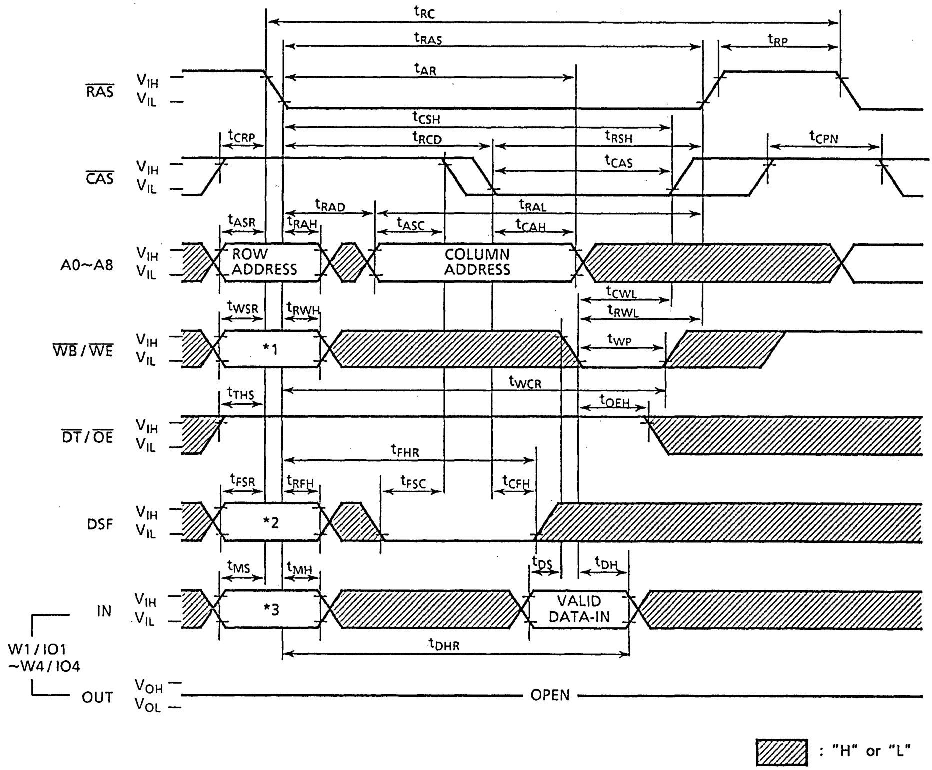
WRITE CYCLE (EARLY WRITE)



*1 $\overline{\text{WB}}/\overline{\text{WE}}$	*2 DSF	*3 W1/IO1~W4/104	Cycle
0	0	WM1 data	Write per bit 1 (New Mask Mode)
	1	Don't Care	Write per bit 2 (Old Mask Mode)
1	0	Don't Care	Normal Write (No Mask Mode)

WM1 data 0: Write Disable
1: Write Enable

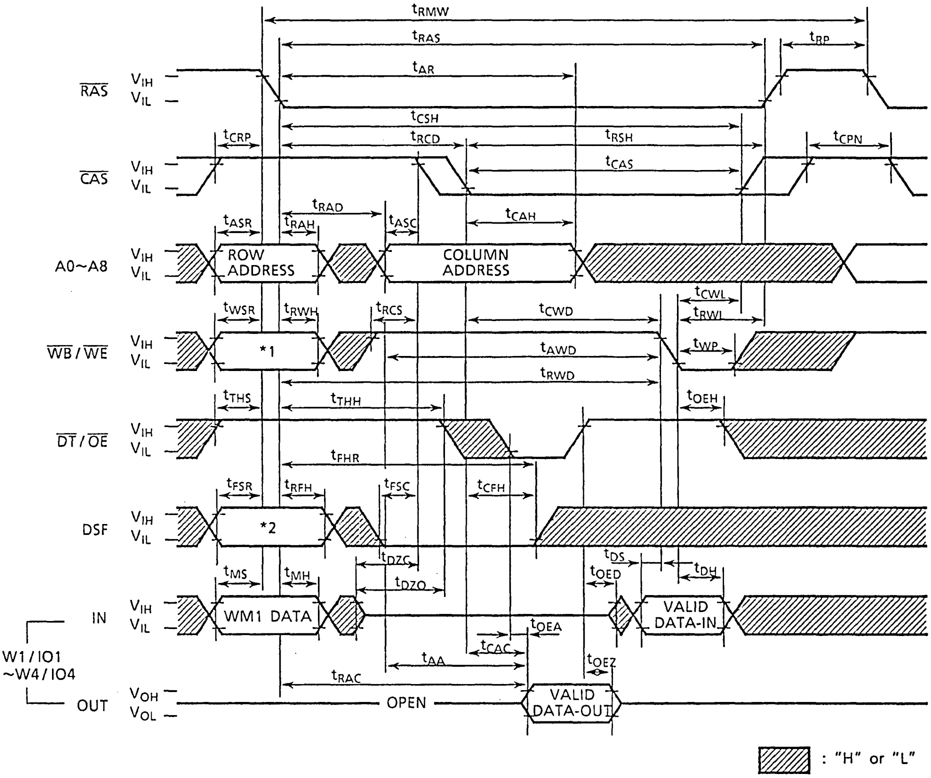
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



*1 $\overline{WB}$/$\overline{WE}$	*2 DSF	*3 W1/IO1~W4/104	Cycle
0	0	WM1 data	Write per bit 1 (New Mask Mode)
	1	Don't Care	Write per bit 2 (Old Mask Mode)
1	0	Don't Care	Normal Write (No Mask Mode)

WM1 data 0: Write Disable
1: Write Enable

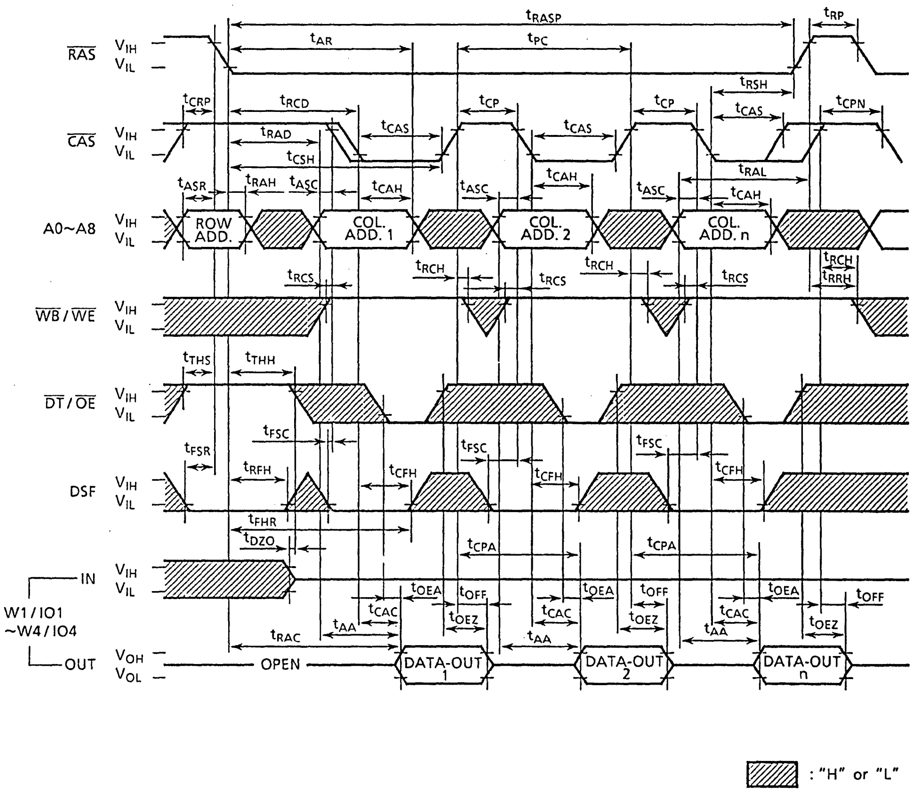
READ-MODIFY-WRITE CYCLE



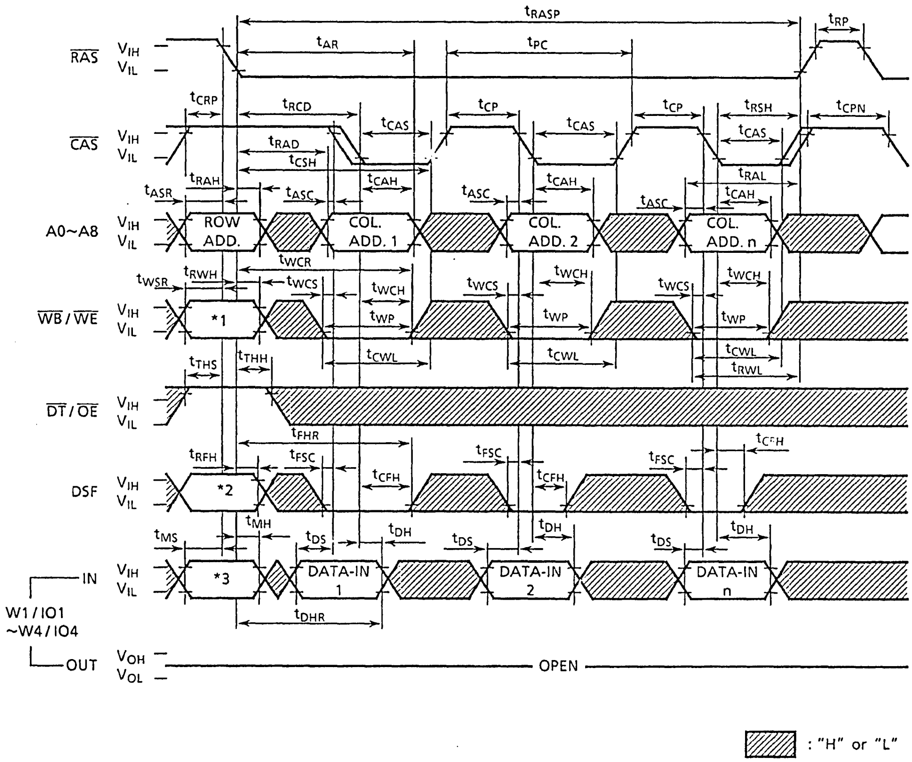
*1 $\overline{WB}/\overline{WE}$	*2 DSF	*3 W1/IO1~W4/104	Cycle
0	0	WM1 data	Write per bit 1 (New Mask Mode)
	1	Don't Care	Write per bit 2 (Old Mask Mode)
1	0	Don't Care	Normal Write (No Mask Mode)

WM1 data 0: Write Disable
1: Write Enable

FAST PAGE MODE READ CYCLE



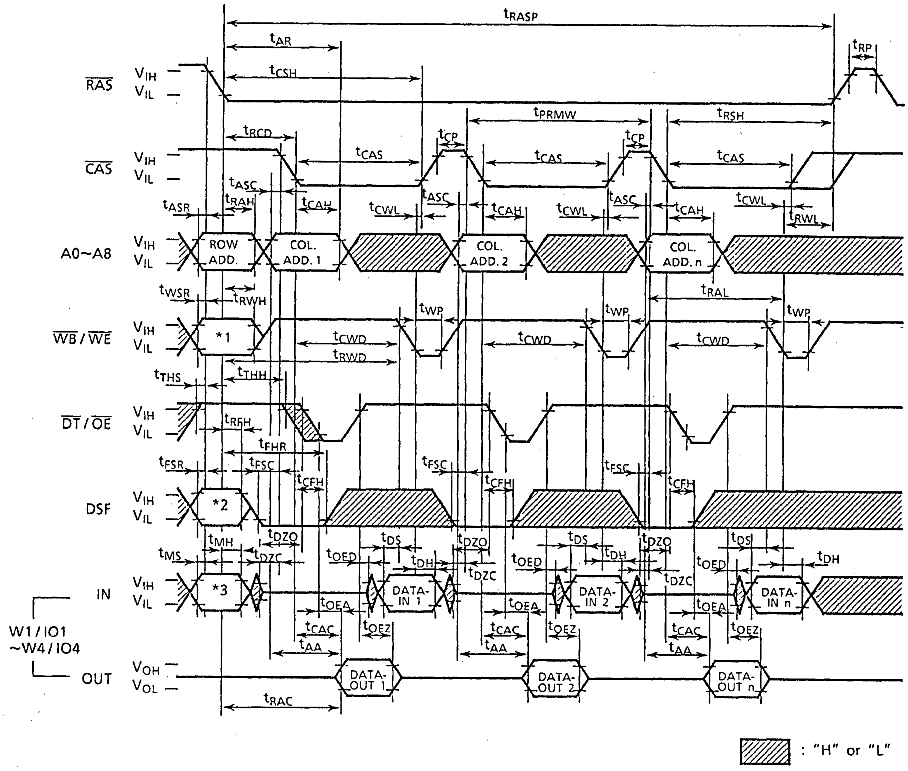
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



*1 $\overline{WB}/\overline{WE}$	*2 DSF	*3 W1/IO1~W4/104	Cycle
0	0	WM1 data	Write per bit 1 (New Mask Mode)
	1	Don't Care	Write per bit 2 (Old Mask Mode)
1	0	Don't Care	Normal Write (No Mask Mode)

WM1 data 0: Write Disable
1: Write Enable

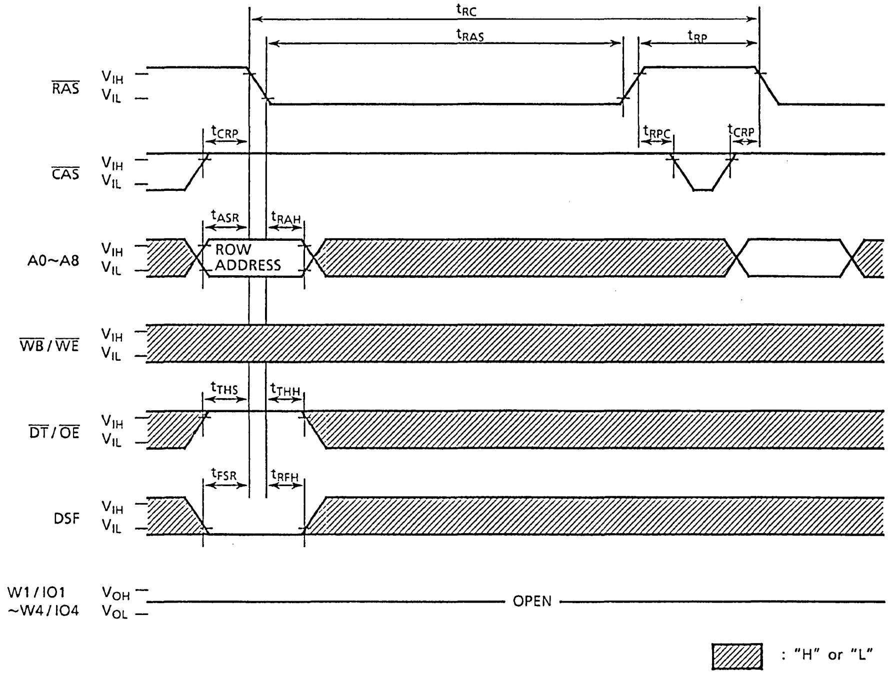
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



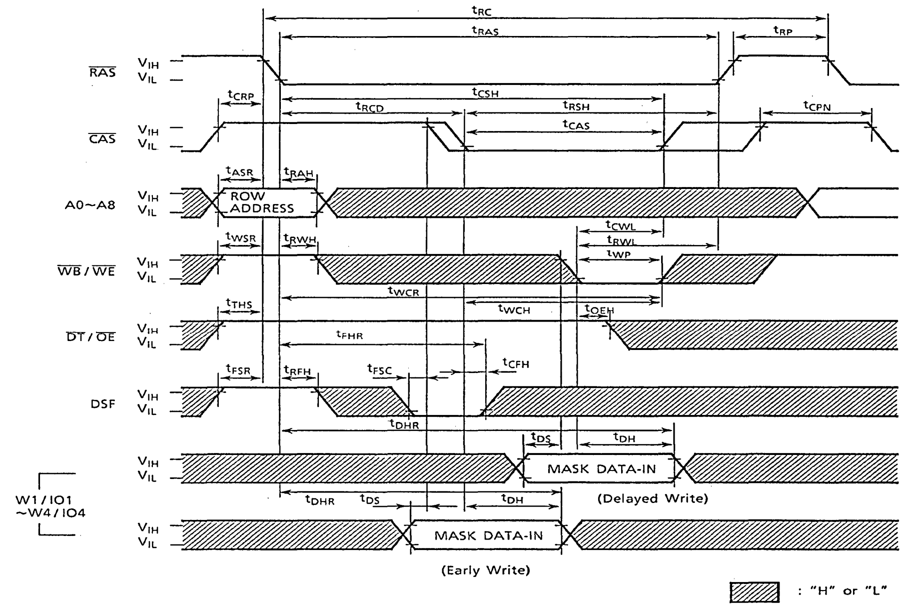
*1 $\overline{WB}/\overline{WE}$	*2 DSF	*3 W1/IO1~W4/104	Cycle
0	0	WM1 data	Write per bit 1 (New Mask Mode)
	1	Don't Care	Write per bit 2 (Old Mask Mode)
1	0	Don't Care	Normal Write (No Mask Mode)

WM1 data 0: Write Disable
1: Write Enable

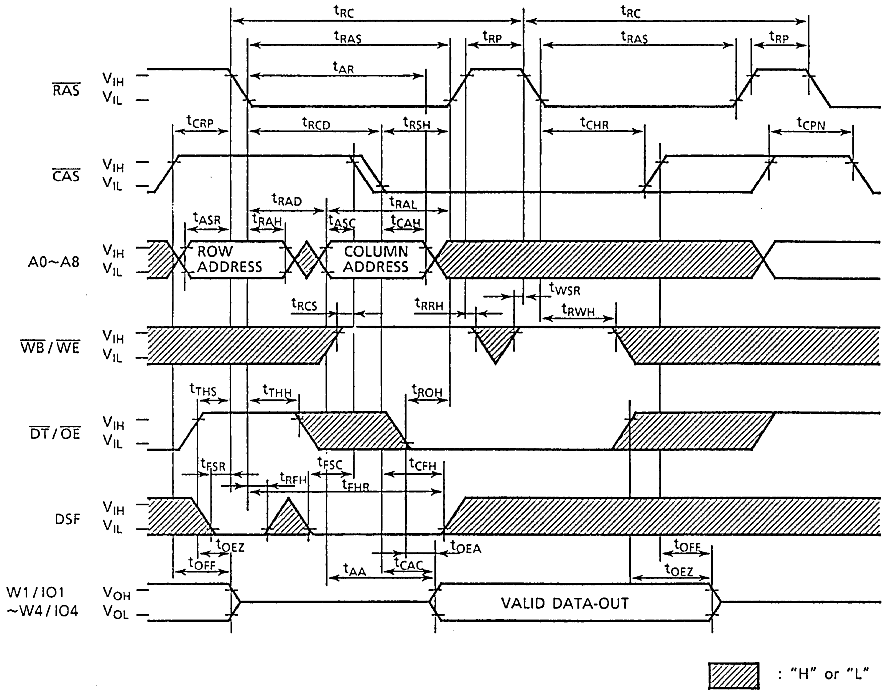
$\overline{RAS}$ ONLY REFRESH CYCLE



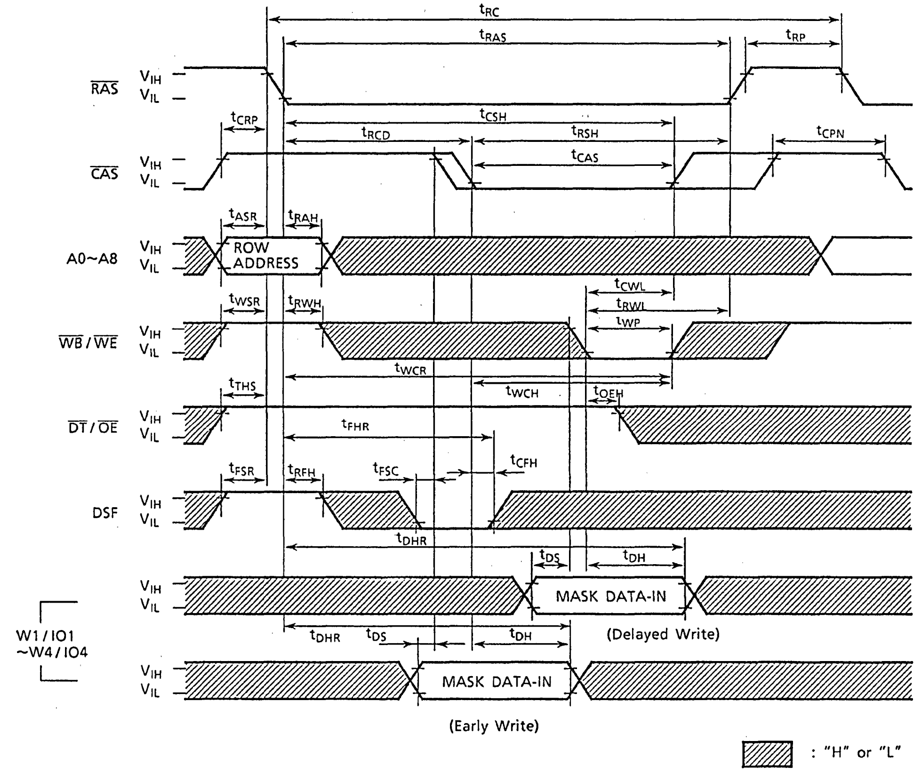
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



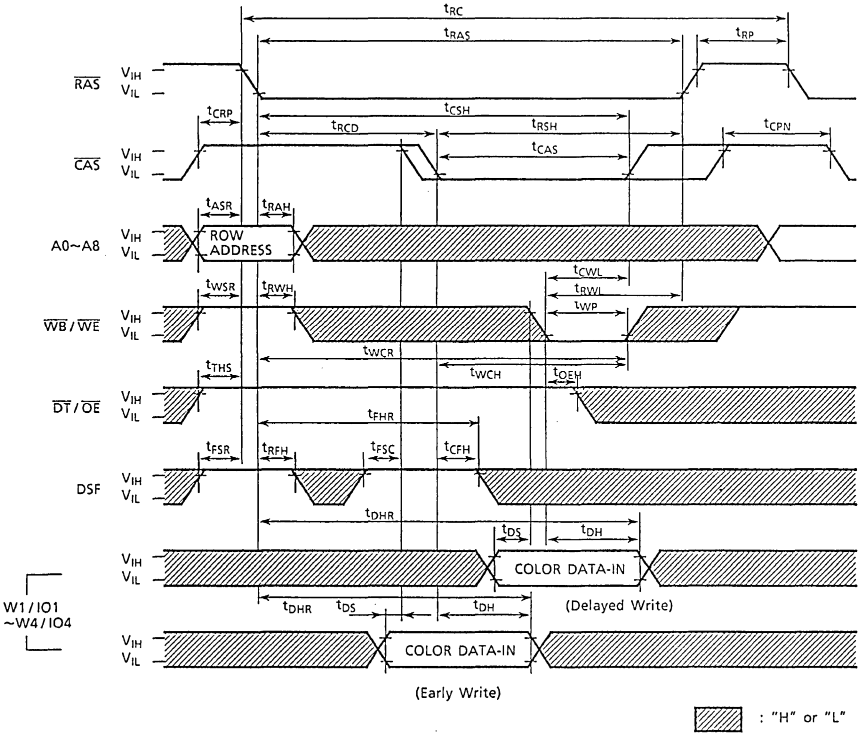
HIDDEN REFRESH CYCLE



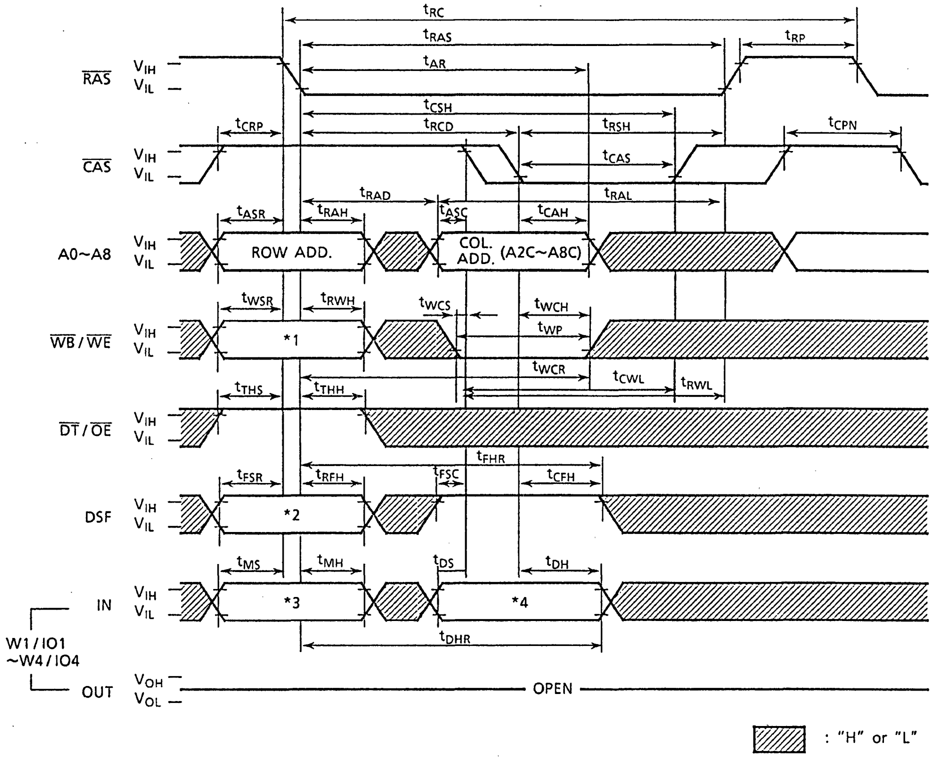
LOAD MASK REGISTER CYCLE



LOAD COLOR REGISTER CYCLE



BLOCK WRITE CYCLE



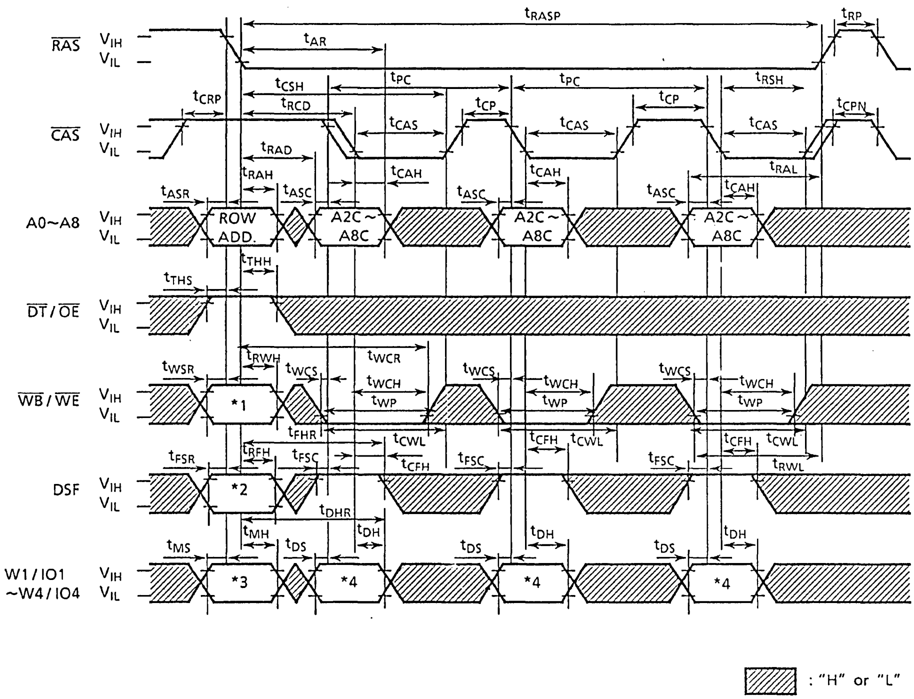
*1 $\overline{WB}/\overline{WE}$	*2 DSF	*3 W1/IO1~W4/104	Cycle
0	0	WM1 data	Block Write (Mask 1) (New Mask Mode)
	1	Don't Care	Block Write (Mask 2) (Old Mask Mode)
1	0	Don't Care	Block Write (No Mask Mode)

WM1 data 0: Write Disable
1: Write Enable

*4) COLUMN SELECT
W1/I01 – Column 0 (A1C=0, AOC=0
W2/I02 – Column 1 (A1C=0, AOC=1
W3/I03 – Column 2 (A1C=1, AOC=0
W4/I04 – Column 3 (A1C=1, AOC=1

Wn/IOn
=0 : Disable
=1 : Enable

PAGE MODE BLOCK WRITE CYCLE



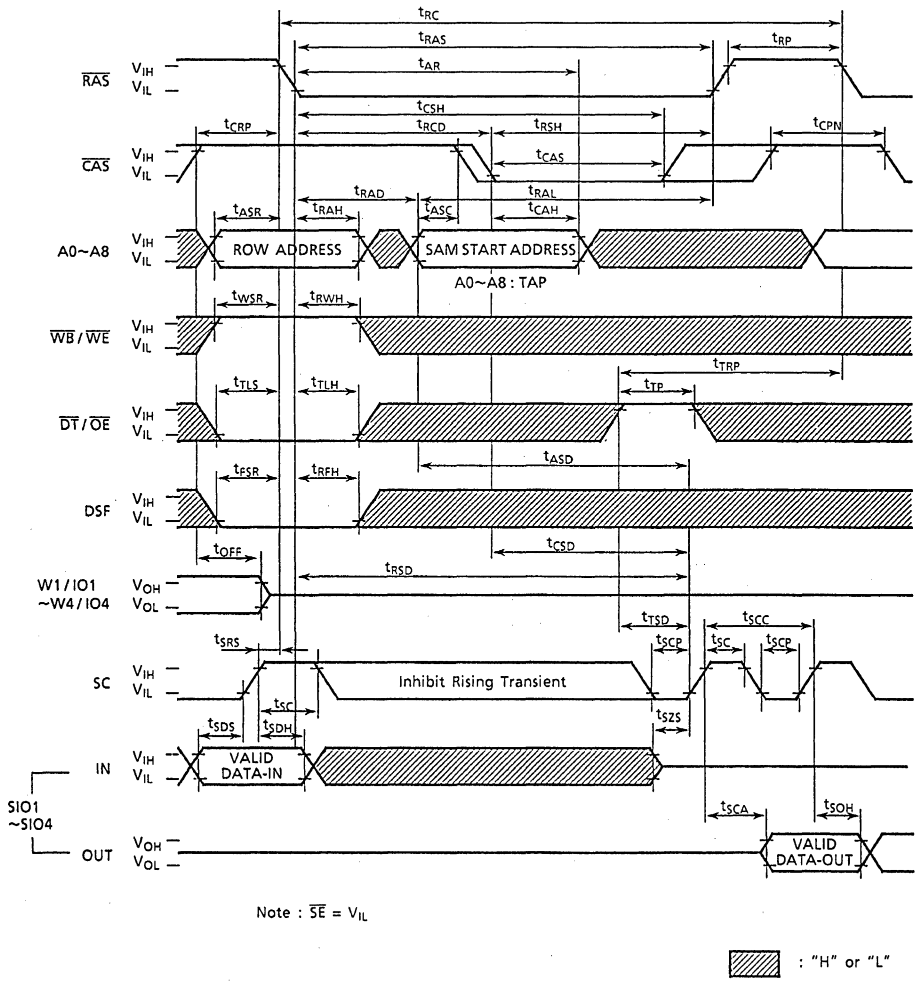
*1 $\overline{WB}/\overline{WE}$	*2 DSF	*3 W1/IO1~W4/104	Cycle
0	0	WM1 data	Block Write (Mask 1) (New Mask Mode)
	1	Don't Care	Block Write (Mask 2) (Old Mask Mode)
1	0	Don't Care	Block Write (No Mask Mode)

WM1 data 0: Write Disable
1: Write Enable

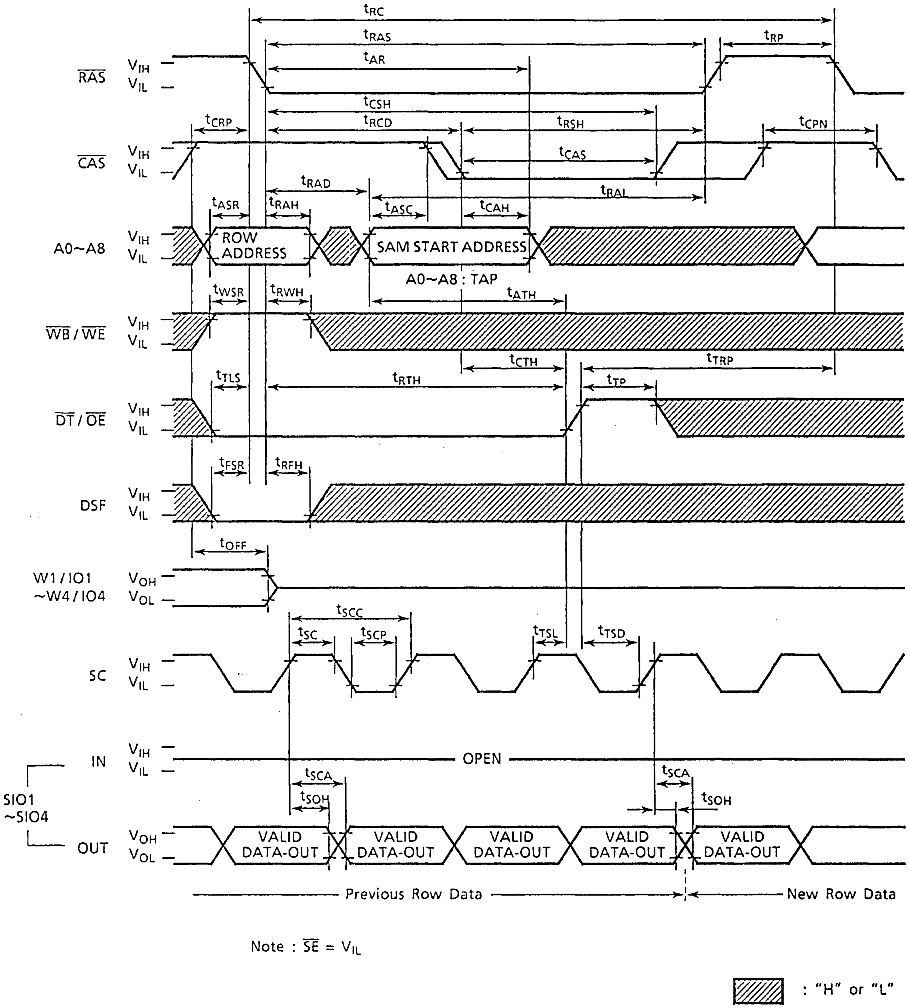
*4) COLUMN SELECT
W1/I01 – Column 0 (A1C=0, AOC=0
W2/I02 – Column 1 (A1C=0, AOC=1
W3/I03 – Column 2 (A1C=1, AOC=0
W4/I04 – Column 3 (A1C=1, AOC=1

} Wn/IOn
=0 : Disable
=1 : Enable

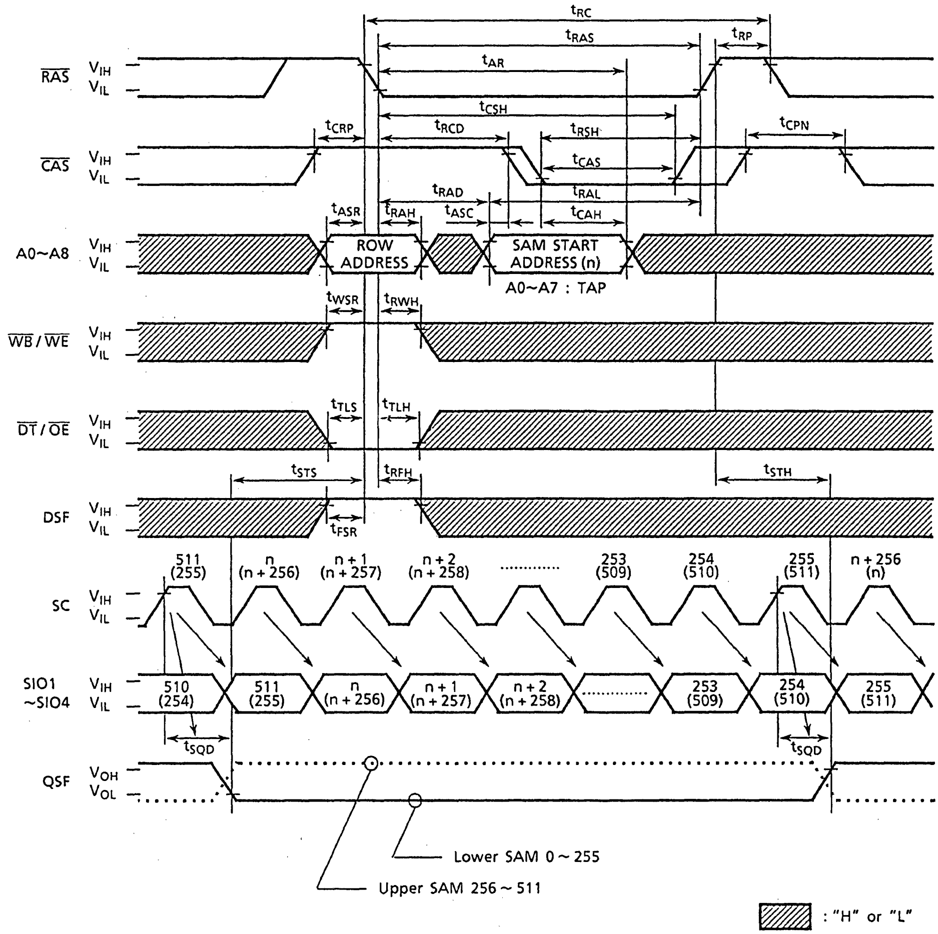
READ TRANSFER CYCLE (Previous is WRITE TRANSFER CYCLE)



REAL TIME READ TRANSFER CYCLE

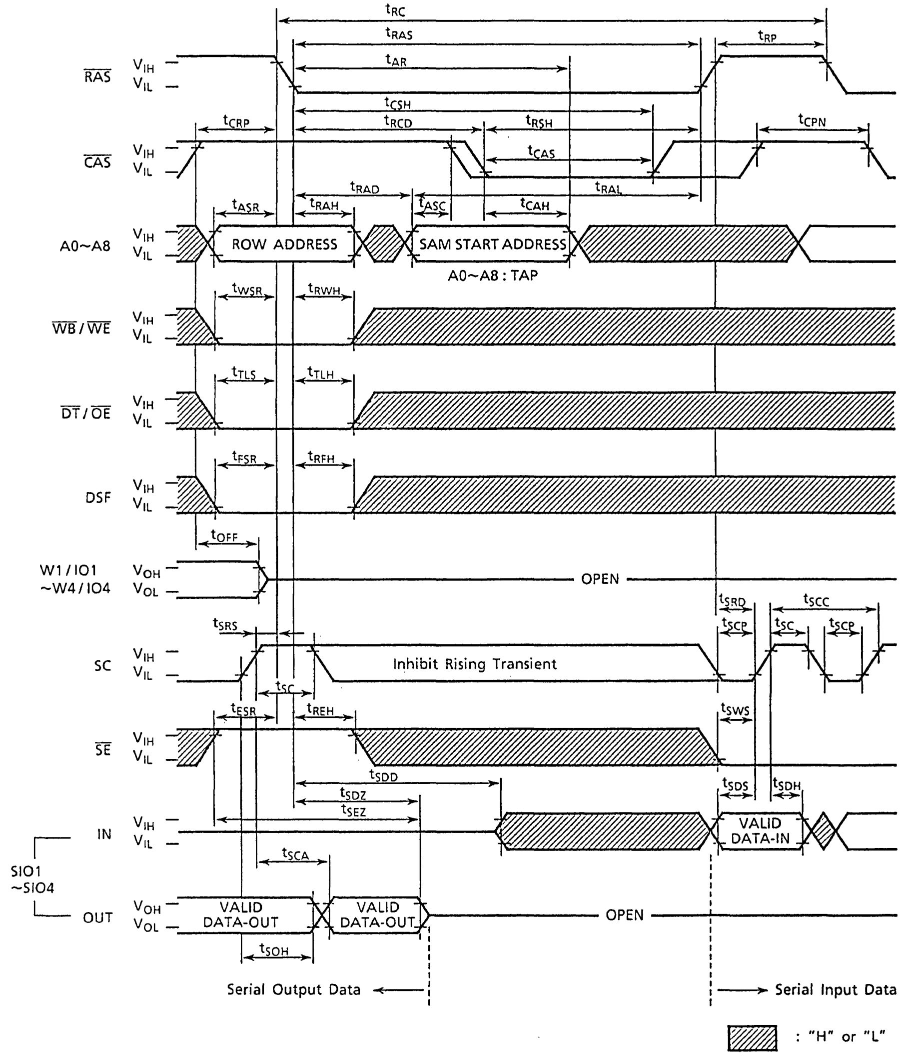


SPLIT READ TRANSFER CYCLE

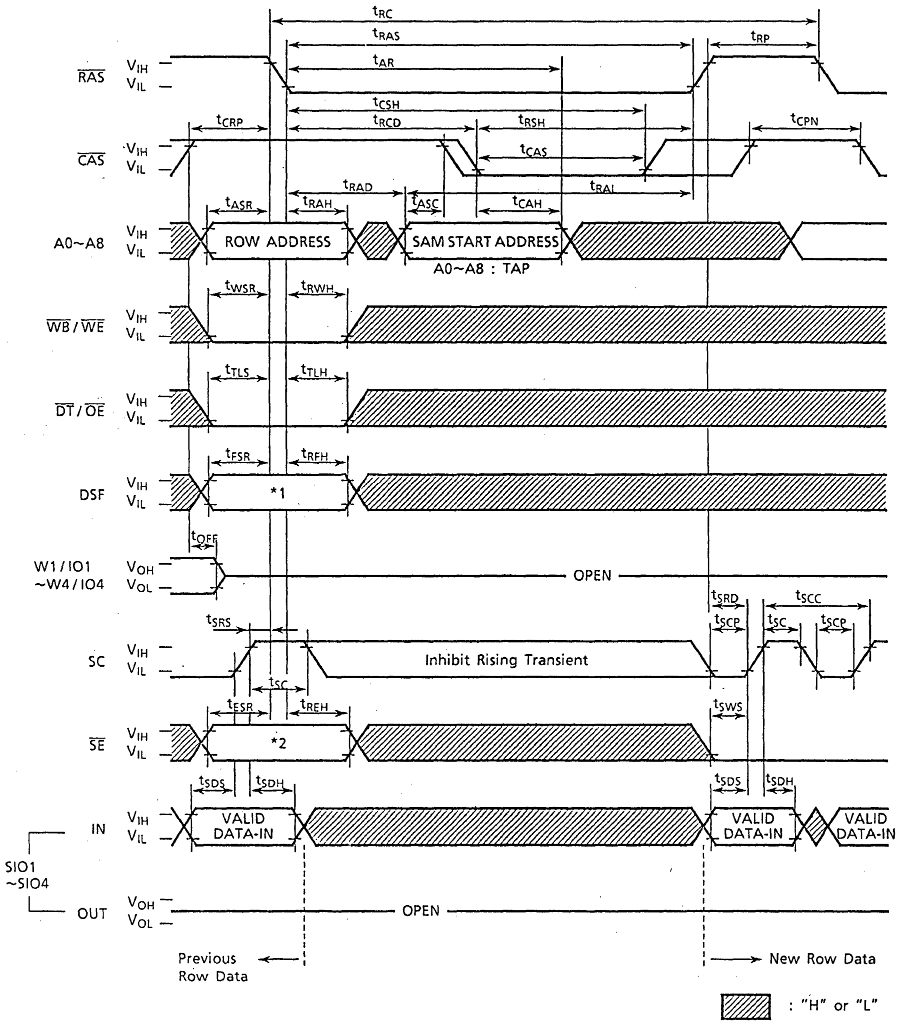


Note : $\overline{SE}$ = V_{IL}

PSEUDO WRITE TRANSFER CYCLE

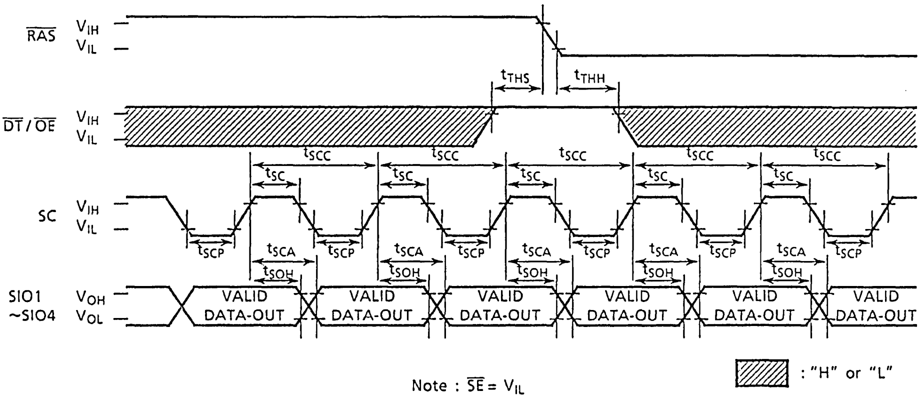


WRITE TRANSFER CYCLE

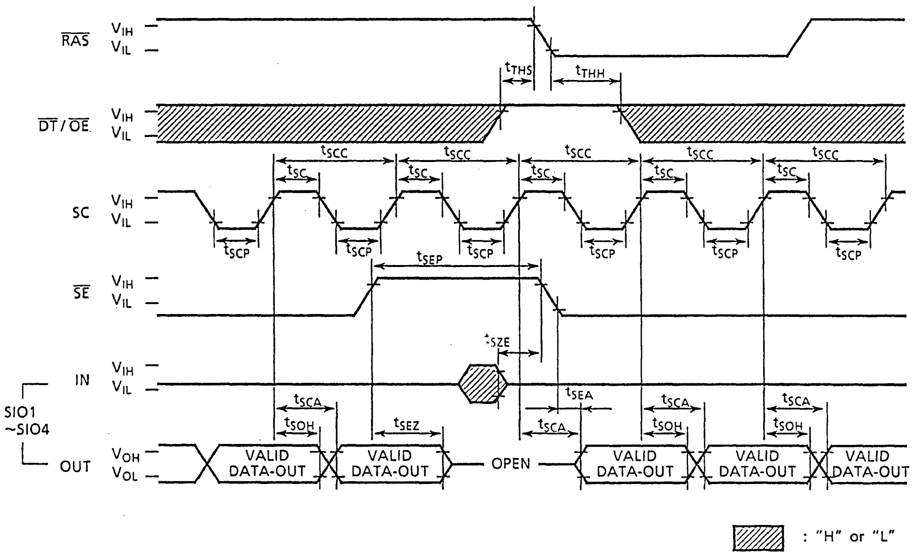


*1 DSF	*2 $\overline{SE}$	Cycle
0	0	Write Transfer
1	*	Write Transfer

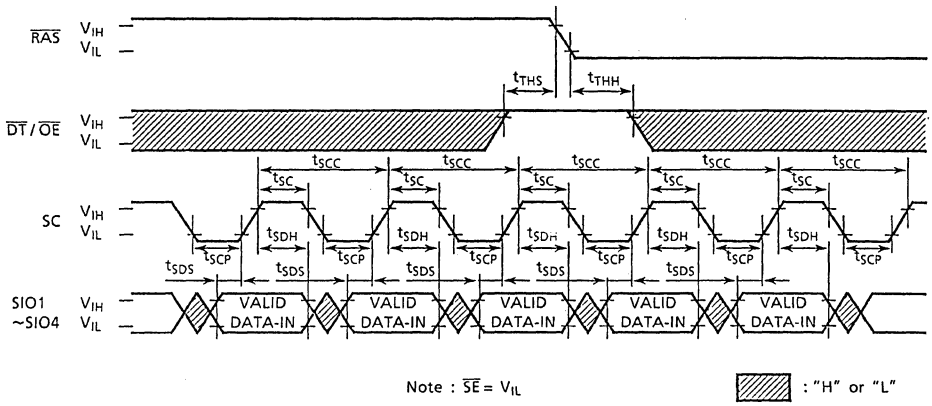
SERIAL READ ($\overline{SE}$ = V_{IL})



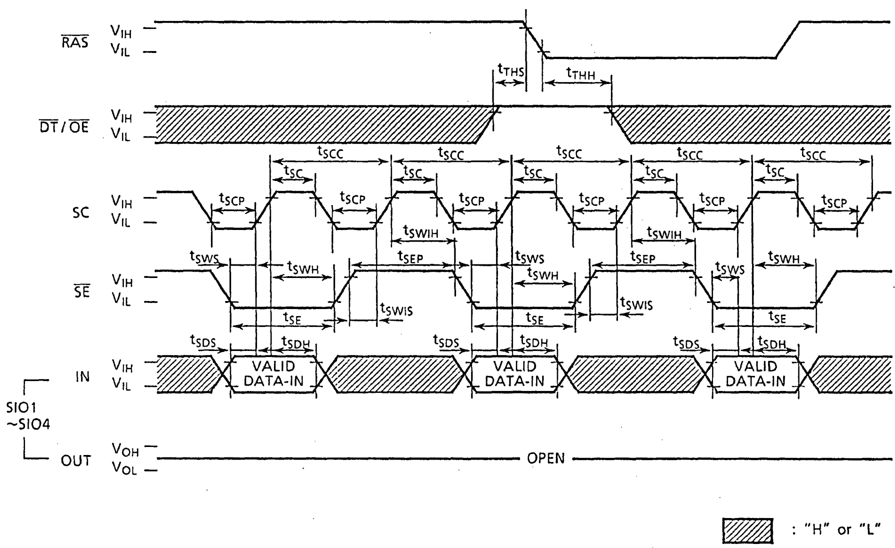
SERIAL READ ($\overline{SE}$ Controlled Outputs)



SERIAL WRITE CYCLE ($\overline{SE}$ = V_{IL})



SERIAL WRITE ($\overline{SE}$ Controlled Inputs)



PIN FUNCTION

ADDRESS INPUTS : A_0~A_8

The 18 address bits required to decode 4 bits of the 1,048,576 cell locations within the dynamic RAM memory array of the TC524259B are multiplexed onto 9 address input pins (A_0~A_8). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

ROW ADDRESS STROBE : $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT}$ / $\overline{OE}$, $\overline{WB}$ / $\overline{WE}$, $\overline{SE}$ and DSF to invoke the various random access and data transfer operating modes shown in Table 2. $\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the RAS control is held "high".

COLUMN ADDRESS STROBE : $\overline{CAS}$

CAS is the control input that latches the column address bits and the state of the special function input DSF to select, in conjunction with the $\overline{RAS}$ control, either read / write operations or the special block write feature on the RAM port when the DSF input is held "low" at the falling edge of $\overline{RAS}$. Refer to the operation truth table shown in Table 1. $\overline{CAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. $\overline{CAS}$ also acts as an output enable for the output buffers on the RAM port.

DATA TRANSFER / OUTPUT ENABLE : $\overline{DT}$ / $\overline{OE}$

The $\overline{DT}$ / $\overline{OE}$ input is a multifunction pin. When $\overline{DT}$ / $\overline{OE}$ is "high" at the falling edge of RAS, RAM port operations are performed and $\overline{DT}$ / $\overline{OE}$ is used as an output enable control. When the $\overline{DT}$ / $\overline{OE}$ is "low" at the falling edge of $\overline{RAS}$, a data transfer operation is started between the RAM port and the SAM port.

WRITE PER BIT / WRITE ENABLE: $\overline{WB}$ / $\overline{WE}$

The $\overline{WB}$ / $\overline{WE}$ input is also a multifunction pin. When $\overline{WB}$ / $\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, during RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB}$ / $\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, during RAM port operations, the write-per-bit function is enabled. The $\overline{WB}$ / $\overline{WE}$ input also determines the direction of data transfer between the RAM array and the serial register (SAM).
When $\overline{WB}$ / $\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer).
When $\overline{WB}$ / $\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (write transfer).

WRITE MASK DATA / DATA INPUT AND OUTPUT: W_1 / IO_1 ~W_4 / IO_4

When the write-per-bit (New Mask Mode) function is enabled, the mask data on the Wi/IOi pins is latched into the write mask register (WM1) at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic "1". Writing is inhibited on data lines where the write-mask data is a logic "0". The write-mask data is valid for only one cycle. Data is written into the RAM port during a write or read-modify-write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB}$ / $\overline{WE}$, whichever occurs late. During an early-write cycle, the outputs are in the high-impedance state. Data is read out of the RAM port during a read or read-modify-write cycle. The output data becomes valid on the Wi / IOi pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}$ / $\overline{OE}$ and column address are satisfied and will remain valid as long as $\overline{CAS}$ and $\overline{DT}$ / $\overline{OE}$ are kept "low". The outputs will return to the high-impedance state at the rising edge of either $\overline{CAS}$ or $\overline{DT}$ / $\overline{OE}$, whichever occurs first.

SERIAL CLOCK: SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 9-bits serial pointer (8-bits in split register mode) which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the starting location which is determined by the column address in the read transfer cycle. When the pointer reaches the most significant address location (decimal 511), the next SC clock will place it at the least significant address location (decimal 0). The serial clock SC must be held at a constant V_{IH} or V_{IL} level during read / pseudo write / write transfer operations and should not be clocked while the SAM port is in the standby mode to prevent the SAM pointer from being incremented.

SERIAL ENABLE: $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "high".

SPECIAL FUNCTION CONTROL INPUT: DSF

The DSF input is latched at the falling edge of $\overline{RAS}$ and $\overline{CAS}$ and allows for the selection of various random port and data transfer operating modes. In addition to the conventional multiport DRAM, the special features consisting of write per bit 2, block write, block write (mask 1 & 2), load color / mask register and split read transfer can be invoked.

SPECIAL FUNCTION OUTPUT: QSF

QSF is an open drain output signal which, during split register operation, indicates which half of the split SAM is being accessed. Since QSF is an open drain output, it must be pulled up to V_{CC} with an appropriate pull-up resistor. QSF "on" (low state) indicates that the lower split SAM (Bits 0 thru 255) is being accessed and QSF" off' (open state) indicates that the upper split SAM (Bits 256 thru 511) is begin accessed. After the QSF has toggled to either an open or low state, a delay of ^{t}STS must be met before a split read transfer operation can be performed on the non-active half of the split SAM.

SERIAL INPUT / OUTPUT: SIO1~SIO4

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode. During subsequent write transfer cycle, the SAM remains in the input mode.

OPERATION MODE

The RAM port and data transfer operating of the TC524259BJ/BZ are determined by the state of $\overline{CAS}$, $\overline{DT}$ / $\overline{OE}$, $\overline{WB}$ / $\overline{WE}$, $\overline{SE}$ and DSF at the falling edge of $\overline{RAS}$ and by the state of DSF at the falling edge of $\overline{CAS}$. The Table 1 and the Table 2 show the operation truth table and the functional truth table for a listing of all available RAM port and transfer operation, respectively.

Table 1. Operaton Truth Table

$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	DSF ($\overline{CAS}$ falling edge) = 0, DSF ($\overline{RAS}$ falling edge) = 0	DSF ($\overline{CAS}$) = 0, DSF ($\overline{RAS}$) = 1	DSF ($\overline{CAS}$) = 1, DSF ($\overline{RAS}$) = 0	DSF ($\overline{CAS}$) = 1, DSF ($\overline{RAS}$) = 1
0	*	*	*	$\overline{CAS}$ before $\overline{RAS}$ Refresh			
1	0	0	0	Write Transfer	Write Transfer with	Write Transfer	Write Transfer
1	0	0	1	Pseudo Write Transfer		Pseudo Write Transfer	
1	0	1	*	Read Transfer	Split Read Transfer	Read Transfer	Split Read Transfer
1	1	0	*	Read/Write per Bit 1	Read/Write per Bit 2	Block Write (Mask 1)	Block Write (Mask 2)
1	1	1	*	Read/Write	Load Mask	Block Write	Load Color

Table 2. Functional Truth Table

Function	$\overline{RAS}$ ↓: $\overline{CAS}$	$\overline{RAS}$ ↓: $\overline{DT}/\overline{OE}$	$\overline{RAS}$ ↓: $\overline{WB}/\overline{WE}$	$\overline{RAS}$ ↓: DSF	$\overline{RAS}$ ↓: $\overline{SE}$	$\overline{CAS}$ ↓: DSF	Address: $\overline{RAS}$ ↓	Address: $\overline{CAS}$ ↓	W/IO: $\overline{RAS}$ ↓	W/IO: $\overline{CAS}$ ↓	W/IO: $\overline{CAS}$ ↓ $\overline{WE}$ ↓	Write Mask	Register: WM 1	Register: Color
$\overline{CAS}$ before $\overline{RAS}$ Refresh	0	*	*	*	*	-	*	-	*	-	-	-	-	-
Write Transfer	1	0	0	0	0	*	Row	TAP	WM1	*	*	WM 1	Load use	-
Pseudo Write Transfer	1	0	0	0	1	*	Row	TAP	*	*	*	-	-	-
Write Transfer	1	0	0	1	*	*	Row	TAP	WM1	-	*	WM 1	Load use	-
Read Transfer	1	0	1	0	*	*	Row	TAP	*	*	*	-	-	-
Split Read Transfer	1	0	1	1	*	*	Row	TAP	*	*	*	-	-	-
Write per Bit 1	1	1	0	0	*	0	Row	Column	WM1	-	DIN	WM 1	Load use	-
Block Write (Mask Z)	1	1	0	0	*	1	Row	Column A2C-8C	WM1	Column Select	-	WM 1	Load use	use
Write per Bit 2	1	1	0	1	*	*	Row	*	WM1	-	*	WM 1	Load use	use
Block Write (Mask 2)	1	1	1	0	*	0	Row	Column	*	-	DIN	-	-	-
Block Write	1	1	1	0	*	1	Row	Column A2C-8C	*	Column Select	-	-	-	use
Load Color	1	1	1	1	*	*	Row	*	*	-	Color	-	-	Load

* : “O” or “1” , TAP : SAM start address , : not used

If the special function control input (DSF) is in the "low" state at the falling edges of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, only the conventional multiport DRAM operating features can be invoked: $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, write transfer, pseudo-write transfer, read transfer and read write modes. If the DSF input is "high" at the falling edge of $\overline{\text{RAS}}$, special features such as split write transfer, split read transfer, flash write and load color register can be invoked. If the DSF input is "low" at the falling edge of $\overline{\text{RAS}}$ and "high" at the falling edge of $\overline{\text{CAS}}$, the block write special feature can be invoked.

RAM PORT OPERATION

FAST PAGE MODE CYCLE

Fast page mode allows data to be transferred into or out of multiple column locations of the same row by performing multiple $\overline{\text{CAS}}$ cycle during a single active $\overline{\text{RAS}}$ cycle. During a fast page cycle, the $\overline{\text{RAS}}$ signal may be maintained active for a period up to 100 µseconds. For the initial fast page mode access, the output data is valid after the specified access times from $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, column address and $\overline{\text{DT}}/\overline{\text{OE}}$. For all subsequent fast page mode read operations, the output data is valid after the specified access times from $\overline{\text{CAS}}$, column address and $\overline{\text{DT}}/\overline{\text{OE}}$, When the write-per-bit function is enabled, the mask data latched at the falling edge of $\overline{\text{RAS}}$ is maintained throughout the fast page mode write or read-modify-write cycle.

$\overline{\text{RAS}}$-ONLY REFRESH

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the 6pecified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{\text{RAS}}$-Only" cycle.

$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH

The TC524259BJ/BZ also offers an internal-refresh function. When $\overline{\text{CAS}}$ is held "low" for a specified period (^{t}CSR) before $\overline{\text{RAS}}$ goes "low", an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle. For successive $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle, $\overline{\text{CAS}}$ can remain "low" while cycling $\overline{\text{RAS}}$.

HIDDEN REFRESH

A hidden refresh is a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh performed by holding $\overline{\text{CAS}}$ "low" from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{\text{RAS}}$ after the specified $\overline{\text{RAS}}$-precharge period (Refer to Figure 1)

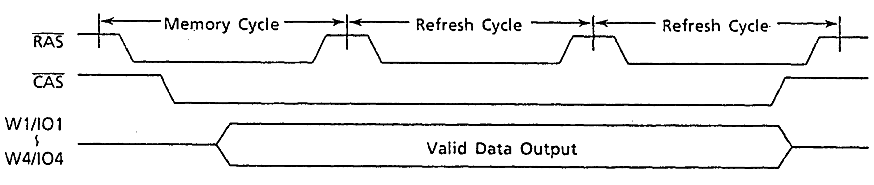


Figure 1. Hidden Refresh Cycle

WRITE-PER-BIT FUNCTION

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. Two types of write-per-bit may be utilized-"New Mask Mode" or "Old Mask Mode". The state of the signals required to select the modes of write-per-bit are shown in Table 3.

The write-per-bit 1 (New Mask Mode) function is enabled when $\overline{\text{WB}}$ / $\overline{\text{WE}}$ and DSF are held "low" at the falling edge of $\overline{\text{RAS}}$ in a random write operation. Also, at the falling edge of $\overline{\text{RAS}}$, the mask data on the W_i / IO_i pins are latched into a write maslc register (WM1). New write mask data must be presented at the W_i / IO_i pins at every falling edge of $\overline{\text{RAS}}$. A "0" on any of the W_i / IO_i pins will disable the corresponding write circuits and new data will not be written into the RAM. A "1" on any of the W_i / IO_i pins will enable the corresponding write circuits and new data will be written into the RAM.

The write-per-bit 2 (Old Mask Mode) function is enabled when $\overline{\text{WB}}$ /$\overline{\text{WE}}$ is "low" and DSF is "high" at the falling edge of $\overline{\text{RAS}}$ in a random write operation. This function does not use the data present on the Wi / IO_i pins at the falling edge of $\overline{\text{RAS}}$ as write mask data. Therefore, data on the W_i / IO_i pins at the falling edge of $\overline{\text{RAS}}$ is a don't care ("H" or "L"). The write mask data which is utilized by this function resides in the write mask register (WM1). The mask data is placed into the "WM1" write mask register by using either the "Load Mask Register Cycle", "Write-per-bit 1 (New Mask Mode) Function", or "Block Write 1 (New Mask Mode) Function"

Table 3. Write-per-bit function truth table

At the falling edge of $\overline{\text{RAS}}$ ($\overline{\text{RAS}}$ ↘)					$\overline{\text{CAS}}$ ↘	Function
$\overline{\text{CAS}}$	$\overline{\text{DT/OE}}$	$\overline{\text{WB/WE}}$	DSF	W/IO	DSF	
H	H	H	L	*	L	Normal Write
H	H	L	L	WM1	L	Write-per-bit 1 (New Mask Mode)
H	H	L	H	*	L	Write-per-bit 2 (Old Mask Mode)

An example of the write-per-bit function illustrating its application to displays is shown in Figures 2 and 3.

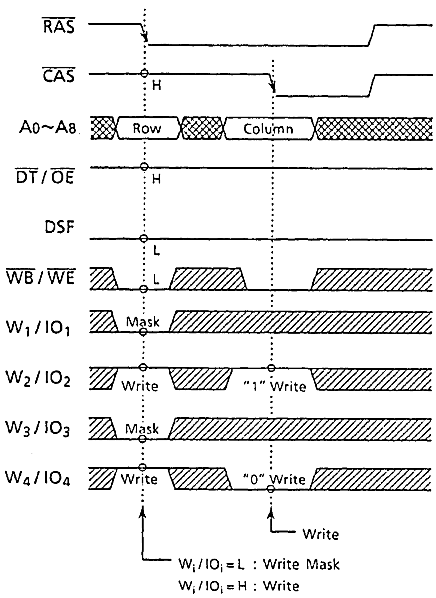


Figure 2. Write-per-bit timing cycle

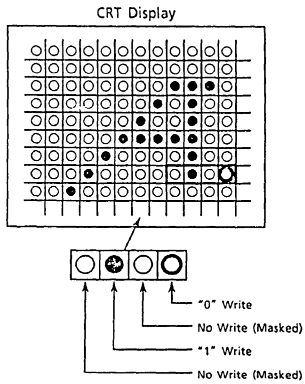


Figure 3. Corresponding bit-map

LOAD COLOR REGISTER

The TC524259B is provided with an on-chip 4-bits register (color register) which is used in the block write function. Each bit of the color register corresponds to one of the DRAM I/O blocks. The load color register cycle is initiated by holding $\overline{CAS}$, $\overline{DT}$ / $\overline{OE}$, $\overline{WB}$ / $\overline{WE}$ and DSF "high" at the falling edge of $\overline{RAS}$ and by holding DSF "low" at the falling edge of $\overline{CAS}$. The data presented on the W_i / IO_i lines are subsequently latched into the color register at the falling edge of $\overline{CAS}$ or $\overline{WB}$ / $\overline{WE}$, whichever occurs later. During the load color register cycle, a valid row address (A_0 thru A_8) is not required. However, the memory cells of the row address which is latched at the falling edge of $\overline{RAS}$ is refreshed.

LOAD MASK REGISTER

The TC524259B has an on-chip 4 bit register (WM1 register) which provides the I/O mask data during the write-per-bit (New and Old Mask Mode) and Block Write (New and Old Mask Mode) functions. Each bit of the mask register corresponds to one of the DRAM I/O blocks. The mask data must be specified in the WM1 register by using the load mask register cycle prior to the execution of "Write-Per-Bit 2" and "Block Write 2" old mask mode functions. The load mask register cycle is initiated by holding $\overline{CAS}$, $\overline{DT}$ / $\overline{OE}$, $\overline{WB}$ / $\overline{WE}$ and DSF "high" at the falling edge of $\overline{RAS}$ and by DSF "high" at the falling edge of $\overline{CAS}$. The data presented on the W_i / IO_i lines are subsequently latched into the mask register at the falling edge of either $\overline{CAS}$ or $\overline{WB}$ / $\overline{WE}$, whichever occurs later. The mask data which is latched into the WM1 register will also be updated by the write-per-bit 1 (New Mask Mode) or Block Write 1 (New Mask Mode) functions. During the load mask register cycle, a valid row address (A_0 thru A_8) is not required. However, the memory cells of the row address which is latched at the falling edge of $\overline{RAS}$ is refreshed.

BLOCK WRITE

Block write is a special RAM port write operation which, in a single $\overline{RAS}$ cycle, writes the data in the color register into 4 consecutive colutnn address locations starting from a selected column in a selected row. Three modes of block write operation may be selected-No Mask Mode, New Mask Mode, Old Mask Mode. Column mask capability is applicable on all three modes. The seven most significant column addresses (A2C~A8C) are latched at the falling edge of $\overline{CAS}$ to designate the starting column address and the two least significant column addresses (A0C~A1C) are "don't care". The column mask data is also provided on the W_i / IO_i pins at the falling edge of $\overline{CAS}$. This column mask data will enable / disable the write operation on any of the 4 consecutive column address locations,

A block write cycle is selected by holding $\overline{CAS}$, and $\overline{DT}$ /$\overline{OE}$ "high" at the falling edge of $\overline{RAS}$ and DSF "high" at the falling edge of $\overline{CAS}$. The state of the $\overline{WB}$ / $\overline{WE}$ and DSF inputs at the falling edge of RAS will select one of the three modes of block write as shown in the following table 4.

When the DSF input at the falling edge of $\overline{RAS}$ is "low", the state of $\overline{WB}$ / $\overline{WE}$ selects either "No Mask Mode" or "New Mask Mode". If $\overline{WB}$ / $\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, the block write (No Mask Mode) is selected. If $\overline{WB}$ / $\overline{WE}$ is "low" at the falling edge of RAS, the block write 1 (New Mask Mode) is selected and the mask data on the W_i / IO_i pins are latched and used like the write—per-bit 1 (New Mask Mode) function.

If DSF is "high" and $\overline{WB}$ / $\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, then the block write 2 (Old Mask Mode) is selected and the mask data stored in the "WM1" register is used. The I/O masking for this function is used in the same manner as the write-per-bit 2 (Old Mask mode).

Table 4. Block Write function truth table

At the falling edge of $\overline{RAS}$ ($\overline{RAS}$↘)					$\overline{CAS}$↘	Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DSF	W_i / IO_i	DSF	
H	H	H	L	*	H	Block Write (No Mask Mode)
H	H	L	L	WM1	H	Block Write (Mask 1) (New Mask Mode)
H	H	L	H	*	H	Block Write (Mask 2) (Old Mask Mode)

An example using the block write 1 (New Mask Mode) function with a data mask on W_i / IO_i , W_4 / IO_4 and column 2 is shown in Figure 5. Also, an example using a window clear clear and fill application is shown in Figure 6.

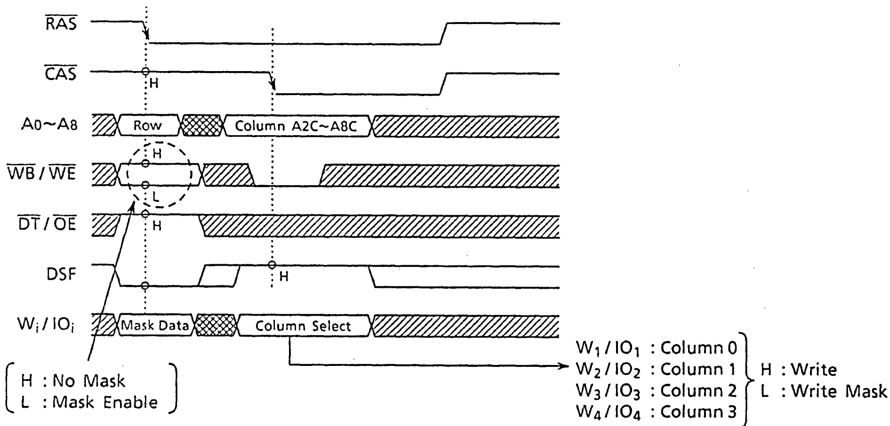


Figure 4. Block Write Timing

	Mask Data	Column Select	Color Resister Data
W_1/IO_1	0	1	0
W_2/IO_2	1	1	0
W_3/IO_3	1	0	1
W_4/IO_4	0	1	1

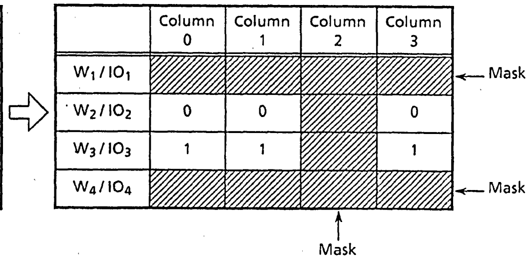


Figure 5. Example of Block Write Operation

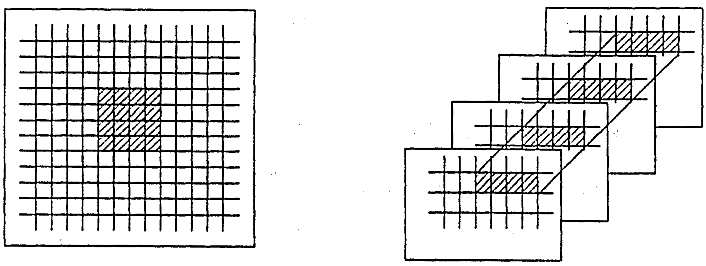


Figure 6. Example of Block Write Application

FAST PAGE MODE BLOCK WRITE CYCLE

Fast page mode block write can be used to perform high speed clear and fill operations. The cycle is initiated by holding the DSF signal "low" at the falling edge of $\overline{RAS}$ and a fast page mode block write is performed during each subsequent $\overline{CAS}$ cycle with DSF held "high" at the falling edge of $\overline{CAS}$.

If the DSF signal is "low" at the falling edge of $\overline{CAS}$, a normal fast page mode read / write operation will occur. Therefore a combination of block write and read / write operations can be performed during a fast page mode block write cycle. Refer to the example shown in Figure 10.

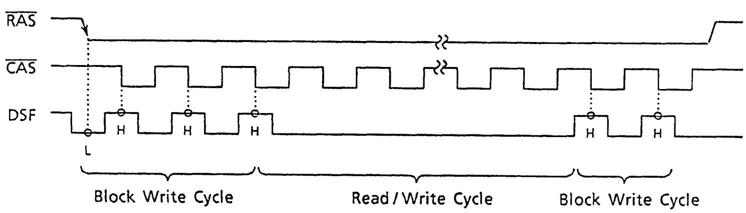


Figure 7. Fast Page Mode Block Write Cycle

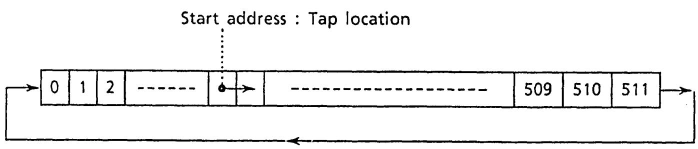
SAM PORT OPERATION

The TC524259B is provided with 512 words by 4 bits serial access memory (SAM) which can be operated in the single register mode or the split register mode.

SINGLE REGISTER MODE

When operating in the single register mode, high speed serial read or write operations can be performed through the SAM port independent of the RAM port operations, except during read / write / pseudo-write transfer cycles. The preceding transfer operation determines the direction of data flow through the SAM port. If the preceding transfer operation is a read transfer, the SAM port is in the output mode. If the preceding transfer operation is a write or pseudo write transfer, the SAM port is in the input mode. The pseudo write transfer operation only switches the SAM port from output mode to input mode; Data is not transferred from SAM to RAM.

Serial data can be read out of the SAM port after a read transfer (RAM—SAM) has been performed. The data is shifted out of the SAM port starting at any of the 512 bits locations. The TAP location corresponds to the column address selected at the falling edge of $\overline{CAS}$ during the read transfer cycle. The SAM registers are configured as circular data registers. The data is shifted out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit, as illustrated below.



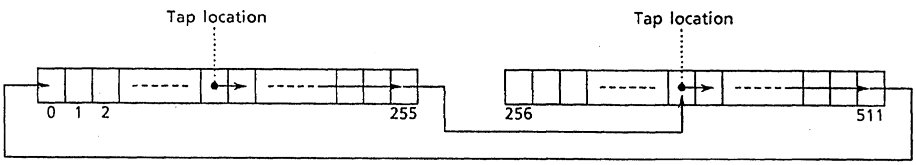
Subsequent real-time read transfer may be performed on-the-fly as many times as desired, within the refresh constraints of the DRAM array. Simultaneous serial read operation can be performed with some timing restrictions. A pseudo write transfer cycle is performed to change the SAM port from output mode to input mode in order to write data into the serial registers through the SAM port. A write transfer cycle must be used subsequently to load the SAM data into the RAM row selected by the row address at the falling edge of $\overline{RAS}$. The starting location in the SAM registers for the next serial write is selected by the column address at the falling edge of $\overline{CAS}$. The truth table for single register mode SAM operation is shown in Table 5.

Table 5. Block Write function truth table

SAM PORT OPERATION	$\overline{DT}$ / $\overline{OE}$ at the falling edge of $\overline{RAS}$	SC	$\overline{SE}$	FUNCTION	Preceded by a
Serial Output Mode	H		L H	Enable Serial Read Disable Serial Read	Read Transfer
Serial Input Mode			L H	Enable Serial Write Disable Serial Write	Write Transfer
Serial Input Mode			L H	Enable Serial Write Disable Serial Write	Pseudo Write Transfer

SPLIT REGISTER MODE

In split register mode, data can be shifted out of one half of the SAM while a split read transfer is being performed on the other half of the SAM. A normal (Non-split) read transfer operation must precede any split read transfer operation. The non—split read transfer will set the SAM port into output mode. The split read transfers will not change the SAM port mode set by preceding normal transfer operation. RAM port operation may be performed independently except during split transfers. In the split register mode, serial data can be shifted out of one of the split SAM registers starting from any at the 256 tap locations, excluding the last address of each split SAM, data is shifted out sequentially starting from the selected tap location to the most significant bit (255 or 511) of the first split SAM and then the SAM pointer moves to the tap location selected for the second split SAM to shift data out sequentially starting from this tap location to the most significant bit (511 or 255) and finally wraps around to the least significant bit, as illustrated in the example below.



REFRESH

The SAM data registers are static flip-flop, therefore a refresh is not required.

DATA TRANSFER OPERATION

The TC524259B features two types of internal data transfer capability between RAM and the SAM, as shown in Figure 8. During a normal (Non-split) transfer, 512 words by 4 bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer). During a split read transfer, 256 words by 4 bits of data can be loaded from the lower/upper half of the RAM into the lower/upper half of the SAM (Split Read Transfer). The normal transfer and split transfer modes are controlled by the DSF special function input signal.

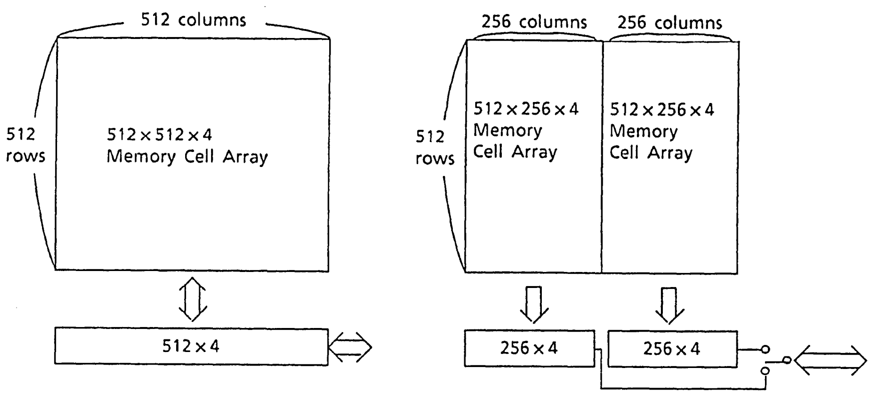


Figure 8. (a) Normal (Non—split) Transfer(b) Split Read Transfer

As shown in Table 6, the TC524259B supports four types of transfer operations: Read transfer, Split read transfor, Write transfer, and Pseudo write transfer. Data transfer operations between RAM and SAM are invoked by holding the $\overline{DT}$ / $\overline{OE}$ signal "low" at the falling edge of $\overline{RAS}$. The type of data transfer operation is determined by the state of $\overline{CAS}$, $\overline{WB}$ / $\overline{WE}$, $\overline{SE}$ and DSF latched at the falling edge of $\overline{RAS}$. During normal (Non-split) data transfer operations, the SAM port is switched from input to output mode (Read transfer) or output to input mode (Write transfer / Pseudo write transfer) whereas it remains unchanged during split read transfer operations. During a data transfer cycle, the row address A_0~A_8 select one of the 512 rows of the memory array to or from which data will be transferred and the column address A_0=A_8 select one of the tap locations in the serial register. The selected tap location is the start position in the SAM port from which the first serial data will be read out during the subsequent serial read cycle or the start position in the SAM port into which the first serial data will be written during the subsequent serial write cycle. During split read transfer cycles, the most significant column address (A8C) is controlled internally to determine which half of the serial register will be reloaded from the RAM array.

Table 4. Block Write function truth table

at the falling edge of $\overline{RAS}$					Tranfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	DSF				
H	L	H	*	L	Read Transfer	RAM → SAM	512 x 4	Input → Output
H	L	L	L	L	Write Transfer	SAM → RAM	512 x 4	Output → Input
H	L	L	H	L	Pseudo Write Transfer	–	–	Output → Input
H	L	L	*	H	Write Transfer	SAM → RAM	256 x 4	Output → Input
H	L	H	*	H	Split Read Transfer	RAM → SAM	256 x 4	Not Changed

READ TRANSFER CYCLE

A read transfer consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}$ / $\overline{OE}$ "low" $\overline{WB}$ / $\overline{WE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of $\overline{DT}$ / $\overline{OE}$. When the transfer is completed, the SAM port is set into the output mode. In a read / real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}$ / $\overline{OE}$ and this data becomes valid on the SIO lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Figure 9 shows the operation block diagram for read transfer operation.

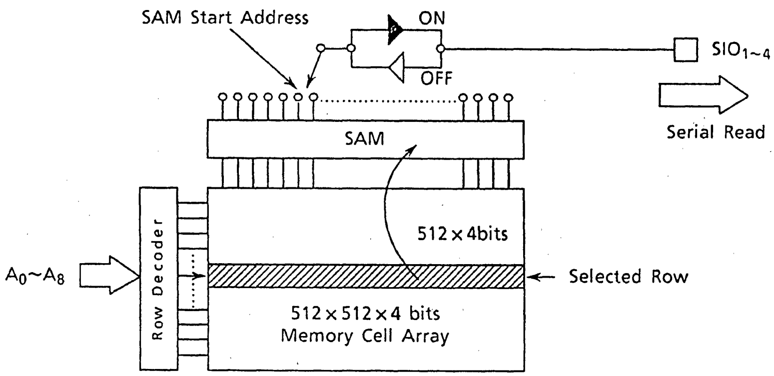


Figure 9. Block Diagram for Read Transfer Operation

In a read transfer cycle (which is preceded by a write transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}$ / $\overline{OE}$, as shown in Figure 10.

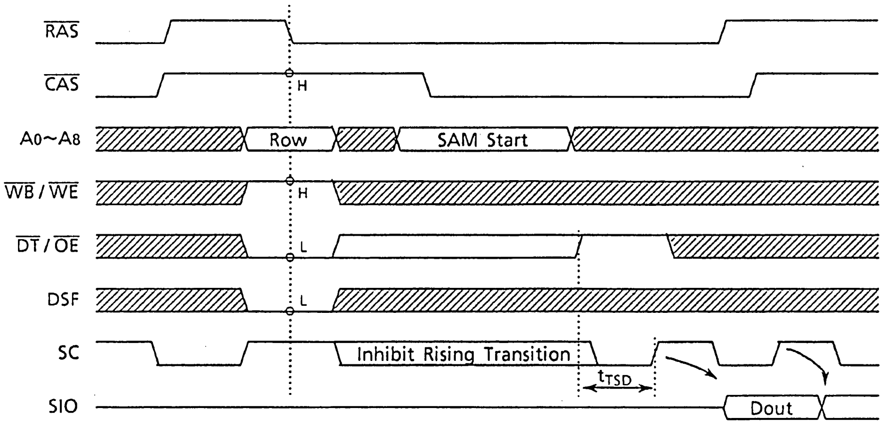


Figure 10. Read Transfer Timing

In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SIO lines until the $\overline{DT}$ / $\overline{OE}$ signal goes "high" and the serial access time t_{SCA} for the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of $\overline{DT}$ / $\overline{OE}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (t_{RTH}, t_{CTH}, and t_{TSL}/t_{TSD} must be satisfied), as shown in Figure 11.

The timing restriction t_{TSL}/t_{TSD} are 5ns min / 15ns min. The split read transfer mode eliminates these timing restrictions.

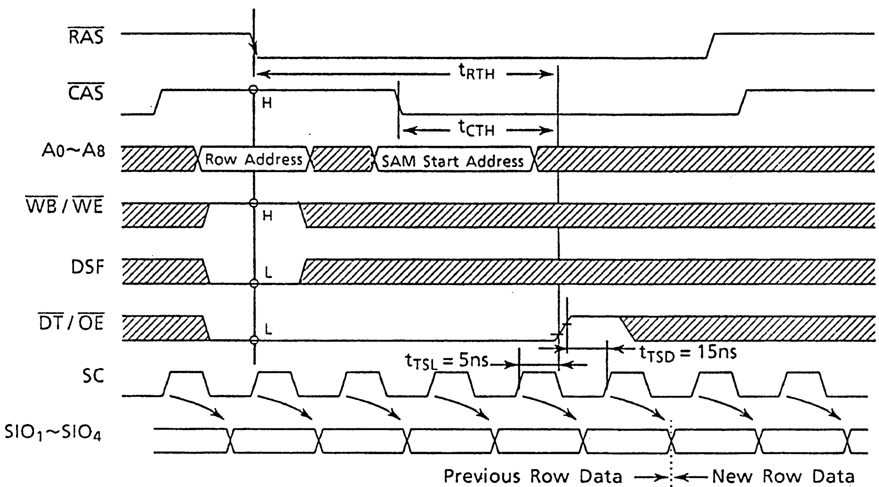
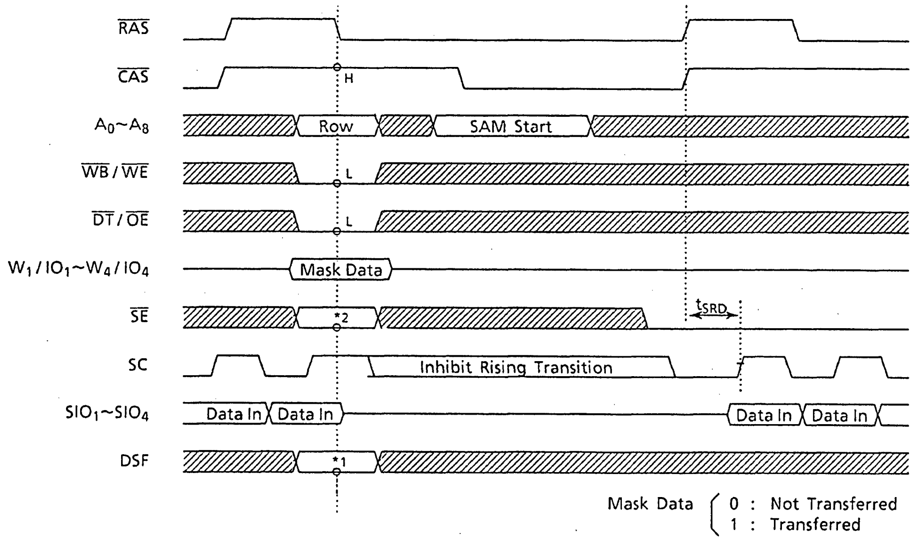


Figure 11. Real Time Read Transfer

WRITE TRANSFER CYCLE

A write transfer cycle transfers the contents of the SAM register into a selected row of the RAM array. If the SAM data to be transferred must first be loaded through the SAM port, a pseudo write transfer operation must precede the write transfer cycles. However, if the SAM data to be transferred into the RAM was previously loaded into the SAM via a read transfer, the SAM to RAM transfer can be executed simply by performing a write transfer cycle. A write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}$ / $\overline{OE}$ "low", $\overline{WB}$ / $\overline{WE}$ "low", $\overline{SE}$ "low" and DSF "low" at the falling edge of $\overline{RAS}$. Also if DSF is "high" under the condition of a "high" $\overline{CAS}$, "low" $\overline{DT}$ / $\overline{OE}$ and "low", $\overline{WB}$ / $\overline{WE}$ at the falling edge of $\overline{RAS}$, a write transfer is invoked independent of the state of $\overline{SE}$.



*1 DSF	*2 SE	Operation
0	L	Write Transfer
1	L or H	Write Transfer

The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.

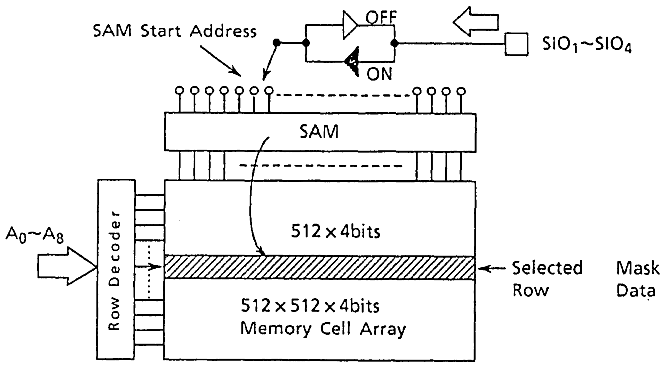


Figure 13. Block Diagram for Write Transfer Operation

When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$, at which time a new row of data can be written in the serial register.

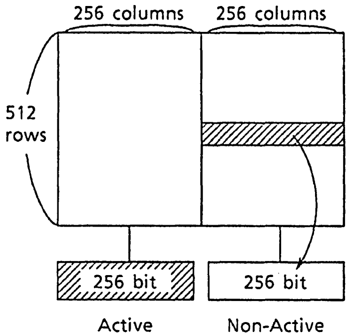
PSEUDO WRITE TRANSFER CYCLE

A pseudo write transfer cycle must be performed before loading data into the serial register after a read transfer operation has been executed. The only purpose of a pseudo write transfer is to change the SAM port mode from output mode to input mode (A data transfer from SAM to RAM does not occur). After the serial register is loaded with new data, a write transfer cycle must be performed to transfer the data from SAM to RAM. A pseudo write transfer is invoked by holding $\overline{CAS}$ “high”, $\overline{DT}$ / $\overline{OE}$ “low”, $\overline{WB}$ / $\overline{WE}$ “low”, $\overline{SE}$ “high” and DSF “low” at the falling edge of $\overline{RAS}$.

The timing conditions are the same as the one for the write transfer cycle except for the state of SE at the falling edge of $\overline{RAS}$.

SPLIT READ TRANSFER AND QSF

The TC524259BJ / BZ features a split read transfer capability between the RAM and the SAM. During split read transfer operation, the serial register is split into two halves which can be controlled independently. Split read transfer operations can be performed to one half of the serial register while serial data can be shifted out of the other half of the serial register, as shown in Figure 14. The most significant column address location (A8C) is controlled internally to determines which half of the serial register will be reloaded from the RAM array. QSF is an output in which indicates which half of the serial register is in an active state. QSF changes state when the last SC clock is applied to active split SAM, as shown in Figure 15.



Active SAM	QSF Level
Lower SAM	"Low"
Upper SAM	"High"

Figure 14. Split Register Mode

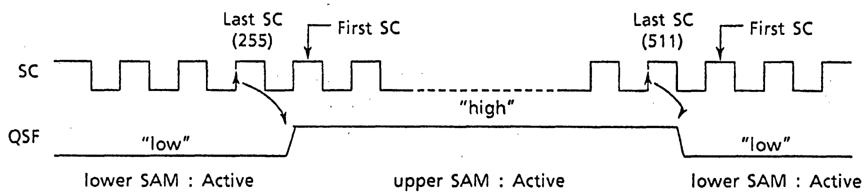


Figure 15. QSF Output State During Split Register Mode

SPLIT READ TRANSFER CYCLE

A split read transfer consists of loading 256 words by 4 bits of data from a selected row of the split RAM array into the corresponding non-active split SAM register.

Serial data can be shifted out of the other half of the split SAM register simultaneously. The block diagram and timing diagram for split read transfer mode are shown in Figure 16 and 17, respectively. During split read transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus eliminating timing restrictions as in the case of on-the-fly read transfers. A split read transfer can be performed after a delay of t_{STS}, from the change of state of the QSF output, is satisfied.

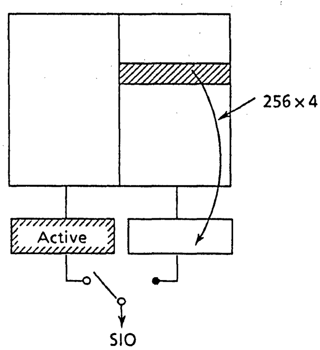


Figure 16. Block Diagram for Split Read Transfer

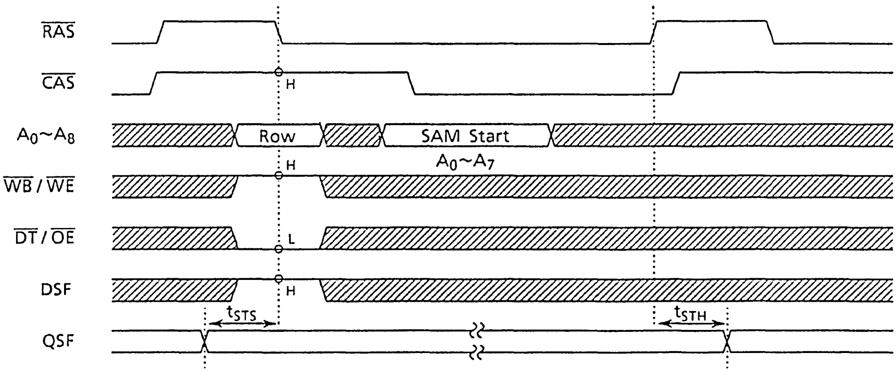


Figure 17. Timing Diagram for Split Read transfer

A normal (Non-split) read transfer operation must precede split read transfer cycles as shown in the example in Figure 18.

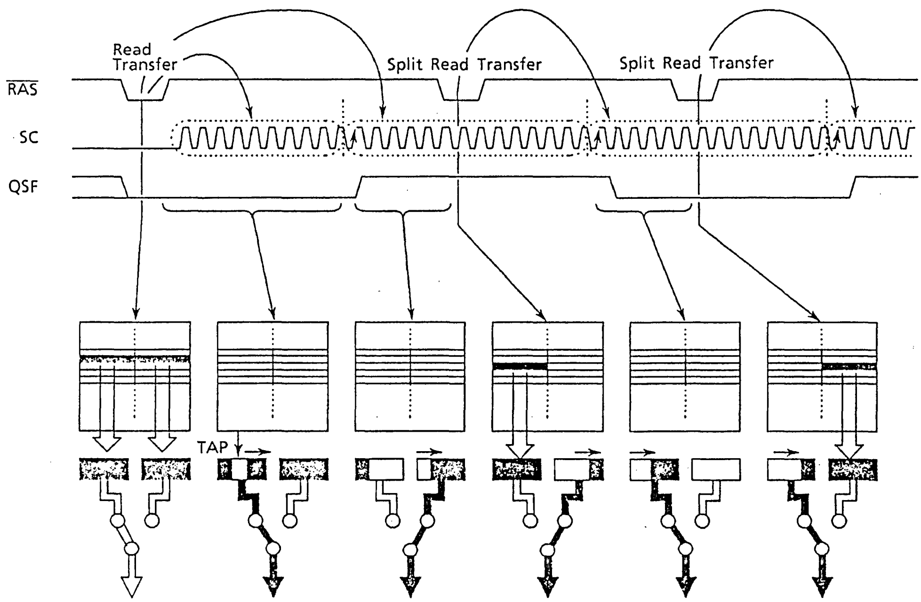


Figure 18. Example of Consecutive Read Transfer Operations

SPLIT—REGISTER OPERATION SEQUENCE (EXAMPLE)

Split read transfers must be preceded by a normal read transfer. Figure 19 illustrates an example of split register operation sequence after device power-up and initialization. After power-up, a minimum of 8 $\overline{RAS}$ and 8 SC clock cycles must be performed to properly initialize the device. A read transfer is then performed and the column address latched at the falling edge of $\overline{CAS}$ sets the SAM tap pointer location which up to that point was in an undefined location. Subsequently, the pointer address is incremented by cycling the serial clock SC from the starting location to the last location in the register (address 511) and wraps around to the tap location set by the split read transfer performed for the lower SAM while the upper SAM is being accessed. The SAM address is incremented as long as SC is clocked. The following split read transfer sets a new tap location in the upper split SAM register address 256 in this example and the pointer is incremented from this location by cycling the SC clock.

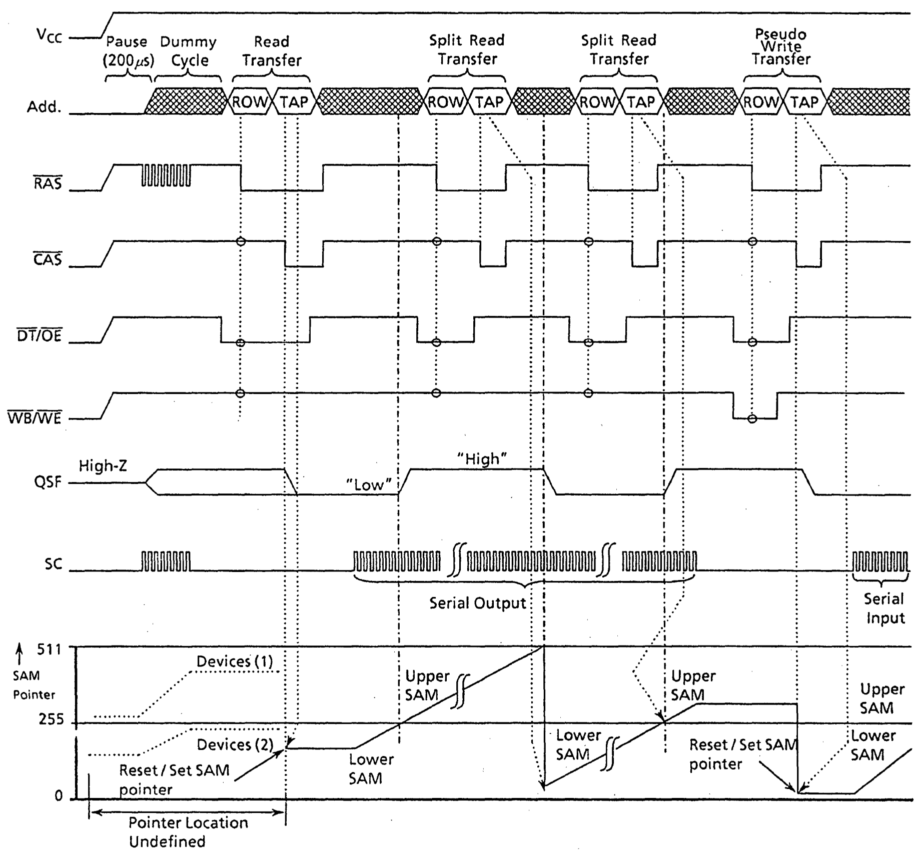
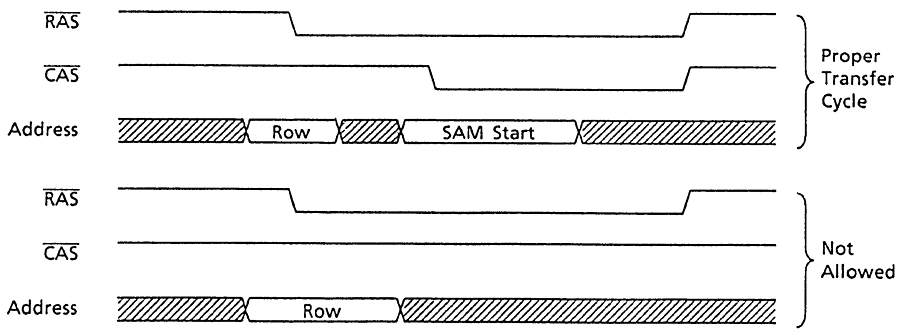


Figure 19. Example of Split SAM Register Operation Sequence

The next operation is a pseudo write transfer which switches the SAM port from output mode to input mode in preparation for either write transfers or split write transfers. The column address latched at the falling edge of $\overline{CAS}$ during the pseudo write transfer sets the serial register tap location. Serial data will be written into the SAM starting from this location.

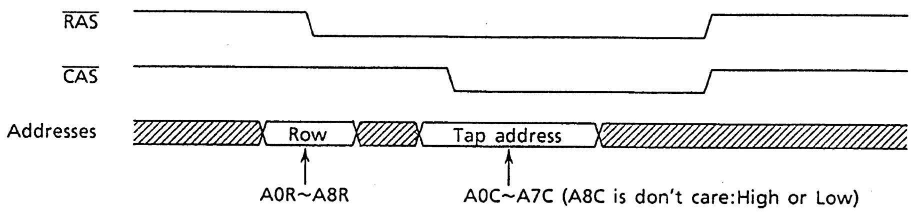
TRANSFER OPERATION WITHOUT CAS

During all transfer cycles, the $\overline{CAS}$ input clock must be cycled, so that the column address are latched at the falling edge of $\overline{CAS}$, to set the SAM tap location. If $\overline{CAS}$ was maintained at a constant "high" level during a transfer cycle, the SAM pointer location would be undefined. Therefore a transfer cycle with $\overline{CAS}$ held "high" is not allowed (Refer to the illustration below).



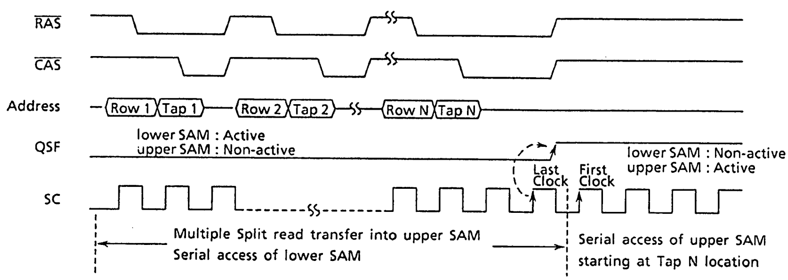
TAP LOCATION SELECTION IN SPLIT READ TRANSFER OPERATION

(a) In a split read transfer Operation, column addresses A0C through A7C must be latched at the falling edge of $\overline{CAS}$ in order to set the tap location in one of the split SAM registers. During a split read transfer, column address A8C is controlled internally and therefore it is ignored internally at the falling edge of $\overline{CAS}$.



During a split transfer, it is not allowed to set the last address location (A0C~A7C=FF), in either the lower SAM or the upper SAM$_1$I, as the tap location.

(b) In the case of multiple split read transfers performed into the same split SAM register, the tap location specified during the last split read transfer, before QSF toggles, will prevail. In the example shown below, multiple split read transfers are performed into the upper SAM (Non-active) while the lower SAM (active) is being accessed at the time when QSF toggles, the first SC serial clock will start shifting serial data starting from the Tap N address location.



SPLIT READ TRANSFER OPERATION ALLOWABLE PERIOD

Figure 26 illustrates the relationship between the serial clock SC and the special function output QSF during split read transfers and highlights the time periods where split read transfer are allowed, relative to SC and QSF.

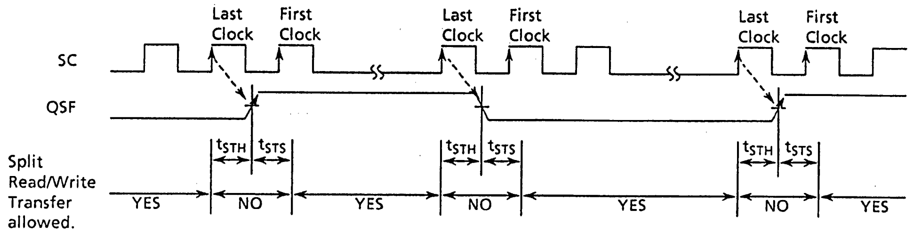
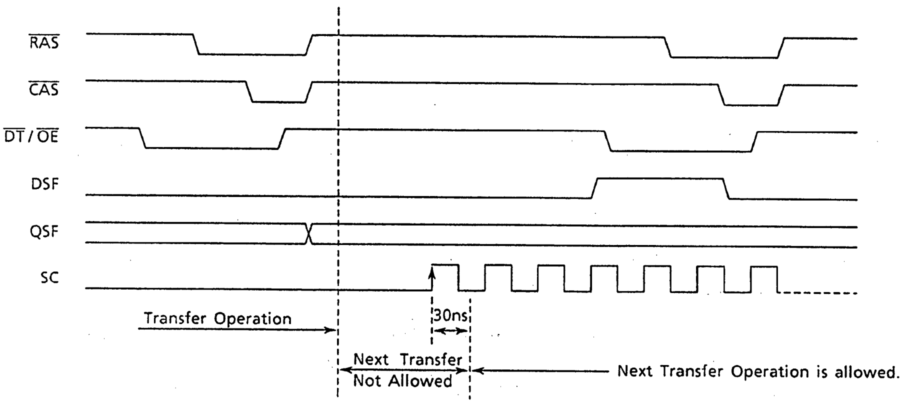


Figure 20. Split Transfer Operation Allowable Periods

As indicated in Figure 20, a split read transfer is not allowed during the period of $t_{STH} + t_{STS}$.

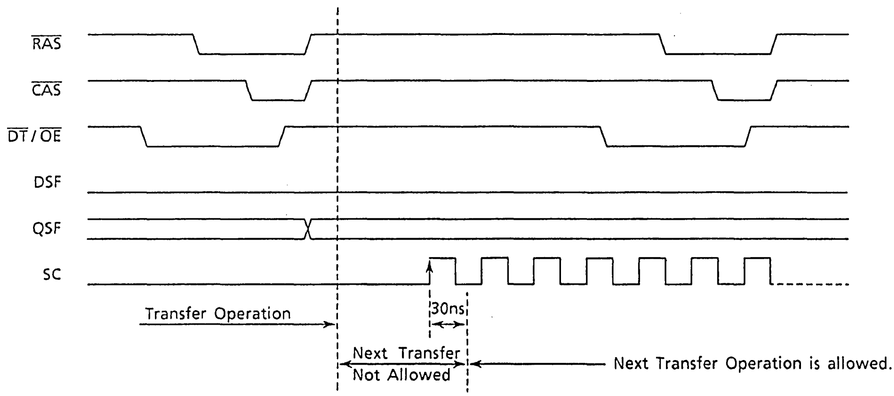
SPLIT READ TRANSFER CYCLE AFTER NORMAL READ TRANSFER CYCLE

A split read transfer may be performed following a normal read transfer provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (Refer to the illustration shown below).



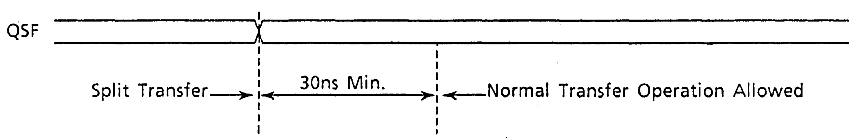
NORMAL READ TRANSFER CYCLE AFTER NORMAL READ TRANSFER CYCLE

Another read transfer may be performed following the read transfer provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (Refer to the illustration shown below).



NORMAL TRANSFER AFTER SPLIT READ TRANSFER

A normal transfer (read / write / pseudo write) may be performed following split read transfer operation provided that a 30ns minimum delay is satisfied after the QSF signal toggles.



POWER-UP

Power must be applied to the $\overline{\text{RAS}}$ and $\overline{\text{DT}}$ / $\overline{\text{OE}}$ input signals to pull them "high" before or at the same time as the V_{CC} supply is turned on. After power-up, a pause of 200 µseconds minimum is required with $\overline{\text{RAS}}$ and $\overline{\text{DT}}$/ $\overline{\text{OE}}$ held "high". After the pause, a minimum of 8 $\overline{\text{RAS}}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{\text{DT}}$ / $\overline{\text{OE}}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ initialization cycles are required instead of 8 $\overline{\text{RAS}}$ cycles.

INITIAL STATE AFTER POWER-UP

When power is achieved with $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{DT}}$/ $\overline{\text{OE}}$ and $\overline{\text{WB}}$ /$\overline{\text{WE}}$ held "high", the internal state of the TC524258B is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 µseconds pause followed by a minimum of 8 $\overline{\text{RAS}}$ cycles and 8 SC cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
QSF	High-Impedance
Color Register	all "0"
WM1 Register	Write Enable
TAP pointer	Invalid

SILICON GATE CMOS 131,072WORDSx8BITS MULTIPORT DRAM

target spec

DESCRIPTION

The TC528128B is a CMOS multiport memory equipped with a 131,072-words by 8-bits dynamic random access memory (RAM) port and a 256-words by 8-bits static serial access memory (SAM) port. The TC528128B supports three types of operations; Random access to and from the RAM port, high speed serial access to and from the SAM port and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally. In addition to the conventional multiport videoram operating modes, the TC528128B features the block write and flash write functions on the RAM port and a split register data transfer capability on the SAM port. The TC528128B is fabricated using Toshiba's CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

FEATURES

- Single power supply of 5V±10% with a built-in V_{BB} generator
- All inputs and outputs : TTL Compatible
- Organization
  RAM Port : 131,072 wordsX8bits
  SAM Port : 256 wordsX8bits
- RAM Port
  Fast Page Mode Read - Modify - Write
  $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh
  $\overline{RAS}$ only Refresh, Write per Bit
  Flash Write, Block Write
  512 refresh cycles / 8ms
- SAM Port
  High Speed Serial Read / Write Capability 256 Tap Locations
  Fully Static Register
- RAM - SAM Bidirectional Transfer
  Read / Write / Pseudo Write Transfer
  Real Time Read Transfer
  Split Read / Write Transfer
- Package
  TC528128BJ : SOJ40-P-400
  TC528128BZ : ZIP40-P-475

KEY PARAMETERS

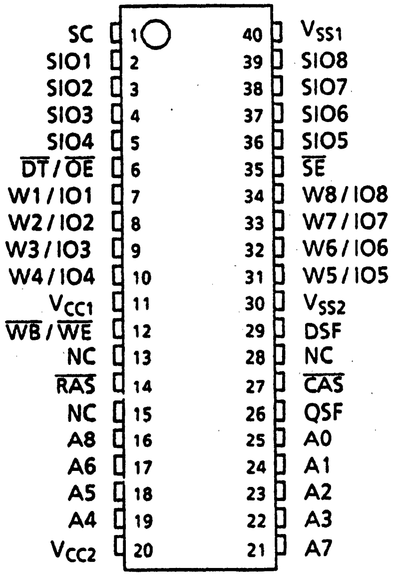
ITEM		TC528128B	
		—80	—10
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	80ns	100ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	25ns	25ns
t_{AA}	Column Address Access Time (Max.)	45ns	50ns
t_{RC}	Cycle Time (Min.)	150ns	180ns
t_{PC}	Page Mode Cycle Time (Min.)	50ns	55ns
t_{SCA}	Serial Access Time (Max.)	25ns	25ns
t_{SCC}	Serial Cycle Time (Min.)	30ns	30ns
I_{CC1}	RAM Operating Current (SAM : Standby)	90mA	75mA
I_{CC2A}	SAM Operating Current (RAM : Standby)	50mA	50mA
I_{CC2}	Standby Current	10mA	10mA

PIN NAME

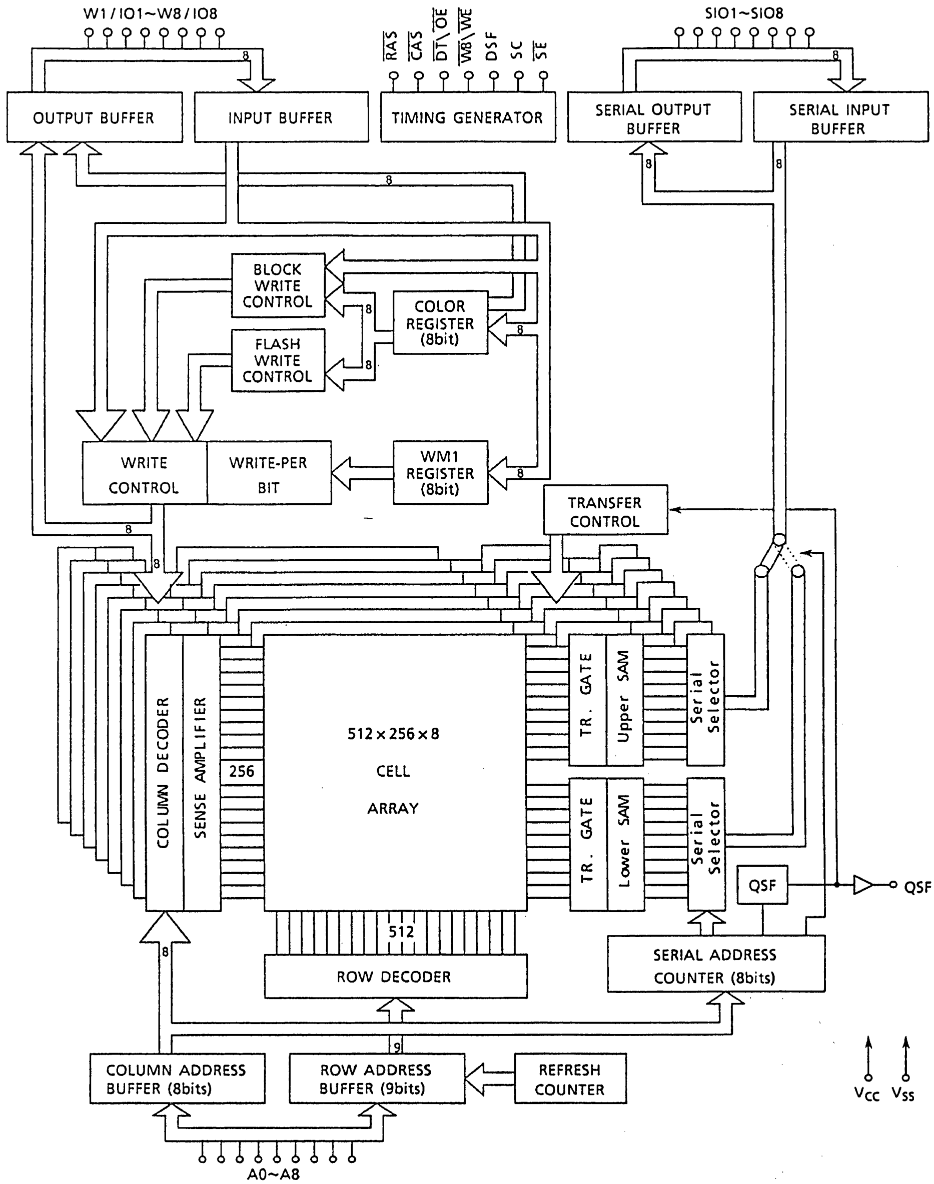
A0~A8	Address inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}/\overline{WE}$	Write per Bit/Write Enable
DSF	Special Function Control
Wl/IOl ~W4/IO8	Write Mask/Data IN, OUT
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIOl~SIO8	Serial Input/Output
QSF	Special Flag Output
V_{CC}/V_{SS}	Power(5V)/Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

TC528128BJ



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}, V_{OUT}	Input Output Voltage	— 1.0~7.0	V	1
V_{CC}	Power Supply Voltage	— 1.0~7.0	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	— 55~150	°C	1
T_{SOLDER}	Soldering Temperature • Time	260•10	°C•sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	6.5	V	2
V_{IL}	Input Low Voltage	—1.0	—	0.8	V	2

CAPACITANCE (V_{CC}=5V, f=1MHz, Ta=25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance	—	7	pF
C_{IO}	Input/Output Capacitance	—	9	
C_O	Output Capacitance (QSF)	—	9	

Note: This parameter is periodically sampled and is not 100% tested.

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

ITEM (RAM PORT)	SAM PORT	SYMBOL	-80		-10		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
OPERATING CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, $t_{RC} = t_{RC}$ min.)	Standby	I_{CC1}	—	90	—	75	mA	3, 4
	Active	I_{CC1A}	—	130	—	115	mA	3, 4
STANDBY CURRENT ($\overline{RAS}$, $\overline{CAS} = V_{IH}$)	Standby	I_{CC2}	—	10	—	10	mA	
	Active	I_{CC2A}	—	50	—	50	mA	3, 4
RAS ONLY REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min.)	Standby	I_{CC3}	—	90	—	75	mA	3, 4
	Active	I_{CC3A}	—	130	—	115	mA	3, 4
PAGE MODE CURRENT ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling, $t_{PC} = t_{RC}$ min.)	Standby	I_{CC4}	—	80	—	65	mA	3, 4
	Active	I_{CC4A}	—	120	—	105	mA	3, 4
CAS BEFORE RAS REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$, $t_{RC} = t_{RC}$ min.)	Standby	I_{CC5}	—	90	—	75	mA	3, 4
	Active	I_{CC5A}	—	130	—	115	mA	3, 4
DATA TRANSFER CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, $t_{RC} = t_{RC}$ min.)	Standby	I_{CC6}	—	110	—	95	mA	3, 4
	Active	I_{CC6A}	—	150	—	135	mA	3, 4
FLASH WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, $t_{RC} = t_{RC}$ min.)	Standby	I_{CC7}	—	100	—	75	mA	3, 4
	Active	I_{CC7A}	—	130	—	115	mA	3, 4
BLOCK WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, $t_{RC} = t_{RC}$ min.)	Standby	I_{CC8}	—	100	—	85	mA	3, 4
	Active	I_{CC8A}	—	140	—	125	mA	3, 4

ITEM	SYMBOL	MIN.	MAX	UNIT	NOTE
INPUT LEAKAGE CURRENT $0V \le V_{IN} \le 6.5V$, All other pins not under test=0V	$I_{I(L)}$	—10	10	µA	
OUTPUT LEAKAGE CURRENT $0V \le V_{OUT} \le 5.5V$, OutputDisable	$I_{O(L)}$	—10	10	µA	
OUTPUT "H" LEVEL VOLTAGE I_{OUT} = - 2mA	V_{OH}	2.4	—	V	
OUTPUT "L" LEVEL VOLTAGE I_{OUT} = 2mA	V_{OL}	—	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes: 5, 6, 7)

SYMBOL	PARAMETER	-80		-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX		
t_{RC}	Random Read or Write Cycle Time	150		180		ns	
t_{RMW}	Read-Modify-Write Cycle Time	195		235			
t_{PC}	Fast Page Mode Cycle Time	50		55			
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	90		100			
t_{RAC}	Access Time from $\overline{RAS}$		80		100		8,14
t_{AA}	Access Time from Column Address		45		50		8,14
t_{CAC}	Access Time from $\overline{CAS}$		25		25		8,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		45		50		8,15
t_{OFF}	Output Buffer Turn-Off Delay	0	20	0	20		10
t_T	Transition Time (Rise and Fall)	3	35	3	35		7
t_{RP}	$\overline{RAS}$ Precharge Time	60		70			
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10000	100	10000		
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode Only)	80	100000	100	100000		
t_{RSH}	$\overline{RAS}$ Hold Time	25		25			
t_{CSH}	$\overline{CAS}$ Hold Time	80		100			
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10000	25	10000		
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	55	20	75		14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	50		14
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45		50			
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10			
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10			
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10			
t_{ASR}	Row Address Set-Up Time	0		0			
t_{RAH}	Row Address Hold Time	10		10			
t_{ASC}	Column Address Set-Up Time	0		0			
t_{CAH}	Column Address Hold Time	15		15			
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55		70			
t_{RCS}	Read Command Set-Up Time	0		0			
t_{RCH}	Read Command Hold Time	0		0			11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0			11
t_{WCH}	Write Command Hold Time	15		15			
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55		70			
t_{WP}	Write Command Pulse Width	15		15			
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25			
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25			

SYMBOL	PARAMETER	-80		-10		UNIT	NOTE
		MIN.	MAX	MIN.	MAX		
t_{DS}	Data Set-Up Time	0		0			12
t_{DH}	Data Hold Time	15		15			12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55		70			
t_{WCS}	Write Command Set-Up Time	0		0			13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100		130			13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65		80			13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45		55			13
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0			
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0		ns	
t_{OEA}	Access Time from $\overline{OE}$		20		25		8
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	0	10	0	20		10
t_{OED}	$\overline{OE}$ to Data Delay Time	10		20			
t_{OEH}	$\overline{OE}$ Command Hold Time	10		20			
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15		15			
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0			
t_{REF}	Refresh Period		8		8	ms	
t_{WSR}	$\overline{WB}$ Set-Up Time	0		0			
t_{RWH}	$\overline{WB}$ Hold Time	15		15			
t_{FSR}	DSF Set-Up Time referenced to $\overline{RAS}$	0		0			
t_{RFH}	DSF Hold Time referenced to $\overline{RAS}$(1)	15		15			
t_{FHR}	DSF Hold Time referenced to $\overline{RAS}$(2)	55		70			
t_{FSC}	DSF Set-Up Time referenced to $\overline{CAS}$	0		0			
t_{CFH}	DSF Hold Time referenced to $\overline{CAS}$	15		15			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0		0			
t_{MH}	Write-Per-Bit Mask Data Hold Time	15		15			
t_{THS}	$\overline{DT}$ High Set-Up Time	0		0		ns	
t_{THH}	$\overline{DT}$ High Hold Time	15		15			
t_{TLS}	$\overline{DT}$ Low Set-Up Time	0		0			
t_{TLH}	$\overline{DT}$ Low Hold Time	15	10000	15	10000		
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	65	10000	80	10000		
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	30		30			
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	25		25			

SYMBOL	PARAMETER	-80 MIN.	-80 MAX.	-10 MIN.	-10 MAX.	UNIT	NOTE
t_{ESR}	$\overline{SE}$ Set-Up Time referenced to $\overline{RAS}$	0		0		ns	
t_{REH}	$\overline{SE}$ Hold Time referenced to $\overline{RAS}$	15		15			
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	60		70			
t_{TP}	$\overline{DT}$ Precharge Time	20		30			
t_{RSD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	80		100			
t_{ASD}	Column Address to First SC Delay Time (Read Transfer)	45		50			
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	25		25			
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		5			
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	15		15			
t_{SRS}	Last SC to $\overline{RAS}$ Set-Up Time (Serial Input)	30		30			
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	25		25			
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	50		50			
t_{SDZ}	Serial Output Buffer Turn-off Delay from $\overline{RAS}$ (Pseudo Write Transfer)	10	50	10	50		10
t_{SCC}	SC Cycle Time	30		30			
t_{SC}	SC Pulse Width (SC High Time)	10		10			
t_{SCP}	SC Precharge Time (SC Low Time)	10		10			
t_{SCA}	Access Time from SC		25		25		9
t_{SOH}	Serial Output Hold Time from SC	5		5			
t_{SDS}	Serial Input Set-Up Time	0		0			
t_{SDH}	Serial Input Hold Time	15		15			
t_{SEA}	Access Time from $\overline{SE}$		25		25		9
t_{SE}	$\overline{SE}$ Pulse Width	25		25			
t_{SEP}	$\overline{SE}$ Precharge Time	25		25			
t_{SEZ}	Serial Output Buffer Turn-off Delay from $\overline{SE}$	0	20	0	20		10
t_{SZE}	Serial Input to SE Delay Time	0		0			
t_{SZS}	Serial Input to First SC Delay Time	0		0			
t_{SWS}	Serial Write Enable Set-Up Time	0		0			
t_{SWH}	Serial Write Enable Hold Time	15		15			
t_{SWIS}	Serial Write Disable Set-Up Time	0		0			
t_{SWIH}	Serial Write Disable Hold Time	15		15			
t_{STS}	Split Transfer Set-Up Time	30		30			
t_{STH}	Split Transfer Hold Time	30		30			
t_{SQD}	SC-QSF Delay Time		25		25		
t_{TQD}	$\overline{DT}$-QSF Delay Time		25		25		
t_{CQD}	$\overline{CAS}$-QSF Delay Time		35		35		
t_{RQD}	$\overline{RAS}$-QSF Delay Time		75		90		

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltage are referenced to V_{SS}.

3. These parameters depend on cycle rate.

4. These parameters depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}/\overline{OE}$ "high") and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T = 5ns.

7. $V_{IH\,(min.)}$ and $V_{IL\,(max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. RAM port outputs are measured with a load equivalent to 1 TTL load and 100pF.
   D_{OUT} reference levels : V_{OH} / V_{OL} = 2.0V / 0.8V.

9. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
   D_{OUT} reference levels : V_{OH} / V_{OL} = 2.0V / 0.8V.

10. $t_{OFF\,(max.)}$, $t_{OEZ\,(max.)}$, $t_{SDZ\,(max.)}$ and $t_{SEZ\,(max.)}$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must he satisfied for a read cycles.

12. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}$ / $\overline{WE}$ leading edge in $\overline{OE}$-controlled write cycles and read-modify-write cycles.

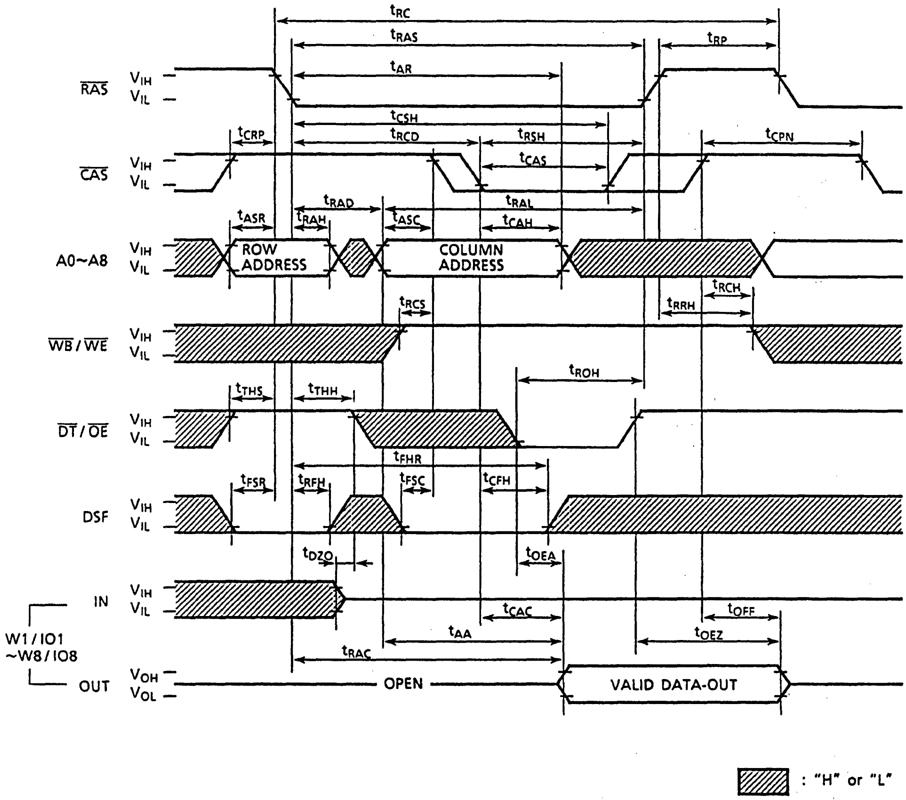
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS\,(min.)}$, the cycle is an early write cycles and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geq t_{RWD\,(min.)}$, $t_{CWD} \geq t_{CWD\,(min.)}$ and $t_{AWD} \geq t_{AWD\,(min.)}$ the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the $t_{RCD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can he met.
    $t_{RCD\,(max.)}$ is specified as a reference point only : If t_{RCD} is greater than the specified $t_{RCD\,(max.)}$ limit, then access time is controlled by t_{CAC}.

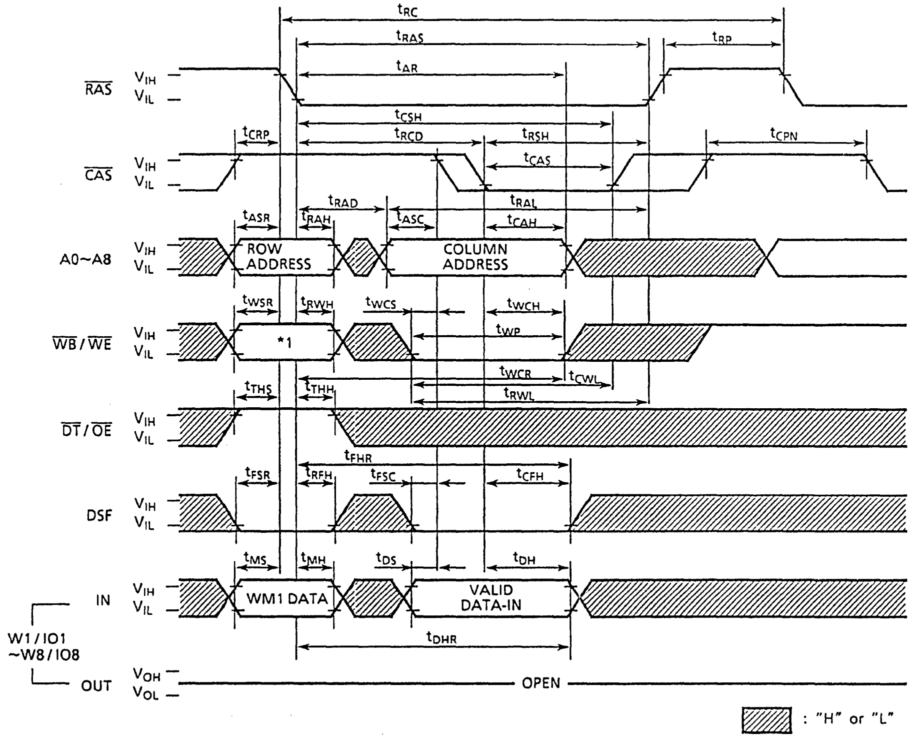
15. Operation within the $t_{RAD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can be met. $t_{RAD\,(max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\,(max.)}$ limit, then access time is controlled by t_{AA}.

TIMING WAVEFORM

READ CYCLE



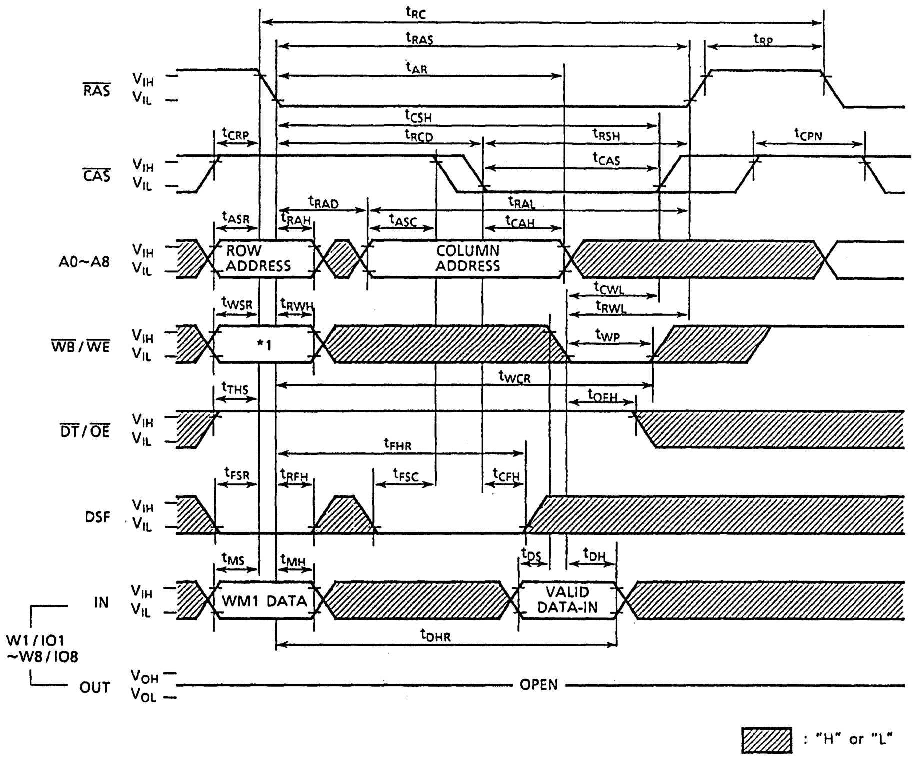
WRITE CYCLE (EARLY WRITE)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data 0: Write Disable
1: Write Enable

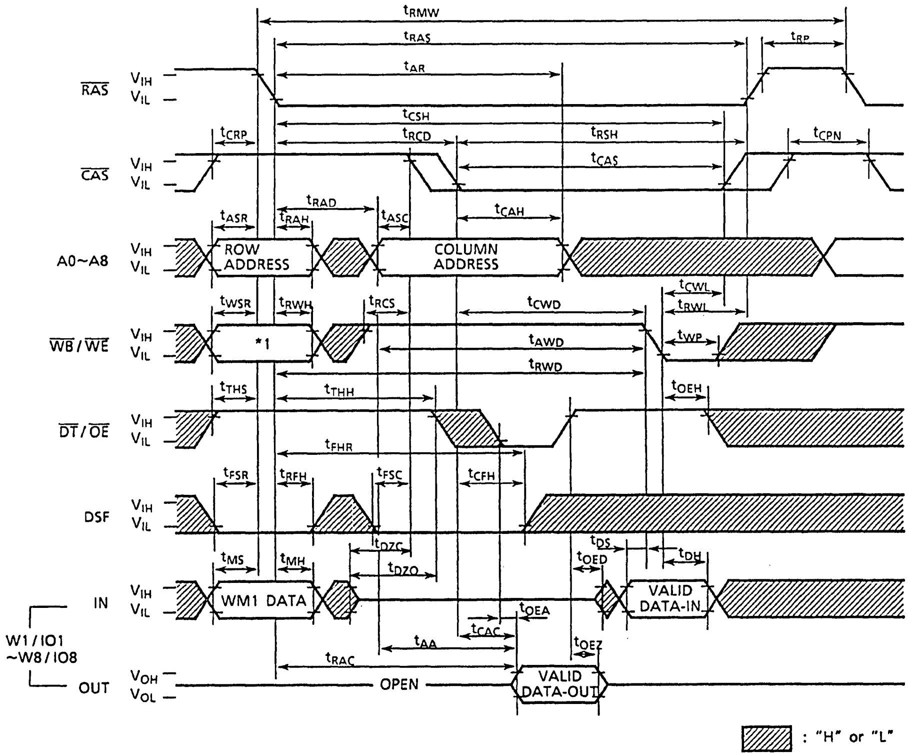
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data 0: Write Disable
1: Write Enable

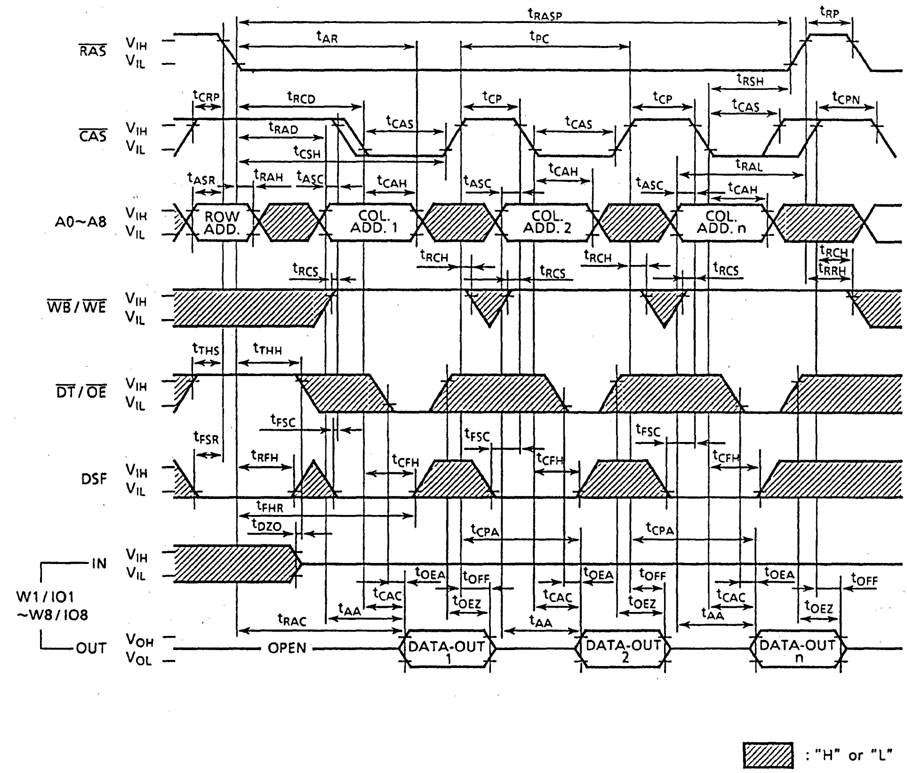
READ-MODIFY-WRITE CYCLE



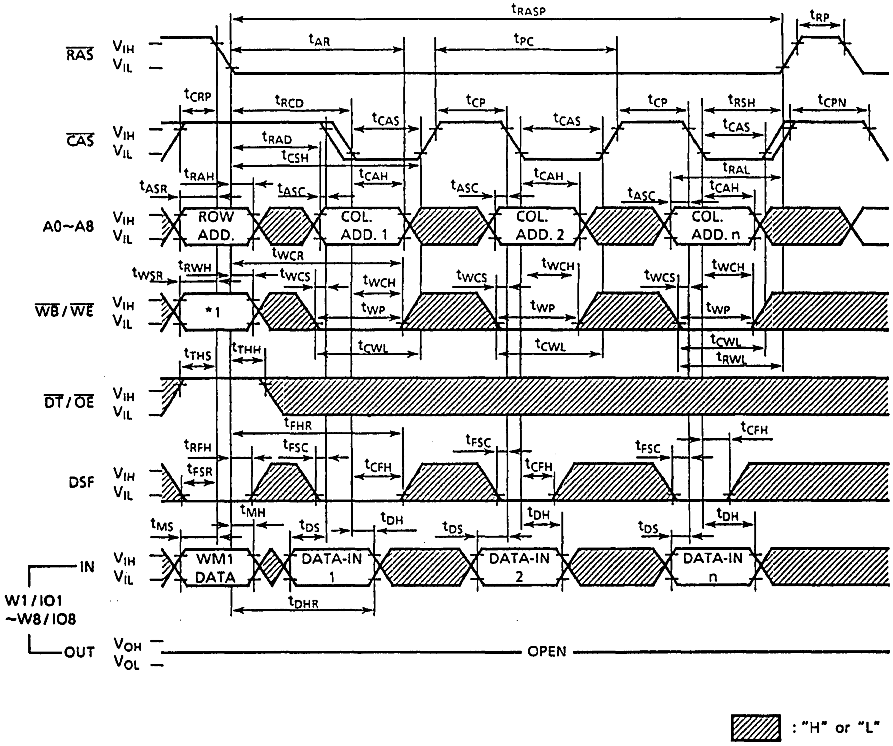
*1 $\overline{WB}/\overline{WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data 0: Write Disable
1: Write Enable

FAST PAGE MODE READ CYCLE



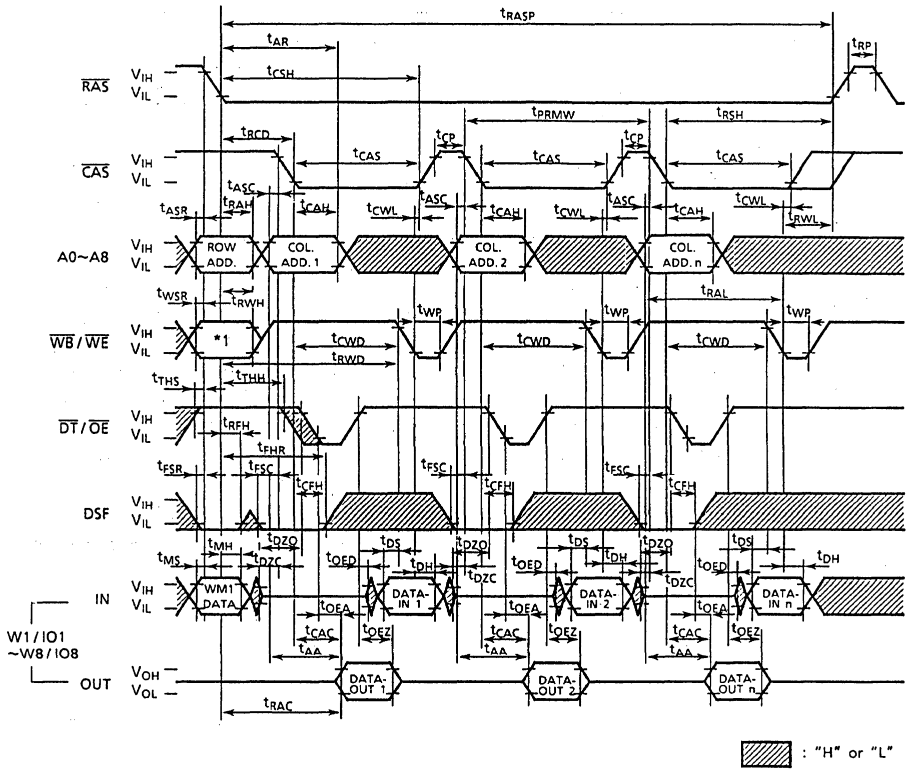
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data 0: Write Disable
1: Write Enable

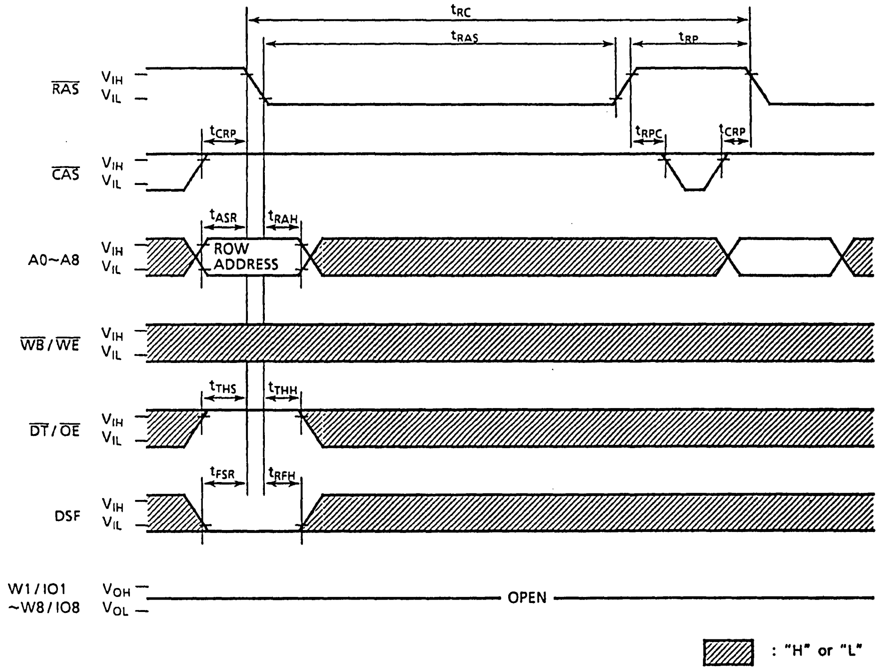
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



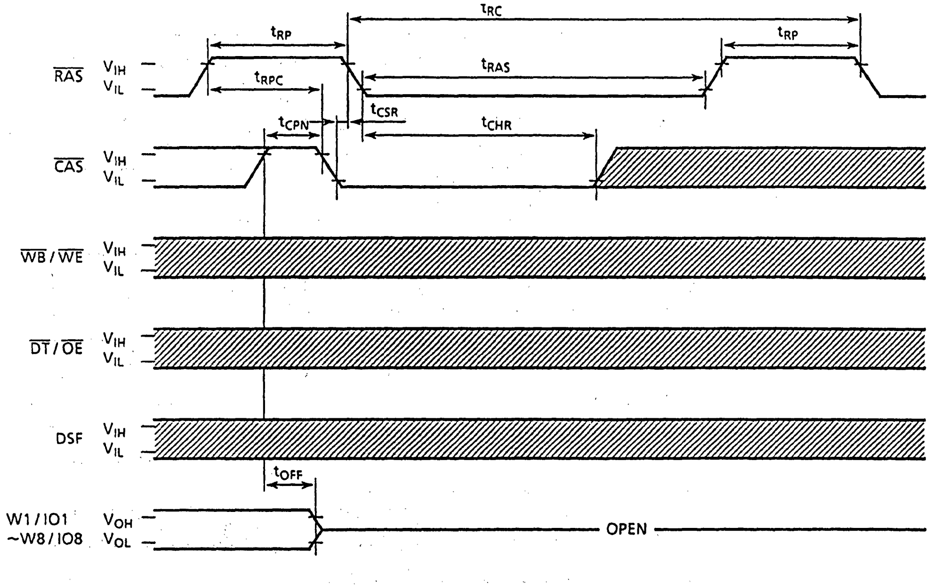
*1 $\overline{WB}/\overline{WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data 0: Write Disable
1: Write Enable

RAS ONLY REFRESH CYCLE



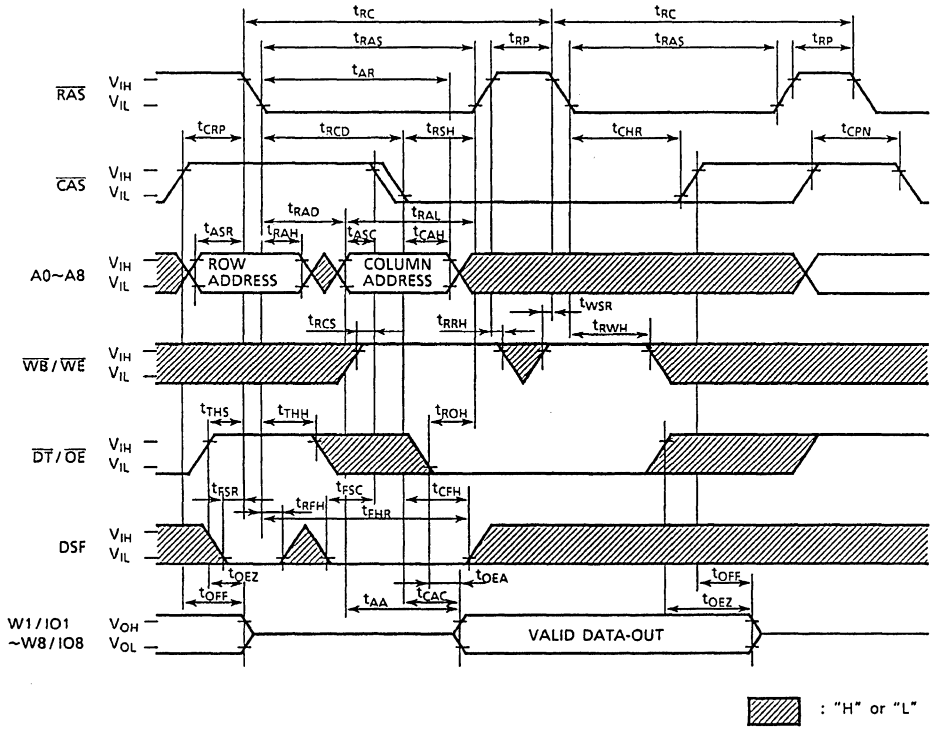
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



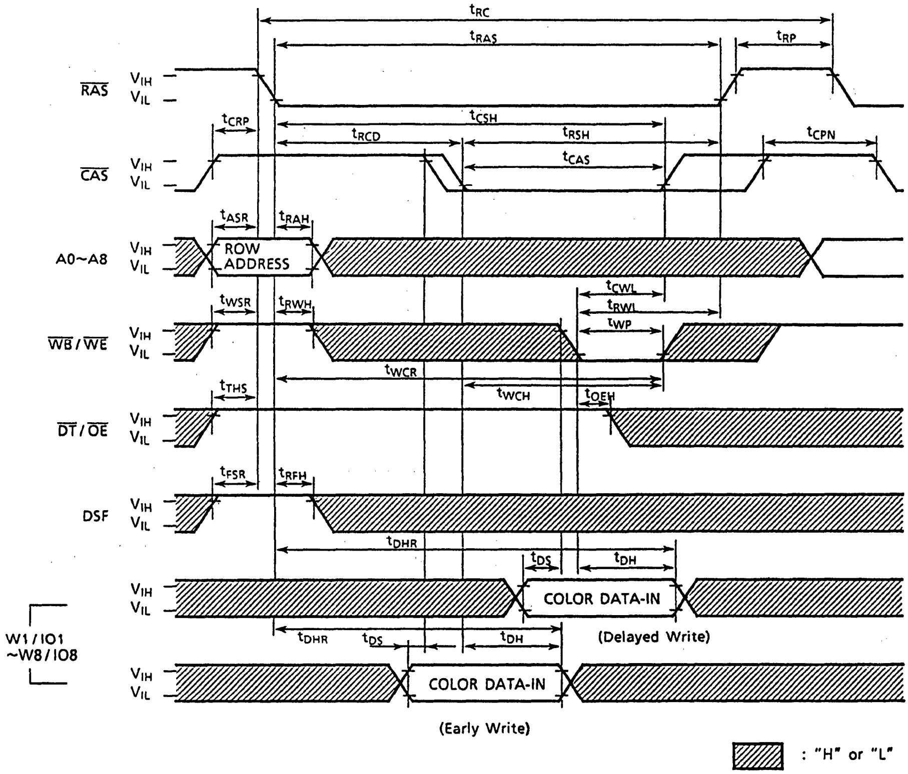
Note : A0 – A8 = Don't Care ("H" or "L")

: "H" or "L"

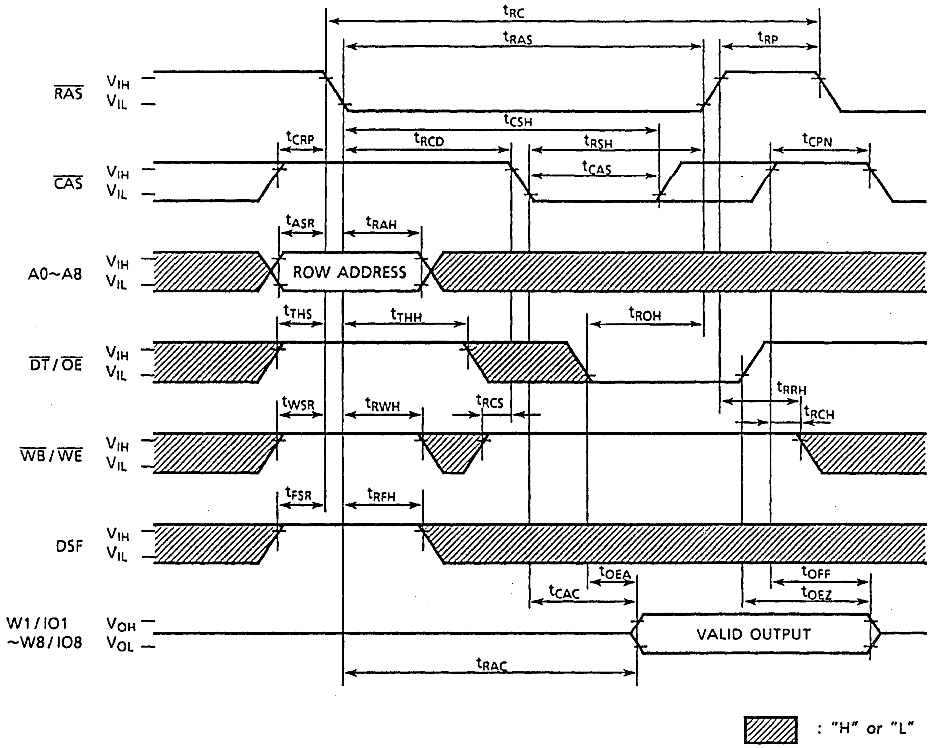
HIDDEN REFRESH CYCLE



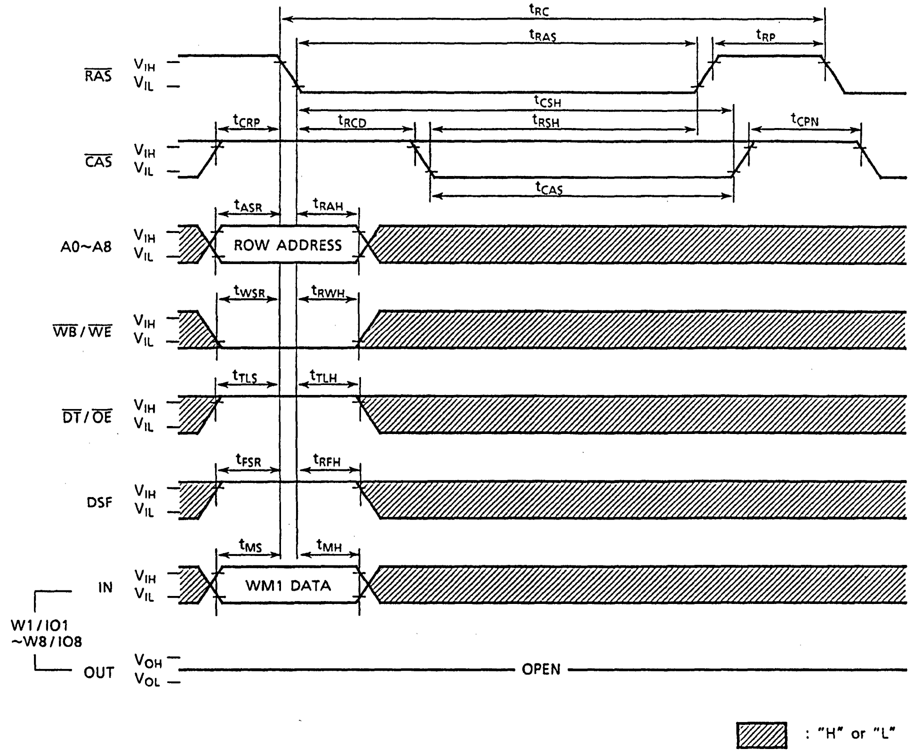
LOAD COLOR REGISTER CYCLE



READ COLOR REGISTER CYCLE

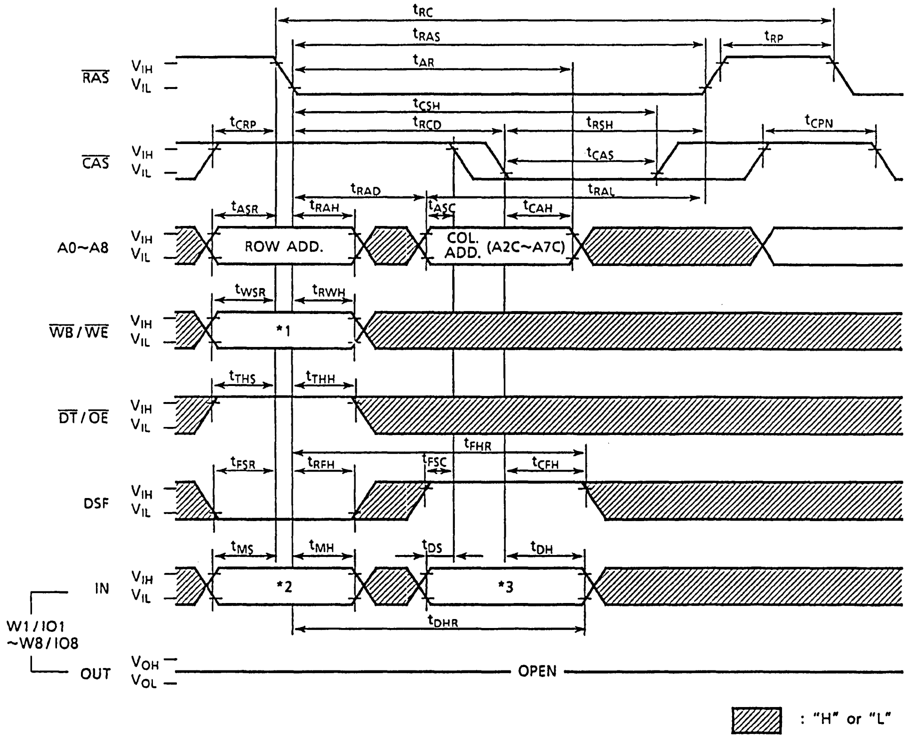


FLASH WRITE CYCLE



WM1	Cycle
0	Flash Write Disable
1	Flash Write Enable

BLOCK WRITE CYCLE



*1 $\overline{WB}/\overline{WE}$	*2 W1/IO1~W8/IO8	Cycle
0	WM1 data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

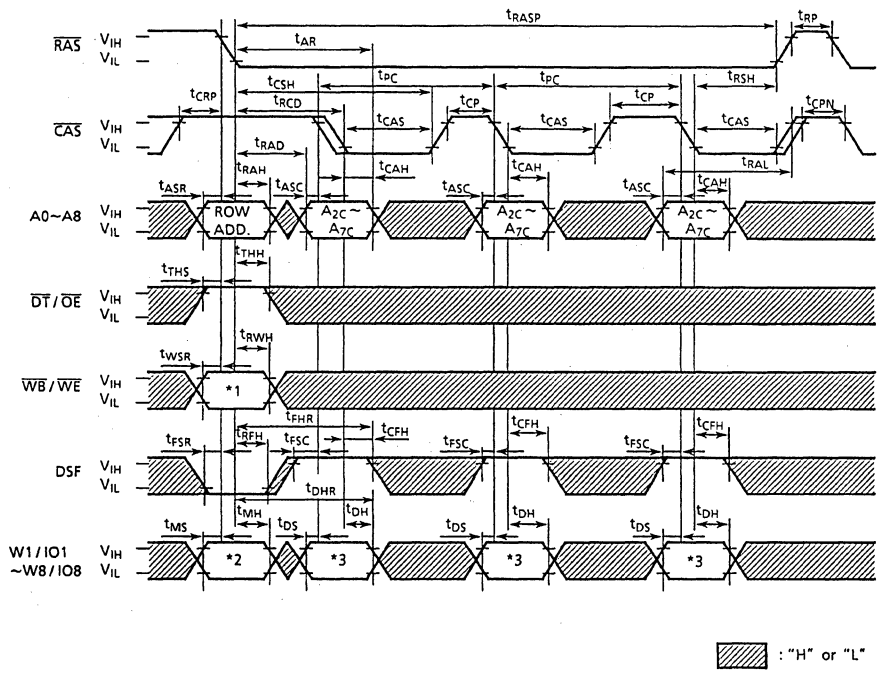
WM1 data 0: Write Disable
1: Write Enable

*3 COLUMN SELECT

W1/IO1 - Column 0 ($A_{1C} = 0$, $A_{0C} = 0$
W2/IO2 - Column 1 ($A_{1C} = 0$, $A_{0C} = 1$
W3/IO3 - Column 2 ($A_{1C} = 1$, $A_{0C} = 0$
W4/IO4 - Column 3 ($A_{1C} = 1$, $A_{0C} = 1$

Wn/IOn
= 0 : Disable
= 1 :

PAGE MODE BLOCK WRITE CYCLE



*1 $\overline{WB}/\overline{WE}$	*2 W1/IO1~W8/IO8	Cycle
0	WM1 data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

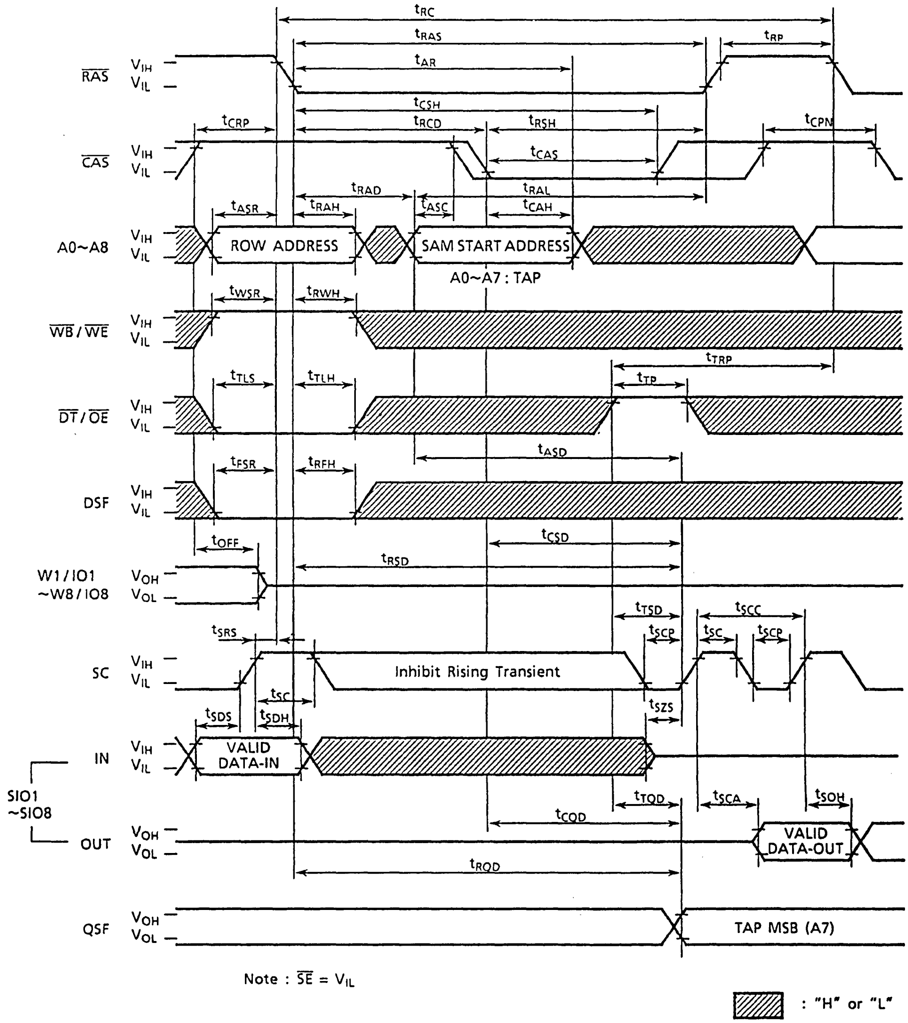
WM1 data	0: Write Disable
	1: Write Enable

*3 COLUMN SELECT

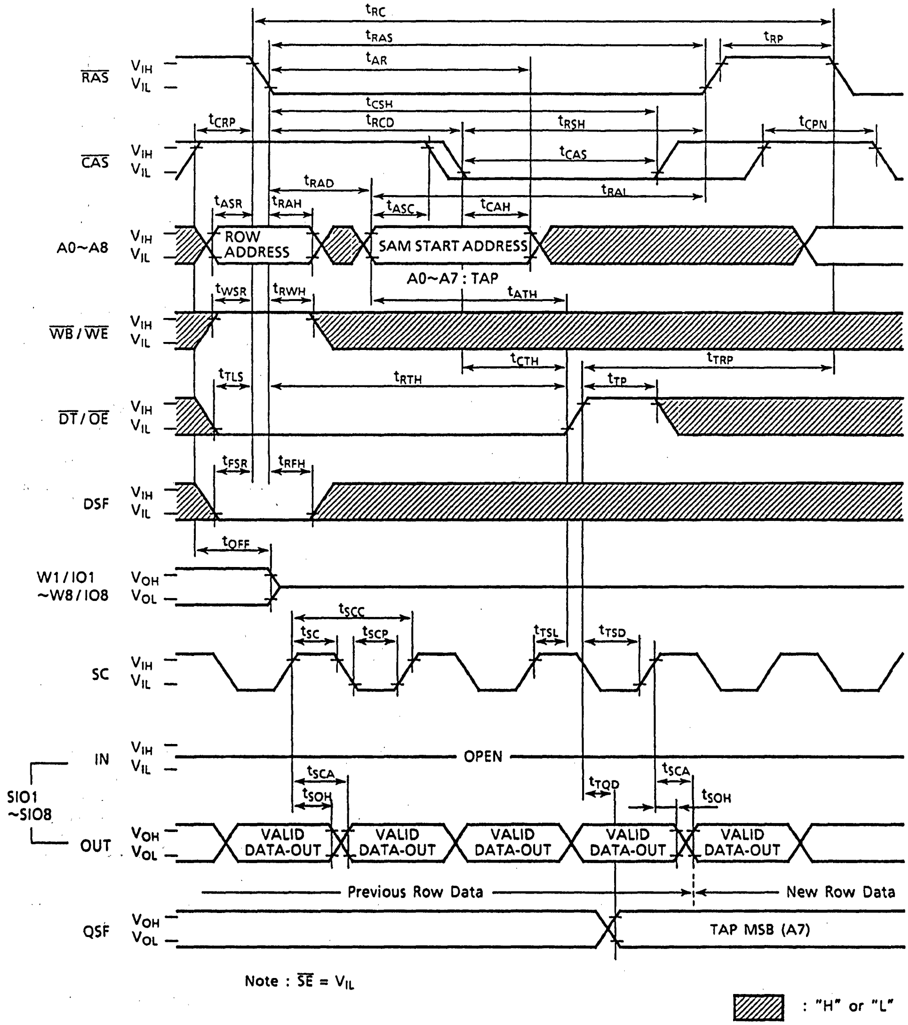
W1/IO1 - Colume 0 ($A_{1C} = 0$, $A_{0C} = 0$
W2/IO2 - Column 1 ($A_{1C} = 0$, $A_{0C} = 1$
W3/IO3 - Column 2 ($A_{1C} = 1$, $A_{0C} = 0$
W4/IO4 - Column 3 ($A_{1C} = 1$, $A_{0C} = 1$

Wn/IOn = 0 : Disable
= 1 :

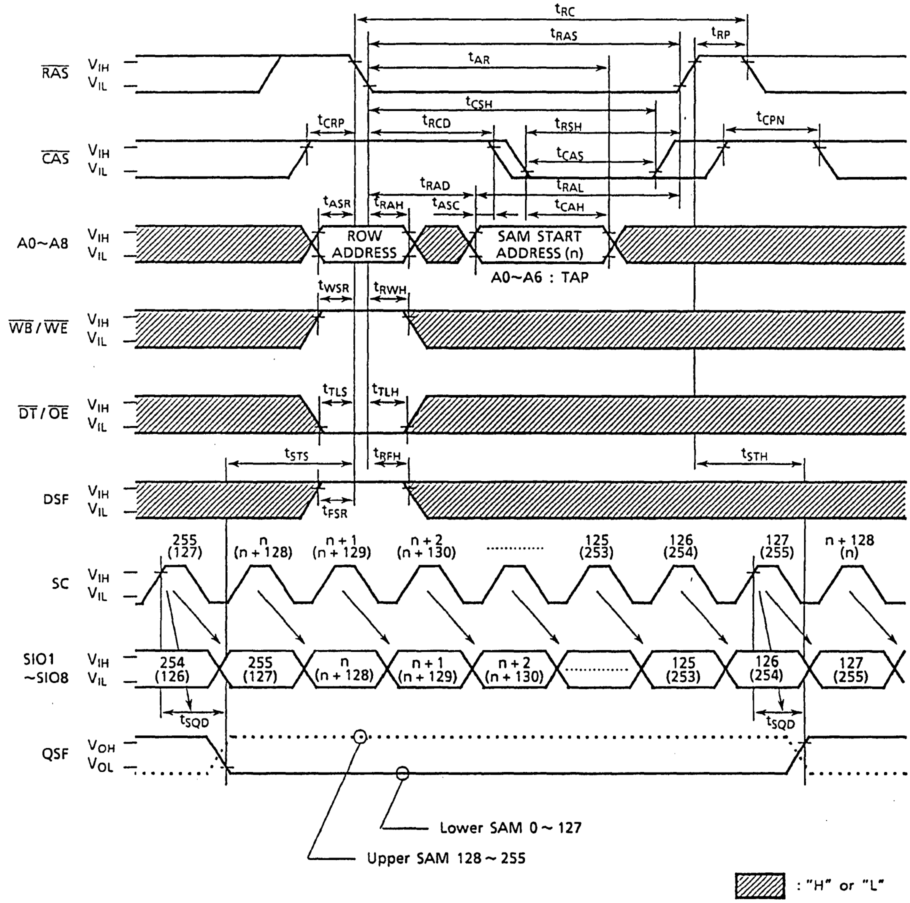
READ TRANSFER CYCLE (Previous Transfer is WRITE TRANSFER CYCLE)



REAL TIME READ TRANSFER CYCLE

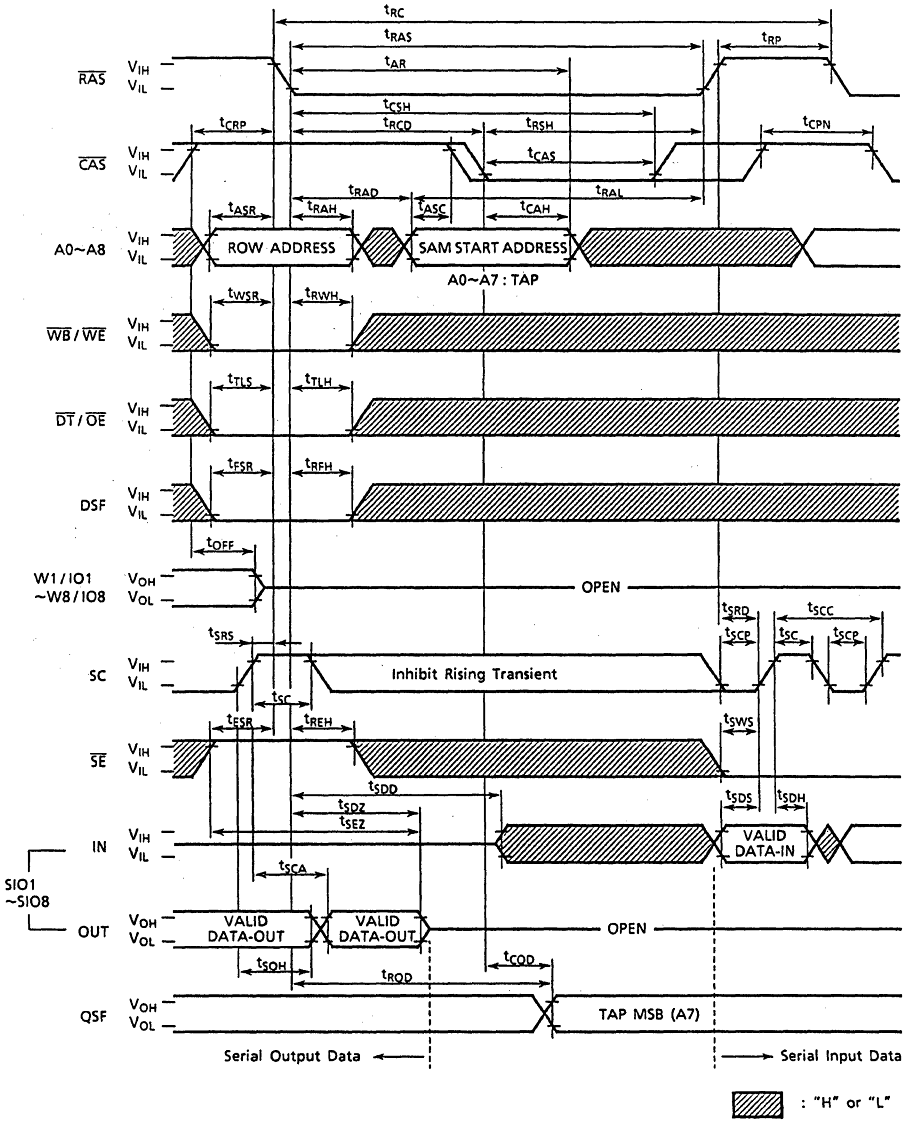


SPLIT READ TRANSFER CYCLE

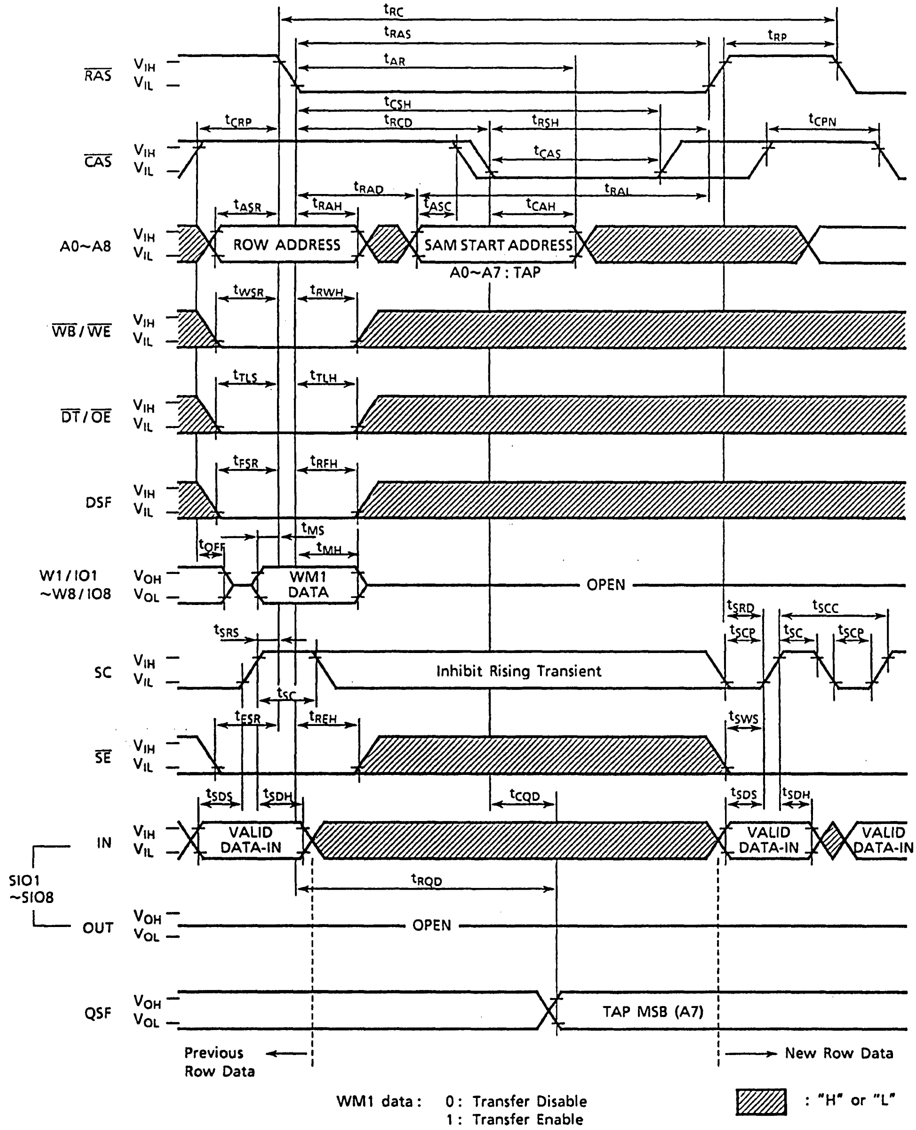


Note : $\overline{SE} = V_{IL}$

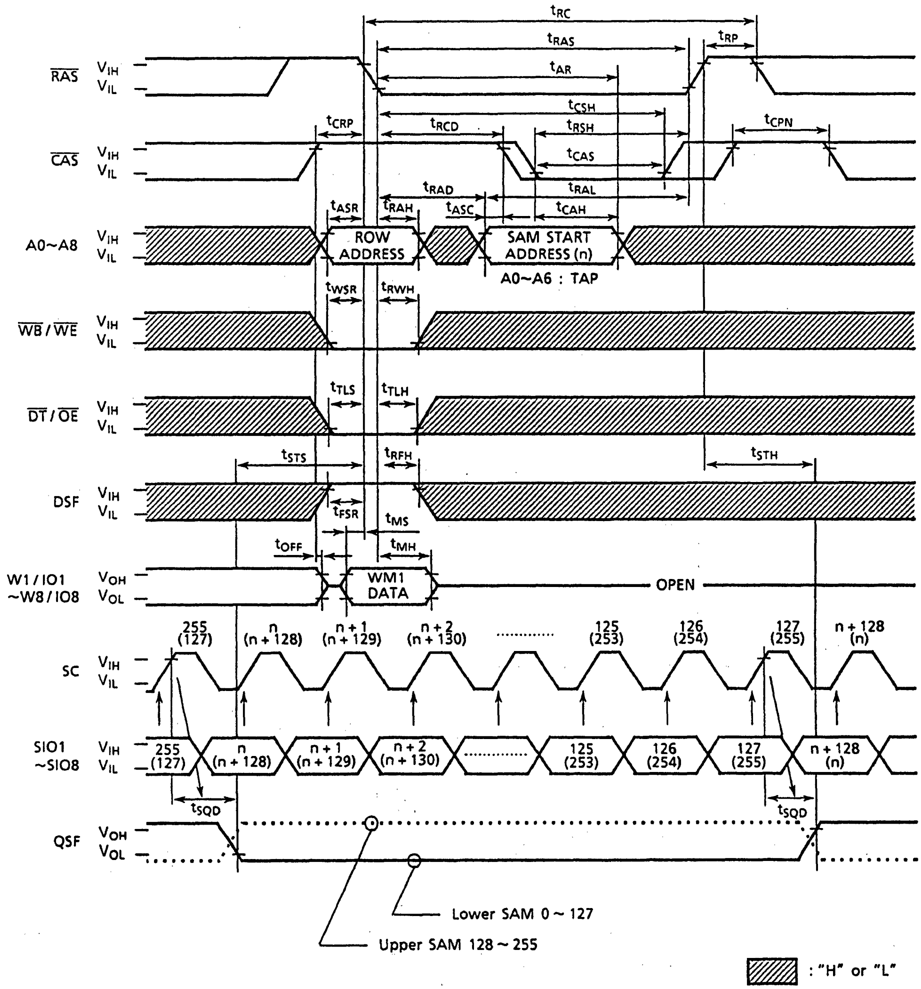
PSEUDO WRITE TRANSFER CYCLE



WRITE TRANSFER CYCLE

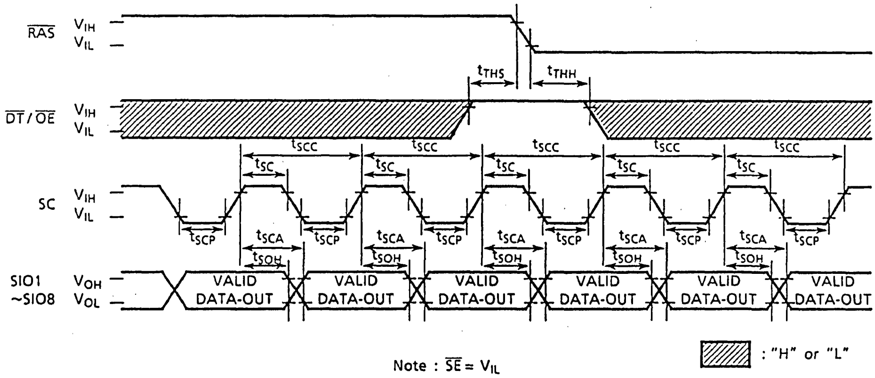


SPLIT WRITE TRANSFER CYCLE

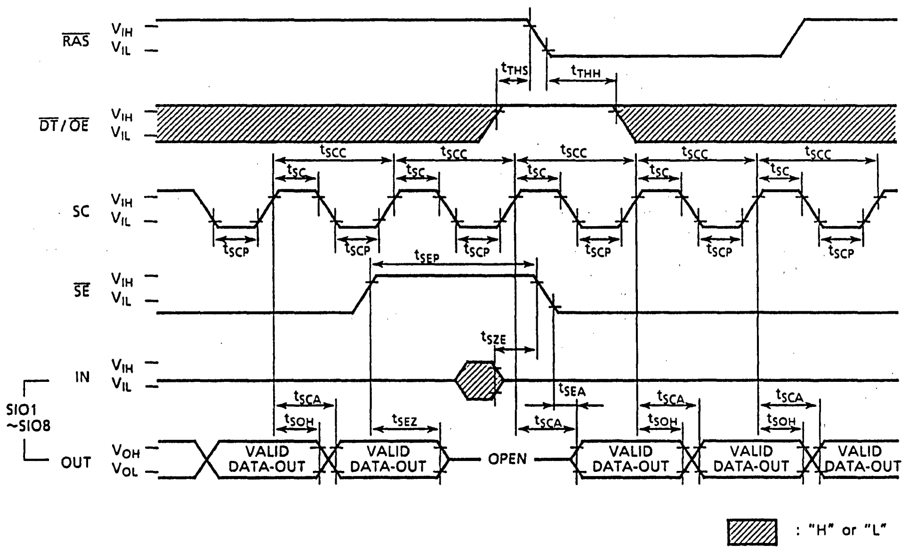


Note : $\overline{SE}$ = V_{IL}

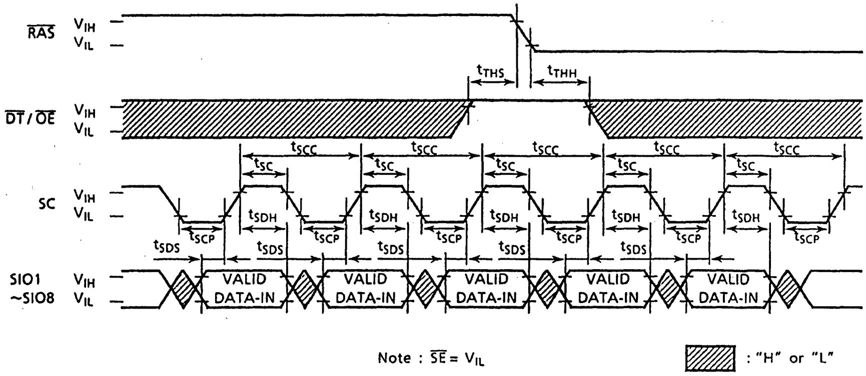
SERIAL READ CYCLE ($\overline{SE}$=V_{IL})



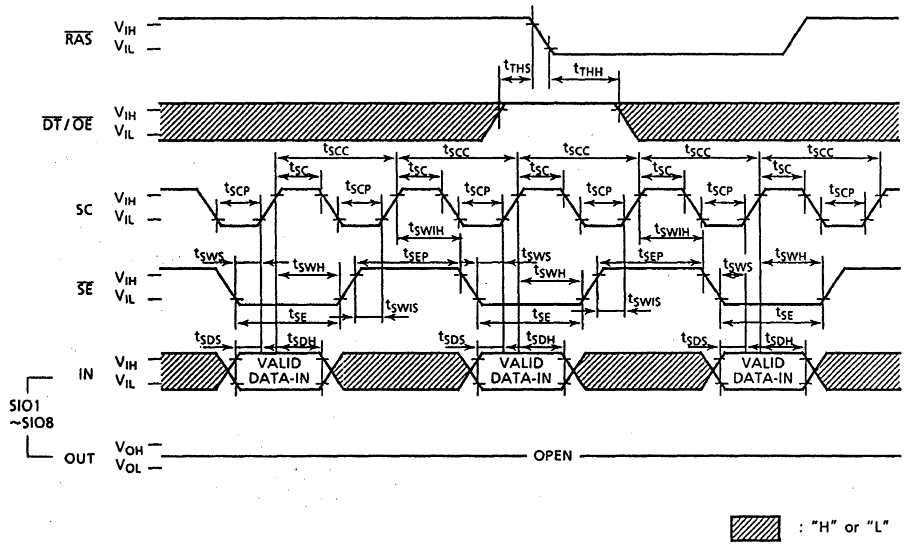
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



SERIAL WRITE CYCLE ($\overline{SE}$=V_{IL})



SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



PIN FUNCTION

ADDRESS INPUTS : A_0 ~ A_8

The 17 address bits required to decode 8 bits of the 1,048,576 cell locations within the dynamic RAM memory array of the TC528128B are multiplexed onto 9 address input pins (A_0~A_8). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{\text{RAS}}$) and the following eight column address bits are latched on the falling edge of the column address strobe ($\overline{\text{CAS}}$).

ROW ADDRESS STROBE : $\overline{\text{RAS}}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{\text{RAS}}$. $\overline{\text{RAS}}$ is the control input that latches the row address bits and the states of $\overline{\text{CAS}}$, $\overline{\text{DT}}/\overline{\text{OE}}$, $\overline{\text{WB}}/\overline{\text{WE}}$, $\overline{\text{SE}}$ and DSF to invoke the various random access and data transfer operating modes shown in Table 2. $\overline{\text{RAS}}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the $\overline{\text{RAS}}$ control is held "high".

COLUMN ADDRESS STROBE : $\overline{\text{CAS}}$

$\overline{\text{CAS}}$ is the control input that latches the column address bits and the state of the special function input DSF to select, in conjunction with the $\overline{\text{RAS}}$ control, either read / write operations or the special block write feature on the RAM port when the DSF input is held "low" at the falling edge of $\overline{\text{RAS}}$. Refer to the operation truth table shown in Table 1. $\overline{\text{CAS}}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. $\overline{\text{CAS}}$ also acts as an output enable for the output buffers on the RAM port.

DATA TRANSFER/OUTPUT ENABLE : $\overline{\text{DT}}/\overline{\text{OE}}$

The $\overline{\text{DT}}/\overline{\text{OE}}$ input is a multifunction pin. When $\overline{\text{DT}}/\overline{\text{OE}}$ is "high" at the falling edge of $\overline{\text{RAS}}$, RAM port operations are performed and $\overline{\text{DT}}/\overline{\text{OE}}$ is used as an output enable control. When the $\overline{\text{DT}}/\overline{\text{OE}}$ is "low" at the falling edge of $\overline{\text{RAS}}$, a data transfer operation is started between the RAM port and the SAM port.

WRITE PER BIT/WRITE ENABLE : $\overline{WB}/\overline{WE}$

The $\overline{WB}/\overline{WE}$ input is also a multifunction pin. When $\overline{WB}/\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, during RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, during RAM port operations, the write-per-hit function is enabled. The $\overline{WB}/\overline{WE}$ input also determines the direction of data transfer between the RAM array and the serial register (SAM). When $\overline{WB}/\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer). When $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (masked-write transfer).

WRITE MASK DATA/DATA INPUT AND OUTPUT : W_1/IO_1~W_8/IO_8

When the write-per-bit function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register (WM1) at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic "1". Writing is inhibited on data lines where the write-mask data is a logic "0". The write-mask data is valid for only one cycle. Data is written into the RAM port during a write or read-modify-write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs late. During an early-write cycle, the outputs are in the high impedance state. Data is read out of the RAM port during a read or read-modify-write cycle. The output data becomes valid on the W_i/IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and column address are satisfied and will remain valid as long as $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ are kept "low". The outputs will return to the high-impedance state at the rising edge of either $\overline{CAS}$ or $\overline{DT}/\overline{OE}$, whichever occurs first.

SERIAL CLOCK : SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 8-bits serial pointer (7-bits in split register mode) which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the starting location which is determined by the column address in the read transfer cycle. When the pointer reaches the most significant address location (decimal 255), the next SC clock will place it at the least significant address location (decimal 0). The serial clock SC must he held at a constant V_{IH} or V_{IL} level during read / pseudo write / write transfer operations and should not he clocked while the SAM port is in the standby mode to prevent the SAM pointer from being incremented.

SERIAL ENABLE : $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "high".

SPECIAL FUNCTION CONTROL INPUT : DSF

The DSF input is latched at the falling edge of $\overline{RAS}$ and $\overline{CAS}$ and allows for the selection of various random port and data transfer operating modes. In addition to the conventional multiport DRAM, the special features consisting of flash write, block write, load color register and split read / write transfer can be invoked.

SPECIAL FUNCTION OUTPUT : QSF

QSF is an output signal which, during split register mode, indicates which half of the split SAM is being accessed. QSF "low" indicates that the lower split SAM (Bit 0~127) is being accessed and QSF "high" indicates that the upper split SAM (Bit 128~255) is being accessed. QSF is monitored so that after it toggles and after allowing for a delay of t_{STS}, split read / write transfer operation can be performed on the non-active split SAM.

SERIAL INPUT/OUTPUT : SIO1~SIO8

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode. During subsequent write transfer cycle, the SAM remains in the input mode.

OPERATION MODE

The RAM port and data transfer operating of the TC524258B are determined by the state of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$ and DSF at the falling edge of $\overline{RAS}$ and by the state of DSF at the falling edge of $\overline{CAS}$. The Table 1 and the Table 2 show the operation truth table and the functional truth table for a listing of all available RAM port and transfer operation, respectively.

Table 1. Operaton Truth Table

$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	DSF ($\overline{CAS}$ falling edge) 0 / DSF ($\overline{RAS}$ falling edge) 0	0 / 1	1 / 0	1 / 1
0	*	*	*	$\overline{CAS}$ before $\overline{RAS}$ Refresh			
1	0	0	0	Masked Write Transfer	Split Write Transfer with Mask	Masked Write Transfer	Split Write Transfer with Mask
1	0	0	1	Pseudo Write Transfer		Pseudo Write Transfer	
1	0	1	*	Read Transfer	Split Read Transfer	Read Transfer	Split Read Transfer
1	1	0	*	Read/Write per Bit	Masked Flash Write	Masked Block Write	Masked Flash Write
1	1	1	*	Read/Write	Load Color	Block Write	Load Color

2. Functional Truth Table

Function	$\overline{RAS}$ ↓					$\overline{CAS}$ ↓	Address		W/IO			Write Mask	Register	
	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DSF	$\overline{SE}$	DSF	$\overline{RAS}$ ↓	$\overline{CAS}$ ↓	$\overline{RAS}$ ↓	$\overline{CAS}$ ↓	$\overline{CAS}$ ↓ $\overline{WE}$ ↓		WM1	Color
$\overline{CAS}$ before $\overline{RAS}$ Refresh	0	*	*	*	*	-	*	-	*	-	-	-	-	-
Masked Write Transfer	1	0	0	0	0	*	Row	TAP	WM1	*	*	WM1	Load use	-
Pseudo Write Transfer	1	0	0	0	1	*	Row	TAP	*	*	*	-	-	-
Split Write Transfer	1	0	0	1	*	*	Row	TAP	WM1	-	*	WM1	Load use	-
Read Transfer	1	0	1	0	*	*	Row	TAP	*	*	*	-	-	-
Split Read Transfer	1	0	1	1	*	*	Row	TAP	*	*	*	-	-	-
Write per Bit	1	1	0	0	*	0	Row	Column	WM1	-	DIN	WM1	Load use	-
Masked Block Write	1	1	0	0	*	1	Row	Column A2C-7C	WM1	Column Select	-	WM1	Load use	use
Masked Flash Write	1	1	0	1	*	*	Row	*	WM1	-	*	WM1	Load use	use
Read Write	1	1	1	0	*	0	Row	Column	*	-	DIN	-	-	-
Block Write	1	1	1	0	*	1	Row	Column A2C-7C	*	Column Select	-	-	-	use
Load Color	1	1	1	1	*	*	Row	*	*	-	Color	-	-	Load

* : "O" or "1" , TAP : SAM start address , : not used

If the special function control input (DSF) is in the "low" state at the falling edges of $\overline{RAS}$ and $\overline{CAS}$, only the conventional multiport DRAM operating features can be invoked: $\overline{CAS}$-before-$\overline{RAS}$ refresh, write transfer, pseudo-write transfer, read transfer and read write modes. If the DSF input is "high" at the falling edge of $\overline{RAS}$, special features such as split write transfer, split read transfer, flash write and load color register can be invoked. If the DSF input is "low" at the falling edge of $\overline{RAS}$ and "high" at the falling edge of $\overline{CAS}$, the block write special feature can be invoked.

RAM PORT OPERATION

FAST PAGE MODE CYCLE

Fast page mode allows data to be transferred into or out of multiple column locations of the same row by performing multiple $\overline{CAS}$ cycle during a single active $\overline{RAS}$ cycle. During a fast page cycle, the $\overline{RAS}$ signal may be maintained active for a period up to 100 μseconds. For the initial fast page mode access, the output data is valid after the specified access times from $\overline{RAS}$, $\overline{CAS}$, column address and $\overline{DT}/\overline{OE}$. For all subsequent fast page mode read operations, the output data is valid after the specified access times from $\overline{CAS}$, column address and $\overline{DT}/\overline{OE}$, When the write-per-bit function is enabled, the mask data latched at the falling edge of $\overline{RAS}$ is maintained throughout the fast page mode write or read-modify-write cycle.

$\overline{RAS}$-ONLY REFRESH

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-Only" cycle.

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

The TC528128B also offers an internal-refresh function. When $\overline{CAS}$ is held "low" for a specified period (t_{CSR}) before $\overline{RAS}$ goes "low", an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ cycle. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, $\overline{CAS}$ can remain "low" while cycling $\overline{RAS}$.

HIDDEN REFRESH

A hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh performed by holding $\overline{CAS}$ "low" from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{RAS}$ after the specified $\overline{RAS}$-precharge period (Refer to Figure 1).

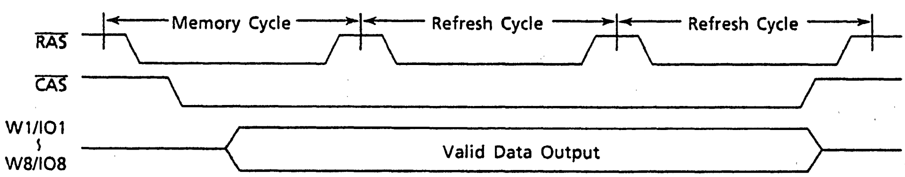


Figure 1. Hidden Refresh Cycle

WRITE-PER-BIT FUNCTION

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB}$ / $\overline{WE}$ is held "low" at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the W_i / IO_i pins is latched onto the write-mask register (WM1). When a "0" is sensed on any of the W_i / IO_i pins, their corresponding write circuits are disabled and new data will not be written, When a "1" is sensed on any of the W_i / IO_i pins, their corresponding write circuits will remain enabled so that new data is written. The truth table of the write-per-bit function is shown in Table 3.

Table 3. Truth table for write-per-bit function

At the falling edge of $\overline{RAS}$				Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	Wi/IOi (i=1~8)	
H	H	H	*	Write Enable
H	H	L	1	Write Enable
			0	Write Mask

An example of the write-per-bit function illustrating its application to displays is shown in Figures 2 and 3.

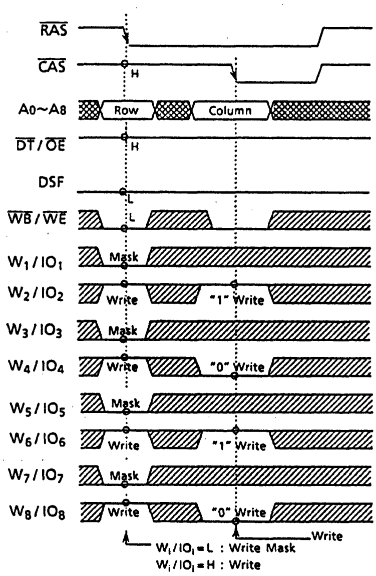


Figure 2. Write-per-bit timing cycle

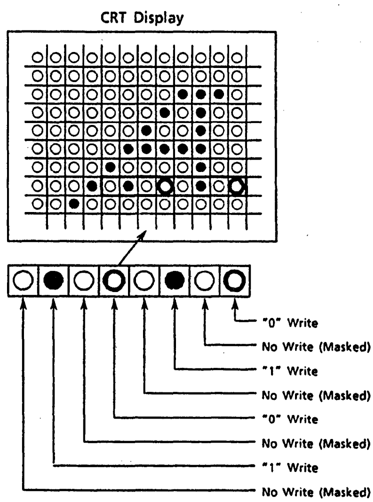


Figure 3. Corresponding bit-map

LOAD COLOR REGISTER/READ COLOR REGISTER

The TC528128B is provided with an on-chip 8-bits register (color register) for use during the flash write or block write operation. Each bit of the color register corresponds to one of the DRAM I/O blocks. The load color register cycle is initiated by holding $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and DSF "high" at the falling edge of $\overline{RAS}$. The data presented on the W_i/IO_i lines is subsequently latched into the color register at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs last. The data stored in the color register can be read out by performing a read color register cycle. This cycle is activated by holding $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and DSF "high" at the falling edge of $\overline{RAS}$ and by holding $\overline{WB}/\overline{WE}$ "high" at the falling edge of $\overline{CAS}$ and throughout the remainder of the cycle. The data in the color register becomes valid on the W_i/IO_i lines after the specified access times from $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ are satisfied. During the load/read color register cycle, valid A_0~A_8 row addresses are not required, but the memory cells on the row address latched at the falling edge of $\overline{RAS}$ are refreshed.

FLASH WRITE

Flash write is a special RAM port write operation which in a single $\overline{RAS}$ cycle, allows for the data in the color register to be written into all the memory locations of a selected row. Each bit of the color register corresponds to one of the DRAM I/O blocks and the flash write operation can be selectively controlled on an I/O basis in the same manner as the write-per-bit operation.

A flash write cycle is performed by holding $\overline{CAS}$ "high", $\overline{WB}/\overline{WE}$ "low" and DSF "high" at the falling edge of $\overline{RAS}$. The mask data must also be provided on the W_i/IO_i lines at the falling edge of $\overline{RAS}$ in order to enable the flash write operation for selected I/O blocks (Refer to Figure 4 and 5).

Flash write is most effective for fast plane clear operations in frame buffer applications. Selected planes can be cleared by performing 512 flash write cycle and by specifying a different row address location during each flash write cycle (Refer to Figure 6). Assuming a cycle time of 180ns, a plane clear operation can be completed in less than 92.2 μseconds.

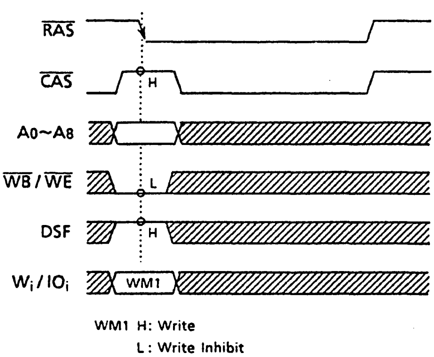


Figure 4. Flash Write Timing

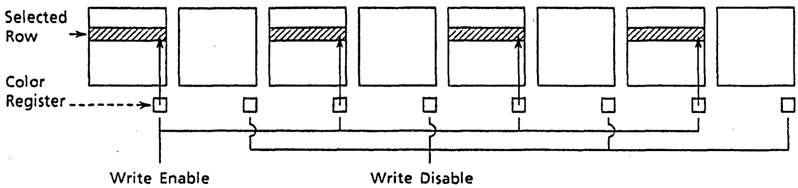


Figure 5. Flash Write

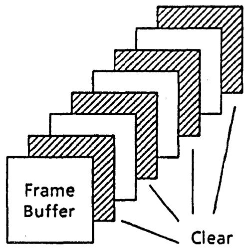


Figure 6. Plane clear application example

BLOCK WRITE

Block write is also a special RAM port write operation which, in a single RAS cycle, allows for the data in the color register to be written into 4 consecutive column address locations starting from a selected column address in a selected row. The block write operation can be selectively controlled on an I/O basis and a column mask capability is also available.

A block write cycle is performed by holding $\overline{CAS}$, $\overline{DT}/\overline{OE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$ and by holding DSF "high" at the falling edge of $\overline{CAS}$. The state of the $\overline{WB}/\overline{WE}$ input at the falling edge of $\overline{RAS}$ determines whether or not the I/O data mask is enabled ($\overline{WB}/\overline{WE}$ must be "low " to enable the I/O data mask or "high" to disable it). At the falling edge of $\overline{RAS}$, a valid row address and I/O mask data are also specified. At the falling edge of $\overline{CAS}$, the starting column address location and column mask data must be provided. During a block write cycle, the 2 least significant column address locations (A0C and A1C) are internally controlled and only the six most significant column addresses (A2C~A7C) are latched at the falling edge of $\overline{CAS}$. (Refer to Figure 7).

An example of the block write function is shown in Figure 8 with a data mask on W_1/IO_1, W_4 / IO_4, W_6 / IO_6, W_7/ IO_7 and column 2. Block write is most effective for window clear and fill operation in frame buffer applications, as shown in the examples in Figure 9.

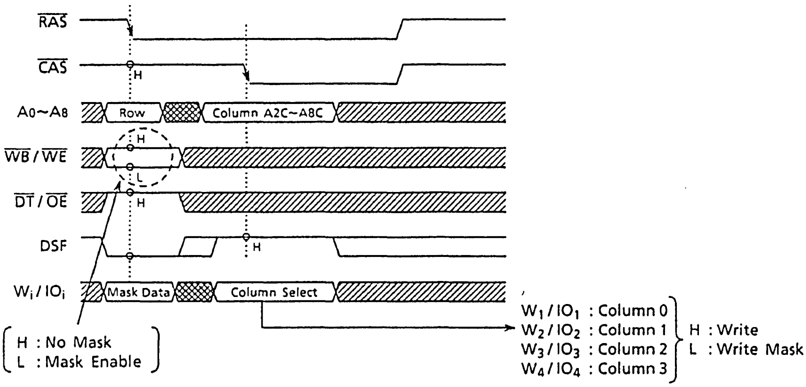


Figure 7. Block Write Timing

	Mask Data	Column Select	Color Resister Data
W_1/IO_1	0	1	0
W_2/IO_2	1	1	0
W_3/IO_3	1	0	1
W_4/IO_4	0	1	1
W_5/IO_5	1	-	1
W_6/IO_6	0	-	1
W_7/IO_7	0	-	0
W_8/IO_8	1	-	0

⇨

	Column 0	Column 1	Column 2	Column 3	
W_1/IO_1					← Mask
W_2/IO_2	0	0		0	
W_3/IO_3	1	1		1	
W_4/IO_4					← Mask
W_5/IO_5	1	1		1	
W_6/IO_6					
W_7/IO_7					
W_8/IO_8	0	0		0	
			↑ Mask		

Figure 8. Example of Block Write Operation

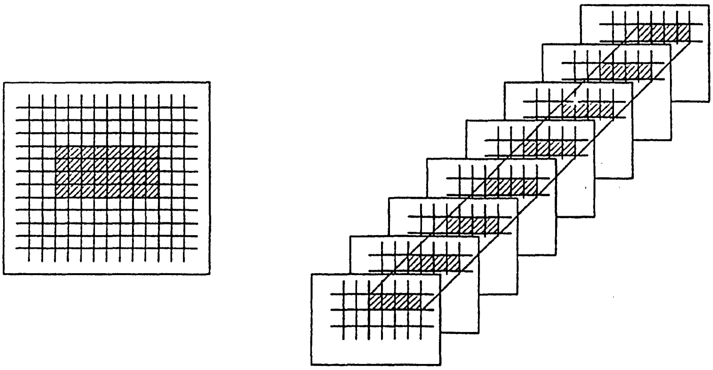


Figure 9. Examples of Block Write Application

FAST PAGE MODE BLOCK WRITE CYCLE

Fast page mode block write can be used to perform high speed clear and fill operations. The cycle is initiated by holding the DSF signal "low" at the falling edge of $\overline{RAS}$ and a fast page mode block write is performed during each subsequent $\overline{CAS}$ cycle with DSF held "high" at the falling edge of $\overline{CAS}$.

If the DSF signal is "low" at the falling edge of $\overline{CAS}$, a normal fast page mode read / write operation will occur. Therefore a combination of block write and read / write operations can be performed during a fast page mode block write cycle. Refer to the example shown in Figure 10.

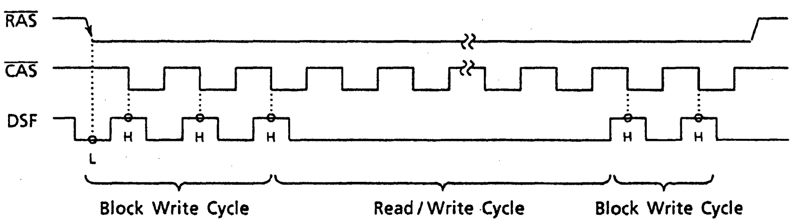


Figure 10. Fast Page Mode Block Write Cycle

SAM PORT OPERATION

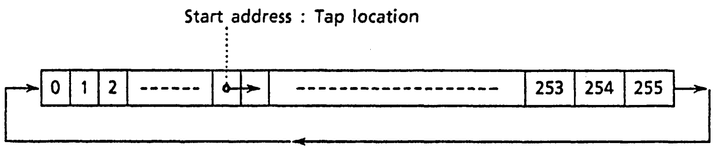
The TC528128B is provided with a 256 words by 8 bits serial access memory (SAM) which can be operated in the single register mode or the split register mode.

SINGLE REGISTER MODE

When operating in the single register mode, high speed serial read or write operations can be performed through the SAM port independent of the RAM port operations, except during read / write / pseudo-write transfer cycles. The preceding transfer operation determines the direction of data flow through the SAM port. If the preceding transfer operation is a read transfer, the SAM port is in the output mode. If the preceding transfer operation is a write or pseudo write transfer, the SAM port is in the input mode. The pseudo write transfer operation only switches the SAM port from output mode to input mode; Data is not transferred from SAM to RAM.

Serial data can be read out of the SAM port after a read transfer (RAM→SAM) has been performed. The data is shifted out of the SAM port starting at any of the 256 bits locations.

The TAP location corresponds to the column address selected at the falling edge of $\overline{CAS}$ during the read transfer cycle. The SAM registers are configured as circular data registers. The data is shifted out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit, as illustrated below.



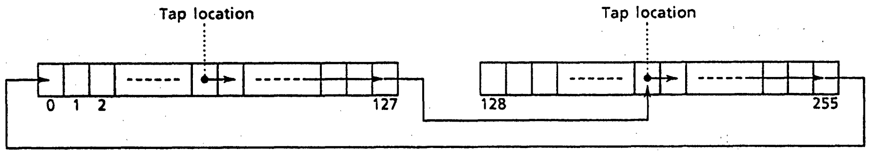
Subsequent real-time read transfer may be performed on-the-fly as many times as desired, within the refresh constraints of the DRAM array. Simultaneous serial read operation can be performed with some timing restrictions. A pseudo write transfer cycle is performed to change the SAM port from output mode to input mode in order to write data into the serial registers through the SAM port. A write transfer cycle must be used subsequently to load the SAM data into the RAM row selected by the row address at the falling edge of $\overline{RAS}$. The starting location in the SAM registers for the next serial write is selected by the column address at the falling edge of $\overline{CAS}$. The truth table for single register mode SAM operation is shown in Table 4.

Table 4. Truth Table for SAM Port Operation

SAM PORT OPERATION	$\overline{DT}/\overline{OE}$ at the falling edge of $\overline{RAS}$	SC	$\overline{SE}$	FUNCTION	Preceded by a
Serial Output Mode	H	⎍	L	Enable Serial Read	Read Transfer
			H	Disable Serial Read	
Serial Input Mode		⎍	L	Enable Serial Write	Write Transfer
			H	Disable Serial Write	
Serial Input Mode		⎍	L	Enable Serial Write	Pseudo Write Transfer
			H	Disable Serial Write	

SPLIT REGISTER MODE

In split register mode, data can be shifted into or out of one half of the SAM while a split read or split write transfer is being performed on the other half of the SAM. A normal (Non-split) read / write / pseudo write transfer operation must precede any split read / write transfer operation. The non-split read, write and pseudo write transfer will set the SAM port into output mode or input mode. The split read and write transfers will not change the SAM port mode set by preceding normal transfer operation. RAM port operation may be performed independently except during split transfers. In the split register mode, serial data can be shifted in or out of one of the split SAM registers starting from any at the 128 tap locations, excluding the last address of each split SAM, data is shifted in or out sequentially starting from the selected tap location to the most significant bit (127 or 255) of the first split SAM and then the SAM pointer moves to the tap location selected for the second split SAM to shift data in or out sequentially starting from this tap location to the most significant bit (255 or 127) and finally wraps around to the least significant bit, as illustrated in the example below.



REFRESH

The SAM data registers are static flip-flop, therefore a refresh is not required.

DATA TRANSFER OPERATION

The TC528128B features two types of internal bidirectional data transfer capability between RAM and the SAM, as shown in Figure 11. During a normal (Non-split) transfer, 256 words by 8 bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer). During a split transfer, 128 words by 8 bits of data can be loaded from the lower / upper half of the RAM into the lower/upper half of the SAM (Split Read Transfer) or from the lower / upper half of the SAM into the lower / upper half of the RAM (Split Write Transfer). The normal transfer and split transfer modes are controlled by the DSF special function input signal.

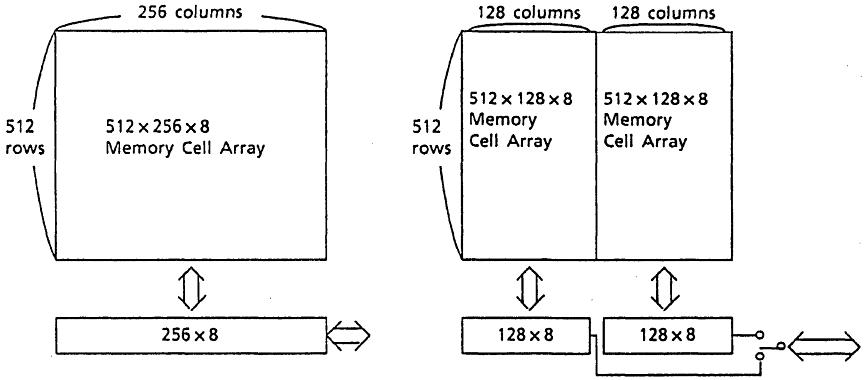


Figure 11. (a) Normal (Non-split) Transfer (b) Split Transfer

As shown in Table 5, the TC528128B supports five types of transfer operations: Read transfer, Split read transfer, Write transfer, Split write transfer and Pseudo write transfer. Data transfer operations between RAM and SAM are invoked by holding the $\overline{DT}/\overline{OE}$ signal "low" at the falling edge of $\overline{RAS}$. The type of data transfer operation is determined by the state of $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$ and DSF latched at the falling edge of $\overline{RAS}$. During normal (Non-split) data transfer operations, the SAM port is switched from input to output mode (Read transfer) or output to input mode (Write transfer / Pseudo write transfer) whereas it remains unchanged during split transfer operations (Split read or split write transfers). During a data transfer cycle, the row address A_0~A_8 select one of the 512 rows of the memory array to or from which data will be transferred and the column address A_0~A_7 select one of the tap locations in the serial register. The selected tap location is the start position in the SAM port from which the first serial data will be read out during the subsequent serial read cycle or the start position in the SAM port into which the first serial data will be written during the subsequent serial write cycle. During split data transfer cycles, the most significant column address (A7C) is controlled internally to determine which half of the serial register will be reloaded from the RAM array.

Table 5. Transfer Modes

at the falling edge of $\overline{RAS}$					Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	DSF				
H	L	H	*	L	Read Transfer	RAM → SAM	256x8	Input → Output
H	L	L	L	L	Write Transfer	SAM → RAM	256x8	Output → Input
H	L	L	H	L	Pseudo Write Transfer	-	-	Output → Input
H	L	H	*	H	Split Read Transfer	RAM → SAM	128x8	Not changed
H	L	L	*	H	Split Write Transfer	SAM → RAM	128x8	Not changed

* : "H" or "L"

READ TRANSFER CYCLE

A read transfer consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low" $\overline{WB}/\overline{WE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of $\overline{DT}/\overline{OE}$. When the transfer is completed, the SAM port is set into the output mode. In a read / real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and this data becomes valid on the SIO lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Figure 12 shows the operation block diagram for read transfer operation.

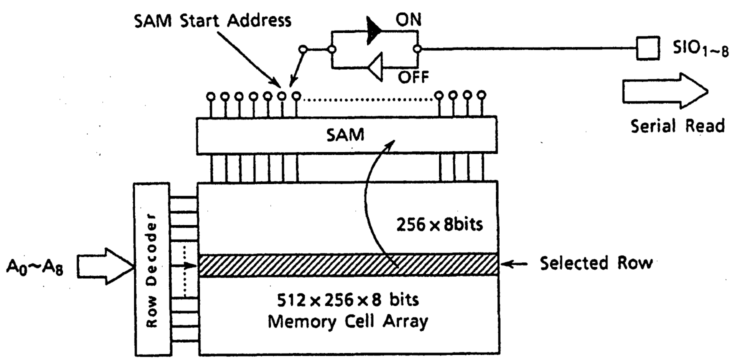


Figure 12. Block Diagram for Read Transfer Operation

In a read transfer cycle (which is preceded by a write transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}/\overline{OE}$, as shown in Figure 13.

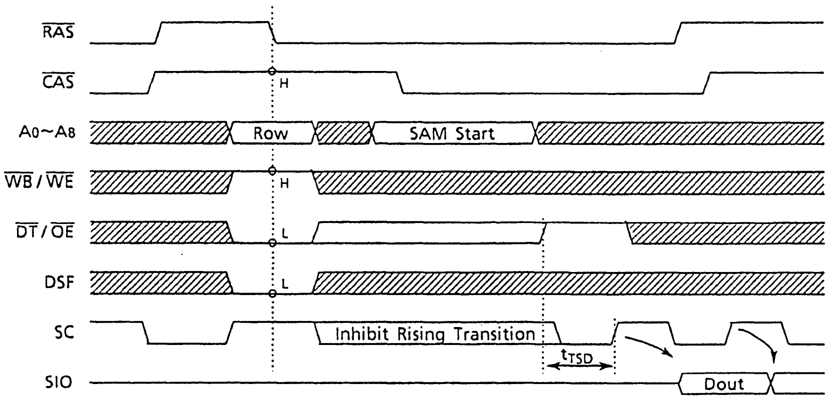


Figure 13. Read Transfer Timing

In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SIO lines until the $\overline{DT}/\overline{OE}$ signal goes "high" and the serial access time t_{SCA} for the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (t_{RTH}, t_{CTH}, and t_{TSL}/t_{TSD} must be satisfied), as shown in Figure 14.

The timing restriction t_{TSL}/ t_{TSD} are 5ns min / 15ns min. The split read transfer mode eliminates these timing restrictions.

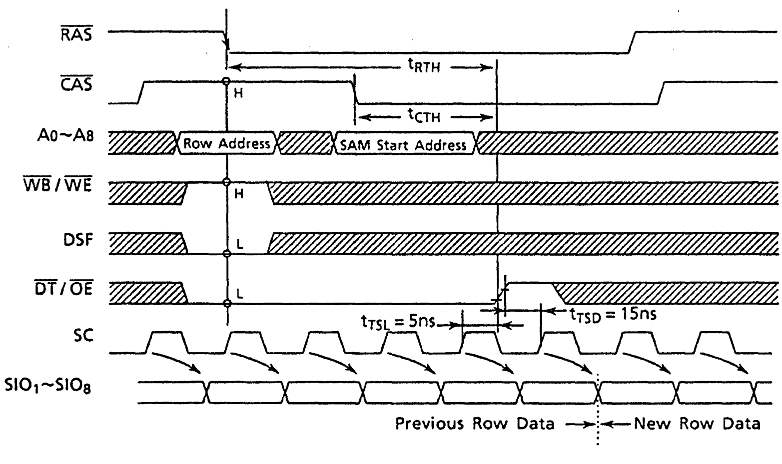


Figure 14. Real Time Read Transfer

WRITE TRANSFER CYCLE

A write transfer cycle consist of loading the content of the SAM register into a selected row of the RAM array. If the SAM data to be transferred must first be loaded through the SAM port, a pseudo write transfer operation must precede the write transfer cycles. However, if the SAM port data to be transferred into the RAM was previously loaded into the SAM via a read transfer, the SAM to RAM transfer can be executed simply by performing a write transfer directly. A write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low", $\overline{SE}$ "low" and DSF "low" at the falling edge of $\overline{RAS}$. This write transfer is selectively controlled per RAM I/O block by setting the mask data on the W_i/IO_i lines at the falling edge of $\overline{RAS}$ (same as in the write-per-bit operation). Figure 15 and 16 show the timing diagram and block diagram for write transfer operations, respectively.

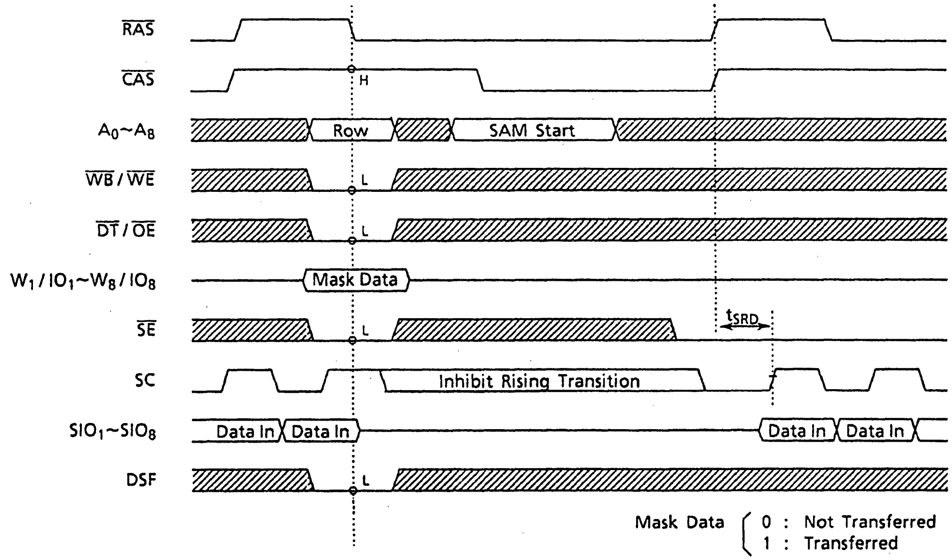


Figure 15. Write Transfer Timing

The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.

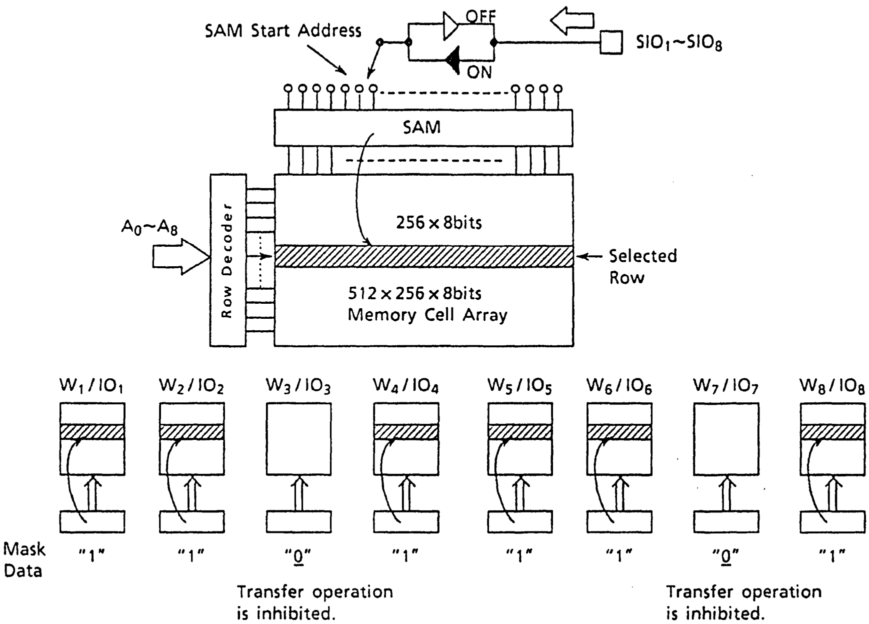


Figure 16. Block Diagram for Write Transfer Operation

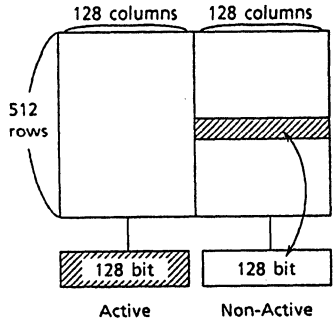
When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC Clock is only allowed after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$, at which time a new row of data can be written in the serial register.

PSEUDO WRITE TRANSFER CYCLE

A pseudo write transfer cycle must be performed before loading data into the serial register after a read transfer operation has been executed. The only purpose of a pseudo write transfer is to change the SAM port mode from output mode to input mode (A data transfer from SAM to RAM does not occur). After the serial register is loaded with new data, a write transfer cycle must be performed to transfer the data from SAM to RAM. A pseudo write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low", $\overline{SE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$. The timing conditions are the same as the one for the write transfer cycle except for the state of $\overline{SE}$ at the falling edge of $\overline{RAS}$.

SPLIT DATA TRANSFER AND QSF

The TC528128B features a bi-directional split data transfer capability between the RAM and the SAM. During split data transfer operation, the serial register is split into two halves which can be controlled independently. Split read or split write transfer operations can be performed to or from one half of the serial register while serial data can be shifted into or out of the other half of the serial register, as shown in Figure 17. The most significant column address location (A7C) is controlled internally to determines which half of the serial register will be reloaded from the RAM array. QSF is an output in which indicates which half of the serial register is in an active state. QSF changes state when the last SC clock is applied to active split SAM, as shown in Figure 18.



Active SAM	QSF Level
lower SAM	"Low"
upper SAM	"High"

Figure 17. Split Register Mode

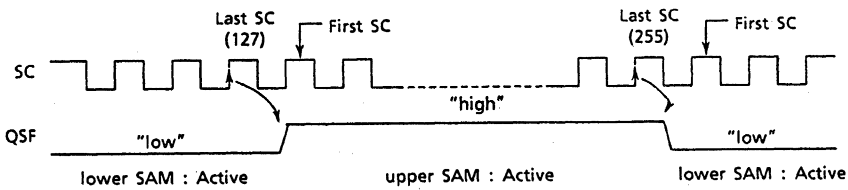


Figure 18. QSF Output State During Split Register Mode

SPLIT READ TRANSFER CYCLE

A split read transfer consists of loading127 words by 8 bits of data from a selected row of the split RAM array into the corresponding non-active split SAM register.

Serial data can be shifted out of the other half of the split SAM register simultaneously. The block diagram and timing diagram for split read transfer mode are shown in Figure 19 and 20, respectively. During split read transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus eliminating timing restrictions as in the case of on-the-fly read transfers. A split read transfer can be performed after a delay of t_{STS}, from the change of state of the QSF output, is satisfied.

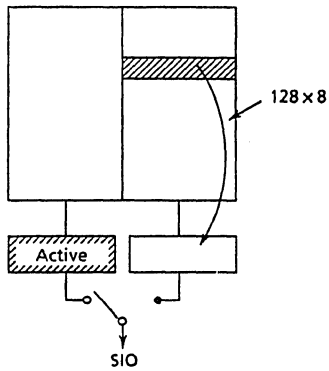


Figure 19. Block Diagram for Split Read Transfer

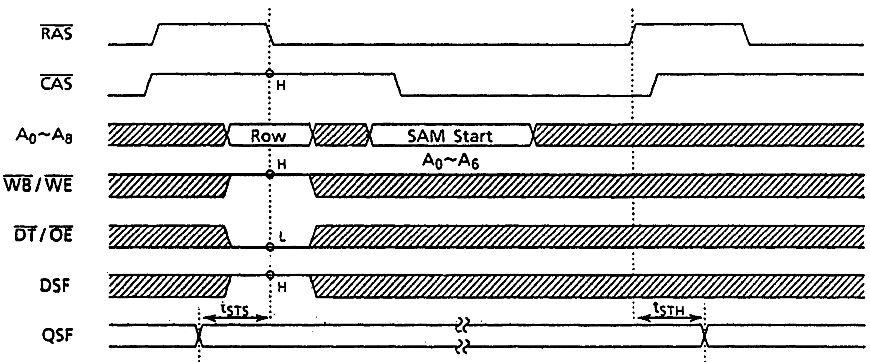


Figure 20. Timing Diagram for Split Read Transfer

A normal (Non-split) read transfer operation must precede split read transfer cycles as shown in the example in Figure 21.

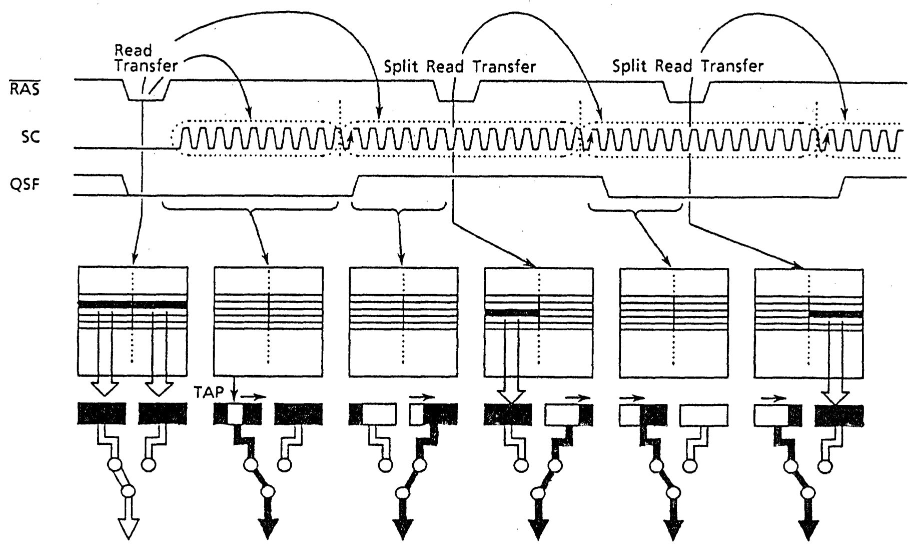


Figure 21. Example of Consecutive Read Transfer Operations

SPLIT WRITE TRANSFER CYCLE

A split write transfer consists of loading 128 words by 8 bits of data from the non-active split SAM register into a selected row of the corresponding split RAM array.

Serial data can be shifted into the other half of the split SAM register simultaneously. The block diagram and timing diagram for split write transfer mode are shown in Figure 22 and 23, respectively. During split write transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus allowing for real time transfer. A split write transfer can be performed after a delay of t_{STS}, from the change of state of the QSF output, is satisfied.

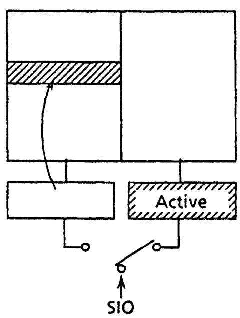


Figure 22. Block Diagram for Split Write Transfer

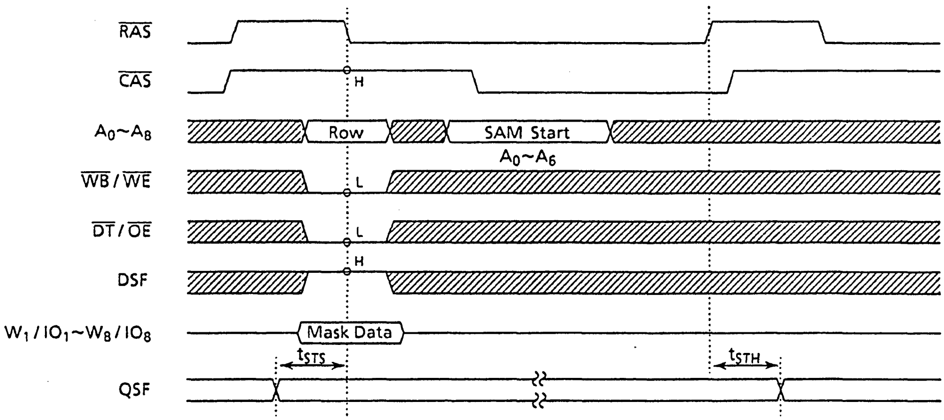


Figure 23. Timing Diagram for Split Write Transfer

A pseudo write transfer operation must precede split transfer cycles as shown in the example in Figure 24. The purpose of the pseudo write transfer operation is to switch the SAM port from output mode to input mode and to set the initial tap location prior to split write transfer operations.

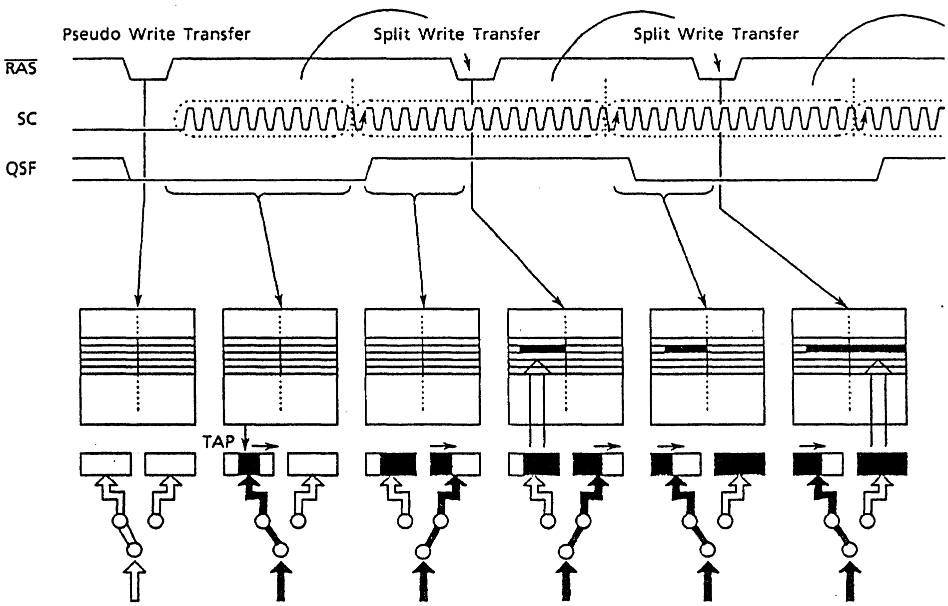


Figure 24. Example of consecutive Write Transfer Operations

SPLIT-REGISTER OPERATION SEQUENCE (EXAMPLE)

Split read / write transfers must be preceded by a normal (Non-split) transfer such as a read, write or pseudo write transfer. Figure 25 illustrates an example of split register operation sequence after device power-up and initialization. After power-up, a minimum of 8 $\overline{RAS}$ and 8 SC clock cycles must be performed to properly initialize the device. A read transfer is then performed and the column address latched at the falling edge of $\overline{CAS}$ sets the SAM tap pointer location which up to that point was in an undefined location. Subsequently, the pointer address is incremented by cycling the serial clock SC from the starting location to the last location in the register (address 255) and wraps around to the tap location set by the split read transfer performed for the lower SAM while the upper SAM is being accessed. The SAM address is incremented as long as SC is clocked. The following split read transfer sets a new tap location in the upper split SAM register address 127 in this example and the pointer is incremented from this location by cycling the SC clock.

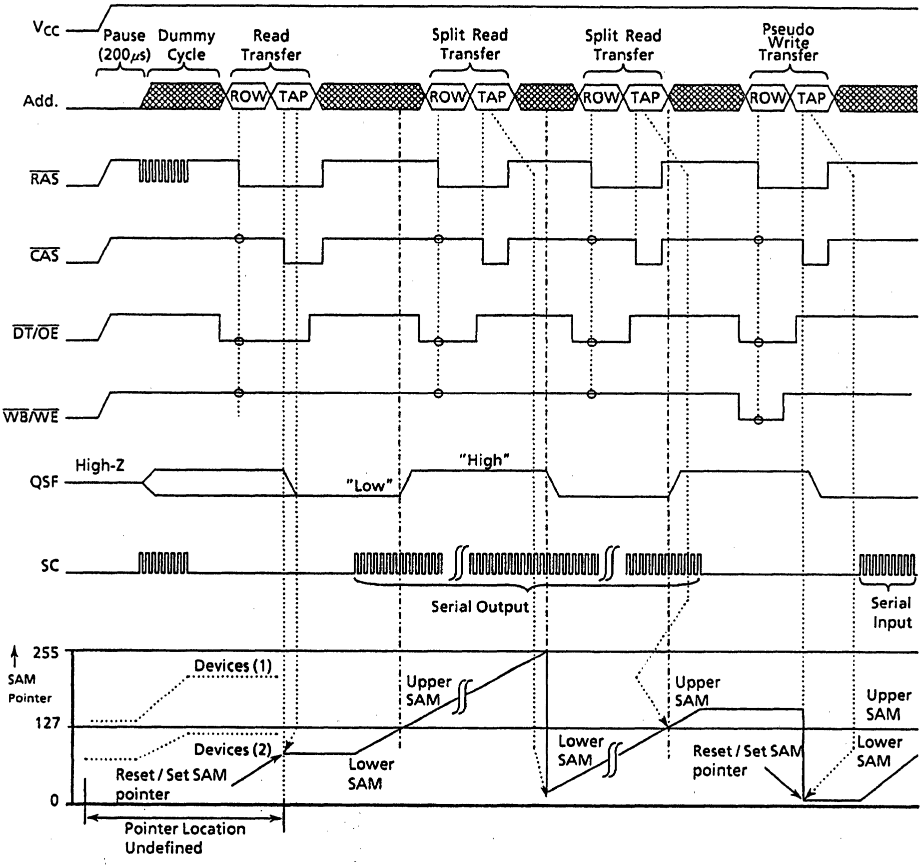
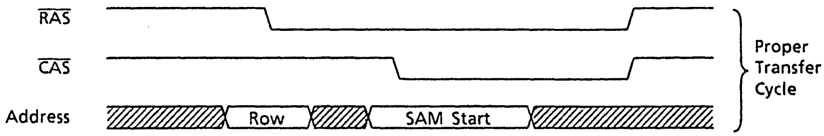


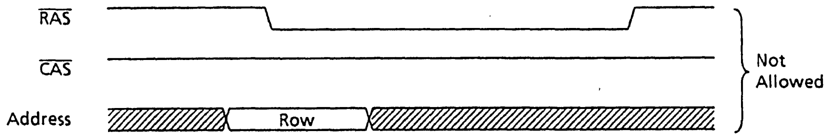
Figure 25. Example of Split SAM Registerr Operation Sequence

The next operation is a pseudo write transfer which switches the SAM port from output mode to input mode in preparation for either write transfers or split write transfers. The column address latched at the falling edge of $\overline{CAS}$ during the pseudo write transfer sets the serial register tap location. Serial data will be written into the SAM starting from this location.

TRANSFER OPERATION WITHOUT $\overline{CAS}$

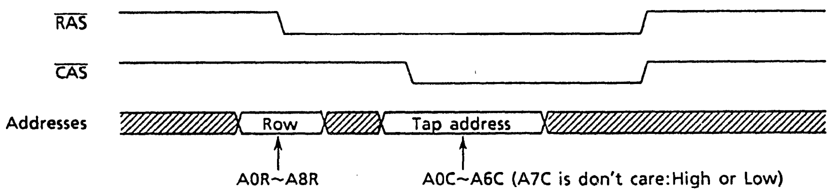
During all transfer Cycles, the $\overline{CAS}$ input clock must be cycled, so that the column address are latched at the falling edge of $\overline{CAS}$, to set the SAM tap location. If $\overline{CAS}$ was maintained at a constant "high" level during a transfer cycle, the SAM pointer location would be undefined. Therefore a transfer cycle with $\overline{CAS}$ held "high" is not allowed (Refer to the illustration below).





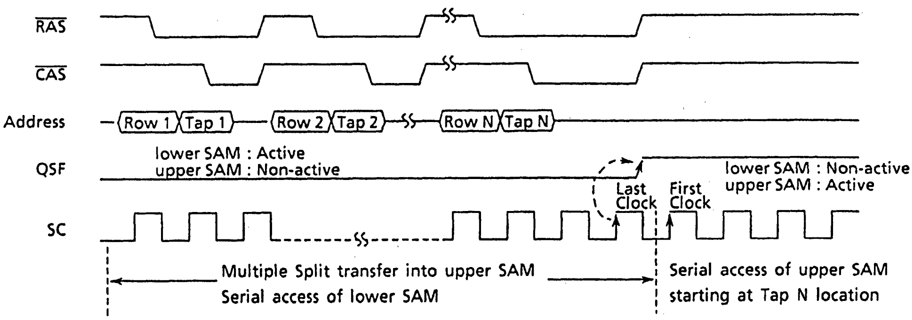
TAP LOCATION SELECTION IN SPLIT TRANSFER OPERATION

(a) In a split transfer operation, column addresses A0C through A6C must be latched at the falling edge of $\overline{CAS}$ in order to set the tap location in one of the split SAM registers. During a split transfer, column address A7C is controlled internally and therefore it is ignored internally at the falling edge of $\overline{CAS}$.



During a split transfer, it is not allowed to set the last address location (A0C~A6C=7F), in either the lower SAM or the upper SAM, as the tap location.

(b) In the case of multiple split transfers performed into the same split SAM register, the tap location specified during the last split transfer, before QSF toggles, will prevail. In the example shown below, multiple split transfers are performed into the upper SAM (Non-active) while the lower SAM (active) is being accessed at the time when QSF toggles, the first SC serial clock will start shifting serial data starting from the Tap N address location.



SPLIT READ / WRITE TRANSFER OPERATION ALLOWABLE PERIOD

Figure 26 illustrates the relationship between the serial clock SC and the special function output QSF during split read / write transfers and highlights the time periods where split transfers are allowed, relative to SC and QSF.

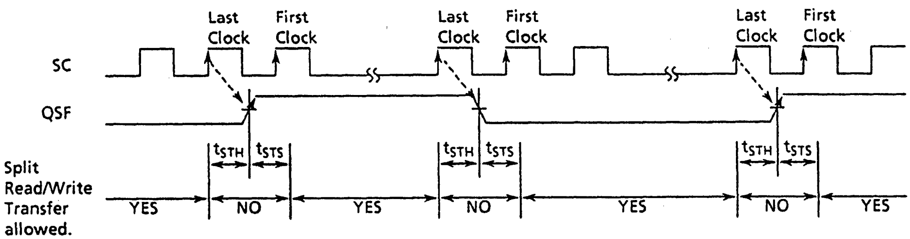
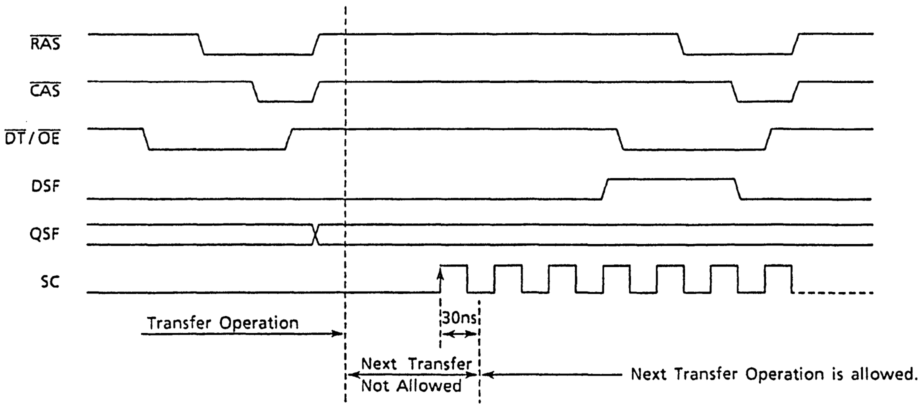


Figure 26. Split Transfer Operation Allowable Periods

As indicated in Figure 26, a split read / write transfer is not allowed during the period of $t_{STH} + t_{STS}$.

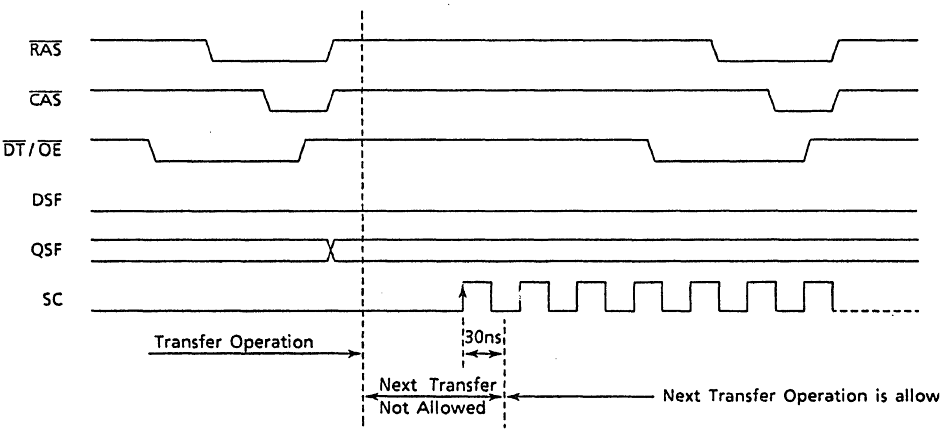
SPLIT TRANSFER CYCLE AFTER NORMAL TRANSFER CYCLE

A split transfer may be performed following a normal transfer (Read / Write / Pseudo-Write transfer) provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (Refer to the illustration shown below).



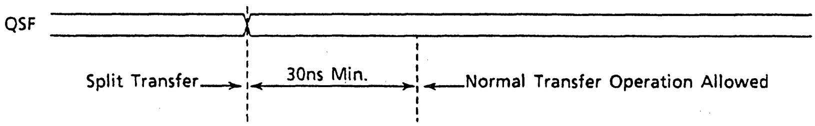
NORMAL READ TRANSFER CYCLE AFTER NORMAL READ TRANSFER CYCLE

Another read transfer may be performed following the read transfer provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (Refer to the illustration shown below).



NORMAL TRANSFER AFTER SPLIT TRANSFER

A normal transfer (read / write / pseudo write) may be performed following split transfer operation provided that a 30ns minimun delay is satisfied after the QSF signal toggles.



POWER-UP

Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them "high" before or at the same time as the V_{CC} supply is turned on. After power-up, a pause of 200 µseconds minimum is required with $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ held "high". After the pause, a minimum of 8 $\overline{RAS}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT}/\overline{OE}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.

INITIAL STATE AFTER POWER-UP

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and $\overline{WB}/\overline{WE}$ held "high", the internal state of the TC528128B is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 µseconds pause followed by a minimum of 8 $\overline{RAS}$ cycles and 8 SC cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
QSF	High-Impedance
Color Register	all "0"
WM1 Register	Write Enable
TAP pointer	Invalid

SILICON GATE CMOS
262,144WORDS X 8BITS MULTIPORT DRAM

target spec

DESCRIPTION

The TC528257 is a 2M bit CMOS multiport memory equipped with a 262,144-words by 8-bits dynamic random access memory (RAM) port and a 512-words by 8-bits static serial access memory (SAM) port. The TC528257 supports three types of operations; Random access to and from the RAM port, high speed serial access to and from the SAM port and bidirectional transfer of data between any selected row in the RAM and the SAM. To realize a high performance graphic frame buffer system the TC528257 features various special operations such as the write - per - bit, the pipelined page mode, the block write and flash write function on the RAM port and the read and masked write transfer operations between the RAM and the SAM port. The TC528257 is fabricated using Toshiba's CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

FEATURES

- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- All inputs and outputs : TTL Compatible
- Organization
  RAM Port : 262,144wordsX8bits
  SAM Port : 512wordsX8bits
- RAM Port
  Fast Page Mode, Read - Modify - Write, Pipelined Fast Page Mode, $\overline{CAS}$ before $\overline{RAS}$ Auto Refresh, Hidden Refresh, $\overline{RAS}$ only Refresh, Write per Bit (New/Old Mask Mode), Masked Flash Write (New/Old Mask Mode), Block Write, Masked Block Write (New/Old Mask Mode), Load Mask Register/Color Register Cycle, 512 refresh cycles / 8ms
- SAM Port
  Serial Read / Write Capability
  Addressable TAP Capability
  Stop Address (Binary Boundary) Capability
  Fully Static Register, Single Register/Split Register Mode Capability
- RAM - SAM Bidirectional Transfer
  Read / Real Time Read Transfer
  Masked Write Transfer
  Split Read / Masked Split Write Transfer
- Package
  TC528257J : SOJ40-P-400
  TC528257FT : TSOP44-P-400B
  TC528257TR : TSOP44-P-400C

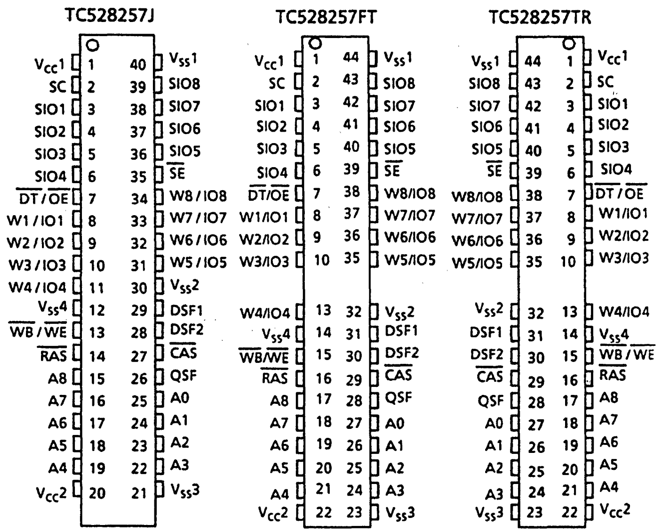
KEY PARAMETERS

ITEM		TC528257	
		—70	—80
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	70ns	80ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	20ns	20ns
t_{AA}	Column Address Access Time (Max.)	35ns	40ns
t_{RC}	Cycle Time (Min.)	130ns	150ns
t_{PC}	Page Mode Cycle Time (Min.)	45ns	50ns
t_{SCA}	Serial Access Time (Max.)	20ns	25ns
t_{SCC}	Serial Cycle Time (Min.)	25ns	30ns
t_{RACP}	t_{RAC} in Pipelined Fast Page	90ns	95ns
t_{CAC1}	t_{CAC} in Pipelined Fast Page	20ns	20ns
t_{PCP}	Pipelined Fast Page Mode Cycle Time	30ns	30ns
I_{CC1}	RAM Operating Current (SAM : Standby)	100mA	85mA
I_{CC2A}	SAM Operating Current (RAM : Standby)	60mA	50mA
I_{CC2}	Standby Current	10mA	10mA

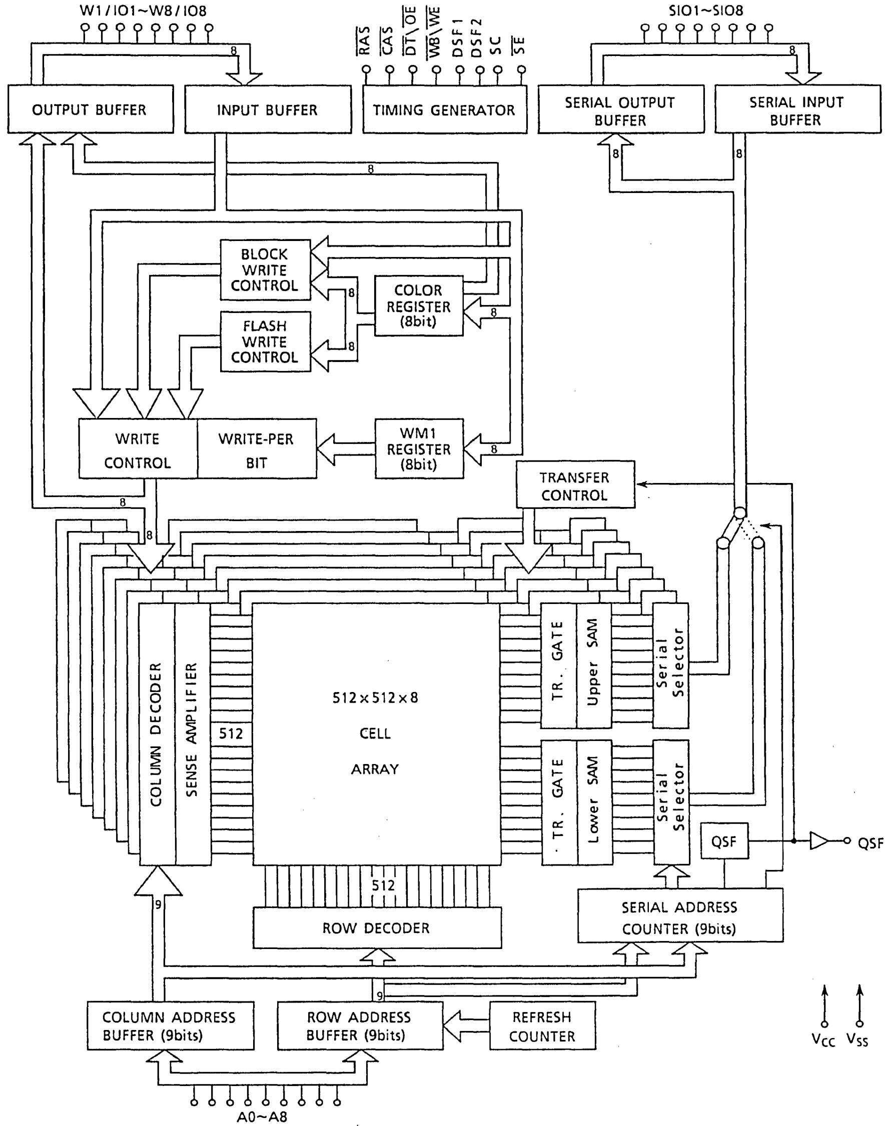
PIN NAME

A0~A8	Address inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}/\overline{WE}$	Write per Bit/Write Enable
DSF1 DSF2	Special Function Control
Wl/IOl ~W8/IO8	Write Mask/Data IN/OUT
SC	Serial Clock
SE	Serial Enable
SIOl~SIO8	Serial Input/Output
QSF	Special Flag Output
V_{CC}/V_{SS}	Power(5V)/Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}, V_{OUT}	Input Output Voltage	— 1.0~7.0	V	1
V_{CC}	Power Supply Voltage	— 1.0~7.0	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	— 55~150	°C	1
T_{SOLDER}	Soldering Temperature • Time	260•10	°C•sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	6.5	V	2
V_{IL}	Input Low Voltage	— 1.0	—	0.8	V	2

CAPACITANCE (V_{CC} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance	—	7	pF
C_{IO}	Input/Output Capacitance	—	9	
C_O	Output Capacitance (QSF)	—	9	

Note: This parameter is periodically sampled and is not 100% tested.

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

ITEM (RAM PORT)	SAM PORT	SYMBOL	-70		-80		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
OPERATING CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ min.)	Standby	I_{CC1}	—	100	—	90	mA	3, 4, 5
	Active	I_{CC1A}	—	160	—	140	mA	3, 4, 5
STANDBY CURRENT ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	Standby	I_{CC2}	—	10	—	10	mA	
	Active	I_{CC2A}	—	65	—	55	mA	3, 4, 5
RAS ONLY REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} $t_{RC} = t_{RC}$ min.)	Standby	I_{CC3}	—	100	—	90	mA	3, 4, 5
	Active	I_{CC3A}	—	160	—	140	mA	3, 4, 5
PAGE MODE CURRENT ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling $t_{PC} = t_{RC}$ min.)	Standby	I_{CC4}	—	90	—	80	mA	3, 4, 5
	Active	I_{CC4A}	—	150	—	130	mA	3, 4, 5
CAS BEFORE RAS REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$ $t_{RC} = t_{RC}$ min.)	Standby	I_{CC5}	—	100	—	90	mA	3, 4, 5
	Active	I_{CC5A}	—	160	—	140	mA	3, 4, 5
DATA TRANSFER CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ min.)	Standby	I_{CC6}	—	135	—	125	mA	3, 4, 5
	Active	I_{CC6A}	—	195	—	175	mA	3, 4, 5
FLASH WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ min.)	Standby	I_{CC7}	—	100	—	90	mA	3, 4, 5
	Active	I_{CC7A}	—	160	—	140	mA	3, 4, 5
BLOCK WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ min.)	Standby	I_{CC8}	—	110	—	100	mA	3, 4, 5
	Active	I_{CC8A}	—	170	—	150	mA	3, 4, 5

ITEM	SYMBOL	MIN.	MAX	UNIT	NOTE
INPUT LEAKAGE CURRENT 0V ≤ V_{IN} ≤ 6.5V, All other pins not under test = 0V	$I_{I(L)}$	—10	10	μA	
OUTPUT LEAKAGE CURRENT 0V ≤ V_{OUT} ≤ 5.5V, Output Disable	$I_{O(L)}$	—10	10	μA	
OUTPUT "H" LEVEL VOLTAGE I_{OUT} = - 2mA	V_{OH}	2.4	—	V	
OUTPUT "L" LEVEL VOLTAGE I_{OUT} = 2mA	V_{OL}	—	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes: 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX		
t_{RC}	Random Read or Write Cycle Time	130		150		ns	
t_{RMW}	Read-Modify-Write Cycle Time	180		200			
t_{PC}	Fast Page Mode Cycle Time	45		50			
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	90		90			
t_{RAC}	Access Time from $\overline{RAS}$		70		80		9, 15
t_{AA}	Access Time from Column Address		35		40		9, 15
t_{CAC}	Access Time from $\overline{CAS}$		20		20		9, 16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		35		40		9, 16
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0		0			
t_{OELZ}	$\overline{OE}$ to Output in Low-Z	0		0			
t_{OFF}	Output Buffer Turn-Off Delay	0	15	0	15		11
t_T	Transition Time (Rise and Fall)	3	50	3	50		8
t_{RP}	$\overline{RAS}$ Precharge Time	50		60			
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10000	80	10000		
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode Only)	70	100000	80	100000		
t_{RSH}	$\overline{RAS}$ Hold Time	20		20			
t_{CSH}	$\overline{CAS}$ Hold Time	70		80			
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10000	20	10000		
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60		15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40		15
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35		40			
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5			
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10			
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10			
t_{ASR}	Row Address Set-Up Time	0		0			
t_{RAH}	Row Address Hold Time	10		10			
t_{ASC}	Column Address Set-Up Time	0		0			
t_{CAH}	Column Address Hold Time	12		15			
t_{RCS}	Read Command Set-Up Time	0		0			
t_{RCH}	Read Command Hold Time	0		0			12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0			12
t_{WCH}	Write Command Hold Time	10		15			
t_{WP}	Write Command Pulse Width	10		10			
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20			
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		20			
t_{DS}	Data Set-Up Time	0		0			13
t_{DH}	Data Hold Time	12		15			13
t_{WCS}	Write Command Set-Up Time	0		0			14
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	95		105			14
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	60		65			14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45		45			14
t_{RES}	$\overline{RAS}$ to SC Boundary - reset time	30		30			

SYMBOL	PARAMETER	-70		-80		UNIT	NOTE
		MIN.	MAX	MIN.	MAX.		
t_{DZC}	Data to $\overline{\text{CAS}}$ Delay Time	0		0			
t_{DZO}	Data to $\overline{\text{OE}}$ Delay Time	0		0			
t_{OEA}	Access Time from $\overline{\text{OE}}$		20		20		9
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{\text{OE}}$		15		15		11
t_{OED}	$\overline{\text{OE}}$ to Data Delay Time	15		15			
t_{OEH}	$\overline{\text{OE}}$ Command Hold Time	15		15		ns	
t_{ODS}	Output Disable Set up time	0		0			
t_{ROH}	$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	15		15			
t_{CSR}	$\overline{\text{CAS}}$ Set-Up Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle	5		5			
t_{CHR}	$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle	10		15			
t_{RPC}	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	0		0			
t_{REF}	Refresh Period		8		8	ms	
t_{WSR}	$\overline{\text{WB}}$ Set-Up Time	0		0			
t_{RWH}	$\overline{\text{WB}}$ Hold Time	10		15			
t_{FSR}	DSF Set-Up Time referenced to $\overline{\text{RAS}}$	0		0			
t_{RFH}	DSF Hold Time referenced to $\overline{\text{RAS}}$ (1)	10		15			
t_{FSC}	DSF Set-Up Time referenced to $\overline{\text{CAS}}$	0		0			
t_{CFH}	DSF Hold Time referenced to $\overline{\text{CAS}}$	12		15			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0		0			
t_{MH}	Write-Per-Bit Mask Data Hold Time	10		15			
t_{THS}	$\overline{\text{DT}}$ High Set-Up Time	0		0			
t_{THH}	$\overline{\text{DT}}$ High Hold Time	10		15			
t_{TLS}	$\overline{\text{DT}}$ Low Set-Up Time	0		0			
t_{TLH}	$\overline{\text{DT}}$ Low Hold Time	10	10000	15	10000		
t_{RTH}	$\overline{\text{DT}}$ Low Hold Time referenced to $\overline{\text{RAS}}$ (Real Time Read Transfer)	60	10000	65	10000	ns	
t_{ATH}	$\overline{\text{DT}}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	25		25			
t_{CTH}	$\overline{\text{DT}}$ Low Hold Time referenced to $\overline{\text{CAS}}$ (Real Time Read Transfer)	20		20			
t_{TRP}	$\overline{\text{DT}}$ to $\overline{\text{RAS}}$ Precharge Time	50		60			
t_{TP}	$\overline{\text{DT}}$ Precharge Time	15		15			
t_{RSD}	$\overline{\text{RAS}}$ to First SC Delay Time (Read Transfer)	70		80			
t_{ASD}	$\overline{\text{RAS}}$ to First SC Delay Time (Read Transfer)	35		40			
t_{CSD}	$\overline{\text{CAS}}$ to First SC Delay Time (Read Transfer)	20		20			
t_{TSL}	Last SC to $\overline{\text{DT}}$ Lead Time (Real Time Read Transfer)	5		5			
t_{TSD}	$\overline{\text{DT}}$ to FIrst SC Delay Time (Read Transfer)	10		15			
t_{SRS}	Last SC to $\overline{\text{RAS}}$ Set-Up Time (Serial Input)	25		30			
t_{SRD}	$\overline{\text{RAS}}$ to First SC Delay Time (Serial Input)	20		25			
t_{SDD}	$\overline{\text{RAS}}$ to Serial Input Delay Time	45		50			

SYMBOL	PARAMETER	-70		-80		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{SCC}	SC Cycle Time	25		30			
t_{SC}	SC Pulse Width (SC High Time)	10		10			
t_{SCP}	SC Precharge Time (SC Low Time)	5		10			
t_{SCA}	Access Time from SC		20		25		10
t_{SOH}	Serial Output Hold Time from SC	5		5			
t_{SDS}	Serial Input Set-Up Time	0		0			
t_{SDH}	Serial Input Hold Time	10		15			
t_{SEA}	Access Time from $\overline{SE}$		20		25		10
t_{SE}	$\overline{SE}$ Pulse Width	20		25			
t_{SEP}	$\overline{SE}$ Precharge Time	20		25			
t_{SEZ}	Serial Output Buffer Turn-off Delay from $\overline{SE}$		15		20		11
t_{SZE}	Serial Output Buffer Turn-off Delay from $\overline{SE}$	0		0			
t_{SZS}	Serial Input to First SC Delay Time	0		0			
t_{SWS}	Serial Write Enable Set-Up Time	0		0			
t_{SWH}	Serial Write Enable Hold Time	10		15			
t_{SWIS}	Serial Write Disable Set-Up Time	0		0			
t_{SWIH}	Serial Write Disable Hold Time	10		10			
t_{STS}	Split Transfer Set-Up Time	25		30			
t_{STH}	Split Transfer Hold Time	25		30			
tSAAT	Split Transfer SC Set-Up Time from RAS	45		55		ns	
tSAA	Split Transfer SC Hold Time from RAS	0		0			
t_{SQD}	SC-QSF Delay Time		20		25		
t_{TQD}	$\overline{DT}$-QSF Delay Time		20		25		
t_{CQD}	$\overline{CAS}$-QSF Delay Time		20		25		
t_{RQD}	$\overline{RAS}$-QSF Delay Time		70		80		
t_{RCDP}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time (Pipeline mode)	20	40	20	45		
t_{CSHP}	$\overline{CAS}$ Hold Time (Pipeline mode)	50		55			
t_{RACP}	Access TIme from $\overline{RAS}$ (Pipeline mode)		90		95		
t_{CAC1}	Access Time from $\overline{CAS}$ (1) (Pipeline mode)		20		20		10
t_{CAC2}	Access Time from $\overline{CAS}$ (2) (Pipeline mode)		50		50		10
t_{CASP}	$\overline{CAS}$ Pulse Width (Pipeline mode)	10		10			
t_{CPP}	$\overline{CAS}$ Precharge Time Pipeline mode)	10		10			
t_{PCP}	Fast Page Mode Cycle Time (Pipeline mode)	30		30			
t_{COH}	$\overline{CAS}$ Hold Time referenced to $\overline{OE}$ (Pipeline mode)	5		5			
t_{RSH1}	$\overline{RAS}$ Hold Time (1) (Pipeline mode)	20		20			
t_{RSH2}	$\overline{RAS}$ Hold Time (2) (Pipeline mode)	50		50			
t_{CWLP}	Write Command to $\overline{CAS}$ lead Time (Pipeline mode)	10		10			
t_{CWP}	$\overline{WE}$ to $\overline{CAS}$ Delay Time (Pipeline mode)	30		30			
t_{OFFP}	Outoff Buffer Turn-off Delay from $\overline{RAS}$ (Pipeline mode)	0	15	0	15		11, 17

RAM Output Reference Level	2.0V/0.8V
SAM Output Reference Level	2.0V/0.8V
RAM Output Load	1 TTL and 50PF
SAM Output Load	1 TTL and 30PF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltage are referenced to V_{SS}.

3. These parameters depend on cycle rate.

4. These parameters depend on output loading. Specified values are obtained with the output open.

5. Address can be changed once or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by any of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles before proper device operation is achieved.

7. AC measurements assume t_T = 5ns.

8. $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. RAM port outputs are measured with a load equivalent to 1 TTL load and 50pF.
   D_{OUT} reference levels : V_{OH} / V_{OL} = 2.0V / 0.8V.

10. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
    D_{OUT} reference levels : V_{OH} / V_{OL} = 2.0V / 0.8V.

11. $t_{OFF\ (max.)}$, $t_{OEZ\ (max.)}$, $t_{OFFP\ (max.)}$ and $t_{SEZ\ (max.)}$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.

12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.

13. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}$ / $\overline{WE}$ leading edge in $\overline{OE}$-controlled-write cycles and read-modify-write cycles.

14. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS\ (min.)}$, the cycle is an early write cycles and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geq t_{RWD\ (min.)}$, $t_{CWD} \geq t_{CWD\ (min.)}$ and $t_{AWD} \geq t_{AWD\ (min.)}$ the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

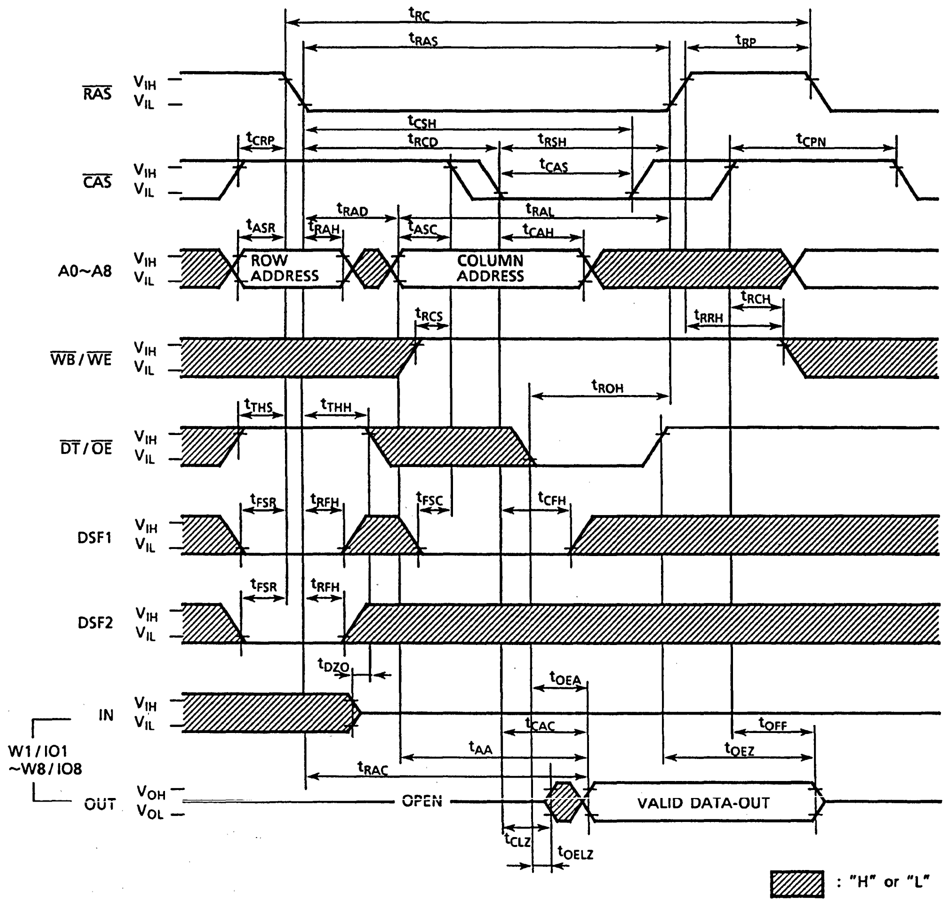
15. Operation within the $_{tRCD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can he met.
    $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified
    $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

16. Operation within the $t_{RAD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

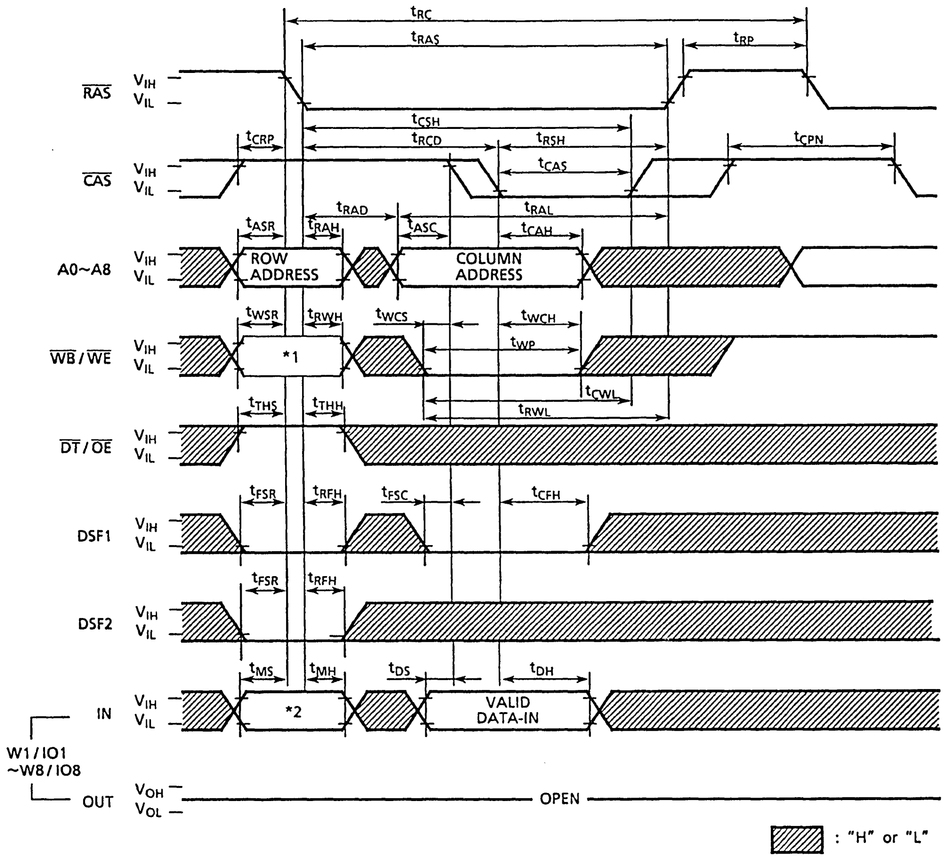
17. t_{OFFP} timing is specified from either $\overline{RAS}$ or $\overline{CAS}$ rising edge, whichever occurs last.

TIMING WAVEFORM

READ CYCLE



WRITE CYCLE (EARLY WRITE)

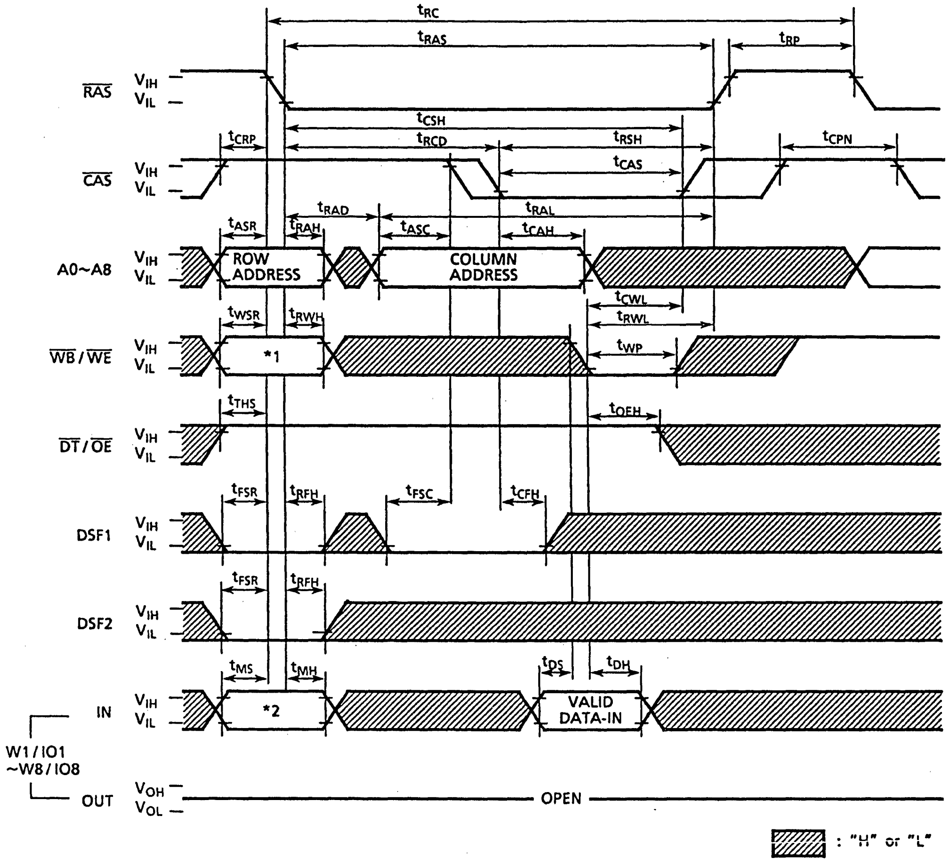


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

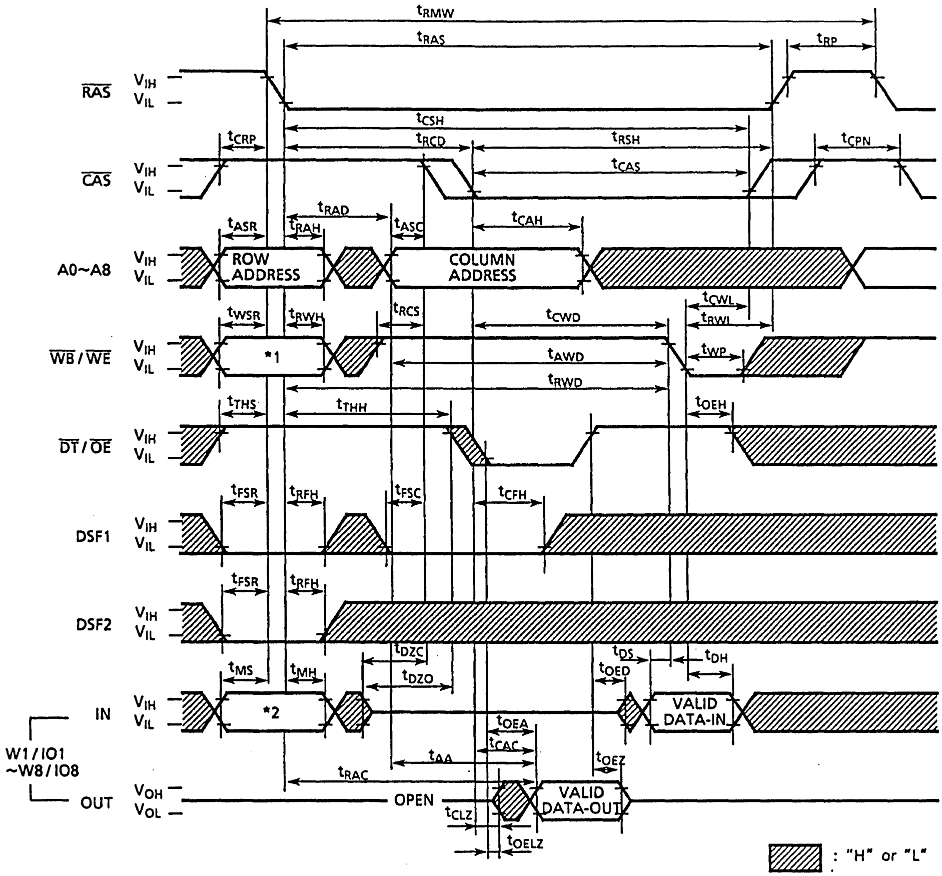


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

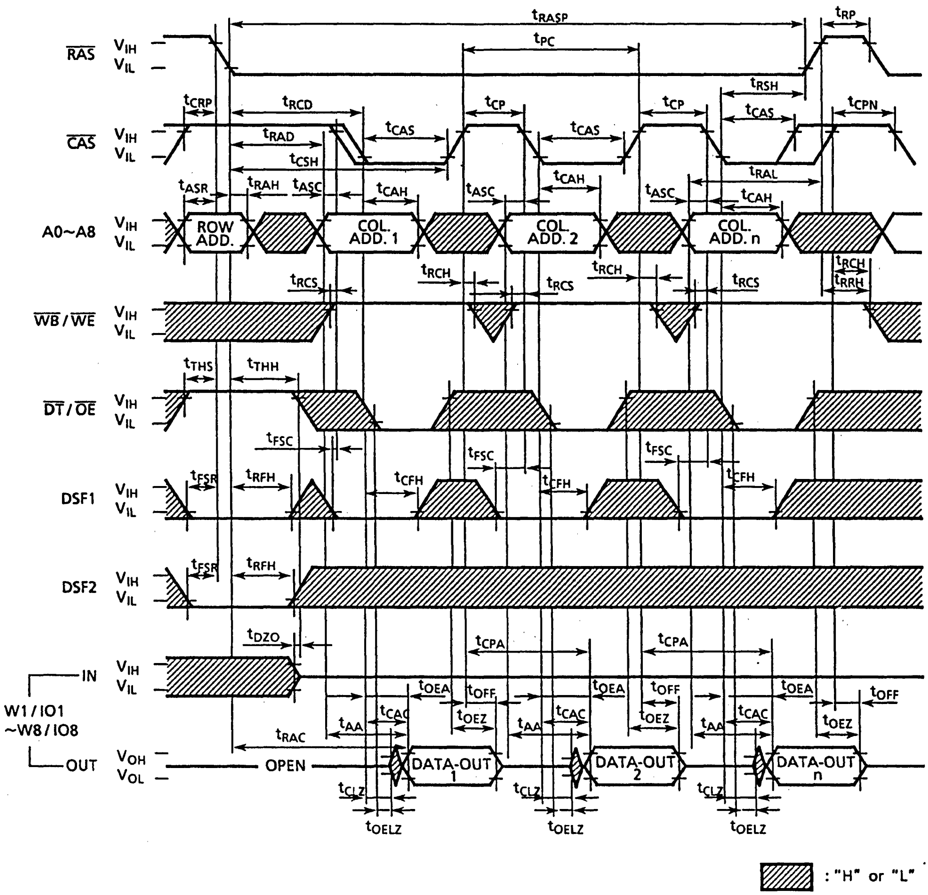
READ-MODIFY-WRITE CYCLE



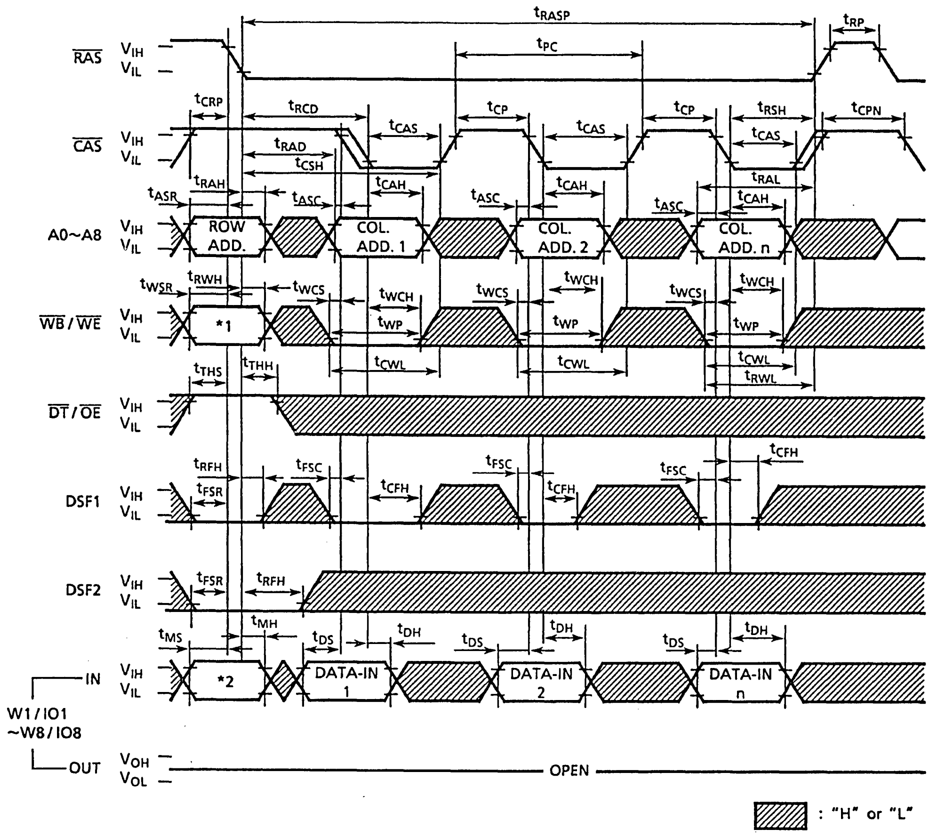
Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable
Don't care : '1' or '0'

FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

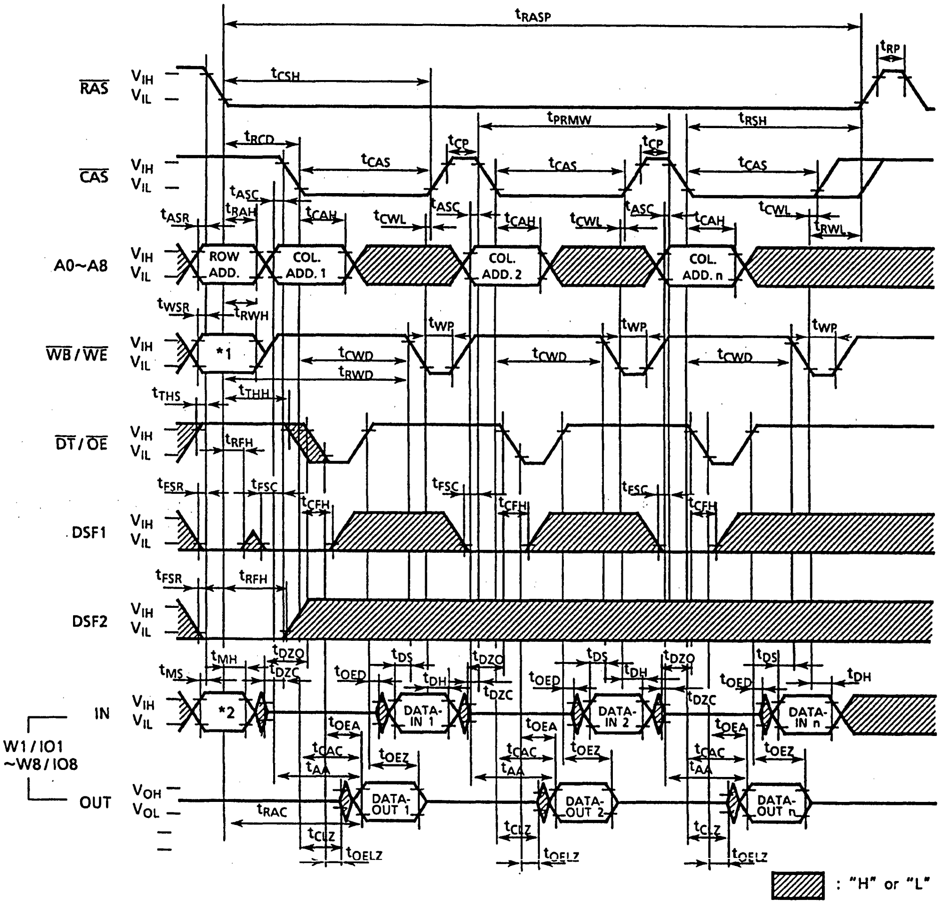


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

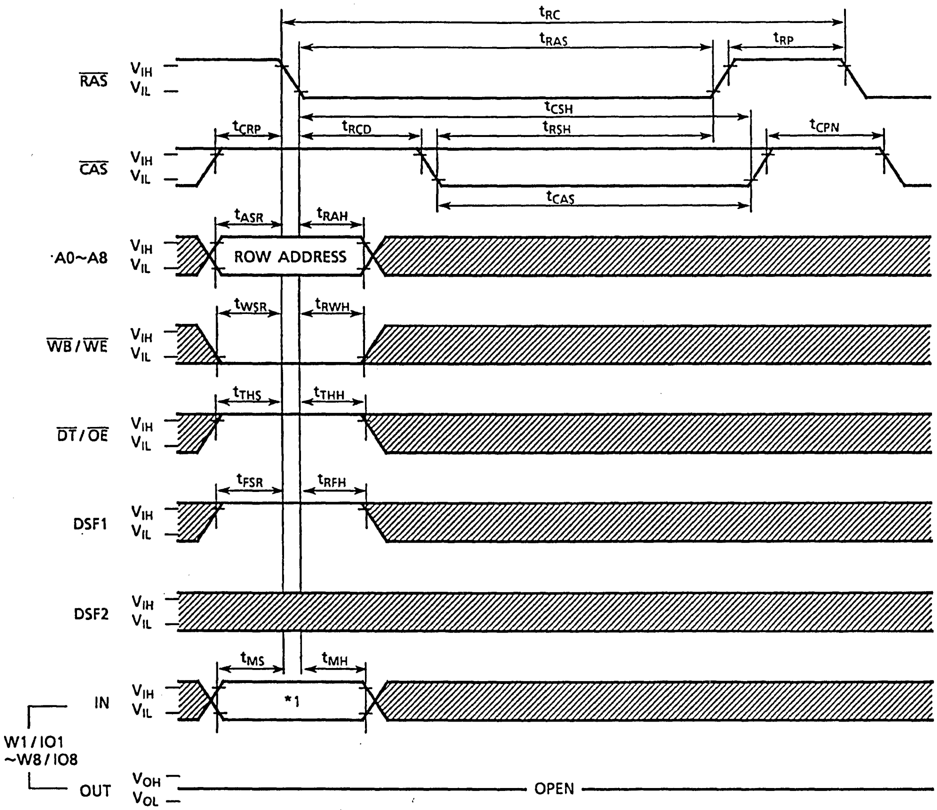


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

FLASH WRITE CYCLE

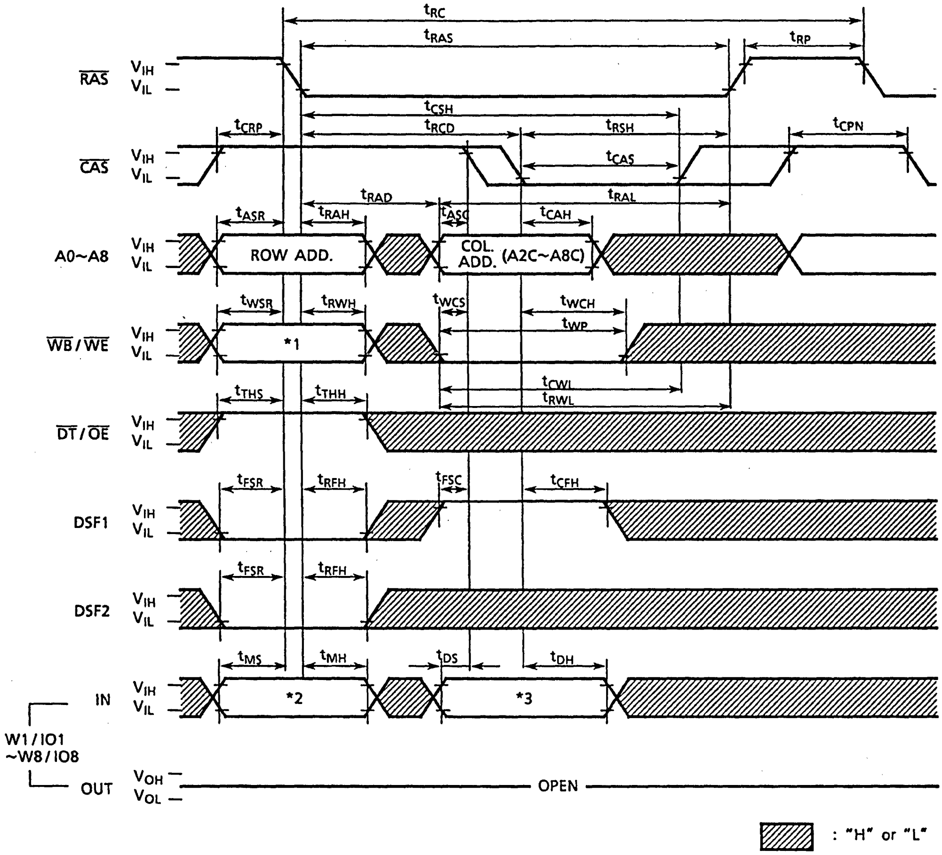


Mask Mode	Cycle
New Mask Mode	WM1 data
Old Mask Mode	Don't care

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

BLOCK WRITE CYCLE (EARLY WRITE)



Mask Mode	*1	*2
No Mask Mode	1	Don't care
New Mask Mode	0	WM1 data
Old Mask Mode	0	Don't care

WM1 data 0: Write Disable
1: Write Enable

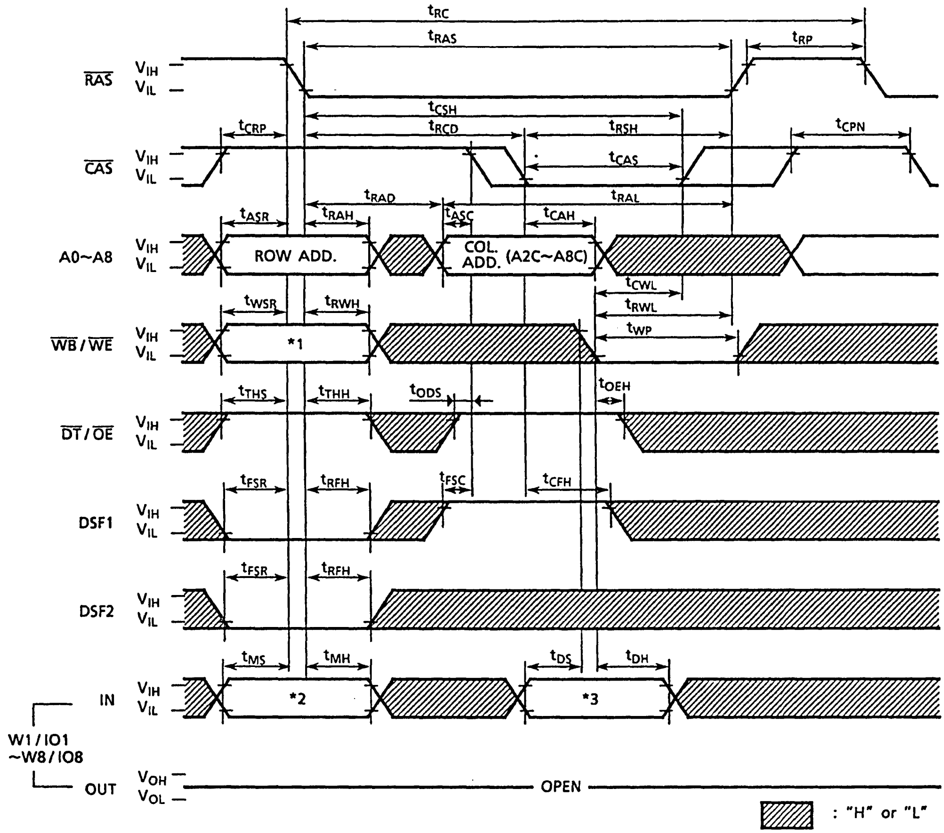
Don't care : '1' or '0'

***3 COLUMN SELECT**

W1/IO1 - Column 0 ($A_{1C} = 0$, $A_{0C} = 0$)
W2/IO2 - Column 1 ($A_{1C} = 0$, $A_{0C} = 1$)
W3/IO3 - Column 2 ($A_{1C} = 1$, $A_{0C} = 0$)
W4/IO4 - Column 3 ($A_{1C} = 1$, $A_{0C} = 1$)

Wn/IOn
= 0 : Disable
= 1 : Enable

BLOCK WRITE CYCLE (DELAYED WRITE)



Mask Mode	*1	*2
No Mask Mode	1	Don't care
New Mask Mode	0	WM1 data
Old Mask Mode	0	Don't care

WM1 data 0: Write Disable
1: Write Enable

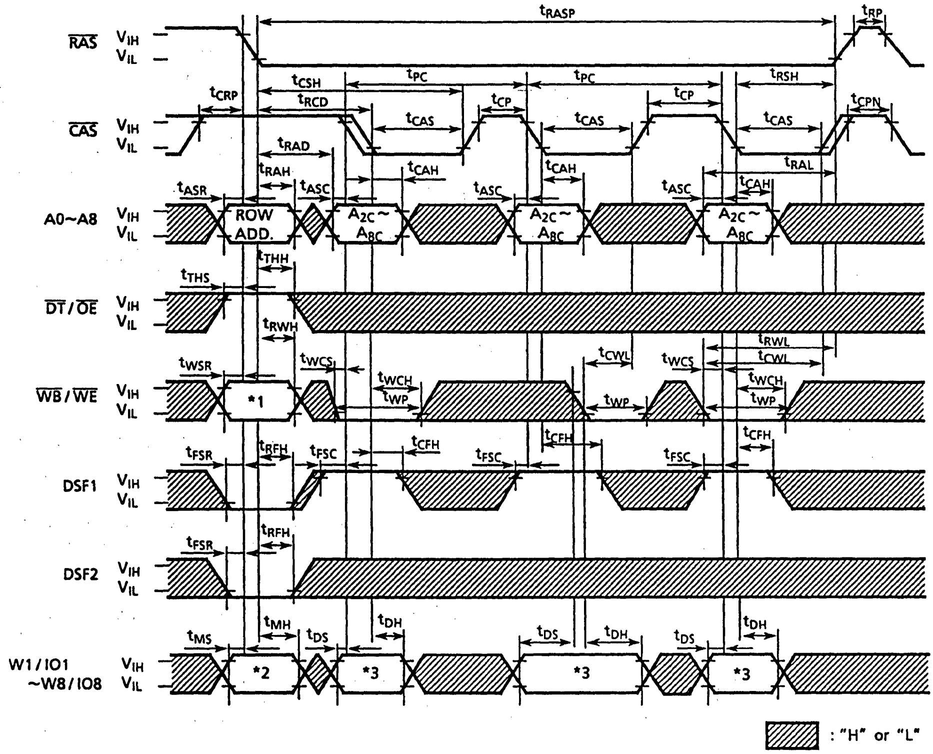
Don't care : '1' or '0'

*3 COLUMN SELECT

W1/IO1 - Column 0 ($A_{1C} = 0$, $A_{0C} = 0$)
W2/IO2 - Column 1 ($A_{1C} = 0$, $A_{0C} = 1$)
W3/IO3 - Column 2 ($A_{1C} = 1$, $A_{0C} = 0$)
W4/IO4 - Column 3 ($A_{1C} = 1$, $A_{0C} = 1$)

Wn/IOn
= 0 : Disable
= 1 : Enable

FAST PAGE MODE BLOCK WRITE CYCLE



Mask Mode	*1	*2
No Mask Mode	1	Don't care
New Mask Mode	0	WM1 data
Old Mask Mode	0	Don't care

WM1 data — 0: Write Disable
1: Write Enable

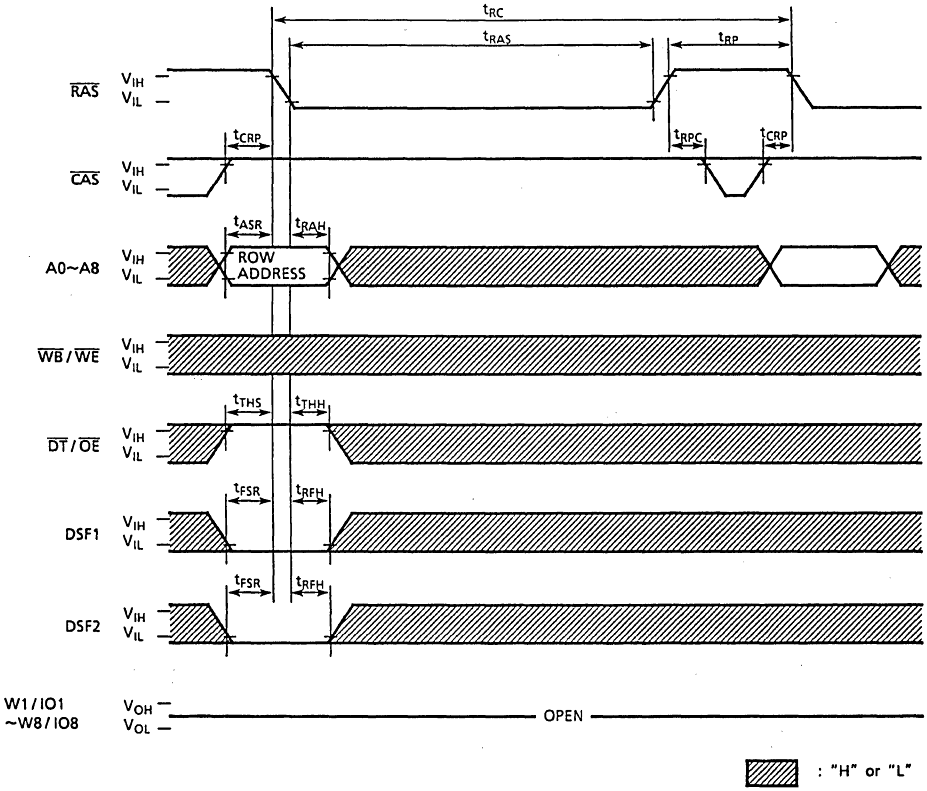
Don't care — : '1' or '0'

*3 COLUMN SELECT

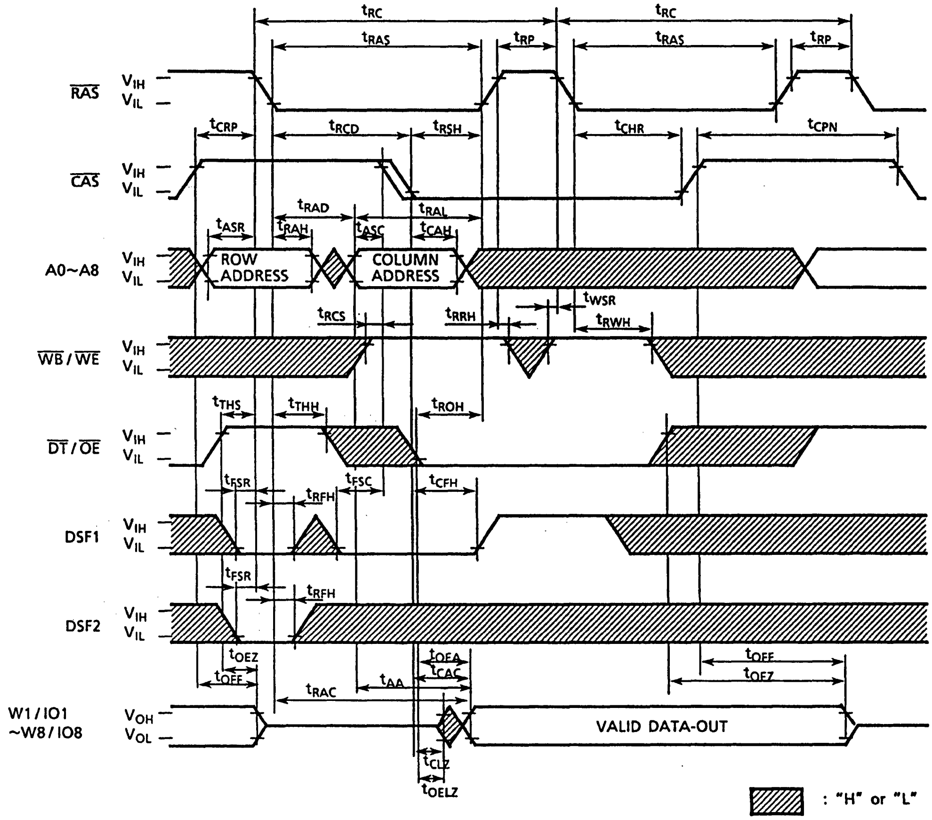
W1/IO1 - Column 0 ($A_{1C} = 0$, $A_{0C} = 0$)
W2/IO2 - Column 1 ($A_{1C} = 0$, $A_{0C} = 1$)
W3/IO3 - Column 2 ($A_{1C} = 1$, $A_{0C} = 0$)
W4/IO4 - Column 3 ($A_{1C} = 1$, $A_{0C} = 1$)

Wn/IOn
= 0 : Disable
= 1 : Enable

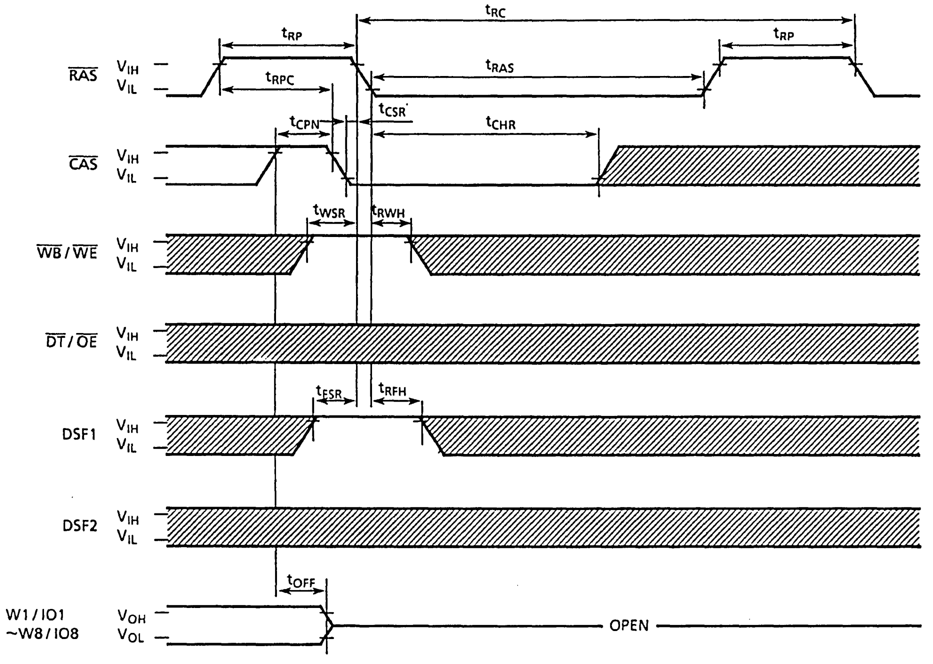
$\overline{RAS}$ ONLY REFRESH CYCLE



HIDDEN REFRESH CYCLE



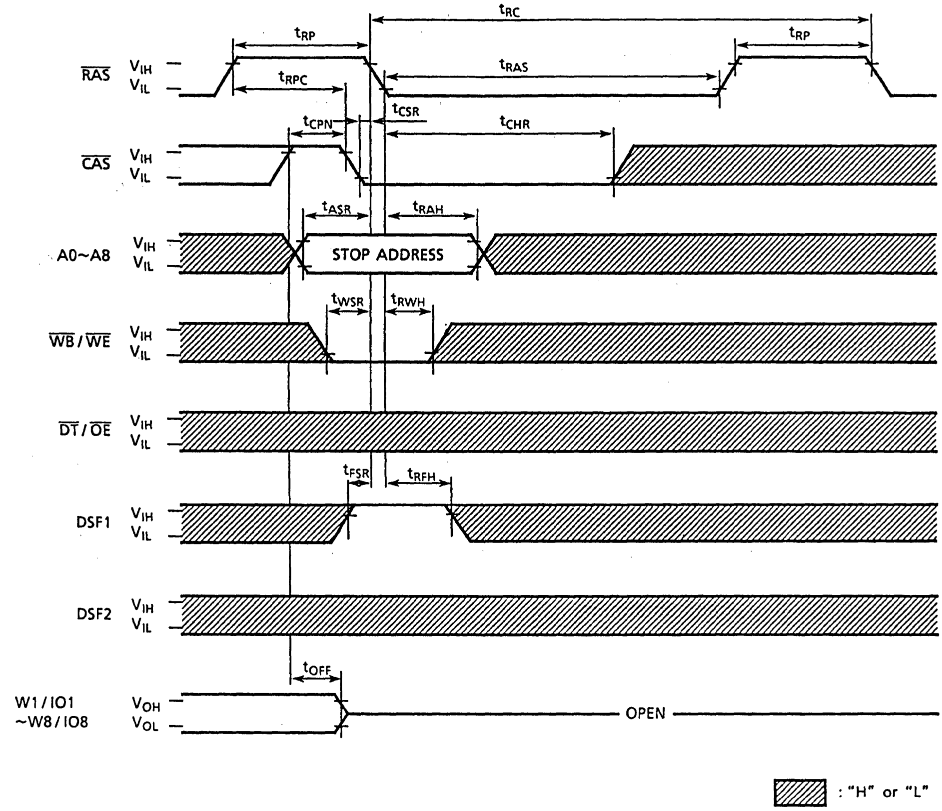
CBR AUTO REFRESH CYCLE



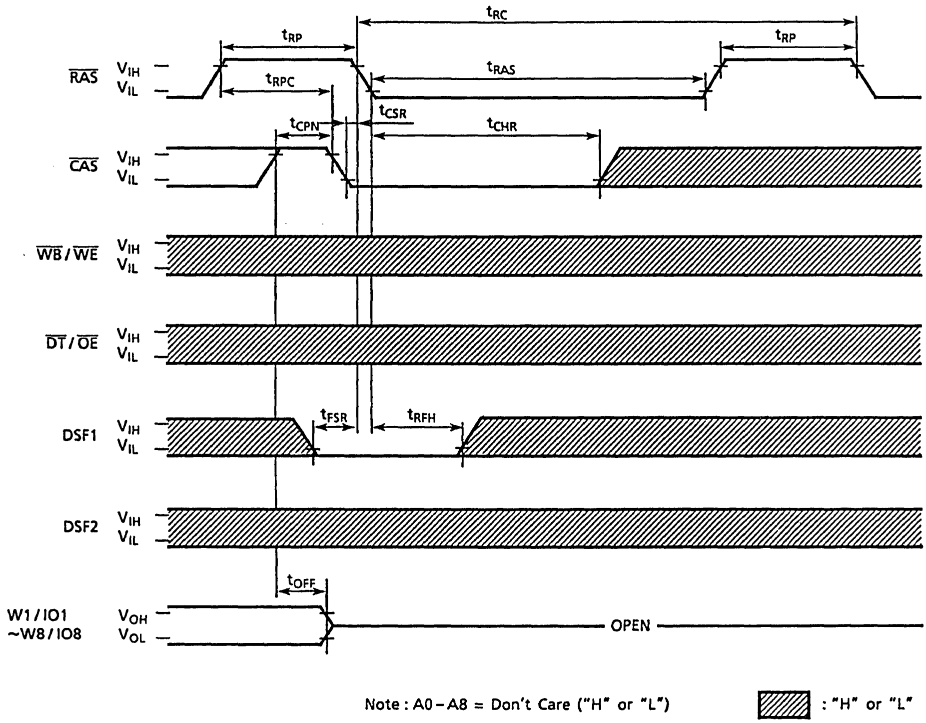
Note : A0 – A8 = Don't Care ("H" or "L")


: "H" or "L"

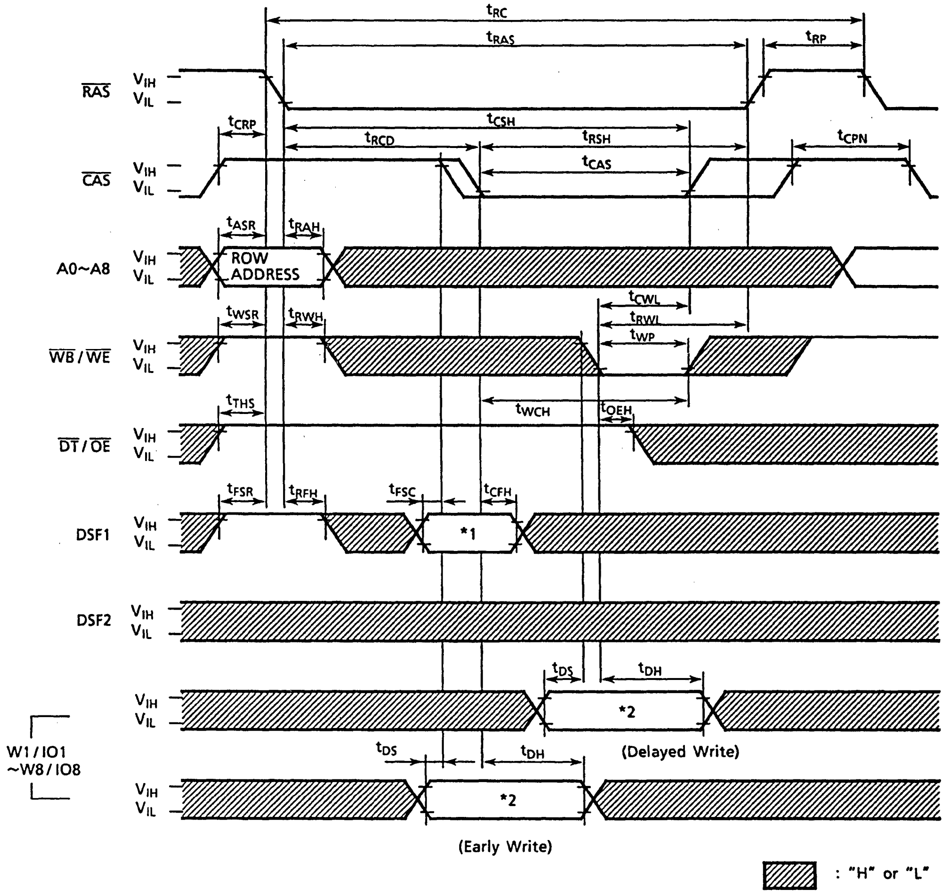
CBR AUTO REFRESH & STOP REGISTER SET CYCLE



CBR AUTO REFRESH & RESET CYCLE

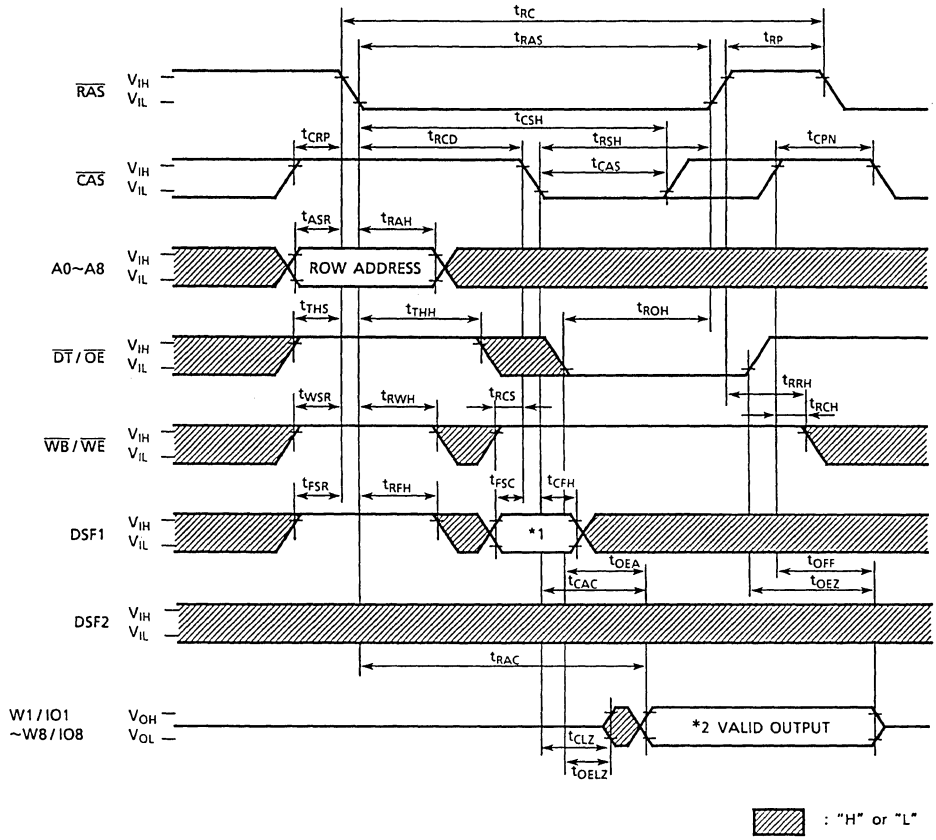


LOAD MASK/COLOR REGISTER CYCLE



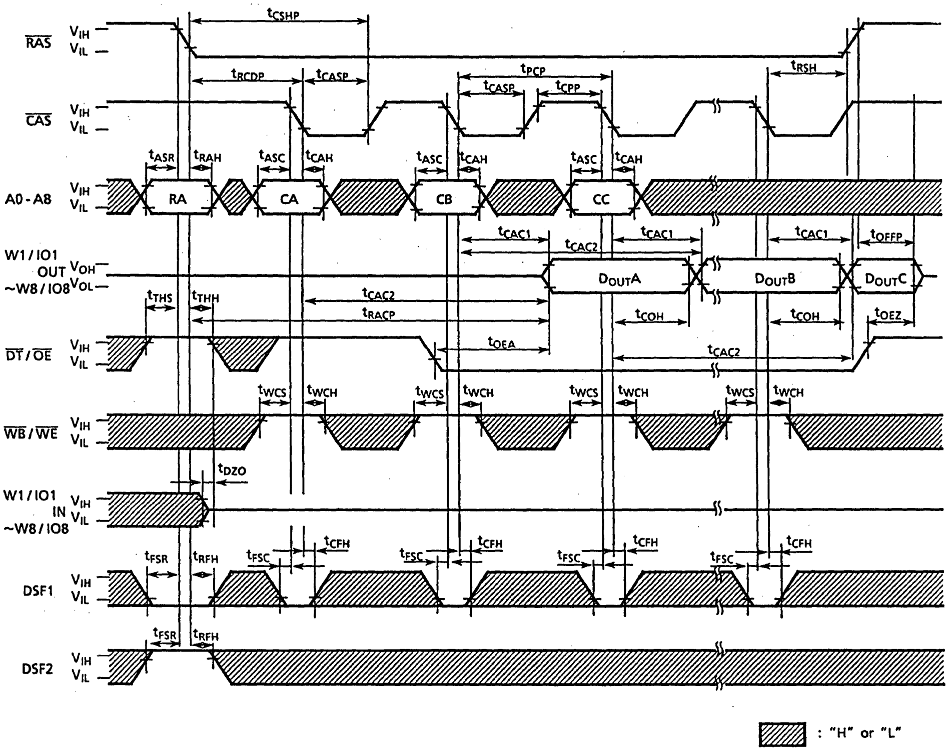
*1	*2	Function
0	Mask data	Load Mask Register Cycle
1	Color data	Load Color Register Cycle

READ MASK/COLOR REGISTER CYCLE

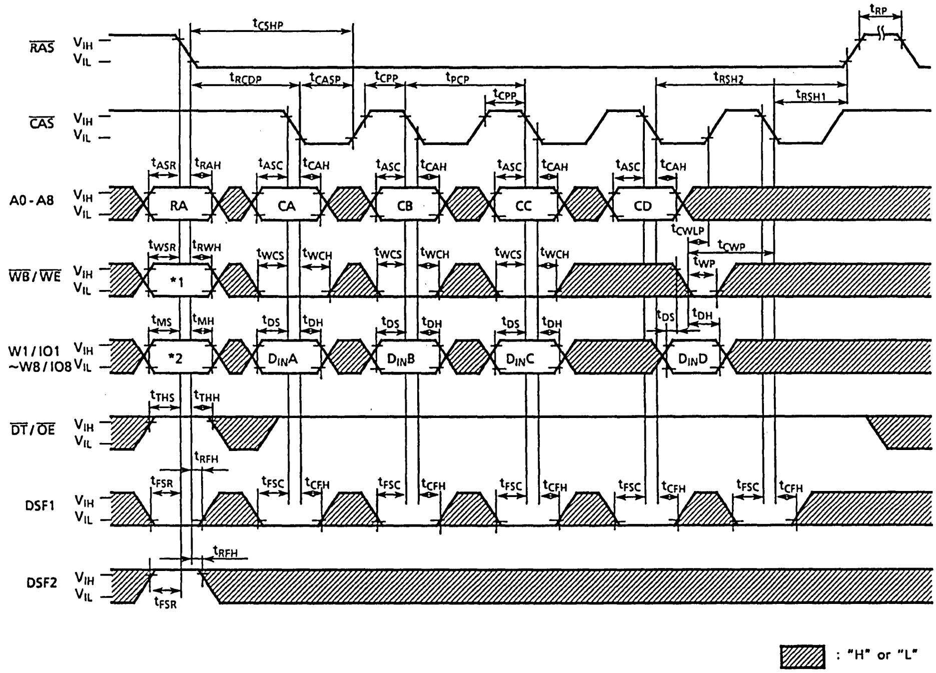


*1	*2	Function
0	Mask data	Load Mask Register Cycle
1	Color data	Load Color Register Cycle

PIPELINED FAST PAGE READ CYCLE



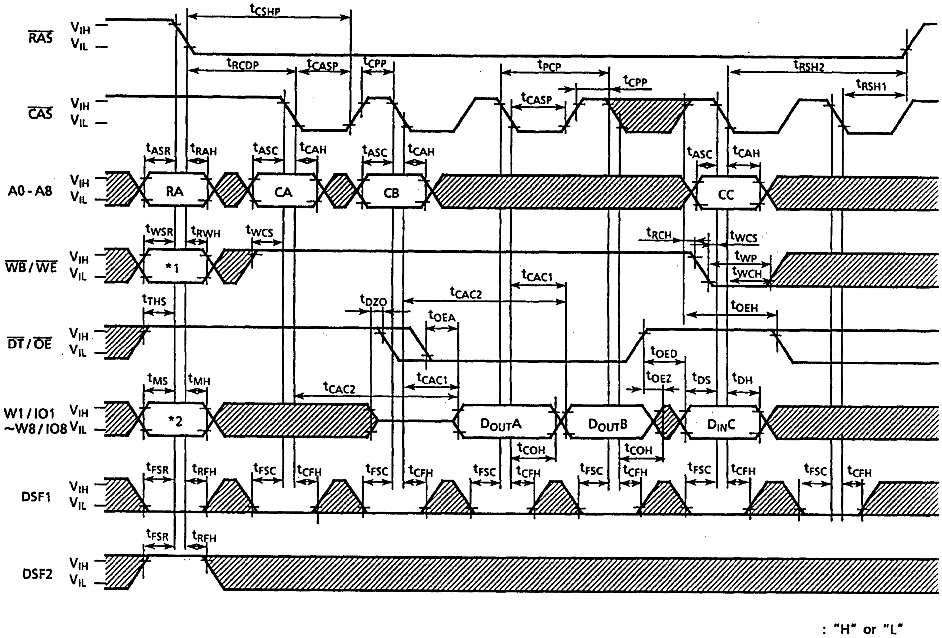
PIPELINED FAST PAGE WRITE CYCLE



Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable
Don't care : '1' or '0'

PIPELINED FAST PAGE READ-WRITE CYCLE

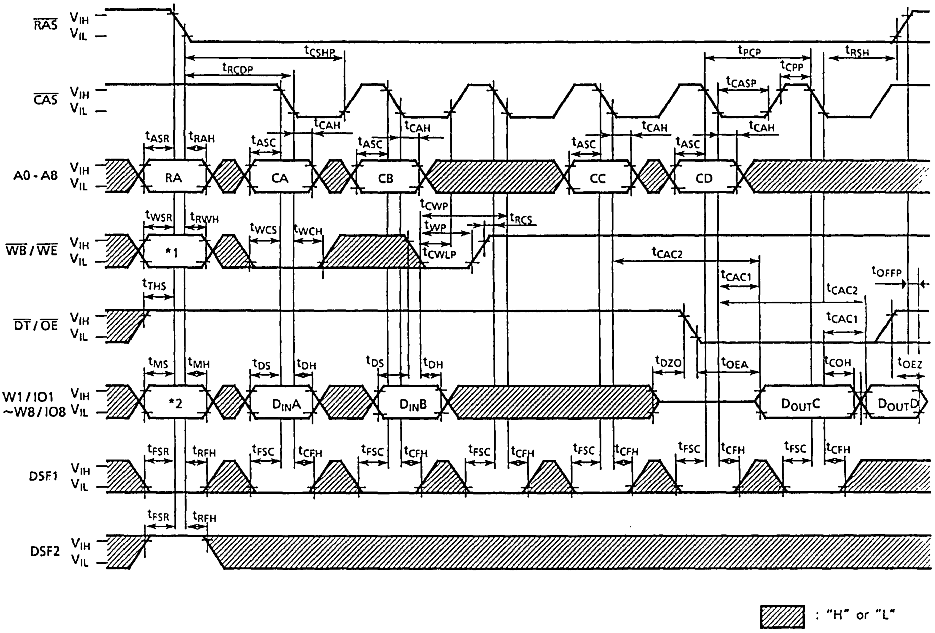


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

PIPELINED FAST PAGE WRITE-READ CYCLE

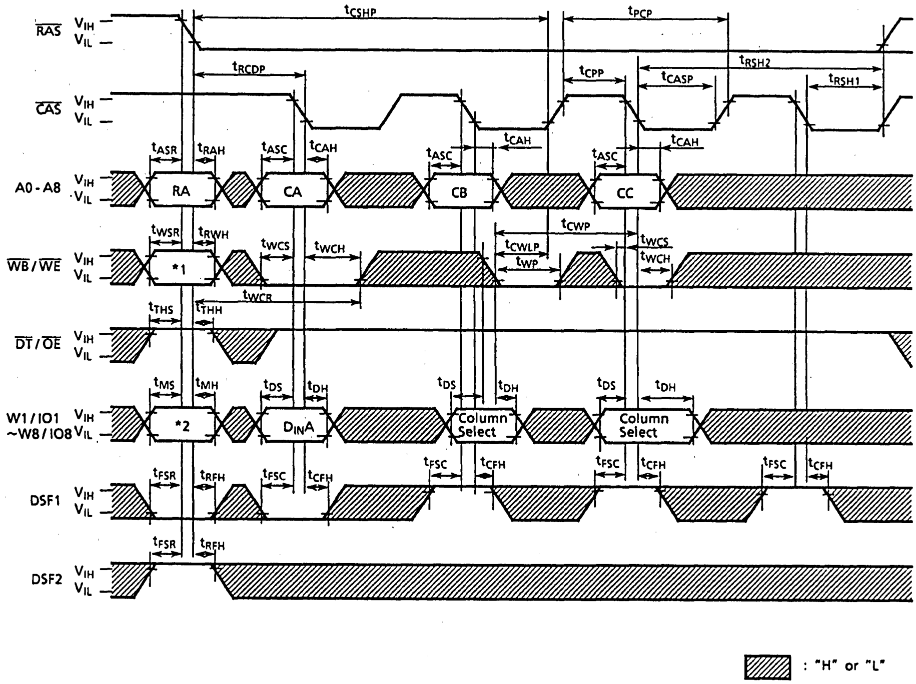


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

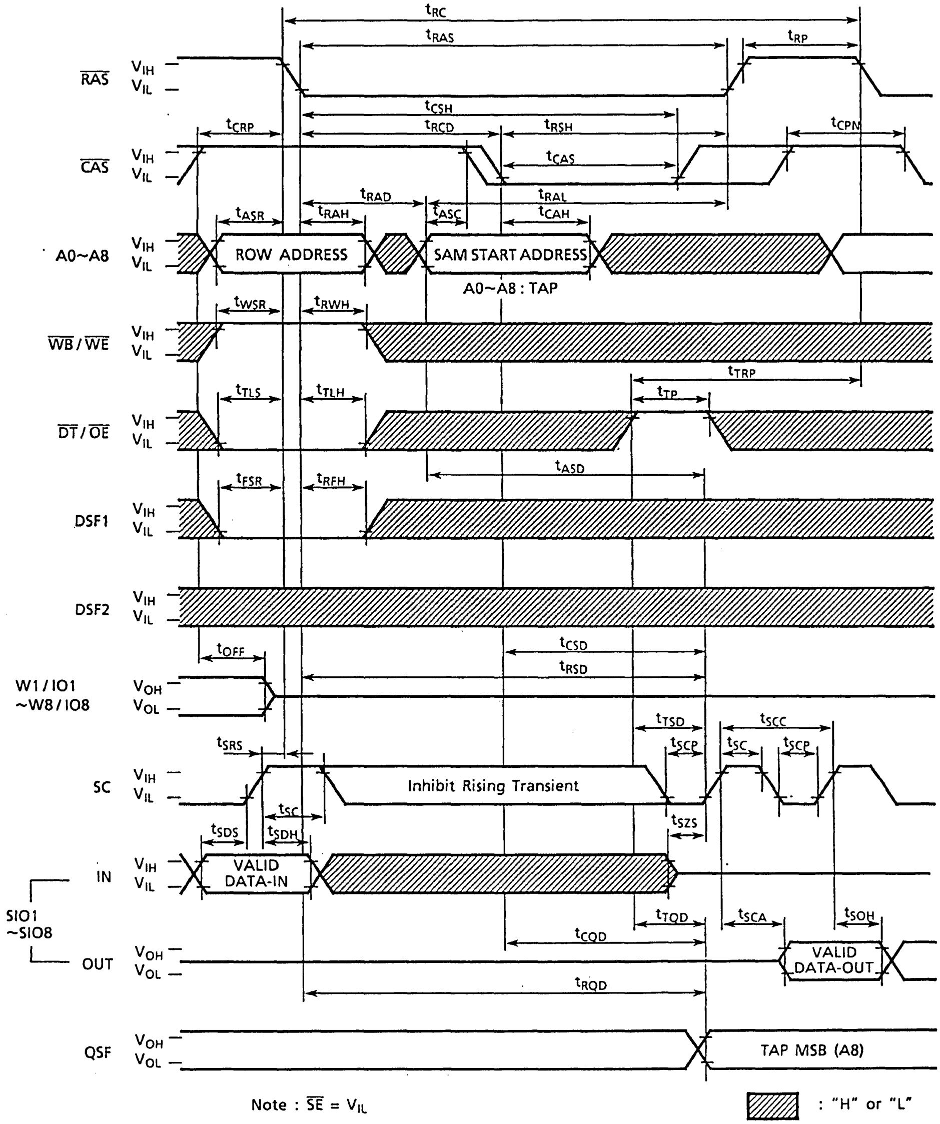
PIPELINED FAST PAGE WRITE-BLOCK WRITE CYCLE



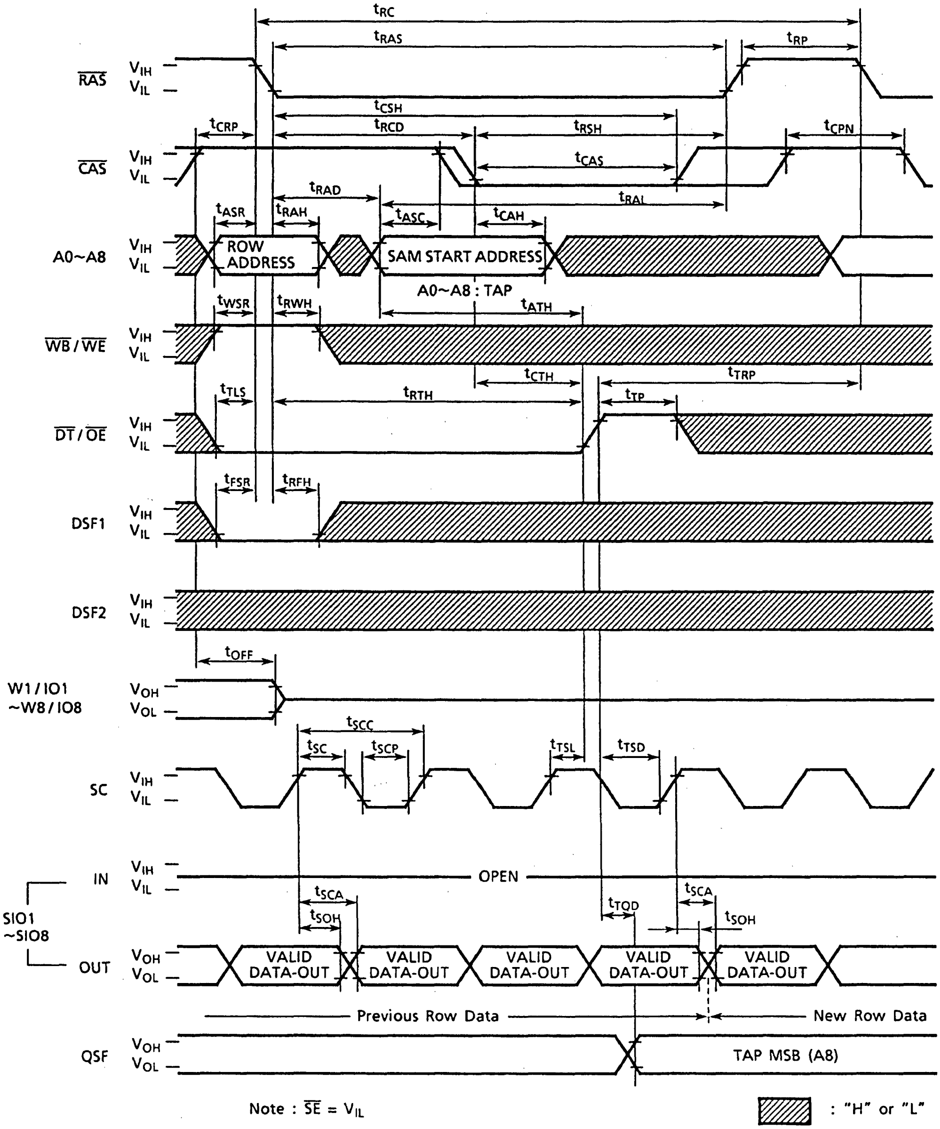
Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable
Don't care : '1' or '0'

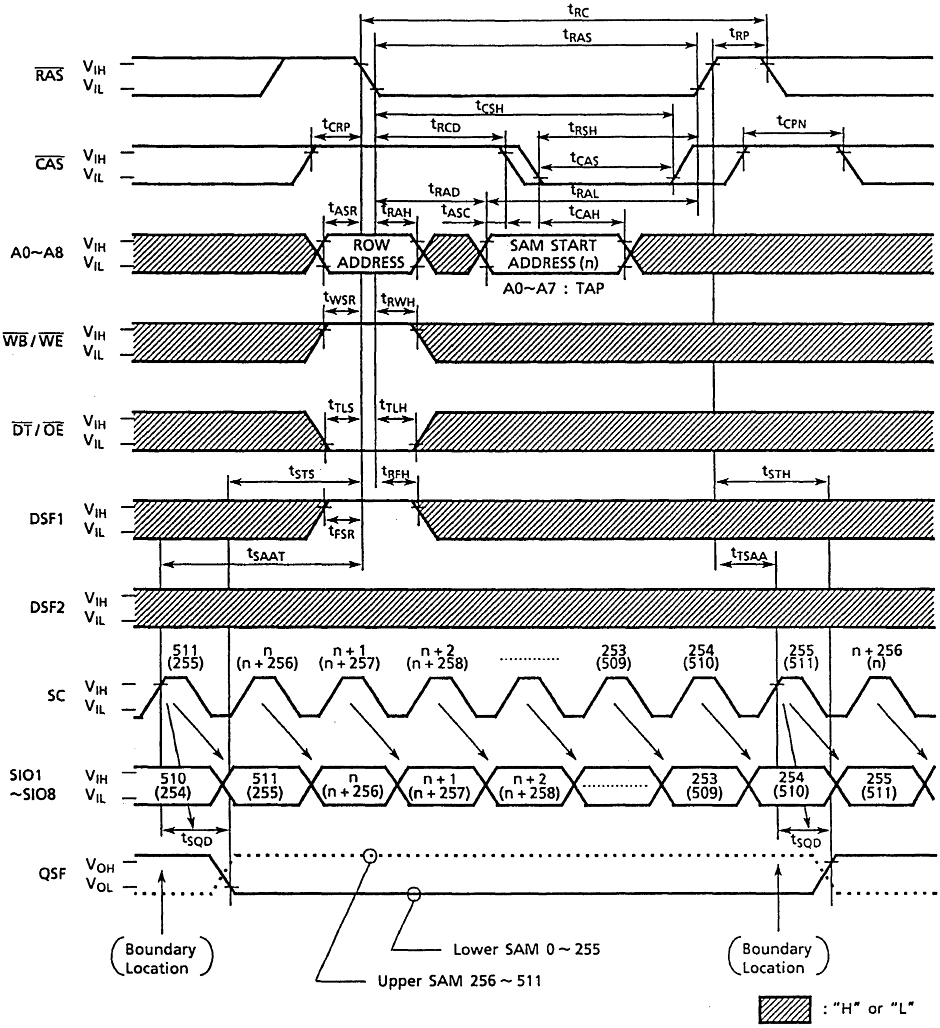
READ TRANSFER CYCLE (Previous Transfer is Write Transfer Cycle)



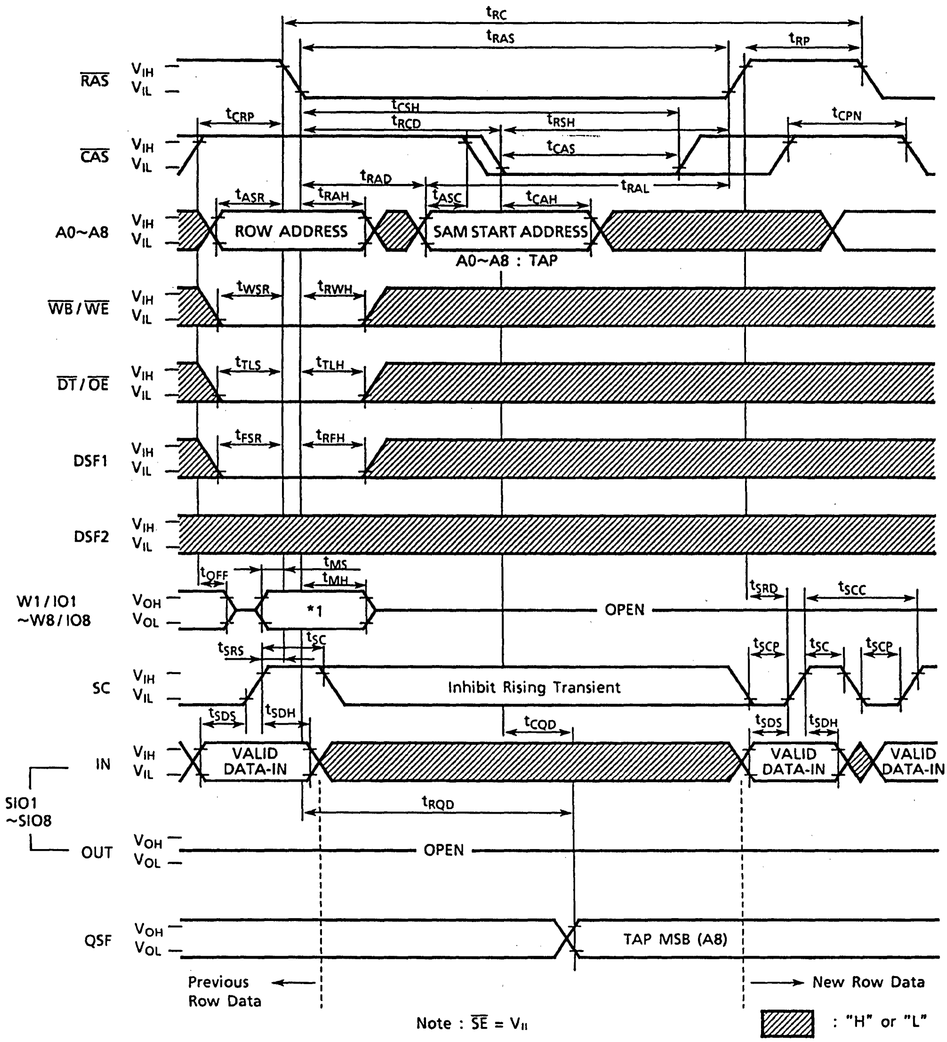
REAL TIME READ TRANSFER CYCLE



SPLIT READ TRANSFER CYCLE



MASKED WRITE TRANSFER CYCLE

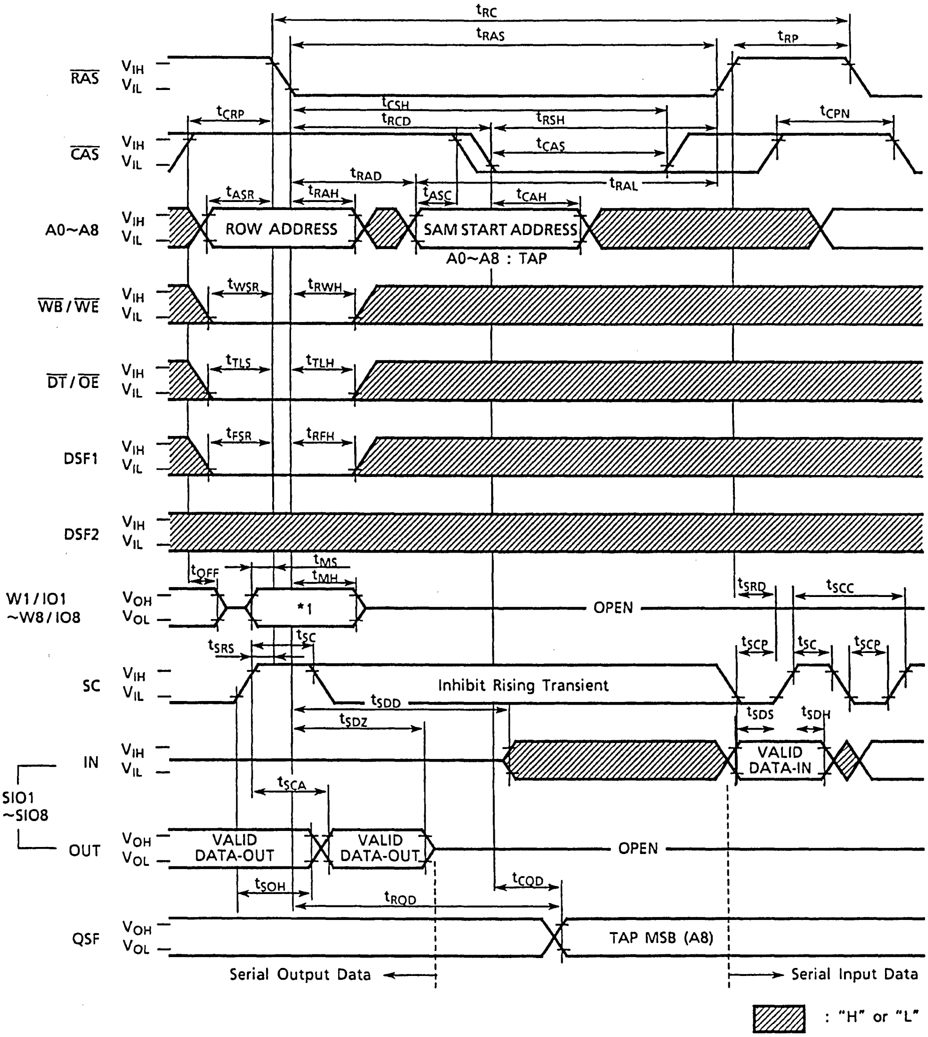


Mask Mode	*1
New Mask Mode	WM1 data
Old Mask Mode	Don't care

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

MASKED WRITE TRANSFER CYCLE (Previous Transfer is Read Transfer Cycle)

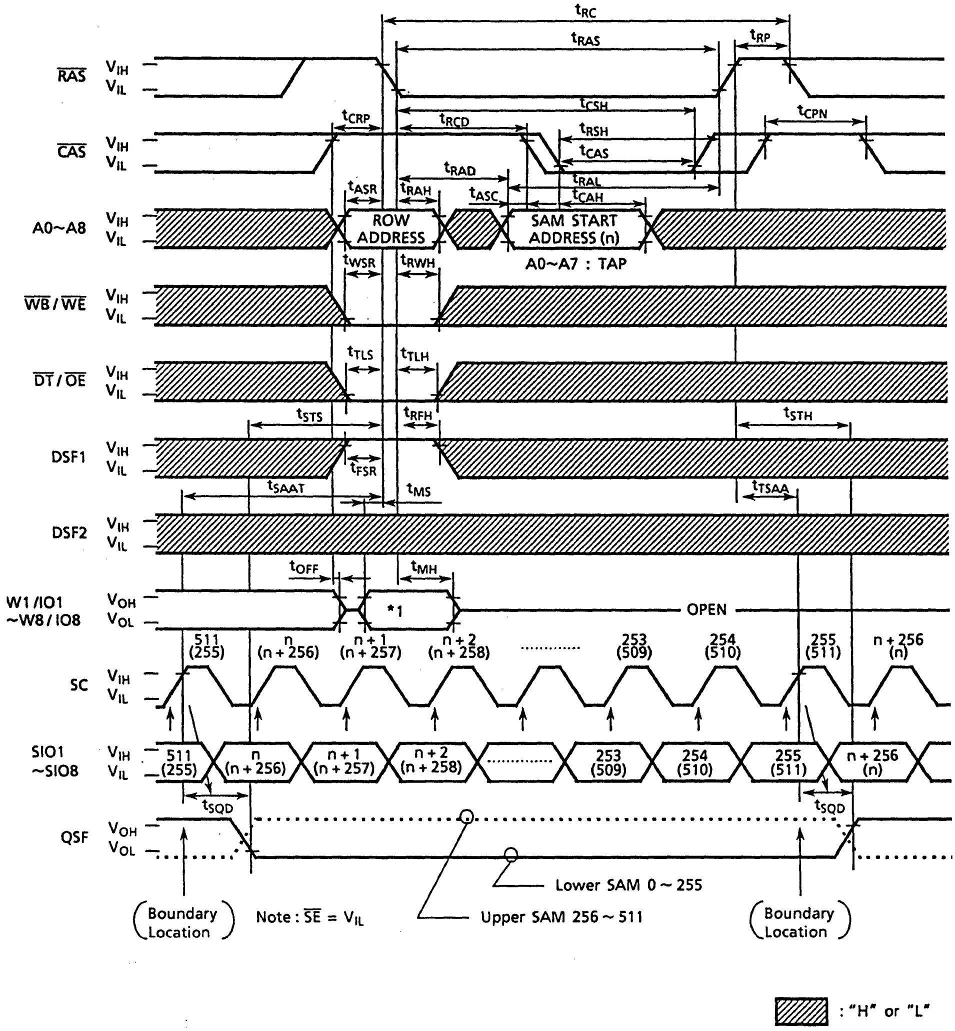


Mask Mode	*1
New Mask Mode	WM1 data
Old Mask Mode	Don't care

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

MASKED SPLIT WRITE TRANSFER CYCLE

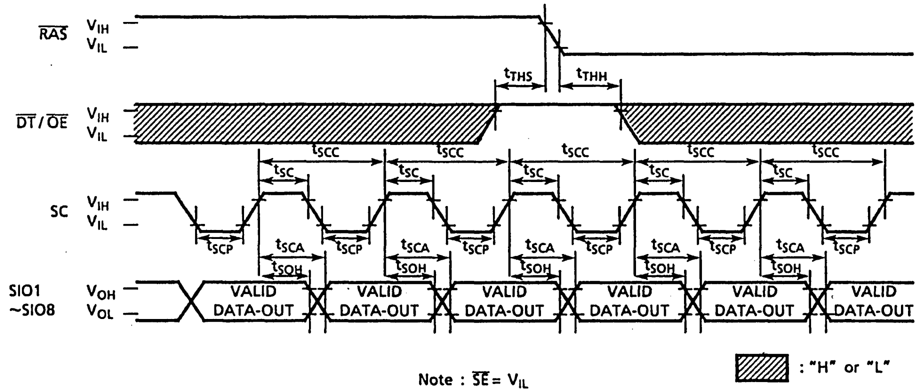


Mask Mode	*1
New Mask Mode	WM1 data
Old Mask Mode	Don't care

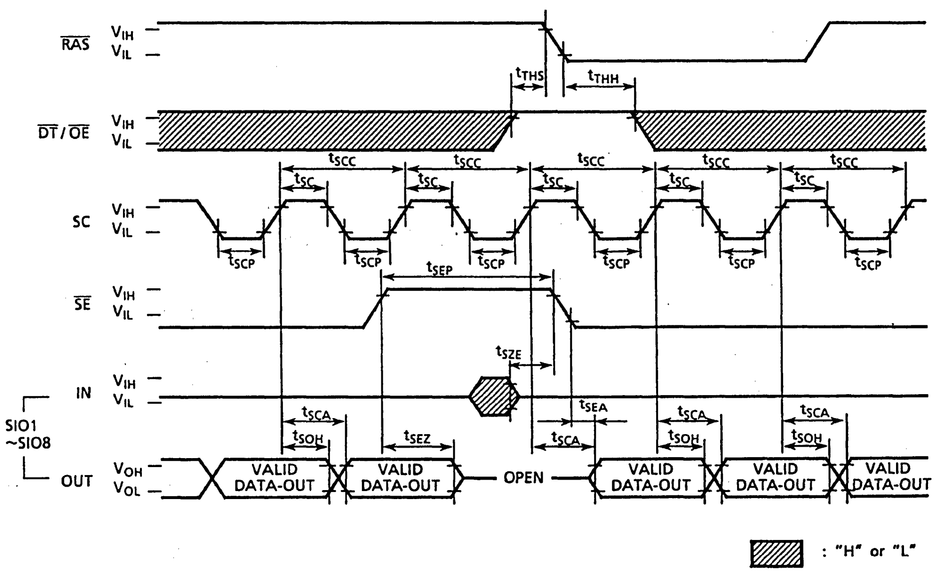
WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

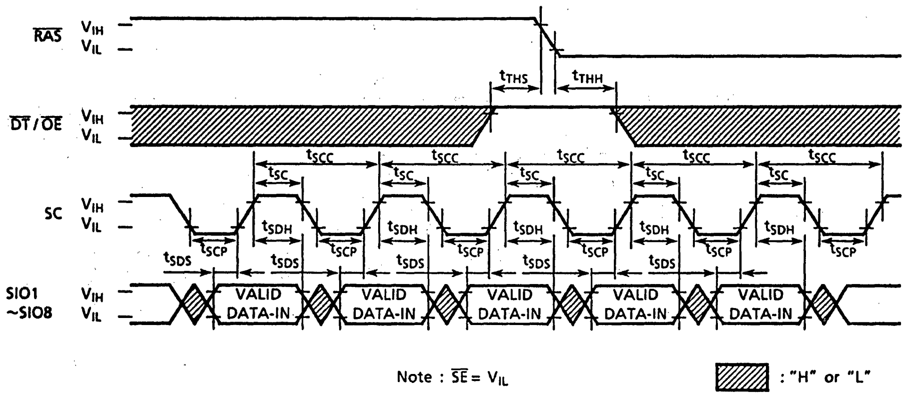
SERIAL READ CYCLE ($\overline{SE}$ = V_{IL})



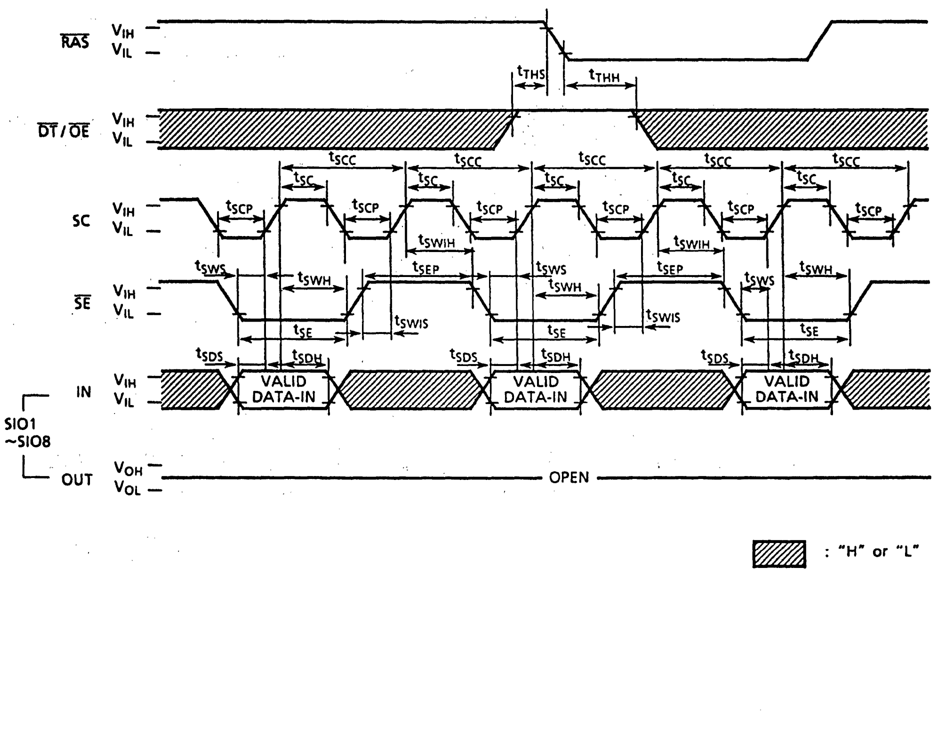
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



SERIAL WRITE CYCLE ($\overline{SE}$ = V_{IL})



SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



PIN FUNCTION

ADDRESS INPUTS : A_0~A_8

The 18 address bits required to decode 8 bits of the 2,097,152 cell locations within the dynamic RAM memory array and they are multiplexed onto 9 address input pins (A_0~A_8). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

ROW ADDRESS STROBE : $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, DSF1 and DSF2 to invoke the various random access and data transfer operating modes shown in Table 1. $\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high".

COLUMN ADDRESS STROBE : $\overline{CAS}$

$\overline{CAS}$ is the control input that latches the column address bits which are also used for the tap address during the transfer operations. The state of the special function input DSF1 is read at the $\overline{CAS}$ falling edge to select the block write mode or load register functions in conjunction with the $\overline{RAS}$ control. $\overline{CAS}$ before $\overline{RAS}$ refresh operations are selected if the signal is "low" at the $\overline{RAS}$ falling edge.

DATA TRANSFER/OUTPUT ENABLE : $\overline{DT}/\overline{OE}$

The $\overline{DT}/\overline{OE}$ input is a multifunction pin. When $\overline{DT}/\overline{OE}$ is "high" at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT}/\overline{OE}$ is used as an output enable control. If it is "low", a data transfer operation is activated between the RAM and the SAM.

WRITE PER BIT/WRITE ENABLE : $\overline{WB}/\overline{WE}$

The $\overline{WB}/\overline{WE}$ input is also a multifunction pin. When the signal is "high" at the falling edge of $\overline{RAS}$, during the RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. If the signal is "low" at the $\overline{RAS}$ falling edge, the write-per-bit function is enabled. The $\overline{WB}/\overline{WE}$ input also determines the direction of data transfer between the RAM array and the SAM.

WRITE MASK DATA/DATA INPUT AND OUTPUT: $W_1/IO_1 \sim W_8/IO_8$

Data is written into the RAM through $W_1/IO_1 \sim W_8/IO_8$ pins during a write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs late. In a read cycle data is read out of the RAM on the W_i / IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and column address. The 4 least bits are also used as the column address mask during a block write cycle.

When the write-per-bit function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register at the falling edge of $\overline{RAS}$. In a load mask and color register cycles, the data on the W_i/IO_i pins is stored into the write mask register and the color register respectively.

SERIAL CLOCK : SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. The serial clock SC also increments the 9-bits serial pointer which is used to select the SAM address. The SC pin must be held at a constant V_{IH} or V_{IL} level during read and masked write transfer operations and should not be clocked while the SAM is in standby mode to prevent the SAM pointer from being incremented.

SERIAL ENABLE : $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer is still incremented while SC is clocked.

SPECIAL FUNCTION CONTROL INPUT: DSF 1, DSF 2

DSF1 is latched at the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to select the various TC528257J/Z/FT/TR operations. If the signal is kept "low", the basical functions featured in conventional multi-port DRAM are enabled. To use the block write, the flash write and the load register functions or the split transfer operations, the DSF1 signal needs to be controlled as shown in Table 1.

When the DSF2 signal is "high" at the falling edge of $\overline{RAS}$, pipelined page mode operations are enabled. The pipeline mode is supported with the read, write and block write functions.

SPECIAL FUNCTION OUTPUT: QSF

QSF is an output signal which, during split register mode, indicates which half of the split SAM is being accessed. QSF "low" indicates that the lower split SAM (Bit 0~255) is being accessed and QSF "high" indicates that the upper split SAM (Bit 256~511) is being accessed. QSF is monitored so that after it toggles and after allowing for a delay of t_{STS}, split read/write transfer operation can be performed on the non-active split SAM.

SERIAL INPUT/OUTPUT : SIO_1, SIO_8

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read or masked write transfer cycle. After a read cycle, the SI/Oi pin is in the output mode. When a masked write transfer cycle is performed, the SI/Oi is switched from output mode to input mode,

OPERATION MODE

The RAM port and data transfer operating of the TG528257 are determined by the state of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, DSF1 and DSF2 at the falling edge of $\overline{RAS}$ and by the state of DSF1 at the falling edge of $\overline{CAS}$. The Table 1 shows the functional truth table for a listing of all available RAM port and transfer operations.

Table 1. Operaton Truth Table

$\overline{\text{RAS}}$ ↓					$\overline{\text{CAS}}$ ↓	Mnemonic Code	Function
CAS	$\overline{\text{DT}}/\overline{\text{OE}}$	$\overline{\text{WB}}/\overline{\text{WE}}$	DSF1	DSF2	DSF1		
0	*	*	0	*	-	CBR	CBR Auto Refresh & Option Reset [1), 2)]
0	*	0	1	*	-	CBRS	CBR Auto Refresh & Stop Register Set[2)]
0	*	1	1	*	-	CBRN	CBR Auto Refresh
1	0	0	0	*	*	MWT	Write Transer (New/Old Mask)[1)]
1	0	0	1	*	*	MSWT	Split Write Transfer (New/Old Mask)[1)]
1	0	1	0	*	*	RT	Read Transfer
1	0	1	1	*	*	SRT	Split Read Transfer
1	1	0	0	0	0	RWM	Read Write (New/Old Mask)[1)]
1	1	0	0	0	1	BWM	BlockWrite (New/Old Mask)[1)]
1	1	0	1	*	*	FWM	FlashWrite (New/Old Mask)[1)]
1	1	1	0	0	0	RW	Read Write (No Mask)
1	1	1	0	0	1	BW	Block Write (No Mask)
1	1	0	0	1	0	RWM(P)	PFP[3)] Read Write (New/Old Mask)[1)]
1	1	0	0	1	1	BWM(P)	PFP[3)] Block Write (New/Old Mask)[1)]
1	1	1	0	1	0	RW(P)	PFP[3)] Read Write (No Mask)
1	1	1	0	1	1	BW(P)	PFP[3)] Block Write (No Mask)
1	1	1	1	*	0	LMR	Load (Old) Mask Register[1)]
1	1	1	1	*	1	LCR	Load Color Register

Note : * =0 or 1, - = Not applicable

1) After LMR operation, MWT, MSWT, RWM, BWM, FWM, RWM (P), BWM (P) use old mask. CBR operation resets the old mask mode to new mask mode.
2) CBRS operation determines binary boundaries in the SAM. CBR operation resets the boundaries.
3) PFP stands for pipelined fast page mode

RAM PORT OPERATION

1. READ WRITE FUNCTION : RW

The TC528257 is equipped with the read write function which is identical to the conventional dynamic RAM's one and supports read, early write, $\overline{OE}$ controlled write and read-modify-write cycles as shown in the timing charts. Fast page and pipelined page modes are available with the read write cycles by performing multiple $\overline{CAS}$ cycles during a single active $\overline{RAS}$ cycle, a page.

2. WRITE-PER-BIT (MASKED WRITE) FUNCTION : RWM

The write-per-bit (masked write) function selectively controls the internal write enable circuits of the RAM port. When $\overline{WB/WE}$ is held "low" at the falling edge of $\overline{RAS}$, during the RWM cycle, the write mask is enabled. At the same time, the mask data on the Wi/IOi pins is latched into the write-mask register. The I/O mask data maintains in a single $\overline{RAS}$ cycle, a page (New Mask Mode). When a load mask register function (LMR) is performed, the write mask data on the Wi/IOi pins is latched into the write-mask register. After the LMR operation, the data at the falling edge of $\overline{RAS}$ during the RWM cycle is ignored and the I/O mask data that was stored in the write-mask register is used (Old Mask Mode) until the mode is reset by CBR operation The truth table of the write-per-bit functon is shown in Table 2.

Table 2. Truth table for write-per-bit function

<table>
<tr><th colspan="4">At the falling edge of $\overline{RAS}$</th><th rowspan="2">Write Mask Register</th><th rowspan="2">Function</th></tr>
<tr><th>$\overline{CAS}$</th><th>$\overline{DT/OE}$</th><th>$\overline{WB/WE}$</th><th>W_i/IO_i (i=1~8)</th></tr>
<tr><td rowspan="4">H</td><td rowspan="4">H</td><td rowspan="4">L</td><td>1</td><td>←</td><td>Write Enable</td></tr>
<tr><td>0</td><td>←</td><td>Write Disable (New Mask)</td></tr>
<tr><td>*</td><td>1</td><td>Write Enable</td></tr>
<tr><td>*</td><td>0</td><td>Write Disable (Old Mask)</td></tr>
</table>

Note: * = 1 or 0 , ← = The data on Wi/IOi is latched.

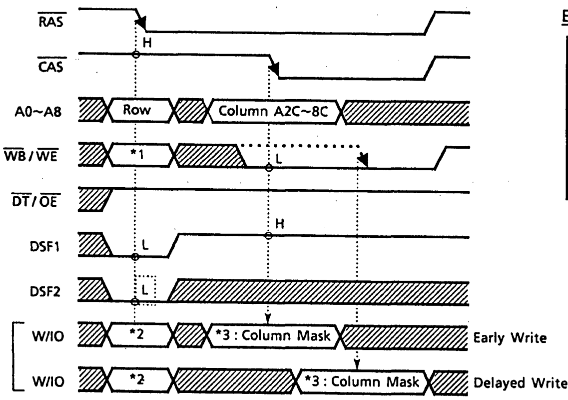
3. BLOCK WRITE AND MASKED BLOCK WRITE : BW & BWM

Block write is a special RAM port write operation which, in a page, allows for the data in the color register to be written into 4 consecutive column address locations starting from a selected column address in a selected row. The block write operation can be selectively disabled on an I/O basis and a column mask capability is also available.

A block write cycle is performed by holding $\overline{CAS}$, $\overline{DT}/\overline{OE}$ "high" and DSF1 "low" at the $\overline{RAS}$ falling edge and by holding DSF1 "high" at the $\overline{CAS}$ falling edge. If the DSF signal is "low" at the $\overline{CAS}$ falling edge, a read write operation will occur. Therefore, a combination of block write, read and write operations can be performed during a fast page mode cycle. The state of $\overline{WB}/\overline{WE}$ input at the falling edge of $\overline{RAS}$ determines whether or not the I/O mask is enabled ($\overline{WB}/\overline{WE}$ must be "low" to enable the I/O mask, BMW mode or "high" to disable it, BW mode). The I/O mask is provided on the Wi/IOi input at the $\overline{RAS}$ falling edge. After LMR operation, however, the old mask is used for the I/O mask function. The column mask data on the Wi/IOi input must be provided at the $\overline{CAS}$ or $\overline{WB}/\overline{WE}$ falling edge whichever is late, while the seven most significant colunm address (A2C~A8C) are latched at the falling edge of $\overline{CAS}$.

An example of the block write function is shown in Figure 1 with a mask on W_3/IO_3, W_4/IO_4, W_6/IO_6, W_8/IO_8 and column 1. The block write is most effective for window clear and fill operation in frame buffer applications.

Figure 1. Block Write Operation



Example

	W/IO							
	1	2	3	4	5	6	7	8
WM1 Register	1	1	(0)	(0)	1	(0)	1	(0)
Column Select	1	(0)	1	1	-	-	-	-
Color Register	1	0	1	0	1	1	0	0

Result

	W/IO							
	1	2	3	4	5	6	7	8
Column 0	1	0			1		0	
Column 1								
Column 2	1	0			1		0	
Column 3	1	0			1		0	

*1	*2	Mask Mode
1	Don't Care	No Mask Mode
0	WM1	New Mask Mode
0	Don't Care	Old Mask Mode

*3 COLUMN SELECT

W_1/IO_1 - Column 0 (A1C = 0, A0C = 0
W_2/IO_2 - Column 1 (A1C = 0, A0C = 1
W_3/IO_3 - Column 2 (A1C = 1, A0C = 0
W_4/IO_4 - Column 3 (A1C = 1, A0C = 1

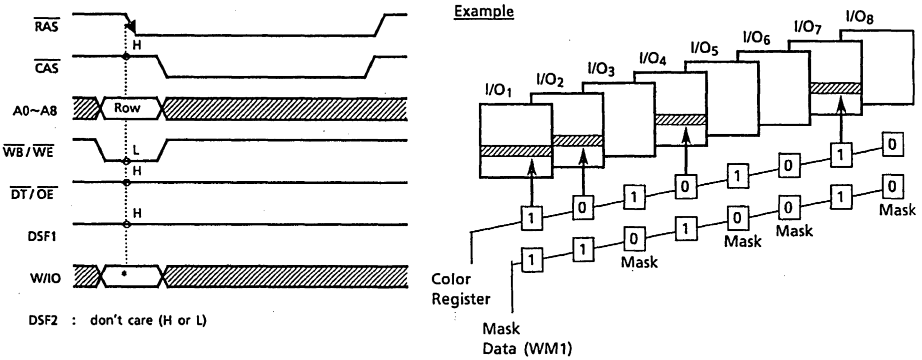
4. FLASH WRITE : FWM

Flash write is also a special RAM port operation which in a single $\overline{RAS}$ cycle, allows for the data in the color register to be written into all the memory locations of a selected row. Each bit of the color register corresponds to one of the DRAM I/O blocks and the flash write operation can be selectively controlled on an I/O basis in the same manner as the write-per-bit operation.

A flash write cycle is performed by holding $\overline{CAS}$ "high", $\overline{WB}/\overline{WE}$ "low" and DSF1 "high" at the falling edge of $\overline{RAS}$. The mask data must also be provided on the Wi/IOi inputs in order to enable the flash write operation for selected I/O blocks. After a LMR operation, however, the old mask in the mask register is used for the I/O block masking.

Flash write is most effective for fast plane clear operations in frame buffer applications. Selected planes can be cleared by performing 512 flash write cycle and by specifying a different row address location during each flash write cycle. Assuming a cycle time of 130ns, a plane clear operation can be completed in less than 66.6 μ sec.

Figure 2. Flash Write Operation



*	Mask Mode
Mask Data	New Mask Mode
Don't Care (H or L)	Old Mask Mode

5. PIPELINED FAST PAGE MODE : RWM (P), BWM (P), RW (P), BW (P)

Pipelined fast page mode allows much faster access to the memory than the conventional page mode. Read, write and block write cycles are available at the pipelined fast page mode timings.

A pipelined fast page mode is performed by holding DSF2 "high" at the falling edge of $\overline{RAS}$. A pipelined fast page read, write and block write operations can run at 30ns cycle time for 70ns version. Also, those mode can be selected every $\overline{CAS}$ cycle by the status of $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and DSF1 pin. There are, however, penalties on the performance as follows

(1) Two $\overline{CAS}$ cycles are required for the read operation. The fast access, hence, takes longer than page mode. Also, one $\overline{CAS}$ cycle is needed to read out the data before the write cycle starts in the same page.

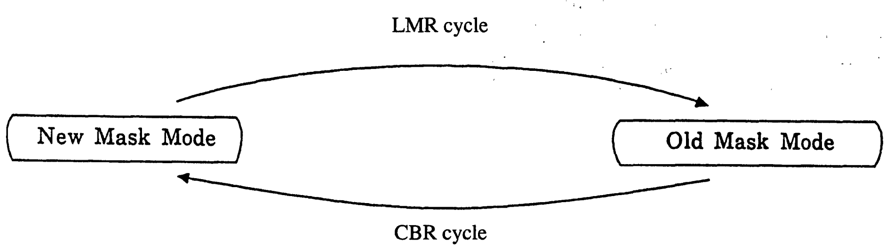
(2) One dummy cycle is needed to complete the write and block write operation. The cycle is, thus, needed between the write and the read operation and is required before the page ends.

A system designer needs to carefully estimate the system performances with the pipelined page mode and the conventional page mode in order to decide which mode should be used.

6. LOAD (OLD) MASK REGISTER : LMR

The TC528257 has an on-chip 8-bit write-mask register which provides the I/O mask data during the masked functions such as the write-per-bit (RWM), masked block write (BWM), flash write (FWM) and write transfer (MWT, MSWT) functions. Each bit of the write-mask register corresponds to one of the DRAM I/O blocks. After the mask data is specified in the write-mask register by using the load mask register (LMR) cycle, the old mask mode is invoked during the masked functions. The I/O mask data in the write-mask register maintains until another LMR operation is performed during the old mask mode. The LMR cycle is initiated by holding $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and DSF1 "high" at the falling edge of $\overline{RAS}$ and by DSF1 "low" at the falling edge of $\overline{CAS}$. The data presented on the Wi/IOi lines are subsequently latched into the write-mask register at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs later. The old mask mode is reset to the new mask mode by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR). During the LMR cycle, the memory calls of the row address which is latched at the falling edge of $\overline{RAS}$ are refreshed.

Figure 3. State Diagram of Mask Mode



7. LOAD COLOR REGISTER : LCR

The TC528257 is provided with an on-chip 8-bits register (color register) for use during the block write or flash write function. Each bit of the color register corresponds to one of the DRAM I/O blocks. The load color register cycle is initiated by holding $\overline{\text{CAS}}$, $\overline{\text{WB}}/\overline{\text{WE}}$, $\overline{\text{DT}}/\overline{\text{OE}}$ and DSF1 "high" at the falling edge of $\overline{\text{RAS}}$. The data presented on the Wi/IOi lines is subsequently latched into the color register at the falling edge of either $\overline{\text{CAS}}$ or $\overline{\text{WB}}/\overline{\text{WE}}$, whichever occurs later. During the load color register cycle, the memory cells on the row address latched at the falling edge of $\overline{\text{RAS}}$ are refreshed.

8. REFRESH

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of 512 rows in the DRAM array within the specified 8 ms refresh period. The TC528257 supports the conventional dynamic RAM refresh operations such as $\overline{\text{RAS}}$ only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh and hidden refresh.

8.1 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh and Option Reset : CBR

The CBR cycle reset the following functions, performing the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh operation at the same time.

- To reset the old mask mode to the new mask mode for the masked functions.
- To reset the stop register and remove the binary boundaries for the split SAM operation,

The systems which implement neither the old mask mode nor the binary boundary in the SAM is recommended to use the CBR cycle for refresh operation.

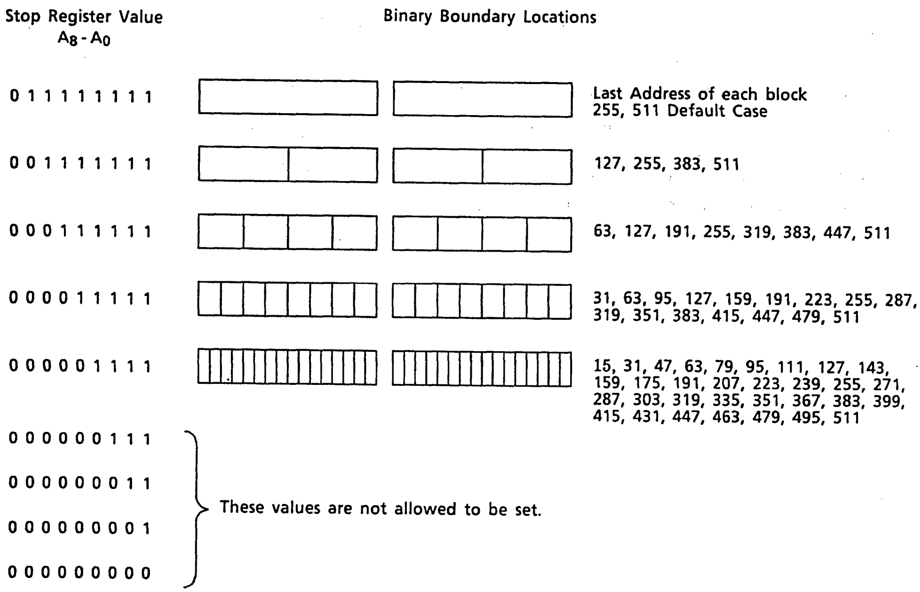
8.2 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh : CBRN

The CBRN cycle performs only the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh operation. The systems which implement either the old mask mode or the binary boundary in the SAM usually use the CBRN cycle for refresh operation except for at the required stop register set or option reset cycles. The CBRN cycle must not be used during the initialization after power-up.

8.3 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh and Stop Register Set : CBRS

The CBRS cycle sets the stop register to place binary boundaries in each half SAM, performing the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh operation at the same time. The CBRS cycle is initiated by $\overline{\text{CAS}}$ holding "low" and by $\overline{\text{WB}}$ /$\overline{\text{WE}}$ and DSF1 "high" at the falling edge of $\overline{\text{RAS}}$. At the same time the data on the address pins, A_0 - A_8 is latched and the binary boundaries in each half SAM will be available when a split transfer operation is performed.

Figure 4 . Stop Register and Binary Boundary Location



DATA TRANSFER OPERATION

The TC528257 features two types of internal bidirectional data transfer capability between the RAM and the SAM, as shown in Figure 5. During a normal transfer, 512 words by 8-bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer), During a split transfer, 256 words by 8-bits of data can be loaded from the lower / upper half of the RAM into the lower / upper half of the SAM (Split Read Transfer) or from the lower/upper half of the SAM into the lower/upper half of the RAM (Split Write Transfer). The normal transfer and split transfer modes are controlled by the DSF1 input signal

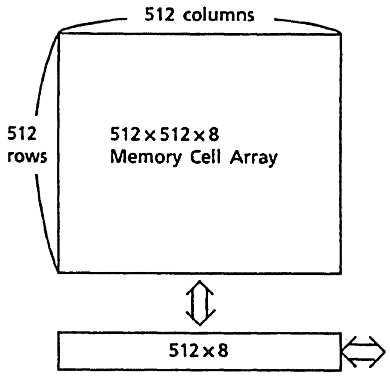
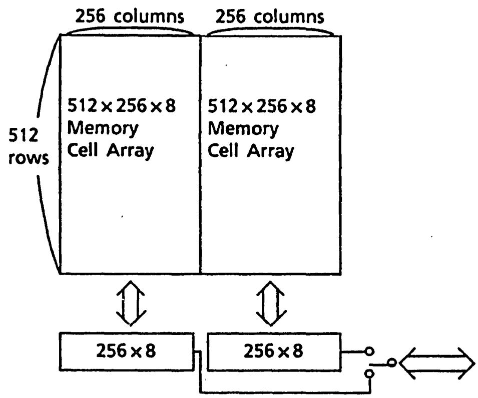


Figure 5. (a) Normal Transfer



(b) Split Transfer

Table 3. Shows the truth table of each Transfer Modes

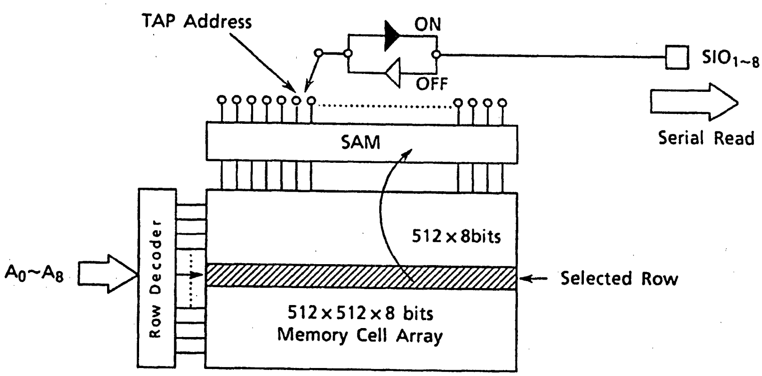
RAS				Mnemonic Code	Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
CAS	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DFS1					
H	L	H	L	RT	Read Transfer	RAM → SAM	512x8	Input → Output
H	L	L	L	WT	Write Transfer (New/Old Mask)	SAM → RAM	512x8	Output → Input
H	L	H	H	SRT	Split Read Transfer	RAM → SAM	256x8	Not changed
H	L	L	H	SWT	Split Write Transfer (New/Old Mask)	SAM → RAM	256x8	Not changed

9. READ TRANSFER CYCLE : RT

A read transfer consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ “high”, $\overline{DT}/\overline{OE}$ “low” $\overline{WB}/\overline{WE}$ “high” and DSF1 “low” at the falling edge of $\overline{RAS}$, The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. At the same time, the SAM port is set into the output mode. The start address of the serial pointer of the SAM (TAP address) is determined by the column address selected at the falling edge of $\overline{CAS}$. By doing a tight timing control between the $\overline{DT}/\overline{OE}$ rising edge and SC falling edge, a real time read transfer operation can also be performed.

Figure 6 shows the operation block diagram for read transfer operation.

Figure 6. Block Diagram for Read Transfer Operation



In a read transfer cycle (which is preceded by a write transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}/\overline{OE}$ and the falling edge of $\overline{RAS}$ and $\overline{CAS}$, as shown in READ TRANSFER CYCLE timing chart.

10. WRITE TRANSFER CYCLE : WT

A write transfer cycle consists of loading the content of the SAM register into a selected row of the RAM array. The write transfer is invoked by holding $\overline{CAS}$ “high”, $\overline{DT}/\overline{OE}$ “low”, $\overline{WB}/\overline{WE}$ “low”, and DSF1 “low” at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM (TAP address). After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.

The write transfer is selectively controlled per RAM I/O block by setting the mask data on the Wi/IOi lines at the falling edge of $\overline{RAS}$ (some as in the write-per-bit operation). Before the serial clock starts loading the data into the SAM through SIO pins, the write transfer operation with all I/O blocks disabled must be performed in order to change the SAM port from output. Please note that the conventional pseudo write transfer is not available in the TC528257. The mask function is switched between the new and old mask mode by the LMR and CBR cycle.

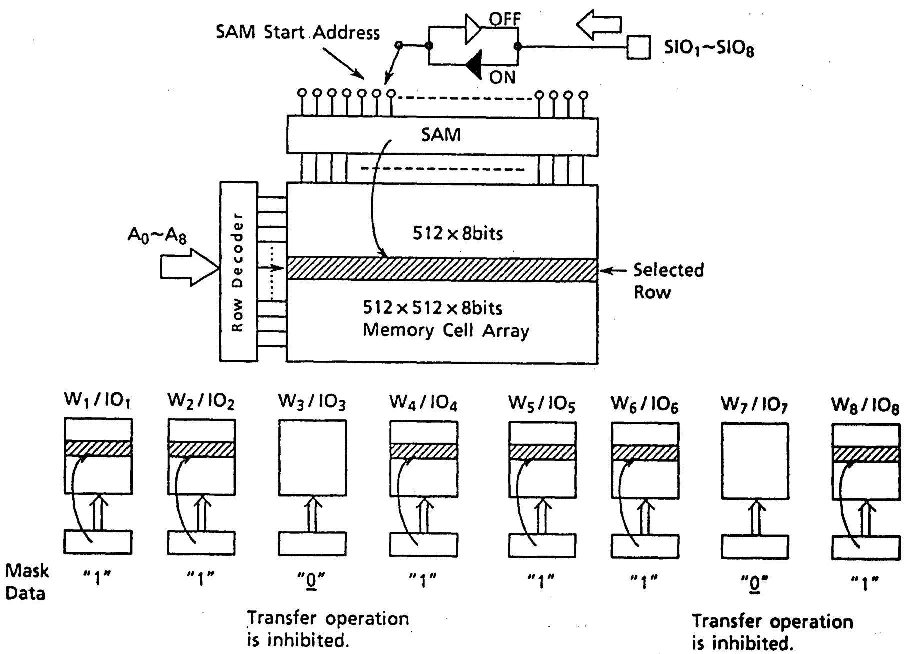


Figure 7. Block Diagram for Write Transfer Operation

When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$, at which time a new row of data can be written in the serial register.

11. SPLIT READ TRANSFER CYCLE : SRT

A split read transfer consists of loading 256 words by 8-bits of data from a selected row of the half RAM array into the corresponding half SAM in stand-by mode, Serial data can be shifted out of the other half of the SAM in active mode simultaneously, as shown in Figure 8. The most significant column address (A8C) is controlled internally to determine which half of the SAM will be reloaded from the RAM-array; During the split read transfer operation, the RAM port control signals do not have to be synchronized with the serial clock SC, thus eliminating the timing restrictions as in the case of real time read transfers. Prior to the execution of the split read transfer operation, a (normal) transfer operation must be performed to determine the absolute tap address location. QSF is an output that indicates which half of the SAM is in the active state.

QSF changes state when the last SC clock is applied to the active SAM, as shown in Figure 9.

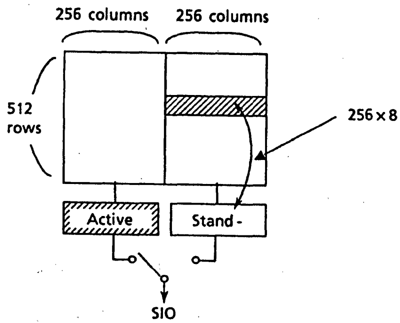


Figure 8. Split Read Transfer

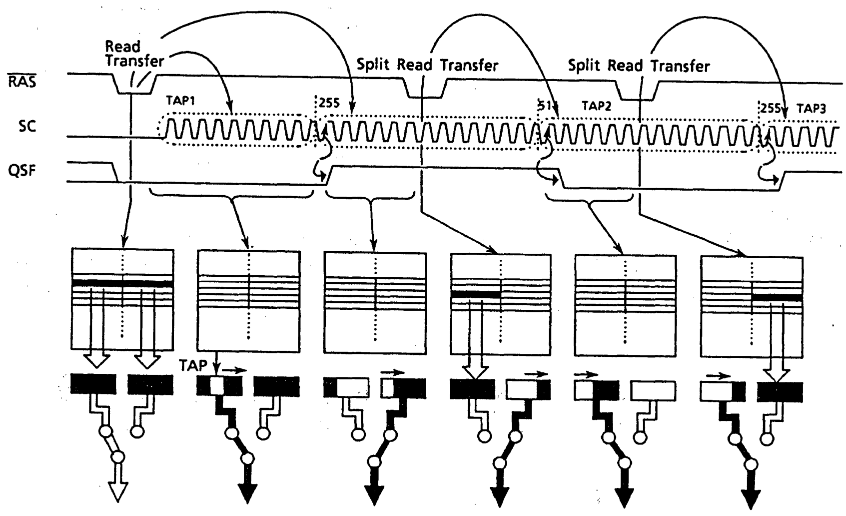


Figure 9. Example of Consecutive Read Transfer Operations

12. SPLIT WRITE TRANSFER : MSWT

A split write transfer is the similar function to the split read transfer. The difference is that the transfer direction is from the stand-by half SAM into a selected row of the corresponding half RAM array, Also, serial data can be shifted into the other half of the SAM simultaneously, as shown in Figure 10. New and old mask capability is supported in the MSWT cycle as is in the write transfer operation. Prior to the execution of the split write transfer operation, a write transfer operation, in which all I/O blocks are usually disabled, must precede to switch the SAM port from output mode to input mode and to set the initial TAP location for the serial input operation.

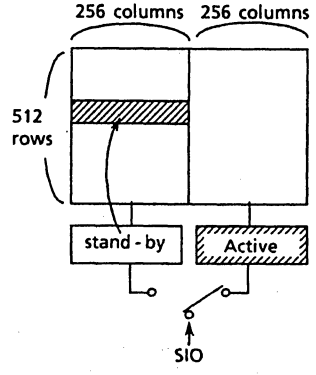


Figure 10. Block Diagram for Split Write Transfer

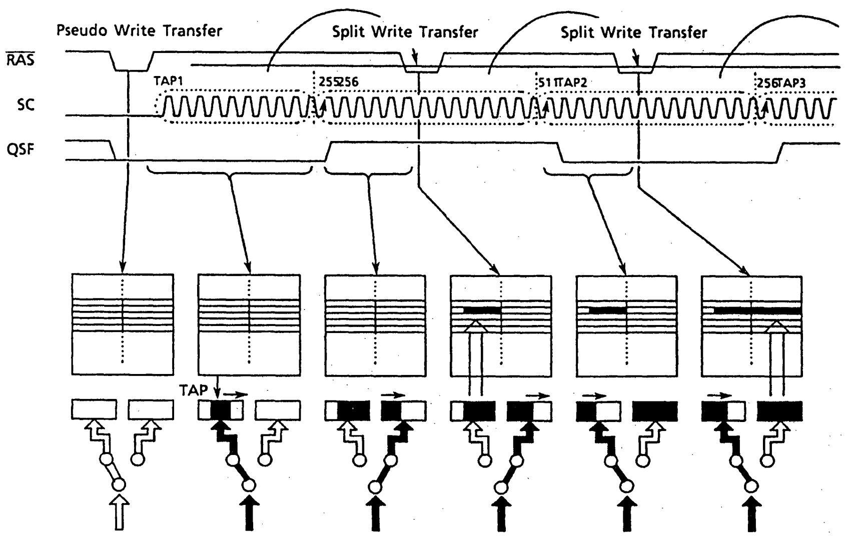
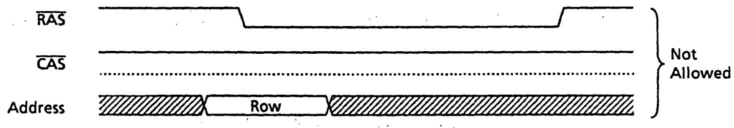


Figure 11. Example of Consecutive Write Transfer Operations

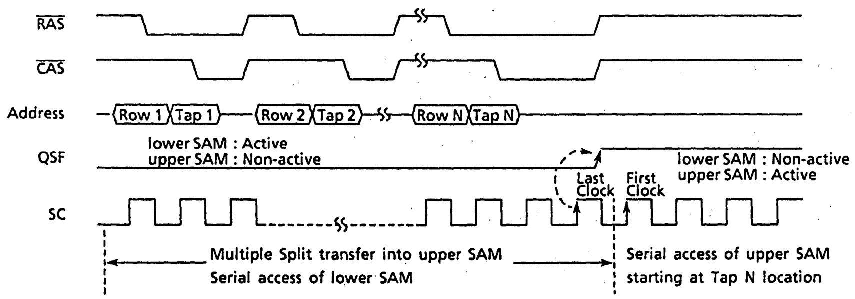
NOTES

(1) Transfer operation without $\overline{CAS}$.

The SAM tap location is undefined if $\overline{CAS}$ is maintained at a constant "high" level during a transfer cycle. A transfer cycle with $\overline{CAS}$ held "high" is, hence, not allowed.



(2) In the case of multiple split transfers performed into the same half SAM, the tap location specified during the last split transfer, before QSF toggles, will prevail, as shown below.



(3) Split transfer operation allowable period.

Figure 12 illustrates the relationship between the serial clock SC and the special function output QSF during split read / write transfers and highlights the time periods where split transfers are allowed, relative to SC and QSF. A split transfer is not allowed during to $t_{STH} + t_{STS}$. In the case that the CBRS operation is executed and the binary boundary in each half SAM is set or updated, an additional period is applied, as shown in Figure 12.

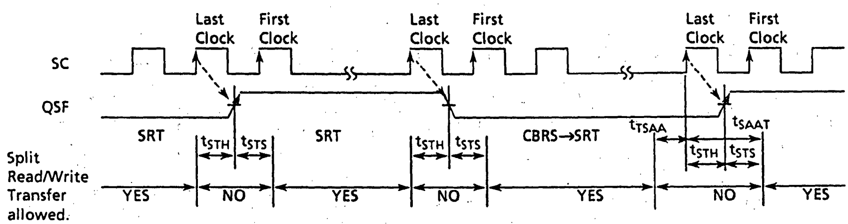
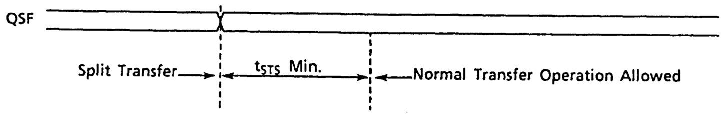


Figure 12. Split Transfer Operation Allowable Periods

The stop register and binary boundary are explained in the CBRS operation and the SAM port operation.

(4) A normal transfer (read/write) may be performed following split transfer operation provided that a t_{STS} minimun delay is satisfied after the QSF signal toggles.



(5) Binary--Boundary SET/RESET Cycle Timing

When the address counter of serial-access-memory (SAM) pointed as the last address of each boundary address, (15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255, 271, 287, 303, 319, 335, 351, 367, 383, 399, 415, 431, 447, 463, 479, 495, 511), the boundary-set or change by CBRS-cycle or the boundary-reset by CBR-cycle may cause the unexpected operation of SAM counter or QSF status.

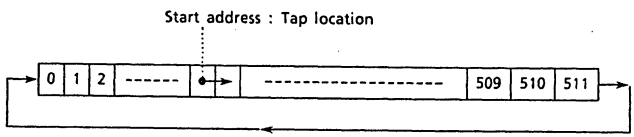
If the system design with these timing is required, please contact to our local sales office.

SAM PORT OPERATION

The TC528257 is provided with 512 words by 8-bits serial access memory (SAM) which can be operated in the single register mode or the split register mode. High speed serial read or write operations can be performed through the SAM port independent of the RAM port operation.

13. SINGLE REGISTER SERIAL READ OPERATION

Serial data can be read out of the SAM port after a read transfer has been performed. The read transfer operation changes the SAM port to the output mode. At every rising edge of the serial clock, the data is read out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit, as illustrated below. Subsequent real - time read transfer may be performed on-the-fly as many times as desired.



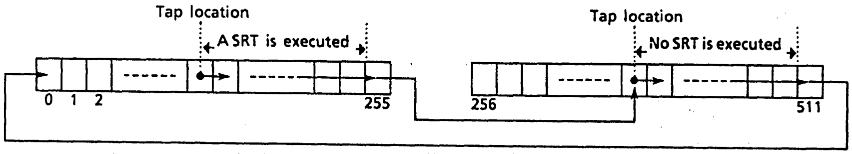
14. SINGLE REGISTER SERIAL WRITE OPERATION

During the serial write operation, the data is written into the SAM at every rising edge of the serial clock. A write transfer cycle, at which all I/Os are usually masked, must be performed to change the SAM port to the input mode. The tap location, which is the start address of the serial write, is set by the column address at the falling edge of $\overline{CAS}$. After the data is filled in the SAM, the serial clock must stop toggling and a write transfer cycle is subsequently used to load the SAM data into the RAM selected by the row address at the falling edge of $\overline{RAS}$. The tap address is set during the same cycle for the next serial write opration.

15. SPLIT REGISTER MODE

The split register mode realizes continuous serial read or write operation. The data can be shifted into or out of one half of the SAM while a split read or write transfer is being performed on the other half of the SAM. Thus, the tight timing control at a real time read operation is eliminated with the split read operation. A normal read / write transfer operation must precede any split read/write transfer operation in order to set the SAM port into output mode or input mode, as the split read or write transfer operations will not change the SAM port mode. Also, a $\overline{CAS}$ before $\overline{RAS}$ refresh and stop register set cycle (CBRS) can be performed to specify the binary boundaries in the SAM.

In the split register mode, serial data can be read from or written into one of the split registers starting from any of the 256 tap locations. The data is read or written sequentially from the tap location to the most significant bit (255 or 511) of the first split SAM and then the SAM pointer moves to the tap location selected for the second split SAM to read or write the data sequentially to the most significant bit (255 or 511) and finally wraps around to the least significant bit, as illustrated in the example below.



16. SPLIT REGISTER MODE WITH BINARY BOUNDARY

After a CBRS cycle is performed, the binary boundary, which is stated in 8.3. $\overline{CAS}$ before $\overline{RAS}$ refresh and stop register set, is set when a SRT cycle is performed. The serial data is read from or written into one half of the SAM starting the tap location to the next binary boundary, while another SRT cycle is performed. Than, the SAM pointer moves to the tap location in the other half SAM and the data is read from or written into the half SAM sequentially. If any SRT operation is not performed before the next boundary, the SAM pointer does not jump to the other half SAM, as illustrated in Figure 12.

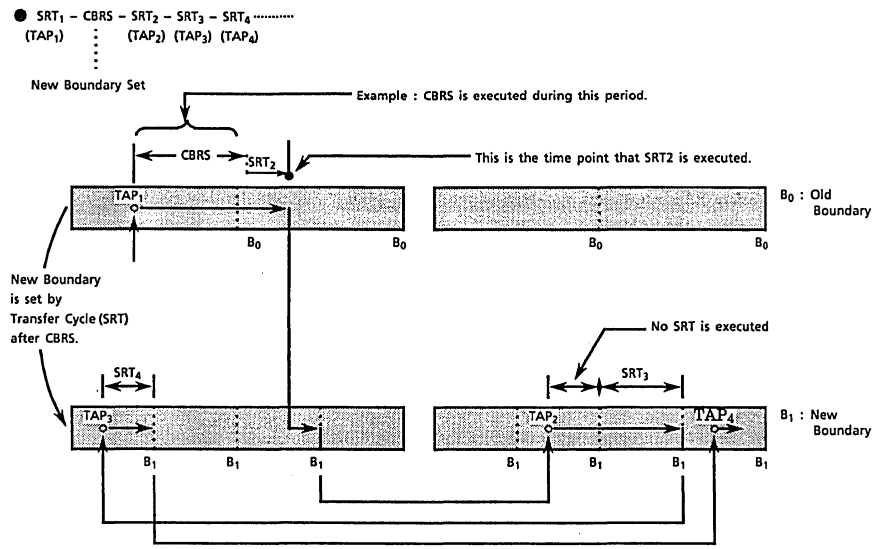


Figure 12. Operation of Split Register Mode with Binary Boundary

The binary boundary is reset by a CBR cycle and the SAM operation mode returns to the normal split register mode, as shown in Figure 13.

Fig. 14 shows the relation between CBR and SC on binary-boundary-reset. When Nth SC clock accesses old binary address is reset and (N + 1)th SC clock accesses old boundary address (old stop address) + 1 on the same split SAM, not jump to TAP address.

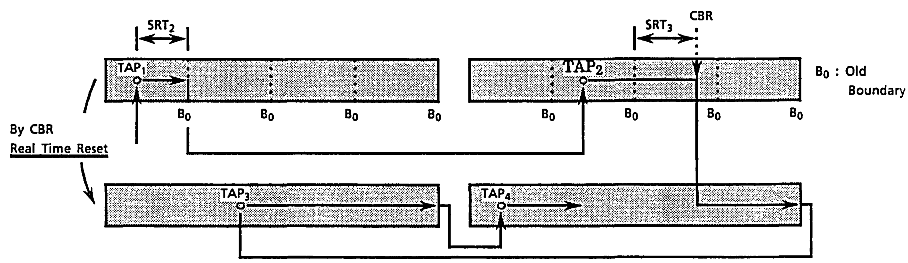


Figure 13. Binary Boundary Reset

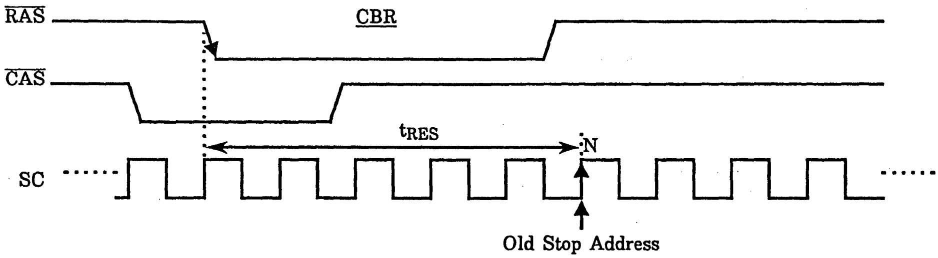


Figure 14. CBR and SC relation of binary-boundary-reset

In an actual system which uses the binary boundary a CBRS cycle is executed to determine a type of the boundary location. Then, a normal RT transfers a row of data into the SAM and set the initial tap location at the same time. An SRT cycle follows it before the SAM pointer reaches to the boundary location. The SRT cycle makes the binary boundary jump effective, as illustrated in Figure 15.

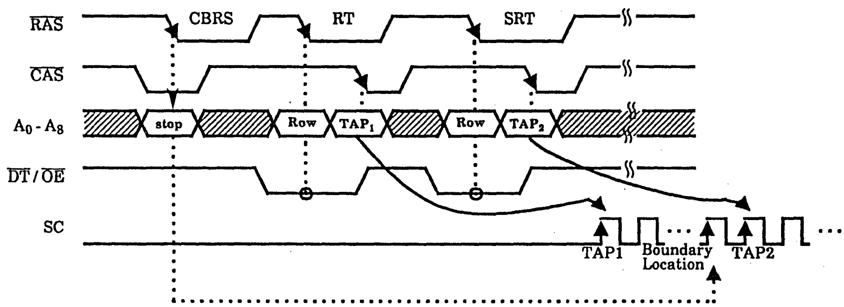


Figure 15. Binary Boundary Jump Set Sequence

There are additional timing specifications, t_{TSAA} and t_{SAAT} to determine the period that does not allow a split transfer, as illustrated in Figure 16.

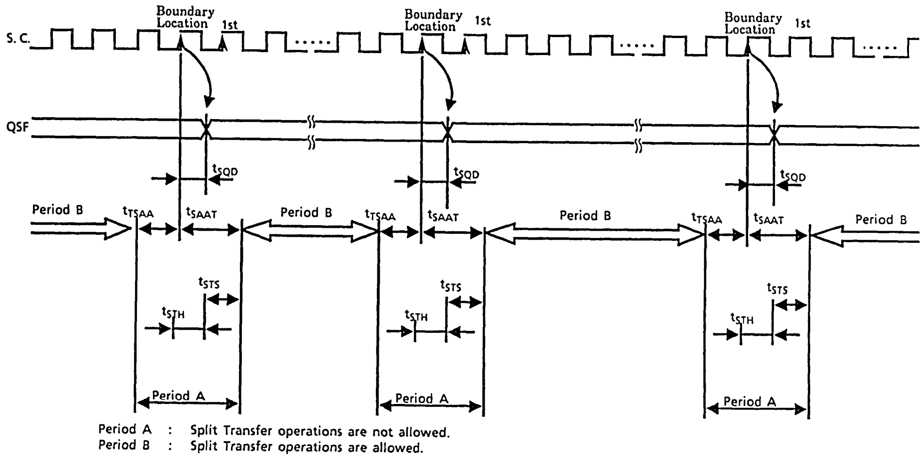


Figure 16. Timing Specification to allow SRT operation

POWER-UP

Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them "high" before or at the same time as the V_{CC} supply is turned on. After power-up, a pause of 200 µseconds minimum is required with $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ held "high". After the pause, a minimum of 8 CBR dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT}/\overline{OE}$ signal must be held "high".

INITIAL STATE AFTER POWER-UP

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and $\overline{WB}/\overline{WE}$ held "high", the internal state of the TC528257 is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 µseconds pause followed by a minimum of 8 CBR cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
QSF	High-Impedance
Color Register	all "0"
Write Mask Register	Write Enable
TAP pointer	Invalid
Sto Register	Default Case

SILICON GATE CMOS
262,144WORDS x 8BITS MULTIPORT DRAM

target spec

DESCRIPTION

The TC528267 is a 2M bit CMOS multiport memory equipped with a 262,144-words by 8-bits dynamic random access memory (RAM) port and a 512-words by 8-bits static serial access memory (SAM) port. The TC528267 supports three types of operations; Random access to and from the RAM port, high speed serial access to and from the SAM port and bidirectional transfer of data between any selected row in the RAM and the SAM. To realize a high performance graphic frame buffer system the TC528267 features various special operations such as the write - per - bit, the pipelined page mode, the block write and flash write function on the RAM port and the read and masked write transfer operations between the RAM and the SAM port. In addition, the TC528267 is fabricated using Toshiba's CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

FEATURES

- Single power supply of 5 V± 10% with a built-in V_{BB} generator
- All inputs and outputs : TTL Compatible
- Organization
  RAM Port : 262,144wordsX8bits
  SAM Port : 512wordsX8bits
- RAM Port
  Extended Fast Page Mode, Read - Modify - Write, Pipelined Fast Page Mode, $\overline{CAS}$ before $\overline{RAS}$ Auto Refresh, Hidden Refresh, $\overline{RAS}$ only Refresh, Write per Bit (New/Old Mask Mode), Masked Flash Write (New/Old Mask Mode), Block Write, Masked Block Write (New/Old Mask Mode), Load Mask Register/Color Register Cycle, 512 refresh cycles / 8ms
- SAM Port
  Serial Read / Write Capability
  Addressable TAP Capability
  Stop Address (Binary Boundary) Capability
  Fully Static Register, SIngle Register/Split Register Mode Capability
- RAM - SAM Bidirectional Transfer
  Read / Real Time Read Transfer
  Masked Write Transfer
  Split Read / Masked Split Write Transfer
- Package
  TC528267J : SOJ40-P-400
  TC528267FT : TSOP44-P-400B
  TC528267TR : TSOP44-P-400C

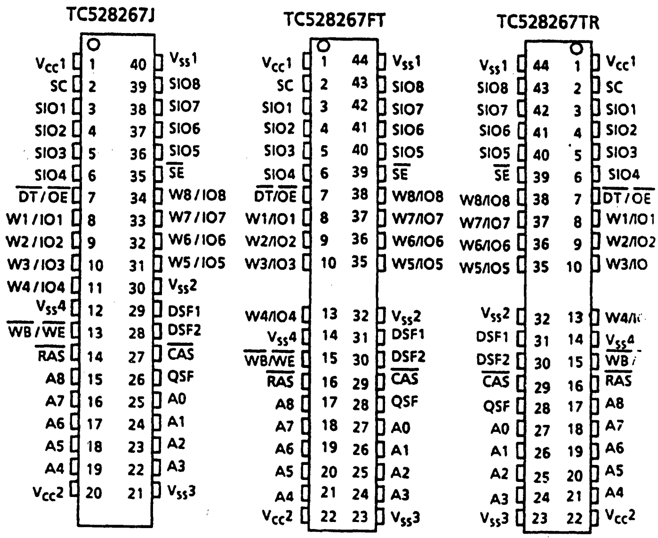
KEY PARAMETERS

ITEM		—70	—80
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	70ns	80ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	20ns	20ns
t_{AA}	Column Address Access Time (Max.)	35ns	40ns
t_{RC}	Cycle Time (Min.)	130ns	150ns
t_{PC}	Page Mode Cycle Time (Min.)	35ns	40ns
t_{SCA}	Serial Access Time (Max.)	20ns	25ns
t_{SCC}	Serial Cycle time (Min.)	25ns	30ns
t_{RACP}	t_{RAC} in Pipelined Fast Page	90ns	95ns
t_{CAC1}	t_{CAC} in Pipelined Fast Page	20ns	20ns
t_{PCP}	Pipelined Fast Page Mode Cycle Time	30ns	30ns
I_{CC1}	RAM Operating Current (SAM : Standby)	100mA	85mA
I_{CC2A}	SAM Operating Current (RAM : Standby)	60mA	50mA
I_{CC2}	Standby Current	10mA	10mA

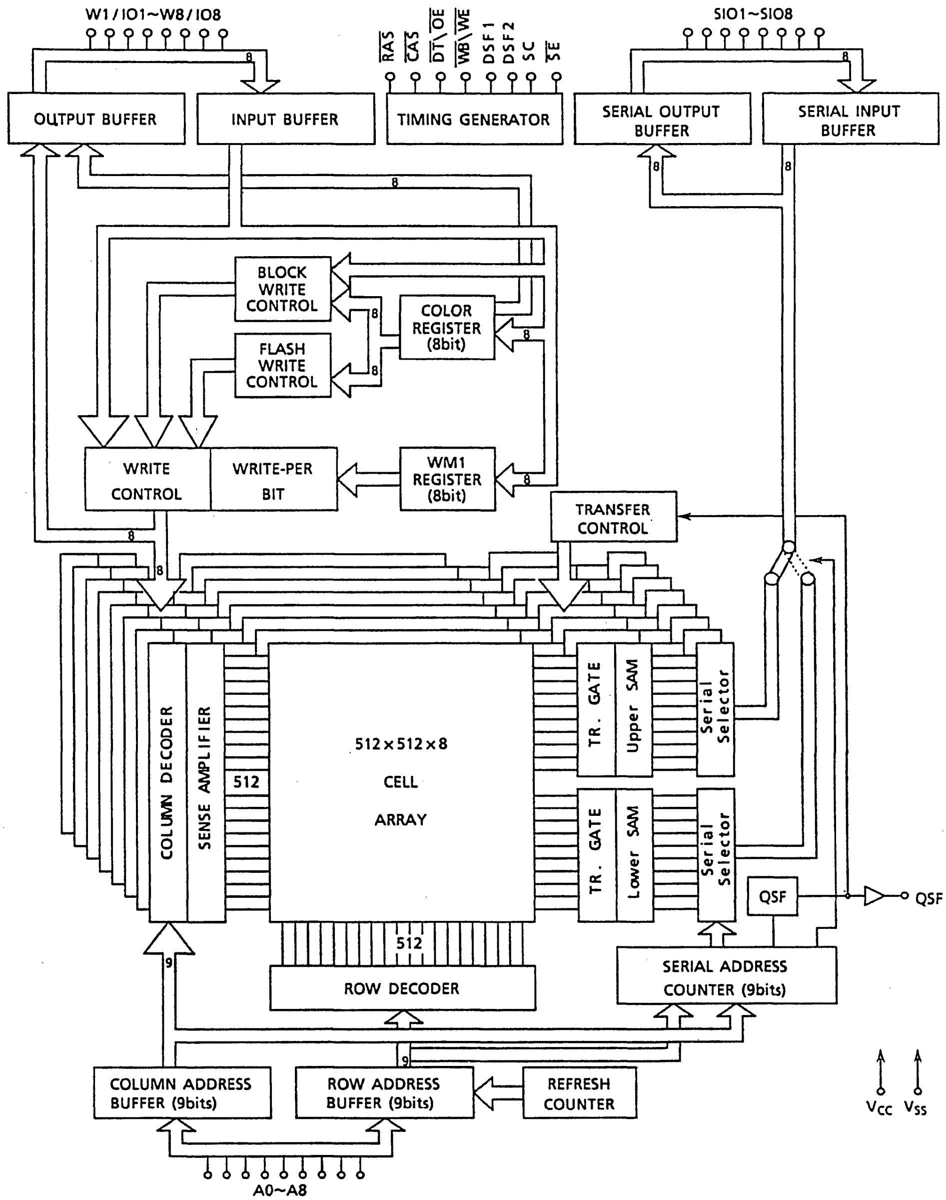
PIN NAME

A0~A8	Address inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}/\overline{WE}$	Write per Bit/Write Enable
DSF1 DSF2	Special Function Control
W1/IO1~W8/IO8	Write Mask/Data IN OUT
SC	Serial Clock
SE	Serial Enable
SIO1~SIO8	Serial Input/Output
QSF	Special Flag Output
V_{CC}/V_{SS}	Power (5V)/Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}, V_{OUT}	Input Output Voltage	— 1.0~7.0	V	1
V_{CC}	Power Supply Voltage	— I .0~7.0	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	— 55~150	°C	1
T_{SOLDER}	Soldering Temperature • Time	260•10	°C•sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	6.5	V	2
V_{IL}	Input Low Voltage	- 1.0	—	0.8	V	2

+: -1V 20ns Pulse width

CAPACITANCE (V_{CC} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance	—	7	pF
C_{IO}	Input/Output Capacitance	—	9	
C_O	Output Capacitance (QSF)	—	9	

Note: This parameter is periodically sampled and is not 100% tested.

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

ITEM (RAM PORT)	SAM PORT	SYMBOL	-70		-80		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
OPERATING CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC1}	—	100	—	90	mA	3, 4, 5
	Active	I_{CC1A}	—	160		140		3, 4, 5
STANDBY CURRENT $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	Standby	I_{CC2}	—	10	—	10		
	Active	I_{CC2A}	—	65	—	55		3, 4, 5
$\overline{RAS}$ ONLY REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	Standby	I_{CC3}	—	100	—	90		3, 4
	Active	I_{CC3A}	—	160	—	140		3, 4, 5
PAGE MODE CURRENT ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{PC} = t_{PC} min.)	Standby	I_{CC4}	—	90	—	80		3, 4, 5
	Active	I_{CC4A}	—	150	—	130		3, 4, 5
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$, t_{RC} = t_{RC} min.)	Standby	I_{CC5}	—	100	—	90		3, 4, 5
	Active	I_{CC5A}	—	160	—	140		3, 4, 5
DATA TRANSFER CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC6}	—	135	—	125		3, 4, 5
	Active	I_{CC6A}	—	195	—	175		3, 4, 5
FLASH WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC7}	—	100	—	90		3, 4, 5
	Active	I_{CC7A}	—	160	—	140		3, 4, 5
BLOCK WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC8}	—	110	—	100		3, 4, 5
	Active	I_{CC8A}	—	170	—	150		3, 4, 5

ITEM	SYMBOL	MIN.	MAX	UNIT	NOTE
INPUT LEAKAGE CURRENT 0V ≤ V_{IN} ≤ 6.5V, All other pins not under test=0V	$I_{I(L)}$	—10	10	μA	
OUTPUT LEAKAGE CURRENT 0V ≤ V_{OUT} ≤ 5.5V, OutputDisable	$I_{O(L)}$	—10	10	μA	
OUTPUT "H" LEVEL VOLTAGE I_{OUT} = - 1mA	V_{OH}	2.4	—	V	
OUTPUT "L" LEVEL VOLTAGE I_{OUT} = 2.1mA	V_{OL}	—	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes: 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130		150		ns	
t_{RMW}	Read-Modify-Write Cycle Time	180		200			
t_{PC}	Fast Page Mode Cycle Time	35		40			
t_{PRMW}	Fast Page Mode Read-Modify-Write CycleTime	90		90			
t_{RAC}	Access Time from $\overline{RAS}$		70		80		9, 15
t_{AA}	Access Time from Column Address		35		40		9, 15
t_{CAC}	Access Time from $\overline{CAS}$		20		20		9, 16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		35		40		9, 16
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0		0			
t_{OELZ}	$\overline{OE}$ to Output in Low-Z	0		0			
t_{OFF}	Output Buffer Turn-Off Delay	0	15	0	15		11, 17
t_T	Transition Time (Rise and Fall)	3	50	3	50		8
t_{RP}	$\overline{RAS}$ Precharge Time	50		60			
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10000	80	10000		
t_{FASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode Only)	70	100000	80	100000		
t_{RSH}	$\overline{RAS}$ Hold Time	20		20			
t_{CSH}	$\overline{CAS}$ Hold Time	70		80			
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10000	20	10000		
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60		15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40		15
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35		40			
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5			
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10			
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10			
t_{ASR}	Row Address Set-Up Time	0		0			
t_{RAH}	Row Address Hold Time	10		10			
t_{ASC}	Column Address Set-Up Time	0		0			
t_{CAH}	Column Address Hold Time	12		15			
t_{RCS}	Read Command Set-Up Time	0		0			
t_{RCH}	Read Command Hold Time	0		0			12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0			12
t_{WCH}	Write Command Hold Time	10		15			
t_{WP}	Write Command Pulse Width	10		10			
t_{WPZ}	Write Command Pulse Width	10		15			11
t_{WEZ}	Write Command Output Buffer Turn-Off Delay		10		15		11
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20			
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		20			
t_{DS}	Data Set-Up Time	0		0			13
t_{DH}	Data Hold Time	12		15			13
t_{WCS}	Write Command Set-Up Time	0		0			14
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	95		105			14
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	60		65			14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45		45			14
t_{COH}	$\overline{CAS}$ Hold TIme referenced to $\overline{OE}$	5		5			
t_{RES}	$\overline{RAS}$ to SC boundary - reset Time	30		30			

SYMBOL	PARAMETER	-70		-80		UNIT	NOTE
		MIN.	MAX	MIN.	MAX.		
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0			
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0			
t_{OEA}	Access Time from $\overline{OE}$		20		20		9
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$		15		15		11
t_{OED}	$\overline{OE}$ to Data Delay Time	15		15			
t_{OEH}	$\overline{OE}$ Command Hold Time	15		15		ns	
t_{ODS}	Output Disable Set up time	0		0			
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15		15			
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	5		5			
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		15			
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0			
t_{REF}	Refresh Period		8		8	ms	
t_{WSR}	$\overline{WB}$ Set-Up Time	0		0			
t_{RWH}	$\overline{WB}$ Hold Time	10		15			
t_{FSR}	DSF Set-Up Time referenced to $\overline{RAS}$	0		0			
t_{RFH}	DSF Hold Time referenced to $\overline{RAS}$(1)	10		15			
t_{FSC}	DSF Set-Up Time referenced to $\overline{CAS}$	0		0			
t_{CFH}	DSF Hold Time referenced to $\overline{CAS}$	12		15			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0		0			
t_{MH}	Write-Per-Bit Mask Data Hold Time	10		15			
t_{THS}	$\overline{DT}$ High Set-Up Time	0		0			
t_{THH}	$\overline{DT}$ High Hold Time	10		15			
t_{TLS}	$\overline{DT}$ Low Set-Up Time	0		0			
t_{TLH}	$\overline{DT}$ Low Hold Time	10	10000	15	10000		
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	60	10000	65	10000	ns	
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	25		25			
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	20		20			
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	50		60			
t_{TP}	$\overline{DT}$ Precharge Time	15		15			
t_{RSD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	70		80			
t_{ASD}	Column Address to First SC Delay Time (Read Transfer)	35		40			
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	20		20			
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		5			
t_{TSD}	$\overline{DT}$ to FIrst SC Delay Time (Read Transfer)	10		15			
t_{SRS}	Last SC to $\overline{RAS}$ Set-Up Time (Serial Input)	25		30			
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	20		25			
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	45		50			

SYMBOL	PARAMETER	-70		-80		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{SCC}	SC Cycle Time	25		30		ns	
t_{SC}	SC Pulse Width (SC High Time)	10		10			
t_{SCP}	SC Precharge Time (SC Low Time)	5		10			
t_{SCA}	Access Time from SC		20		25		10
t_{SOH}	Serial Output Hold Time from SC	5		5			
t_{SDS}	Serial Input Set-Up Time	0		0			
t_{SDH}	Serial Input Hold Time	10		15			
t_{SEA}	Access Time from $\overline{SE}$		20		25		10
t_{SE}	$\overline{SE}$ Pulse Width	20		25			
t_{SEP}	$\overline{SE}$ Precharge Time	20		25			
t_{SEZ}	Serial Output Buffer Turn-off Delay from $\overline{SE}$		15		20		11
t_{SZE}	Serial to $\overline{SE}$ Delay Time	0		0			
t_{SZS}	Serial Input to First SC Delay Time	0		0			
t_{SWS}	Serial Write Enable Set-Up Time	0		0			
t_{SWH}	Serial Write Enable Hold Time	10		15			
t_{SWIS}	Serial Write Disable Set-Up Time	0		0			
t_{SWIH}	Serial Write Disable Hold Time	10		10			
t_{STS}	Split Transfer Set-Up Time	25		30			
t_{STH}	Split Transfer Hold Time	25		30			
t_{SAAT}	Split Transfer SC Set-Up Time from RAS	45		55			
t_{SAA}	Split Transfer SC Hold Time from RAS	0		0			
t_{SQD}	SC-QSF Delay Time		20		25		
t_{TQD}	$\overline{DT}$-QSF Delay Time		20		25		
t_{CQD}	$\overline{CAS}$-QSF Delay Time		20		25		
t_{RQD}	$\overline{RAS}$-QSF Delay Time		70		80		
t_{RCDP}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time (Pipeline mode)	20	40	20	45		
t_{CSHP}	$\overline{CAS}$ Hold Time (Pipeline mode)	50		55			
t_{RACP}	Access TIme from $\overline{RAS}$ (Pipeline mode)		90		95		
t_{CAC1}	Access Time from $\overline{CAS}$ (1) (Pipeline mode)		20		20		10
t_{CAC2}	Access Time From $\overline{CAS}$ (2) (Pipeline mode)		50		50		10
t_{CASP}	$\overline{CAS}$ Pulse Width (Pipeline mode)	10		10			
t_{CPP}	$\overline{CAS}$ Precharge Time Pipeline mode)	10		10			
t_{PCP}	Fast Page Mode Cycle Time (Pipeline mode)	30		30			
t_{RSH1}	$\overline{RAS}$ Hold Time (1) (Pipeline mode)	20		20			
t_{RSH2}	$\overline{RAS}$ Hold Time (2) (Pipeline mode)	50		50			
t_{CWLP}	Write Command to $\overline{CAS}$ lead Time (Pipeline mode)	10		10			
t_{CWP}	$\overline{WE}$ to $\overline{CAS}$ Delay Time (Pipeline mode)	30		30			
t_{OFFP}	Outoff Buffer Turn-off Delay from $\overline{RAS}$ (Pipeline mode)	0	15	0	15		11, 17

RAM Output Reference Level	2.0V/0.8V
SAM Output Reference Level	2.0V/0.8V
RAM Output Load	1 TTL and 50PF
SAM Output Load	1 TTL and 30PF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltage are referenced to V_{SS}.

3. These parameters depend on cycle rate.

4. These parameters depend on output loading. Specified values are obtained with the output open.

5. Address can be changed once or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200 µs is required after power-up followed by any 8 $\overline{CAS}$ before $\overline{RAS}$ initialisation cycles before proper device operation is achieved.

7. AC measurements assume t_T = 5ns.

8. $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. RAM port outputs are measured with a load equivalent to 1 TTL load and 50pF.
   D_{OUT} reference levels : V_{OH} / V_{OL} = 2.0V / 0.8V.

10. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
    D_{OUT} reference levels : V_{OH} / V_{OL} = 2.0V / 0.8V.

11. $t_{OFF\ (max.)}$, $t_{OEZ\ (max.)}$, $t_{OFFP\ (max.)}$,$t_{WPZ\ (max.)}$, $t_{WEZ\ (max.)}$, and $t_{SEZ\ (max.)}$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.

12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.

13. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}$ / $\overline{WE}$ leading edge in $\overline{OE}$-controlled-write cycle and read-modify-write cycles.

14. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS\ (min.)}$, the cycle is an early write cycles and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geq t_{RWD\ (min.)}$, $t_{CWD} \geq t_{CWD\ (min.)}$ and $t_{AWD} \geq t_{AWD\ (min.)}$ the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

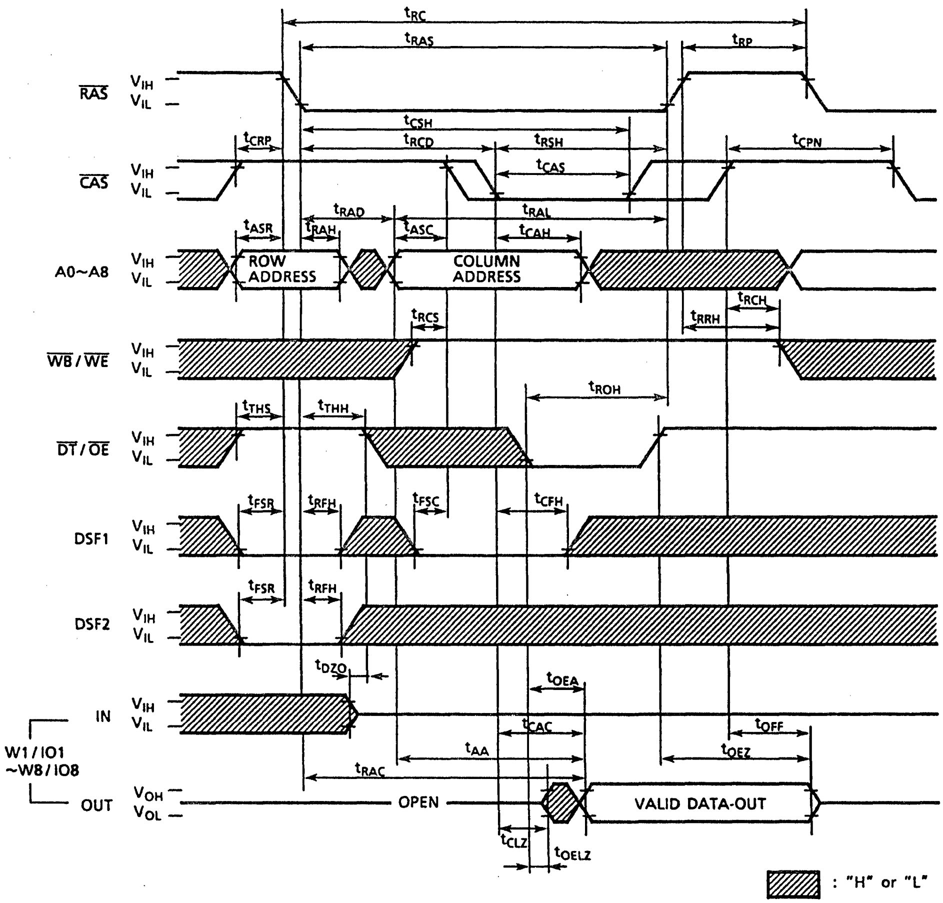
15. Operation within the $t_{RCD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can be met.
    $t_{RCD\ (max.)}$ is specified as a reference point only : If t_{RCD} is greater than the specified
    $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

16. Operation within the $t_{RAD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

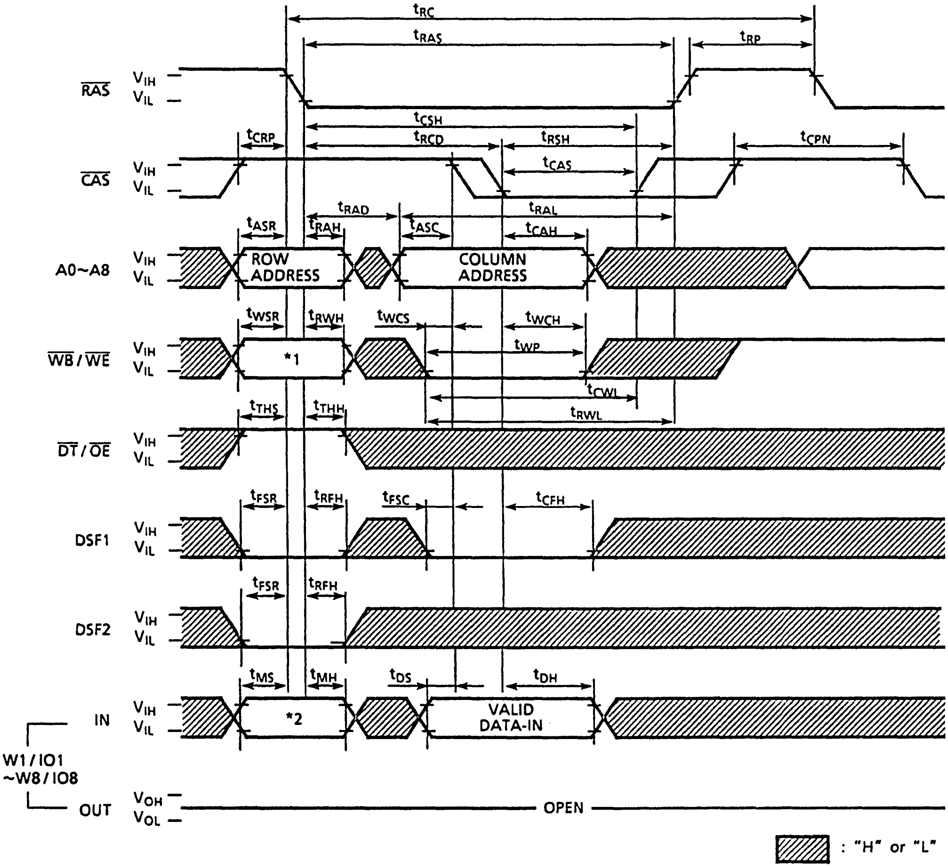
17. t_{OFF}, t_{OFFP} timing is specified from either $\overline{RAS}$ or $\overline{CAS}$ rising edge, whichever occurs last.

TIMING WAVEFORM

READ CYCLE



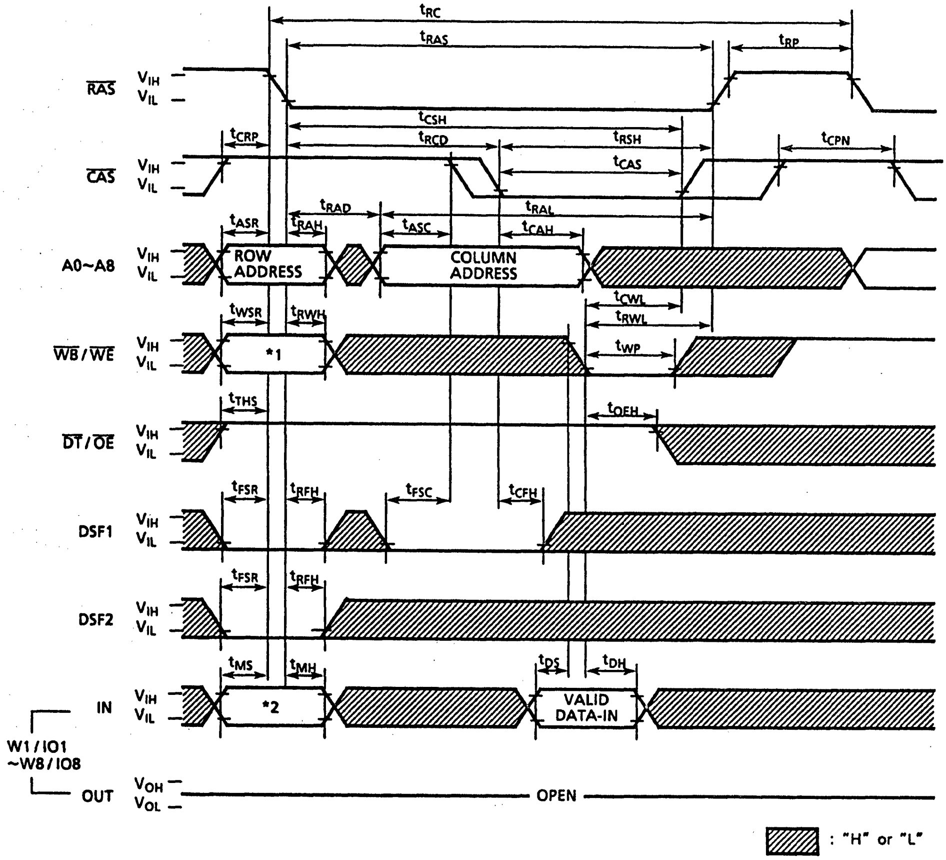
WRITE CYCLE (EARLY WRITE)



Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data   0: Write Disable
            1: Write Enable
Don't care : '1' or '0'

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

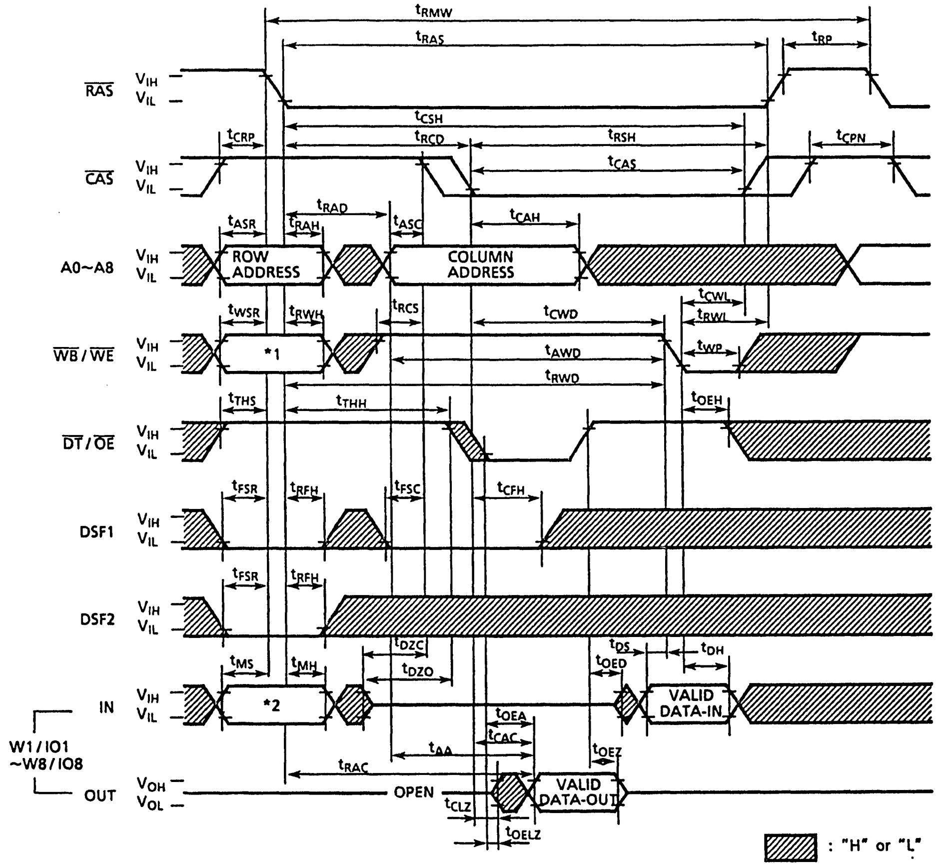


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data — 0: Write Disable
1: Write Enable

Don't care — : '1' or '0'

READ-MODIFY-WRITE CYCLE

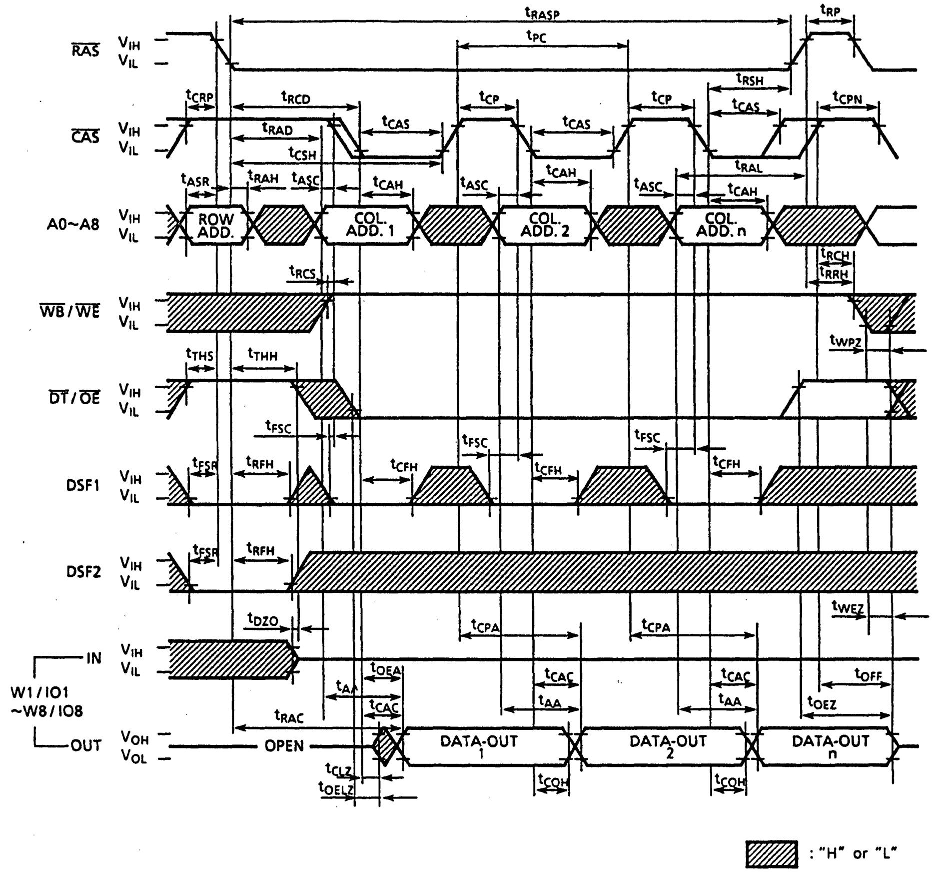


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

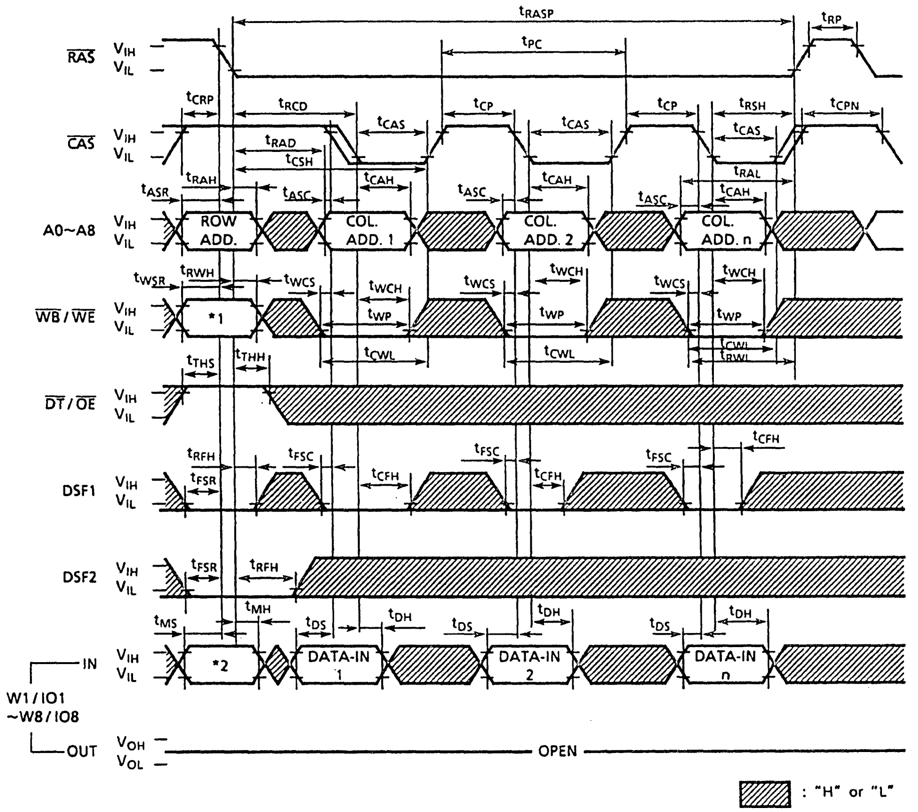
WM1 data — 0: Write Disable
1: Write Enable

Don't care — : '1' or '0'

EXTENDED FAST PAGE MODE READ CYCLE



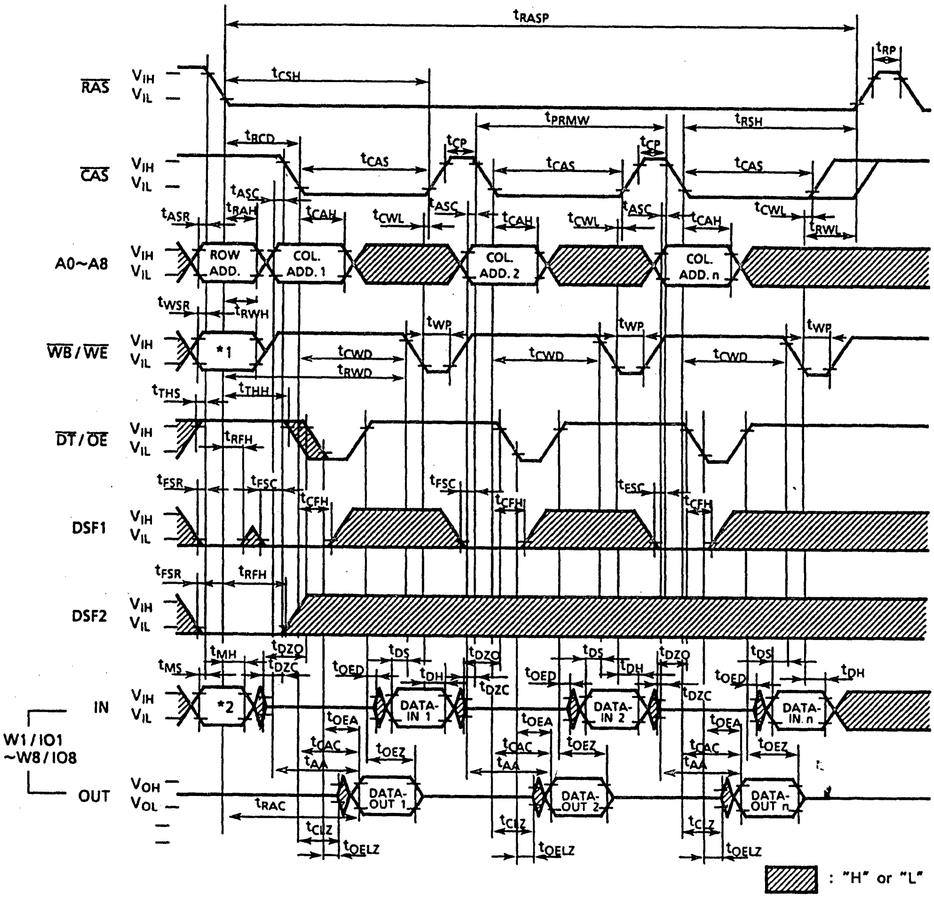
EXTENDED FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable
Don't care : '1' or '0'

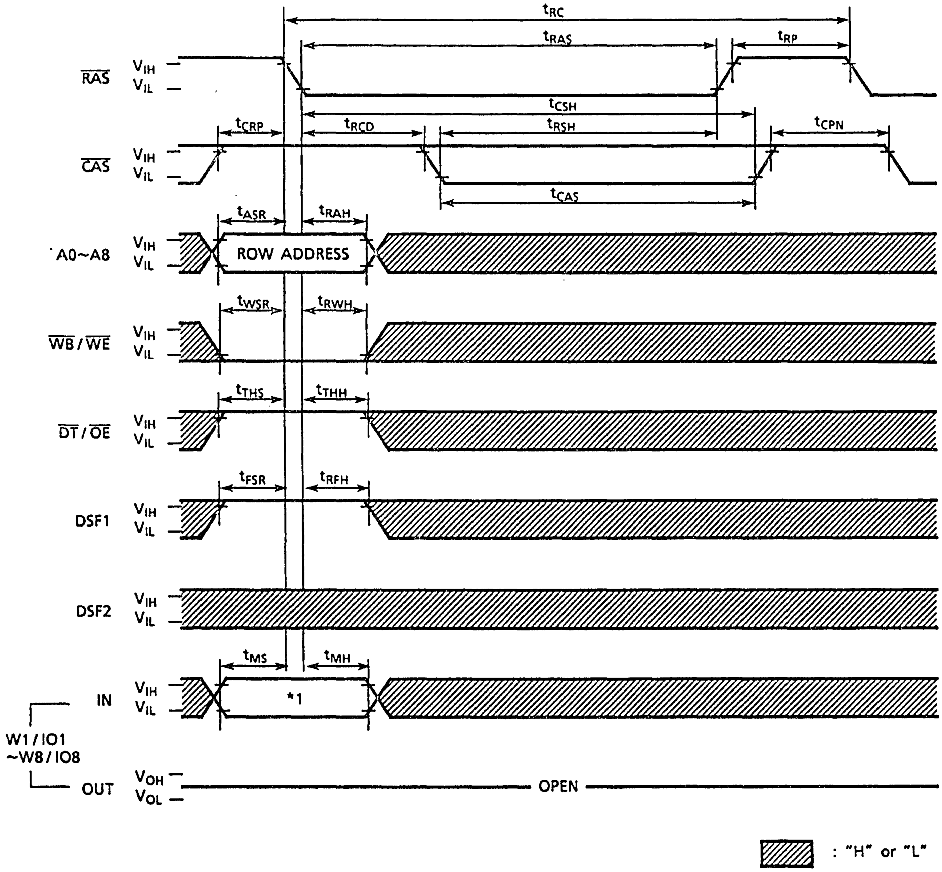
EXTENDED FAST PAGE MODE READ-MODIFY-WRITE CYCLE



Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable
Don't care : '1' or '0'

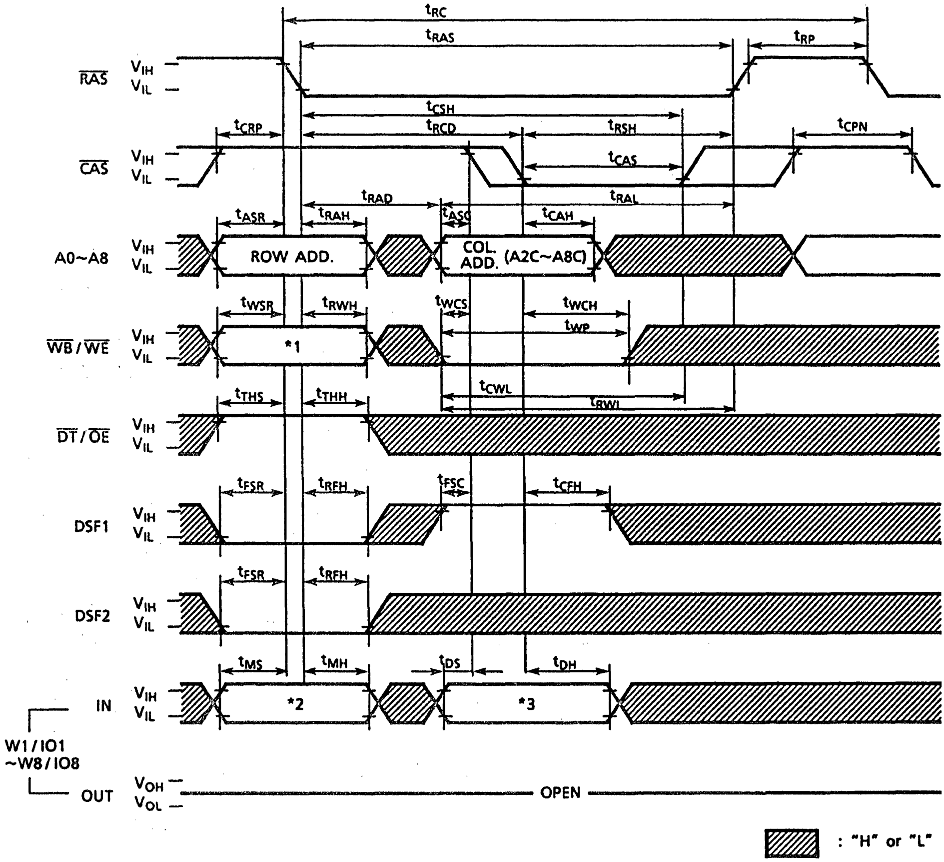
FLASH WRITE CYCLE



Mask Mode	*1
New Mask Mode	WM1 data
Old Mask Mode	Don't care

WM1 data 0: Flash Write Disable
1: Flash Write Enable
Don't care : '0' or '1'

BLOCK WRITE CYCLE (EARLY WRITE)



Mask Mode	*1	*2
No Mask Mode	1	Don't care
New Mask Mode	0	WM1 data
Old Mask Mode	0	Don't care

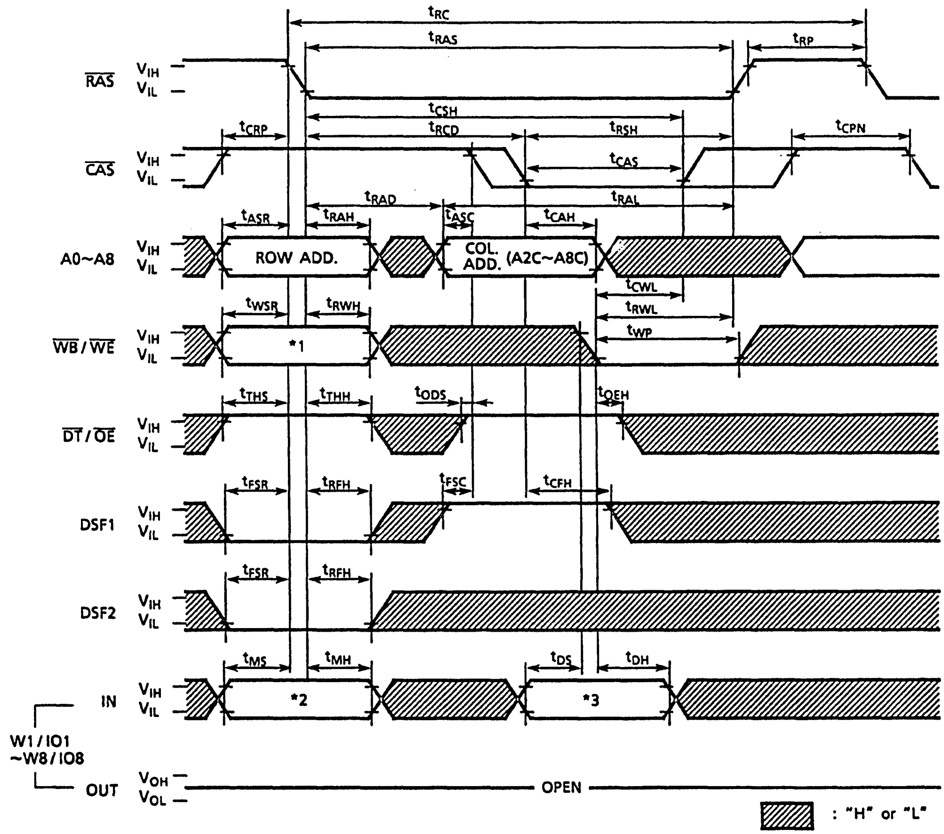
WM1 data 0: Write Disable
1: Write Enable
Don't care : '0' or '1'

***3 COLUMN SELECT**

W1/IO1 - Column 0 (A_{1C}=0, A_{0C}=0
W2/IO2 - Column 1 (A_{1C}=0, A_{0C}=1
W3/IO3 - Column 2 (A_{1C}=1, A_{0C}=0
W4/IO4 - Column 3 (A_{1C}=1, A_{0C}=1

} Wn/IOn
=0 : Disable
=1 : Enable

BLOCK WRITE CYCLE (DELAYED WRITE)



Mask Mode	*1	*2
No Mask Mode	1	Don't care
New Mask Mode	0	WM1 data
Old Mask Mode	0	Don't care

WM1 data 0: Write Disable
1: Write Enable

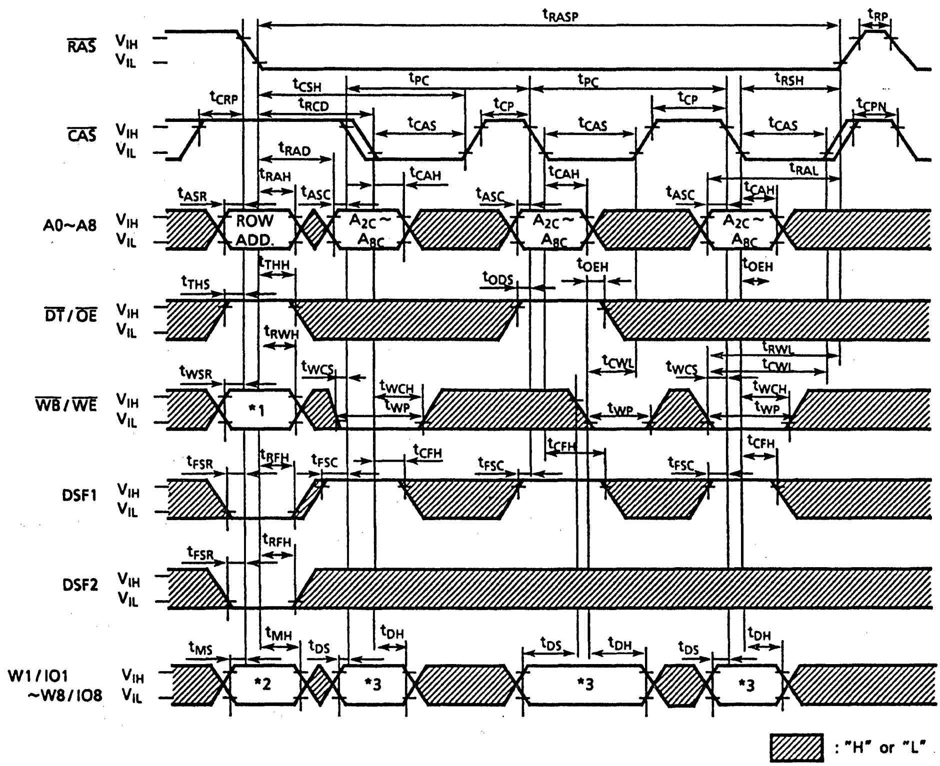
Don't care : '0' or '1'

*3 COLUMN SELECT

W1/IO1 - Column 0 (A_{1C}=0, A_{0C}=0
W2/IO2 - Column 1 (A_{1C}=0, A_{0C}=1
W3/IO3 - Column 2 (A_{1C}=1, A_{0C}=0
W4/IO4 - Column 3 (A_{1C}=1, A_{0C}=1

Wn/IOn
=0 : Disable
=1 : Enable

FAST PAGE MODE BLOCK WRITE CYCLE



Mask Mode	*1	*2
No Mask Mode	1	Don't care
New Mask Mode	0	WM1 data
Old Mask Mode	0	Don't care

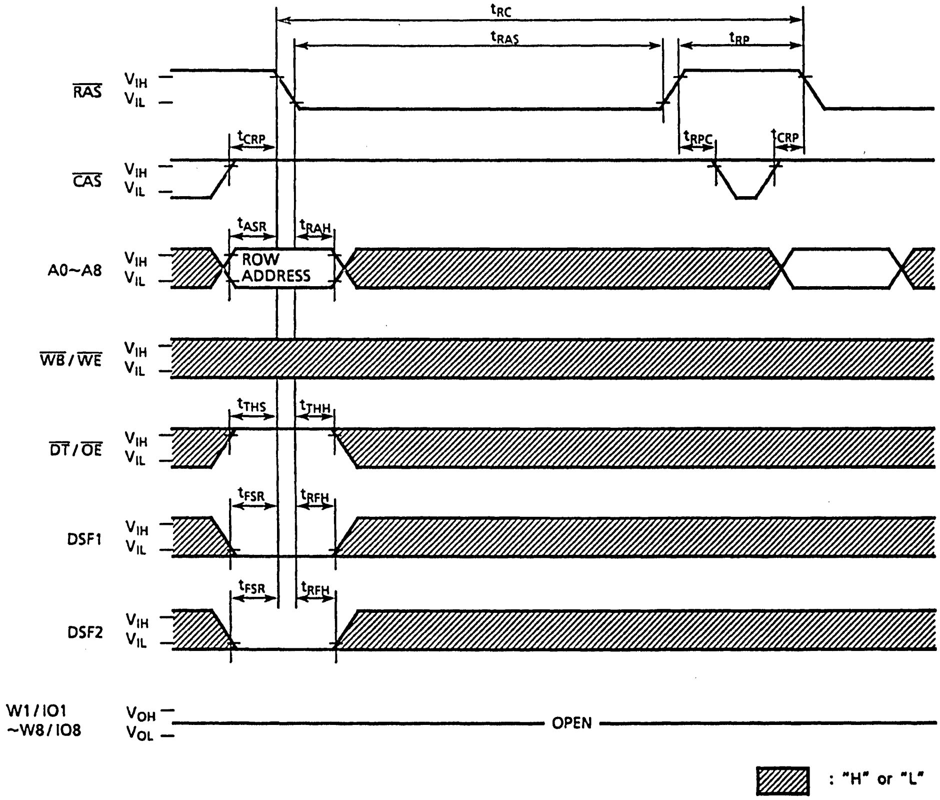
WM1 data 0: Write Disable
1: Write Enable
Don't care : '0' or '1'

***3 COLUMN SELECT**

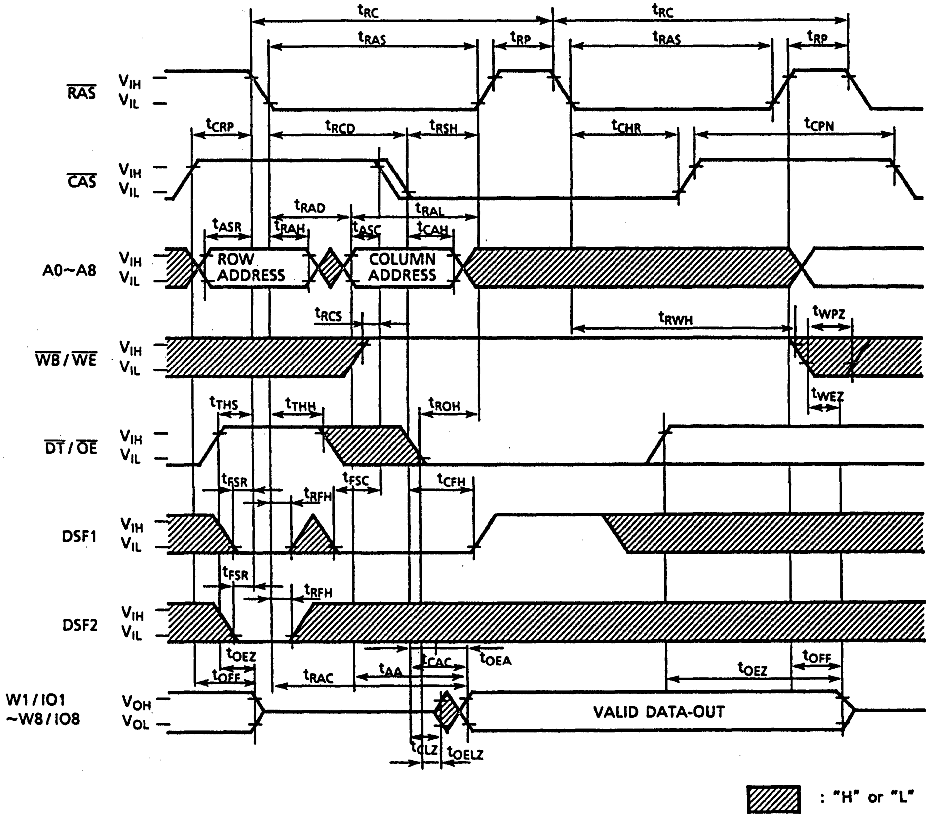
W1/IO1 - Column 0 (A_{1C}=0, A_{0C}=0
W2/IO2 - Column1 (A_{1C}=0, A_{0C}=1
W3/IO3 - Column 2 (A_{1C}=1, A_{0C}=0
W4/IO4 - Column 3 (A_{1C}=1, A_{0C}=1

Wn/IOn
=0 : Disable
=1 : Enable

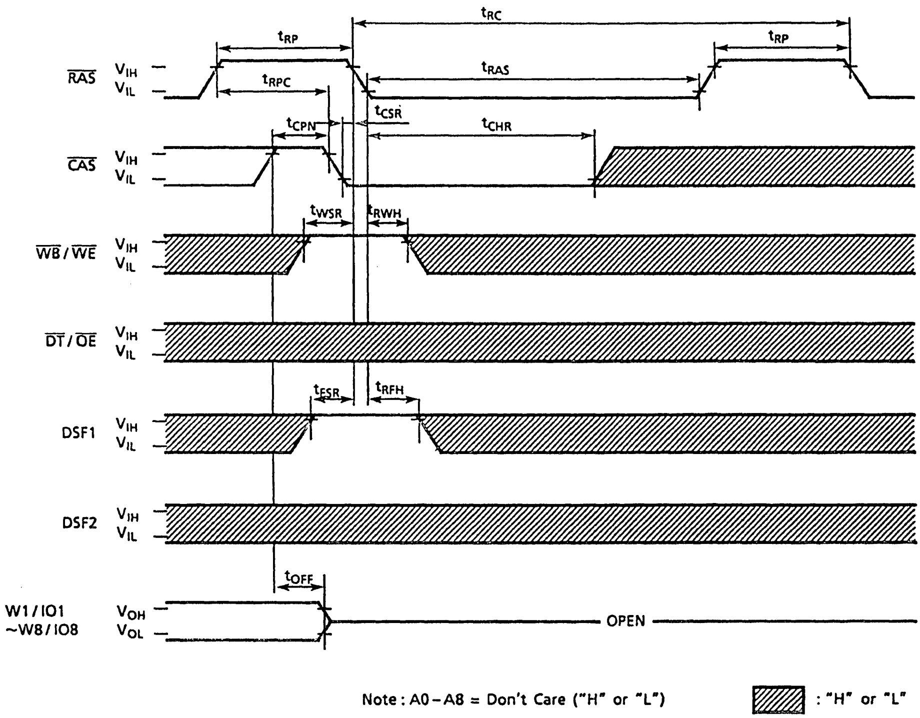
$\overline{RAS}$ ONLY REFRESH CYCLE



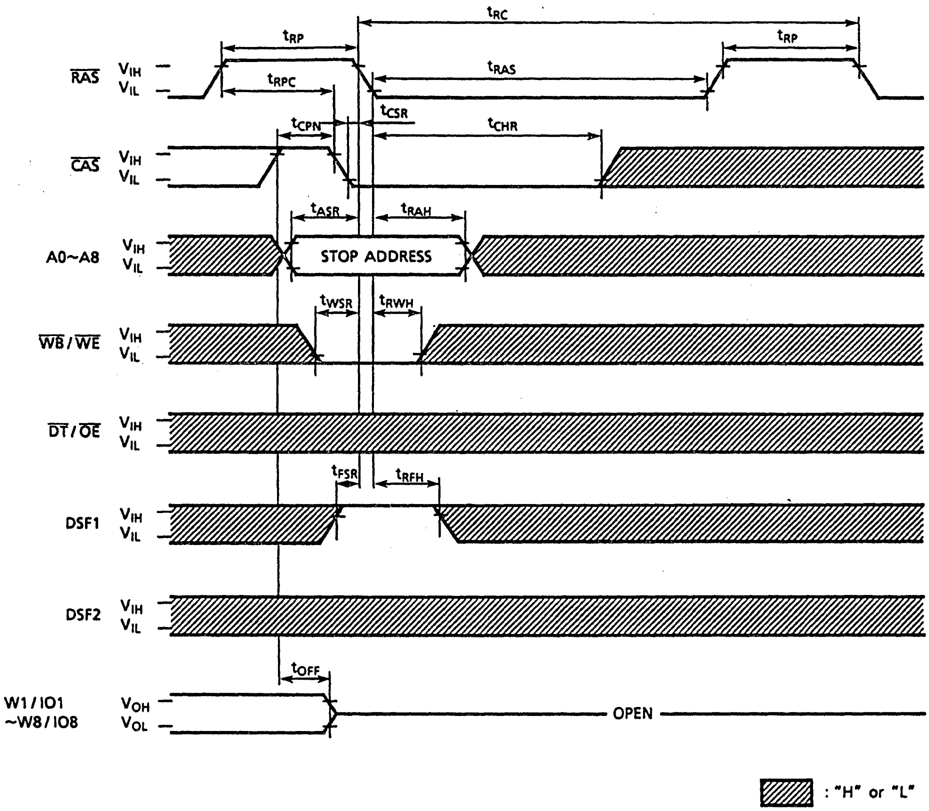
HIDDEN REFRESH CYCLE



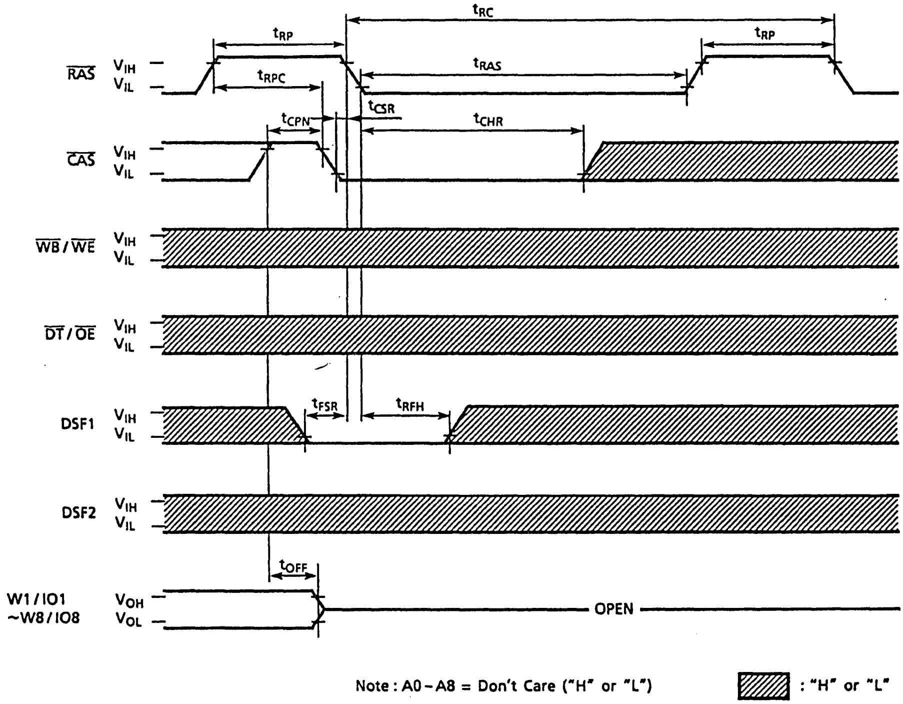
CBR AUTO REFRESH CYCLE



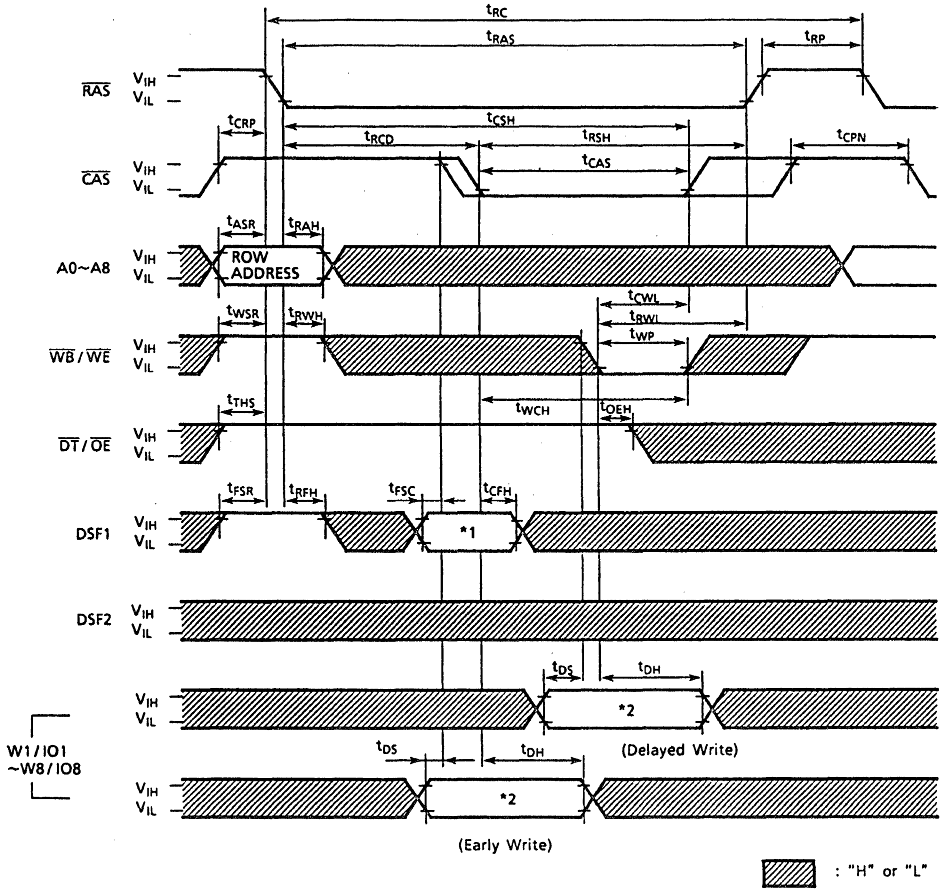
CBR AUTO REFRESH & STOP REGISTER SET CYCLE



CBR AUTO REFRESH & RESET CYCLE

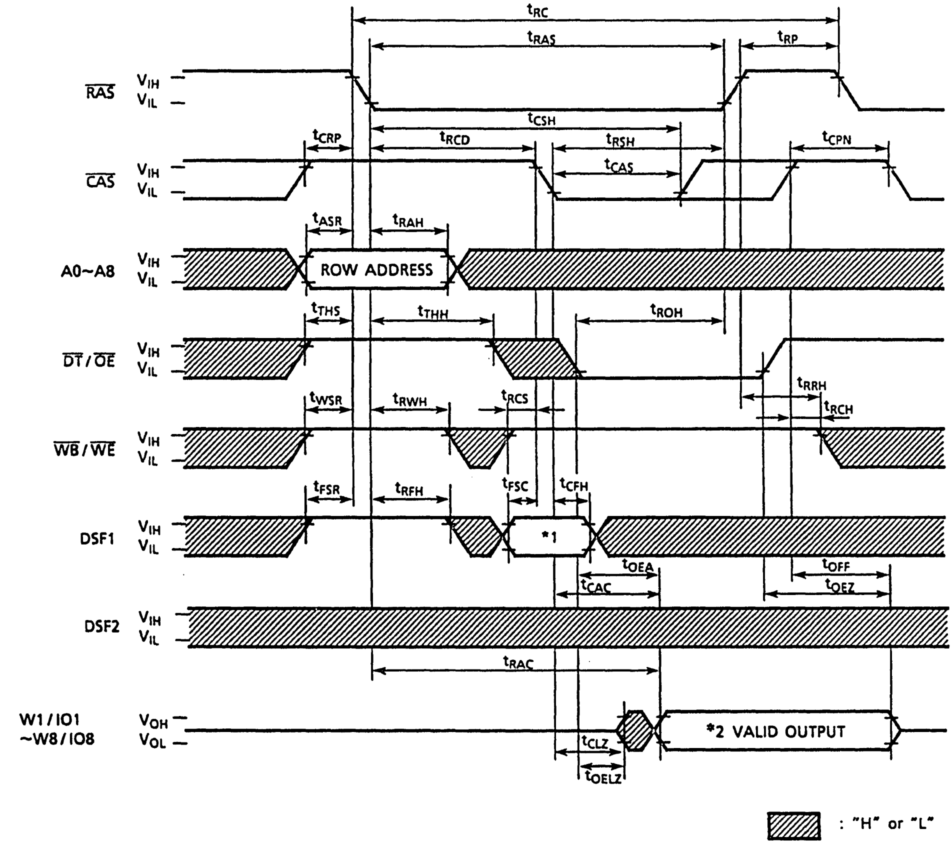


LOAD MASK/COLOR REGISTER CYCLE



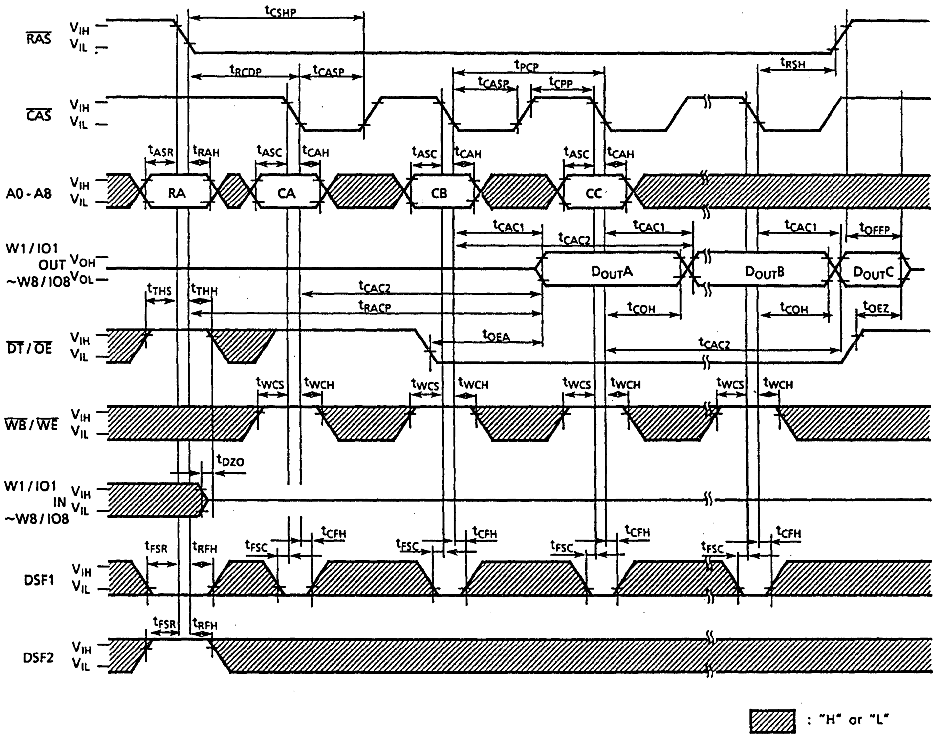
*1	*2	Function
0	Mask data	Load Mask Register Cycle
1	Color data	Load Color Register Cycle

READ MASK/COLOR REGISTER CYCLE

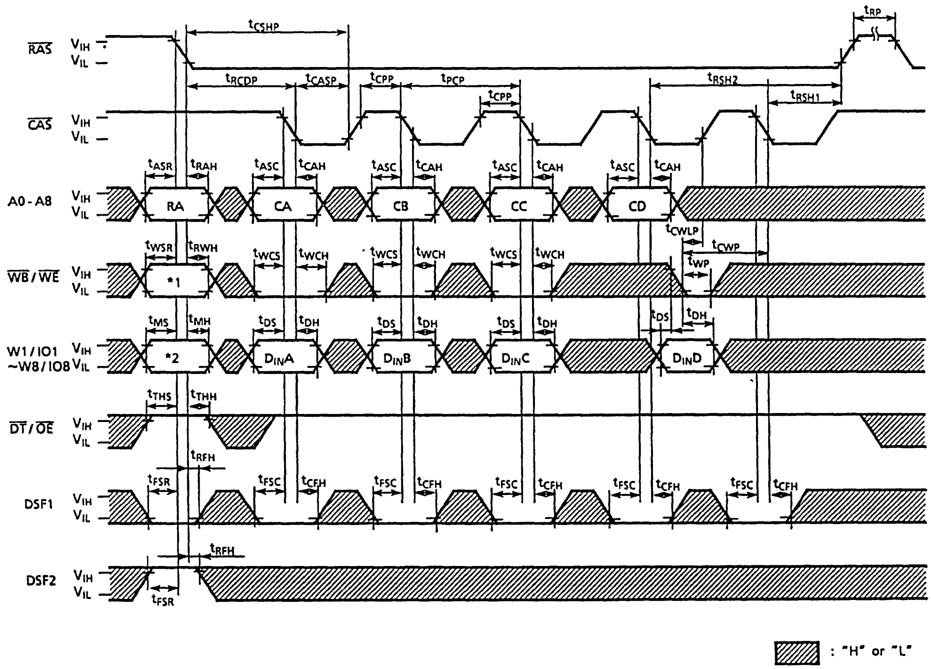


*1	*2	Function
0	Mask data	Read Mask Register Cycle
1	Color data	Read Color Register Cycle

PIPELINED FAST PAGE READ CYCLE



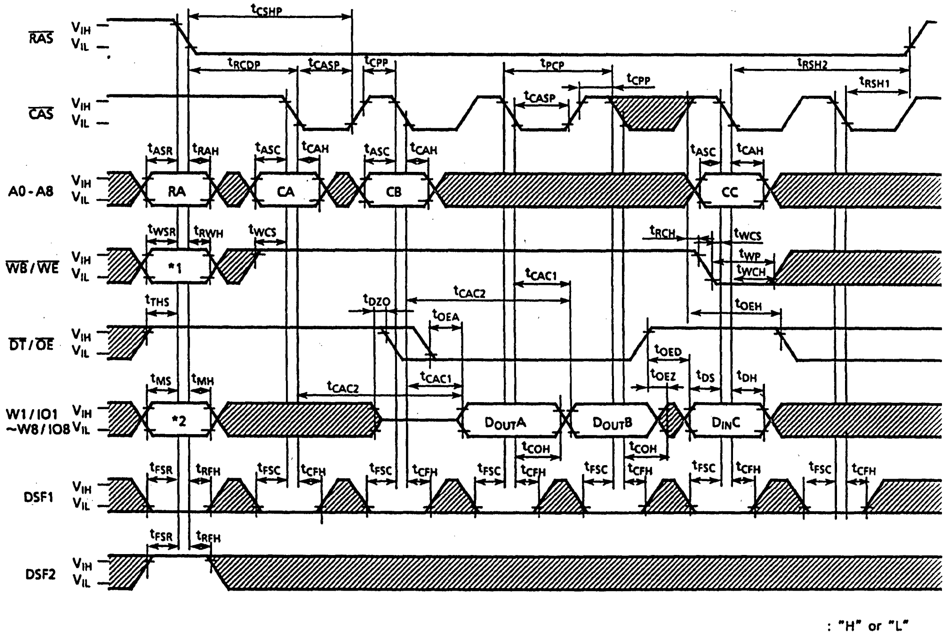
PIPELINED FAST PAGE WRITE CYCLE



Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data   0: Write Disable
            1: Write Enable
Don't care : '1' or '0'

PIPELINED FAST PAGE READ-WRITE CYCLE

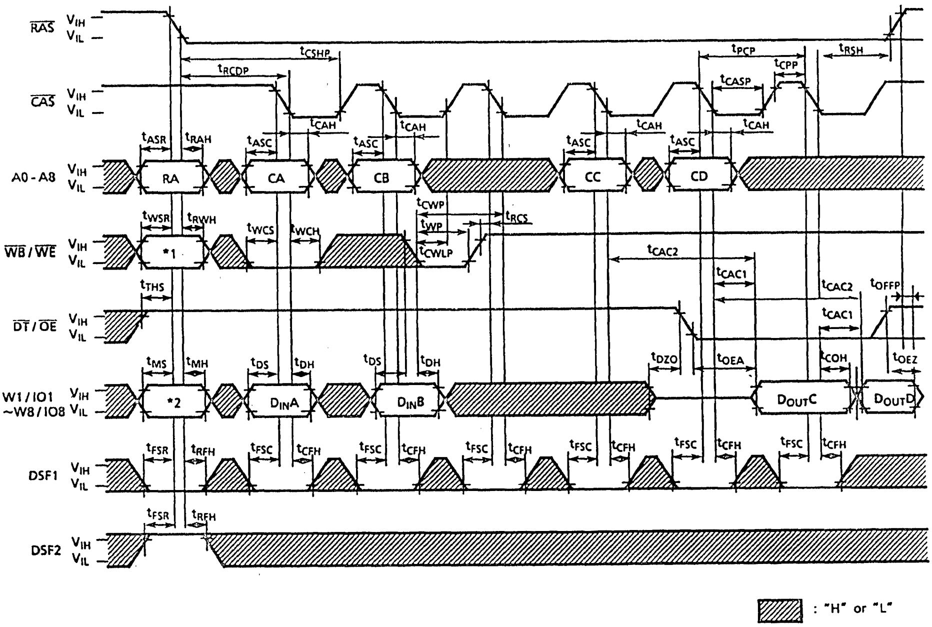


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data — 0: Write Disable
1: Write Enable

Don't care — : '1' or '0'

PIPELINED FAST PAGE WRITE-READ CYCLE

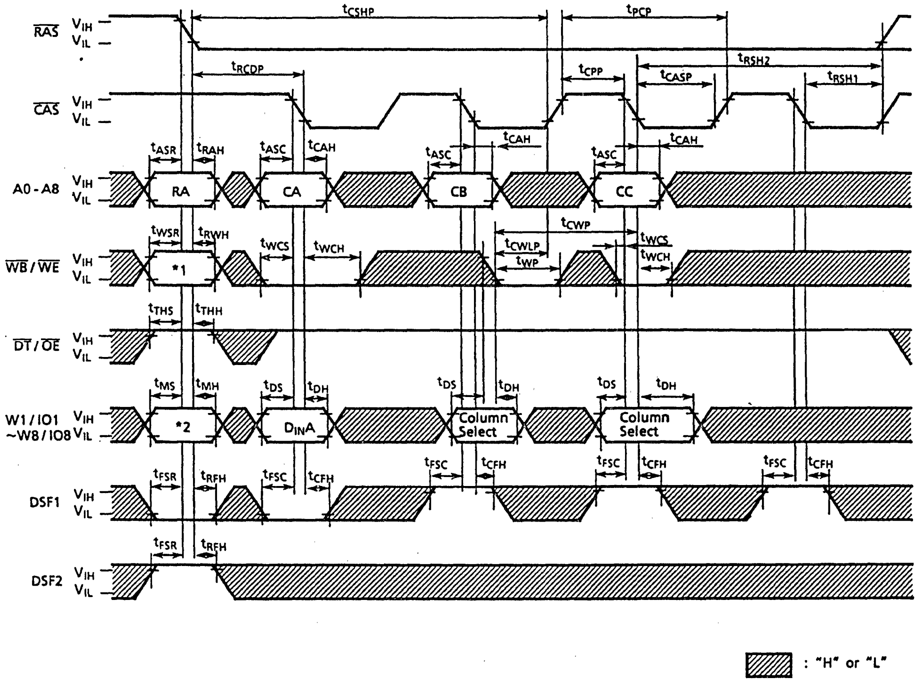


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data   0: Write Disable
            1: Write Enable

Don't care   : '1' or '0'

PIPELINED FAST PAGE WRITE-BLOCK WRITE CYCLE

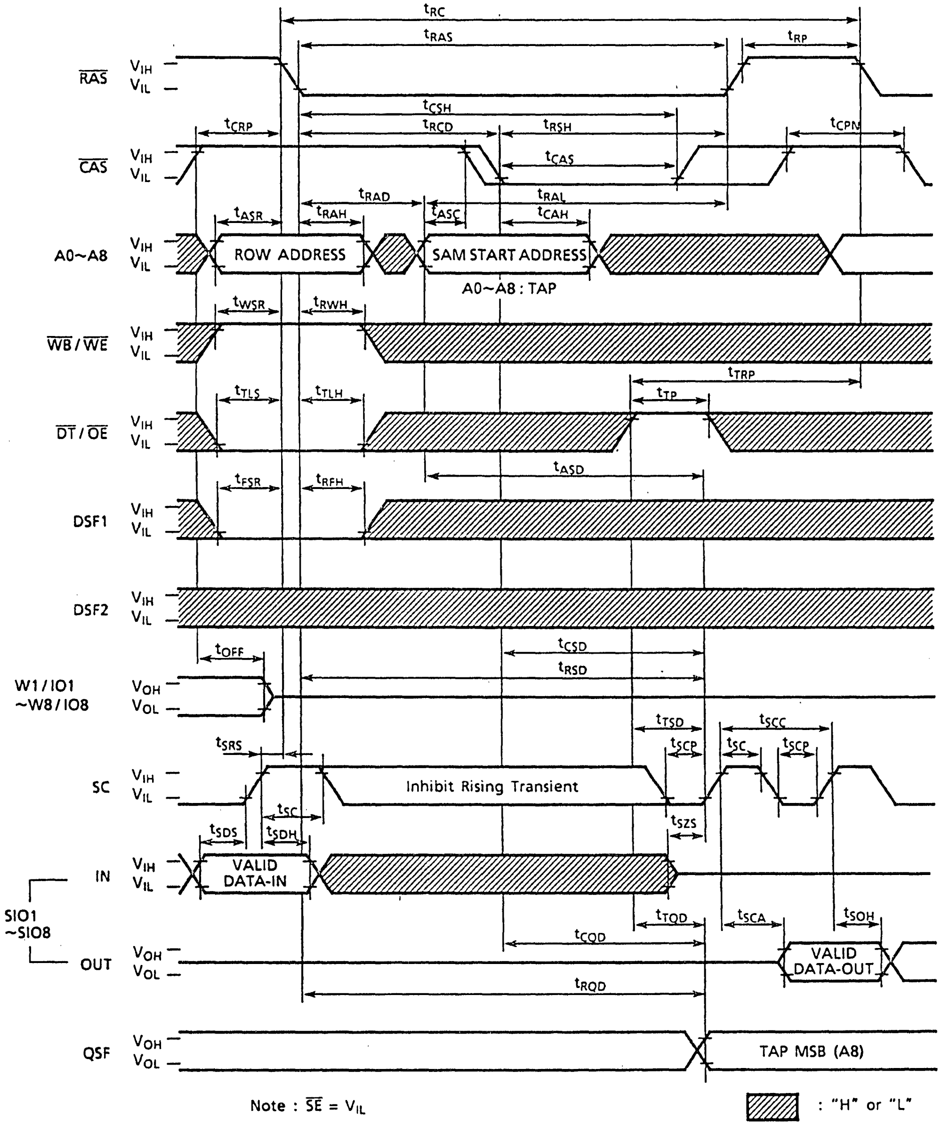


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

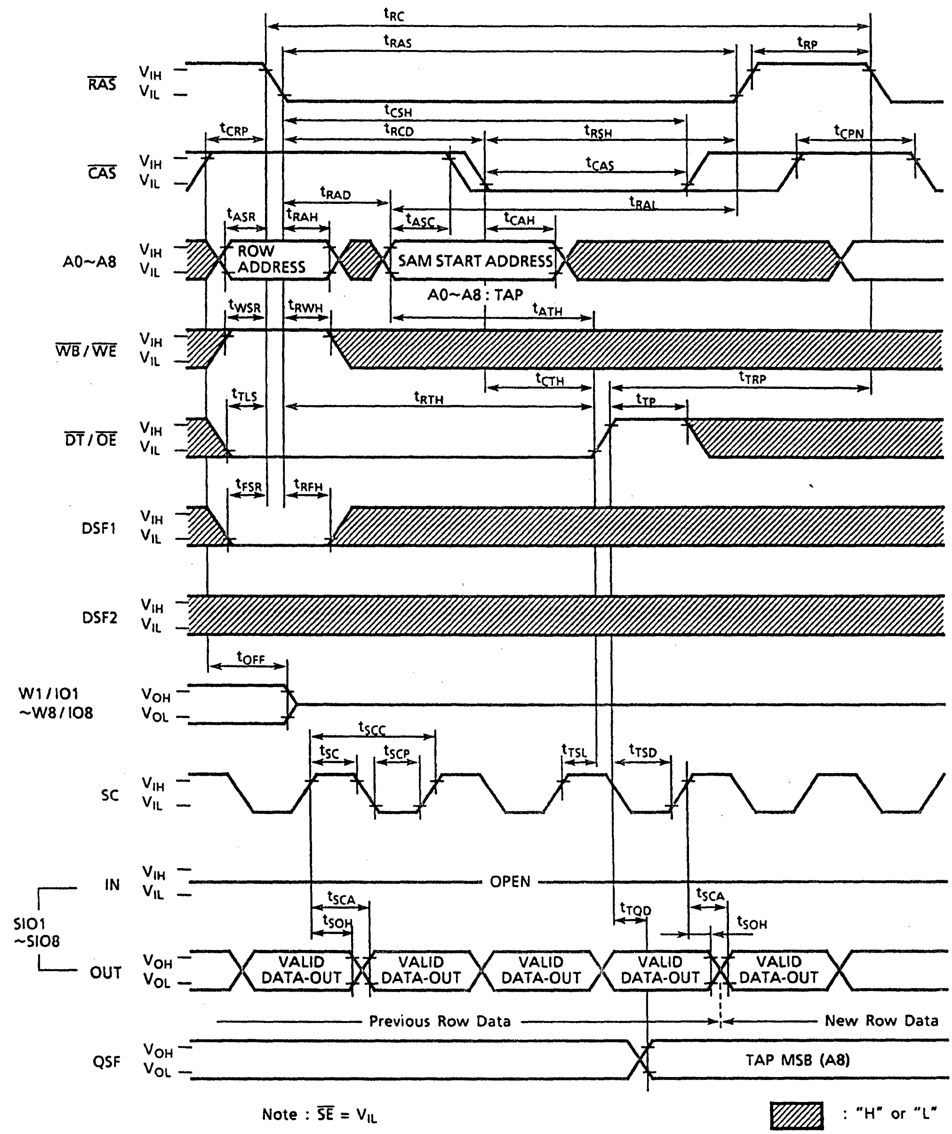
WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

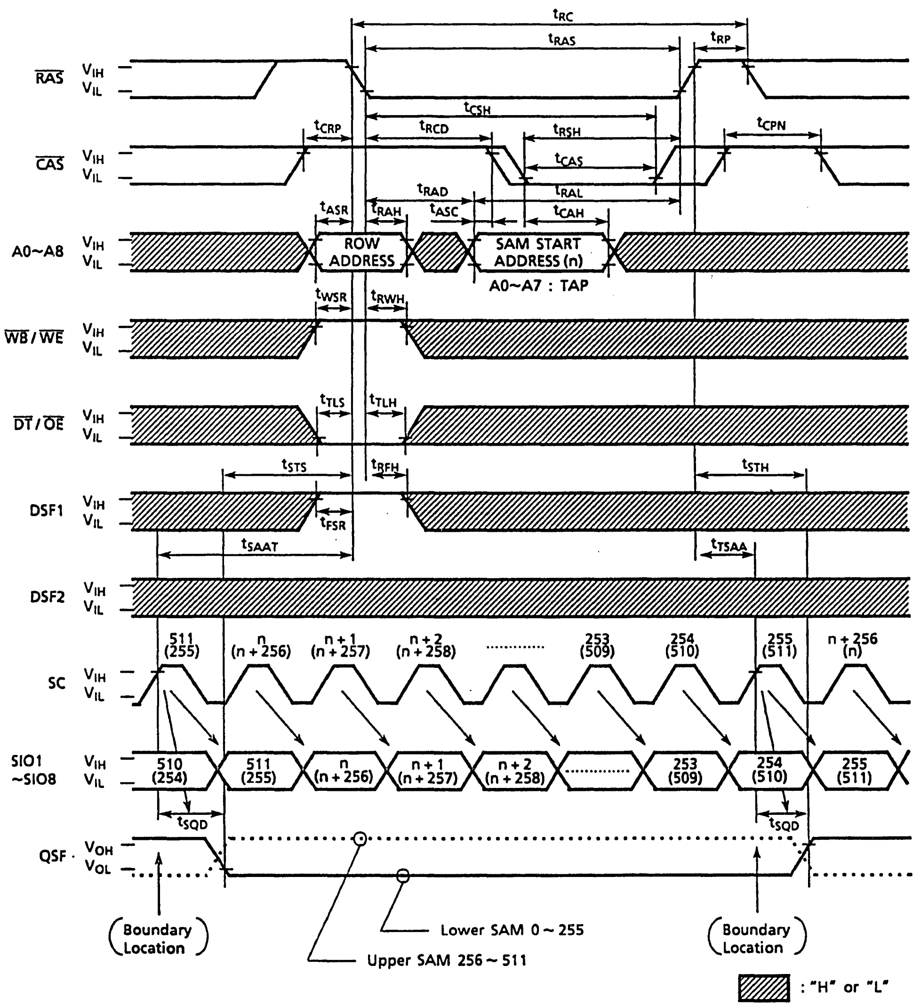
READ TRANSFER CYCLE (Previous Transfer is Write Transfer Cycle)



REAL TIME READ TRANSFER CYCLE

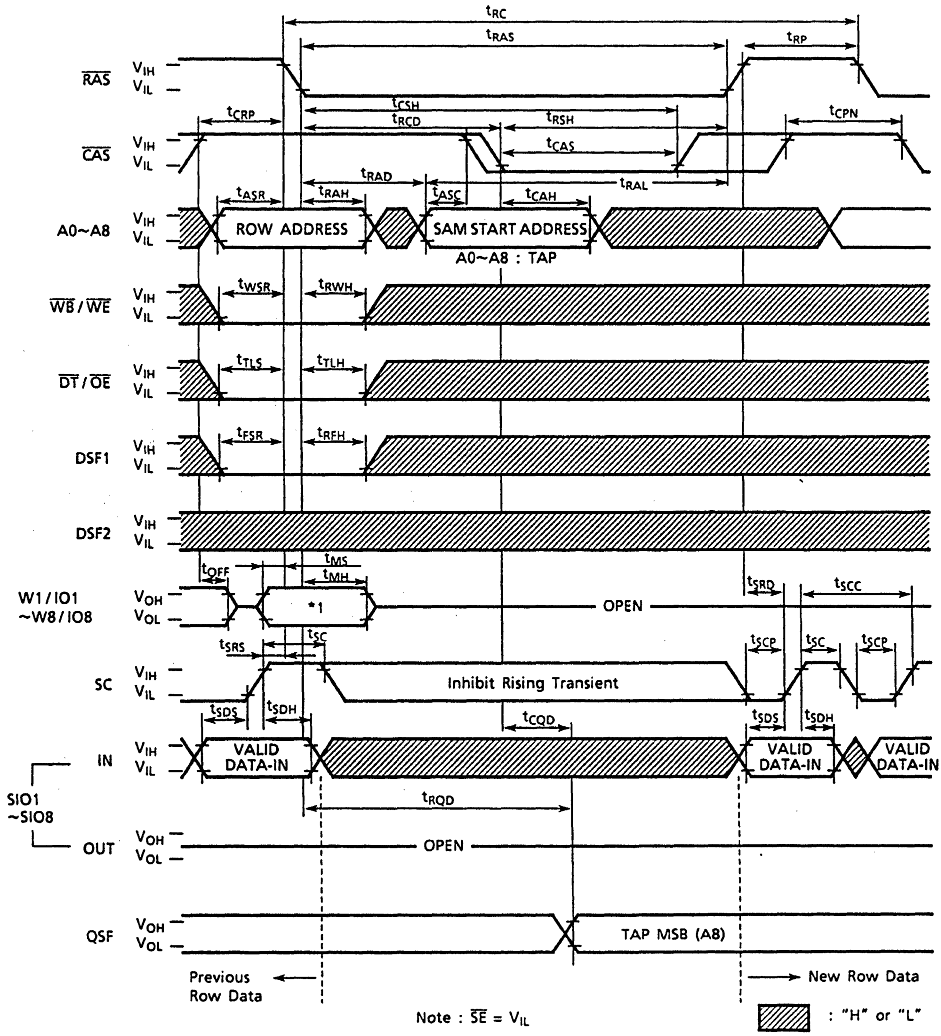


SPLIT READ TRANSFER CYCLE



Note : $\overline{SE}$ = V_{IL}

MASKED WRITE TRANSFER CYCLE

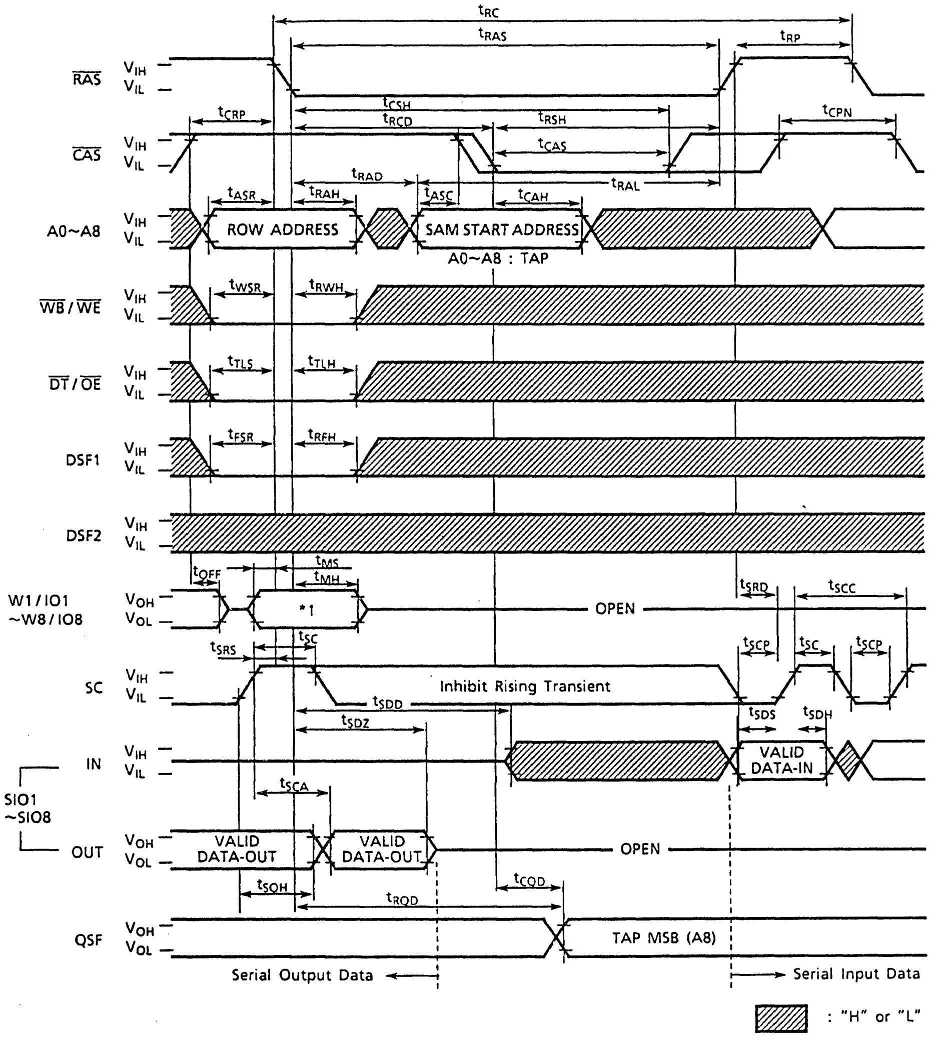


Mask Mode	*1
New Mask Mode	WM1 data
Old Mask Mode	Don’t care

WM1 data 0: Transfer Disable
1: Transfer Enable

Don’t care : ‘0’ or ‘1’

MASKED WRITE TRANSFER CYCLE (Previous Transfer is Read Transfer Cycle)

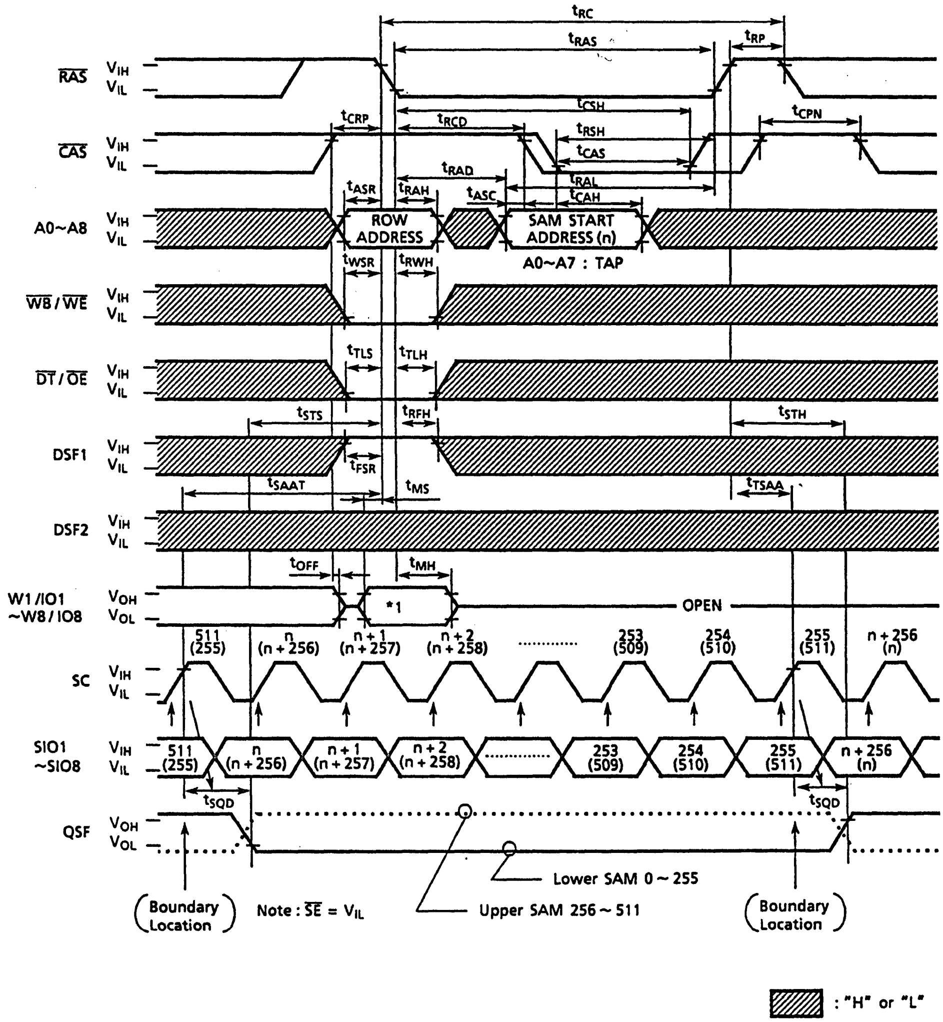


Mask Mode	*1
New Mask Mode	WM1 data
Old Mask Mode	Don't care

WM1 data 0: Transfer Disable
1: Transfer Enable

Don't care : '0' or '1'

MASKED SPLIT WRITE TRANSFER CYCLE

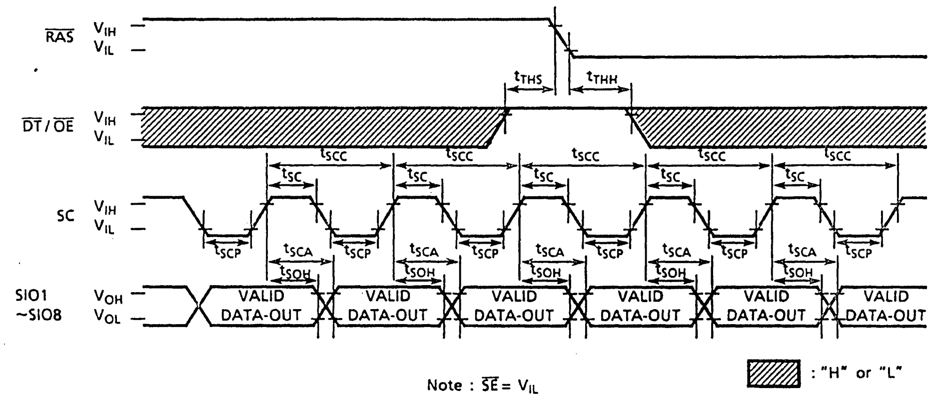


Mask Mode	*1
New Mask Mode	WM1 data
Old Mask Mode	Don't care

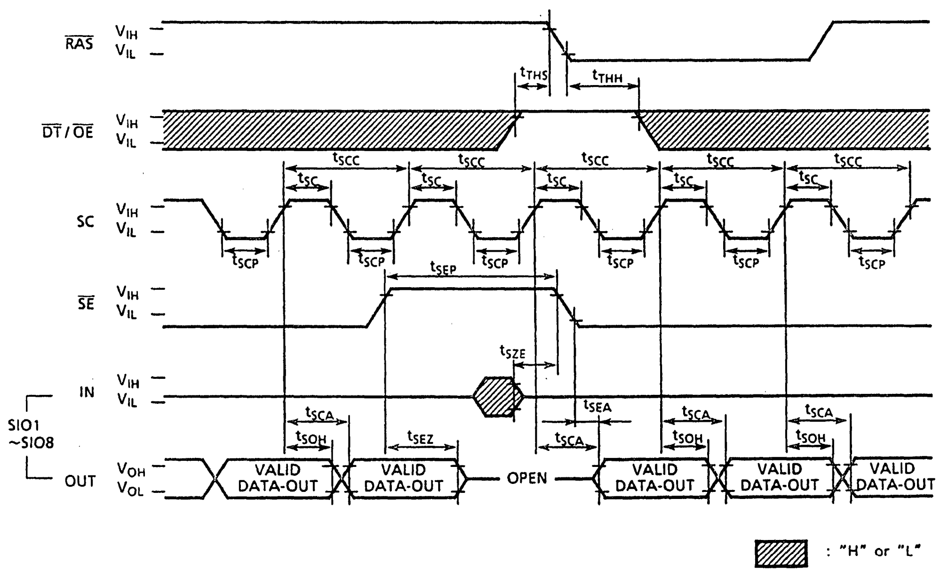
WM1 data 0: Transfer Disable
1: Transfer Enable

Don't care : '0' or '1'

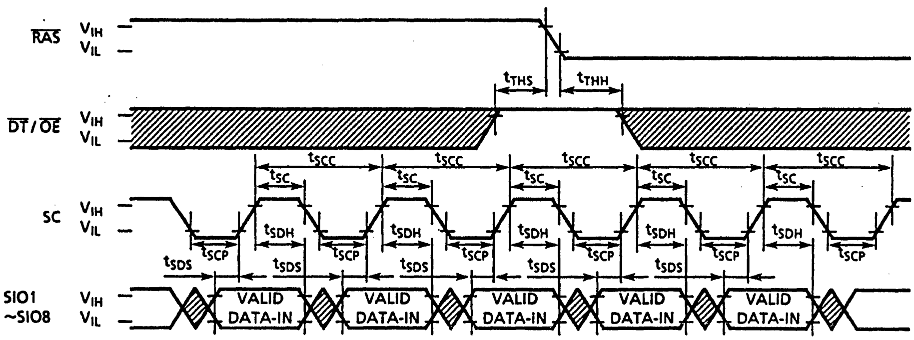
SERIAL READ CYCLE ($\overline{SE}$ = V_{IL})



SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)

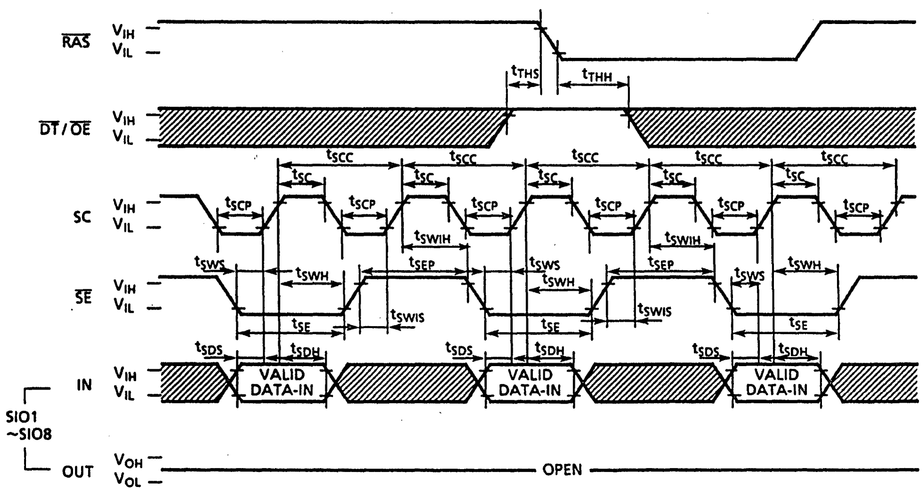


SERIAL WRITE CYCLE ($\overline{SE} = V_{IL}$)



Note : $\overline{SE} = V_{IL}$: "H" or "L"

SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



: "H" or "L"

PIN FUNCTION

ADDRESS INPUTS : A_0~A_8

The 18 address bits are required to decode 8 bits of the 2,097,152 cell locations within the dynamic RAM memory array and they are multiplexed onto 9 address input pins (A_0~A_8). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

ROW ADDRESS STROBE : $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, DSF1 and DSF2 to invoke the various random access and data transfer operating modes shown in Table 1. $\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high".

COLUMN ADDRESS STROBE : $\overline{CAS}$

$\overline{CAS}$ is the control input that latches the column address bits which are also used for the tap address during the transfer operations. The state of the special function input DSF1 is read at the $\overline{CAS}$ falling edge to select the block write mode or load register functions in conjunction with the $\overline{RAS}$ control. $\overline{CAS}$ before $\overline{RAS}$ refresh operations are selected if the signal is "low" at the $\overline{RAS}$ falling edge.

DATA TRANSFER/OUTPUT ENABLE : $\overline{DT}/\overline{OE}$

The $\overline{DT}/\overline{OE}$ input is a multifunction pin. When $\overline{DT}/\overline{OE}$ is "high" at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT}/\overline{OE}$ is used as an output enable control. If it is "low", a data transfer operation is activated between the RAM and the SAM.

WRITE PER BIT/WRITE ENABLE : $\overline{WB}/\overline{WE}$

The $\overline{WB}/\overline{WE}$ input is also a multifunction pin. When the signal is "high" at the falling edge of $\overline{RAS}$, during the RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. If the signal is "low" at the $\overline{RAS}$ falling edge, the write-per-bit function is enabled. The $\overline{WB}/\overline{WE}$ input also determines the direction of data transfer between the RAM array and the SAM.

WRITE MASK DATA/DATA INPUT AND OUTPUT: W_1/IO_1~W_8/IO_8

Data is written into the RAM through W_1/IO_1~W_8/IO_8 pins during a write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs late. In a read cycle data is read out of the RAM on the W_i / IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and column address. The 4 least bits are also used as the column address mask during a block write cycle.

When the write-per-bit function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register at the falling edge of $\overline{RAS}$. In a load mask and color register cycles, the data on the W_i/IO_i pins is stored into the write mask register and the color register respectively.

SERIAL CLOCK : SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. The serial clock SC also increments the 9-bits serial pointer which is used to select the SAM address. The SC pin must be held at a constant V_{IH} or V_{IL} level during read and masked write transfer operations and should not be clocked while the SAM is in standby mode to prevent the SAM pointer from being incremented.

SERIAL ENABLE : $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer is still incremented while SC is clocked.

SPECIAL FUNCTION CONTROL INPUT: DSF1, DSF2

DSF1 is latched at the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to select the various TC528267 operations. If the signal is kept "low", the basical functions featured in conventional multi-port DRAM are enabled. To use the block write, the flash write and the load register functions or the split transfer operations, the DSF1 signal needs to be controlled as shown in Table 1.

When the DSF2 signal is "high" at the falling edge of $\overline{RAS}$, pipelined page mode operations are enabled. The pipeline mode is supported with the read, write and block write functions.

SPECIAL FUNCTION OUTPUT: QSF

QSF is an output signal which, during split register mode, indicates which half of the split SAM is being accessed. QSF "low" indicates that the lower split SAM (Bit 0~255) is being accessed and QSF "high" indicates that the upper split SAM (Bit 256~511) is being accessed. QSF is monitored so that after it toggles and after allowing for a delay of t_{STS}, split read/write transfer operation can be performed on the non-active split SAM.

SERIAL INPUT/OUTPUT : SIO_1~SIO_8

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read or masked write transfer cycle. After a read cycle, the SI/Oi pin is in the output mode. When a masked write transfer cycle is performed, the SI/Oi is switched from output mode to input mode,

OPERATION MODE

The RAM port and data transfer operating of the TG528267 are determined by the state of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, DSF1 and DSF2 at the falling edge of $\overline{RAS}$ and by the state of DSF1 at the falling edge of $\overline{CAS}$. The Table 1 shows the functional truth table for a listing of all available RAM port and transfer operations.

Table 1. Functional Truth Table

RAS ↘					CAS ↘	Mnemonic Code	Function
CAS	DT/OE	WB/WE	DSF1	DSF2	DSF1		
0	*	*	0	*	-	CBR	CBR Auto Refresh & Option Reset 1), 2)
0	*	0	1	*	-	CBRS	CBR Auto Refresh & Stop Register 2)
0	*	1	1	*	-	CBRN	CBR Auto Refresh
1	0	0	0	*	*	MWT	Write Transer (New/Old Mask)1)
1	0	0	1	*	*	MSWT	Split Write Transfer (New/Old Mask)1)
1	0	1	0	*	*	RT	Read Transfer
1	0	1	1	*	*	SRT	Split Read Transfer
1	1	0	0	0	0	RWM	Read Write (New/Old Mask)1)
1	1	0	0	0	1	BWM	Block Write (New/Old Mask)1)
1	1	0	1	*	*	FWM	Flash Write (New/Old Mask)1)
1	1	1	0	0	0	RW	Read Write with Extended Fast Page Mode (No Mask)
1	1	1	0	0	1	BW	Block Write (No Mask)
1	1	0	0	1	0	RWM(P)	PFP3) Read Write (New/Old Mask)1)
1	1	0	0	1	1	BWM(P)	PFP3) Block Write (New/Old Mask)1)
1	1	1	0	1	0	RW(P)	PFP3) Read Write (No Mask)
1	1	1	0	1	1	BW(P)	PFP3) Block Write (No Mask)
1	1	1	1	*	0	LMR	Load (Old) Mask Register1)
1	1	1	1	*	1	LCR	Load Color Register

Note : * =0 or 1, - = Not applicable

1) After LMR operation, MWT, MSWT, RWM, BWM, FWM, RWM (P), BWM (P) use old mask. CBR operation resets the old mask mode to new mask mode.
2) CBRS operation determines binary boundaries in the SAM. CBR operation resets the boundaries.
3) PFP stands for pipelined fast page mode

RAM PORT OPERATION

1. READ WRITE FUNCTION : RW

The TC528267 is equipped with the read write function which is identical to the conventional dynamic RAM's one and supports read, early write, $\overline{OE}$ controlled write and read-modify-write cycles as shown in the timing charts. Extended fast page and pipelined page modes are also available with the read write cycles by performing multiple $\overline{CAS}$ cycles during a single active $\overline{RAS}$ cycle, a page.

1.1 EXTENDED FAST PAGE MODE

Extended fast page mode allows faster access to the memory in an actual system than the conventional fast page mode. An output data remains valid after the $\overline{CAS}$ signal goes high to prepare the next output data. Thus, the system has longer period to read the data from the RAM. Read, write and read-modify-write cycles are available during the extended fast page mode.

2. WRITE-PER-BIT (MASKED WRITE) FUNCTION : RWM

The write-per-bit (masked write) function selectively controls the internal write enable circuits of the RAM port. When $\overline{WB/WE}$ is held "low" at the falling edge of $\overline{RAS}$, during the RWM cycle, the write mask is enabled. At the same time, the mask data on the Wi/IOi pins is latched into the write-mask register. The I/O mask data maintains in a single $\overline{RAS}$ cycle, a page (New Mask Mode). When a load mask register function (LMR) is performed, the write mask data on the Wi/IOi pins is latched into the write-mask register. After the LMR operation, the data at the falling edge of $\overline{RAS}$ during the RWM cycle is ignored and the I/O mask data that was stored in the write-mask register is used (Old Mask Mode) until the mode is reset by CBR operation. The truth table of the write-per-bit function is shown in Table 2.

Table 2. Truth table for write-per-bit function

At the falling edge of $\overline{RAS}$				Write Mask Register	Function
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	W_i/IO_i (i=1~8)		
H	H	L	1	←	Write Enable
			0	←	Write Disable (New Mask)
			*	1	Write Enable
			*	0	Write Disable (Old Mask)

Note: * = 1 or 0 , ← = The data on Wi/IOi is latched.

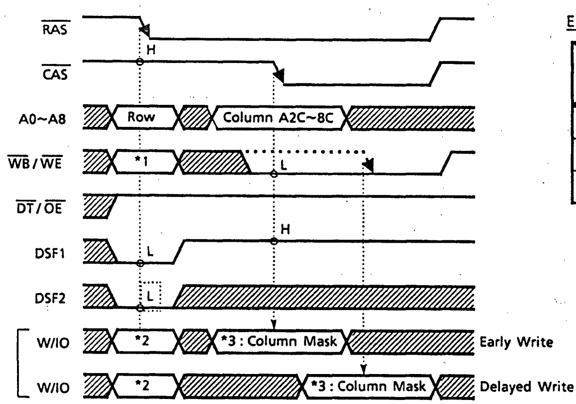
3. BLOCK WRITE AND MASKED BLOCK WRITE : BW & BWM

Block write is a special RAM port write operation which, in a page, allows for the data in the color register to be written into 4 consecutive column address locations starting from a selected column address in a selected row. The block write operation can be selectively disabled on an I/O basis and a column mask capability is also available.

A block write cycle is performed by holding $\overline{CAS}$, $\overline{DT}/\overline{OE}$ "high" and DSF1 "low" at the $\overline{RAS}$ falling edge and by holding DSF1 "high" at the $\overline{CAS}$ falling edge. If the DSF signal is "low" at the $\overline{CAS}$ falling edge, a read write operation will occur. Therefore, a combination of block write, read and write operations can be performed during a fast page mode cycle. The state of $\overline{WB}/\overline{WE}$ input at the falling edge of $\overline{RAS}$ determines whether or not the I/O mask is enabled ($\overline{WB}/\overline{WE}$ must be "low" to enable the I/O mask, BMW mode or "high" to disable it, BW mode). The I/O mask is provided on the Wi/IOi input at the $\overline{RAS}$ falling edge. After LMR operation, however, the old mask is used for the I/O mask function. The column mask data on the Wi/IOi input must be provided at the $\overline{CAS}$ or $\overline{WB}/\overline{WE}$ falling edge whichever is late, while the seven most significant colunm address (A2C~A8C) are latched at the falling edge of $\overline{CAS}$.

An example of the block write function is shown in Figure 1 with a mask on W_3/IO_3, W_4/IO_4, W_6/IO_6, W_8/IO_8 and column 1. The block write is most effective for window clear and fill operation in frame buffer applications.

Figure 1. Block Write Operation



Example

	W/IO 1	2	3	4	5	6	7	8
WM1 Register	1	1	(0)	(0)	1	(0)	1	(0)
Column Select	1	(0)	1	1	–	–	–	–
Color Register	1	0	1	0	1	1	0	0

Result

	W/IO 1	2	3	4	5	6	7	8
Column 0	1	0			1		0	
Column 1								
Column 2	1	0			1		0	
Column 3	1	0			1		0	

*1	*2	Mask Mode
1	Don't Care	No Mask Mode
0	WM1	New Mask Mode
0	Don't Care	Old Mask Mode

*3 COLUMN SELECT

W_1/IO_1 - Column 0 (A1C=0, A0C=0
W_2/IO_2 - Column 1 (A1C=0, A0C=1
W_3/IO_3 - Column 2 (A1C=1, A0C=0
W_4/IO_4 - Column 3 (A1C=1, A0C=1

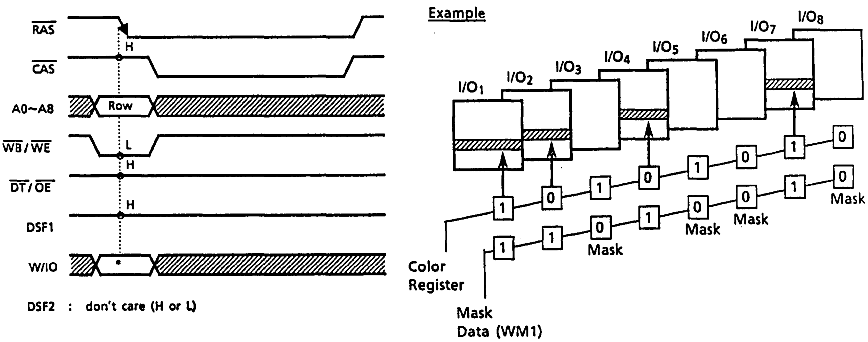
4. FLASH WRITE : FWM

Flash write is also a special RAM port operation which in a single $\overline{RAS}$ cycle, allows for the data in the color register to be written into all the memory locations of a selected row. Each bit of the color register corresponds to one of the DRAM I/O blocks and the flash write operation can be selectively controlled on an I/O basis in the same manner as the write-per-bit operation.

A flash write cycle is performed by holding $\overline{CAS}$ "high", $\overline{WB}/\overline{WE}$ "low" and DSF1 "high" at the falling edge of $\overline{RAS}$. The mask data must also be provided on the Wi/IOi inputs in order to enable the flash write operation for selected I/O blocks. After a LMR operation, however, the old mask in the mask register is used for the I/O block masking.

Flash write is most effective for fast plane clear operations in frame buffer applications. Selected planes can be cleared by performing 512 flash write cycle and by specifying a different row address location during each flash write cycle. Assuming a cycle time of 130ns, a plane clear operation can be completed in less than 66.6 µsec.

Figure 2. Flash Write Operation



*	Mask Mode
Mask Data	New Mask Mode
Don't Care (H or L)	Old Mask Mode

5. PIPELINED FAST PAGE MODE : RWM (P), BWM (P), RW (P), BW (P)

Pipelined fast page mode allows much faster access to the memory than the conventional page mode. Read, write and block write cycles are available at the pipelined fast page mode timings.

A pipelined fast page mode is performed by holding DSF2 "high" at the falling edge of $\overline{\text{RAS}}$. A pipelined fast page read, write and block write operations can run at 30ns cycle time for 70ns version. Also, those mode can be selected every $\overline{\text{CAS}}$ cycle by the status of $\overline{\text{DT}}/\overline{\text{OE}}$, $\overline{\text{WB}}/\overline{\text{WE}}$ and DSF1 pin. There are, however, penalties on the performance as follows :

(1) Two $\overline{\text{CAS}}$ cycles are required for the read operation. The fast access, hence, takes longer than page mode. Also, one $\overline{\text{CAS}}$ cycle is needed to read out the data before the write cycle starts in the same page.

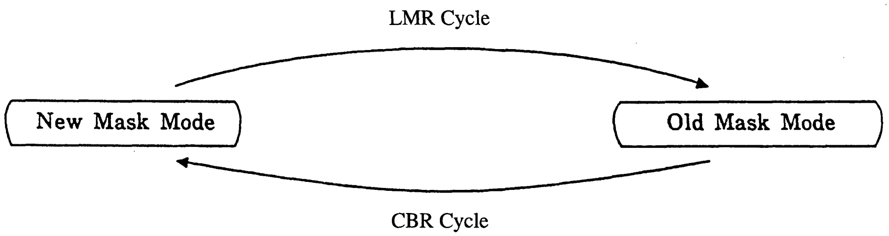
(2) One dummy cycle is needed to complete the write and block write operation. The cycle is, thus, needed between the write and the read operation and is required before the page ends.

A system designer needs to carefully estimate the system performances with the pipelined page mode and the conventional page mode in order to decide which mode should be used.

6. LOAD (OLD) MASK REGISTER : LMR

The TC528267 has an on-chip 8 bit write-mask register which provides the I/O mask data during the masked functions such as the write-per-bit (RWM), masked block write (BWM), flash write (FWM) and write transfer (MWT, MSWT) functions. Each bit of the write-mask register corresponds to one of the DRAM I/O blocks. After the mask data is specified in the write-mask register by using the load mask register (LMR) cycle, the old mask mode is invoked during the masked functions. The I/O mask data in the write-mask register maintains until another LMR operation is performed during the old mask mode. The LMR cycle is initiated by holding $\overline{\text{CAS}}$, $\overline{\text{DT}}/\overline{\text{OE}}$, $\overline{\text{WB}}/\overline{\text{WE}}$ and DSF1 "high" at the falling edge of $\overline{\text{RAS}}$ and by DSF1 "low" at the falling edge of $\overline{\text{CAS}}$. The data presented on the Wi/IOi lines are subsequently latched into the write-mask register at the falling edge of either $\overline{\text{CAS}}$ or $\overline{\text{WB}}/\overline{\text{WE}}$, whichever occurs later. The old mask mode is reset to the new mask mode by a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle (CBR). During the LMR cycle, the memory calls of the row address which is latched at the falling edge of $\overline{\text{RAS}}$ are refreshed.

Figure 3. State Diagram of Mask Mode



7. LOAD COLOR REGISTER : LCR

The TC528267 is provided with an on-chip 8-bits register (color register) for use during the block write or flash write function. Each bit of the color register corresponds to one of the DRAM I/O blocks. The load color register cycle is initiated by holding $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and DSF1 "high" at the falling edge of $\overline{RAS}$. The data presented on the Wi/IOi lines is subsequently latched into the color register at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs later. During the load color register cycle, the memory cells on the row address latched at the falling edge of $\overline{RAS}$ are refreshed.

8. REFRESH

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of 512 rows in the DRAM array within the specified 8 ms refresh period. The TC528267 supports the conventional dynamic RAM refresh operations such as $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh and hidden refresh.

8.1 $\overline{CAS}$ before $\overline{RAS}$ Refresh and Option Reset : CBR

The CBR cycle reset the following functions, performing the $\overline{CAS}$ before $\overline{RAS}$ refresh operation at the same time.

- To reset the old mask mode to the new mask mode for the masked functions.
- To reset the stop register and remove the binary boundaries for the split SAM operation,

The systems which implement neither the old mask mode nor the binary boundary in the SAM is recommended to use the CBR cycle for refresh operation.

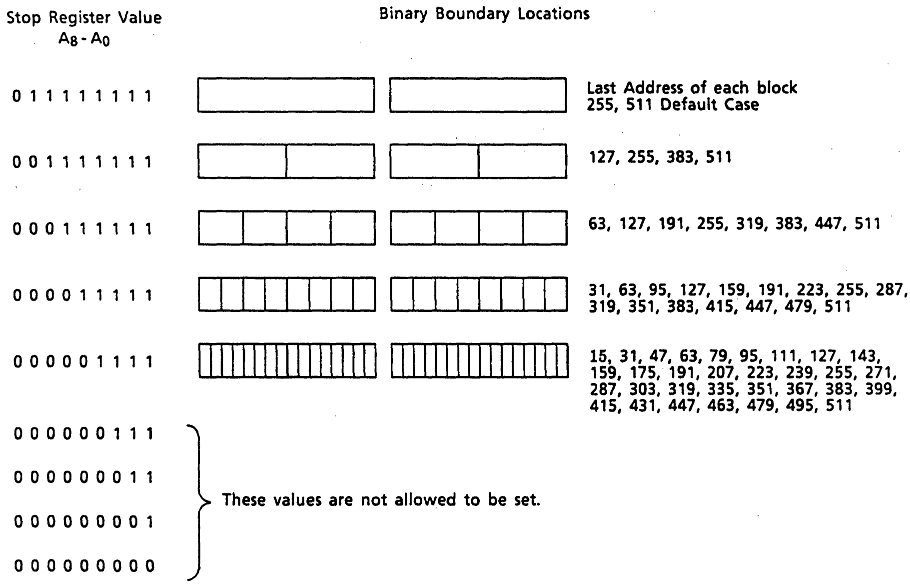
8.2 $\overline{CAS}$ before $\overline{RAS}$ Refresh : CBRN

The CBRN cycle performs only the $\overline{CAS}$ before $\overline{RAS}$ refresh operation. The systems which implement either the old mask mode or the binary boundary in the SAM usually use the CBRN cycle for refresh operation except for at the required stop register set or option reset cycles. The CBRN cycle must not be used during the initialization after power-up,

8.3 $\overline{CAS}$ before $\overline{RAS}$ Refresh and Stop Register Set : CBRS

The CBRS cycle sets the stop register to place binary boundaries in each falf SAM, performing the $\overline{CAS}$ before $\overline{RAS}$ refresh operation at the same time. The CBRS cycle is initiated by $\overline{CAS}$ holding "low" and by $\overline{WB/WE}$ and DSF1 "high" at the falling edge of $\overline{RAS}$. At the same time the data on the address pins, A_0 - A_8 is latched and the binary boundaries in each half SAM will be available when a split transfer operation is performed,

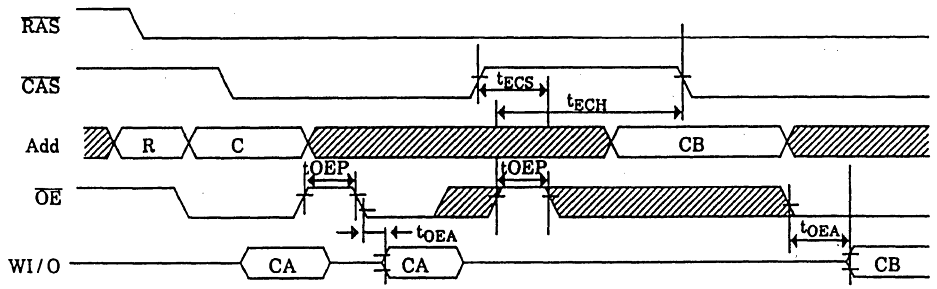
Figure 4 . Stop Register and Binary Boundary Location



NOTE

$\overline{OE}$ control of Extended Fast Page mode Read cycle

When $\overline{OE}$ is toggled while $\overline{CAS}$ is "Low" level in fast page mode read cycle, the same data is valid on WI/O. However, the data will not be valid when $\overline{OE}$ goes low with $\overline{CAS}$ high condition. The data will come out in following $\overline{CAS}$ cycle. Such a $\overline{OE}$ control have to satisfy t_{OEP} (10ns min), t_{ECS} (10ns min), t_{ECH} (10ns min). Please refer following Figure.



DATA TRANSFER OPERATION

The TC528267 features two types of internal bidirectional data transfer capability between the RAM and the SAM, as shown in Figure 5. During a normal transfer, 512 words by 8 bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer), During a split transfer, 256 words by 8 bits of data can be loaded from the lower / upper half of the RAM into the lower / upper half of the SAM (Split Read Transfer) or from the lower/upper half of the SAM into the lower/upper half of the RAM (Split Write Transfer). The normal transfer and split transfer modes are controlled by the DSF1 input signal

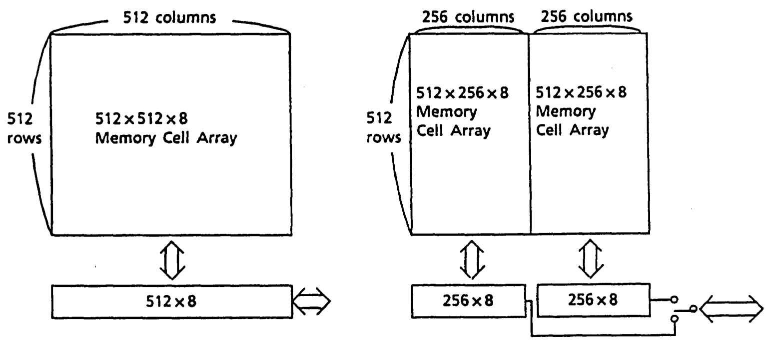


Figure 5. (a) Normal Transfer (b) Split Transfer

Table 3. shows the truth table of each Transfer Modes

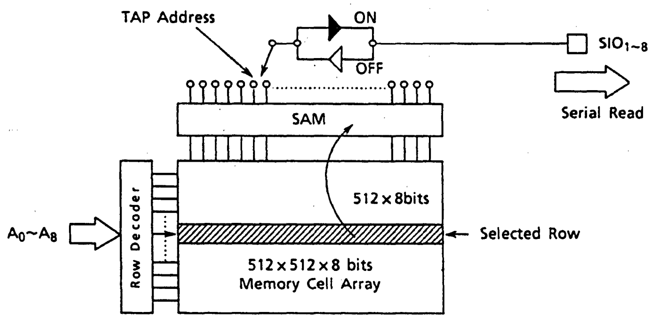
$\overline{RAS}$ ↓				Mnemonic Code	Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DFS1					
H	L	H	L	RT	Read Transfer	RAM → SAM	512x8	Input → Output
H	L	L	L	WT	Write Transfer (New/Old Mask)	SAM → RAM	512x8	Output → Input
H	L	H	H	SRT	Split Read Transfer	RAM → SAM	256x8	Not changed
H	L	L	H	SWT	Split Write Transfer (New/Old Mask)	SAM → RAM	256x8	Not changed

9. READ TRANSFER CYCLE : RT

A read transfer consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low" $\overline{WB}/\overline{WE}$ "high" and DSF1 "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. At the same time, the SAM port is set into the output mode. The start address of the serial pointer of the SAM (TAP address) is determined by the column address selected at the falling edge of $\overline{CAS}$. By doing a tight timing control between the $\overline{DT}/\overline{OE}$ rising edge and SC falling edge, a real time read transfer operation can also be performed.

Figure 6 shows the operation block diagram for read transfer operation.

Figure 6. Block Diagram for Read Transfer Operation



In a read transfer cycle (which is preceded by a write transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}/\overline{OE}$ and the falling edge of $\overline{RAS}$ and $\overline{CAS}$, as shown in READ TRANSFER CYCLE timing chart.

10. WRITE TRANSFER CYCLE : WT

A write transfer cycle consists of loading the content of the SAM register into a selected row of the RAM array. The write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low", and DSF1 "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM (TAP address). After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.

The write transfer is selectively controlled per RAM I/O block by setting the mask data on the Wi/IOi lines at the falling edge of $\overline{RAS}$ (some as in the write-per-bit operation). Before the serial clock starts loading the data into the SAM through SIO pins, the write transfer operation with all I/O blocks disabled must be performed in order to change the SAM port from output. Please note that the conventional pseudo write transfer is not available in the TC528267. The mask function is switched between the new and old mask mode by the LMR and CBR cycle.

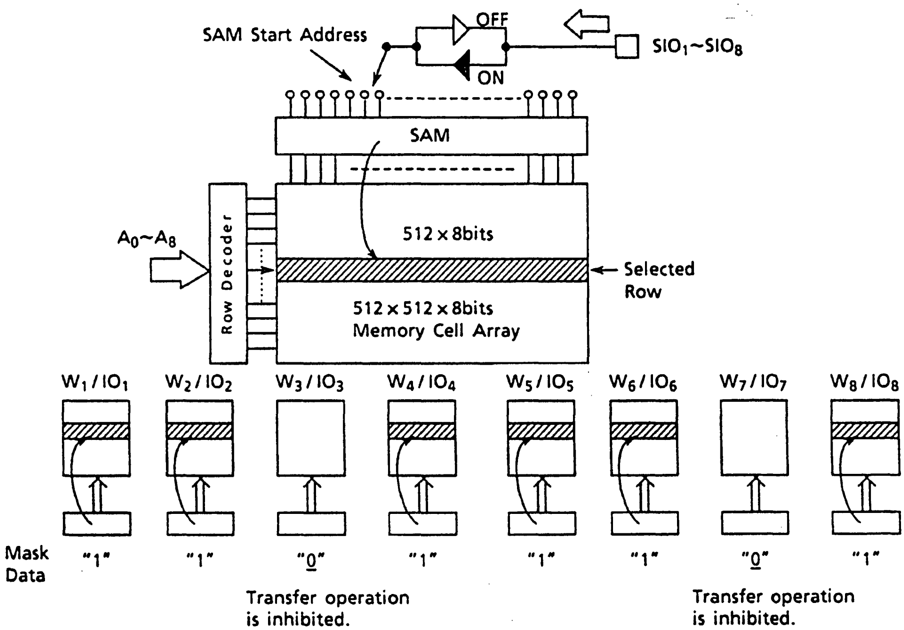


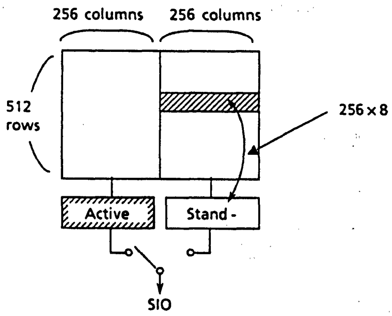
Figure 7. Block Diagram for Write Transfer Operation

When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$, at which time a new row of data can be written in the serial register.

11. SPLIT READ TRANSFER CYCLE : SRT

A split read transfer consists of loading 256 words by 8 bits of data from a selected row of the half RAM array into the corresponding half SAM in stand-by mode. Serial data can be shifted out of the other half of the SAM in active mode simultaneously, as shown in Figure 8. The most significant column address (A8C) is controlled internally to determine which half of the SAM will be reloaded from the RAM array. During the split read transfer operation, the RAM port control signals do not have to be synchronized with the serial clock SC, thus eliminating the timing restrictions as in the case of real time read transfers. Prior to the execution of the split read transfer operation, a (normal) transfer operation must be performed to determine the absolute tap address location. QSF is an output that indicates which half of the SAM is in the active state.

QSF changes state when the last SC clock is applied to the active SAM, as shown in Figure 9.



Active SAM	QSF Level
lower SAM	"Low"
upper SAM	"High"

Figure 8. Split Read Transfer

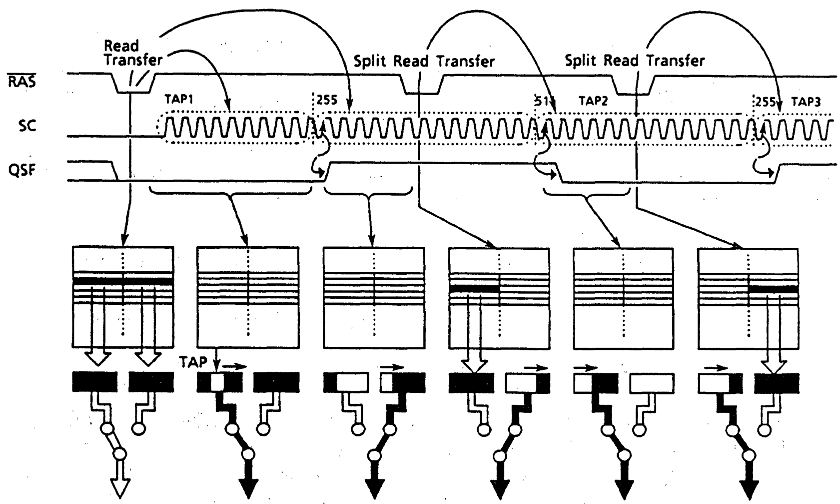


Figure 9. Example of Consecutive Read Transfer Operations

12. SPLIT WRITE TRANSFER : MSWT

A split write transfer is the similar function to the split read transfer. The difference is that the transfer direction is from the stand-by half SAM into a selected row of the corresponding half RAM array. Also, serial data can be shifted into the other half of the SAM simultaneously, as shown in Figure 10. New and old mask capability is supported in the MSWT cycle as is in the write transfer operation. Prior to the execution of the split write transfer operation, a write transfer operation, in which all I/O blocks are usually disabled, must precede to switch the SAM port from output mode to input mode and to set the initial TAP location for the serial input operation.

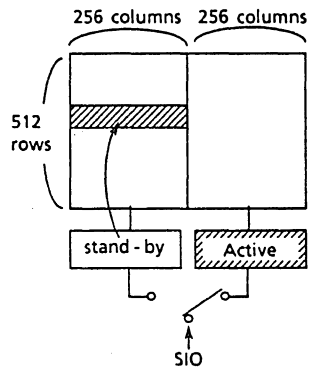


Figure 10. Block Diagram for Split Write Transfer

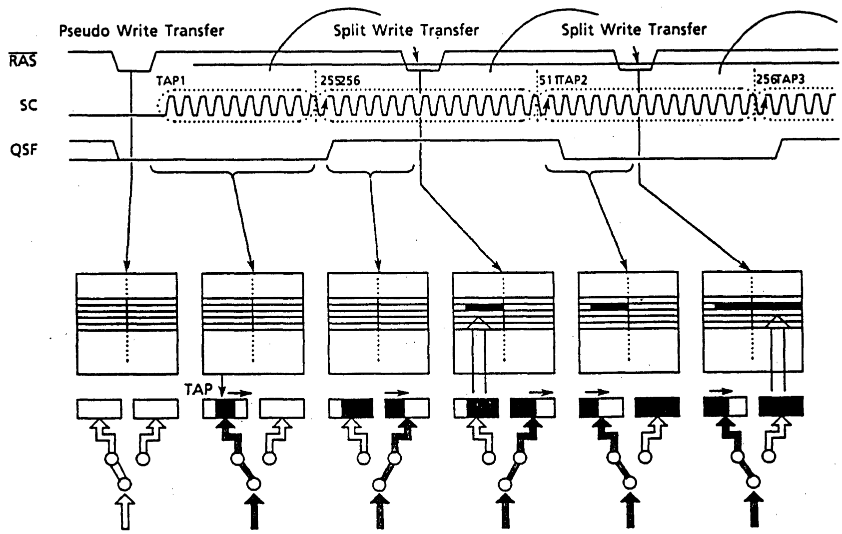
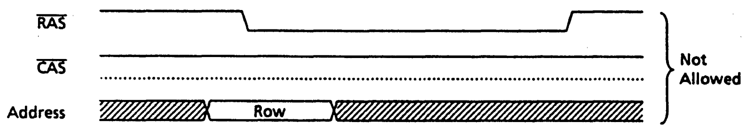


Figure 11. Example of Consecutive Write Transfer Operations

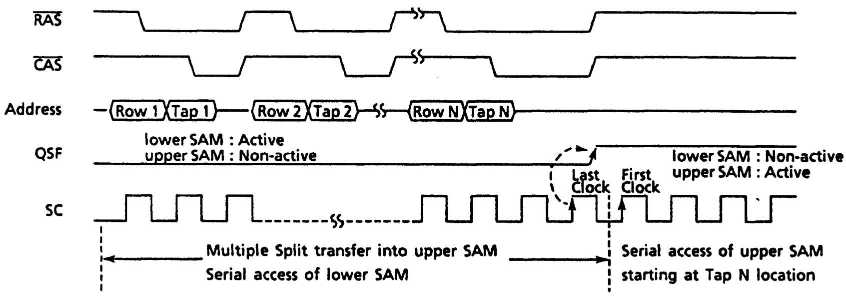
NOTES

(1) Transfer operation without $\overline{CAS}$.

The SAM tap location is undefined if $\overline{CAS}$ is maintained at a constant "high" level during a transfer cycle. A transfer cycle with $\overline{CAS}$ held "high" is, hence, not allowed.



(2) In the case of multiple split transfers performed into the same half SAM, the tap location specified during the last split transfer, before QSF toggles, will prevail, as shown below.



(3) Split transfer operation allowable period.

Figure 12 illustrates the relationship between the serial clock SC and the special function output QSF during split read / write transfers and highlights the time periods where split transfers are allowed, relative to SC and QSF. A split transfer is not allowed during to $t_{STH} + t_{STS}$. In the case that the CBRS operation is executed and the binary boundary in each half SAM is set or updated, an additional period is applied, as shown in Figure 12.

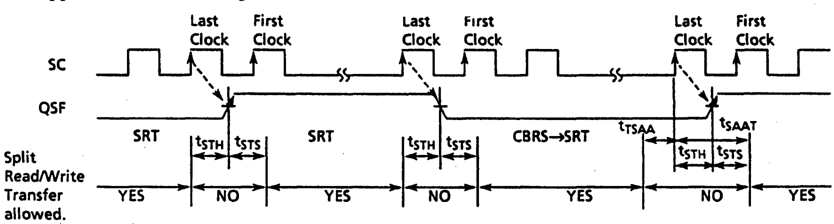
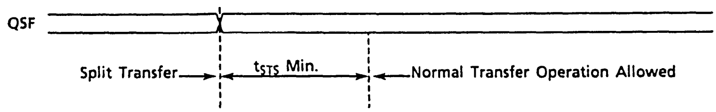


Figure 12. Split Transfer Operation Allowable Periods

The stop register and binary boundary are explained in the CBRS operation and the SAM port operation.

(4) A normal transfer (read/write) may be performed following split transfer operation provided that a t_{STS} minimun delay is satisfied after the QSF signal toggles.



(5) Binary-Boundary SET/RESET Cycle Timing.
When the address counter of serial-access-memory (SAM) pointed as the last address of each boundary address. (15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255, 271, 287, 303, 319, 335, 351, 367, 383, 399, 415, 431, 447, 463, 479, 495, 511), the boundary-set or change by CBRS-cycle or the boundary-reset by CBR-cycle may cause the unexpected operation of SAM counter or QSF status.

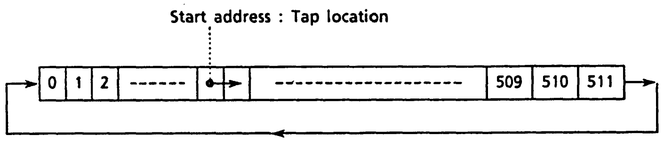
If the system design with these timing is required. Please contact to our local sales office.

SAM PORT OPERATION

The TC528267 is provided with 512 words by 8 bits serial access memory (SAM) which can be operated in the single register mode or the split register mode. High speed serial read or write operations can be performed through the SAM port independent of the RAM port operation.

13. SINGLE REGISTER SERIAL READ OPERATION

Serial data can be read out of the SAM port after a read transfer has been performed. The read transfer operation changes the SAM port to the output mode. At every rising edge of the serial clock, the data is read out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit, as illustrated below. Subsequent real-time read transfer may be performed on-the-fly as many times as desired.



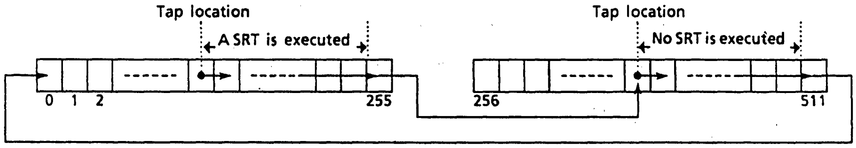
14. SINGLE REGISTER SERIAL WRITE OPERATION

During the serial write operation, the data is written into the SAM at every rising edge of the serial clock. A write transfer cycle, at which all I/Os are usually masked, must be performed to change the SAM port to the input mode. The tap location, which is the start address of the serial write, is set by the column address at the falling edge of $\overline{CAS}$. After the data is filled in the SAM, the serial clock must stop toggling and a write transfer cycle is subsequently used to load the SAM data into the RAM selected by the row address at the falling edge of $\overline{RAS}$. The tap address is set during the same cycle for the next serial write opration.

15. SPLIT REGISTER MODE

The split register mode realizes continuous serial read or write operation. The data can be shifted into or out of one half of the SAM while a split read or write transfer is being performed on the other half of the SAM. Thus, the tight timing control at a real time read operation is eliminated with the split read operation. A normal read / write transfer operation must precede any split read/write transfer operation in order to set the SAM port into output mode or input mode, as the split read or write transfer operations will not change the SAM port mode. Also, a $\overline{CAS}$ before $\overline{RAS}$ refresh and stop register set cycle (CBRS) can be performed to specify the binary boundaries in the SAM.

In the split register mode, serial data can be read from or written into one of the split registers starting from any of the 256 tap locations. The data is read or written sequentially from the tap location to the most significant bit (255 or 511) of the first split SAM and then the SAM pointer moves to the tap location selected for the second split SAM to read or write the data sequentially to the most significant bit (255 or 511) and finally wraps around to the least significant bit, as illustrated in the example below.



16. SPLIT REGISTER MODE WITH BINARY BOUNDARY

After a CBRS cycle is performed, the binary boundary, which is stated in 8.3. $\overline{CAS}$ before $\overline{RAS}$ refresh and stop register set, is set when a SRT cycle is performed. The serial data is read from or written into one half of the SAM starting the tap location to the next binary boundary, while another SRT cycle is performed. Then, the SAM pointer moves to the tap location in the other half SAM and the data is read from or written into the half SAM sequentially. If any SRT operation is not performed before the next boundary, the SAM pointer does not jump to the other half SAM, as illustrated in Figure 12.

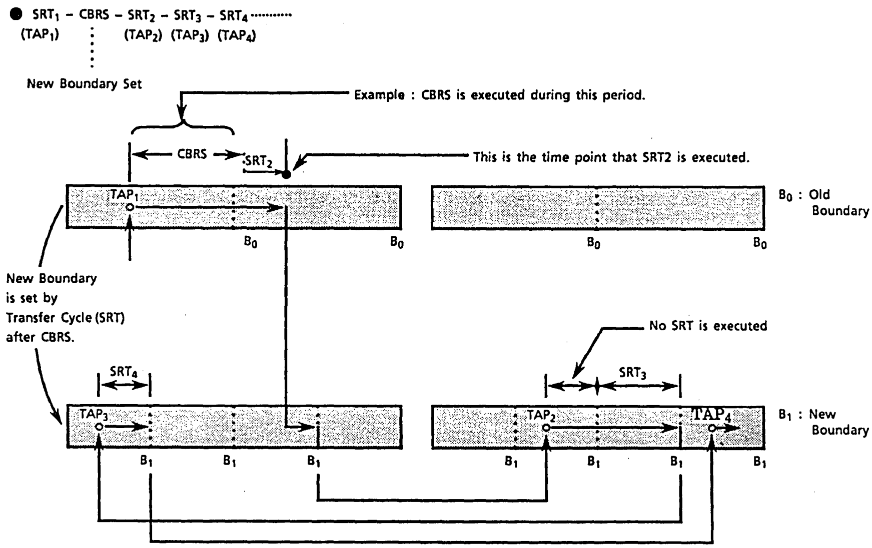


Figure 12. Operation of Split Register Mode with Binary Boundary

The binary boundary is reset by a CBR cycle and the SAM operation mode returns to the normal split register mode, as shown in Figure 13.

Fig. 14 shows the relation between CBR and SC on binary-boundary-reset. When Nth SC clock accesses old binary address is reset and (N + 1)th SC clock accesses old boundary address (old stop address) + 1 on the same split SAM, not jump to TAP address.

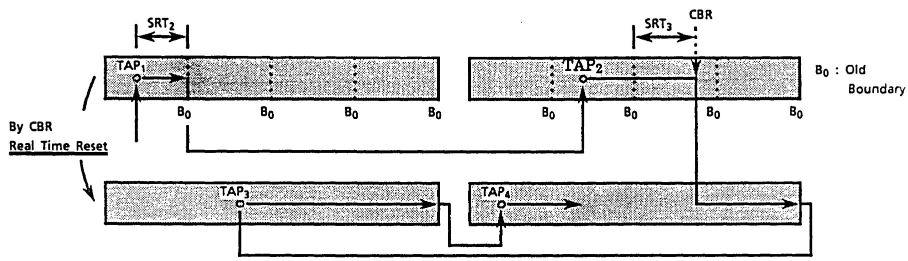


Figure 13. Binary Boundary Reset

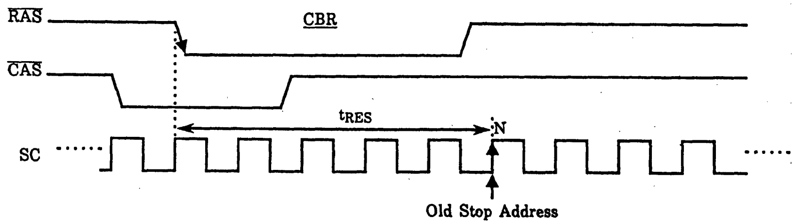


Figure 14. CBR and SC relation of binary-boundary-reset

In an actual system which uses the binary boundary a CBRS cycle is executed to determine a type of the boundary location. Then, a normal RT transfers a row of data into the SAM and set the initial tap location at the same time. An SRT cycle follows it before the SAM pointer reaches to the boundary location. The SRT cycle makes the binary boundary jump effective, as illustrated in Figure 15.

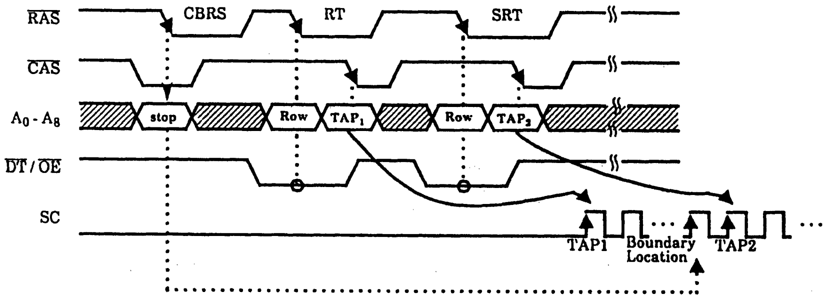


Figure 15. Binary Boundary Jump Set Sequence

There are additional timing specifications, t_{TSAA} and t_{SAAT} to determine the period that does not allow a split transfer, as illustrated in Figure 16.

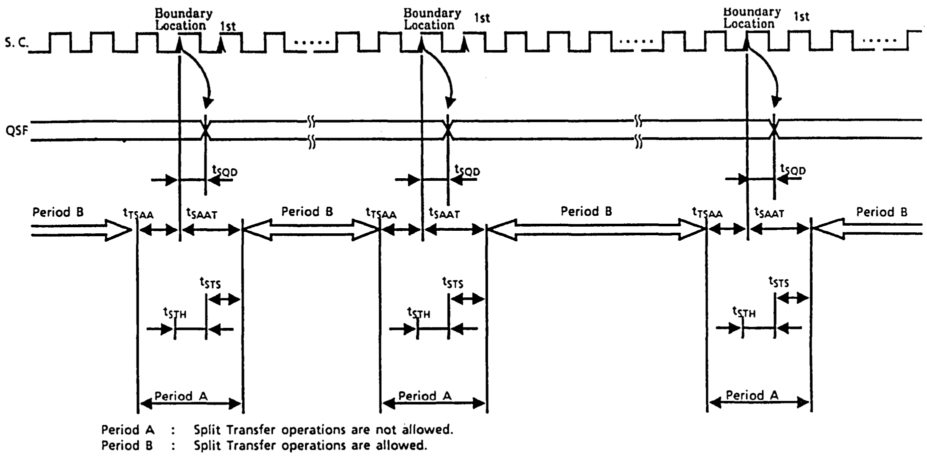


Figure 16. Timing Specification to allow SRT operation

POWER-UP

Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them "high" before or at the same time as the V_{CC} supply is turned on. After power-up, a pause of 200 μseconds minimum is required with $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ held "high". After the pause, a minimum of 8 CBR dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT}/\overline{OE}$ signal must be held "high".

INITIAL STATE AFTER POWER-UP

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and $\overline{WB}/\overline{WE}$ held "high", the internal state of the TC528267 is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 μseconds pause followed by a minimum of 8 CBR cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
QSF	High-Impedance
Color Register	all "0"
Write Mask Register	Write Enable
TAP pointer	Invalid
Stop Register	Default Case

TOSHIBA

TC524162
TC524165

SILICON GATE CMOS
262,144 WORDS x 16 BITS MULTIPORT DRAM

target spec

DESCRIPTION

The TC524162/165 is a 4M bit CMOS multiport memory equipped with a 262,144-words by 16-bits dynamic random access memory (RAM) port and a 512-words by 16-bits static serial access memory (SAM) port. The TC524162/165 supports three types of operations; Random access to and from the RAM port, high speed serial access to and from the SAM port and transfer of data between any selected row in the RAM to the SAM. To realize a high performance graphic frame buffer system the TC524162/165 features various special operations such as the write-per-bit, the pipelined page mode, the block write and flash write function on the RAM port and the read transfer operations from the RAM to the SAM port. In addition, extended fast page mode is available where an output data remains valid during the $\overline{CAS}$ is high (TC524165 only). The TC524162/165 is fabricated using Toshiba's CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

FEATURES

- Single power supply of 5V± 10% with a built-in V_{BB} generator
- All inputs and outputs : TTL Compatible
- Organization
  RAM Port : 262,144wordsX16bits
  SAM Port : 512wordsX16bits
- RAM Port
  Fast Page Mode (TC524160/162), Extended Fast Page Mode (TC524165), Read - Modify - Write, Pipelined Fast Page Mode, $\overline{CAS}$ before $\overline{RAS}$ Auto Refresh, Hidden Refresh, $\overline{RAS}$ only Refresh, Write per Bit (New/Old Mask Mode), Masked Flash Write (New/Old Mask Mode), Block Write, Masked Block Write (New/Old Mask Mode), Load Mask Register/Color Register Cycle, 512 refresh cycles / 8ms
- SAM Port
  Addressable TAP Capability
  Stop Address (Binary Boundary) Capability
  Fully Static Register, Single Register/Split Register Mode Capability
- RAM - SAM Transfer
  Read / Real Time Read Transfer
  Split Read Transfer
- Package
  TC524162/165SF : SSOP64-P-525
  TC524162/165FT: TSOP70-P-400
  TC524162/165TR: TSOP70-P-400A

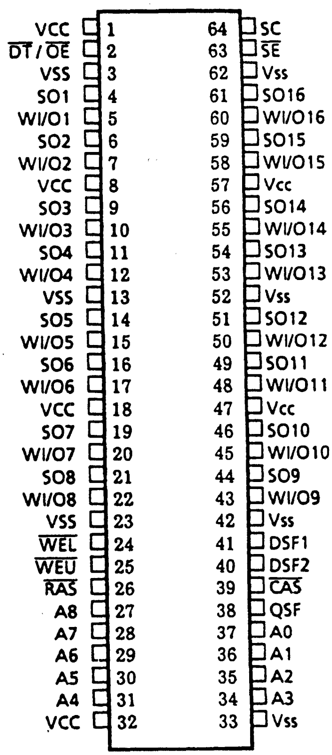
KEY PARAMETERS

ITEM		— 60	— 70
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	15ns	20ns
t_{AA}	Column Address Access Time (Max.)	30ns	35ns
t_{RC}	Cycle Time (Min.)	115ns	130ns
t_{PC}	Page Mode Cycle Time (Min.)	35ns	40ns
t_{SCA}	Serial Access Time (Max.)	15ns	20ns
t_{SCC}	Serial Cycle Time (Min.)	18ns	23ns
t_{RACP}	t_{RAC} in Pipelined Fast Page	85ns	90ns
t_{CACI}	t_{CAC} in Pipelined Fast Page	15ns	20ns
t_{PCP}	Pipelined Fast Page Mode Cycle Time	30ns	30ns
I_{CC1}	RAM Operating Current (SAM : Standby)	110mA	100mA
I_{CC2A}	SAM Operating Current (RAM : Standby)	60mA	60mA
I_{CC2}	Standby Current	10mA	10mA

PIN NAME

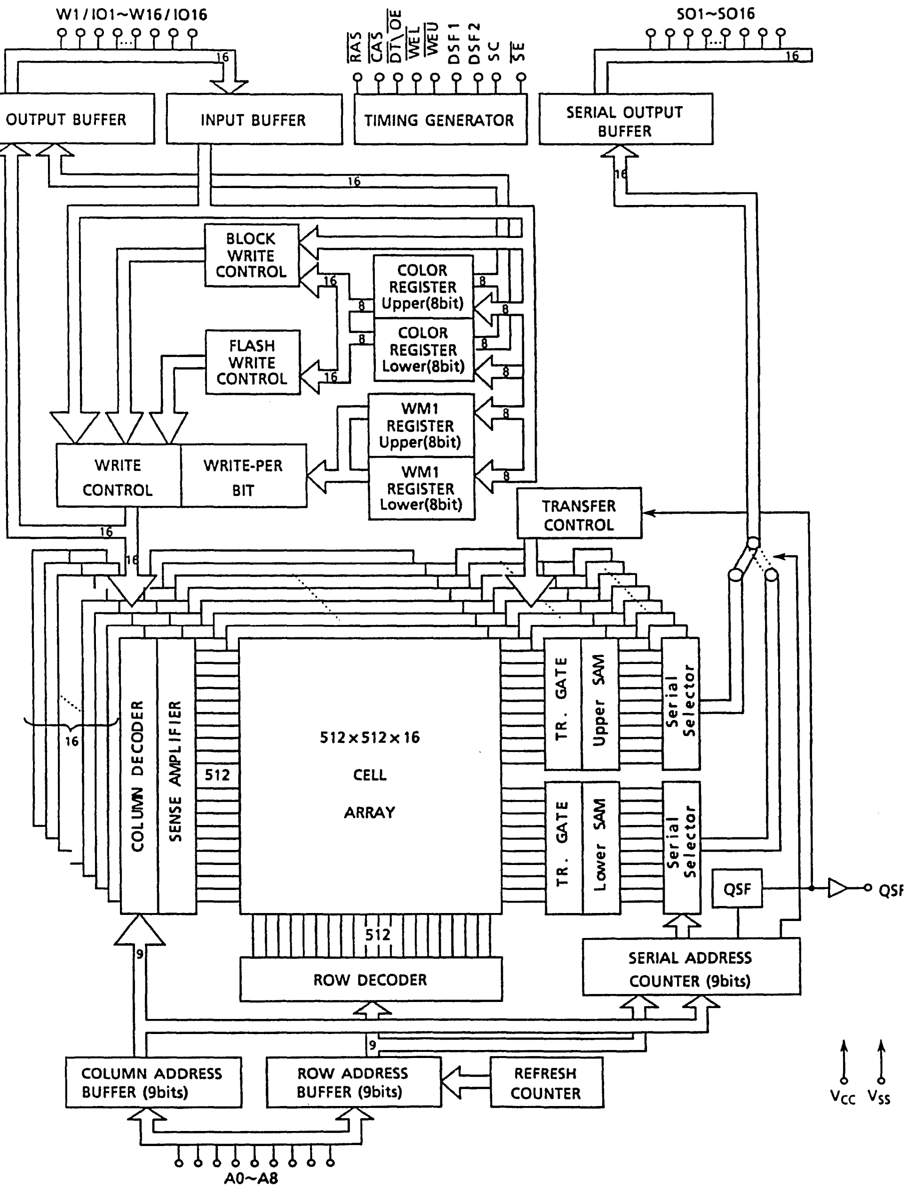
A0~A8	Address inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{DT}}/\overline{\text{OE}}$	Data Transfer/Output Enable
$\overline{\text{WEL}}/\overline{\text{WEU}}$	Write per Bit/Write Enable
DSF1 DSF2	Special Function Control
W1/IO1~W1/IO16	Write Mask/Data IN, OUT
SC	Serial Clock
$\overline{\text{SE}}$	Serial Enable
SO1~SO16	Serial/Output
QSF	Special Flag Output
V_{CC}/V_{SS}	Power(5V)/Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)



525mil TSOP/SSOP (0.8mm pitch)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}, V_{OUT}	Input Output Voltage	— 1.0~7.0	V	1
V_{CC}	Power Supply Voltage	— 1 .0~7.0	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	— 55~150	°C	1
T_{SOLDER}	Soldering Temperature • Time	260•10	°C•sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	Vcc + 0.3	V	2
V_{IL}	Input Low Voltage	- 0.5*	—	0.8	V	2

+: -1V 20ns Pulse width

CAPACITANCE (V_{CC} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance	—	7	pF
C_{IO}	Input/Output Capacitance	—	9	
C_O	Output Capacitance (QSF)	—	9	

Note: This parameter is periodically sampled and is not 100% tested.

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

ITEM (RAM PORT)	SAM PORT	SYMBOL	-60 MIN.	-60 MAX.	-70 MIN.	-70 MAX.	UNIT	NOTE
OPERATING CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ min.)	Standby	I_{CC1}	—	110	—	100	mA	3, 4, 5
	Active	I_{CC1A}	—	160		150		3, 4, 5
STANDBY CURRENT ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	Standby	I_{CC2}	—	10	—	10		
	Active	I_{CC2A}	—	60	—	60		
$\overline{RAS}$ ONLY REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} $t_{RC} = t_{RC}$ min.)	Standby	I_{CC3}	—	110	—	100		3
	Active	I_{CC3A}	—	160	—	150		3
PAGE MODE CURRENT ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling $t_{PC} = t_{PC}$ min.)	Standby	I_{CC4}	—	100	—	90		3, 4, 5
	Active	I_{CC4A}	—	150	—	140		3, 4, 5
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$ $t_{RC} = t_{RC}$ min.)	Standby	I_{CC5}	—	110	—	100		3
	Active	I_{CC5A}	—	160	—	150		3
DATA TRANSFER CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ min.)	Standby	I_{CC6}	—	130	—	120		3, 4, 5
	Active	I_{CC6A}	—	180	—	170		3, 4, 5
FLASH WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ min.)	Standby	I_{CC7}	—	110	—	100		3, 4, 5
	Active	I_{CC7A}	—	160	—	150		3, 4, 5
BLOCK WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ min.)	Standby	I_{CC8}	—	120	—	110		3, 4, 5
	Active	I_{CC8A}	—	170	—	160		3, 4, 5

ITEM	SYMBOL	MIN.	MAX	UNIT	NOTE
INPUT LEAKAGE CURRENT 0V ≤ V_{IN} ≤ 6.5V, All other pins not under test = 0V	$I_{I(L)}$	—10	10	μA	
OUTPUT LEAKAGE CURRENT 0V ≤ V_{OUT} ≤ 5.5V, Output Disable	$I_{O(L)}$	—10	10	μA	
OUTPUT "H" LEVEL VOLTAGE I_{OUT} = (- 1mA	V_{OH}	2.4	—	V	
OUTPUT "L" LEVEL VOLTAGE I_{OUT} = (2.1mA	V_{OL}	—	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes: 6, 7, 8)

SYMBOL	PARAMETER	-60		-70		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	115		130			
t_{RMW}	Read-Modify-Write Cycle Time	140		180			
t_{PC}	Fast Page Mode Cycle Time	35		40			
t_{PRMW}	Fast Page Mode Read-Modify-Write CycleTime	85		85			
t_{RAC}	Access Time from $\overline{RAS}$		60		70		13
t_{AA}	Access Time from Column Address		30		35		13
t_{CAC}	Access Time from $\overline{CAS}$		15		20		14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		30		35		14
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0		0			
t_{OFF}	Output Buffer Turn-Off Delay	0	15	0	15		9, 15
t_{T}	Transition Time (Rise and Fall)	3	50	3	50		8
t_{RP}	$\overline{RAS}$ Precharge Time	45		50			
t_{RAS}	$\overline{RAS}$ Pulse Width	60	100000	70	100000		
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode Only)	60	100000	70	100000		
t_{RSH}	$\overline{RAS}$ Hold Time	20		20			
t_{CSH}	$\overline{CAS}$ Hold Time	60		70			
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10000	20	10000		
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50		13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35		13
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35			
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10			
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10			
t_{ASR}	Row Address Set-Up Time	0		0			
t_{RAH}	Row Address Hold Time	10		10			
t_{ASC}	Column Address Set-Up Time	0		0			
t_{CAH}	Column Address Hold Time	10		10			
t_{RCS}	Read Command Set-Up Time	0		0			
t_{RCH}	Read Command Hold Time	0		0			10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0			10
t_{WCH}	Write Command Hold Time	10		10			
t_{WP}	Write Command Pulse Width	10		10			
t_{WPZ}	Write Command Pulse Width	10		10			9
t_{WEZ}	Write Command Output Buffer Turn-Off Delay		10		15		9
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20			
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20			
t_{DS}	Data Set-Up Time	0		0			11
t_{DH}	Data Hold Time	10		10			11
t_{WCS}	Write Command Set-Up Time	0		0			12
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	80		90			12
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	50		55			12
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	40		40			12

SYMBOL	PARAMETER	-60		-70		UNIT	NOTE
		MIN.	MAX	MIN.	MAX.		
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0			
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0			
t_{OEA}	Access Time from $\overline{OE}$		15		20		
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$		15		15		9
t_{OED}	$\overline{OE}$ to Data Delay Time	10		10			
t_{OEH}	$\overline{OE}$ Command Hold Time	10		10		ns	
t_{ODS}	Output Disable Set up time	0		0			
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15		15			
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	5		5			
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	15		15			
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0			
t_{REF}	Refresh Period		8		8	ms	
t_{WSR}	$\overline{WB}$ Set-Up Time	0		0			
t_{RWH}	$\overline{WB}$ Hold Time	10		10			
t_{FSR}	DSF Set-Up Time referenced to $\overline{RAS}$	0		0			
t_{RFH}	DSF Hold Time referenced to $\overline{RAS}$ (1)	10		10			
t_{FSC}	DSF Set-Up Time referenced to $\overline{CAS}$	0		0			
t_{CFH}	DSF Hold Time referenced to $\overline{CAS}$	10		10			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0		0			
t_{MH}	Write-Per-Bit Mask Data Hold Time	10		10			
t_{THS}	$\overline{DT}$ High Set-Up Time	0		0			
t_{THH}	$\overline{DT}$ High Hold Time	10		10			
t_{TLS}	$\overline{DT}$ Low Set-Up Time	0		0			
t_{TLH}	$\overline{DT}$ Low Hold Time	10	10000	10	10000		
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	55	10000	60	10000		
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	25		25		ns	
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	20		20			
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	45		50			
t_{TP}	$\overline{DT}$ Precharge Time	10		15			
t_{RSD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	60		70			
t_{ASD}	Column Address to First SC Delay Time (Read Transfer)	30		35			
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	20		20			
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		5			
t_{TSD}	$\overline{DT}$ to FIrst SC Delay Time (Read Transfer)	10		10			
t_{SRS}	Last SC to $\overline{RAS}$ Set-Up Time (Serial Input)	18		23			
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	15		20			
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	40		45			
t_{SCC}	SC Cycle Time	18		23			

SYMBOL	PARAMETER	-60		-70		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{SC}	SC Pulse Width (SC High Time)	5		10			
t_{SCP}	SC Precharge Time (SC Low Time)	5		5			
t_{SCA}	Access Time from SC		15		20		
t_{SOH}	Serial Output Hold Time from SC	5		5			
t_{SDS}	Serial Input Set-Up Time	0		0			
t_{SDH}	Serial Input Hold Time	10		10			
t_{SEA}	Access Time from $\overline{SE}$		15		20		
t_{SE}	$\overline{SE}$ Pulse Width	10		20			
t_{SEP}	$\overline{SE}$ Precharge Time	10		20			
t_{SEZ}	Serial Output Buffer Turn-off Delay from$\overline{SE}$		15		15		9
t_{SZE}	Serial Input to $\overline{SE}$ Delay Time	0		0			
t_{SZS}	Serial Input to First SC Delay Time	0		0			
t_{SWS}	Serial Write Enable Set-Up Time	0		0			
t_{SWH}	Serial Write Enable Hold Time	10		10			
t_{SWIS}	Serial Write Disable Set-Up Time	0		0			
t_{SWIH}	Serial Write Disable Hold Time	10		10			
t_{STS}	Split Transfer Set-Up Time	18		23			
t_{STH}	Split Transfer Hold Time	18		23			
t_{SQD}	SC-QSF Delay Time		15		20		
t_{TQD}	$\overline{DT}$-QSF Delay Time		15		20		
t_{CQD}	$\overline{CAS}$-QSF Delay Time		15		20	ns	
t_{RQD}	$\overline{RAS}$-QSF Delay Time		60		70		
t_{RCDP}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time (Pipeline mode)	20	35	20	40		
t_{CSHP}	$\overline{CAS}$ Hold Time (Pipeline mode)	45		50			
t_{RACP}	Access TIme from $\overline{RAS}$ (Pipeline mode)		85		90		
t_{CAC1}	Access Time from $\overline{CAS}$ (1) (Pipeline mode)		15		20		
t_{CAC2}	Access Time From $\overline{CAS}$ (2) (Pipeline mode)		50		50		
t_{CASP}	$\overline{CAS}$ Pulse Width (Pipeline mode)	10		10			
t_{CPP}	$\overline{CAS}$ Precharge Time Pipeline mode)	10		10			
t_{PCP}	Fast Page Mode Cycle Time (Pipeline mode)	30		30			
t_{COH}	$\overline{CAS}$ Hold Time referenced to $\overline{OE}$ (Pipeline mode)	5		5			
t_{RSH1}	$\overline{RAS}$ Hold Time (1) (Pipeline mode)	20		20			
t_{RSH2}	$\overline{RAS}$ Hold Time (2) (Pipeline mode)	50		50			
t_{CWLP}	Write Command to $\overline{CAS}$ lead Time (Pipeline mode)	10		10			
t_{CWP}	$\overline{WE}$ to $\overline{CAS}$ Delay Time (Pipeline mode)	30		30			
t_{OFFP}	Outoff Buffer Turn-off Delay from $\overline{RAS}$ (Pipeline mode)	0	15	0	15		9, 15
t_{OEP}	$\overline{OE}$ High width	10		10			16
t_{ECS}	$\overline{CAS}$ High to $\overline{OE}$ Low (Fast Page mode)	10		10			16
t_{ECH}	$\overline{OE}$ High to $\overline{CAS}$ Low (Fast Page mode)	10		10			16
t_{TSAA}	Boundary TAP SC Set-up time	0		0			
t_{SATT}	SRT inhibit after Boundary SC	36		46			

A.C. MEASUREMENT CONDITION

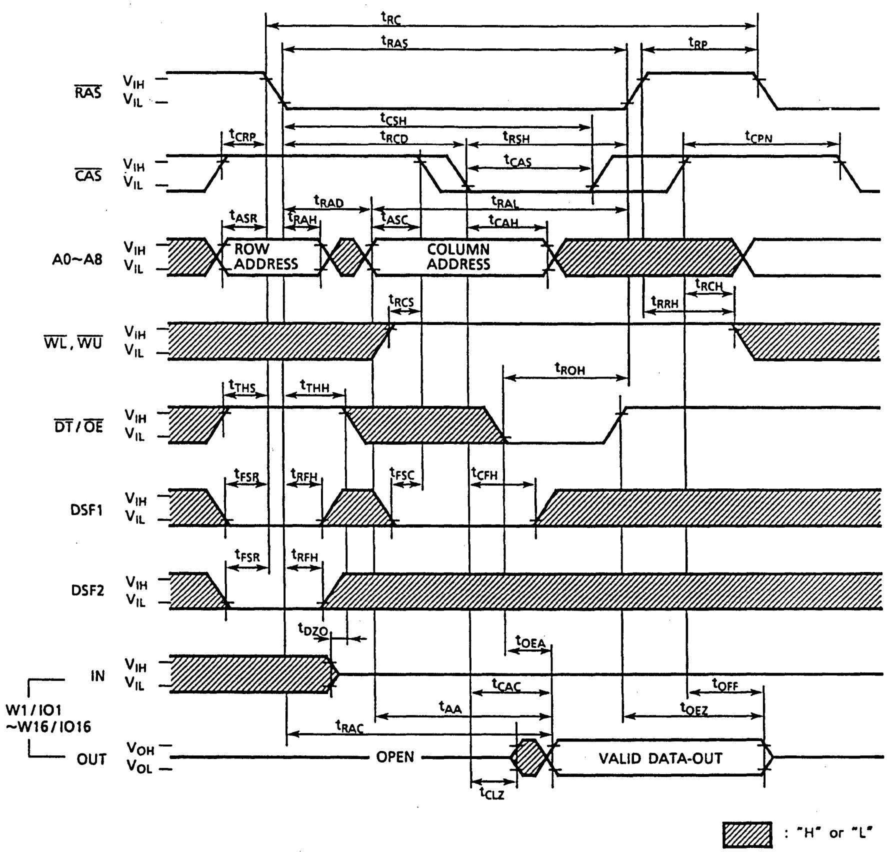
RAM Output Reference Level	2.0V/0.8V
SAM Output Reference Level	2.0V/0.8V
RAM Output Load	1TTL and 50PF
SAM Output Load	1TTL and 50PF
Input Reference Level	2.2V/1.0V

NOTES:

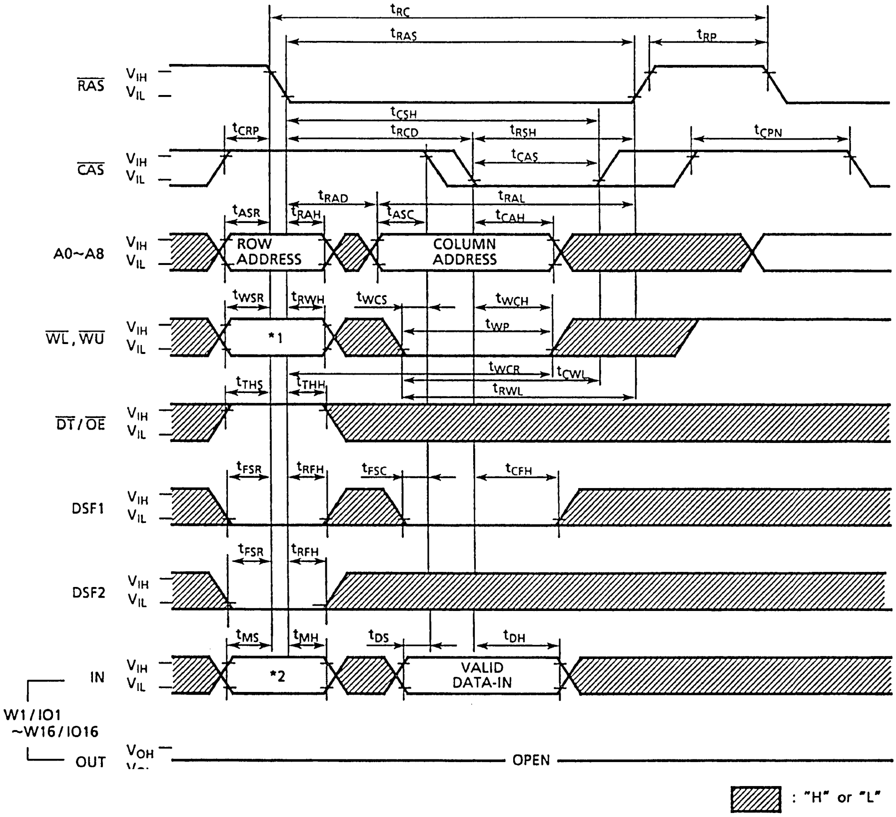
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. These parameters depend on cycle rate.
4. These parameters depend on output loading. Specified values are obtained with the output open. (I out=ØmA)
5. Address can be changed once or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).
6. An initial pause of 200µs is required after power-up followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}/\overline{OE}$ "high") and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume t_T = 5ns. (Between $V_{IH\ (min)}$ and $V_{IL\ (max)}$)
8. $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. $t_{OFF\ (max.)}$, $t_{OEZ\ (max.)}$, $t_{OFFP\ (max.)}$,$t_{WPZ\ (max.)}$, $t_{WEZ\ (max.)}$, and $t_{SEZ\ (max.)}$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
11. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WEU}$ / $\overline{WEL}$ leading edge in $\overline{OE}$-controlled write cycle and read-modify-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS\ (min.)}$, the cycle is an early write cycles and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geq t_{RWD\ (min.)}$, $t_{CWD} \geq t_{CWD\ (min.)}$ and $t_{AWD} \geq t_{AWD\ (min.)}$ the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the $t_{RCD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can be met.
$t_{RCD\ (max.)}$ is specified as a reference point only : If t_{RCD} is greater than the specified
$t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.
14. Operation within the $t_{RAD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.
15. t_{OFF}, t_{OFFP} timing is specified from either $\overline{RAS}$ or $\overline{CAS}$ rising edge, whichever occurs last.
16. TC524165 only

TIMING WAVEFORM

READ CYCLE



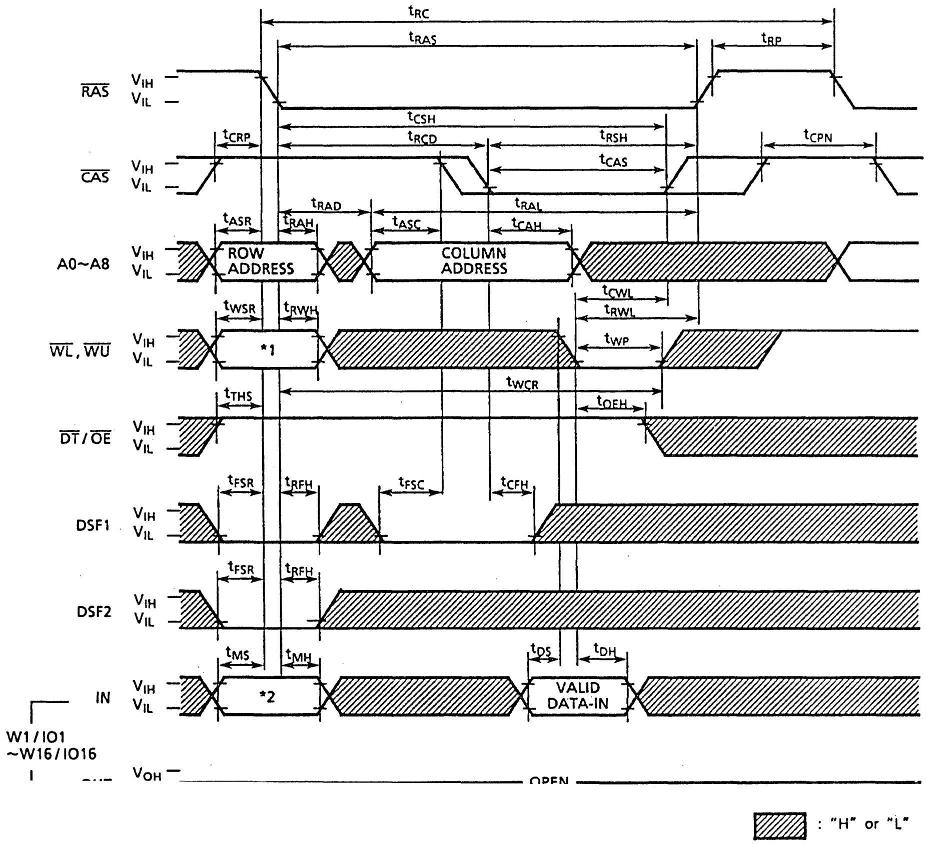
WRITE CYCLE (EARLY WRITE) *Note 1, 3



Mask Mode	*1		*2	Cycle
	WL	WU		
No Mask Mode	1	1	Don't care	Normal Write
New Mask Mode	0 0 1	0 1 0	WM1 data	Write per Bit
Old Mask Mode	0 0 1	0 1 0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable
Don't care : '1' or '0'

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE) *Note 2, 3

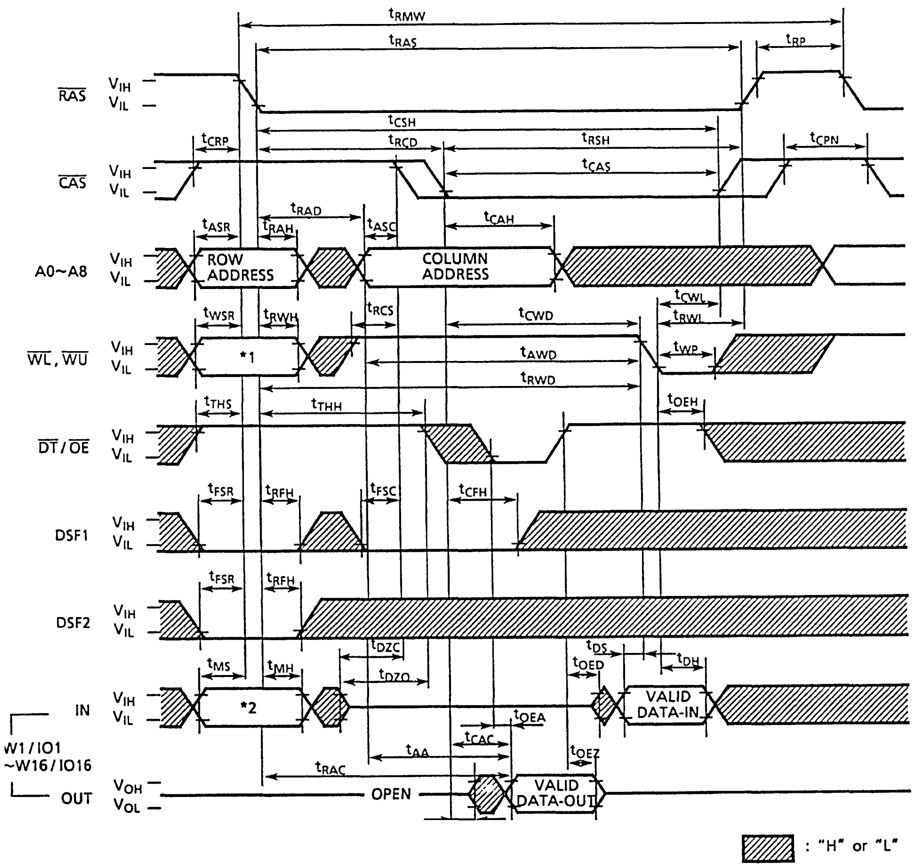


Mask Mode	*1		*2	Cycle
	$\overline{WL}$	$\overline{WU}$		
No Mask Mode	1	1	Don't care	Normal Write
New Mask Mode	0 0 1	0 1 0	WM1 data	Write per Bit
Old Mask Mode	0 0 1	0 1 0	Don't care	Write per Bit

WM1 data — 0: Write Disable
1: Write Enable

Don't care — : '1' or '0'

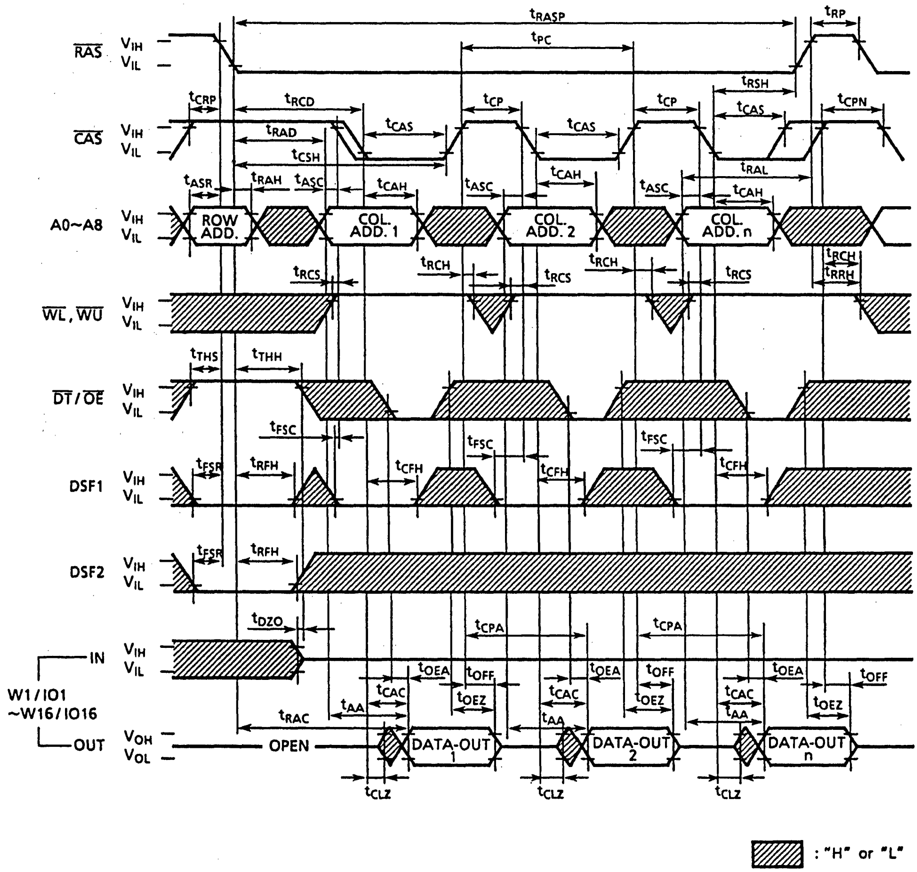
READE-MODIFY-WRITE CYCLE *Note 1, 2, 3



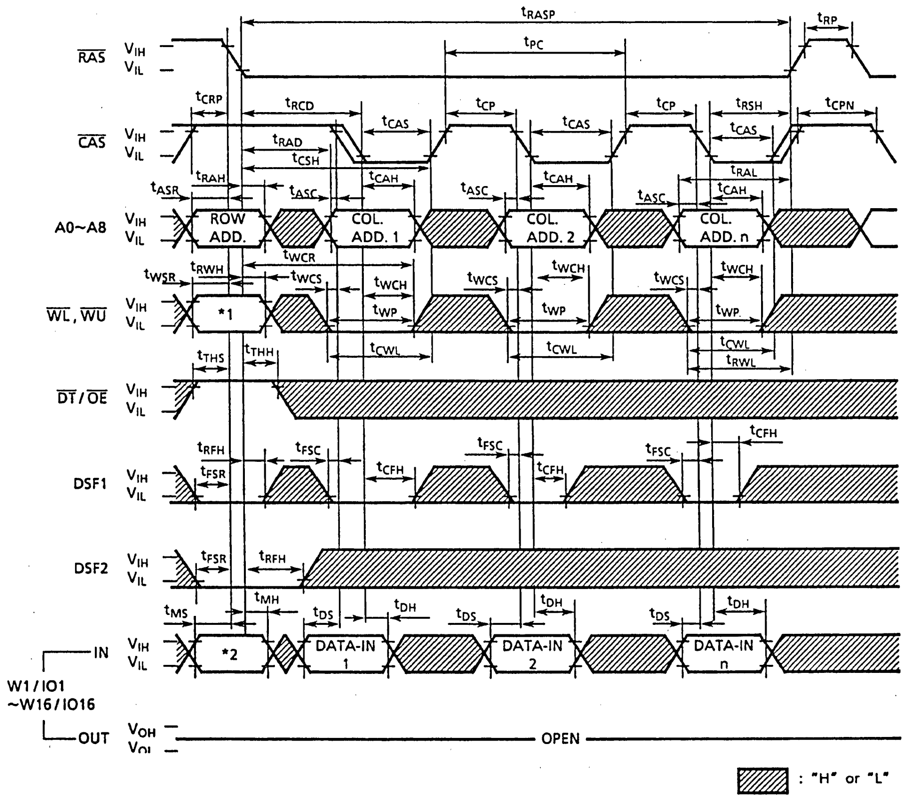
Mask Mode	*1		*2	Cycle
	$\overline{WL}$	$\overline{WU}$		
No Mask Mode	1	1	Don't care	Normal Write
New Mask Mode	0 0 1	0 1 0	WM1 data	Write per Bit
Old Mask Mode	0 0 1	0 1 0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable
Don't care : '1' or '0'

FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE) *Note 1, 2

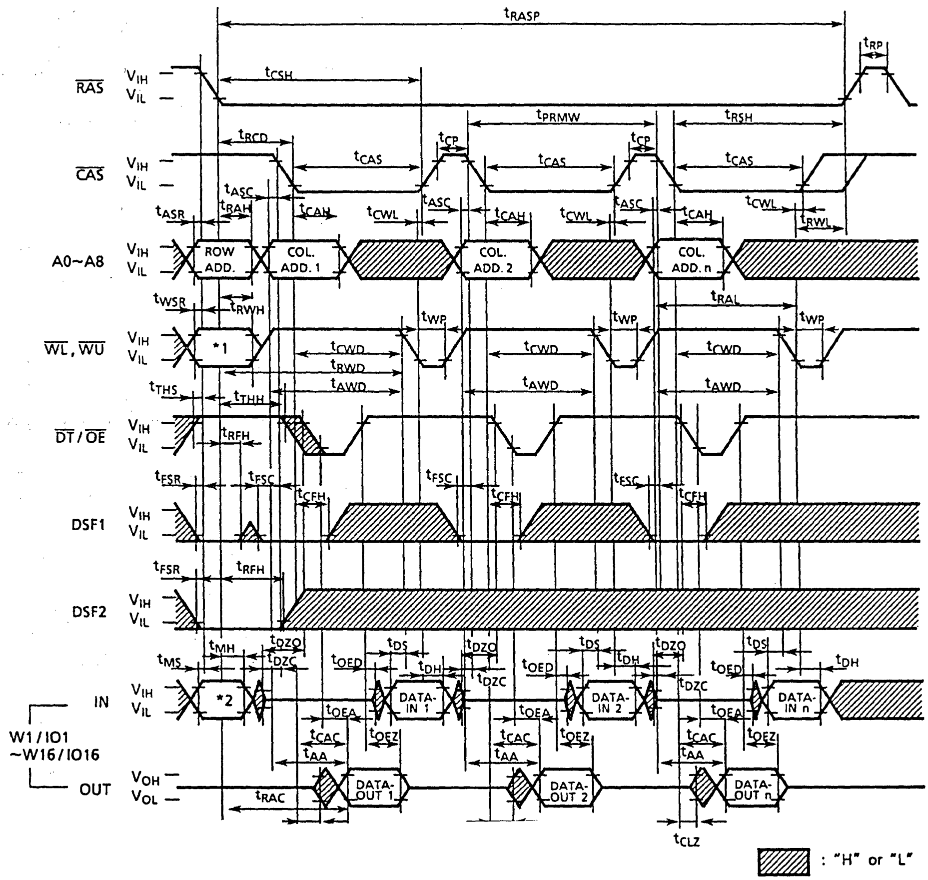


Mask Mode	*1		*2	Cycle
	WL	WU		
No Mask Mode	1	1	Don't care	Normal Write
New Mask Mode	0 0 1	0 1 0	WM1 data	Write per Bit
Old Mask Mode	0 0 1	0 1 0	Don't care	Write per Bit

WM1 data — 0: Write Disable; 1: Write Enable

Don't care — : '1' or '0'

FAST PAGE MODE READ-MODIFY-WRITE CYCLE *Note 2, 3

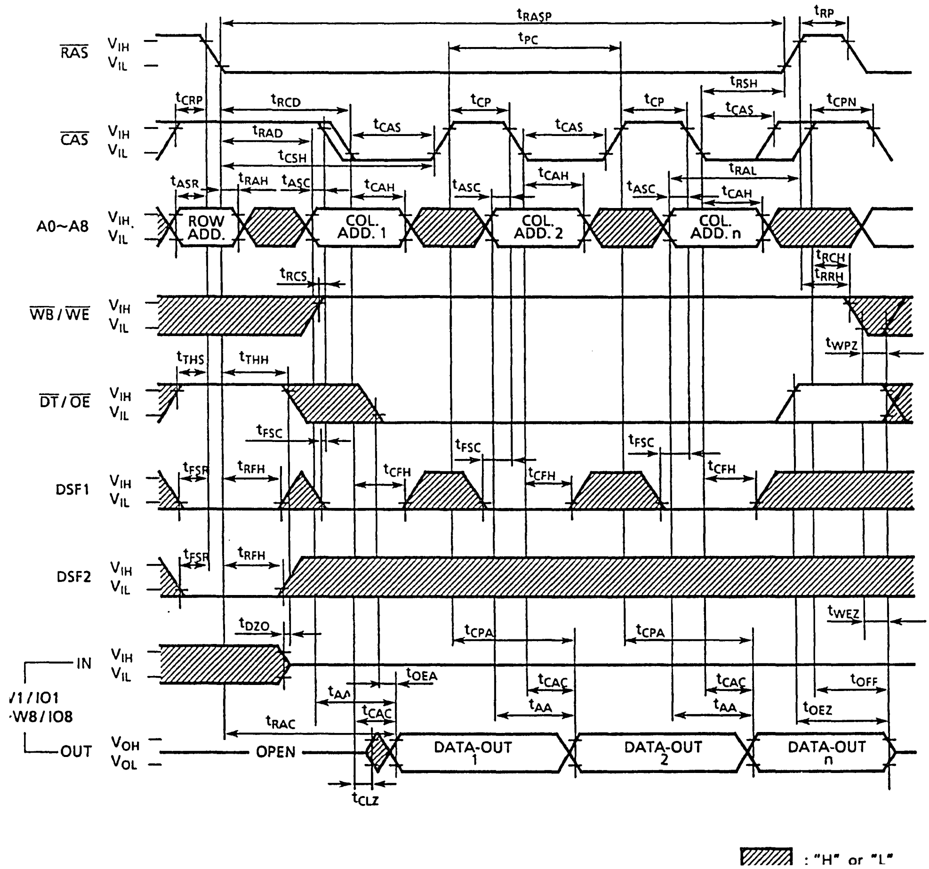


Mask Mode	*1		*2	Cycle
	WL	WU		
No Mask Mode	1	1	Don't care	Normal Write
New Mask Mode	0 0 1	0 1 0	WM1 data	Write per Bit
Old Mask Mode	0 0 1	0 1 0	Don't care	Write per Bit

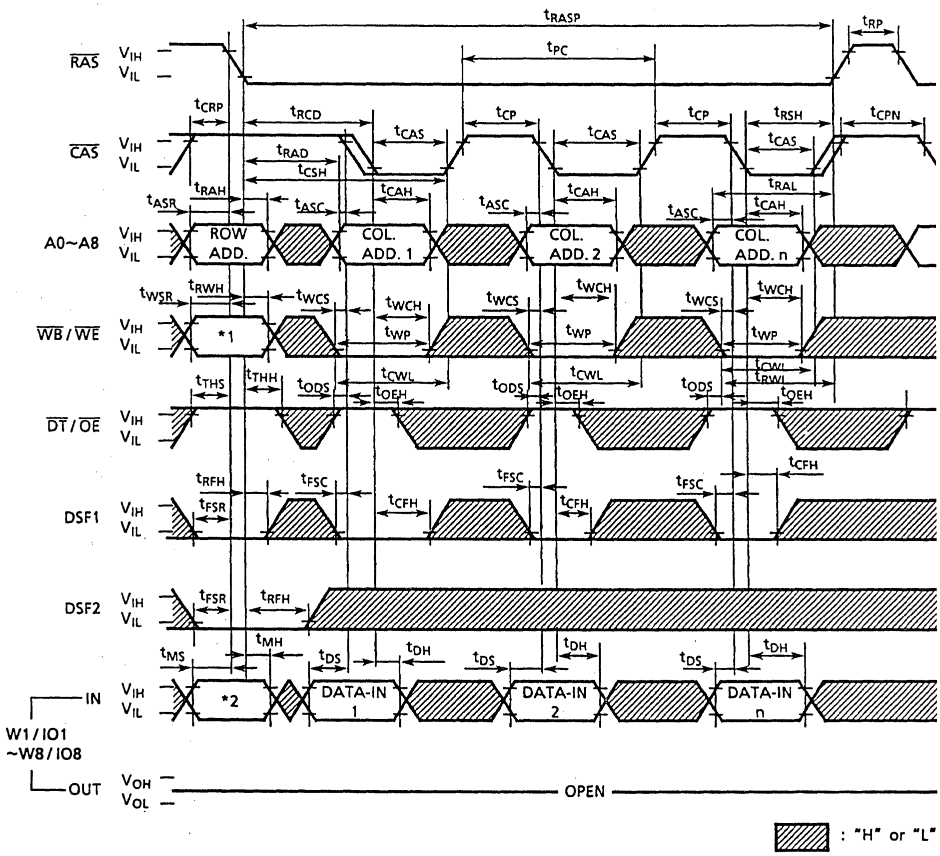
WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

EXTENDED FAST PAGE MODE READ CYCLE (TC524165 only)



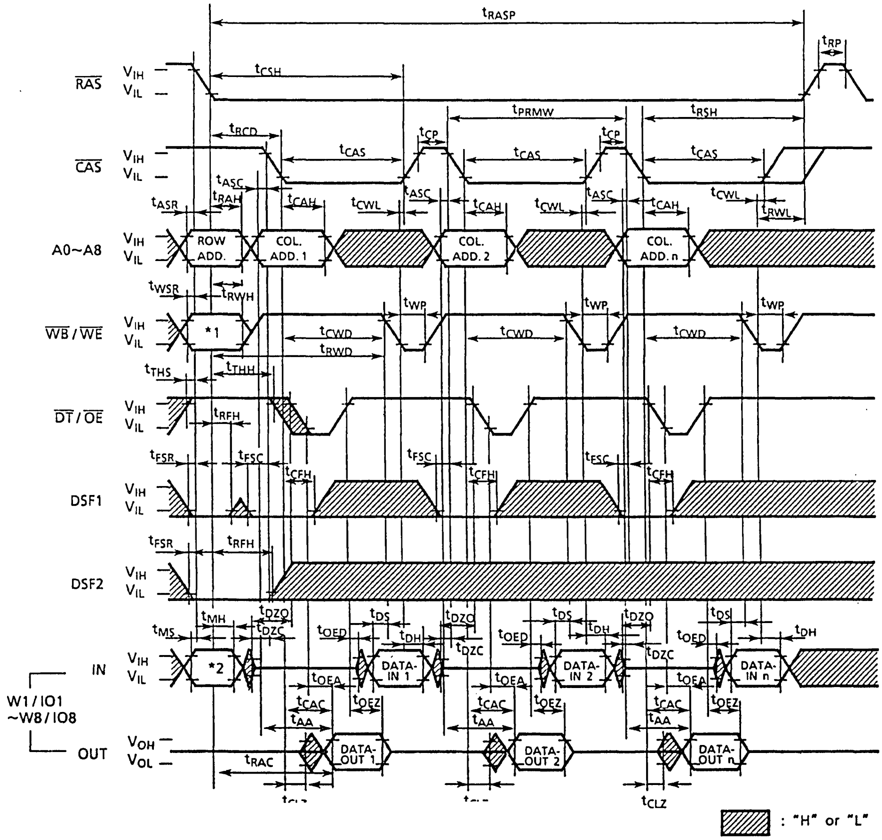
EXTENDED FAST PAGE MODE WRITE CYCLE (EARLY WRITE) (TC524165 only)



Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable
Don't care : '1' or '0'

EXTENDED FAST PAGE MODE READ-MODIFY-WRITE CYCLE (TC524165 only))

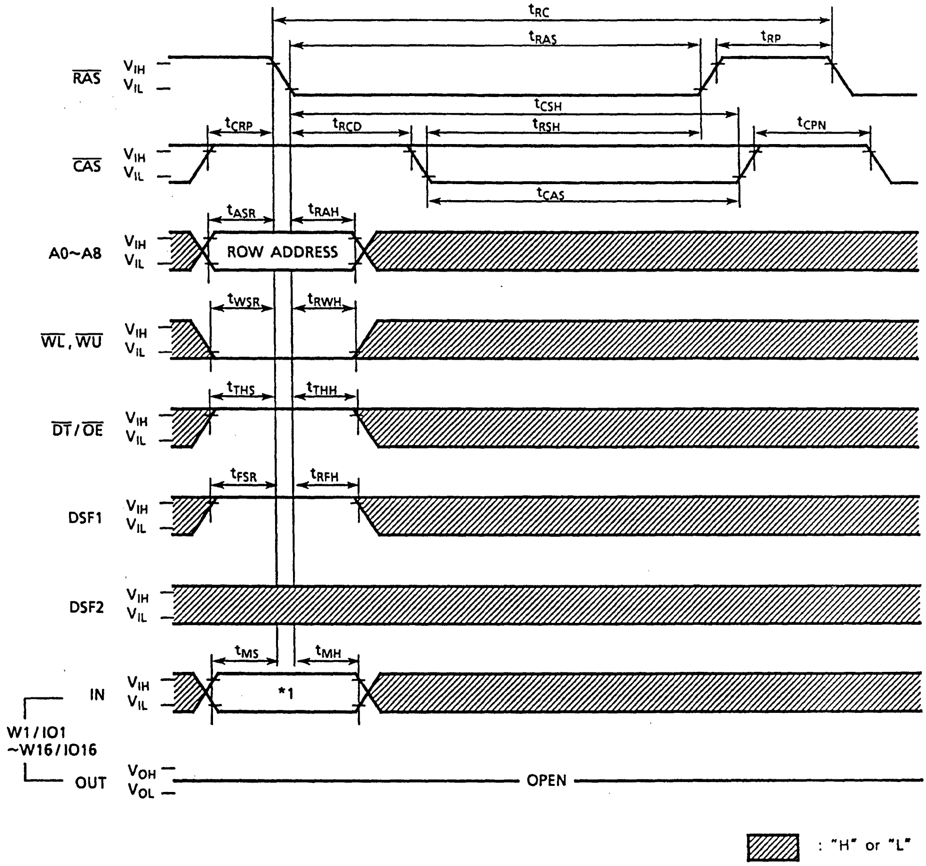


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

FLASH WRITE CYCLE

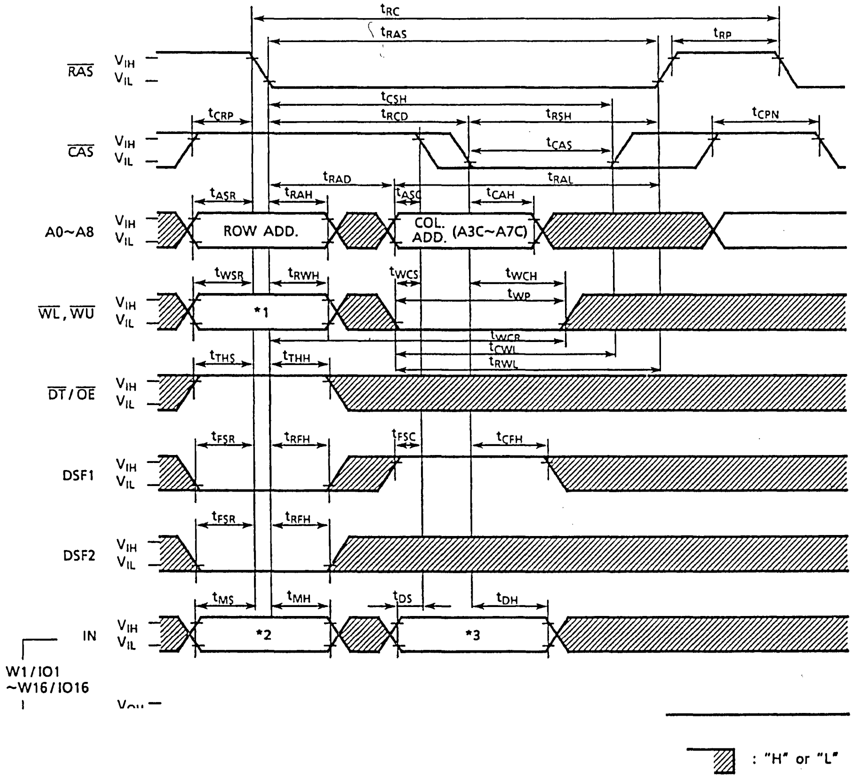


Mask Mode	*1
New Mask Mode	WM1 data
Old Mask Mode	Don't care

WM1 data 0: Write Disable
1: Write Enable

Don't care : '0' or '1'

BLOCK WRITE CYCLE (EARLY WRITE) *Note 1, 3



Mask Mode	*1		*2
	WL	WU	
No Mask Mode	1	1	Don't care
New Mask Mode	0 0 1	0 1 0	WM1 data
Old Mask Mode	0 0 1	0 1 0	Don't care

WM1 data 0: Write Disable
1: Write Enable

Don't care : '0' or '1'

*3 COLUMN SELECT

Lower Byte

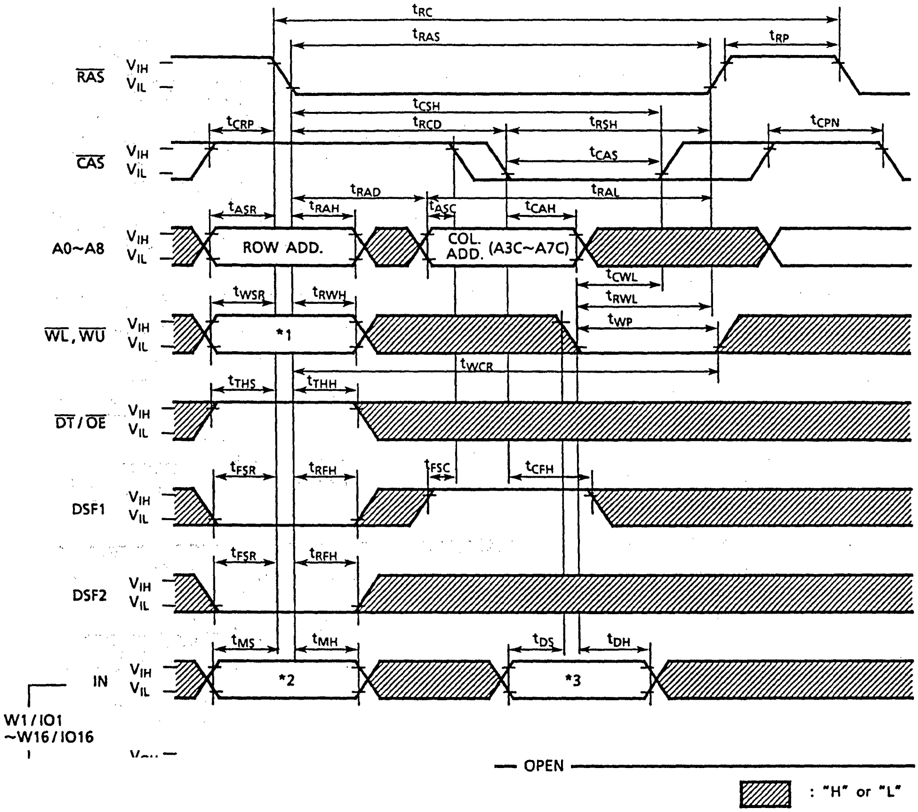
- W1/IO1 - Column 0 (A2C=0, A1C=0, A0C=0)
- W2/IO2 - Column 1 (A2C=0, A1C=0, A0C=1)
- W3/IO3 - Column 2 (A2C=0, A1C=1, A0C=0)
- W4/IO4 - Column 3 (A2C=0, A1C=1, A0C=1)
- W5/IO5 - Column 4 (A2C=1, A1C=0, A0C=0)
- W6/IO6 - Column 5 (A2C=1, A1C=0, A0C=1)
- W7/IO7 - Column 6 (A2C=1, A1C=1, A0C=0)
- W8/IO8 - Column 7 (A2C=1, A1C=1, A0C=1)

Upper Byte

- W9/IO9 - Column 0 (A2C=0, A1C=0, A0C=0)
- W10/IO10 - Column 1 (A2C=0, A1C=0, A0C=1)
- W11/IO11 - Column 2 (A2C=0, A1C=1, A0C=0)
- W12/IO12 - Column 3 (A2C=0, A1C=1, A0C=1)
- W13/IO13 - Column 4 (A2C=1, A1C=0, A0C=0)
- W14/IO14 - Column 5 (A2C=1, A1C=0, A0C=1)
- W15/IO15 - Column 6 (A2C=1, A1C=1, A0C=0)
- W16/IO16 - Column 7 (A2C=1, A1C=1, A0C=1)

Wn/IOn
=0 : Disable
=1 : Enable

BLOCK WRITE CYCLE (DELAYED WRITE) *Note 2, 3



Mask Mode	*1		*2
	$\overline{WL}$	$\overline{WU}$	
No Mask Mode	1	1	Don't care
New Mask Mode	0 0 1	0 1 0	WM1 data
Old Mask Mode	0 0 1	0 1 0	Don't care

WM1 data 0: Write Disable
1: Write Enable

Don't care : '0' or '1'

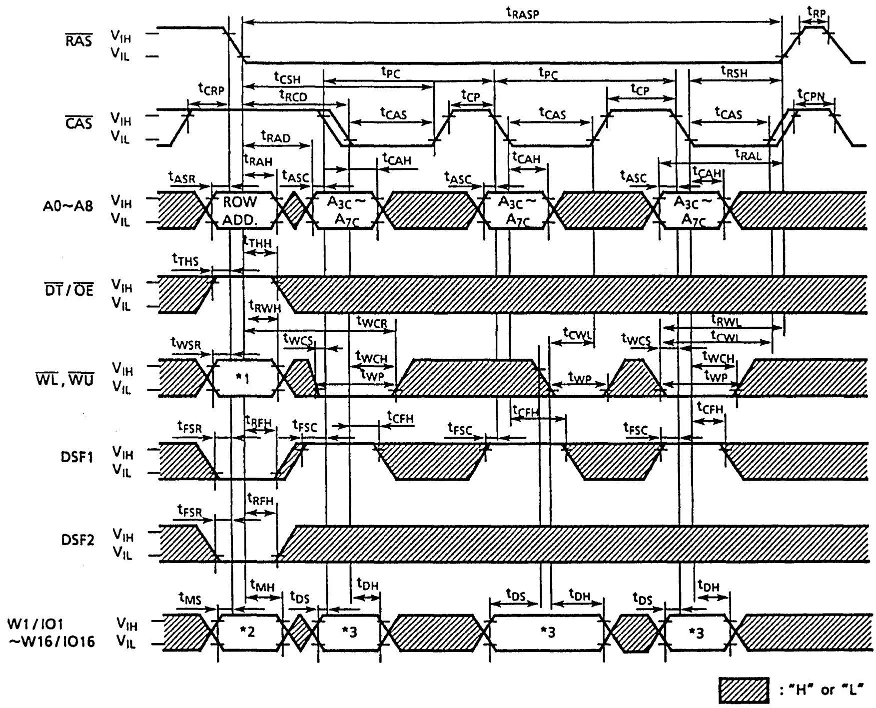
*3 COLUMN SELECT

Lower Byte
- W1/IO1 - Column 0 (A2C=0, A1C=0, A0C=0)
- W2/IO2 - Column 1 (A2C=0, A1C=0, A0C=1)
- W3/IO3 - Column 2 (A2C=0, A1C=1, A0C=0)
- W4/IO4 - Column 3 (A2C=0, A1C=1, A0C=1)
- W5/IO5 - Column 4 (A2C=1, A1C=0, A0C=0)
- W6/IO6 - Column 5 (A2C=1, A1C=0, A0C=1)
- W7/IO7 - Column 6 (A2C=1, A1C=1, A0C=0)
- W8/IO8 - Column 7 (A2C=1, A1C=1, A0C=1)

Upper Byte
- W9/IO9 - Column 0 (A2C=0, A1C=0, A0C=0)
- W10/IO10 - Column 1 (A2C=0, A1C=0, A0C=1)
- W11/IO11 - Column 2 (A2C=0, A1C=1, A0C=0)
- W12/IO12 - Column 3 (A2C=0, A1C=1, A0C=1)
- W13/IO13 - Column 4 (A2C=1, A1C=0, A0C=0)
- W14/IO14 - Column 5 (A2C=1, A1C=0, A0C=1)
- W15/IO15 - Column 6 (A2C=1, A1C=1, A0C=0)
- W16/IO16 - Column 7 (A2C=1, A1C=1, A0C=1)

Wn/IOn
=0 : Disable
=1 : Enable

FAST PAGE MODE BLOCK WRITE CYCLE *Note 1, 2, 3



Mask Mode	*1		*2
	WL	WU	
No Mask Mode	1	1	Don't care
New Mask Mode	0 0 1	0 1 0	WM1 data
Old Mask Mode	0 0 1	0 1 0	Don't care

WM1 data 0: Write Disable
1: Write Enable

Don't care : '0' or '1'

*3 COLUMN SELECT

Lower Byte

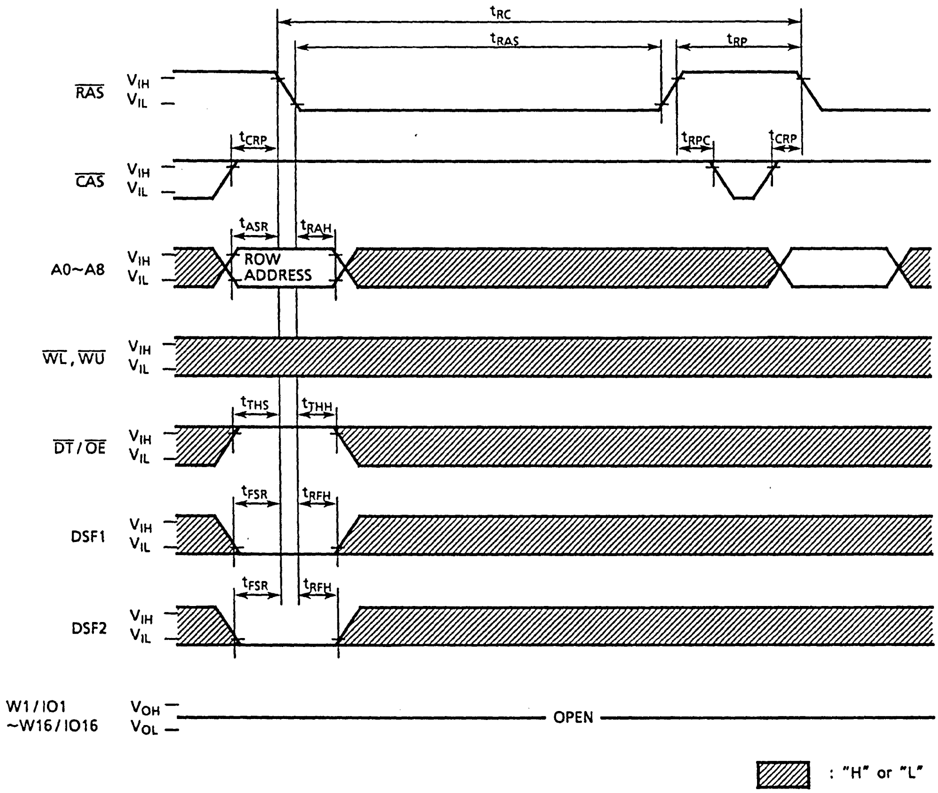
- W1/IO1 - Column 0 (A2C=0, A1C=0, A0C=0)
- W2/IO2 - Column 1 (A2C=0, A1C=0, A0C=1)
- W3/IO3 - Column 2 (A2C=0, A1C=1, A0C=0)
- W4/IO4 - Column 3 (A2C=0, A1C=1, A0C=1)
- W5/IO5 - Column 4 (A2C=1, A1C=0, A0C=0)
- W6/IO6 - Column 5 (A2C=1, A1C=0, A0C=1)
- W7/IO7 - Column 6 (A2C=1, A1C=1, A0C=0)
- W8/IO8 - Column 7 (A2C=1, A1C=1, A0C=1)

Upper Byte

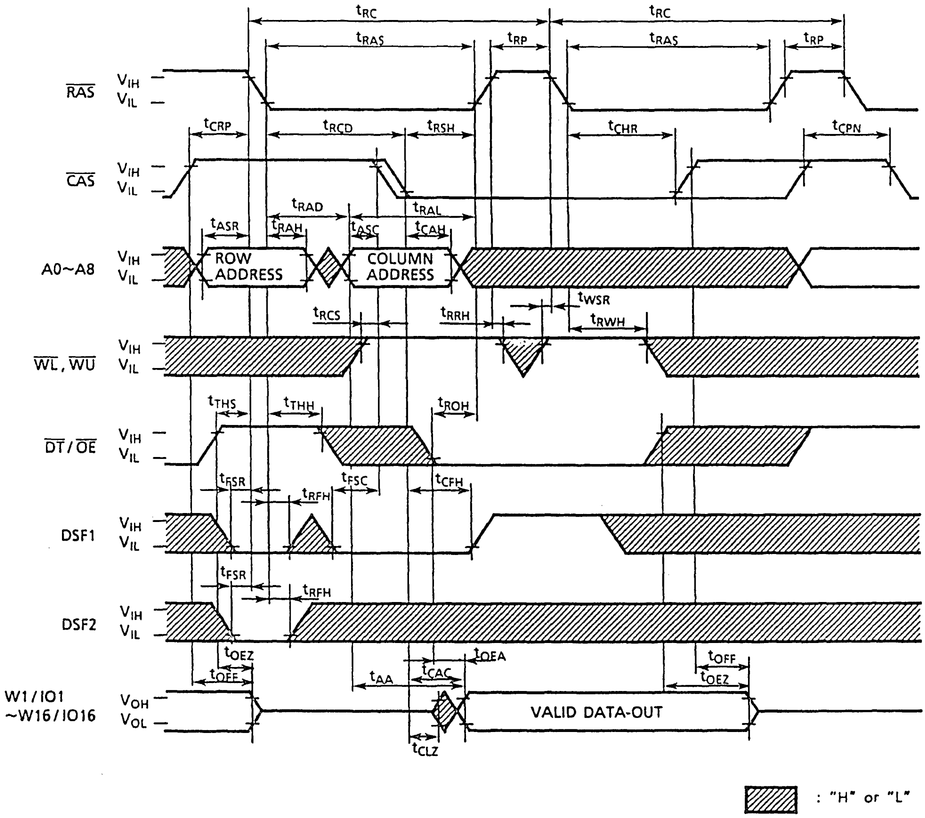
- W9/IO9 - Column 0 (A2C=0, A1C=0, A0C=0)
- W10/IO10 - Column 1 (A2C=0, A1C=0, A0C=1)
- W11/IO11 - Column 2 (A2C=0, A1C=1, A0C=0)
- W12/IO12 - Column 3 (A2C=0, A1C=1, A0C=1)
- W13/IO13 - Column 4 (A2C=1, A1C=0, A0C=0)
- W14/IO14 - Column 5 (A2C=1, A1C=0, A0C=1)
- W15/IO15 - Column 6 (A2C=1, A1C=1, A0C=0)
- W16/IO16 - Column 7 (A2C=1, A1C=1, A0C=1)

Wn/IOn
=0 : Disable
=1 : Enable

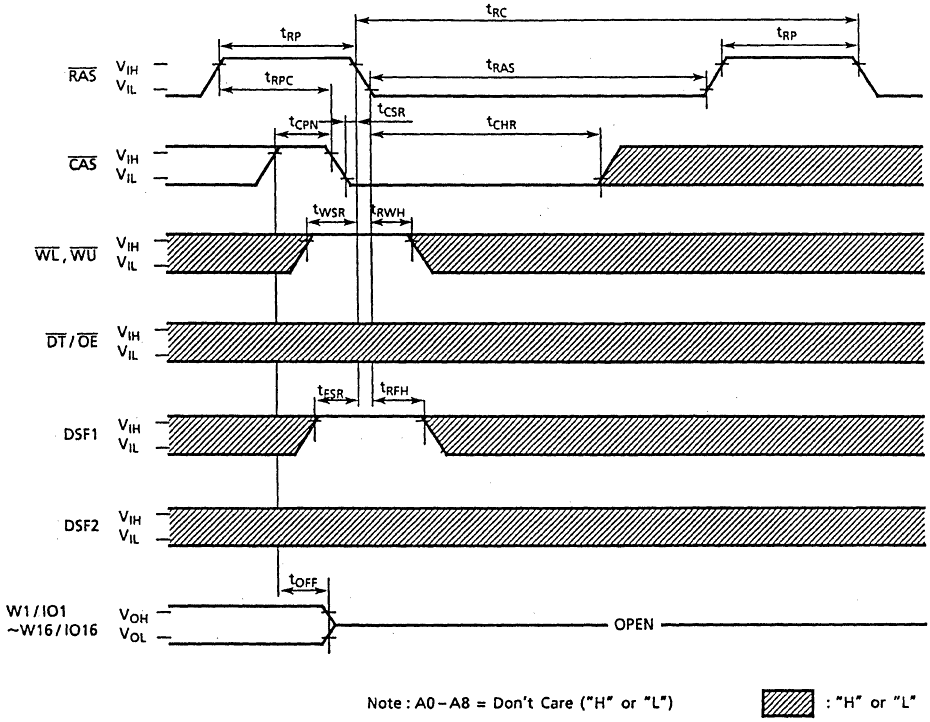
$\overline{RAS}$ ONLY REFRESH CYCLE



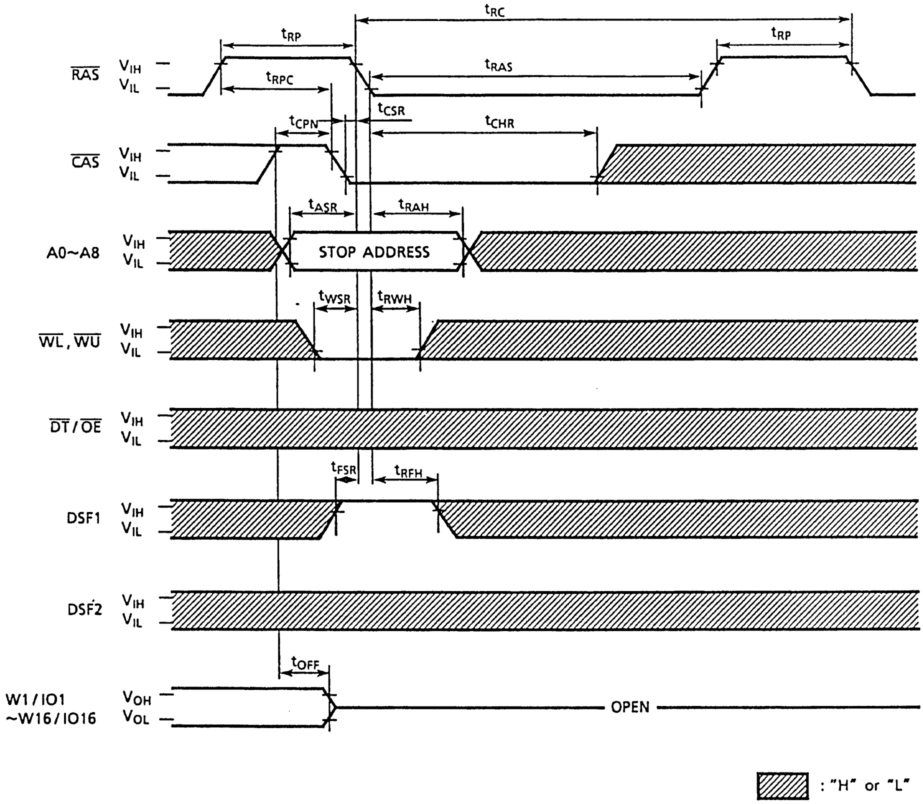
HIDDEN REFRESH CYCLE



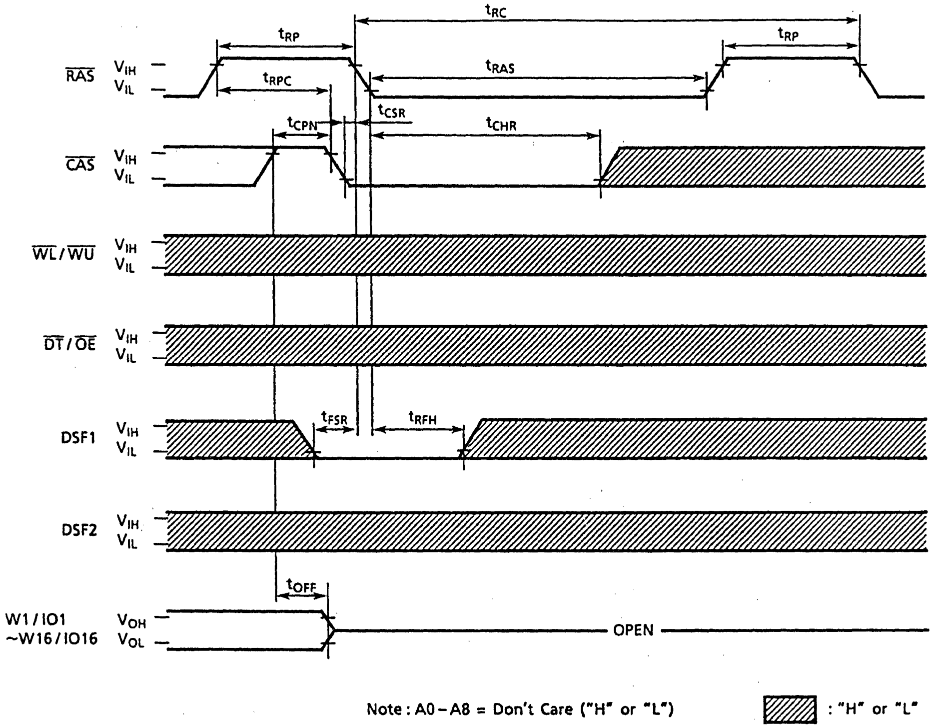
CBR AUTO REFRESH CYCLE



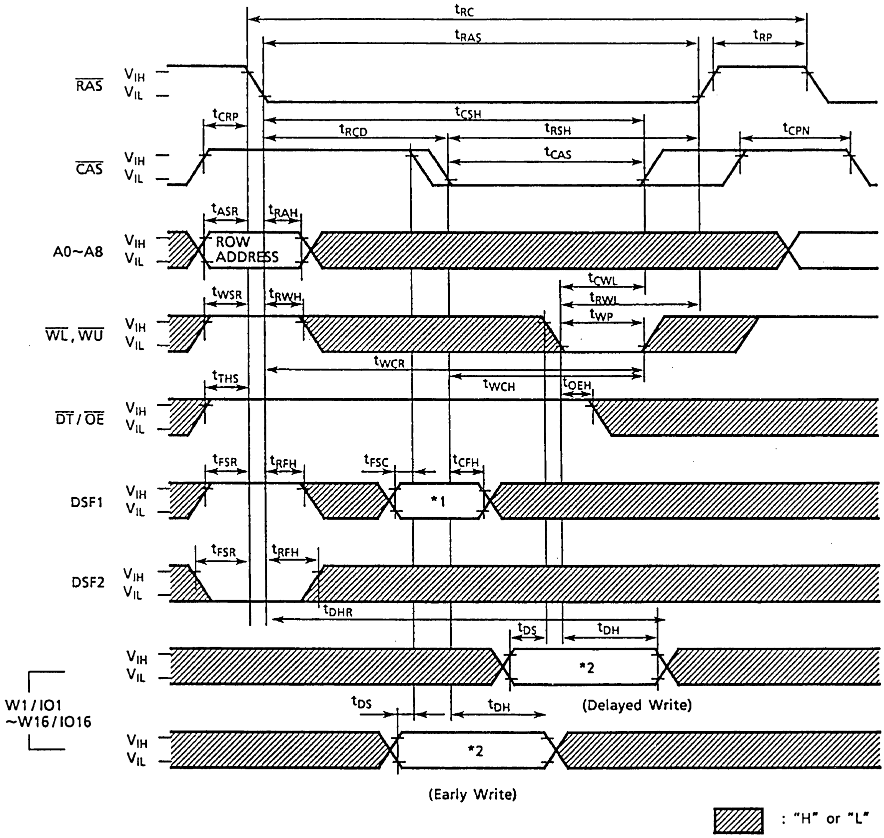
CBR AUTO REFRESH & STOP REGISTER SET CYCLE



CBR AUTO REFRESH & RESET CYCLE

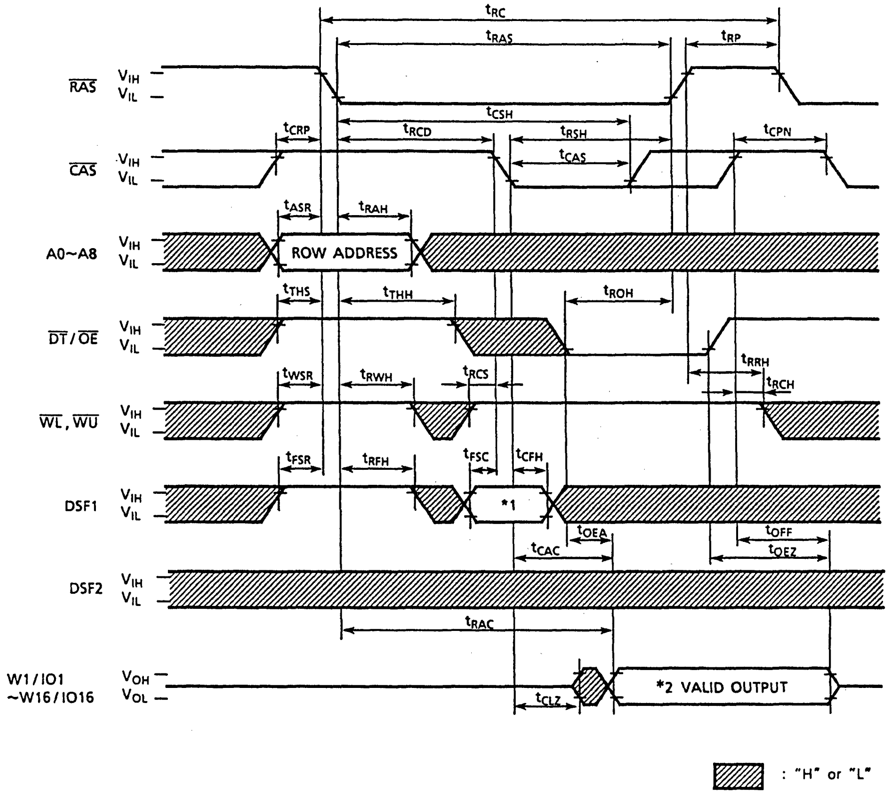


LOAD MASK/COLOR REGISTERCYCLE *Note 4, 5



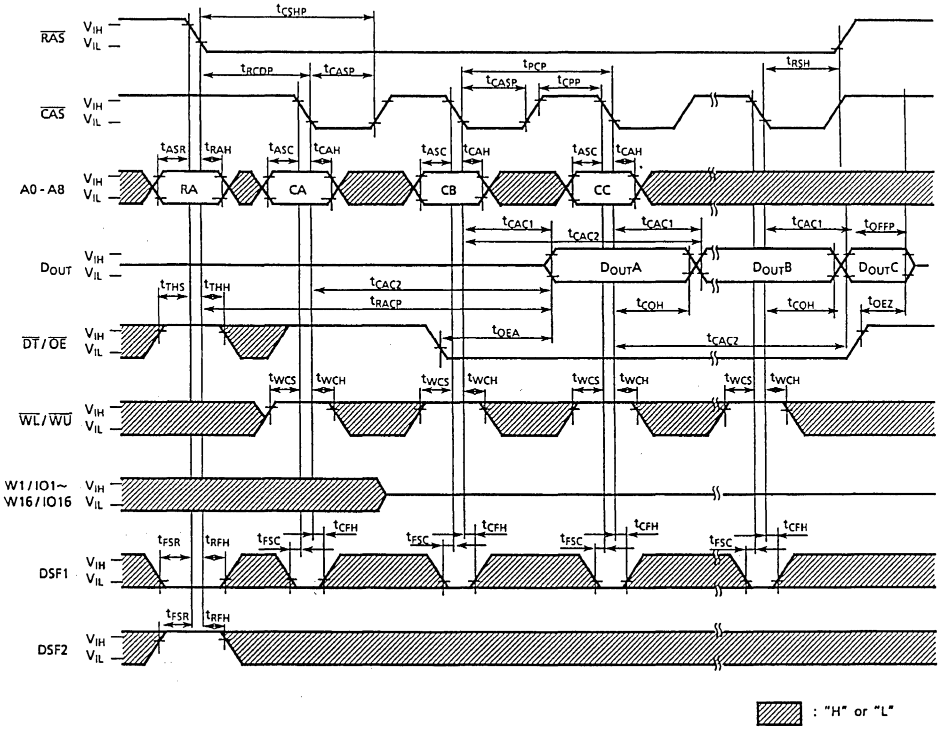
*1	*2	Function
0	Mask data	Load Mask Register Cycle
1	Color data	Load Color Register Cycle

READ MASK/COLOR REGISTER CYCLE

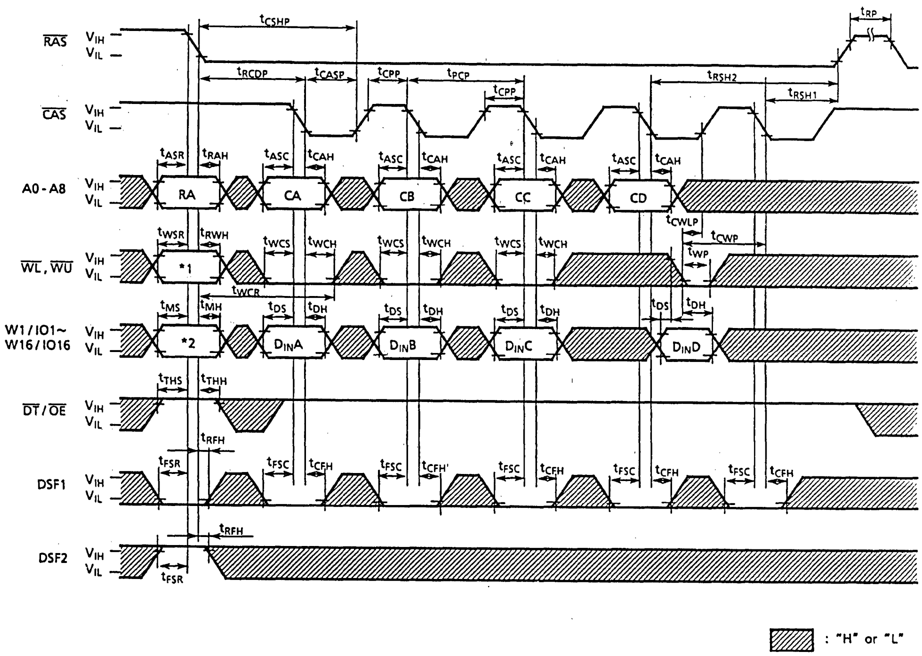


*1	*2	Function
0	Mask data	Load Mask Register Cycle
1	Color data	Load Color Register Cycle

PIPELINED FAST PAGE READ CYCLE



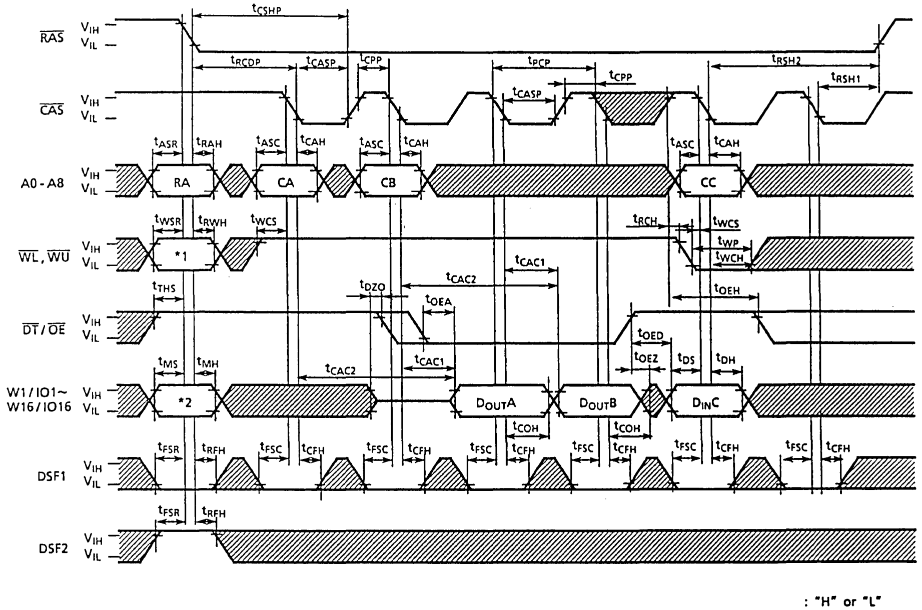
PIPELINED FAST PAGE WRITE CYCLE *Note 1, 2, 3



Mask Mode	*1		*2	Cycle
	WL	WU		
No Mask Mode	1	1	Don't care	Normal Write
New Mask Mode	0 0 1	0 1 0	WM1 data	Write per Bit
Old Mask Mode	0 0 1	0 1 0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable
Don't care : '1' or '0'

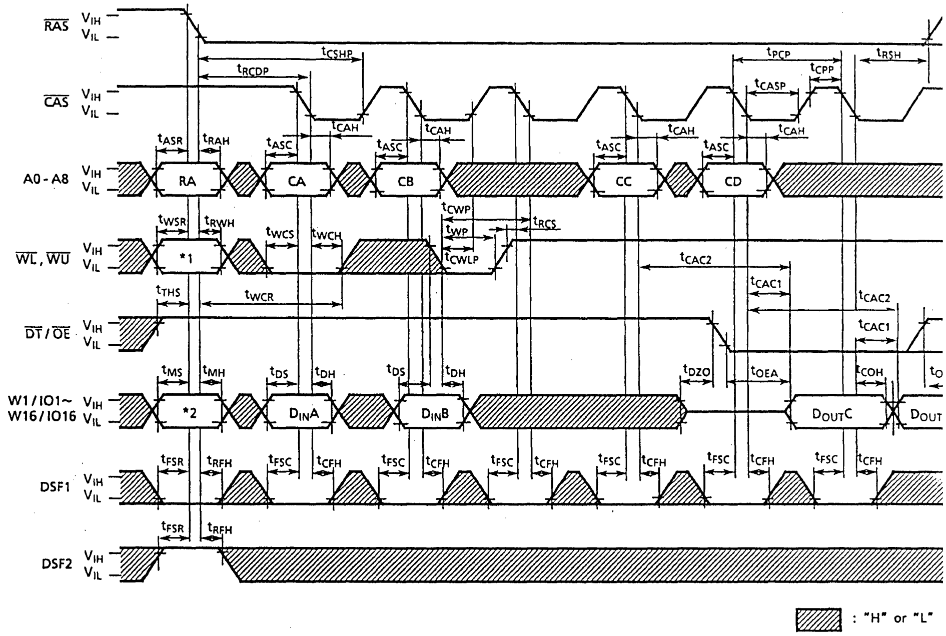
PIPELINED FAST PAGE READ-WRITE CYCLE



Mask Mode	*1		*2	Cycle
	$\overline{WL}$	$\overline{WU}$		
No Mask Mode	1	1	Don't care	Normal Write
New Mask Mode	0 0 1	0 1 0	WM1 data	Write per Bit
Old Mask Mode	0 0 1	0 1 0	Don't care	Write per Bit

WM1 data   0: Write Disable
            1: Write Enable
Don't care   : '1' or '0'

PIPELINED FAST PAGE WRITE-READ CYCLE

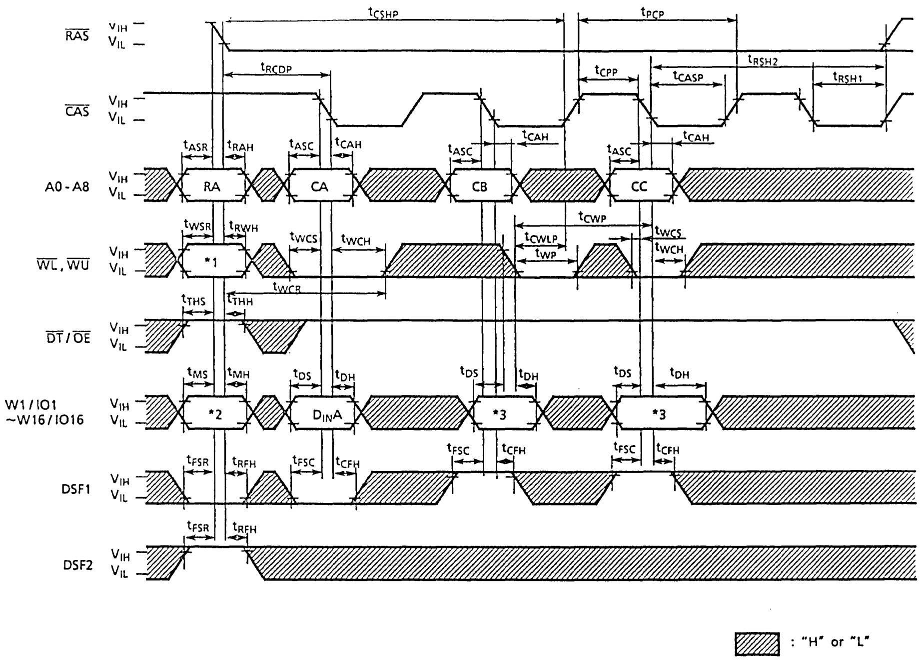


Mask Mode	*1		*2	Cycle
	WL	WU		
No Mask Mode	1	1	Don't care	Normal Write
New Mask Mode	0 0 1	0 1 0	WM1 data	Write per Bit
Old Mask Mode	0 0 1	0 1 0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

PIPELINED FAST PAGE WRITE-BLOCK WRITE CYCLE



Mask Mode	*1		*2
	WL	WU	
No Mask Mode	1	1	Don't care
New Mask Mode	0 0 1	0 1 0	WM1 data
Old Mask Mode	0 0 1	0 1 0	Don't care

WM1 data 0: Write Disable
 1: Write Enable

Don't care : '0' or '1'

*3 COLUMN SELECT

Lower Byte

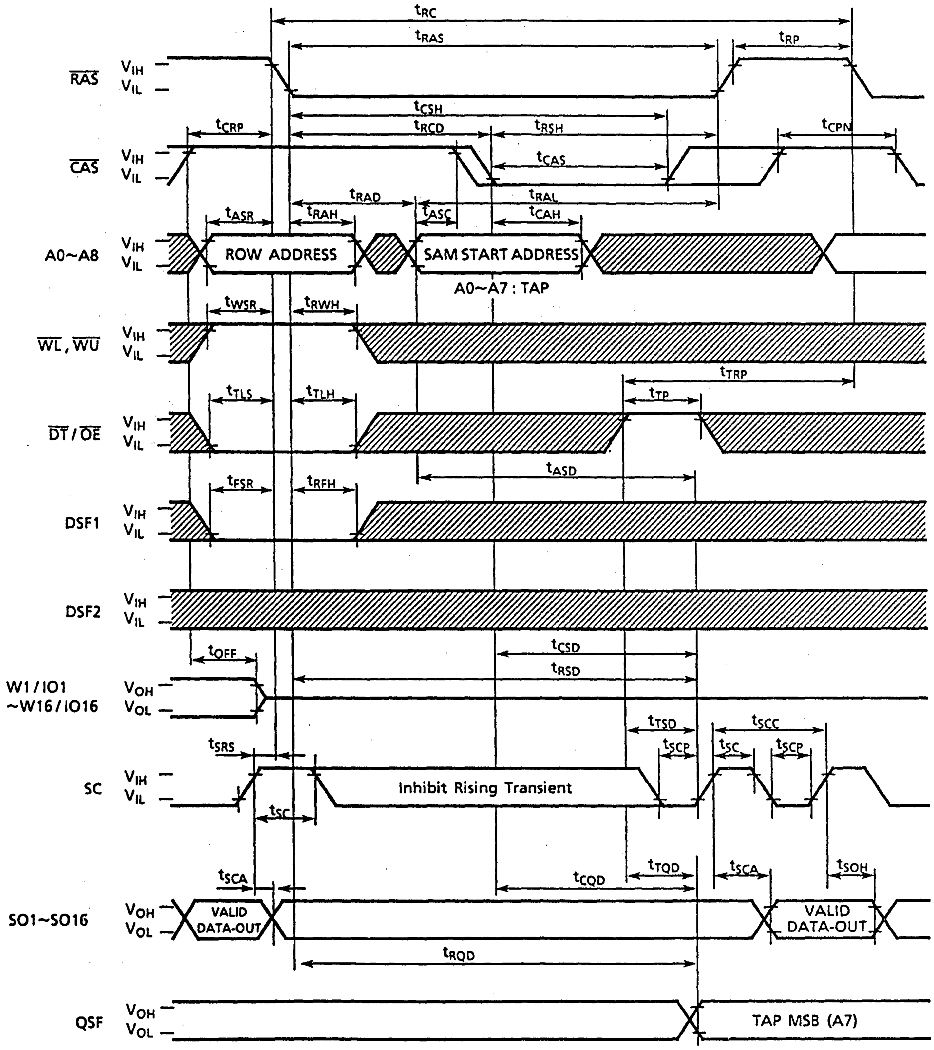
- W1/IO1 - Column 0 (A2C=0, A1C=0, A0C=0)
- W2/IO2 - Column 1 (A2C=0, A1C=0, A0C=1)
- W3/IO3 - Column 2 (A2C=0, A1C=1, A0C=0)
- W4/IO4 - Column 3 (A2C=0, A1C=1, A0C=1)
- W5/IO5 - Column 4 (A2C=1, A1C=0, A0C=0)
- W6/IO6 - Column 5 (A2C=1, A1C=0, A0C=1)
- W7/IO7 - Column 6 (A2C=1, A1C=1, A0C=0)
- W8/IO8 - Column 7 (A2C=1, A1C=1, A0C=1)

Upper Byte

- W9/IO9 - Column 0 (A2C=0, A1C=0, A0C=0)
- W10/IO10 - Column 1 (A2C=0, A1C=0, A0C=1)
- W11/IO11 - Column 2 (A2C=0, A1C=1, A0C=0)
- W12/IO12 - Column 3 (A2C=0, A1C=1, A0C=1)
- W13/IO13 - Column 4 (A2C=1, A1C=0, A0C=0)
- W14/IO14 - Column 5 (A2C=1, A1C=0, A0C=1)
- W15/IO15 - Column 6 (A2C=1, A1C=1, A0C=0)
- W16/IO16 - Column 7 (A2C=1, A1C=1, A0C=1)

Wn/IOn
=0 : Disable
=1 : Enable

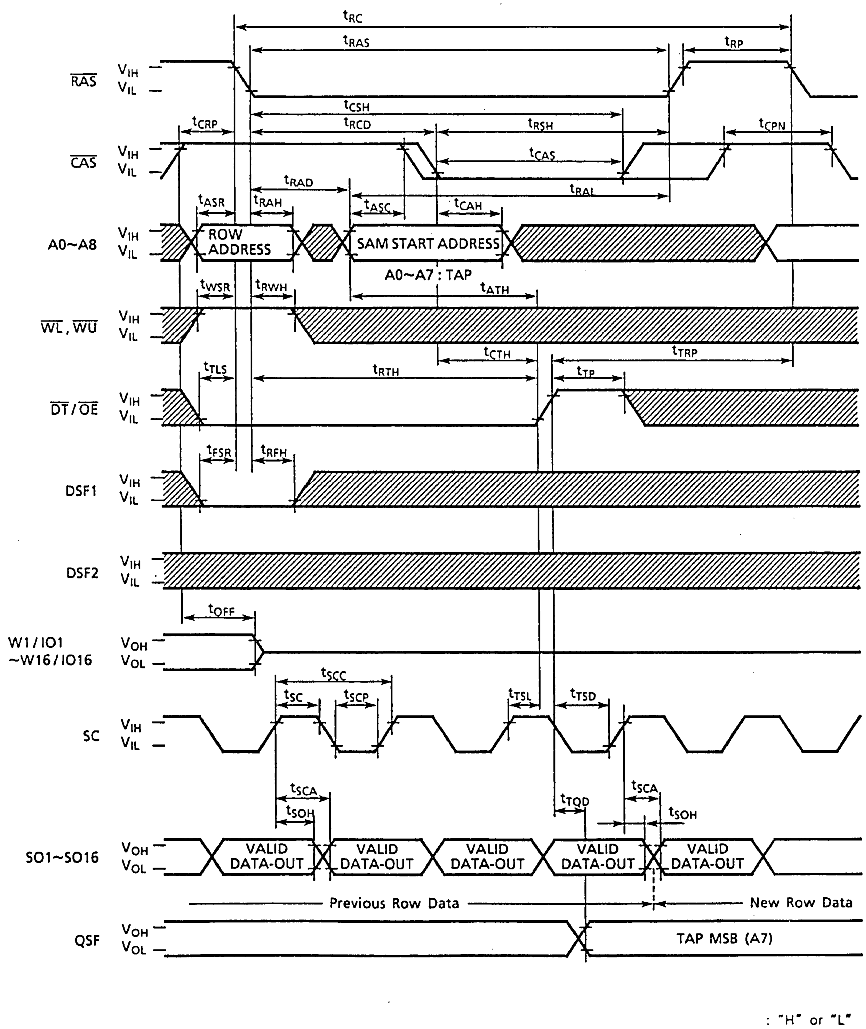
READ TRANSFER CYCLE



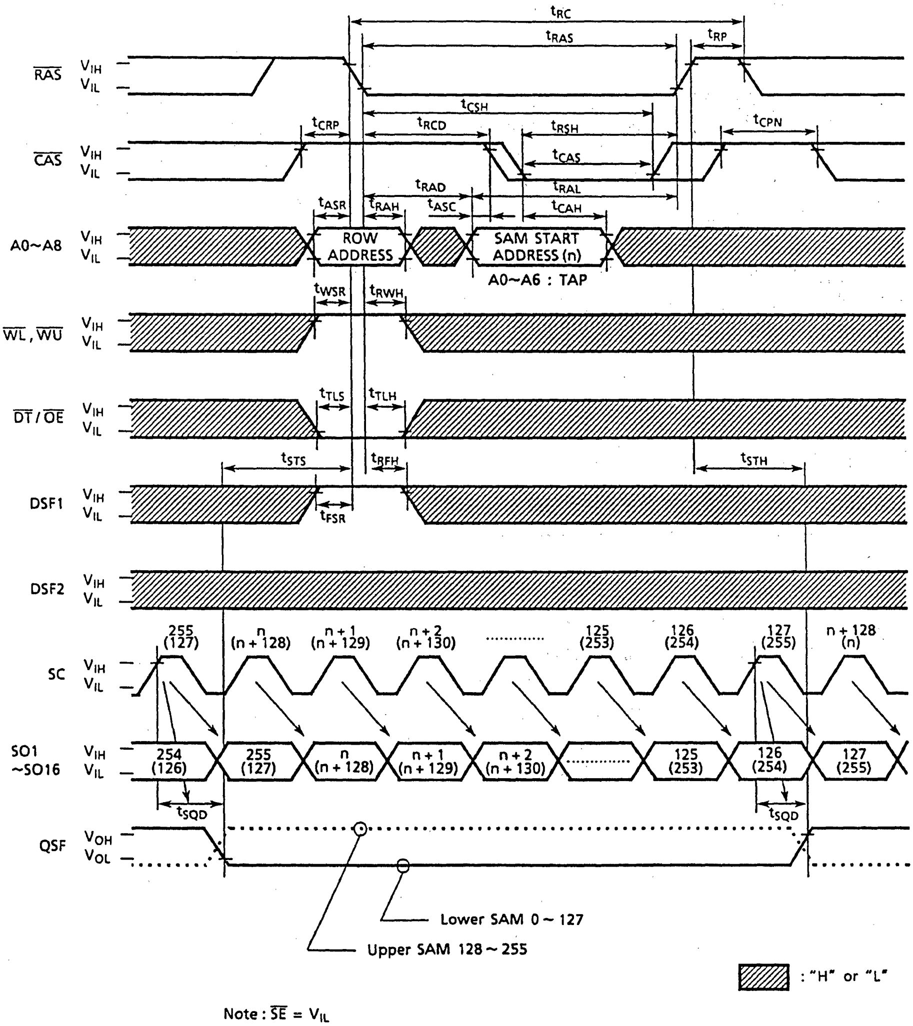
Note : $\overline{SE}$ = V_{IL}

▨ : "H" or "L"

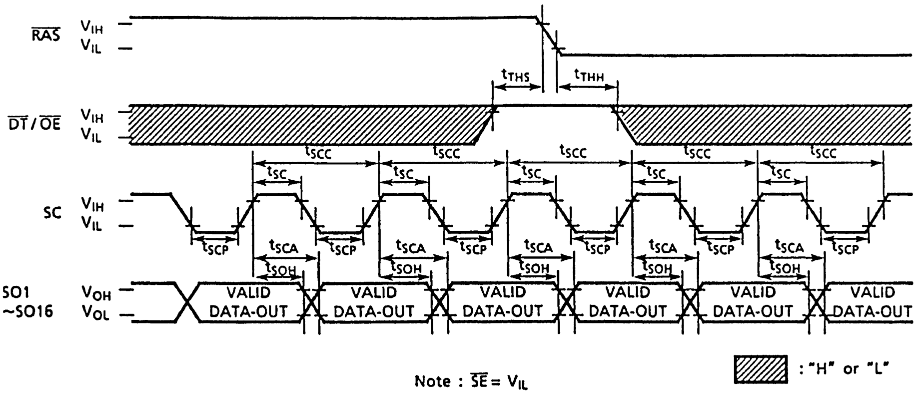
REAL TIME READ TRANSFER CYCLE



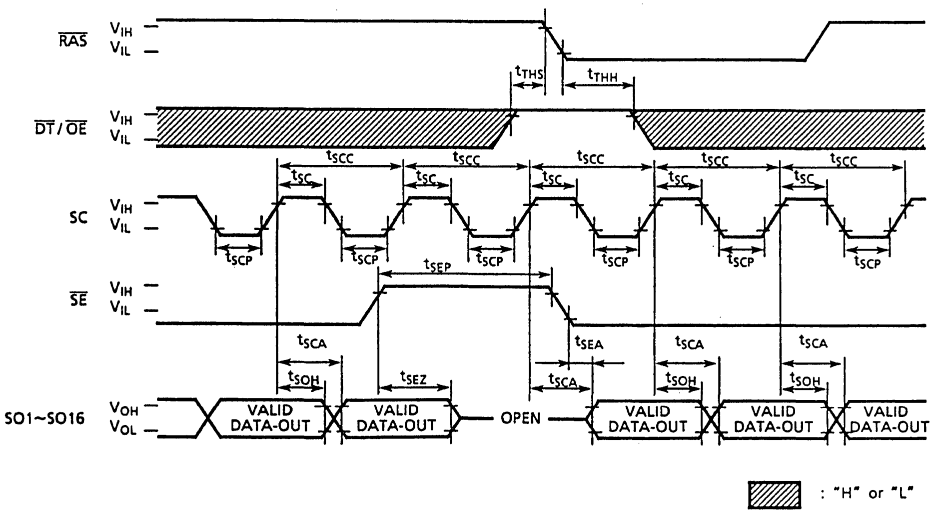
SPLIT READ TRANSFER CYCLE



SERIAL READ CYCLE ($\overline{SE} = V_{IL}$)



SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



PIN FUNCTION

ADDRESS INPUTS : A_0~A_8

The 18 address bits are required to decode16 bits of the 2,097,152 cell locations within the dynamic RAM memory array and they are multiplexed onto 9 address input pins (A_0~A_8). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

ROW ADDRESS STROBE : $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WEU}/\overline{WEL}$, DSF1 and DSF2 to invoke the various random access and data transfer operating modes shown in Table 1.

$\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high".

COLUMN ADDRESS STROBE : $\overline{CAS}$

$\overline{CAS}$ is the control input that latches the column address bits which are also used for the tap address during the transfer operations. The state of the special function input DSF1 is read at the $\overline{CAS}$ falling edge to select the block write mode or load register functions in conjunction with the $\overline{RAS}$ control. $\overline{CAS}$ before $\overline{RAS}$ refresh operations are selected if the signal is "low" at the $\overline{RAS}$ falling edge.

DATA TRANSFER/OUTPUT ENABLE : $\overline{DT}/\overline{OE}$

The $\overline{DT}/\overline{OE}$ input is a multifunction pin. When $\overline{DT}/\overline{OE}$ is "high" at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT}/\overline{OE}$ is used as an output enable control. If it is "low", a data transfer operation is activated between the RAM and the SAM.

WRITE PER BIT/WRITE ENABLE : $\overline{WB}/\overline{WE}$

The $\overline{WEU}/\overline{WEL}$ input is also a multifunction pin. When the signal is "high" at the falling edge of $\overline{RAS}$, during the RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. If the signal is "low" at the $\overline{RAS}$ falling edge, the write-per-bit function is enabled.

	$\overline{WEU}$	$\overline{WEL}$	Function
$\overline{RAS}\downarrow$	H	H	Read/Write
	L	H	Upper byte write per bit
	H	L	Lower byte Write per bit
	L	L	Word Write per bit

WRITE MASK DATA/DATA INPUT AND OUTPUT: W_1 /IO_1~W_{16} /IO_{16}

Data is written into the RAM through W_1/IO_1~W_{16} /IO_{16} pins during a write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WEU}/\overline{WEL}$, whichever occurs late. In a read cycle data is read out of the RAM on the W_i / IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and column address. The Lower and Upper 8 bits are also used as the column address mask during a block white cycle. The each 8 bits correspond to Lower/Upper byte column.

When the write-per-bit function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register at the falling edge of $\overline{RAS}$. In a load mask and color register cycles, the data on the W_i/IO_i pins is stored into the write mask register and the color register respectively.

SERIAL CLOCK : SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted out of the SAM registers at the rising edge of SC. The serial clock SC also increments the 9-bits serial pointer which is used to select the SAM address. The SC pin must be held at a constant V_{IH} or V_{IL} level during read transfer operations and should not be clocked while the SAM is in standby mode to prevent the SAM pointer from being incremented.

No control signal disable SC input, and in any time SC toggle cause SAM pointer drarge regardless Sout (controlled by $\overline{SE}$).

SERIAL ENABLE : $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer is still incremented while SC is clocked.

SPECIAL FUNCTION CONTROL INPUT: DSF1, DSF2

DSF1 is latched at the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to select the various TC524162/165 operations. If the signal is kept "low", the basical functions featured in conventional multi-port DRAM are enabled. To use the block write, the flash write and the load register functions or the split transfer operations, the DSF1 signal needs to be controlled as shown in Table 1.

When the DSF2 signal is "high" at the falling edge of $\overline{RAS}$, pipelined page mode operations are enabled. The pipeline mode is supported with the read, write and block write functions.

SPECIAL FUNCTION OUTPUT: QSF

QSF is an output signal which, during split register mode, indicates which half of the split SAM is being accessed. QSF "low" indicates that the lower split SAM (Bit 0~255) is being accessed and QSF "high" indicates that the upper split SAM (Bit 256~511) is being accessed. QSF is monitored so that after it toggles and waiting a delay of t_{STS}, split read transfer operation can be performed on the non-active split SAM.

SERIAL OUTPUT : SO_1~SO_{16}

Serial output SO_1~SO_{16} are the output pin of SAM register. SAM data out is valid t_{SCA} after SC rising edge. These SO_1~SO_{16} output is controlled by $\overline{SE}$. SO_i is going to Hi-Z state when $\overline{SE}$ goes high.

OPERATION MODE

The RAM port and data transfer operating of the TG524162/165 are determined by the state of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WEU}/\overline{WEL}$, DSF1 and DSF2 at the falling edge of $\overline{RAS}$ and by the state of DSF1 at the falling edge of $\overline{CAS}$. The Table 1 shows the functional truth table for a listing of all available RAM port and transfer operations.

Table 1. Functional Truth Table

RAS ↓					CAS ↓	Mnemonic Code	Function
CAS	DT/OE	WEU[4]/WEL	DSF1	DSF2	DSF1		
0	*	*	0	*	-	CBR	CBR Auto Refresh & Option Reset [1), 2)]
0	*	0	1	*	-	CBRS	CBR Auto Refresh & Stop Register Set[2)]
0	*	1	1	*	-	CBRN	CBR Auto Refresh
1	0	1	0	*	*	RT	Read Transfer
1	0	1	1	*	*	SRT	Split Read Transfer
1	1	0	0	0	0	RWM	Read Write (New/Old Mask)[1)]
1	1	0	0	0	1	BWM	BlockWrite (New/Old Mask)[1)]
1	1	0	1	*	*	FWM	FlashWrite (New/Old Mask)[1)]
1	1	1	0	0	0	RW	Read Write (No Mask)
1	1	1	0	0	1	BW	Block Write (No Mask)
1	1	0	0	1	0	RWM(P)	PFP[3)] Read Write (New/Old Mask)[1)]
1	1	0	0	1	1	BWM(P)	PFP[3)] Block Write (New/Old Mask)[1)]
1	1	1	0	1	0	RW(P)	PFP[3)] Read Write (No Mask)
1	1	1	0	1	1	BW(P)	PFP[3)] Block Write (No Mask)
1	1	1	1	*	0	LMR	Load (Old) Mask Register[1)]
1	1	1	1	*	1	LCR	Load Color Register

Note : * =0 or 1, - = Not applicable

1) After LMR operation, RWM, BWM, FWM, RWM (P), BWM (P) use old mask.
   Either CBR operation or LMR operation with no mask bits resets the old mask mode to new mask mode.
2) CBRS operation determines binary boundaries in the SAM.
   CBR operation resets the boundaries.
3) PFP stands for pipelined fast page mode.
4) The state of WEU/WEL is defined as Logical "AND" of WEU and WEL state.

RAM PORT OPERATION

1. READ WRITE FUNCTION : RW

The TC524162/165 is equipped with the read write function which is identical to the conventional dynamic RAM's one and supports read, early write, $\overline{OE}$ controlled write and read-modify-write cycles as shown in the timing charts. Extended fast page (TC524165) and pipelined page modes are also available with the read write cycles by performing multiple $\overline{CAS}$ cycles during a single active $\overline{RAS}$ cycle.

1.1 EXTENDED FAST PAGE MODE (TC524165)

Extended fast page mode allows faster access to the memory in an actual system than the conventional fast page mode. An output data remains valid after the $\overline{CAS}$ signal goes high to prepare the next output data. Thus, the system has longer period to read the data from the RAM. Read, write and read-modify-write cycles are available during the extended fast page mode.

2. WRITE-PER-BIT (MASKED WRITE) FUNCTION : RWM

The write-per-bit (masked write) function selectively controls the internal write enable circuits of the RAM port. When $\overline{WE}$ is held "low" at the falling edge of $\overline{RAS}$, during the RWM cycle, the write mask is enabled. At the same time, the mask data on the Wi/IOi pins is latched into the write-mask register. The I/O mask data maintains in a single $\overline{RAS}$ cycle, a page (New Mask Mode). When a load mask register function (LMR) is performed, the write mask data on the Wi/IOi pins is latched into the write-mask register. After the LMR operation, the data at the falling edge of $\overline{RAS}$ during the RWM cycle is ignored and the I/O mask data that was stored in the write-mask register is used (Old Mask Mode) until the mode is reset by either CBR operation or LMR operation with no mask bits. The truth table of the write-per-bit function is shown in Table 2.

Table 2. Truth table for write-per-bit function

At the falling edge of $\overline{RAS}$				Write Mask Register	Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	W_i/IO_i (i=1~16)		
H	H	L	1	←	Write Enable
			0	←	Write Disable (New Mask)
			*	1	Write Enable
			*	0	Write Disable (Old Mask)

Note: * = 1 or 0 , ← = The data on Wi/IOi is latched.

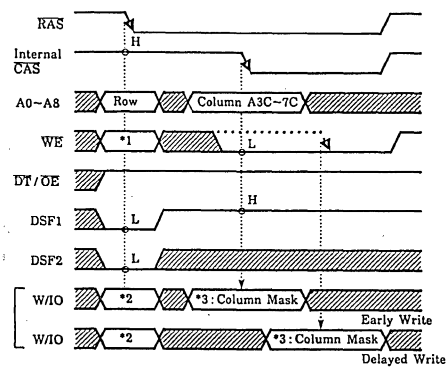
3. BLOCK WRITE AND MASKED BLOCK WRITE : BW &B WM

Block write is a special RAM port write operation which, in a page, allows for the data in the color register to be written into 8 consecutive column address locations starting from a selected column address in a selected row. The block write operation can be selectively disabled on an I/O basis and a column mask capability is also available.

A block write cycle is performed by holding $\overline{CAS}$, $\overline{DT}/\overline{OE}$ "high" and DSF1 "low" at the $\overline{RAS}$ falling edge and by holding DSF1 "high" at the $\overline{CAS}$ falling edge. If the DSF signal is "low" at the $\overline{CAS}$ falling edge, a normal read/write operation will occur. Therefore, a combination of block write, read and write operations can be performed during a fast page mode cycle. The state of $\overline{WEU}/\overline{WEL}$ input at the falling edge of $\overline{RAS}$ determines whether or not the I/O mask is enabled ($\overline{WEU}/\overline{WEL}$ must be "low" to enable the I/O mask, BMW mode or "high" to disable it, BW mode). The I/O mask is provided on the Wi/IOi input at the $\overline{RAS}$ falling edge. After LMR operation, however, the old mask is used for the I/O mask function. The column mask data on the W_i/IO_i input must be provided at the $\overline{CAS}$ or $\overline{WEU}/\overline{WEL}$ falling edge whichever is late, while the six most significant colunm address (A3C~A8C) are latched at the falling edge of $\overline{CAS}$. This latched column address determines the start column address of consecutive block.

The block write is most effective for window clear and fill operation in frame buffer applications.

Figure 1. Block Write Operation



Example (Shown on Lower byte. The same manner on Upper byte)

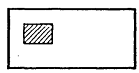
	W/IO 1	2	3	4	5	6	7	8
WM1 Register (Lower)	1	1	(0)	(0)	1	(0)	1	(0)
Column Select (Lower byte)	1	(0)	1	1	1	(0)	(0)	1
Color Register (Lower)	1	0	1	0	1	1	0	0

Result

	W/IO 1	2	3	4	5	6	7	8
Column 0	1	0			1		0	
Column 1								
Column 2	1	0			1		0	
Column 3	1	0			1		0	
Column 4	1	0			1		0	
Column 5								
Column 6								
Column 7	1	0			1		0	

Application

- High Speed Window Cear
- High Speed Rectangular Fill



*1	*2	Mask Mode
1	Don't Care	No Mask Mode
0	WM1	New Mask Mode
0	Don't Care	Old Mask Mode

*3 : COLUMN MASK

Lower Byte

W1/IO1 - Column 0 (A2C=0, A1C=0, A0C=0)
W2/IO2 - Column 1 (A2C=0, A1C=0, A0C=1)
W3/IO3 - Column 2 (A2C=0, A1C=1, A0C=0)
W4/IO4 - Column 3 (A2C=0, A1C=1, A0C=1)
W5/IO5 - Column 4 (A2C=1, A1C=0, A0C=0)
W6/IO6 - Column 5 (A2C=1, A1C=0, A0C=1)
W7/IO7 - Column 6 (A2C=1, A1C=1, A0C=0)
W8/IO8 - Column 7 (A2C=1, A1C=1, A0C=1)

Upper Byte

W9/IO9 - Column 0 (A2C=0, A1C=0, A0C=0)
W10/IO10 - Column 1 (A2C=0, A1C=0, A0C=1)
W11/IO11 - Column 2 (A2C=0, A1C=1, A0C=0)
W12/IO12 - Column 3 (A2C=0, A1C=1, A0C=1)
W13/IO13 - Column 4 (A2C=1, A1C=0, A0C=0)
W14/IO14 - Column 5 (A2C=1, A1C=0, A0C=1)
W15/IO15 - Column 6 (A2C=1, A1C=1, A0C=0)
W16/IO16 - Column 7 (A2C=1, A1C=1, A0C=1)

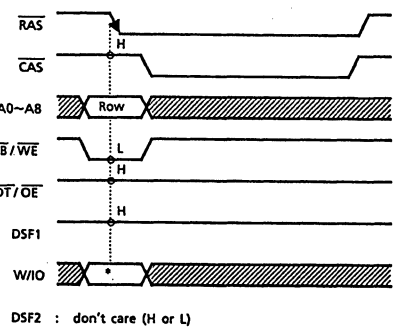
4. FLASH WRITE : FWM

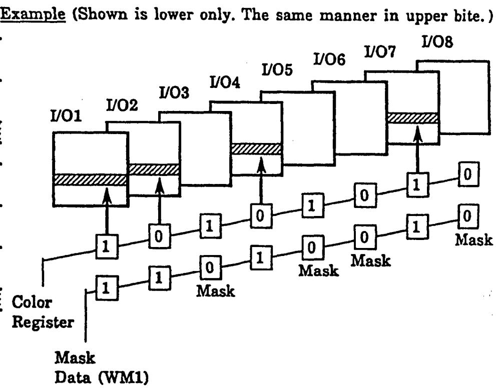
Flash write is also a special RAM port operation which in a single $\overline{RAS}$ cycle, allows for the data in the color register to be written into all the memory locations of a selected row. Each bit of the color register corresponds to one of the DRAM I/O blocks and the flash write operation can be selectively controlled on an I/O basis in the same manner as the write-per-bit operation.

A flash write cycle is performed by holding $\overline{CAS}$ "high", $\overline{WEU}/\overline{WEL}$ "low" and DSF1 "high" at the falling edge of $\overline{RAS}$. The mask data must also be provided on the W_i/IO_i inputs in order to enable the flash write operation for selected I/O blocks. After a LMR operation, however, the old mask in the mask register is used for the I/O block masking.

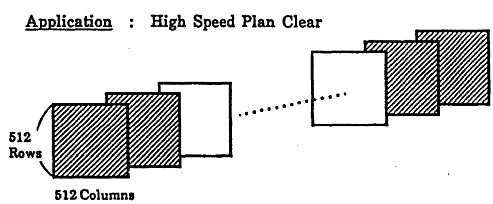
Flash write is most effective for fast plane clear operations in frame buffer applications. Selected planes can be cleared by performing 512 flash write cycle and by specifying a different row address location during each flash write cycle. Assuming a cycle time of 130ns, a plane clear operation can be completed in less than 66.6 µsec.

Figure 2. Flash Write Operation





*	Mask Mode
Mask Data	New Mask Mode
Don't Care (H or L)	Old Mask Mode



5. PIPELINED FAST PAGE MODE : RWM (P), BWM (P), RW (P), BW (P)

Pipelined fast page mode allows much faster access to the memory than the conventional page mode. Read, write and block write cycles are available at the pipelined fast page mode timings.

A pipelined fast page mode is performed by holding DSF2 "high" at the falling edge of $\overline{RAS}$. A pipelined fast page read, write and block write operations can run at 30ns cycle time for 70ns version. Also, those mode can be selected every $\overline{CAS}$ cycle by the status of $\overline{DT}/\overline{OE}$, $\overline{WEU}/\overline{WEL}$ and DSF1 pin. There are, however, penalties on the performance as follows:

(1) Two $\overline{CAS}$ cycles are required for the read operation. The fast access, hence, takes longer than page mode. Also, one $\overline{CAS}$ cycle is needed to read out the data before the write cycle starts in the same page.

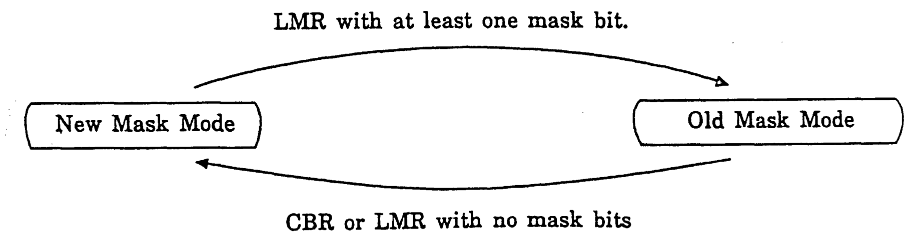
(2) One dummy cycle is needed to complete the write and block write operation. The cycle is, thus, needed between the write and the read operation and is required before the page ends.

A system designer needs to carefully estimate the system performances with the pipelined page mode and the conventional page mode in order to decide which mode should be used.

6. LOAD (OLD) MASK REGISTER LMR

The TC524162/165 has an on-chip 8 bit write-mask register which provides the I/O mask data during the masked functions such as the write-per-bit (RWM), masked block write (BWM) and flash write (FWM) functions. Each bit of the write-mask register corresponds to one of the DRAM I/O blocks. After the mask data is specified in the write-mask register by using the load mask register (LMR) cycle, the old mask mode is invoked during the masked functions. The I/O mask data in the write-mask register maintains until another LMR operation is performed during the old mask mode. The LMR cycle is initiated by holding $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WEU}/\overline{WEL}$ and DSF1 "high" at the falling edge of $\overline{RAS}$ and by DSF1 "low" at the falling edge of $\overline{CAS}$. The data presented on the Wi/IOi lines are subsequently latched into the write-mask register at the falling edge of either $\overline{CAS}$ or $\overline{WEU}/\overline{WEL}$, whichever occurs later. The old mask mode is reset to the new mask mode by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR) or a LMR cycle with no mask bits, all "1" on W_i/IO_i pins. During the LMR cycle, the memory cells of the row address which is latched at the falling edge of $\overline{RAS}$ are refreshed.

Figure 3. State Diagram of Mask Mode



7. LOAD COLOR REGISTER : LCR

The TC524162/165 is provided with an on-chip 8-bits register (color register) for use during the block write or flash write function. Each bit of the color register corresponds to one of the DRAM I/O blocks. The load color register cycle is initiated by holding $\overline{CAS}$, $\overline{WEU}/\overline{WEL}$, $\overline{DT}/\overline{OE}$ and DSF1 "high" at the falling edge of $\overline{RAS}$. The data presented on the W_i/IO_i lines is subsequently latched into the color register at the falling edge of either $\overline{CAS}$ or $\overline{WEU}/\overline{WEL}$, whichever occurs later. During the load color register cycle, the memory cells on the row address latched at the falling edge of $\overline{RAS}$ are refreshed.

8. REFRESH

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of 512 rows in the DRAM array within the specified 8 ms refresh period. The TC524162/165 supports the conventional dynamic RAM refresh operations such as $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh and hidden refresh.

8.1 $\overline{CAS}$ before $\overline{RAS}$ Refresh and Option Reset : CBR

The CBR cycle reset the following functions, performing the $\overline{CAS}$ before $\overline{RAS}$ refresh operation at the same time.

- To reset the old mask mode to the new mask mode for the masked functions.
- To reset the stop register and remove the binary boundaries for the split SAM operation.

The systems which implement neither the old mask mode nor the binary boundary in the SAM is recommended to use the CBR cycle for refresh operation.

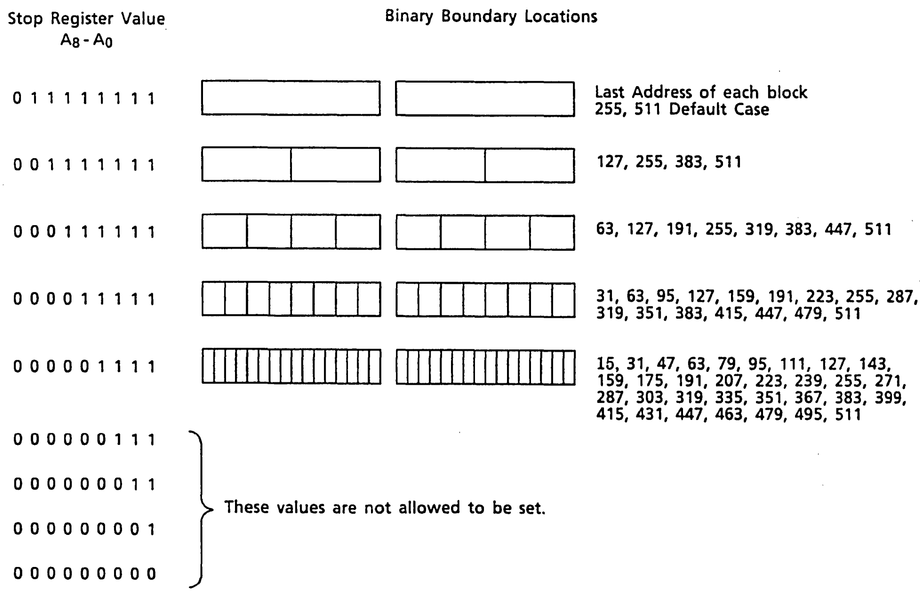
8.2 $\overline{CAS}$ before $\overline{RAS}$ Refresh : CBRN

The CBRN cycle performs only the $\overline{CAS}$ before $\overline{RAS}$ refresh operation. The systems which implement either the old mask mode or the binary boundary in the SAM usually use the CBRN cycle for refresh operation except for at the required stop register set or option reset cycles. The CBRN cycle must not be used during the initialization after power-up,

8.3 $\overline{CAS}$ before $\overline{RAS}$ Refresh and Stop Register Set : CBRS

The CBRS cycle sets the stop register to place binary boundaries in each half SAM, performing the $\overline{CAS}$ before $\overline{RAS}$ refresh operation at the same time. The CBRS cycle is initiated by $\overline{CAS}$ holding "low" and by $\overline{WEU}$ $\overline{/WEL}$ and DSF1 "high" at the falling edge of $\overline{RAS}$. At the same time the data on the address pins, A_0 - A_8 is latched and the binary boundaries in each half SAM will be available when a split transfer operation is performed,

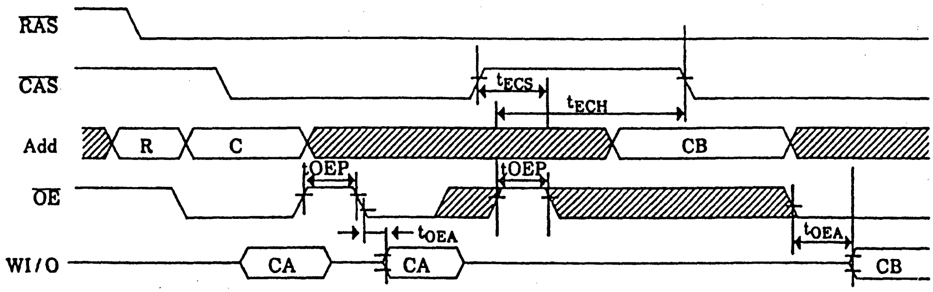
Figure 4 . Stop Register and Binary Boundary Location



NOTE

$\overline{OE}$ control of Extended Fast Page mode Read cycle (TC524163/165)

When $\overline{OE}$ is toggled while $\overline{CAS}$ is "Low" level in fast page mode read cycle, the same data is valid on WI/O. However, the data will not be valid when $\overline{OE}$ goes low with $\overline{CAS}$ high condition. The data will come out in following $\overline{CAS}$ cycle. Such a $\overline{OE}$ control have to satisfy t_{OEP} (10ns min), t_{ECS} (10ns min), t_{ECH} (10ns min). Please refer following Figure.



DATA TRANSFER OPERATION

The TC524162/165 features internal data transfer capability between the RAM and the SAM, as shown in Figure 5. During a normal transfer, 512 words by16 bits of data can be loaded from RAM to SAM (Read Transfer). During a split transfer, 256 words by16 bits of data can be loaded from the lower/upper half of the RAM into the lower/upper half of the SAM (Split Read Transfer). The normal transfer and split transfer modes are controlled by the DSF1 input signal

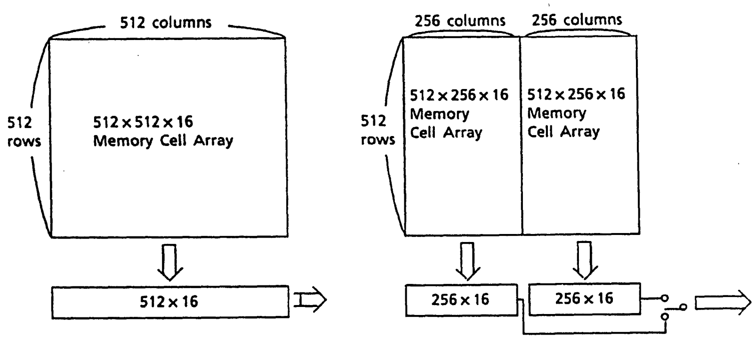


Figure 5. (a) Normal Transfer (b) Split Transfer

Table 3. Shows the truth table of each Transfer Modes

RAS↓				Mnemonic Code	Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DFS1					
H	L	H	L	RT	Read Transfer	RAM → SAM	512x16	Input → Output
H	L	H	H	SRT	Split Read Transfer	RAM → SAM	256x16	Half SAM active

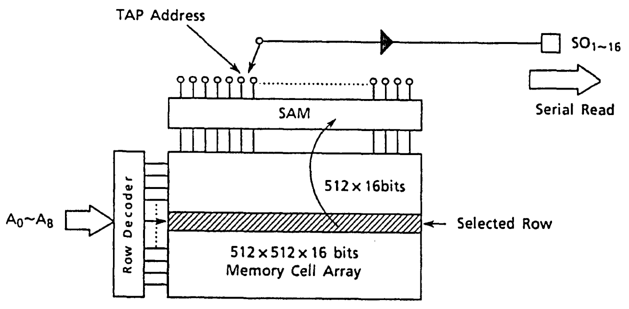
9. READ TRANSFER CYCLE : RT

A read transfer consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low" $\overline{WEU}/\overline{WEL}$ "high" and DSF1 "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The start address of the serial pointer of the SAM (TAP address) is determined by the column address selected at the falling edge of $\overline{CAS}$.

By doing a tight timing control between the $\overline{DT}/\overline{OE}$ rising edge and SC falling edge, a real time read transfer operation can also be performed.

Figure 6 shows the operation block diagram for read transfer operation

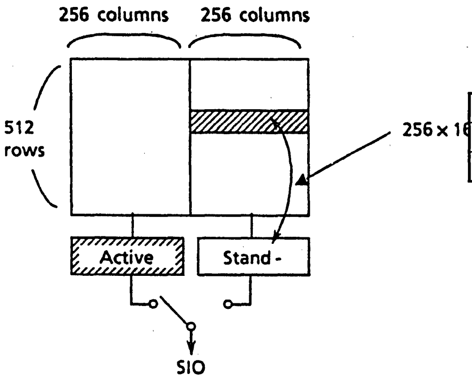
Figure 6. Block Diagram for Read Transfer Operation.



In a read transfer cycle, the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}/\overline{OE}$ and the falling edge of $\overline{RAS}$ and $\overline{CAS}$, as shown in READ TRANSFER CYCLE timing chart.

10. SPLIT READ TRANSFER CYCLE : SRT

A split read transfer consists of loading 256 words by 16 bits of data from a selected row of the half RAM array into the corresponding half SAM in stand-by mode. Serial data can be shifted out of the other half of the SAM in active mode siumltaneously, as shown in Figure 7. The most significant column address (A8C) is controlled internally to determine which half of the SAM will be reloaded from the RAM array. During the split read transfer operation, the RAM port control signals do not have to be synchronized with the serial clock SC, thus eliminating the timing restrictions as in the case of real time read transfers. Prior to the execution of the split read transfer operation, a (normal) transfer operation must be performed to determine the absolute tap address location. QSF is an output that indicates which half of the SAM is in the active state. QSF changes state when the last SC clock is applied to the active SAM, as shown in Figure 8.



Active SAM	QSF Level
lower SAM	"Low"
upper SAM	"High"

Figure 7. Split Read Transfer

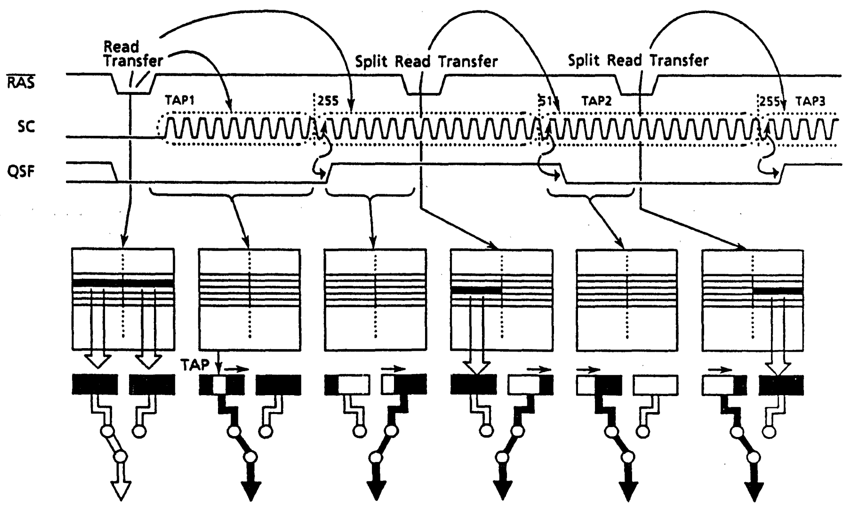
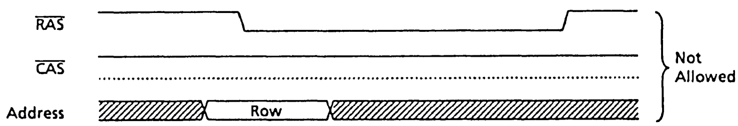


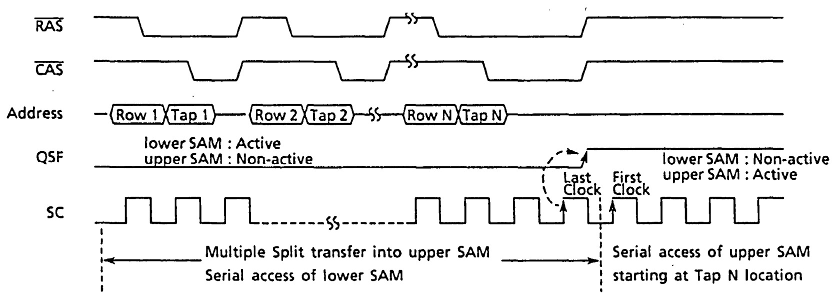
Figure 8. Example of Consecutive Read Transfer Operations

NOTES

(1) Transfer operation without $\overline{CAS}$.
The SAM tap location is undefined if $\overline{CAS}$ is maintained at a constant "high" level during a transfer cycle. A transfer cycle with $\overline{CAS}$ held "high" is, hence, not allowed.



(2) In the case of multiple split transfers performed into the same half SAM, the tap location specified during the last split transfer, before QSF toggles, will prevail, as shown below.



(3) Split transfer operation allowable period.
Figure 9 illustrates the relationship between the serial clock SC and the special function output QSF during split read / write transfers and highlights the time periods where split transfers are allowed, relative to SC and QSF. A split transfer is not allowed during to $t_{STH} + t_{STS}$. In the case that the CBRS operation is executed and the binary boundary in each half SAM is set or updated, an additional period is applied, as shown in Figure 9.

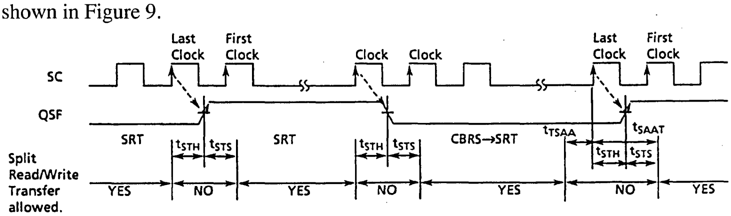
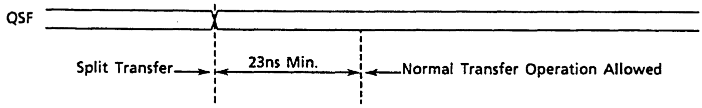


Figure 9. Split Transfer Operation Allowable Periods

Figure 12. Split Transfer Operation Allowable Periods

The stop register and binary boundary are explained in the CBRS operation and the SAM port operation.

(4) A normal transfer may be performed following split transfer operation provided that a 23ns minimum delay is satisfied after the QSF signal toggles.

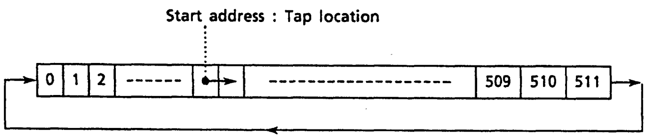


SAM PORT OPERATION

The TC524162/165 is provided with 512 words by16 bits serial access memory (SAM) which can be operated in the single register mode or the split register mode. High speed serial read or write operations can be performed through the SAM port independent of the RAM port operation.

11. SINGLE REGISTER SERIAL READ OPERATION

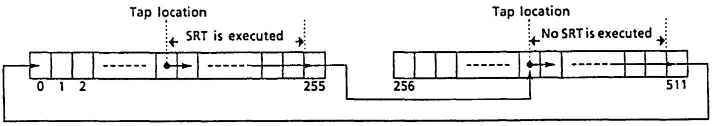
Serial data can be read out of the SAM port after a read transfer has been performed. At every rising edge of the serial clock, the data is read out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit, as illustrated below. Subsequent real-time read transfer may be performed on-the-fly as many times as desired.



12. SPLIT REGISTER MODE

The split register mode realizes continuous serial read operation. The data can be shifted into or out of one half of the SAM while a split read transfer is being performed on the other half of the SAM. Thus, the tight timing control at a real time read operation is eliminated with the split read operation. A normal read transfer operation must precede any split read transfer operation in order to set the TAP address. Also, a $\overline{CAS}$ before $\overline{RAS}$ refresh and stop register set cycle (CBRS) can be performed to specify the binary boundaries in the SAM.

In the split register mode, serial data can be read from one of the split registers starting from any of the 256 tap locations. The data is read sequentially from the tap location to the most significant bit (255 or 511) of the first split SAM and then the SAM pointer moves to the tap location selected for the second split SAM to read the data sequentially to the most significant bit (255 or 511) and finally wraps around to the least significant bit, as illustrated in the example below.



13. SPLIT REGISTER MODE WITH BINARY BOUNDARY

After a CBRS cycle is performed, the binary boundary, which is stated in 8.3. $\overline{CAS}$ before $\overline{RAS}$ refresh and stop register set, is set when a SRT cycle is performed. The serial data is read from one half of the SAM starting the tap location to the next binary boundary, while another SRT cycle is performed. Then, the SAM pointer moves to the tap location in the other half SAM and the data is read from the half SAM sequentially. If any SRT operation is not performed before the next boundary, the SAM pointer does not jump to the other half SAM, as illustrated in Figure 10.

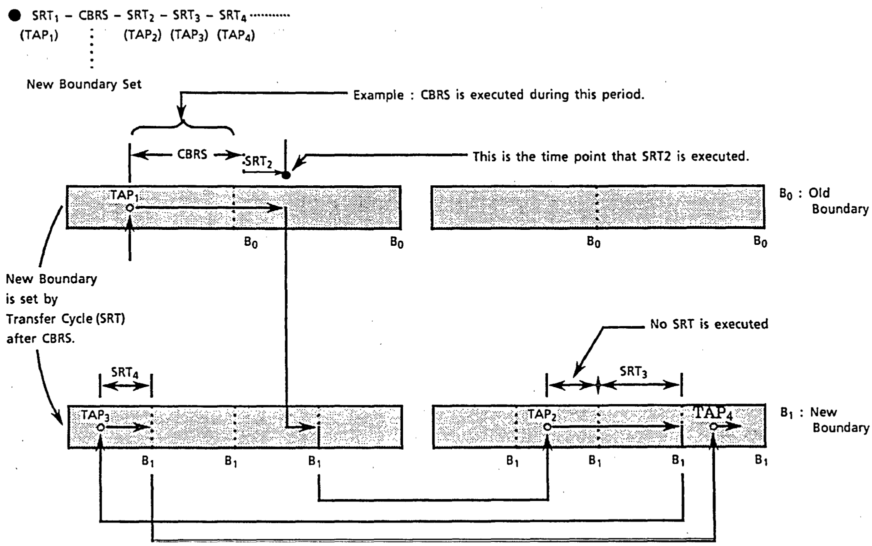


Figure 10. Operation of Split Register Mode with Binary Boundary

The binary boundary is reset by a CBR cycle and the SAM operation mode returns to the normal split register mode, as shown in Figure 11.

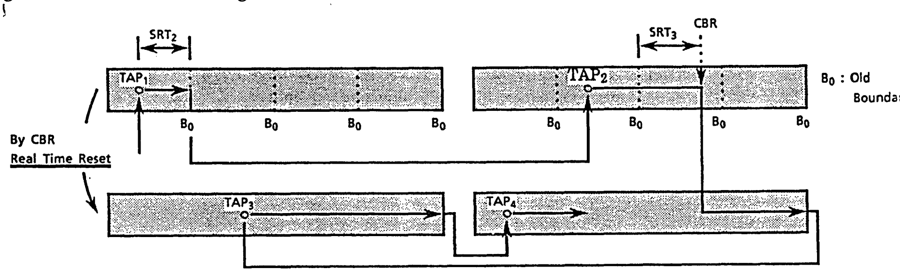


Figure 11. Binary Boundary Reset

Fig. 12 shows the relation between CBR and SC on binary-boundary-reset. When Nth SC-colck accesses old binary address is reset and (N+1)th SC clock accesses old boundary address (old stop address) + 1 on the same split SAM, not jump to TAP address.t

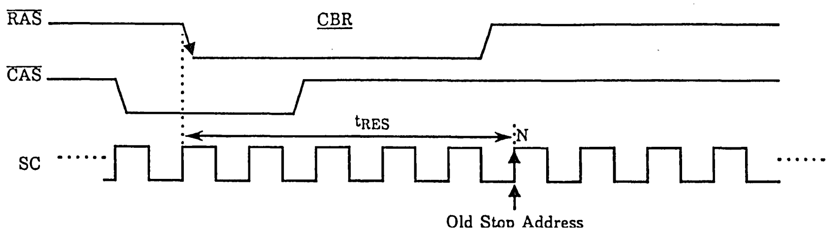


Figure 12. CBR and SC relation of binary-boundary-reset

In an actual system which uses the binary boundary a CBRS cycle is executed to determine a type of the boundary location. Then, a normal RT transfers a row of data into the SAM and set the initial tap location at the same time. An SRT cycle follows it before the SAM pointer reaches to the boundary location. The SRT cycle makes the binary boundary jump effective, as illustrated in Figure 13.

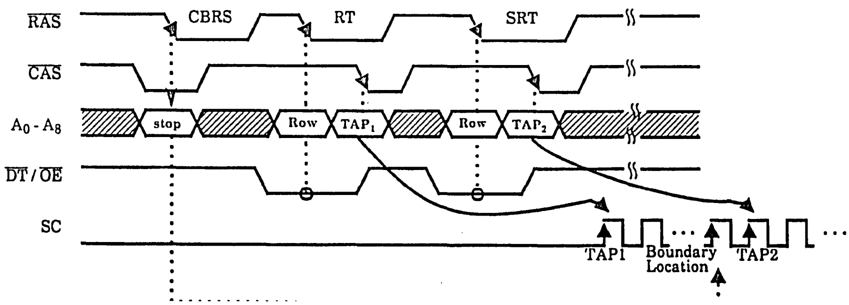


Figure 13. Binary Boundary Jump Set Sequence

There are additional timing specifications, t_{TSAA} and t_{SAAT} to determine the period that does not allow a split transfer, as illustrated in Figure 14.

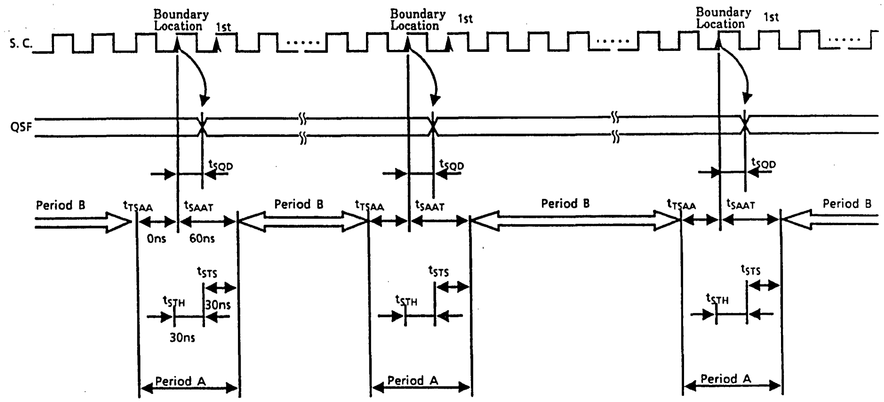


Figure 14. Timing Specification to allow SRT operation

POWER-UP

Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them "high" before or at the same time as the V_{CC} supply is turned on. After power-up, a pause of 200 µseconds minimum is required with $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ held "high". After the pause, a minimum of 8 CBR dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT}/\overline{OE}$ signal must be held "high".

INITIAL STATE AFTER POWER-UP

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and $\overline{WEU}/\overline{WEL}$ held "high", the internal state of the TC524162/165 is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state setting cycle is performed after the initialization of the device is performed (200 µseconds pause followed by a minimum of 8 CBR cycles) and before valid operations begin.

	State after power-up
QSF	High-Impedance
Color Register	all "0"
Write Mask Register	Write Enable
TAP pointer	Invalid
Stop Register	Default Case

SILICON GATE CMOS
262,144 WORDS x 16 BITS MULTIPORT DRAM

target spec

DESCRIPTION

The TC524262/265 is a 4M bit CMOS multiport memory equipped with a 262,144-words by 16-bits dynamic random access memory (RAM) port and a 512-words by 16-bits static serial access memory (SAM) port. The TC524262/265 supports three types of operations; Random access to and from the RAM port, high speed serial access from the SAM port and transfer of data from any selected row in the RAM to the SAM. To realize a high performance graphic frame buffer system the TC524262/265 features various special operations such as the write - per - bit, the pipelined page mode, the block write and flash write function on the RAM port and the read transfer operations from the RAM to the SAM port. In addition, extended fast page mode is available where an output data remains valid during the $\overline{CASL}/\overline{CASU}$ is high (TC524265 only). The TC524262/265 is fabricated using Toshiba's CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

FEATURES

- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- All inputs and outputs TTL Compatible
- Organization
  - RAM Port : 262,144wordsX16bits
  - SAM Port : 512wordsX16bits
- RAM Port
  - Fast Page Mode (TC524262)
  - Extended Fast Page Mode (TC524265)
  - Read - Modify - Write
  - Pipelined Fast Page Mode
  - $\overline{CAS}$ before $\overline{RAS}$ Auto Refresh
  - Hidden Refresh
  - $\overline{RAS}$ only Refresh
  - Write per Bit (New / Old Mask Mode)
  - Masked Flash Write (New / Old Mask Mode)
  - Block Write
  - Masked Block Write (New/Old Mask Mode)
  - Load Mask Register / Color Register Cycle
  - 512 refresh cycles/8ms
- SAM Port
  - Addressable TAP Capability
  - Stop Address (Binary Boundary) Capability
  - Fully Static Register
  - Single Register/Split Register Mode Capability
- RAM - SAM Transfer
  - Read/Real Time Read Transfer
  - Split Read Transfer
- Package
  - TC524262/265SF : SSOP64 - P - 525
  - TC524262/265FT : TSOP70 - P - 400
  - TC524262/265TR : TSOP70 - P - 400A

KEY PARAMETERS

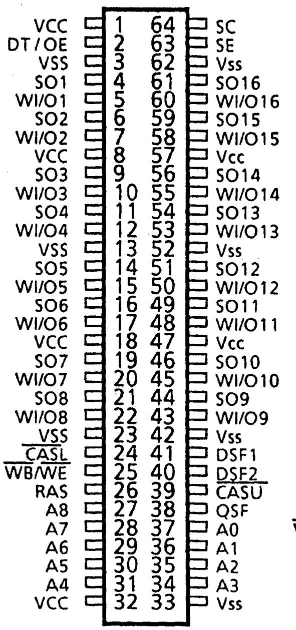
ITEM		—60	—70
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	15ns	20ns
t_{AA}	Column Address Access Time (Max.)	30ns	35ns
t_{RC}	Cycle Time (Min.)	115ns	130ns
t_{PC}	Page Mode Cycle Time (Min.)	35ns	40ns
t_{SCA}	Serial Access Time (Max.)	15ns	20ns
t_{SCC}	Serial Cycle Time (Min.)	18ns	23ns
t_{RACP}	t_{RAC} in Pipelined Fast Page	85ns	90ns
t_{CAC1}	t_{CAC} in Pipelined Fast Page	15ns	20ns
t_{PCP}	Pipelined Fast Page Mode Cycle Time	30ns	30ns
I_{CC1}	RAM Operating Current (SAM : Standby)	110mA	100mA
I_{CC2A}	SAM Operating Current (RAM : Standby)	60mA	60mA
I_{CC2}	Standby Current	10mA	10mA

PIN NAME

A0~A8	Address inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CASL}$/$\overline{CASU}$	Column Address Strobe
$\overline{DT}$/$\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}$/$\overline{WE}$	Write per Bit/Write Enable
DSF1 DSF2	Special Function Control
Wl/IOl ~W1/IO16	Write Mask/Data IN, OUT
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIOl~SIO6	Serial Input/Output
QSF	Special Flag Output
V_{CC}/V_{SS}	Power (5V) / Ground
N.C.	No Connection

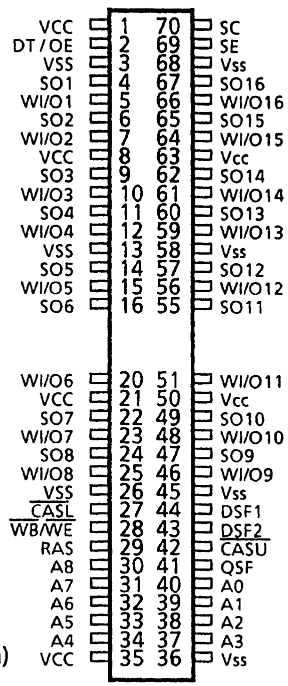
PIN CONNECTION (TOP VIEW)

TC524262/265SF

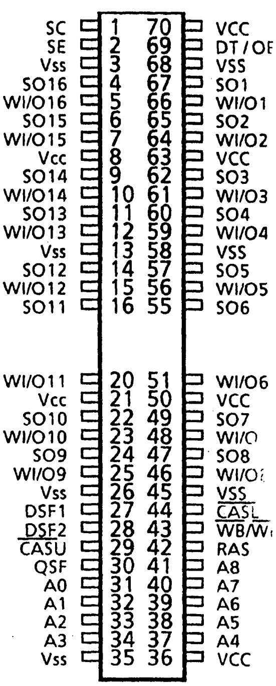


525mil SSOP (0.8mm pitch)

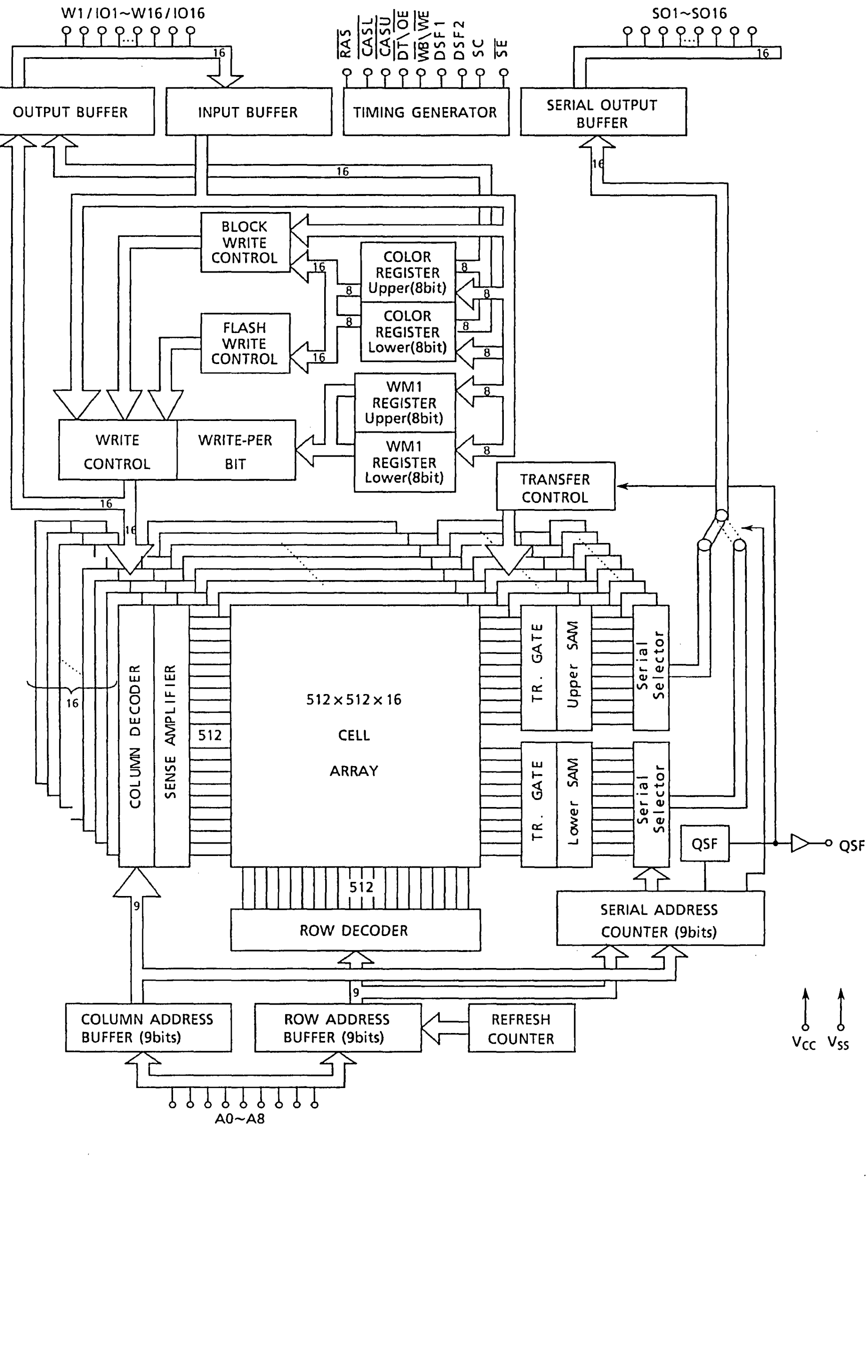
TC524262/265FT



TC524262/265TR



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}, V_{OUT}	Input Output Voltage	— 1.0~7.0	V	1
V_{CC}	Power Supply Voltage	— 1.0~7.0	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	— 55~150	°C	1
T_{SOLDER}	Soldering Temperature • Time	260•10	°C•sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.3	V	2
V_{IL}	Input Low Voltage	- 1.0	—	0.8	V	2

CAPACITANCE (V_{CC} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance	—	7	pF
C_{IO}	Input/Output Capacitance	—	9	
C_O	Output Capacitance (QSF)	—	9	

Note: This parameter is periodically sampled and is not 100% tested.

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

ITEM (RAM PORT)	SAM PORT	SYMBOL	-60 MIN.	-60 MAX.	-70 MIN.	-70 MAX.	UNIT	NOTE
OPERATING CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, $t_{RC} = t_{RC}$ min.)	Standby	I_{CC1}	—	110	—	100	mA	3, 4, 5
	Active	I_{CC1A}	—	160	—	150	mA	3, 4, 5
STANDBY CURRENT ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	Standby	I_{CC2}	—	10	—	10	mA	
	Active	I_{CC2A}	—	60	—	60	mA	3, 4
RAS ONLY REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, $t_{RC} = t_{RC}$ min.)	Standby	I_{CC3}	—	110	—	100	mA	3
	Active	I_{CC3A}	—	160	—	150	mA	3
PAGE MODE CURRENT ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, $t_{PC} = t_{RC}$ min.)	Standby	I_{CC4}	—	100	—	90	mA	3, 4, 5
	Active	I_{CC4A}	—	150	—	140	mA	3, 4, 5
CAS BEFORE RAS REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$, $t_{RC} = t_{RC}$ min.)	Standby	I_{CC5}	—	110	—	100	mA	3
	Active	I_{CC5A}	—	160	—	150	mA	3
DATA TRANSFER CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, $t_{RC} = t_{RC}$ min.)	Standby	I_{CC6}	—	130	—	120	mA	3, 4, 5
	Active	I_{CC6A}	—	180	—	170	mA	3, 4, 5
FLASH WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, $t_{RC} = t_{RC}$ min.)	Standby	I_{CC7}	—	110	—	100	mA	3, 4, 5
	Active	I_{CC7A}	—	160	—	150	mA	3, 4, 5
BLOCK WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, $t_{RC} = t_{RC}$ min.)	Standby	I_{CC8}	—	120	—	110	mA	3, 4, 5
	Active	I_{CC8A}	—	170	—	160	mA	3, 4, 5

ITEM	SYMBOL	MIN.	MAX	UNIT	NOTE
INPUT LEAKAGE CURRENT $0V \leq V_{IN} \leq V_{CC} + 0.3V$, All other pins not under test = 0V	$I_{I(L)}$	—10	10	μA	
OUTPUT LEAKAGE CURRENT $0V \leq V_{OUT} \leq V_{CC} + 0.3V$, OutputDisable	$I_{O(L)}$	—10	10	μA	
OUTPUT "H" LEVEL VOLTAGE (RAM and SAM) I_{OUT} = - 1mA	V_{OH}	2.4	—	V	
OUTPUT "L" LEVEL VOLTAGE (RAM and SAM) I_{OUT} = 2.1mA	V_{OL}	—	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes: 6, 7)

SYMBOL	PARAMETER	-60		-70		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX		
t_{RC}	Random Read or Write Cycle Time	115		130		ns	
t_{RMW}	Read-Modify-Write Cycle Time	140		180			
t_{PC}	Fast Page Mode Cycle Time	35		40			
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	85		85			
t_{RAC}	Access Time from $\overline{RAS}$		60		70		13
t_{AA}	Access Time from Column Address		30		35		13
t_{CAC}	Access Time from $\overline{CAS}$		15		20		14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		30		35		14
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0		0			
t_{OFF}	Output Buffer Turn-Off Delay	0	15	0	15		9, 15
t_T	Transition Time (Rise and Fall)	3	50	3	50		8
t_{RP}	$\overline{RAS}$ Precharge Time	45		50			
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10000	70	10000		
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode Only)	60	100000	70	100000		
t_{RSH}	$\overline{RAS}$ Hold Time	20		20			
t_{CSH}	$\overline{CAS}$ Hold Time	60		70			
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10000	20	10000		
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50		13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35		13
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35			
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5			
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10			
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10			
t_{ASR}	Row Address Set-Up Time	0		0			
t_{RAH}	Row Address Hold Time	10		10			
t_{ASC}	Column Address Set-Up Time	0		0			
t_{CAH}	Column Address Hold Time	10		10			
t_{RCS}	Read Command Set-Up Time	0		0			
t_{RCH}	Read Command Hold Time	0		0			10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0			10
t_{WCH}	Write Command Hold Time	10		10			
t_{WP}	Write Command Pulse Width	10		10			
t_{WPZ}	Write Command Pulse Width	10		10			9
t_{WEZ}	Write Command Output Buffer Turn-Off Delay		10		15		9
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20			
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20			
t_{DS}	Data Set-Up Time	0		0			12

SYMBOL	PARAMETER	-60		-70		UNIT	NOTE
		MIN.	MAX	MIN.	MAX		
t_{DH}	Data Hold Time	10		10			11
t_{WCS}	Write Command Set-Up Time	0		0			12
t_{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	80		90			12
t_{AWD}	Column Address to $\overline{\text{WE}}$ Delay Time	50		55			12
t_{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	40		40			12
t_{DZC}	Data to $\overline{\text{CAS}}$ Delay Time	0		0			
t_{DZO}	Data to $\overline{\text{OE}}$ Delay Time	0		0			
t_{OEA}	Access Time from $\overline{\text{OE}}$		15		20	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{\text{OE}}$		15		15		9
t_{OED}	$\overline{\text{OE}}$ to Data Delay Time	10		10			
t_{OEH}	$\overline{\text{OE}}$ Command Hold Time	10		10			
t_{ODS}	Output Disable Set up time	0		0			
t_{ROH}	$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	15		15			
t_{CSR}	$\overline{\text{CAS}}$ Set-Up Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle	5		5			
t_{CHR}	$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle	15		15			
t_{RPC}	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	0		0			
t_{REF}	Refresh Period (512cycle)		8		8	ms	
t_{WSR}	$\overline{\text{WB}}$ Set-Up Time	0		0			
t_{RWH}	$\overline{\text{WB}}$ Hold Time	10		10			
t_{FSR}	DSF Set-Up Time referenced to $\overline{\text{RAS}}$	0		0			
t_{RFH}	DSF Hold Time referenced to $\overline{\text{RAS}}$(1)	10		10			
t_{FSC}	DSF Set-Up Time referenced to $\overline{\text{CAS}}$	0		0			
t_{CFH}	DSF Hold Time referenced to $\overline{\text{CAS}}$	10		10			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0		0			
t_{MH}	Write-Per-Bit Mask Data Hold Time	10		10			
t_{THS}	$\overline{\text{DT}}$ High Set-Up Time	0		0			
t_{THH}	$\overline{\text{DT}}$ High Hold Time	10		10			
t_{TLS}	$\overline{\text{DT}}$ Low Set-Up Time	0		0			
t_{TLH}	$\overline{\text{DT}}$ Low Hold Time	10	10000	10	10000	ns	
t_{RTH}	$\overline{\text{DT}}$ Low Hold Time referenced to $\overline{\text{RAS}}$ (Real Time Read Transfer)	55	10000	60	10000		
t_{ATH}	$\overline{\text{DT}}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	25		25			
t_{CTH}	$\overline{\text{DT}}$ Low Hold Time referenced to $\overline{\text{CAS}}$ (Real Time Read Transfer)	20		20			
t_{TRP}	$\overline{\text{DT}}$ to $\overline{\text{RAS}}$ Precharge Time	45		50			
t_{TP}	$\overline{\text{DT}}$ Precharge Time	10		15			
t_{RSD}	$\overline{\text{RAS}}$ to First SC Delay Time (Read Transfer)	60		70			
t_{ASD}	Column Address to First SC Delay Time (Read Transfer)	30		35			
t_{CSD}	$\overline{\text{CAS}}$ to First SC Delay Time (Read Transfer)	20		20			

SYMBOL	PARAMETER	-60		-70		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		5			
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	10		10			
t_{SRS}	Last SC to $\overline{RAS}$ Set-Up Time (Serial Input)	18		23			
t_{SCC}	SC Cycle Time	18		23			
t_{SC}	SC Pulse Width (SC High Time)	5		10			
t_{SCP}	SC Precharge Time (SC Low Time)	5		5			
t_{SCA}	Access Time from SC		15		20		
t_{SOH}	Serial Output Hold Time from SC	5		5			
t_{SEA}	Access Time from $\overline{SE}$		15		20		
t_{SE}	$\overline{SE}$ Pulse Width	10		20			
t_{SEP}	$\overline{SE}$ Precharge Time	10		20			
t_{SEZ}	Serial Output Buffer Turn-off Delay from $\overline{SE}$		15		15		9
t_{STS}	Split Transfer Set-Up Time	18		23			
t_{STH}	Split Transfer Hold Time	18		23			
t_{SQD}	SC-QSF Delay Time		15		20		
t_{TQD}	$\overline{DT}$-QSF Delay Time		15		20		
t_{CQD}	$\overline{CAS}$-QSF Delay Time		15		20		
t_{RQD}	$\overline{RAS}$-QSF Delay Time		60		70		
t_{RCDP}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time (Pipeline mode)	20	35	20	40		
t_{CSHP}	$\overline{CAS}$ Hold Time (Pipeline mode)	45		50		ns	
t_{RACP}	Access Time from $\overline{RAS}$ (Pipeline mode)		85		90		
t_{CAC1}	Access Time from $\overline{CAS}$ (1) (Pipeline mode)		15		20		
t_{CAC2}	Access Time from $\overline{CAS}$ (2) (Pipeline mode)		50		50		
t_{CASP}	$\overline{CAS}$ Pulse Width (Pipeline mode)	10		10			
t_{CPP}	$\overline{CAS}$ Precharge Time (Pipeline mode)	10		10			
t_{PCP}	Fast Page Mode Cycle Time (Pipeline mode)	30		30			
t_{COH}	$\overline{CAS}$ Hold Time referenced to $\overline{OE}$ (Pipeline mode)	5		5			
t_{RSH1}	$\overline{RAS}$ Hold Time (1) (Pipeline mode)	20		20			
t_{RSH2}	$\overline{RAS}$ Hold Time (2) (Pipeline mode)	50		50			
t_{CWLP}	Write Command to $\overline{CAS}$ lead Time (Pipeline mode)	10		10			
t_{CWP}	$\overline{WE}$ to $\overline{CAS}$ Delay Time (Pipeline mode)	30		30			
t_{OFFP}	Output Buffer Turn - off Delay from $\overline{RAS}$ (Pipeline mode)	0	15	0	15		9, 15
t_{OEP}	$\overline{OE}$ High width	10		10			16
t_{ECS}	$\overline{CAS}$ High to $\overline{OE}$ Low (Fast Page mode)	10		10			16
t_{ECH}	$\overline{OE}$ High to $\overline{CAS}$ Low (Fast Page mode)	10		10			16
t_{TSAA}	Boundary TAP SC Set-up time	0		0			
t_{SATT}	SRT inhibit after Boundary SC	36		46			

A.C. MEASUREMENT CONDITION

RAM Output Reference Level	2.0V/0.8V
SAM Output Reference Level	2.0V/0.8V
RAM Output Load	1 TTL and 50PF
SAM Output Load	1 TTL and 30PF
Input Reference Level	2.2V/1.0V.

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltage are referenced to V_{SS}.

3. These parameters depend on cycle rate.

4. These parameters depend on output loading. Specified values are obtained with the output open. (I out=ØmA)

5. Address can be changed once or less while $\overline{RAS}$=V_{IL}. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. After power-up, a pause of 200 µseconds minimum is required with $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ held "high". After the pause, a minimum of 8 CBR dummy cycles must be required.

7. AC measurements assume t_T 5ns. (Between $V_{IH\ (min)}$ and $V_{IL\ (max)}$)

8. $t_{OFF\ (max.)}$, $t_{OEZ\ (max.)}$, $t_{OFFP\ (max.)}$, $t_{WPS\ (max.)}$, $t_{WEZ\ (max.)}$, and $t_{SEZ\ (max.)}$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.

9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.

10. These parameters are referenced to $\overline{CASL}$ / $\overline{CASU}$ leading edge of early write cycles and to $\overline{WB}$ / $\overline{WE}$ leading edge in $\overline{OE}$-controlled write cycle and read-modify-write cycles.

11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS\ (min.)}$, the cycle is an early write cycles and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geq t_{RWID\ (min.)}$, $t_{CWD} \geq t_{CWD\ (min.)}$ and $t_{AWD} \geq t_{AWD\ (min.)}$ the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

12. Operation within the $t_{RCD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

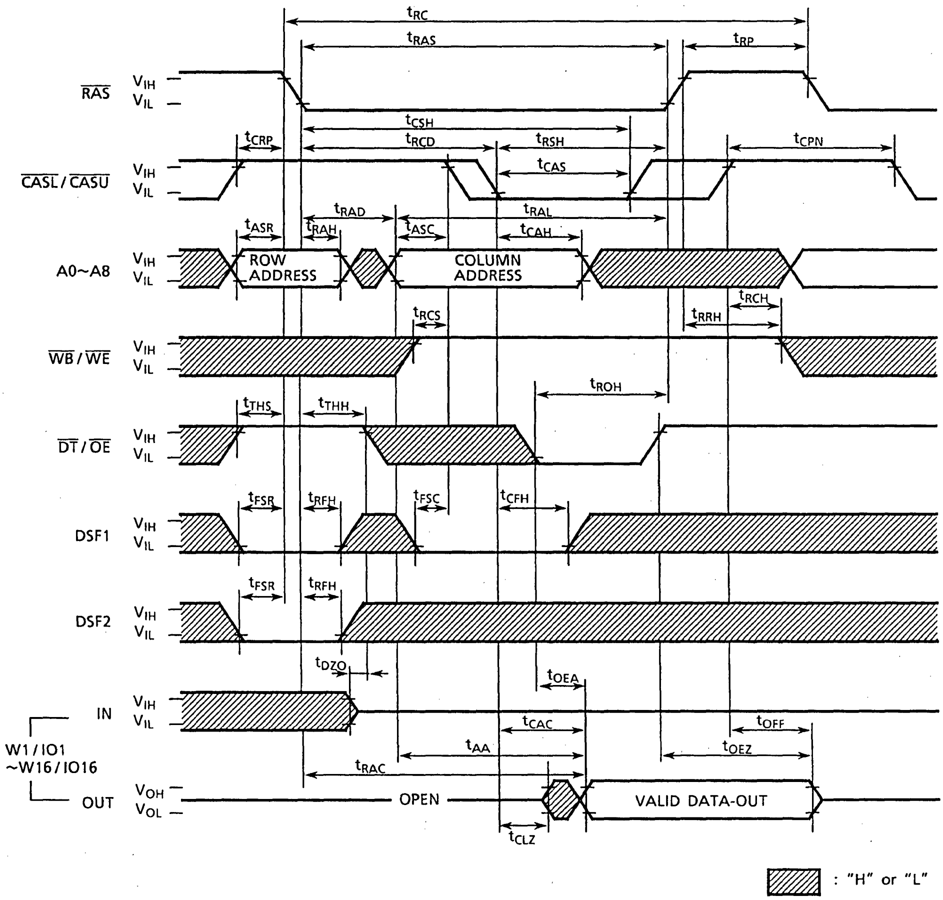
13. Operation within the $t_{RAD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

14. t_{OFF}, t_{OFFP} timing is specified from either $\overline{RAS}$ or $\overline{CASL}$ / $\overline{CASU}$ rising edge, whichever occurs last.

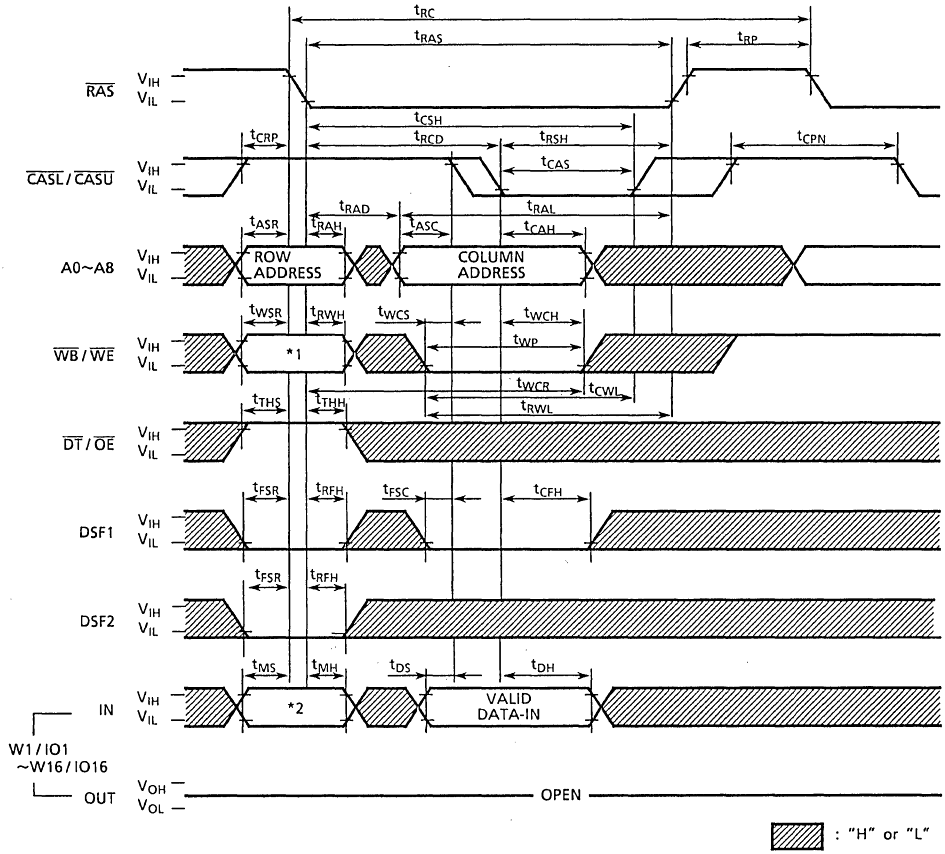
15. TC524265 only

TIMING WAVEFORM

READ CYCLE *Note 1, 2, 3



WRITE CYCLE (EARLY WRITE) *Note 1, 2, 4

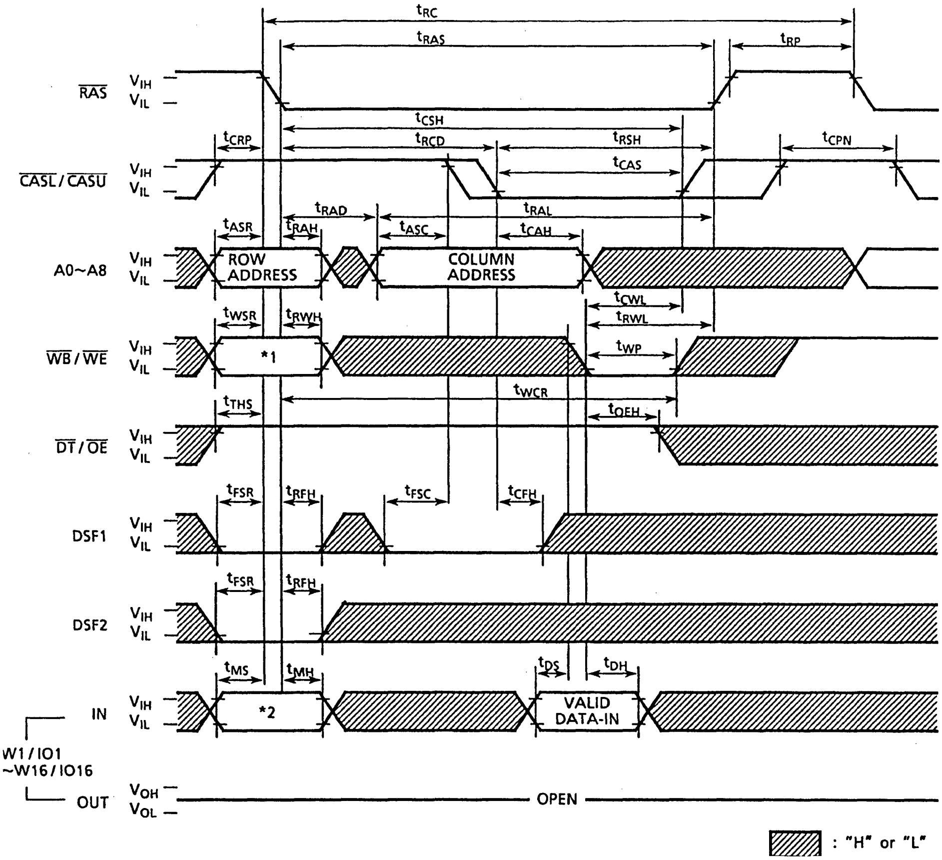


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0 :Write Disable
1 :Write Enable

Don't care :'1' or '0'

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE) *Note 1, 2, 4

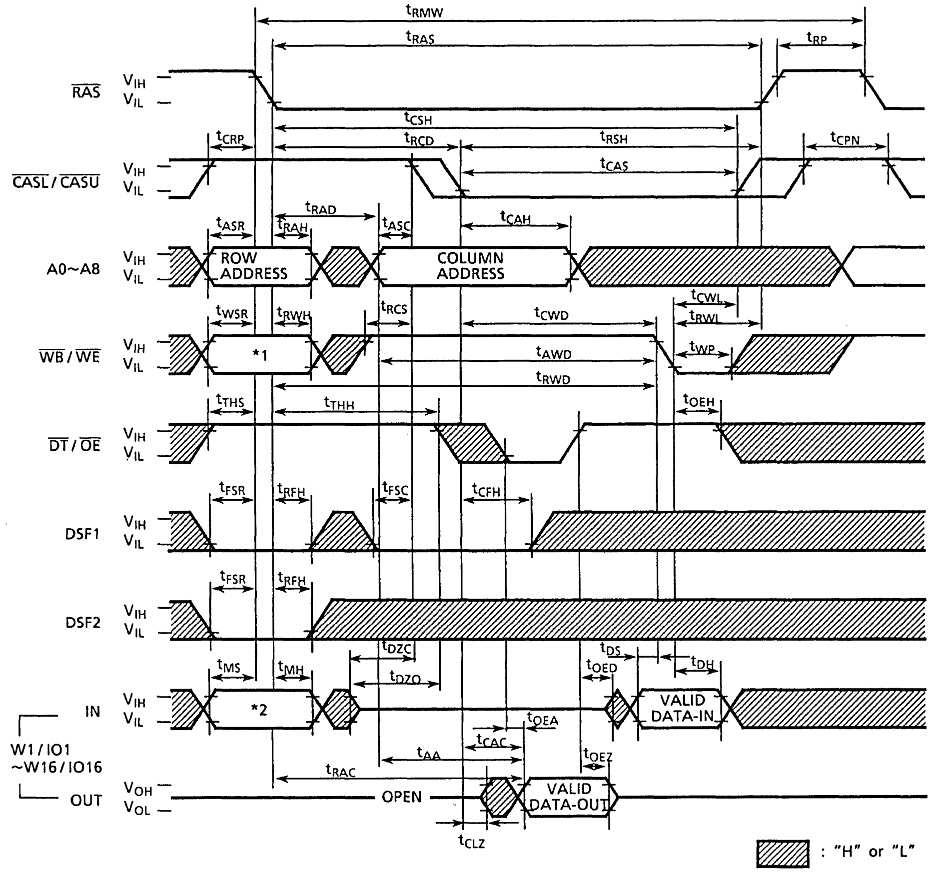


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0 :Write Disable
1 :Write Enable

Don't care :'1' or '0'

READ - MODIFY - WRITE CYCLE *Note 1, 2, 3, 4

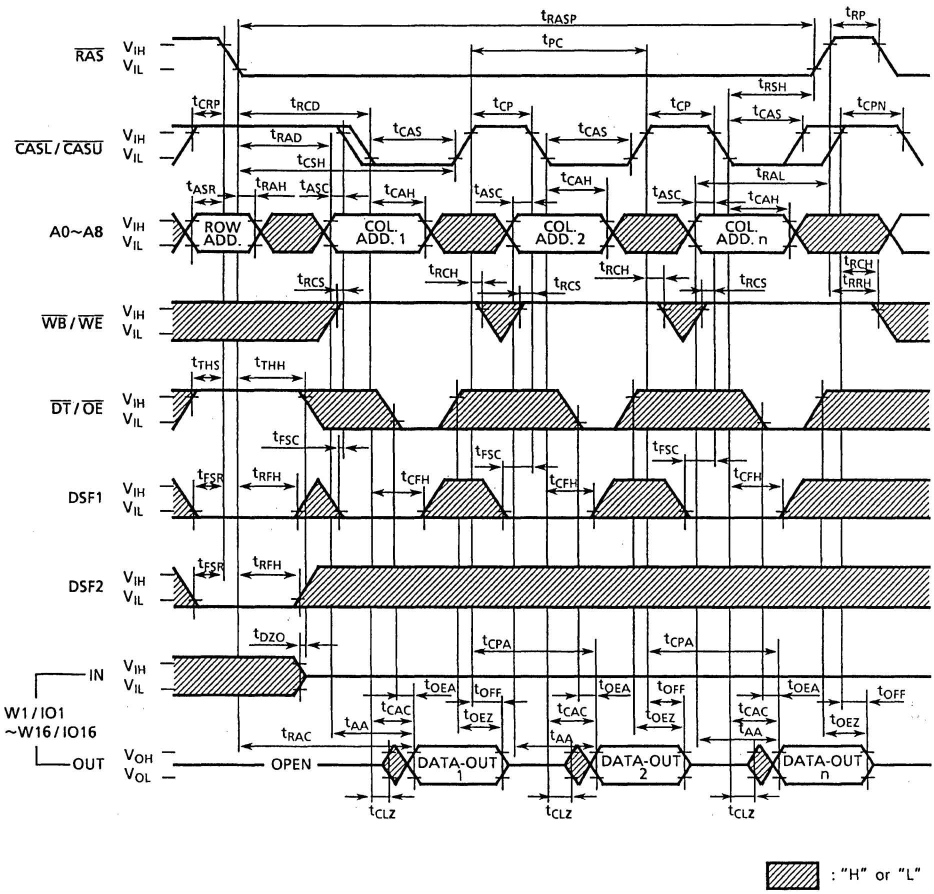


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

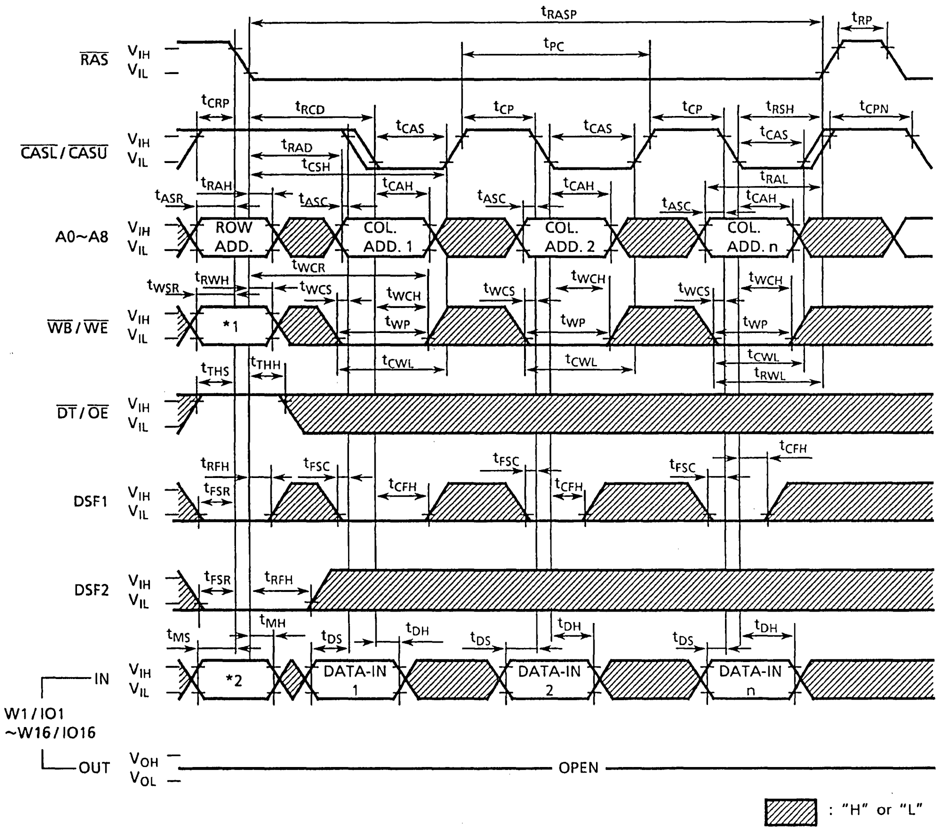
WM1 data 0 :Write Disable
1 :Write Enable

Don't care :'1' or '0'

FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE) *Note 1, 2, 4

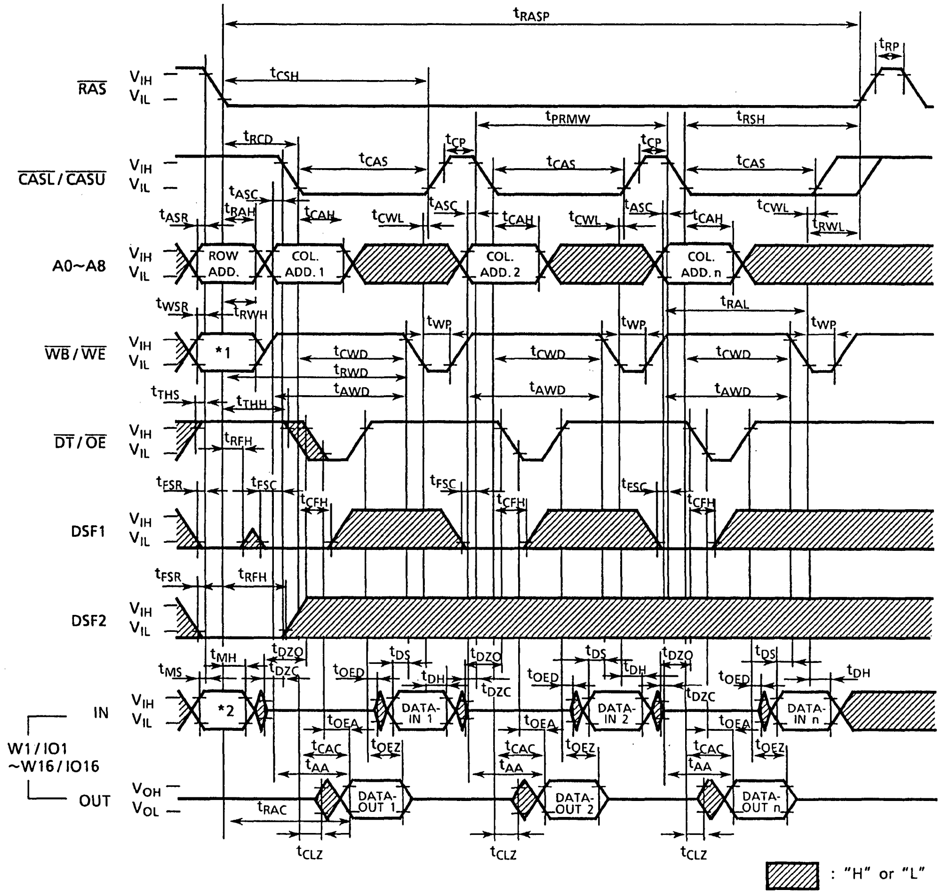


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0 :Write Disable
1 :Write Enable

Don't care :'1' or '0'

FAST PAGE MODE READ - MODIFY - WRITE CYCLE*Note 1, 2, 3, 4

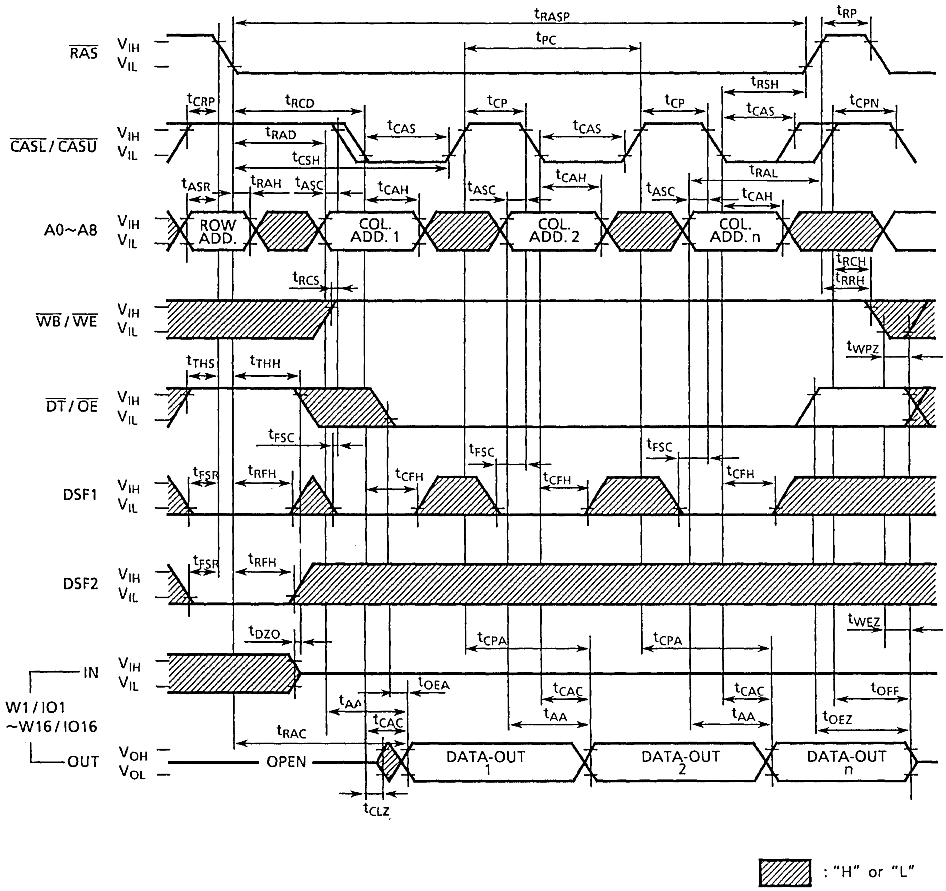


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

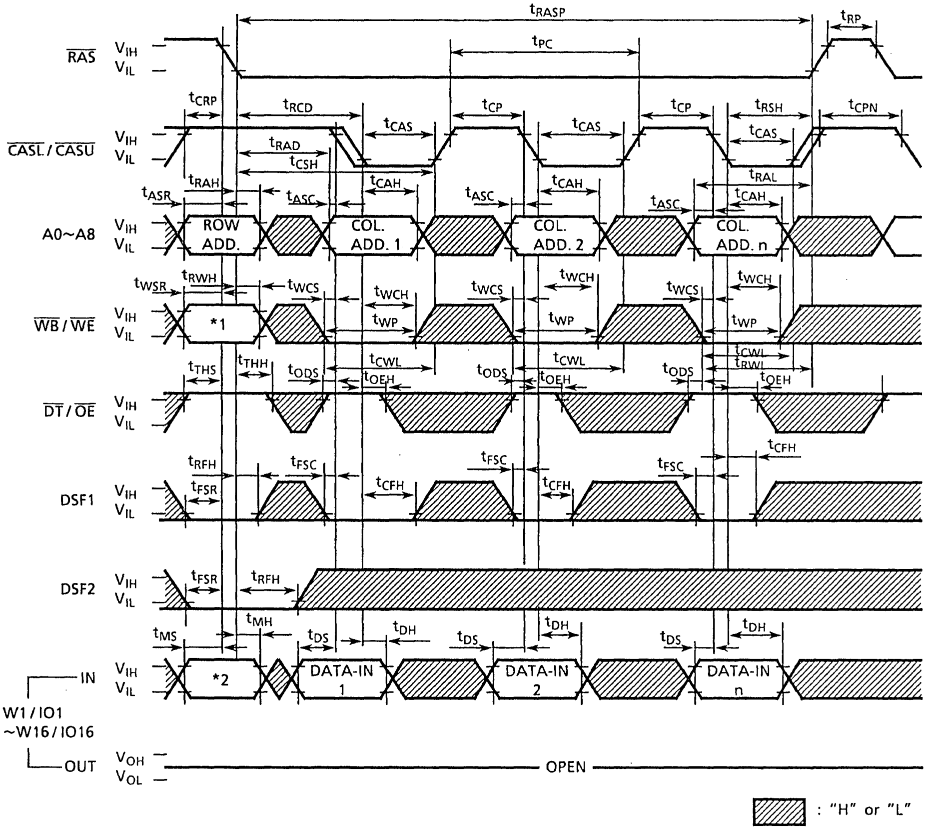
WM1 data 0 :Write Disable
1 :Write Enable

Don't care :'1' or '0'

EXTENDED FAST PAGE MODE READ CYCLE (TC524265 only)



EXTENDED FAST PAGE MODE WRITE CYCLE (EARLY WRITE) (TC524265 only)

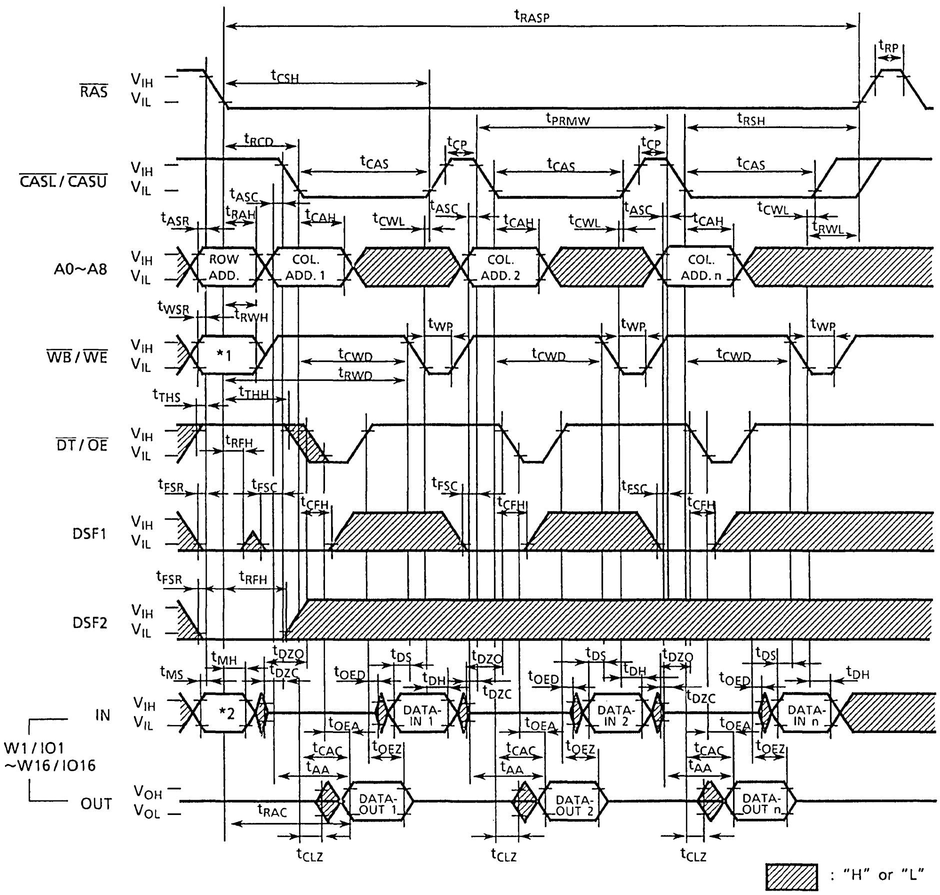


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0 :Write Disable
1 :Write Enable

Don't care :'1' or '0'

EXTENDED FAST PAGE MODE READ - MODIFY - WRITE CYCLE (TC524265 only)

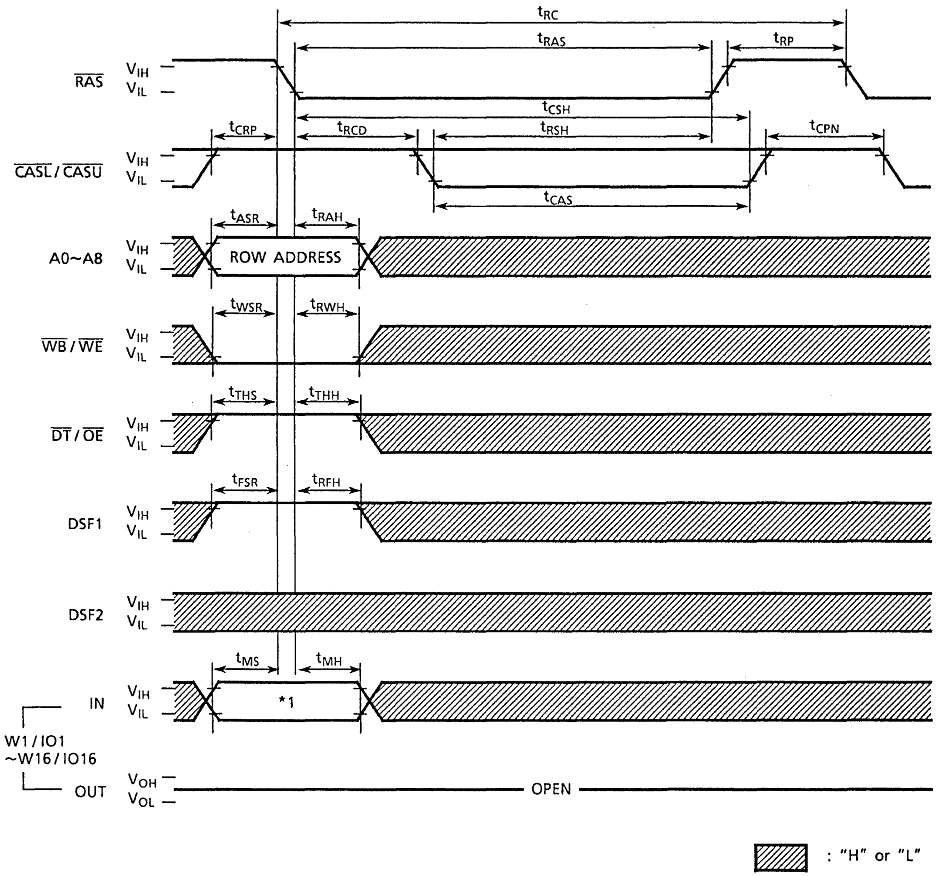


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0 :Write Disable
1 :Write Enable

Don't care :'1' or '0'

FLASH WRITE CYCLE

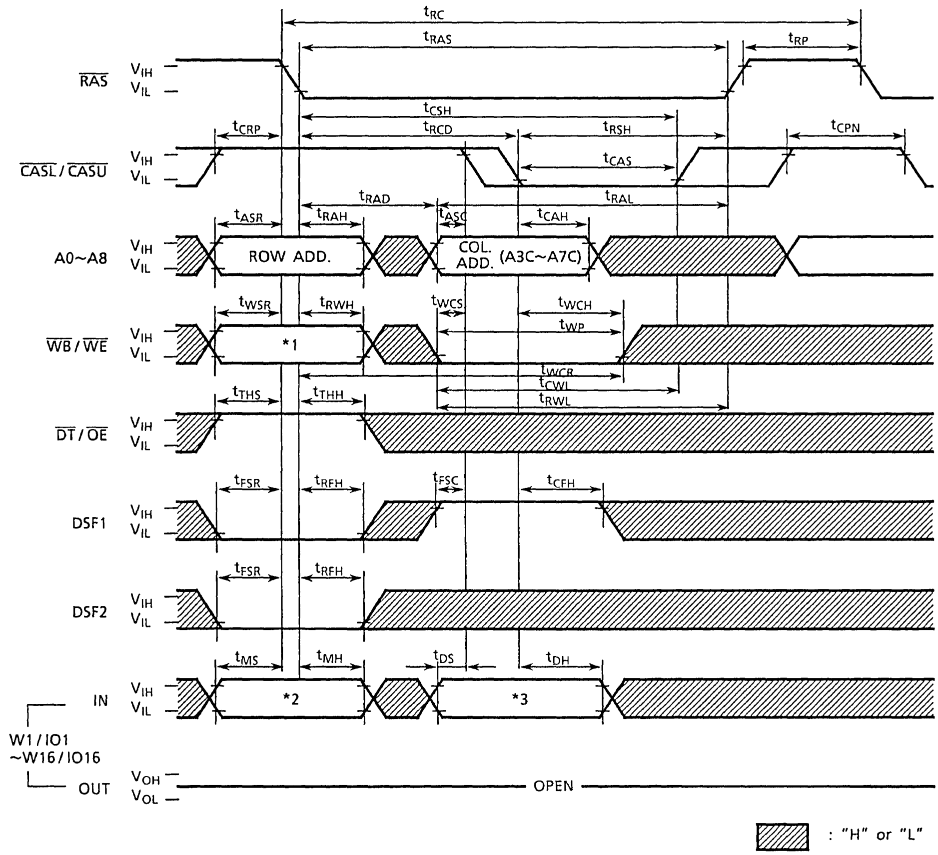


Mask Mode	*2
New Mask Mode	WM1 data
Old Mask Mode	Don't care

WM1 data 0 :Write Disable
1 :Write Enable

Don't care :'1' or '0'

BLOCK WRITE CYCLE (EARLY WRITE) *NOTE 1, 2, 4



Mask Mode	*1	*2
No Mask Mode	1	Don't care
New Mask Mode	0	WM1 data
Old Mask Mode	0	Don't care

WM1 data 0 :Write Disable
1 :Write Enable
Don't care :'1' or '0'

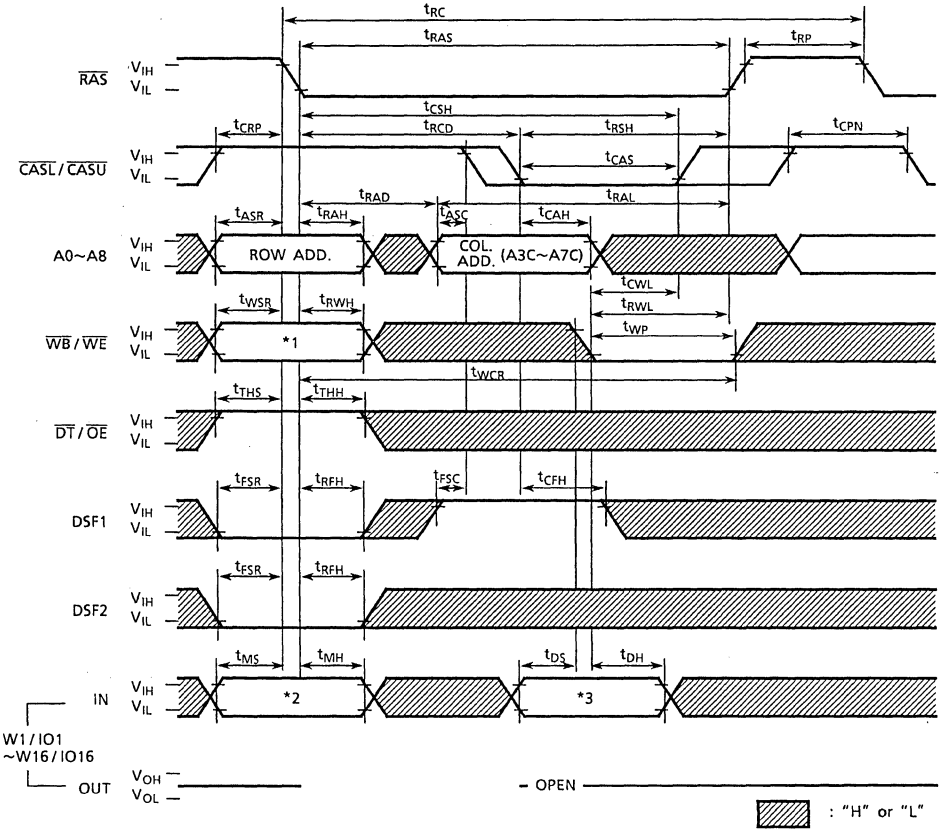
*3) COLUMN SELECT

Lower Byte
- W1/IO1 -Column 0 (A2C = 0, A1C = 0, A0C = 0)
- W2/IO2 -Column 1 (A2C = 0, A1C = 0, A0C = 1)
- W3/IO3 -Column 2 (A2C = 0, A1C = 1, A0C = 0)
- W4/IO4 -Column 3 (A2C = 0, A1C = 1, A0C = 1)
- W5/IO5 -Column 4 (A2C = 1, A1C = 0, A0C = 0)
- W6/IO6 -Column 5 (A2C = 1, A1C = 0, A0C = 1)
- W7/IO7 -Column 6 (A2C = 1, A1C = 1, A0C = 0)
- W8/IO8 -Column 7 (A2C = 1, A1C = 1, A0C = 1)

Upper Byte
- W9/IO9 -Column 0 (A2C = 0, A1C = 0, A0C = 0)
- W10/IO10 -Column 1 (A2C = 0, A1C = 0, A0C = 1)
- W11/IO11 -Column 2 (A2C = 0, A1C = 1, A0C = 0)
- W12/IO12 -Column 3 (A2C = 0, A1C = 1, A0C = 1)
- W13/IO13 -Column 4 (A2C = 1, A1C = 0, A0C = 0)
- W14/IO14 -Column 5 (A2C = 1, A1C = 0, A0C = 1)
- W15/IO15 -Column 6 (A2C = 1, A1C = 1, A0C = 0)
- W16/IO16 -Column 7 (A2C = 1, A1C = 1, A0C = 1)

Wn/IOn
= 0 : Disable
= 1 : Enable

BLOCK WRITE CYCLE (DELAYED WRITE *NOTE 1, 2, 4



Mask Mode	*1	*2
No Mask Mode	1	Don't care
New Mask Mode	0	WM1 data
Old Mask Mode	0	Don't care

WM1 data 0 :Write Disable
1 :Write Enable
Don't care :'1' or '0'

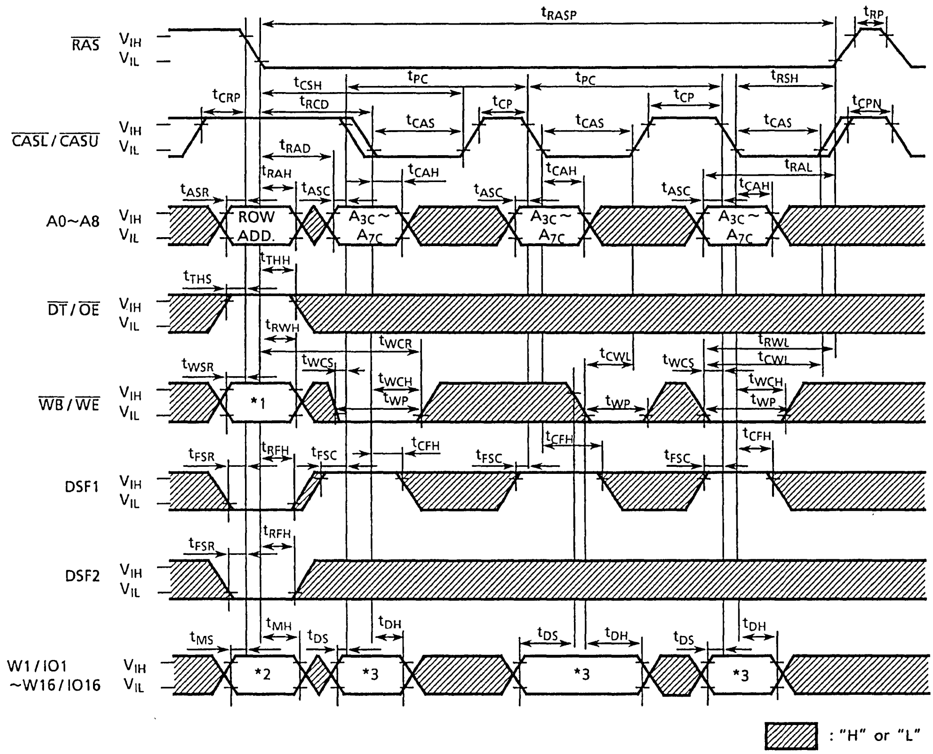
*3) COLUMN SELECT

Lower Byte
- W1/IO1 -Column 0 (A2C = 0, A1C = 0, A0C = 0)
- W2/IO2 -Column 1 (A2C = 0, A1C = 0, A0C = 1)
- W3/IO3 -Column 2 (A2C = 0, A1C = 1, A0C = 0)
- W4/IO4 -Column 3 (A2C = 0, A1C = 1, A0C = 1)
- W5/IO5 -Column 4 (A2C = 1, A1C = 0, A0C = 0)
- W6/IO6 -Column 5 (A2C = 1, A1C = 0, A0C = 1)
- W7/IO7 -Column 6 (A2C = 1, A1C = 1, A0C = 0)
- W8/IO8 -Column 7 (A2C = 1, A1C = 1, A0C = 1)

Upper Byte
- W9/IO9 -Column 0 (A2C = 0, A1C = 0, A0C = 0)
- W10/IO10 -Column 1 (A2C = 0, A1C = 0, A0C = 1)
- W11/IO11 -Column 2 (A2C = 0, A1C = 1, A0C = 0)
- W12/IO12 -Column 3 (A2C = 0, A1C = 1, A0C = 1)
- W13/IO13 -Column 4 (A2C = 1, A1C = 0, A0C = 0)
- W14/IO14 -Column 5 (A2C = 1, A1C = 0, A0C = 1)
- W15/IO15 -Column 6 (A2C = 1, A1C = 1, A0C = 0)
- W16/IO16 -Column 7 (A2C = 1, A1C = 1, A0C = 1)

Wn/IOn
= 0 : Disable
= 1 : Enable

FAST PAGE MODE BLOCK WRITE CYCLE *NOTE 1, 2, 4



Mask Mode	*1	*2
No Mask Mode	1	Don't care
New Mask Mode	0	WM1 data
Old Mask Mode	0	Don't care

WM1 data 0 :Write Disable
1 :Write Enable
Don't care :'1' or '0'

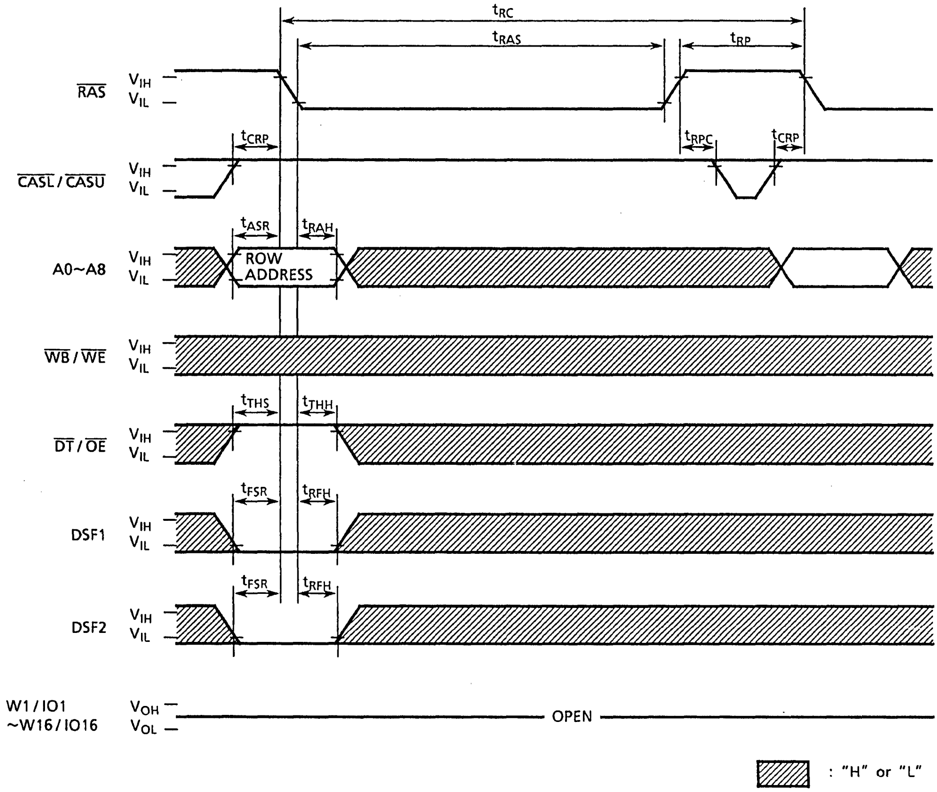
*3) COLUMN SELECT

Lower Byte
- W1/IO1 -Column 0 (A2C = 0, A1C = 0, A0C = 0)
- W2/IO2 -Column 1 (A2C = 0, A1C = 0, A0C = 1)
- W3/IO3 -Column 2 (A2C = 0, A1C = 1, A0C = 0)
- W4/IO4 -Column 3 (A2C = 0, A1C = 1, A0C = 1)
- W5/IO5 -Column 4 (A2C = 1, A1C = 0, A0C = 0)
- W6/IO6 -Column 5 (A2C = 1, A1C = 0, A0C = 1)
- W7/IO7 -Column 6 (A2C = 1, A1C = 1, A0C = 0)
- W8/IO8 -Column 7 (A2C = 1, A1C = 1, A0C = 1)

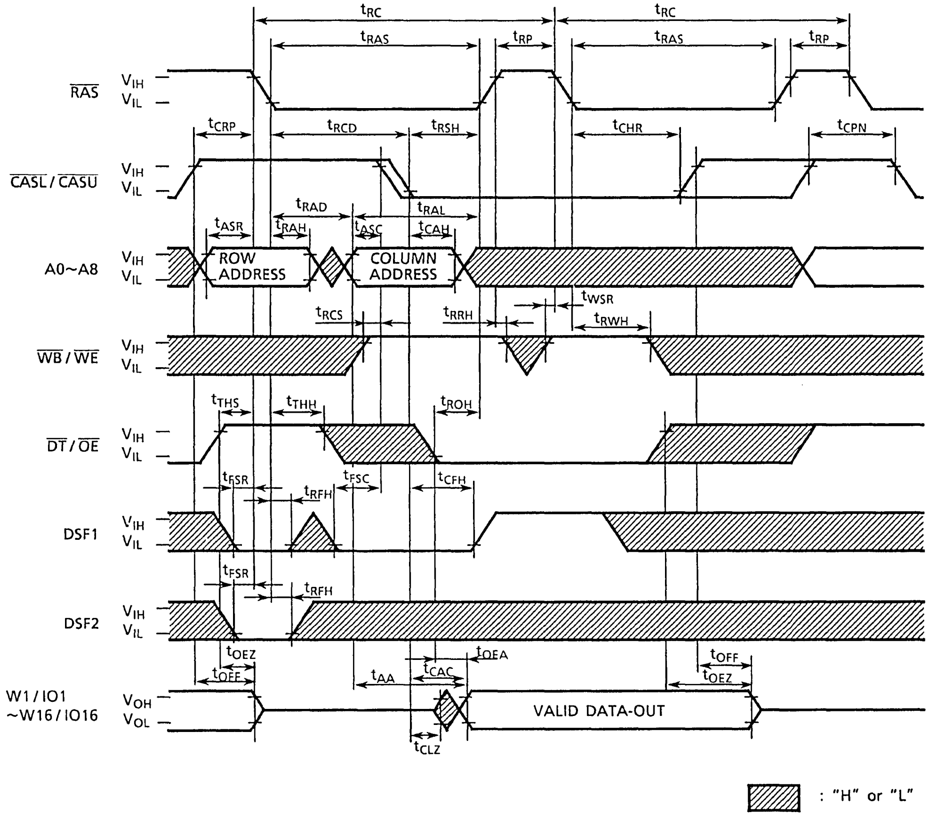
Upper Byte
- W9/IO9 -Column 0 (A2C = 0, A1C = 0, A0C = 0)
- W10/IO10 -Column 1 (A2C = 0, A1C = 0, A0C = 1)
- W11/IO11 -Column 2 (A2C = 0, A1C = 1, A0C = 0)
- W12/IO12 -Column 3 (A2C = 0, A1C = 1, A0C = 1)
- W13/IO13 -Column 4 (A2C = 1, A1C = 0, A0C = 0)
- W14/IO14 -Column 5 (A2C = 1, A1C = 0, A0C = 1)
- W15/IO15 -Column 6 (A2C = 1, A1C = 1, A0C = 0)
- W16/IO16 -Column 7 (A2C = 1, A1C = 1, A0C = 1)

Wn/IOn
= 0 : Disable
= 1 : Enable

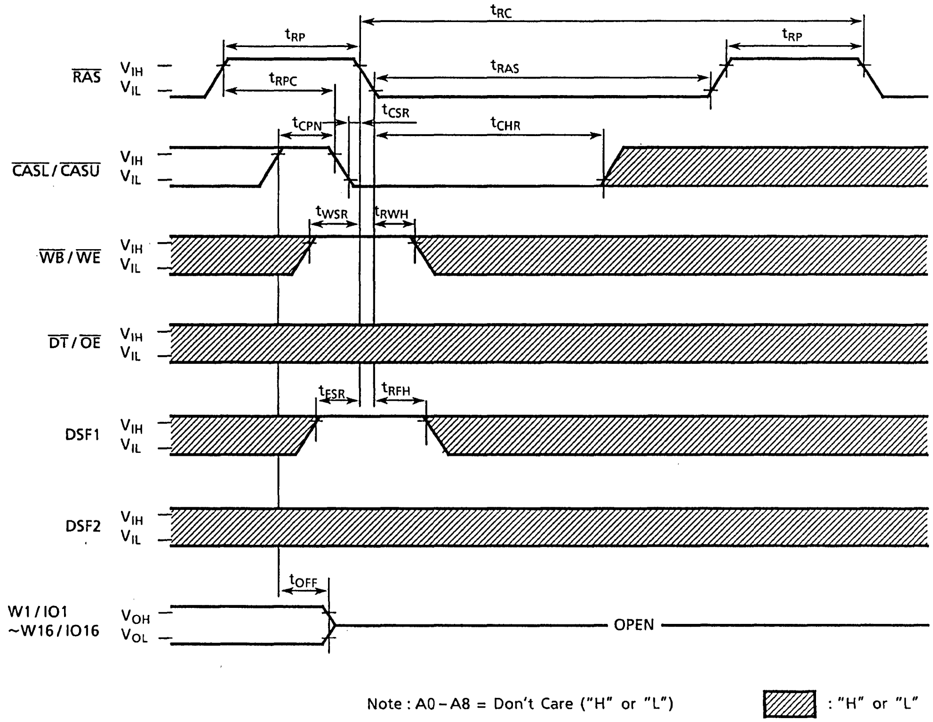
$\overline{RAS}$ ONLY REFRESH CYCLE



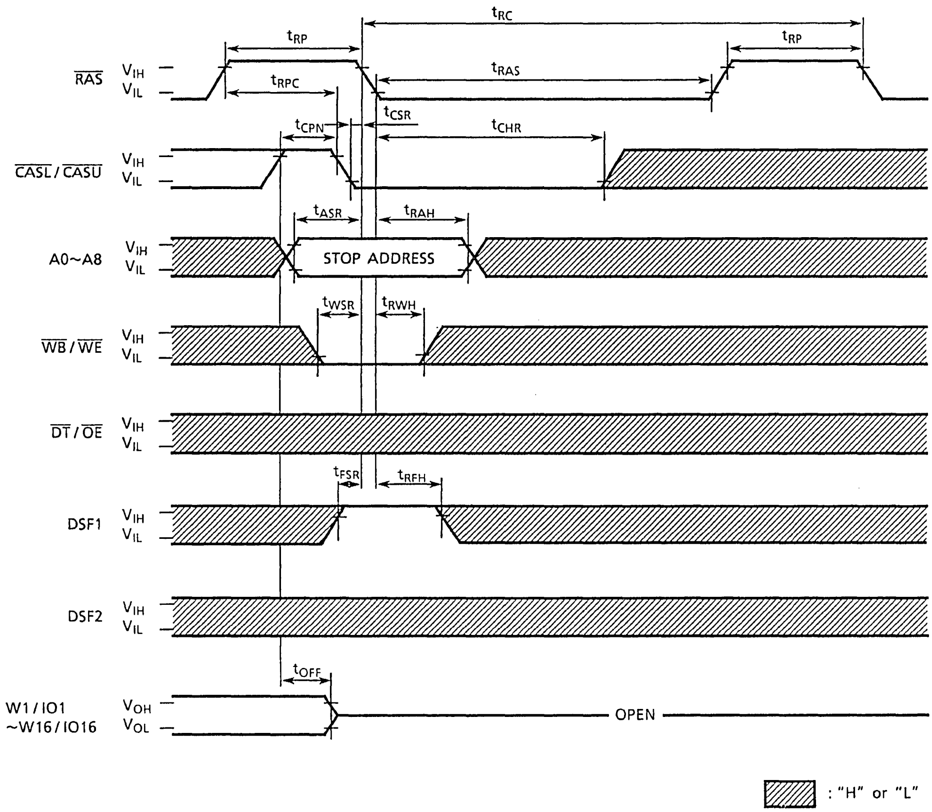
HIDDEN REFRESH CYCLE



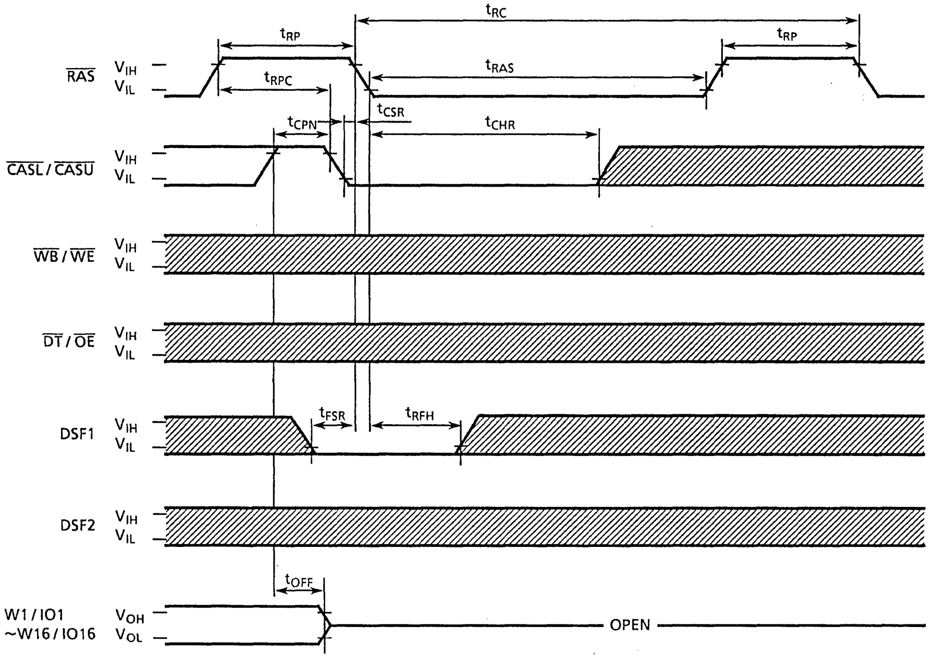
CBR AUTO REFRESH CYCLE



CBR AUTO REFRESH & STOP REGISTER SET CYCLE



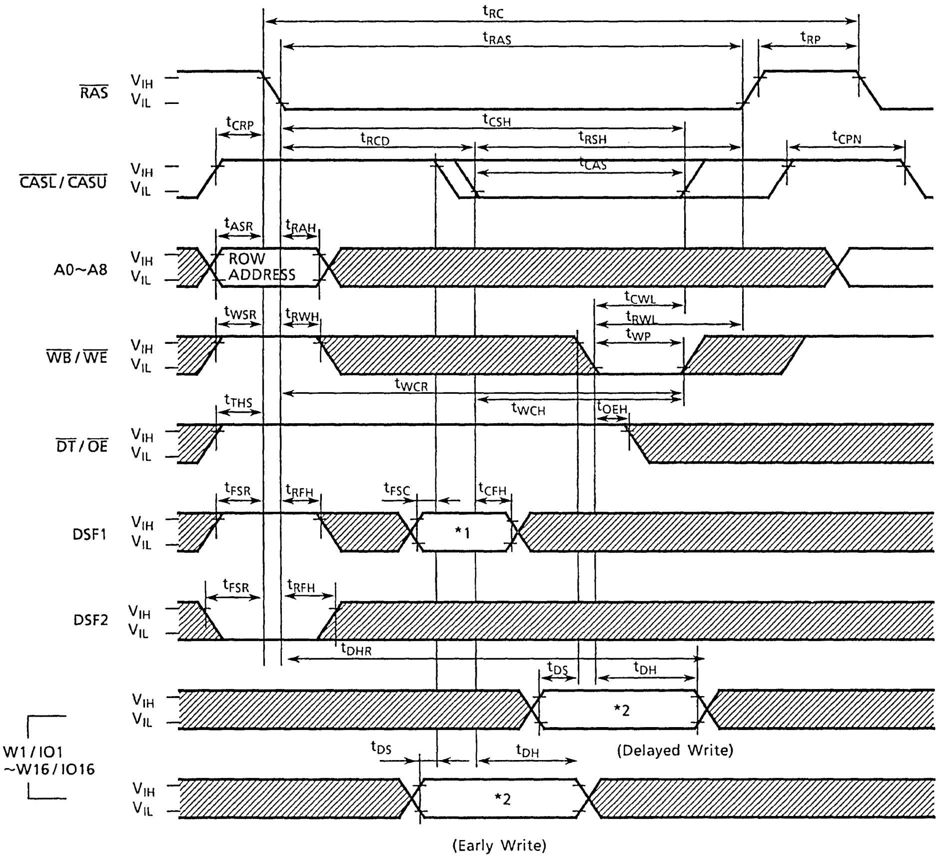
CBR AUTO REFRESH & RESET CYCLE



Note : A0 – A8 = Don't Care ("H" or "L")

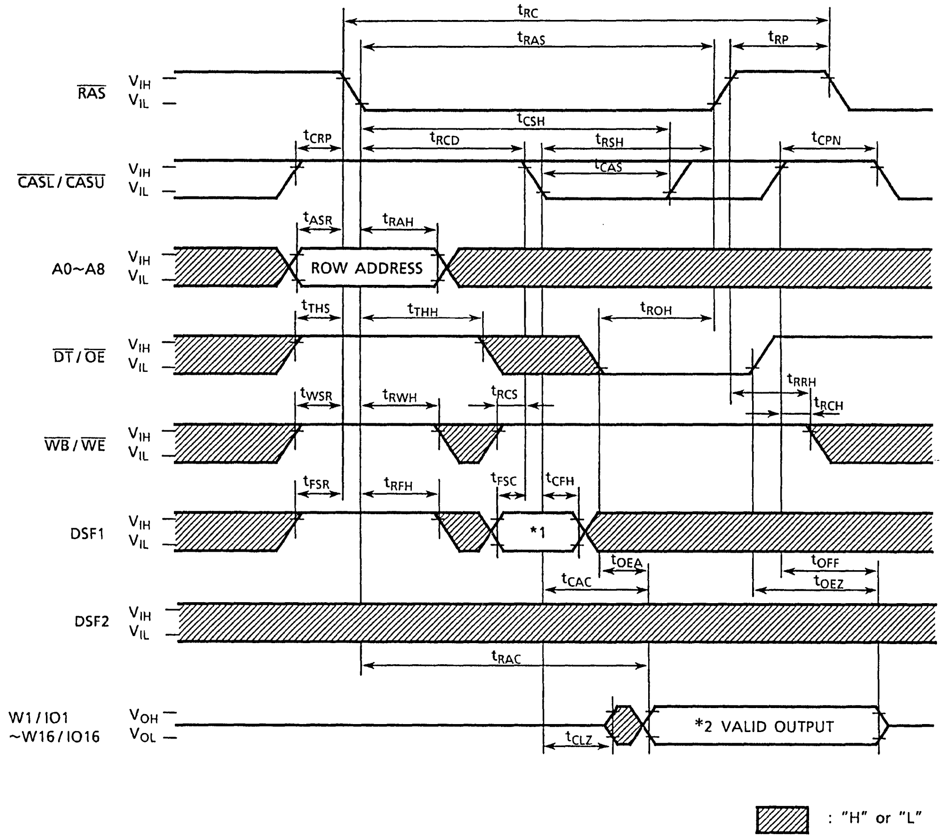
: "H" or "L"

LOAD MASK/COLOR REGISTER CYCLE *Note 5



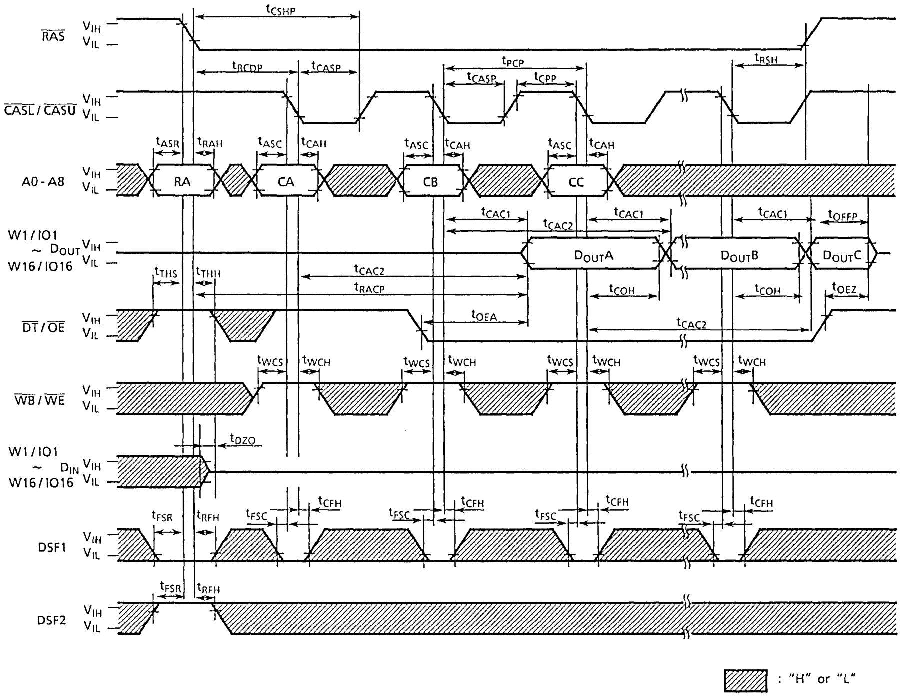
$\overline{CASL}$	$\overline{CASU}$	*1	*2	Cycle
0	0	0	Mask data	Load Mask Register
		1	Color data	Load Color Register
0	1	0	Mask data	Load Mask Register (Lower Byte)
		1	Color data	Load Color Register (Lower Byte)
1	0	0	Mask data	Load Mask Register (Upper Byte)
		1	Color data	Load Color Register (Upper Byte)

READ MASK / COLOR REGISTER CYCLE

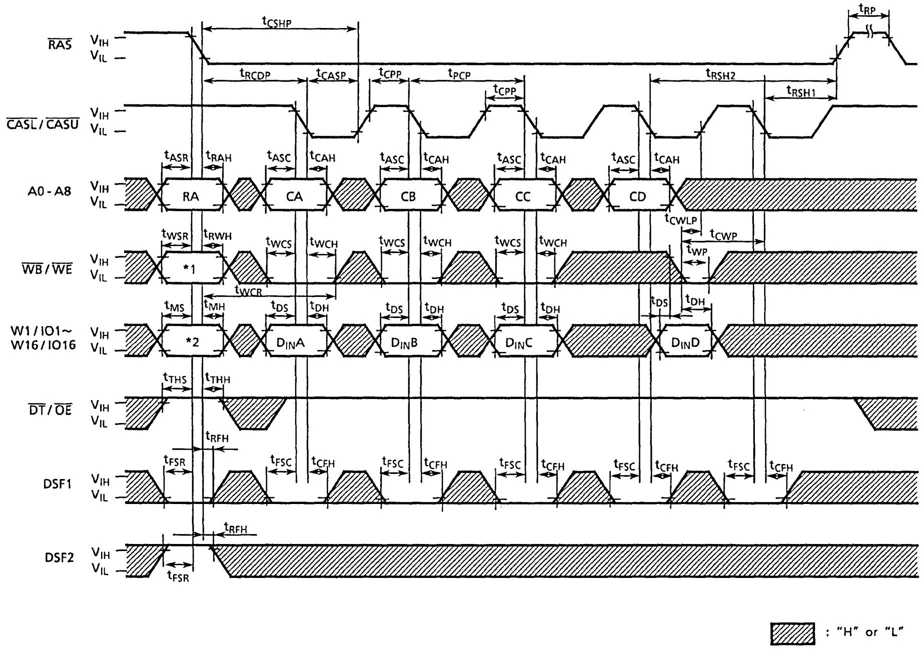


CASL	CASU	*1	*2	Cycle
0	0	0	Mask data	Load Mask Register
		1	Color data	Load Color Register
0	1	0	Masky data	Load Mask Register (Lower Byte)
		1	Color data	Load Color Register (Lower Byte)
1	0	0	Mask data	Load Mask Register (Upper Byte)
		1	Color data	Load Color Register (Upper Byte)

PIPELINED FAST PAGE READ CYCLE *Note 6



PIPELINED FAST PAGE WRITE CYCLE *Note 6

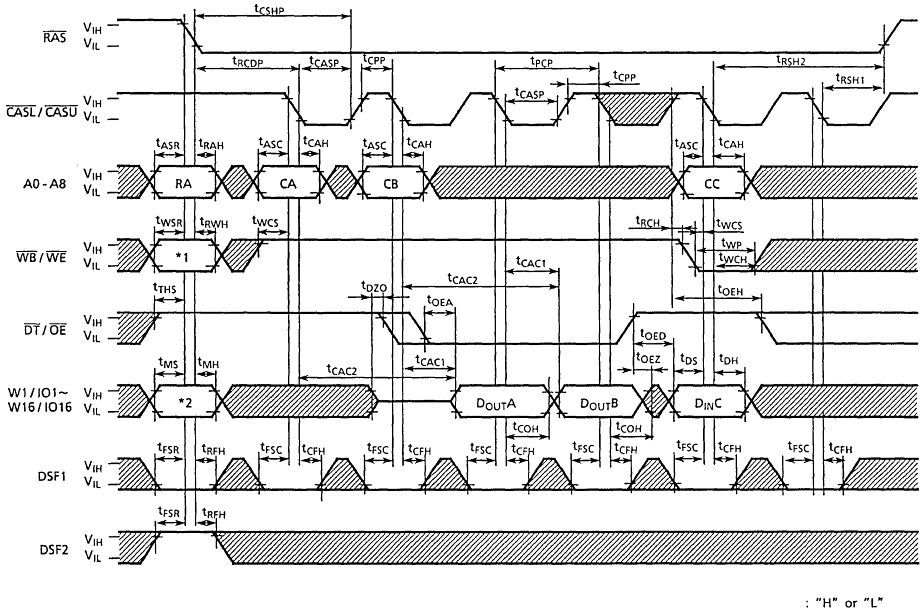


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0 :Write Disable
1 :Write Enable

Don't care :'1' or '0'

PIPELINED FAST PAGE READ - WRITE CYCLE

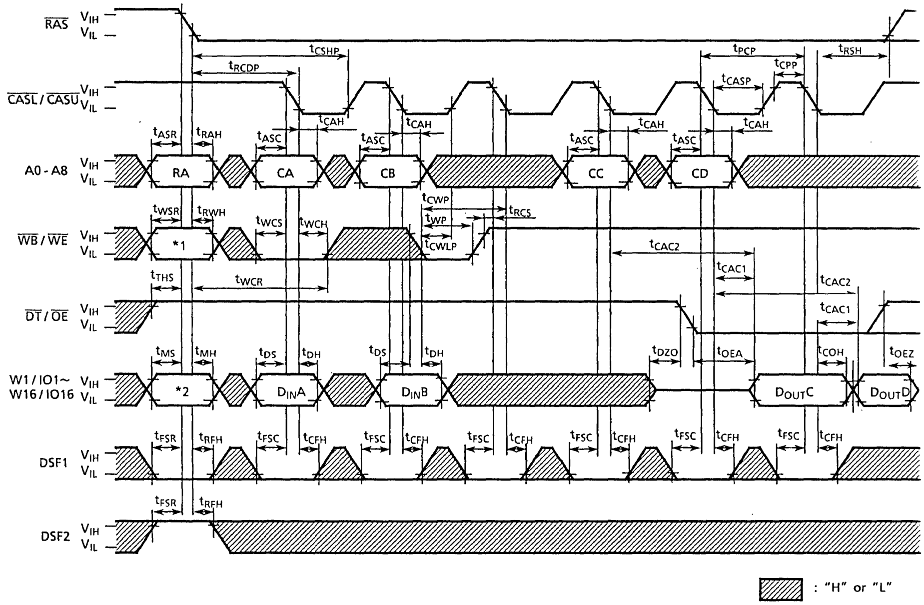


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0 :Write Disable
1 :Write Enable

Don't care 0 :'1' or '0'

PIPELINED FAST PAGE WRITE - READ CYCLE

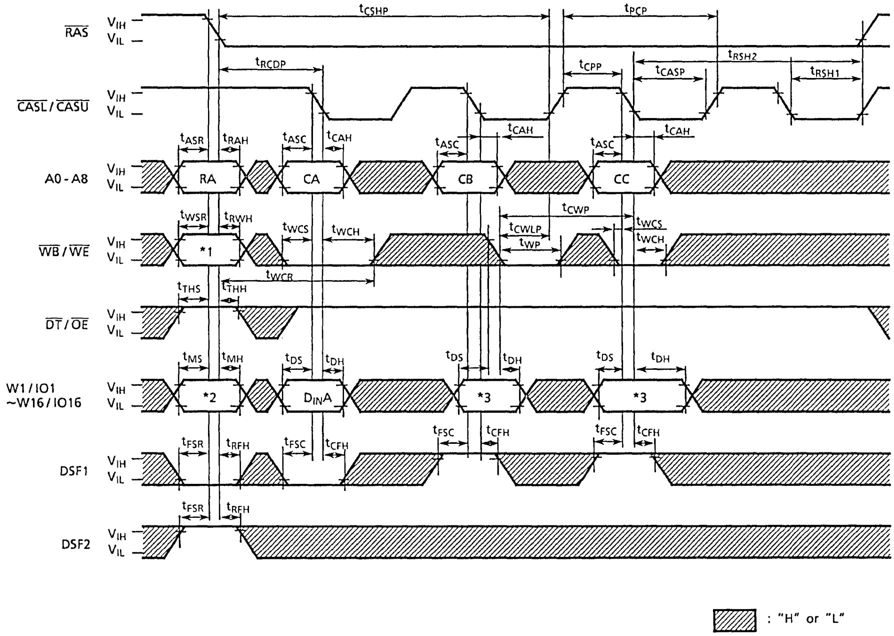


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0 :Write Disable
1 :Write Enable

Don't care :'1' or '0'

PIPELINED FAST PAGE WRITE - BLOCK WRITE CYCLE



Mask Mode	*1	*2
No Mask Mode	1	Don't care
New Mask Mode	0	WM1 data
Old Mask Mode	0	Don't care

WM1 data 0 :Write Disable
1 :Write Enable
Don't care :'1' or '0'

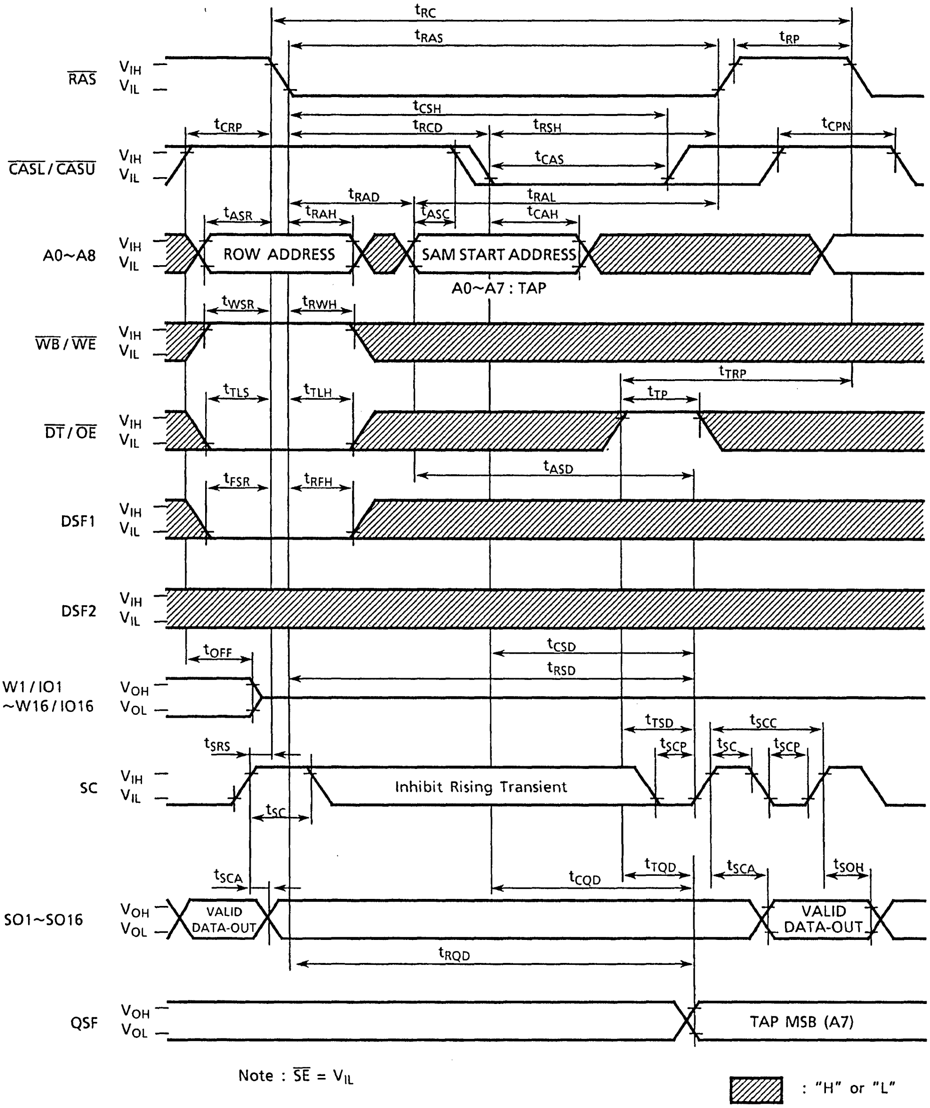
*3) COLUMN SELECT

Lower Byte
- W1/IO1 -Column 0 (A2C = 0, A1C = 0, A0C = 0)
- W2/IO2 -Column 1 (A2C = 0, A1C = 0, A0C = 1)
- W3/IO3 -Column 2 (A2C = 0, A1C = 1, A0C = 0)
- W4/IO4 -Column 3 (A2C = 0, A1C = 1, A0C = 1)
- W5/IO5 -Column 4 (A2C = 1, A1C = 0, A0C = 0)
- W6/IO6 -Column 5 (A2C = 1, A1C = 0, A0C = 1)
- W7/IO7 -Column 6 (A2C = 1, A1C = 1, A0C = 0)
- W8/IO8 -Column 7 (A2C = 1, A1C = 1, A0C = 1)

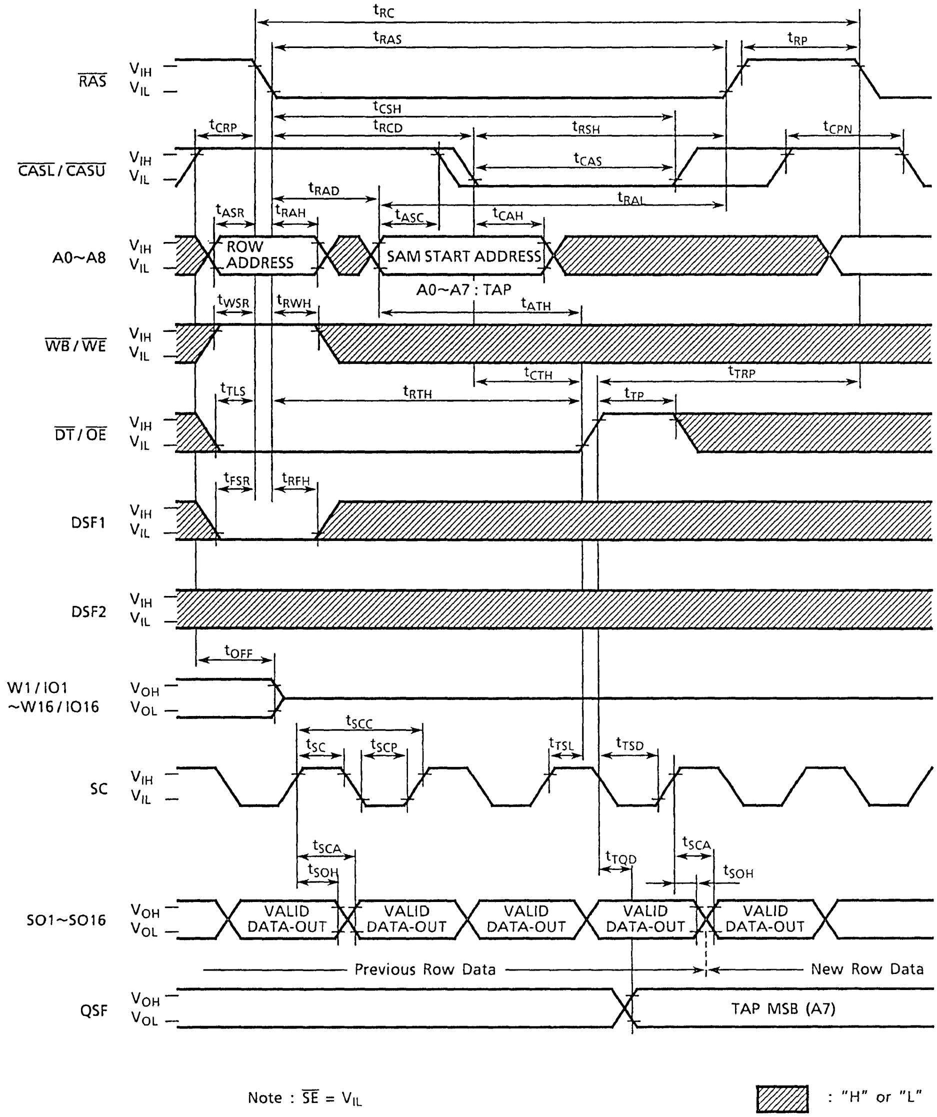
Upper Byte
- W9/IO9 -Column 0 (A2C = 0, A1C = 0, A0C = 0)
- W10/IO10 -Column 1 (A2C = 0, A1C = 0, A0C = 1)
- W11/IO11 -Column 2 (A2C = 0, A1C = 1, A0C = 0)
- W12/IO12 -Column 3 (A2C = 0, A1C = 1, A0C = 1)
- W13/IO13 -Column 4 (A2C = 1, A1C = 0, A0C = 0)
- W14/IO14 -Column 5 (A2C = 1, A1C = 0, A0C = 1)
- W15/IO15 -Column 6 (A2C = 1, A1C = 1, A0C = 0)
- W16/IO16 -Column 7 (A2C = 1, A1C = 1, A0C = 1)

Wn/IOn
= 0 : Disable
= 1 : Enable

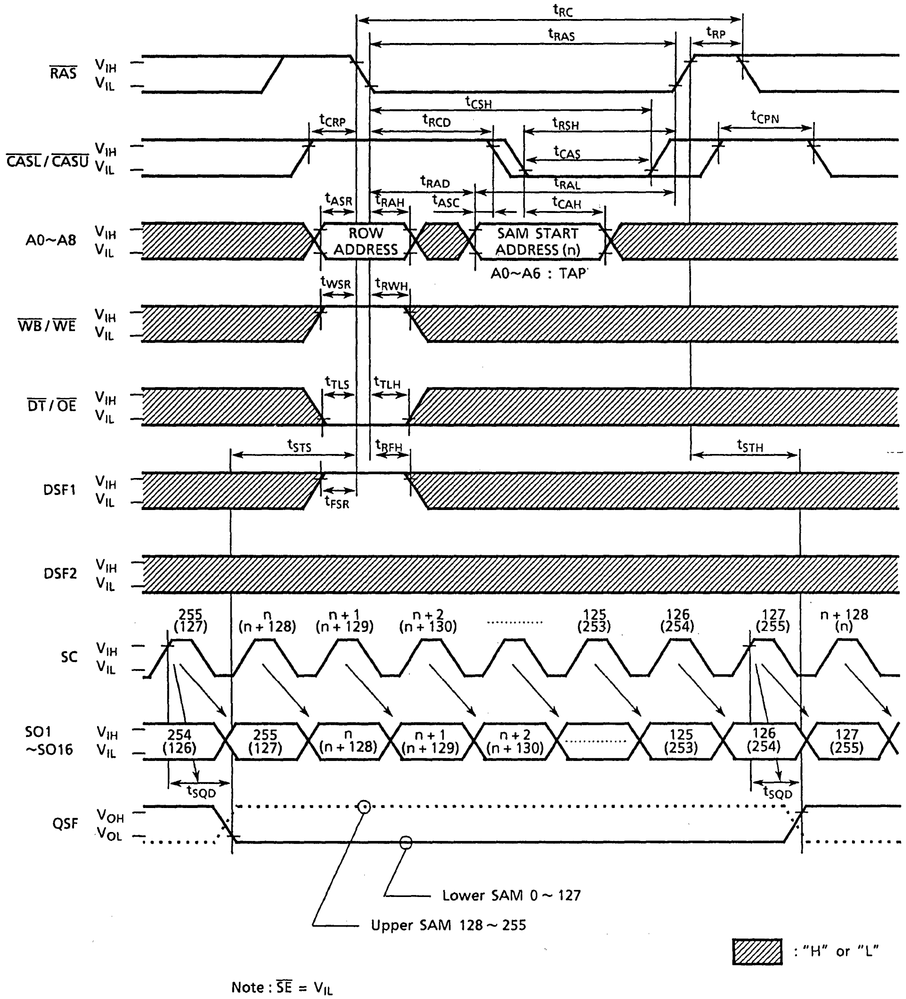
READ TRANSFER CYCLE



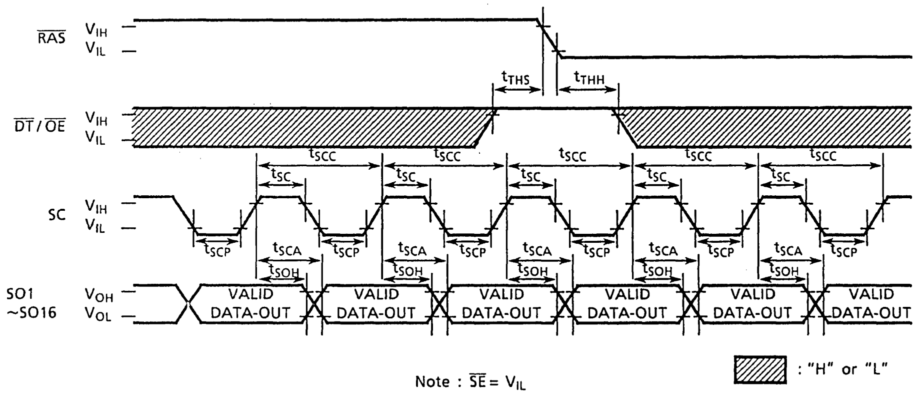
REAL TIME READ TRANSFER CYCLE



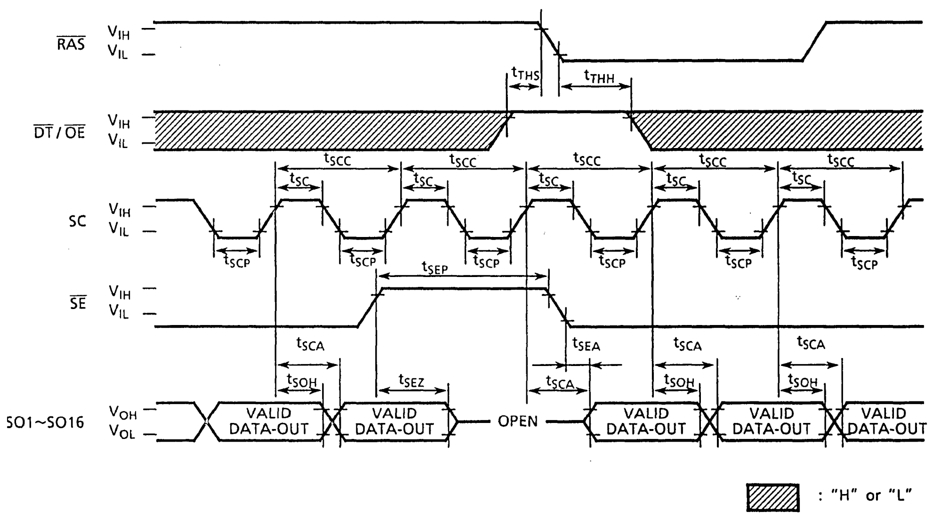
SPLIT READ TRANSFER CYCLE



READ TRANSFER CYCLE ($\overline{SE}$ = V_{IL})



SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



PIN FUNCTION

ADDRESS INPUTS : $A_0 \sim A_8$

The 18 address bits required to decode 16 bits of the 4,194,304 cell locations within the dynamic RAM memory array and they are multiplexed onto 9 address input pins (A_0~A_8). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe ($\overline{CASL}/\overline{CASU}$).

ROW ADDRESS STROBE : $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CASL}/\overline{CASU}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, DSF1 and DSF2 to invoke the various random access and data transfer operating modes shown in Table 1.

$\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high".

COLUMN ADDRESS STROBE : $\overline{CASL}/\overline{CASU}$

$\overline{CASL}/\overline{CASU}$ is the control input that latches the column address bits which are also used for the tap address during the transfer operations. The state of the special function input DSFl is read at the $\overline{CASL}/\overline{CASU}$ falling edge to select the block write mode or load register functions in conjunction with the $\overline{RAS}$ control. $\overline{CAS}$ before $\overline{RAS}$ refresh operations are selected if the signal is "low" at the $\overline{RAS}$ falling edge.

DATA TRANSFER/OUTPUT ENABLE : $\overline{DT}/\overline{OE}$

The $\overline{DT}/\overline{OE}$ input is a multifunction pin. When $\overline{DT}/\overline{OE}$ is "high" at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT}/\overline{OE}$ is used as an output enable control. If it is "low", a data transfer operation is activated between the RAM and the SAM.

WRITE PER BIT/WRITE ENABLE : $\overline{WB}/\overline{WE}$

The $\overline{WB}/\overline{WE}$ input is also a multifunction pin. When the signal is "high" at the falling edge of $\overline{RAS}$, during RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. If the signal is "low" at the $\overline{RAS}$ falling edge, the write - per - bit function is enabled.

WRITE MASK DATA/DATA INPUT AND OUTPUT : W_1/IO_1~W_{16}/IO_{16}

Data is written into the RAM through W_1/IO_1~W_{16} /IO_{16} pins during a write cycle. The input data is latched at the falling edge of either $\overline{CASL}/\overline{CASU}$ or $\overline{WB}/\overline{WE}$, whichever occurs late. In a read cycle data is read out of the RAM on the W_i/IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and column address. The Lower and Upper 8 bits are also used as the column address mask during a block white cycle. The each 8 bits correspond to Lower/Upper byte column.

When the write-per-bit function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register at the falling edge of $\overline{RAS}$. In a load mask and color register cycles, the data on the W_i/IO_i pins is stored into the write mask register and the color register respectively.

SERIAL CLOCK: SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted out of the SAM registers at the rising edge of SC. The serial clock SC also increments the 9-bits serial pointer which is used to select the SAM address. The SC pin must be held at a constant V_{IH} or V_{IL} level during read transfer operations and should not be clocked while the SAM is in standby mode to prevent the SAM pointer from being incremented.

No control signal disable SC input, and in any time SC toggle cause SAM pointer drarge regardless Sout (controlled by $\overline{SE}$).

SERIAL ENABLE : $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer location is still incremented while SC is clocked.

SPECIAL FUNCTION CONTROL INPUT : DSF1, DSF2

DSF1 is latched at the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to select the various TC524262/265 operations. If the signal is kept "low", the basical functions featured in conventional multi - port DRAM are enabled. To use the block write, the flash write and the load register functions or the split transfer operations, the DSF 1 signal needs to be controlled as shown in Table 1.

When the DSF 2 signal is "high" at the falling edge of $\overline{RAS}$, pipelined page mode operations are enabled. The pipeline mode is supported with the read, write and block write functions.

SPECIAL FUNCTION OUTPUT: QSF

QSF is an output signal which, during split register mode, indicates which half of the split SAM is being accessed. QSF "low" indicates that the lower split SAM (Bit 0~255) is being accessed and QSF "high" indicates that the upper split SAM (Bit 256~511) is being accessed. QSF is monitored so that after it toggles and waiting a delay of t_{STS}, split read transfer operation can be performed on the non-active split SAM.

SERIAL OUTPUT: SO_1~SO_{16}

Serial output SO_1~SO_{16} are the output pin of SAM register. SAM data out is valid t_{SCA} after SC rising edge. These SO_1~SO_{16} output is controlled by $\overline{SE}$. SO_i is going to Hi-Z state when $\overline{SE}$ goes high.

OPERATION MODE

The RAM port and data transfer operating of the TC524262/265 are determined by the state of $\overline{CASL}$/$\overline{CASU}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, DSF 1 and DSF 2 at the falling edge of $\overline{RAS}$ and by the state of DSF1 at the falling edge of $\overline{CAS}$. The Table 1 shows the functional truth table for a listing of all available RAM port and transfer operations.

Table 1. Functional Truth Table

$\overline{RAS}$ ↓					$\overline{CAS}$ ↓	Mnemonic Code	Function
$\overline{CASL}$/ $\overline{CASU}$	$\overline{DT}$/ $\overline{OE}$	$\overline{WB}$/ $\overline{WE}$	DSF1	DSF2	DSF1		
0	*	*	0	*	—	CBR	CBR Auto Refresh & Option Reset [1), 2)]
0	*	0	1	*	—	CBRS	CBR Auto Refresh & Stop Register Set[2)]
0	*	1	1	*	—	CBRN	CBR Auto Refresh
1	0	1	0	*	*	RT	Read Transfer
1	0	1	1	*	*	SRT	Split Read Transfer
1	1	0	0	0	0	RWM	Read Write (New/O1d Mask)[1)]
1	1	0	0	0	1	BWM	Block Write (New/O1d Mask)[1)]
1	1	0	1	*	*	FWM	Flash Write (New/Old Mask)[1)]
1	1	1	0	0	0	RW	Read Write (No Mask)
1	1	1	0	0	1	BW	Block Write (No Mask)
1	1	0	0	1	0	RWM (P)	PFP[3)] Read Write (New/01d Mask)[1)]
1	1	0	0	1	1	BWM (P)	PFP[3)] Block Write (New/old Mask)[1)]
1	1	1	0	1	0	RW (P)	FFP[3)] Read Write (No Mask)
1	1	1	0	1	1	BW (P)	PFP[3)] Block Write (No Mask)
1	1	1	1	*	0	LMR	Load (Old) Mask Register[1)]
1	1	1	1	*	1	LCA	Load Color Register

Note : * = 0 or 1, - = Not applicable.

1) After LMR operation, RWM, BWM, FWM, RWM (P), BWM (P) use old mask. Either CBR operation or LMR operation with no mask bits resets the old mask mode to new mask mode.
2) CBRS operation determines binary boundaries in the SAM. CBR operation resets the boundaries.
3) PFP stands for pipelined fast page mode.
4) The state of $\overline{CASL}$/$\overline{CASU}$ is defined as Logical "AND" of $\overline{CASL}$ and $\overline{CASU}$ state.

RAM PORT OPERATION

1. READ WRITE FUNCTION : RW

The TC524262 / 265 is equipped with the read write function which is identical to the conventional dynamic RAM's one and supports read, early write, $\overline{OE}$ controlled write and read-modify-write cycles as shown in the timing charts. Extended fast page (TC524265) and pipelined page modes are also available with the read write cycles by performing multiple $\overline{CAS}$ cycles during a single active $\overline{RAS}$ cycle.

1.1 EXTENDED FAST PAGE MODE (TC524265)

Extended fast page mode allows faster access to the memory in an actual system than the conventional fast page mode. An output data remains valid after the $\overline{CAS}$ signal goes high to prepare the next output data. Thus, the system has longer period to read the data from the RAM. Read, write and read-modify-write cycles are available during the extended fast page mode.

2. WRITE-PER-BIT (MASKED WRITE) FUNCTION : RWM

The write-per-bit (masked write) function selectively controls the internal write enable circuits of the RAM port. When $\overline{WE}$ is held "low" at the falling edge of $\overline{RAS}$, during the RWM cycle, the write mask is enabled. At the same time, the mask data on the W_i/IO_i pins is latched into the write-mask register. The I/O mask data maintains in a single $\overline{RAS}$ cycle, a page (New Mask Mode). When a load mask register function (LMR) is performed, the write mask data on the W_i/IO_i pins is latched into the write-mask register. After the LMR operation, the data at the falling edge of RAS during the RWM cycle is ignored and the I/O mask data that was stored in the write-mask register is used (Old Mask Mode) until the mode is reset by either CBR operation or LMR operation with no mask bits. The truth table of the write-per-bit functon is shown in Table 2.

Table 2. Truth table for write-per-bit function

At the falling edge of RAS				Write Mask Register	Function
$\overline{CASL}/\overline{CASU}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$W_i/IO/_i$ (i = 1~16)		
H	H	L	1	←	Write Enable
			0	←	Write Disable (New Mask)
			*	1	Write Enable
			*	0	Write Disable (Old Mask)

Note:* = 1 or 0 , ← = The data on W_i/IO_i is latched.

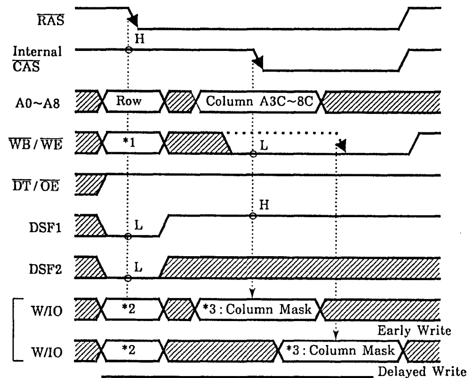
3. BLOCK WRITE AND MASKED BLOCK WRITE : BW &B WM

Block write is a special RAM port write operation which, in a page, allows for the data in the color register to be written into 8 consecutive column address locations starting from a selected column address in a selected row. The block write operation can be selectively disabled on an I/O basis and a column mask capability is also available.

A block write cycle is performed by holding $\overline{\text{CASL}}/\overline{\text{CASU}}$, $\overline{\text{DT}}/\overline{\text{OE}}$ "high" and DSF1 "low" at the $\overline{\text{RAS}}$ falling edge and by holding DSF1 "high" at the $\overline{\text{CASL}}/\overline{\text{CASU}}$ falling edge. If the DSF signal is "low" at the $\overline{\text{CASL}}/\overline{\text{CASU}}$ falling edge, a normal read write operation will occur. Therefore, a combination of block write, read and write operations can be performed during a fast page mode cycle. The state of $\overline{\text{WB}}/\overline{\text{WE}}$ input at the falling edge of $\overline{\text{RAS}}$ determines whether or not the I/O mask is enabled ($\overline{\text{WB}}/\overline{\text{WE}}$ must be "low" to enable the I/O mask, BMW mode or "high" to disable it, BW mode). The I/O mask is provided on the W_i/IO_i input at the RAS falling edge. After LMR operation, however, the old mask is used for the I/O mask function. The column mask data on the W_i/IO_i input must be provided at the $\overline{\text{CASL}}/\overline{\text{CASU}}$ or $\overline{\text{WB}}/\overline{\text{WE}}$ falling edge whichever is late, while the six most significant colunm address (A3C ~ A8C) are latched at the falling edge of $\overline{\text{CASL}}/\overline{\text{CASU}}$. This latched column address determines the start column address of consecutive block.

The block write is most effective for window clear and fill operation in frame buffer applications.

Figure 1. Block Write Operation



*1	*2	Mask Mode
1	Don't Care	No Mask Mode
0	WM1	New Mask Mode
0	Don't Care	Old Mask Mode

Example (Shown on Lower byte. The same manner on Upper byte)

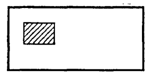
	W/IO							
	1	2	3	4	5	6	7	8
WM1 Register (Lower)	1	1	(0)	(0)	1	(0)	1	(0)
Column Select (Lower byte)	1	(0)	1	1	1	(0)	(0)	1
Color Register (Lower)	1	0	1	0	1	1	0	0

Result

	W/IO							
	1	2	3	4	5	6	7	8
Column 0	1	0			1		0	
Column 1								
Column 2	1	0			1		0	
Column 3	1	0			1		0	
Column 4	1	0			1		0	
Column 5								
Column 6								
Column 7	1	0			1		0	

Application

- High Speed Window Cear
- High Speed Rectangular Fill



*3) COLUMN MASK

Lower Byte

W1/IO1 -Column 0 (A2C = 0, A1C = 0, A0C = 0)
W2/IO2 -Column 1 (A2C = 0, A1C = 0, A0C = 1)
W3/IO3 -Column 2 (A2C = 0, A1C = 1, A0C = 0)
W4/IO4 -Column 3 (A2C = 0, A1C = 1, A0C = 1)
W5/IO5 -Column 4 (A2C = 1, A1C = 0, A0C = 0)
W6/IO6 -Column 5 (A2C = 1, A1C = 0, A0C = 1)
W7/IO7 -Column 6 (A2C = 1, A1C = 1, A0C = 0)
W8/IO8 -Column 7 (A2C = 1, A1C = 1, A0C = 1)

Upper Byte

W9/IO9 -Column 0 (A2C = 0, A1C = 0, A0C = 0)
W10/IO10 -Column 1 (A2C = 0, A1C = 0, A0C = 1)
W11/IO11 -Column 2 (A2C = 0, A1C = 1, A0C = 0)
W12/IO12 -Column 3 (A2C = 0, A1C = 1, A0C = 1)
W13/IO13 -Column 4 (A2C = 1, A1C = 0, A0C = 0)
W14/IO14 -Column 5 (A2C = 1, A1C = 0, A0C = 1)
W15/IO15 -Column 6 (A2C = 1, A1C = 1, A0C = 0)
W16/IO16 -Column 7 (A2C = 1, A1C = 1, A0C = 1)

4. FLASH WRITE : FWM

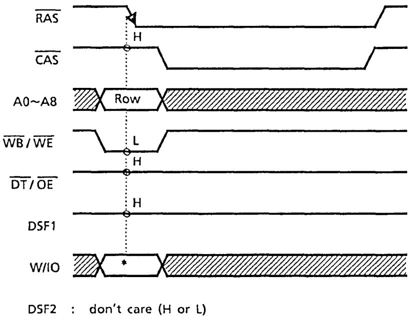
Flash write is a special RAM port write operation which in a single $\overline{RAS}$ cycle, allows for the data in the color register to be written into all the memory locations of a selected row. Each bit of the color register corresponds to one of the DRAM I/O blocks and the flash write operation can be selectively controlled on an I/O basis in the same manner as the write-per-bit operation.

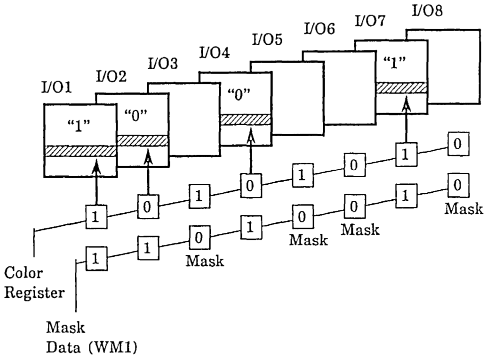
A flash write cycle is performed by holding $\overline{CASL}/\overline{CASU}$ "high", $\overline{WB}/\overline{WE}$ "low" and DSF1 "high" at the falling edge of $\overline{RAS}$. The mask data must also be provided on the W_i/IO_i inputs in order to enable the flash write operation for selected I/O blocks. After a LMR operation, however, the old mask in the mask register is used for the I/O block masking.

Flash write is most effective for fast plane clear operations in frame buffer applications. Selected planes can be cleared by performing 512 flash write cycle and by specifying a different row address location during each flash write cycle. Assuming a cycle time of 130ns, a plane clear operation can be completed in less than 66.6 µseconds.

Figure 2. Flash Write Operation

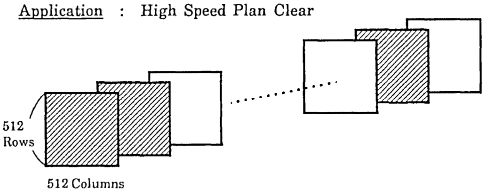
Example (Shown is lower only. The same manner in upper byte.)





*	Mask Mode
Mask Data	New Mask Mode
Don't Care (H or L)	Old Mask Mode

Application : High Speed Plan Clear



5. PIPELINED FAST PAGE MODE : RWM (P). BWM (P), RW (P), BW (P)

Pipelined fast page mode allows much faster access to the memory than the conventional page mode. Read, write and block write cycles are available at the pipelined fast page mode timings.

A pipelined fast page mode is performed by holding DSF 2 "high" at the falling edge of $\overline{RAS}$. A pipelined fast page read, write and block write operations can run at 30ns cycle time. Also, those mode can be selected every $\overline{CAS}$ cycle by the status of $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and DSF 1 pin. There are, however, penalties on the performance as follows :

(I) Two $\overline{CAS}$ cycles are required for the read operation. The first access, hence, takes longer than page mode. Also, one $\overline{CAS}$ cycle is needed to read out the data before the write cycle starts in the same page.

(2) One dummy cycle is needed to complete the write and block write operation. The cycle is, thus, needed between the write and the read operation and is required before the page ends.

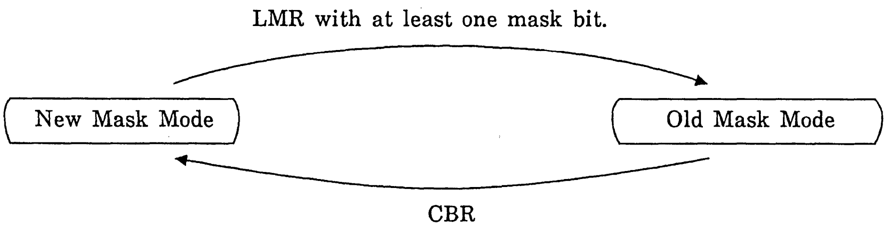
A system designer needs to carefully estimate the system performances with the pipelined page mode and the conventional page mode in order to decide which mode should be used.

6. LOAD (OLD) MASK REGISTER : LMR

The TC524262/265 has an on-chip 8 bit write-mask register which provides the 1/0 mask data during the masked functions such as the write-per-bit (RWM), masked block write (BWM) and flash write (FWM) functions. Each bit of the write - mask register corresponds to one of the DRAM I/O blocks. After the mask data is specified in the write-mask register by using the load mask register (LMR) cycle, the old mask mode is invoked during the masked functions.

The I/O mask data in the write - mask register maintains until another LMR operation is performed during the old mask mode. The LMR cycle is initiated by holding $\overline{CASL}/\overline{CASU}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and DSF1 "high" at the falling edge of $\overline{RAS}$ and by DSF1 "low" at the falling edge of CAS. The data presented on the W_i/IO_i lines are subsequently latched into the write-mask register at the falling edge of either $\overline{CASL}/\overline{CASU}$ or $\overline{WB}/\overline{WE}$, whichever occurs later. The old mask mode is reset to the new mask mode by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR). During the LMR cycle, the memory cells of the row address which is latched at the falling edge of $\overline{RAS}$ are refreshed.

Figure 3 State Diagram of Mask Mode



7. LOAD COLOR REGISTER : LCR

The TC524262 / 265 is provided with an on-chip 8-bits register (color register) for use during the block write or flash write function. Each bit of the color register corresponds to one of the DRAM I/O blocks. The load color register cycle is initiated by holding $\overline{CASL}/\overline{CASU}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and DSF1 "high" at the falling edge of $\overline{RAS}$. The data presented on the W_i/IO_i lines is subsequently latched into the color register at the falling edge of either $\overline{CASL}/\overline{CASU}$ or $\overline{WB}/\overline{WE}$, whichever occurs later. During the load color register cycle, the memory cells on the row address latched at the falling edge of $\overline{RAS}$ are refreshed.

8. REFRESH

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of 512 rows in the DRAM array within the specified 8 ms refresh period. The TC524262/265 supports the conventional dynamic RAM refresh operations such as $\overline{RAS}$ only refresh, $\overline{CAS}$ before RAS refresh and hidden refresh.

8.1 $\overline{CAS}$ before $\overline{RAS}$ Refresh and Option Reset : CBR

The CBR cycle reset the following functions, performing the $\overline{CAS}$ before $\overline{RAS}$ refresh operation at the same time.

- To reset the old mask mode to the new mask mode for the masked functions.
- To reset the stop register and remove the binary boundaries for the split SAM operation.

The systems which implement neither the old mask mode nor the binary boundary in the SAM is recommended to use the CBR cycle for refresh operation.

8.2 $\overline{CAS}$ before $\overline{RAS}$ Refresh : CBRN

The CBRN cycle performs only the $\overline{CAS}$ before $\overline{RAS}$ refresh operation. The systems which implement either the old mask mode or the binary boundary in the SAM usually use the CBRN cycle for refresh operation except for at the required stop register set or option reset cycles. The CBRN cycle must not be used during the initialization after power - up.

8.3 $\overline{CAS}$ before $\overline{RAS}$ Refresh and Stop Register Set : CBRS

The CBRS cycle sets the stop register to place binary boundaries in each half SAM, performing the CAS before RAS refresh operation at the same time. The CBRS cycle is initiated by $\overline{CASL}/\overline{CASU}$ and $\overline{WB}/\overline{WE}$ holding "low" and by DSF 1 "high" at the falling edge of $\overline{RAS}$. At the same time the data on the address pins, A_0 - A_8 is latched and the binary boundaries in each half SAM will be available when a split transfer operation is performed.

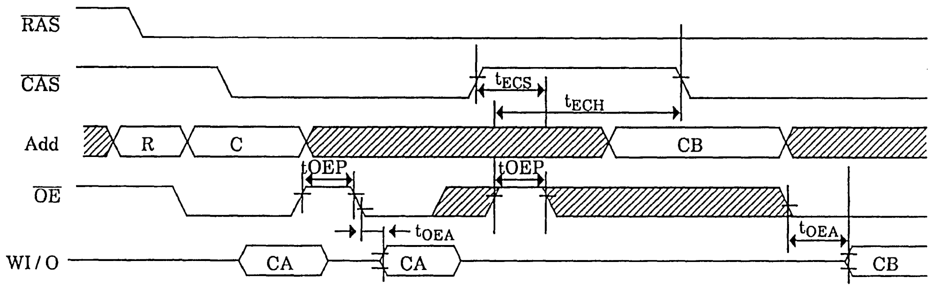
Figure 4 Stop Register and Binary Boundary Location

Stop Register Value A_8 - A_0	Binary Boundary Locations
0 1 1 1 1 1 1 1 1	Last Address of each block 255, 511 Default Case
0 0 1 1 1 1 1 1 1	127, 255, 383, 511
0 0 0 1 1 1 1 1 1	63, 127, 191, 255, 319, 383, 447, 511
0 0 0 0 1 1 1 1 1	31, 63, 95, 127, 159, 191, 223, 255, 287, 319, 351, 383, 415, 447, 479, 511
0 0 0 0 0 1 1 1 1	15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255, 271, 287, 303, 319, 335, 351, 367, 383, 399, 415, 431, 447, 463, 479, 495, 511
0 0 0 0 0 0 1 1 1	These values are not allowed to be set.
0 0 0 0 0 0 0 1 1	
0 0 0 0 0 0 0 0 1	
0 0 0 0 0 0 0 0 0	

NOTE

$\overline{OE}$ control of Extended Fast Pace mode Read cycle (TC524265)

When $\overline{OE}$ is toggled while $\overline{CAS}$ is "low" level in fast page mode read cycle, the same data is valid on WI/O. However, the data will not be valid when $\overline{OE}$ goes low with $\overline{CAS}$ high condition. The data will come out in following $\overline{CAS}$ cycle. Such a $\overline{OE}$ control have to satisfy t_{OEP} (10ns min), t_{ECS} (10ns min), t_{ECH} (10ns min). Please refer following Figure.



DATA TRANSFER OPERATION

The TC524262/265 features internal data transfer capability between the RAM and the SAM, as shown in Figure 5. During a normal transfer, 512 words by 16 bits of data can be loaded from RAM to SAM (Read Transfer). During a split transfer, 256 words by 16 bits of data can be loaded from the lower/ upper half of the RAM into the lower/ upper half of the SAM (Split Read Transfer). The normal transfer and split transfer modes are controlled by the DSF1 input signal

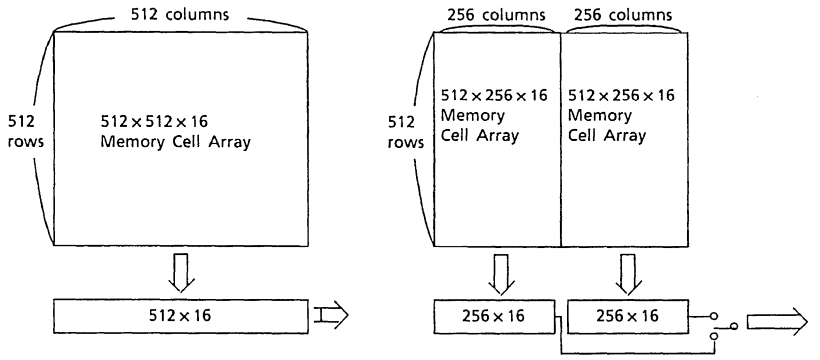


Figure 5. (a) Normal Transfer (b) Split Transfer

Table 3. shows the truth table of each Transfer Modes

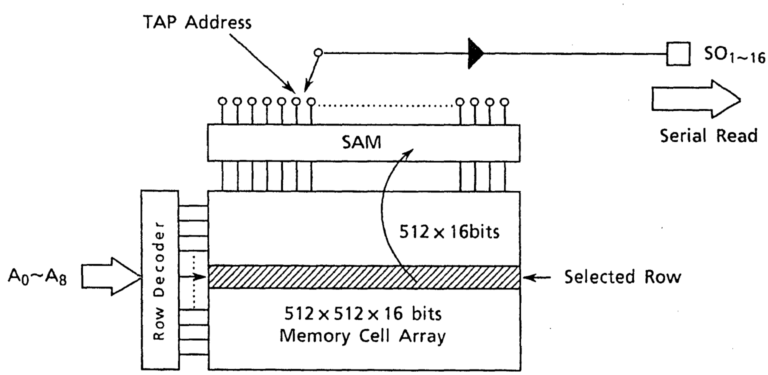
RAS				Mnemonic Code	Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
$\overline{CASL}$/ $\overline{CASU}$	$\overline{DT}$/ $\overline{OE}$	$\overline{WB}$/ $\overline{WE}$	DSF1					
H	L	H	L	RT	Read Transfer	RAM ~ SAM	512x16	Input ~ Output
H	L	H	H	5RT	Split Read Transfer	RAM —SAM	256x16	Half SAM active

9. READ TRANSFER CYCLE : RT

A read transfer consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CASL}$/$\overline{CASU}$ "high", $\overline{DT}$/$\overline{OE}$ "low" $\overline{WB}$/$\overline{WE}$ "high" and DSF 1 "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The start address of the serial pointer of the SAM (TAP address) is determined by the column address selected at the falling edge of $\overline{CASL}$/$\overline{CASU}$. By doing a tight timing control between the $\overline{DT}$/ $\overline{OE}$ rising edge and SC falling edge, a real time read transfer operation can also be performed.

Figure 6 shows the operation block diagram for read transfer operation.

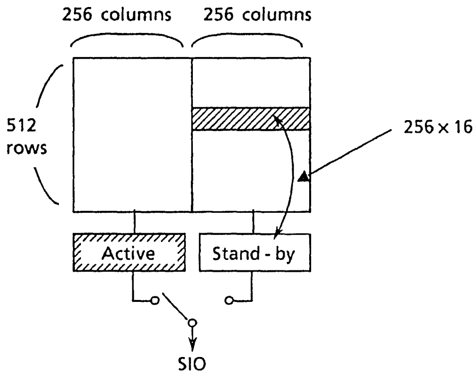
Figure 6. Block Diagram for Read Transfer Operation



In a read transfer cycle, the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}$/$\overline{OE}$ and the falling edge of $\overline{RAS}$ and $\overline{CASL}$/$\overline{CASU}$ as shown in READ TRANSFER CYCLE timing chart.

10. SPLIT READ TRANSFER CYCLE : SRT

A split read transfer consists of loading 256 words by 16 bits of data from a selected row of the half RAM array into the corresponding half SAM in stand-by mode, Serial data can be shifted out of the other half of the SAM in active mode simultaneously, as shown in Figure 7. The most significant column address (A8C) is controlled internally to determine which half of the SAM will be reloaded from the RAM array. During the split read transfer operation, the RAM port control signals do not have to be synchronized with the serial clock SC, thus eliminating the timing restrictions as in the case of real time read transfers. Prior to the execution of the split read transfer operation, a (normal) transfer operation must be performed to determine the absolute tap address location. QSF is an output that indicates which half of the SAM is in the active state. QSF changes state when the last SC clock is applied to the active SAM, as shown in Figure 8.



Active SAM	QSF Level
lower SAM	"Low"
upper SAM	"High"

Figure 7. Split Read Transfer

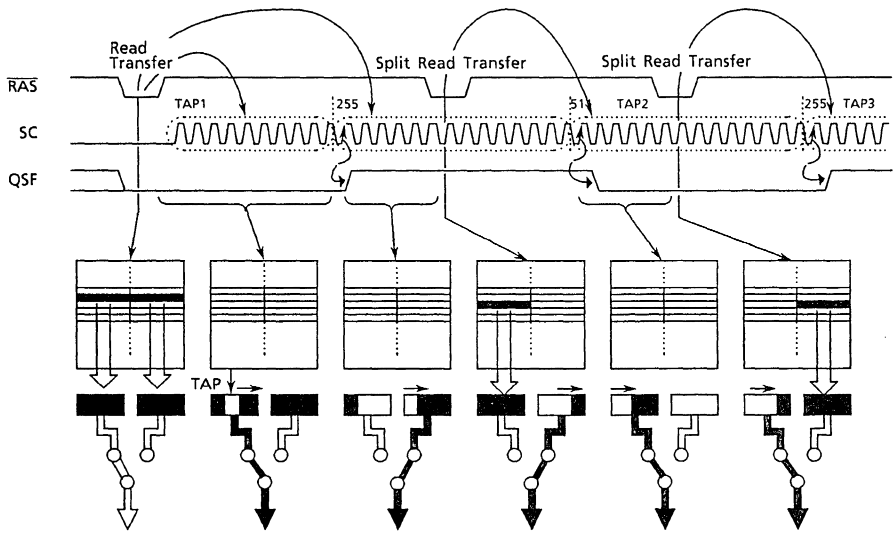
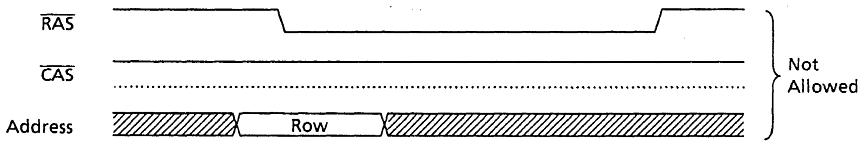


FIgure 8. Example of Consecutive Read Transfer Operations

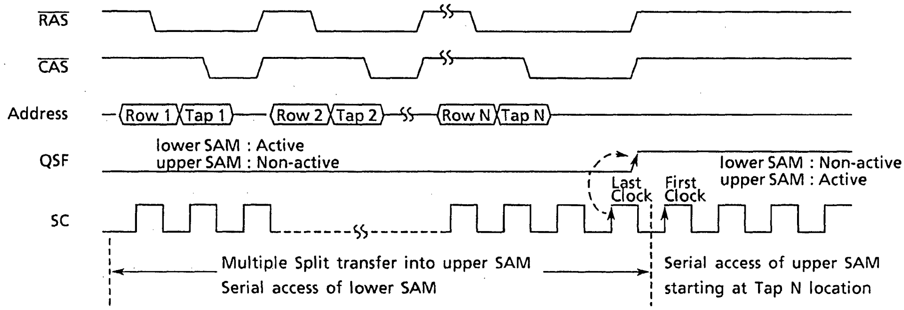
NOTES

(1) Transfer operation without CASL / CASU.

The SAM tap location is undefined if CASL / CASU is maintained at a constant "high" level during a transfer cycle. A transfer cycle with CASL / CASU held "high" is, hence, not allowed.



(2) In the case of multiple split transfers performed into the same half SAM, the tap location specified during the last split transfer, before QSF toggles, will prevail, as shown below.



(3) Split transfer operation allowable period.

Figure 9 illustrates the relation ship between the serial clock SC and the special function output QSF during split read/write transfers and highlights the time periods where split transfers are allowed, relative to SC and QSF. A split transfer is not allowed during to $t_{STH} + t_{STS}$. In the case that the CBRS operation is executed and the binary boundary in each half SAM is set or updated, an additional period is applied, as shown in Figure 9.

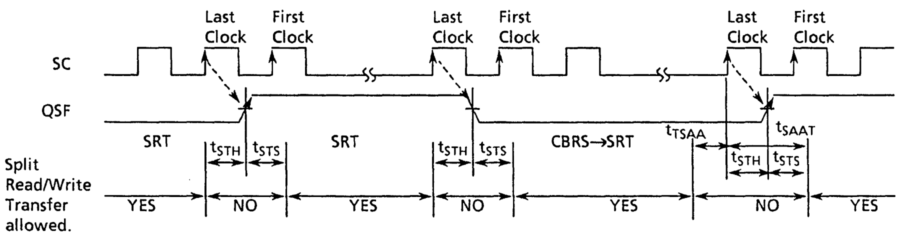
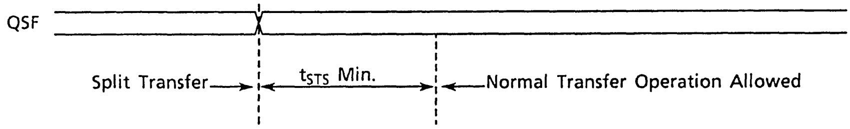


Figure 9. Split Transfer Operation Allowable Periods

The stop register and binary boundary are explained in the CBRS operation and the SAM port operation.

(4) A normal transfer may be performed following split transfer operation provided that a t_{STS} minimun delay is satisfied after the QSF signal toggles.

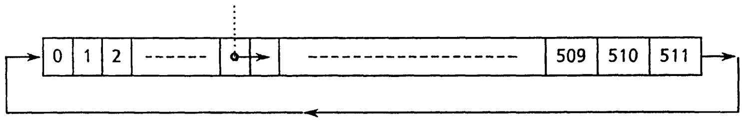


SAM PORT OPERATION

The TC524262 / 265 is provided with 512 words by 16 bits serial access memory (SAM) which can be operated in the single register mode or the split register mode. High speed serial read can be performed through the SAM port independent of the RAM port operation.

11. SINGLE REGISTER SERIAL READ OPERATION

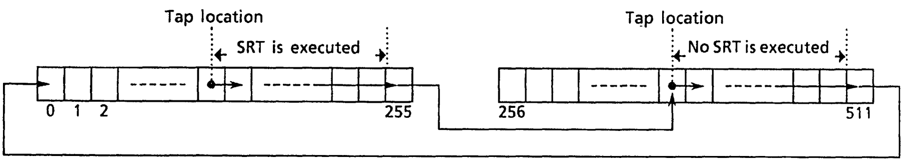
Serial data can be read out of the SAM port after a read transfer has been performed. At every rising edge of the serial clock, the data is read out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit, as illustrated below. Subsequent real - time read transfer may be performed on-the-fly as many times as desired.



12. SPLIT REGISTER MODE

The split register mode realizes continuous serial read operation. The data can be shifted into or out of one half of the SAM while a split read transfer is being performed on the other half of the SAM. Thus, the tight timing control at a real time read operation is eliminated with the split read operation. A normal read transfer operation must precede any split read transfer operation in order to set the TAP address. Also, a $\overline{CAS}$ before $\overline{RAS}$ refresh and stop register set cycle (CBRS) can be performed to specify the binary boundaries in the SAM.

In the split register mode, serial data can be read from one of the split registers starting from any of the 256 tap locations. The data is read sequentially from the tap location to the most significant bit (255 or 511) of the first split SAM and then the SAM pointer moves to the tap location selected for the second split SAM to read the data sequentially to the most significant bit (255 or 511) and finally wraps around to the least significant bit, as illustrated in the example below.



13. SPLIT REGISTER MODE WITH BINARY BOUNDARY

After a CBRS cycle is performed, the binary boundary, which is stated in 8.3. $\overline{CAS}$ before $\overline{RAS}$ refresh and stop register set, is set when a SRT cycle is performed. The serial data is read from one half of the SAM starting the tap location to the next binary boundary, while another SRT cycle is performed. Then, the SAM pointer moves to the tap location in the other half SAM and the data is read from the half SAM sequentially. If any SRT operation is not performed before the next boundary, the SAM pointer does not jump to the other half SAM, as illustrated in Figure 10.

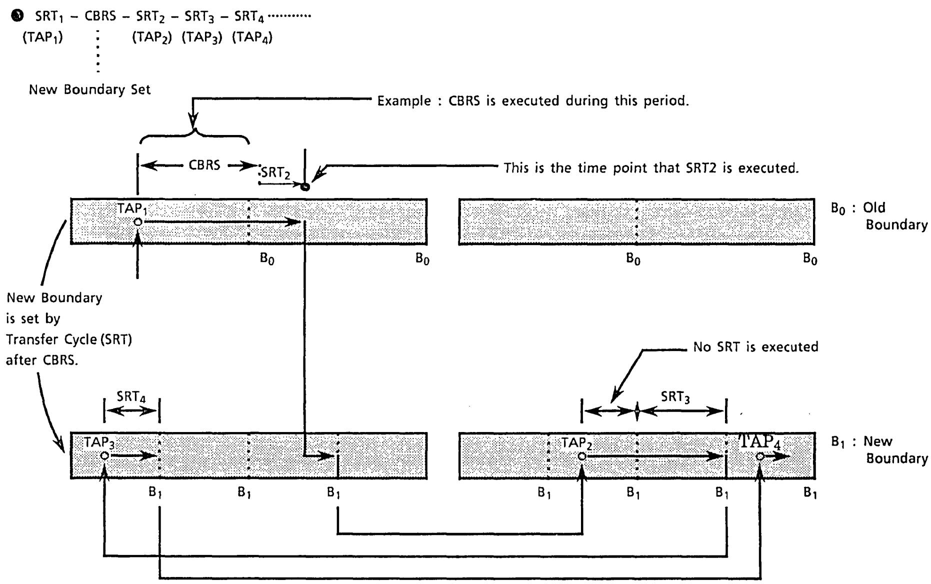


Figure 10. Operation of Spit Register Mode with Binary Boundary

The binary boundary is reset by a CBR cycle and the SAM operation mode returns to the normal split register mode, as shown in Figure 11.

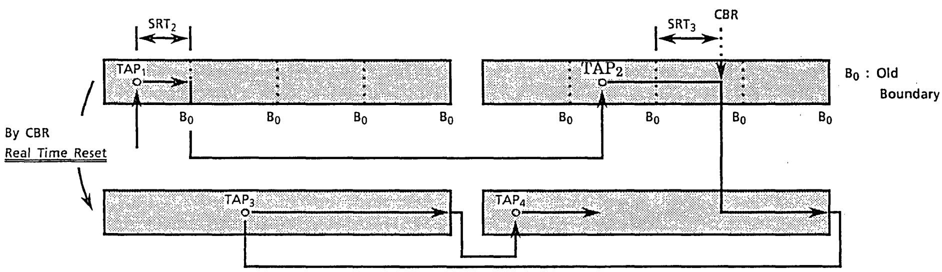


Figure 11. Binary Boundary Reset

Fig. 12 shows the relation between CBR and SC on binary-boundary-reset. When Nth SC-clock accesses old binary address is reset and (N + 1)th SC clock accesses old boundary address (old stop address) + 1 on the same split SAM, not jump to TAP address.

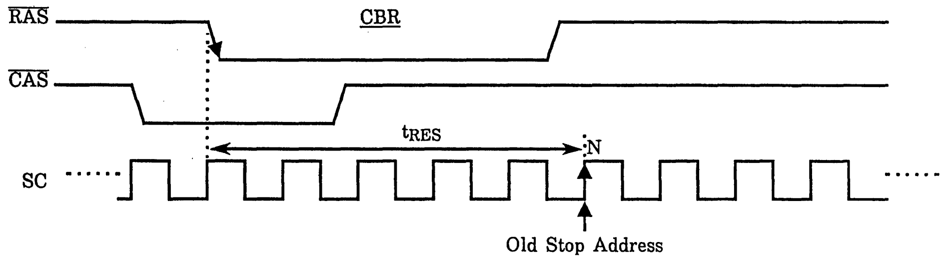


Figure 12. CBR and SC relation of binary-boundary-reset

In an actual system which uses the binary boundary a CBRS cycle is executed to determine a type of the boundary location. Then, a normal RT transfers a row of data into the SAM and set the initial tap location at the same time. An SRT cycle follows it before the SAM pointer reaches to the boundary location. The SRT cycle makes the binary boundary jump effective, as illustrated in Figure 13.

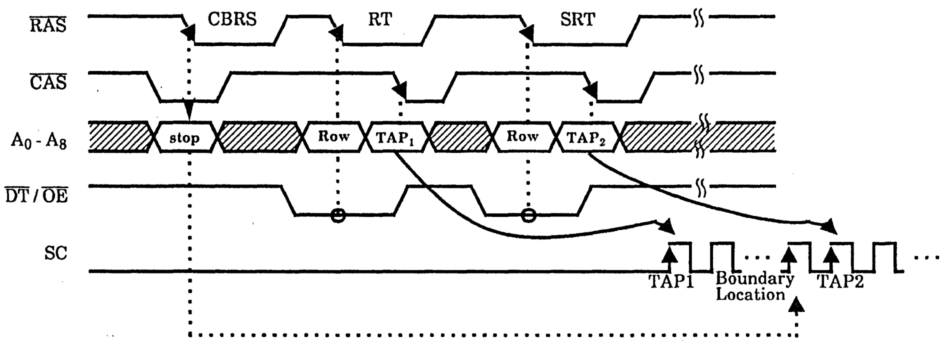


Figure 13. Binary Boundary Jump Set Sequence

There are additional timing specifications, t_{TSAA} and t_{SAAT} to determine the period that does not allow a split transfer, as illustrated in Figure 14.

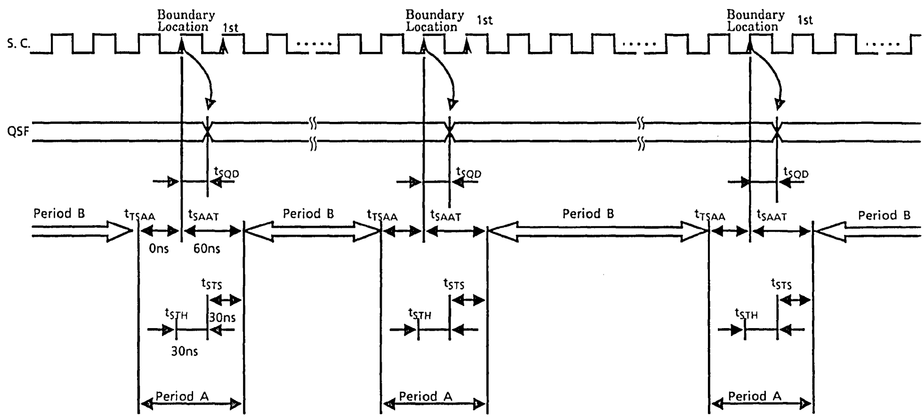


Figure 14. Timing Specification to allow SRT operation

POWER-UP

Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them "high" before or at the same time as the V_{CC} supply is turned on. After power-up, a pause of 200 µseconds minimum is required with $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ held "high". After the pause, a minimum of 8 CBR dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT}/\overline{OE}$ signal must be held "high".

INITIAL STATE AFTER POWER-UP

When power is achieved with $\overline{RAS}$, $\overline{CASL}/\overline{CASU}$, $\overline{DT}/\overline{OE}$ and $\overline{WB}/\overline{WE}$ held "high", the internal state of the TC524262 / 265 is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state setting cycle is performed after the initialization of the device is performed (200 µseconds pause followed by a minimum of 8 CBR cycles) and before valid operations begin.

	State after power-up
QSF	High-Impedance
Color Register	all "0"
Write Mask Register	Write Enable
TAP pointer	Invalid
Stop Register	Default Case

TOSHIBA

TC59S1604
TC59S1608

target spec

SILICON GATE CMOS
2,097,152 BY 8 BIT SYNCHRONOUS DRAM

DESCRIPTION

The TC59S1604/1608 is a JEDEC-standard synchronous DRAM (SDRAM) using a single 3.3Part -volt power supply. Various operational modes can be initiated by controlling the state of the RAS, CAS, WE, CS, CKE and DQM signals at the rising edge of the clock.

The synchronous DRAM is offered in the following organizations.

Part Number	Organization
TC59S1604	4Mx4
TC59S1608	2Mx8

FEATURES

- Fully synchronous DRAM
- Operating frequency of up to 100 MHz
- All inputs and outputs LVTTL compatible
- All inputs and outputs referenced to the rising edge of the clock
- Two bank organization to allow concurrent access/refresh and precharge operation
- RAM - SAM Transfer
  Read / Real Time Read Transfer
  Split Read Transfer
- $\overline{RAS}$ latency of 6 clocks at 100 MHz
- $\overline{CAS}$ latency of 3 clocks at 100 MHz
- Random column address update possible every 2 clock cycles
- Programmable burst length and addressing mode
- Programmable clock latency
- Auto refresh and self refresh
- Toshiba standard DRAM process

KEY PARAMETERS

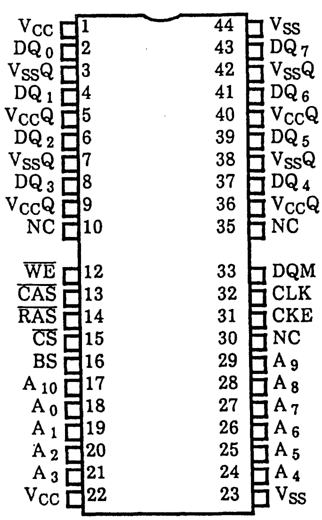
	TC59S1608FT/TR-10			TC59S1608FT/TR-12		
	100 MHz	66 MHz	50 MHz	80 MHz	50 MHz	40 MHz
t_{RC}	10	7	5	10	7	5
t_{RAS}	6	4	3	6	4	3
t_{RP}	4	3	2	4	3	2
t_{CAC}	3	2	2	3	2	2
t_{PC}	2	2	2	2	2	2
t_{RRD}	2	2	1	2	2	1

PIN DEFINITION

NAME	I/O	FUNCTION
A_0 - A_8	I	Address Input A_{0-10} for Row Address A_{0-8} for Column Address
BS	I	Bank Select
DQ_0 - DQ_7	I/O	Data Input/Output
$\overline{RAS}$	I	Row Address Asserted
$\overline{CAS}$	I	Column Address Asserted
$\overline{WE}$	I	Write Enable
DQM	I	Output Disable/Write Mask
$\overline{CS}$	I	Chip Select
CLK	I	Clock Input
CKE	I	Clock Enable
V_{CC}		Power for Internal Circuit
V_{SS}		Ground for Internal Circuit
V_{CCQ}		Power for Output Pin
V_{SSQ}		Ground for Output Pin

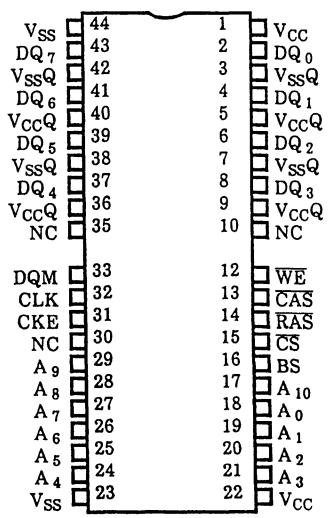
PIN OUT (2M x 8 Synchronous DRAM)

TC59S16800FT



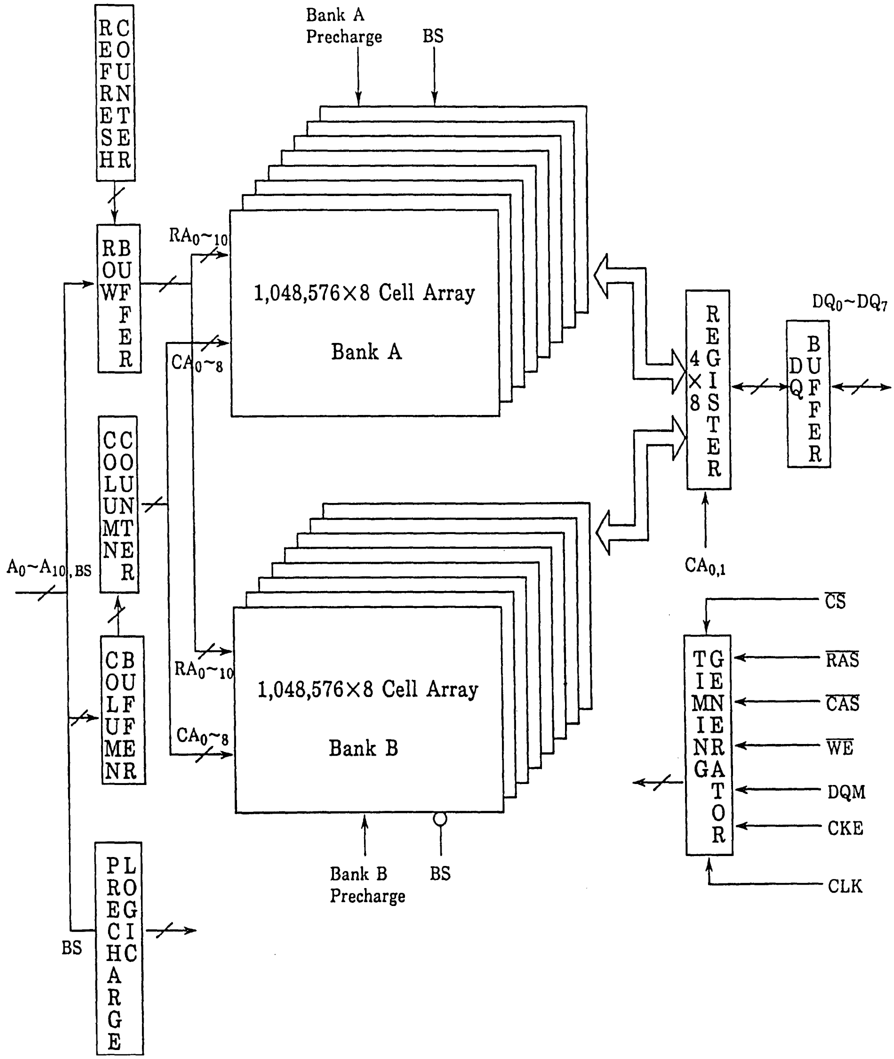
400mil 44Pin TSOP Ⅱ
(0.8mm pin pitch)

TC59S16800TR



400mil 44Pin TSOP Ⅱ
(Reverse Type)

BLOCK DIAGRAM



OPERATION

1. OPERATIONAL MODES

All the operations of the synchronous DRAM are initiated by a command which is sampled at every clock rising edge. The truth table for the operation commands is as shown in Table 1. The Chip Select signal, $\overline{CS}$, activates the DRAM and accepts any command when it is low.

Table 1. Function Truth Table

Command	CKE	DQM	BS	A10	A9-0	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Mode Register Set	H(2)	X	V	V	V	L	L	L	L
Auto Refresh	H(1)	X	X	X	X	L	L	L	H
Self-Refresh Entry	L(1)	X	X	X	X	L	L	L	H
Bank Deactivate/Precharge	H(2)	X	V	L	X	L	L	H	L
Precharge All	H(2)	X	X	H	X	L	L	H	L
Bank Activate	H(2)	X	V	V	V	L	L	H	H
Write	H(2)	X	V	L	V	L	H	L	L
Write and Autoprecharge	H(2)	X	V	H	V	L	H	L	L
Read	H(2)	X	V	L	V	L	H	L	H
Read and Autoprecharge	H(2)	X	V	H	V	L	H	L	H
No Operation	H(2)	X	X	X	X	L	H	H	L
No Operation	H(2)	X	X	X	X	L	H	H	H
Device Deselect	H(2)	X	X	X	X	H	X	X	X
Clock Suspend/Standby Mode	L(2)	X	X	X	X	X	X	X	X
Data Write/Output Enable	H(2)	L	X	X	X	X	X	X	X
Data Mask/Output Disable	H(2)	H	X	X	X	X	X	X	X

Note

(1) This level indicates at same cycle.
(2) This level indicates at previous cycle.
(3) V=Valid X=Don't Care L=Low level H=High level

2. PRECHARGE

The Precharge cycle is initiated with the $\overline{RAS}$ and $\overline{WE}$ signal low and the $\overline{CAS}$ signal high at a Clock rising edge. A10 signal is used to select from two precharge operation, Bank Precharge and Precharge All. When the A10 signal is high, both banks are precharged simultaneously. When the A10 signal is low, the bank select signal selects one of the two banks to be precharged. This operation is performed on a bank independently from the other bank, which can be held active.

3. ACCESS CYCLE

A Row Address Strobe cycle activates one of the two banks which corresponds to the status of the Bank Select signal. The Column Address Strobe cycle follows and initiates the sequential read or write operation which is synchronized at every Clock rising edge with up to 100MHz frequency. The addressing mode during the sequential read or write is programmable from two types, Sequential mode or Interleave mode. The number of the reads or writes (burst length) per a Column Address Strobe cycle is also programmable with the Mode Register Set cycle. The output buffer will be turned off after the specified read cycles are done.

If the two banks are alternately accessed, the Hidden Row Address application can be achieved, as illustrated in Figure 5, 6 and 7. The precharge operation is assumed to be performed in the bank which is not being accessed.

3.1 Page Mode

The Page Mode of the synchronous DRAM is similar to the fast page mode of a conventional dynamic RAM. The column address can be randomly updated by the Column Address Strobe cycle as many times as a system wants within the t_{RAC} maximum and refresh requirement. The minimum period until the next Column Address Strobe cycle is specified as t_{PC}, which is 2 cycles. A different column address within the page can be accessed while accessing other column addresses. The $\overline{CAS}$ command should be asserted even clock cycle followed by previous $\overline{CAS}$ command. After a burst length access, a delay time of t_{RST} is required before the next $\overline{CAS}$ command is asserted. The last clock of the read cycle is the clock that causes the DQ lines to go HI-Z after the burst length data read. $\overline{CAS}$ Command can be asserted at any clock edge after t_{WR} from last input at write cycle. (Figures 16,17) The feature is also applicable to the access between the two different pages which were independently selected in the two banks at the Row Address Strobe cycles. The Bank Select signal is used to choose one of the two pages to be accessed. (Figure 8)

3.2 READ AND WRITE OPERATION

The synchronous DRAM supports sequential read and write operations. The write operation is selected when the Write Enable signal is asserted at a Column Address Strobe cycle. Otherwise, the RAM will be in the read mode. Therefore, a read modify write operation is not available with the RAM. Because of the pipelined operation implemented in the RAM, the initial read data from the Column Address Strobe cycle becomes available at the cycle which is specified as the t_{CAC} in clock cycles. The number of read - outs per $\overline{CAS}$ cycle is determined with the burst length.

A read operation can be switched to a write operation at a multiple of the t_{PC} cycle from the Column Address Strobe cycle for the read operation, although the data is still being read within the burst length. In this case the DQM signal has to be controlled, otherwise bus contention occurs during the transition. (Figure 9 , 18)

When a precharge command is asserted during read operation, the read data is going to be invalid after Read $\overline{CAS}$ Latency delay. The precharge command doesn't affect the column operation of device, therefore the data is continuously output after the precharge command assertion, however this data is unkown. (Figure 18)

When a read command is asserted during a Write operation, the write data that is input to the device prior to the read command is written into the RAM array. The data input after read command assertion is not written into RAM. (Figure 19)

Write cycle is completed when precharge command cycle is asserted. 2 Clock cycle of DQM mask have to be asserted when precharge command is performed before full length of burst write cycle. (Figure 9 , 19)

When the A10 singal is high at a Read / Write command, the autoprecharge cycle is activated. Therefore precharge is performed automatically. The autoprecharge cycle can not be interruped.

3.3 CLOCK MASK AND INPUT / OUTPUT MASK

In the event that a system can not accept or provide the data within a clock cycle, the clock suspension mode is useful. Once the CKE signal is negated, the Clock is internally freezed from the next cycle. A read or write operation is, thus, suspended until the CKE signal is asserted again.

The Input / Output Mask signal (DQM) has two functions, synchronized output enable during a read cycle and word mask during a write cycle. The Read cycle requires 1 clock latency before the functions are actually performed. In case of the Write cycle, word mask functions are performed in the same cycle (0 clock Latency), as illustrated in Figure 2.

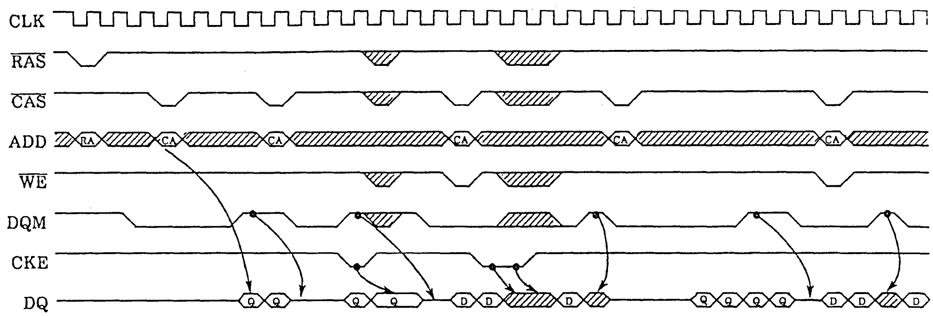


Figure 2. Clock Mask and Input/Output Mask (4 wrap mode)

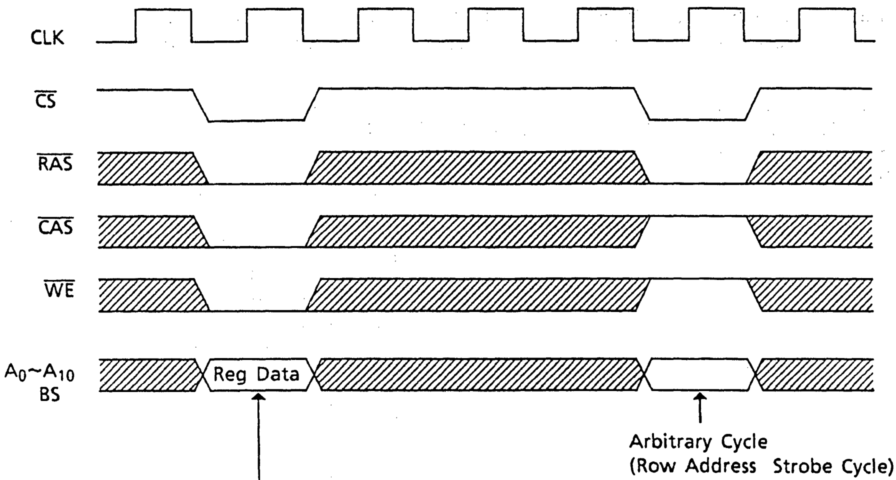
4. REFRESH OPERATION

There are two refresh modes available with the RAM, Auto Refresh and Self Refesh cycles. The auto refresh cycle starts when the $\overline{CS}$ and $\overline{RAS}$ and $\overline{CAS}$ signals are low and the CKE and $\overline{WE}$ signals are high at the Clock rising edge, which is similar to $\overline{CAS}$ before $\overline{RAS}$ refresh of a conventional DRAM. Bank A / B are refreshed alternately by Auto Refresh. The Auto Refresh has autoprecharge function, therefore precharge operation is executed automatically. Next command can be asserted after t_{RC} from refresh command. (Figure 13)

The Self Refresh mode starts when $\overline{CS}$, CKE, $\overline{RAS}$ and $\overline{CAS}$ are Low at the clock rising edge. To exit from the self refresh cycles, the CKE signal is asserted and a delay of t_{RC} is required. Then the next arbitrary operation can be performed. (Figure 14).

5. MODE REGISTER SET CYCLE

The RAM has programmable addressing modes during the consecutive column access cycles. One of the modes is selected at a Mode Set cycle. The random access time in clock cycles, and the latency are also programmed at the same cycle. A system can choose the best suitable modes to maximize its performance. The Mode Set Cycle is initiated when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ signals are low at the clock rising edge. Four clocks are needed to change the mode, as illustrated in Figure 3.



BS	0	Reserved
A_{10}	0	
A_9	0	
A_8	0	
A_7	T	Test Mode
A_6	L	Latency field
A_5	L	
A_4	L	
A_3	S/I	Addressing mode (Sequential / Interleave)
A_2	B	Burst Length field
A_1	B	
A_0	B	

Figure 3. Mode Register Set Cycle

5.1 LATENCY

In order to maximize the performance of a system the latency along with relevant parameters can be set with the mode set cycle. The maximum frequency is specified on each latency as shown on the cover page.

BS	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
O	O	O	O	T	L	L	L	S/I	B	B	B

Latency field (A_6~A_4)

A_6	A_5	A_4	t_{CAC} (Cycle)
0	1	0	2
0	1	1	3
1	0	0	4

Note : Any other combinations are not available on A_6~A_4 besides the above three types.

5.2 ADDRESSING MODES

There are two addressing modes available with the RAM, Sequential mode and Interleave mode. A system has to perform at least one mode register set cycle to specify one of the addressing modes prior to any operation.

BS	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
O	O	O	O	T	L	L	L	S/I	B	B	B

Burst Length field (A_2~A_0)

A_2	A_1	A_0	Sequential	Interleave
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8

Other combinations are prohibited

Interleave/Sequential Select (A_3)

A_3	Addressing Mode
0	Sequential
1	Intrerleave

With any addressing mode the access which is initiated by a $\overline{CAS}$ cycle can start at any arbitrary column address. The data will be sequencially read or written into the RAM up to the specified number by the burst length field. The sequential mode is suitable for a cache line fill application, where the sequential access returns from the end to the beginning of a block whose boundary is determined at every burst length in a row. The interleave mode controls the address so each address is flipped to its invert at the clock rising edge every time one bit less siguificant address returns to the previous state. Intel's 486 microprocesser implements the 4 bit interleave mode for the burst cache fill operation.

5.3 TEST MODE

When A7 bit is set, the device enters Test Mode. The A7 bit should be set to “0” during normal operation.

6. POWER DOWN MODE

The I_{CC} current is reduced by cutting off the Input and Output Buffer. The Input Buffer and Output Buffer are controlled by the CKE signal, however while either bank is active, CKE doesn't control the Input and Output Buffers. Power down mode cut off the Input and Output Buffers except the CLK Buffer and CKE Buffer. (Figure 15)

7. POWER UP

To ensure that the outputs are high-Z, DQM and CKE should track $V_{CC.}$ After power up, a pause of 200µ seconds minimum is required. Following this pause time, minimum of 8 Auto Refresh dummy cycles must be performed to stabilize the internal circuity before any operations start. The default value of the Mode Register after power up is undefined. therefore a Mode Register set cycle must be performed before proper operation.

S/I	Burst Length	Addressing Sequence							
Sequential ($A_3 = 0$)	4 bit (A_2~A_0 = 010)	0	1	2	3				
		2	3	0	1				
		7	4	5	6				
		13	14	15	12				
Sequential ($A_3 = 0$)	8 bit (A_2~A_0 = 011)	0	1	2	3	4	5	6	7
		2	3	4	5	6	7	0	1
		7	0	1	2	3	4	5	6
		13	14	15	8	9	10	11	12
Interleave ($A_3 = 1$)	4 bit (A_2~A_0 = 010)	0	1	2	3				
		1	0	3	2				
		7	6	5	4				
		13	12	15	14				
Interleave ($A_3 = 1$)	8 bit (A_2~A_0 = 011)	0	1	2	3	4	5	6	7
		1	0	3	2	5	4	7	6
		7	6	5	4	3	2	1	0
		13	12	15	14	9	8	11	10

Figure 4. Column Access Addressing Example

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70° C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{CCQ}	Supply Voltage for DQ Buffer	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	- 0.5		0.8	V

CAPACITANCE (Ta=0~70° C, V_{CC} = 3.3V ± 10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance		5	pF
C_O	Input/Output Capacitance		7	pF

DC CHARACTERISTICS (Ta=0~70° C, V_{CC}=3.3V±0.3V)

PARAMETER			Limits -10 (100MHz)	Limits -12 (80MHz)
$\overline{RAS}$ Operation Current ROW Address Strobe Command & Precharge Command Cycling t_{PRD} = min t_{RC} = min	Single Bank Operation		80mA	70mA
	Interleave Operation		140mA	130mA
$\overline{CAS}$ Operation Current Column Address Strobe Command Cycling t_{PRD} = min t_{PC} = min			90mA	80mA
No Operation Current Both Bank Active $\overline{CS}$ = V_{IH} FIX			10mA	10mA
Standby Current Both Bank Precharged $\overline{CS}$ = V_{IH} FIX	CKE = V_{IL}	TTL Input	2mA	2mA
		CMOS Input	1mA	1mA
	CKE = V_{IH}	TTL Input	7mA	7mA
		CMOS Input	5mA	5mA
Auto Refresh Current Auto Refresh Command Cycling t_{PRD} = min t_{RC} = min			80mA	70mA
Self Refresh Current CKE = V_{IL} CMOS Input			1mA	1mA

PARAMETER	min	max
Input Leakage Current	-10μA	10μA
Output Leakage Current	-10μA	10μA
Output "H" Level Voltage (Iout = -4mA)	2.4V	
Output "L" Level Voltage (Iout = 4mA)		0.4V

AC CHARACTERISTICS (Ta=0~70°C, V_{CC} = 3.3V ± 0.3V)

SYMBOL	PARAMETER	-10		-12		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX		
t_{RC}	Random Read/Write Cycle Time	100		120		ns	2
t_{RAC}	Access Time from $\overline{RAS}$		60		72	ns	2, 4
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	30	24	36	ns	2, 4
t_{RP}	$\overline{RAS}$ Precharge Time	40		48		ns	2
t_{RRD}	$\overline{RAS}$ to $\overline{RAS}$ Delay	20		24		ns	2
t_{CAC}	Access Time from $\overline{CAS}$		30		36	ns	2
t_{PC}	Page mode Cycle Time	2		2		Cycle	
t_{RSH}	$\overline{CAS}$ to Precharge Delay Time	2		2		Cycle	
t_{CKA}	Access Time from CLK		10		12	ns	
t_{WR}	Write Recovery Time	1		1		Cycle	
t_{RST}	Burst Cycle Reset time	20		24		ns	2
t_{OH}	Output data hold time	5		6		ns	
t_{OD}	Output data disable time	5	10	6	12	ns	
t_{ACT}	Power down mode exit time	0	15	0	18	ns	
t_{SB}	Power down mode entry time	0	15	0	18	ns	
t_{RAS}	$\overline{RAS}$ to Precharge Delay	60	100	72	100	ns/us	2
t_{STUP}	Input Signal SetupTime	2		2		ns	
t_{HOLD}	Input Signal hold time	3		4		ns	
t_{T}	Transition time	1	10	1	10	ns	
t_{PRD}	CLK Period	10		12		ns	
t_{CLKH}	CLK High Time	2		3		ns	
t_{CLKL}	CLK Low Time	2		3		ns	
t_{PEF}	Refresh Period (4k Refresh)		64		64	ms	
t_{RSC}	Mode Register Set Cycle Time	40		48		ns	2
t_{RH}	Register Set Data hold time	8		10		ns	
t_{RS}	Register Set Data setup time	2		2		ns	

NOTES

1. AC measurements assume t_T=2ns.
   Measured with a load equivalent to 2 TTL Load and 50pF.
   Mid point is reference level for measuring timing of input and output signals. Vref=1.4V

2. CLK times of this parameter are decided by operation CLK period.

$$\text{CLK time=round up} \left(\frac{\text{Timing Parameter}}{t_{PRD}} \right)$$

TC59S16800FT/TR-10

CLK Freq	t_{RC}	t_{RP}	t_{RRD}	t_{CAC}	t_{RAS}
	100ns	40ns	20ns	30ns	60ns
33*~50MHz	5	2	1	2	3
51~66MHz	7	3	2	2	4
67~75MHz	8	3	2	3	5
76~83MHz	9	4	2	3	5
84~100MHz	10	4	2	3	6

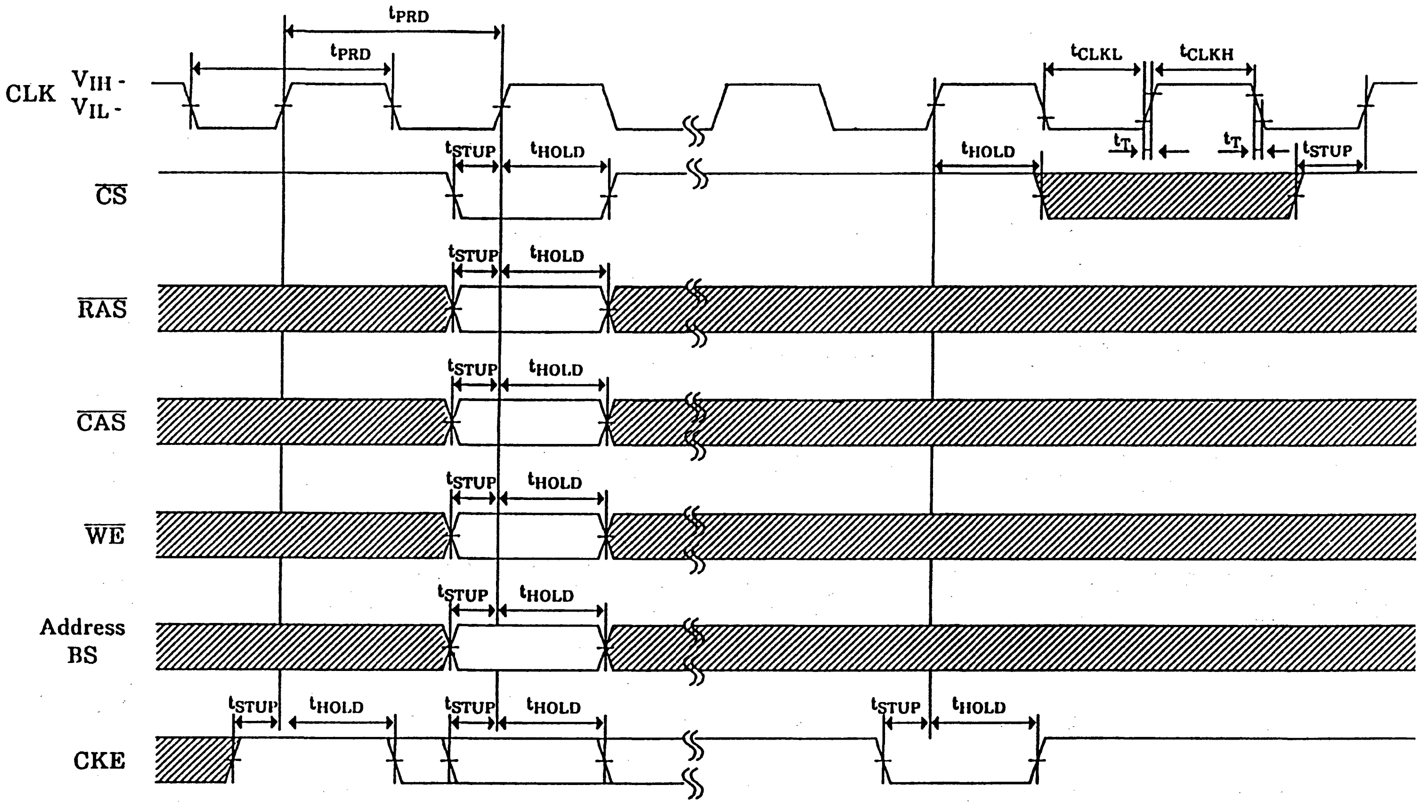
TC59S16800FT/TR-12

CLK Freq	t_{RC}	t_{RP}	t_{RRD}	t_{CAC}	t_{RAS}
	120ns	48ns	24ns	36ns	72ns
25*~41MHz	5	2	1	2	3
42MHz	7	3	1	2	4
43~55MHz	7	3	2	2	4
56~62MHz	8	3	2	3	5
63~69MHz	9	4	2	3	5
70~80MHz	10	4	2	3	6

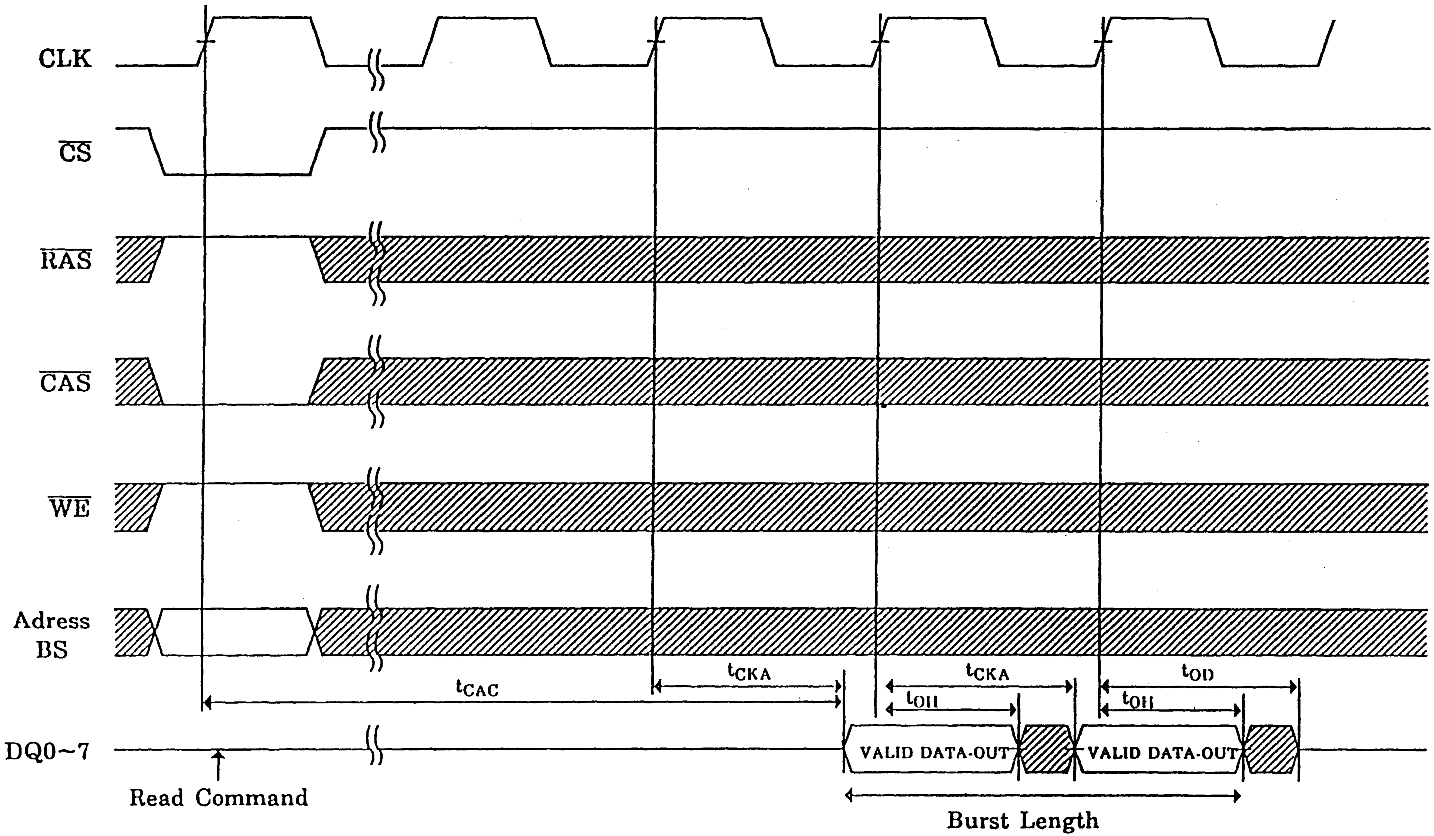
3. *:It is the minimum frequency so the synchronous DRAM has performance advantage over standard DRAMs.

4. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met.

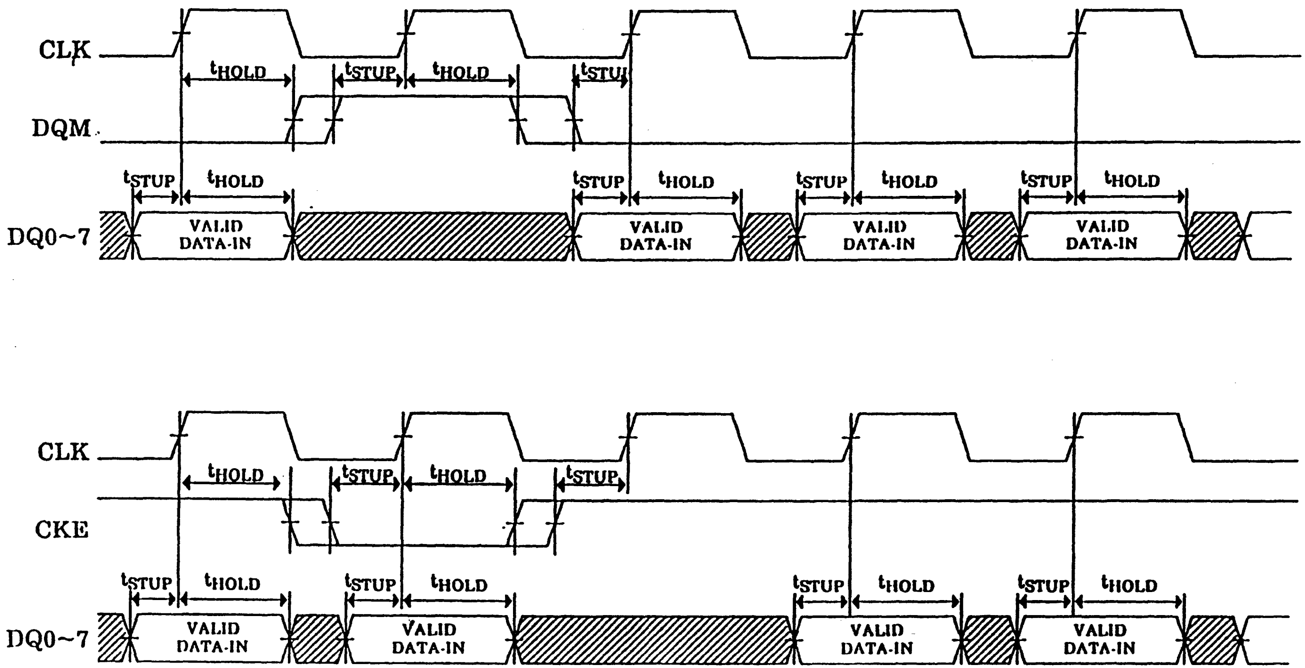
COMMAND INPUT WAVEFORMS



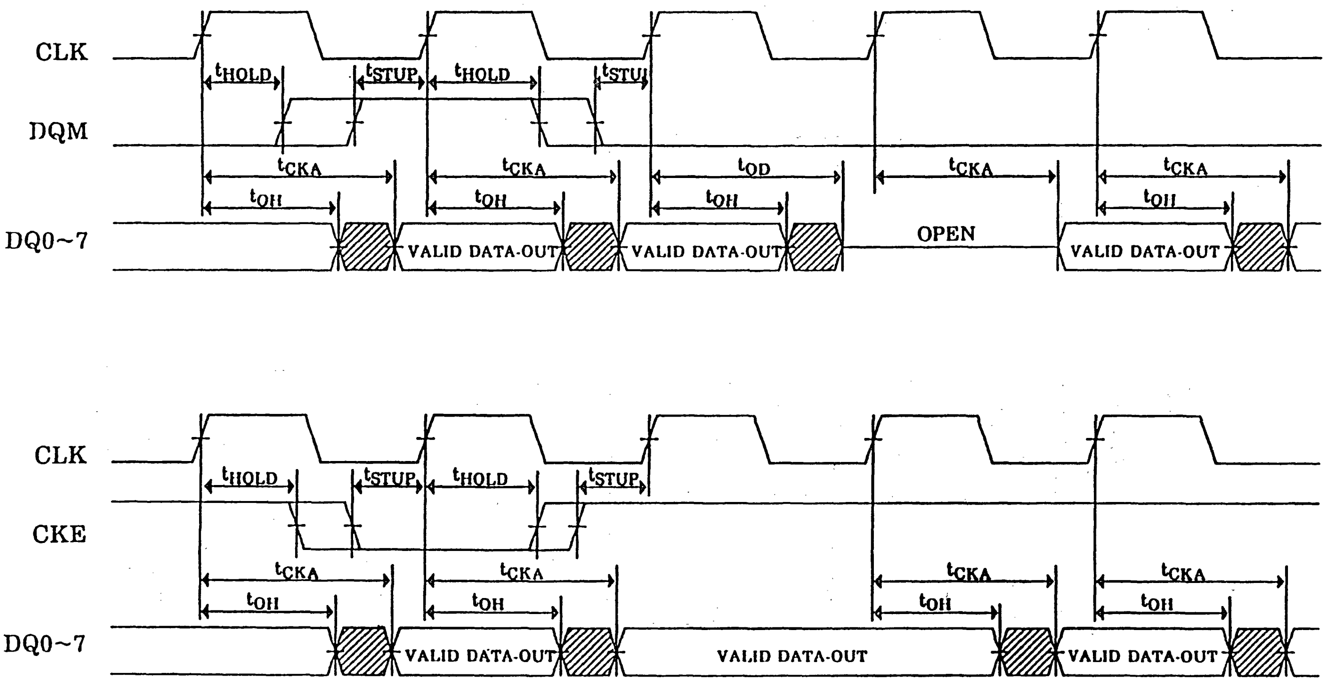
OUTPUT WAVEFORMS



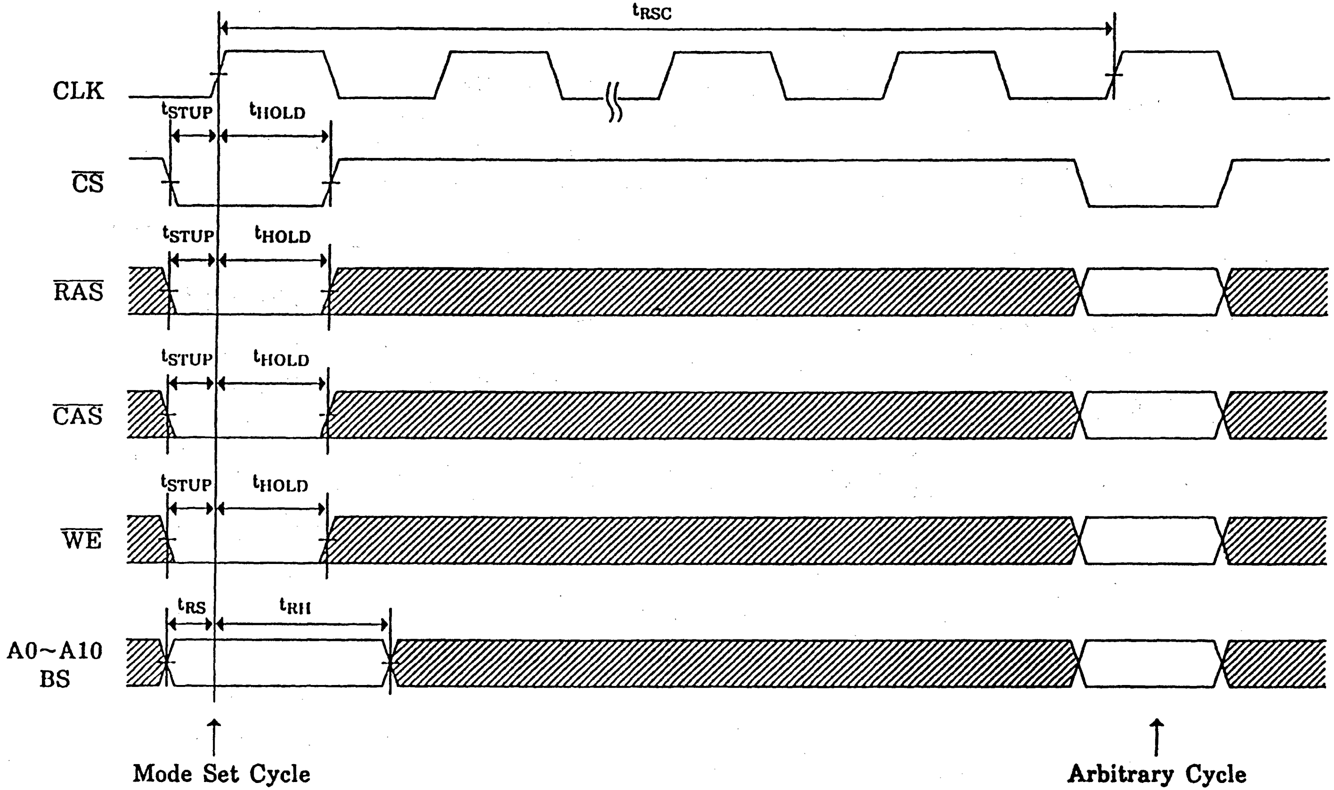
INPUT MASK / CLOCK MASK CYCLE



OUTPUT MASK / CLOCK MASK CYCLE



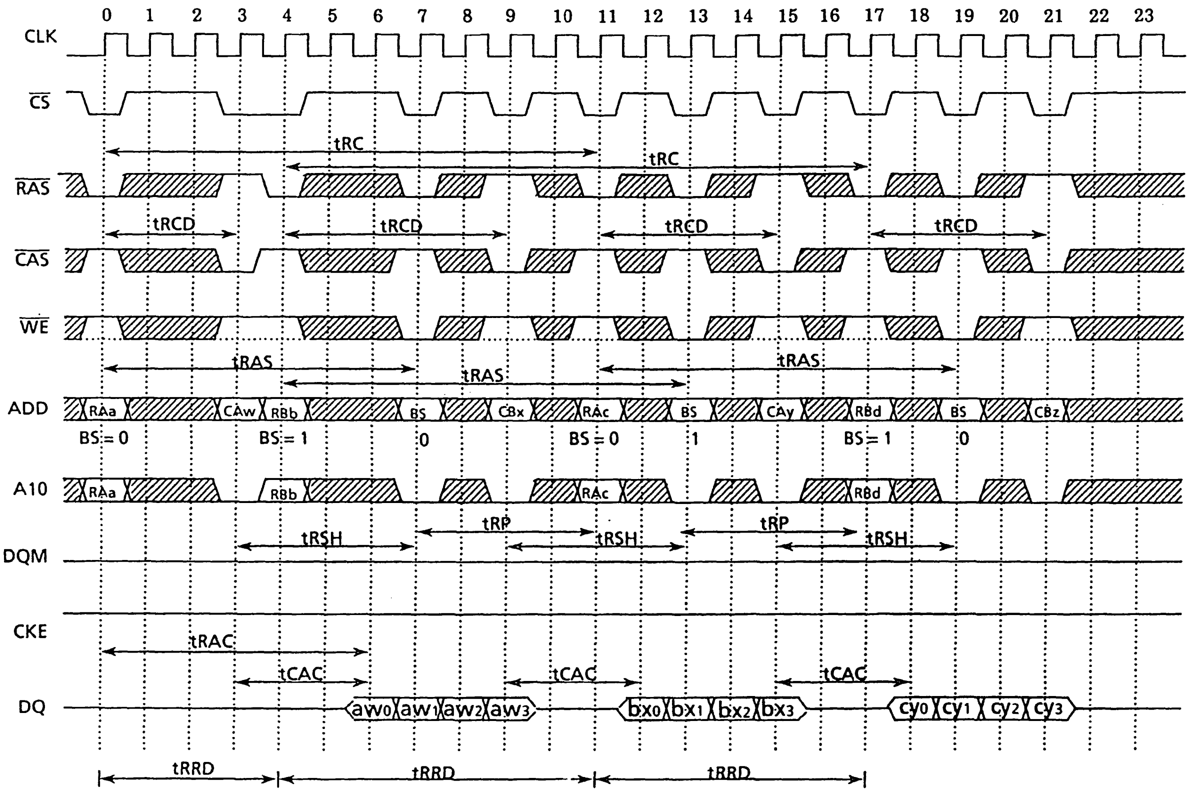
MODE REGISTER SET CYCLE



INTERLEAVED BANK READ (4 WRAP MODE)

Figure 5 - 1

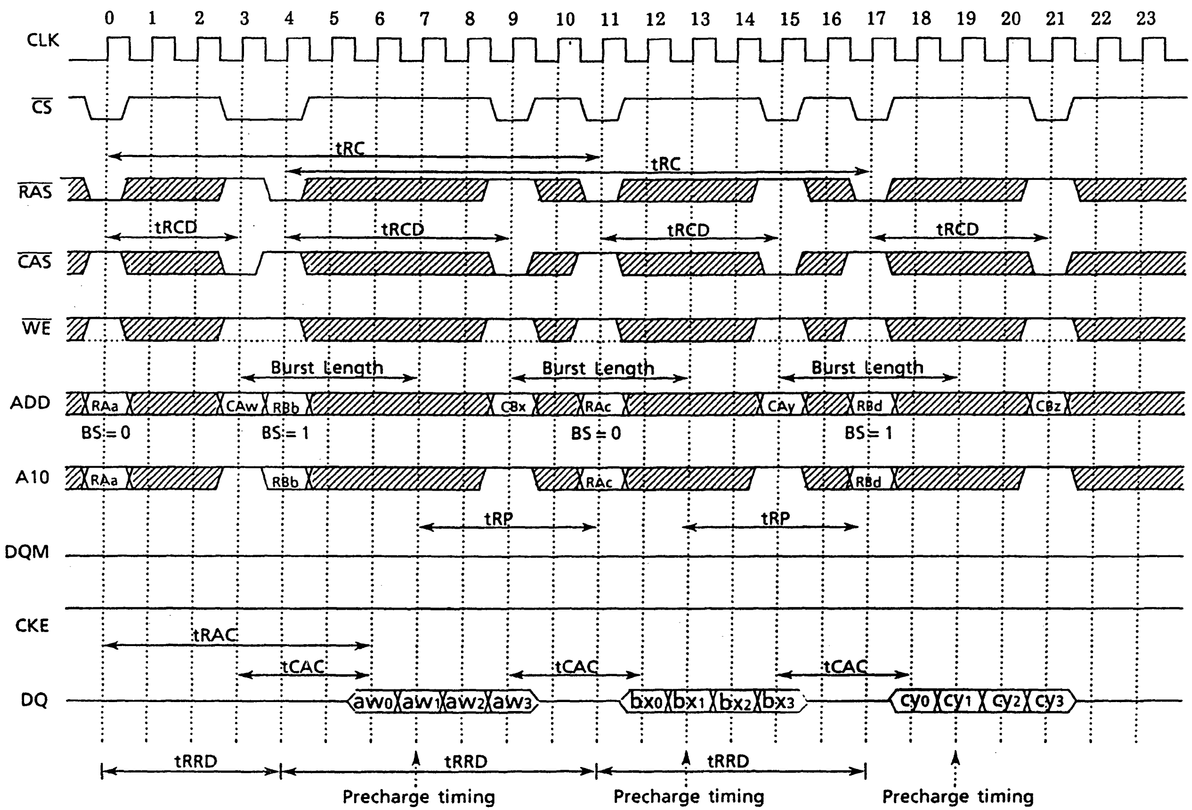
(CLK = 100MHz) (External Precharge)



INTERLEAVED BANK READ (4 WRAP MODE)

Figure 5 - 2

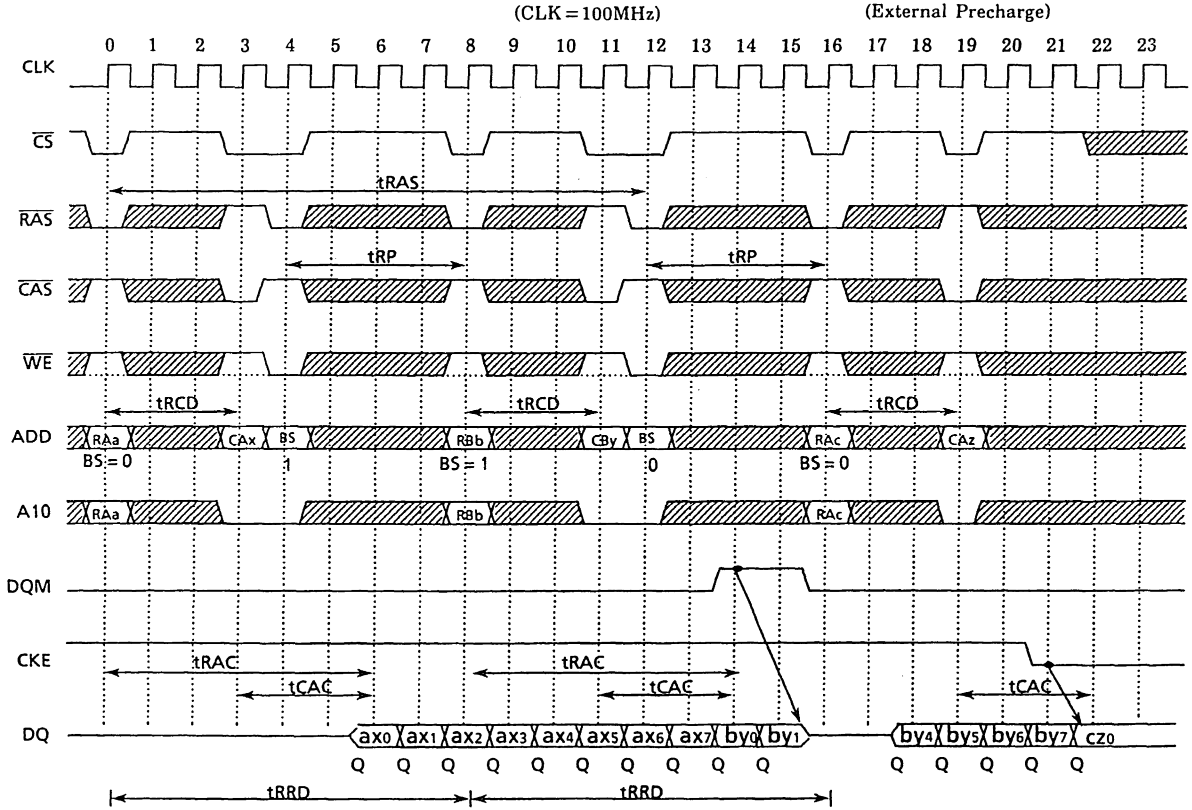
(CLK = 100MHz) (Auto Precharge)



16M Synchronous DRAM

INTERLEAVED BANK READ (8 WRAP MODE)

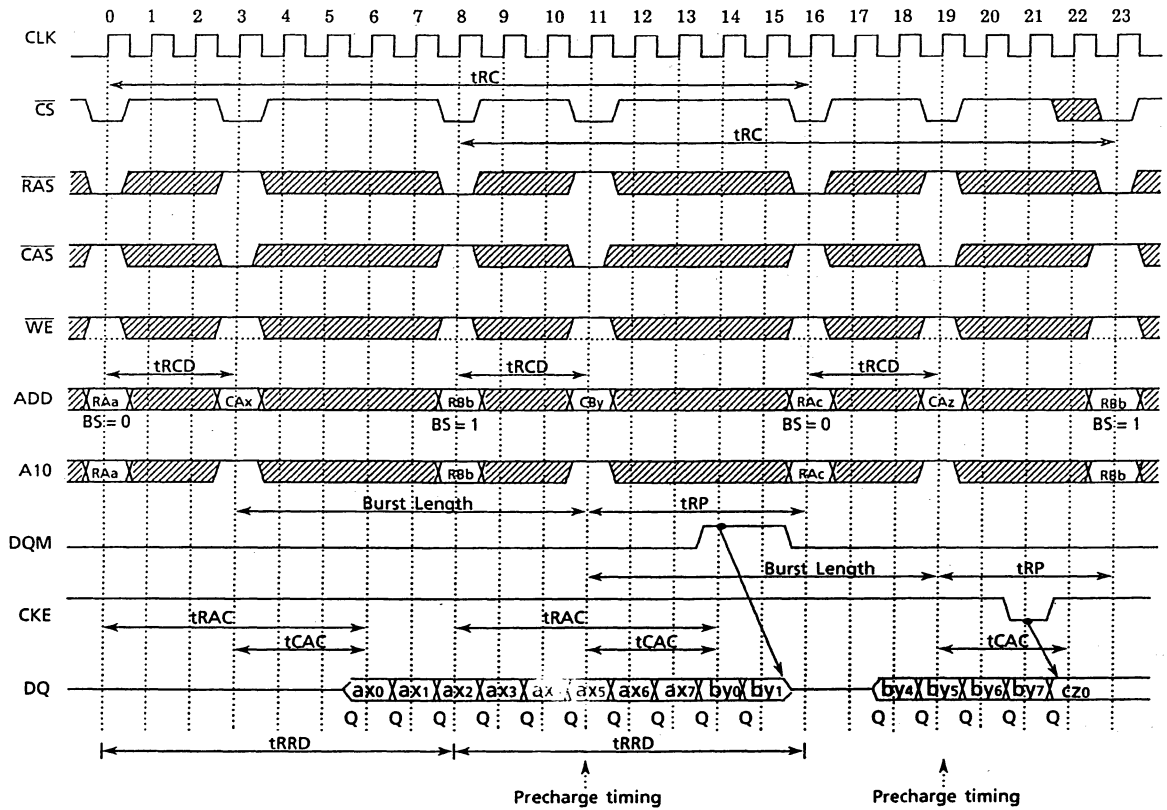
Figure 6 - 1



INTERLEAVED BANK READ (8 WRAP MODE)

Figure 6 - 2

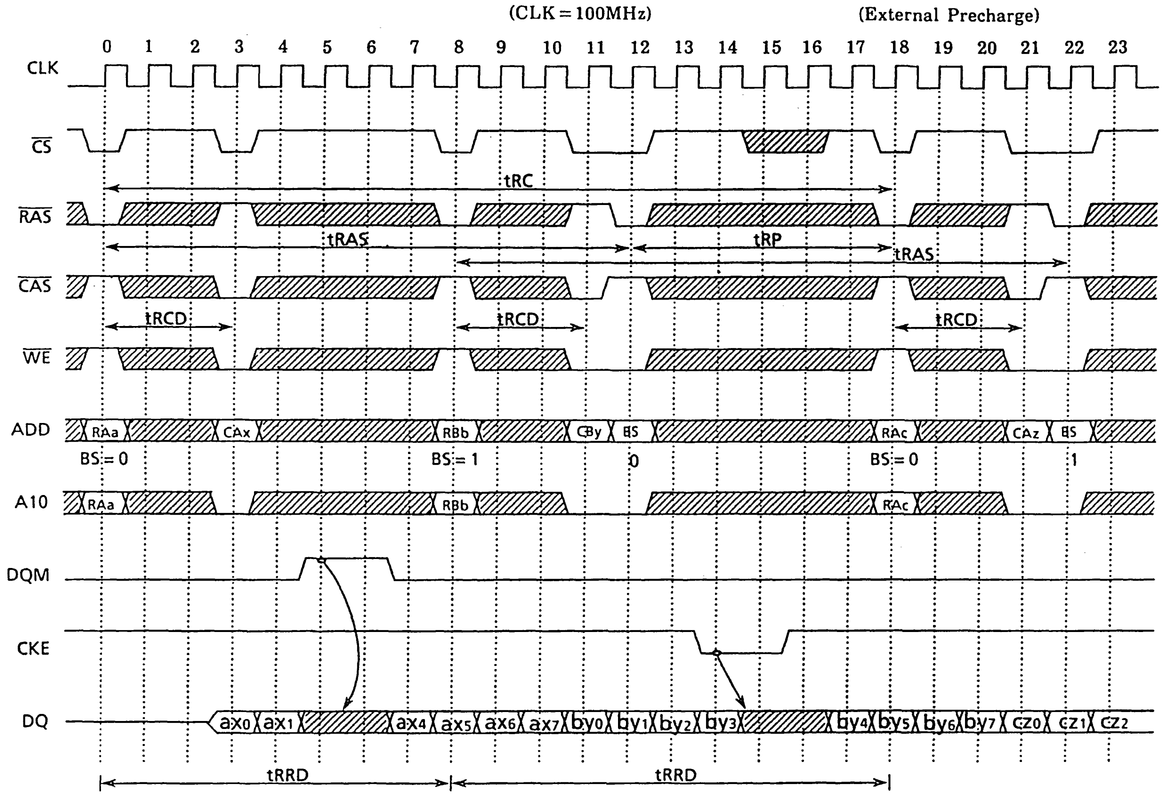
(CLK = 100MHz) (Auto Precharge)



16M Synchronous DRAM

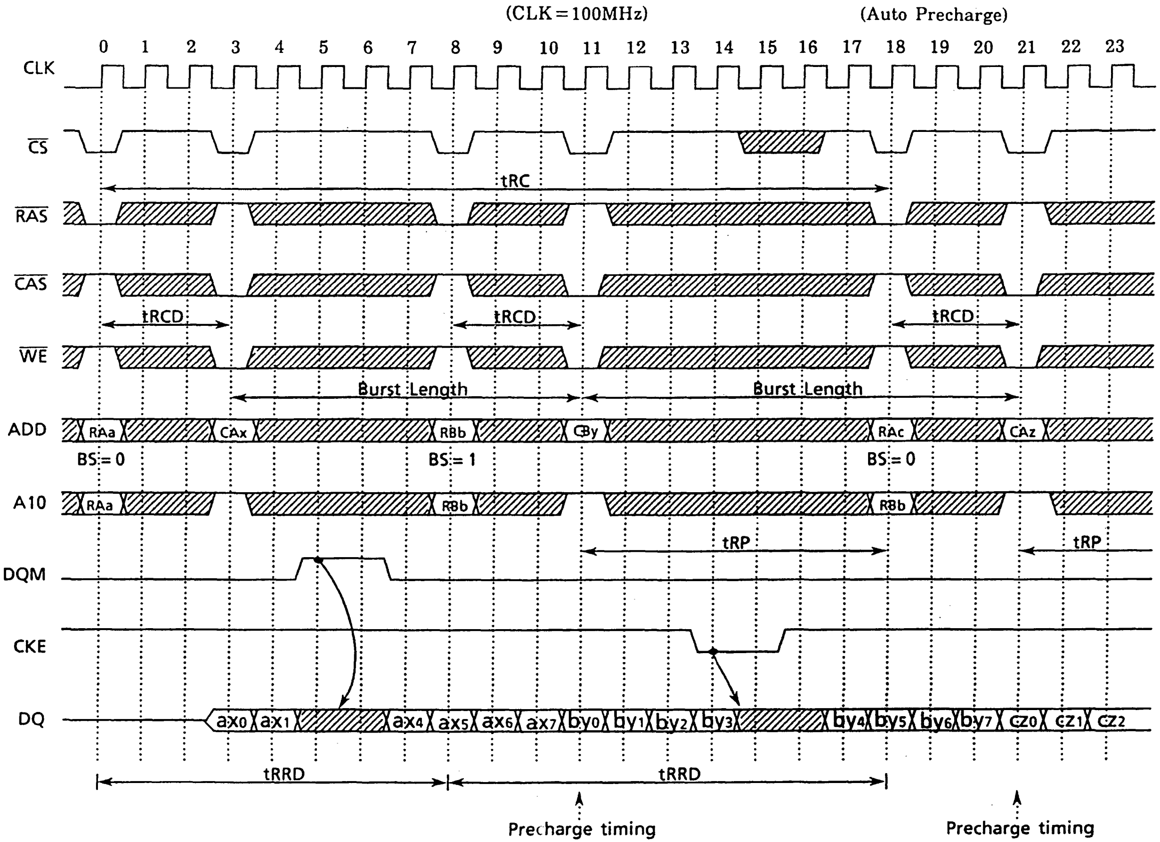
INTERLEAVED BANK WRITE (8 WRAP MODE)

Figure 7-1



INTERLEAVED BANK WRITE (8 WRAP MODE)

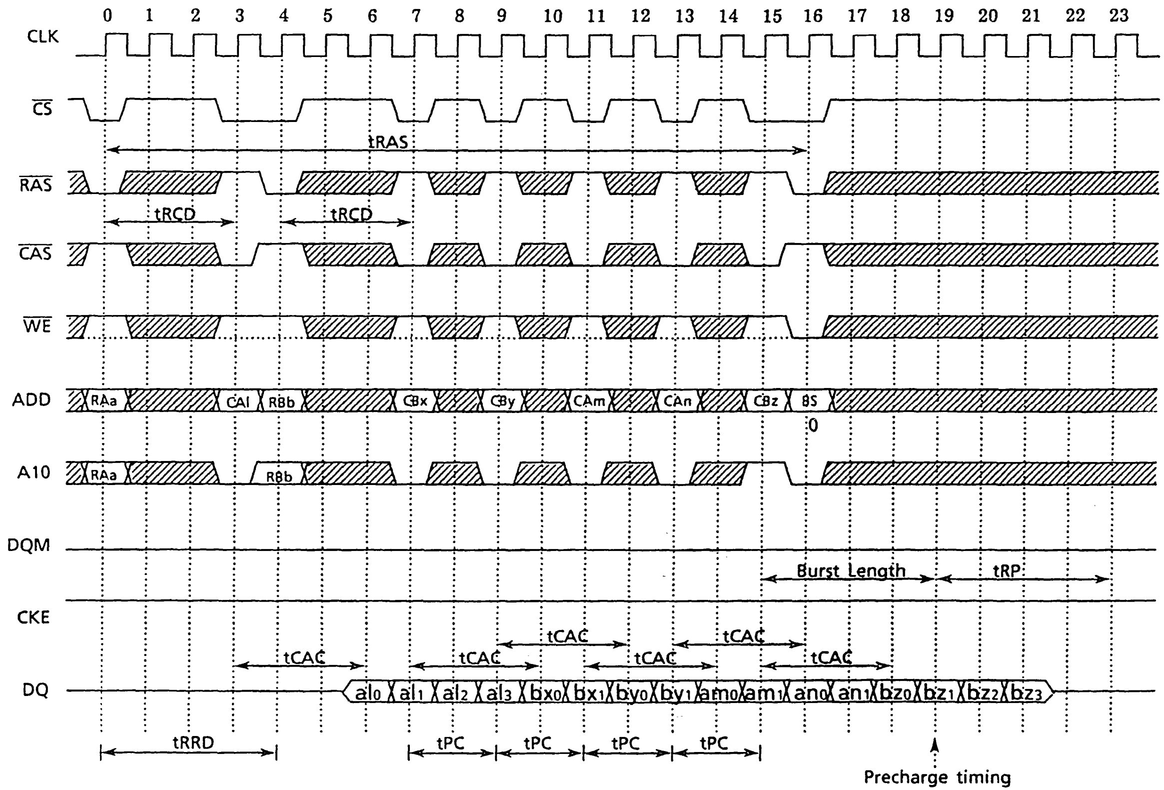
Figure 7 - 2



ACTIVE PAGE RANDOM READ (4 WRAP MODE)

Figure 8

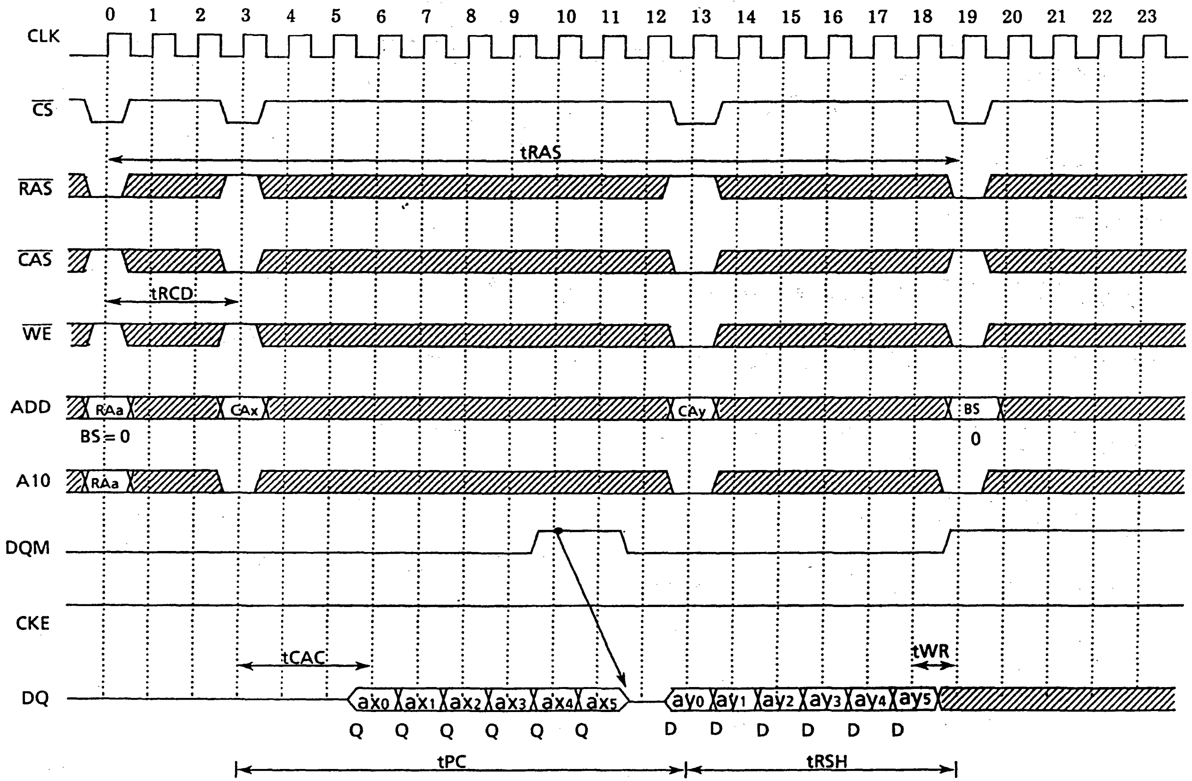
(CLK = 100MHz)



ACTIVE PAGE READ TO WRITE (8 WRAP MODE)

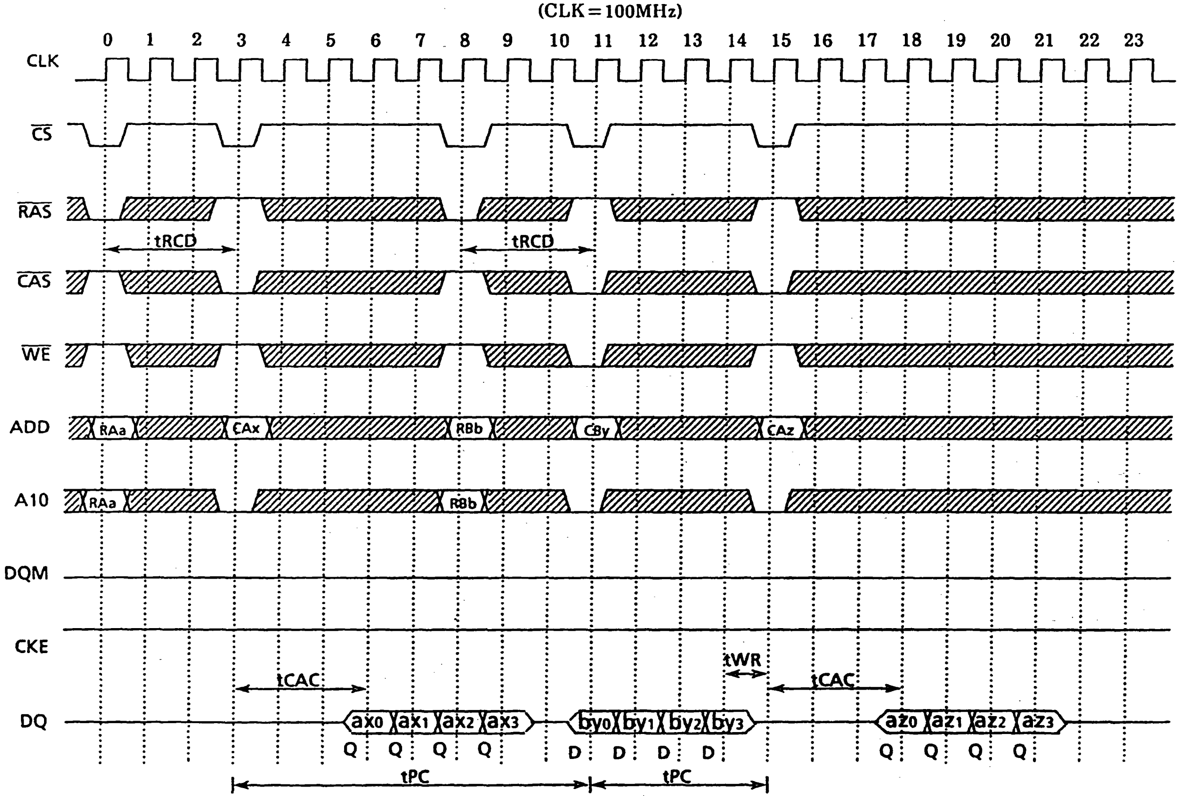
Figure 9

(CLK = 100MHz)



ACTIVE PAGE READ-WRITE-READ (4 WRAP MODE)

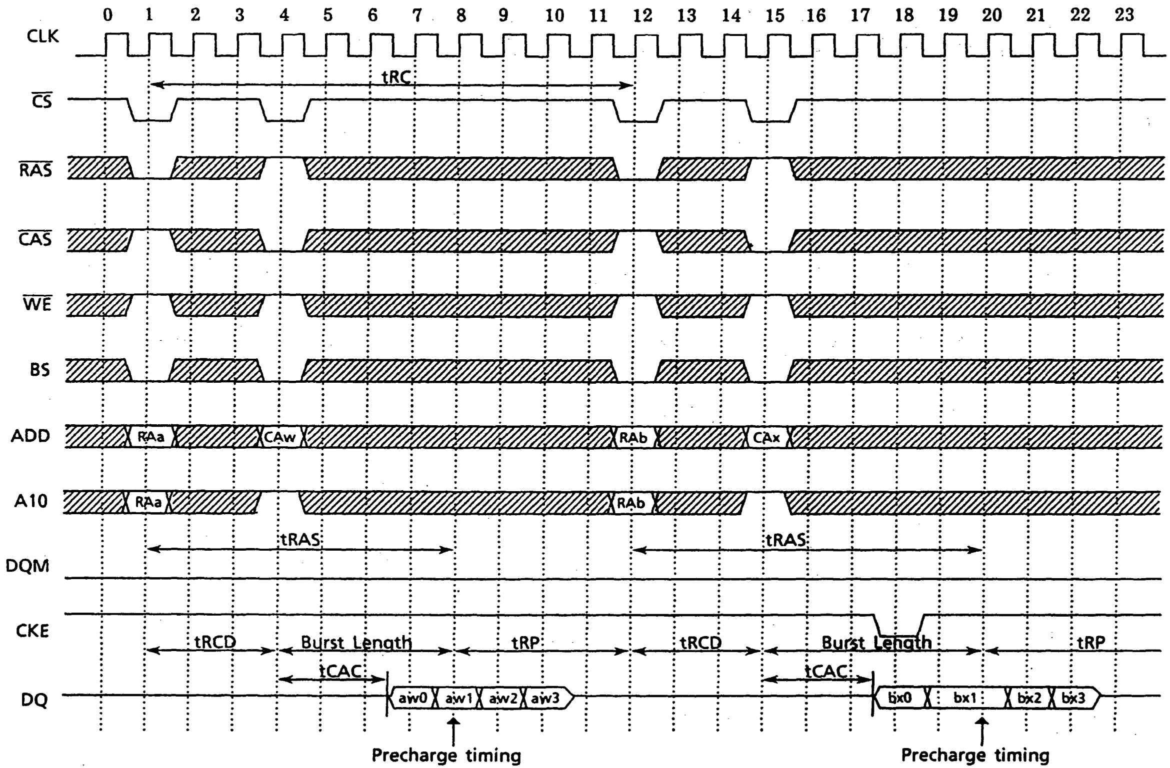
Figure 10



READ AND AUTOPRECHARGE (4 WRAP MODE)

Figure 11

(CLK = 100MHz)



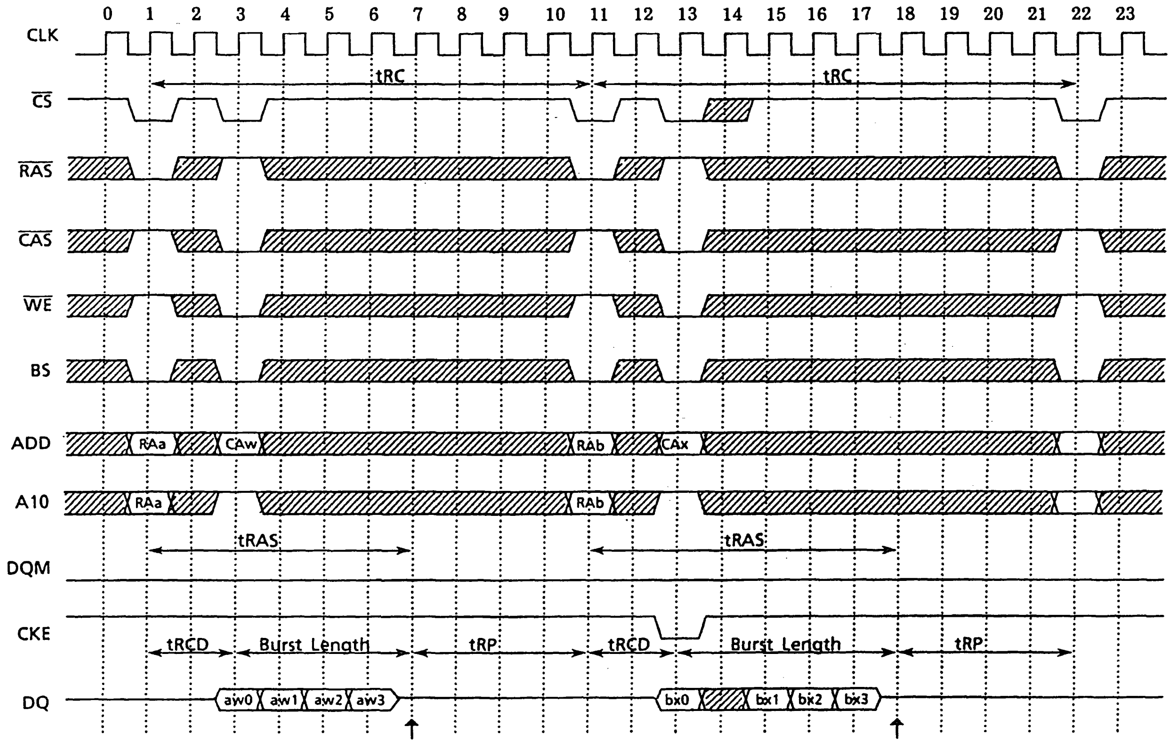
Note : Internal Precharge is performed at tRCD + Burst Length.

16M Synchronous DRAM

WRITE AND AUTOPRECHARGE (4 WRAP MODE)

Figure 12

(CLK = 100MHz)



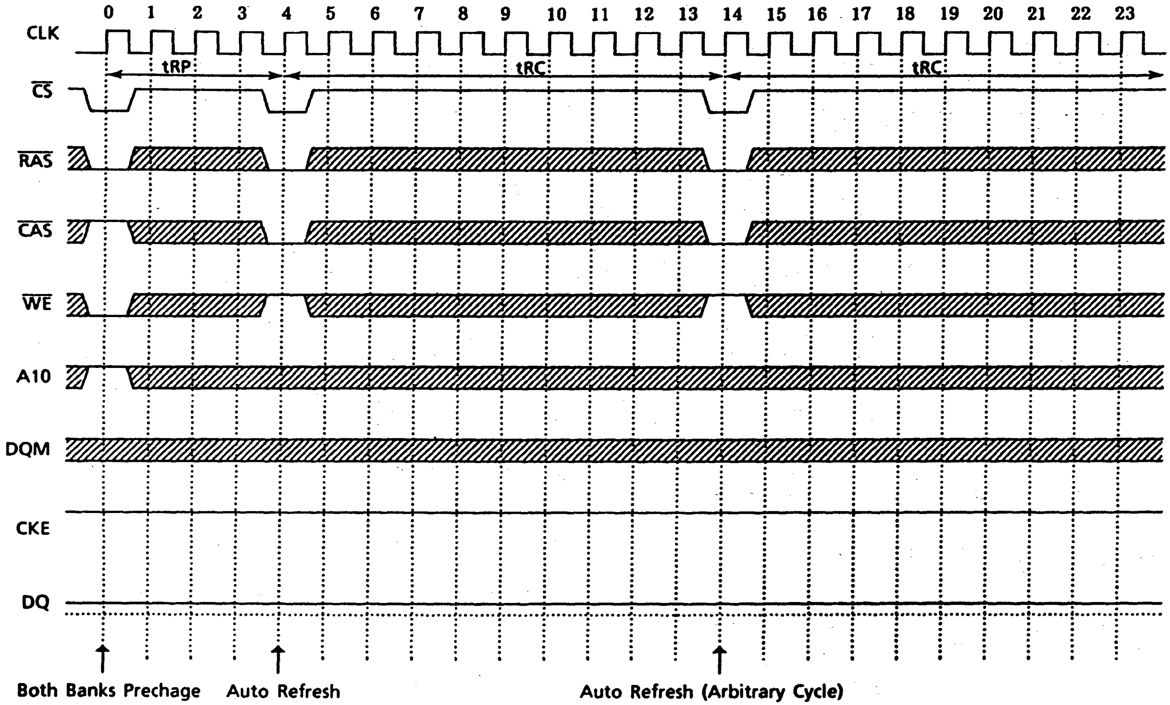
Note : Internal Precharge is performed at tRCD + Burst Length.

16M Synchronous DRAM

Figure 13

AUTO REFRESH CYCLE

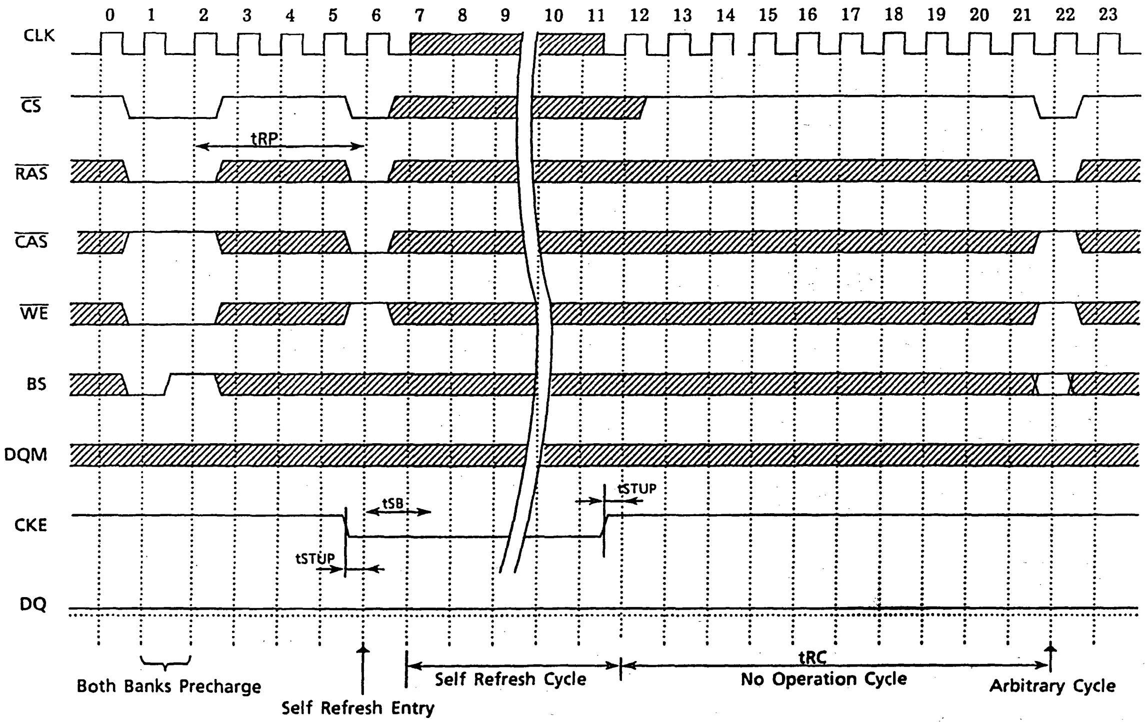
(CLK = 100MHz)



SELF REFRESH CYCLE

Figure 14

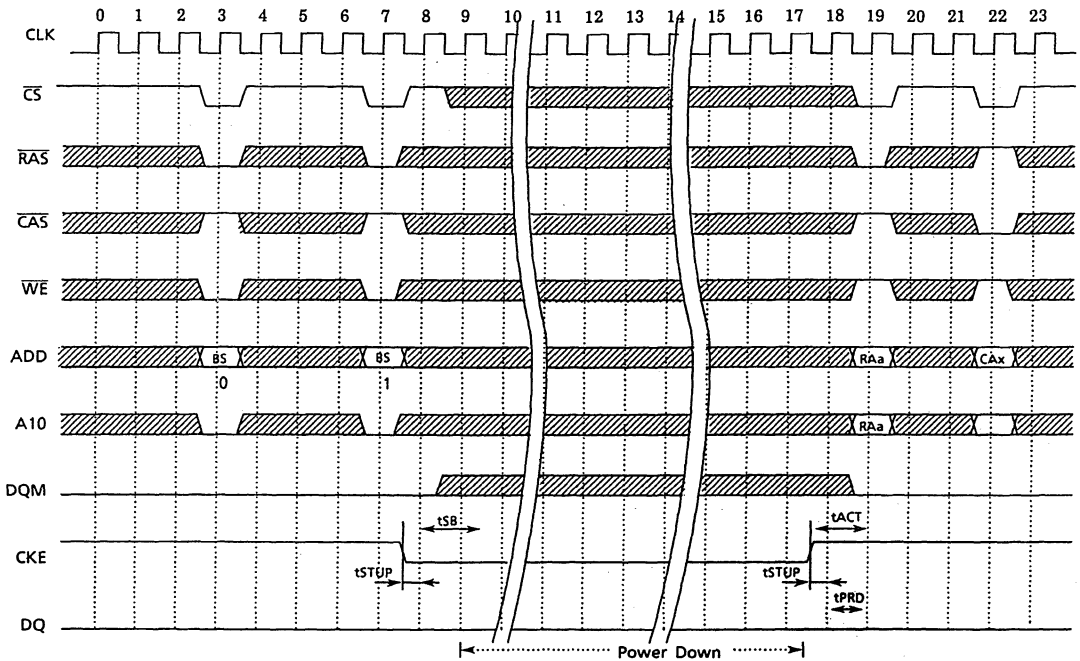
(CLK = 100MHz)



POWER DOWN MODE

Figure 15

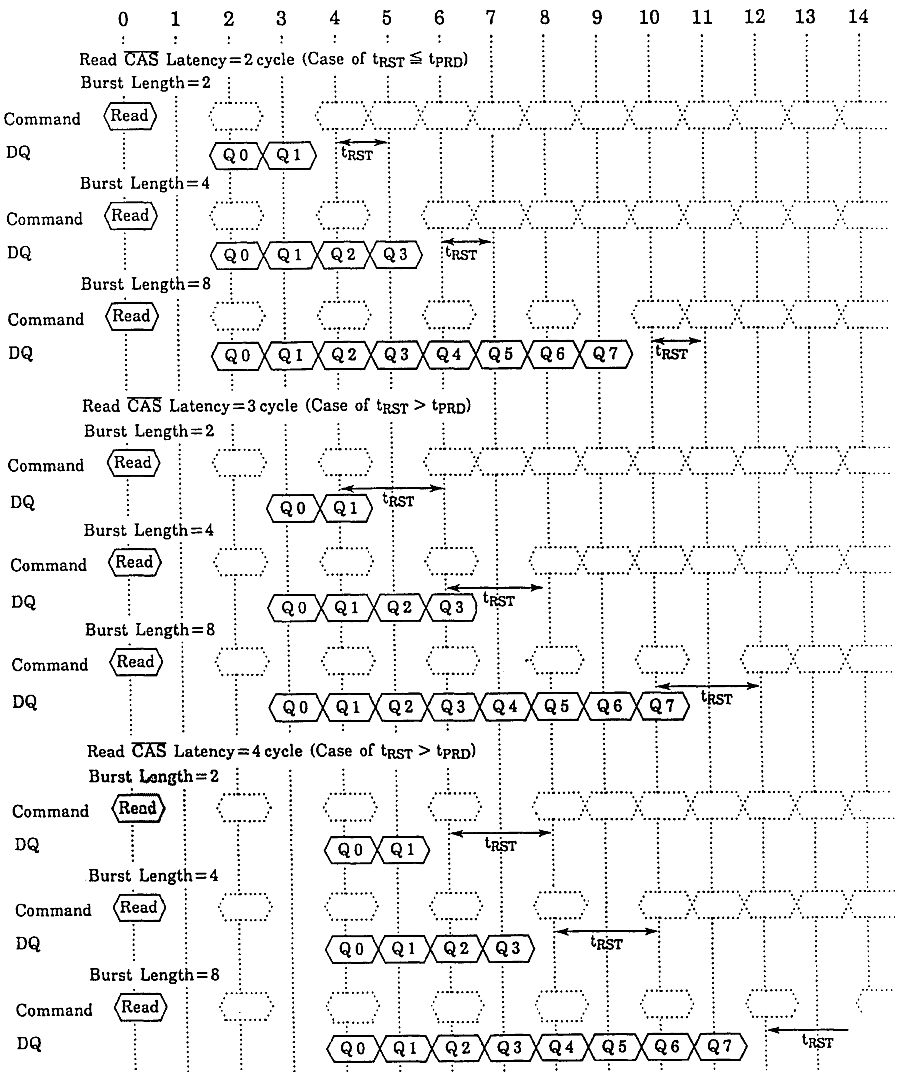
(CLK = 100MHz)



Note : The Power Down Mode is initiated with the CKE signal Low after two Banks percharged.
In Power Down Mode, the $\overline{RAS}$, $\overline{CAS}$, Add, $\overline{WE}$, DQM, $\overline{CS}$, and DQ Butter are inactive.
Exiting from the Power Down Mode, command input clock from CKE rising edge is specified by later case of tACT or tSTUP + tPR[illegible]

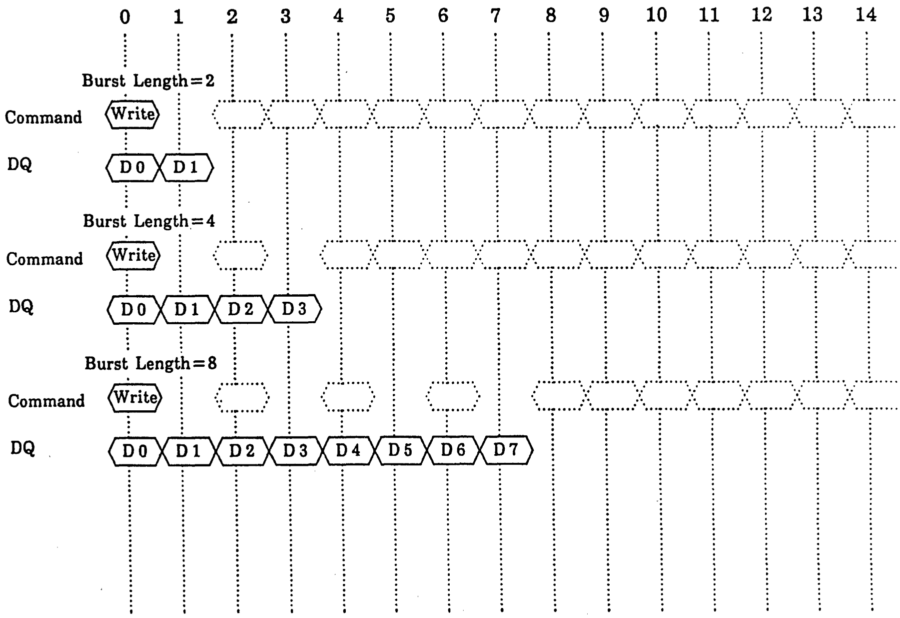
RESTRICTION OF FOLLOWING COMMAND FROM READ COMMAND

Figure 16



RESTRICTION OF FOLLOWING COMMAND FROM WRITE COMMAND

Figure 17



BURST READ INTERRUPTED

Figure 18

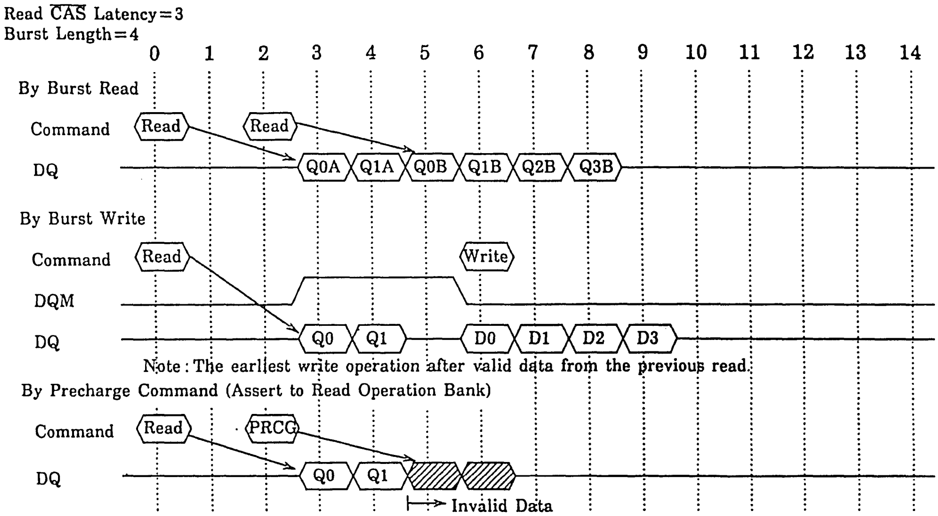
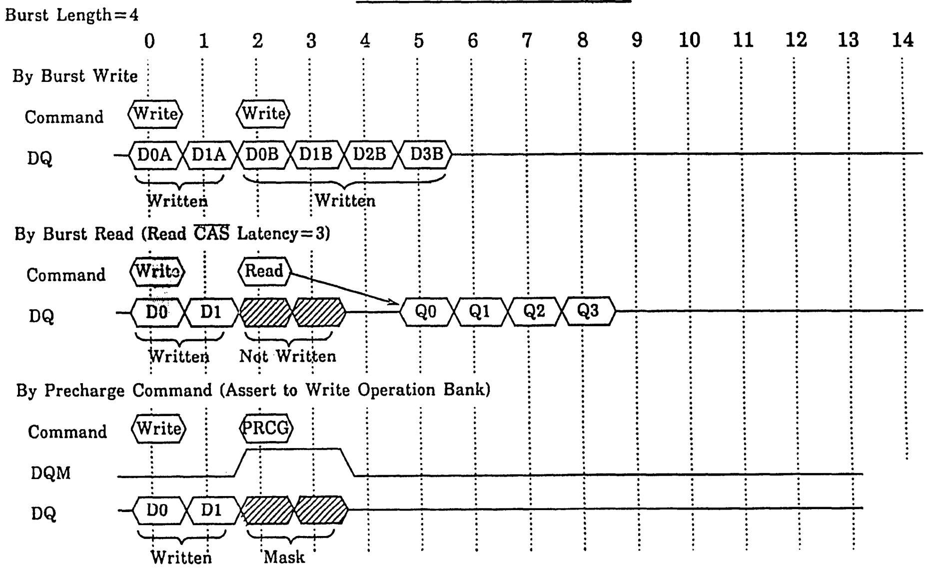


Figure 19

Burst Write Interrupted



SILICON GATE CMOS 512KX9 RDRAM™

target spec

DESCRIPTION

This a new generation ultra high speed CMOS Rambus™ DRAM organized as 512KX9. It uses advanced circuit design techniques with standard CMOS process technology. The sense amplifiers act as a cache and burst up to 256 bytes at a rate of 2 nanoseconds per byte.

FEATURES

- Rambus Interface:
  500 MB/sec peak transfer rate per RDRAM
  Low signal swing byte wide (9 bit) interface to the Rambus Channel
  Synchronous protocol for fast block-oriented transfers
  Flexible addressing controlled by on-chip registers
  Direct connection to Rambus ASICs, MPUs, and Peripherals
- 48 ns from beginning of read request to first byte, 2 ns per byte thereafter
- 2 cache lines per RDRAM - Each cache line is 1 KByte each
- RDRAM entirely self-contained, on-board $\overline{RAS}$/$\overline{CAS}$ and refresh logic
- Vertically oriented surface mount plastic package (SVP)

SYSTEM BENEFITS

- Eliminates second level caches
- Vastly imporves graphics performance at lower cost
- Decreases part count - Eliminates cache, buffers, address decoders, extra buses etc.
- Same pinout as 2MX9 RDRAM
- Full Rambus Channel performance in configurations as small as one RDRAM
- Alleviates need for expensive multi-chip modules at high system clock rates
- Systems are modular - faster MPUs and larger Rambus memories can be installed without changing board layout or logic design

PIN DESCRIPTION

SIGNAL	I/O	DESCRIPTION
BusData [0-8]	I/O	Bus data for request, write, and read protocols. These are low swing signals referenced to Vref. The data lines carry the request packet with the address, operation codes, as well as the count of the bytes to be transferred. Active low.
RxClk	I	Receive clock. This clock is aligned with incoming request and write data packets. This clock is completely synchronized with the request and data sent out on the Rambus™ Interface.
TxClk	I	Transmit clock: This clock is aligned with the data being sent out on reads as well as the acknowledge packets. This is a low swing signal referenced to Vref.
Vref	I	This is the logic threshold voltage for low swing signals.
BusCtrl	I/O	Control signal to frame packets, Transmit opcode, and acknowledge requests. Signal is active low.
BusEnable	I	Control signal to enable the bus. This signal is pulsed to power up the bus. Long assertions of this signal will reset all devices on the bus. Signal is active low.
Vdd, VddA		+5V power supply. VddA is a separate supply for clock receivers.
Gnd, GndA		Circuit ground. GndA is a separate ground for clock receivers.
SIn	I	Reset daisy chain input. TTL levels. Active high.
SOut	O	Reset daisy chain output. TTL levels. Active high.

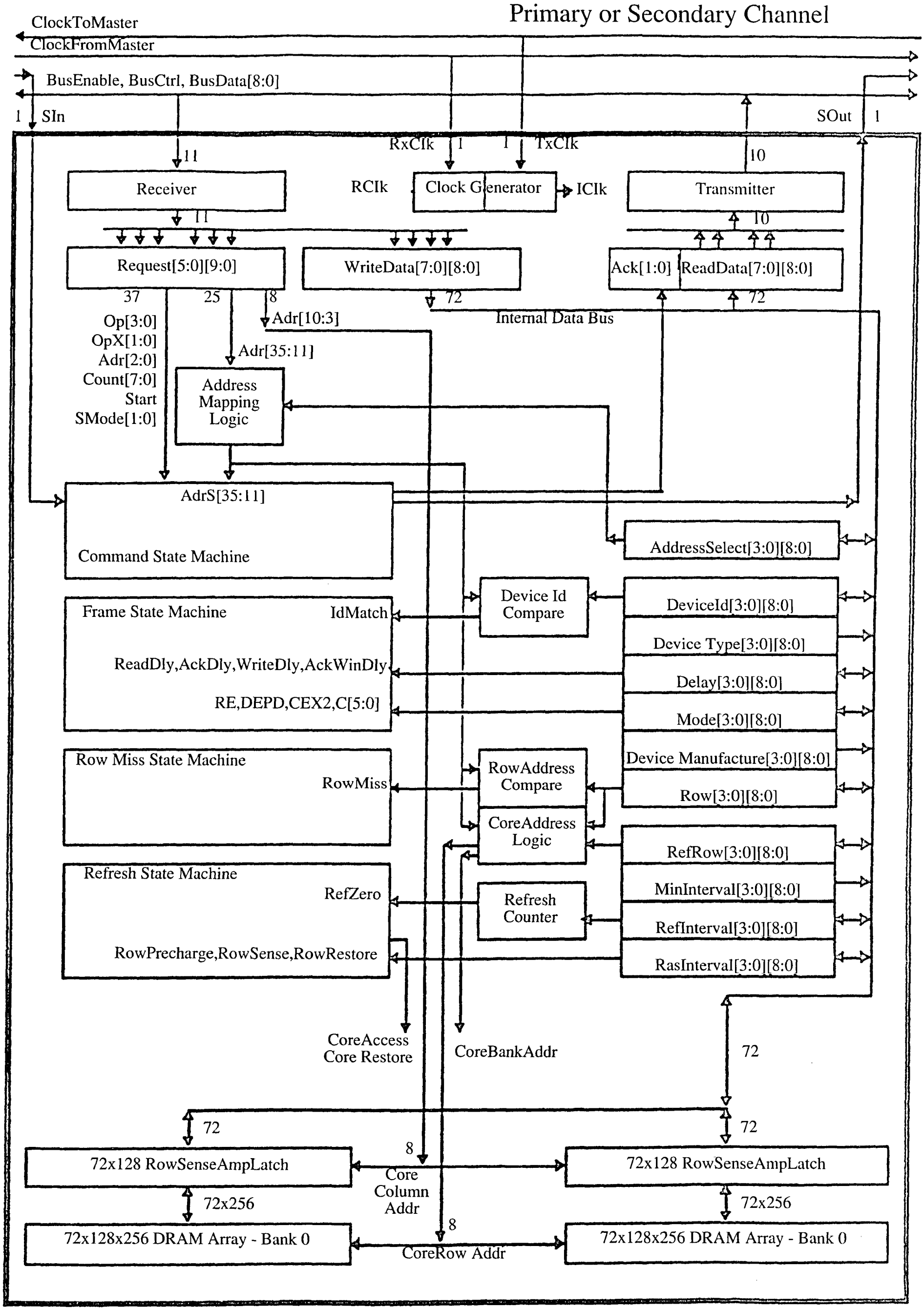
(1) VddA and GndA must be tied to VDD and Gnd, respectiviely where the RDRAM connects to the PC board.

PIN OUT

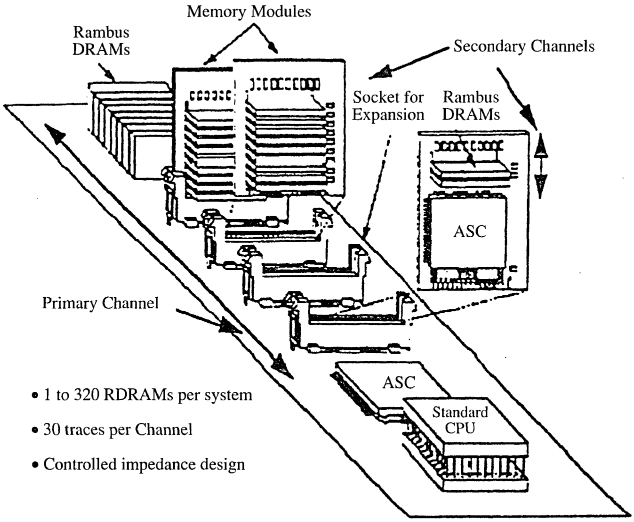
32 pin SVP SIP (TOP VIEW)

1	Vdd
2	Gnd
3	BusData8
4	Gnd
5	BusData7
6	(NC)
7	Bus Enable
8	Vdd
9	BusData6
10	Gnd
11	BusData5
12	VddA
13	RxClk
14	GndA
15	TxClk
16	Vdd
17	BusData4
18	Gnd
19	BusCtrl
20	SIn
21	Vref
22	SOut
23	BusData3
24	Gnd
25	BusData2
26	(NC)
27	BusData1
28	Gnd
29	BusData0
30	(NC)
31	Gnd
32	Vdd

BLOCK DIAGRAM



SYSTEM CONFIGURATION



PROTOCOL

The RDRAM responds to bus transactions initiated by a Rambus master device. The Rambus master sends out a request packet on the Rambus Channel and all RDRAM devices on the bus receive the information in the request packet. The request packet contains address and control information necessary to specify the transaction. The transaction can be a read or write operation from or to a block of memory, and can be between one and 256 bytes in length. The RDRAM examines the contents of each request packet to determine the required action. If the address in the packet targets this particular RDRAM, then it replies with an Achnowledge packet which indicates to the master whether the RDRAM can service the request. For memory write transactions, the master follows the request packet with the write data packet, which is stored into the RDRAM's core column sense amplifiers. For memory read transactions, the RDRAM reads data from the RDRAM core's sense amplifiers and sends it to the master. The interval between the request packet and the following acknowledge and data packets is programmable during device initialization. Once programmed, the delays are fixed during normal operation.

CACHING

Each RDRAM contains two completely independent direct mapped cache banks. Each bank has its own memory core sub-array, sense amplifiers, and cache tag. The Rambus Interface circuitry manages both the memory core and cache operation. The master only needs to retry those transactions that cause a miss. Each cache in the RDRAM is 1 KByte. The 1 KByte cache size contributes to a significant hit rate to those caches and the access time to data in these caches is low. If the data specified by the request packet is not available in the sense amplifiers, the RDRAM begins a row access operation to write back the current row and retrieve the requested row. Simultaneously, the RDRAM sends a negative Acknowledge packet to the requesting master device. The master may then retry the operation a Retry time later. The most recently requested rows are latched in the sense amplifiers until the master requests a new row. The sense amplifiers thus act as a cache for very fast read and write accesses.

ADDRESSING

Unlike traditional DRAMs, each RDRAM decodes its own addresses. The mapping of addresses to Rambus devices is set during device initialization. The address mapping is very flexible, supporting device interleaving and mixing of Rambus devices of various sizes and types. Address mapping, self-refresh, packet interval timing, and other functions are controlled by use of on-chip registers. Registers are accessed using the same read and write transactions as memory, but are located in a separate address space.

ABSOLUTE MAXIMUM RATINGS

The following table represents stress ratings only, and functional operation at the maximums is not guaranteed. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although devices contain protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{IN, ABS}$	Voltage applied to any low-swing pin with respect to Gnd	-0.5	Vdd+0.5	V
$V_{IN, TTL, ABS}$	Voltage applied to any TTL pin with respect to Gnd	-0.5	Vdd+0.5	V
$V_{DD, ABS}$	Voltage on VDD with respect to Gnd	-0.5	6.5	V
$T_{J, ABS}$	Junction temperature under bias	-55	125	°C
T_{STORE}	Storage temperature	-55	125	°C

THERMAL PARAMETERS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_J	Junction operating temperature	0	100	°C
θ_{JC}	Junction-to-Case thermal resistance		TBD	°C/Watt

CAPACITANCE

SYMBOL	PARAMETER and CONDITIONS	MIN.	MAX.	UNIT
$C_{IN,TTL}$	TTL input parasitic capacitance		10	pF
$C_{OUT,TTL}$	TTL output parasitic capacitance		15	pF

RECOMMENDED ELECTRICAL CONDITIONS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}, V_{DDA}	Supply voltage	4.5	5.5	V
V_{REF}	Reference voltage	1.9	2.4	V
V_{IL}	Input low voltage	V_{REF}-0.4	V_{REF}-0.2	V
V_{IH} Input high voltage	Input high voltage	V_{REF}+0.2	V_{REF}+0.4	V
$V_{IL, TTL}$	TTL input low voltage	-0.5	0.8	V
$V_{IH, TTL}$	TTL input high voltage	2.0	V_{dd} + 0.5	V

ELECTRICAL CHARACTERISTICS.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
I_{REF}	V_{REF} current @ V_{REF}=2.4V	-10	10	µA
I_{IN}	Input current @ ($0 \le V_{IN} \le V_{DD}$)	-10	10	µA
I_{OL}	Output low current (at maximum programmed value) @ V_{OUT} = 1.6V to 2.2V		35	mA
Δ_{IOL}	Error in programmed output low current (from unit to unit)	-0.55	0.55	mA
I_{OH}	Output high current @ V_{OUT} = 2.0V to 2.7V	-10	10	µA
$I_{IN, TTL}$	TTL input leakage current @ ($0 \le_{VIN, TTL} \le V_{DD}$)	-10.0	10.0	µA
$V_{OL, TTL}$	TTL output voltage @ V_{OL}=1.0mA		0.4	V
$V_{OH, TTL}$	TTL output high voltage @ V_{OH}=-0.25mA	2.4		V

RECOMMENDED TIMING CONDITIONS.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CR}, t_{CF}	TxClk and RxClk input rise and fall times	0.3	0.7	ns
t_{CYCLE}	TxClk and RxClk cycle times	4	10	ns
t_{CH}, t_{CL}	TxClk and RxClk high and low times	1.3	t_{CYCLE} -1.3	ns
I_{TR}	TxClk-RxClk differential	0	t_{CYCLE} -1.2	ns
t_{DR}, t_{DF}	Data/Control input rise and fall times	0.3	0.7	ns
t_{QR}, t_{QF}	Data/Control output rise and fall times	0.4	0.6	ns
t_S	Data/Control-to-RClk setup time	0.3		ns
t_H	RClk-to-Data/Control hold time	0.3		ns
t_{REF}	Refresh interval		16	ms
t_{LOCK}	RDRAM internal clock generator lock time	10		µs

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{SD}	SIn-to-SOut propagation delay @ $C_{LOAD, TTL}$=40pF	5	50	ns
t_Q	TClk-to-Data/Control output time	$t_{CYCLE}/4$ +0.3	$t_{CYCLE}/4$ +0.3	ns

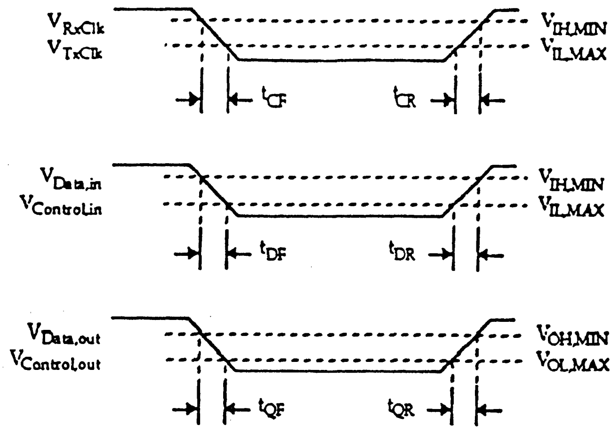
RAMBUS CHANNEL TIMING

The Rambus channel timings shown below are presented to show important timings on the Rambus channel for common operations. Please refer to the detailed Rambus Technology Guide for all possible interactions that could occur on the Rambus channel. All timings are from the point of view of the channel master, and thus have the bus over head delay of 4ns per bus transversal included.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYCLE}	TxClk and RxClk cycle times	4	10	ns
$t_{RESPONSE}$	Start of request packet to Ack or Nack	7(1)	10(1)	t_{CYCLE}
$t_{READHIT}$	Start of request packet to first read data for Row Hit	12(1)	15(1)	t_{CYCLE}
$t_{WRITEHIT}$	Start of request packet to start of write data	4(1)	7(1)	t_{CYCLE}
$t_{READRETRY}$	Start of RowMiss packet to RowMatch packet	26(2)		t_{CYCLE}
$t_{WRITERETRY}$	Start of RowMiss packet ot RowMatch packet	26(2)		t_{CYCLE}
$t_{READBURST32}$	Start of request packet to end of 32 byte read for Row Hit	28(3)		t_{CYCLE}
$t_{READBURST256}$	Start of request packet to end of 256 byte read for Row Hit	140(3)		t_{CYCLE}
$t_{WRITEBURST32}$	Start of request packet to end of 32 byte write for Row Hit	20(4)		t_{CYCLE}
$t_{WRITEBURST256}$	Start of request packet to end of 256 byte write for Row Hit	132(4)		t_{CYCLE}

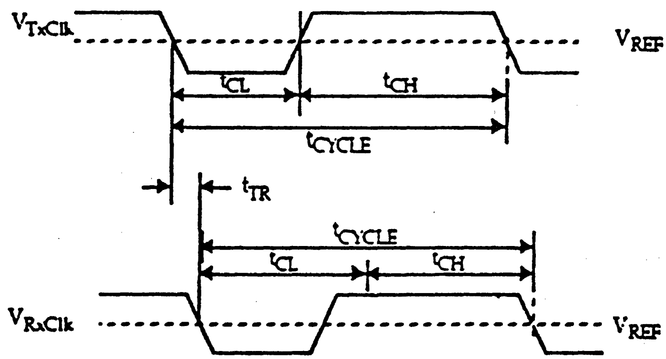
(1) Programmable
(2) Minimum at $t_{CYCLEMIN}$. Delay programmable to give equivalent timings at long t_{CYCLE}
(3) Calculated with $t_{READHITMIN}$
(4) Calculated with $t_{WRITEHITMIN}$

RISE/FALL TIMING

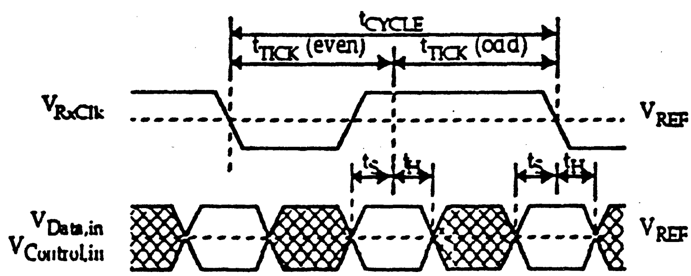


Where:
$V_{OH,MIN} = V_{TERM} - Z_O * (I_{OH,MIN})$
$V_{OL,MAX} = V_{TERM} - Z_O * (I_{OL,MAX} * \text{programmed value})$

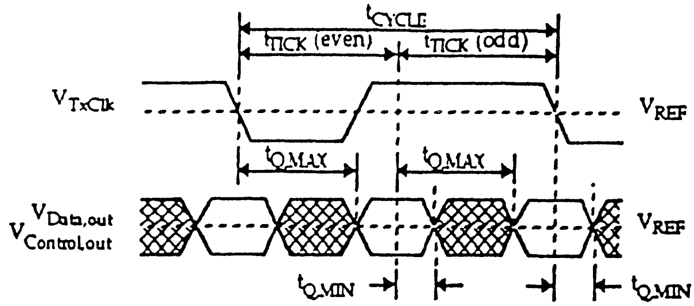
CLOCK TIMING



RECEIVE DATA TIMING

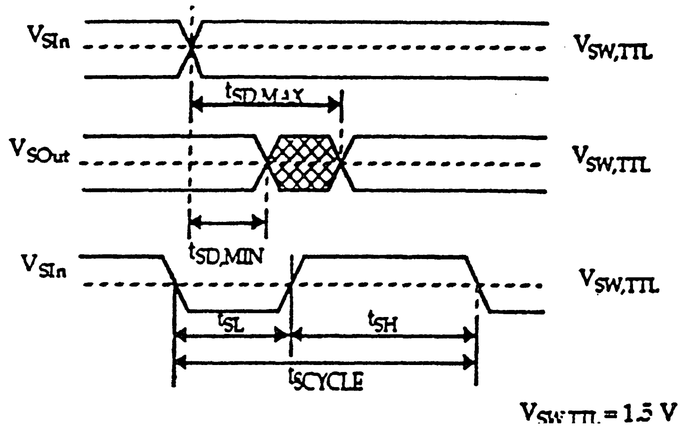


RISE/FALL TIMING

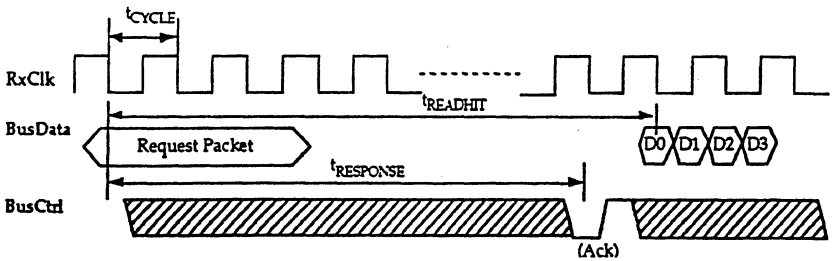


* t_{TICK} is defined as one-half t_{CYCLE}.

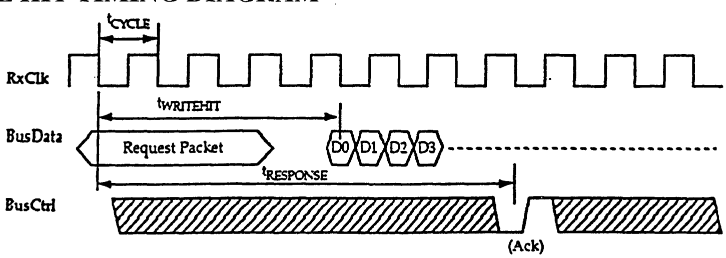
SERIAL CONFIGURATION PIN TIMING



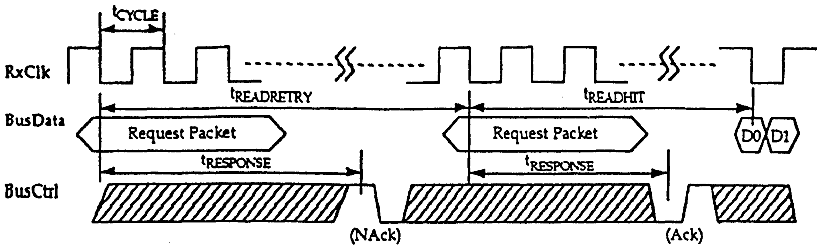
READ HIT TIMING DIAGRAM



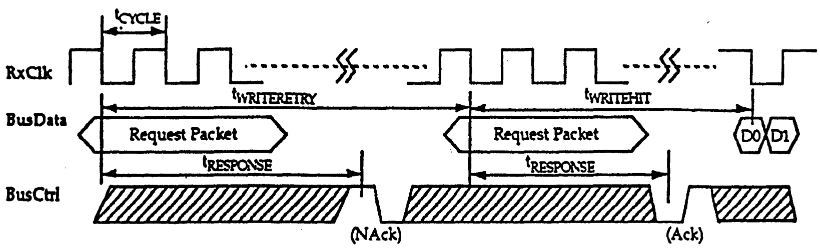
WRITE HIT TIMING DIAGRAM



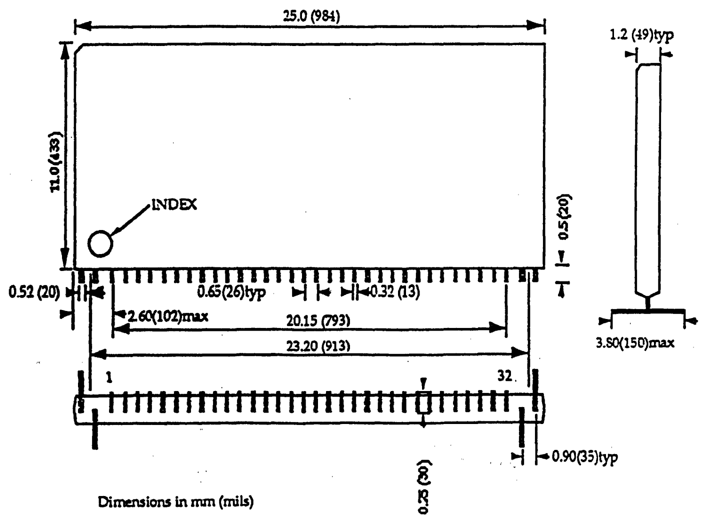
READ MISS TIMING DIAGRAM



WRITE MISS TIMING DIAGRAM



SURFACE VERTICAL PACKAGE (SVP) PACKAGE OUTLINE MM (MILS)



SILICON GATE CMOS 18 Mbit RDRAM™

target spec

DESCRIPTION

The TC59R1609VK is a new generation ultra high speed CMOS Rambus™ DRAM organized as 2MX9. The TC59R1609VK uses advanced circuit design techniques with standard CMOS process technology. It utilizes the sense amplifiers as a cache and bursts up to 256 bytes at a rate of 500 MBytes per second.

FEATURES

- Rambus Interface:
  500 MB/sec peak transfer rate per RDRAM
  Low signal swing byte wide (9 bits) interface to the Rambus Channel
  Synchronous protocol for fast block-oriented transfers
  Flexible addressing controlled by on-chip registers
  Direct connection to Rambus ASICs, MPUs, and Peripheral
- Multiple cache lines per RDRAM
- RDRAM entirely self-contained
- Vertical surface mount package

SYSTEM BENEFITS

- Same pinout as 4.5 Mbit TC59R0409VK RDRAM
- Incremental memory granularity is 2 MB
- Alleviates need for expensive multi chip modules at high system clock rates
- Systems are modular - faster controllers and larger Rambus memories can be installed without changing board layout or logic design

PIN DESCRIPTION

SIGNAL	I/O	DESCRIPTION
BusData [0-8]	I/O	Bus data for request, write, and read protocols. These are low swing signals referenced to Vref. The data lines carry the request packet with the address, operation codes, as well as the count of the bytes to be transferred. Active low.
RClk	I	Receive clock. This clock is aligned with incoming request anad write data packets. This clock is completely synchronized with the request and data sent out on the Rambus™ Interface.
TClk	I	Transmit clock: This clock is aligned with the data being sent out on reads as well as the acknowledge packets. This is a low swing signal referenced to Vref.
Vref	I	This is the logic threshold voltage for low swing signals.
BusCtrl	I	Control signals to frame packets, Transmit opcode, and acknowledge requests. Signal is active low.
BusEnable	I	Control signals to enable the bus. This signal is pulsed to power up the bus. Long assertions of this signal will reset all devices on the bus. Signal is active low.
Vdd, VddA		+5V power supply. VddA is a separate supply for clock receivers.
Gnd, GndA		Circuit ground. GndA is a separate ground for clock receivers.
SIn	I	Reset daisy chain input. CMOS levels. Active high.
SOut	O	Reset daisy chain output. CMOS levels. Active high.

PIN OUT

32 pin SMT SIP (TOP VIEW)

1	Vdd
2	Gnd
3	BusData8
4	Gnd
5	BusData7
6	(NC)
7	Bus Enable
8	Vdd
9	BusData6
10	Gnd
11	BusData5
12	VddA
13	RClk
14	GndA
15	TClk
16	Vdd
17	BusData4
18	Gnd
19	BusCtrl
20	SIn
21	Vref
22	SOut
23	BusData3
24	Gnd
25	BusData2
26	(NC)
27	BusData1
28	Gnd
29	BusData0
30	(NC)
31	Gnd
32	Vdd

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
RClk	Receive Clock Frequency	100	250	MHz
TClk	Transmit Clock Frequency	100	250	MHz

FIGURE 1. READ HIT TIMING DIAGRAM

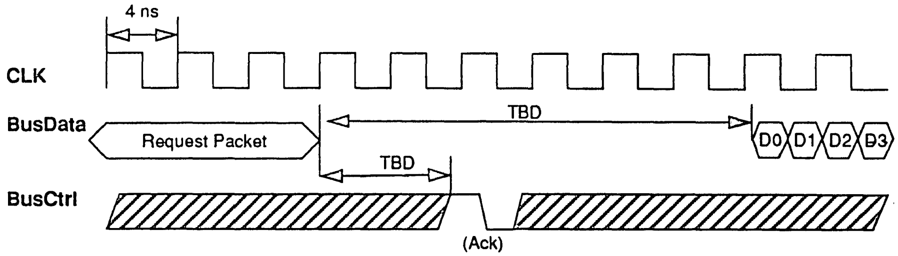


FIGURE2. WRITE HIT TIMING DIAGRAM

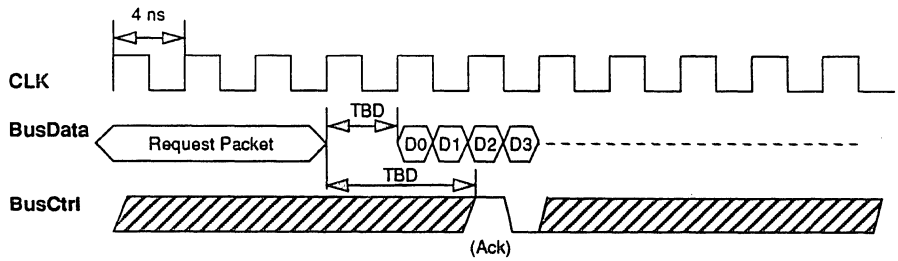


FIGURE 3. READ MISS TIMING DIAGRAM

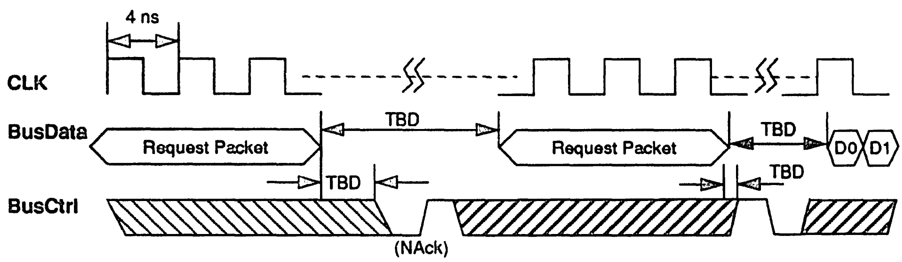
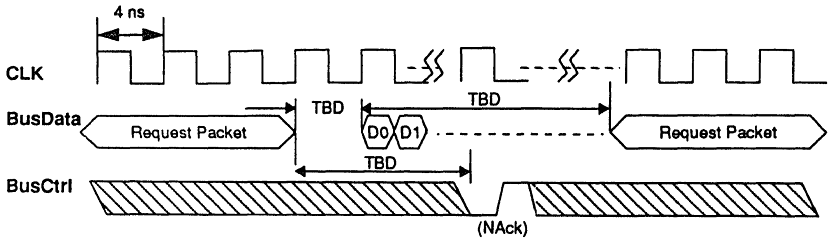
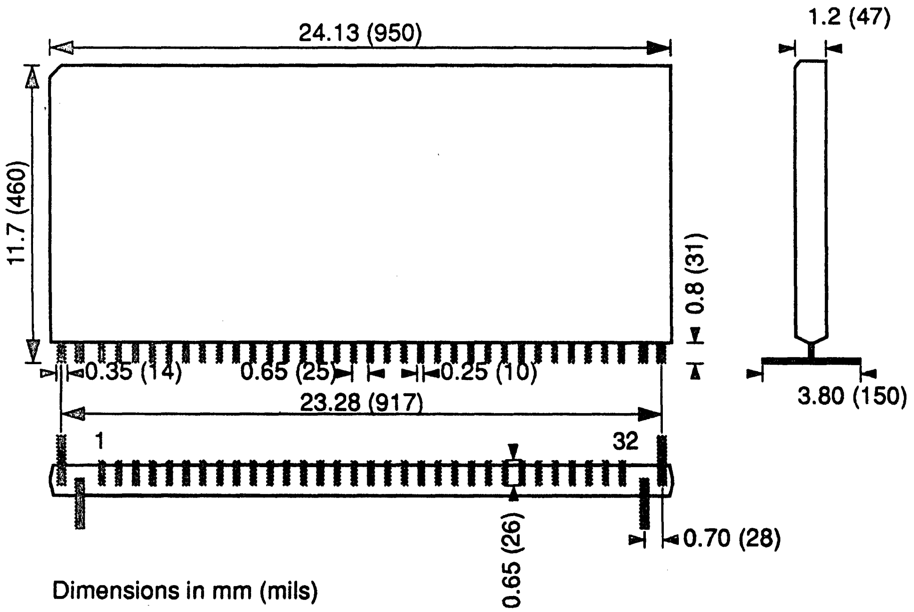


FIGURE 4. WRITE MISS TIMING DIAGRAM



PACKAGE OUTLINE MM (MILS)



Dimensions in mm (mils)

256KX4 VIDEO RAM APPLICATION NOTE

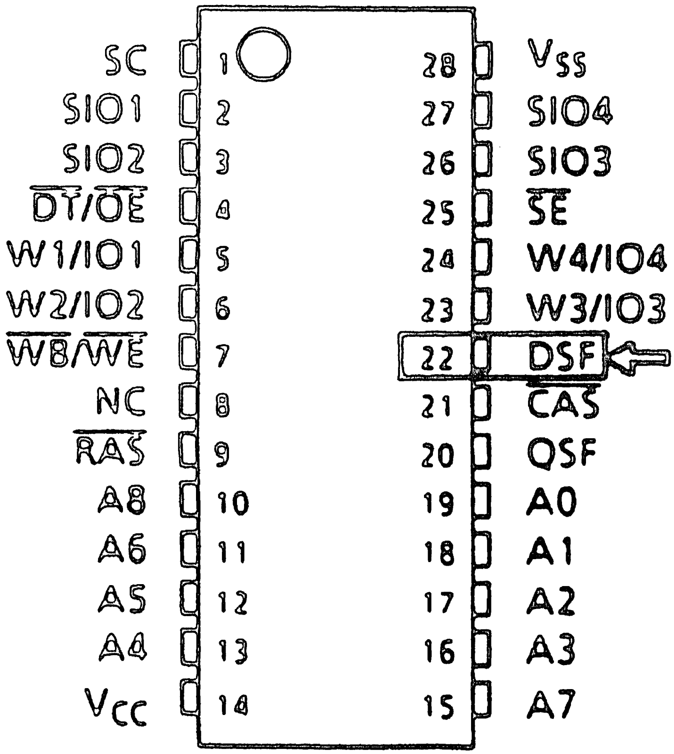
The TC524258 can be used in a TC524256 basic feature application if:

1) DSF (Pin 29) is grounded
2) QSF (Pin 26) is open (N/C)
3) If using Write Transfer function, see note below.

Due to the complexity of the VRAM device, we highly recommend that the customer perform system testing to ensure proper operation and compatibility.

Note: The TC524256B uses "Write Transfer" and the TC524258B uses "Masked Write Transfer". Therefore, the I/O at $\overline{RAS}$ falling edge must be "1" to ensure that data will not be masked. Please refer to Datasheet for details.

TC524258BJ



128KX8 VIDEO RAM APPLICATION NOTE

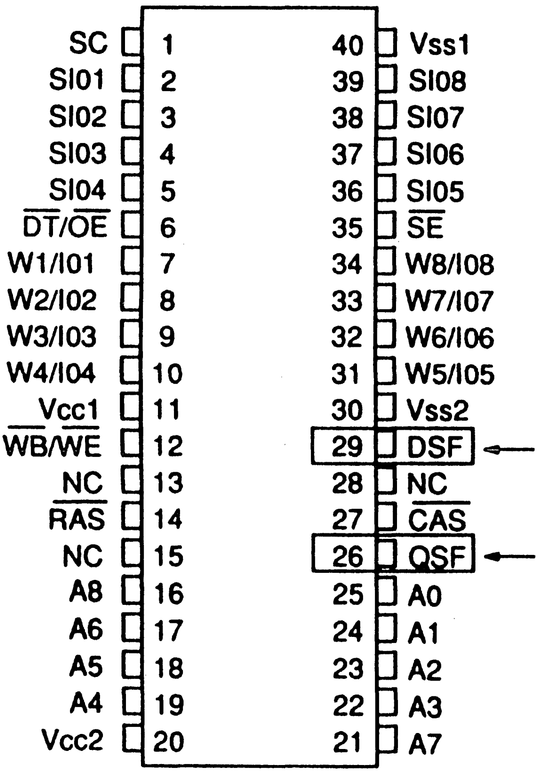
The TC528128 can be used in a TC528126 basic feature application if:

1) DSF (Pin 29) is grounded
2) QSF (Pin 26) is open (N/C)
3) If using Write Transfer function, see note below.

Due to the complexity of the VRAM device, we highly recommend that the customer perform system testing to ensure proper operation and compatibility.

Note: The TC528126B uses "Write Transfer" and the TC528128B uses "Masked Write Transfer". Therefore, the I/O at RAS falling edge must be "1" to ensure that data will not be masked. Please refer to Datasheet for details.

TC528128BJ



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