8000 Series Components Manual

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Tundra Semiconductor Corporation: formerly Newbridge Microsystems.

8000 Series Components Manual

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Corporate Profile

Tundra Semiconductor Corporation is a privately-held, international, fabless semiconductor company focused on the design, development and delivery of bus-bridging components for embedded systems. Previously Newbridge Microsystems, a division of Newbridge Networks Corporation, Tundra commenced operations under its new name on December 18, 1995.

Our mission statement is simple: We at Tundra are committed to providing high-quality components that enable embedded systems designers to get to market faster with a more competitive product. Tundra takes a 'total product solution' approach to new products, with evaluation boards, executable models, device drivers, application notes, and manuals, in addition to our acclaimed applications engineering support.

Tundra offers a well accepted and expanding family of VMEbus bus-bridging components, plus a growing line of embedded PCI bus-bridging chips that support processors such as the Motorola® 68K and QUICC™ and PowerQUICC™ lines.

In addition, we offer a family of DES (Data Encryption Standard) -based encryption chips as well as a line of industry-standard 8000 Series peripheral IC's.

HEADQUARTERS

603 MARCH RD
KANATA, ON K2K 2M5
CANADA
Tel: 613-592-0714
Fax: 613-592-1320

or from within North America
Tel: 1-800-267-7231

Visit our website at:
www.tundra.com
Email: support@tundra.com

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Section 1

1 Product Index and Ordering

1.1 How to Order

This chapter is organized into the following sections:

- “Product Listing” on page 1-2, lists our entire 8000 series product family.
- “8000 Series Product Index” on page 1-2, shows you the valid option codes for each of our devices. It also points to related technical and mechanical information for each device.
- “Ordering Information and Product Code” on page 1-3, lists Tundra’s packaging, temperature and speed codes.
- “Product Cross Reference” on page 1-4, compares our 8000 series products with similar products of other companies.
- “Package Codes and Mechanicals” on page 1-6, provides a mechanical drawing of each package type.

To use this chapter effectively, determine which of our devices best suits your needs by using the Product Listing on the following page. Then, use the Ordering Information and Product Code tables to help you find the product that matches your system requirements.

If you require any assistance call the nearest Representative, Distributor, or our factory to place an order. (See “Worldwide Sales Network” on page Sales-1.)

1.2 Product Listing

		Ordering Information Page	Package Codes and Mechanicals Page	Technical Information Page
8000 Series Products				
CA80C85B	High Performance 8-Bit CMOS Processor	1-1	1-8	2-1
CA82C37A	Programmable DMA Controller	1-1	1-8, 1-10	2-17
CA82C52	CMOS Serial Controller Interface	1-1	1-7, 1-9	2-45
CA82C54	Programmable Interval Timer	1-1	1-6, 1-9	2-69
CA82C55A	Programmable Peripheral Interface	1-1	1-8, 1-10	2-91
CA82C59A	Programmable Interrupt Controller	1-1	1-7, 1-9	2-123

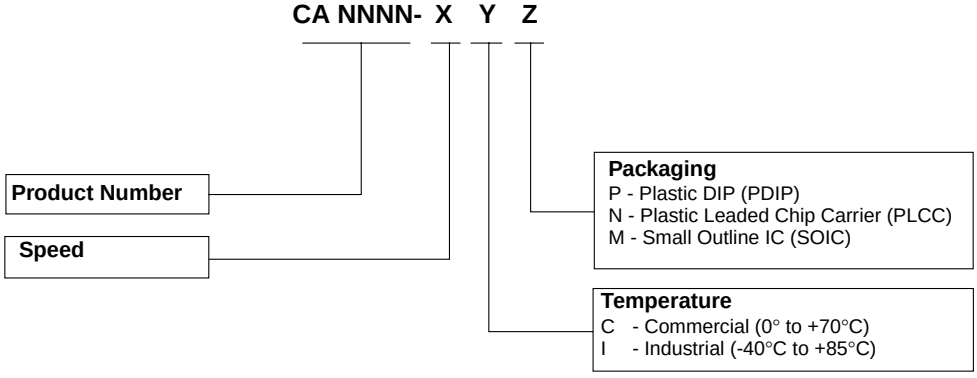
1.3 8000 Series Product Index

Product	Description	Speed	Temperature Range	Package Codes and Lead Counts		
				P	N	M
CA80C85B	High Performance 8-Bit CMOS Processor	3, 5, 6, 8 MHz	C, I	40	44	—
CA82C37A	Programmable DMA Controller	5, 8, 10 MHz	C, I	40	44	—
CA82C52	CMOS Serial Controller Interface	16 MHz	C, I	28	28	—
CA82C54	Programmable Interval Timer	5, 8, 10 MHz	C, I	24	28	—
CA82C55A	Programmable Peripheral Interface	5, 8, 10 MHz	C, I	40	44	—
CA82C59A	Programmable Interrupt Controller	8, 10 MHz	C, I	28	28	28

Speed, Temperature Range and Package Codes are defined on the next page.

This table shows only the most commonly available package options. Where a package lead count is not given, the device is either not available in that package, or is available by special order only. Please contact the factory directly for more information.

1.4 Ordering Information and Product Code



Tundra products are designated by a Product Code. When ordering, refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact our factory directly.

Note that all products are not necessarily available in all packages.

1.5 Product Cross Reference

Tundra Semiconductor Corp.			Intel	Harris	Mitsubishi	NEC		OKI
						New Line	Former Line	
CA80C85B	-3CP	High Performance 8-Bit CMOS Processor	—	—	—	—	—	—
	-5CP		P8085AH-2	—	M5M80C85AP-2	—	µPD8085AC-2, µPD8085AHC-2	MSM80C85A-2RS
	-6CP		P8085H-1	—	—	—	—	—
	-8CP		—	—	—	—	—	—
	-8CN		—	—	—	—	—	—
CA82C37A	-5CP	Programmable DMA Controller	P8237A, P8237A-4, P8237A-5, P82C37A-5	CP82C37A-5	M5M82C37AP-5	—	—	MSM82C37A-5RS
	-5CN		—	CS82C37A-5	—	—	—	MSM82C37A-5JS
	-8CP		—	CP82C37A	—	—	—	—
	-8CN		—	CS82C37A	—	—	—	—
	-10CP		—	—	—	µPD71037C	µPD8237AC-5	—
	-10CN				—	µPD71037L	—	—
CA82C52	-16CP	CMOS Serial Controller Interface	—	CP82C52	—	—	—	—
	-16CN		—	CS82C52	—	—	—	—
CA82C54	-5CP	Programmable Interval Timer	—	—	—	—	—	—
	-5CN		—	—	—	—	—	—
	-8CP		P8254, P82C54, P8254-5,	CP82C54	M5M82C54P	µPD71054	µPD8253AC-2	MSM82C53-5RS
	-8CN		P8253, P8253-5	CS82C54	—	—	—	—
	-10CP		N82C54	—	—	—	—	MSM82C54-2RS
	-10CN		P8254-2, P82C54-2 N82C54-2	—	—	—	—	MSM82C54-2JS
CA82C55A	-5CP	Programmable Peripheral Interface	P8255, P8255-5	CP82C55A-5	M5L8255AP-5, M5M82C55AP-5	µPD71055	µPD8255AC-2	MSM82C55A-5RS
	-5CN		N8255, N8255-5	—	—	—	—	—
	-8CP		P82C551-2	—	M5M82C55AP-2	—	—	MSM82C55A-2RS
	-8CN		N82C55A-2	CS82C55A	—	—	—	MSM82C55A-2JS
	-10CP		—	—	—	—	—	—
	-10CN		—	—	—	—	—	—
CA82C59A	-8CP	Programmable Interrupt Controller	P8259-2, P82C59A-2 N8259-2	CP82C59A CS82C59A	M5M82C59AP-2 —	— —	— —	MSM82C59A-2RS MSM82C59A-2JS
	-8CN							
	-10CP		—	—	—	—	—	—
	-10CN		—	—	—	—	—	—
	-10CM		—	—	—	—	—	—

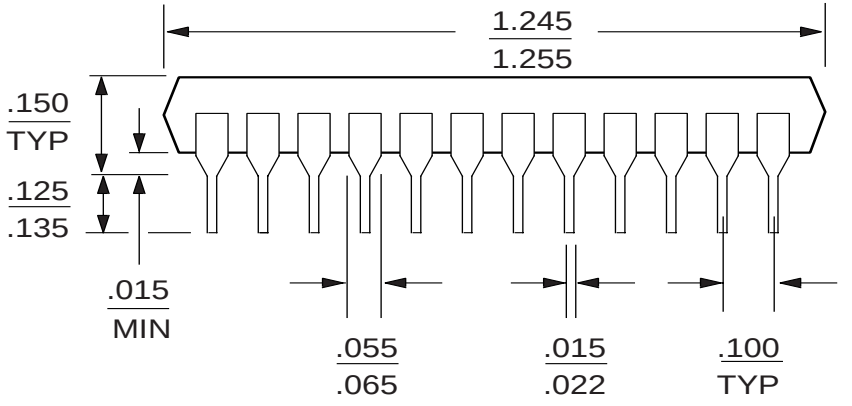
Tundra Semiconductor Corp.			AMD	Samsung	Toshiba	UMC
CA80C85B	-3CP	High Performance 8-Bit CMOS Processor	—	—	—	—
	-5CP		AM8085A-2, AM8085AH-2 AM8085AH-1	—	TMP8085AHP-2, TMP8085AP-2	—
	-6CP		—	—	—	—
	-8CP		—	—	—	—
	-8CN		—	—	—	—
CA82C37A	-5CP	Programmable DMA Controller	P8237A-5	—	—	UM8237A-4
					TMP82C37AP-5	UM8237A-5
	-5CN		—	—	—	—
	-8CP		—	—	—	—
	-8CN		—	—	—	—
	-10CP		—	KS82C37A-10CP	—	—
	-10CN		—	KS82C37A-10CL	—	—
CA82C52	-16CP	CMOS Serial Controller Interface	—	KS82C52-16CP	—	—
	-16CN		—	KS82C52-16CL	—	—
CA82C54	-5CP	Programmable Interval Timer	—	—	—	—
	-5CN		—	—	—	—
	-8CP		P82C54	KS82C54-8CP	—	UM8254
	-8CN		N82C54	KS82C54-8CL	—	UM8254-2
	-10CP		P82C54-2	KS82C54-10CP	TMP82C54P-2	
	-10CN		N82C54-2	KS82C54-10CL	—	
CA82C55A	-5CP	Programmable Peripheral Interface	2.5 MHz or 3.3 MHz Only CS82C55A-5	—	—	—
	-5CN		CP82C55A	—	—	—
	-8CP		—	KS82C55A-8CP	TMP82C55AP-2	—
	-8CN		—	KS82C55A-8CL	—	—
	-10CP		—	KS82C55A-10CP	TMP82C55AP-10	—
	-10CN		—	KS82C55A-10CL	—	—
CA82C59A	-8CP	Programmable Interrupt Controller	P8259A-2, P82C59A-2 N8259A-2, N82C59A-2	—	TMP82C59AP-2	UM8259A
	-8CN		—	—	—	—
	-10CP		—	KS82C59A-10CP	—	—
	-10CN		—	KS82C59A-10CL	—	—
	-10CM		—	—	TMP82C59AM-2	—

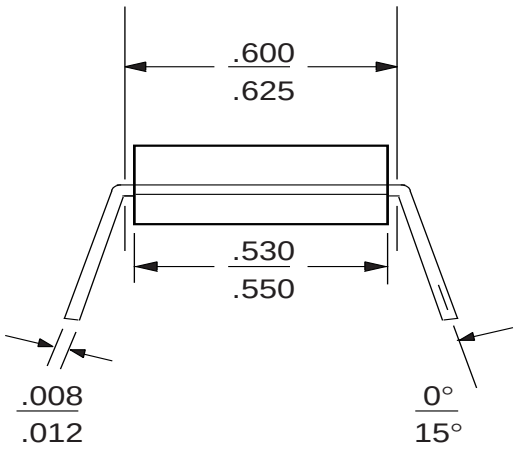
These products no longer supported by their original manufacturers.

1.6 Package Codes and Mechanicals

1.6.1 PDIP (Package Code: P)

24 - pin PDIP

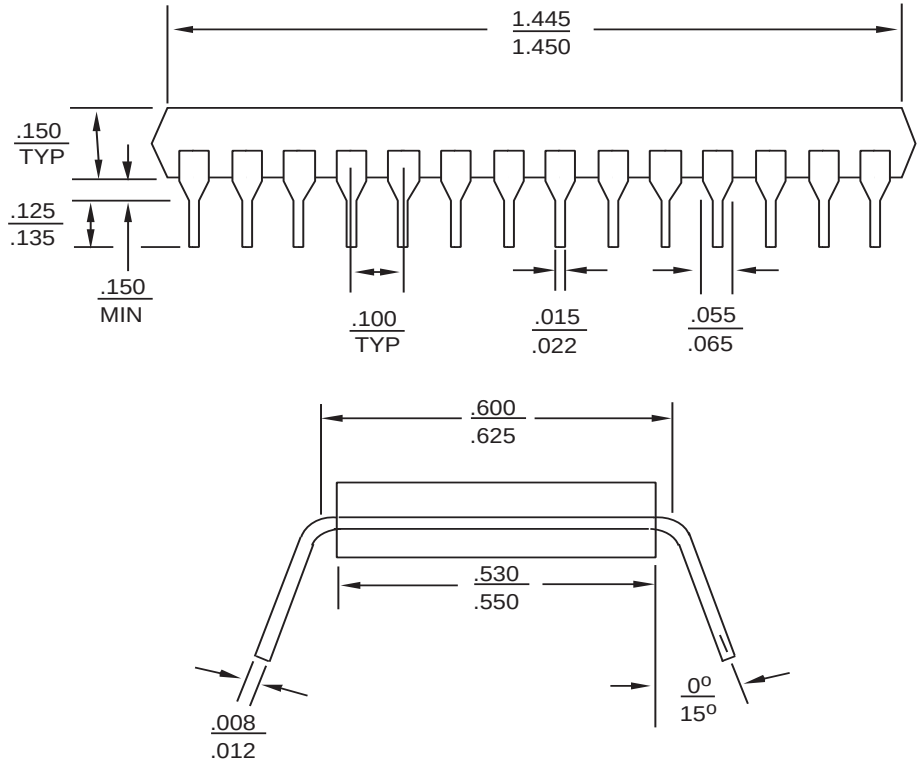




All dimensions in inches.

Note: This package conforms to JEDEC reference MS-011, Variation AA.

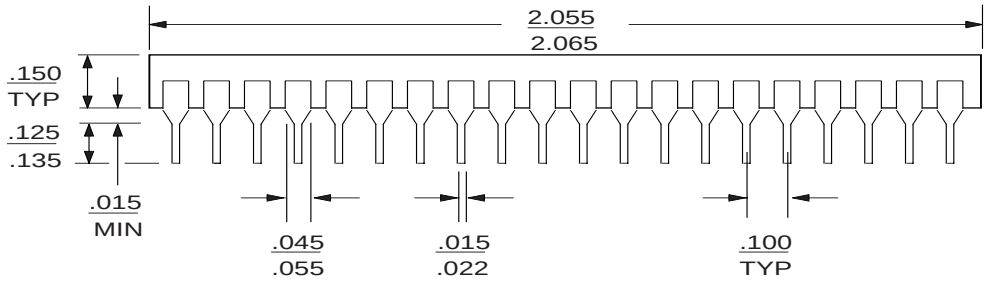
28 - pin PDIP

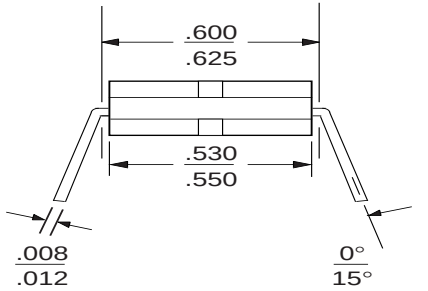


All dimensions in inches

Note: This package conforms to JEDEC reference MS-011, Variation AB.

40 - pin PDIP



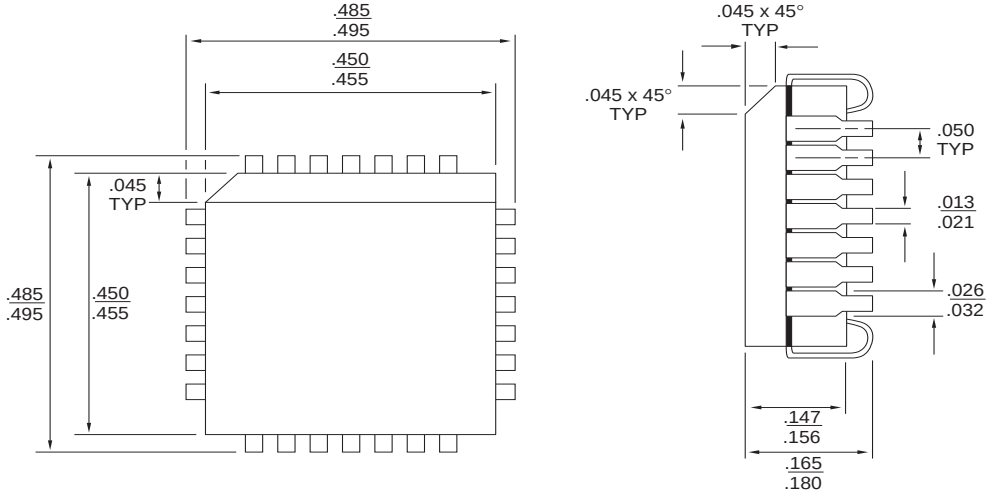


All dimensions in inches

Note: This package conforms to JEDEC reference MS-011, Variation AC.

1.6.2 PLCC (Package Code: N)

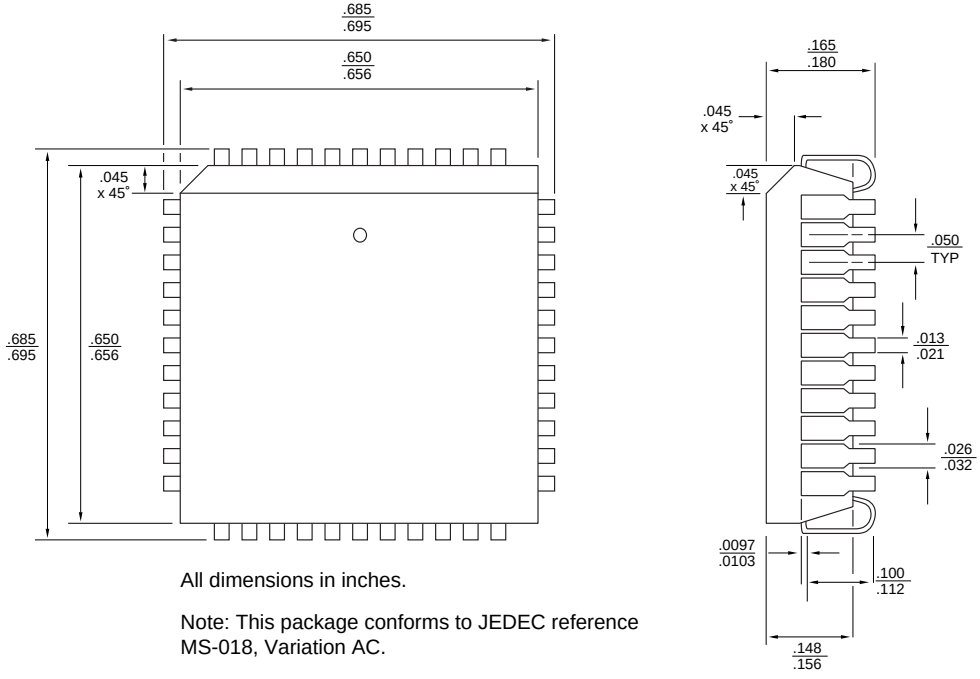
28 - pin PLCC



All dimensions in inches.

Note: This package conforms to JEDEC reference MS-018, Variation AB.

44 - pin PLCC

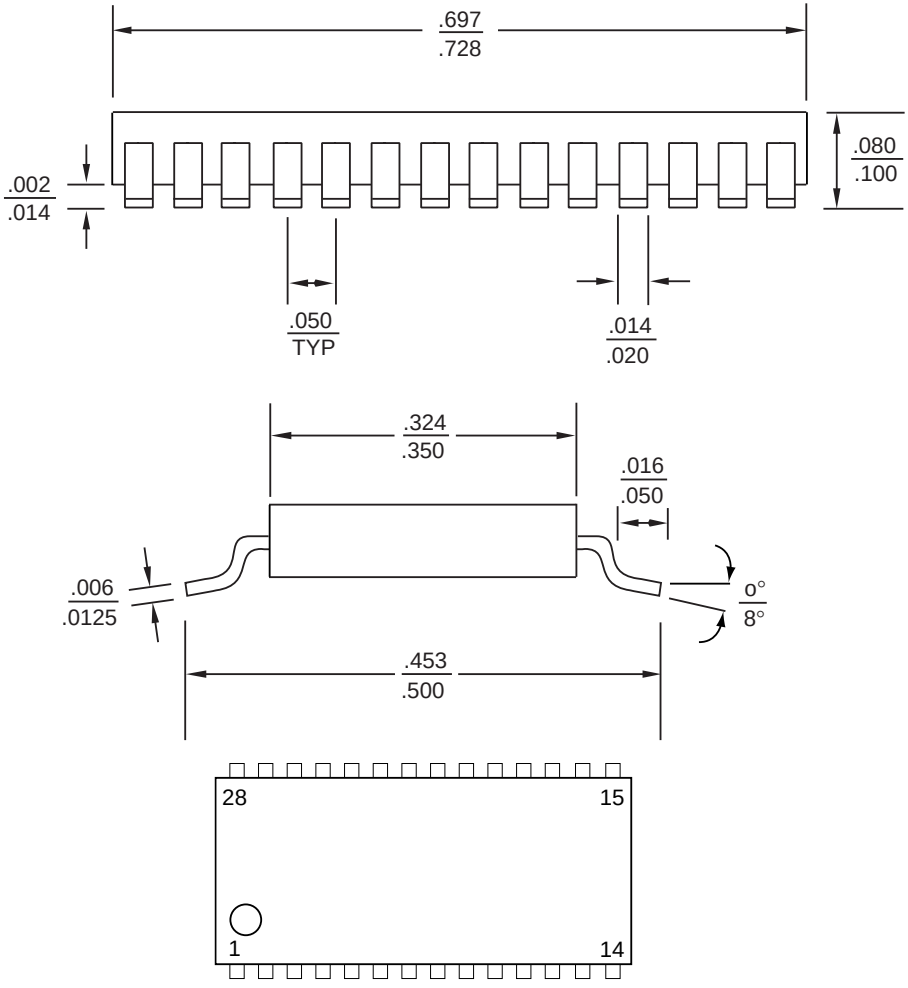


All dimensions in inches.

Note: This package conforms to JEDEC reference MS-018, Variation AC.

1.6.3 SOIC (Package Code: M)

28 - pin SOIC



All dimensions in inches

Note: This package conforms to JEDEC reference MO-059, Variation AC.

Section 2

CA80C85B

HIGH PERFORMANCE 8-BIT CMOS MICROPROCESSOR

- **Enhanced, high performance CA80C85B microprocessor features pin and functional compatibility with industry standard 8085 and 8085A**
- **Very low power consumption achieved with proven CMOS implementation**
- **TTL compatible input/output voltages**
- **Fast - Available in 8 MHz, 6 MHz, 5 MHz and 3 MHz speed versions**
- **Full support of extended instruction set, and standard 8080 and 8085/8085A instruction sets**
- **Runs over 10,000 CP/M® programs**
- **On-chip clock generator (using external crystal, LC or RC network)**
- **Direct addressing to 64K bytes**
- **Four Interrupt inputs (one non-maskable)**
- **One of the multi-sourced, Calmos™ 8000 series products**

The CA80C85B is an 8-bit microprocessor having complete pin and functional compatibility with industry standard 8085s and 8085As. In addition, it supports the special 8085 extended instruction set. The CA80C85B includes an on-board system controller, clock generator, serial I/O port and direct addressing capability to 64K bytes of memory. The device also utilizes a multiplexed data bus, with 16-bit addresses split between an 8-bit address bus and an 8-bit data bus.

The CA80C85B is manufactured in CMOS and supplied in a PDIP package configuration suitable for commercial and industrial applications.

The CA80C85B provides the systems designer with single component CPU functionality, thereby reducing the parts count. Its low power consumption and TTL I/O compatibility make the CA80C85B particularly well suited to portable or standby type applications.

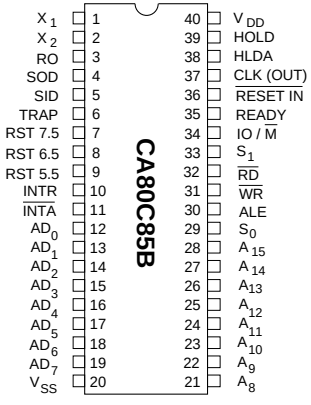


Figure 2-1: PDIP Pin Configurations

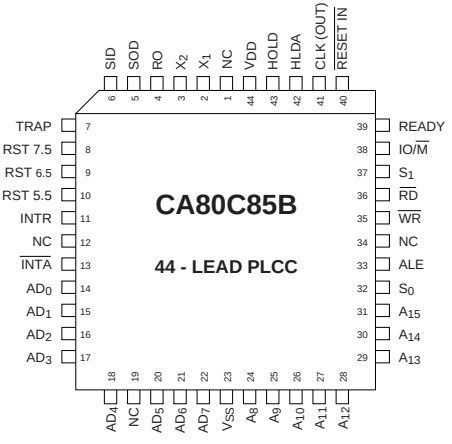


Figure 2-2: PLCC Pin Configurations

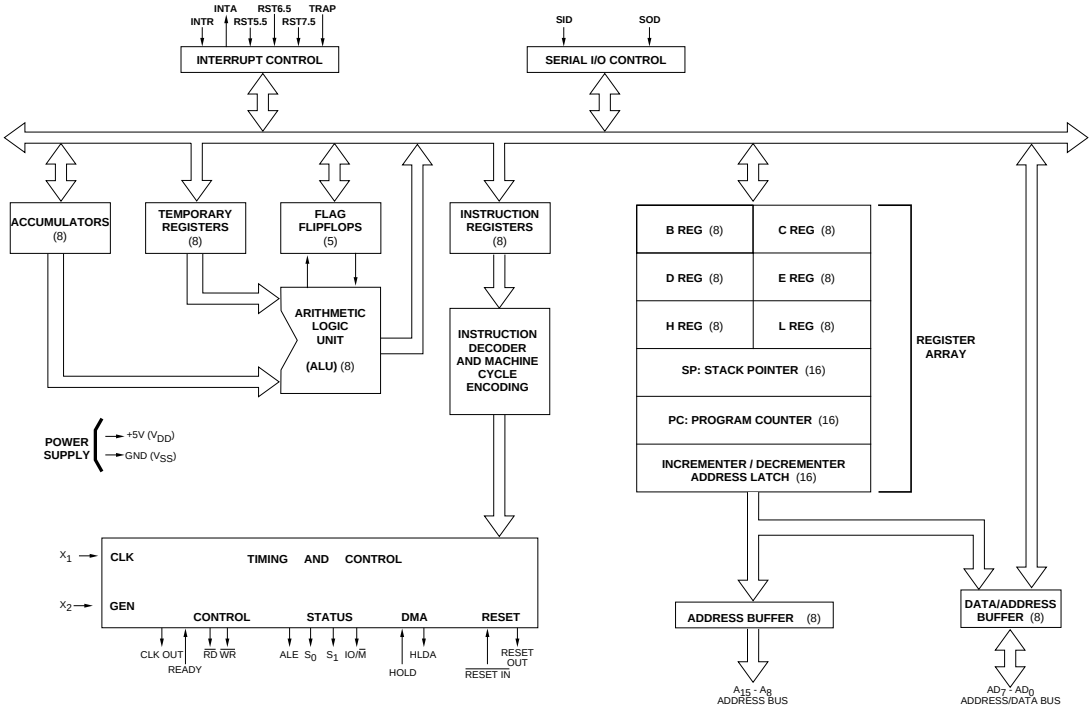


Figure 2-3: CA80C85B Block Diagram

Table 2-1: Pin Descriptions

Symbol PDIP	Pin	Type	Name and Function
A_8 - A_{15}	21 - 28	O	**High Address Bus**: the most significant 8 bits of the memory address.
AD_0 - AD_7	12 - 19	I/O	**Low Address and Data Bus**: the least significant 8 bits of the memory address multiplexed with an 8-bit data bus.
ALE	30	O	**Address Latch Enable Out**: This signal occurs during the first clock state of a machine cycle. The falling edge of the ALE may be used to strobe the status information.
CLK	37	O	**Clock**: This signal can be used as a system clock. The period of CLK is twice the period of the X_1, X_2 input.
HLDA	38	O	**Hold Acknowledge**: Indicates that the CPU has received the HOLD request and that the bus will be relinquished in the next clock cycle.
HOLD	39	I	**Hold Request**: Is used to indicate that another master is requesting the use of the address and data buses. When HOLD is acknowledged (HLDA), the Address, Data, $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$ lines are set to the high impedance state. Note that the CPU can regain control of the bus only after the HOLD is removed.
$\overline{INTA}$	11	O	**Interrupt Acknowledge**: This active low signal indicates that the interrupt request input (INTR) has been recognized and acknowledged.
INTR	10	O	**Interrupt Request**: This is a general purpose interrupt. When INTR goes HIGH, it will inhibit the Program Counter, generate an interrupt acknowledge ($\overline{INTA}$) signal, and sample the data bus for a RESTART or CALL instruction.
IO/$\overline{M}$	34	O	**Machine Cycle Status**: See S_0 and S_1 status bits for further details.
$\overline{RD}$	32	O	**Read Control**: Active low signal is used to indicate that selected memory or I/O device is to be read with the data bus available for the data transfer. $\overline{RD}$ is set to a high impedance state during HOLD, HALT and RESET modes.
READY	35	I	**Ready**: This signal is set to HIGH during read or write cycles to indicate that the selected memory or I/O device is ready to send or receive data.
$\overline{RESET\ IN}$	36	I	**Reset In**: Active low signal sets the Program Counter to zero, and resets the interrupt enable (INTE) and HLDA flipflop. Note that so long as $\overline{RESET\ IN}$ is held low, the CPU is held in a reset condition.
RO	3	O	**Reset Out**: Indicates that the CPU is being reset. This signal can be used as a system RESET.
RST7.5 RST6.5 RST5.5	7, 8, 9	I	**Restart Interrupts**: These inputs provide three maskable interrupts which invoke an automatic internal restart. RST7.5 is the highest relative priority, followed by RST6.5 and RST5.5. All three interrupts have a higher priority than INTR.
S_0 - S_1 IO/$\overline{M}$	29, 33, 34	O	**Status Outputs**: These signals provide an indication of the machine status during any given cycle. All become valid at the beginning of a machine cycle, and remain stable for the duration of that cycle. The status may be latched by the falling edge of the ALE signal.
SID	5	I	**Serial Input Data**: Data on SID is loaded into accumulator bit 7 when a RIM instruction is executed.
SOD	4	O	**Serial Output Data**: This signal is set or reset by the SIM instruction.
TRAP	6	I	**Trap Interrupt**: Is a non-maskable restart interrupt. It is the highest priority interrupt, and is unaffected by an interrupt enable (INTE).
V_{DD}	40	–	**Power**: +5V supply
V_{SS}	20	–	**Ground**: Ground reference.
$\overline{WR}$	31	O	**Write Control**: This active low signal is used to indicate that selected memory or I/O device is to be written to, with the data bus available for the data transfer. WR is set to a high impedance state during HOLD, HALT, and RESET modes.
X_1, X_2	1,2	I	**X_1, X_2**: These two inputs are connected to clock source which is used to drive the internal clock generator. The clock source may be a crystal, LC or RC network. An external clock cal also be connected directly to X_1, to produce an internal processor clock frequency of one half of the input frequency.

FUNCTIONAL DESIGN

The CA80C85B utilizes a stack architecture to enable any part of the external memory to be employed as a Last In/First Out (LIFO) memory stack. A 16-bit stack pointer controls the addressing of this stack. The arrangement allows extensive subroutine nesting and multiple level interrupts to be handled without losing the system status. In addition, the device accepts serial input data and provides serial output data, functions which are controlled by the interrupt mask instructions.

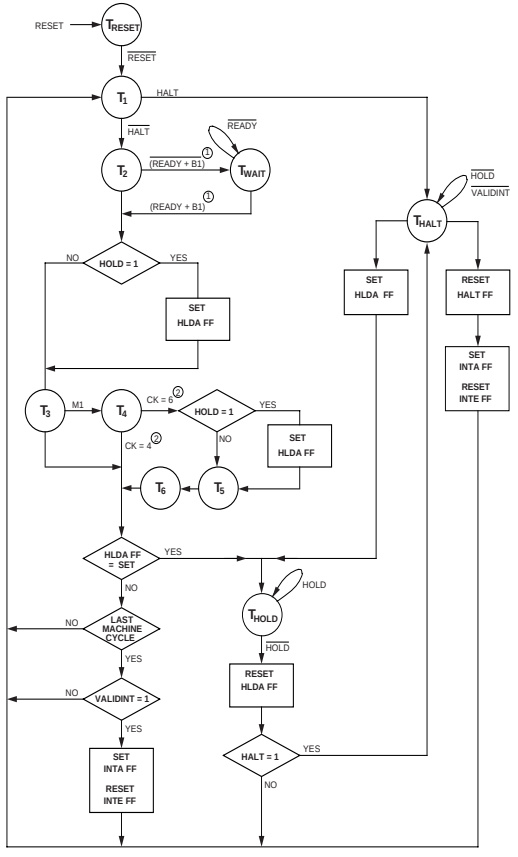
The CA80C85B provides 16-bit arithmetic operation with immediate operators and decimal capability. An 8-bit accumulator, four user accessible flag bits, an 8-bit parallel binary arithmetic unit and six 8-bit data registers, all shown in the block diagram of Figure 2-3, are also provided. CA80C85B timing signals are supplied by an internal clock generator (which can be used with either crystal or RC timing circuits), or by an external clock input signal. Status outputs convey memory I/O instruction and Read/Write timing indications.

For typical, single function type configurations, the CA80C85B is supplied in a 40-pin package, the low pin count a result of multiplexing the Address and Data Bus lines. Pin functions are described in Table 2-1, with the 40-pin DIP pin configuration illustrated in Figure 2-1. The lower processor pin count of this device can be reflected throughout a system design by similar pin count reductions in peripheral chips. Further, this optimization can be achieved without incurring complex or critical timing problems.

The CA80C85B has five levels of interrupts, including three maskable restart interrupts, one non-maskable TRAP interrupt and a bus vectored interrupt, INTR. Bus control is provided by the $\overline{RD}$, $\overline{WR}$, S_0, S_1, IO/$\overline{M}$ and $\overline{INTA}$ interrupt acknowledge signals. When a HOLD control input signal is received, both Address and Data Bus are set to a high-impedance state, and an HLDA output signal acknowledges that microprocessor operation is stopped, and that the buses are available for use by other devices. Note that HOLD and all other interrupt signals are synchronized with the processor's internal clock. This is illustrated in the processor state transition diagram of Figure 2-4.

In addition to the Data Bus, a simple serial interface is provided by the Serial Input Data (SID) and Serial Output Data (SOD) lines.

At the software level, the CA80C85B supports the full extended instruction set, offering 10 additional instructions for the production of more efficient code. The five existing condition code flags have also been enhanced with two additional flag bits, one of which indicates a 2s complement overflow.



Notes:
1. *BI* indicates that the bus is idle during this machine cycle, though the processor itself is active
2. *CK* indicates the number of clock cycles in this machine cycle.

Figure 2-4: State Transition Diagram

Table 2-2: 3 MHz AC Characteristics

T_A = –40° to +85°C, V_{DD} = +5v + 10%, t_{CYC} = 320 ns, C_L = 150 pF

Symbol	Parameter	Limits		Units
		Min	Max	
t_1	CLK Low Time	80	-	ns
t_2	CLK High Time	120	-	ns
t_{AC}	A_8 - A_{15} Valid to Leading Edge of Control (Note 1)	270	-	ns
t_{ACL}	A_0 - A_7 Valid to Leading Edge of Control	240	-	ns
t_{AD}	A0 - A15 Valid to Valid Data In	-	575	ns
t_{AFR}	Address Float After Leading Edge of $\overline{RD}$, $\overline{INTA}$	-	0	ns
t_{AL}	A_8 - A_{15} Valid Before Trailing Edge of ALE (Note 1)	115	-	ns
t_{ALL}	A_0 - A_7 Valid Before Trailing Edge of ALE	90	-	ns
t_{ARY}	READY Valid from Address Valid	-	220	ns
t_{CA}	Address (A_8 - A_{15}) Valid After Control	120	-	ns
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	400	-	ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50	-	ns
t_{CYC}	CLK Cycle Period	320	2000	ns
t_{DW}	Data Valid to Trailing Edge of $\overline{WR}$	420	-	ns
t_f	CLK Fall Time	-	30	ns
t_{HABE}	HLDA to Bus Enable	-	210	ns
t_{HABF}	Bus Float After HLDA	-	210	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110	-	ns
t_{HDH}	HOLD Hold Time	0	-	ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170	-	ns
t_{INH}	INTR Hold Time	0	-	ns
t_{INS}	INTR RST and TRAP Setup Time to Falling Edge of CLK	160	-	ns
t_{LA}	Address Hold Time After ALE	100	-	ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130	-	ns
t_{LCK}	ALE Low During CLK High	100	-	ns
t_{LDR}	ALE to Valid Data During Read	-	460	ns
t_{LDW}	ALE to Valid Data During Write	-	200	ns
t_{LL}	ALE Width	140	-	ns
t_{LRY}	ALE to Ready Stable	-	110	ns
t_r	CLK Rise Time	-	30	ns
t_{RAE}	Trailing Edge of RD to re-Enabling of Address	150	-	ns
t_{RD}	$\overline{RD}$ (or $\overline{INTA}$) to Valid Data	-	300	ns
t_{RDH}	Data Hold Time After $\overline{RD}$, $\overline{INTA}$	0	-	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400	-	ns
t_{RYH}	READY Hold Time	0	-	ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	110	-	ns
t_{WD}	Data Valid After Trailing Edge of $\overline{WR}$	100	-	ns
t_{WDL}	Leading Edge of $\overline{WR}$ to Data Valid	-	40	ns
t_{XKF}	X_1 Rising to CLK Falling	20	150	ns
t_{XKR}	X_1 Rising to CLK Rising	20	120	ns

Note: 1. A_8 - A_{15} Address Specs apply to IO/$\overline{M}$, S0 and S1. Except A_8 - A_{15} are undefined during T_4 - T_6 of cycle whereas IO/$\overline{M}$, S_0 and S_1 are stable.

Table 2-3: 5 MHz AC Characteristics

T_A = –40° to +85°C, V_{DD} = +5v + 10%, t_{CYC} = 200 ns, C_L = 150 pF

Symbol	Parameter	Limits		Units
		Min	Max	
t_1	CLK Low Time	40	-	ns
t_2	CLK High Time	70	-	ns
t_{AC}	A_8 - A_{15} Valid to Leading Edge of Control (Note 1)	115	-	ns
t_{ACL}	A_0 - A_7 Valid to Leading Edge of Control	115	-	ns
t_{AD}	A_0 - A_{15} Valid to Valid Data In	-	330	ns
t_{AFR}	Address Float After Leading Edge of $\overline{RD}$, $\overline{INTA}$	-	0	ns
t_{AL}	A_8 - A_{15} Valid Before Trailing Edge of ALE (Note 1)	50	-	ns
t_{ALL}	A_0 - A_7 Valid Before Trailing Edge of ALE	50	-	ns
t_{ARY}	READY Valid from Address Valid	-	100	ns
t_{CA}	Address (A_8 - A_{15}) Valid After Control	60	-	ns
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	230	-	ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	25	-	ns
t_{CYC}	CLK Cycle Period	200	2000	ns
t_{DW}	Data Valid to Trailing Edge of $\overline{WR}$	230	-	ns
t_f	CLK Fall Time	-	30	ns
t_{HABE}	HLDA to Bus Enable	-	150	ns
t_{HABF}	Bus Float After HLDA	-	150	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	40	-	ns
t_{HDH}	HOLD Hold Time	0	-	ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	120	-	ns
t_{INH}	INTR Hold Time	0	-	ns
t_{INS}	INTR RST and TRAP Setup Time to Falling Edge of CLK	150	-	ns
t_{LA}	Address Hold Time After ALE	50	-	ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	60	-	ns
t_{LCK}	ALE Low During CLK High	50	-	ns
t_{LDR}	ALE to Valid Data During Read	-	250	ns
t_{LDW}	ALE to Valid Data During Write	-	140	ns
t_{LL}	ALE Width	80	-	ns
t_{LRY}	ALE to Ready Stable	-	30	ns
t_r	CLK Rise Time	-	30	ns
t_{RAE}	Trailing Edge of RD to re-Enabling of Address	85	-	ns
t_{RD}	$\overline{RD}$ (or $\overline{INTA}$) to Valid Data	-	150	ns
t_{RDH}	Data Hold Time After $\overline{RD}$, $\overline{INTA}$	0	-	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	220	-	ns
t_{RYH}	READY Hold Time	0	-	ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	100	-	ns
t_{WD}	Data Valid After Trailing Edge of $\overline{WR}$	60	-	ns
t_{WDL}	Leading Edge of $\overline{WR}$ to Data Valid	-	20	ns
t_{XKF}	X_1 Rising to CLK Falling	20	110	ns
t_{XKR}	X_1 Rising to CLK Rising	20	100	ns

Note: 1. A_8 - A_{15} Address Specs apply to IO/$\overline{M}$, S0 and S1. Except A_8 - A_{15} are undefined during T_4 - T_6 of cycle whereas IO/$\overline{M}$, S_0 and S_1 are stable.

Table 2-4: 6 MHz AC Characteristics

T_A = –40° to +85°C, V_{DD} = +5v + 5%, t_{CYC} = 167 ns, C_L = 150 pF

Symbol	Parameter	Limits		Units
		Min	Max	
t_1	CLK Low Time	34	-	ns
t_2	CLK High Time	59	-	ns
t_{AC}	A_8 - A_{15} Valid to Leading Edge of Control (Note 1)	96	-	ns
t_{ACL}	A_0 - A_7 Valid to Leading Edge of Control	96	-	ns
t_{AD}	A_0 - A_{15} Valid to Valid Data In	-	292	ns
t_{AFR}	Address Float After Leading Edge of $\overline{RD}$, $\overline{INTA}$	-	0	ns
t_{AL}	A_8 - A_{15} Valid Before Trailing Edge of ALE (Note 1)	42	-	ns
t_{ALL}	A_0 - A_7 Valid Before Trailing Edge of ALE	42	-	ns
t_{ARY}	READY Valid from Address Valid	-	83	ns
t_{CA}	Address (A_8 - A_{15}) Valid After Control	50	-	ns
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	192	-	ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	20	-	ns
t_{CYC}	CLK Cycle Period	167	2000	ns
t_{DW}	Data Valid to Trailing Edge of $\overline{WR}$	192	-	ns
t_f	CLK Fall Time	-	25	ns
t_{HABE}	HLDA to Bus Enable	-	125	ns
t_{HABF}	Bus Float After HLDA	-	125	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	33	-	ns
t_{HDH}	HOLD Hold Time	0	-	ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	100	-	ns
t_{INH}	INTR Hold Time	0	-	ns
t_{INS}	INTR RST and TRAP Setup Time to Falling Edge of CLK	125	-	ns
t_{LA}	Address Hold Time After ALE	42	-	ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	50	-	ns
t_{LCK}	ALE Low During CLK High	42	-	ns
t_{LDR}	ALE to Valid Data During Read	-	225	ns
t_{LDW}	ALE to Valid Data During Write	-	100	ns
t_{LL}	ALE Width	67	-	ns
t_{LRY}	ALE to Ready Stable	-	25	ns
t_r	CLK Rise Time	-	25	ns
t_{RAE}	Trailing Edge of RD to Re-enabling of Address	65	-	ns
t_{RD}	$\overline{RD}$ (or $\overline{INTA}$) to Valid Data	-	125	ns
t_{RDH}	Data Hold Time After $\overline{RD}$, $\overline{INTA}$	0	-	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	183	-	ns
t_{RYH}	READY Hold Time	0	-	ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	84	-	ns
t_{WD}	Data Valid After Trailing Edge of $\overline{WR}$	50	-	ns
t_{WDL}	Leading Edge of $\overline{WR}$ to Data Valid	-	16	ns
t_{XKF}	X_1 Rising to CLK Falling	20	110	ns
t_{XKR}	X_1 Rising to CLK Rising	20	100	ns

Note: 1. A_8 - A_{15} Address Specs apply to IO/$\overline{M}$, S0 and S1. Except A_8 - A_{15} are undefined during T_4 - T_6 of cycle whereas IO/$\overline{M}$, S_0 and S_1 are stable.

Table 2-5: 8 MHz AC Characteristics

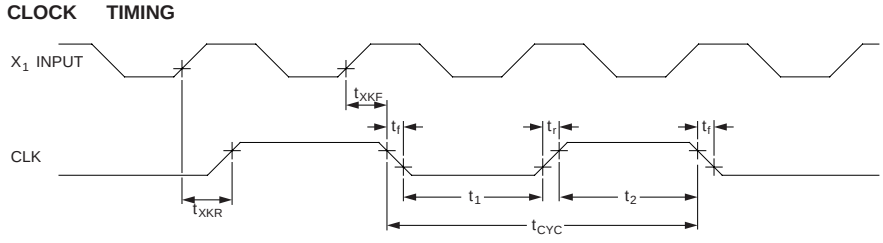
T_A = –40° to +85°C, V_{DD} = +5v + 5%, t_{CYC} = 125 ns, C_L = 150 pF

Symbol	Parameter	Limits		Units
		Min	Max	
t_1	CLK Low Time	25	-	ns
t_2	CLK High Time	44	-	ns
t_{AC}	A_8 - A_{15} Valid to Leading Edge of Control (Note 1)	72	-	ns
t_{ACL}	A_0 - A_7 Valid to Leading Edge of Control	72	-	ns
t_{AD}	A_0 - A_{15} Valid to Valid Data In	-	220	ns
t_{AFR}	Address Float After Leading Edge of $\overline{RD}$, $\overline{INTA}$	-	0	ns
t_{AL}	A_8 - A_{15} Valid Before Trailing Edge of ALE (Note 1)	31	-	ns
t_{ALL}	A_0 - A_7 Valid Before Trailing Edge of ALE	31	-	ns
t_{ARY}	READY Valid from Address Valid	-	63	ns
t_{CA}	Address (A_8 - A_{15}) Valid After Control	37	-	ns
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	144	-	ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	15	-	ns
t_{CYC}	CLK Cycle Period	125	2000	ns
t_{DW}	Data Valid to Trailing Edge of $\overline{WR}$	144	-	ns
t_f	CLK Fall Time	-	25	ns
t_{HABE}	HLDA to Bus Enable	-	94	ns
t_{HABF}	Bus Float After HLDA	-	94	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	25	-	ns
t_{HDH}	HOLD Hold Time	0	-	ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	78	-	ns
t_{INH}	INTR Hold Time	0	-	ns
t_{INS}	INTR RST and TRAP Setup Time to Falling Edge of CLK	94	-	ns
t_{LA}	Address Hold Time After ALE	32	-	ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	38	-	ns
t_{LCK}	ALE Low During CLK High	32	-	ns
t_{LDR}	ALE to Valid Data During Read	-	168	ns
t_{LDW}	ALE to Valid Data During Write	-	75	ns
t_{LL}	ALE Width	50	-	ns
t_{LRY}	ALE to Ready Stable	-	25	ns
t_r	CLK Rise Time	-	25	ns
t_{RAE}	Trailing Edge of $\overline{RD}$ to Re-enabling of Address	45	-	ns
t_{RD}	$\overline{RD}$ (or $\overline{INTA}$) to Valid Data	-	94	ns
t_{RDH}	Data Hold Time After $\overline{RD}$, $\overline{INTA}$	0	-	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	138	-	ns
t_{RYH}	READY Hold Time	0	-	ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	63	-	ns
t_{WD}	Data Valid After Trailing Edge of $\overline{WR}$	34	-	ns
t_{WDL}	Leading Edge of $\overline{WR}$ to Data Valid	-	16	ns
t_{XKF}	X_1 Rising to CLK Falling	20	69	ns
t_{XKR}	X_1 Rising to CLK Rising	20	63	ns

Note: 1. A_8 - A_{15} Address Specs apply to IO/$\overline{M}$, S0 and S1. Except A_8 - A_{15} are undefined during T_4 - T_6 of cycle whereas IO/$\overline{M}$, S_0 and S_1 are stable.

Figure 2-5: Timing Diagrams

a) Clock Timing



b) Read Operation

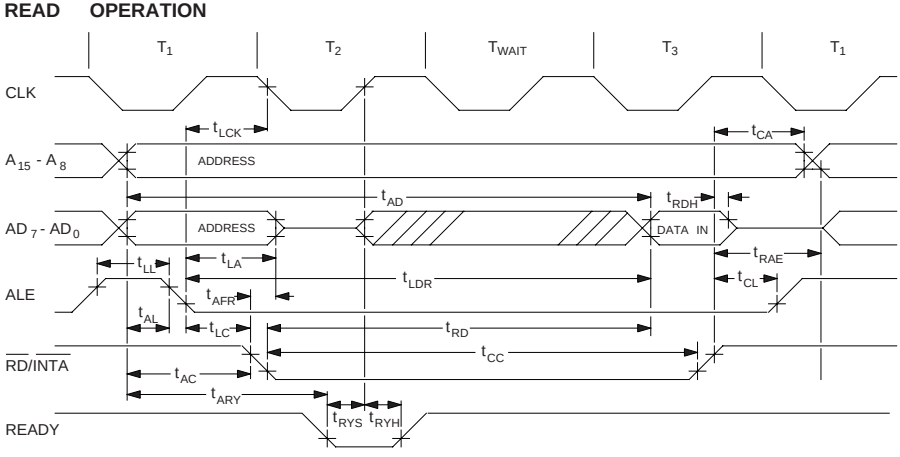
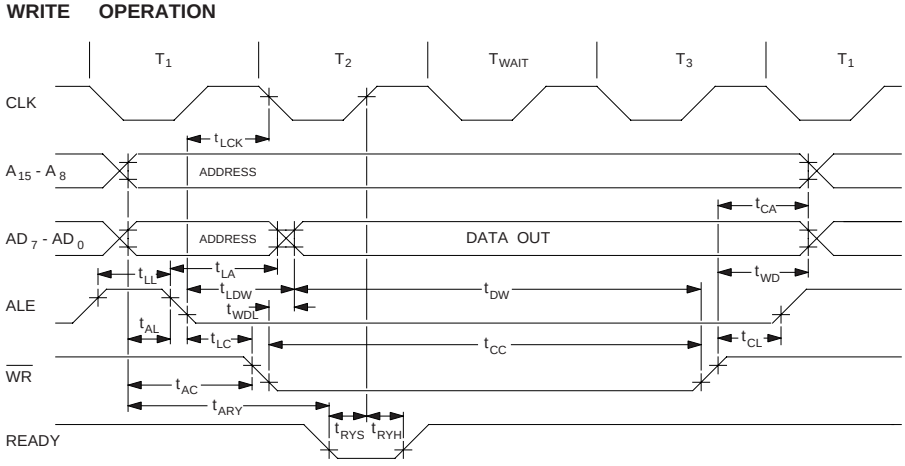


Figure 4: Timing Diagrams con't

c) Write Operation



d) Hold Operation

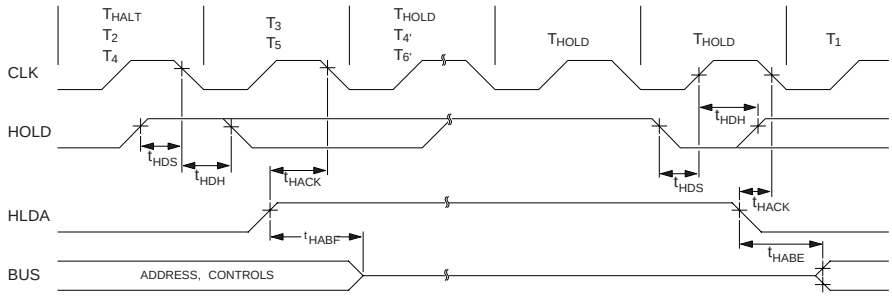
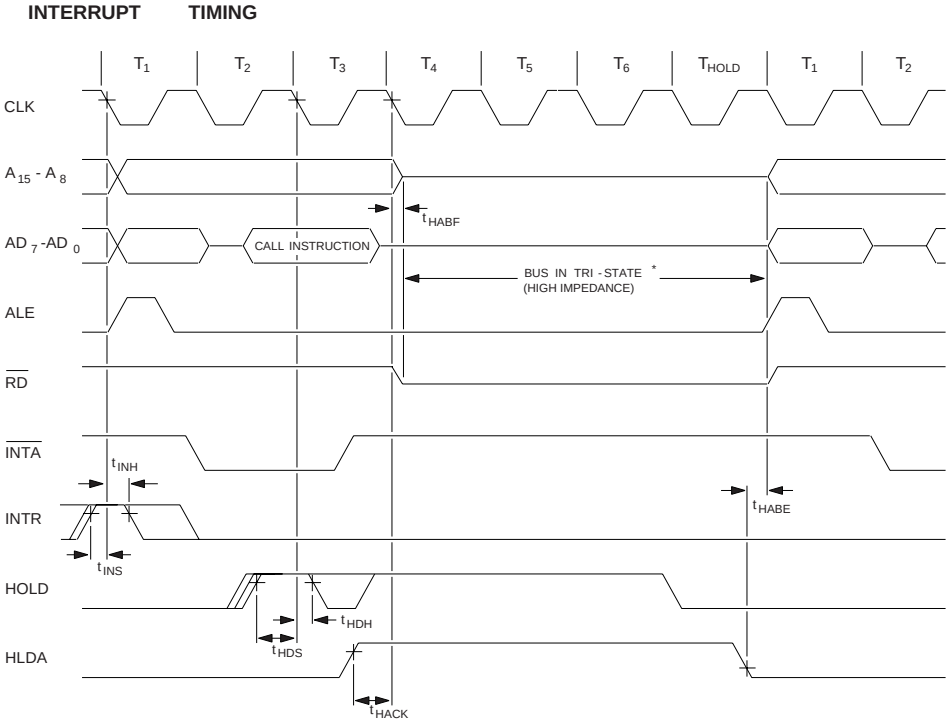


Figure 4: Timing Diagrams con't

e) Interrupt Timing



*NOTE: IO/$\overline{M}$ is also floating in a high-impedance state during this time

Table 2-6: DC Characteristics (Commercial and Industrial Temperature Range Devices)

T_A = –40° to +85°C, V_{DD} = +5v + 10%, t_{CYC} = 320 ns (except as noted)

Symbol	Parameter	Test Condition	Limits		Units
			Min	Max	
I_{DD1}	Power Supply Current	t_{CYC} = 320 ns, T_A = –40 °C		24	mA
		t_{CYC} = 320 ns, T_A = +25 °C		17	mA
I_{DD2}	Power Supply Current	t_{CYC} = 200 ns, T_A = –40 °C		29	mA
		t_{CYC} = 200 ns, T_A = +25 °C		21	mA
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$ and $V_{IN} = 0$	-10	10	µA
I_{OL}	Output Leakage Current	$0v \le V_{OUT} \le V_{DD}$	-10	10	µA
V_{HY}	Hysteresis, RESET		0.25		V
V_{IH}	Input High Voltage		2.2	V_{DD}+0.3	V
V_{IHR}	Input High Level, RESET		2.4	V_{DD}+0.3	V
V_{IL}	Input Low Voltage		–0.3	+0.8	V
V_{ILR}	Input Low Level, RESET		–0.3	+0.8	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	2.4		V
		I_{OH} = –40 µA	4.2		V

Table 2-7: Absolute Maximum Ratings

Storage Temperature	–65°C to +160°C
Voltage On Any Pin with respect to Ground	–0.3 to VDD +0.3 Volts
Output Currents	100mA
Power Dissipation	1 Watt
Lead Temperature (Soldering: 10 seconds)	300°C

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Clock Inputs

Clock inputs to the CA80C85B are supplied via the two inputs X_1 and X_2. The X_1 input can be driven either from an external clock, or used with the X_2 input and a crystal to produce an oscillator function. The minimum input

frequency required in both cases is 1 MHz. The actual internal microprocessor clock frequency is one half of the frequency applied or generated externally. For example, a 6 MHz crystal or external clock waveform is required for 3 MHz operation, and a 12 MHz clock source is required for 6 MHz operation.

The X_1/X_2 circuitry is intended to be used with a crystal cut for parallel resonance at the required clock frequency. Such crystals require closely controlled load capacitance in order to resonate at the specified frequency. The CA80C85B has an equivalent parallel capacitance of between 10 and 20 pF. Since most crystals will require higher values of capacitance to resonate at precisely their specified frequency, additional capacitance must be added as shown in Figure 2-6(a).

When the X_1 input is driven from an external clock, X_2 is left open. In this case, X_1 should be driven with a CMOS driver or a TTL device with a pull-up resistor, as shown in Figure 2-6(b). The clock low time must be greater than 80 ns for the 3 MHz device and 30 ns for the 6 MHz.

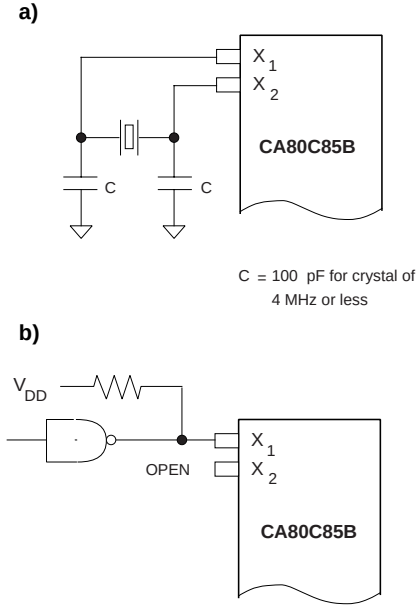


Figure 2-6: External Clock Circuits

Serial I/O

The Set Interrupt Mask (SIM) and Read Interrupt Mask (RIM) instructions provide several functions related to serial port I/O and interrupt mask operations. The SIM instruction is used to output serial data, and to program the interrupt mask register. The output signal, SOD, is set or reset as specified by the SIM instruction, with the accumulator contents constructed as shown in Figure 2-7.

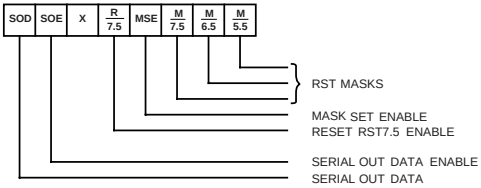


Figure 2-7: SIM Instruction Data Byte

The RIM instruction is used to read the serial input data (SID), as well as the interrupt mask. The accumulator contents after a RIM instruction has been executed are as shown in Figure 2-8.

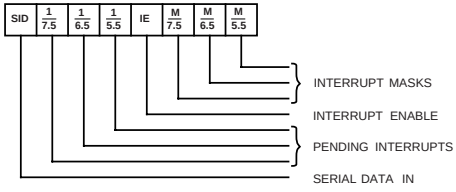


Figure 2-8: RIM Instruction Data Byte

Interrupts

The five interrupt levels provided by the CA80C85B are listed by descending order of priority in Table 2-8. TRAP and RSTx.5 are RESTART interrupts. When acknowledged, these four interrupts cause the processor to save the program counter (PC) on the stack, then branch to the restart address specified in the table.

The TRAP interrupt is non-maskable. It is set with a rising edge (low to high) followed by a stable high level until sampled by the processor. To reactivate the TRAP interrupt, the input signal must first go low, then high.

To preserve the status of the Interrupt Enable (IE) flag after a TRAP interrupt has occurred, the interrupt mask must be read and saved immediately after the interrupt has been acknowledged (refer to RIM instruction).

The RST7.5 is a maskable interrupt, set on a rising edge only, and then latched.

The RST6.5 and RST5.5 are maskable interrupts, set with a high level applied to their respective inputs. The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{\text{RESET IN}}$.

The INTR interrupt is also set by a high level applied to the input pin. It is similar in operation to the 8080 INT interrupt in that the action of the processor is dependent on the instruction placed on the bus during the $\overline{\text{INTA}}$.

Note that the servicing of any of the five interrupts disables all future interrupts (except TRAPS) until an EI instruction is executed. Of course, an interrupt of higher priority may interrupt a previous interrupt in process if the interrupts have been re-enabled within the interrupt service routine.

Table 2-8: Interrupt Restart Address

Interrupt	Restart Address (HEX)
TRAP	24H
RST7.5	3CH
RST6.5	34H
RST5.5	2CH
INTR	Dependent upon the instruction received on the bus during an INTA

Status Outputs

The status of the CA80C85B can be determined from the combination of S_0, S_1 and IO/$\overline{M}$ output signals. These signals are latched on the falling edge of an ALE signal, and are valid while ALE is low. Table 2-9 lists the seven possible types of machine cycles as defined by S_0, S_1 and IO/$\overline{M}$. Note in the Figure 2-5 timing diagrams that the $\overline{RD}$ and $\overline{WR}$ control lines become active after the status signals, when the transfer of data is to take place.

Table 2-9: Machine Cycle Status Conditions

S_0	S_1	IO/$\overline{M}$	Status
1	0	0	Memory Write
0	1	0	Memory Read
1	0	1	I/O Write
0	1	1	I/O Read
1	1	0	Opcode Fetch
1	1	1	Interrupt Acknowledge
Z	0	0	Halt
Z	X	X	Hold
Z	X	X	Reset

Z - High impedance state
X - Don't care condition

Extended Instructions and Condition Codes

The CA80C85B Flag Register features two additional condition code flags, for a total of seven. These are illustrated in Figure 2-9. The ten opcodes which comprise the extended instruction set of the CA80C85B microprocessor are described in Table 2-10.

S	Z	UI	AC	0	P	V	C	FLAG
7	6	5	4	3	2	1	0	BIT

V - 2's complement overflow for both
8 and 16-bit arithmetic operations

UI - Underflow indicator (DCX instruction)
or
Overflow indicator (INX instruction)

UI = 01 x 02 + 01 x R + 02 x R

where:
01 = sign of operand 1
02 = sign of operand 2
R = sign of result

For subtraction and comparisons, replace 02 with $\overline{02}$

Figure 2-9: Extended Condition Codes

Table 2-10: CA80C85B Extended Instruction Set

Name	Opcodes	Flags	Cycles	States	Description
ARHL	0 0 0 1 0 0 0 0 Addressing: Register	CY	2	7	**Arithmetic Shift of H and L to the Right:** The contents of registers H and L are shifted right one bit is shifted into the carry bit. The result is saved in registers H and L. H7=H7; Hn-1=Hn; L7=H0; Ln-1=Ln; CY=L0
DSUB	0 0 0 0 1 0 0 0 Addressing: Register	Z, S, P, CY,	3	10	**Double Subtraction:** The contents of registers B and Care subtracted from the contents of registers H and L. The result is saved in registers H and L. (H) (L)=(H) (L) - (B) (C)
JNUI	1 1 0 1 1 1 0 1 low-order address high-order address Addressing: Immediate	none	2 or 3	7 or 10	**Jump on NOT UI Flag:** Control is transferred to the instruction address specified in bytes 2 and 3 of the current instruction. The result is saved in registers H and L. (H) (L)=(H) (L) - (B) (C)
JUI	1 1 1 1 1 1 0 1 low-order address high-order address Addressing: Immediate	none	2 or 3	7 or 10	**Jump on UI Flag:** Control is transferred to the instruction address specified in bytes 2 and 3 of the current instruction. if the Unsigned Indicator Flag (UI) is set. Otherwise control continues sequentially. (H) (L)=(H) (L) - (B) (C)
LDHI	0 0 1 0 1 0 0 0 data Addressing: Immediate Register	none	3	10	**Load D and E with L Plus Immediate Byte:** The immediate byte is added to the contents of registers H and L, and the result is saved in registers D and E. (D) (E) = (H) (L) + (byte 2)
LDSI	0 0 1 1 1 0 0 0 data Addressing: Immediate Register	none	3	10	**Load D and E with SP Plus Immediate Byte:** The 2 bytes of register SP are added to the immediate byte, and the result is saved in registers D and E. (D) (E) = (SPH) (SPL) + (byte 2)
LHLX	1 1 1 0 1 1 0 1 data Addressing: Register Indirect	none	3	10	**Load H and L Indirect Through D and E:** The contents of the memory location given by registers D and E are moved to register L. The contents of the next location are moved to register H L=((D) (E)); H=((D)(E) + 1)
RDEL	0 0 0 1 1 0 0 0 Addressing: Register	CY, V	3	10	**Rotate D and E Left Through Carry:** The contents of the registers D and E are rotated one bit left through the carry flag. The low-order bit is set equal to the CY flag and the CY flag is set to the value shifted out of the high-order bit Dn+1=Dn; D0; E7; CY=D7; En+1=En; E0=CY
RSTV	1 1 0 0 1 0 1 1 Addressing: Register Indirect	none	1 or 3	6 or 12	**Restart on Overflow:** If overflow flag V is set, then the actions below are performed. Otherwise, control continues sequentially. If (V): SP - 1=PCH; SP - 2=PCL; SP=SP - 2; PC=40HEX
SHLX	1 1 0 1 1 0 0 1 Addressing:	none	3	10	**Store H and L Indirect Through D and E:** The contents of register L are moved to the memory location given by registers D and E. The contents of register H are

- **Pin and functional compatibility with the industry standard 8237/8237A**
- **Fully static, high speed - 10, 8 and 5 MHz versions available**
- **Low power CMOS implementation**
- **TTL input/output compatibility**
- **Compatible with 8080/85, 8086/88, 80286/386 and 68000 μP families**
- **Fully static**
- **Four independent maskable DMA channels with autoinitialize capability**
- **Memory-to-memory transfer**
- **Fixed or rotating DMA request priority**
- **Independent polarity control for DREQ and DACK signals**
- **Address increment or decrement selection**
- **Cascadable to any number of channels**

The CA82C37A is a high performance, programmable Direct Memory Access (DMA) controller offering pin-for-pin functional compatibility with industry standard 8237/8237A. It features four channels, each independently programmable, and is cascadable to any number of channels. Each channel can be programmed to auto-initialize following DMA termination.

In addition, the CA82C37A supports memory-to-memory transfer capability and memory block initialization, as well as a programmable transfer mode.

The CA82C37A is designed to improve system performance by allowing external devices to transfer data directly from the system memory. High speed and very low power consumption make it an ideal component for aerospace and defence applications. The low power consumption also makes it an attractive addition in portable systems, or systems with low power standby modes.

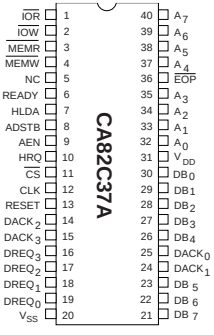


Figure 2-1: PDIP Pin Configurations

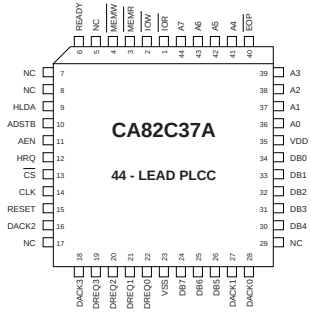


Figure 2-2: PLCC Pin Configurations

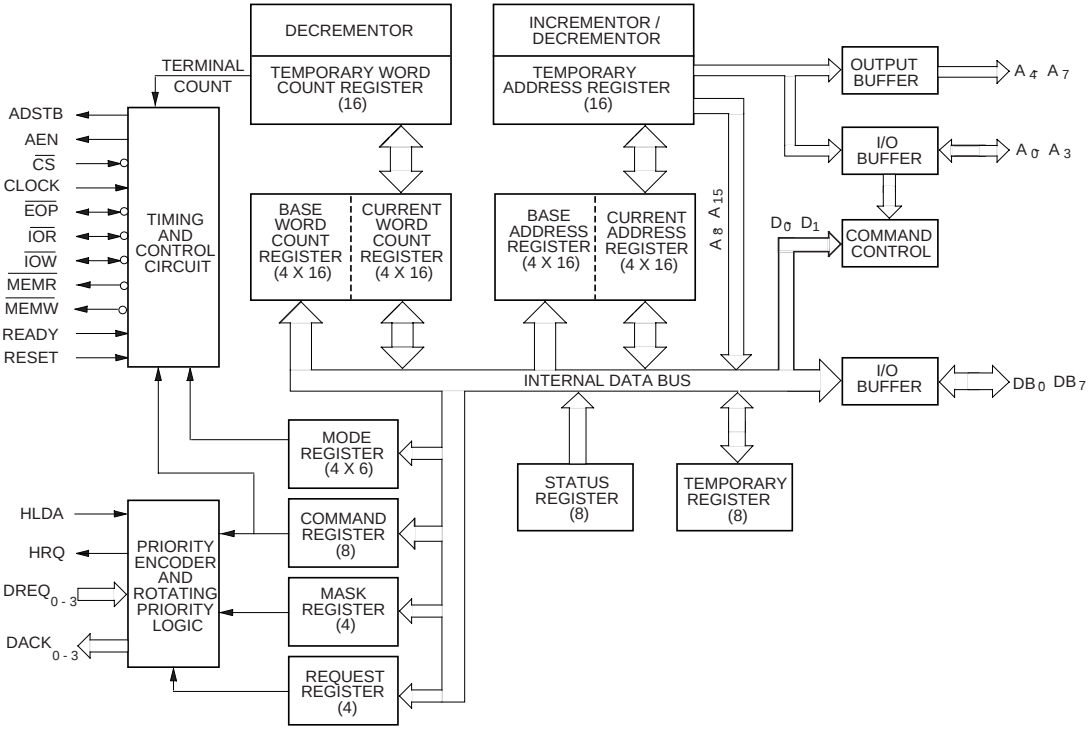


Figure 2-3: CA82C37A Block Diagram

Table 2-1: Pin Descriptions

Symbol	Pins		Type	Name and Function
	PLCC	PDIP		
A_{0-3}	36-39	32-35	I/O	**Low Address Bus**: Bi-directional, 3-state signals. The 4 least significant address lines. Idle Cycle (Inputs). Addresses the CA82C37A control register to be loaded or read. Active Cycle (Outputs). Lower 4 bits of the transfer address.
A_{4-7}	41-44	37-40	O	**High Address Bus**: 3-state output signals. The 4 most significant address lines representing the upper 4 bits of the transfer address. Enabled during DMA service only.
ADSTB	10	8	O	**Address Strobe**: Active HIGH output signal to control latching of the upper address byte. Drives the strobe input of external transparent octal latches. During block operations, ADSTB is activated only if the upper address byte needs updating, eliminating S1 states and accelerating operation.
AEN	11	9	O	**Address Enable**: Active HIGH output signal to enable the 8-bit latch containing the higher order address byte onto the system address bus. During DMA transfers, it can disable other system bus drivers.
CLK	14	12	I	**Clock Input**: Generates timing signals to control internal operations and data transfer rate. Input can be driven from DC to maximum frequency. CLK may be stopped in Active or Idle Cycle for standby operation.
$\overline{CS}$	13	11	I	**Chip Select**: Active LOW input signal to select the CA82C37A as an I/O device (Idle Cycle) for CPU communication on the data bus.
$DACK_{0-3}$	28, 27, 16, 18	14, 15, 24, 25	O	**DMA Acknowledge**: Individual channel active LOW (RESET) or HIGH (programmable) output lines. Informs a peripheral that the requested DMA transfer has been granted.
DB_{0-7}	34-30 26-24	21-23 26-30	I/O	**Data Bus**: Bi-directional tri-state data lines connected to the system data bus. Idle Cycle. During I/O Read (Program condition), outputs are enabled and contents of CA82C37A internal registers are read by the CPU. In I/O Write, outputs are disabled and data from the data bus are written into the registers. Active Cycle. The upper byte of the transfer address is output to the data bus during DMA I/O device to-memory transfers. In memory-to-memory transfers, data is read into the CA82C37A Temporary Register from data bus inputs during the read-from-memory transfer, and written to the new memory location by data bus outputs during the write-to-memory transfer.
$DREQ_{0-3}$	19, 20, 21, 22	16, 17, 18, 19	I	**DMA Request**: Asynchronous DMA service request input lines from I/O devices. DMA service is requested by activation of the channel from a specific device. DREQ must be maintained until DACK (service acknowledge) is activated. I/O Device Priority. Order of service is programmable.Priority may be Fixed (descending order from Channel 0) or Rotating (Most recent channel served gets the lowest priority).

Table 2-1: Pin Descriptions Cont'd

Symbol	Pins		Type	Name and Function
	PLCC	PDIP		
$\overline{EOP}$	40	36	I/O	**End of Process**: Active LOW bi-directional 3-state signal. The CA82C37A terminates DMA service when $\overline{EOP}$ is activated. Internal $\overline{EOP}$ (Output). $\overline{EOP}$ is activated when the word count for any channel turns over from 0000(H) to FFFF(H) and a TC pulse is generated. In memory-to-memory transfers, service is terminated when TC for channel 1 occurs. External $\overline{EOP}$ (Input). An external $\overline{EOP}$ signal pulling $\overline{EOP}$ low terminates active DMA service. An $\overline{EOP}$ signal also resets the DMA request. If auto-initialize is enabled, the base registers are written to the current registers of the channel. If the channel is not programmed for auto-initialize, the mask bit (Mask Register) and TC bit (Status Register) are set for the currently active channel. The mask bit is not changed if the channel is set for autoinitialize. Since $\overline{EOP}$ is driven by an open drain transistor on-chip, it should be maintained HIGH with a pull-up resistor in order to avoid erroneous $\overline{EOP}$ inputs.
HLDA	9	7	I	**Hold Acknowledge**: Active HIGH input signal to the CPU following an HRQ. Notifies the CA82C37A that the CPU has released control of the system buses.
HRQ	12	10	O	**Hold Request**: Active HIGH out put signal to the CPU. Requests control of the system buses. HRQ is issued following a request for DMA service (DREQ) from a peripheral, and is acknowledged by the HLDA signal.
$\overline{IOR}$	2	2	I/O	**I/O Read**: Active LOW bi-directional, 3-state signal. Idle Cycle. CPU input control signal for reading the Control Registers. Active Cycle. Output control signal to read data from a peripheral device during a DMA cycle.
$\overline{IOW}$	2	2	I/O	**I/O Write**: Active LOW bi-directional, 3-state signal. Idle Cycle. CPU input control signal for loading information into the CA82C37A. Active Cycle. Output control signal to load data to a peripheral device during a DMA cycle.
$\overline{MEMR}$	3	3	O	**Memory Read**: Active LOW 3-state output signal. CA82C37A reads data from a selected memory address during a DMA Read or Memory-to-Memory transfer.
$\overline{MEMW}$	4	4	O	**Memory Write**: Active LOW 3-state output signal. CA82C37A writes data to a selected memory address during a DMA Write or Memory-to-Memory transfer.
READY	6	6	I	**Ready**: A LOW Ready signal extends the Memory Read and Write pulse widths from the CA82C37A to accommodate slow I/O peripherals or memories. Transitions must not be made during the specified setup/hold time.
RESET	15	13	I	**Reset**: Active HIGH asynchronous input signal. Clears the Command, Status, Request and Temporary Registers, the Mode Register Counter and the First/Last Flip-Flop. The Mask Register is set to ignore DMA requests. The CA82C37A is in Idle Cycle following Reset.
V_{DD}	35	31	-	**Power**: 5 V ± 10% DC Supply.
V_{SS}	23	20	-	**Ground**: 0 V

FUNCTIONAL DESCRIPTION

The CA82C37A DMA controller is a state-driven address and control signal generator designed to accelerate data transfer in systems by moving data from an I/O device to memory, or a block memory to an I/O device. Data transfers are direct, rather than being stored enroute in a temporary register.

The CA82C37A also mediates memory-to-memory block transfers and will move data from a single location to a memory block. Temporary storage of data is required, but the transfer rate is significantly faster than CPU processes. The device provides operating modes to carry out both single byte and block transfers of data. An operational flowchart of the CA82C37A is shown in Figure 2-4.

The organization of the CA82C37A is shown in the block diagram. It is composed of three logic blocks, a series of internal registers and a counter section. The logic blocks include the Timing Control, Command Control and Priority Encoder circuits.

The Timing Control block generates internal timing signals from the clock input and produces external control signals.

Command Control decodes incoming instructions from the CPU, and the Priority Encoder block regulates DMA channel priority.

The internal registers hold internal states and instructions from the CPU. Addresses and word counts are computed in the counter section.

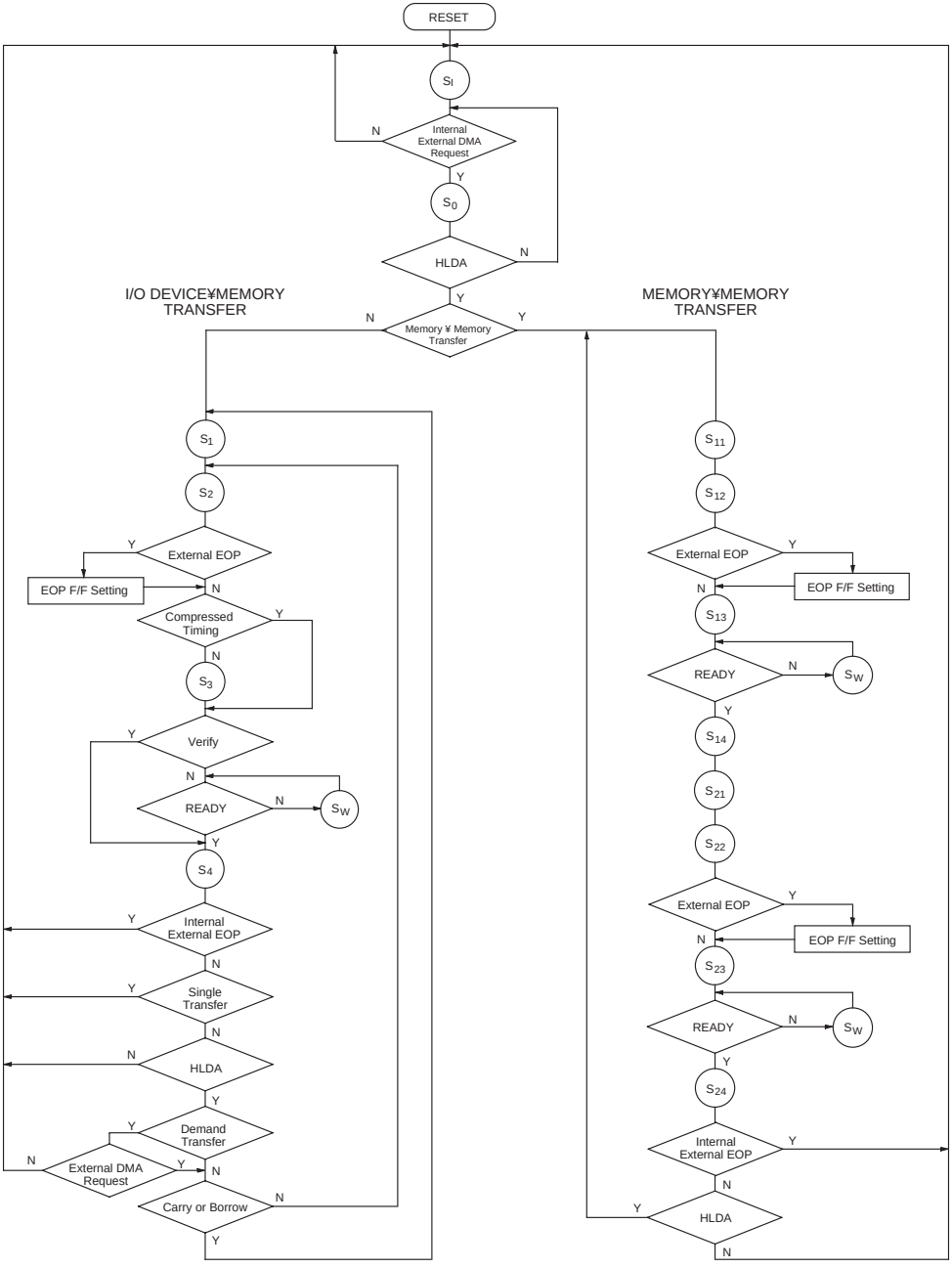


Figure 2-4: Operational Flowchart

Table 2-2: AC Characteristics, DMA (Master) Mode (T_A = -40° to +85°C, V_{DD} = 5V ±10%, V_{SS} = 0V)

Symbol	Parameter	Limits (5 MHz)		Limits (8 MHz)		Limits (10 MHz)		Units
		Min	Max	Min	Max	Min	Max	
t_{AEL}	AEN HIGH from CLK LOW (S_1) Delay Time	-	175	-	105	-	90	ns
t_{AET}	AEN LOW from CLK HIGH (S_1) Delay Time	-	130	-	80	-	80	ns
t_{AFAB}	ADR Active to Float Delay from CLK HIGH	-	90	-	55	-	55	ns
t_{AFC}	$\overline{READ}$ or $\overline{WRITW}$ Float Delay from CLK HIGH	-	120	-	75	-	75	ns
t_{AFDB}	DB Active to Float Delay from CLOCK HIGH	-	170	-	135	-	100	ns
t_{AHR}	ADR from $\overline{READ}$ HIGH Hold Time	t_{CY} - 100	-	t_{CY} - 75	-	t_{CY} - 75	-	ns
t_{AHS}	DB from ADSTB LOW Hold Time (see Note 1)	30	-	25	-	20	-	ns
t_{AHW}	ADR from $\overline{WRITE}$ HIGH Hold Time	t_{CY} - 50	-	t_{CY} - 50	-	t_{CY} - 50	-	ns
t_{AK}	DACK Valid from CLK LOW Delay Time	-	170	-	105	-	90	ns
	$\overline{EOP}$ HIGH from CLK HIGH Delay Time	-	170	-	105	-	90	ns
	$\overline{EOP}$ LOW from CLK HIGH Delay Time	-	100	-	60	-	60	ns
t_{ASM}	ADR Stable from CLK HIGH	-	110	-	90	-	80	ns
t_{ASS}	DB to ADSTB LOW Setup Time	100	-	85	-	50	-	ns
t_{CH}	CLK HIGH Time (Transitions 10 ns)	70	-	55	-	45	-	ns
t_{CL}	CLK LOW Time (Transitions 10 ns)	70	-	55	-	40	-	ns
t_{CY}	CLK Cycle Time	200	-	125	-	100	-	ns
t_{DCL}	CLK HIGH to $\overline{READ}$ or $\overline{WRITE}$ LOW Delay	-	190	-	120	-	90	ns
t_{DCTR}	$\overline{READ}$ HIGH from CLK HIGH (S_4) Delay Time	-	190	-	115	-	95	ns
t_{DCTW}	WRITE HIGH from CLK HIGH (S_4) Delay Time	-	130	-	80	-	80	ns
t_{DQ1}	HRQ Valid from CLK HIGH Delay Time	-	120	-	75	-	75	ns
t_{DQ2}	HRQ Valid from CLK HIGH Delay Time	-	120	-	75	-	75	ns
t_{EPS}	$\overline{EOP}$ LOW from CLK LOW Setup Time	40	-	25	-	25	-	ns
t_{EPW}	$\overline{EOP}$ Pulse Width	220	-	135	-	80	-	ns

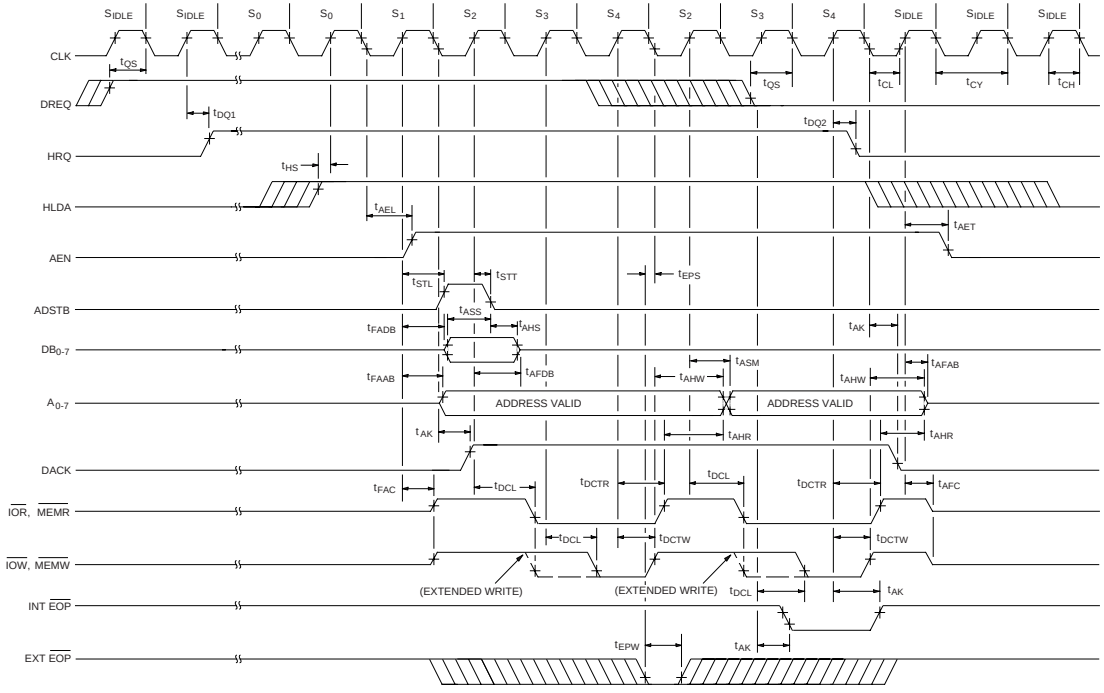
Table 2-2: AC Characteristics, DMA (Master) Mode (T_A = -40° to +85°C, V_{DD} = 5V ±10%, V_{SS} = 0V) Cont'd

Symbol	Parameter	Limits (5 MHz)		Limits (8 MHz)		Limits (10 MHz)		Units
		Min	Max	Min	Max	Min	Max	
t_{FAAB}	ADR Float to Active Delay from CLK HIGH	-	110	-	90	-	80	ns
t_{FAC}	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK HIGH	-	150	-	90	-	90	ns
t_{FADB}	DB Float to Active Delay from CLK HIGH	-	110	-	90	-	80	ns
t_{HS}	HLDA Valid to CLK HIGH Setup Time	75	-	45	-	45	-	ns
t_{IDH}	Input Data from $\overline{MEMR}$ HIGH Hold Time	0	-	0	-	0	-	ns
t_{IDS}	Input Data to $\overline{MEMR}$ HIGH Setup Time	155	-	90	-	80	-	ns
t_{ODH}	Output Data from $\overline{MEMW}$ HIGH Hold Time	15	-	15	-	15	-	ns
t_{ODV}	Output Data Valid to $\overline{MEMW}$ HIGH	125	-	85	-	65	-	ns
t_{QS}	DREQ to CLK LOW (S_1, S_4) Setup Time	0	-	0	-	0	-	ns
t_{RH}	CLK to READY LOW Hold Time	20	-	20	-	10	-	ns
t_{RS}	READY to CLK LOW Setup Time	60	-	35	-	35	-	ns
t_{STL}	ADSTB HIGH from CLK HIGH Delay Time	-	80	-	50	-	50	ns
t_{STT}	ADSTB LOW from CLK HIGH Delay Time	-	90	-	90	-	90	ns

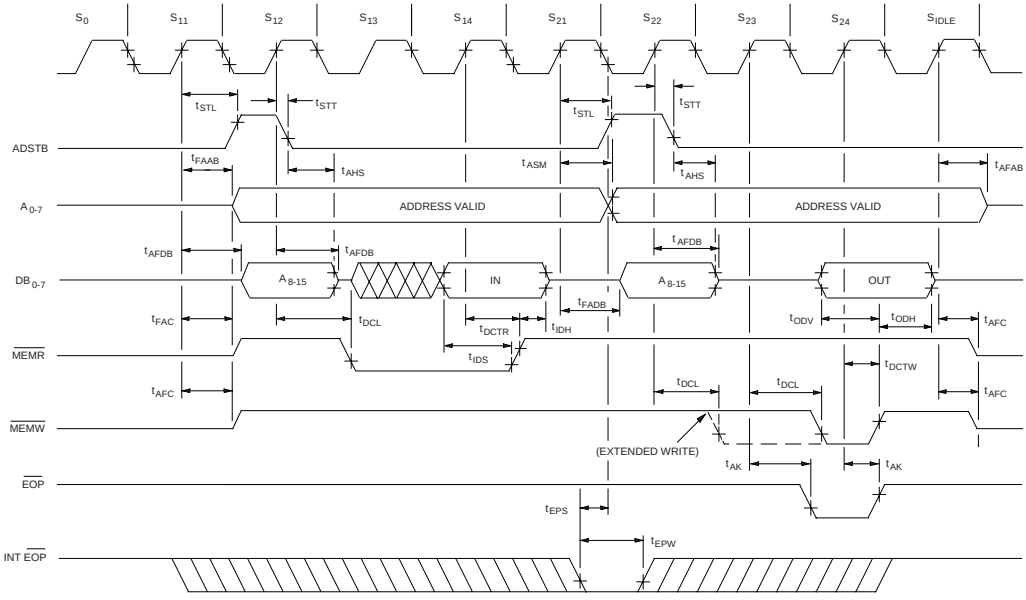
Note 1: t_{AHS} = 20 ns minimum for industrial temperature range devices.

Figure 2-5: Timing Diagrams (Master Mode)

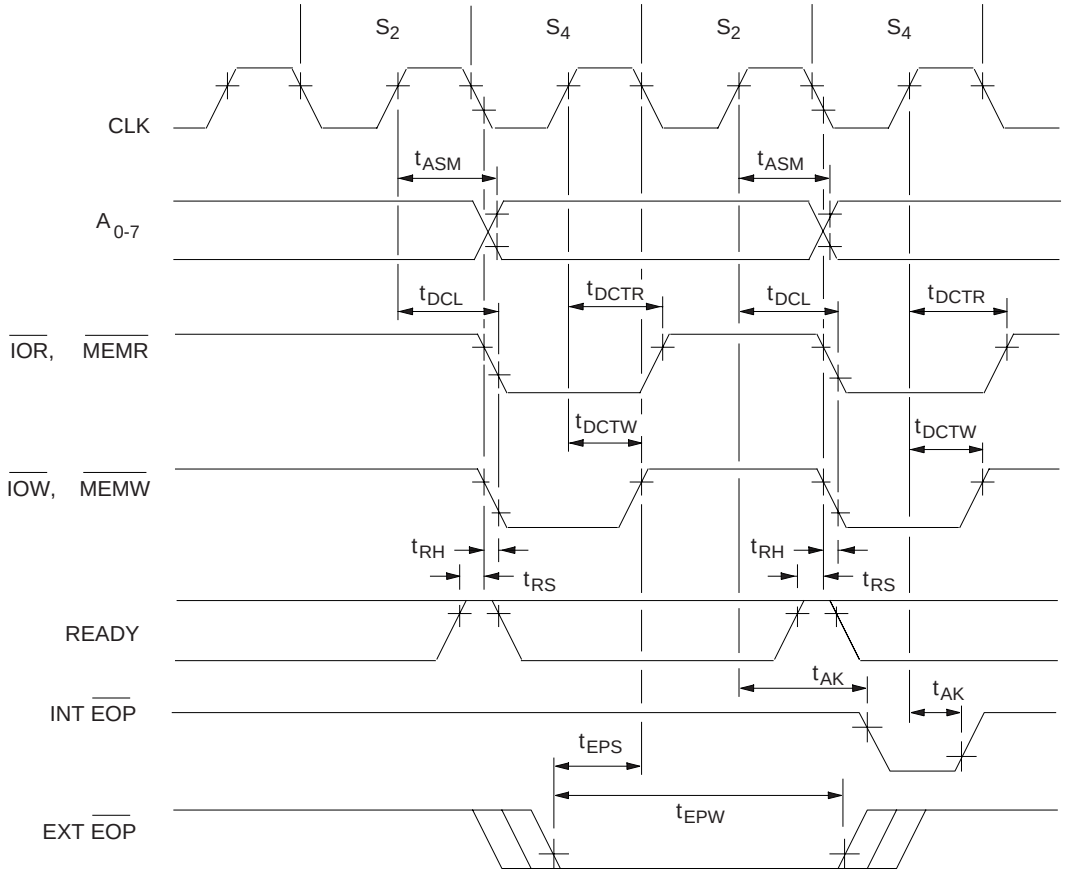
a) DMA Transfer Timing



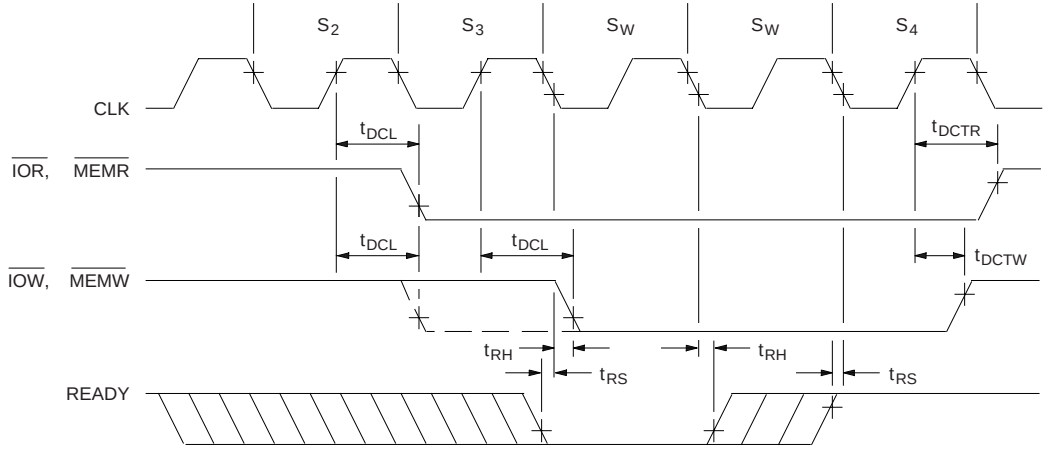
b) Memory-to-Memory Transfer Timing



c) Compressed Transfer Timing



d) Ready Timing



e) Reset Timing

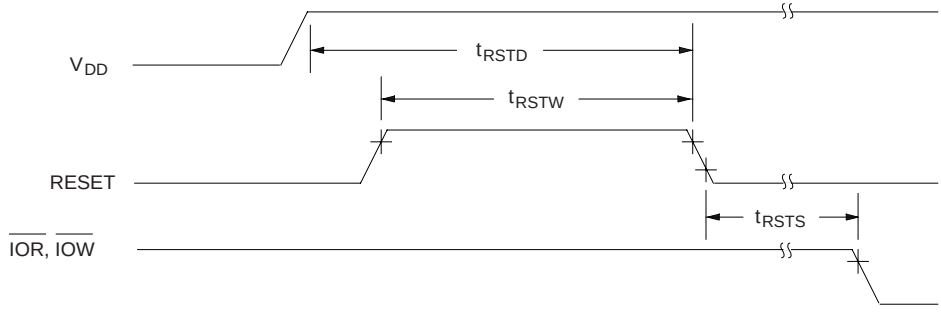
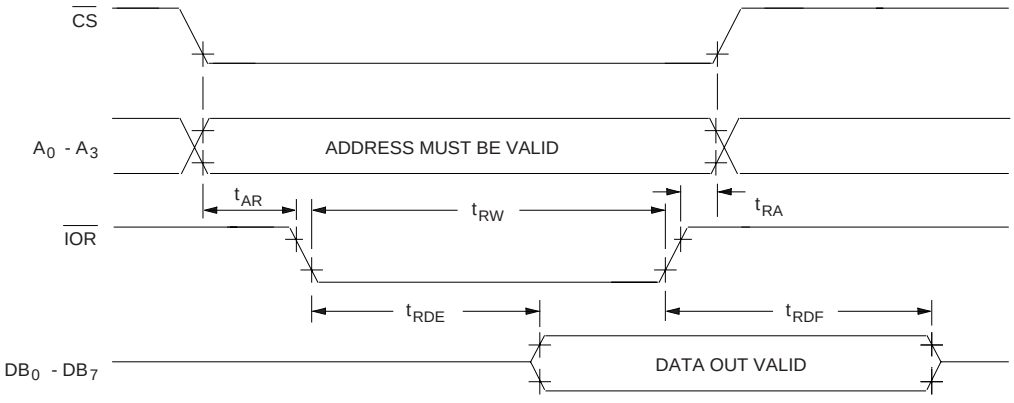


Table 2-3: AC Characteristics, Peripheral (Slave) Mode (T_A = -40° to +85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

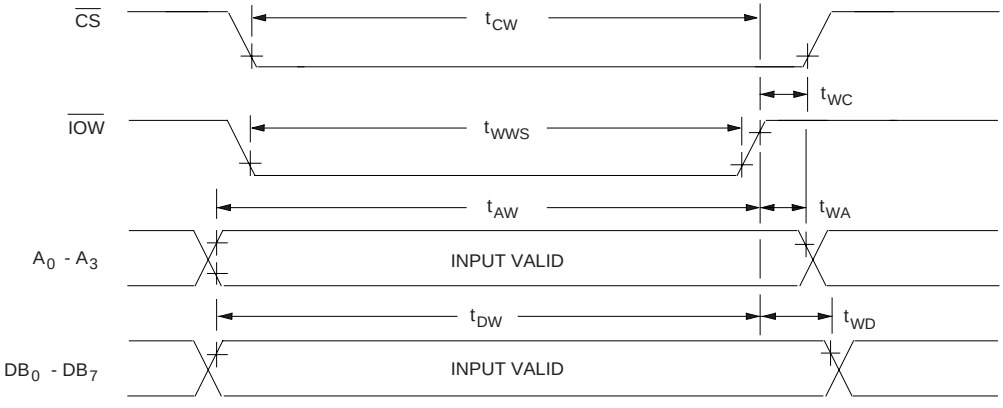
Symbol	Parameter	Limits (5 MHz)		Limits (8 MHz)		Limits (10 MHz)		Units
		Min	Max	Min	Max	Min	Max	
t_{AR}	ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	10	-	10	-	0	-	ns
t_{AW}	ADR Valid to $\overline{WRITE}$ HIGH Setup Time	130	-	90	-	60	-	ns
t_{CW}	$\overline{CS}$ LOW to $\overline{WRITE}$ HIGH Setup Time	130	-	100	-	85	-	ns
t_{DW}	Data Valid to $\overline{WRITE}$ HIGH Setup Time	130	-	90	-	60	-	ns
t_{RA}	ADR or CS Hold from $\overline{READ}$ HIGH	0	-	0	-	0	-	ns
t_{RDE}	Data Access from $\overline{READ}$	-	140	-	120	-	110	ns
t_{RDF}	DB Float Delay from $\overline{READ}$ HIGH	0	70	0	70	0	70	ns
t_{RSTD}	Pwr Supply HIGH to RESET LOW Setup Time	500	-	500	-	500	-	ns
t_{RSTS}	Reset to First $\overline{IOWR}$	$2 \bullet t_{CY}$	-	$2 \bullet t_{CY}$	-	$2 \bullet t_{CY}$	-	ns
t_{RSTW}	RESET Pulse Width	300	-	200	-	100	-	ns
t_{RW}	$\overline{READ}$ Width	200	-	155	-	120	-	ns
t_{WA}	ADR from $\overline{WRITE}$ HIGH Hold Time	0	-	0	-	0	-	ns
t_{WC}	CS HIGH from $\overline{WRITE}$ HIGH Hold Time	0	-	0	-	0	-	ns
t_{WD}	Data from $\overline{WRITE}$ HIGH Hold Time	10	-	10	-	10	-	ns
t_{WWS}	$\overline{WRITE}$ Width	150	-	100	-	90	-	ns

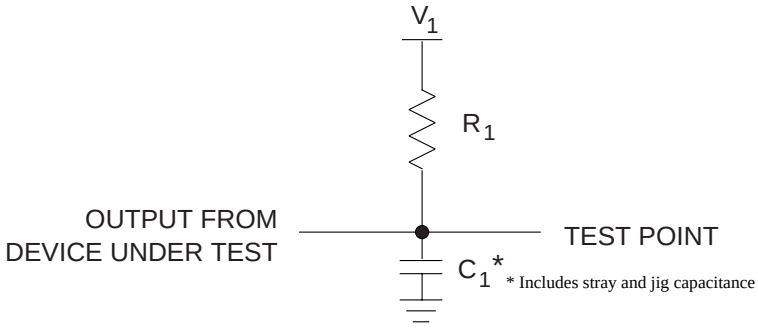
Figure 2-6: Timing Diagrams (Slave Mode)

a) Slave Mode Read Timing



b) Slave Mode Write Timing





Pins	V_1	R_1	C_1
All Outputs Except $\overline{EOP}$	1.7 V	520	100 pF
$\overline{EOP}$	VDD	1.6 k	50 pF

Figure 2-7: AC Test Circuits

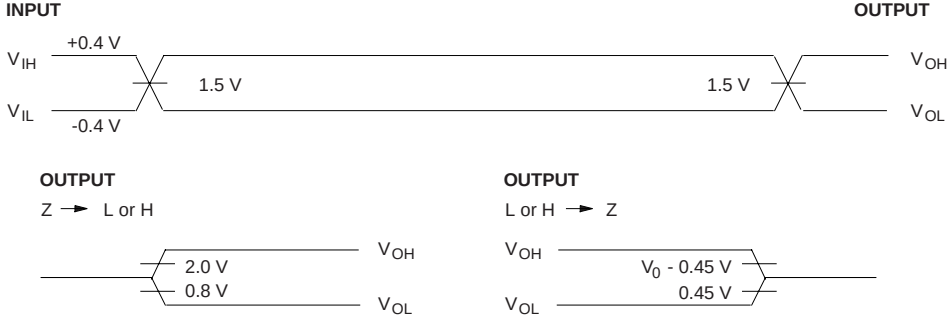


Figure 2-8: AC Testing Input, Output Waveforms

Table 2-4: DC Characteristics (T_A = -40° to +85°C, except as noted, V_{DD}=+5 V ±10%, V_{SS}=0V)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{DDOP}	Operating Power Supply Current	V_{DD} = 5.5 V V_{IN} = V_{DD} or V_{SS} Outputs Open	-	2.0	mA/ mHz
I_{IL}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-1.0	+1.0	µA
I_{OL}	Output Leakage Current	0 V ≤ V_{OUT} ≤ V_{DD}	-10.0	+10.0	µA
V_{IH}	Input High Voltage	Note 8	2.0	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	Note 8	-0.3	0.8	V
V_{IHS}	Schmitt Trigger Input High Voltage	Note 9	2.1	V_{DD} + 0.3	V
V_{ILS}	Schmitt Trigger Input Low Voltage	Note 9	-0.3	0.7	V
V_{HY}	Schmitt Trigger Hysteresis	Note 9	-	0.4	V
V_{OH}	Output High Voltage	IOH = -2.5 mA IOH = -100 µA	2.4 VDD - 0.4	- -	V V
V_{OL}	Output Low Voltage	IOL = +3.2 mA	-	0.4	V

Notes:

1. *Input timing parameters assume rise and fall transition times of 20 ns or less.*
2. *The net $\overline{IOW}$ or $\overline{MEMW}$ pulse width for a normal write will be t_{CY} - 100 ns, and for an extended write will be 2•t_{CY} - 100 ns. The net IOR or MEMR pulse width for a normal read will be 2•t_{CY} - 50 ns and for a compressed read will be t_{CY} - 50 ns.*
3. *DREQ should be held active until DACK is returned.*
4. *DREQ and DACK signals may be active HIGH or active LOW. The timing diagrams assume active HIGH.*
5. *Successive read and/or write operations by the external processor to program or examine the controller must be timed to allow at least 100 ns (CA82C37A-10) and 200 ns (CA82C37A-5) as recovery time between active read or write pulses.*
6. *$\overline{EOP}$ is an open drain output, and requires a pullup resistor to V_{DD}.*
7. *Pin 5 can be either tied to V_{DD}, or left unconnected.*
8. *Applies to pins $\overline{IOR}$, $\overline{IOW}$, DB_{7-0}, A_{3-0} and $\overline{EOP}$*
9. *Applies to pins READY, HLDA, CLK, $\overline{CS}$, RESET and $DREQ_{3-0}$*

Table 2-5: Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0V, V_{IN} = +5 V or V_{SS})

Symbol	Parameter	Test Conditions	Min	Max	Units
$C_{I/O}$	I/O Capacitance	FREQ = 1 MHz Unmeasured pins returned to V_{SS}	-	15	pF
C_{IN}	Input Capacitance		-	10	pF
C_{OUT}	Output Capacitance		-	10	pF

Table 2-6: Recommended Operating Conditions

DC Supply Voltage		+4.5 V to +5.5 V
Operating Temperature Range	Commercial	0°C to +70°C
	Industrial	-40°C to +85°C

Table 2-7: Absolute Maximum Ratings

DC Supply Voltage	-.03 to +7.0 V
Input, Output or I/O Voltage Applied	V_{SS} - 0.3 V to V_{DD} + 0.3 V
Storage Temperature Range	-55°C to +150°C
Maximum Package Power Dissipation	1 W
Input Pin Current (@ 25°C)	-10.0 mA to +10.0 mA
Lead Temperature (soldering: 10 sec.)	300°C

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

INTERNAL REGISTERS

The CA82C37A contains 27 registers that are used internally for control and temporary data storage. These registers are listed in Table 2-8 below, and described in the subsections following.

Table 2-8: Internal Registers

Name	Number	Size
Base Address Registers	4	16-bit
Base Word Count Registers	4	16-bit
Command Register	1	8-bit
Current Address Registers	4	16-bit
Current Word Count registers	4	16-bit
Mask Register	1	4-bit
Mode Registers	4	6-bit
Request Register	1	4-bit
Status Register	1	8-bit
Temporary Address Register	1	16-bit
Temporary Register	1	8-bit
Temporary Word Count Register	1	16-bit

Base Address and Base Word Count Registers

Each of the four (4) channels has a pair of Base Address and Base Word Count Registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values.

The base registers are written simultaneously with their corresponding current register (in 8-bit bytes) by the microprocessor when in the Program Condition. These registers cannot be read by the microprocessor.

Command Register

The operation of the CA82C37A is controlled by the 8-bit Command Register. It is programmed by the microprocessor and is cleared by a Reset or a Master Clear instruction.

Figure 2-9 lists the function of the command bits, while Table 2-12 contains the Read and Write addresses.

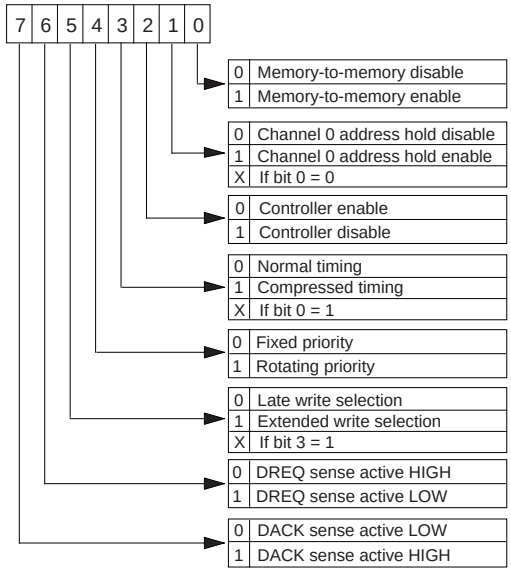


Figure 2-9: Command Register

Current Address Register

Each of the channels has a 16-bit Current Address Register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer, with the values of the address stored in the Current Address Register during the transfer.

This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized (by an Auto-initialize) back to its original value, where an Auto-initialize takes place only after an $\overline{EOP}$.

In memory-to-memory mode, the channel 0 Current Address Register can be prevented from incrementing or decrementing by setting the address hold bit in the Command Register.

Current Word Register

Each of the channels also has a 16-bit Current Word Count register which is used to determine the number of transferso be performed. The actual number of transfers is one more than the number programmed in the Current Word Count

register (i.e. programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer, and when the value in the register goes from zero to FFFFH, a terminal count (TC) is generated.

This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialize back to its original value. Again, Auto-initialization can occur only after an $\overline{EOP}$. If not Auto-initialized, this register will have a count of FFFFH after TC.

Mask Register

Each of the channels has associated with it one mask bit in the 4-bit Mask register which can be set to disable an incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed to Autoinitialize. The Mask Register bit for each channel can be set or cleared either individually or simultaneously as a group under software control.

To set and reset the mask bits for all channels at once, refer to the Write All Mask Bits command in Table 2-12, and to Figure 2-10.

The entire register can also be set by a Reset or Master Clear. This disables all hardware DMA requests until a clear Mask register instruction allows them to occur. The instruction to individually set or clear single mask bits is similar in form to that used with the Request register. Refer to the Figure 2-11 and to Write Single Mask Bit command in Table 2-12 for details.

In reading the Mask Register, bits 4-7 will always read as logical ones, and bits 0-3 will display the mask bits of channel 0-3, respectively. The 4 bits of the Mask Register may be cleared simultaneously by using the Clear Mask Register command (see Table 2-12).

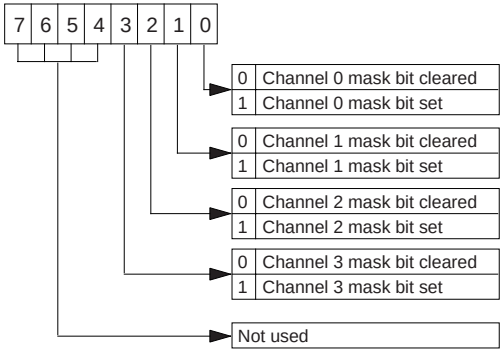


Figure 2-10: Mask Register (Write Operation)

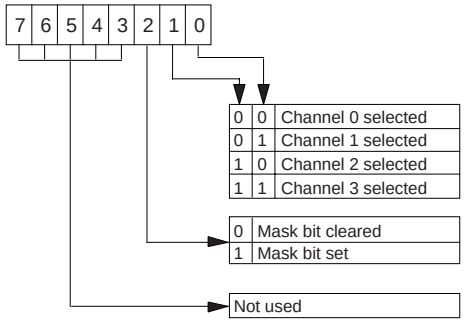


Figure 2-11: Mask Register (Set/Reset

Mode Register

Each of the channels has a 6-bit mode register associated with it. When this register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode Register is to be written. When the processor reads a Mode Register, bits 0 and 1 are both ones. See Figure 2-12 and Table 2-12 for Mode Register functions and addresses.

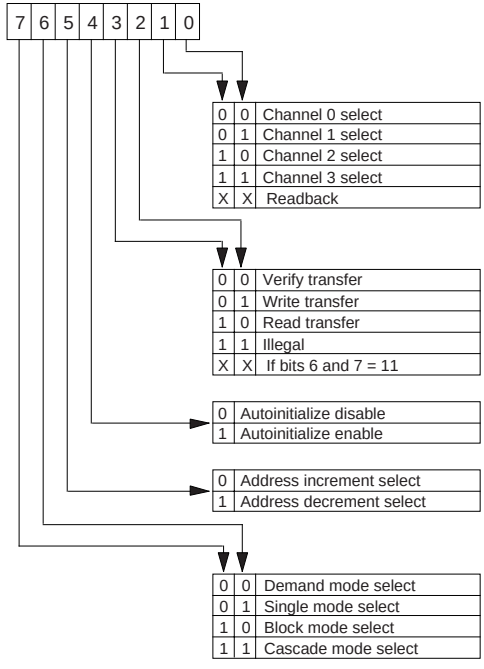


Figure 2-12: Mode Register

Request Register

The CA82C37A responds to requests for DMA service initiated by the software and by a DREQ. Each channel has a non-maskable request bit associated with it in the 4-bit Request Register. These are subject to prioritization by the priority Encoder network with each bit set or reset separately under software control. To set/reset a bit, the software loads the proper form of the data word. The entire register is cleared by a Reset. See Table 2-12 for register address coding, and Figure 2-13 for Request Register format.

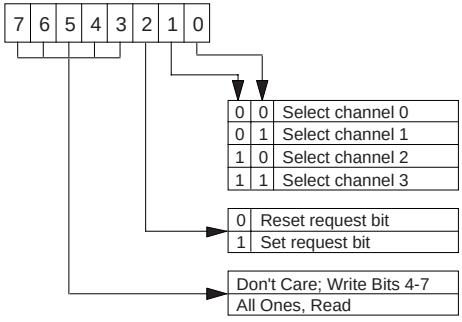


Figure 2-13: Request Register

A software request for DMA operation can be made in block or single modes. For memory-to-memory transfers, the software request for channel 0 should be set. When reading the request register, bits 4-7 will always read as ones, and bits 0-3 will display the request bits of channels 0-3 respectively.

Status Register

The CA82C37A Status Register can be read by the microprocessor. It contains information about which channels have reached a terminal count and which channels have pending DMA requests.

Bits 0-3 are set every time a TC is reached by that channel or an external $\overline{EOP}$ is applied. Theses bits are cleared upon Reset, Master Clear and on each Status Read.

Bits 4-7 are set whenever their corresponding channel is requesting service, regardless of the mask bit state. If the mask bits are set, software can poll the status register to determine which channels have DREQs, and selectively clear a mask bit, thus allowing user defined service priority. Status bits 4-7 are updated while the clock is high, and latched on the falling edge. Status bits 4-7 are cleared upon Reset or Master Clear.

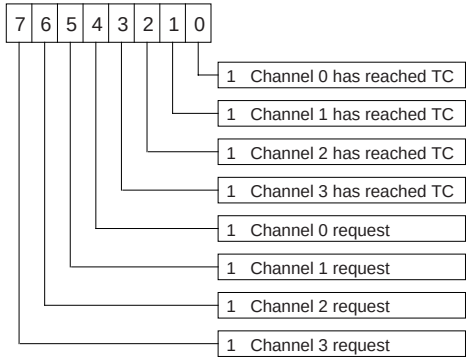


Figure 2-14: Status Register

Temporary Register

The Temporary Register is used to hold data during memory-to-memory transfers. When the transfers are completed, the last word moved can be read by the microprocessor.

Note that the Temporary Register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset or Master Clear.

OPERATIONAL DESCRIPTION

DMA Operation

In a system, the CA82C37A address and control outputs and data bus pins are usually connected in parallel with the system buses with an external latch required for the upper address byte. When inactive, the controller's outputs are in a high impedance state. When activated by a DMA request (and bus control has been relinquished by the host), the CA82C37A drives the buses and generates the control signals to perform the data transfer. The operation performed by activating one of the four DMA request inputs has previously been programmed into the controller via the command, mode, address, and word count registers.

For example, if a block of data is to be transferred from RAM to an I/O device, the starting address of the data is loaded into the CA82C37A Current and Base Address Registers for a particular channel, and the length of the block is loaded into that channel's Word Count Register. The corresponding Mode Register is programmed for a memory-to-I/O operation (read transfer) with various options selected by the Command Register and other Mode Register bits. The channel's mask bit is cleared to enable recognition of a DMA request (DREQ), where the DREQ can be generated by a hardware signal or by a software command.

Once initiated, the block DMA transfer proceeds as the controller outputs the data address, simultaneous $\overline{MEMR}$ and $\overline{IOW}$ pulses, then selects an I/O device via the DMA acknowledge (DACK) outputs. The data byte flows directly from the RAM to the I/O device. After each byte is transferred, the address is automatically incremented (or decremented) and the word count is decremented. The operation is then repeated for the next byte. The controller stops transferring data when the word count register underflows, or an external $\overline{EOP}$ is applied.

To better understand CA82C37A operation, consider the states generated by each clock cycle. The DMA controller operates in two major cycles, active and idle. After being programmed, the controller is normally idle until a DMA request occurs on an unmasked channel, or a software request is given. The CA82C37A then requests control of the system buses and enters the active cycle. The active cycle is composed of several internal states, depending on the options that have been selected and the type of operation that has been requested.

When performing I/O-to-memory or memory-to-I/O DMA the CA82C37A can enter seven distinct states, each composed of one full clock period. State 1 (S_{idle}) is the idle state. It is entered when the CA82C37A has no valid DMA requests pending, at the end of a transfer sequence, or when a Reset or Master Clear occurs. While in S_{idle}, the DMA controller is inactive, though it may be in the process of being programmed by the processor (Program Condition).

State 0 (S0) is the first state of a DMA service. The CA82C37A has requested a hold but the processor has not yet returned an acknowledge. The CA82C37A may still be programmed until it has received HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3, and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the Ready line on the CA82C37A.

Note that the data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active at the same time. The data is neither read into nor driven out of the CA82C37A in I/O-to-memory or memory-to-I/O transfers.

The CA82C37A can enter eight distinct states when performing memory-to-memory DMA, each composed of one full clock period. Four states are required for the read-from-memory step, and four for the write-to-memory operations. Data bytes in transit are stored briefly in the Temporary Register.

Table 2-9: Memory-to-Memory Transfer States

Transfer States	State Numbers	Notes
Read-from-Memory	S11, S12, S13, S14	Memory-to-Memory transfers require 8 states for a single transfer, 4 states for the Read-to-Memory half, and 4 Write-to-Memory states to complete the transfer.
Write-to-Memory	S21, S22, S23, S24	

Idle Cycle

When none of the channels is requesting service, the CA82C37A enters the Idle cycle and performs Sidle states. In this cycle, the CA82C37A samples the DREQ lines on the falling edge of every clock cycle to determine if any channel is requesting a DMA service.

Note that DMA requests will be ignored in standby operation where the clock has been stopped. The device will respond to a $\overline{cs}$ (chip select), in case of an attempt by the micro-processor to write or read the internal registers of the CA82C37A. When $\overline{cs}$ is low and HLDA is low, the CA82C37A enters the Program Condition. The CPU can then establish, change or inspect the internal definition of the part by reading or writing the internal registers.
The CA82C37A may be programmed with the clock stopped, provided HLDA is low and at least one rising clock edge occurred after HLDA was driven low, so the controller is in a S_{idle} state. Address lines A_0 - A_3 are inputs to the device and select which registers are read or written. The $\overline{ior}$ and $\overline{iow}$ lines are used to select and time the read or write operations.

Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional address bit. This bit is used to determine the upper or lower byte of the 16-bit Address and Word Count registers. The flip-flop is reset by a Master Clear or Reset. Separate software commands can also set or reset this flip-flop.

Special software commands can be executed by the CA82C37A in the Program Condition. These commands are decoded as sets of addresses with $\overline{cs}$, $\overline{ior}$, and $\overline{iow}$, and do not make use of the data bus. The commands include: Set and Clear First/Last Flip-Flop, Master Clear, Clear Mode Register Counter, and Clear Mask Register.

Active Cycle

When the CA82C37A is in the Idle cycle, and a software request or an unmasked channel requests a DMA service, the device outputs an HRQ to the micro-processor and enters the Active cycle. It is in this cycle that the DMA service will take place, in one of the four modes described below:

Single Transfer Mode

In single transfer Mode, the device is programmed to make one transfer only. The word count is decremented and the address decremented or incremented following each transfer. When the word count rolls over from zero to FFFFH, a terminal count bit in the Status Register is set, an $\overline{eop}$ pulse is generated, and the channel autoinitializes if this option has been selected. If not programmed to Autoinitialize, the mask bit is set, along with the TC bit and $\overline{eop}$ pulse.

DREQ must be held active until DACK becomes active. If DREQ is held active throughout the single transfer, HRQ goes inactive and releases the bus to the system. It again goes active and, upon receipt of a new HLDA, another single transfer is performed, unless a higher priority channel takes over. In 8080A, 8085A, or 8088/86 systems, this ensures one full machine cycle execution between DMA transfers. Details of the timing between the CA82C37A and other bus control protocols depends upon the characteristics of the microprocessor involved.

Block Transfer Mode

In Block Transfer Mode, the CA82C37A is activated by DREQ or software request and continues making data transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process ($\overline{eop}$) is encountered. DREQ need only be held active until DACK becomes active. Again, Autoinitialization occurs at the end of the service if the channel has been programmed for that option.

Demand Transfer Mode

In Demand Transfer Mode the CA82C37A continues making transfers until a TC or an external $\overline{eop}$ is encountered, or until DREQ goes inactive. Thus, transfers continue until the I/O device has exhausted its data capacity. When the I/O device has caught up, DMA service is re-established by means of a DREQ. In the interim between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the CA82C37A Current Address and Current Word Count Registers.

Higher priority channels may intervene in the demand process, once DREQ has gone inactive. Only an EOP can cause an Autoinitialization at the end of the service. The EOP is generated either by TC or by an external signal.

Cascade Mode

This mode is used to cascade more than one CA82C37A for simple system expansion. The HRQ and HLDA signals from additional CA82C37A devices are connected, respectively, to the DREQ and DACK signals of a channel in the initial CA82C37A. This allows the DMA requests of the additional devices to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial CA82C37A is used only for setting the priority of additional devices, it does not output an address or control signals of its own. These could conflict with the outputs of the active channel in the extra devices.

The CA82C37A will respond to DREQ and generate DACK but all other outputs except HRQ will be disabled. An external EOP will be ignored by the initial device, but will have the usual effect on the added device.

Figure 2-15 shows two additional devices cascaded with an initial device and using two of the initial device's channels. This forms a two-level DMA system. More CA82C37As could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

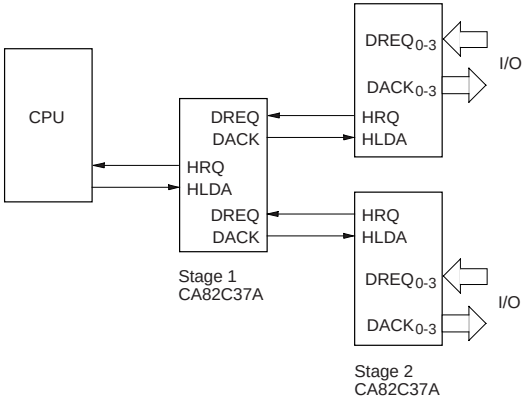


Figure 2-15: Cascaded CA82C37As

When programming cascaded controllers, start with the first level device (the one closest to the microprocessor). After Reset, the DACK outputs are programmed to be active low and are held in the high state. If they are used to drive HLDA directly, the second level device(s) cannot be programmed until DACK polarity is selected as active high on the initial device. In addition, the initial device's mask bits function normally on cascaded channels, so they may be used to inhibit second-level services.

Transfer Types

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{\text{MEMW}}$ and $\overline{\text{IOR}}$. Read transfers move data from memory to an I/O device by activating $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$ (refer to Table 2-10).

Verify transfers are pseudo-transfers. The CA82C37A operates like Read or Write transfers, generating addresses and responding to $\overline{\text{EOP}}$, etc., however the memory and I/O control lines all remain inactive. Verify mode is not allowed for memory-to-memory operation. Note that Ready is ignored during verify transfers.

Table 2-10: I/O Memory Transfer States *

Operational State	Description	Notes
S1	AEN High Low Order Bits: A_0 - A_7 High Order Bits: DB_0 - DB_7 ADSTB High DACK Active	S1 state is omitted if there is no change in the 8 high order bit transfer address during demand and block mode transfers.
S2	$\overline{\text{IOR}}$ Low or $\overline{\text{MEMR}}$ goes Low	S2 state (and S3) are I/O or memory I/O timing control states
S3	$\overline{\text{IOW}}$ Low or $\overline{\text{MEMW}}$ goes Low	S3 is omitted when compressed timing is used.
S4	$\overline{\text{IOR}}$ High $\overline{\text{IOW}}$ High $\overline{\text{MEMR}}$ High $\overline{\text{MEMW}}$ High Word count register decremented by 1 Address register incremented (or decremented) by 1	S4 state completes the DMA transfer of one word.

* In I/O memory transfers, data is transferred directly without being handled by the CA82C37A.

Auto-initialize

By programming a bit in the Mode Register, a channel may be set up as an Auto-initialize channel. During Auto-initialization, the original values of the Current Address and Current Word Count Registers are automatically restored from the Base Address and Base Word Count Registers of that channel following $\overline{EOP}$. The base registers are loaded at the same time as the current registers by the micro-processor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in Autoinitialize. Following Auto-initialization, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected, or a software request is made.

Memory-to-Memory

The CA82C37A incorporates a memory-to-memory transfer feature, to perform block moves of data from one memory address space to another with minimum of program effort and time. Programming bit 0 in the Command Register selects channels 0 and 1 to operate as memory-to-memory transfer channels.

The transfer is initiated by setting the software or hardware DREQ for channel 0. The CA82C37A requests a DMA service in the normal manner. When HLDA goes high, the device, using four-state transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the CA82C37A internal Temporary Register. Another four-state transfer moves the data to memory using the address in the channel 1 Current Address register. The Current Address is incremented or decremented in the normal manner, and the channel 1 Current Word Count is decremented.

When the word count of channel 1 goes to FFFFH, a TC is generated, causing an $\overline{EOP}$ output which terminates the service. When Channel 0 word count decrements to FFFFH the channel 0 TC bit in the Status Register is not set nor is an $\overline{EOP}$ generated in this mode. However, channel 0 is Auto-initialized, if that option has been selected.

If full Auto-initialization for a memory-to-memory operation is desired, the channel 0 and channel 1 word counts must be set to the same value before the transfer begins. Otherwise, should channel 0 underflow before channel 1, it Auto-initializes and sets the data source address back to the beginning of the block. Should the channel 1 word count underflow before channel 0, the memory-to-memory DMA service terminates, and channel 1 Auto-initializes but not channel 0.

In memory-to-memory mode, Channel 0 may be programmed to retain the same address for all transfers, allowing a single byte to be written to an entire block of memory. This channel 0 address hold feature is selected by bit 1 in the Command Register.

The CA82C37A responds to external $\overline{EOP}$ signals during memory-to-memory transfers, but only relinquishes the system buses after the transfer is complete (i.e. after an S24 state). Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of memory-to-memory transfers is found in Figure 2-5b. Memory-to-memory operations can be detected as an active AEN with no DACK outputs.

Priority

The CA82C37A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon their descending numerical value. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After a channel has been recognized for service, remaining channels are prevented from interfering with the service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotated accordingly. The next lower channel from the channel serviced has highest priority on the following request. Priority rotates every time control of the system buses is returned to the CPU.

Table 2-11: Priority Decision Modes

Priority Mode		Fixed	Rotating			
Service Terminated Channel		-	CH_0	CH_1	CH_2	CH_3
Order of priority or next DMA	Highest	CH_0	CH_1	CH_2	CH_3	CH_0
		CH_1	CH_2	CH_3	CH_0	CH_1
		CH_2	CH_3	CH_0	CH_1	CH_2
	Lowest	CH_3	CH_0	CH_1	CH_2	CH_3

With rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. Thus any one channel is prevented from monopolizing the system.

Note that regardless of which priority scheme is chosen, priority is evaluated every time a HLDA is returned to the CA82C37A.

Compressed Timing

In order to achieve even greater throughput where system characteristics permit, the CA82C37A can compress the transfer time to two clock cycles. From Figure 2-5a it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when

A8 - A15 need updating (see Address Generation). Timing for compressed transfers is found in Figure 2-5c. $\overline{EOP}$ will be output in S2 if compressed timing is selected.

Compressed timing is not allowed for memory-to-memory transfers.

Address Generation

In order to reduce the pin count, the CA82C37A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. Lower order address bits are output by the CA82C37A directly. Lines A_0 - A_7 should be connected to the address bus. The timing diagram of Figure 2-5a shows the time relationships between CLK, AEN, ADSTB, DB_0 - DB_7 and A_0 - A_7.

During Block and Demand Transfer mode service, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A_7 to A_8 takes place in the normal sequence of addresses. To save time and speed transfers, the CA82C37A executes the S1 states only when updating of A_8 - A_{15} in the latch is necessary. This means for long services, S1 states and ADSTB may occur only once every 256 transfers, a saving of 255 clock cycles for each 256 transfers.

External EOP Operation

The $\overline{EOP}$ pin is bidirectional and open drain, and can be driven by external signals to terminate DMA operation. It is important to note that the CA82C37A will not accept external $\overline{EOP}$ signals when it is in an S_{idle} state. The controller must be active to latch external $\overline{EOP}$. Once latched, the external $\overline{EOP}$ will be acted upon during the next S2 state, unless the CA82C37A enters an idle state first. In the latter case, the latched $\overline{EOP}$ is cleared. External $\overline{EOP}$ pulses that occur between active DMA transfers in demand mode are not recognized, since the CA82C37A is in an S1 state.

PROGRAMMING

The CA82C37A accepts programming from the host processor any time that HLDA is inactive, and at least one rising clock edge has occurred after HLDA has gone low. It is necessary for the host processor to ensure that programming and HLDA are mutually exclusive. Note that a problem can occur if a DMA request occurs on an unmasked channel while the CA82C37A is being programmed. For example: where the CPU is starting to reprogram the two byte Address Register of channel 1 when channel 1 receives a DMA request: if the CA82C37A is enabled (bit 2 in the Command Register is set to 0), and channel 1 is unmasked, then a DMA service will occur after only one byte of the Address Register has been reprogrammed. This condition can be avoided by disabling the controller (bit 2 in the Command Register is set to 1) or masking the channel before programming any of its registers. Once the programming is complete, the controller can be enabled or the channel unmasked.

It is highly recommended that after power-up all internal locations be loaded with some known value, even if some channels are unused.

Table 2-12: Software Command and Register Codes

Operation	A_3	A_2	A_1	A_0	$\overline{IOR}$	$\overline{IOW}$
Read Status Register	1	0	0	0	0	1
Write Command Register	1	0	0	0	1	0
Read Request Register	1	0	0	1	0	1
Write Request Register	1	0	0	1	1	0
Read Command Register	1	0	1	0	0	1
Write Single Bit Mask	1	0	1	0	1	0
Read Mode Register	1	0	1	1	0	1
Write Mode Register	1	0	1	1	1	0
Set Byte Pointer F/F	1	1	0	0	0	1
Clear Byte Pointer F/F	1	1	0	0	1	0
Read Temporary Register	1	1	0	1	0	1
Master Clear	1	1	0	1	1	0
Clear Mode Register Counter	1	1	1	0	0	1
Clear Mask Register	1	1	1	0	1	0
Read All Mask Bits	1	1	1	1	0	1
Write All Mask Bits	1	1	1	1	1	0

Software Commands

There are several special software commands which can be executed by reading or writing to the CA82C37A. These commands do not depend on the specific data pattern on the data bus, but are activated by the I/O operation itself. Note that on read type commands, the data value is not guaranteed.

The CA82C37A software commands are summarized below:

Clear First/Last Flip-Flop

This command is executed prior to writing or reading new address or word count information to the CA82C37A. It initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor address upper and lower bytes in the correct sequence.

Set First/Last Flip-Flop

This command sets the flip-flop to first select the high byte on read and write operations to Address and Word Count Registers.

Master Clear

This software command has the same effect as the hardware Reset. The Command, Status, Request, and Temporary Registers, and the Internal First/Last Flip-Flop and Mode Register counter are cleared and the Mask Register is set. The device then enters the Idle cycle.

Clear Mask Register

This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Clear Mode Register Counter

Since only one address location is available for reading Mode Registers, an internal two-bit counter is included to select Mode Registers during read operations.

To read the Mode Registers, first execute the Clear Mode Register Counter command, then do consecutive reads until the desired channel is read. Read order is channel 0 first, channel 3 last. The lower two bits on all Mode Registers will read as ones.

Table 2-13: Word Count and Address Register Command Codes

Channel	Register	Operation	Signals							Internal Flip-Flop	Data Bus DB_0 - DB_7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A_3	A_2	A_1	A_0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A_0 - A_7
			0	1	0	0	0	0	0	1	A_8 - A_{15}
	Current Address	Read	0	0	1	0	0	0	0	0	A_0 - A_7
			0	0	1	0	0	0	0	1	A_8 - A_{15}
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W_0 - W_7
			0	1	0	0	0	0	1	1	W_8 - W_{15}
	Current Word Count	Read	0	0	1	0	0	0	1	0	W_0 - W_7
			0	0	1	0	0	0	1	1	W_8 - W_{15}
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A_0 - A_7
			0	1	0	0	0	1	0	1	A_8 - A_{15}
	Current Address	Read	0	0	1	0	0	1	0	0	A_0 - A_7
			0	0	1	0	0	1	0	1	A_8 - A_{15}
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W_0 - W_7
			0	1	0	0	0	1	1	1	W_8 - W_{15}
	Current Word Count	Read	0	0	1	0	0	1	1	0	W_0 - W_7
			0	0	1	0	0	1	1	1	W_8 - W_{15}
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A_0 - A_7
			0	1	0	0	1	0	0	1	A_8 - A_{15}
	Current Address	Read	0	0	1	0	1	0	0	0	A_0 - A_7
			0	0	1	0	1	0	0	1	A_8 - A_{15}
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W_0 - W_7
			0	1	0	0	1	0	1	1	W_8 - W_{15}
	Current Word Count	Read	0	0	1	0	1	0	1	0	W_0 - W_7
			0	0	1	0	1	0	1	1	W_8 - W_{15}
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A_0 - A_7
			0	1	0	0	1	1	0	1	A_8 - A_{15}
	Current Address	Read	0	0	1	0	1	1	0	0	A_0 - A_7
			0	0	1	0	1	1	0	1	A_8 - A_{15}
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W_0 - W_7
			0	1	0	0	1	1	1	1	W_8 - W_{15}
	Current Word Count	Read	0	0	1	0	1	1	1	0	W_0 - W_7
			0	0	1	0	1	1	1	1	W_8-W_{15}

APPLICATIONS

Figure 2-16 shows an application for a DMA system utilizing the CA82C37A DMA controller and an 80C88 microprocessor. The CA82C37A DMA controller is used here to improve system performance by allowing an I/O device to transfer data directly to, or from the system memory.

Components

The system clock is generated by the CA82C84A clock driver and is inverted to meet the clock high and low times required by the CA82C37A DMA controller. The four OR gates are used to support an 80C88 microprocessor in minimum mode by producing the control signals used by the processor to access memory or I/O. A decoder is used to generate the chip select for the DMA controller and memory.

Since the most significant bits of the address are output on the address/data bus, an 82C82 octal latch is used to demultiplex the address. Hold Acknowledge (HLDA) and Address Enable (AEN) are ORed together to insure that the DMA controller does not encounter bus contention with the microprocessor.

Operation

A DMA request (DREQ) is generated by the I/O device. After receiving the DMA request, the DMA controller issues a Hold Request (HRQ) to the microprocessor. The system buses are not released to the DMA controller until a Hold Acknowledge signal is returned to the DMA controller from the 80C88 processor. After the Hold Acknowledge has been received, addresses and control signals are generated by the DMA controller to accomplish the DMA transfers. Data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active. Recall that data is not read into or driven out of the DMA controller in I/O-to-memory or memory-to- I/O data transfers.

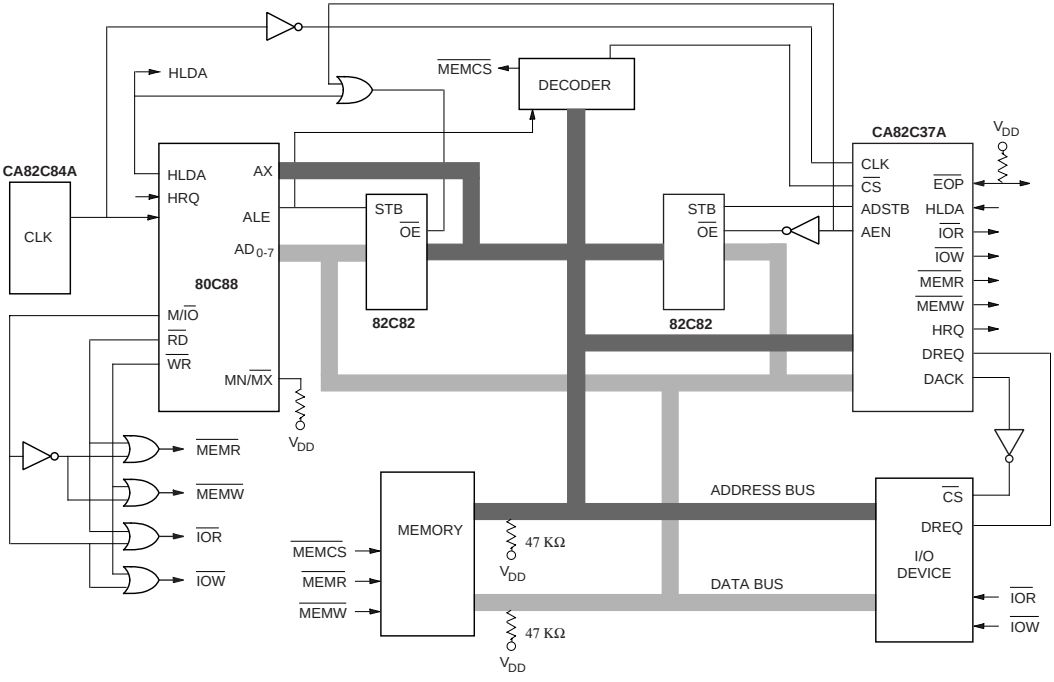


Figure 2-16: Application for DMA System

CA82C52

CMOS SERIAL CONTROLLER INTERFACE

- **Pin and functional compatibility with the industry standard 8252**
- **TTL Input/output compatibility**
- **Low power CMOS implementation**
- **High speed - DC to 16 MHz operation**
- **Single chip UART/BRG**
- **Crystal or external clock input**
- **On chip baud rate generator featuring 72 selectable baud rates**
- **Interrupt mode with mask capability**
- **Microprocessor bus oriented interface**
- **Line break generation and detection**
- **Loopback and echo modes**
- **Fully static operation**

The Tundra CA82C52 is a high performance, single chip programmable Universal Asynchronous Receiver/ Transmitter (UART) and Baud Rate Generator (BRG). The Baud Rate Generator can be programmed for one of 72 different baud rates using a single industry standard crystal or external frequency source. A programmable buffered clock output is available and can be programmed to provide either a buffered oscillator or 16X baud rate clock for general purpose system usage.

The CA82C52 features full TTL/CMOS compatibility, allowing it to be designed into mixed TTL/NMOS/CMOS system environments.

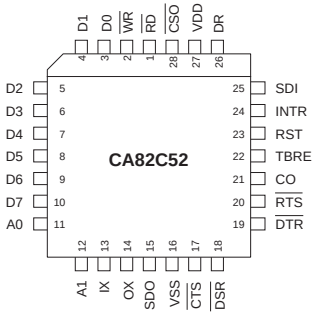


Figure 2-1: PLCC Pin Configurations

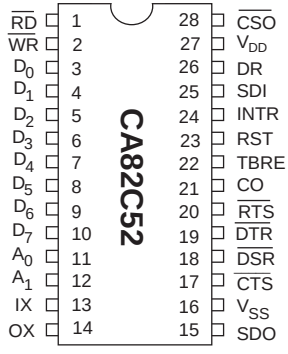


Figure 2-2: PDIP Pin Configurations

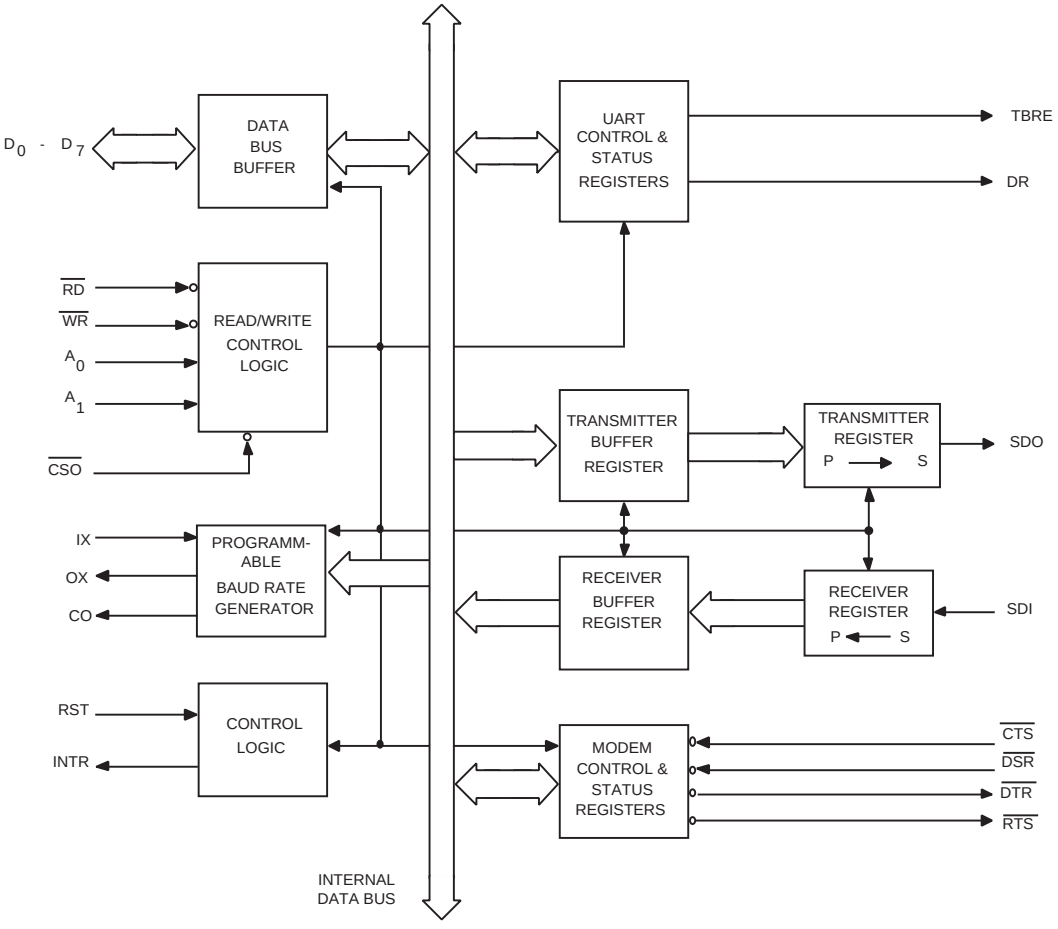


Figure 2-3: CA82C52 Block Diagram

Table 2-1: Pin Descriptions

Symbol	Pins		Type	Name and Function
	PLCC	PDIP		
A_0, A_1	11, 12	11, 12	I	Address Inputs: The address lines select the various internal registers during CPU bus operations.
CO	21	21	O	Clock Out: This output is user programmable to provide either a buffered IX output or a buffered Baud Rate Generator (16x) clock output. The buffered IX (Crystal or external clock source) output is provided when the Baud Rate Select Register (BRSR) bit 7 is set to a zero. Writing a logic one to BRSR bit 7 causes the CO output to provide a buffered version of the internal Baud Rate Generator clock which operates at 16 times the programmed baud rate.
$\overline{CSO}$	28	28	I	Chip Select: Chip select acts as an enable signal for the $\overline{RD}$ and $\overline{WR}$ input signals.
$\overline{CTS}$	17	17	I	Clear to Send: The logical state of the $\overline{CTS}$ line is reflected in the $\overline{CTS}$ bit of the Modem Status Register. Any change of state in $\overline{CTS}$ causes INTR to be set true when INTEN and MIEN are true. A false level on $\overline{CTS}$ will inhibit transmission of data on the SDO output and will hold SDO in the Mark (high) state. If $\overline{CTS}$ goes false during transmission, the current character being transmitted will be completed. $\overline{CTS}$ does not affect Loop Mode operation.
D_0 - D_7	3 - 10	3 - 10	I/0	Data Bits 0 - 7: The Data Bus provides eight, 3-state input/output lines for the transfer of data, control and status information between the CA82C52 and the CPU. For character formats of less than 8 bits, the corresponding D_7, D_6 and D_5 are considered don't cares for data write operations and are 0 for data read operations. These lines are normally in a high impedance state except during read operations. D_0 is the Least Significant Bit (LSB) and is the first serial data bit to be received or transmitted.
DR	26	26	O	Data Ready: A true level indicates that a character has been received, transferred to the RBR and is ready for transfer to the CPU. DR is reset on a data READ of the Receiver Buffer Register (RBR) or when RST is true.
$\overline{DSR}$	18	18	I	Data Set Ready: The logical state of the $\overline{DSR}$ line is reflected in the Modem Status Register. Any change of state of $\overline{DSR}$ will cause INTR to be set if INTEN and MIEN are true. The state of this signal does not affect any other circuitry within the CA82C52
$\overline{DTR}$	19	19	O	Data Terminal Ready: The $\overline{DTR}$ signal can be set low by writing a logic 1 to the appropriate bit in the Modem Control Register (MCR). This signal is cleared high by writing a logic 0 to the $\overline{DTR}$ bit in the MCR or whenever a RST (high) is applied to the CA82C52.
INTR	24	24	O	Interrupt Request: The INTR output is enabled by the INTEN bit in the Modem Control Register (MCR). The MIEN bit selectively enables modem status changes to provide an input to the INTR logic. Figure 2-16 shows the overall relationship of these interrupt control signals.
IX, OX	13, 14	13, 14	I/O	Crystal/Clock: Crystal connections for the internal Baud Rate Generator. IX can also be used as an external clock input in which case OX should be left open.
$\overline{RD}$	1	1	I	Read: The $\overline{RD}$ input causes the CA82C52 to output data to the data bus (D_0 - D_7). The data output depends upon the state of the address inputs (A_0, A_1). $\overline{CSO}$ enables the RD input.
RST	23	23	I	Reset: The RST input forces the CA82C52 into an Idle mode in which serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The UART Status Register (USR) is cleared except for the TBRE and TC bits, which are set. The CA82C52 remains in an Idle state until programmed to resume serial data activities. The RST input is a Schmitt trigger input.

Table 2-1: Pin Descriptions Cont'd

Symbol	Pins		Type	Name and Function
	PLCC	PDIP		
$\overline{RTS}$	20	20	O	Request to Send: The $\overline{RTS}$ signal can be set low by writing a logic 1 to the appropriate bit in the MCR. This signal is cleared high by writing a logic 0 to the $\overline{RTS}$ bit in the MCR or whenever a reset RST (high) is applied to the CA82C52.
SDI	25	25	I	Serial Data Input: Serial data input to the CA82C52 receiver circuits. A Mark (1) is high, and a Space (0) is low. Data inputs on SDI are disabled when operating in the loop mode or when RST is true.
SDO	15	15	O	Serial Data Output: Serial data output from the CA82C52 transmitter circuitry. A Mark (1) is a logic one (high) and Space (0) is a logic zero (low). SDO is held in the Mark condition when the transmitter is disabled, when $\overline{CTS}$ is false, RST is true, when the Transmitter Register is empty, or when in the Loop Mode.
TBRE	22	22	O	Transmitter Buffer Register Empty: The TBRE output is set high whenever the Transmitter Buffer Register (TBR) has transferred its data to the Transmitter Register. Application of a reset (RST) to the CA82C52 will also set the TBRE output. TBRE is cleared low whenever data is written to the TBR
V_{DD}	27	27	–	Power: 5V ± 10% DC Supply
V_{SS}	16	16	–	Ground: 0 V
$\overline{WR}$	2	2	I	Write: The $\overline{WR}$ input causes data from the data bus (D_0 - D_7) to be input to the CA82C52. Addressing and chip select action is the same as for read operations

FUNCTIONAL DESCRIPTION

The CA82C52 UART contains a programmable baud rate generator that provides clocking for the transmitter and receiver circuits. The clock output, CO, is a buffered version of either the clock input (IX) to the device or a clock rate that is 16 x the actual baud rate generated.

The transmitter is used for sending serial data out through the SDO pin. The Transmitter Buffer Register accepts 5- to 8-bit wide parallel data from the data bus and transfers it to the Transmitter Register which then shifts the data out serially through the SDO pin. This form of double buffering technique allows continuous data flow transmission.

The receiver accepts serial data via the SDI pin and converts it to parallel form for the system CPU to read. Data is received serially into the Receiver Shift Register from the SDI pin, then sent to the Receiver Buffer Register for access by the CPU. The receiver also detects parity errors, overrun errors, frame errors and break characters.

The Modem Control and Status block provides the means for communicating with the modem or data set. The Modem Control Register is used to select one of four modes of communication; normal mode, loop mode, echo mode and transmit break. The Modem Control Register defines which interrupts will be enabled and will also set the modem control output lines, $\overline{RTS}$ and $\overline{DTR}$. The Modem Status Register keeps track of any changes in the modem control input lines, $\overline{CTS}$ and $\overline{DSR}$, as well as allowing the CPU to read their inputs.

The format of the data character being transmitted (eg: number of data bits, parity control and the number of stop bits) is controlled by the UART Control Register. Changes in the status of the device at any given time is reflected in the UART Status Register.

Operating Modes

Normal Mode: Configures the CA82C52 for normal full or half-duplex communications. Data will not be looped back in any form between the serial data input pin and the serial data output pin (see Figure 2-4a).

Transmit Break: This mode of operation causes the transmitter to transmit break characters only. A break character is composed of all logical zeros for the start, data, parity and stop bits.

Echo Mode: When selected, echo mode causes the CA82C52 to re-transmit data received on the SDI pin out to the SDO pin. In this mode of operation, any data written to the Transmitter Buffer Register will not be sent out on the SDO pin (Figure 2-4b).

Loop Test Mode: This mode internally re-directs data that would normally be transmitted back to the receiver circuitry. The transmitted data will not appear at the SDO pin. Also, data that is received on the SDI pin will be ignored by the device. This mode of operation is useful for performing self test(s) on the device (Figure 2-4c).

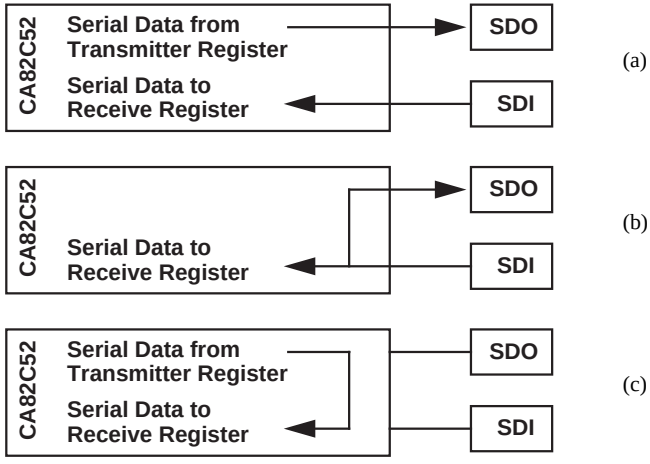


Figure 2-4: Operating Modes

Table 2-2: AC Characteristics (T_A = -40° to +85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits (16 MHz)		Units
			Min	Max	
FC	Clock Frequency	$t_{CHCL} + t_{CLCH}$ must be ≥ 62.5 ns	0	16	MHz
t_{CHCL}	Clock High Time		25		ns
t_{CLCH}	Clock Low Time		25		ns
t_{CTHCTL}	Control Disable to Control Enable		190		ns
t_{CTHSX}	Select Hold From Control Trailing Edge		50		ns
t_{CTLCTH}	Control Pulse Width	Control Consists of $\overline{RD}$ or $\overline{WR}$	150		ns
t_{DVWH}	Data Setup Time		50		ns
t_{FCO}	Clock Output Fall Time	C_L = 50 pf		15	ns
t_{RCO}	Clock Output Rise Time	C_L = 50 pf		15	ns
t_{RHDZ}	Read Disable	2	0	60	ns
t_{RLDV}	Read Low to Data Valid	1		120	ns
T_R/T_F	IX Input Rise/Fall Time (External Clock)	tx ≤ $^1/_6$ FC or 50 ns, whichever is smaller		tx	ns
t_{SVCTL}	Select Setup to Control Leading Edge		30		ns
t_{WHDX}	Data Hold Time		20		ns

Table 2-3: Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0V, V_{IN} = +5 V or V_{SS})

Symbol	Parameter	Test Conditions	Min	Max	Units
$C_{I/O}$	I/O Capacitance	FREQ = 1 MHz Unmeasured pins returned to V_{SS}	-	15	pF
C_{IN}	Input Capacitance		-	10	pF
C_{OUT}	Output Capacitance		-	10	pF

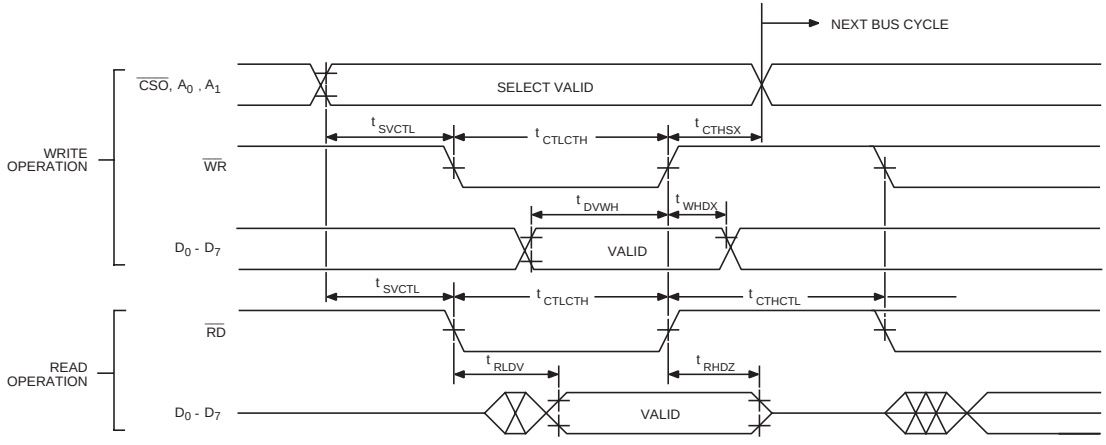
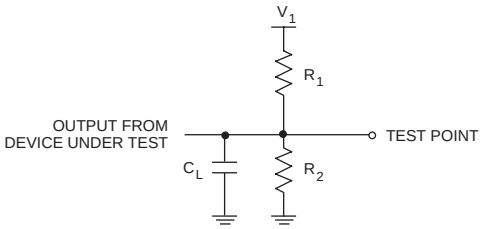
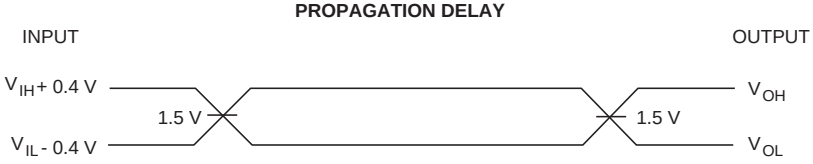


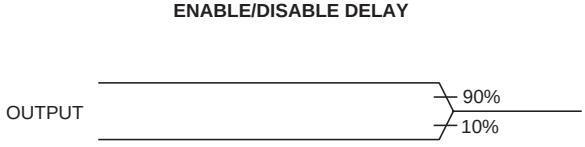
Figure 2-5: Bus Operation Timing Diagram



	TEST CONDITION	V_1	R_1	R_2	C_L
1	Propagation Delay	1.7 V	520 Ω	∞	100 pF
2	Disable Delay	V_{DD}	5 k Ω	5 k Ω	50 pF

Figure 2-6: AC Test Circuits





A.C. Testing: All input signals must switch between V_{IL} - 0.4 V and V_{IH} + 0.4 V. TR and TF must be ≤ 15 ns.

Figure 2-7: AC Testing I/O Waveform

Table 2-4: DC Characteristics (T_A = -40° to +85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits (16 MHz)		Units
			Min	Max	
FC	Clock Frequency	$t_{CHCL} + t_{CLCH}$ must be ≥ 62.5 ns	0	16	MHz
I_{DD}	Operating Power Supply Current (see Note 1)	External Clock F = 2.45576 MHz V_{DD} = 5.5 V, V_{IN} = V_{DD} or V_{SS} Outputs Open	–	3	mA
I_{IL}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS} on input pins	-1.0	+1.0	µA
I_{OL}	I/O Leakage Current	V_{OUT} = V_{DD} or V_{SS} on 3-state pins	-10.0	+10.0	µA
V_{IH}	Input High Voltage	Note 2	2.0	V_{DD} + 0.3	V
V_{IH} (CLK)	Input High Voltage Clock	External Clock	0.7V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	Note 2	-0.3	0.8	V
V_{IL} (CLK)	Input Low Voltage Clock	External Clock	-0.3	0.3V_{DD}	V
V_{IHS}	Schmitt Trigger Input High Voltage	Note 3	2.1	V_{DD} + 0.3	V
V_{ILS}	Schmitt Trigger Input Low Voltage	Note 3	-0.3	0.7	V
V_{HY}	Schmitt Trigger Hysteresis	Note 3	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.5 mA	3.0	–	V
		I_{OH} = -100 µA	V_{DD} - 0.4		
V_{OL}	Output Low Voltage	I_{OL} = +2.5 mA	–	0.4	V

Note 1: I_{DD} is typically ≤ 1 ma/MHz
Note 2: Applies to data bus pins (D_7 - D_0)
Note 3: Applies to pins $\overline{\text{RD}}$, $\overline{\text{WR}}$, A_0, A_1, $\overline{\text{CTS}}$, $\overline{\text{DSR}}$, *RST, SDI and* $\overline{\text{CSO}}$

Table 2-5: Recommended Operating Conditions

DC Supply Voltage		+4.5 V to +5.5 V
Operating Temperature Range	Commercial	0°C to +70°C
	Industrial	-40°C to +85°C

Table 2-6: Absolute Maximum Ratings

DC Supply Voltage	-.03 to +7.0 V
Input, Output or I/O Voltage Applied	V_{SS} - 0.3 V to V_{DD} + 0.3 V
Storage Temperature Range	-55°C to +150°C
Maximum Package Power Dissipation	1 W
Input Pin Current (@ 25°C)	-10.0 mA to +10.0 mA
Lead Temperature (soldering: 10 sec.)	300°C

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PROGRAMMING INSTRUCTIONS

Reset

During and after power-up, the CA82C52 Reset input (RST) should be held high for at least two IX clock cycles in order to initialize and drive the CA82C52 circuits to an idle mode until proper programming can be done. A high on RST causes the following events to occur:

- Resets the internal Baud Rate Generator (BRG) circuits, clock counters and bit counters. The Baud Rate Select Register (BRSR) is not affected.
- Clears the UART Status Register (USR) except for Transmission Complete (TC) and Transmit Buffer Register Empty (TBRE) which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. Note that the UART Control Register (UCR) is not affected.

Following removal of the reset condition (RST = low), the CA82C52 remains in the idle mode until programmed to its desired system configuration.

Control Words

The complete functional definition of the CA82C52 is programmed by the systems software. A set of control words (UCR, BRSR and MCR) must be sent out by the CPU to initialize the CA82C52 to support the desired communication format. These control words will program the character length, number of stop bits, even/odd/no parity, baud rate etc. Once programmed, the CA82C52 is ready to perform its communication functions.

The control registers can be written to in any order. However, the MCR should be written to last because it controls the interrupt enables, modem control outputs and the receiver enable bit. Once the CA82C52 is programmed and operational, these registers can be updated any time the CA82C52 is not immediately transmitting or receiving data.

Table 2-7 shows the control signals required to access the CA82C52 internal registers.

Table 2-7: Control Signals

$\overline{CSO}$	A1	A0	$\overline{WR}$	$\overline{RD}$	Operation
0	0	0	0	1	Data Bus → Transmitter Buffer Register (TBR)
0	0	0	1	0	Receiver Buffer Register (RBR) → Data Bus
0	0	1	0	1	Data Bus → UART Control Register (UCR)
0	0	1	1	0	UART Status Register → Data Bus
0	1	0	0	1	Data Bus → Modem Control Register (MCR)
0	1	0	1	0	Modem Control Register (MCR) → Data Bus
0	1	1	0	1	Data Bus → Bit Rate Select Register (BRSR)
0	1	1	1	0	Modem Status Register (MSR) → Data Bus

UART Control Register (UCR)

The UCR is a write only register which configures the UART transmitter and receiver circuits. Data bits D_7 and D_6 are not used but should always be set to a logic zero (0) in order to ensure software compatibility with future product upgrades. During the Echo Mode, the transmitter always repeats the received word and parity, even when the UCR is programmed with different or no parity.

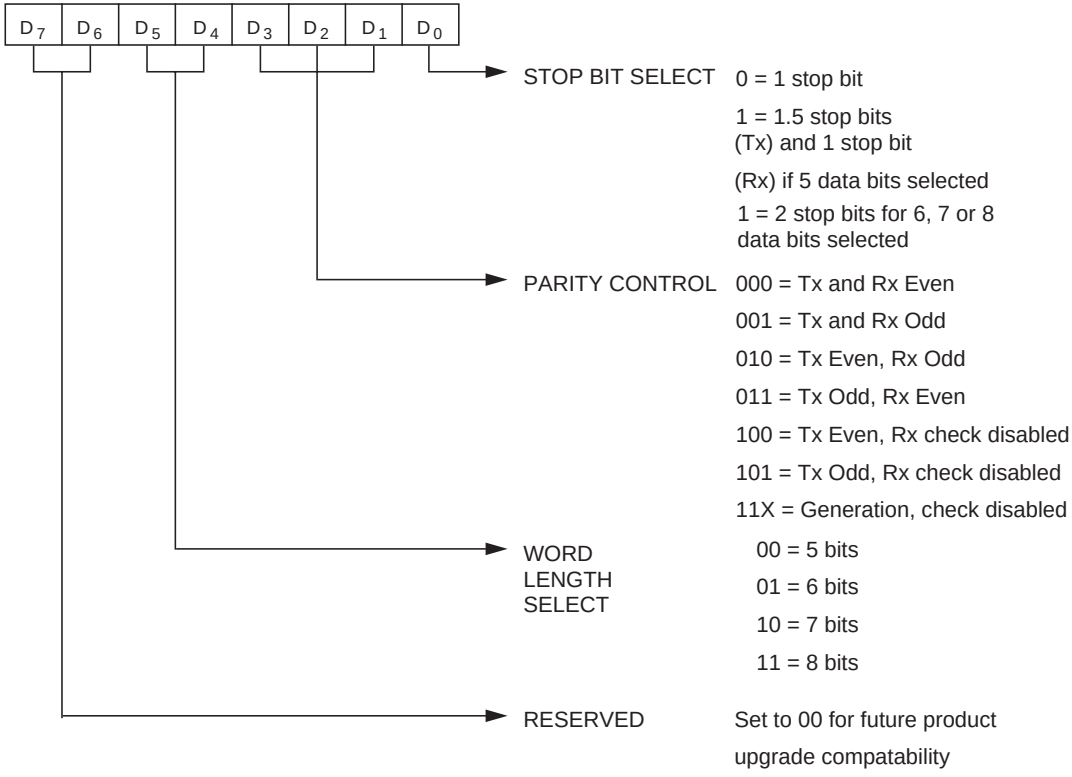


Figure 2-8: UCR

Baud Rate Select Register (BRSR)

The CA82C52 is designed to operate with a single crystal or external clock driving the IX input pin. The Baud Rate Select Register is used to select the divide ratio (one of 72) for the internal Baud Rate Generator circuitry. The internal circuitry is separated into two separate counters, a Prescaler and a Divisor Select. The Prescaler can be set to any one of four division rates. Those rates are: ÷ 1, ÷ 3, ÷ 4 or ÷ 5.

The prescaler design has been optimized to provide standard baud rates using any one of three popular crystals. Using one of these system clock frequencies: 1.8432 MHz, 2.4576 MHz or 3.072 MHz and Prescaler divide ratios of ÷ 3, ÷ 4, or ÷ 5 respectively, the Prescaler output will provide a constant 614.4 kHz. When this frequency is further divided by the Divisor Select counter, any of the standard baud rates from 50 Baud to 38.4 k Baud can be selected (Table 2-8). Non-standard baud rates up to 1 M baud can be selected using different input frequencies (crystal or external frequency input up to 16 MHz) and/or different Prescaler and Divisor Select ratios.

Regardless of the baud rate, the baud rate generator provides a clock which is 16 times the desired baud rate. For example, in order to operate at a 1 M baud data rate, a 16 MHz crystal, a Prescale rate of ÷ 1, and a Divisor Select rate of external is used. This provides a 16 MHz clock as the output of the Baud Rate Generator to the Transmitter and Receiver circuits.

The CO select bit in the BRSR determines if the buffered version of the external frequency input (IX input) or the Baud Rate Generator output (16x baud rate clock) is output on the CO output. The Baud Rate Generator output is always a 50% nominal duty cycle except when external is selected and the Prescaler is set to ÷ 3 or ÷ 5.

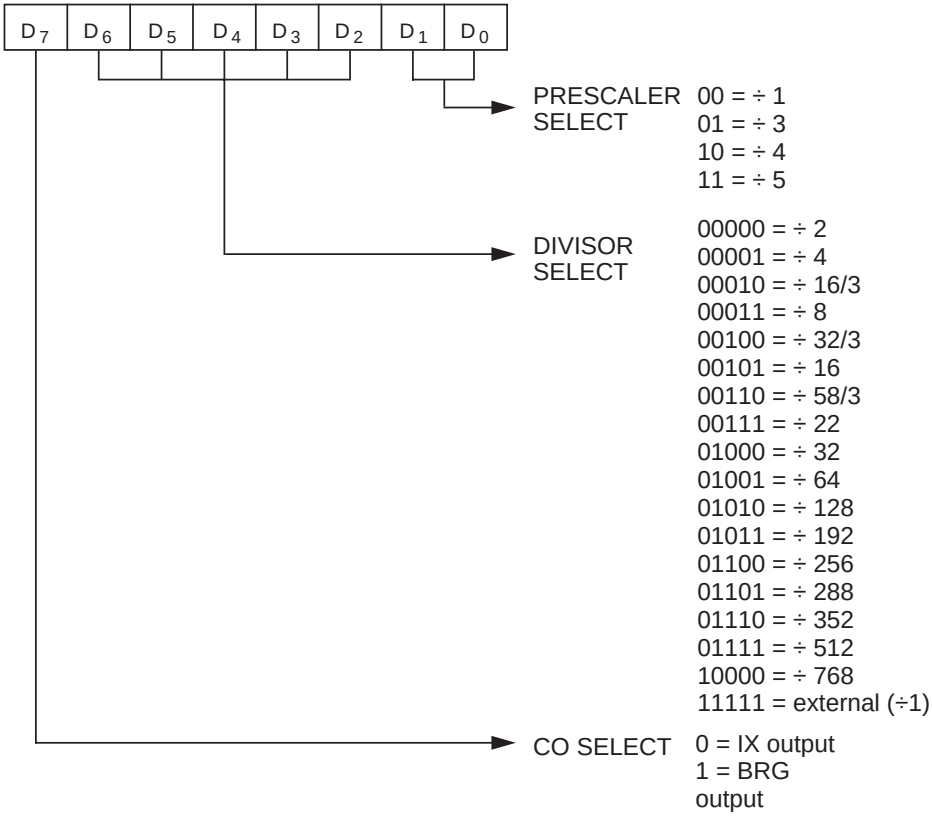


Figure 2-9: BRSR

Modem Control Register

The MCR is a general purpose control register which can be written to and read from. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their associated bits in this register. Note that a logic one asserts a true logic level (low) at these output pins. The Interrupt Enable (INTEN) bit is the overall control for the INTR output pin. When INTEN is false, INTR is held false (low).

Table 2-8: Baud Rate Divisors

Baud Rate	Divisor
38.4 K	External
19.2 K	2
9600	4
7200	16/3
4800	8
3600	32/3
2400	16
2400*	58/3
1800	22
1200	32
600	64
300	128
200	192
150	256
134.5*	288
110*	352
75	512
50	768

**All baud rates are exact except for those in Table 2-9.*

The baud rates listed in Table 2-8 are based upon the following input frequency/Prescale divisor combinations:

- 1.8432 MHz and Prescale = ÷ 3
- 2.4576 MHz and Prescale = ÷ 4
- 3.072 MHz and Prescale = ÷ 5

Table 2-9: Baud Rate% Error

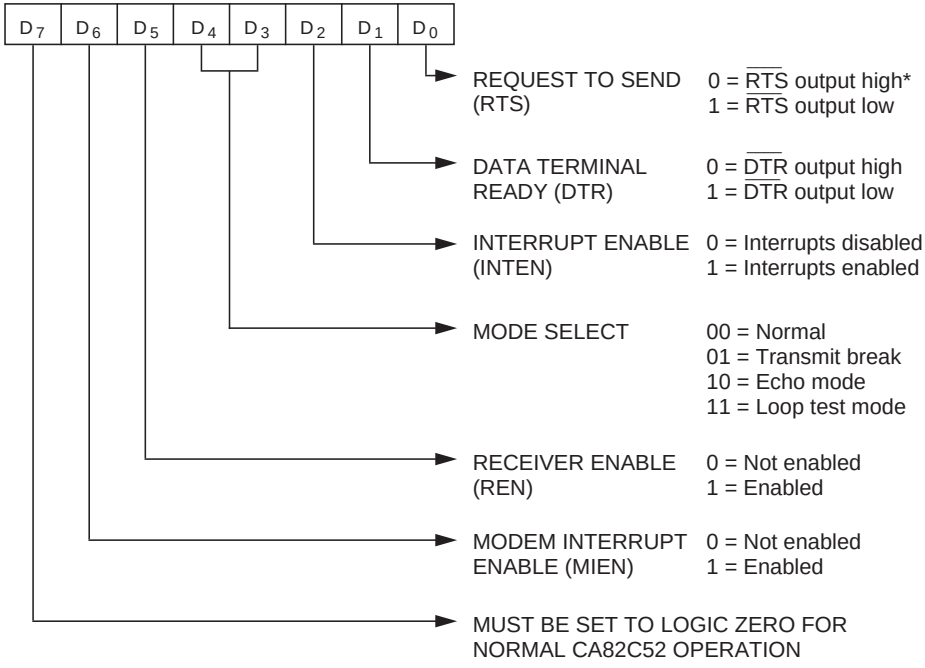
Baud Rate	Actual	Percent Error
2000	1986.2	0.69%
134.5	133.33	0.87%
110	109.71	0.26%

The Operating Mode bits configure the CA82C52 into one of four possible modes. "Normal" configures the CA82C52 for normal full or half duplex communications. "Transmit Break" enables the transmitter to only transmit break characters (Start, Data and Stop bits are all logic zero). The Echo Mode causes any data that is received on the SDI input pin to be re-transmitted on the SDO output pin. Note that this output is a buffered version of the data seen on the SDI input and is not a re-synchronized output. Also note that normal UART transmission via the Transmitter Register is disabled when operating in the Echo mode (Figure 2-11). The Loop Test Mode internally routes transmitted data to the receiver circuitry for the purpose of self test. The transmit data is disabled from the SDO output pin.

The Receiver Enable (REN) bit gates off the input to the receiver circuitry when in the false state.

Modem Interrupt Enable will permit any change in modem status line inputs ($\overline{CTS}$, $\overline{DSR}$) to cause an interrupt when this bit is enabled. Bit D_7 must always be written to with a logic zero to ensure correct CA82C52 operation

.



* See Modem Status Register description for a description of register flag images with respect to output pins.

Figure 2-10: MCR

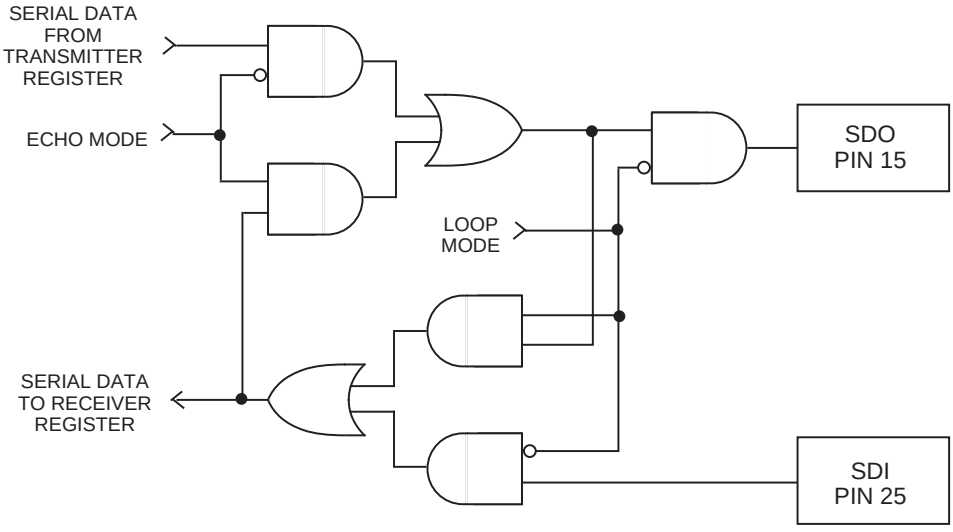


Figure 2-11: LOOP and ECHO Mode Functionality

UART Status Register (USR)

The USR provides a single register that the controlling system can examine to determine if errors have occurred or if other status changes in the CA82C52 require attention. For this reason, the USR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the CA82C52.

Three error flags OE, FE and PE report the status of any error conditions detected in the receiver circuitry. These error flags are updated with every character received during reception of the stop bits. The Overrun Error (OE) indicates that a character in the Receiver Register has been received and cannot be transferred to the Receiver Buffer Register (RBR) because the RBR was not read by the CPU. Framing Error (FE) indicates that the last character received contained improper stop bits. This could be caused by the absence of the required stop bit(s) or by a stop bit(s) that was too short to be properly detected. Parity Error (PE) indicates that the last character received contained a parity error based on the programmed parity of the receiver and the calculated parity of the received character data and parity bits.

The Received Break (RBRK) status bit indicates that the last character received was a break character. A break character would be considered to be an invalid data character in that the entire character including parity and stop bits are a logic zero.

The Modem Status bit is set whenever a transition is detected on any of the modem input lines ($\overline{CTS}$ or $\overline{DSR}$). A subsequent read of the Modem Status Register will show the state of these two signals. Assertion of this bit will cause an interrupt (INTR) to be generated if the MIEN and INTEN bits in the MCR register are enabled.

The Transmission Complete (TC) bit indicates that both the TBR and Transmitter Registers are empty and the CA82C52 has completed transmission of the last character it was commanded to transmit. The assertion of this bit will cause an interrupt (INTR) if the INTEN bit in the MCR register is true.

The Transmitter Buffer Register Empty (TBRE) bit indicates that the TBR register is empty and ready to receive another character.

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Assertion of the TBRE or DR bits do not affect the INTR logic and associated INTR output pin since the CA82C52 has been designed to provide separate requests via the DR and TBRE output pins. If a single interrupt for any status change in the CA82C52 is desired this can be accomplished by 'ORing' DR, TBRE and INTR together.

Reading the USR clears all of the status bits in the USR register but does not affect associated output pins.

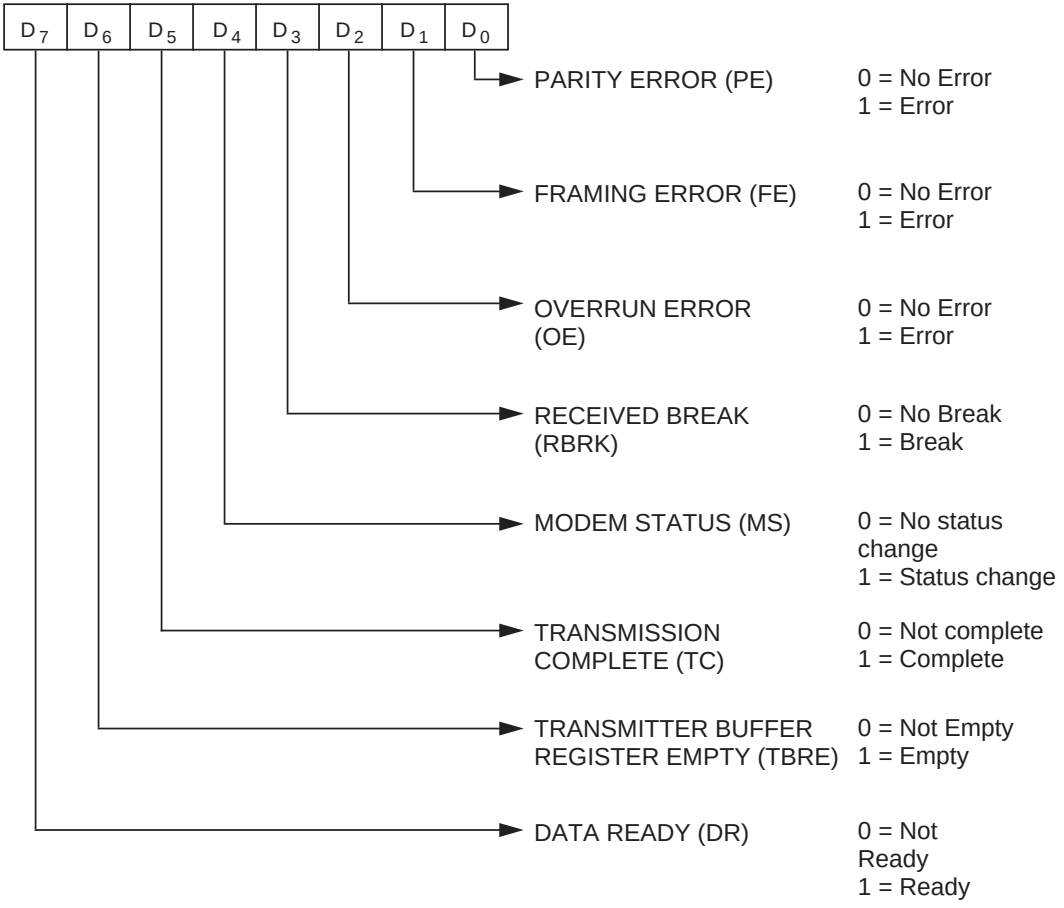


Figure 2-12: USR

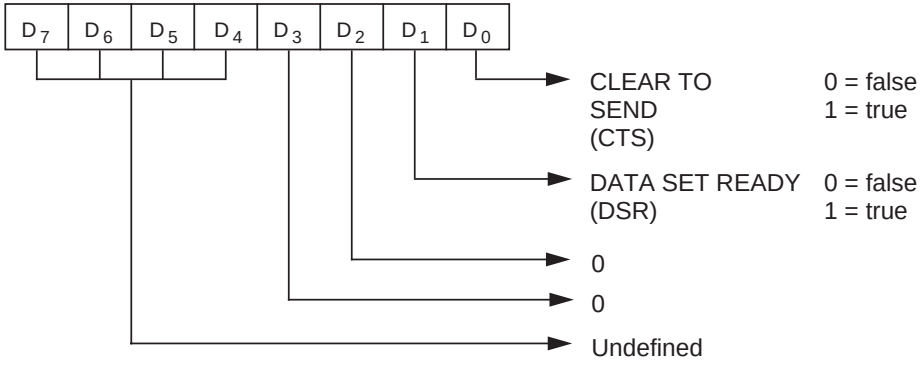
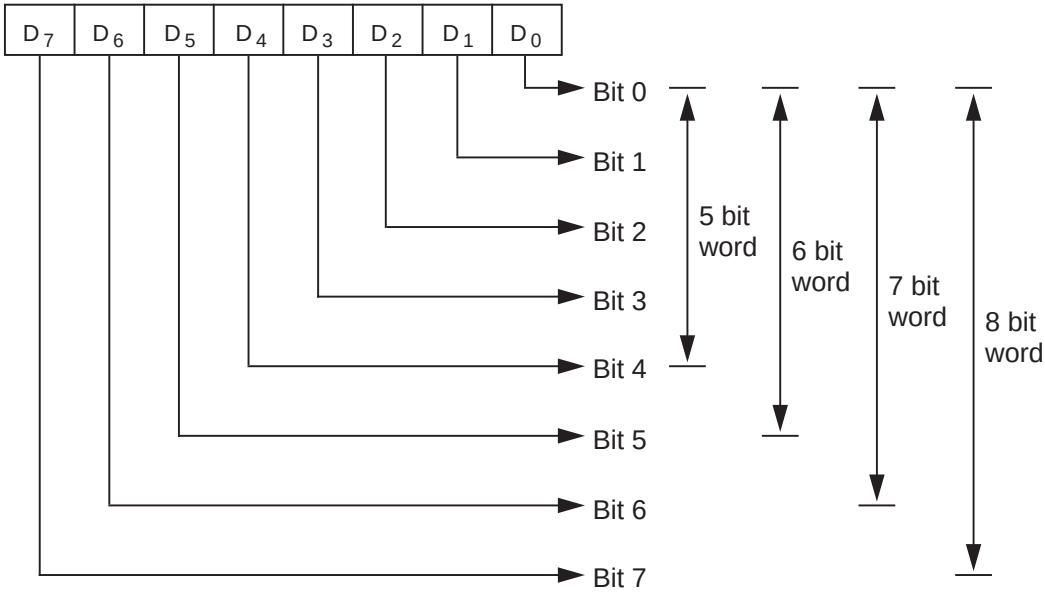


Figure 2-13: MSR



Note:The LSB, Bit 0 is the first serial data bit received.

Figure 2-14: RBR

Modem Status Register (MSR)

The MSR allows the CPU to read the modem signal inputs by accessing the data bus interface of the CA82C52. Like all of the register images of external pins in the CA82C52, true logic levels are represented by a high (1) signal level. By following this consistent definition, the system software need not be concerned with whether external signals are high or low true. In particular, the modem signal inputs are low true, thus a 0 (true assertion) at a modem input pin is represented by a 1 (true) in the MSR.

Any change of state in any modem input signals will set the Modem Status (MS) bit in the USR register. When this happens, an interrupt (INTR) will be generated if the MIEN and INTEN bits of the MCR are enabled.

The Data Set Ready ($\overline{DSR}$) input is a status indicator from the modem to the CA82C52 which indicates that the modem is ready to provide received data to the CA82C52 receiver circuitry.

Clear to Send ($\overline{CTS}$) is both a status and control signal from the modem that tells the CA82C52 that the modem is ready to receive transmit data from the CA82C52 transmitter output (SDO). A high (false) level on this input will inhibit the CA82C52 from beginning transmission and if asserted in the middle of a transmission will only permit the CA82C52 to finish transmission of the current character.

Receiver Buffer Register (RBR)

The receiver circuitry in the CA82C52 is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the Least Significant Bit (LSB = D_0). Bit D_0 of a data word is always the first data bit received. The unused bits in a less than 8 bit word, at the parallel interface, are set to a logic zero (0) by the CA82C52.

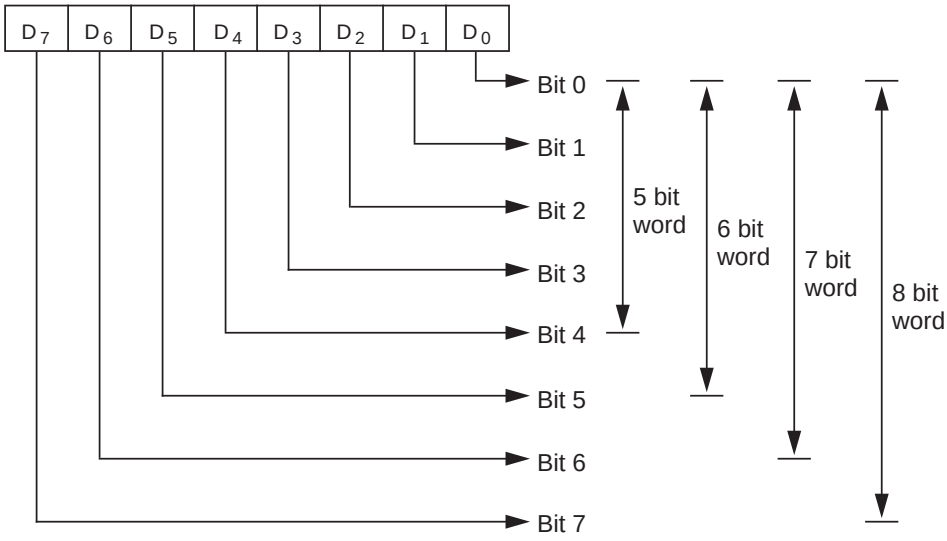
Received data at the SDI input pin is shifted into the Receiver Register by an internal 1 x clock which has been synchronized to the incoming data based on the position of the start bit. When a complete character has been shifted into the Receiver Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. Both the DR output pin and DR flag in the USR register are set. This double buffering of the received data permits continuous reception of data without losing any of the received data.

While the Receiver Register is shifting a new character into the CA82C52, the Receiver Buffer Register is holding a previously received character for the system CPU to read. Failure to read the data in the RBR before complete reception of the next character can result in the loss of the data in the Receiver Register. The OE flag in the USR register indicates the overrun condition.

Transmitter Buffer Register (TBR)

The Transmitter Buffer Register (TBR) accepts parallel data from the data bus (D_0-D_7) and holds it until the Transmitter Register is empty and ready to accept a new character for transmission. The transmitter always has the same word length and number of stop bits as the receiver. For words of less than 8 bits the unused bits at the microprocessor data bus are ignored by the transmitter.

Bit 0, which corresponds to D_0 at the data bus, is always the first serial data bit transmitted. Provision is made for the transmitter parity to be the same or different from the receiver. The TBRE output pin and flag (USR register) reflect the status of the TBR. The TC flag (USR register) indicates when both the TBR and TR are empty.



Note:The LSB, Bit 0 is the first serial data bit transmitted.

Figure 2-15: TBR

INTERRUPT STRUCTURE

The CA82C52 has provisions for software masking of interrupts generated for the INTR output pin. Two control bits in the MCR register, MIEN and INTEN, control modem status interrupts and overall CA82C52 interrupts respectively. Figure 2-16 illustrates the logical control function provided by these signals.

The modem status inputs ($\overline{DSR}$ and $\overline{CTS}$) will trigger the edge detection circuitry with any change of status. Reading the MSR register will clear the detect circuit but has no effect on the status bits themselves. These status bits always reflect the state of the input pins regardless of the mask control signals. Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

The edge detection circuits for the USR register signals will trigger only for a positive edge (true assertion) of these status bits. Reading the USR register not only clears the edge detect circuit but also clears (sets to 0) all of the status bits. The output pins associated with these status bits are not affected by reading the USR register.

A hardware reset of the CA82C52 sets the TC status bit in the USR. When interrupts are subsequently enabled an interrupt can occur due to the fact that the positive edge detection circuitry in the interrupt logic has detected the setting of the TC bit. If this interrupt is not desired, the USR should be read prior to enabling interrupts. This action resets the positive edge detection circuitry in the interrupt control logic (Figure 2-16).

Note: For USR and MSR, the setting of status bits is inhibited during status register READ operations. If a status condition is generated during a READ operation, the status bit is not set until the trailing edge of the RD pulse.

If the bit was already set at the time of the READ operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the RD pulse instead of being set again.

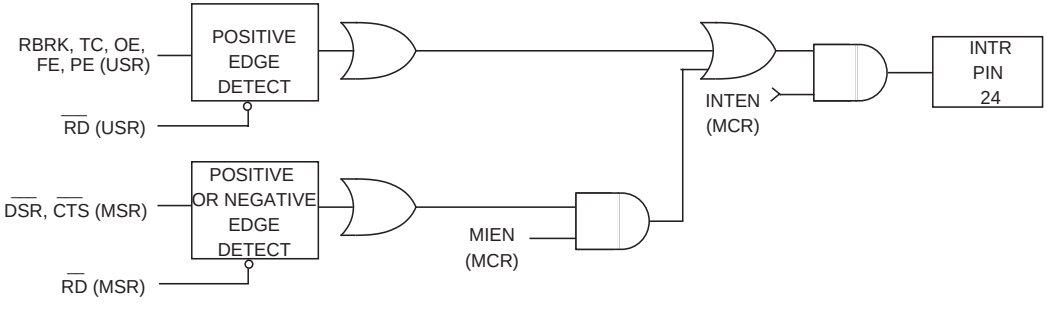


Figure 2-16: Interrupt Structure

SOFTWARE RESET

A software reset of the CA82C52 is a useful method for returning to a completely known state without exercising a complete system reset. Such a reset would consist of writing to the UCR, BRSR and MCR registers. The USR an RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

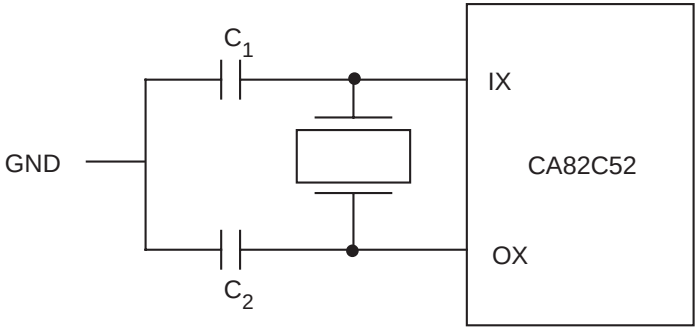
CRYSTAL OPERATION

The CA82C52 crystal oscillator circuitry is designed to operate with a fundamental mode, parallel resonant crystal. To summarize, Table 2-10 and Figure 2-17 show the required crystal parameters and crystal circuit configuration respectively.

When using an external clock source, the IX input is driven and the OX output is left open. Power consumption when using an external clock is typically 50% of that required when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

Table 2-10: Crystal Specifications

Parameter	**Typical Crystal Specs**
Frequency	1.0 to 16 MHz
Type of Operation	Parallel resonant, Fundamental mode
Load Capacitance (CL)	20 or 32 pF (typ.)
R series (Max.)	100 W (f = 16 MHz, CL = 32 pF) 200 W (f = 16 MHz, CL = 20 pF)



* C1 = C2 = 20 pf for CL = 20 pf
* C1 = C2 = 47 pf for CL = 32 pf

Figure 2-17: Typical Crystal Circuit

APPLICATIONS

The following example (Figure 2-18) shows the interface for an CA82C52 in an 80C86 system.

Use of the Interrupt Controller (CA82C59A) is optional. It is only necessary if an interrupt driven system is desired.

By using the CA82C84A clock generator, the system can be built with a single crystal providing both the processor clock and the clock for the CA82C52. The CA82C52 has special divider circuitry which is designed to supply industry standard baud rates with a 2.4576 MHz input frequency. Using a 15 MHz crystal as shown, results in less than a 2% frequency error which is adequate for many applications. For more precise baud rate requirements, a 14.7456 MHz crystal will drive the 80C86 at 4.9 MHz and provide the 82C52 with the standard baud rate input frequency of 2.4576 MHz. If baud rates above 156 k baud are desired, the OSC output can be used instead of the PCLK (÷6) output for asynchronous baud rates up to 1 M baud.

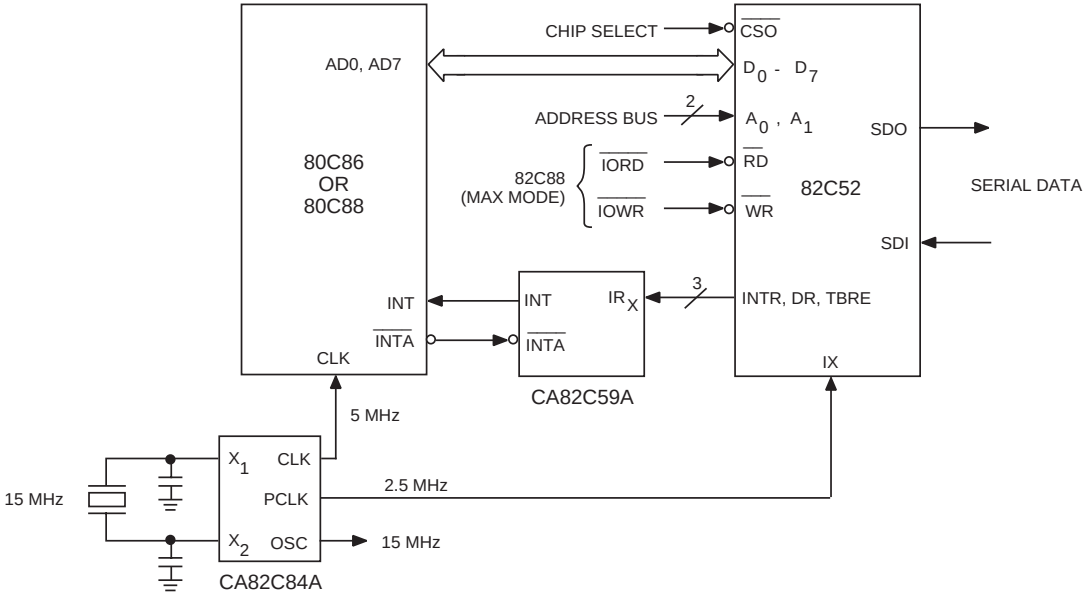


Figure 2-18: 80C86/CA82C52 Interface

CA82C54

PROGRAMMABLE INTERVAL TIMER

- **A high performance device featuring pin and functional compatibility with the industry standard 8254**
- **Supports 8086/88 and 80186/188 micro-processors**
- **High Speed: zero wait state 10 MHz and 8 MHz versions available**
- **Low power CMOS implementation**
- **TTL input/output compatibility**
- **Compatible with 8080/85, 8086/88, 80286/386 and 68000 μP families**
- **Fully static operation**
- **Three independent 16 bit counters**
- **Six programmable counter modes**
- **Status read-back command**
- **Binary or BCD counting**

The CA82C54 is a counter/timer device that includes complete pin and functional compatibility with the industry standard 8254. Designed for fast 10 MHz operation, it has three independently programmable 16 bit counters and six programmable counter modes. Counting can be performed in both binary and BCD formats.

The CA82C54 offers a very flexible, hardware solution to the generation of accurate time delays in microprocessor systems. A general purpose, multi-timing element, it can be used to implement event counters, elapsed time indicators, waveform generators plus a host of other functions.

The low power consumption of the CA82C54 makes it ideally suited to portable systems or those with low power standby modes.

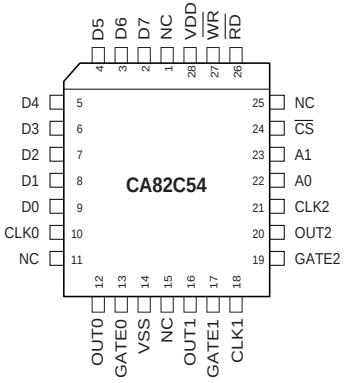


Figure 2-1: PLCC Pin Configurations

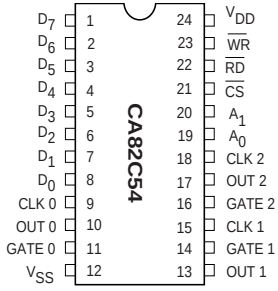


Figure 2-2: PDIP Pin Configurations

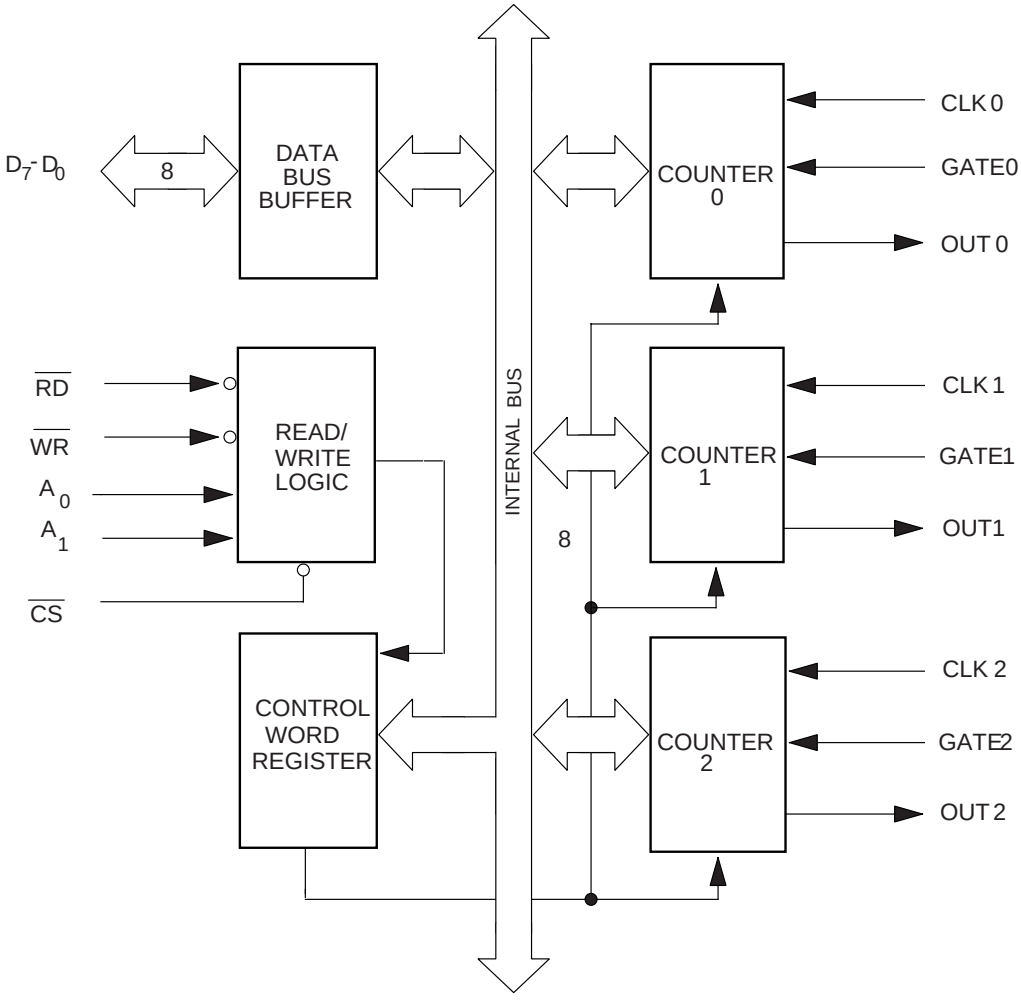


Figure 2-3: CA82C54 Block Diagram

Table 2-1: Pin Descriptions

Symbol	Pins		Type	Name and Function
	PLCC	PDIP		
A_0, A_1	22, 23	19, 20	I	**Address**: These two address pins are used to select the Control Word Register (for read or write operations), or one of the three Counters. They are normally connected to the system address bus. A_1 A_0 **Selects:** 0 0 Counter 0 0 1 Counter 1 1 0 Counter 2 1 1 Control Word Register
CLK 0	10	9	I	**Clock 0**: Clock input of Counter 0.
CLK 1	18	15	I	**Clock 1**: Clock input of Counter 1.
CLK 2	21	18	I	**Clock 2**: Clock input of Counter 2.
$\overline{CS}$	24	21	I	**Chip Select**: Active LOW control signal to enable the CA82C54 to respond to $\overline{RD}$ and $\overline{WR}$ signals. If $\overline{CS}$ is not LOW, $\overline{RD}$ and $\overline{WR}$ are ignored.
D_7 - D_0	2 - 9	1 - 8	I/O	**Data**: Bi-directional 3-state data bus lines, connected to system data bus.
GATE 0	13	11	I	**Gate 0**: Gate input of Counter 0.
GATE 1	17	14	I	**Gate 1**: Gate input of Counter 1.
GATE 2	19	16	I	**Gate 2**: Gate input of Counter 2.
OUT 0	12	10	O	**Output 0**: Output of Counter 0.
OUT 1	16	13	O	**Output 1**: Output of Counter 1.
OUT 2	20	17	O	**Output 2**: Output of Counter 2.
$\overline{RD}$	26	22	I	**Read Control**: Active LOW control signal used to enable the CA82C54 for read operations by the CPU.
VDD	28	24	-	**Power**: 5 v ± 10% DC Supply
VSS	14	12	-	**Ground**: 0 v
$\overline{WR}$	27	23	I	**Write Control**: Active LOW control signal used to enable the CA82C54 to be written to by the CPU.

FUNCTIONAL DESCRIPTION

The CA82C54 is a versatile programmable interval timer/counter designed for use in high speed 8, 16 and 32-bit microprocessor systems. It provides a means of generating accurate time delays in hardware that is fully software configurable. It can be treated as an array of I/O ports, with minimal software overhead.

The internal structure of the CA82C54 is illustrated in the block diagram of Figure 2-3. Major functional blocks include a data bus buffer, read/write logic, control word register, and three programmable counters.

Data Bus Buffer Block

The 8-bit, 3-state data bus buffer provides controllable, bi-directional interface between the CA82C54 and the microprocessor system bus.

Read/Write Logic Block

The read/write logic block generates internal control signals for the different functional blocks using address and control information obtained from the system. The active LOW signals; $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ are used to select the CA82C54 for operation, read a counter, and write to a counter (or the control word register) respectively. $\overline{CS}$ must be LOW for $\overline{RD}$ or $\overline{WR}$ to be recognized. Note that $\overline{RD}$ and $\overline{WR}$ must NOT be active at the same time.

The inputs A_0 and A_1 are used to select the control word register, or one of the three counters that is to be written to or read from (see Table 2-1). A_0 and A_1 connect directly to the corresponding signals of the microprocessor address bus, while $\overline{CS}$ is derived from the address bus using either a linear select method, or an address decoder device.

Control Word Register

The control word register is a write only register that is selected by the read/write logic block when A_0 and $A_1 = 1$. When $\overline{CS}$ and $\overline{WR}$ are LOW, data is written into the CA82C54 control word register from the CPU via the data bus buffer. Control word data is interpreted as a number of different commands which are used to program the various device functions. For example, status information is available with the Read-Back Command. These are discussed further in the section on programming.

Counter Blocks

The CA82C54 contains three identical, independent counter blocks. Each counter provides the same functions, but can be programmed to operate in different modes relative to each other. A typical CA82C54 counter is illustrated in Figure 2-4, and contains the following functional elements: control logic, counter, output latches, count registers and status register.

The Control Logic provides the interface between the counter proper, the program instructions contained in the control word register and the external signals CLK n, GATE n and OUT n. It also keeps the status register information current, controls the access of OL and CR to the internal data bus, and the loading of CE from the CR registers.

The Counter proper (shown in the Figure 2-4 as CE, for counting element) is a 16-bit presettable synchronous down counter.

The Output Latches (shown as OL_M and OL_L) provide a mechanism whereby the CPU can read the current contents of the CE. These two 8-bit latches (M for most significant byte and L for least significant byte) together form a 16-bit latch capable of holding the complete contents of the CE. Note that this arrangement is also convenient for communicating 16-bit values over the 8-bit internal data bus.

During normal operation, the contents of OL track with the contents of CE. When a Counter Latch Command is issued by the CPU to a particular counter, its OL latches the current value of CE so that it can be read by the CPU (the CE cannot be read directly). OL then returns to tracking with CE. Note that only one latch (OL_M followed by OL_L) at a time is enabled by the counter's control logic.

The Count Registers (shown as CR_M and CR_L) behave as input latches to the CE, and provide a mechanism whereby the initial count value can be downloaded from the CPU to the CE. Similar in operation to OL, CR is controlled by the counter control logic. When a two byte initial count is to be downloaded, it is transferred one byte at a time across the internal CA82C54 data bus to the appropriate register (CR_M if the most significant byte, CR_L otherwise). CE is loaded by transferring both bytes simultaneously from CR. Note that CR is the interface between CE and the data bus, since CE cannot be accessed directly.

Both CR_M and CR_L are cleared automatically when the counter is programmed and a new initial count is to be written. Thus, regardless of the counter's previous programming, both CR bytes will be initialized to a known zero state. This is important in the case where one byte counts are programmed (either most significant or least significant byte), so that the unused byte is always zero, and won't corrupt the initial count value loaded into CE.

The Status Register and Latch is used to hold the current contents of the control word register and the status of the output and null count flag (see section on Programming). The contents of the status register must be latched to become available to the data bus, where they can be read by the CPU.

Note that the Control Word Register is also shown in the Counter block diagram. While not a part of the counter proper, its contents determine the functional operation of the counter, including mode selections programmed.

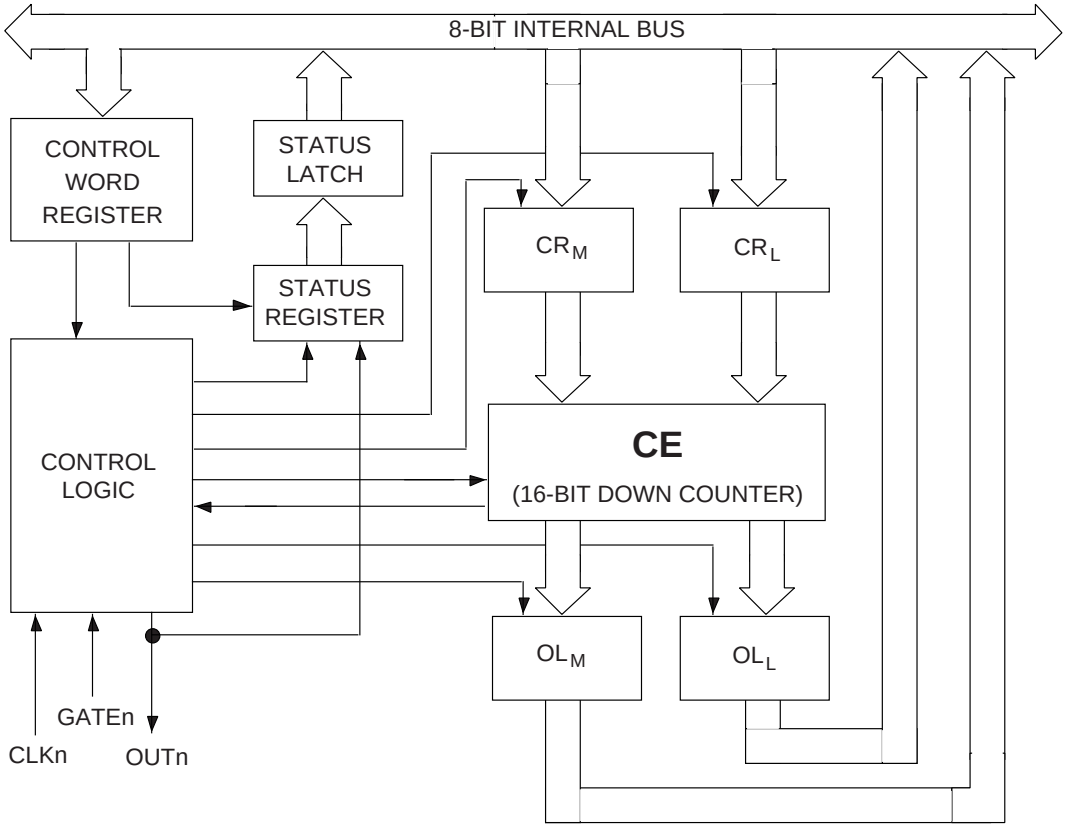


Figure 2-4: Block Diagram of a Counter

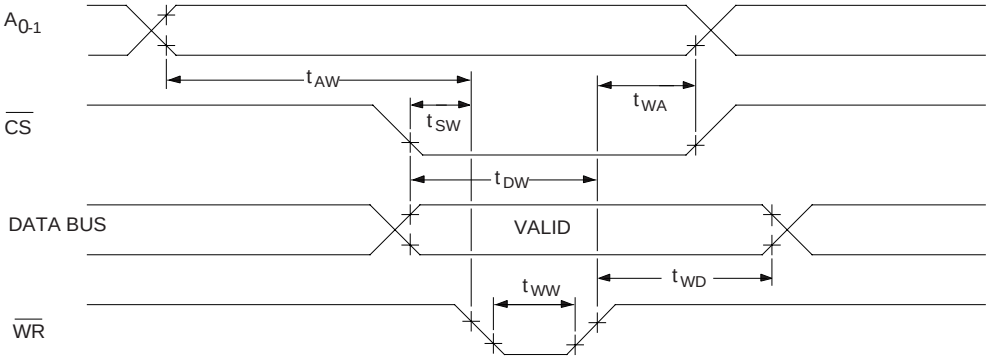
Table 2-2: AC Characteristics (T_A = -40° to +85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V) Bus Parameters[1]

Symbol	Parameter	Test Condition	Limits (8 MHz)		Limits (10 MHz)		Units
			Min	Max	Min	Max	
t_{AD}	Data delay from address		-	220	-	185	ns
t_{AR}	Address stable before $\overline{RD}$ ↓		45	-	30	-	ns
t_{AW}	Address stable before $\overline{WR}$ ↓		0	-	0	-	ns
t_{CL}	CLK setup for count latch		-40	45	-40	40	ns
t_{CLK}	Clock period		125	DC	100	DC	ns
t_{DF}	$\overline{RD}$ ↑ to data floating		5	90	5	65	ns
t_{DW}	Data setup time before $\overline{WR}$ ↑		120	-	95	-	ns
t_F	Clock fall time		-	25	-	25	ns
t_{GH}	Gate hold time after CLK ↑	Note 2	50	-	50	-	ns
t_{GL}	Gate width low		50	-	50	-	ns
t_{GS}	Gate setup time to CLK ↑		50	-	40	-	ns
t_{GW}	Gate width high		50	-	50	-	ns
t_{OD}	Output delay from CLK ↓		-	150	-	100	ns
t_{ODG}	Output delay from Gate ↓		-	120	-	100	ns
t_{PWH}	High pulse width	Note 3	60	-	30	-	ns
t_{PWL}	Low pulse width	Note 3	60	-	50	-	ns
t_R	Clock rise time		-	25	-	25	ns
t_{RA}	Address hold time after $\overline{RD}$ ↑		0	-	0	-	ns
t_{RD}	Data delay from $\overline{RD}$ ↓		-	120	-	85	ns
t_{RR}	$\overline{RD}$ pulse width		150	-	95	-	ns
t_{RV}	Command recovery time		200	-	165	-	ns
t_{SR}	CS stable before $\overline{RD}$ ↓		0	-	0	-	ns
t_{SW}	CS stable before $\overline{WR}$ ↓		0	-	0	-	ns
t_{WA}	Address hold time $\overline{WR}$ ↑		0	-	0	-	ns
t_{WC}	CLK delay for loading		0	55	0	55	ns
t_{WD}	Data hold time after $\overline{WR}$ ↑		0	-	0	-	ns
t_{WG}	Gate delay for sampling		-5	50	-5	40	ns
t_{WO}	OUT delay from Mode Write		-	260	-	240	ns
t_{WW}	$\overline{WR}$ pulse width		150	-	95	-	ns

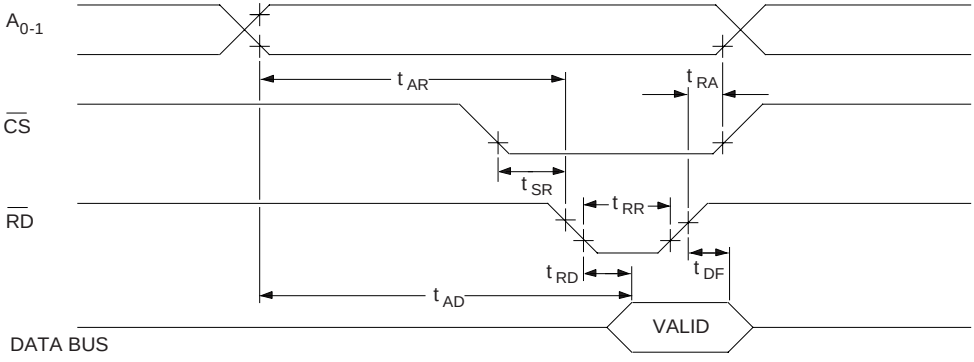
Notes: 1. AC timings measured at V_{OH} = 2.0 V, V_{OL} = 0.8 V
2. In Modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 120 ns of the rising clock edge may not be detected, (70 ns for CA82C54-10).
3. Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.

Figure 2-5: Timing Diagrams

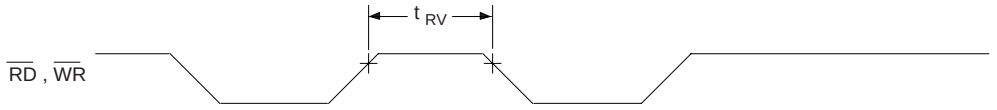
a) Write Timing



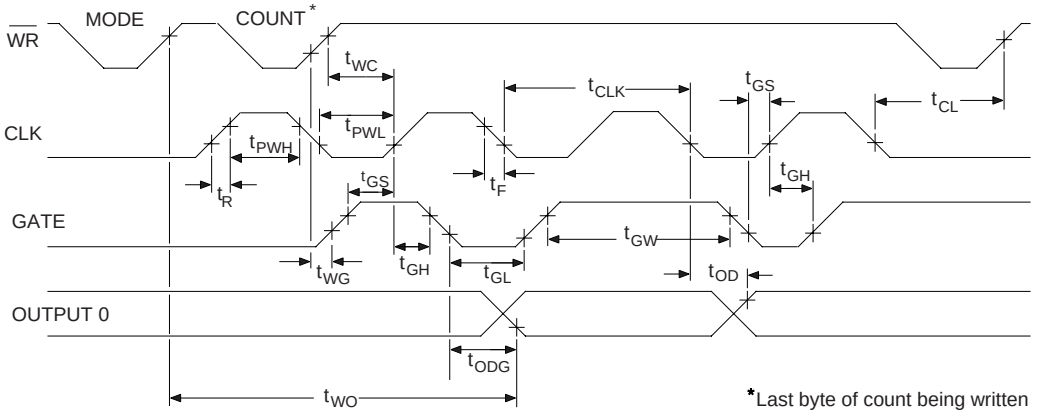
b) Read Timing

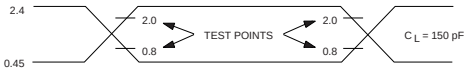


c) Recovery Timing



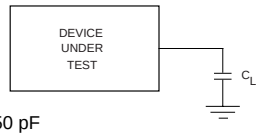
d) Clock and Gate Timing





All input signals must switch between 0.45V and 2.4V.
All timing measurements are made at 0.8V and 2.0V

Figure 2-6: AC Testing I/O Waveform



C_L = 150 pF
C_L includes jig capacitance

Figure 2-7: AC Testing Loading Circuit

Table 2-3: DC Characteristics (T_A = -40°C to +85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{DD}	V_{DD} Supply Current	CLK Freq = 5 MHz, CA82C54-5 CLK Freq = 8 MHz, CA82C54-8 CLK Freq = 10 MHz, CA82C54-10	-	20	mA
I_{IL}	Input Load Current	V_{IN} = V_{DD} or V_{SS}	-1.0	1.0	µA
I_{OFL}	Output Float Leakage	V_{OUT} = V_{DD} to 0.45V	-10	10	µA
V_{IH}	Input High Voltage		2.0	V_{DD} + 0.3V	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	V_{DD} - 0.4V	-	V
		I_{OH} = -2.5 mA	3.0	-	V
V_{OL}	Output Low Voltage	I_{OL} = 2.5 mA	-	0.4	V

Table 2-4: Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0V, V_{IN} = +5 V or V_{SS})

Symbol	Parameter	Test Conditions	Min	Max	Units
$C_{I/O}$	I/O Capacitance	FREQ = 1 MHz Unmeasured pins returned to V_{SS}	-	15	pF
C_{IN}	Input Capacitance		-	10	pF
C_{OUT}	Output Capacitance		-	10	pF

Table 2-5: Recommended Operating Conditions

DC Supply Voltage		+4.5 V to +5.5 V
Operating Temperature Range	Commercial	0°C to +70°C
	Industrial	-40°C to +85°C

Table 2-6: Absolute Maximum Ratings

DC Supply Voltage	-.03 to +7.0 V
Input, Output or I/O Voltage Applied	V_{SS} - 0.3 V to V_{DD} + 0.3 V
Storage Temperature Range	-55°C to +150°C
Maximum Package Power Dissipation	1 W
Input Pin Current (@ 25°C)	-10.0 mA to +10.0 mA
Lead Temperature (soldering: 10 sec.)	300°C

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PROGRAMMING

When installed in microprocessor systems the CA82C54 Programmable Interval Timer appears to the system software as an array of peripheral I/O ports, namely: three counters, and a control register for MODE programming.

After power-up, the state of the CA82C54 is undefined. Thus, the mode, the count value and the output of all the counters are undefined. The subsequent operation of each counter is determined when it is programmed, and each counter must be programmed before it can be used. Unused counters need not be programmed.

Counters are programmed by writing a Control Word and then an initial count value for the counter in question. All Control Words are written into the Control Word Register, which is selected when A_1, A_0 = 11. The Control Word itself specifies which counter is being programmed. It is illustrated in Figure 2-8.

By contrast, initial counts are written into the counters, not the Control Word Register. A_1, A_0 inputs are used to select the counter to be written into. The format of the initial count is determined by the Control Word used.

A number of commands are available to the user which allow access to the programmable features of the CA82C54. These are described in detail below.

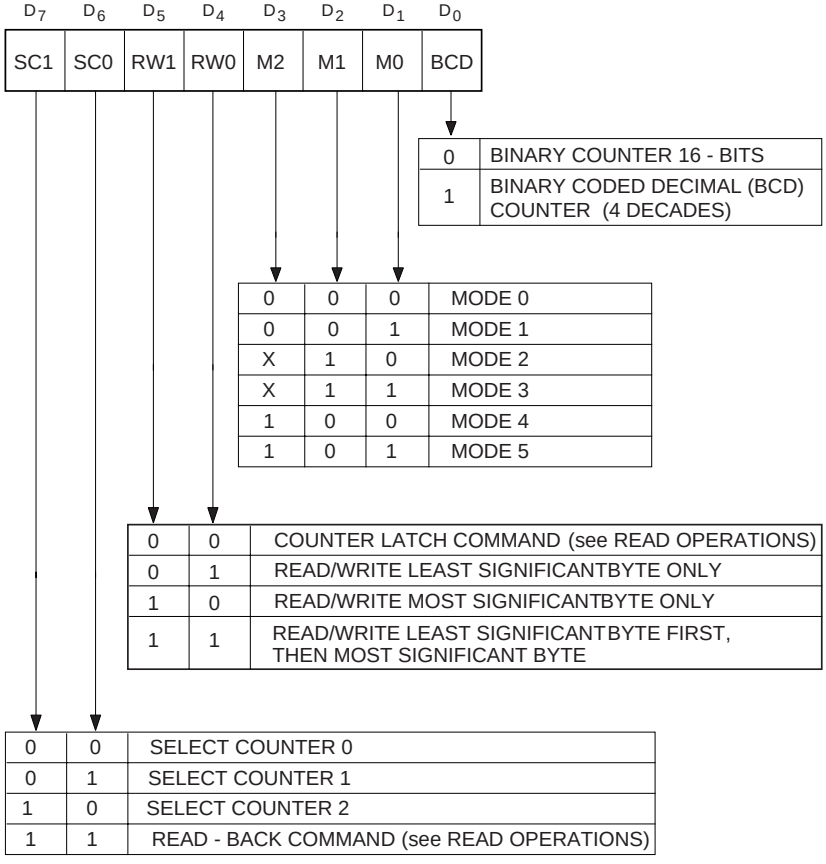


Figure 2-8: Control Word Format

Write Operations

Programming for the CA82C54 is very flexible, and requires that only two conventions be followed:

- For each Counter, the Control Word must be written before the initial count is written.
- The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A_1, A_0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write 2-byte counts, the following precaution applies: a program must not transfer control (between writing the first and second byte) to another routine which also writes into the same Counter. Otherwise, the Counter will be loaded with an incorrect count.

Table 2-7: Sample Programming Sequences

Example	Step	Operation	A_1	A_0
1	1	Control Word-Counter 0	1	1
	2	LSB of count-Counter 0	0	0
	3	MSB of count-Counter 0	0	0
	4	Control Word-Counter 1	1	1
	5	LSB of count-Counter 1	0	1
	6	MSB of count-Counter 1	0	1
	7	Control Word-Counter 2	1	1
	8	LSB of count-Counter 2	1	0
	9	MSB of count-Counter 2	1	0
2	1	Control Word-Counter 1	1	1
	2	Control Word-Counter 0	1	1
	3	LSB of count-Counter 1	0	1
	4	Control Word-Counter 2	1	1
	5	LSB of count-Counter 0	0	0
	6	MSB of count-Counter 1	0	1
	7	LSB of count-Counter 2	1	0
	8	MSB of count-Counter 0	0	0
	9	MSB of count-Counter 2	1	0

Note: In both examples, all counters are programmed to read/write 2-byte counts. These are two of many programming sequences.

Read Operations

It is often desirable to read the value of a counter without disturbing the count in progress, a procedure easily accomplished in the CA82C54.

There are three possible methods for reading the counters. The first is through the Read-Back Command. The second is a simple read operation of the counter, which is selected with the A_1, A_0 inputs. The only requirement is that the CLK input of the selected counter must be inhibited by using either the GATE input or external logic; or the count must first be latched. Otherwise, the count may be in process of changing when it is read, giving an undefined result. The third method involves a special software command called the Counter Latch Command, described in more detail below.

Counter Latch Command

The Counter Latch Command, like a Control Word, is written to the Control Word Register, which is selected when A_1, A_0 = 11. Also like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D_5 and D_4, distinguish this command from a Control Word.

The selected counter's output latch (OL) latches the count at the time the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the counter is reprogrammed). The count is then unlatched automatically and the OL returns to following the counting element (CE). This allows reading the contents of the Counters on the fly without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one counter. Each latched Counter's OL holds its count until it is read. Counter Latch Commands do not affect the programmed Mode of the counter in any way.

If a counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the counter is

programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other counters may be inserted between them.

Another feature of the CA82C54 is that reads and writes of the same counter may be interleaved; for example, if the counter is programmed for two byte counts, the following sequence is valid:

1) Read least significant byte.
2) Write new least significant byte.
3) Read most significant byte.
4) Write new most significant byte.

If a counter is programmed to read and write two-byte counts, the following precaution applies: a program must not transfer control (between reading first and second byte) to another routine which also reads from that same counter. Otherwise, an incorrect count will be read.

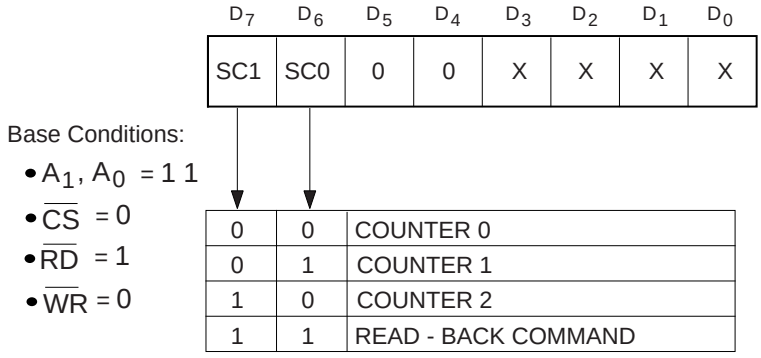


Figure 2-9: Counter Latch Command Format

Read-Back Command

The Read-Back Command allows the user to check the count value, the programmed Mode and the current state of the OUT pin and Null count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in Figure 2-10. The command applies to the counters selected by setting their corresponding bits D_3, D_2, $D_1 = 1$.

The Read-Back Command may be used to latch multiple counter output latches (OL) by setting the COUNT bit $D_5 = 0$ and selecting the desired counter(s). This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count Read-Back Commands are issued to the same counter without reading the count, all but the first are ignored. That is, the count which will be read is the count at the time the first Read-Back Command was issued.

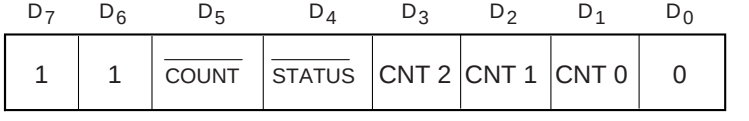
The Read-Back Command may also be used to latch status information of selected counter(s) by setting bit $D_4 = 0$ (STATUS). Status must be latched to be read; as counter status is obtained by a read from that counter.

The counter status format is shown in Figure 2-11. Bits D_5 through D_0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D_7 contains the current state of the OUT pin. This allows the user to monitor counter output via software, thus eliminating some hardware from a system.

NULL COUNT bit D_6 indicates when the last count written to the Counter Register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions. Until the count is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Table 2-8.

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored. That is, the status that will be read is the status of the counter at the time the first status Read-Back Command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both COUNT and STATUS bits D_5, $D_4 = 0$. This is functionally the same as issuing two separate Read-Back Commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status Read-Back Commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Table 2-9.



Base Conditions:

- $A_1, A_0 = 1\ 1$
- $\overline{CS} = 0$
- $\overline{RD} = 1$
- $\overline{WR} = 0$

D_5: 0 = Latch count of selected counter(s)
D_4: 0 = Latch status of selected counter(s)
D_3: 1 = Selected Counter 2
D_2: 1 = Selected Counter 1
D_1: 1 = Selected Counter 0

Figure 2-10: Read-Back Command Format

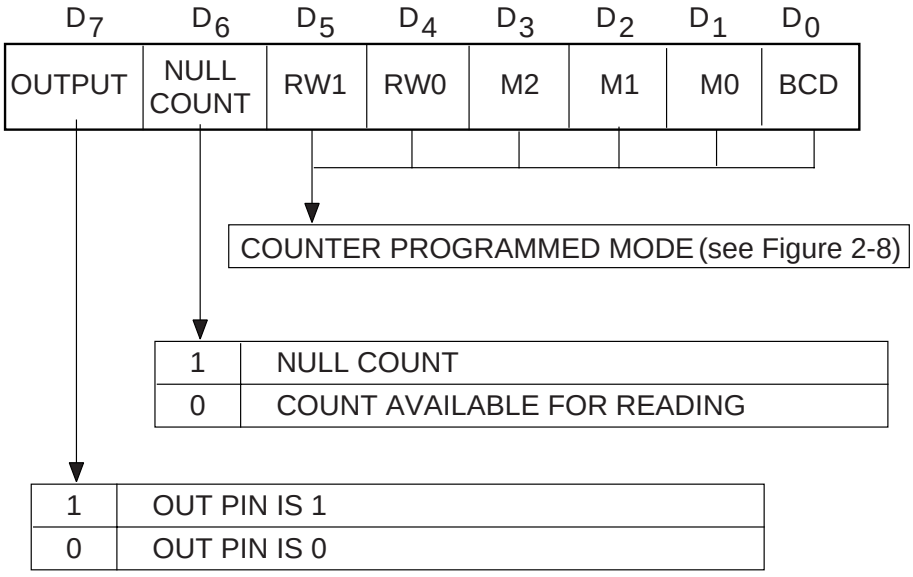


Figure 2-11: Status Byte

Table 2-8: Null Count Operation

	This Action:	Causes:
A	Write to the control word register[1]	Null Count = 1
B	Write to the count register (CR)[2]	Null Count = 1
C	New count is loaded into CE (CR → CE)	Null Count = 0

Notes: 1. Only the counter specified by the control word will have its null count set = 1. Null counts of other counters are unaffected.
2. If the counter is programmed for two-byte counts (least significant byte then most significant byte) null count goes to 1 when second byte is written.

Table 2-9: Read-Back Command Example

Command Description	Result	Command Word							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read back count and status of Counter 0	Count and status latched for Counter 0	1	1	0	0	0	0	1	0
Read back status of Counter 1	Status latched for Counter 1	1	1	1	0	0	1	0	0
Read back status of Counters 2, 1	Status latched for Counter 2 only	1	1	1	0	1	1	0	0
Read back count of Counter 2	Count latched for Counter 2	1	1	0	1	1	0	0	0
Read back count and status of Counter 1	Count latched for Counter 1, but not status	1	1	0	0	0	1	0	0
Read back status of Counter 1	Command ignored, status already latched for Counter 1	1	1	1	0	0	0	1	0

OPERATIONAL DESCRIPTION

The following operations are common to all modes.

Control Word: When a Control Word is written to a Counter, all Control Logic is Reset, and OUT is initialized to a known state. No CLK pulses are needed.

Gate: The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3, and 4 the GATE input is level sensitive, and the logic level is sampled on the rising edge of CLK. In Modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these modes, a rising edge of GATE (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is sampled on the next rising edge of CLK, then is immediately reset. In this way, a trigger will be detected no matter when it occurs and a high logic level does not have to be maintained until the next CLK pulse. A summary is given in Table 2-12.

Note that in Modes 2 and 3, the GATE input is both edge- and level-sensitive. If a CLK source other than the system clock is used in Modes 2 and 3, GATE should be pulsed immediately after the $\overline{WR}$ for a new count value.

Table 2-10: Minimum and Maximum Initial Counts

Mode	Minimum Count	Maximum Count*
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

*0 is equivalent to 2^{16} for binary and 10^4 for BCD counting.

Counter: New counts are loaded, with the largest possible initial count being zero (0), equivalent to 2^{16} for binary counting and 10^4 for BCD counting, as in Table 2-10.

Counters decremented on the falling edge of CLK do not stop when they reach zero. In Modes 0, 1, 4, and 5 the Counters wrap around to the highest count (either FFFF hex for binary counting or 9999 for BCD counting), then continue counting. Modes 2 and 3 are periodic; the Counters reload themselves with the initial count, then continue counting from there.

If both the count and status registers of a counter are latched, the first read operation of that counter will return the latched status, regardless of which was latched first. The next one or two reads (the counter can be programmed for one or two type counts) will return the latched count. Subsequent reads will return an unlatched count. Read and Write operations are summarized in Table 2-11.

Table 2-11: Read/Write Operations Summary

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

Table 2-12: Gate Pin Operations Summary

Signal Status Modes	Low, or Going Low	Rising	High
0	•Disables counting	-	•Enables counting
1	-	•Initiates counting •Resets output after next clock	-
2	•Disables counting •Sets output immediately high	•Initiates counting	•Enables counting
3	•Disables counting •Sets output immediately high	•Initiates counting	•Enables counting
4	•Disables counting	-	•Enables counting
5	-	•Initiates counting	-

MODE DEFINITIONS

The following terms are useful in describing the operation of the CA82C54.

- CLK pulse: A rising edge, followed by a falling edge, of a Counter's CLK input.
- Trigger: A rising edge of a Counter's GATE input.
- Counter loading: Transfer of a count from the CR to the CE (see Functional Description)

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is set low, and remains low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

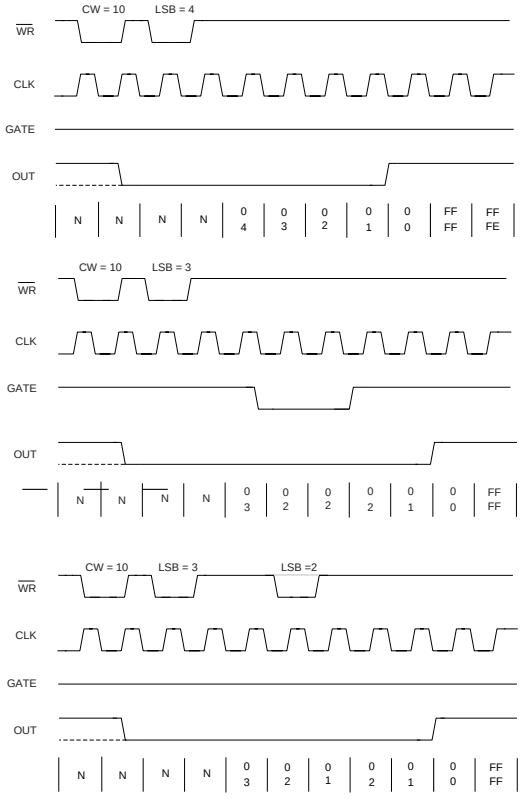
After a Control Word and initial count are written to a Counter, the initial count is loaded on the next CLK pulse. Since this CLK pulse does not decrement the count, OUT does not go high until N + 1 CLK pulses after the initial count is written (where N is the initial count value).

If a new count is written to the Counter, it is loaded on the next CLK pulse and counting continues from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N + 1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later. A CLK pulse is not required to load the Counter as this has already been done.



Notes: These conventions apply to all mode timing diagrams:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The counter is always selected (CS always low).
3. CW stands for Control Word; CW = 10 means a control word of 10, hex is written to the counter.
4. LSB is the Least Significant Byte of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the counter is programmed to read/write LSB only, the most significant byte cannot be read. N stands for an undefined count. Vertical lines show transitions between count values.

Figure 2-12: Mode 0 Timing

Mode 1: Hardware Retriggerable One-Shot

OUT is initially high. To begin the one-shot pulse, OUT goes low on the CLK pulse following a trigger and remains low until the Counter reaches zero. OUT then goes high and remains high until the CLK pulse following the next trigger.

After a Control Word and initial count have been written, the Counter is armed. A trigger causes the Counter to be loaded and OUT to be set low on the next CLK pulse, starting the one-shot pulse. An initial count of N results in a one-shot pulse N CLK cycles long. Since the one-shot is retriggerable, OUT remains low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In this case, the new count is loaded into the Counter and the one-shot pulse continues for the duration of the count.

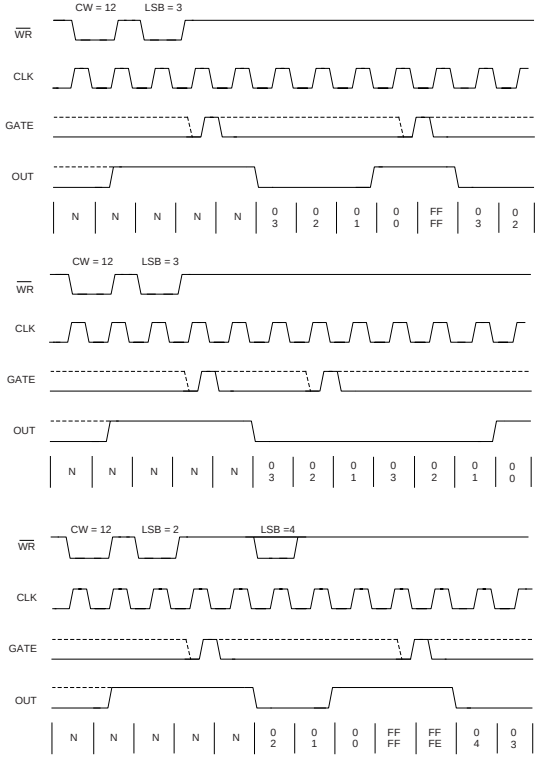


Figure 2-13: Mode 1 Timing

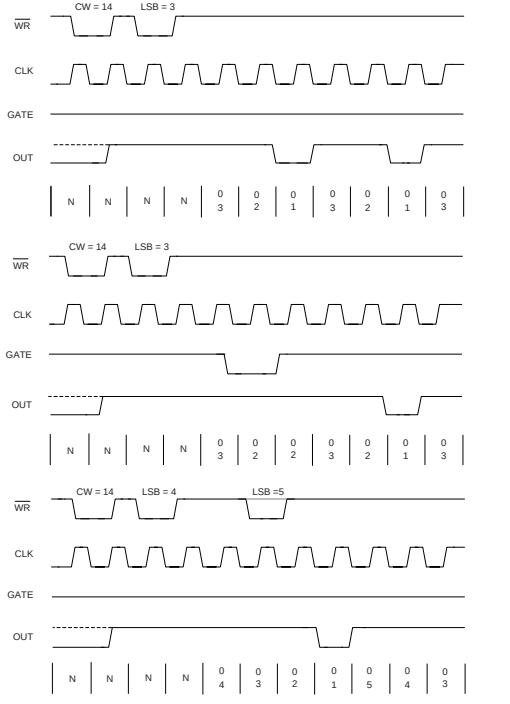
Mode 2: Rate Generator

This mode functions like a divide-by-N counter and is typically used for generating Real Time Clock Interrupts. OUT is initially high. When the initial count has decremented to 1, OUT goes low for one CLK pulse, then high again. The Counter reloads the initial count and the process is

repeated. Mode 2 is periodic, with the same sequence repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the initial count into the Counter on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After a Control Word and initial count have been written, the Counter is loaded on the next CLK pulse. OUT goes low NCLK pulses after the initial count is written, which allows the Counter to be synchronized by software.



Note: A GATE transition should not occur one clock cycle prior to reaching the terminal count (TC).

Figure 2-14: Mode 2 Timing

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after a new count is written, but before the end of the current period, the Counter is loaded with the new count on the next CLK pulse and counting continues from the new count. Else, the new count is loaded at the end of the current counting cycle. In Mode 2, a count of 1 is illegal.

Mode 3: Square Wave Mode

Mode 3 is typically used for Baud rate generation, and is similar to Mode 2 except for the duty cycle of OUT. OUT is initially high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is also periodic, with the sequence above repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately (no CLK pulse is needed). A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

The Counter is loaded on the next CLK pulse after a Control Word and initial count have been written. This allows the Counter to be synchronized by software.

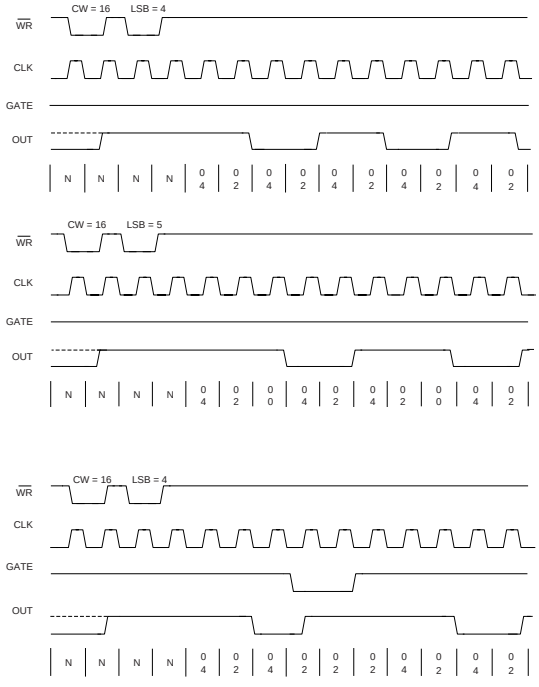
Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter is loaded with the new count on the next CLK pulse and counting continues from the new count. Otherwise, the new count is loaded at the end of the current half-cycle.

Mode 3 is implemented as follows according to whether the initial count value is even or odd:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then decremented by two on succeeding CLK pulses. When the count expires, OUT goes low and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

Odd counts: OUT is initially high. The initial count minus one (to give an even number) is loaded on one CLK pulse and then decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, OUT goes low and the Counter is reloaded with the initial count minus one.

Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT is high for (N + 1)/2 counts and low for (N - 1)/2 counts.



Note: A GATE transition should not occur one clock prior to terminal count.

Figure 2-15: Mode 3 Timing

Mode 4: Software Triggered Strobe

OUT is initially high. When the initial count expires, OUT goes low for one CLK pulse and then goes high again. Counting sequence is triggered by writing initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

The Counter is loaded on the next CLK pulse after a Control Word and initial count have been written. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it is loaded on the next CLK pulse and counting continues from the new count. If a two-byte count is written, the following events occur:

1) Writing the first byte has no effect on counting.
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be retriggered by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

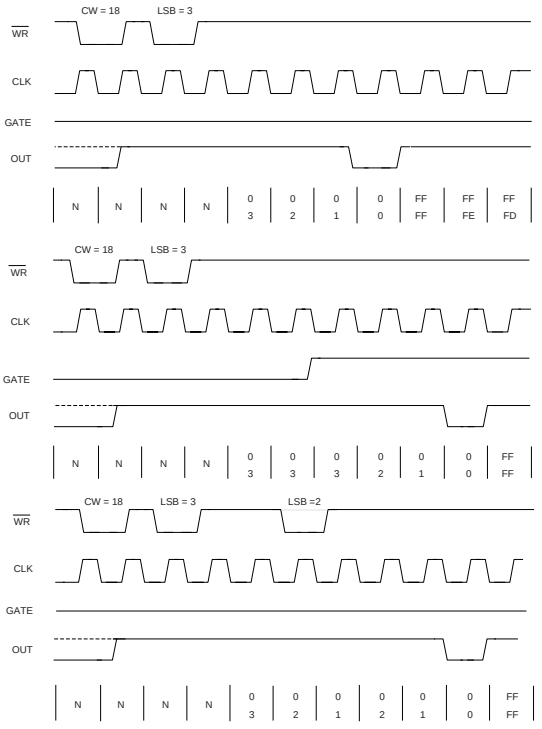


Figure 2-16: Mode 4 Timing

Mode 5: Retriggerable Hardware Triggered Strobe

OUT is initially high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT goes low for one CLK pulse, then goes high again.

After a Control Word and initial count has been written, the counter is loaded on the first CLK pulse following a trigger. This CLK pulse does not decrement the count, so, given an initial count of N, OUT does not strobe low until N + 1 CLK pulses after a trigger.

A trigger causes the Counter to be loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable, so OUT will not go low until N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written, but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

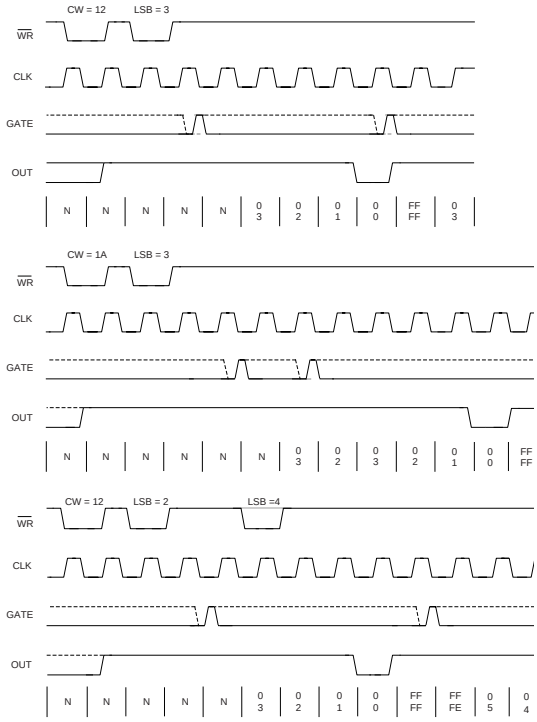


Figure 2-17: Mode 5 Timing

- **Pin and functional compatibility with the industry standard 8255A**
- **Supports 8086/8088 and 80186/188 microprocessors**
- **Very high speed - 10, 8 and 5 MHz zero wait state operation**
- **Low power CMOS Implementation**
- **TTL input/output compatibility**
- **24 programmable I/O pins**
- **Direct bit set/reset capability**
- **Bi-directional bus operation**
- **Enhanced control word read capability**
- **Bus-hold circuitry on all I/O ports eliminates the need for external pull-up resistors**

The CA82C55A Programmable Peripheral Interface is a high performance CMOS device offering pin for pin functional compatibility with the industry standard 8255A. It includes 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. Bus hold circuitry on all I/O ports together with TTL compatibility over the full temperature range eliminates the need for pull-up resistors.

The CA82C55A is a general purpose programmable I/O device designed for use with several different microprocessors. Its high speed and high performance make it ideally suited for aerospace and defence applications, while the low power consumption suits it to portable systems and systems with low power standby modes.

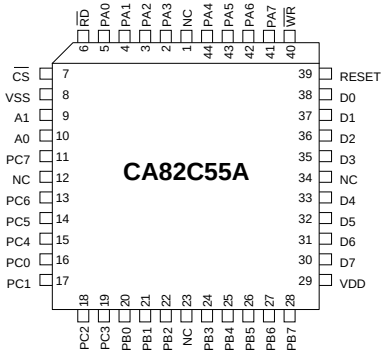


Figure 2-1: PLCC Pin Configurations

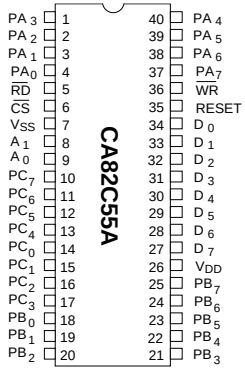


Figure 2-2: PDIP Pin Configurations

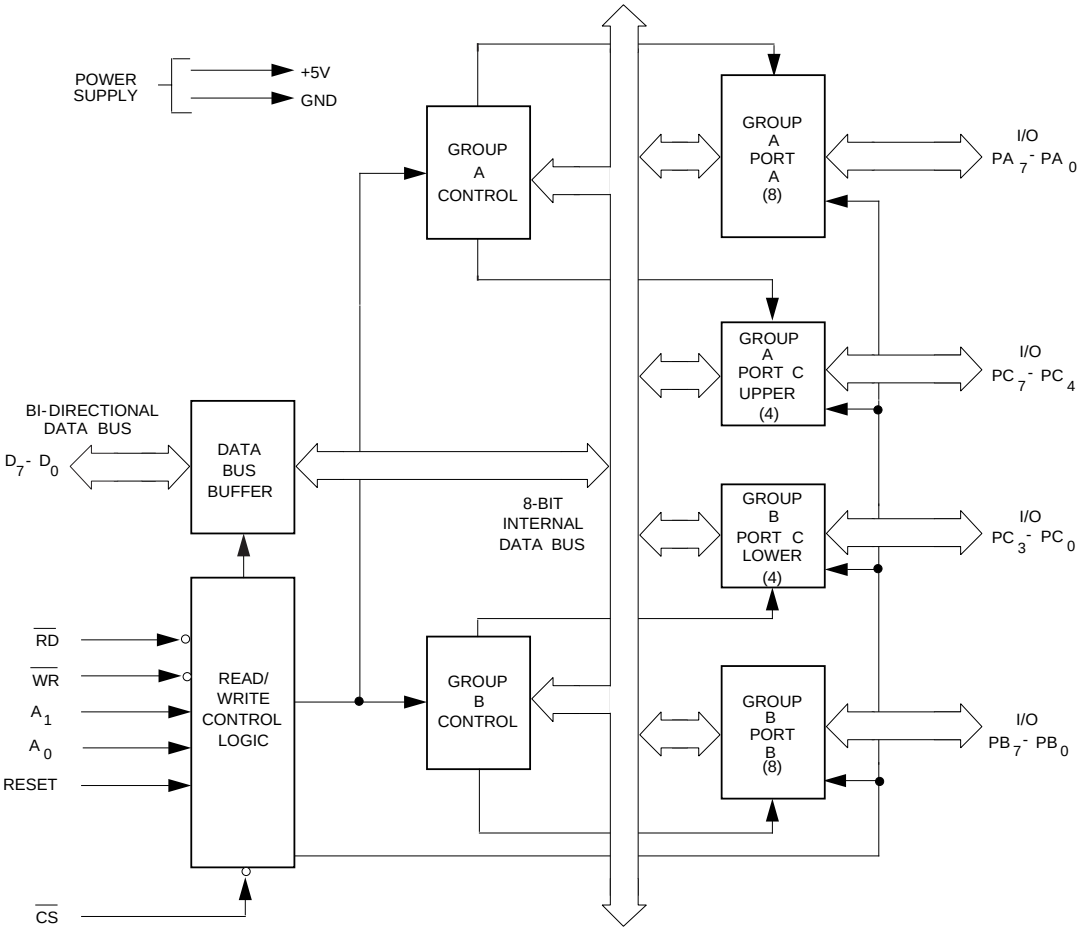


Figure 2-3: CA82C55A Block Diagram

Table 2-1: Pin Descriptions

Symbol	Pin(s) PLCC	Pin(s) PDIP	Type	Name and Function
A_1, A_0	9, 10	8, 9	I	**Address**: These input signals, in conjunction with $\overline{RD}$ and $\overline{WR}$, control the selection of one of the three ports or the control word registers.

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input Operation (Read)
0	0	0	1	0	Port A - Data Bus
0	1	0	1	0	Port B - Data Bus
1	0	0	1	0	Port C - Data Bus
1	1	0	1	0	Control Word - Data Bus

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Output Operation (Write)
0	0	1	0	0	Data Bus - Port A
0	1	1	0	0	Data Bus - Port B
1	0	1	0	0	Data Bus - Port C
1	1	1	0	0	Data Bus - Control

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Disable Function
X	X	X	X	1	Data Bus - 3 - State
X	X	1	1	0	Data Bus - 3 - State

$\overline{CS}$	7	6	I	**Chip Select**: A low on this input enables the CA82C55A to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
D_{0-7}	38-30	34-27	I/O	**Data Bus**: Bi-directional, tri-state data bus lines, connected to system data bus.
PA_{0-7}	5-2 44-41	4-1 40-37	I/O	**Port A, Pins 0-7**: An 8-bit data output latch/buffer and an 8-bit data input buffer.
PB_{0-7}	20-28	18-25	I/O	**Port B, Pins 0-7**: An 8-bit data output latch/buffer and an 8-bit data input buffer.
PC_{0-3}	16-19	14-17	I/O	**Port C, Pins 0-3**: Lower nibble of an 8-bit data output latch/buffer an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.
PC_{4-7}	15-13, 11	13-10	I/O	**Port C, Pins 4-7**: Upper nibble of Port C.
$\overline{RD}$	6	5	I	**Read Control**: This input is low during CPU read operations.
RESET	39	35	I	**Reset**: A high on this input clears the control register and all ports are set to the input mode.
V_{DD}	29	26		**Power**: 5 V ± 10% DC Supply
V_{SS}	8	7		**Ground**: 0 V
$\overline{WR}$	40	36	I	**Write Control**: This input is low during CPU write operations.

FUNCTIONAL DESCRIPTION

General

The CA82C55A is a programmable peripheral interface device designed for use in high speed, low power microcomputer systems. It is a general purpose I/O component which functions to interface peripheral equipment to the microcomputer system bus. The functional configuration of the CA82C55A is programmed by the system software such that no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bi-directional 8-bit buffer is used to interface the CA82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. The data bus buffer also transfers control words and status information.

Read/Write and Control Logic

This block manages all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control buses and issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the system software. The CPU outputs a control word to the CA82C55A. The control word contains information such as mode, bit set, bit reset, etc., that initializes the functional configuration of the CA82C55A.

Each of the Control blocks (Group A and Group B) accepts commands from the Read/Write Control Logic, receives control words from the internal data bus and issues the proper commands to its associated ports.

- Control Group A - Port A and Port C upper (C_7 - C_4)
- Control Group B - Port B and Port C lower (C_3 - C_0)

The control word register can be both written and read as shown in the address decode table in the pin descriptions (Table 2-1). The control word format for both Read and Write operations is shown in Figure 2-8. Bit D_7 will always be a logic ONE when the control word is read, as this implies control word mode information.

Ports A, B and C

The CA82C55A contains three 8-bit ports (A, B and C). All can be configured in a wide variety of functional characteristics by the system software, but each also has its own special features.

Port A: One 8-bit data output latch/buffer and one 8-bit input latch. Both pull-up and pull-down bus hold devices are present on Port A.

Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer. Only pull-up bus hold devices are present on Port B.

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). Port C can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only pull-up bus hold devices are present on Port C.

Figure 2-4 illustrates the bus-hold circuit configuration for Ports A, B and C.

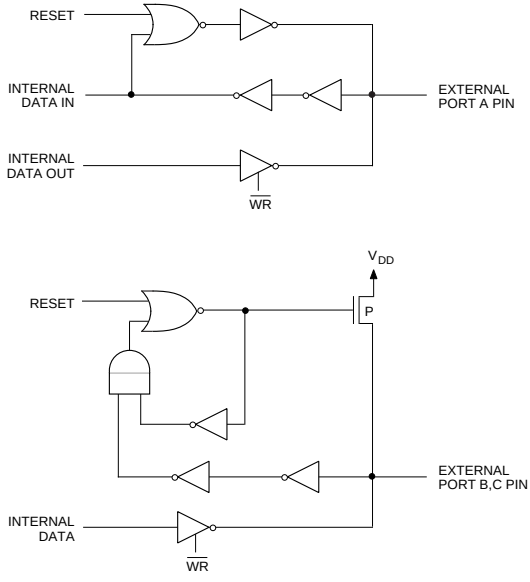


Figure 2-4: Ports A, B & C Bus-Hold Configuration

Table 2-2: AC Characteristics (T_A = -40° to +85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

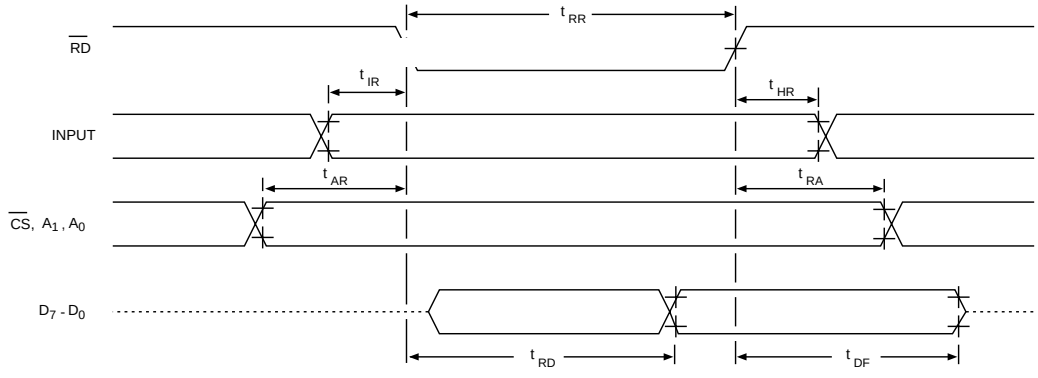
Symbol	Parameter	Test Conditions	Limits (5 MHz)		Limits (8 MHz)		Limits (10 MHz)		Units
			Min	Max	Min	Max	Min	Max	
t_{AD}	$\overline{ACK}$ = 0 to Output			300		175		125	ns
t_{AIT}	$\overline{ACK}$ = 1 to INTR = 1			350		150		100	ns
t_{AK}	$\overline{ACK}$ Pulse Width		300		200		100		ns
t_{AOB}	$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1			350		150		100	ns
t_{AR}	Address Stable Before $\overline{RD}$ ↓		20		0		0		ns
t_{AW}	Address Stable Before $\overline{WR}$ ↓		0		0		0		ns
t_{DF}	$\overline{RD}$ ↑ to Data Floating		10	100	10	75	10	75	ns
t_{DW}	Data Setup Time Before $\overline{WR}$ ↑		100		100		50		ns
t_{HR}	Peripheral Data After $\overline{RD}$		20		0		0		ns
t_{IR}	Peripheral Data Before $\overline{RD}$		20		0		0		ns
t_{KD}	$\overline{ACK}$ = 1 to Output Float		20	250	20	250	20	175	ns
t_{PH}	Peripheral Data After $\overline{STB}$ High		180		50		40		ns
t_{PS}	Peripheral Data Before $\overline{STB}$ High		20		20		20		ns
t_{RA}	Address Hold Time After $\overline{RD}$ ↑		20		0		0		ns
t_{RD}	Data Delay from $\overline{RD}$ ↓			200		120		95	ns
t_{RES}	Reset Pulse Width	See Note 2	500		500		400		ns
t_{RIB}	$\overline{RD}$ = 1 to IBF = 0			300		150		120	ns
t_{RIT}	$\overline{RD}$ = 0 to INTR = 0			400		200		160	ns
t_{RR}	$\overline{RD}$ Pulse Width		300		150		100		ns
t_{RV}	Recovery Time between $\overline{RD}$/$\overline{WR}$		850		200		100		ns
t_{SIB}	$\overline{STB}$ = 0 to IBF = 1			300		150		100	ns
t_{SIT}	$\overline{STB}$ = 1 to INTR = 1			300		150		100	ns
t_{ST}	$\overline{STB}$ Pulse Width		300		100		50		ns
t_{WA}	Address Hold Time After $\overline{WR}$ ↑	Ports A & B	30		20		10		ns
		Port C	30		20		10		ns
t_{WB}	$\overline{WR}$ = 1 to Output			350		350		150	ns
t_{WD}	Data Hold Time After $\overline{WR}$ ↑	Ports A & B	40		30		20		ns
		Port C	40		30		20		ns
t_{WIT}	$\overline{WR}$ = 0 to INTR = 0	See Note 1		850		200		160	ns
t_{WOB}	$\overline{WR}$ = 1 to $\overline{OBF}$ = 0			650		150		120	ns
t_{WW}	$\overline{WR}$ Pulse Width		300		100		70		ns

Notes:1. INTR ↑ may occur as early as $\overline{WR}$ ↓.

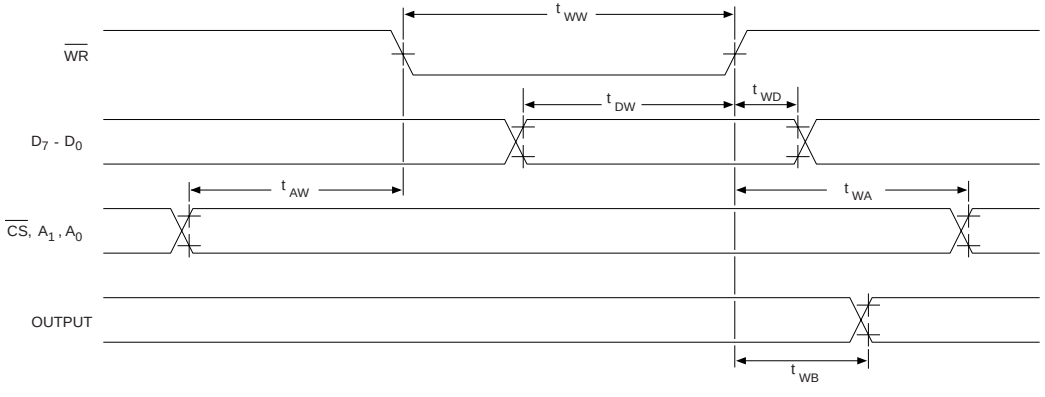
2. Width of initial Reset pulse after power on must be at least 50 µSec. Subsequent Reset pulses may be 500 ns minimum.

Figure 2-5: Timing Diagrams

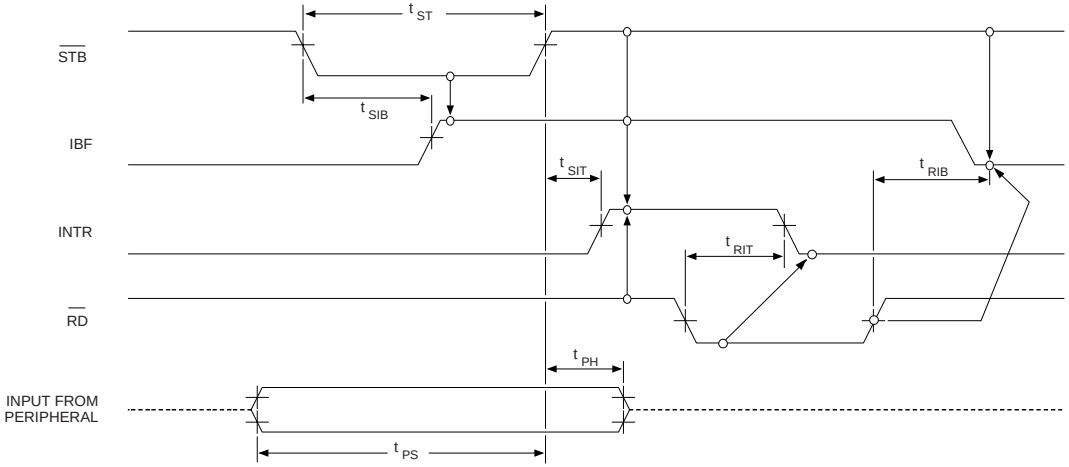
a) Mode 0 (Basic Input)



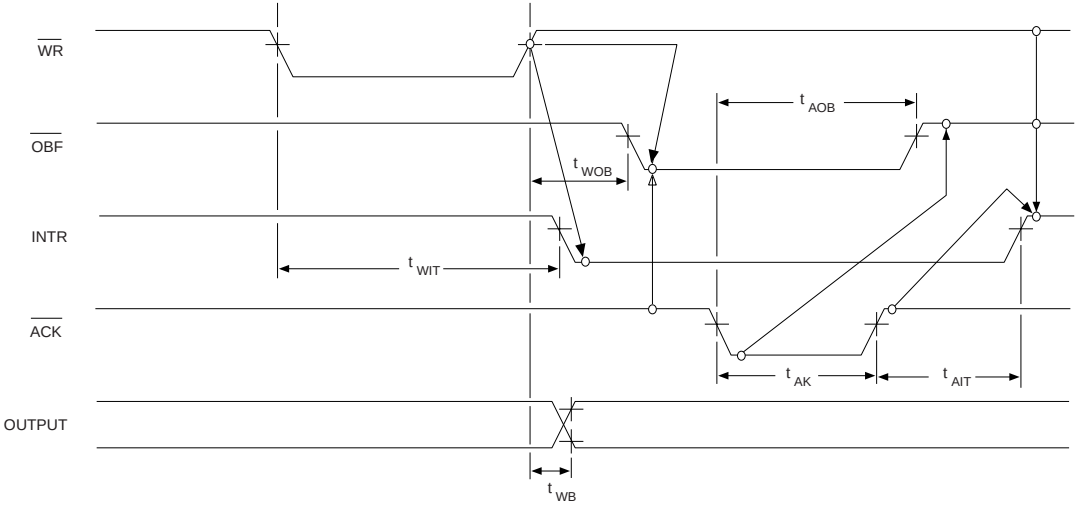
b) Mode 0 (Basic Output)



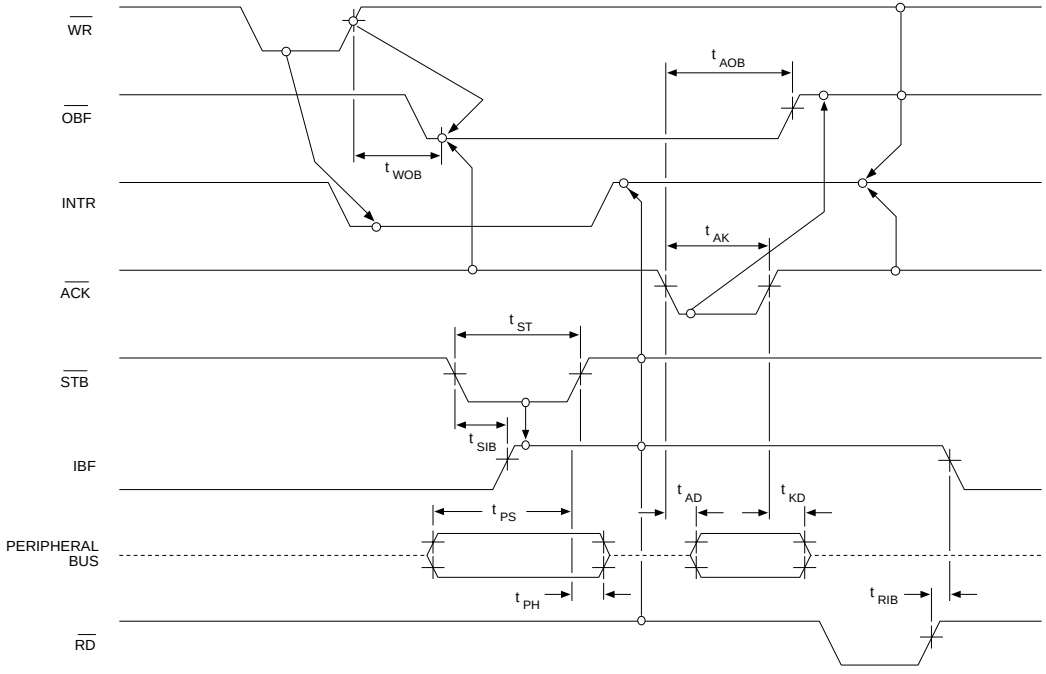
c) Mode 1 (Strobed Input)



d) Mode 1(Strobed Output)

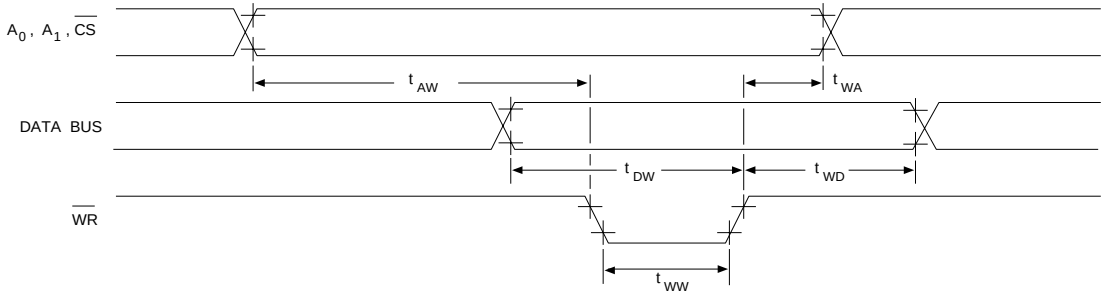


e) Mode 2 (Bi-directional)

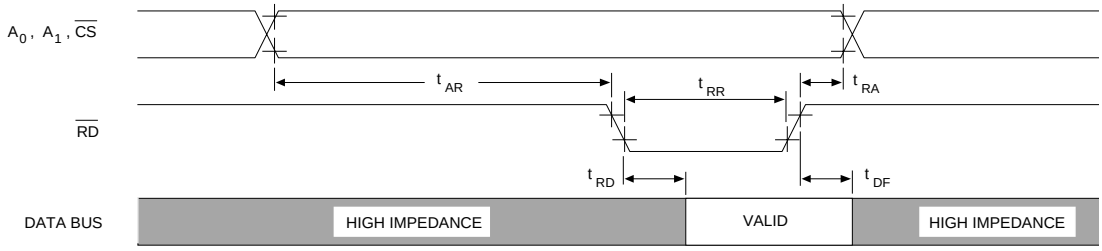


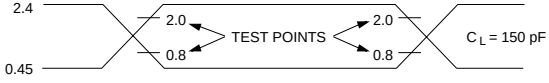
Note: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$, and $\overline{STB}$ occurs before $\overline{RD}$, is permissible ($INTR = IBF \bullet \overline{MASK} \bullet \overline{STB} \bullet \overline{RD} + \overline{OBF} \bullet \overline{MASK} \bullet \overline{ACK} \bullet \overline{WR}$).

f) Write Timing



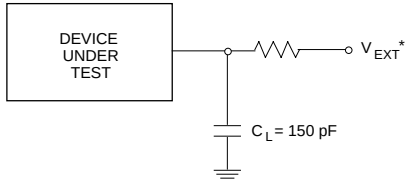
g) Read Timing





A.C. Testing Inputs are driven at 2.4V for a Logic 1 and 0.45V for a Logic 0. Timing measurements are made at 2.0V for a Logic 1 and 0.8 V for a Logic 0.

Figure 2-6: AC Testing I/O Waveform



*V_{EXT} is set at various voltages during testing to guarantee the specification. C_L includes jig capacitance.

Figure 2-7: AC Testing Load Circuit

Table 2-3: DC Characteristics (T_A = -40° to +85° C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{DD}	V_{DD} Supply Current	(Note 3)	-	10	mA
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$ or V_{SS} (Note 1)	-1.0	1.0	µA
I_{OFL}	Output Float Leakage Current	$V_{IN} = V_{DD}$ to 0V (Note 2)	-10	10	µA
I_{PHH}	Port Hold High Leakage Current	V_{OUT} = 3.0 V Ports A, B and C	-50	-350	µA
I_{PHL}	Port Hold Low Leakage Current	V_{OUT} = 1.0 V Port A only	+50	+350	µA
V_{IH}	Input High Voltage	Note 4	2.0	V_{DD}	V
V_{IL}	Input Low Voltage	Note 4	-0.3	0.8	V
V_{IHS}	Schmitt Trigger Input High Voltage	Note 5	2.1	V_{DD} + 0.3	V
V_{ILS}	Schmitt Trigger Input Low Voltage	Note 5	-0.3	0.7	V
V_{HY}	Schmitt Trigger Hysteresis	Note 5	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.5 mA	3.0	-	V
		I_{OH} = -100 µA	V_{DD} - 0.4	-	V
V_{OL}	Output Low Voltage	I_{OL} = 2.5 mA	-	0.4	V

Notes: 1. Pins A_1, A_0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, Reset.
2. Data Bus; Ports B, C.
3. Outputs Open
4. Applies to pins D_{7-0}, PA_{7-0}, PB_{7-0}, PC_{7-0}
5. Applies to pins: A_1, A_0, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, and RESET

Table 2-4: Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0V, V_{IN} = +5 V or V_{SS})

Symbol	Parameter	Test Conditions	Min	Max	Units
$C_{I/O}$	I/O Capacitance	FREQ = 1 MHz Unmeasured pins returned to V_{SS}	-	15	pF
C_{IN}	Input Capacitance		-	10	pF

Table 2-5: Recommended Operating Conditions

DC Supply Voltage		+4.5 V to +5.5 V
Operating Temperature Range	Commercial	0°C to +70°C
	Industrial	-40°C to +85°C

Table 2-6: Absolute Maximum Ratings

DC Supply Voltage	-.03 to +7.0 V
Input, Output or I/O Voltage Applied	V_{SS} - 0.3 V to V_{DD} + 0.3 V
Storage Temperature Range	-55°C to +150°C
Maximum Package Power Dissipation	1 W
Input Pin Current (@ 25°C)	-10.0 mA to +10.0 mA
Lead Temperature (soldering: 10 sec.)	300°C

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

- Mode 0 - Basic input/output
- Mode 1 - Strobed input/output
- Mode 2 - Bi-directional Bus

When the Reset input goes high all ports will be set to the input mode with all 24 port lines held at a logic one level by the internal bus hold devices. After the reset is removed, no additional initialization is required for the CA82C55A to remain in the input mode. No pullup or pulldown devices are required. During the execution of the system program, any of the other modes may be deleted by using a single output instruction. This allows a single CA82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined such that their functional definition can be tailored to almost any I/O structure. For example, Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, and Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis

.

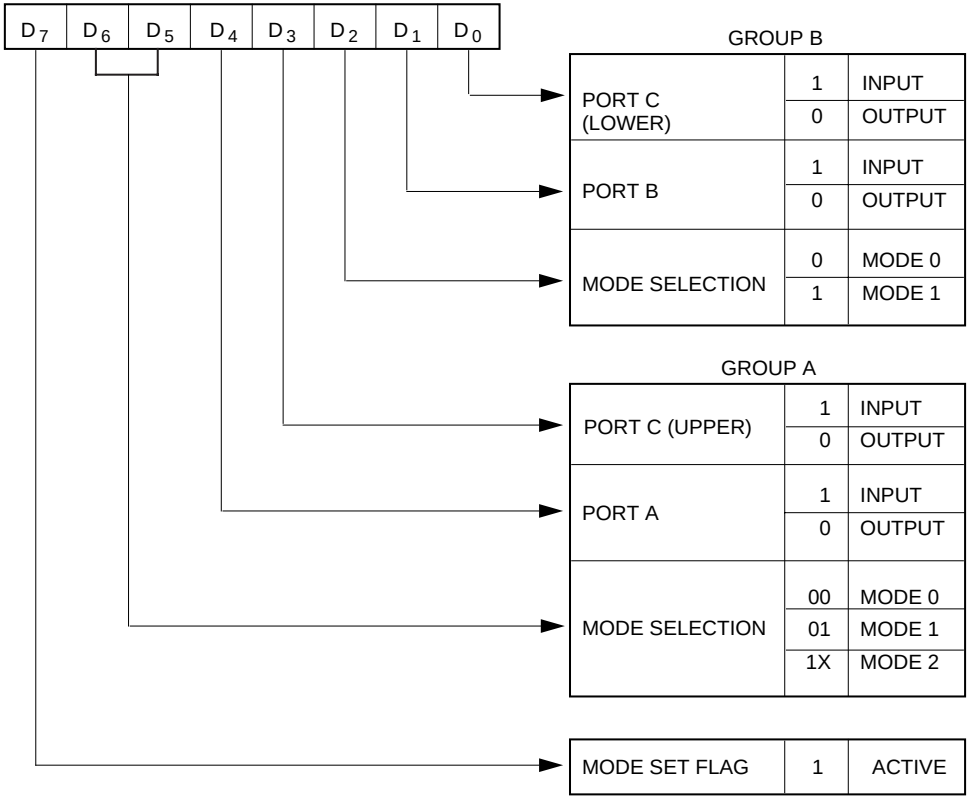


Figure 2-8: Mode Definition Format

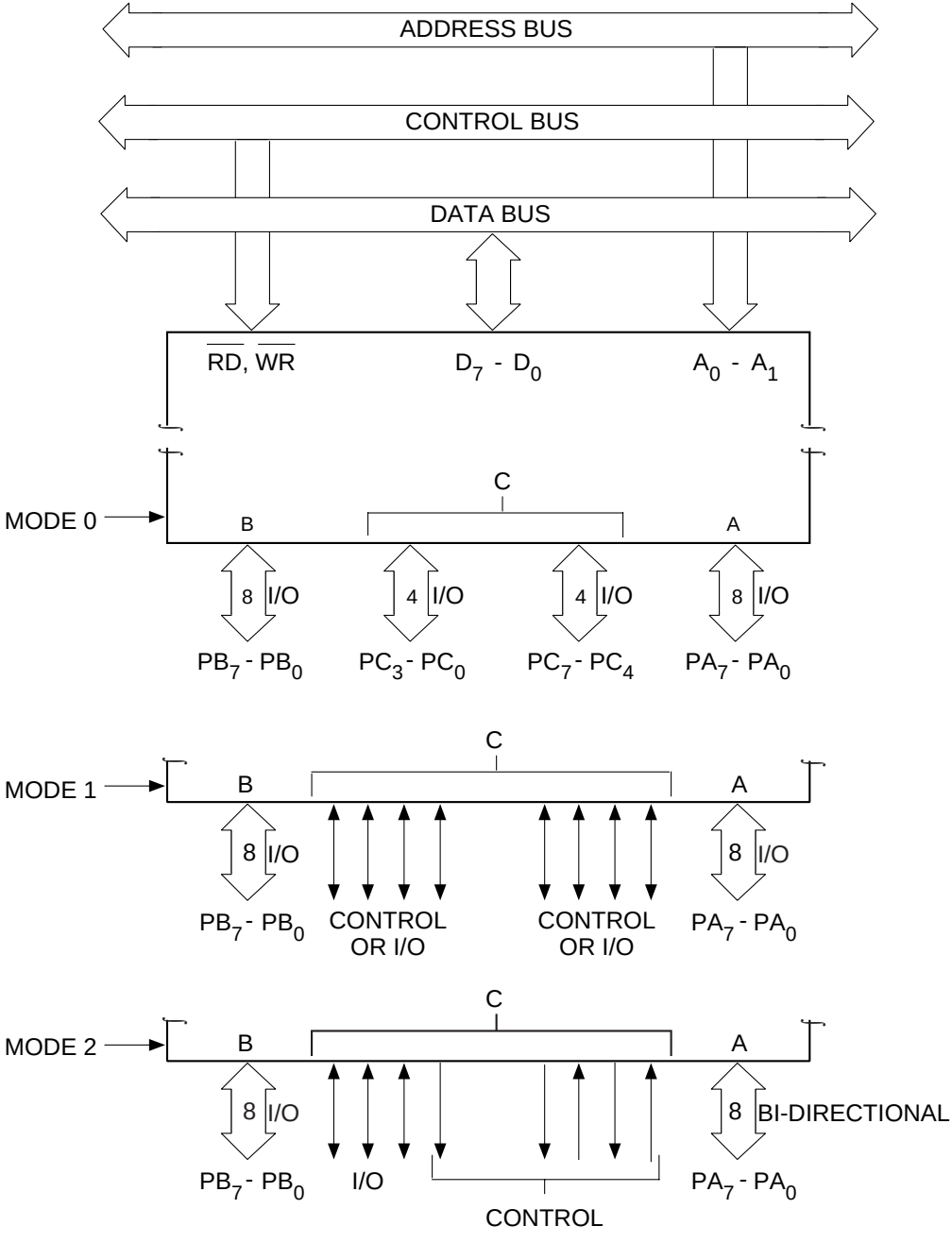


Figure 2-9: Mode Definitions and Bus Interface

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single output instruction. This feature reduces the software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation as if they were data output ports.

Interrupt Control Functions

When the CA82C55A is operating in Mode 1 or Mode 2, control signals are provided for use as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop using the bit set/reset function of Port C.

This function allows the Programmer to allow or disallow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) - INTE is SET - Interrupt enable

(BIT-RESET) - INTE is RESET - Interrupt disable

Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

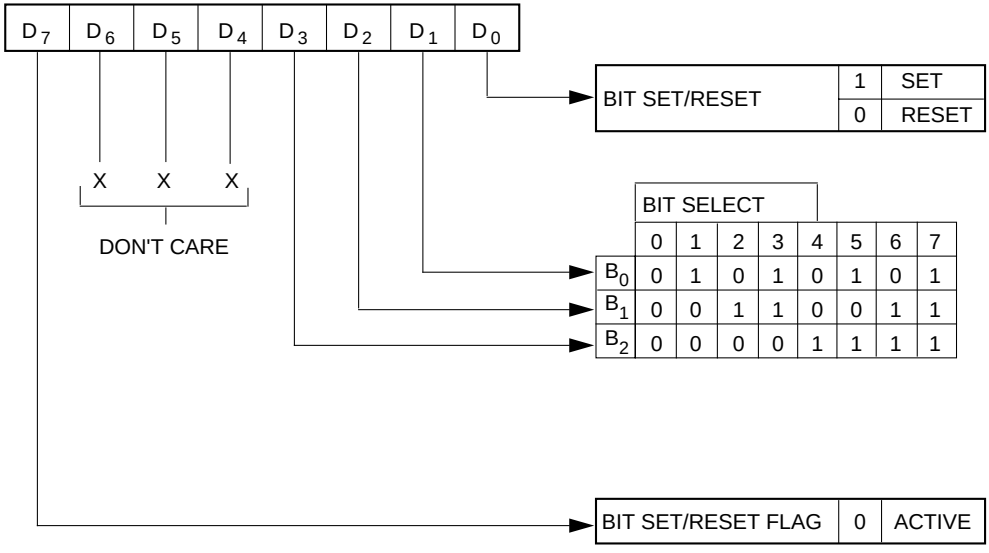


Figure 2-10: Bit Set/Reset Format

Operating Modes

Mode 0 (Basic Input/Output)

This mode provides simple input and output operations for each of the three ports. No handshaking is required. Data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this mode.

Refer to Figure 2-11 for an example of a Mode 0 Configuration

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	0

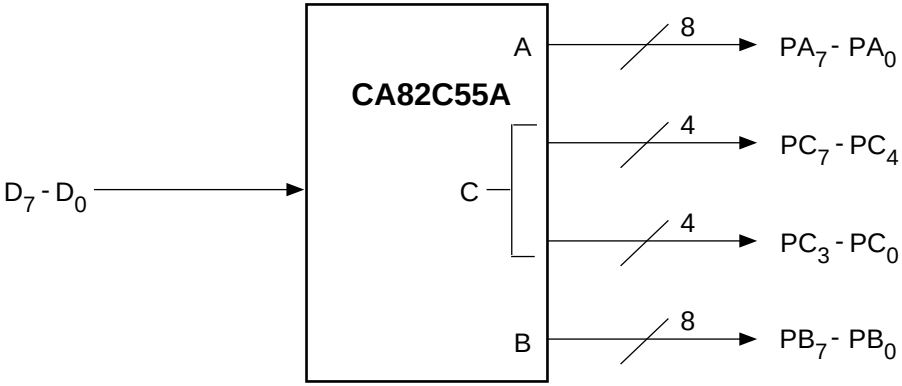


Figure 2-11: Mode 0 Configuration

Table 2-7: Mode 0 Port Definition

Control Word #	Control Word Bits								Port Direction			
		Group A				Group B			Group A		Group B	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	PA_7-PA_0	PC_7-PC_4	PC_3-PC_0	PB_7-PB_0
0	1	0	0	0	0	0	0	0	OUTPUT	OUTPUT	OUTPUT	OUTPUT
1	1	0	0	0	0	0	0	1	OUTPUT	OUTPUT	INPUT	OUTPUT
2	1	0	0	0	0	0	1	0	OUTPUT	OUTPUT	OUTPUT	INPUT
3	1	0	0	0	0	0	1	1	OUTPUT	OUTPUT	INPUT	INPUT
4	1	0	0	0	1	0	0	0	OUTPUT	INPUT	OUTPUT	OUTPUT
5	1	0	0	0	1	0	0	1	OUTPUT	INPUT	INPUT	OUTPUT
6	1	0	0	0	1	0	1	0	OUTPUT	INPUT	OUTPUT	INPUT
7	1	0	0	0	1	0	1	1	OUTPUT	INPUT	INPUT	INPUT
8	1	0	0	1	0	0	0	0	INPUT	OUTPUT	OUTPUT	OUTPUT
9	1	0	0	1	0	0	0	1	INPUT	OUTPUT	INPUT	OUTPUT
10	1	0	0	1	0	0	1	0	INPUT	OUTPUT	OUTPUT	INPUT
11	1	0	0	1	0	0	1	1	INPUT	OUTPUT	INPUT	INPUT
12	1	0	0	1	1	0	0	0	INPUT	INPUT	OUTPUT	OUTPUT
13	1	0	0	1	1	0	0	1	INPUT	INPUT	INPUT	OUTPUT
14	1	0	0	1	1	0	1	0	INPUT	INPUT	OUTPUT	INPUT
15	1	0	0	1	1	0	1	1	INPUT	INPUT	INPUT	INPUT

Mode 1 (Strobed Input/Output)

This mode transfers I/O data to or from a specified port in conjunction with strobes or handshaking signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these handshaking signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B).
- Each group contains one 8-bit data port and one
- 4-bit control/data port.
- The 8-bit data port can be either input or output.
- Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definitions

$\overline{\text{STB}}$ (Strobe Input): A LOW on this input loads data into the input latch.

IBF (Input Buffer Full F/F): A HIGH on this output indicates that the data has been loaded into the input latch. IBF is set by the $\overline{\text{STB}}$ input being low and is reset by the rising edge of the $\overline{\text{RD}}$ input.

INTR (Interrupt Request): A HIGH on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{\text{STB}}$ being a ONE, IBF is a ONE and INTE is a ONE. It is reset by the falling edge of $\overline{\text{RD}}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A Controlled by bit set/reset of PC_4

INTE B Controlled by bit set/reset of PC_2

Output Control Signal Definition

$\overline{\text{OBF}}$ (Output Buffer Full F/F): The $\overline{\text{OBF}}$ output will go LOW to indicate that the CPU has written data out to the specified port. The $\overline{\text{OBF}}$ F/F will be set by the rising edge of the $\overline{\text{WR}}$ input and reset by the $\overline{\text{ACK}}$ Input being low.

$\overline{\text{ACK}}$ (Acknowledge Input): A LOW on this input informs the CA82C55A that the data from Port A or Port B has been accepted. (i.e. a response from the peripheral device indicating that it has received the data output by the CPU).

I**NTR (Interrupt Request)**: A HIGH on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{\text{ACK}}$ is a ONE, $\overline{\text{OBF}}$ is a ONE and INTE is a ONE. It is reset by the falling edge of $\overline{\text{WR}}$.

INTE A Controlled by bit set/reset of PC_6

INTE B Controlled by bit set/reset of PC_2

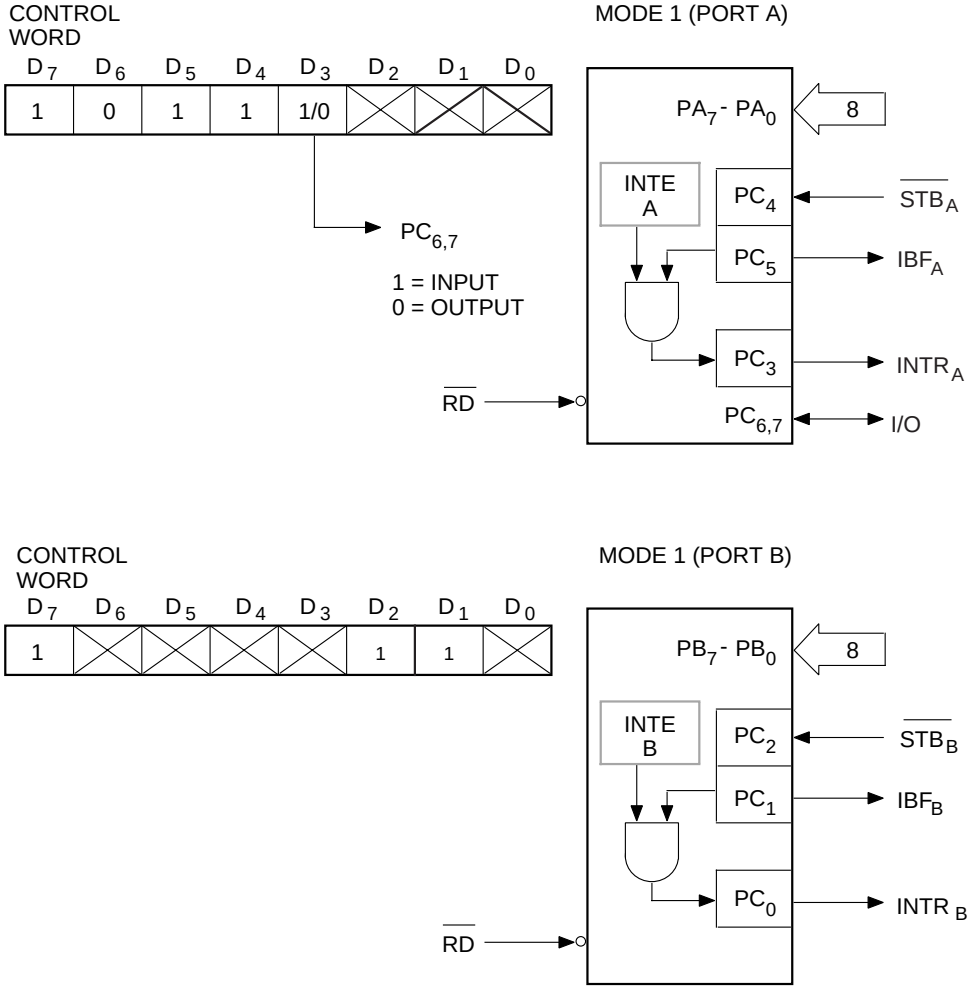


Figure 2-12: Mode 1 Input

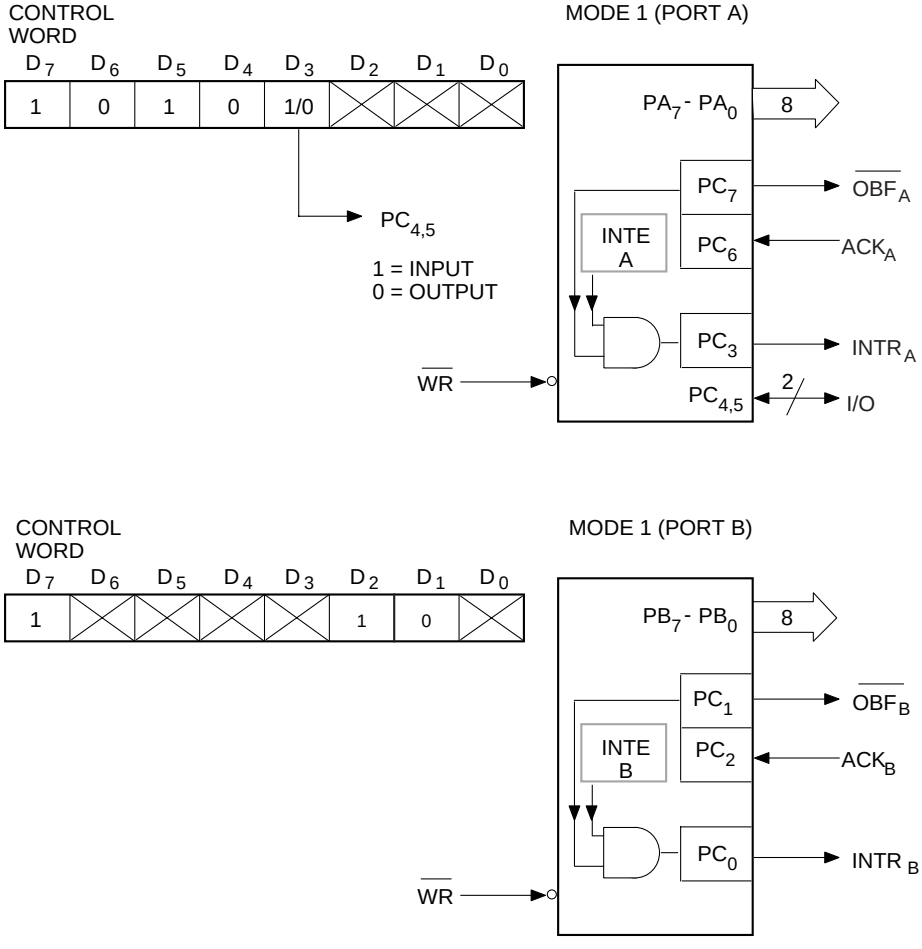


Figure 2-13: Mode 1 Output

Mode 2 (Strobed Bi-directional Bus I/O)

This mode provides a means for communicating with a peripheral device or a structure on a single 8-bit bus to facilitate both the transmitting and the receiving of data

(bi-directional bus I/O). Handshaking signals maintain proper bus flow discipline in a similar manner to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definition:

- Used in Group A only.
- One 8-bit, bi-directional bus port (Port A) and a 5-bit control port (Port C).
- Both inputs and outputs are latched.

The 5-bit control port (Port C) is used for control and status of the 8-bit, bi-directional bus port (Port A).

Bi-directional Bus I/O Control Signal Definition

INTR (Interrupt Request): A HIGH on this output can be used to interrupt the CPU for input or output operations.

Output Operations

$\overline{\text{OBF}}$ (Output Buffer Full): The $\overline{\text{OBF}}$ output will go LOW to indicate that the CPU has written data out to Port A.

$\overline{\text{ACK}}$ (Acknowledge): A LOW on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with $\overline{\text{OBF}}$): Controlled by bit set/reset of PC_6.

Input Operations

$\overline{\text{STB}}$ (Strobe Input): A LOW on this input loads data into the input latch.

IBF (Input Buffer Full F/F): A HIGH on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF): Controlled by bit set/reset of PC_4.

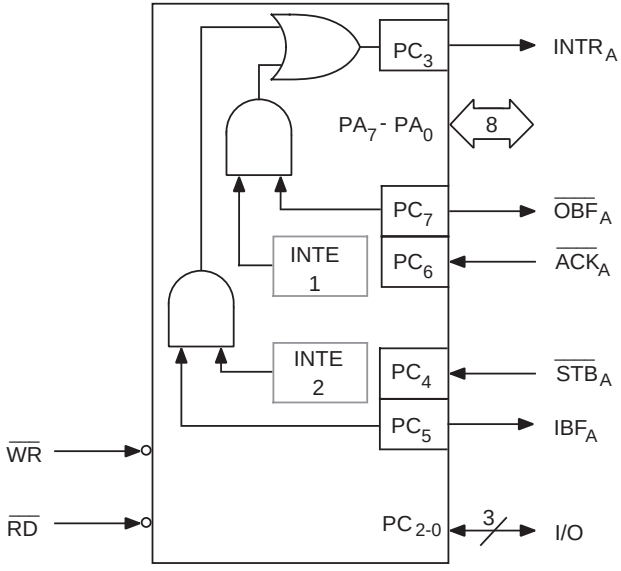


Figure 2-14: Mode 2

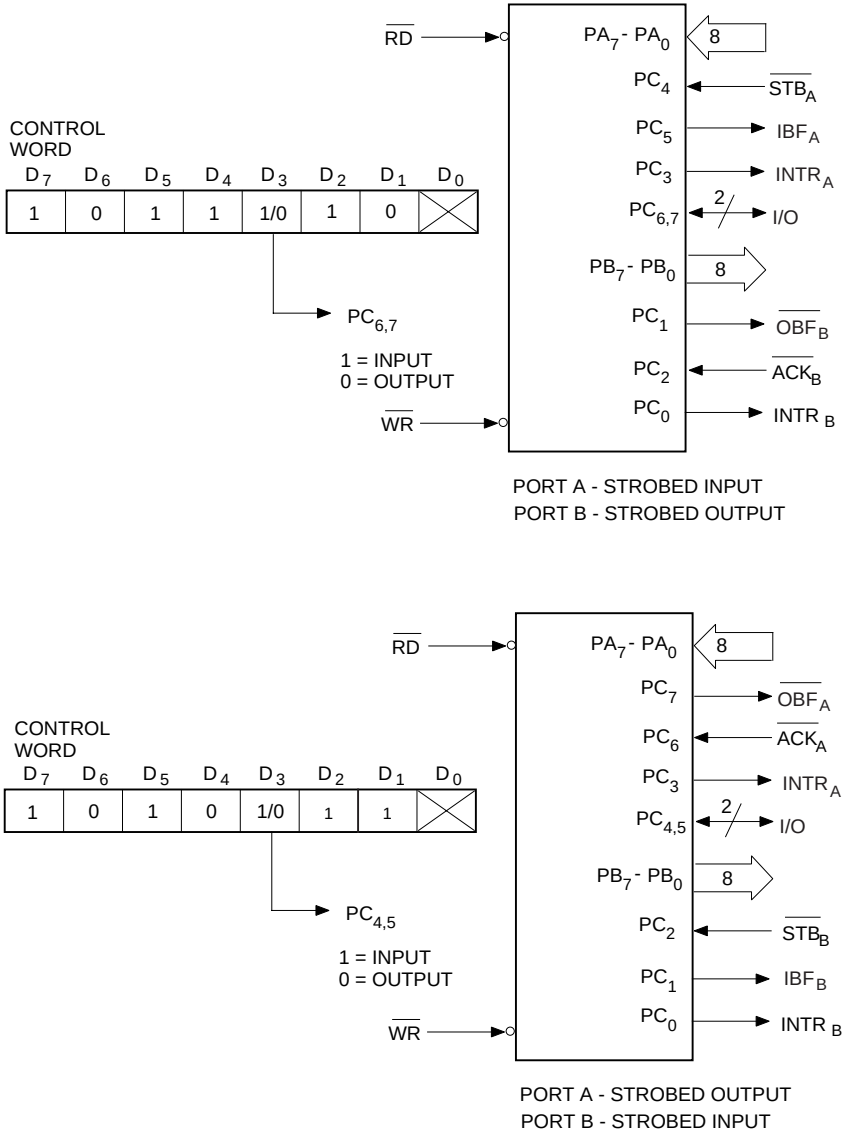


Figure 2-15: Combinations of Mode 1

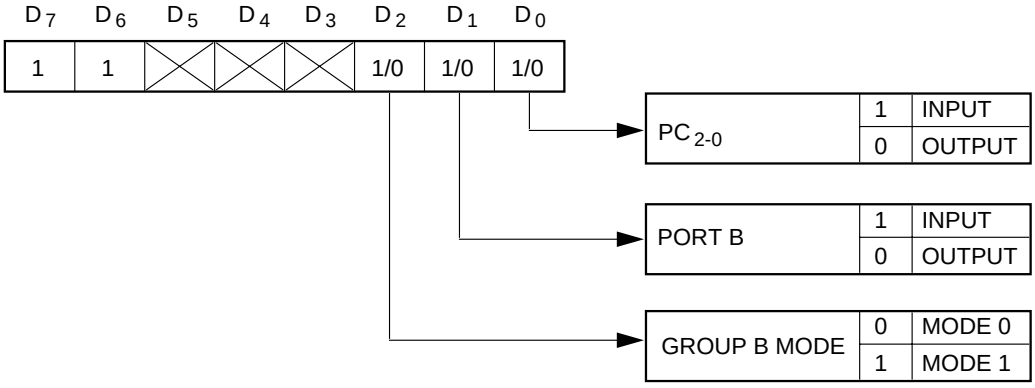


Figure 2-16: Mode Control Word

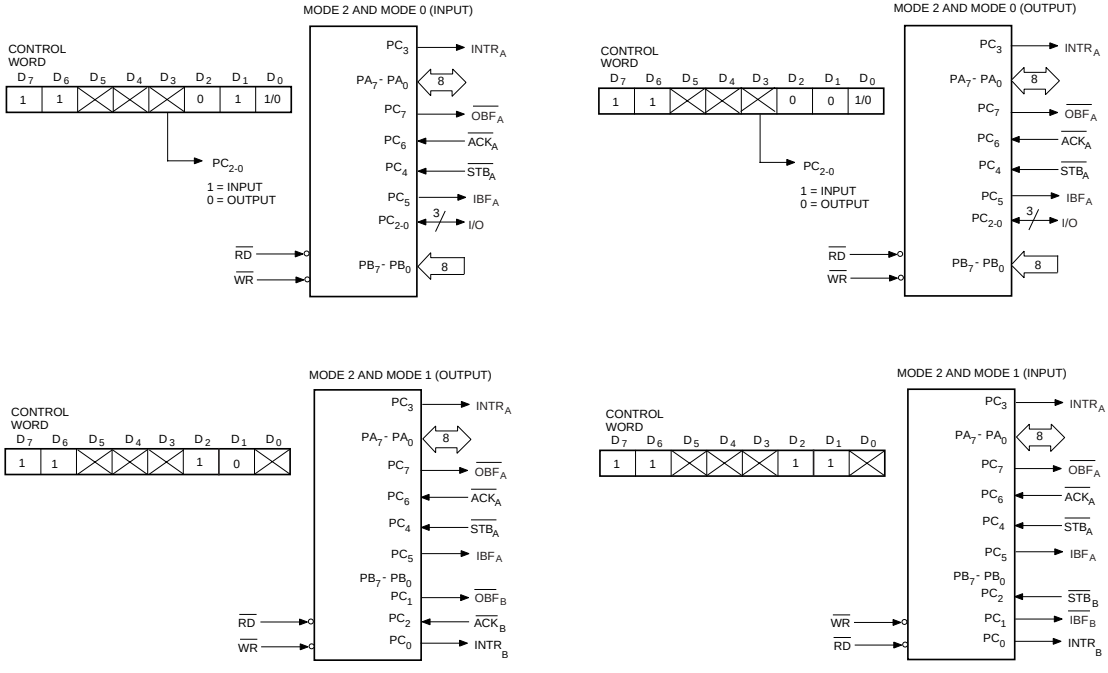


Figure 2-17: Mode 1/4 Combinations

Table 2-8: Mode Definition Summary

PORT		MODE 0	MODE 1				MODE 2
PORT A	PA_0 PA_1 PA_2 PA_3 PA_4 PA_5 PA_6 PA_7	All IN or All OUT	All IN or All OUT				All BI-DIRECTIONAL
PORT B	PB_0 PB_1 PB_2 PB_3 PB_4 PB_5 PB_6 PB_7	All IN or All OUT	All IN or All OUT				Not Used in MODE 2
			A IN, B IN	A IN, B OUT	A OUT, B IN	A OUT, B OUT	
PORT C	PC_0 PC_1 PC_2 PC_3 PC_4 PC_5 PC_6 PC_7	All IN or All OUT	$INTR_B$ IBF_B $\overline{STB}_B$ $INTR_A$ $\overline{STB}_A$ IBF_A I/O I/O	$INTR_B$ $\overline{OBF}_B$ $\overline{ACK}_B$ $INTR_A$ $\overline{STB}_A$ IBF_A I/O I/O	$INTR_B$ IBF_B $\overline{STB}_B$ $INTR_A$ I/O $\overline{I/O}$ $\overline{ACK}_A$ $\overline{OBF}_A$	$INTR_B$ $\overline{OBF}_B$ $\overline{ACK}_B$ $INTR_A$ I/O $\overline{I/O}$ $\overline{ACK}_A$ $\overline{OBF}_A$	I/O I/O I/O $INTR_A$ $\overline{STB}_A$ $\overline{OBF}_A$ $\overline{ACK}_A$ OBF_A

Special Mode Combination Considerations

Several combinations of modes are possible. For any combination, some or all of the Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a Set Mode command.

The state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus during a read of Port C. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC_2, PC_4, and PC_6 bit positions as shown in Table 2-9.

Through a Write Port C command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a Write Port C command, and the interrupt enable flags cannot be accessed. The Set/Reset Port C Bit command must be used to write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag.

With a Set/Reset Port C Bit command, any Port C line programmed as an output (including INTR, IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, are not affected by a Set/Reset Port C Bit command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the Set/Reset Port C Bit command will affect the Group A and Group B interrupt enable flags (see Table 2-9).

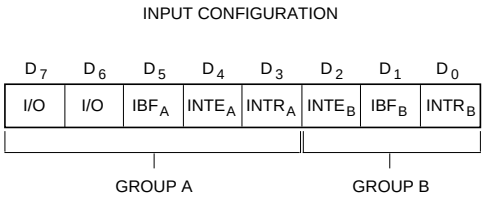
Current Drive Capability

Any output on Port A, B or C can sink or source 2.5 mA. Thus the CA82C55A can directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the CA82C55A is in Modes 1 or 2, Port C generates or accepts handshaking signals with the peripheral device. Reading Port C allows the programmer to test or verify the status of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. This function is performed by executing a normal read operation of Port C.



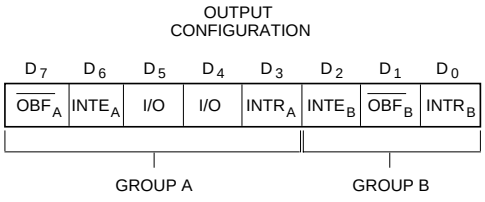


Figure 2-18: Mode 1 Status Word Format

(Defined by Mode 0 or Mode 1 Selection)

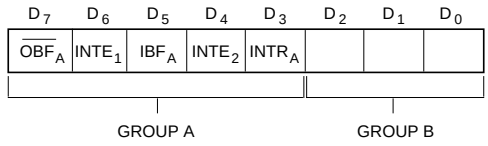


Figure 2-19: Mode 2 Status Word Format

Table 2-9: Interrupt Enable Flags In Modes 1 and 2

Interrupt Enable Flag	Position	Alternate Port C Pin Signal (Mode)
$INTE_B$	PC_2	$\overline{ACK}_B$ (Output Mode 1) or $\overline{STB}_B$ (Input Mode 1)
$INTE_{A2}$	PC_4	$\overline{STB}_A$ (Input Mode 1 or Mode 2)
$INTE_{A1}$	PC_6	$\overline{ACK}_A$ (Output Mode 1 or Mode 2)

APPLICATIONS

The CA82C55A is a very powerful device for interfacing peripheral equipment to the microcomputer system. It is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a service routine associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the CA82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the interface characteristics of the I/O device for both data transfer and timing, and matching this information to the examples and tables in the Operational Description, a control word can easily be developed to initialize the CA82C55A to exactly fit the application. Figure 2-20 to Figure 2-26 illustrate a few examples of typical CA82C55A applications.

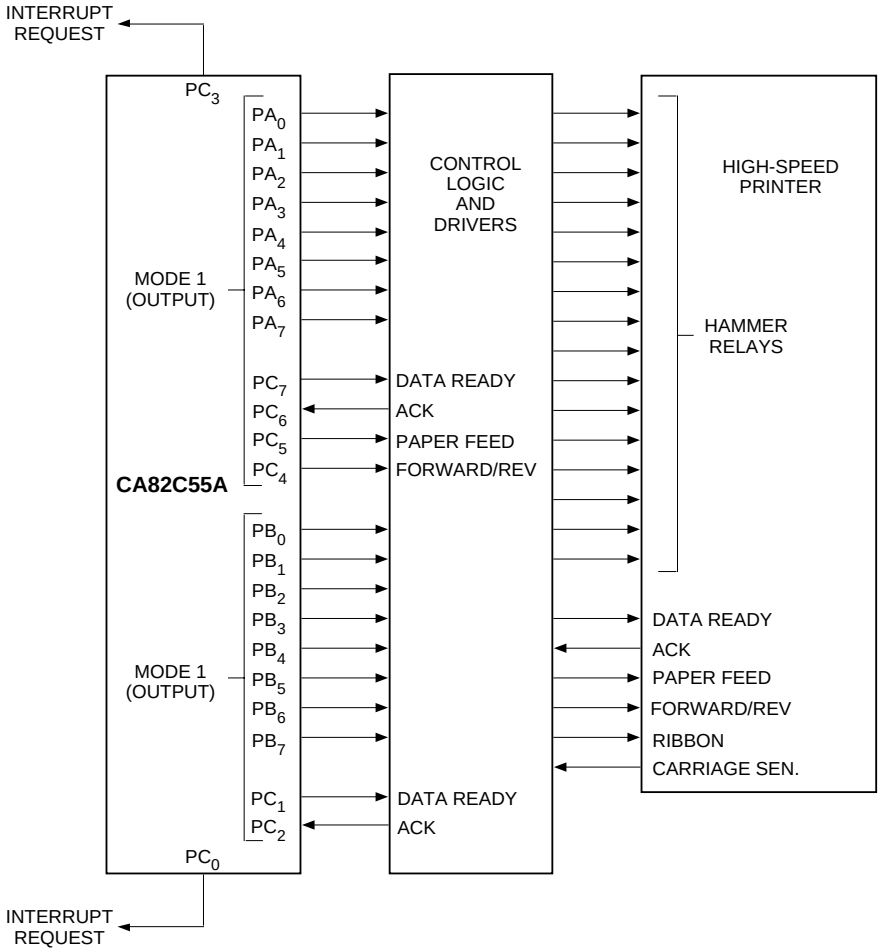


Figure 2-20: Printer Interface

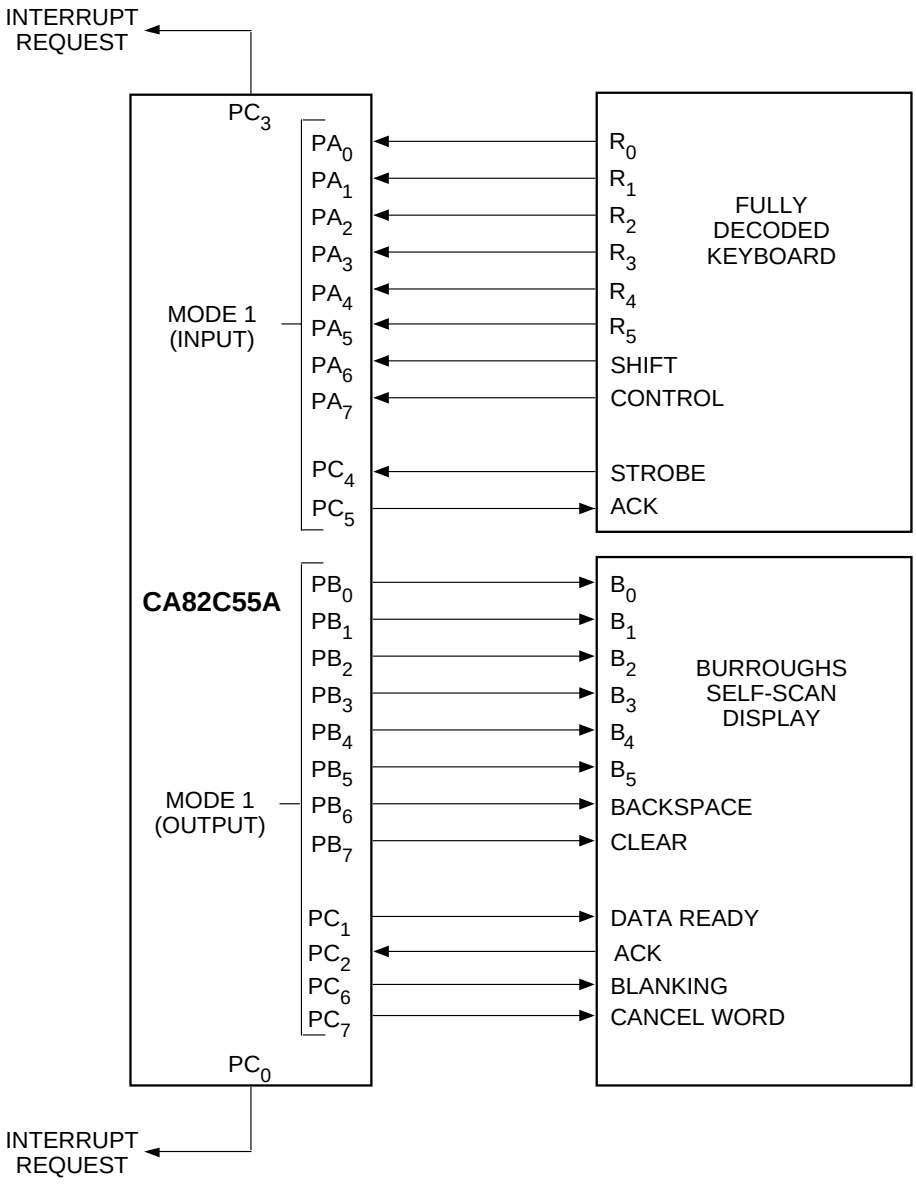


Figure 2-21: Keyboard and Display Interface

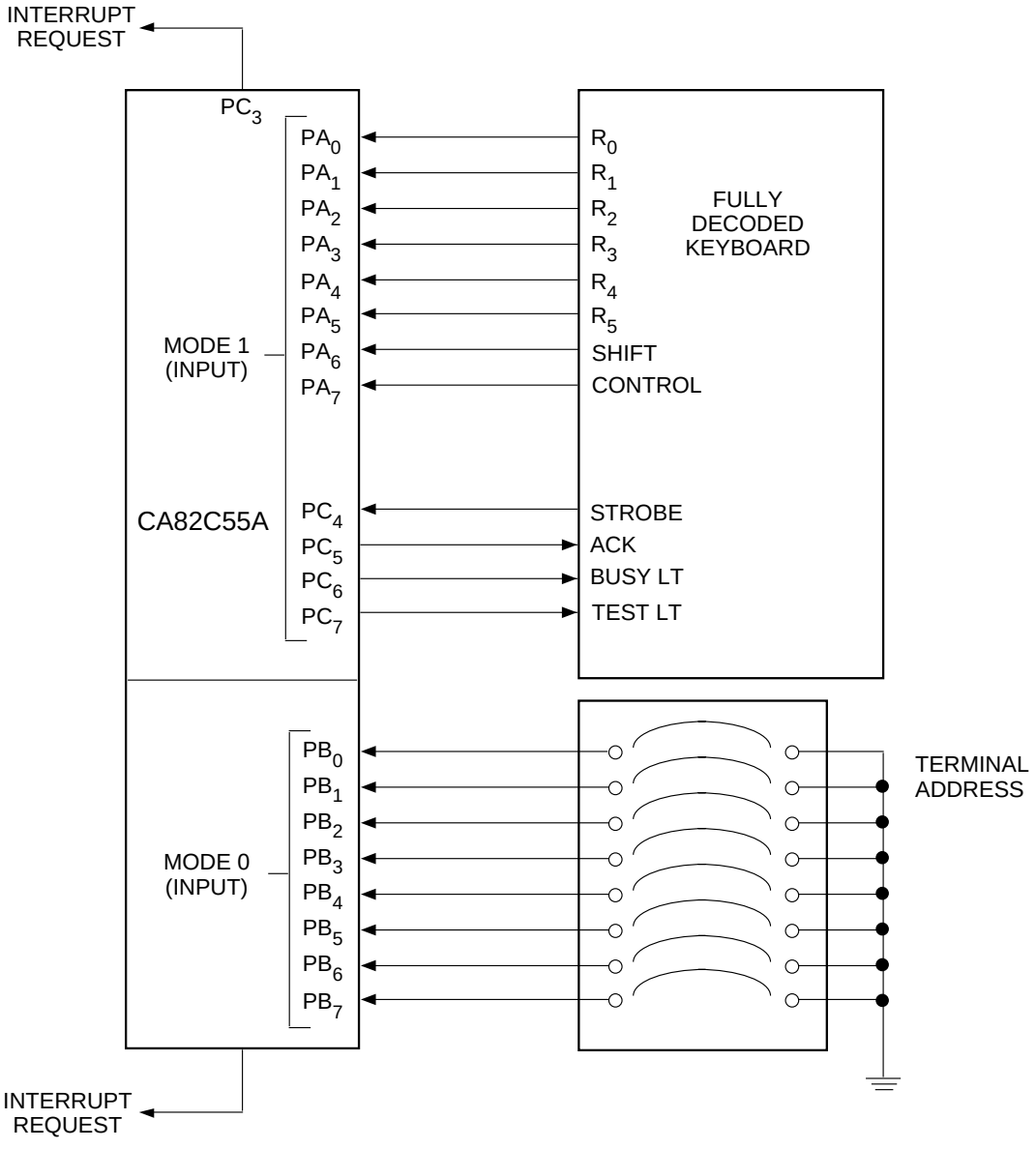


Figure 2-22: Keyboard and Terminal Address Interface

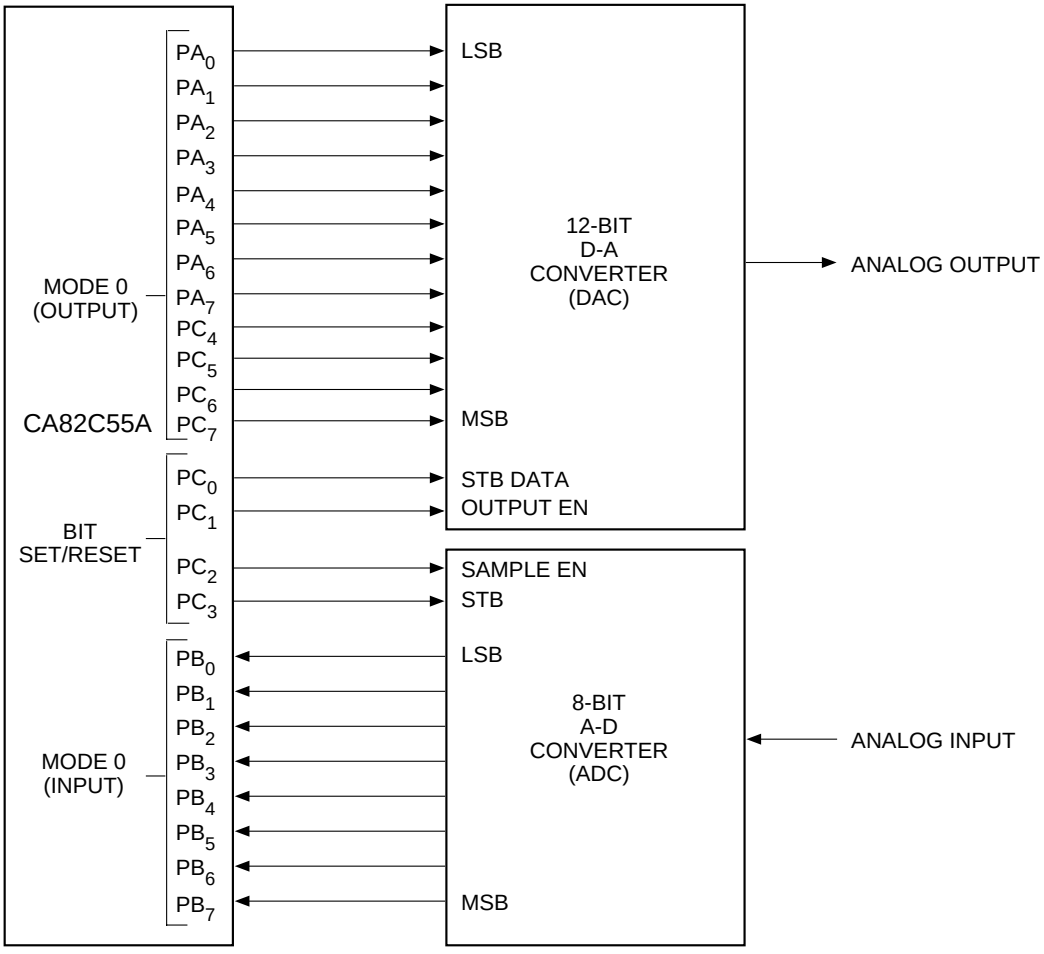


Figure 2-23: Digital to Analog, Analog to Digital

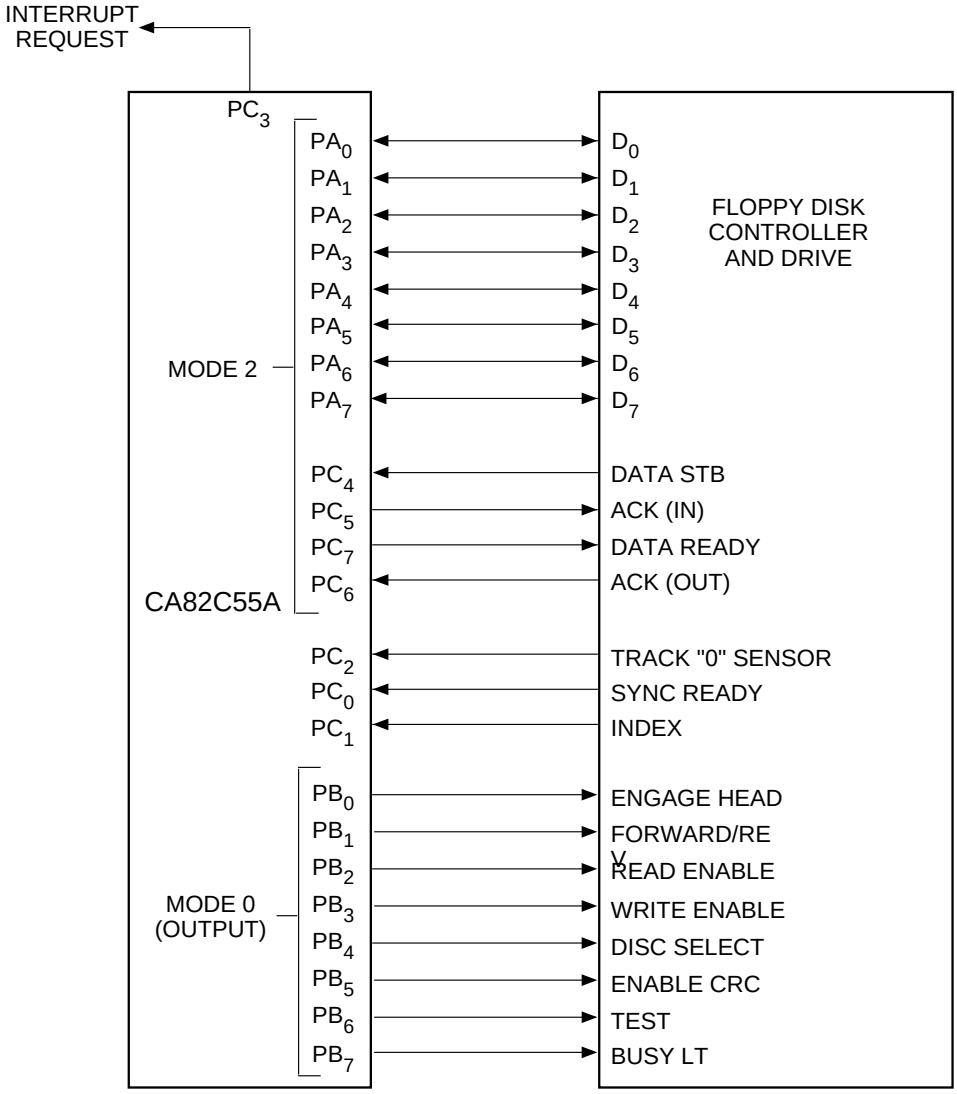


Figure 2-24: Basic CRT Controller Interface

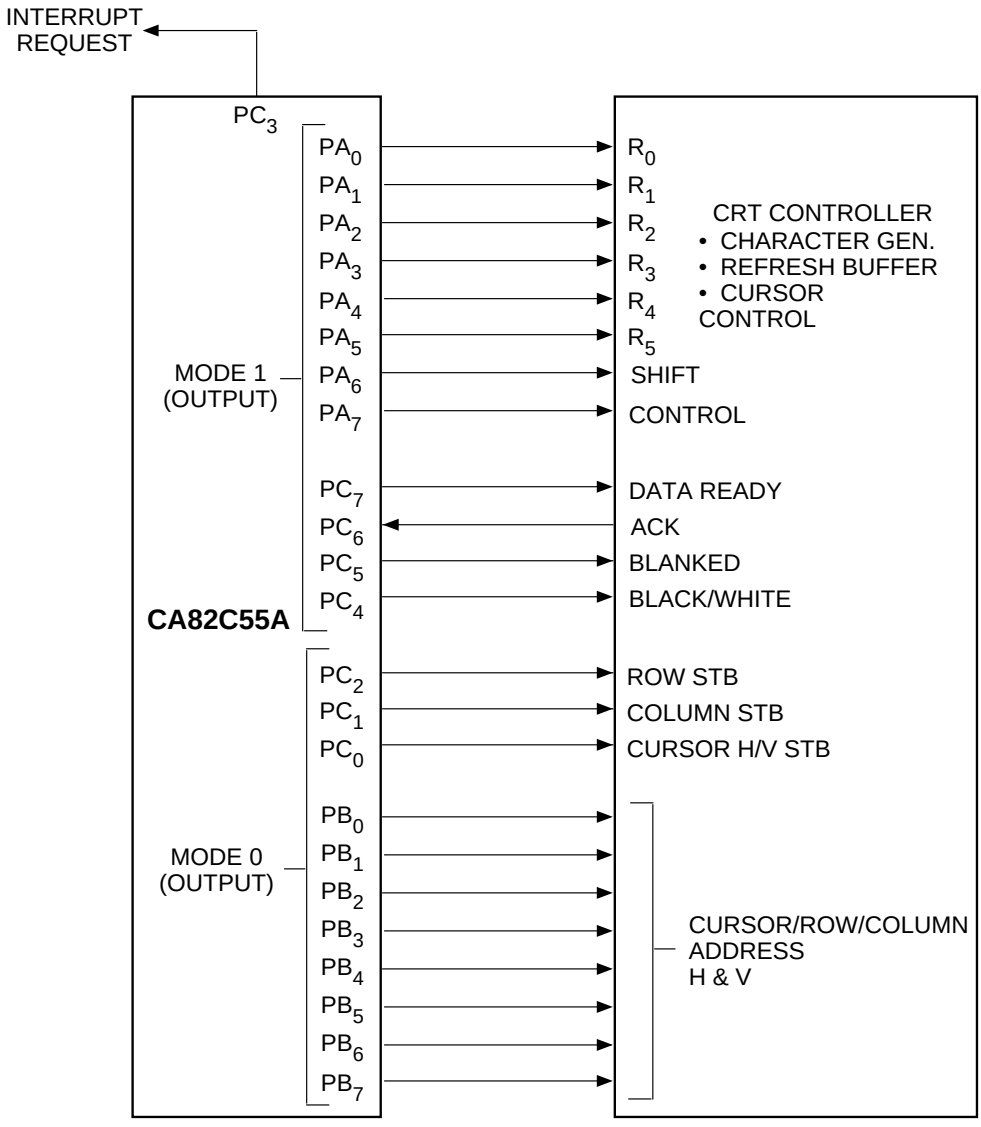


Figure 2-25: Basic Floppy Disk Interface

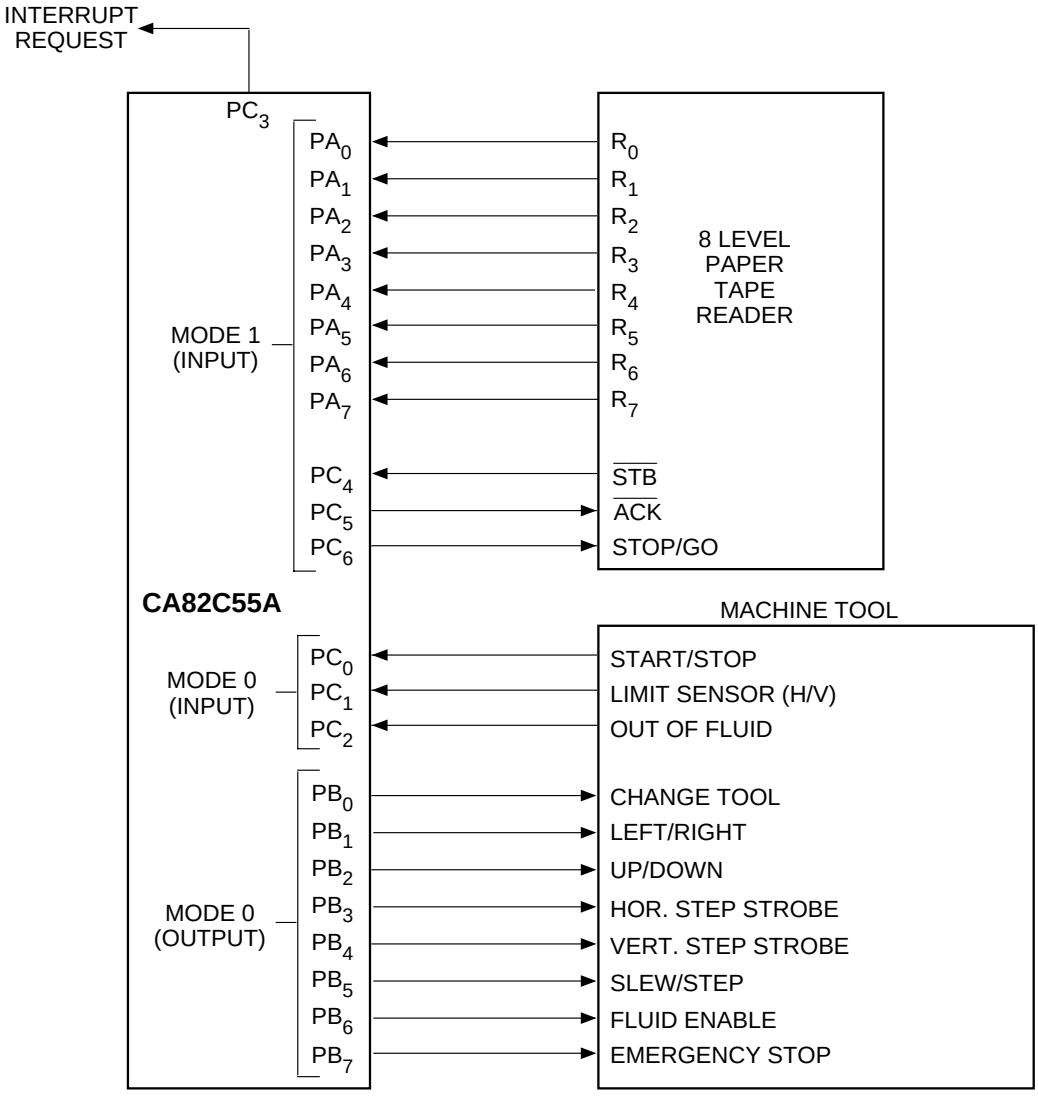


Figure 2-26: Machine Tool Controller Interface

CA82C59A

PROGRAMMABLE INTERRUPT CONTROLLER

- **Pin and functional compatibility with the industry standard 8259/8259A**
- **Fully static, high speed design (10 & 8 MHz)**
- **Compatible with 8080/85, 8086/88, 80286/386 and 68000 family microprocessor systems**
- **TTL input/output compatibility**
- **Low power CMOS implementation**
- **Eight level priority controller**
- **Expandable to 64 levels**
- **Programmable interrupt modes, with each interrupt maskable**
- **Edge- or level-triggered interrupt request inputs**
- **Polling operation**

The Tundra CA82C59A is a high performance, completely programmable interrupt controller. It can process eight interrupt request inputs, assigning a priority level to each one, and is cascadable up to 64 interrupt requests. Individual interrupting sources are maskable. Its two modes of operation (Call and Vector) allow it to be used with virtually all 8000 and 80000 type processors, as well as with the 68000 family of microprocessors.

Featuring fully static, very high speed operation, the CA82C59A is designed to relieve the system CPU from polling in a multi-level priority interrupt system.

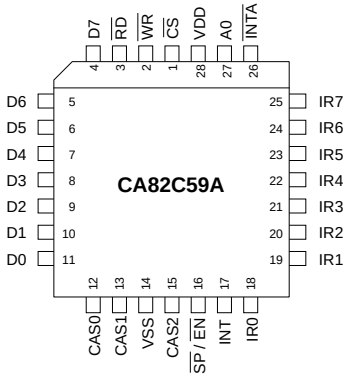


Figure 2-1: PLCC Pin Configurations

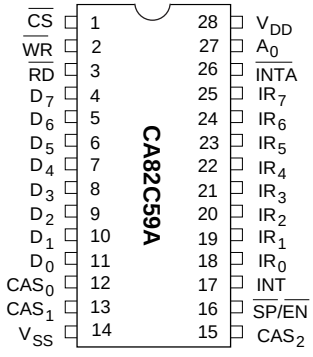


Figure 2-2: PDIP/SOIC Pin Configurations

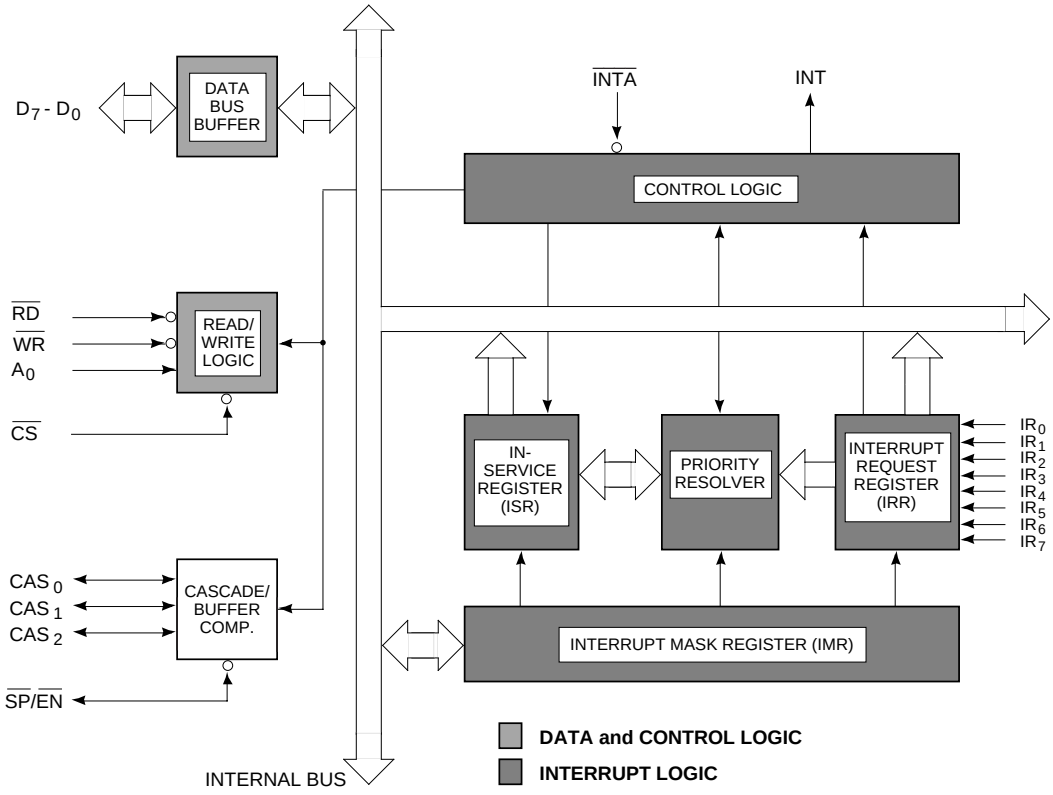


Figure 2-3: CA82C59A Block Diagram

Table 2-1: Pin Descriptions

Symbol	Pins		Type	Name and Function
	PLCC	PDIP		
A_0	27	27	I	It is used by the CA82C59A to decipher various command words written by the CPU, and Status information read by the CPU. It is typically connected to the CPU - A_0 address line.
CAS_{0-2}	12, 13, 15	12, 13, 15	I/O	Cascade Line: These signals are outputs for the master CA82C59A, and inputs for slaved CA82C59As. The CAS lines are used as a private bus by a CA82C59A master to control a multiple CA82C59A system structure.
$\overline{CS}$	1	1	I	Chip Select: An active LOW signal used to enable $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the CA82C59A. Note that $\overline{INTA}$ functions are independent of $\overline{CS}$.
D_7 - D_0	4 - 11	4 - 11	I/O	Data Bus: Bi-directional, tri-state, 8-bit data bus for the transfer of control, status and interrupt vector information.
INT	17	17	O	Interrupt: This signal goes HIGH when a valid interrupt request is asserted. It is used to interrupt the CPU, and is thus connected to the CPU interrupt pin.
$\overline{INTA}$	26	26	I	Interrupt Acknowledge: Signal used to enable the CA82C59A interrupt vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
IR_{0-7}	18 - 25	18 - 25	I	Interrupt Requests: Asynchronous input signals, an interrupt request is executed by raising an IR input (LOW to HIGH), and holding it HIGH until it is acknowledged (Edge Triggered Mode), or just by a HIGH level on an IR input (Level Triggered Mode).
$\overline{RD}$	3	3	I	Read: Active LOW signal used to enable the CA82C59A to output status information onto the data bus for the CPU, when CS is LOW.
$\overline{SP}/\overline{EN}$	16	16	I/O	Slave Program/Enable Buffer: Active LOW, dual function control signal. When in the Buffered Mode, it can be used as an output to control buffer transceivers ($\overline{EN}$). When not in the buffered mode it can be used as an input to designate a master (SP = 1) or a slave (SP = 0).
V_{DD}	28	28	-	Power: 5 v ± 10% DC Supply
V_{SS}	14	14	-	Ground: 0 v
$\overline{WR}$	2	2	I	Write: Active LOW signal used to enable the CA82C59A to accept command words from the CPU, when $\overline{CS}$ is LOW.

FUNCTIONAL DESCRIPTION

The CA82C59A Programmable Interrupt Controller is designed for use in interrupt driven micro-computer systems. Acting as an overall peripherals manager, its functions include:

- Accepting interrupt requests from assorted peripheral devices
- Determining which is the highest priority
- Establishing whether or not the new interrupt is of a higher priority than any interrupts which might be currently being serviced, and if so,
- Issuing an interrupt to the CPU
- Then providing the CPU with the interrupt service routine address of the interrupting peripheral

Each peripheral device usually has a specific interrupt service routine which is particular to its operational or functional requirements within the system. The CA82C59A can be programmed to hold a pointer to the service routine addresses associated with each of the peripheral devices under its control. Thus when a peripheral interrupt is passed through to the CPU, the CA82C59A can set the CPU Program Counter to the interrupt service routine required. These pointers (or vectors) are addresses in a vector table.

The CA82C59A is intended to run in one of two major operational modes, according the type of CPU being used in the system. The CALL Mode is used for 8085 type microprocessor systems, while the VECTOR Mode is reserved for those systems using more sophisticated processors such as the 8088/86, 80286/386 or 68000 family.

In either mode, the CA82C59A can manage up to eight interrupt request levels individually, with a maximum capability of up to 64 interrupt request levels when cascaded with other CA82C59As. A selection of priority modes is also available such that interrupt requests can be processed in a number of different ways to meet the requirements of a variety of system configurations.

Priority modes can be changed or reconfigured dynamically at any time during system operation using the operation command words (OCWs), allowing the overall interrupt structure to be defined for a complete system. Note that the CA82C59A is programmed by the system software as an *I/O peripheral.*

The major functional components of the CA82C59A are laid out in the block diagram of Figure 2-3. Vector data and device programming information are transferred from the system bus to the CA82C59A via the 3-state, bi-directional Data Bus Buffer which is connected to the internal bus of the controller. Control data between the CA82C59A and the CPU, and between master and slave CA82C59A devices, is managed by one of three functional blocks:

- The Read/Write Control block processes CPU initiated reads and writes to the CA82C59A registers
- The Control Logic block receives and generates the signals that control the sequence of events during an interrupt
- The Cascade Control block is used to operate a private bus (CAS_0 - CAS_2) connecting master and slave CA82C59As in those systems having cascaded CA82C59As.

Programming data passed over the system bus is saved in the Initialization and Command Word Registers. Note that the contents of these registers cannot be read back by the CPU.

Peripheral interrupt requests (IR_0 - IR_7) are handled by the functional blocks comprising the Interrupt Request Register (IRR), the Interrupt Mask Register (IMR), the In-Service Register (ISR) and the Priority Decision Logic block. Interrupt requests are received at the IRR, the IMR masks those interrupts which cannot be accepted by the CA82C59A, and the ISR shows those interrupt requests which are currently being processed. These three registers can all be read by the CPU under software control. The Priority Decision Logic block determines which interrupt will be processed next according to a variety of indicators which include the current priority, mode status, current interrupt mask and interrupt service status.

The actual operation of the CA82C59A and its many modes are described in the section following device specifications and characteristics.

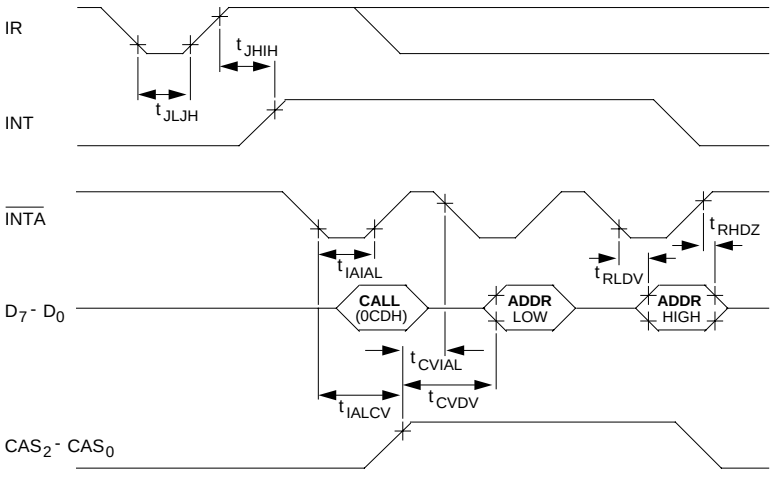
Table 2-2: AC Characteristics (T_A = -40° to +85°C, V_{DD} = 5V ± 10%)

Symbol	Parameter	Test Conditions	Limits (8 MHz)		Limits (10 MHz)		Units
			Min	Max	Min	Max	
t_{AHDV}	Data valid from stable address	Note 5	-	200	-	160	ns
t_{AHRL}	A_0 / $\overline{CS}$ setup to $\overline{RD}$/$\overline{INTA}$ ↓		5	-	5	-	ns
t_{AHWL}	A_0 /$\overline{CS}$ setup to $\overline{WR}$ ↓		5	-	5	-	ns
t_{CHCL}	End of Command to next Command (Not same command type) End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence (same as t_{RV2})	Note 1	200	-	160	-	ns
t_{CVDV}	Cascade valid to valid data	Note 5	-	200	-	130	ns
t_{CVIAL}	Cascade setup to second or third $\overline{INTA}$ ↓ (slave only)	Slave	40	-	30	-	ns
t_{DVWH}	Data setup to $\overline{WR}$ ↑	160	-	100	-	ns	
t_{IAIAH}	$\overline{INTA}$ pulse width HIGH	$\overline{INTA}$ Sequence	160	-	100	-	ns
t_{IAIAL}	$\overline{INTA}$ pulse width LOW	160	-	100	-	ns	
t_{IALCV}	Cascade valid from first $\overline{INTA}$ ↓ (master only)	Note 5	-	260	-	160	ns
t_{JHIH}	Interrupt output delay	Note 5	-	200	-	120	ns
t_{JLJH}	Interrupt request width (LOW)1	Note 2	100	-	100	-	ns
t_{RHAX}	A_0 / $\overline{CS}$ hold after $\overline{RD}$/ $\overline{INTA}$ ↑	0	-	0	-	ns	
t_{RHDZ}	Data float after $\overline{RD}$/ $\overline{INTA}$ ↑	Note 6	10	85	10	65	ns
t_{RHEH}	Enable inactive from $\overline{RD}$ ↑ or $\overline{INTA}$ ↑	Note 5	-	50	-	50	ns
t_{RHRL}	End of $\overline{RD}$ to next $\overline{RD}$ End of INTA to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only		160	-	100	-	ns
t_{RLDV}	Data valid from $\overline{RD}$/ $\overline{INTA}$ ↓	Note 5	-	120	-	95	ns
t_{RLEL}	Enable active from $\overline{RD}$↓ or $\overline{INTA}$ ↓	Note 5	-	100	-	70	ns
t_{RLRH}	$\overline{RD}$ pulse width	160	-	100	-	ns	
t_{RV1}	Command recovery time	Note 3	200	-	100	-	ns
t_{RV2}	$\overline{INTA}$ recovery time	Note 4	200	-	100	-	ns
t_{WHAX}	A_0 / $\overline{CS}$ hold after $\overline{WR}$ ↑	0	-	0	-	ns	
t_{WHDX}	Data hold after $\overline{WR}$ ↑	0	-	0	-	ns	
t_{WHWL}	End of $\overline{WR}$ to next $\overline{WR}$	160	-	100	-	ns	
t_{WLWH}	$\overline{WR}$ pulse width	160	-	100	-	ns	

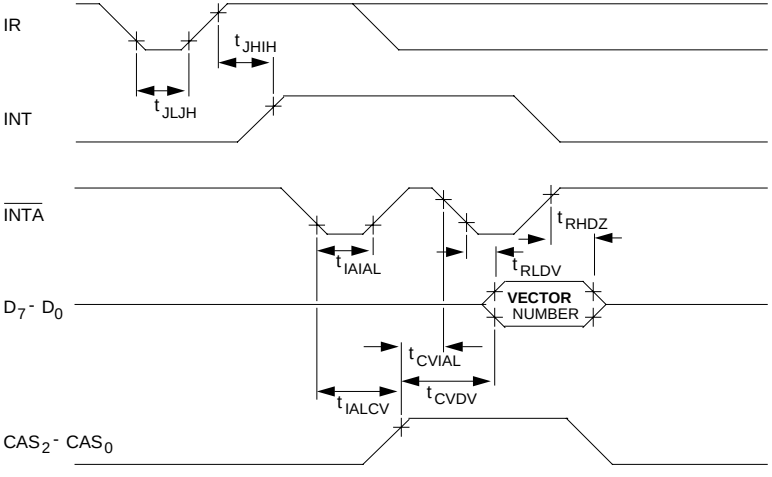
Notes:
1. The time to move $\overline{INTA}$ to/from command (read/write).
2. The time to clear the input latch in edge-triggered mode.
3. The time to move from read to write operation.
4. The time to move to the next $\overline{INTA}$ operation.
5. See Figure 2-6, Note 5 for load circuit values.
6. See Figure 2-6, Note 6 for load circuit values.

Figure 2-4: Timing Diagrams

a) Interrupt Cycle (CALL Mode)

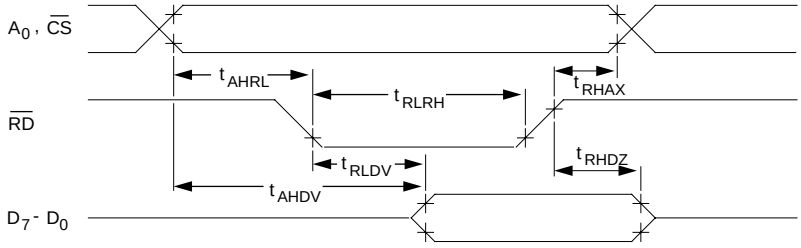


b) Interrupt Cycle (VECTOR Mode)

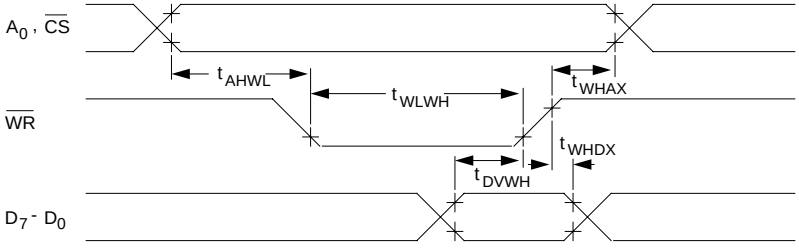


Note that IR input should remain at a high level until the leading edge of the first INTA pulse.

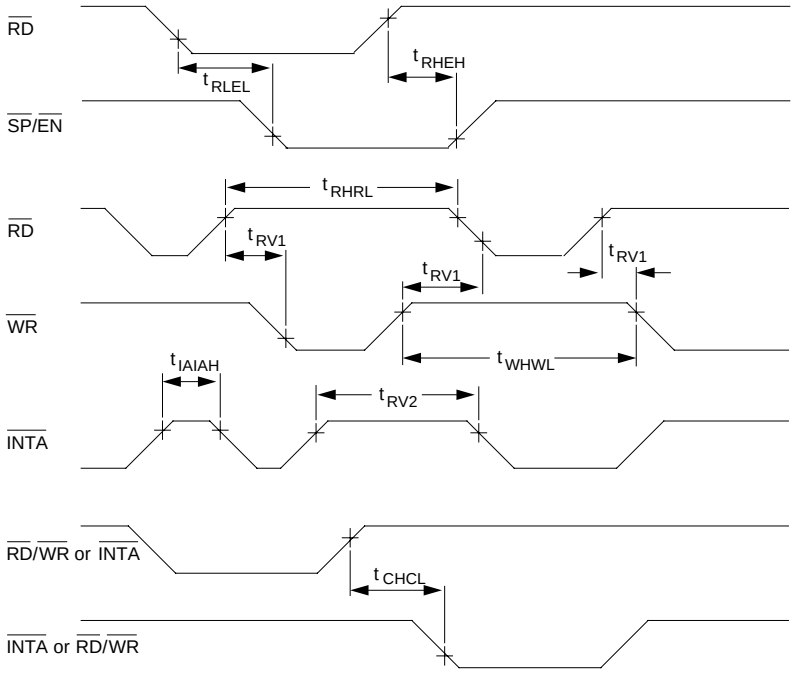
c) Read Cycle

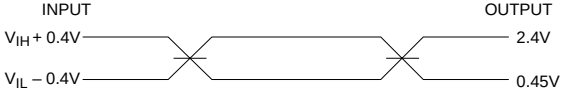


d) Write Cycle



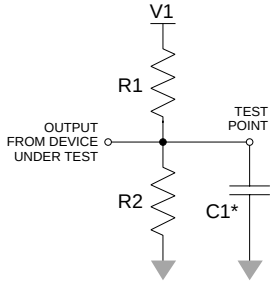
e) Other Timing





AC Testing: All input signals must switch between V_{IL} - 0.4V and V_{IH} + 0.4V. Input rise and fall times must be ≤ 15 ns. All timing measurements are made at 2.4V and 0.45V.

Figure 2-5: AC Testing I/O Waveforms



Note	V1	R1	R2	C1
5	1.7V	523 Ω	open	100pf
6	4.5V	1.8k Ω	1.8k Ω	30pf

*Includes stray and jig capacitance

Figure 2-6: AC Testing Load Circuit

Table 2-3: DC Characteristics (T_A = -40° to +85°C, V_{DD} = 5V ± 10%)

Symbol	Parameter	Test Conditions	Limit		Unit
			Min	Max	
I_{DD}	V_{DD} supply current		-	10	mA
I_{LI}	Input leakage current	0v ≤ VIN ≤ VDD	-1.0	+1.0	µA
I_{LIR}	IR input load current	V_{IN} = 0v V_{IN} = V_{DD}	-	-300 10	µA µA
I_{LOL}	Output leakage current	0v ≤ V_{OUT} ≤ VDD	-10.0	+10.0	µA
V_{IH}	Input HIGH voltage	Note 1	2.0	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage	Note 1	-0.3	0.8	V
V_{IHS}	Schmitt Trigger Input High Voltage	Note 2	2.1	V_{DD} + 0.3	V
V_{ILS}	Schmitt Trigger Input Low Voltage	Note 2	-0.3	0.7	V
V_{HY}	Schmitt Trigger Hysteresis	Note 2	-	0.4	V
V_{OH}	Output HIGH voltage	I_{OH} = -2.5 mA I_{OH} = -100 µA	3.0 V_{DD} - 0.4	-	V V
V_{OL}	Output LOW voltage	I_{OL} = +2.5 mA	-	0.4	V

Note 1: Applies to pins IR_7 -IR_0, D_7 - D_0, CAS_{2-0}, $\overline{SP}/\overline{EN}$
Note 2: Applies to pins $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{INTA}$, A_0

Table 2-4: Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0V, V_{IN} = +5 V or V_{SS})

Symbol	Parameter	Test Conditions	Min	Max	Units
$C_{I/O}$	I/O Capacitance	FREQ = 1 MHz Unmeasured pins returned to V_{SS}	-	15	pF
C_{IN}	Input Capacitance		-	10	pF
C_{OUT}	Output Capacitance		-	10	pF

Table 2-5: Recommended Operating Conditions

DC Supply Voltage		+4.5 V to +5.5 V
Operating Temperature Range	Commercial	0°C to +70°C
	Industrial	-40°C to +85°C

Table 2-6: Absolute Maximum Ratings

DC Supply Voltage	-.03 to +7.0 V
Input, Output or I/O Voltage Applied	V_{SS} - 0.3 V to V_{DD} + 0.3 V
Storage Temperature Range	-55°C to +150°C
Maximum Package Power Dissipation	1 W
Input Pin Current (@ 25°C)	-10.0 mA to +10.0 mA
Lead Temperature (soldering: 10 sec.)	300°C

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

OPERATIONAL DESCRIPTION

The CA82C59A is designed to operate in one of two mutually exclusive modes, selected according to the type of system processor used; **Call Mode** for 8080/85 type processors, and **Vector Mode** for 8088/86 and 80286/386 type processors. The major difference between these two modes is the way in which interrupt service routine address data is passed to the system CPU. Unless specifically programmed to the contrary, the CA82C59A defaults to the CALL Mode of operation, (see section on Programming).

Call Mode

In CALL mode, the interrupt service routine address is passed in two steps, (first the lower byte of the address, followed by the upper byte), in response to three Interrupt Acknowledge ($\overline{INTA}$) signals sent by the CPU to the CA82C59A. In a system containing a single Interrupt Controller, the sequence of steps to respond to a peripheral interrupt request is outlined below, and shown graphically in Figure 2-7. The interrupt service routine addresses are loaded into the CA82C59A during the initialization procedures.

Step	Event Sequence
3)	One or more interrupt request lines (IR_0 - IR_7) are raised HIGH, setting corresponding IRR bits.
4)	The requests are evaluated by the CA82C59A, and if their priority is high enough, or if they are not masked, an INT signal is sent to the CPU.
5)	The CPU acknowledges the INT with an interrupt acknowledge ($\overline{INTA}$).
6)	On receipt of the $\overline{INTA}$, the CA82C59A sets the highest priority ISR bit, and resets the corresponding IRR bit. In addition, the CA82C59A sends a CALL instruction (0CDH) to the CPU via the data bus.
7)	The CALL instruction causes the CPU to send two more $\overline{INTA}$ signals to the CA82C59A.
8)	On receipt of the first of these two $\overline{INTA}$ signals, the CA82C59A sends the low order 8-bit address byte to the CPU via the data bus. On receipt of the second $\overline{INTA}$, the high order address byte is sent to the CPU.
9)	This completes the 3-byte CALL instruction procedure. The ISR bit is reset at the end of the interrupt sequence except in the Automatic EOI mode, where the ISR bit is reset automatically at the end of the third $\overline{INTA}$.

Vector Mode

In VECTOR mode, the interrupt service routine address is calculated by the CPU from a one byte interrupt vector supplied by the CA82C59A. The significant bits T_{7-3} of the interrupt vectors are loaded into the CA82C59A during the initialization procedures.

Note that no data is transferred by the CA82C59A to the CPU after the first $\overline{INTA}$ signal (the CA82C59A data bus buffers are disabled). It is similar to the CALL mode in that this cycle is used for internal operations that freeze the state of the interrupts for priority resolution or, in cascaded mode; to issue the interrupt code on the cascade lines (CAS_{0-2}) at the end of this cycle.

The sequence of steps that occur to respond to a peripheral interrupt request in Vector mode are outlined below and illustrated in Figure 2-10.

Step	Event Sequence
1)	One or more interrupt request lines (IR_0 - IR_7) are raised HIGH, setting corresponding IRR bits.
2)	The requests are evaluated by the CA82C59A, and if their priority is high enough, or if they are not masked, an INT signal is sent to the CPU.
3)	The CPU acknowledges the INT with an interrupt acknowledge ($\overline{INTA}$).
4)	After receipt of the first $\overline{INTA}$ signal from the CPU, the CA82C59A sets the highest priority ISR bit and resets the corresponding IRR bit. The CA82C59A data bus buffer is not active during this cycle (high impedance state).
5)	Following receipt of the second $\overline{INTA}$ signal generated by the CPU, the CA82C59A sends an 8-bit interrupt vector to the CPU via the data bus.
6)	This completes the 1-byte VECTOR mode procedure. In the Automatic End-of-Interrupt (AEOI) mode, the ISR bit is reset at the end of the second $\overline{INTA}$. In other EOI modes the ISR bit remains set until an appropriate EOI command is received after the end of the interrupt sequence.

The interrupt sequence procedures when several CA82C59As are cascaded together is shown for both CALL and VECTOR modes in Figure 2-9 and in Figure 2-12 respectively.

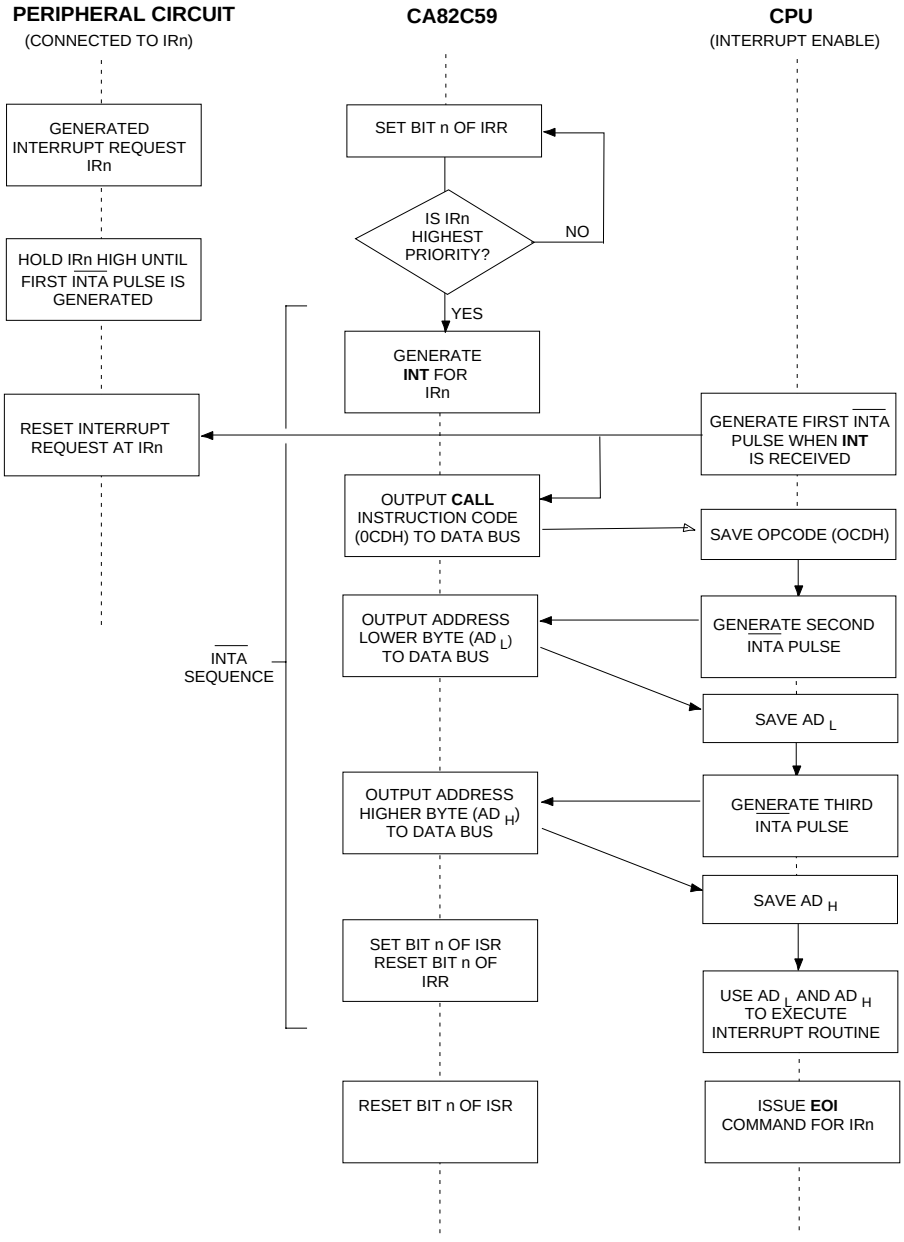


Figure 2-7: Call Mode Operation (Single CA82C59A Systems)

CONTENTS OF FIRST INTERRUPT VECTOR BYTE

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CALL CODE	1	1	0	0	1	1	0	1

The lower address of the appropriate service routine is enabled onto the data bus during the second $\overline{\text{INTA}}$ pulse. When the Interval = 4, bits A_5 - A_7 are programmed, and A_0 - A_4 are inserted automatically by the CA82C59A When the Interval = 8, bits A_6 and A_7 only are programmed, with A_0 - A_5 inserted automatically by the CA82C59A.

CONTENTS OF SECOND INTERRUPT VECTOR BYTE

IR	INTERVAL = 4							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
7	A_7	A_6	A_5	1	1	1	0	0
6	A_7	A_6	A_5	1	1	0	0	0
5	A_7	A_6	A_5	1	0	1	0	0
4	A_7	A_6	A_5	1	0	0	0	0
3	A_7	A_6	A_5	0	1	1	0	0
2	A_7	A_6	A_5	0	1	0	0	0
1	A_7	A_6	A_5	0	0	1	0	0
0	A_7	A_6	A_5	0	0	0	0	0

IR	INTERVAL = 8							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
7	A_7	A_6	1	1	1	0	0	0
6	A_7	A_6	1	1	0	0	0	0
5	A_7	A_6	1	0	1	0	0	0
4	A_7	A_6	1	0	0	0	0	0
3	A_7	A_6	0	1	1	0	0	0
2	A_7	A_6	0	1	0	0	0	0
1	A_7	A_6	0	0	1	0	0	0
0	A_7	A_6	0	0	0	0	0	0

During the third $\overline{\text{INTA}}$ pulse, the higher address of the appropriate service routine is enabled onto the bus. This address was initially programmed as byte 2 of the initialization sequence (A_8 - A_{15}).

CONTENTS OF THIRD INTERRUPT VECTOR BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8

Figure 2-8: Call Mode Address Byte Sequence

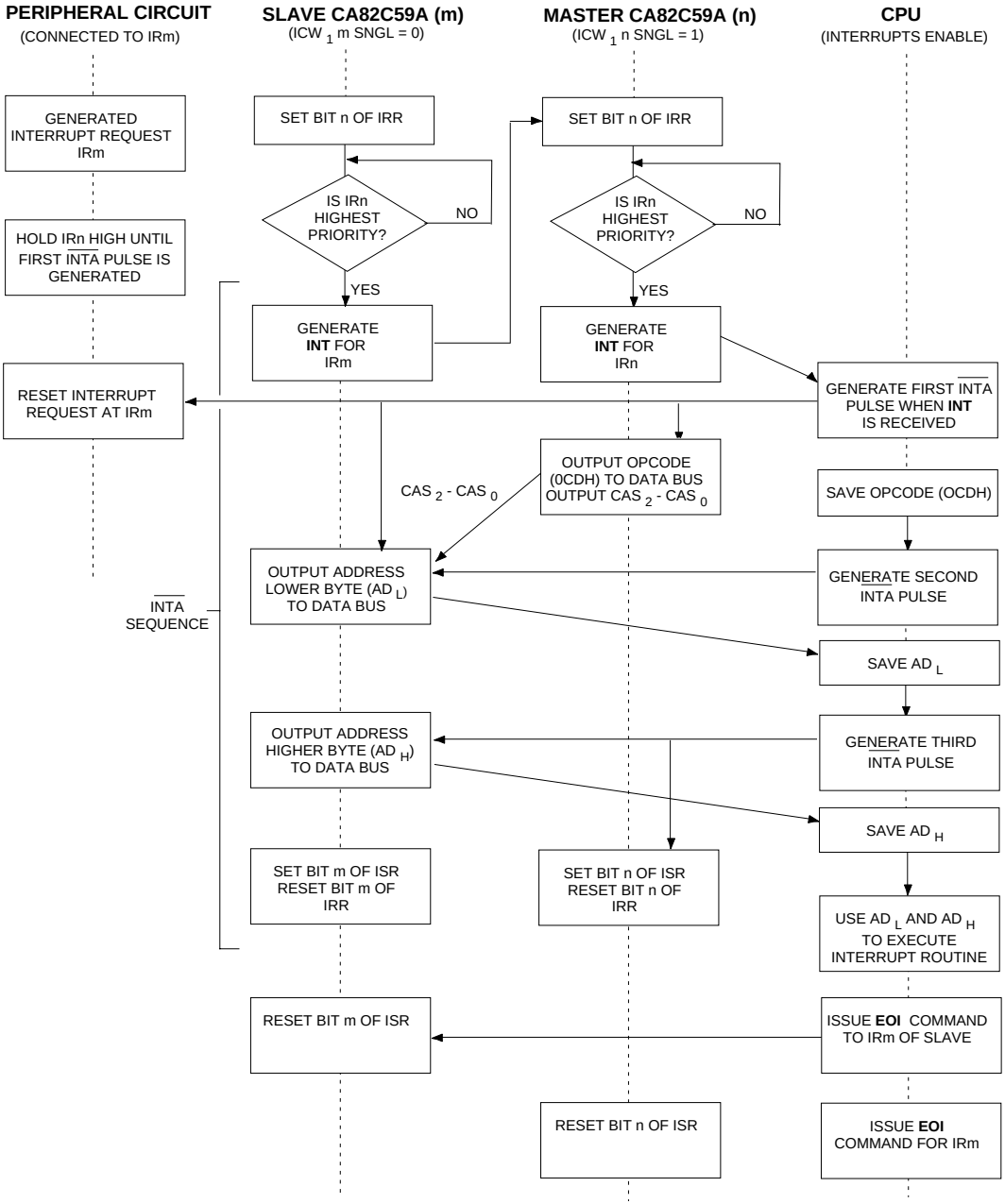


Figure 2-9: Call Mode Operation (Cascaded CA82C59A Systems)

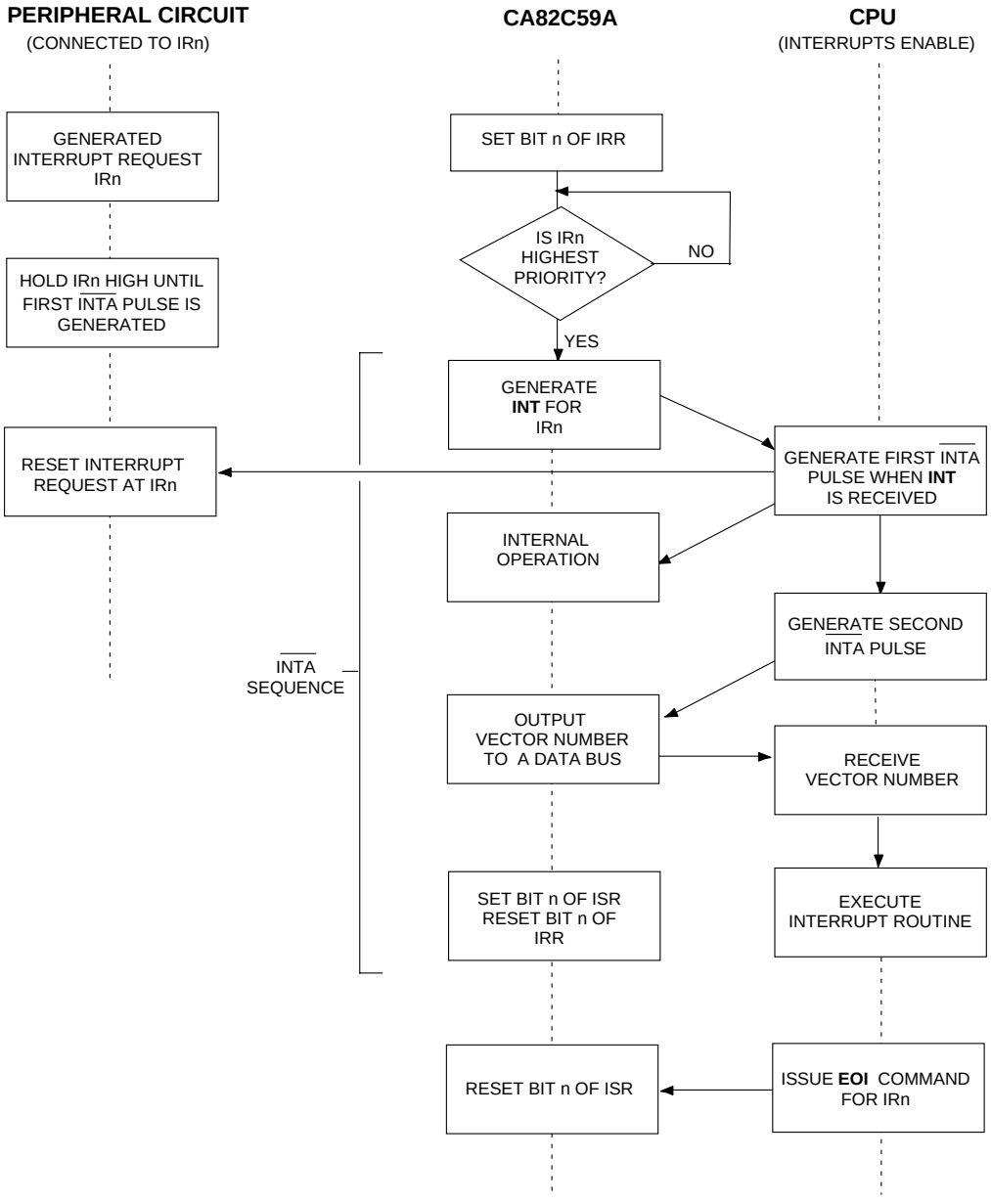


Figure 2-10: Vector Mode Operation (Single CA82C59A Systems)

CONTENTS OF FIRST INTERRUPT VECTOR BYTE

IR	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
7	T_7	T_6	T_5	T_4	T_3	1	1	1
6	T_7	T_6	T_5	T_4	T_3	1	1	0
5	T_7	T_6	T_5	T_4	T_3	1	0	1
4	T_7	T_6	T_5	T_4	T_3	1	0	0
3	T_7	T_6	T_5	T_4	T_3	0	1	1
2	T_7	T_6	T_5	T_4	T_3	0	1	0
1	T_7	T_6	T_5	T_4	T_3	0	0	1
0	T_7	T_6	T_5	T_4	T_3	0	0	0

The value T_7 to T_3 is programmed during byte 2 of the initialization (ICW_2). During the second $\overline{INTA}$ pulse, the interrupt vector of the appropriate service routine is enabled onto the bus. The low order three bits are supplied by the CA82C59A according to the IR input causing the interrupt.

Figure 2-11: Vector Mode Address Byte

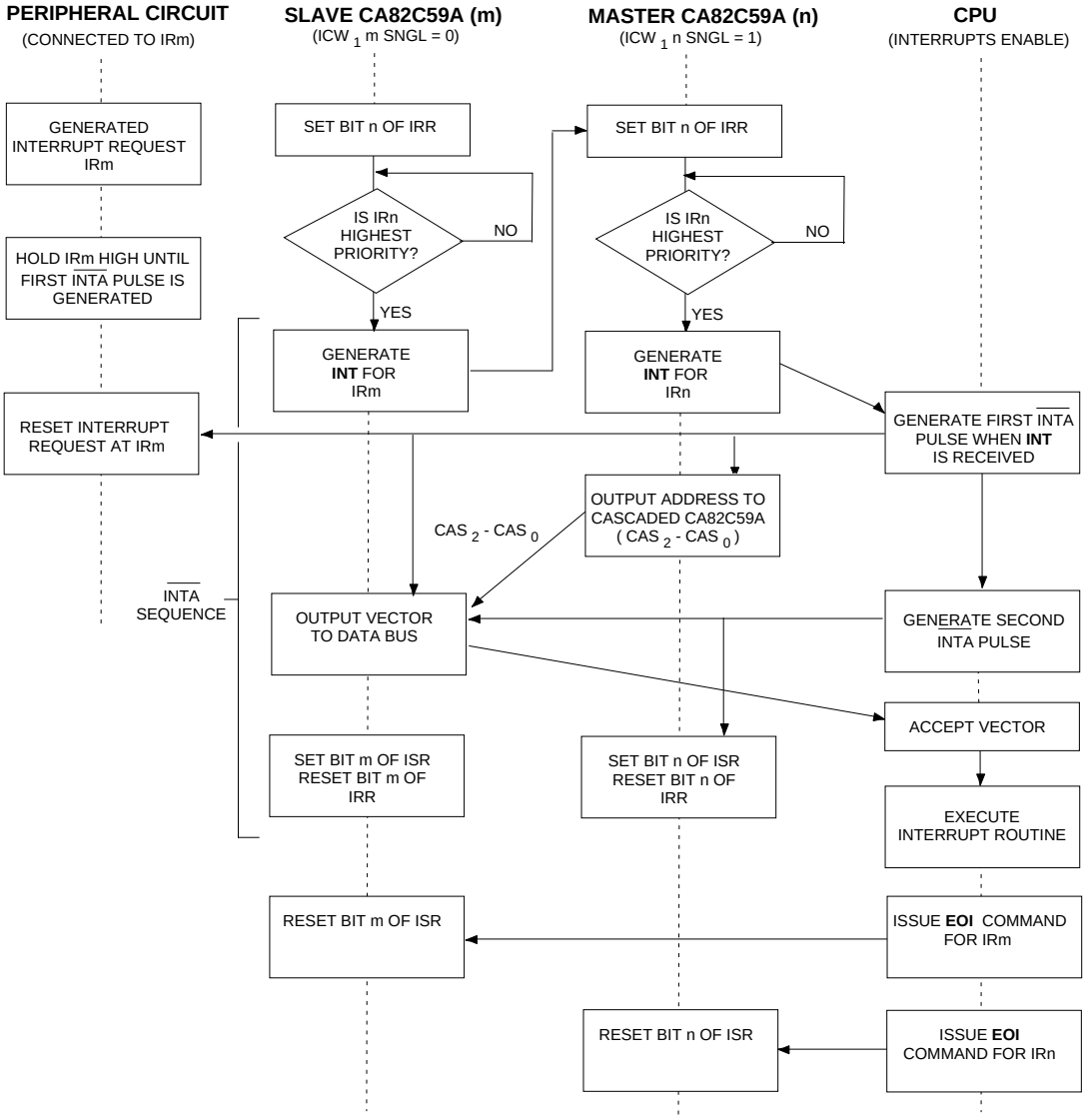


Figure 2-12: Vector Mode Operation (Cascaded CA82C59A Systems)

REGISTERS

The CA82C59A contains a number of registers, used to keep track of interrupts which are being serviced, or pending, as well as those which are masked. These registers are described in Table 2-7. They can be written to using the command word structure, or in the case of IRR, are set by external peripheral devices requesting interrupt service. The contents of all registers can be read by the CPU for status updates (see Table 2-8).

Table 2-7: CA82C59A Registers

Symbol	Name	Function
IMR	Interrupt Mask Register	An 8 - bit wide register that contains the interrupt request lines which are masked.
IRR	Interrupt Request Register	An 8 - bit wide register that contains the levels requesting an interrupt to be acknowledged. The highest request level is RESET from the IRR when an interrupt is acknowledged, (not affected by IMR).
ISR	In-Service Register	An 8 - bit wide register that contains the priority levels which are currently being serviced. The ISR is updated when an End of Interrupt Command (EOI) is received.

Table 2-8: Register Read/Write Operations

Operations		Other Conditions	Bit Programming			
CA82C59A	CPU		$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_0
IRR to Data Bus ISR to Data Bus	IRR Read ISR Read	IRR set by OCW_3 ISR set by OCW_3	0	0	1	0
Polling data to Data Bus	Polling of IRR and ISR	Polling data is read instead				
IMR to Data Bus	IMR Read		0	0	1	1
Data Bus to ICW_1 Reg. Data Bus to OCW_2 Reg. Data Bus to OCW_3 Reg.	ICW_1 Write OCW_2 Write OCW_3 Write	Set ICW_1 (D_4 = 1) Set OCW_2 (D_4, D_3 = 0) Set OCW_3 (D_4 = 0, D_3 = 1)	0	1	0	0
Data Bus to ICW_2 Reg. Data Bus to ICW_3 Reg. Data Bus to ICW_4 Reg.	ICW_2 Write ICW_3 Write ICW_4 Write	Refer to section on Control Words for ICW_2 - ICW_4 writing procedure	0	1	0	1
Data Bus to IMR	OCW_1 Write	After initialization				
Data Bus set to High Impedance State			0 1	1 x	1 x	x x
Illegal State			0	0	0	x

PROGRAMMING

The CA82C59A is initialized and programmed with special command words issued by the CPU. These commands fall into two major categories: Initialization Command Words (ICW_1 - ICW_4), and Operational Command Words

(OCW_1 - OCW_3). Initialization commands are used to bring the CA82C59A to a known state when the system is first activated, or after a system restart.

Operational commands are used once the CA82C59A is in operation (and after it has been initialized), to set, or alter specific interrupt program modes. The format and use of these two command types is described below.

Initialization Commands

The CA82C59A is initialized by a sequence of 2 to 4 command words (ICWs), where the actual number of commands sent depends on the system configuration, and the initial operating modes to be programmed. Note that each CA82C59A in the system must be initialized before operations begin in earnest (Figure 2-14).

The initialization sequence is started when the CPU sends $A_0 = 0$ and ICW_1 with $D_4 = 1$ (Figure 2-13). During initialization, the events below occur automatically:

- Edge sense circuit is reset. Thus, after initialization, an interrupt request must make a LOW-to-HIGH transition to be recognized.
- IMR is cleared.
- The priority of IR_7 is set to 7 (the lowest priority).
- Special Mask Mode is reset.
- Status read is set to IRR.
- If SNGL bit of $ICW_1 = 1$, then ICW_3 must be programmed.
- If IC_4 bit of $ICW_1 = 0$, then functions selected in ICW_4 are reset: Non-buffered Mode, no Automatic EOI, Call Mode operation.
- If $IC_4 = 1$, then CA82C59A will expect ICW_4.

Bit Definitions (ICW_1, ICW_2)

IC_4 — Set if ICW_4 is to be issued. This bit must be set for systems operating in Vector Mode.

SNGL — Set if this CA82C59A is not cascaded to other CA82C59As in the system (ICW_3 not issued). When CA82C59As are cascaded, SNGL is reset and ICW_3 is issued.

ADI — CALL Address Interval. If ADI = 1, then interval = 4. If ADI = 0, then interval = 8.

LTIM — Level Trigger Mode. If LTIM = 1, edge detect logic on the IR inputs is disabled, and the CA82C59A operates in level triggered mode.

$A_{5\text{-}15}$ — Service routine Page Starting Address (Call Mode). In a single CA82C59A system, the 8 interrupt request levels generate CALLs to 8 equally spaced locations in memory. These are spaced at intervals of either 4 or 8 memory locations according to the ADI value. Thus, the service routines associated with each CA82C59A in the system occupy pages of 32 or 64 bytes respectively.
Bits A_0 - A_4 are automatically inserted to give an address length of 2 bytes (A_0 - A_{15}). Note that the 8-byte interval is compatible with CA80C85B restart instructions.

$A_{11\text{-}15}$ — Service routine Vector Address Byte. In the vector mode, bits A_{11} - A_{15} are inserted in the five most significant places of the vector byte.
The three least significant bits are inserted by the CA82C59A according to the interrupt request level. The ADI and A_5 - A_{10} bits are ignored.

Bit Definitions (ICW_3)

This word is used only when SNGL = 0 in ICW_1, at which time the contents then depend on whether it is being sent to a master CA82C59A, or a slave device.

Master Mode — Sent to the master CA82C59A, each bit of ICW_3 represents a potential slave device connected to an IR input. If a slave exists, the corresponding bit in ICW_3 is set. Where a slave is not attached to an IR input of the master, the corresponding bit is reset. In operation, the master outputs byte 1 of the interrupt sequence to the bus, then enables the appropriate slave (via the cascade bus CAS_{0-2}) to output bytes 2 and 3 (Call Mode) or byte 2 only (Vector Mode).

Slave Mode — When sent to a slave CA82C59A, bits ID_{0-2} contain the slave address on the cascade bus. Each slave device in the system must be initialized with a unique address. Remaining bits are not used.
In operation, the slave compares the cascade input to its 3-bit address and if they match, outputs byte 2 and 3 (Call Mode), or byte 2 only (Vector Mode) to the bus.

Bit Definitions (ICW_4)

This word is used only when bit IC_4 in ICW_1 is set. Note that only five bits are used.

μPM — Microprocessor System Mode: μPM = 0 for Call Mode, μPM = 1 for Vector Mode.

AEOI — This bit is set if the Automatic End of Interrupt Mode is to be programmed.

M/S — When Buffered Mode is selected, the M/S bit is used to determine the master/slave programming. That is, M/S = 1 indicates the device is a master, while M/S = 0 indicates a slave. If the BUF bit is not set, M/S is not used.

BUF — Buffered Mode is programmed by setting BUF = 1. In buffered mode, the output pin SP/EN becomes an enable output, and the M/S bit determines whether the device is a master or a slave.

SFNM — Special Fully Nested Mode is programmed by setting SFNM = 1.

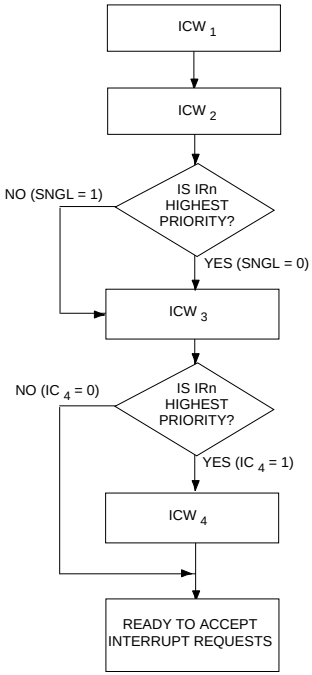


Figure 2-13: Initialization Flow Chart

Operational Commands

Once the CA82C59A has been initialized, it can accept and process interrupt requests received on its IR input lines. Interrupts are processed according to the modes programmed during the initialization process. A number of commands, sent to the CA82C59A from the CPU, allow the programmed modes or the interrupt request priorities to be changed on the fly during operation. These commands are described in the following sections (and in Figure 2-15).

Bit Definitions (OCW_1)

OCW_1 is used to set and clear mask bits in the IMR, thus enabling or disabling specific IR inputs. In the Special Mask Mode, the ISR is also masked.

M_{0-7} Bits M_{0-7} correspond to the 8 IR inputs. If bit $M_n = 1$, the IR_n input is disabled. If $M_n = 0$, the IR_n input is enabled.

Bit Definitions (OCW_2)

OCW_2 is used to program the different End of Interrupt (EOI) Modes, and alter the interrupt request priorities.

L_{0-2} These bits designate the interrupt level to be acted upon when bit SL = 1 (active).

EOI The End of Interrupt command is issued by the CPU, rather than by the CA82C59A (in automatic EOI mode). Note that this bit is used in conjunction with bits R and SL to control the interrupt priority assignments and rotations.

SL Set Interrupt Level bit. This lowest priority interrupt is assigned to the IR input corresponding to the octal value of L_{0-2}.

R This bit determines if interrupt priority rotation is in effect. R = 1 indicates priorities will be rotated, perhaps combined with other modes.

Bit Definitions (OCW_3)

OCW_3 is used to program the Special Mask Mode, the Polling Mode, and select internal registers to be read by the CPU.

RIS If RIS = 0, select ISR. If RIS = 1, select IRR.

RR Read Register bit. If RR = 1, output the contents of the register selected by bit RIS onto the bus. The register selection is retained, so OCW_3 does not have to be reissued in order to read the same register again.

P If P = 1, the Polling Mode is selected for this CA82C59A. In this mode the CPU will poll for new interrupt requests, rather than having the CA82C59A actively set the CPU INT input.

SMM If Special Mask Mode is enabled (ESMM = 1), then SMM = 1 programs the special mask mode, and SMM = 0 clears the special mask mode.

ESMM If ESMM = 1, then the special mask mode is enabled and can be set or reset by the SMM bit. If ESMM = 0, the special mask mode is disabled and SMM is ignored.

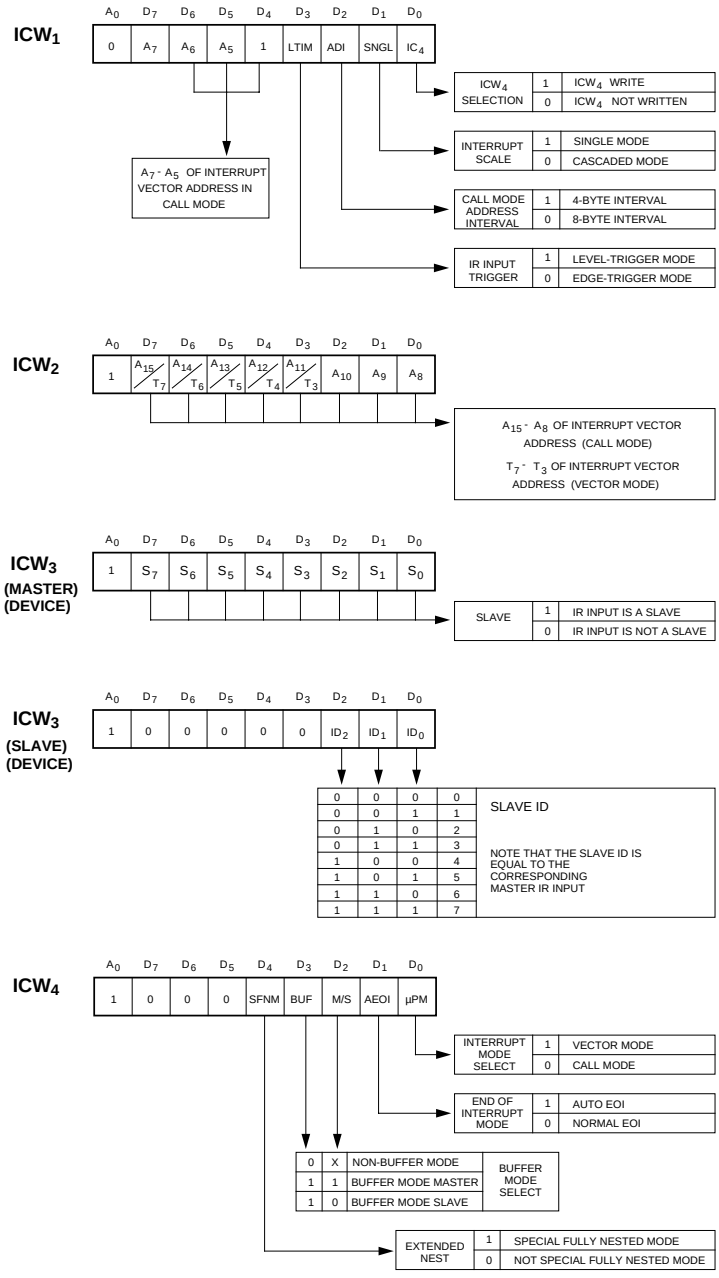


Figure 2-14: Initialization Command Word Format

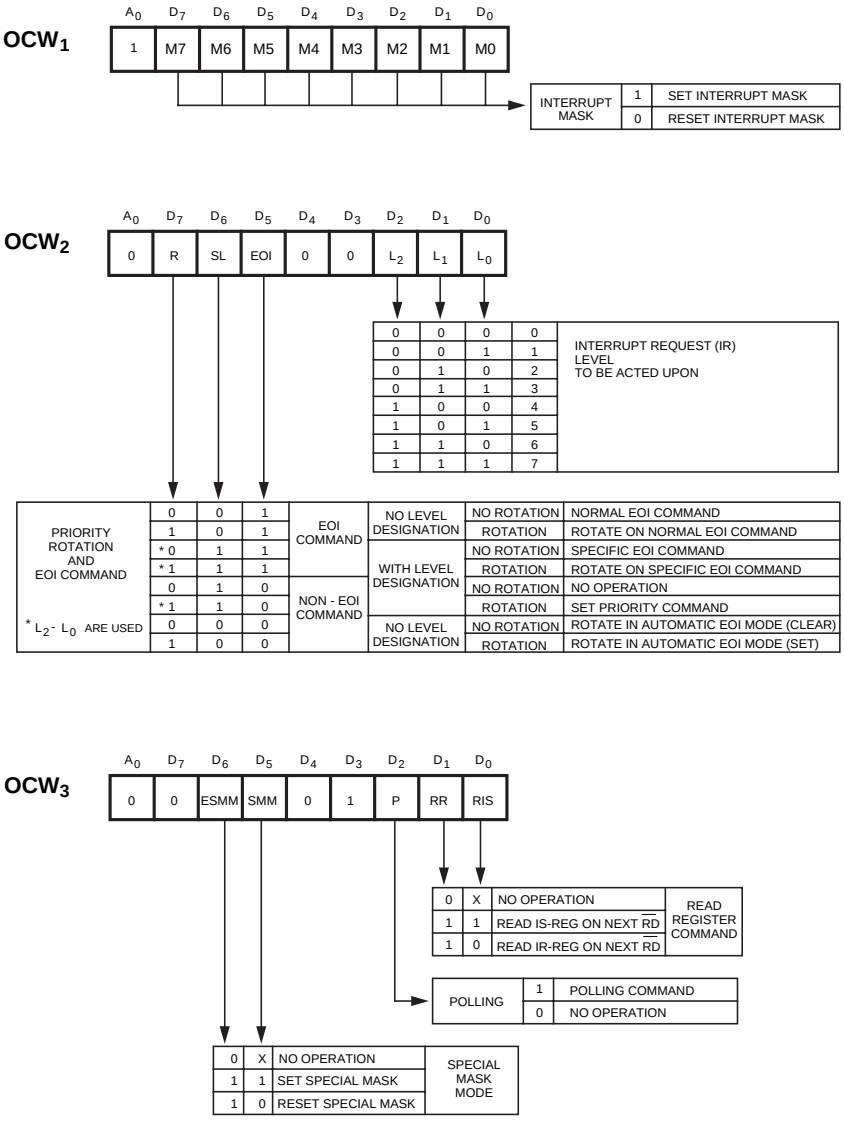


Figure 2-15: Operational Command Word Format

OPERATIONAL MODES

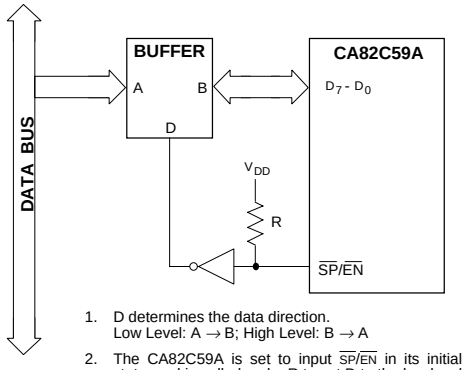
The CA82C59A can be programmed to operate in a number of different modes which are summarized and described below. Depending on the mode, some are set during initialization, and some during operation (with the command word structure).

Mode	Location Set
Buffer Mode	BUF, M/S (ICW_4)
Cascaded Mode	SNGL (ICW_1)
•Master Mode	(ICW_3)
•Slave Mode	ID_{0-2} (ICW_3)
End of Interrupt (EOI) Modes	EOI (OCW_2)
•Automatic EOI Mode	AEOI (ICW_4)
•Non-specific EOI	EOI, SL, R (OCW_2)
•Specific EOI	EOI, SL, R (OCW_2)
Nested Modes	
•Fully Nested Mode	default mode
•Special Fully Nested Mode	SFNM(ICW_4)
	AEOI (ICW_4)
Polling Mode	P (OCW_3)
Rotation Modes	
•Automatic Rotation Mode	R, SL, EOI (OCW_2)
•Specific Rotation Mode	R, SL, L_{0-2} (OCW_2)
Special Mask Mode	ESMM, SMM (OCW_3)
System Modes	
•CALL Mode	µPM(ICW_4)
•VECTOR Mode	µPM (ICW_4)
	IC4 (ICW_1)
Trigger Modes	
•Edge Triggered Mode	LTIM (ICW_1)
•Level Triggered Mode	LTIM (ICW_1)

Buffer Mode

In larger systems the CA82C59A may be required to drive the data bus through a buffer. To handle this situation, the Buffer Mode is programmed during initialization (using the BUF and M/S bits in ICW_4).

When in buffer mode, $\overline{SP}/\overline{EN}$ is used to enable the data bus buffers, and determine the direction of data flow through the buffer (Figure 2-16). This signal is active when the output ports of the CA82C59A are activated.



1. D determines the data direction. Low Level: A → B; High Level: B → A
2. The CA82C59A is set to input $\overline{SP}/\overline{EN}$ in its initial state, and is pulled up by R to set D to the low level during initialization.

Figure 2-16: Buffer Mode

Note that when cascaded CA82C59As are required to be used in the buffer mode, the master/slave selection is done using the M/S bit of ICW_4, (and SNGL bit of ICW_1 is set to 1). M/S is set to 1 for the master mode, 0 for the slave mode.

Cascaded Mode

In systems that contain more than 8 priority interrupt levels, several CA82C59A devices can be easily cascaded together to handle a maximum of 64 interrupt levels. In a cascaded configuration, one CA82C59A serves as a master, controlling up to 8 slaves (able to handle 8 interrupts each). The master selects the slaves via the cascade local bus (CAS_{0-2}), enabling the corresponding slave to output the interrupt service routine address (or vector) following each of the second and third $\overline{INTA}$ signals (second $\overline{INTA}$ signal only in Vector mode). At the end of the interrupt cycle, the EOI command must be issued twice, one for the master, and one for the appropriate slave.

The CAS_{0-2} bus lines are normally held in a LOW state, and activated only for slave inputs (non-slave inputs to the master do not affect the cascade bus). The slave address will be held on the cascade bus from the trailing edge of the first $\overline{INTA}$ signal to the trailing edge of the last $\overline{INTA}$ signal (either second or third depending on the system mode).

Within the system, each slave can be programmed to operate in a different mode (except AEOI), independently of other slave devices. The interrupt output (INT) of each slave is tied to one of the interrupt request lines (IR_{0-7}) of the master device. Unused IR pins on the master device can be connected to other peripheral devices (as in the single stand-alone mode of operation), or left unconnected.

Note that an address decoder is required to activate the chip select ($\overline{CS}$) input of each CA82C59A in the system.

Master Mode

A CA82C59A operating in the Master Mode can be controlling both peripheral interrupts as well as other CA82C59A slave devices. Since both types of inputs are connected to the IR_{0-7} pins, it is necessary to differentiate between the two. This is accomplished in the initialization control word (ICW_3) sent out to the master. ICW_3 sets the S_n bits corresponding to IR_n pins connected to slaves equal to one (1), while Sm bits corresponding to IR_m pins connected to peripheral inputs are reset to zero.

Peripheral interrupt requests to IR_m pins ($S_m = 0$) are handled by the master as if it were operating singly. That is, the CAS line remain LOW, and the master provides the interrupt or vector as required.

Slave interrupt requests to IR_n pins ($S_n = 1$) are handled as follows; the master sends an interrupt to the CPU if the slave requesting the interrupt has priority. If so, the master outputs the slave address n to the CAS bus on the first $\overline{INTA}$ signal, then lets the slave complete the remainder of the interrupt cycle. Note again however, that two EOI commands are required to terminate the sequence, one each for the master and slave.

Slave Mode

When a slave CA82C59A receives a peripheral interrupt request, and it has no higher interrupt requests pending, the slave sends an interrupt request to the master via its INT output. This interrupt request is passed by the master to the CPU, which then initiates the interrupt cycle, in turn causing the master to output the slave's address on the CAS bus. Each slave in the system continuously monitors the CAS bus, comparing the addresses thereon until a match is found with its own address. When the slave initiating the interrupt request finds an address match, it completes the interrupt sequence as though it were a single CA82C59A.

Note: Since the master holds the CAS bus LOW (corresponding to CAS address 0) when processing peripheral interrupt requests, address 0 should not be used as a slave address unless the system contains the full complement of 8 slaves.

End of Interrupt (EOI) Modes

The EOI Modes are used to terminate the request for interrupt service sequence, update the ISR register and alter the interrupt priorities. The EOI mode selected depends on the nesting mode currently programmed. The options are discussed in the sections following.

Automatic EOI (AEOI) Mode

In AEOI Mode, the ISR bit corresponding to the interrupt is set and reset automatically during the final $\overline{INTA}$ signal. This means that the CPU does not have to issue an EOI command at the end of the interrupt routine.

Caution is urged in using AEOI however, as the ISR does not save the routine currently in service in this mode. Thus, unless the interrupts are disabled by the interrupt service routine, a stack overflow situation can result from newly generated interrupts (which bypass the priority structure), or from level triggered interrupts.

The Automatic EOI mode is programmed by setting the AEOI bit in $ICW_4 = 1$.

Non-specific (Normal) EOI Mode

When the CA82C59A is operated in the Fully Nested Mode, it can easily determine which ISR bit is to be reset at the conclusion of an interrupt sequence. In this case, the non-specific EOI command is used to reset the highest priority level selected from the interrupts in service, (the valid assumption being that the last interrupt level acknowledged and serviced necessarily corresponds to the highest priority ISR bit set).

A Non-specific EOI Mode is selected via OCW_2, where EOI = 1, SL = 0 and R = 0). Refer to Figure 2-17.

a) Non-specific EOI Command

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OCW_2	0	0	1	0	0	X	X	X

b) Specific EOI Command

OCW_2	0	1	1	0	0	L_2	L_1	L_0

c) Rotate on Non-specific EOI Command

OCW_2	1	0	1	0	0	X	X	X

d) Rotate on Specific EOI Command

OCW_2	1	1	1	0	0	L_2	L_1	L_0

Figure 2-17: EOI Commands

Specific EOI Mode

The Specific EOI Mode is required when the fully nested (normal) mode is not used, and the CA82C59A is unable to determine the last interrupt level acknowledged (such as might be encountered if the Special Mask Mode is programmed). The Specific EOI command identifies the ISR bit (interrupt level) to be reset using bits L_{0-2} of OCW_2, which also has the following bit settings: EOI = 1, SL = 1 and R = 0. Refer to Figure 2-17.

Mask Modes

The Mask Modes are used to selectively enable or disable interrupt requests. This is distinct from the automatic disabling of an interrupt which is in effect while a request from the same interrupt is being serviced.

Normal Mask Mode

Interrupt request lines IR_{0-7} can be individually masked in the Interrupt Mask Register (IMR), using OCW_1. Each bit in IMR masks one interrupt request line if it is set (= 1), with no effect on the other interrupt request lines. Bit 0 masks IR_0, bit 1 masks IR_1 etc.

Special Mask Mode

The Special Mask Mode is used to dynamically alter the interrupt priority structure under software control during program execution. In this mode, when a mask bit is set in OCW1, it disables further interrupts at that level, and enables interrupts from all other levels that are not masked. This includes those interrupts which are lower (as well as higher) in priority.

The Special Mask Mode is set by ESMM = 1 and SMM = 1 in OCW_3. To clear this mode, the CPU must issue another OCW_3 with ESMM = 1 and SMM = 0. Setting ESMM = 0 alone has no effect. To correctly enter the Special Mask Mode, use the following procedure:

1) CPU reads the ISR
2) CPU writes the ISR data from (1) to the IMR
3) CPU selects Special Mask Mode by issuing OCW3 with ESMM = 1 and SMM = 1.

This procedure ensures that all interrupt requests not currently in service will be enabled.

Note that if IMR is not set equal to ISR when Special Mask Mode is selected, bits which may be set in the ISR will be ignored. If a corresponding bit is not set in IMR, that interrupt request may be serviced, causing all interrupts of lower priority to be effectively disabled. This is illustrated in Figure 2-18.

When the Special Mask Mode is selected, the Specific EOI Mode must be used to terminate the interrupt sequence, so the CPU can explicitly specify which ISR bit is to be reset.

Nested Modes

The nesting modes are used to determine, and change, the priority of incoming interrupt requests.

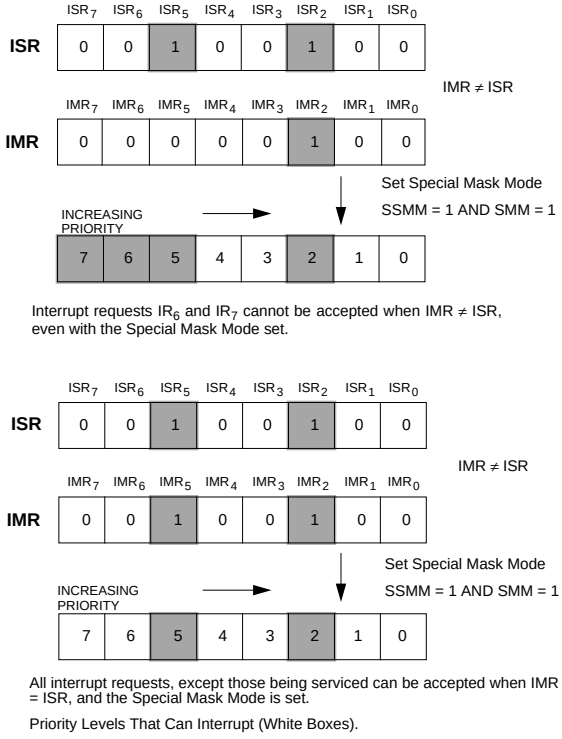


Figure 2-18: Special Mask Mode

Fully Nested Mode

The default nesting mode, entered automatically after initialization, unless another mode has been programmed. In the Fully Nested Mode, the interrupt request priorities are set in descending order from 0 to 7. That is: IR_0 is the highest priority interrupt, IR_7 the lowest.

When an interrupt is acknowledged, the highest priority request is selected, the corresponding ISR bit is set, and the service routine address information is output to the data bus. The ISR bit is reset by the EOI command from the CPU, or auto-

matically if AEOI Mode is programmed, at the completion of the interrupt sequence. While the ISR bit is set, all interrupt requests of equal or lower priority are inhibited. Interrupt requests of higher priority will generate an interrupt to the CPU, but whether or not these will be acknowledged depends on the system software logic. Interrupt priorities can be altered in this mode using one of the Rotation Modes.

Note that fully nested interrupt priorities are not necessarily preserved in those systems containing cascaded CA82C59As, as it is possible for interrupts of higher priority than the one being serviced to be ignored. This situation occurs when a slave accepts a peripheral interrupt request (and passes the request to the master). When the master accepts the request, it locks out further interrupts from that slave. Should an interrupt of higher priority come in to the same slave, it will not be recognized until the interrupt being serviced has completed processing. To preserve interrupt priorities in this situation, use the Special Fully Nested Mode.

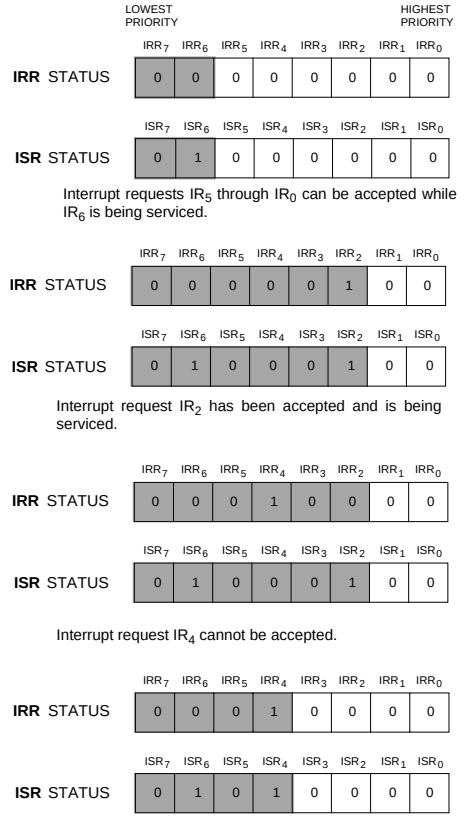


Figure 2-19: Fully Nested Mode

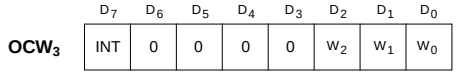
Special Fully Nested Mode

This mode is very similar to the Fully Nested Mode, but is used in systems with cascaded CA82C59s, so as to preserve the interrupt priorities within each slave, as well as within the master. The Special Fully Nested Mode is programmed by setting the SFNM bit in the ICW_4 word in both the master and the slave during initialization. This allows interrupt requests of a higher level than the one being serviced to be accepted by the master from the same slave. That is, the slave is not locked out from the priority logic in the master, and higher priority interrupts within the slave will be recognized by the master, which will generate an interrupt to the CPU.

Caution should be exercised in this mode during the End Of Interrupt processing. It is essential that the system software check whether or not the interrupt just serviced was the only one from that slave. After the first non-specific EOI has been issued to the slave, the CPU should read the slave's ISR and check that no other bits are set (ISR = 0). Only if the slave ISR is zero, should a non-specific EOI be sent to the master to complete the interrupt sequence. If bits are set in the slave ISR, no EOI should be sent to the master.

Polling Mode

The Polling Mode is used to bypass the CA82C59A Interrupt control logic in favour of CPU software control over interrupt request processing. This allows systems to be built up with more than one master CA82C59A, and consequently, the system can contain more than 64 interrupt priority levels (since each master can handle 64 levels individually). In this case, the CPU polls each master looking for the highest priority interrupt request within the realm of each master.



NOTES:

1. W_0 - W_2 is binary code of highest priority level requesting service.
2. INT is equal to one (1) if there is an interrupt.

Figure 2-20: Poll Command

In the Polling Mode, the INT outputs of the CA82C59A masters, and the INT input of the CPU are disabled. Interrupt service to individual peripheral devices is accomplished in system software by using the Poll Command (Bit 'P' = 1 in OCW_3). When a poll command has been issued, the CA82C59A waits for the CPU to perform a register read. This read is treated by the CA82C59A as an interrupt acknowledge, and it sets the appropriate ISR bit and determines the priority level if there is an interrupt request pending. It then outputs the polling data byte onto the data bus (see Figure 2-20), including the binary code of the highest priority level requesting service. The CPU then processes the interrupt according to the polling data read, terminating the interrupt sequence with an EOI.

Rotation Modes

The different Rotation Modes allow the interrupt request priorities to be changed either automatically, or under software control. This is particularly useful for situations where there are a number of equal priority devices, or where a particular application may call for a specific priority change.

Automatic Rotation Mode

The Automatic Rotation Mode is recommended where there are a number of equal priority devices. In this mode the device is assigned the lowest priority immediately after it has had an interrupt request serviced. Its priority is subsequently increased as other devices have their interrupt requests serviced, and are then rotated to the bottom of the priority list. In the worst case, a device would have to wait for a maximum of seven other device interrupts of equal priority to be serviced once, before it was serviced. The effect of rotation on interrupt priority is illustrated in Figure 2-21.

Automatic Rotation can be activated in one of two ways, both using the command word OCW_2, and both combined with EOI modes:

- Rotation in Non-specific EOI Mode (R = 1, SL = 0 and EOI = 1)
- Rotation in Automatic EOI Mode (R = 1, SL = 0 and EOI = 0). This mode must be cleared by the CPU (accomplished by sending OCW_2 with: R = 0, SL = 0 and EOI = 1.

Specific Rotation Mode

The Specific Rotation Mode provides a mechanism to arbitrarily change interrupt priority assignments. This is accomplished by programming the lowest priority interrupt request line (specified by bits L_{0-2} in OCW_2), thereby fixing the other priorities. That is, if IR_4 is programmed as the lowest priority device, then IR_5 will have the highest priority.

Caution: Because this change in priority levels is different from the normal Fully Nested Mode, it is essential that the user manage the interrupt nesting via the system software.

Specific rotation can be activated in one of two ways, both using the command word OCW_2:

- The Set Priority command is issued in OCW_2 with: R = 1, SL = 1 and L_{0-2} equal to the binary code of the lowest priority device.
- As part of the Specific EOI Mode, with OCW_2, (Rotate on Specific EOI command) values: R = 1, SL = 1, EOI = 1 and L_{0-2} equal to the binary priority level code of the lowest priority device. When the specific EOI is issued by the CPU, the CA82C59A resets the ISR bit designated by bits L_{0-2} in OCW_2, then rotates the priorities so that the interrupt just reset becomes the lowest priority.

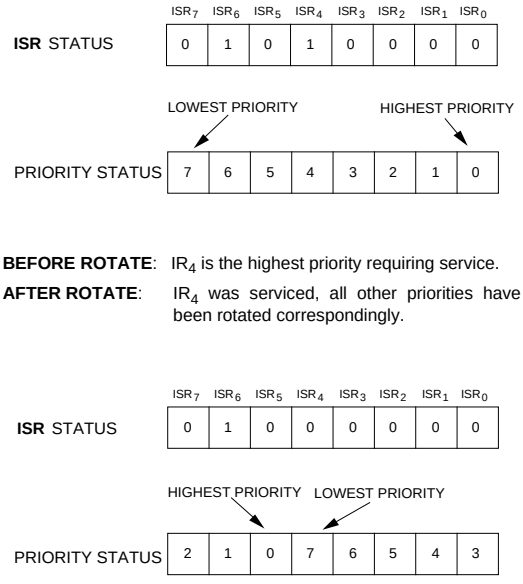


Figure 2-21: Effect of Rotation

a) Rotate in Automatic EOI Mode (Set)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OCW_2	1	0	0	0	0	X	X	X

b) Rotate in Automatic EOI Mode (Reset)

OCW_2	0	0	0	0	0	X	X	X

c) Rotate on Non-specific EOI Command

OCW_2	1	0	1	0	0	X	X	X

d) Rotate on Specific EOI Command

OCW_2	1	1	1	0	0	L_2	L_1	L_0

e) Set Priority Command (Specific Rotation)

OCW_2	1	1	0	0	0	L_2	L_1	L_0

Figure 2-22: Rotation Commands

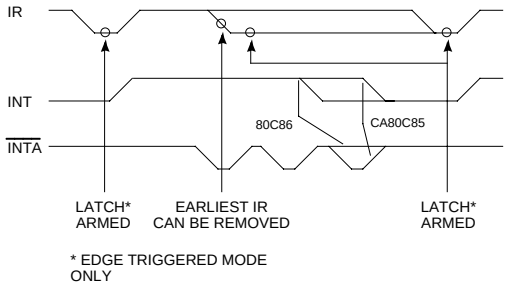


Figure 2-23: Trigger Mode Timing

System Modes

The CA82C59A must operate in the system mode that corresponds to the processor type used in the system. Call Mode is used for 8085 type systems (and features an interrupt cycle controlled by three $\overline{INTA}$ signals), while Vector Mode is used for more sophisticated 8088/86 and 80286/386 type systems (and features an interrupt cycle controlled by only two $\overline{INTA}$ signals). These modes are described in more detail back in the Operational Description section.

Trigger Modes

In the CA82C59A, the interrupt request lines (IR_{0-7}) can be programmed for either edge or level triggering sensitivity, with the requirement that all IR lines must be in the same mode. That is, all edge triggered, or all level triggered. Figure 2-24 illustrates the priority cell diagram which shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the IR lines.

Note that to ensure a valid interrupt request is registered by the CA82C59A, it is essential that the IR input remain HIGH until after the first $\overline{INTA}$ has been received. In both modes, if the IR input goes LOW before this time, the interrupt will be registered as a default IR_7 regardless of which IR input initiated the interrupt request. This default IR_7 can be used to detect (and subsequently ignore) spurious interrupt signals such as those caused by glitches or noise on the IR input lines. The technique is described below:

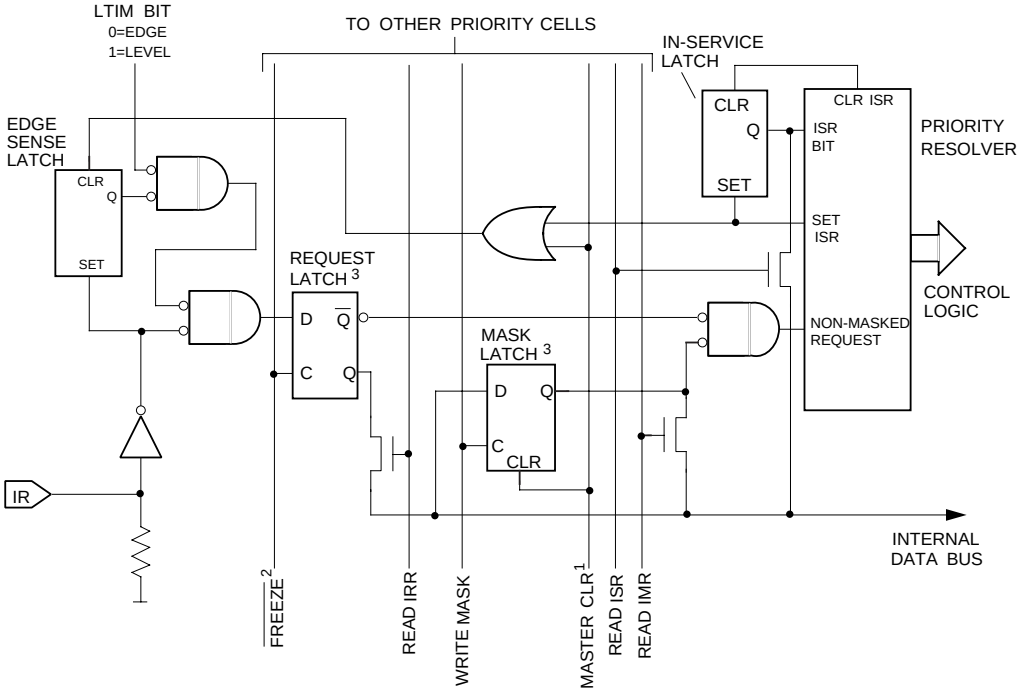
- If the IR_7 input is not used, it can be assigned solely to intercepting spurious interrupt requests, invoking a simple service routine that contains a return only, thus effectively ignoring the interrupt.
- If IR_7 is used for a peripheral interrupt, a default IR_7 is detected with the extra step of reading the ISR. A normal IR_7 interrupt causes the corresponding bit to be set in the ISR, while a default IR_7 interrupt does not. It is necessary that the system software keep track of whether or not the IR_7 service routine has been entered. In the event that another IR_7 interrupt occurs before servicing is complete, it will be a default IR_7 interrupt (and should be ignored)

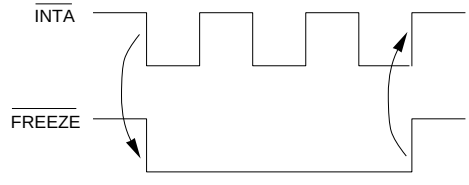
Edge Triggered Mode

Programmed by setting the LTIM bit in ICW_3: LTIM = 0 for low-to-high-transition edge triggering. An interrupt request is detected by a rising edge on an IR line. The IR line must remain HIGH until after the falling edge of the first $\overline{INTA}$ signal has been received from the CPU. This is required to latch the corresponding IRR bit. It is recommended that the IR line be kept HIGH to help filter out noise spikes that might cause spurious interrupts. To send the next interrupt request, temporarily lower the IR line, then raise it.

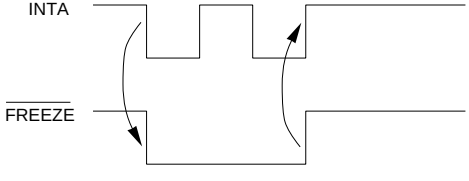
Level Triggered Mode

Programmed by setting the LTIM bit in ICW_3: LTIM = 1 for level triggering. An interrupt request is detected by a HIGH level on an IR line. This HIGH level must be maintained until the falling edge of the first $\overline{INTA}$ signal (as in the edge-triggered mode), to ensure the appropriate IRR bit is set. However, in the level triggered mode, interrupts are requested as long as the IR line remains HIGH. Thus, care should be exercised so as to prevent a stack overflow condition in the CPU.





CA80C85 MODE



80C86 MODE

NOTES:

1. MASTER CLEAR ACTIVE ONLY DURING ICW1
2. $\overline{\text{FREEZE}}$ IS ACTIVE ONLY DURING $\overline{\text{INTA}}$ AND POLL SEQUENCES
3. D-LATCH TRUTH TABLE

C	D	Q	OPERATION
1	D_i	D_i	FOLLOW
0	X	Q_{n-1}	HOLD

Figure 2-24: Priority Cell Structure

APPLICATION DIAGRAMS

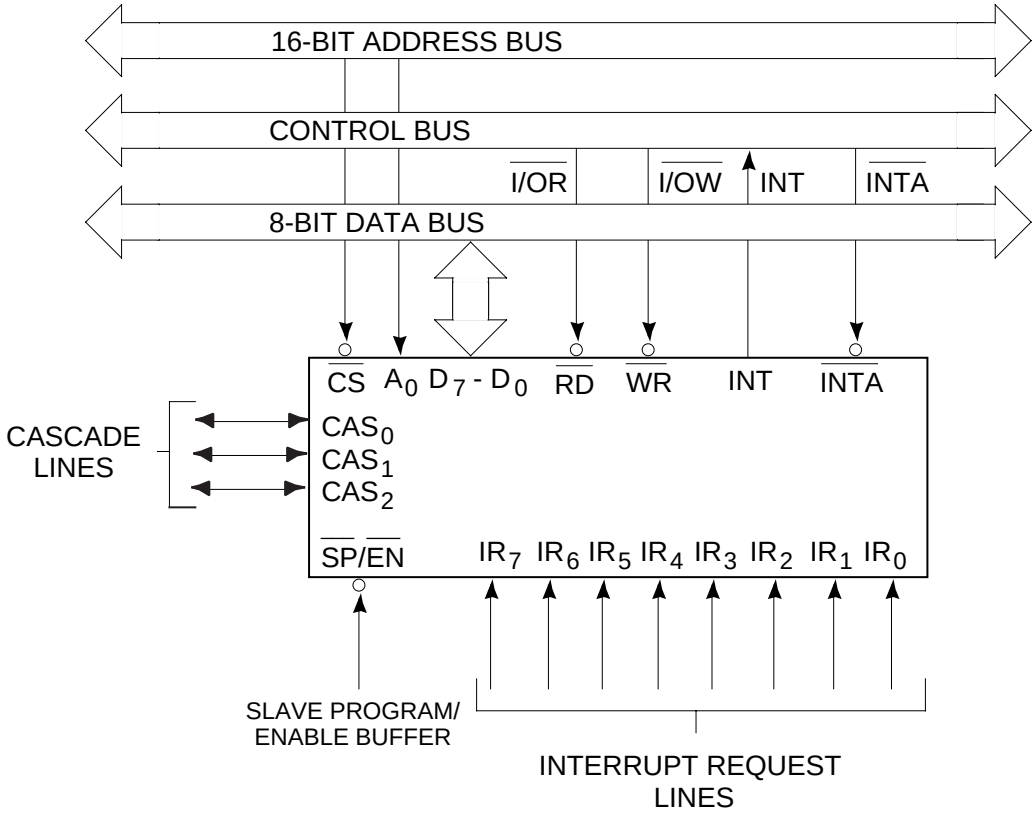
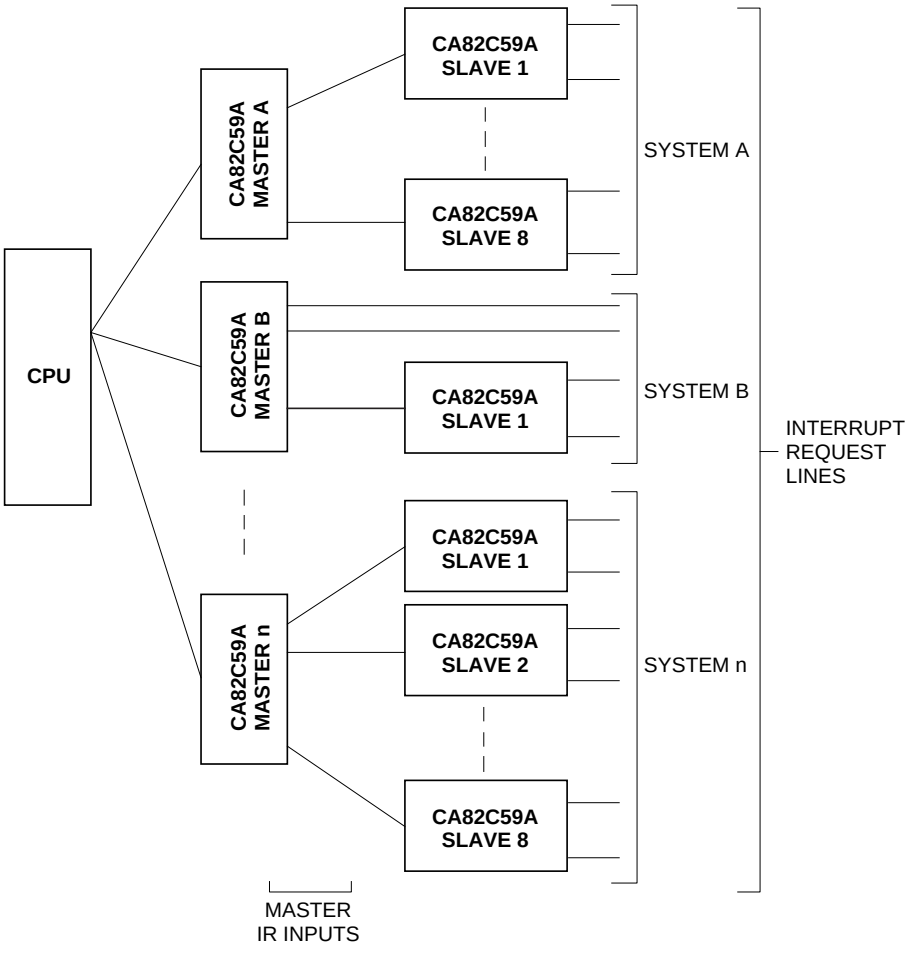


Figure 2-25: CA82C59A In Standard System Configuration



NOTES:

1. MASTER CA82C59As IN POLL MODE

2. MAXIMUM OF 64 INPUTS PER SYSTEM

3. TOTAL CAPACITY LIMITED BY CPU

Figure 2-26: Multiple CA82C59As In A Cascaded System

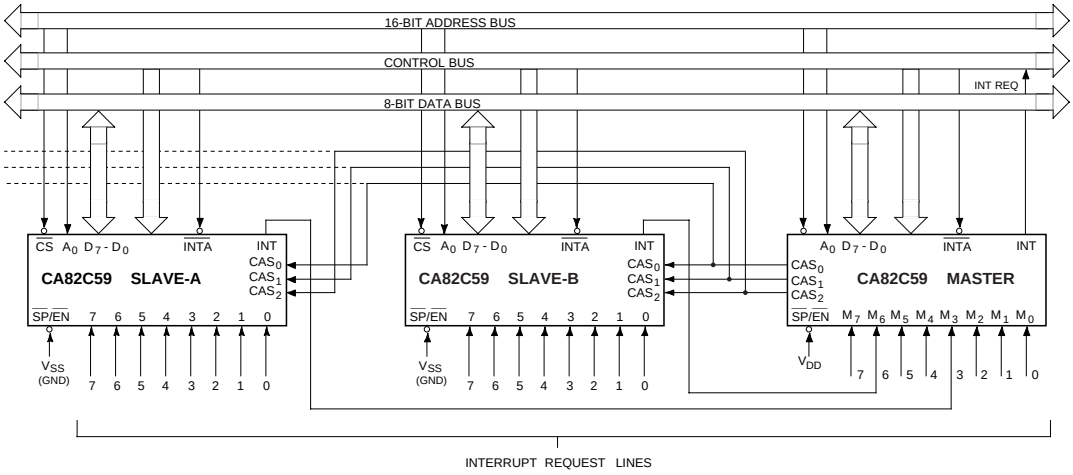


Figure 2-27: Multiple CA82C59A Masters In A Polled System

Section 3

Worldwide Sales Network

USA Sales Representatives

Eastern

D.C., Maryland, Virginia

Chesapeake Technologies
3905 National Dr., Suite 425
Burtonsville, MD 20866

Tel: 301-236-0530
Fax: 301-384-9596

Chesapeake Technologies
12-616E Hampton Dr.
Midlothian, VA 23113

Tel: 804-379-1816
Fax: 804-379-3474

Connecticut, Maine, Massachusetts, New Hampshire, New Jersey, New York, Rhode Island, Vermont, Eastern Pennsylvania

Daner Hayes Inc.
300 Eliot St., Suite 342
Ashland, MA 01721

Tel: 508-881-0400
Fax: 508-881-8227

Upstate New York, Delaware, Ohio

Supertech
32 Trotter Dr.
Henrietta, NY 14467

Tel: 716-359-4652
Fax: 716-321-1581

EMA, Inc.
Aurora Office Plaza, Suite 291
251 West Garfield Rd.
Aurora, OH 44202

Tel: 216-562-6104
Fax: 216-562-7498

EMA, Inc.
35 Compark Road,
Centreville, OH 45459

Tel: 937-433-2800
Fax: 937-433-3147

Florida

Apollo Technical Sales Co.
1275S Patrick Dr., #M2
Satellite Beach, FL 32937-3963

Tel: 407-777-7511
Fax: 407-777-5251

Apollo Technical Sales Co.
2264 Tamarron Terrace, #2005
Palm Harbor, FL 34683

Tel: 813-781-3646
Fax: 813-781-5522

Central

Illinois, Michigan, Wisconsin

Horizon Technical Sales
4340 Cross Street,
Downer's Grove, IL 60515

Tel: 630-852-2500
Fax: 630-852-2520

Horizon Technical Sales
6011 Hilldale Dr.
Hartford, WI 53027-9541

Tel: 414-670-6776
Fax: 414-670-6778

Alabama, Georgia, Mississippi, North Carolina, South Carolina, Tennessee

BITS, Inc.
2707 Artie St., Suite 10
Huntsville, AL 35805

Tel: 205-534-4020
Fax: 205-534-0410

BITS, Inc.
1 Meca Way
Norcross, GA 30093

Tel: 770-564-5599
Fax: 770-564-5588

BITS, Inc.
7706 Six Forks Rd., Suite 101
Raleigh, NC 27615

Tel: 919-676-1880
Fax: 919-676-1881

BITS, Inc.
2305 Keaton Ave., Suite E
Charlotte, NC 28269

Tel: 704-510-1064
Fax: 704-510-1065

Arkansas, Louisiana, Oklahoma, Texas

Quad State Sales and Marketing
12160 Abrams Rd., Suite 406
Dallas, TX 75243

Tel: 972-669-8567
Fax: 972-669-8834

Quad State Sales and Marketing
8310 Capital of Texas Highway
North, Suite 365
Austin, TX 787331

Tel: 512-346-7002
Fax: 512-346-3601

Quad State Sales and Marketing
10565 Katy Freeway, Suite 212
Houston, TX 77024

Tel: 713-467-7749
Fax: 713-467-5942

Quad State Sales and Marketing
110 West Commercial, Suite 210
Broken Arrow, OK 74013

Tel: 918-258-7723
Fax: 918-258-7653

Minnesota, North Dakota, South Dakota, Western Wisconsin

Electromec Sales Inc.
1601 East Highway 13, Suite 102
Burnsville, MN 55337

Tel: 612-894-8200
Fax: 612-894-9352

Missouri, Southern Illinois, Iowa, Kansas, Nebraska

Please contact Tundra Semiconductor directly at: 1-800-267-7231

USA Sales Representatives Cont'd

Mountain

Arizona, New Mexico

ETS (Electronic Technical Sales)
1403 West 10th Place., Ste. B110
Tempe, AZ 85281

Tel: 602-921-7122
Fax: 602-921-7125
1-800-424-2540

ETS (Electronic Technical Sales)
6220 W. Helton Place
Tucson, AZ 85746

Tel: 520-883-3728
Fax: 520-883-0029

Colorada, Idaho, Montana, Utah, Wyoming

WESCOM Marketing Inc.
4860 Ward Rd.
Wheat Ridge, CO 80033

Tel: 303-422-8957
Fax: 303-422-9892

WESCOM Marketing Inc.
3500 S. Main St.
Salt Lake City, UT 84115

Tel: 801-269-0419
Fax: 801-269-0665

Western

Northern California, Northern Nevada

Quorum Technical Sales
4701 Patrick Hanry Dr.
Santa Clara, CA 95054

Tel: 408-980-0812
Fax: 408-748-1163

Southern California, Southern Nevada

Harper & Two
2798 Junipero Avenue
Signal Hill, CA 90806

Tel: 310-424-3030
Fax: 310-424-6622

Harper & Two
9845 Erma Road Suite 201
San Diego, CA 92131

Tel: 619-549-5360
Fax: 619-549-5365

Oregon, Wahington State

Electronic Sources, Inc.
6850 S.W. 105th, Suite B
Beaverton, OR
97008

Tel: 503-627-0838
Fax: 503-627-0238

Electronic Sources, Inc.
1603 116th Ave. NE, Suite 115,
Bellevue, WA 98004

Tel: 206-451-3500
Fax: 206-451-1038

International Sales Representatives

Australia

ACD
Unit 2, 17-19 Melrich Rd.
Bayswater, Victoria
Australia 3153

Tel: 61-3-9762-7644
Fax: 61-3-9762-5446

ACD
106 Belmore Rd.
North Riverwood, NSW
Australia 2210

Tel: 61-2-534-6200
Fax: 61-2-534-4910

ACD
20D William Street,
Norwood, South Australia
Australia

Tel: 61-8-364-2844
Fax: 61-8-364-2811

ACD
Unit 1, Technology Park
Bently, West Australia
Australia

Tel: 61-9-472-3232
Fax: 61-9-470-2303

Belgium, The Netherlands

Microtron
Generaal Dewittelaan 7
2800 Mechelen
Belgium

Tel: 32 1521 2223
Fax: 32 1521 0069

Canada

J-Squared Technologies Inc.
3395 American Dr.
Bldg. 306, Unit 2
Mississauga, Ont.
L4V IT6

Tel: 905-672-2030
Fax: 905-672-2047

J-Squared Technologies Inc.
300 March Road, Suite 501
Kanata, Ontario
K2K 2E2

Tel: 613 592 9540
Fax: 613 592 7051

J-Squared Technologies Inc.
100 Alexis Nihon, Suite 960
Ville St. Laurent, PQ
H4M 2P5

Tel: 514-747-1211
Fax: 514-747-9824

J-Squared Technologies Inc.
4170 Stillcreek Dr., Suite 200
Burnaby, BC
V5C 6C6

Tel: 604-473-4666
Fax: 604-473-4699

J-Squared Technologies Inc.
2723 37th Ave., NE, Suite 206
Calgary, AB
T1Y 5R8

Tel: 403-291-6755
Fax: 403-291-6757

Denmark, Norway, Sweden

IE Komponenter AB
Ulvsundavagen 106C
Box 11113
161 11 Bromma, Sweden

Tel: 46 8 804685
Fax: 46 8 262286

Finland

Integrated Electronics OyAb
Laurinmaenkuja 3
FIN-00440 Helsinki
Finland

Tel: 358-9-586-1770
Fax: 358-9-586-1771

France

Compress
47 Rue de L'Estérel
539 94 633 Rungis CEDEX
FRANCE

Tel: 33 1 41 802902
Fax: 33 1 46 866763

Germany

P I Electronic Engineering, GmbH
Keitlanderstrasse 48
74354 Besegheim-Ottmarsheim,
Germany

Tel: 49 71 4381 1153
Fax: 49 71 4358 853

Hong Kong

Please contact Tundra Semiconductor directly at: 613-592-0714

India

Hynetic Electronics
No. 50, 2nd Cross
Gavipuram Extension,
Bangalore, 560019, India

Tel: 91-80-620852
Fax: 91-80-624073

Israel

Migvan Technologies and Engineering Ltd.
13 Hashiloach St.
PO Box 7022
Petach-Tikva 49170, Israel

Tel: 972-3-9240784
Fax: 972-3-9240787

Italy

EL. CO. MI. S.r.l.
Viale G Matteotti, 26
20095 Cusano Milanino (MI),
Italy

Tel: 39 2 619 6452
Fax: 39 2 613 4836

International Sales Representatives Cont'd

Japan

K.K. Rocky

4-44-11, Nogata
Nakano-ku,
Tokyo, 165 Japan

Tel: 813 3228 4511
Fax: 813 3388 1391

Tokyo Electron Ltd.

TBS Broadcast Center
3-6 Akasaka, 5-Chome
Minato-Ku
Tokyo, 107 Japan

Tel: 81-35561-7216
Fax: 81-35561-7389

Korea

VME Tech Inc.

627-19 Shinsa-dong Kangnam-gu,
5th Floor, Shinsa Building,
Seoul, Korea 135-120

Tel: 82-2-3443-1491
Fax: 82-2-3443-1495

New Zealand

ACD

University Paton NZ Ltd.
Unit 7, 110 Mays Road,
Penrose
Auckland, NZ

Tel: 649-636-5984
Fax: 649-636-5985

Singapore

BBS Electronics

1 Genting Link
#05-04 Perfect Industrial Building
Singapore, 349 518
Singapore

Tel: 65 748 9851
Fax: 65 748 5965

South Africa

Prime Source (Pty) Ltd.

3 Olympia Street
Marlboro, Sandton
South Africa

Tel: 27 11 444 7237
Fax: 27 11 444 7298

Switzerland

Egli, Fischer & Co, Ltd. Zurich

Gotthardstrasse 6
Ch-8022
Zurich, Switzerland

Tel: 41 1 209 81 11
Fax: 41 1 201 22 75

Taiwan

Data Fast Electronics

6 Fl, No 27-1, Alley 169
Kang Ning Street
Hsi Chih
Taipei, Taiwan

Tel: 886 2 6921051
Fax: 886 2 6958240

United Kingdom

Welvar Electronics Ltd.

MBM Box 66
Manor Lane, Rochester
Kent, England ME5 1HS

Tel: 44 1 634 815033
Fax: 44 1 634 832133

Thame Components

Thame Park Road
Thame, Oxfordshire 0X9 3UQ

Tel: 44 1 844 261188
Fax: 44 1 844 261681