UMC

T-52-33-15

UM82C01

Capacitance Keyboard Encoder (CKE)

Features

- 16x8 matrix, can build up to 128 key capacitance keyboard
- Single chip with 16 scan drive outputs and 8 sense inputs
- Two packages 28 pin for 88 key KB and 40 pin for 128 key KB
- Keyboard scanning and encoding under complete control of the user's computer, especially 8048 microcomputer
- Single 5V supply
- High-speed CMOS technology
- Serve as easy interface to 8048
- New CMOS sense technology, CMOS analog sense circuit is built in
- Byte wide sense, higher performance than serial sense technology
- Wide frequency range, 1MHz to 11 MHz 8048 can be used

General Description

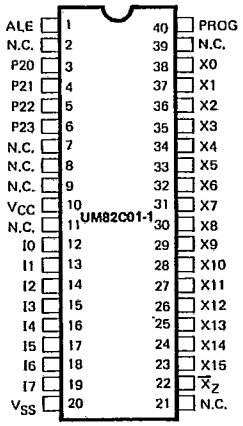
UM82C01 is a CMOS LSI, which offers interface between microcomputer and capacitive keyboard matrix. 40 pin UM82C01-1 is capable of scanning up to 128 low cost capacitive keys. 28 pin UM82C01-2 serves keyboard applications with less than 88 keys.

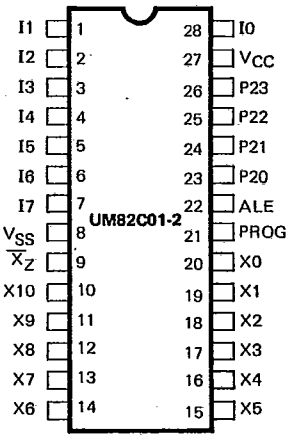
The keyboard scan is under complete control of the 8048 series microcomputer writing to expand I/O port. Port 2 data is multiplexed to initiate one of the scan lines. Sense circuit will receive the scan signal through capacitive keys if one key is pressed. Sense circuit includes CMOS analog and digital circuits which senses action by following amplifying and latching of analog signals from capacitive switches, these 8 data bits are then divided and latched making two nibbles. Two instructions can read these two nibbles from port 2. Then the microcomputer can analyze them and generate the scan code.

Antiscan is used to enhance the simple capacitive switches that are usually used in capacitive keyboards, offering switching threshold in sense input. This provides the keyboard with mechanical hysteresis which is built into the more expensive hall-effect and reed switches.

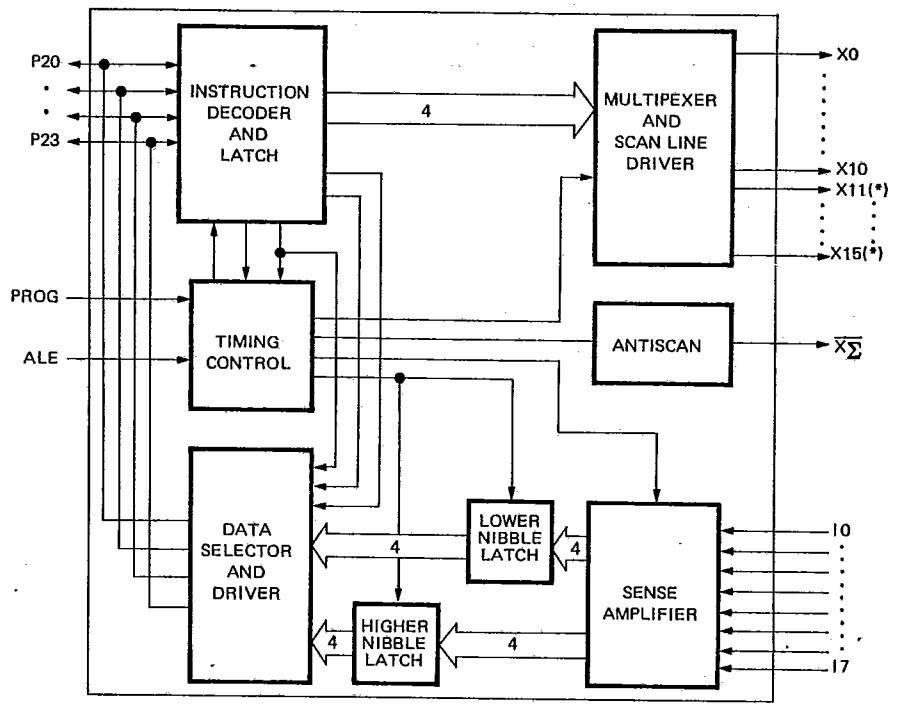
I/O And Peripherals

Pin Configurations





Block Diagram



(*) Only in UM82C01-1

Absolute Maximum Ratings *

Operating Temperature . . . . . 0° to 70°C
Storage Temperature . . . . . −55° to 150°C
Power Supply . . . . . Max. 7V
Voltage on Any Pin . . . . . V_{SS} −0.7V to V_{CC} +0.7V

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(Operating Voltage 5V ± 10%)

Item	Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Digital	Input Low Voltage	V_{IL}	−0.5		0.8	V	
	Input High Voltage	V_{IH}	2.0		V_{CC}	V	
	Output Low Voltage, I/O Port	V_{OLP}			0.45	V	I_{OL} = 5 mA
	Output High Voltage, I/O Port	V_{CHP}	V_{CC}-0.45		V_{CC}	V	I_{OH} = −400μA
	Output Low Voltage, Scan Line	V_{OLS}			0.45	V	I_{OL} = 5 mA
	Output High Voltage, Scan Line	V_{OHS}	V_{CC}-0.45		V_{CC}	V	I_{OH} = −5 mA
Analog	Input High to Reference	ΔV_H	0.1		1.8	V	Lying on Voltage Reference V_{REF}
	Input Low to Reference	ΔV_L	−0.1		−1.8	V	
Operating Current		I_{CC}			15	mA	
Stand by Power Supply Current		I_{SB}			200	μA	No sensing and Scanning

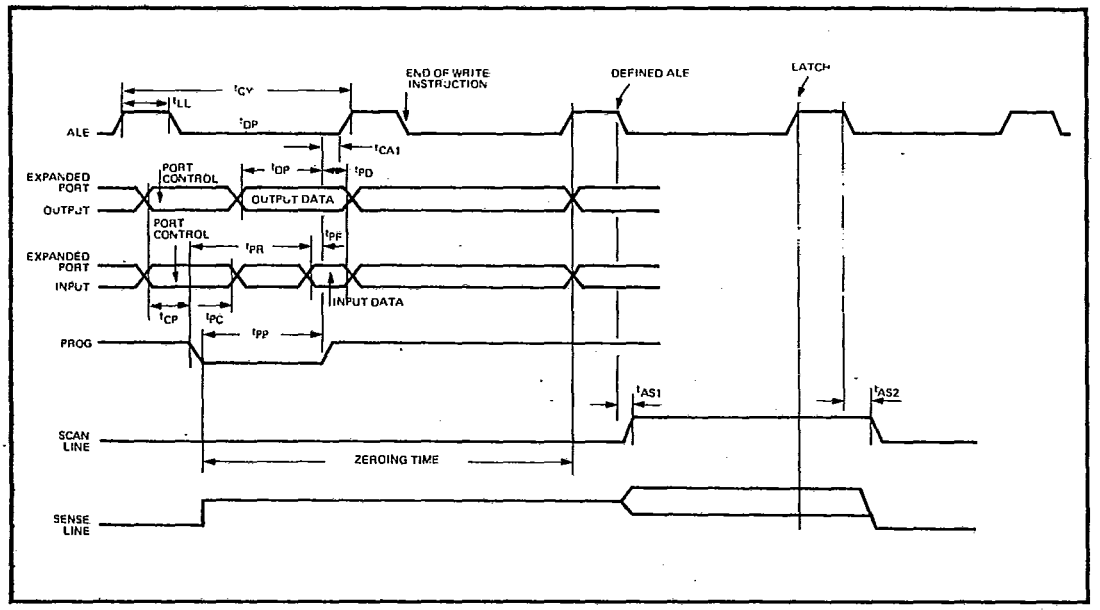
A.C. Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Characteristics	Symbol	UM82C01						Units	Conditions
		4 MHz			11 MHz				
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Address Latch Width	t_{LL}	700			150			ns	
Cycle Time	t_{CY}	3.75			1.36			μs	
Port Control Setup to PROG	t_{CP}	420			100			ns	
Port Control Hold to PROG	t_{PC}	800			160			ns	
Port Output Data Setup	t_{DP}	1350			400			ns	
Port Data Hold from PROG	t_{PD}	320			90			ns	
PROG Strobe to ALE	t_{CAI}	210			50			ns	
PROG Pulse Width	t_{PP}	2370			700			ns	
PROG to Port 2 Input Valid	t_{PR}			2130			700	ns	
Input Data Hold from PROG	t_{PF}			380			140	ns	
ALE to SCAN Setup	t_{AS_1}			200			100	ns	
ALE to SCAN Ended	t_{AS_2}			200			100	ns	

I/O And Peripherals

Timing Diagram



Pin Description

Symbol	Designation	I/O	Description
P20-P23	I/O Port	I/O	This four-bit bidirectional port contains the address and control bits from 8048 μC on a high to low transition of PROG. During a low to high transition of the PROG signal, the port contains the selected scan data for UM82C01 if the last command is a write operation. The sense nibble data from UM82C01 is latched during the low to high transition if the last command is a read operation. There exists a state flow in two continuous read operations which is called "read cycle". Upper nibble coming from sense inputs I4 to I7 is transferred in P20 to P23 from UM82C01 during low to high transition of PROG of MOVD A, P5 instruction, and lower nibble coming from I0 to I3 is transferred in P20 to P23 during low to high transition of PROG of MOVD A, P4 instruction.
ALE	Address Latch Enable Strobe	I	This pin comes direct from 8048 ALE. It is used as the time base as well as address latch strobe. Our target is to let 8048 work between 1 MHz to 11 MHz, so ALE varies from 66.6 KHz to 733.3 KHz. General PC key boards use 4 to 5 MHz 8048, hence, ALE is typically a 266.6 KHz strobe signal for a 4 MHz 8048. When ALE first goes from low to high in a write cycle, the PROG is activated and goes to low and at this time, Port 2 containing port address and write instruction codes is valid and should be latched by UM82C01 to initiate the scan mode.

Pin Description (Continued)

Symbol	Designation	I/O	Description
ALE	Address Latch Enable Strobe	I	UM82C01 begins Zeroing stage of its sense amplifier at this instant. PROG will go to high before second ALE of this write instruction. The Zeroing stage ends at the next ALE low to high transient. Timing Diagram, shows that this edge triggers the selected scan line to be active. The second ALE, which is next to end write instruction, is used to control scan line to inactive and its active transient is the high to low edge. In read cycle, when first ALE goes from high to low, PROG is activated to go to low, port 2 containing port address and read instruction code is valid and should be latched by UM82C01 to initiate the read mode.
PROG	Control Strobe	I	An active low strobe comes direct from 8048 PROG. 8048, PROG is a control strobe to expanded I/O. UM82C01 is designed to locate expanded port 4 and port 5 in 8048. Every time PROG is activated, UM82C01 is initiated in either write or read mode. When PROG goes inactive in a write cycle, selected scan data is valid in port 2 and is latched by UM82C01 to encode the scan line. In a read cycle, latched upper and lower nibbles are valid circularly in port 2 at every PROG low to high transition.
X0-X15	Scan Line Out	O	These are the 16 full range drive outputs. One of the lines is activated in a write cycle. Selected scan data is latched and used to decode these sixteen scan lines so the scanning is fully programmable by 8048. The selected scan line is activated in the defined ALE rising edge and ended in the next ALE falling edge. (Reference to Timing Diagram). The defined ALE is the first ALE after the write insruction is finished. There are eleven scan lines for 28 pin UM82C01-2, X11 to X15 and are included in scan line driver for 40 pin UM82C01-1.
$\overline{X}_Z$	Antiscan Out	O	This is the antiscan output. This output is activated whenever no scanning occurs, and is deactivated when any one of X0 to X15 is activated. Antiscan is used to reduce the voltage in sense input when there is no scanning which prevents logic error.
I0-I7	Sense Line Input	I	These eight lines are inputs from capacitance keyboard matrix. The small current pulses caused by the scan lines and pressed keyswitches are detected here.
V_{CC}	Power Supply	I	Connected to +5V power supply.
V_{SS}	Ground	I	Normally connected to +0V ground.

I/O And Peripherals

Application Description

The Microprocessor

The capacitance keyboard encoder (CKE) UM82C01 is designed to serve as an interface to 8048 series 8-bit microprocessors. The user can control the keyboard function easily through programming of microprocessor, which includes scanning reading and serves as an interface to host computer.

The Keyboard

A keyboard is an aray of switches. The array consists of a two dimensional matrix. One side of the matrix (X-lines) is used to drive the array with a microprocessor chosen signal, while the other side (I-Lines) is connected to sense circuits. In traditional configuration, users make use of mechanical contact switches. With a new sensing mechanism, capacitive switches present a good solution.

The Capacitive Switch

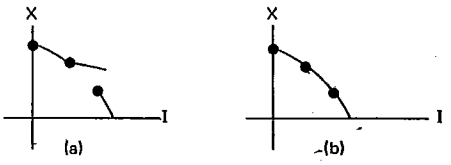


Figure 1. Mechanical Switch (a) Key off (b) Key on

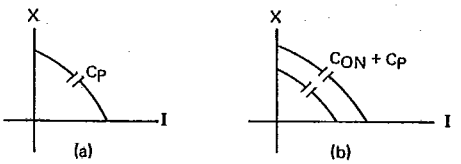
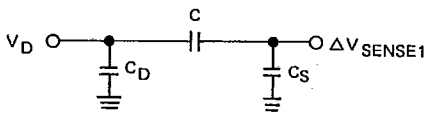


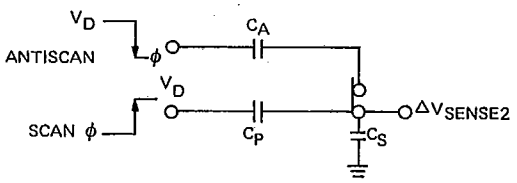
Figure 2. Capacitive Switch (a) Key off (b) key on

Fig. 1 shows the traditional mechanical switch, (a) When the key switch is off, X-lines and I-lines are open to each other, (b) When the key switch is on, X-lines and I-lines short together. Fig. 2, shows the capacitive switch, (a) The key switch is off; only a small parasitic capacitance exists between X-lines and I-lines (b) The key switch is on, a Con + Cp appears between X-lines and I-lines.



$$\Delta V_{SENSE1} = V_D \cdot \frac{\frac{1}{C_S}}{\frac{1}{C_S} + \frac{1}{C}} = V_D \cdot \frac{C}{C_S + C}$$

Figure 3a. Equivalent circuit for Capacitive Key



$$\Delta V_{SENSE2} = V_D \frac{C_P}{C_S + C_P + C_A} - V_D \frac{C_A}{C_S + C_P + C_A}$$

Figure 3b. Equivalent circuit for Capacitive Key with Antiscan Consideration

In Fig. 3a, an equivalent circuit for a capacitive key is shown. The voltage ΔV_{SENSE1} is decided by the scanning voltage V_D, capacitance C and C_S.

In Fig. 3b, an antiscanning consideration is presented. The scanning trigger edge is taking place with the inverse voltage "antiscan". After this edge, the voltage ΔV_{SENSE2} is decided by the voltage divided by C_P minus the voltage divided by C_A.

Writing

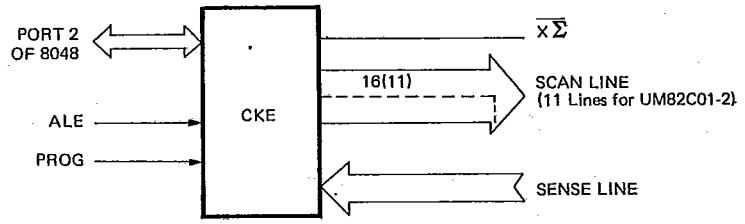


Figure 4. Logic Symbol of the CKE

In system configuration, the CKE is designed to stand in the expanded I/O port of 8048 microcomputer. The CKE uses the PORT 2, ALE and PROG to serve as an interface to the microprocessor. When 8048 writes a scan code to CKE, the CKE must be accessed through the expanded PORT 4. When 8048 reads the sensing code from the CKE, the CKE must be accessed through the expanded PORTS 4 and 5. PORTS 6 and 7 are reserved for the user.

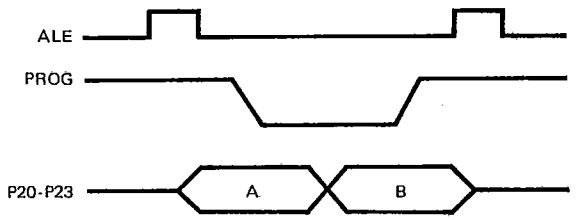


Figure 5. PROG Timing of 8048 I/P PORT Expansion

Address	P21	P20	PORT	Definitions
	0	0	PORT 4	Writing Port
	0	1	PORT 5	(Same as PORT 4)
	1	0	PORT 6	
	1	1	PORT 7	

Instruction	P23	P22	Instruction	Definitions
	0	0	READ	
	0	1	WRITE	Writing Instruction
	1	0	OR	
	1	1	AND	

Figure 6. Expanded Port Definition in Writing Cycle

I/O And Peripherals

By using PORT 4 (PORT 5 the same) of 8048 series microcomputer, the user can write his scanning data to the CKE chip. After the writing, two NOP instructions should be used to permit correct decoding and scanning. The timing diagram is shown in Fig. 7.

For example, if the user wants to scan X_1-line, the recommended Assembly is as listed:

Label	Command	Arguments	Comments
	⋮		
SCAN1:	MOV	A, #ϕ1H	;#ϕ1H Can Vary From ;#$\phi\phi$H To #ϕFH
	MOVD	P4, A	
	NOP		; Wait Until CKE Starts
	NOP		; Scanning.
	⋮		

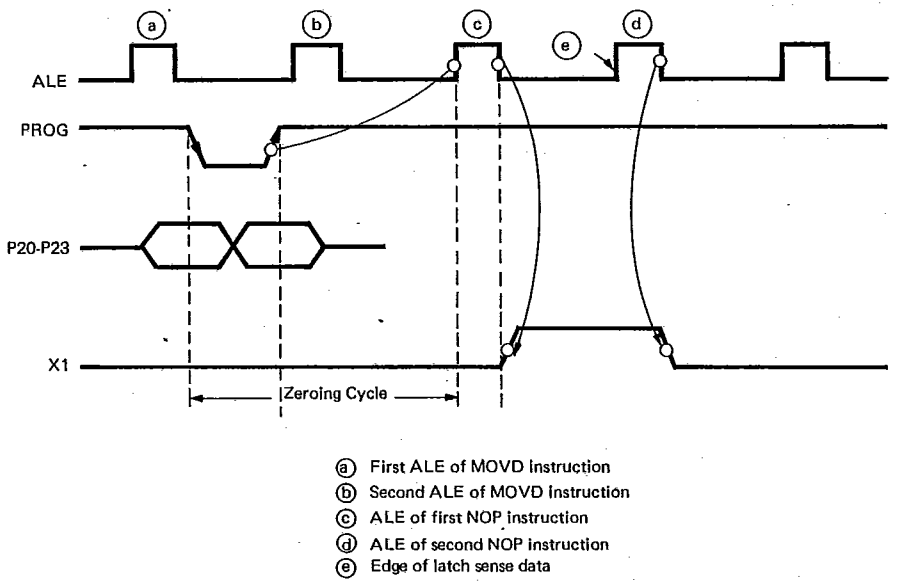


Figure 7. Timing Diagram of Writing and Scanning

Scanning

The CKE latches port address and instruction at the PROG high to low edge in Fig. 7, then enters the writing mode. At the PROG low to high edge, the CKE latches the data in P20–P23 which is now defined as the expanded PORT 4, and decodes the data to select the programmed scan line. Although the decoding and selection does not take much time, the scan line does not activate immediately.

From the PROG falling edge to the rising edge of the ALE, to the MOVD instruction in Fig. 7, the Sense Amplifier of CKE is "Zeroing". After the zeroing cycle, all the sense inputs are balanced at the reference voltage, and the selected scan line is activated at the falling edge of this ALE.

The scanning lines X_0 to X_{15} can each be decoded from the hexadecimal data programmed in PORT 4 at the writing cycle.

The scanning cycle equals an ALE cycle, so the scanning closes at the ALE falling edge of second NOP instruction as shown in Fig. 7. Before the end of scanning, Sense Amplifier will latch the sense data; These will be discussed in the Sensing section.

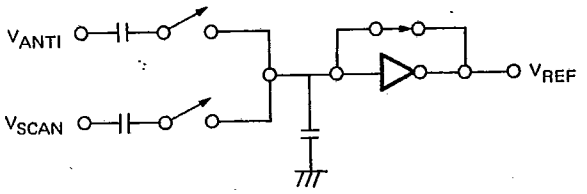
Antiscan

Antiscan line X_Σ is low whenever any scanning is activated, and is high when all scan lines X_0 to X_{15} are low.

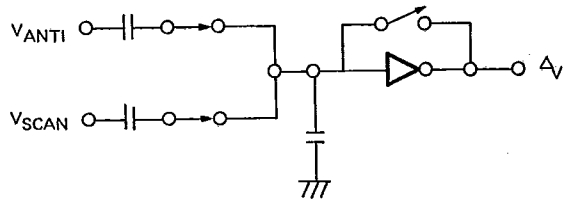
If no key is pressed, the antiscan will generate a $-\Delta V$ to the reference voltage, so that the Sense Amplifier will sense a voltage lower than reference voltage and latch a denoted low after amplification. If any key is pressed and the key is scanned, the voltage divided by the on capacitance will be a $+\Delta V$, so that the Sense Amplifier will sense a voltage higher than reference and latch a logic high after amplification.

The effect on whether antiscanning is larger than scanning depends on whether the key is pressed or not A new CMOS sense technology called "Sense Amplifier" is built in the CKE. In Fig. 8, we show the zeroing and sensing of this technology. In zeroing cycle, the switch between the input and output of the inverter is closed, so the sense input pad equals the reference voltage. After zeroing cycle, the shorting switch at the inverting stage is opened and sensing circuit is activated. In Fig. 7, we can see scanning also starts after zeroing. In fact, sensing is there writing for scanning. During the scanning cycle,

Sensing



(a) Zeroing



(b) Sensing

Fig. 8. Zeroing and Sensing

the CKE will latch the sensing input at the edge in Fig. 7.

The CKE uses byte-wide sensing, and has 8-bit latches. After latching, the data is separated into two nibbles, Higher Nibble and Lower Nibble, and stored.

Reading

Because the CKE serves as an interface to 8048 microcomputer by expanded PORT, the data must be 4-bits wide. Whenever there is data in the latches, the user can read the sensing data in nibble form. The CKE is designed to stand at PORT 4 and PORT 5 in the reading cycle.

I/O And Peripherals

Address	P21	P20	PORT	Definitions
	0	0	PORT 4	Reading Lower Nibble
	0	1	PORT 5	Reading Higher Nibble
	1	0	PORT 6	Not used
	1	1	PORT 7	Not Used

Instruction	P23	P22	Instruction	Definitions
	0	0	Read	Reading Instruction
	0	1	Write	
	1	0	Or	
	1	1	And	

The latched data can be read by 8048 in two read instructions, these two instructions need not but can be continuous, and higher nibble is defined to be read from PORT 5, lower nibble from PORT 4. Users must pay attention for if no reading is instructed before the next writing, UM82C01 will reject the writing instruction until the reading instruction has been executed.

The recommended reading Assembly is as listed and the timing diagram is shown in Fig. 10.

```
Label       Command     Arguments     Comments
                :
Read 1:     MOVD        A, P5         ; Read Higher Nibble
            SWAP        A
            MOV         Rn, A
Read 2:     MOVD        A, P4         ; Read Lower Nibble and
            ORL         A, Rn         ; Combine Nibbles to Byte
                :
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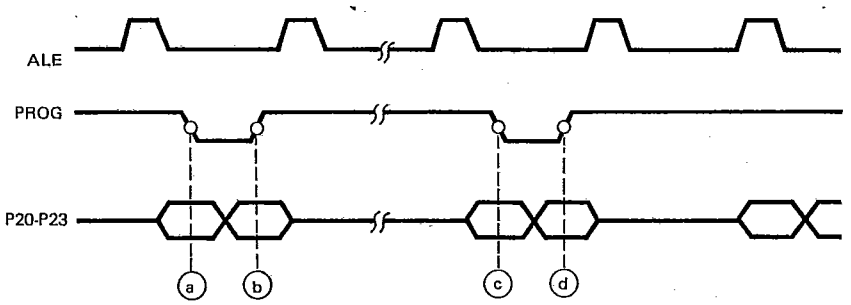


(a) Port address and instruction of READ 1
(b) High nibble output from CKE
(c) Port address and instruction of READ 2
(d) Lower nibble output from CKE

Figure 10. Port Timing of Reading

After the reading cycle, the microcomputer can use the read data to generate scan code or key code easily.

Application Note

UM82C01 is a new solution for capacitance keyboard. The application therefore differs from the present capacitance Con and P. C. board parasitic capacitance Cp of general capacitance keyboards and consideration should be given to design them in. Con and Cp are listed in Table 1. C_S, C_A and C_{BS} are listed in Table 2. Table 3 (a) and (b) are recommendations for capacitance selection.

Table 1. Definition of Con and C_p

Name	Symbol	Min.	Typ.	Max.	Unit
Key on Capacitance	C_{ON}	8	20		pf
P.C.B. Parasitic Capacitance	C_P		1	3	pf

Table 2. Definition of C_S, C_A and C_{BS}

Name	Symbol	Min.	Typ.	Max.	Unit
Shunt Capacitance	C_S		80	150	pf
Antiscan Capacitance	C_A	4		8	pf
Capacitance between two senses	C_{BS}			5	pf

Table 3. Recommended Application of C_A for various C_{ON}

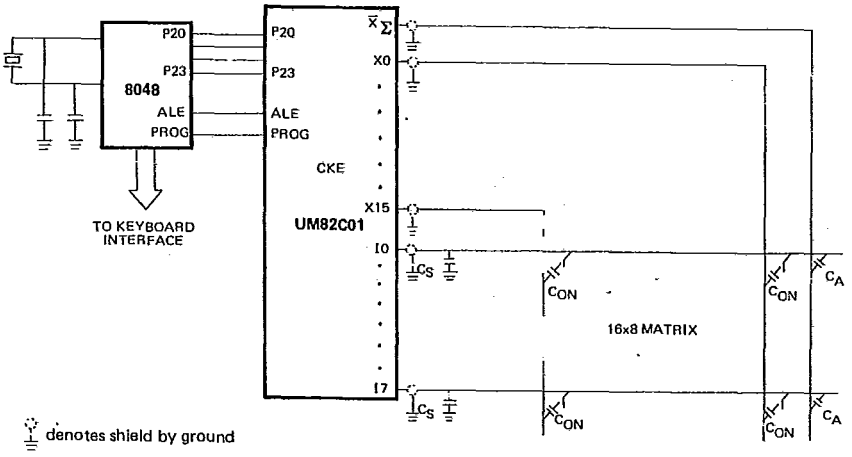
Symbol	Range		Unit
	Lower	Upper	
C_{ON}	10	25	pf
C_A	4	8	pf
C_P	0	3	pf

(a)

Symbol	Range		Unit
	Lower	Upper	
C_{ON}	25	35	pf
C_A	8	15	pf
C_P	0	3	pf

(b)

Typical Application



Ordering Information

Part Number	KB Type	Package
UM82C01–1	128 Key	40 DIP
UM82C01–2	88 Key	28 DIP

I/O And Peripherals