Four-pole Double-throw 5V Low-Resistance Analog Switch IC, CH440G/P/R

Double-pole Double-throw 5V Low-Resistance Analog Switch IC, CH442E

Single-pole Double-throw 5V Low-Resistance Analog Switch IC, CH443K

Double-pole Four-throw 5V Low-Resistance Analog Switch IC, CH444G/P

Single-pole 16-throw, or Differential Channel Double-pole Eight-throw 5V Low-Resistance Analog Switch IC, CH448F

Four-pole Double-throw 3.3V Low-Resistance Analog Switch IC, CH445P

Datasheet
Version: 3B
http://wch.cn

1. Overview

CH440G, CH440P, CH440R, CH442E, CH443K, CH444G, CH444P and CH448F are analog switches with 5V rated supply voltage, high bandwidth and low ON resistance, and support 3.3V or lower supply voltage.

CH445P is an analog switch with 3.3V rated supply voltage, high bandwidth and low ON resistance, and supports 2.5V or lower supply voltage.

CH440G, CH440P, CH440R and CH445P are quad 2:1 bidirectional analog switches with low ON resistance and high bandwidth, quad 2:1 MUX (QPDT), which can be used for video or USB signal one-of-two switch.

CH442E is a dual 2:1 bidirectional analog switch with low ON resistance and high bandwidth, dual 2:1 MUX (QPDT), which can be used for video or USB signal one-of-two switch.

CH443K is a single 2:1 bidirectional analog switch with low ON resistance and high bandwidth, single 2:1 MUX (SPDT), which can be used for video or other signals one-of-two switch, or used for simple logic gate functions such as "AND/OR/NOT", or used for digital signal level switch under 2 voltage domains.

CH444G and CH444P are dual 4:1 bidirectional analog switch with low ON resistance and high bandwidth, dual 4:1 MUX (DPQT), which can be used for video or USB signal one-of-four switch.

CH448F is an 8:1 bidirectional analog switch with a pair of differential signals, low ON resistance and high bandwidth, dual 8:1 MUX (DPOT), which can be used for video or USB signal one-of-eight switch. In addition, 16:1 MUX (one of sixteen) can be achieved by the combined control of 2 channel global enable pins.

2. Features

- Low ON resistance, Ron typical value of about 5 Ω.
- High bandwidth, support video signal, low-speed, full-speed and high-speed USB signals.
- Switch quickly, Ton/Toff typical value is less than 5nS.
- 2KV HBM ESD.
- CH440/CH442/CH444/CH445/CH448 provides global enable pin, and supports multi-channel analog switch unified enable and unified switch.
- CH448 supports differential signals and provides independent global enable pins for both signal channels.
- For CH448, the voltage of the control signals is independent of the supply voltage. CH448 supports 5V, 3.3V and 2.5V control signals.

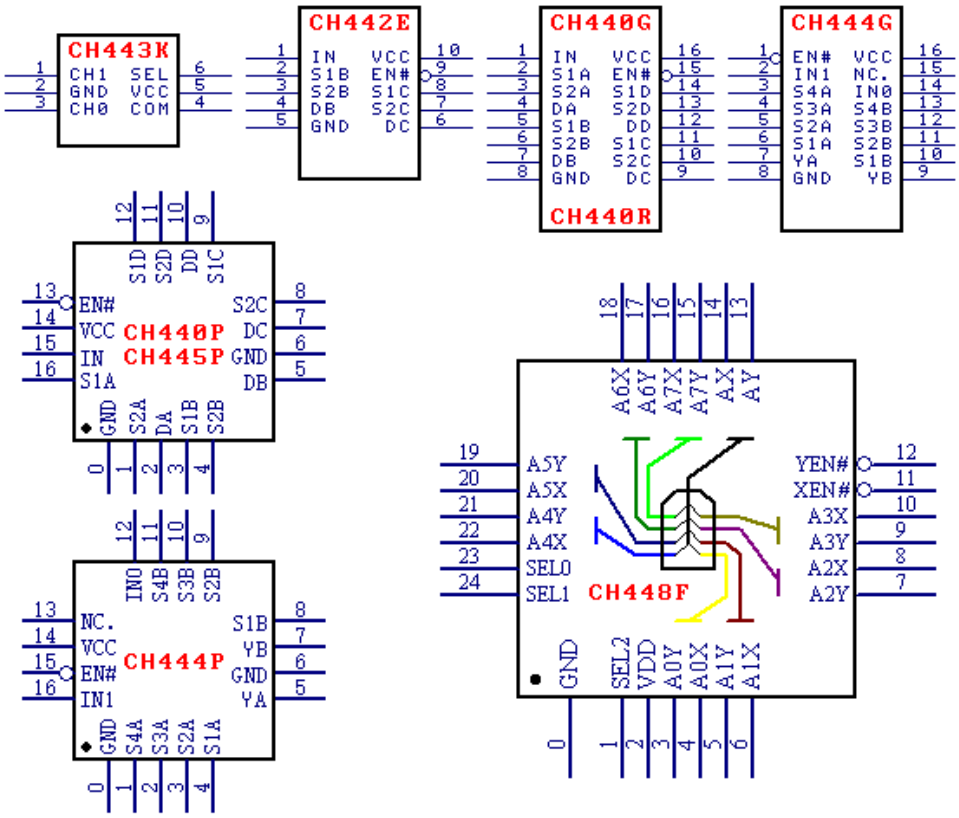
- Wide supply voltage range, low static power dissipation. The 5V switch supports 5V rated supply voltage (5V to 2.5V control signals), available to 2.5V power supply. The 3.3V switch supports 3.3V rated supply voltage (3.3V to 2.5V control signals), available to 1.8V power supply.
- Packages: SOP16, TSSOP16, QFN16, QFN24, MSOP10, SOT363 and others, compatible with RoHS.

3. Package

Package	Body size		Lead pitch		Description	Part No.
SOP16	3.9mm	150mil	1.27mm	50mil	Standard 16-pin patch	CH440G
QFN16	3*3mm		0.50mm	19.7mil	Quad no-lead 16-pin	CH440P
TSSOP16	4.4mm	173mil	0.65mm	25mil	Thin shrink small outline 16-pin patch	CH440R
MSOP10	3.0mm	118mil	0.50mm	19.7mil	Micro small outline 10-pin patch	CH442E
SOT363 SC70-6L	1.25mm	49mil	0.65mm	26mil	Small outline 6-pin patch	CH443K
SOP16	3.9mm	150mil	1.27mm	50mil	Standard 16-pin patch	CH444G
QFN16	3*3mm		0.50mm	19.7mil	Quad no-lead 16-pin	CH444P
QFN16	3*3mm		0.50mm	19.7mil	Quad no-lead 16-pin	CH445P
QFN24	4*4mm		0.50mm	19.7mil	Quad no-lead 24-pin	CH448F

Notes: 1. The CH440E has been replaced by CH442E. They have the same pins and functions.

2. A device with small volume usually has a small parasitic L/C. For high frequency signal applications, it is recommended to first choose devices in small packages such as QFN or SOT.
3. For QFN package, the EPAD is marked as 0# pin. It is necessary to be connected for CH448F.
4. The packing type of CH443K is tray, and the quantity of the devices in each whole tray is 3000. It can be sold at retail, but the quantity will not be counted one by one at retail.
5. As the volume of CH443K is small, the front printed only includes code 43, not full model name.



4. Pin definitions

4.1. CH440G/P/R, CH445P

CH440G CH440R	CH440P CH445P	Pin Name	Pin Type	Pin Description
16	14	VCC	Power	Positive power
8	6, 0	GND	Power	Ground, digital signal reference ground
15	13	EN#	Input	Global enable input, active low
1	15	IN	Input	2:1 analog switch selection input: Select 2# (S2x) when at high level; Select 1# (S1x) when at low level.
4, 7, 9, 12	2, 5, 7, 10	DA, DB, DC, DD	Analog signal	Common terminal of 2:1 analog switch
2, 5, 11, 14	16, 3, 9, 12	S1A, S1B, S1C, S1D	Analog signal	1# of 2:1 analog switch Selected when IN pin inputs low
3, 6, 10, 13	1, 4, 8, 11	S2A, S2B, S2C, S2D	Analog signal	2# of 2:1 analog switch Selected when IN pin inputs high

4.2. CH442E

Pin No.	Pin Name	Pin Type	Pin Description
10	VCC	Power	Positive power
5	GND	Power	Ground, digital signal reference ground
9	EN#	Input	Global enable input, active low
1	IN	Input	2:1 analog switch selection input: Select 2# (S2x) when at high level; select 1# (S1x) when at low level
4, 6	DB, DC	Analog signal	Common terminal of 2:1 analog switch
2, 8	S1B, S1C	Analog signal	1# of 2:1 analog switch, selected when IN pin inputs
3, 7	S2B, S2C	Analog signal	2# of 2:1 analog switch, selected when IN pin inputs high

4.3. CH443K

Pin No.	Pin Name	Pin Type	Pin description
5	VCC	Power	Positive power
2	GND	Power	Ground, digital signal reference ground
6	SEL (IN)	Input	2:1 analog switch selection input: CH1 selected when at high level. CH0 selected when at low level
4	COM (DB)	Analog signal	Common terminal of 2:1 analog switch
3	CH0 (S1B)	Analog signal	CH0 of 2:1 analog switch, selected when SEL pin inputs low
1	CH1 (S2B)	Analog signal	CH1 l of 2:1 analog switch, selected when SEL pin inputs high

4.4. CH444G and CH444P

CH444G	CH444P	Pin Name	Pin Type	Pin Description
16	14	VCC	Power	Positive power
8	6, 0	GND	Power	Ground, digital signal reference ground

1	15	EN#	Input	Global enable input, active low
2, 14	16, 12	IN1, IN0	Input	4:1 analog switch selection input: Select 1# (S1x) at 00; Select 2# (S2x) at 01; Select 3# (S3x) at 10; Select 4# (S4x) at 11
7, 9	5, 7	YA, YB	Analog signal	Common terminal of 4:1 analog switch
6, 10	4, 8	S1A, S1B	Analog signal	1# of 4:1 analog switch, selected when IN1&0 pins input 00
5, 11	3, 9	S2A, S2B	Analog signal	2# 4:1 analog switch, selected when IN1&0 pins input 01
4, 12	2, 10	S3A, S3B	Analog signal	3# of 4:1 analog switch, selected when IN1&0 pins input 10
3, 13	1, 11	S4A, S4B	Analog signal	4# of 4:1 analog switch, selected when IN1&0 pins input 11
15	13	NC.	No connection	Reserved pin. Do not connect it

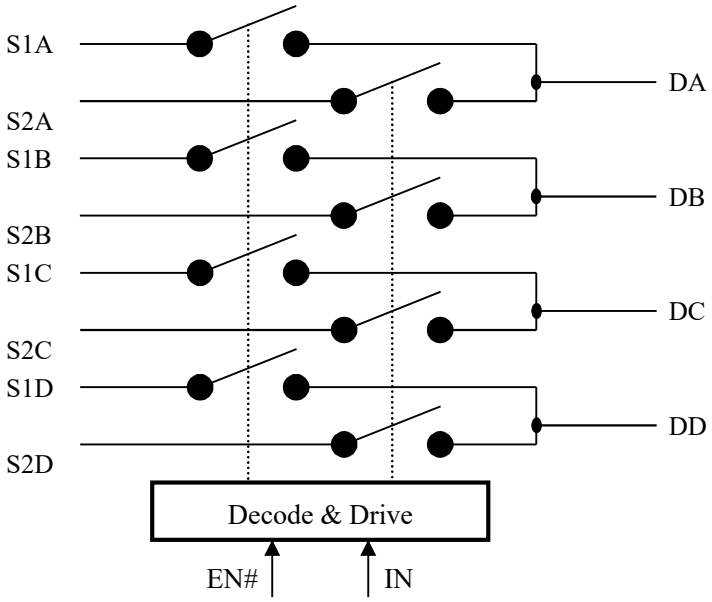
4.5. CH448F

Pin No.	Pin Name	Pin Type	Pin Description
2	VDD	Power	Positive power
0	GND	Power	Ground, digital signal reference ground
11	XEN#	Input	Channel X global enable input, active low
12	YEN#	Input	Channel Y global enable input, active low
1, 24, 23	SEL2, SEL1, SEL0	Input	8:1 analog switch selection input: Select 0# (A0*) at 000 ; Select 1# (A1*) at 001; Select 2# (A2*) at 010 ; Select 3# (A3*) at 011; Select 4# (A4*) at 100 ; Select 5# (A5*) at 101; Select 6# (A6*) at 110 ; Select 7# (A7*) at 111
14	AX	Analog signal	Common terminal of X-channel 8:1 analog switch
13	AY	Analog signal	Common terminal of Y-channel 8:1 analog switch
4, 3	A0X, A0Y	Analog signal	0# of 8:1 analog switch, selected when SEL2&1&0 pins input 000
6, 5	A1X, A1Y	Analog signal	1# of 8:1 analog switch, selected when SEL2&1&0 pins input 001
8, 7	A2X, A2Y	Analog signal	2# of 8:1 analog switch, selected when SEL2&1&0 pins input 010
10, 9	A3X, A3Y	Analog signal	3# of 8:1 analog switch, selected when SEL2&1&0 pins input 011
22, 21	A4X, A4Y	Analog signal	4# of 8:1 analog switch, selected when SEL2&1&0 pins input 100
20, 19	A5X, A5Y	Analog signal	5# of 8:1 analog switch, selected when SEL2&1&0 pins input 101
18, 17	A6X, A6Y	Analog signal	6# of 8:1 analog switch, selected when SEL2&1&0 pins input 110
16, 15	A7X, A7Y	Analog signal	7# of 8:1 analog switch, selected when SEL2&1&0 pins input 111

5. Functional description

5.1. CH440G/P/R, CH445P

CH440G, CH440P, CH440R and CH445P are QPDT analog switches, including a quad single-pole double-throw 2:1 switch.

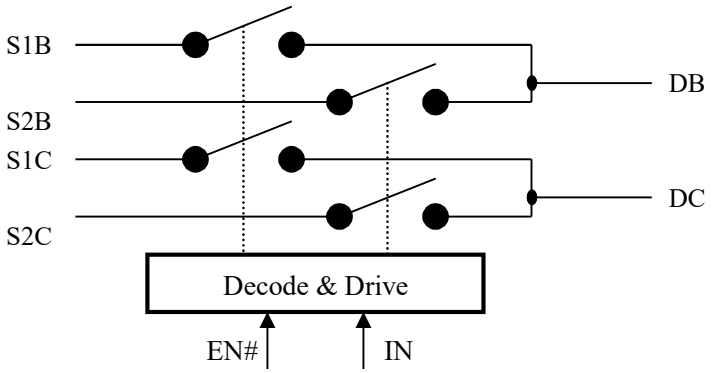


CH440G, CH440P, CH440R and CH445P are controlled by the EN# pin to implement unified enabled, and selected by IN pin to implement unified switch. The following table is the control table.

EN#	IN	DA	DB	DC	DD
0	0	Select S1A	Select S1B	Select S1C	Select S1D
0	1	Select S2A	Select S2B	Select S2C	Select S2D
1	X	All off	All off	All off	All off

5.2. CH442E

CH442E is DPDT analog switch, with a dual single-pole double-throw 2:1 switch.

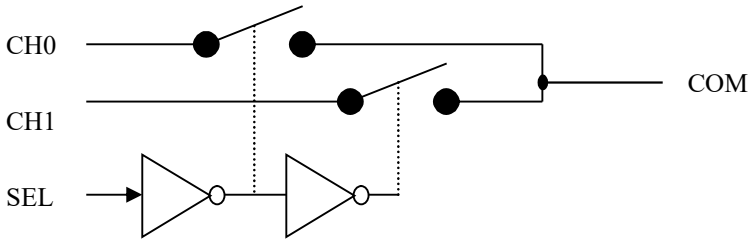


CH442E is controlled by the EN# pin to implement unified enabled, and selected by IN pin to implement unified switch. The following table is the control table.

EN#	IN	DB	DC
0	0	Select S1B	Select S1C
0	1	Select S2B	Select S2C
1	X	All off	All off

5.3. CH443K

CH443K is a single-pole double-throw (SPDT) analog switch, and can be used for simple logic gate functions such as "AND/OR/NOT" and for digital signal level switch under 2 voltage domains.

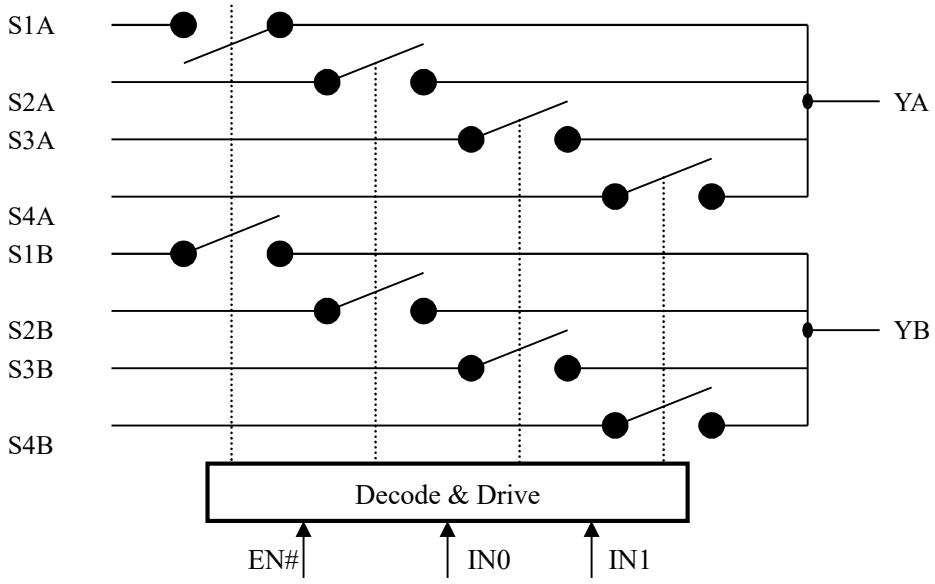


CH443K is selected by SEL pin to implement switch. The following table is its control table.

SEL	COM
0	Select CH0
1	Select CH1

5.4. CH444G, CH444P

CH444G and CH444P are DPQT analog switches, with a dual single-pole four-throw 4:1 switch.



CH444G and CH444P are controlled by the EN# pin to implement unified enabled, and selected by IN1 and IN0 pins to implement unified switch. The following table is its control table.

EN#	IN1	IN0	YA	YB
0	0	0	Select S1A	Select S1B
0	0	1	Select S2A	Select S2B
0	1	0	Select S3A	Select S3B
0	1	1	Select S4A	Select S4B
1	X	X	All off	All off

5.5. CH448F

CH448F is DPOT analog switch, with a dual single-pole eight-throw 8:1 switch.

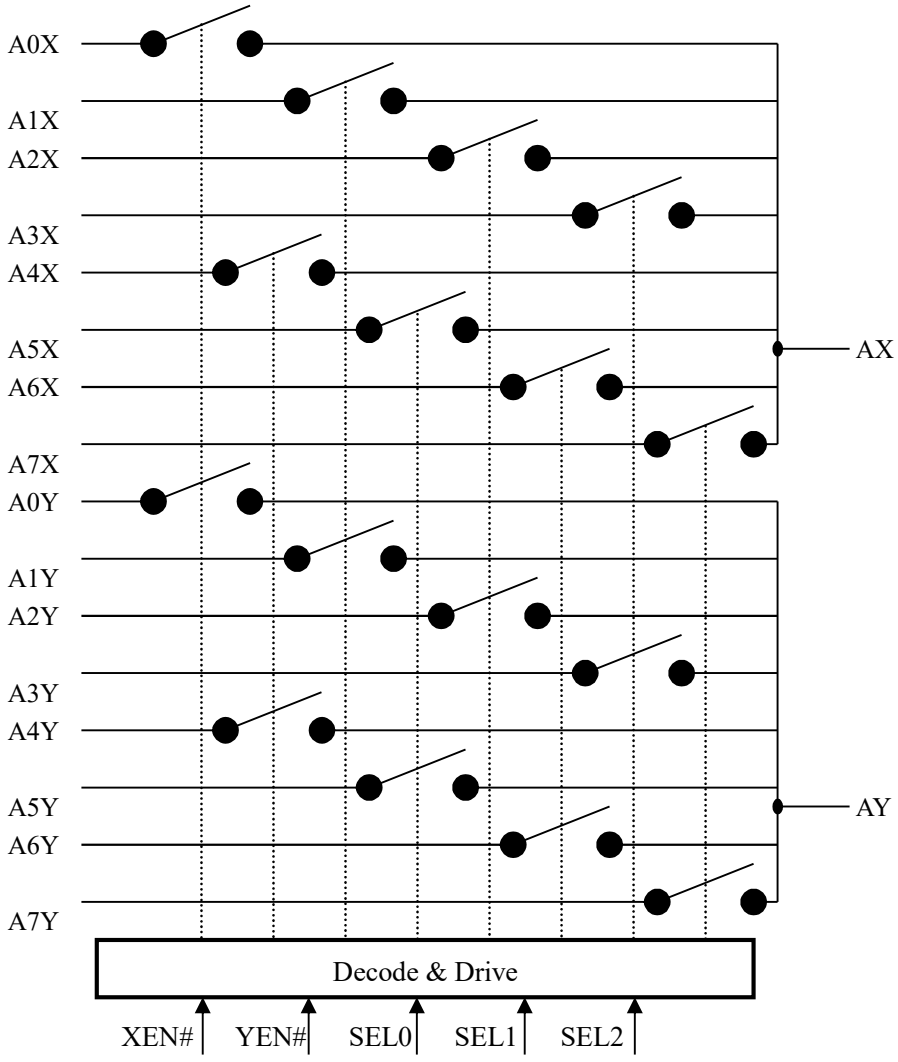
The AX and AY channels can be enabled independently. When they are not enabled simultaneously and they are shorted as a common terminal, they can form a single-pole 16-throw 16:1 switch. In this case, the analog signal bandwidth drops to about 250MHz.

When the AX and AY channels are uniformly enabled, a high-speed differential channel is formed. The X and Y differential signals can be set to +/- (p/n) or the inverse according to PCB design optimization requirements.

The digital input pins of CH448F include SEL2, SEL1, SEL0, XEN# and YEN#. Their signals are usually driven by the I/O of the external MCU. The voltage on the above digital input pins can be independent of the supply voltage VDD of CH448F.

Combination of CH448F supply voltage and digital pin control voltage		CH448F supply voltage VDD, maximum voltage of analog signal		
		5V	3.3V	2.5V
I/O voltage of MCU (voltage on CH448F digital input pins)	5V	√	√	√
	3.3V	Function support	√	√
	2.5V	Function support	Function support	√
	1.8V	×	Function support	Function support

Note: “Function support” in the table above refers that function is implemented completely, but CH448F may have a static power dissipation of not more than 600uA.



In the differential channel one-of-eight mode, CH448F is controlled by XEN# and YEN# pins that are shorted to implement unified enable, and selected by SEL2, SEL1 and SEL0 pins to implement unified switch. The following table is the control table.

XEN#	YEN#	SEL2	SEL1	SEL0	AX	AY
0		0	0	0	Select A0X	Select A0Y
0		0	0	1	Select A1X	Select A1Y
0		0	1	0	Select A2X	Select A2Y
0		0	1	1	Select A3X	Select A3Y
0		1	0	0	Select A4X	Select A4Y
0		1	0	1	Select A5X	Select A5Y
0		1	1	0	Select A6X	Select A6Y
0		1	1	1	Select A7X	Select A7Y
1		X	X	X	All off	All off

In the single-ended signal one-of-16 mode, AX and AY are shorted as the common terminal of the analog switch. CH448F is controlled by XEN# and YEN# pins independently to implement asynchronous enable, and selected by SEL2, SEL1 and SEL0 pins to implement one-of-16 switch. The following table is the control table.

XEN#	YEN#	SEL2	SEL1	SEL0	AX	AY
0	1	0	0	0	Select A0X	
0	1	0	0	1	Select A1X	
0	1	0	1	0	Select A2X	
0	1	0	1	1	Select A3X	
0	1	1	0	0	Select A4X	
0	1	1	0	1	Select A5X	
0	1	1	1	0	Select A6X	
0	1	1	1	1	Select A7X	
1	0	0	0	0		Select A0Y
1	0	0	0	1		Select A1Y
1	0	0	1	0		Select A2Y
1	0	0	1	1		Select A3Y
1	0	1	0	0		Select A4Y
1	0	1	0	1		Select A5Y
1	0	1	1	0		Select A6Y
1	0	1	1	1		Select A7Y
1	1	X	X	X	All off	

6. Parameters

6.1. Absolute maximum ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Symbol	Parameter description	Min.	Max.	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-55	125	℃

VCC	Supply voltage of a 5V device (VCC/VDD connects to power, GND to ground)	-0.5	6.5	V
VCC	Supply voltage of a 3.3V device (VCC/VDD connects to power, GND to ground)	-0.5	4.4	V
VIO	Voltage on digital or analog input/output pins	-0.5	VCC+0.4	V
VID8	Voltage on CH448 digital input pins (not related to VDD)	-0.5	6.5	V
Isw	Continuous through current of the analog switch	0	30	mA
Iall	Total continuous through current of all analog switches	0	120	mA

6.2. Electrical characteristics of 5V (rated) switch @5V

Test conditions: TA=25℃, VCC=VDD=5V, excluding CH445

Symbol	Parameter description	Min.	Typ.	Max.	Unit
VCC	VCC/VDD supply voltage	4.0	5.0	5.5	V
ICC	Static supply current, with all digital pins connected to VCC or GND		0.1	10	uA
ICCX	Static supply current, with all digital pins at 3.4V		0.5	2	mA
VIL	Low level input voltage of digital pin	0		1.0	V
VIH	High level input voltage of digital pin	2.0		VCC	V
VIL8	Low level input voltage of CH448 digital pin	0		1.1	V
VIH8	High level input voltage of CH448 digital pin	2.2		5.5	V
ILEAK	Input leakage current of digital pin		0.1	10	uA
IOFF	Leakage current of analog switch in off state		±0.01	±1	uA
VANA	Recommended voltage range of analog signal	0		2.8	V
VANAX	Allowed voltage range of analog signal	-0.3		VCC+0.3	V
RON1	Analog switch ON resistance, with analog signal voltage of 0V		4	6	Ω
RON2	Analog switch ON resistance, with analog signal voltage of 2V		5	8	Ω
RON3	Analog switch ON resistance, with analog signal voltage of 3.4V		11	16	Ω
RON4	Analog switch ON resistance, with analog signal voltage of 5V		8	12	Ω

6.3. Electrical characteristics of 5V (rated) switch @3.3V

Test conditions: TA=25℃, VCC=VDD=3.3V, excluding CH445

Symbol	Parameter description	Min.	Typ.	Max.	Unit
VCC3	VCC/VDD supply voltage	2.1	3.3	3.9	V
ICC3	Static supply current, with all digital pins connected to VCC or GND		0.1	5	uA
ICCX3	Static supply current, with all digital pins at 2.3V		0.3	1	mA
VIL3	Low level input voltage of digital pin	0		0.7	V
VIH3	High level input voltage of digital pin	1.8		VCC3	V
VIL38	Low level input voltage of CH448 digital pin	0		0.7	V
VIH38	High level input voltage of CH448 digital pin	1.8		5.5	V

ILEAK3	Input leakage current of digital pin		0.1	5	uA
IOFF3	Leakage current of analog switch in off state		±0.005	±0.5	uA
VANA3	Recommended voltage range of analog signal	0		1.5	V
VANAX3	Allowed voltage range of analog signal	-0.3		VCC3+0.3	V
RON1	Analog switch ON resistance, with analog signal voltage of 0V		5	9	Ω
RON2	Analog switch ON resistance, with analog signal voltage of 1.2V		9	14	Ω
RON3	Analog switch ON resistance, with analog signal voltage of 2.0V		23	30	Ω
RON4	Analog switch ON resistance, with analog signal voltage of 3.3V		10	15	Ω

6.4. Timing parameters of 5V (rated) analog switch

Test conditions: TA=25℃, VCC=VDD=5V, VANA=0V, excluding CH445

Symbol	Parameter description	Min.	Typ.	Max.	Unit
CIN	Digital input pin capacitance, F=1MHz		4	8	pF
COFF	Analog signal pin capacitance when the switch is off, F=1MHz		6	10	pF
CON	Analog signal pin capacitance when the switch is on, F=1MHz		9	14	pF
CON4	Analog pin capacitance when CH444 switch is on, F=1MHz		13	19	pF
BW	Analog switch -3dB bandwidth	400	550		MHz
BW4	CH444 analog switch -3dB bandwidth	300	400		MHz
TON	Analog switch ON delay, RL=75Ω, CL=10pF		3	7	nS
TOFF	Analog switch OFF delay, RL=75Ω, CL=10pF		2	7	nS

6.5. Electrical characteristics of 3.3V (rated) switch @3.3V

Test conditions: TA=25℃, VCC=3.3V, only for CH445

Symbol	Parameter description	Min.	Typ.	Max.	Unit
VCC	Supply voltage	2.9	3.3	3.7	V
ICC	Static supply current, with all digital pins connected to VCC or GND		0.1	6	uA
ICCX	Static supply current, with all digital pins at 2.3V		0.07	0.3	mA
VIL	Low level input voltage of digital pin	0		0.9	V
VIH	High level input voltage of digital pin	2.0		VCC	V
ILEAK	Input leakage current of digital pin		0.1	6	uA
IOFF	Leakage current of analog switch in off state		±0.01	±1	uA
VANA	Recommended voltage range of analog signal	0		2.0	V
VANAX	Allowed voltage range of analog signal	-0.3		VCC+0.3	V
RON1	Analog switch ON resistance, with analog signal voltage of 0V		3.5	6	Ω

RON2	Analog switch ON resistance, with analog signal voltage of 1.5V		4.5	8	Ω
RON3	Analog switch ON resistance, with analog signal voltage of 2.3V		7	11	Ω
RON4	Analog switch ON resistance, with analog signal voltage of 3.3V		5.5	9	Ω

6.6. Electrical characteristics of 3.3V (rated) switch @2.5V

Test conditions: TA=25℃, VCC=2.5V, only for CH445

Symbol	Parameter description	Min.	Typ.	Max.	Unit
VCC2	Supply voltage	1.5	2.5	2.8	V
ICC2	Static supply current, with all digital pins connected to VCC or GND		0.05	3	uA
ICCX2	Static supply current, with all digital pins at 1.8V		0.04	0.2	mA
VIL2	Low level input voltage of digital pin	0		0.7	V
VIH2	High level input voltage of digital pin	1.5		VCC2	V
ILEAK2	Input leakage current of digital pin		0.05	3	uA
IOFF2	Leakage current of analog switch in off state		±0.005	±0.5	uA
VANA2	Recommended voltage range of analog signal	0		1.3	V
VANAX2	Allowed voltage range of analog signal	-0.3		VCC2+0.3	V
RON1	Analog switch ON resistance, with analog signal voltage of 0V		4.5	7	Ω
RON2	Analog switch ON resistance, with analog signal voltage of 1.1V		6	9	Ω
RON3	Analog switch ON resistance, with analog signal voltage of 1.8V		11	16	Ω
RON4	Analog switch ON resistance, with analog signal voltage of 2.5V		7.5	11	Ω

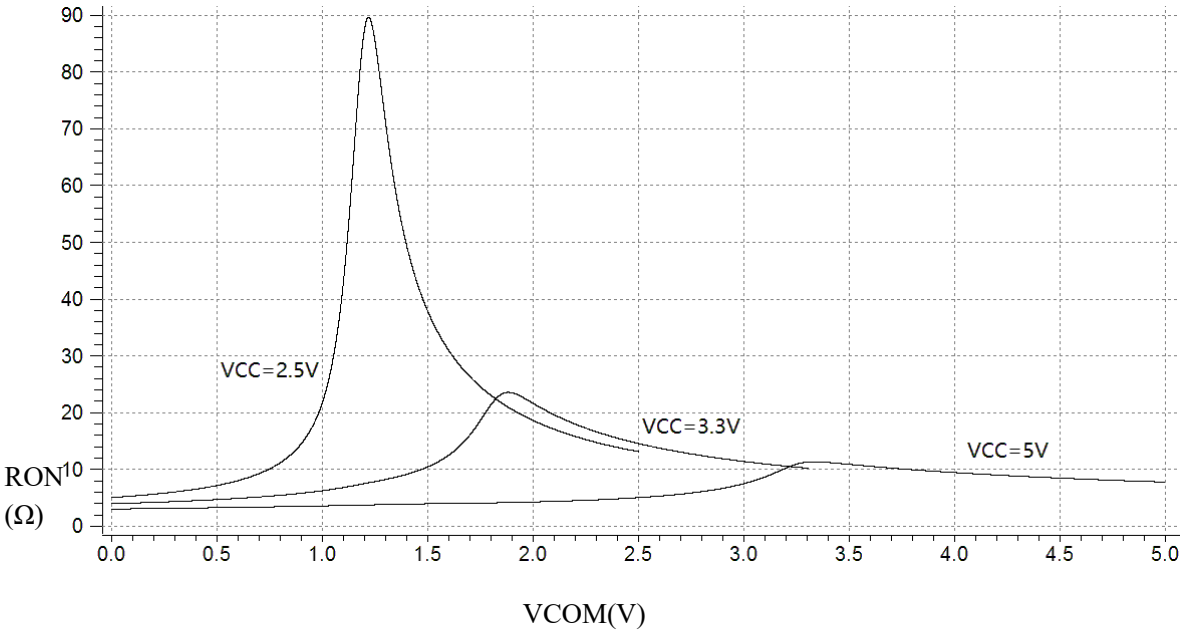
6.7. Timing parameters of 3.3V (rated) analog switch

Test conditions: TA=25℃, VCC=3.3V, VANA=0V, only for CH445

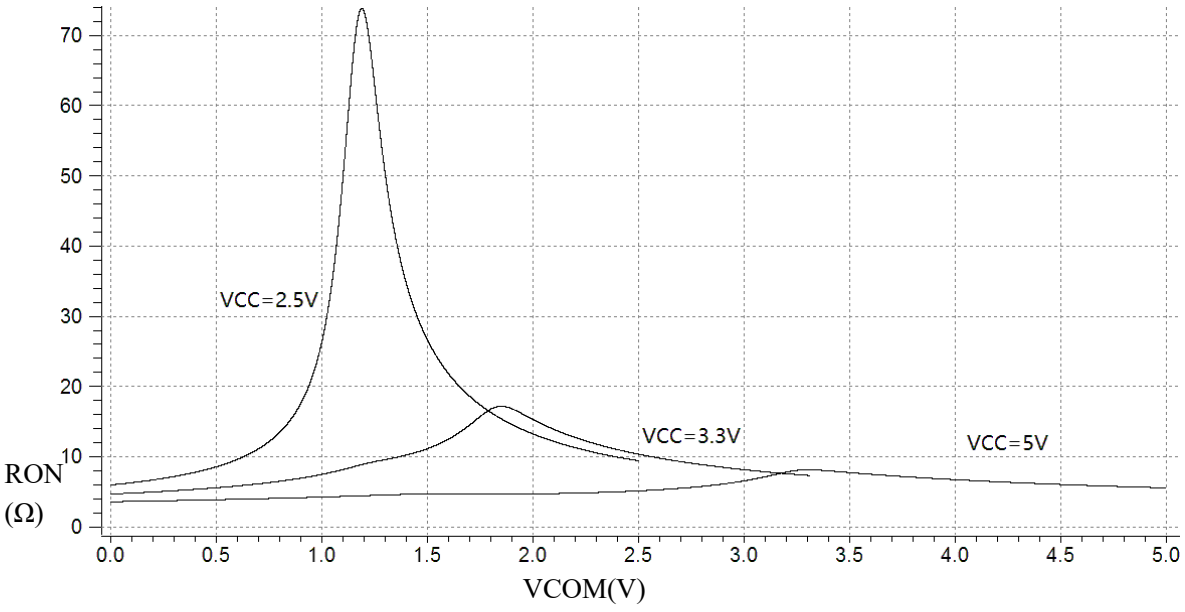
Symbol	Parameter description	Min.	Typ.	Max.	Unit
CIN	Digital input pin capacitance, F=1MHz		3	6	pF
COFF	Analog signal pin capacitance when the switch is off, F=1MHz		6	10	pF
CON	Analog signal pin capacitance when the switch is on, F=1MHz		9	15	pF
BW	Analog switch -3dB bandwidth	400	500		MHz
TON	Analog switch ON delay, RL=75Ω, CL=10pF		2.5	5	nS
TOFF	Analog switch OFF delay, RL=75Ω, CL=10pF		1.8	5	nS

6.8. Characteristic diagram

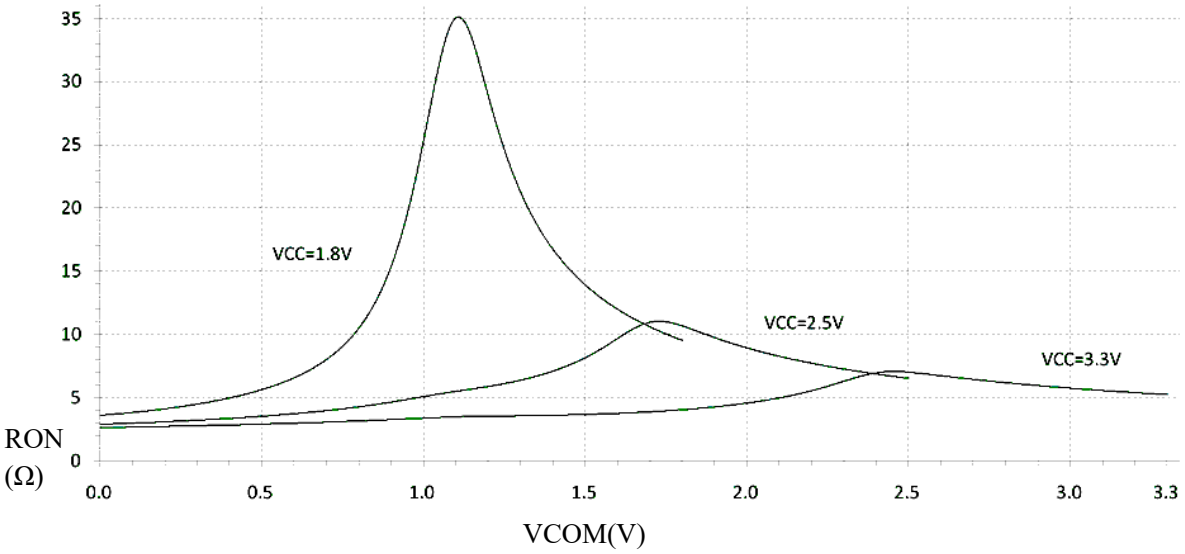
6.8.1 Correlation between analog switch ON resistance RON and analog signal voltage VCOM of CH440 and CH444 (TA=25℃)



6.8.2 Correlation between analog switch ON resistance RON and analog signal voltage VCOM of CH442, CH443 and CH448 (TA=25℃)



6.8.3 Correlation between analog switch ON resistance RON and analog signal voltage VCOM of CH445 (TA=25℃)



7. Applications

7.1. Video signal switch

The CH440, CH442, CH443, CH444, CH445 and CH448 feature high bandwidth and low resistance, more suitable for video signal switch, such as selecting from dual or quad video signal sources.

As the analog circuit and the digital circuit share VCC/VDD and GND, the GND pin must be in good connection, and the VCC/VDD pin must be connected to an external decoupling capacitor, to reduce interference. It is also recommended to appropriately reduce the edge angle of the digital input signal, to reduce transmission frequency.

7.2. USB signal switch

CH440, CH442, CH443, CH444, CH445 and CH448 support low-speed, full-speed and high-speed USB signal switch. The CH445 is preferred for 3.3V supply voltage. For super-speed USB3.0 signal switch, please refer to CH482/CH483 datasheet.

7.3. CH443 single logic gate function

Abbreviation	Description	SEL	CH0	CH1	COM
BUF	Buffer of strong drive push-pull output	Input A	To GND	To VCC	Output = A
INV	Inverter of strong drive push-pull output	Input A	To VCC	To GND	Output = ! A
AND	AND gate	Input A	To GND	Input B	Output = A & B
IAND	First NOT, then AND	Input A	Input B	To GND	Output = ! A & B
OR	OR gate	Input A	Input B	To VCC	Output = A | B
IOR	First NOT, then OR	Input A	To VCC	Input B	Output = ! A | B
MUX	Multiplexer	Input S	Input A	Input B	Output = S ? B : A
BUF_OD	Buffer of open-drain (open source) output	Input A	To GND	Suspend	Output = A ? z : 0
INV_OD	Inverter of open-drain (open source) output	Input A	Suspend	To GND	Output = A ? 0 : z

TLBUF	Three-state output gate of low enable output	Input OE	Input A	Suspend	Output = ! OE ? A : z
THBUF	Three-state output gate of high enable output	Input OE	Suspend	Input A	Output = OE ? A : z

7.4. CH443 digital signal level switch

CH443 can be used for single digital signal level switch, supports boost and buck. SEL is a digital signal input pin, and COM is a digital signal output pin. The SEL signal is usually driven by I/O of the external MCU, and the voltage can be independent of CH443 supply voltage (VCC). The signal amplitude of COM terminal is determined by value of voltage connected with CH0 and CH1, and the voltage of CH0 and CH1 must be less than or equal to CH443 supply voltage (VCC).

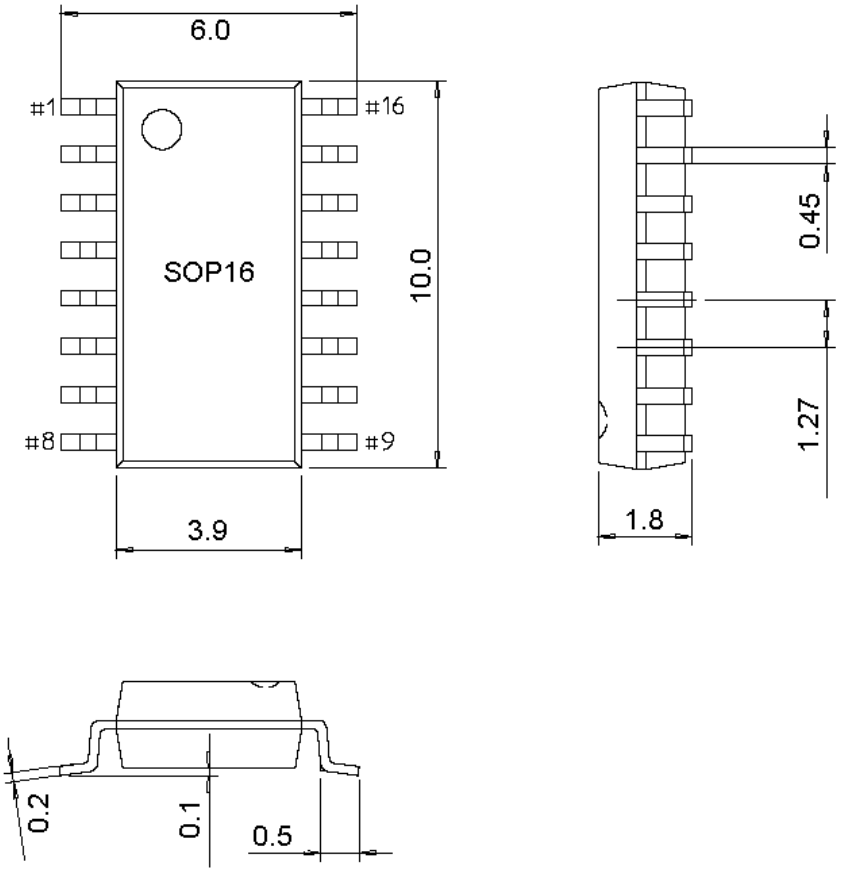
Source control voltage	Target voltage	CH443 supply voltage VCC	SEL input	CH0	CH1	COM output
5V	3.3V	5V or 3.3V	0/5V	To GND	To 3.3V	SEL buck 5->3.3
5V	2.5V	5V or 3.3V or 2.5V	0/5V	To GND	To 2.5V	SEL buck 5->2.5
5V	1.8V	5V or 3.3V or 2.5V	0/5V	To GND	To 1.8V	SEL buck 5->1.8
3.3V	2.5V	3.3V or 5V or 2.5V	0/3.3V	To GND	To 2.5V	SEL buck 3.3->2.5
3.3V	1.8V	3.3V or 5V or 2.5V	0/3.3V	To GND	To 1.8V	SEL buck 3.3->1.8
2.5V	1.8V	2.5V or 3.3V or 5V	0/2.5V	To GND	To 1.8V	SEL buck 2.5->1.8
3.3V	5V	5V	0/3.3V	To GND	To 5V	SEL boost 3.3->5
2.5V	5V	5V	0/2.5V	To GND	To 5V	SEL boost 2.5->5
1.8V	5V	5V	0/1.8V	To GND	To 5V	Available, but not recommended
2.5V	3.3V	3.3V or 5V	0/2.5V	To GND	To 3.3V	SEL boost 2.5->3.3
1.8V	3.3V	3.3V or 5V	0/1.8V	To GND	To 3.3V	SEL boost 1.8->3.3
1.8V	2.5V	2.5V or 3.3V or 5V	0/1.8V	To GND	To 2.5V	SEL boost 1.8->2.5
Same as above	Same as above	Same as above	Same as above	Swap CH0 and CH1 as above		Inverted buck or boost

Note: When the source control voltage is less than CH443 supply voltage (VCC), CH443 may have static power dissipation of not more than 600uA.

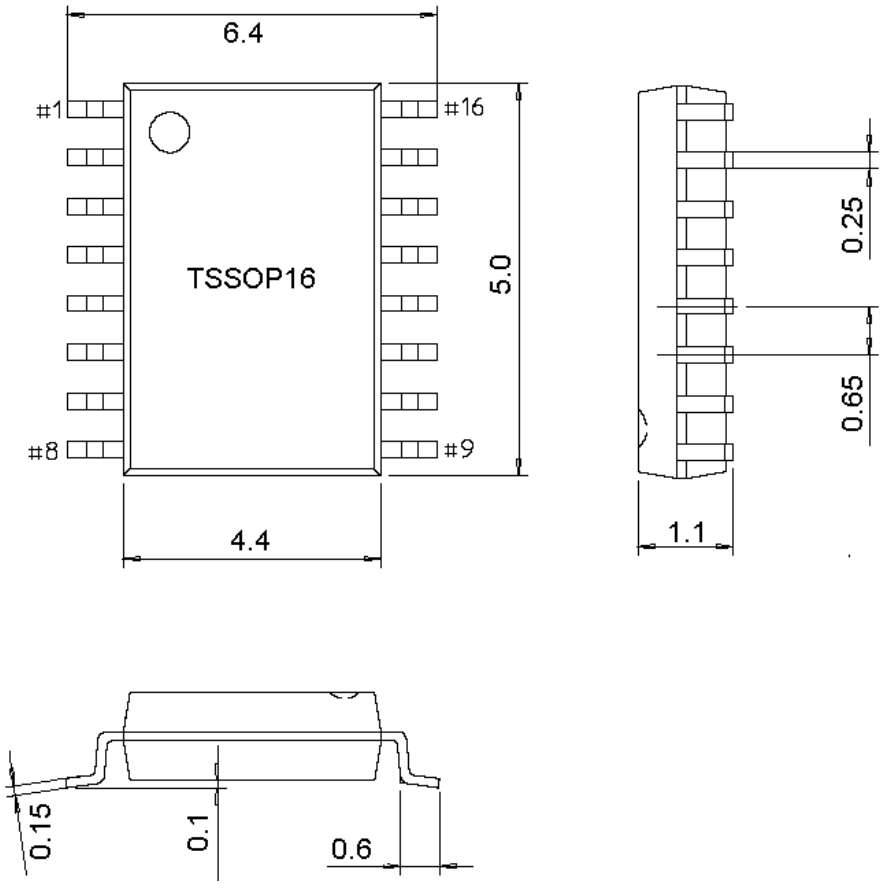
8. Package information

Note: All dimensions are in millimeters. The pin center spacing values are nominal values, and the error of other dimensions is not more than ±0.2mm.

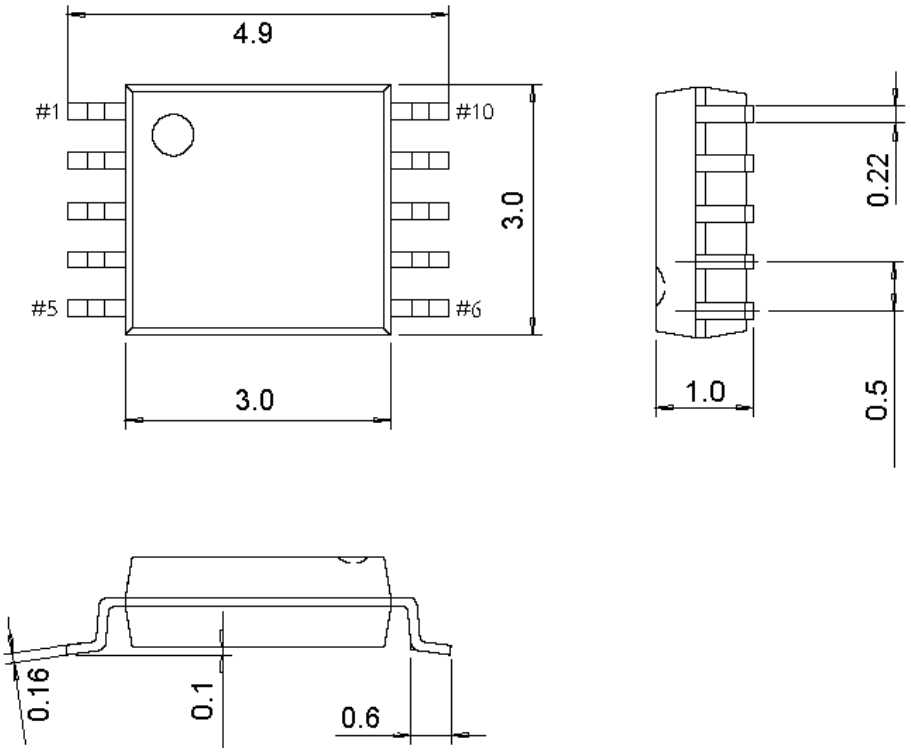
8.1. SOP16



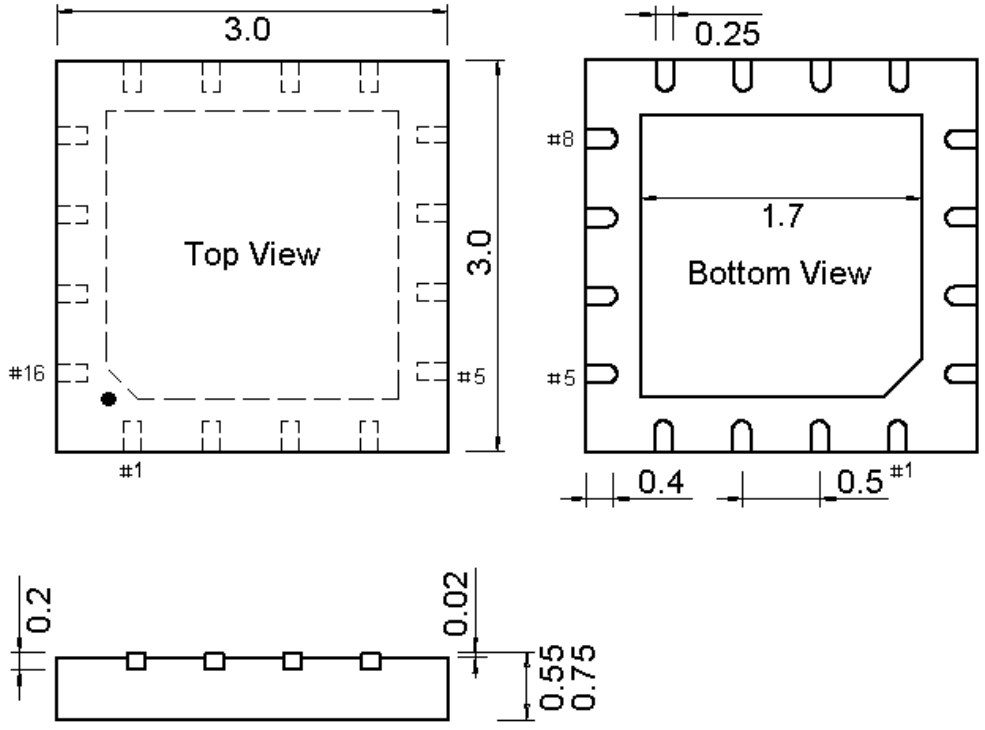
8.2. TSSOP16



8.3. MSOP10



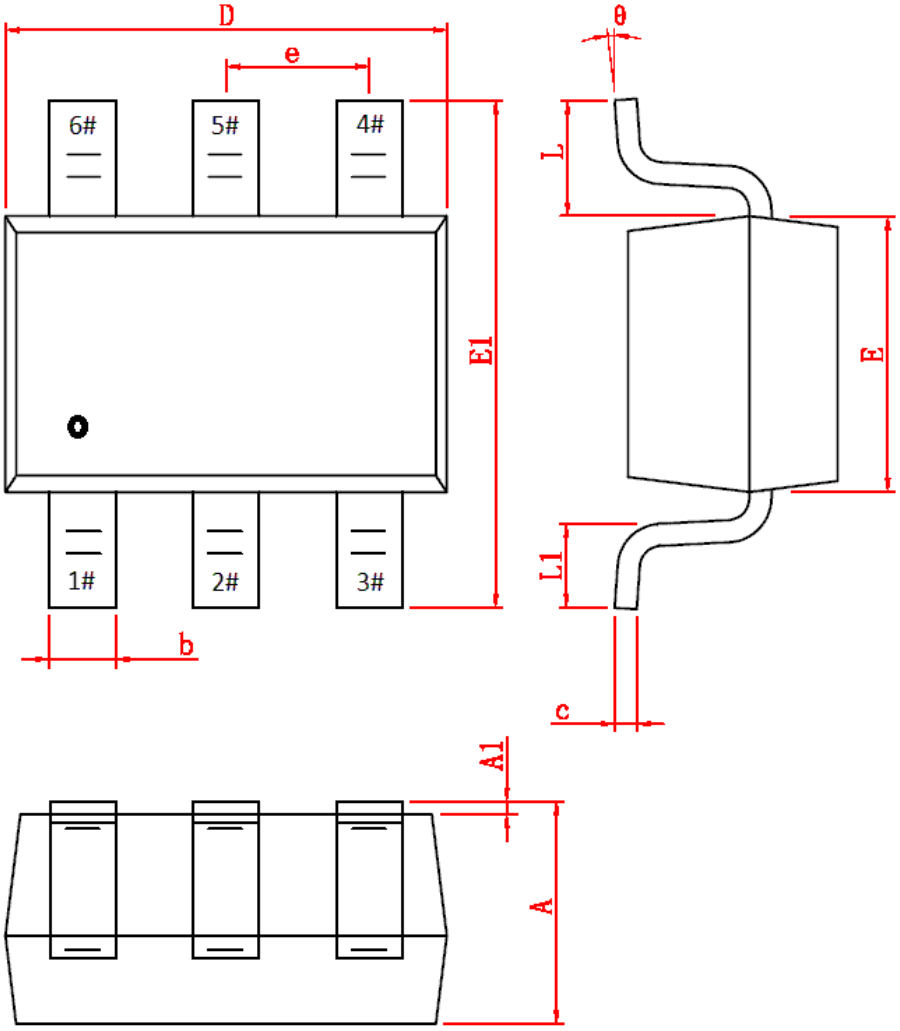
8.4. QFN16-3*3



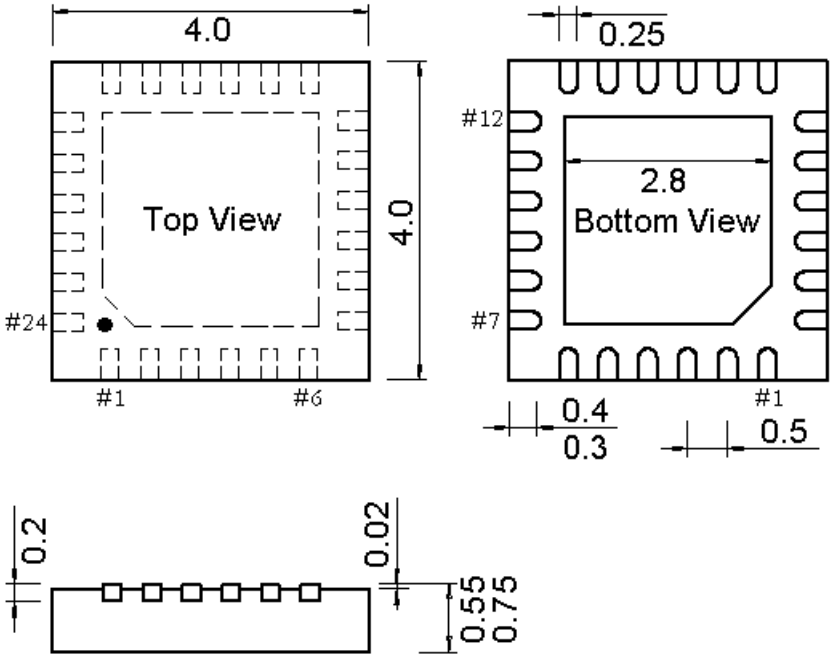
8.5. SOT363

SOT363 (SC70-6L) package dimensions.

Symbol	Metric, mm			Inch, mil		
	Min.	Type	Max.	Min.	Type	Max.
A	0.9	1.0	1.1	35	39	43
A1	0.0	0.05	0.1	0	2	4
b	0.15	0.25	0.35	6	10	14
c	0.08	0.12	0.15	3	5	6
D	2.0	2.1	2.2	79	83	87
E	1.15	1.25	1.35	45	49	53
E1	2.15	2.3	2.45	85	91	96
e		0.65			26	
L		0.53			21	
L1	0.25	0.35	0.45	10	14	18
θ	0°		8°	0°		8°



8.6. QFN24-4*4


4.0
Top View
4.0
#24
#1
#6
0.25
#12
2.8
Bottom View
#7
#1
0.4
0.3
0.5
0.2
0.02
0.55
0.75