8-bit Enhanced USB MCU CH559

Datasheet

Version: 1.6

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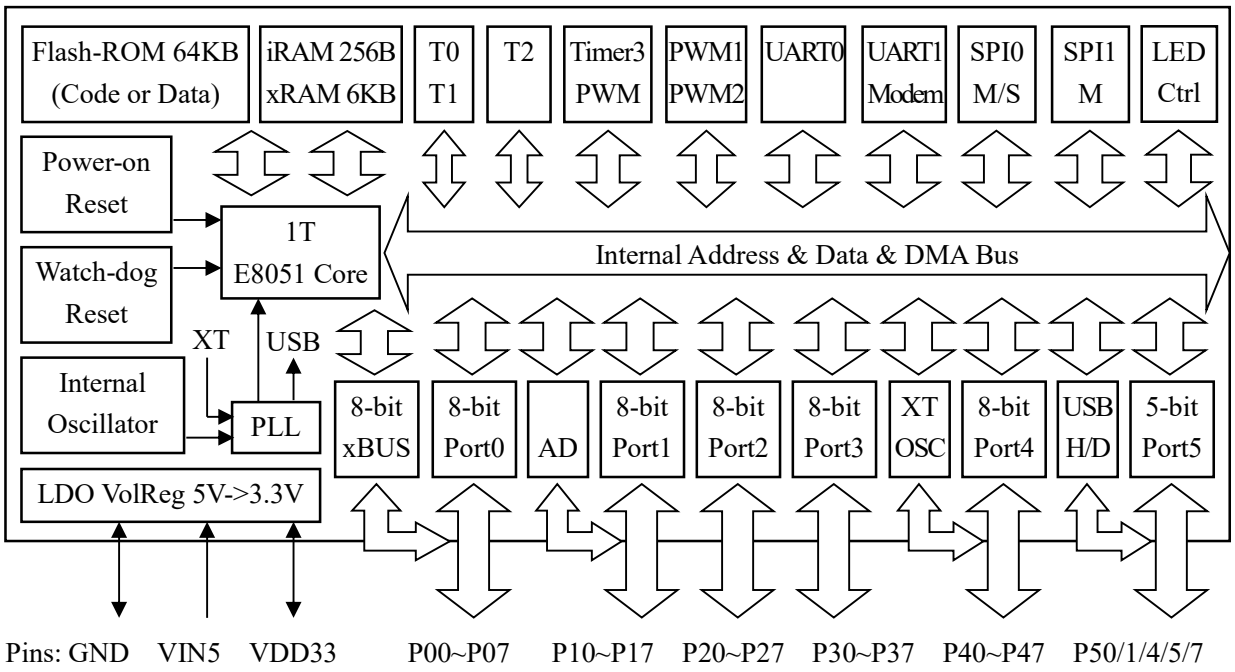
1. Overview

The CH559 is an enhanced E8051 MCU compatible with MCS51 instruction set. 79% of its instructions are single-byte single-cycle instructions, and the average instruction speed is 8 to 15 times faster than that of the standard MCS51.

CH559 supports up to 56MHz system clock, built-in 64KB Flash-ROM, 256B on-chip iRAM, 6KB on-chip xRAM, and some of xRAM support DMA mode.

CH559 has a built-in ADC converter, 4 timers/PWM, 2 UARTs, 2SPIs, and dual port Root-HUB, which support USB-Host and USB-Device modes.

Here is CH559 internal block diagram, for reference only.



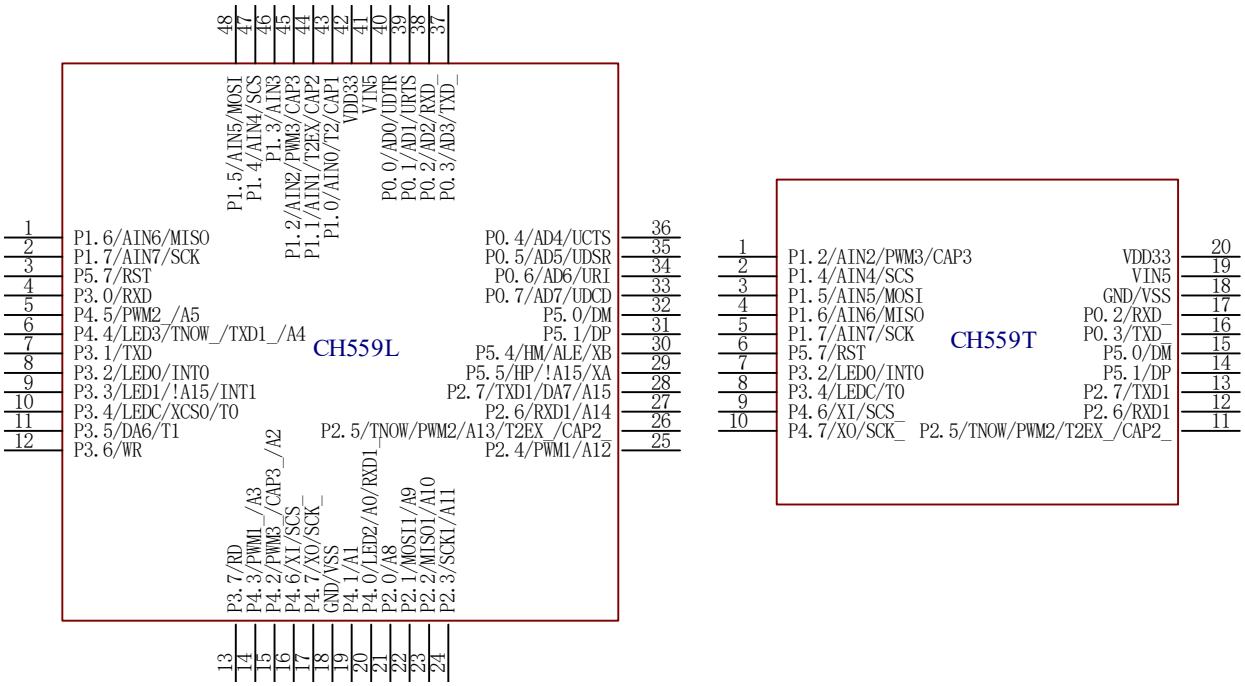
2. Features

- Core: Enhanced E8051 core, compatible with MCS51 instruction set, 79% of its instructions are single-byte single-cycle instructions, and the average instruction speed is 8 to 15 times faster than that of the standard MCS51, with special XRAM data fast copy instruction, and dual DPTR pointer.
- ROM: Non-volatile 64KB Flash-ROM, which supports 100K writing cycles, it can be all used for program memory. Or it can be divided into three pieces, 60KB for program memory, 1KB for data-flash and 3KB for BootLoader or ISP code.
- RAM: 256-byte on-chip iRAM, for fast data cache or stack pointer; 6KB on-chip xRAM, for mass data or DMA operation; support off-chip SRAM extending up to 32KB.
- USB: Built-in USB controller and dual USB transceiver, supports USB-Host and USB-Device modes, supports USB 2.0 full speed (12Mbps) and low speed (1.5Mbps). In USB-Host mode, CH559 may

manage 2 USB devices at the same time. Maximum support 64-byte packet, built-in FIFO and support DMA mode.

- Timer: 4 timers. T0, T1 and T2 are standard MCS51 timers, T2 is extended to support 2 captures. TMR3 is built in 8-level FIFO, support DMA and signal capturing and 16-bit PWM output.
- PWM: 3 PWM outputs. PWM1 and PWM2 are 2 8-bit PWM outputs, TMR3 supports 16-bit PWM output.
- UART: 2 UARTs. UART0 is a standard MCS51 UART. UART1 is compatible with 16C550, built-in 8-level FIFO, supports Modem signals, supports RS485 half-duplex mode, and supports local address presetting for auto-matching or multi-device communication.
- SPI: 2 SPIs, high speed rate up to Fsys/2, support simplex multiplexing of serial data input and output. SPI0 has built-in FIFO, supports Master/Slave mode. SPI1 only supports Master mode.
- ADC: 8-channel 10-bit or 11-bit A/D converter, built-in 2-level FIFO, supports DMA, sampling rate up to 1Mbps, and support 2 channels auto-switching detection.
- LED-CTRL: LED control card interface, built-in 4-level FIFO, supports DMA mode, and 1/2/4-channel data interface, high speed rate up to Fsys/2.
- XBUS: 8-bit parallel external bus, compatible with standard MCS51 bus, used to connect off-chip SRAM memory or other peripherals, supports direct 15-bit address or ALE multiplexed low 8-bit address, and supports 4 bus speeds.
- GPIO: Supports up to 45 GPIO pins (including XI/XO, RST and USB signal pins), 3.3V voltage output, and all support 5V-tolerant input except P1.0-P1.7, XI, XO or RST.
- Interrupt: Supports 14 interrupt sources, including 6 interrupts compatible with the standard MCS51 (INT0, T0, INT1, T1, UART0, T2), and 8 extended interrupts (SPI0, TMR3, USB, ADC, UART1, PWM1, GPIO, WDOG). GPIO interrupt can be selected from 7 pins.
- Watch-Dog: 8-bit configure presetting watchdog timer WDOG, support timer interrupt.
- Reset: Supports 4 reset sources, built-in power on reset, supports software reset and watchdog overflow reset, configurable external input reset.
- Clock: Built-in 12MHz clock, support external crystal oscillator through alternate GPIO pins, built-in PLL for USB clock and Fsys.
- Power: Built-in 5V to 3.3V LDO, 3.3V working voltage internal, support 3.3V and 5V voltage input. Support low power sleep mode, support USB, UART0, UART1, SPI0 and some GPIOs wake-up.
- Unique ID for identification.

3. Package



Package	Body size		Lead pitch		Description	Part No.
LQFP-48	7*7mm		0.5mm	19.7mil	Standard LQFP 48-pin patch	CH559L
SSOP-20	5.30mm	209mil	0.65mm	25mil	Shrink small outline package 20-pin patch	CH559T

4. Pin definitions

Pin No.		Pin	Alternate	Description
SSOP20	LQFP48	Name	(Left preferential)	
19	41	VIN5	V5	5V external power input of internal 5V->3.3V LDO, requires an external 0.1uF decoupling capacitor.
20	42	VDD33	VDD/VCC	Internal voltage regulator output and internal 3.3V working power input, When supply voltage is less than 3.6V, connect VIN5 to input the external power supply. When supply voltage is greater than 3.6V, an external 3.3uF decoupling capacitor is required.
18	18	GND	VSS	Ground.
-	40	P0.0	AD0/UDTR	P0 port: 8-bit open-drain bidirectional port by default, can be configured to quasi-bidirectional port by configuring the P0_PU register to enable the internal pull-up resistor. P0 will automatically switch to push-pull output modes temporarily when accessing xbus, as bidirectional data buses AD0-AD7; or output the lower 8 bits of address as needed when accessing xbus in address multiplexing mode.
-	39	P0.1	AD1/URTS	
17	38	P0.2	AD2/RXD_	
16	37	P0.3	AD3/TXD_	
-	36	P0.4	AD4/UCTS	
-	35	P0.5	AD5/UDSR	
-	34	P0.6	AD6/URI	
-	33	P0.7	AD7/UDCD	

				UDTR, URTS: UART1 modem signal outputs. UCTS, UDSR, URI, UDCD: UART1 modem signal inputs. RXD_, TXD_: RXD, TXD pin mapping.
-	43	P1.0	AIN0/T2/CAP1	AIN0 ~ AIN7: 8-channel ADC analog signal input. T2: Timer/counter2 external count input/clock output. T2EX: Timer/counter2 reload/capture input. CAP1, CAP2: Timer/counter2 capture input 1, 2. CAP3/PWM3: Timer/counter3 capture input/PWM output. SCS, MOSI, MISO, SCK: SPI0 interfaces. SCS is chip select input. MOSI is master output/slave input. MISO is master input/slave output. SCK is serial clock.
-	44	P1.1	AIN1/T2EX/CAP2	
1	45	P1.2	AIN2/PWM3/CAP3	
-	46	P1.3	AIN3	
2	47	P1.4	AIN4/SCS	
3	48	P1.5	AIN5/MOSI	
4	1	P1.6	AIN6/MISO	
5	2	P1.7	AIN7/SCK	
-	21	P2.0	A8	P2 will automatically switch to push-pull output modes temporarily when accessing xbus, and output the higher 8 bits A8-A15 of address as needed. MOSI1, MISO1, SCK1: SPI1 interfaces. MOSI1 is master output. MISO1 is master input. SCK1 is serial clock output. PWM1, PWM2: PWM1 output. PWM2 output. TNOW: UART1 transmitting indicating. T2EX_/CAP2_: T2EX/CAP2 pin mapping. RXD1, TXD1: UART1 serial data input, serial data output. DA7: Address A7 output when accessing xbus in direct-address mode.
-	22	P2.1	MOSI1/A9	
-	23	P2.2	MISO1/A10	
-	24	P2.3	SCK1/A11	
-	25	P2.4	PWM1/A12	
11	26	P2.5	TNOW/PWM2/A13 /T2EX_/CAP2_	
12	27	P2.6	RXD1/A14	
13	28	P2.7	TXD1/DA7/A15	
-	4	P3.0	RXD	RXD, TXD: UART0 serial data input, serial data output. INT0, INT1: External interrupt 0, external interrupt 1 input. LED0, LED1, LEDC: LED data0, data1, clock output. !A15: External parallel bus address A15 inverted output, for chip selection. T0, T1: Timer0, timer1 external input. XCS0: Chip selection output of external bus address from 4000h to 7FFFh. DA6: Address A6 output when accessing xbus in direct-address mode. WR, RD: External bus write signal, read signal.
-	7	P3.1	TXD	
7	8	P3.2	LED0/INT0	
-	9	P3.3	LED1/!A15/INT1	
8	10	P3.4	LEDC/XCS0/T0	
-	11	P3.5	DA6/T1	
-	12	P3.6	WR	
-	13	P3.7	RD	
-	20	P4.0	LED2/A0/RXD1_	A0～A5: Low 6-bit address output when accessing xbus in direct-address mode. LED2, LED3: LED data2, data3 output. RXD1_, TNOW_/TXD1_: RXD1, TNOW/TXD1 pin mapping. PWM3_/CAP3_: PWM3/CAP3 pin mapping.
-	19	P4.1	A1	
-	15	P4.2	PWM3_/CAP3_/A2	
-	14	P4.3	PWM1_/A3	
-	6	P4.4	LED3/TNOW_/TXD1_/ A4	

-	5	P4.5	PWM2_/A5	PWM1_, PWM2_:PWM1, PWM2 pin mapping. XI, XO: External crystal oscillator input, inverted output. SCS_, SCK_: SPI0 SCS, SCK pin mapping.
9	16	P4.6	XI/SCS_	
10	17	P4.7	X0/SCK_	
15	32	P5.0	DM	DM, DP: USB host HUB0 or USB device D-, D+ signals.
14	31	P5.1	DP	
-	30	P5.4	HM /ALE/XB	XB, XA: iRS485 B/inverted and A/in-phase signals. ALE: Address latch signal output in address multiplexing mode.
-	29	P5.5	HP /!A15/XA	!A15: External bus address A15 inverted output, for chip selection. HM, HP: USB host expanded HUB1 D-, D+ signals
6	3	P5.7	RST	External reset input, built-in pull-down resistor.

Note: The USB transceiver is designed built-in based on USB2.0. The P5.0/P5.1/P5.4/P5.5 cannot be connected to resistors in series when they are used for USB.

5. Special function register (SFR)

Abbreviations and descriptions in this datasheet.

Abbreviation	Description
RO	Software can only read these bits.
WO	Software can only write to this bit. The read value is invalid.
RW	Software can read and write to these bits.
h	End with it to indicate a hexadecimal number
b	End with it to indicate a binary number

5.1 SFR introduction and address distribution

CH559 controls, manages the device, and sets the working mode with special function registers (SFR and xSFR).

SFRs use address from 80h to FFh of internal data memory, and can only be accessed by direct-address instructions. Some addresses support bit addressing such as x0h and x8h, to avoid modifying the values of other bits when accessing a specific bit. Other registers with the addresses that are not the multiple of 8 can only be accessed by bytes.

Some SFRs can be written only in safe mode, and are read-only in unsafe mode, such as: GLOBAL_CFG, PLL_CFG, CLOCK_CFG, SLEEP_CTRL, WAKE_CTRL.

Some SFRs have one or more names, such as: SPI0_CK_SE/SPI0_S_PRE, UDEV_CTRL/UHUB0_CTRL, UEP1_CTRL/UH_SETUP, UEP2_CTRL/UH_RX_CTRL, UEP2_T_LEN/UH_EP_PID, UEP3_CTRL/UH_TX_CTRL, UEP3_T_LEN/UH_TX_LEN, P5_PIN/P4_CFG.

Some addresses may correspond to multiple seperate SFRs, such as: TL2/T2CAP1L, TH2/T2CAP1H, SAFE_MOD/CHIP_ID, T3_COUNT_L/T3_CK_SE_L, T3_COUNT_H/T3_CK_SE_H, SER1_FIFO/SER1_RBR/SER1_THR/SER1_DLL, SER1_IER/SER1_DLM, SER1_IIR/SER1_FCR, SER1_ADDR/SER1_DIV, ROM_CTRL/ROM_STATUS.

xSFRs occupy address from 2440h to 298Fh of the external data memory xdata, or 40H-8Fh of pdata. xSFRs can only be accessed by bytes by indirect addressing through the MOVX instruction, it is based on the DPTR pointer by default, but you can also use faster R0 or R1 as the pdata type pointer to access xSFR named pU* and pLED_* after bXIR_XSFR is set to 1.

Some xSFRs may have one or more names, such as: UEP2_3_MOD/UH_EP_MOD, UEP2_DMA_H/UH_RX_DMA_H, UEP2_DMA_L/UH_RX_DMA_L, UEP2_DMA/UH_RX_DMA, UEP3_DMA_H/UH_TX_DMA_H, UEP3_DMA_L/UH_TX_DMA_L, UEP3_DMA/UH_TX_DMA.

Some addresses correspond to multiple seperate xSFRs, such as: LED_DATA/LED_FIFO_CN.

CH559 contains all the standard registers of 8051, and adds some other device control registers. See the table below for the specific SFRs.

Table 5.1 Table of special function registers

SFR	0, 8	1, 9	2, A	3, B	4, C	5, D	6, E	7, F
0xF8	SPI0_STAT	SPI0_DATA	SPI0_CTRL	SPI0_CK_SE SPI0_S_PRE	SPI0_SETUP	XBUS_SPEED	RESET_KEEP	WDOG_COUNT
0xF0	B	ADC_STAT	ADC_CTRL	ADC_CHANN	ADC_FIFO_L	ADC_FIFO_H	ADC_SETUP	ADC_EX_SW
0xE8	IE_EX	IP_EX	SLEEP_CTRL	WAKE_CTRL	ADC_DMA_AL	ADC_DMA_AH	ADC_DMA_CN	ADC_CK_SE
0xE0	ACC	USB_INT_EN	USB_CTRL	USB_DEV_AD	UDEV_CTRL UHUB0_CTRL	UHUB1_CTRL	USB_DMA_AL	USB_DMA_AH
0xD8	USB_INT_FG	USB_INT_ST	USB_MIS_ST	USB_HUB_ST	UEP0_CTRL	UEP0_T_LEN	UEP4_CTRL	UEP4_T_LEN
0xD0	PSW	USB_RX_LEN	UEP1_CTRL UH-SETUP	UEP1_T_LEN	UEP2_CTRL UH_RX_CTRL	UEP2_T_LEN UH_EP_PID	UEP3_CTRL UH_TX_CTRL	UEP3_T_LEN UH_TX_LEN
0xC8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2 T2CAP1L	TH2 T2CAP1H	PIN_FUNC	GPIO_IE
0xC0	P4_OUT	P4_IN	P4_DIR	P4_PU	P0_DIR	P0_PU	PORT_CFG	P5_PIN P4_CFG
0xB8	IP	P1_IE	P1_DIR	P1_PU	P2_DIR	P2_PU	P3_DIR	P3_PU
0xB0	P3	GLOBAL_CFG	PLL_CFG	CLOCK_CFG	SPI1_STAT	SPI1_DATA	SPI1_CTRL	SPI1_CK_SE
0xA8	IE	T3_STAT	T3_CTRL	T3_DMA_CN	T3_DMA_AL	T3_DMA_AH	T3_FIFO_L	T3_FIFO_H
0xA0	P2	SAFE_MOD CHIP_ID	XBUS_AUX	T3_SETUP	T3_COUNT_L T3_CK_SE_L	T3_COUNT_H T3_CK_SE_H	T3_END_L	T3_END_H
0x98	SCON	SBUF	SER1_FIFO SER1_DLL	PWM_DATA2	PWM_DATA	PWM_CTRL	PWM_CK_SE	PWM_CYCLE
0x90	P1	SER1_IER SER1_DLM	SER1_IIR SER1_FCR	SER1_LCR	SER1_MCR	SER1_LSR	SER1_MSR	SER1_ADDR SER1_DIV
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	ROM_DATA_L	ROM_DATA_H
0x80	P0	SP	DPL	DPH	ROM_ADDR_L	ROM_ADDR_H	ROM_CTRL ROM_STATUS	PCON

Notes: (1) Those in red text can be accessed by bits;

(2) The following table shows the corresponding description of different color boxes.

	Register address
	SPI0 register
	ADC register
	USB register

	Timer/counter2 register
	Port setting register
	SPI1 register
	PWM1 and PWM2 register
	UART1 register
	Timer/counter 0 and 1 register
	Flash-ROM register

5.2 SFR classification and reset value

Table 5.2 Description and reset value of SFR and xSFR

Function	Name	Address	Description	Reset value
System setting registers	B	F0h	General purpose register B	0000 0000b
	ACC	E0h	Accumulator	0000 0000b
	PSW	D0h	Program status register	0000 0000b
	GLOBAL_CFG	B1h	Global configuration register (Bootloader)	1110 0000b
			Global configuration register (application)	1100 0000b
	CHIP_ID	A1h	Chip ID (read-only)	0101 1001b
	SAFE_MOD	A1h	Safe mode control register (write only)	0000 0000b
	DPH	83h	Data pointer high	0000 0000b
	DPL	82h	Data pointer low	0000 0000b
	DPTR	82h	16-bit SFR consists of DPL and DPH	0000h
	SP	81h	Stack pointer	0000 0111b
Clock, sleep and power supply control registers	WDOG_COUNT	FFh	Watchdog count register	0000 0000b
	RESET_KEEP	FEh	Value keeper during reset (power on reset)	0000 0000b
	WAKE_CTRL	EBh	Wake-up control register	0000 0000b
	SLEEP_CTRL	EAh	Sleep control register	0000 0000b
	CLOCK_CFG	B3h	System clock configuration register	1001 1000b
	PLL_CFG	B2h	PLL clock configuration register	1101 1000b
	PCON	87h	Power control register (power on reset)	0001 0000b
Interrupt control registers	IP_EX	E9h	Extend interrupt priority register	0000 0000b
	IE_EX	E8h	Extend interrupt enable register	0000 0000b
	GPIO_IE	CFh	GPIO interrupt enable register	0000 0000b
	IP	B8h	Interrupt priority register	0000 0000b
	IE	A8h	Interrupt enable register	0000 0000b
Flash-ROM registers	ROM_DATA_H	8Fh	Flash-ROM data register high	xxxx xxxxb
	ROM_DATA_L	8Eh	Flash-ROM data register low	xxxx xxxxb
	ROM_DATA	8Eh	16-bit SFR consists of ROM_DATA_L and ROM_DATA_H	xxxxh
	ROM_STATUS	86h	Flash-ROM status register (read only)	1000 0000b
	ROM_CTRL	86h	Flash-ROM control register (write only)	0000 0000b
	ROM_ADDR_H	85h	Flash-ROM address register high	xxxx xxxxb
	ROM_ADDR_L	84h	Flash-ROM address register low	xxxx xxxxb
	ROM_ADDR	84h	16-bit SFR consists of ROM_ADDR_L and	xxxxh

			ROM_ADDR_H	
Port setting registers	XBUS_SPEED	FDh	XBUS speed configuration register	1111 1111b
	XBUS_AUX	A2h	XBUS auxiliary configuration register	0000 0000b
	PIN_FUNC	CEh	Pin function selection register	0000 0000b
	P4_CFG	C7h	Port4 configuration register	0000 0000b
	P5_IN	C7h	Port5 input register (read-only):	0000 0000b
	PORT_CFG	C6h	Port configuration register	0000 1111b
	P0_PU	C5h	Port0 pull-up enable register (En_P0_Pullup=0)	0000 0000b
			Port0 pull-up enable register (En_P0_Pullup=1)	1111 1111b
	P0_DIR	C4h	Port0 direction control register	0000 0000b
	P4_PU	C3h	Port4 pull-up enable register	1111 1111b
	P4_DIR	C2h	Port4 direction control register	0000 0000b
	P4_IN	C1h	Port4 input register (read-only):	1111 1111b
	P4_OUT	C0h	Port4 output register	0000 0000b
	P3_PU	BFh	Port3 pull-up enable register	1111 1111b
	P3_DIR	BEh	Port3 direction control register	0000 0000
	P2_PU	BDh	Port2 pull-up enable register	1111 1111b
	P2_DIR	BCh	Port2 direction control register	0000 0000b
	P1_PU	BBh	Port1 pull-up enable register	1111 1111b
	P1_DIR	BAh	Port1 direction control register	0000 0000b
	P1_IE	B9h	Port1 input enable register	1111 1111b
	P3	B0h	Port3 input & output register	1111 1111b
	P2	A0h	Port2 input & output register	1111 1111b
	P1	90h	Port1 input & output register	1111 1111b
	P0	80h	Port0 input & output register	1111 1111b
Timer/counter 0 and 1 registers	TH1	8Dh	Timer1 count register high	xxxx xxxxb
	TH0	8Ch	Timer0 count register high	xxxx xxxxb
	TL1	8Bh	Timer1 count register low	xxxx xxxxb
	TL0	8Ah	Timer0 count register low	xxxx xxxxb
	TMOD	89h	Timer0/1 mode register	0000 0000b
	TCON	88h	Timer0/1 control register	0000 0000b
UART0 registers	SBUF	99h	UART0 data register	xxxx xxxxb
	SCON	98h	UART0 control register	0000 0000b
Timer/counter 2 registers	TH2	CDh	Timer2 count register high	0000 0000b
	TL2	CCh	Timer2 count register low	0000 0000b
	T2COUNT	CCh	16-bit SFR consists of TL2 and TH2	0000h
	T2CAP1H	CDh	Timer2 capture 1 data high byte (read only)	xxxx xxxxb
	T2CAP1L	CCh	Timer2 capture 1 data low byte (read only)	xxxx xxxxb
	T2CAP1	CCh	16-bit SFR consists of T2CAP1L and T2CAP1H	xxxxh
	RCAP2H	CBh	Count reload/capature 2 data register high	0000 0000b

	RCAP2L	CAh	Count reload/capature 2 data register low	0000 0000b
	RCAP2	CAh	16-bit SFR consists of RCAP2L and RCAP2H	0000h
	T2MOD	C9h	Timer2 mode register	0000 0000b
	T2CON	C8h	Timer2 control register	0000 0000b
Timer/counter 3 register	T3_FIFO_H	AFh	Timer3 FIFO register high	xxxx xxxxb
	T3_FIFO_L	AEh	Timer3 FIFO register low	xxxx xxxxb
	T3_FIFO	AEh	16-bit SFR consists of T3_FIFO_L and T3_FIFO_H	xxxxh
	T3_DMA_AH	ADh	DMA address register high	0000 xxxxb
	T3_DMA_AL	ACh	DMA address register low	xxxx xxx0b
	T3_DMA	ACh	16-bit SFR consists of T3_DMA_AL and T3_DMA_AH	0xxxh
	T3_DMA_CN	ABh	DMA remainder word count register	0000 0000b
	T3_CTRL	AAh	Timer3 control register	0000 0010b
	T3_STAT	A9h	Timer3 status register	0000 0000b
	T3_END_H	A7h	Timer3 final count value high	xxxx xxxxb
	T3_END_L	A6h	Timer3 final count value low	xxxx xxxxb
	T3_END	A6h	16-bit SFR consists of T3_END_L and T3_END_H	xxxxh
	T3_COUNT_H	A5h	Timer3 current count high byte (read only)	0000 0000b
	T3_COUNT_L	A4h	Timer3 current count low byte (read only)	0000 0000b
	T3_COUNT	A4h	16-bit SFR consists of T3_COUNT_L and T3_COUNT_H	0000h
	T3_CK_SE_H	A5h	Timer3 clock divisor setting high byte	0000 0000b
	T3_CK_SE_L	A4h	Timer3 clock divisor setting low byte	0010 0000b
	T3_CK_SE	A4h	16-bit SFR consists of T3_CK_SE_L and T3_CK_SE_H	0020h
	T3_SETUP	A3h	Timer3 setup register	0000 0100b
PWM1 and PWM2 registers	PWM_CYCLE	9Fh	PWM cycle period register	xxxx xxxxb
	PWM_CK_SE	9Eh	PWM clock divisor setting register	0000 0000b
	PWM_CTRL	9Dh	PWM control register	0000 0010b
	PWM_DATA	9Ch	PWM1 data register	xxxx xxxxb
	PWM_DATA2	9Bh	PWM2 data register	xxxx xxxxb
SPI0 registers	SPI0_SETUP	FCh	SPI0 setup register	0000 0000b
	SPI0_S_PRE	FBh	SPI0 slave preset value register	0010 0000b
	SPI0_CK_SE	FBh	SPI0 clock divisor setting register	0010 0000b
	SPI0_CTRL	FAh	SPI0 control register	0000 0010b
	SPI0_DATA	F9h	SPI0 data register	xxxx xxxxb
	SPI0_STAT	F8h	SPI0 status register	0000 1000b
SPI1 registers	SPI1_CK_SE	B7h	SPI1 clock divisor setting register	0010 0000b
	SPI1_CTRL	B6h	SPI1 control register	0000 0010b
	SPI1_DATA	B5h	SPI1 data register	xxxx xxxxb
	SPI1_STAT	B4h	SPI1 status register	0000 1000b

UART1 registers	SER1_DLL	9Ah	UART1 baud rate divisor latch LSB	xxxx xxxxb
	SER1_FIFO	9Ah	UART1 FIFO data register	xxxx xxxxb
	SER1_DIV	97h	UART1 predivisor latch register	0xxx xxxxb
	SER1_ADDR	97h	UART1 bus address preset register	1111 1111b
	SER1_MSR	96h	UART1 MODEM status register (read-only)	1111 0000b
	SER1_LSR	95h	UART1 line status register (read-only)	0110 0000b
	SER1_MCR	94h	UART1 MODEM control register	0000 0000b
	SER1_LCR	93h	UART1 line control register	0000 0000b
	SER1_IIR	92h	UART1 interrupt identification register (read-only)	0000 0001b
	SER1_FCR	92h	FIFO control register (write-only)	0000 0000b
	SER1_DLM	91h	UART1 baud rate divisor latch MSB	1000 0000b
	SER1_IER	91h	UART1 interrupt enable register	0000 0000b
ADC registers	ADC_EX_SW	F7h	ADC extend switch control register	0000 0000b
	ADC_SETUP	F6h	ADC setup register	0000 1000b
	ADC_FIFO_H	F5h	ADC FIFO high byte (read-only)	0000 0xxxb
	ADC_FIFO_L	F4h	ADC FIFO low byte (read-only)	xxxx xxxxb
	ADC_FIFO	F4h	16-bit SFR consists of ADC_FIFO_L and ADC_FIFO_H	0xxxh
	ADC_CHANN	F3h	ADC channel selection register	0000 0000b
	ADC_CTRL	F2h	ADC control register	0000 0000b
	ADC_STAT	F1h	ADC status register	0000 0100b
	ADC_CK_SE	EFh	ADC clock divisor setting register	0001 0000b
	ADC_DMA_CN	EEh	DMA remainder word count register	0000 0000b
	ADC_DMA_AH	EDh	DMA address high byte	0000 xxxxb
	ADC_DMA_AL	ECh	DMA address low byte	xxxx xxx0b
	ADC_DMA	ECh	16-bit SFR consists of ADC_DMA_AL and ADC_DMA_AH	0xxxh
USB registers	USB_DMA_AH	E7h	Current DMA address high byte (read-only)	000x xxxxb
	USB_DMA_AL	E6h	Current DMA address low byte (read-only)	xxxx xxx0b
	USB_DMA	E6h	16-bit SFR consists of USB_DMA_AL and USB_DMA_AH	xxxxh
	UHUB1_CTRL	E5h	USB HUB1 control register	1100 x000b
	UHUB0_CTRL	E4h	USB HUB0 control register	0100 x000b
	UDEV_CTRL	E4h	USB device port control register	0100 x000b
	USB_DEV_AD	E3h	USB device address register	0000 0000b
	USB_CTRL	E2h	USB control register	0000 0110b
	USB_INT_EN	E1h	USB interrupt enable register	0000 0000b
	UEP4_T_LEN	DFh	Endpoint4 transmittal length register	0xxx xxxxb
	UEP4_CTRL	DEh	Endpoint4 control register	0000 0000b
	UEP0_T_LEN	DDh	Endpoint0 transmittal length register	0xxx xxxxb
	UEP0_CTRL	DCh	Endpoint0 control register	0000 0000b
	USB_HUB_ST	DBh	USB host HUB port status register (read only)	0000 0000b

	USB_MIS_ST	DAh	USB miscellaneous status register (read only)	xx10 1000b
	USB_INT_ST	D9h	USB interrupt status register (read only)	00xx xxxxb
	USB_INT_FG	D8h	USB interrupt flag register	0010 0000b
	UEP3_T_LEN	D7h	Endpoint3 transmittal length register	0xxx xxxxb
	UH_TX_LEN	D7h	USB host transmittal length register	0xxx xxxxb
	UEP3_CTRL	D6h	Endpoint3 control register	0000 0000b
	UH_TX_CTRL	D6h	USB host transmittal endpoint control register	0000 0000b
	UEP2_T_LEN	D5h	Endpoint2 transmittal length register	0000 0000b
	UH_EP_PID	D5h	USB host endpoint and token PID register	0000 0000b
	UEP2_CTRL	D4h	Endpoint2 control register	0000 0000b
	UH_RX_CTRL	D4h	USB host receiver endpoint control register	0000 0000b
	UEP1_T_LEN	D3h	Endpoint1 transmittal length register	0xxx xxxxb
	UEP1_CTRL	D2h	Endpoint1 control register	0000 0000b
	UH_SETUP	D2h	USB host auxiliary setup register	0000 0000b
	USB_RX_LEN	D1h	USB receiving length register (read only)	0xxx xxxxb
USB registers on xSFR	UEP4_1_MOD	2446h	Endpoint1&4 mode control register	0000 0000b
	UEP2_3_MOD	2447h	Endpoint2&3 mode control register	0000 0000b
	UH_EP_MOD	2447h	USB host endpoint mode control register	0000 0000b
	UEP0_DMA_H	2448h	Endpoint0&4 buffer start address high byte	000x xxxxb
	UEP0_DMA_L	2449h	Endpoint0&4 buffer start address low byte	xxxx xxx0b
	UEP0_DMA	2448h	16-bit SFR consists of UEP0_DMA_L and UEP0_DMA_H	xxxxh
	UEP1_DMA_H	244Ah	Endpoint1 buffer start address high byte	000x xxxxb
	UEP1_DMA_L	244Bh	Endpoint1 buffer start address low byte	xxxx xxx0b
	UEP1_DMA	244Ah	16-bit SFR consists of UEP1_DMA_L and UEP1_DMA_H	xxxxh
	UEP2_DMA_H	244Ch	Endpoint 2 buffer start address high byte	000x xxxxb
	UEP2_DMA_L	244Dh	Endpoint 2 buffer start address low byte	xxxx xxx0b
	UEP2_DMA	244Ch	16-bit SFR consists of UEP2_DMA_L and UEP2_DMA_H	xxxxh
	UH_RX_DMA_H	244Ch	USB host rx endpoint buffer start address high byte	000x xxxxb
	UH_RX_DMA_L	244Dh	USB host rx endpoint buffer start address low byte	xxxx xxx0b
	UH_RX_DMA	244Ch	16-bit SFR consists of UH_RX_DMA_L and UH_RX_DMA_H	xxxxh
	UEP3_DMA_H	244Eh	Endpoint3 buffer start address high byte	000x xxxxb
	UEP3_DMA_L	244Fh	Endpoint3 buffer start address low byte	xxxx xxx0b
	UEP3_DMA	244Eh	16-bit SFR consists of UEP3_DMA_L and UEP3_DMA_H	xxxxh
	UH_TX_DMA_H	244Eh	USB host tx endpoint buffer start address high byte	000x xxxxb
	UH_TX_DMA_L	244Fh	USB host tx endpoint buffer start address low byte	xxxx xxx0b

	UH_TX_DMA	244Eh	16-bit SFR consists of UH_TX_DMA_L and UH_TX_DMA_H	xxxxh
	pU*	254*h	pdata type above while bXIR_XSFR is set to 1, which is faster than xdata type	
LED control card registers on xSFR	LED_STAT	2880h	LED status register	010x 0000b
	LED_CTRL	2881h	LED control register	0000 0010b
	LED_FIFO_CN	2882h	FIFO counter status register (read-only)	0000 0000b
	LED_DATA	2882h	LED data register (write-only)	xxxx xxxxb
	LED_CK_SE	2883h	LED clock divisor setting register	0001 0000b
	LED_DMA_AH	2884h	DMA address high byte	000x xxxxb
	LED_DMA_AL	2885h	DMA address low byte	xxxx xxx0b
	LED_DMA	2884h	16-bit SFR consists of LED_DMA_AL and LED_DMA_AH	xxxxh
	LED_DMA_CN	2886h	LED DMA remainder word count register	xxxx xxxxb
	LED_DMA_XH	2888h	Auxiliary DMA buffer address high byte	000x xxxxb
	LED_DMA_XL	2889h	Auxiliary DMA buffer address low byte	xxxx xxx0b
	LED_DMA_X	2888h	16-bit SFR consists of LED_DMA_XL and LED_DMA_XH	xxxxh
	pLED_*	298*h	Used to address xSFR above in pdata type while bXIR_XSFR is set to 1, which is faster than xdata type	

5.3 General 8051 register

Table 5.3.1 List of general 8051 registers

Name	Address	Description	Reset value
B	F0h	B register	00h
A, ACC	E0h	Accumulator	00h
PSW	D0h	Program status register	00h
GLOBAL_CFG	B1h	Global configuration register (Bootloader)	E0h
		Global configuration register (application)	C0h
CHIP_ID	A1h	Chip ID (read-only)	59h
SAFE_MOD	A1h	Safe mode control register (write only)	00h
PCON	87h	Power control register (power on reset)	10h
DPH	83h	Data pointer high	00h
DPL	82h	Data pointer low	00h
DPTR	82h	16-bit SFR consists of DPL and DPH	0000h
SP	81h	Stack pointer	07h

B register (B):

Bit	Name	Access	Description	Reset value
[7:0]	B	RW	Arithmetic register, mainly used for multiplication and division operations; it supports bit addressing	00h

A accumulator (A, ACC):

Bit	Name	Access	Description	Reset value
[7:0]	A/ACC	RW	Arithmetic accumulator, supports bit addressing	00h

Program status register (PSW):

Bit	Name	Access	Description	Reset value
7	CY	RW	Carry flag: used to record the carry or borrow of the highest bit. This bit is set when the last arithmetic operation resulted in a carry (addition) or a borrow (subtraction). It is cleared to 0 by all other arithmetic operations.	0
6	AC	RW	Auxiliary carry flag. This bit is set to 1 when the last arithmetic operation resulted in a carry into(addition) or a borrow from(subtraction)the high order nibble. It is cleared to 0 by all other arithmetic operations	0
5	F0	RW	Flag0: It supports bit addressing. User-defined. Can be reset or set by software.	0
4	RS1	RW	Register bank select control bit 1	0
3	RS0	RW	Register bank select control bit 0	0
2	OV	RW	Overflow flag: This bit is set to 1 when the operation result exceeds 8-bit binary number in addition/subtraction operations, and the flag will overflow. Otherwise it will be aleared to 0.	0
1	F1	RW	Flag1: It supports bit addressing. User-defined. Can be reset or set by software.	0
0	P	RO	Parity flag: It records the parity of “1” in accumulator A after the instruction is executed. This bit is set to 1 if the number of “1” is odd. It is cleared if the number of “1” is even.	0

The program status word (PSW) contains status that reflects the current state of the CPU and it supports bit addressing. It contains the carry bit, the auxiliary carry (for BCD operation), parity bit, overflow bit and the 2 register bank select bits RS0 and RS1. The space of register bank may be accessed by direct or indirect way.

Table 5.3.2 List of register bank RS1 and RS0

RS1	RS0	Register bank
0	0	Bank0 (00h-07h)
0	1	Bank1 (08h-0Fh)
1	0	Bank2 (10h-17h)
1	1	Bank3 (18h-1Fh)

Table 5.3.3 Operations affecting flag bits (X means that flag bit is related to the operation result)

Operation	CY	OV	AC	Operation	CY	OV	AC
ADD	X	X	X	SETB C	1		
ADDC	X	X	X	CLR C	0		
SUBB	X	X	X	CPL C	X		

MUL	0	X		MOV C, bit	X		
DIV	0	X		ANL C, bit	X		
DA A	X			ANL C,/bit	X		
RRC A	X			ORL C, bit	X		
RLC A	X			ORL C,/bit	X		
CJNE	X						

Data pointer register (DPTR):

Bit	Name	Access	Description	Reset value
[7:0]	DPL	RW	Data pointer low byte	00h
[7:0]	DPH	RW	Data pointer high byte	00h

The16-bit data pointer (DPTR) consists of DPL and DPH, which is used to access xSFR, xBUS, xRAM data memory and program memory. Actually, DPTR has 2 physical 16-bit data pointers DPTR0 and DPTR1, which are dynamically switched by DPS in XBUS_AUX.

Stack pointer (SP):

Bit	Name	Access	Description	Reset value
[7:0]	SP	RW	Stack pointer, mainly used for program and interrupt call, also for data push and pull.	07h

Specific function of stack: protect breakpoint and protect site, and carry out management on the first-in last-out principle. During instack, SP pointer automatically adds 1, saving the data and breakpoint information. During outstack, SP pointer points to the data unit and automatically substracts 1. The initial value of SP is 07h after reset, and the corresponding default stack storage starts from 08h.

5.4 Unique register

Global configuration register (ACC), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
[7:6]	Reserved	RO	Always 11	11b
5	bBOOT_LOAD	RO	Boot loader status bit, for discriminating Bootloader or Application. Set to 1 by power on reset. Cleared to 0 by software reset. For all chips with ISP boot loader: 1 = it has never been reset by software, usually in ISP boot loader state. 0 = it has been reset by software, usually in application state.	1
4	bSW_RESET	RW	Software reset. If it is set to 1, software reset occurs. Automatically reset by hardware.	0
3	bCODE_WE	RW	Flash-ROM write enable: 0 = Write protection. 1 = Flash-ROM can be written and erased.	0
2	bDATA_WE	RW	Flash-ROM DataFlash write enable:	0

			0 = Write protection. 1 = DataFlash can be written and erased.	
1	bXIR_XSFR	RW	MOVX_@R0/R1 command field control: 0 = MOVX_@R0/R1 for standard xdata area xRAM/xBUS/xSFR. 1 = MOVX_@R0/R1 for xSFR only, not for xRAM/xBUS	0
0	bWDOG_EN	RW	Watchdog reset enable: 0 = as timer only. 1 = enable reset if timer overflow.	0

Chip ID (CHIP_ID):

Bit	Name	Access	Description	Reset value
[7:0]	CHIP_ID	RO	Always 59h, used for chip identification	59h

Safe mode control register (SAFE_MOD):

Bit	Name	Access	Description	Reset value
[7:0]	SAFE_MOD	WO	To enter or get out of safe mode	00h

Some SFRs can only be written in safe mode, while they are always read-only in non-safe mode. Steps to enter safe mode:

(1). Write 55h to register.

(2). Write AAh to register.

(3). 13-23 system frequency periods are in safe mode, one or more safe SFRs or general SFRs can be changed during this time.

(4). After the period expires, safe mode ends automatically.

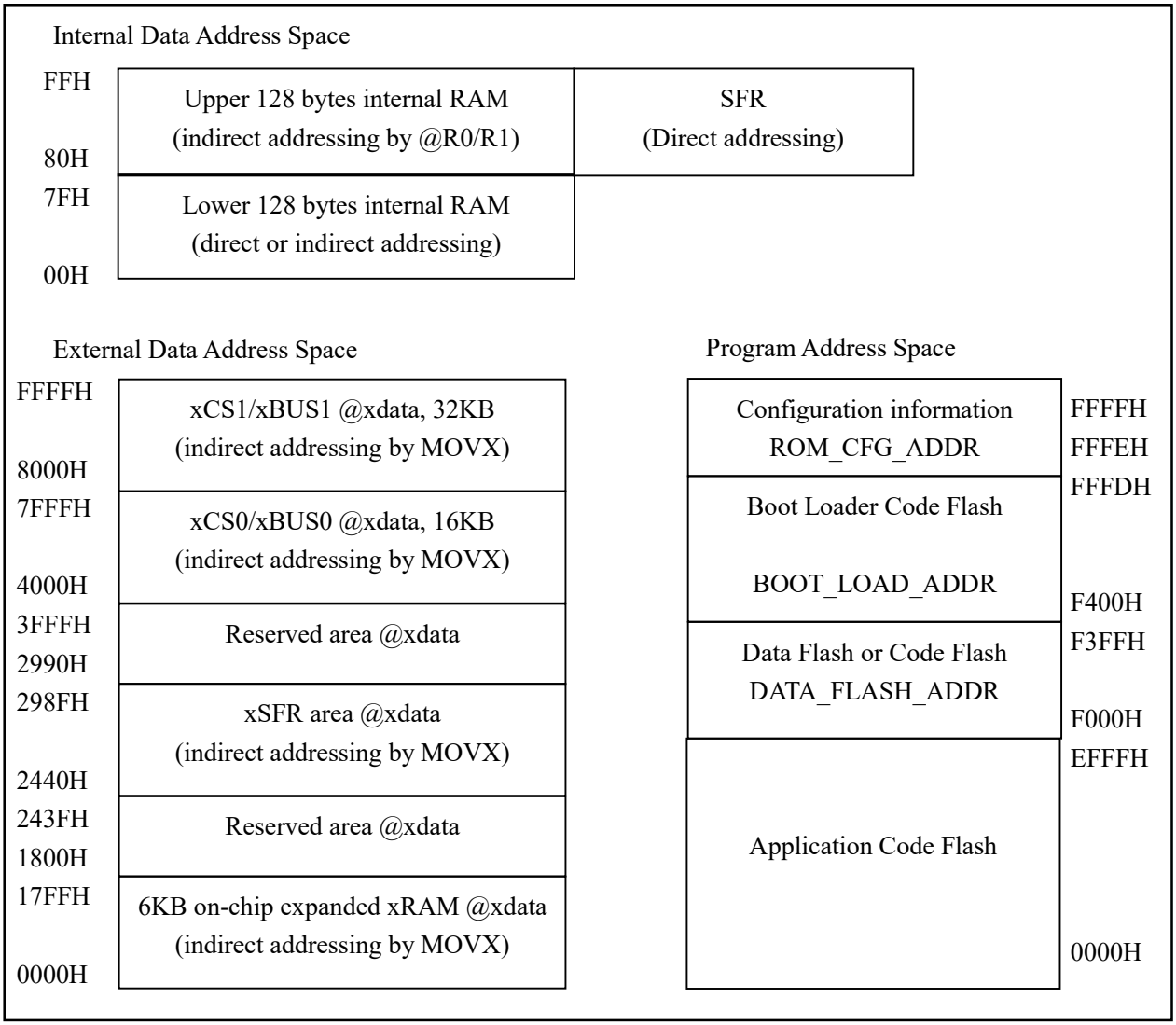
(5). Write anything to this register can get out of safe mode in advance.

6. Memory structure

6.1 Memory space

CH559 addressing memory is divided into program memory, internal code memory and external data memory.

Figure 6.1 Diagram of memory structure



6.2 Program memory

Program memory is total 64KB, as shown in Figure 6.1, and all is used for flash-ROM, including CodeFlash to save the command code, DataFlash to save the non-volatile data, and Configuration Information space to configure the information.

DataFlash addressing from F000h to F3FFH, supports byte (8 bit) read, dual-byte(16 bit) write and block (1K byte) erase, keeping the data after chip power-down, and also may be used for CodeFlash.

CodeFlash includes application code of low address and Bootloader code of high address, they can also be combined with DataFlash for storing single application code.

Configuration information is total 16 bit, and may be configured by programmer, refer to Table 6.1.

Table 6.2 Description of flash-ROM Configuration Information

Address	Name	Description	Recommended value
15	Code_Protect	Code and data protection mode of flash-ROM: 0 = Reading behavior forbidden. 1 = Reading behavior permit.	0/1
14	No_Boot_Load	BootLoader start mode enable: 0 = Start from address 0000h. 1 = Start from address F400h.	1
13	En_Long_Reset	Additional delay during power-up reset enable: 0 = Standard short reset. 1 = Long reset, add 87mS.	0
12	XT_OSC_Strong	Crystal oscillator output driving ability: 0 = Standard. 1 = Enhanced.	0
11	En_P5.7_RESET	P5.7 reset function enable: 0 = Disable. 1 = Enable.	1
10	En_P0_Pullup	P0 pull-up resistor enable during system reset: 0 = Disable. 1 = Enable.	1
9	Must_1	(Auto set to 1 by the programmer)	1
8	Must_0	(Auto set to 0 by the programmer)	0
[7:0]	All_1	(Auto set to FFh by the programmer)	FFh

6.3 Data memory space

Internal data memory is total 256 bytes, as shown in figure 6.1, are all used for SFR and iRAM, iRAM is used for stack and fast data cache ,including R0-R7, bit data, byte data, and idata.

External data memory is total 64KB, as shown in figure 6.1, 6KB of it are used for on-chip xRAM and xSFR, except the reserved area, others (4000h to FFFFh) are all used for external parallel bus.

6.4 flash-ROM register

Table 6.4 List of flash-ROM registers

Name	Address	Description	Reset value
ROM_DATA_H	8Fh	Flash-ROM data register high byte	xxh
ROM_DATA_L	8Eh	Flash-ROM data register low byte	xxh
ROM_DATA	8Eh	16-bit SFR consists of ROM_DATA_L and ROM_DATA_H	xxxxh
ROM_STATUS	86h	flash-ROM status register (read only)	80h
ROM_CTRL	86h	flash-ROM control register (write only)	00h
ROM_ADDR_H	85h	flash-ROM address register high byte	xxh
ROM_ADDR_L	84h	flash-ROM address register low byte	xxh
ROM_ADDR	84h	16-bit SFR consists of ROM_ADDR_L and ROM_ADDR_H	xxxxh

Flash-ROM address register (ROM_ADDR):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_ADDR_H	RW	Flash-ROM address register high byte	xxh
[7:0]	ROM_ADDR_L	RW	Flash-ROM address register low byte, supports even address only	xxh

Flash-ROM data register (ROM_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_DATA_H	RW	Flash-ROM data register high byte	xxh
[7:0]	ROM_DATA_L	RW	Flash-ROM data register low byte	xxh

Flash-ROM control register (ROM_CTRL):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_CTRL	WO	Flash-ROM control register	00h

Flash-ROM status register (ROM_STATUS):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	1
6	bROM_ADDR_OK	RO	Flash-ROM address valid: 0 = Invalid. 1 = Valid.	0
[5:2]	Reserved	RO	Reserved	0000b
1	bROM_CMD_ERR	RO	Flash-ROM command error: 0 = Valid. 1 = Unknown command.	0
0	bROM_CMD_TOUT	RO	Flash-ROM operation result: 0 = Success. 1 = Time out.	0

6.5 flash-ROM operation steps

1. Flash-ROM erase, changing all data bits in the target block to 1:
   (1). Get into safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
   (2). Enable writing by setting GLOBAL_CFG, bCODE_WE corresponds to code, and bDATA_WE to data;
   (3). Set ROM_ADDR, write in 16-bit destination address, high 6-bit valid only;
   (4). Set ROM_CTRL to 0A6h, execute block erase, and the program will suspend during the operation;
   (5). After the operation ,the program goes on, read ROM_STATUS to check the operation result. If multiple blocks need to be erased, repeat steps from (3) to(5);
   (6). Get into safe mode again, SAFE_MOD = 55h;SAFE_MOD = 0AAh;

(7). Disable writing by setting GLOBAL_CFG, bCODE_WE = 0, bDATA_WE = 0.

2. Flash-ROM write, changing some data bits in the target dual byte from 1 to 0:
   (1). Get into safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
   (2). Enable writing by setting GLOBAL_CFG, bCODE_WE corresponds to code, and bDATA_WE to data;
   (3). Set ROM_ADDR, write in 16-bit destination address, high 15-bit valid only;
   (4). Set ROM_DATA, write in 16-bit data, step (3) and step (4) may be exchanged;
   (5). Set ROM_CTRL to 09Ah, execute writing, and the program will suspend during the operation;
   (6). After the operation ,the program goes on, read ROM_STATUS to check the operation result. If multiple data need to be written , repeat steps from (3) to (6);
   (7). Get into safe mode again, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
   (8). Set GLOBAL_CFG to disable writing, bCODE_WE = 0, bDATA_WE = 0.

3. Flash-ROM read:
   Read data or code from the destination address through instruction MOVC or pointer of program area.

6.6 On-board program and ISP download

When Code_Protect = 1, code and data in CH559 flash-ROM may be read and written through synchronous serial interface by the programmer. When Code_Protect = 0, all code and data in CH559 flash-ROM are protected, it can be erased but not read, Code_Protect will be removed after erase when power-up.

When CH559 presets Bootloader, CH559 supports downloading application code through USB or UART. Without Bootloader, application code and Bootloader may only download through specialized programmer. Reserve 5 wires between CH559 and programmer for on-board programming in the circuit.

Table 6.6.1 Wires between CH559 and programmer

Pin	GPIO	Description
RST	P5.7	Reset control, get into programming state when high level
SCS	P1.4	Chip selection, high level default, active low
SCK	P1.7	Clock in
MOSI	P1.5	Data in
MISO	P1.6	Data out

6.7 Global unique ID

CH559 MCUs all have a global unique identification number (ID) when out of factory. ID and verification total 8 bytes, located in the special read-only register form address 20h. User can get ID by reading CodeFlash when E_DIS is 1 and global interrupt is disabled. For details, please refer to program routine GETID.C.

Table 6.7.1 Chip ID address table

Address	ID description
20h, 21h	ID number first word, little-endian
22h, 23h	ID number second word, little-endian
24h, 25h	ID number third word, little-endian
26h, 27h	ID number word CUSUM verification

The ID number can be used with the downloading tools to encrypt the target program. For the general application, only the first 32 bits of the ID number are used.

7. Power management, sleep and reset

7.1 External power in

CH559 works at voltage 3.3V inside, I/O input and output at 3.3V ,except pins: P1.0～P1.7, XI, XO, RST, all pins may tolerate 5V input, built-in 5V to 3.3V LDO, support external 3.3V and 5V input, reference below:

External power voltage	VIN5 voltage: 3.3V-5V	VDD33 voltage: 3.3V
3.3V Including <3.6V	3.3V voltage input. A decoupling capacitor not less than 0.1uF to the ground necessarily.	External 3.3V input is used for internal operating voltage. A decoupling capacitor not less than 0.1uF to the ground necessarily.
5V Including >3.6V	5V voltage input. A decoupling capacitor not less than 0.1uF to the ground necessarily.	Internal voltage adapter 3.3V output and internal 3.3V operating power input. A decoupling capacitor not less than 3.3uF to the ground necessary.

After power-on or system reset, CH559 is in running status by default. When some function modules are unused, close their clocks to reduce power dissipation. When CH559 is no need to run, set PD in PCON to get into sleep modes, and may be waked up by USB, UART0, UART1, SPI0 or some GPIOs.

7.2 Power and sleep control register

Table 7.2.1 Power and sleep control registers

Name	Address	Description	Reset value
WDOG_COUNT	FFh	Watchdog count register	00h
RESET_KEEP	FEh	Reset keep register	00h
WAKE_CTRL	EBh	Wake-up control register	00h
SLEEP_CTRL	EAh	Sleep control register	00h
PCON	87h	Power control register	10h

Watchdog count register (WDOG_COUNT):

Bit	Name	Access	Description	Reset value
[7:0]	WDOG_COUNT	RW	Watchdog current count value, the interrupt flag bWDOG_IF_TO will auto-set 1 when Watchdog count register overflows. WDOG_COUNT overflows when count to 0FFh and turn to 00h.	00h

Reset keep register (RESET_KEEP):

Bit	Name	Access	Description	Reset value
[7:0]	RESET_KEEP	RW	Reset keeping register, it may be modified by setting, except	00h

			power-on reset may set it 0, no other resets may change it.	

Wake-up control register (WAKE_CTRL), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bWAK_BY_USB	RW	USB event wake-up enable: 1 = Enable. 0 = Disable.	0
6	bWAK_RXD1_LO	RW	UART1 pin RXD1 low-level input event wake-up enable: 0 = Disable. 1 = Enable. Select XA/XB differential input in iRS485 mode, otherwise, select RXD1 or RXD1_ according to bIER_PIN_MOD1=1/0	0
5	bWAK_P1_5_LO	RW	P1.5 low-level wake-up enable 0 = Disable. 1 = Enable.	0
4	bWAK_P1_4_LO	RW	P1.4 low-level wake-up enable 0 = Disable. 1 = Enable.	0
3	bWAK_P0_3_LO	RW	P0.3 low-level wake-up enable 0 = Disable. 1 = Enable.	0
2	bWAK_CAP3_LO	RW	Timer3 low-level input event wake-up in capture mode: 0 = Disable. 1 = Enable. Select CAP3 or CAP3_ according to bTMR3_PIN_X=0/1.	0
1	bWAK_P3_2E_3L	RW	P3.2 edge change and P3.3 low-level wake-up enable: 0 = Disable. 1 = Enable.	0
0	bWAK_RXD0_LO	RW	UART0 pin RXD0 low-level input wake-up enable: 0 = Disable. 1 = Enable. Select RXD0 or RXD0_ according to bUART0_PIN_X=0/1	0

Sleep control register (SLEEP_CTRL), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bSLP_OFF_USB	RW	USB clock off control 1 = clock off.	0
6	bSLP_OFF_ADC	RW	ADC clock off control 1 = clock off.	0
5	bSLP_OFF_UART1	RW	UAR1 clock off control 1 = clock off.	0

4	bSLP_OFF_P1S1	RO	PWM1 and SPI1 clock off control 1 = clock off.	0
3	bSLP_OFF_SPI0	RW	SPI0 clock off control 1 = clock off.	0
2	bSLP_OFF_TMR3	RW	Timer3 clock off control 1 = clock off.	0
1	bSLP_OFF_LED	RW	LED-CTRL clock off control 1 = clock off.	0
0	bSLP_OFF_XRAM	RW	xRAM clock off control 1 = clock off.	0

Power control register (PCON):

Bit	Name	Access	Description	Reset value
7	SMOD	RW	Baud rate selection for UART0 mode 1/2/3 when timer1 is used to generate UART0 baud rate: 0 = Slow mode. 1 = Fast mode.	0
6	Reserved	RO	Reserved	0
5	bRST_FLAG1	RO	Recent reset flag high bit	0
4	bRST_FLAG0	RO	Recent reset flag low bit	1
3	GF1	RW	General purpose flag bit 1 User-defined. Can be reset or set by software	0
2	GF0	RW	General purpose flag bit 0 User-defined. Can be reset or set by software	0
1	PD	RW	Power-down enable bit Sleep after set to 1. Auto cleared by wake-up hardware.	0
0	Reserved	RO	Reserved	0

Table 7.2.2 Description of recent reset flag

bRST_FLAG1	bRST_FLAG0	Description of reset flag
0	0	Software reset, source: bSW_RESET=1 and (bBOOT_LOAD=0 or bWDOG_EN=1)
0	1	Power on reset, source: voltage on VDD33 is lower than checking voltage
1	0	Watchdog reset, source: bWDOG_EN=1 and watchdog timeout overflows
1	1	External input manual reset by RST pin, source: En_P5.7_RESET=1 and P5.7 high-level input

7.3 Reset control

CH559 has 4 reset sources: power-on reset, external input reset, software reset and watchdog reset. The latter three are hot reset.

7.3.1 Power on reset

Power-on reset (POR) generates from internal voltage detecting circuit. It keeps detecting voltage on VDD33. POR is generated when the detecting voltage is lower than Vpot, and auto delay Tpor to keep reset status. CH559 runs at the end of delay.

Only power on reset can enable CH559 to reload the configuration information and reset RESET_KEEP, other hot resets do not affect.

7.3.2 External input reset

External input reset is generated by the high-level on RST. When En_P5.7_RESET = 1, and high-level on RST keeping time is longer than the Trsrt, the reset occurs. After high-level ends, auto delay Trdl to keep reset status, CH559 runs from address 0 after delay.

7.3.3 Software reset

CH559 supports internal software reset to reset the CPU and restart without external intervention. Set bSW_RESET in GLOBAL_CFG to 1 to execute software reset, and auto delay Trdl to keep reset status. CH559 runs from address 0 after delay, and the bSW_RESET bit is reset automatically by hardware.

When bSW_RESET is set to 1, if bBOOT_LOAD=0 or bWDOG_EN=1, then bRST_FLAG1/0 will indicate the software reset after reset. When bSW_RESET is set to 1, if bBOOT_LOAD=1 and bWDOG_EN=0, then bRST_FLAG1/0 will keep the reset flag of last time and no new flag.

Bootloader runs first after power-on reset if ISP Bootloader is downloaded, it switches to the application code through software reset based on requirement. This software reset will clear bBOOT_LOAD, but not affect bRST_FLAG1/0 (as bBOOT_LOAD=1 before reset), so bRST_FLAG1/0 still indicates power on reset status after switching to application state.

7.3.4 Watchdog reset

Watchdog reset occurs when the watchdog timer overflows. Watchdog timer is an 8-bit counter, whose clock frequency is Fsys/262144, and the overflow signal is generated when count to 0FFh and turn to 00h.

Watchdog timer overflow signal will trigger bWDOG_IF_TO to 1, which is automatically reset when WDOG_COUNT is reloaded or when it goes into corresponding interrupt service.

Write different initial values to WDOG_COUNT to realize different timing period Twdc. When the system clock is 12MHz, Twdc is about 5.9s when 00h is written, and about 2.8s when 80h is written.

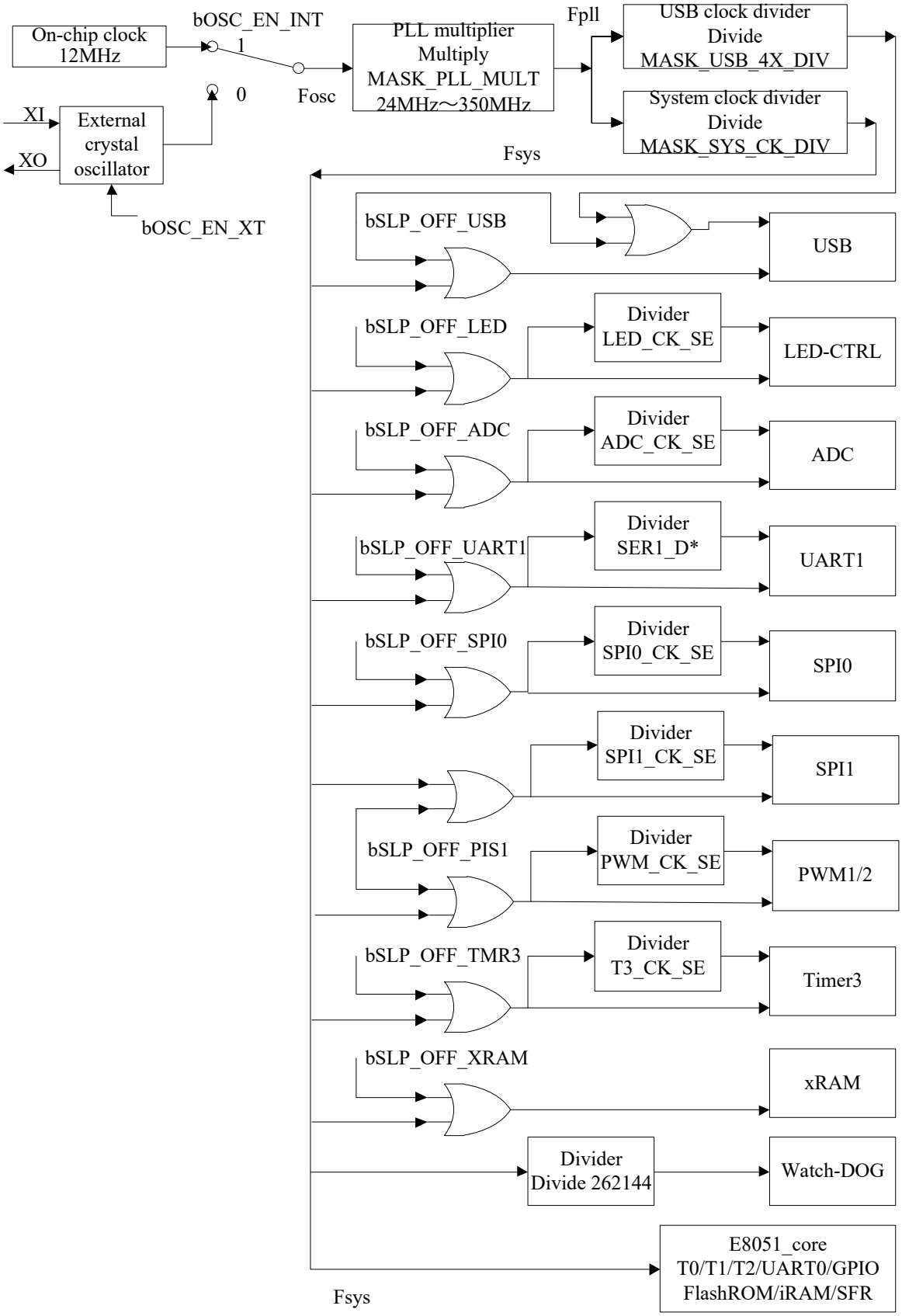
When watchdog timer overflows and bWDOG_EN=1, watchdog reset occurs. Auto delay Trdl to keep reset status. CH559 runs from address 0 after delay.

Clear WDOG_COUNT timely to avoid watchdog reset when bWDOG_EN = 1.

8. System clock

8.1 Diagram of clock

Figure 8.1.1 Clock system and structure diagram



Select one of internal clock or external clock as source clock, then generate high frequency Fpll after frequency multiplier PLL. Generate system clock Fsys and USB module clock Fusb4x after 2 frequency dividers. The system clock Fsys is provided to different modules of CH559 directly or after clock gate, to

reduce power dissipation, set sleep control register to close unused modules clocks.

8.2 Register description

Table 8.2.1 List of clock control registers

Name	Address	Description	Reset value
CLOCK_CFG	B3h	System clock configuration register	98h
PLL_CFG	B2h	PLL clock configuration register	D8h

System clock configuration register (CLOCK_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bOSC_EN_INT	RW	On-chip crystal oscillator enable 1 = Enable. 0 = On-chip crystal oscillator disabled and external crystal oscillator enabled	1
6	bOSC_EN_XT	RW	External crystal oscillator enable 1 = Enable, a crystal or ceramic oscillator to XI (P4.6) and XO (P4.7). An external quartz crystal or ceramic oscillator needs to be connected between XI and XO. 0 = Disable external oscillator.	0
5	bWDOG_IF_TO	RO	Watchdog interrupt flag: 1 = Interrupt from timer overflow. 0 = No interrupt. This bit will be automatically reset after WDOG_COUNT reloads or gets into corresponding interrupt service.	0
[4:0]	MASK_SYS_CK_DIV	RW	System clock frequency division factor 00000b means 100000b.	11000b

PLL clock configuration register (PLL_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
[7:5]	MASK_USB_4X_DIV	RW	USB clock divisor factor, 000b means 1000b.	110b
[4:0]	MASK_PLL_MULT	RW	PLL reference clock multiplier factor	11000b

8.3 Clock Configuration

CH559 uses on-chip 12 MHz clock after power-on by default. And select on-chip clock or external clock by CLOCK_CFG. Pins XI and XO may be used as GPIOs when external crystal oscillator is disabled. Connect an oscillator between pins XI and XO when external crystal oscillator is enabled. In addition, connect a oscillating capacitor between XI and GND, XO and GND. When external clock is input directly, connect it to XI and keep XO suspended.

Source clock frequency: Fosc = bOSC_EN_INT ? 12MHz : Fxt
PLL frequency: Fpll = Fosc * (PLL_CFG & MASK_PLL_MULT)
USB clock divisor factor: Kusb = (PLL_CFG & MASK_USB_4X_DIV) >> 5
USB clock: Fusb4x = Fpll / (Kusb? Kusb: 8)

System clock divisor factor: Ksys = CLOCK_CFG & MASK_SYS_CK_DIV
System frequency: Fsys = Fpll / (Ksys? Ksys: 32)
Default status after reset, Fosc=12MHz, Fpll=288MHz, Fub4x=48MHz, Fsys=12MHz.

Steps to switch to external crystal oscillator:
(1). Get into safe mode, SAFE_MOD = 55h, SAFE_MOD = AAh;
(2). Set bOSC_EN_XT in CLOCK_CFG to 1 with "OR" operation, other bits remain unchanged, to enable crystal oscillator;
(3). Delay several milliseconds, usually 5mS ~ 10mS, to wait oscillator work steadily;
(4). Get into safe mode again, SAFE_MOD = 55h, SAFE_MOD = AAh;
(5). Clear bOSC_EN_INT in CLOCK_CFG with "AND" operation, other bits remain unchanged, to switch to external crystal oscillator;
(6). Get out of safe mode. Write any value into SAFE_MOD to get out of safe mode.

Steps to modify system frequency:
(1). Calculate PLL_CFG and CLOCK_CFG in advance to avoid beyond term of safe mode;
(2). Get into safe mode, SAFE_MOD = 55h, SAFE_MOD = AAh;
(3). Write new value to PLL_CFG;
(4). Write new value to CLOCK_CFG;
(5). Get out of safe mode. Write any value into SAFE_MOD to get out of safe mode.

Notes:
(1). PLL frequency is recommended not to beyond 24MHz~350MHz;
(2). Priority-use-of lower Fsys to reduce dynamic power dissipation and get wider Working temperature;;
(3). Set Fusb4x 48MHz when USB module enabled;
(4). Changing external crystal and modifying system frequency are two separate operations, suggestion in two conditions:
  (A). If external crystal oscillator frequency is less than 13MHz, switch to external crystal first and then modify system frequency.
  (B). If external crystal oscillator frequency is more than 13MHz, reduce PLL reference clock multiplier factor to avoid Fpll overflow first, then switch to external crystal, and modify system frequency at last, or modify system frequency when modify PLL_CFG.

9. Interrupt

CH559 supports maximum 14 interrupt sources, including 6 sources compatible with standard MCS51 interrupt: INT0, T0, INT1, T1, UART0, T2, and 8 extend interrupt sources: SPI0, TMR3, USB, ADC, UART1, PWM1, WDOG, and GPIO which can be selected from 7 I/O pins.

9.1 Register description

Table 9.1.1 List of interrupt vector

Interrupt	Entry address	Interrupt No.	Description	Default priority
INT_NO_INT0	0x0003	0	External interrupt0 (bLED_OUT_EN=0) or LED control card interrupt (bLED_OUT_EN=1)	High priority

INT_NO_TMR0	0x000B	1	Timer0 interrupt	↓
INT_NO_INT1	0x0013	2	External interrupt1	↓
INT_NO_TMR1	0x001B	3	Timer1 interrupt	↓
INT_NO_UART0	0x0023	4	UART0 interrupt	↓
INT_NO_TMR2	0x002B	5	Timer2 interrupt	↓
INT_NO_SPI0	0x0033	6	SPI0 interrupt	↓
INT_NO_TMR3	0x003B	7	Timer3 interrupt	↓
INT_NO_USB	0x0043	8	USB interrupt	↓
INT_NO_ADC	0x004B	9	ADC interrupt	↓
INT_NO_UART1	0x0053	10	UART1 interrupt	↓
INT_NO_PWM1	0x005B	11	PWM1 interrupt	↓
INT_NO_GPIO	0x0063	12	GPIO interrupt	Low
INT_NO_WDOG	0x006B	13	Watchdog timer interrupt	priority

Table 9.1.2 List of interrupt registers

Name	Address	Description	Reset value
IP_EX	E9h	Extend interrupt priority register	00h
IE_EX	E8h	Extend interrupt enable register	00h
GPIO_IE	CFh	GPIO interrupt enable register	00h
IP	B8h	Interrupt priority register	00h
IE	A8h	Interrupt enable register	00h

Interrupt enable register (IE):

Bit	Name	Access	Description	Reset value
7	EA	RW	Global interrupt enable 1= Interrupt is enabled when E_DIS is 0. 0 = All interrupt requests are disabled.	0
6	E_DIS	RW	Global interrupt disable 1 = All interrupt requests are disabled. 0 = Interrupt is enabled when EA is 1. This bit is usually used to disable interrupt temporarily during flash-ROM operation.	0
5	ET2	RW	Timer2 interrupt enable 1 = T2 interrupt is enabled. 0 = T2 interrupt is disabled.	0
4	ES	RW	UART0 interrupt enable 1 = UART0 interrupt is enabled. 0 = UART0 interrupt is disabled.	0
3	ET1	RW	Timer1 interrupt enable 1 = T1 interrupt is enabled. 0 = T1 interrupt is disabled.	0
2	EX1	RW	External interrupt1 enable	0

			1 = INT1 interrupt is enabled. 0 = INT1 interrupt is disabled.	
1	ET0	RW	Timer0 interrupt enable 1 = T0 interrupt is enabled. 0 = T0 interrupt is disabled.	0
0	EX0	RW	External interrupt0 and LED control card interrupt enable 1 = INT0/LED interrupt (selected by bLED_OUT_EN) is enabled. 0 = INT0/LED interrupt is disabled.	0

Extend interrupt enable register (IE_EX):

Bit	Name	Access	Description	Reset value
7	IE_WDOG	RW	Watchdog timer interrupt enable 1 = WDOG interrupt is enabled. 0 = WDOG interrupt is disabled.	0
6	IE_GPIO	RW	GPIO interrupt enable 1 = GPIO interrupt is enabled. 0 = GPIO interrupt is disabled.	0
5	IE_PWM1	RW	PWM1 interrupt enable 1 = PWM1 interrupt is enabled. 0 = PWM1 interrupt is disabled.	0
4	IE_UART1	RW	UART1 interrupt enable 1 = UART1 interrupt is enabled. 0 = UART1 interrupt is disabled.	0
3	IE_ADC	RW	ADC interrupt enable 1 = ADC interrupt is enabled. 0 = ADC interrupt is disabled.	0
2	IE_USB	RW	USB interrupt enable 1 = USB interrupt is enabled. 0 = USB interrupt is disabled.	0
1	IE_TMR3	RW	Timer3 interrupt enable 1 = Timer3 interrupt is enabled. 0 = Timer3 interrupt is disabled.	0
0	IE_SPI0	RW	SPI0 interrupt enable 1 = SPI0 interrupt is enabled. 0 = SPI0 interrupt is disabled.	0

GPIO interrupt enable register (GPIO_IE):

Bit	Name	Access	Description	Reset value
7	bIE_IO_EDGE	RW	GPIO edge interrupt mode enable: 0 = Level interrupt mode. bIO_INT_AC = 1 and interrupt will be requested constantly if there is a valid GPIO input	0

			level; otherwise, bIO_INT_AC = 0 and no interrupt request occurs with invalid GPIO input level. 1 = Edge interrupt mode. There are interrupt flag bIO_INT_ACT and interrupt request with valid GPIO input edge, bIO_INT_ACT cannot be cleared by software, but it is automatically cleared when reset or interrupt program is running in level interrupt mode.	
6	bIE_RXD1_LO	RW	1 = UART1 RX PIN interrupt is enabled (valid while low level in level mode or falling edge in edge mode). 0 = UART1 RX PIN interrupt is disabled. In IRS485 mode, XA/XB differential input is selected; In non-IRS485 mode, select RXD1 (bIER_PIN_MOD1 = 1) or RXD1_ (bIER_PIN_MOD1 = 0).	0
5	bIE_P5_5_HI	RW	1 = P5.5 interrupt is enabled (valid with high level in level mode or rising edge in edge mode). 0 = P5.5 interrupt is disabled.	0
4	bIE_P1_4_LO	RW	1 = P1.4 interrupt is enabled (valid with low level in level mode or falling edge in edge mode). 0 = P1.4 interrupt is disabled.	0
3	bIE_P0_3_LO	RW	1 = P0.3 interrupt is enabled (valid with low level in level mode or falling edge in edge mode). 0 = P0.3 interrupt is disabled.	0
2	bIE_P5_7_HI	RW	1 = P5.7 interrupt is enabled (valid with high level in level mode or rising edge in edge mode). 0 = P5.7interrupt is disabled.	0
1	bIE_P4_1_LO	RW	1 = P4.1 interrupt is enabled (valid with low level in level mode or falling edge in edge mode). 0 = P4.1 interrupt is disabled.	0
0	bIE_RXD0_LO	RW	1 = UART0 RX interrupt is enabled (valid with low level in level mode or falling edge in edge mode). 0 = UART0 RX interrupt is disabled. Select RXD0 (bUART0_PIN_X = 0) or RXD0_ (bUART0_PIN_ X = 1).	0

Interrupt priority register (IP):

Bit	Name	Access	Description	Reset value
7	PH_FLAG	RO	High priority interrupt running flag	0
6	PL_FLAG	RO	Low priority interrupt running flag	0
5	PT2	RW	Timer2 interrupt priority control bit	0
4	PS	RW	UART0 interrupt priority control bit	0
3	PT1	RW	Timer1 interrupt priority control bit	0
2	PX1	RW	External interrupt1 priority control bit	0
1	PT0	RW	Timer0 interrupt priority control bit	0

0	PX0	RW	External interrupt0 and LED control card interrupt priority control bit	0

Extend interrupt priority register (IP_EX):

Bit	Name	Access	Description	Reset value
7	bIP_LEVEL	RO	Current interrupt nesting level flag 0 = No interrupt or dual interrupt nesting. 1 = Single interrupt nesting.	0
6	bIP_GPIO	RW	GPIO interrupt priority control	0
5	bIP_PWM1	RW	PWM1 interrupt priority control	0
4	bIP_UART1	RW	UART1 interrupt priority control	0
3	bIP_ADC	RW	ADC interrupt priority control	0
2	bIP_USB	RW	USB interrupt priority control	0
1	bIP_TMR3	RW	Timer3 interrupt priority control	0
0	bIP_SPI0	RW	SPI0 interrupt priority control	0

IP and IP_EX registers are used for interrupt priority setting. The corresponding interrupt source will be high (low) priority if this bit is 1 (0). There is default priority order (refer to Table 9.1.1) for interrupt sources in the same level, the current interrupt priority is shown by PH_FALG combined with PL_FLAG.

Table 9.1.3 Current interrupt priority description

PH_FLAG	PL_FLAG	Interrupt priority state at present
0	0	No interrupt at present
0	1	Low priority interrupt is running at present
1	0	High priority interrupt is running at present
1	1	Unexpected event, unknown error

10. I/O port

10.1 GPIO introduction

CH559 provides maximum 45 I/O pins. Some of them have alternate functions. P0~P3 input&output and P4 output can be addressing by bit.

The pins are general I/O port state if not set reused. All I/O ports have real “read-change-write” function and support SETB or CLR command to change the direction and level of pins while they are used as general digital I/O pins.

10.2 GPIO register

All registers and bits in this section are generally expressed: “n” (n = 0, 1, 2, 3) to express the serial number of ports, “x” (x = 0, 1, 2, 3, 4, 5, 6, 7) to express the serial number of bits.

Table 10.2.1 List of GPIO registers

Name	Address	Description	Reset value
P0	80h	P0 input/output register	FFh
P0_DIR	C4h	P0 direction control register	00h
P0_PU	C5h	P0 pull-up enable register	00h/FFh
P1	90h	P1 input/output register	FFh
P1_IE	B9h	P1 input enable register	FFh
P1_DIR	BAh	P1 direction control register	00h
P1_PU	BBh	P1 pull-up enable register	FFh
P2	A0h	P2 input/output register	FFh
P2_DIR	BCh	P2 direction control register	00h
P2_PU	BDh	P2 pull-up enable register	FFh
P3	B0h	P3 input/output register	FFh
P3_DIR	BEh	P3 direction control register	00h
P3_PU	BFh	P3 pull-up enable register	FFh
P4_OUT	C0h	P4 output register	00h
P4_IN	C1h	P4 input register (read-only):	FFh
P4_DIR	C2h	P4 direction control register	00h
P4_PU	C3h	P4 pull-up enable register	FFh
P4_CFG	C7h	P4 configuration register	00h
P5_IN	C7h	P5 input register (read-only):	00h
PIN_FUNC	CEh	Pin function selection register	00h
PORT_CFG	C6h	Port configuration register	0Fh
XBUS_SPEED	FDh	Bus speed configuration register	FFh
XBUS_AUX	A2h	Bus auxiliary configuration register	00h

Port configuration register (PORT_CFG):

Bit	Name	Access	Description	Reset value
[7:4]	bPn_DRV	RW	Port Pn output driver ability select: 0 = Driver current is 5mA level. 1 = Driver current is 20mA level for P0/P2/P3, 10mA for P1.	0000b
[3:0]	bPn_OC	RW	Port Pn open-drain output enable: 0 = Push-pull output. 1 = Open-drain output	1111b

Port Pn input/output register (Pn):

Bit	Name	Access	Description	Reset value
[7:0]	Pn.0～Pn.7	RW	Pn.x pin state input and data output bits, supports addressing by bit.	FFh

Port Pn direction control register (Pn_DIR):

Bit	Name	Access	Description	Reset value
[7:0]	Pn_DIR	RW	Pn.x pin direction setting	00h

P0 pull-up enable register (P0_PU) and Pn pull-up enable register (Pn_PU), n=1/2/3:

Bit	Name	Access	Description	Reset value
[7:0]	P0_PU	RW	P0.x pin pull-up resistor enable (when En_P0_Pullup=0)	00h
			P0.x pin pull-up resistor enable (when En_P0_Pullup=1)	FFh
[7:0]	Pn_PU	RW	Pn.x pin pull-up resistor enable: 0 = Pull-up resistor disabled. 1 = Pull-up resistor enabled.	FFh

Port Pn configuration is realized by bPn_OC (in PORT_CFG), Pn_DIR and Pn_PU, details as follows.

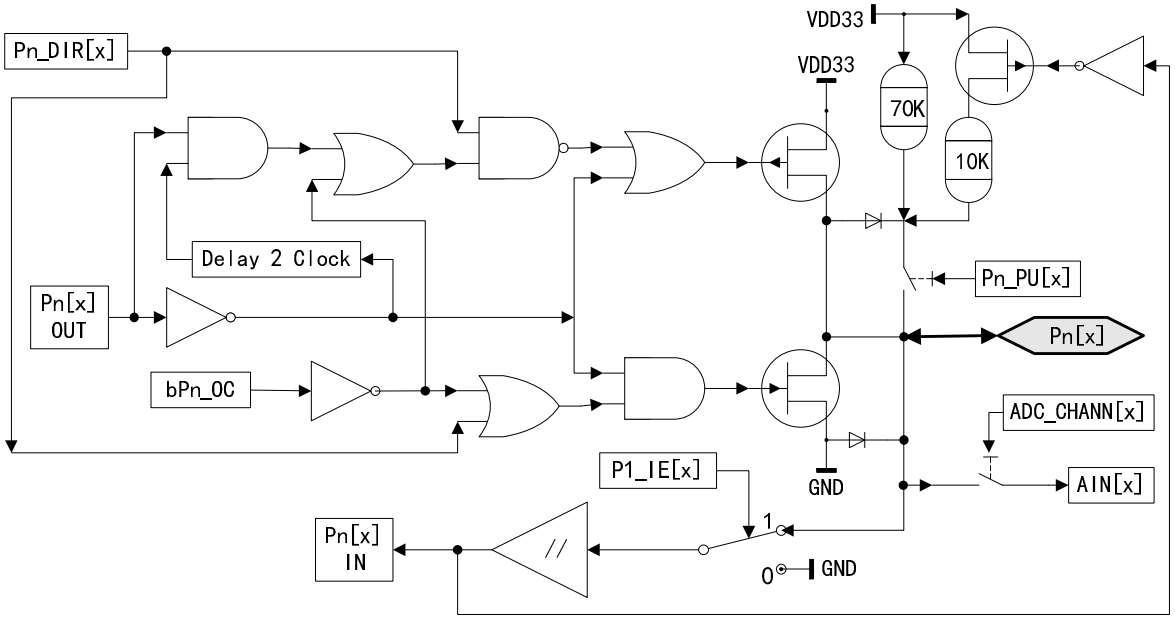
Table 10.2.2 Port configuration register combination

bPn_OC	Pn_DIR	Pn_PU	Description of working mode
0	0	0	High impedance input mode, pins without pull-up resistor
0	0	1	Pull-up input mode, pins with pull-up resistor
0	1	X	Push-pull output mode with symmetry driving ability, a port can output or absorb large current in this mode
1	0	0	High-impedance input weak standard bi-directional mode with open drain output, pins without pull-up resistor
1	1	0	High-impedance input standard bi-directional mode, open-drain output, pins without pull-up resistor, it will automatically generate 2 clock period of high level to accelerate conversion when output transfer from low level to high level
1	0	1	Weak standard bi-direction mode (as 8051) with pull-up resistor of pin, open drain output, input function is also supported
1	1	1	Standard bi-direction mode (standard 8051) with pull-up resistor of pin, open drain output, input function is also supported. it will automatically generate 2 clock period of high level to accelerate conversion when output transfer from low level to high level

Ports P0-P3 support pure input, push-pull output and standard bi-direction modes, P4 supports pure input and push-pull output modes. There are controllable internal pull-up resistors attached to VDD33 and protection diodes attached to GND for all pins.

Figure 10.2.1 shows pins p1.x of P1, also suitable for ports P0, P2 and P3 without P1_IE, AIN or ADC_CHANN.

Figure 10.2.1 Equivalent schematic diagram of I/O pins



P1 input enable register (P1_IE):

Bit	Name	Access	Description	Reset value
[7:0]	P1_IE	RW	Pin P1.x input enable 0 = Enable ADC analog input, and disable digital input. 1 = Enable digital input.	FFh

10.3 P4 port

P4 output register (P4_OUT):

Bit	Name	Access	Description	Reset value
[7:0]	P4_OUT.0～P4_OUT.7	RW	Pin P4.x data output bit, support addressing by bit	00h

P4 input register (P4_IN):

Bit	Name	Access	Description	Reset value
[7:0]	P4_IN	RO	Pin P4.x state input bit	FFh

P4 pull-up enable register (P4_PU):

Bit	Name	Access	Description	Reset value
[7:0]	P4_PU	RW	Pin P4.x pull-up resistor enable 0 = Pull-up resistor disabled. 1 = Pull-up resistor enabled.	FFh

P4 direction control register (P4_DIR):

Bit	Name	Access	Description	Reset value
[7:0]	P4_DIR	RW	Pin P4.x direction setting: 0 = Input. 1 = Output.	00h

P4 configuration register (P4_CFG) and P5 input register (P5_IN):

Bit	Name	Access	Description	Reset value
7	P5.7	R0	Pin P5.7 state input bit	0
6	bIO_INT_ACT	R0	GPIO interrupt request activation state: When bIE_IO_EDGE=0: 1 = There is valid GPIO input level and interrupt occurs. 0 = Invalid input level. When bIE_IO_EDGE=1, it is used as edge interrupt flag: 1 = A valid edge is detected, it cannot be reset by software and only can be reset automatically when reset or interrupt program is running in level interrupt mode.	0
5	P5.5	R0	Pin P5.5 state input bit, controllable pull-down resistor inside	0
4	P5.4	R0	Pin P5.4 state input bit, controllable pull-down resistor inside	0
3	bSPI0_PIN_X	RW	SPI0 SCS/SCK mapping enable 0 = Enable P1.4/P1.7. 1 = Enable P4.6/P4.7.	0
2	bP4_DRV	RW	P4 output ability select: 0 = Driving current is 5mA level. 1= Driving current is 20mA level.	0
1	P5.1	R0	Pin P5.1 state input bit, controllable pull-down resistor inside	0
0	P5.0	R0	Pin P5.0 state input bit, controllable pull-down resistor inside	0

10.4 GPIO alternate functions and mapping

Some of I/O pins of CH559 have alternate functions and are general I/O pins when powered, they are set corresponding pins if used as different function modules.

Pin function selection register (PIN_FUNC):

Bit	Name	Access	Description	Reset value
7	bPWM1_PIN_X	RW	Pin PWM1/PWM2 mapping enable bit: 0 = PWM1/2 enable P2.4/P2.5. 1 = PWM1/2 enable P4.3/P4.5.	0

6	bTMR3_PIN_X	RW	Pin PWM3/CAP3 mapping enable bit: 0 = PWM3/CAP3 enable P1.2. 1 = PWM3/CAP3 enable p4.2.	0
5	bT2EX_PIN_X	RW	Pin T2EX/CAP2 mapping enable bit: 0 = T2EX/CAP2 enable P1.1. 1 = T2EX/CAP2 enable P2.5.	0
4	bUART0_PIN_X	RW	Pin UART0 mapping enable bit: 0 = RXD0/TXD0 enable P3.0/P3.1. 1 = RXD0/TXD0 enable P0.2/P0.3.	0
3	bXBUS_EN	RW	XBUS function enable bit: 0 = Disable xbus. 1 = P0 used as 8-bit data bus and P3.6/P3.7 used as read/write select during bus access.	0
2	bXBUS_CS_OE	RW	XBUS chip selection output enable bit: 0 = Disable chip selection output, and it can be decoded by external circuit. 1 = P3.4 used as output of CS0 (XSC0 is 0, active low), bus address A15 is inverted and exported to P3.3 when ALE is disabled (CS is 1, active low).	0
1	bXBUS_AH_OE	RW	XBUS address high 8 bits output enable bit: 0 = Output is disabled. 1 = P2 outputs bus address high 8 bits during MOVX_@DPTR command access to external bus.	0
0	bXBUS_AL_OE	RW	XBUS address low 8 bits output enable bit: 0 = Reusable address mode, it outputs address low 8 bits or data according to demand when access to external bus, latched by external circuit controlled by ALE. 1 = Direct address mode, it outputs address low 8 bits A0-A7 by P4.0-P4.5, P3.5 and P2.7.	0

Table 10.4.1 List of GPIO pins alternate functions

GPIO	Other functions: left-to-right priority
P0[0]	AD0, UDTR/bUDTR, P0.0
P0[1]	AD1, URTS/bURTS, P0.1
P0[2]	AD2, RXD_/bRXD_, P0.2
P0[3]	AD3, TXD_/bTXD_, P0.3
P0[4]	AD4, UCTS/bUCTS, P0.4
P0[5]	AD5, UDSR/bUDSR, P0.5
P0[6]	AD6, URI/bURI, P0.6
P0[7]	AD7, UDCD/bUDCD, P0.7
P1[0]	AIN0, T2/bT2, CAP1/bCAP1, P1.0
P1[1]	AIN1, T2EX/bT2EX, CAP2/bCAP2, P1.1
P1[2]	AIN2, PWM3/bPWM3, CAP3/bCAP3, P1.2
P1[3]	AIN3, P1.3

P1[4]	AIN4, SCS/bSCS, P1.4
P1[5]	AIN5, MOSI/bMOSI, P1.5
P1[6]	AIN6, MISO/bMISO, P1.6
P1[7]	AIN7, SCK/bSCK, P1.7
P2[0]	A8, P2.0
P2[1]	MOSI1/bMOSI1, A9, P2.1
P2[2]	MISO1/bMISO1, A10, P2.2
P2[3]	SCK1/bSCK1, A11, P2.3
P2[4]	PWM1/bPWM1, A12, P2.4
P2[5]	TNOW/bTNOW, PWM2/bPWM2, A13, T2EX_/bT2EX_, CAP2_/bCAP2_, P2.5
P2[6]	RXD1/bRXD1, A14, P2.6
P2[7]	TXD1/bTXD1, DA7/bDA7, A15, P2.7
P3[0]	RXD/bRXD, P3.0
P3[1]	TXD/bTXD, P3.1
P3[2]	LED0/bLED0, INT0/bINT0, P3.2
P3[3]	LED1/bLED1, !A15, INT1/bINT1, P3.3
P3[4]	LEDC/bLEDC, XCS0/bXCS0, T0/bT0, P3.4
P3[5]	DA6/bDA6, T1/bT1, P3.5
P3[6]	WR/bWR, P3.6
P3[7]	RD/bRD, P3.7
P4[0]	LED2/bLED2, A0, RXD1_/bRXD1_, P4.0
P4[1]	A1, P4.1
P4[2]	PWM3_/bPWM3_, CAP3_/bCAP3_, A2, P4.2
P4[3]	PWM1_/bPWM1_, A3, P4.3
P4[4]	LED3/bLED3, TNOW_/bTNOW_, TXD1_/bTXD1_, A4, P4.4
P4[5]	PWM2_/bPWM2_, A5, P4.5
P4[6]	XI, SCS_/bSCS_, P4.6
P4[7]	XO, SCK_/bSCK_, P4.7
P5[0]	DM/bDM, P5.0
P5[1]	DP/bDP, P5.1
P5[4]	HM/bHM, ALE, XB, P5.4
P5[5]	HP/bHP, !A15, XA, P5.5
P5[7]	RST/bRST, P5.7

The left-to-right priority shown in table above is the priority of some modules competing for using GPIO. For example, P2 has been set output bus address high 8 bits but only A8-A10 addresses are used actually, then P2.4/P2.5 can be used as PWM1/PWM2 in higher priority, P2.6 can be used as RXD1, P2.7can be used as TXD1 or DA7 in higher priority, so the waste of P2.4 and P2.7 can be avoided when A12-A15 addresses are unused.

11. External Bus (xBUS)

11.1 External bus register

External bus auxiliary configuration register (XBUS_AUX):

Bit	Name	Access	Description	Reset value
7	bUART0_TX	R0	UART0 Tx state instruction: 1 = it is transmitting.	0
6	bUART0_RX	R0	UART0 Rx state instruction: 1 = it is receiving.	0
5	bSAFE_MOD_ACT	R0	Safe mode state instruction: 1 = it is in safe mode.	0
4	bALE_CLK_EN	RW	Pin ALE clock output enable: 1 = ALE outputs system frequency divided by 12 without XBUS operation, that is Fsys/12. 0 = Clock signal is disabled, it only outputs address low 8 bits latch signal while access to external bus to reduce EMI.	0
3	GF2	RW	General flag bit2: User-defined. Can be reset or set by software.	0
2	bDPTR_AUTO_INC	RW	Enable DPTR add by 1 automatically after MOVX_@DPTR command	0
1	Reserved	RO	Reserved	0
0	DPS	RW	Dual DPTR data pointer select bit: 0 = DPTR0. 1 = DPTR1.	0

External bus speed configuration register (XBUS_SPEED):

Bit	Name	Access	Description	Reset value
7	bXBUS1_SETUP	RW	XBUS1 setup time selection: 0 = 2 clock period. 1 = 3 clock period	1
6	bXBUS1_HOLD	RW	XBUS1 hold time selection: 0 = 1 clock period. 1 = 2 clock period.	1
5	bXBUS1_WIDTH1	RW	XBUS1 bus pulse width high bit	1
4	bXBUS1_WIDTH0	RW	XBUS1 bus pulse width low bit	1
3	bXBUS0_SETUP	RW	XBUS0 setup time selection: 0 = 2 clock period. 1 = 3 clock period.	1
2	bXBUS0_HOLD	RW	XBUS0 hold time selection: 0 = 1 clock period. 1 = 2 clock period.	1
1	bXBUS0_WIDTH1	RW	XBUS0 bus pulse width high bit	1
0	bXBUS0_WIDTH0	RW	XBUS0 bus pulse width low bit	1

bXBUSn_WIDTH1 and bXBUSn_WIDTH0 (n=0, 1), used to select valid pulse width of bus CS n writing and reading:

00 = 2 clock period.
01 = 4 clock period.
10 = 8 clock period.
11 = 16 clock period.

11.2 External bus pins

Table 11.2.1 List of external bus pins

GPIO	Direct address mode pin	Alternate address mode pin	Function description
P3.7	RD	RD	External bus read signal output pin, active low, sampling input while rising edge
P3.6	WR	WR	External bus write signal output pin, active low
P0.0～P0.7	D0～D7	D0～D7	8-bit bidirectional data bus
		A0～A7	Reused as address low 8 bits A[0:7] output, latched by external circuit controlled by ALE.
P4.0～P4.5	A0～A5	unused	Bus direct address A[0:5] output pin, P4_DIR must be set output
P3.5	A6	unused	Bus direct address A6 output pin
P2.7	A7		Bus direct address A7 output pin
		A15	Bus address A15 output pin
P2.0～P2.6	A8～A14	A8～A14	Bus address A[8:14] output pin
P3.4	XCS0	XCS0	CS0 output pin, address ranges from 4000h to 7FFFh, active low.
P3.3	!A15	!A15	Bus address A15 invert output pin, equivalent to CS1 output, address ranges from 8000h to FFFFh, active low, only in ALE disable mode
P5.5	!A15	!A15	Bus address A15 invert output pin, equivalent to CS1 output, address ranges from 8000h to FFFFh, active low, only in ALE enable mode
P5.4		ALE	Address low 8 bits latch control reuse output pin, active high
	ALE		System frequency divided by 12 output pin, duty cycle is 1/12

Some of the pins above that are not used in external bus mode can be used for other modules according to GPIO alternate priority, and pins not used from P4.0 to P4.5 can also be set P4_DIR hold input mode.

When bXBUS_CS_OE=1, bus address A15 invert signal will select output pin according to ALE output mode. !A15 will select P5.5 to output when ALE output is enabled, and select P3.3 to output when ALE output is disabled. ALE output state is decided by bUH1_DISABLE, bXBUS_EN, bXBUS_AL_OE combined with bALE_CLK_EN. Please refer to Table 11.2.2.

Table 11.2.2 P5.4 pin reuse ALE output state table

bUH1_DISABLE	bXBUS_EN	bXBUS_AL_OE	bALE_CLK_EN	P5.4 description
0	X	X	X	Disable ALE output, used as HM in first order(P5.5 used as HP)
1	0	X	0	Disable ALE output ,used as XB

				acquiescently (P5.5 used as XA)
1	0	X	1	ALE only output system clock signal divided by 12
1	1	1	0	Disable ALE output ,used as XB acquiescently (P5.5 used as XA)
1	1	1	1	ALE only output system clock signal divided by 12
1	1	0	0	ALE only output address latch signal low 8 bits
1	1	0	1	ALE outputs address latch signal low 8 bits, outputs system clock signal divided by 12 during idle time

12. Timer

12.1 Timer0/1

Timer0 and Timer1 are 2 16-bit timers and counters, which are configured by registers TCON and TMOD. TCON is used for start-up control, overflow interrupt and external interrupt control of T0 and T1. Each timer is 16-bit consist of two 8-bit units, high byte of timer0 is THO, and low byte is TL0. High byte of timer1 is TH1, and low byte is TL1. Timer1 may also be used for UART0 baud rate generator.

Table 12.1.1 List of Timer0/1 registers

Name	Address	Description	Reset value
TH1	8Dh	High byte of Timer1 count	xxh
TH0	8Ch	High byte of Timer0 count	xxh
TL1	8Bh	Low byte of Timer1 count	xxh
TL0	8Ah	Low byte of Timer0 count	xxh
TMOD	89h	Timer0/1 mode register	00h
TCON	88h	Timer0/1 control register	00h

Timer/counter 0/1 control register (TCON):

Bit	Name	Access	Description	Reset value
7	TF1	RW	Timer1 overflow interrupt flag bit. Automatically cleared after entry of Timer1 interrupt service.	0
6	TR1	RW	Timer1 start/stop bit. Set 1 to start. Set and reset by software.	0
5	TF0	RW	Timer0 overflow interrupt flag bit. Automatically cleared after entry of Timer0 interrupt service.	0
4	TR0	RW	Timer0 start/stop bit. Set 1 to start. Set and reset by software.	0
3	IE1	RW	INT1 interrupt flag. Automatically cleared when MCU enters interrupt routine.	0
2	IT1	RW	INT1 interrupt type: 0 = Low level action. 1 = Falling edge action.	0
1	IE0	RW	INT0 interrupt flag. Automatically cleared when MCU enters	0

			interrupt routine.	
0	IT0	RW	INT0 interrupt type: 0 = Low level action. 1 = Falling edge action.	0

Timer/counter 0/1 mode register (TMOD):

Bit	Name	Access	Description	Reset value
7	bT1_GATE	RW	Gate control timer1: 0 = Whether Timer1 is started is independent of INT1. 1 = Timer1 run enable while P3.3 (INT1) pin is high and TR1 is 1.	0
6	bT1_CT	RW	Counter or timer mode selection for timer1: 0 = Timer, use internal clock. 1 = Counter, use P3.5 (T1) pin falling edge as clock	0
5	bT1_M1	RW	Timer1 mode high bit	0
4	bT1_M0	RW	Timer1 mode low bit	0
3	bT0_GATE	RW	Gate control timer0: 0 = Whether Timer 0 is started is independent of INT0. 1 = Timer0 run enable while P3.2 (INT0) pin is high and TR0 is 1.	0
2	bT0_CT	RW	Counter or timer mode selection for timer0: 0 = Timer, use internal clock, 1 = Counter, use P3.4 (T0) pin falling edge as clock	0
1	bT0_M1	RW	Timer0 mode high bit	0
0	bT0_M0	RW	Timer0 mode low bit	0

Table 12.1.2 List of Timern working mode (n=0, 1)

bTn_M1	bTn_M0	Timern working mode (n=0, 1)
0	0	Mode0: 13-bit timer or counter n by cascaded THn and lower 5 bits of TLn, the upper 3 bits of TLn are ignored. When the counts of all 13 bits change from 1 to 0, set the overflow flag TFn and reset the initial value.
0	1	Mode1: 16-bit timer or counter n by cascaded THn and TLn. When the counts of all 16 bits change from 1 to 0, set the overflow flag TFn and reset the initial value.
1	0	Mode2: 8-bit overload timer/counter n, TLn is used for count unit, and THn is used as the overload count unit. When the counts of all 8 bits change from 1 to 0, set the overflow flag TFn and automatically load the initial value from THn.
1	1	Mode3: For timer0, it is divided into TL0 and TH0. TL0 is used as an 8-bit timer/counter, occupying all control bits of Timer0. TH0 is also used as an 8-bit timer, occupying TR1, TF1 and interrupt resources of Timer1. In this case, Timer1 is still available, but the startup control bit TR1 and overflow flag bit TF1 cannot be used. For timer 1, it stops after it enters mode3.

Timern count low byte (TLn) (n=0, 1):

Bit	Name	Access	Description	Reset value
[7:0]	TLn	RW	Timern count low byte	xxh

Timern count high byte (THn) (n=0, 1):

Bit	Name	Access	Description	Reset value
[7:0]	THn	RW	Timern count high byte	xxh

12.2 Timer2

Timer2 is a 16-bit auto-reload timer and counter, configured by registers T2CON and T2MOD, high byte of Timer2 is TH2, and low is TL2. Timer2 may be used for baud rate generator for UART0, and provide 2 level capture which capture value stored in registers RCAP2 and T2CAP1.

Table 12.2.1 List of Timer2 registers

Name	Address	Description	Reset value
TH2	CDh	Timer2 count high byte	00h
TL2	CCh	Timer2 count low byte	00h
T2COUNT	CCh	16-bit SFR consists of TL2 and TH2	0000h
T2CAP1H	CDh	Timer2 capture 1 data high byte (read only)	xxh
T2CAP1L	CCh	Timer2 capture 1 data low byte (read only)	xxh
T2CAP1	CCh	16-bit SFR consists of T2CAP1L and T2CAP1H	xxxxh
RCAP2H	CBh	High byte of reload & capature value	00h
RCAP2L	CAh	Low byte of reload & capature value	00h
RCAP2	CAh	16-bit SFR consists of RCAP2L and RCAP2H	0000h
T2MOD	C9h	Timer2 mode register	00h
T2CON	C8h	Timer2 control register	00h

Timer/counter2 control register (T2CON):

Bit	Name	Access	Description	Reset value
7	TF2	RW	Timer2 overflow interrupt flag when bT2_CAP1_EN=0. Set it to 1 when the counts of all 16 bits of Timer2 change from 1 to 0. Reset by software. This bit will not be set when either RCLK=1 or TCLK=1.	0
7	CAP1F	RW	Timer2 capture 1 interrupt flag when bT2_CAP1_EN=1, set by T2 edge trigger, reset by software.	0
6	EXF2	RW	Timer2 external trigger flag, set by T2EX edge trigger if EXEN2=1, reset by software.	0
5	RCLK	RW	Select UART0 receiving clock: 0 = Timer1 overflow pulse. 1 = Timer2 overflow pulse.	0
4	TCLK	RW	Select UART0 transmittal clock:	0

			0 = Timer1 overflow pulse. 1 = Timer2 overflow pulse.	
3	EXEN2	RW	Enable T2EX trigger function: 0 = Ignore T2EX. 1 = Enable trigger reload or capture by T2EX edge.	0
2	TR2	RW	Timer2 run enable, 1 = run. Set and reset by software.	0
1	C_T2	RW	Timer2 clock source selection: 0 = Timer base internal clock. 1 = External edge counter base T2 falling edge.	0
0	CP_RL2	RW	Timer2 function selection (force 0 if RCLK = 1 or TCLK = 1): 0 = Timer and auto reload if count overflow or T2EX edge. 1 = Capture by T2EX edge.	0

Timer/counter2 mode register (T2MOD):

Bit	Name	Access	Description		Reset value
7	bTMR_CLK	RW	Fastest internal clock mode for T0/T1/T2 under faster clock mode: 0 = Use divided clock. 1 = Use original Fsys as clock without dividing. This bit has no effect on selecting standard clock timer		0
6	bT2_CLK	RW	Timer2 internal clock frequency selection: 0 = Standard clock, Fsys/12 for timer mode, Fsys/4 for UART0 clock mode. 1 = Faster clock, Fsys/4 @bTMR_CLK = 0 or Fsys @bTMR_CLK = 1 for timer mode, Fsys/2 @bTMR_CLK = 0 or Fsys @bTMR_CLK = 1 for UART0 clock mode		0
5	bT1_CLK	RW	Timer1 internal clock frequency selection: 0 = Standard clock, Fsys/12. 1 = Faster clock, Fsys/4 if bTMR_CLK = 0, or Fsys if bTMR_CLK = 1.		0
4	bT0_CLK	RW	Timer0 internal clock frequency selection: 0 = Standard clock, Fsys/12. 1 = Faster clock, Fsys/4 if bTMR_CLK = 0, or Fsys if bTMR_CLK = 1.		0
3	bT2_CAP_M1	RW	Timer2 capture mode high bit	Timer2 capture point selection: X0: from falling edge to falling edge. 01: from any edge to any edge (level change). 11: from rising edge to rising edge.	0
2	bT2_CAP_M0	RW	Timer2 capture mode low bit		0
1	T2OE	RW	Timer2 clock output enable: 0 = Disable output. 1 = Enable clock output at T2 pin, frequency = TF2/2.		0

0	bT2_CAP1_EN	RW	Enable T2 trigger function for capture 1 of timer2 if RCLK=0, TCLK=0, CP_RL2=1, C_T2=0, T2OE=0: 1 = Enable capture 1 function to capture T2 valid edge. 0 = Disable capture 1.	0

Count reload/capature 2 data register (RCAP2):

Bit	Name	Access	Description	Reset value
[7:0]	RCAP2H	RW	High byte of reload value in timer/counter mode. High byte of timer captured by CAP2 in capture mode.	00h
[7:0]	RCAP2L	RW	Low byte of reload value in timer/counter mode. Low byte of timer captured by CAP2 in capture mode	00h

Timer2 counter (T2COUNT), only valid when bT2_CAP1_EN=0:

Bit	Name	Access	Description	Reset value
[7:0]	TH2	RW	High byte of timer2	00h
[7:0]	TL2	RW	Low byte of timer2	00h

Timer2 capture 1 data (T2CAP1), only valid when bT2_CAP1_EN=1:

Bit	Name	Access	Description	Reset value
[7:0]	T2CAP1H	RO	High byte of timer captured by CAP1	xxh
[7:0]	T2CAP1L	RO	Low byte of timer captured by CAP1	xxh

12.3 Timer3

Table 12.3.1 List of Timer3 registers

Name	Address	Description	Reset value
T3_FIFO_H	AFh	Timer3 FIFO high byte	xxh
T3_FIFO_L	AEh	Timer3 FIFO low byte	xxh
T3_FIFO	AEh	16-bit SFR consists of T3_FIFO_L and T3_FIFO_H	xxxxh
T3_DMA_AH	ADh	DMA address high byte	0xh
T3_DMA_AL	ACh	DMA address low byte	xxh
T3_DMA	ACh	16-bit SFR consists of T3_DMA_AL and T3_DMA_AH	0xxxh
T3_DMA_CN	ABh	DMA remainder word count register	00h
T3_CTRL	AAh	Timer3 control register	02h
T3_STAT	A9h	Timer3 status register	00h
T3_END_H	A7h	Timer3 count end value high byte	xxh
T3_END_L	A6h	Timer3 count end value low byte	xxh
T3_END	A6h	16-bit SFR consists of T3_END_L and T3_END_H	xxxxh
T3_COUNT_H	A5h	Timer3 current count high byte (read only)	00h
T3_COUNT_L	A4h	Timer3 current count low byte (read only)	00h

T3_COUNT	A4h	16-bit SFR consists of T3_COUNT_L and T3_COUNT_H	0000h
T3_CK_SE_H	A5h	Timer3 clock divisor setting high byte	00h
T3_CK_SE_L	A4h	Timer3 clock divisor setting low byte	20h
T3_CK_SE	A4h	16-bit SFR consists of T3_CK_SE_L and T3_CK_SE_H	0020h
T3_SETUP	A3h	Timer3 setup register	04h

Timer3 setup register (T3_SETUP):

Bit	Name	Access	Description	Reset value
7	bT3_IE_END	RW	1 = Enable interrupt for capture mode count timeout (exceed end value) or PWM mode cycle end. 0 = Disable.	0
6	bT3_IE_FIFO_OV	RW	1 = Enable interrupt for FIFO overflow. 0 = Disable.	0
5	bT3_IE_FIFO_REQ	RW	1 = Enable interrupt for capture mode FIFO > = 4 or PWM mode FIFO < = 3. 0 = Disable.	0
4	bT3_IE_ACT	RW	1 = Enable interrupt for capture mode input action or PWM mode trigger. 0 = Disable.	0
3	Reserved	RO	Reserved	0
2	bT3_CAP_IN	RO	Current capture input level after noise filtrating	1
1	bT3_CAP_CLK	RW	1 = Force no minimum pulse width limit for capture input. Only valid when T3_CK_SE = 1. Used for high-speed signal capture.	0
0	bT3_EN_CK_SE	RW	1 = Enable to accessing divisor setting register. 0 = Enable to accessing current count register.	0

Timer3 current count register (T3_COUNT), only valid when bT3_EN_CK_SE=0:

Bit	Name	Access	Description	Reset value
[7:0]	T3_COUNT_H	RO	Timer3 current count high byte	00h
[7:0]	T3_COUNT_L	RO	Timer3 current count low byte	00h

Timer3 clock divisor setting register (T3_CK_SE), valid only when bT3_EN_CK_SE=1:

Bit	Name	Access	Description	Reset value
[7:0]	T3_CK_SE_H	RW	Timer3 clock divisor setting high byte, lower 4 bits valid only, higher 4 bits are fixed to 0.	00h
[7:0]	T3_CK_SE_L	RW	Timer3 clock divisor low byte	20h

Timer3 count end value register (T3_END):

Bit	Name	Access	Description	Reset value
[7:0]	T3_END_H	RW	Timer3 count end value high byte	xxh
[7:0]	T3_END_L	RW	Timer3 count end value low byte	xxh

Timer3 status register (T3_STAT):

Bit	Name	Access	Description	Reset value
7	bT3_IF_DMA_END	RW	Interrupt flag for DMA completion: 1 = There is an interrupt. 0 = No interrupt. Write 1 to clear or write T3_DMA_CN to clear.	0
6	bT3_IF_FIFO_OV	RW	1 = FIFO overflow interrupt. 0 = No interrupt. Write 1 to clear.	0
5	bT3_IF_FIFO_REQ	RW	1 = Interrupt flag for request FIFO data (capture mode FIFO > = 4 or PWM mode FIFO < = 3) 0 = No interrupt. Write 1 to clear.	0
4	bT3_IF_ACT	RW	When bT3_IE_ACT=1: 1 = Interrupt flag for capture mode input action or PWM mode trigger. 0 = No interrupt. Write 1 to clear or access FIFO to clear.	0
4	bT3_IF_END	RW	When bT3_IE_ACT=0: 1 = Interrupt flag for capture mode count timeout (exceed end value) or PWM mode cycle end. 0 = No interrupt. Write 1 to clear.	0
[3:0]	MASK_T3_FIFO_CNT	R0	Timer3 FIFO current count	0000b

Timer3 control register (T3_CTRL):

Bit	Name	Access	Description	Reset value
7	bT3_CAP_M1	RW	Timer3 capture mode high bit; PWM data repeat mode high bit	0
6	bT3_CAP_M0	RW	Timer3 capture mode low bit; PWM data repeat mode high bit	0
5	bT3_PWM_POLAR	RW	Timer3 PWM output polarity: 0 = Default low and active high. 1 = Default high and active low.	0
5	bT3_CAP_WIDTH	RW	Minimum pulse width for timer3 capture: 0 = 4 divided clocks.	0

			1 = 1 divided clock.	
4	bT3_DMA_EN	RW	DMA enable and DMA interrupt enable for timer3: 1 = Enable. 0 = Disable.	0
3	bT3_OUT_EN	RW	Timer3 output enable: 1 = Enable. 0 = Disable.	0
2	bT3_CNT_EN	RW	Timer3 count enable: 1 = Enable. 0 = Disable.	0
1	bT3_CLR_ALL	RW	1 = Force clear FIFO and count of timer3. Reset by software.	1
0	bT3_MOD_CAP	RW	Timer3 mode: 0 = Timer or PWM. 1 = Capture.	0

Note: Timer3 capture point selection in capture mode: bT3_CAP_M1 & bT3_CAP_M0:

00 = Disable capture;

01 = Trigger by any edge, capture from any edge to any edge (level change);

10 = Trigger by falling edge, capture from falling edge to falling edge;

11 = Trigger by rising edge, capture from rising edge to rising edge.

Data repeater times in PWM mode: bT3_CAP_M1 & bT3_CAP_M0:

00 = 1 times;

01 = 4 times;

10 = 8 times;

11 = 16 times.

DMA remainder word count register (T3_DMA_CN):

Bit	Name	Access	Description	Reset value
[7:0]	T3_DMA_CN	RW	DMA remainder word count, support preset initial value, automatic decreasing after DMA.	00h

DMA address register (T3_DMA):

Bit	Name	Access	Description	Reset value
[7:0]	T3_DMA_AH	RW	DMA address high byte, automatic increasing after DMA, low 4 bits valid only, high 4 bits are fixed to 0, support first 4k of xRAM only	0xh
[7:0]	T3_DMA_AL	RW	DMA address low byte, automatic increasing after DMA, high 7 bits valid only, low bit is fixed to 0, support even address only	xxh

FIFO register (T3_FIFO):

Bit	Name	Access	Description	Reset value
[7:0]	T3_FIFO_H	RW	Timer3 FIFO high byte	xxh
[7:0]	T3_FIFO_L	RW	Timer3 FIFO low byte	xxh

12.4 PWM

CH559 Timer3 supports 16-bit PWM and two 8-bit PWM. Support default output setting low-level or high-level, modify duty cycle dynamically, and get the wanted after a simple RC circuit just like a low speed DAC.

PWM3 duty cycle = T3_FIFO / T3_END, from 0% to 100%. If T3_FIFO >T3_END, PWM3 duty cycle = 100%.

PWM1 duty cycle = PWM_DATA / PWM_CYCLE, from 0% to 100%. If PWM_DATA >PWM_CYCLE, PWM1 duty cycle = 100%.

PWM2 duty cycle = PWM_DATA2 / PWM_CYCLE, from 0% to 100%. If PWM_DATA2 >PWM_CYCLE, PWM2 duty cycle = 100%.

Suggestion: enable PWM output and set push-pull in application.

12.4.1 PWM1 and PWM2

Table 12.4.1 PWM1 and PWM2 registers

Name	Address	Description	Reset value
PWM_CYCLE	9Fh	PWM cycle register	xxh
PWM_CK_SE	9Eh	PWM clock divisor setting register	00h
PWM_CTRL	9Dh	PWM control register	02h
PWM_DATA1	9Ch	PWM1 data register	xxh
PWM_DATA2	9Bh	PWM2 data register	xxh

PWM2 data register (PWM_DATA2):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_DATA2	RW	PWM data for PWM2 PWM2 duty cycle = PWM_DATA2 / PWM_CYCLE	xxh

PWM1 data register (PWM_DATA1):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_DATA1	RW	PWM data for PWM1 PWM1 duty cycle = PWM_DATA / PWM_CYCLE	xxh

PWM control register (PWM_CTRL):

Bit	Name	Access	Description	Reset value
7	bPWM_IE_END	RW	1 = enable interrupt for PWM mode cycle end or MFM empty buffer	0
6	bPWM2_POLAR	RW	PWM2 output polarity if bPWM_MOD_MFM = 0: 0 = Default low and active high. 1 = Default high and active low.	0
6	bMFM_BUF_EMPTY	RO	MFM empty buffer status if bPWM_MOD_MFM = 1	0
5	bPWM_POLAR	RW	PWM1 output polarity: 0 = Default low and active high. 1 = Default high and active low.	0
4	bPWM_IF_END	RW	Interrupt flag for cycle end 1 = There is an interrupt for cycle end. Write 1 to clear, or write PWM_CYCLE, or load new data to clear.	0
3	bPWM_OUT_EN	RW	PWM1 output enable: 1 = Enable. 0 = Disable.	0
2	bPWM2_OUT_EN	RW	PWM2 output enable if bPWM_MOD_MFM=0: 1 = Enable. 0 = Disable.	0
2	bMFM_BIT_CNT2	RO	MFM code bit count status if bPWM_MOD_MFM=1: 0 = Lower 4 bits. 1 = Upper 4 bits.	0
1	bPWM_CLR_ALL	RW	1 = Force clear FIFO and count of PWM1/2. Reset by software.	1
0	bPWM_MOD_MFM	RW	MFM encode mode for PWM: 0 = PWM. 1 = MFM encode.	0

PWM clock divisor setting register (PWM_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_CK_SE	RW	PWM clock divisor	00h

PWM cycle register (PWM_CYCLE):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_CYCLE	RW	Set PWM cycle, 00 means 100h.	xxh

12.5 Timer

12.5.1 Timer0/1

(1). Set timer internal clock frequency by T2MOD. Timer0/1 frequency is Fsys/12 when bTn_CLK (n=0/1)

= 0 , Fsys/4 when bTMR_CLK = 0 and Fsys when bTMR_CLK = 1 if bTn_CLK = 1.

(2). Set Timer working mode by TMOD.

Mode0: 13-bit timer/counter

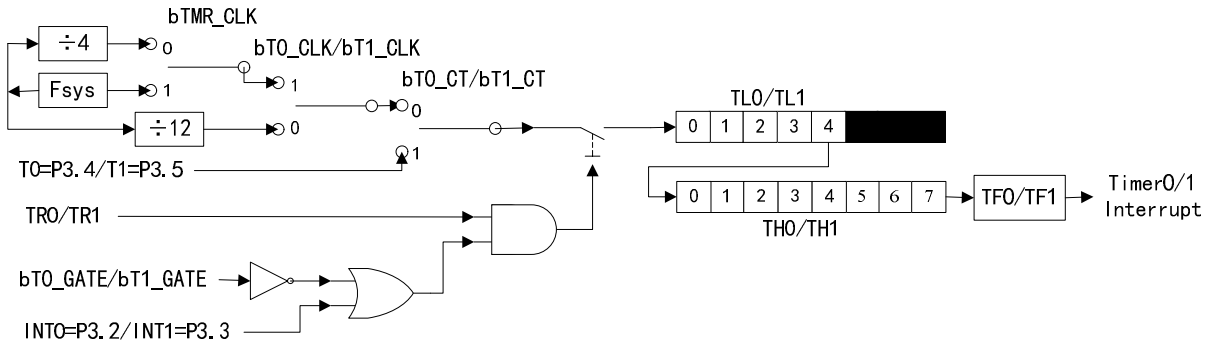


Figure 12.5.1.1 Timer0/1 mode0

Mode1: 16-bit timer/counter

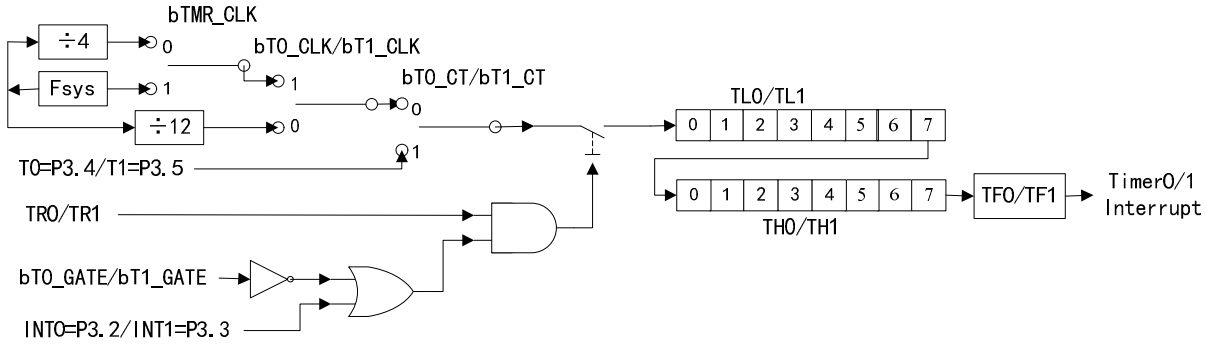


Figure 12.5.1.2 Timer0/1 mode1

Mode2: auto reload 8-bit timer/counter

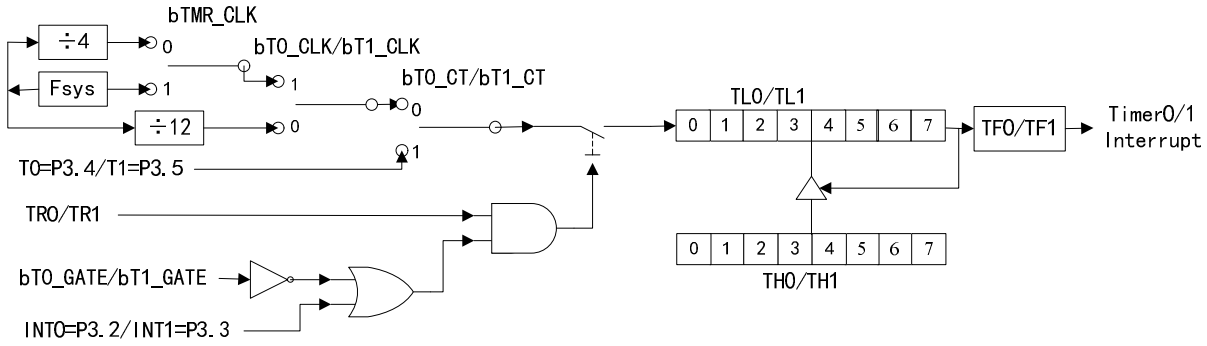


Figure 12.5.1.3 Timer0/1 mode2

Mode3: Timer0 is divided into 2 separate 8-bit timer/counter, and borrowed TR1 of Timer1. Timer1 substitutes the borrowed TR1 control bit by whether starting mode3. Timer1 stops when it gets into mode3.

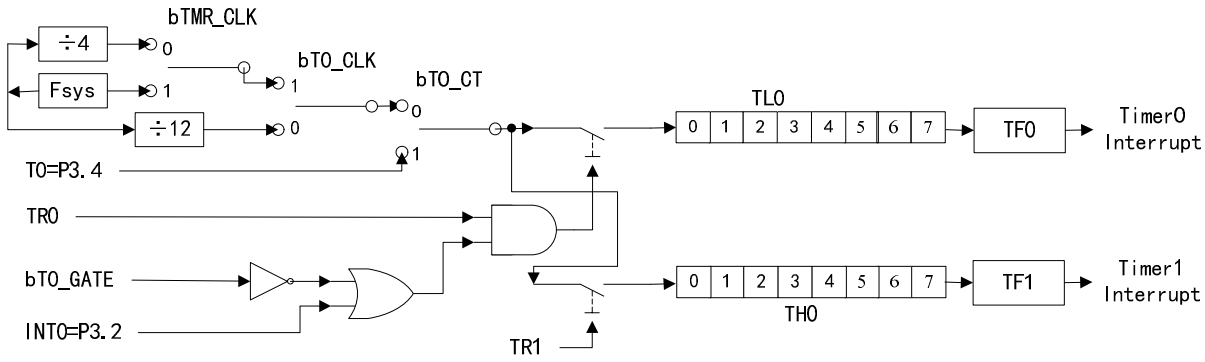


Figure 12.5.1.4 Timer0 mode3

(3). Set timer/counter initial value TLn and THn (n = 0/1).

(4). Set TRn (n = 0/1) in TCON to enable or disable timer/counter, and query status through TFn (n = 0/1).

12.5.2 Timer2

Timer2 16-bit reload timer/counter mode:

(1). Clear RCLK and TCLK in T2CON, select non-baud rate generator mode.

(2). Clear C_T2 in T2CON to use internal clock, jump to step(3); or set it to 1 to use pin T2 falling-edge as count clock, skip step (3).

(3). Set T2MOD to select Timer internal clock. Timer2 frequency is Fsys/12 when bT2_CLK = 0, Fsys/4 when bTMR_CLK = 0 and Fsys when bTMR_CLK = 1 if bT2_CLK = 1.

(4). Clear CP_RL2 in T2CON, to select Timer2 16-bit reload timer /counter function.

(5). Set RCAP2L and RCAP2H as reload value when timer overflow, and TL2 and TH2 initial value (generally the same as RCAP2L and RCAP2H), set TR2 to 1 to enable Timer2.

(6). Query TF2 or Timer2 interrupt to get current timer/counter status.

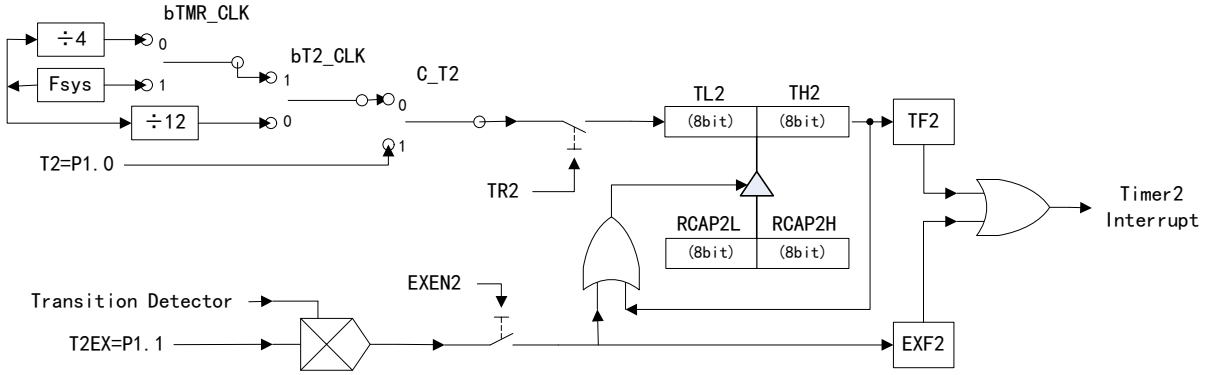


Figure 12.5.2.1 Timer2 16-bit reload timer/counter

Timer2 clock output mode:

Refer to 16-bit reload timer/counter mode, set T2OE in T2MOD to 1 to enable pin T2 output clock of half TF2 frequency.

Timer2 UART0 baud rate generator mode:

(1). Clear C_T2 in T2CON to enable internal clock, or set it to 1 to set T2 falling-edge as clock, select baud rate mode according to RCLK and TCLK in T2CON.

(2). Set T2MOD to select Timer internal clock. Timer2 frequency is Fsys/12 when bT2_CLK = 0, Fsys/4

when bTMR_CLK = 0 and Fsys when bTMR_CLK = 1 if bT2_CLK = 1.

(3). Set RCAP2L and RCAP2H as reload value when timer overflow, set TR2 to 1 to enable Timer2.

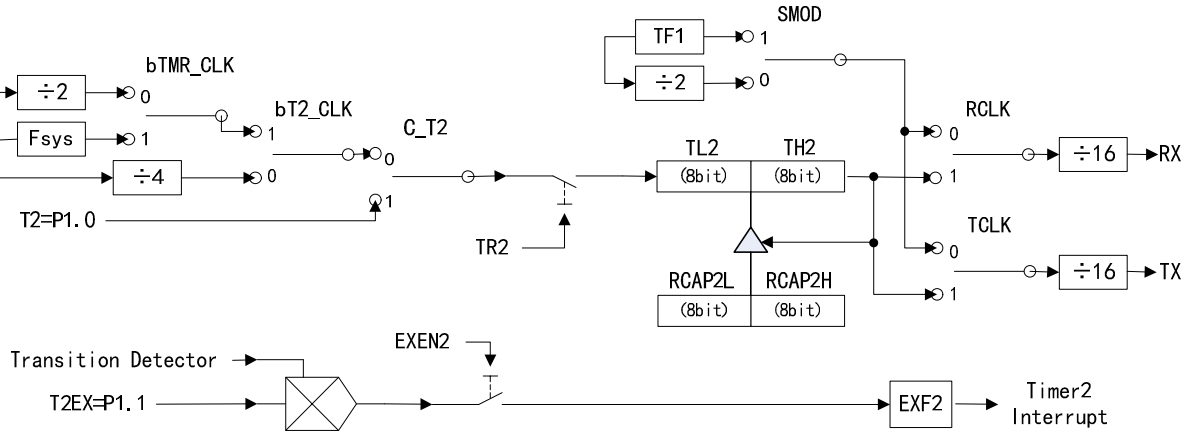


Figure 12.5.2.2 Timer2 UART0 baud rate generator

Timer2 dual-channel capture mode:

(1). Clear RCLK and TCLK in T2CON, to select non-baud rate generator mode.

(2). Clear C_T2 in T2CON to enable internal clock, and jump to step (3); or set it to 1 to set T2 falling-edge as counter clock, and skip step (3).

(3). Set T2MOD to select Timer internal clock. Timer2 frequency is Fsys/12 when bT2_CLK = 0, Fsys/4 when bTMR_CLK = 0 and Fsys when bTMR_CLK = 1 if bT2_CLK = 1.

(4). Set bT2_CAP_M1 and bT2_CAP_M0 in T2MOD to select edge capture mode.

bT2_CAP_M1 & bT2_CAP_M0: timer2 capture point selection:

x0 = from falling edge to falling edge;

01 = from any edge to any edge (level changing);

11 = from rising edge to rising edge.

(5). Set CP_RL2 in T2CON to select pin T2EX capture function of Timer2.

(6). Set TL2 and TH2 timer initial value, set TR2 to 1 to enable Timer2.

(7). RCAP2L and RCAP2H keep TL2 and TH2 value, set EXF2 to 1 and trigger interrupt after capture. The signal width of 2 valid edges is the difference between last time capturing of RCAP2L / RCAP2H and next.

(8). If C_T2 = 0 in T2CON and bT2_CAP1_EN = 1 in T2MOD, that will enable Pin T2 capture function, T2CAP1L and T2CAP1H keep TL2 and TH2 value, set CAP1F to 1 to trigger interrupt after capture.

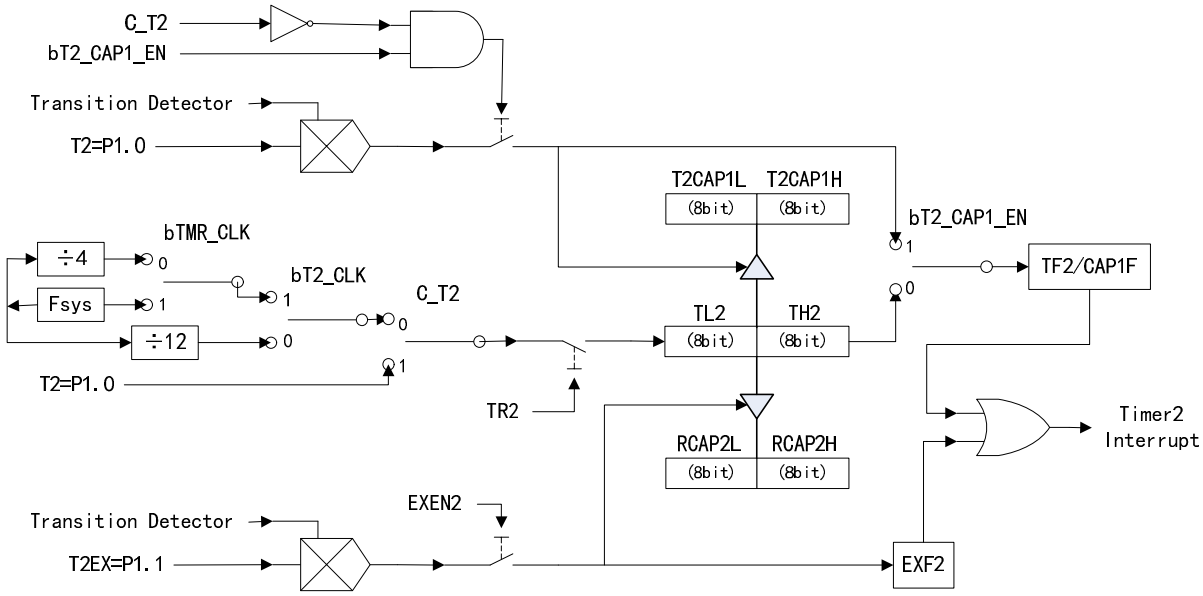


Figure 12.5.2.3 Timer2 capture mode

12.5.3 Timer3

(1). Set bT3_EN_CK_SE in T3_SETUP to 1, enable T3_CK_SE, set frequency divisor, timer3 clock is Fsys/T3_CK_SE, clear bT3_EN_CK_SE after setting.

(2). Set T3_END value or PWM cycles.

(3). Enable T3_SETUP as required.

(4). Set control bit of T3_CTRL, select working mode, clear bT3_CLR_ALL, and set bT3_CNT_EN 1 to enable Timer3.

(5). Configure T3_DMA_AL, T3_DMA_AH, T3_DMA_CN as required, and set bT3_DMA_EN to enable DMA.

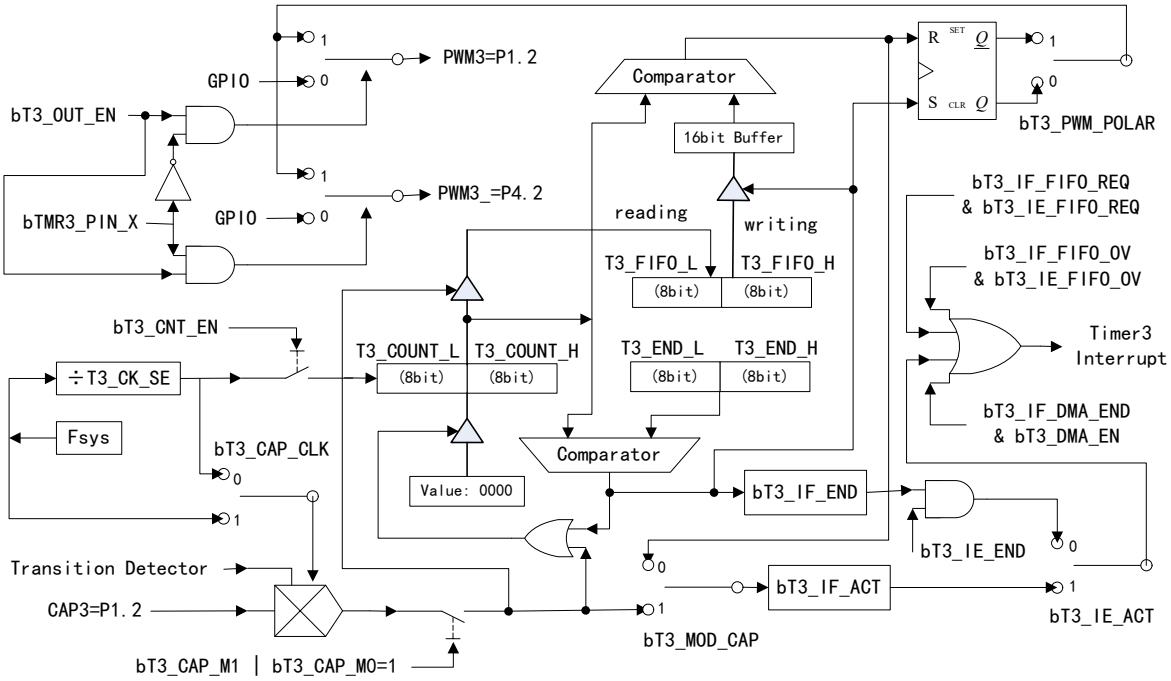


Figure 12.5.3.1 Timer3 16-bit timer/PWM/capture

Timer3 capture data format:
Timer3 may capture the width of two valid edges, and the width is shown with the counter of frequency divided and read through DMA or FIFO after or during capturing. it consists of 16 bits, high-bit is a flag and low 15-bit is width counter. After capture enable, data is generated when a valid edge is detected or timer overflows. The first will be dropped since it is not the width between two valid edges.

(1). bT3_CAP_M1 and bT3_CAP_M0=11
Rising edge valid, capture the width from rising-edge to rising-edge. And the width overflow if the highest bit is 1, that mean not found next rising edge after T3_END, and should be added to next width data which highest bit is 0; if the highest bit is 0, that mean the width of last rising edge. In this mode, recommend to set T3_END to detect special super wide and end signal. And the normal signal does not overflow.

For example, set T3_END to 4000h, the original capture data is below:
1234h, 2345h, 0456h, C000h, C000h, 1035h, 3579h, C000h, 2468h, 0987h
After combination: 1234h, 2345h, 0456h, 9035h, 3579h, 6468h, 0987h

(2). BT3_CAP_M1 and bT3_CAP_M0=10
Same with (1), but falling valid, capture the width from falling-edge to falling-edge.

(3). bT3_CAP_M1 and bT3_CAP_M0=01
Any edge valid, capture the width from any edge to edge. If the high bit is 1, that means the width of high-level, and 0 means the width of low–level. Low 15-bit is width counter. In this mode, set T3_END max value to avoid overflow, but not beyond 15-bit valid data.

13. Universal asynchronous receiver-transmitter (UART)

13.1 UART introduction

The CH559 provides 2 full- duplex UARTs: UART0 and UART1.

UART0 is a standard MCS51 UART, which receives and transmits data with SBUF. Reading for receiving, writing for transmitting.

UART1 is an enhanced UART with following features:
(1). Compatible with 16C550 and enhanced;
(2). Supports 5/6/7/8 data bits and 1/2 stop bits;
(3). Supports odd, even, no parity, space, and mark parity modes;
(4). Programmable baud rate, supports 115200bps and up to 3Mbps;
(5). Built-in receive and transmit buffers and 8-byte FIFO, supports 4 trigger levels;
(6). Supports MODEM: CTS, DSR, RI, DCD, DTR and RTS, can be converted to RS232 level;
(7). Supports hardware flow control signals CTS and RTS auto hand shark and speed control, compatible with TL16C550C;
(8). Supports UART frame error and break detection;
(9). Built-in SIR coding and encoding, supports 2400bps to 115200bps IrDA communication;
(10). Supports full-duplex and half-duplex communication, provides transmitting and receiving indicator for RS485;
(11). Built-in half-duplex transceiver, supports multi-device communication like RS485;
(12). Supports preset local address in slave mode, to match data packet over bus in multi-device

communication.

13.2 UART register

Table 13.2.1 List of UART registers

Name	Address	Description	Reset value
SBUF	99h	UART0 data buffer register	xxh
SCON	98h	UART0 control register	00h
SER1_DLL	9Ah	UART1 baud rate divisor latch LSB	xxh
SER1_RBR	9Ah	UART1 receiver buffer register (read-only)	xxh
SER1_THR	9Ah	UART1 transmitter hold register (write-only)	xxh
SER1_FIFO	9Ah	UART1 FIFO register	xxh
SER1_DIV	97h	UART1 predivisor latch register	xxh
SER1_ADDR	97h	UART1 bus address preset register	FFh
SER1_MSR	96h	UART1 modem status register (read-only)	F0h
SER1_LSR	95h	UART1 line status register (read-only)	60h
SER1_MCR	94h	UART1 modem control register	00h
SER1_LCR	93h	UART1 line control register	00h
SER1_IIR	92h	UART1 interrupt identification register (read-only)	01h
SER1_FCR	92h	UART1 FIFO control register (write-only)	00h
SER1_DLM	91h	UART1 baud rate divisor latch MSB	80h
SER1_IER	91h	UART1 interrupt enable register	00h

13.2.1 UART0 register description

UART0 control register (SCON):

Bit	Name	Access	Description	Reset value
7	SM0	RW	UART0 mode bit0, data bit selection: 0 = 8-bit data. 1 = 9-bit data.	0
6	SM1	RW	UART0 mode bit1, baud rate selection: 0 = Fixed. 1 = Variable, generated by T1 or T2.	0
5	SM2	RW	UART0 multi-device communication enable: When receiving data in mode2 and mode3: 1 = RI is not set to 1 and the reception is invalid if RB8 is 0; RI is set to 1 and the reception is valid if RB8 is 1. 0 = RI is set when receiving and the reception is valid no matter RB8 is 0 or 1. In mode1: 1 = Reception is only valid when receiving valid stop bit. In mode0, SM2 must be set to 0.	0
4	REN	RW	UART0 receive enable: 0 = Disable. 1 = Enable.	0

3	TB8	RW	The 9th transmitted data bit in mode2/3, can be a parity bit. In multi-device communication, it indicates whether the host sends an address byte or a data byte, data byte when TB8=0, and address byte when TB8=1.	0
2	RB8	RW	The 9th bit received data bit in mode2/3. In mode 1, RB8 is used to store the received stop bit if SM2=0. In mode 0, RB8 is not used.	0
1	TI	RW	Transmit interrupt flag, set by hardware after completion of a serial transmittal. Cleared by software.	0
0	RI	RW	Receive interrupt flag, set by hardware after completion of a serial receiving. Cleared by software.	0

Table 13.2.1.1 UART0 working mode

SM0	SM1	Description
0	0	Mode0, shift register, baud rate fixed to: Fsys/12.
0	1	Mode1, 8-bit UART, baud rate = variable by timer1 or timer2 overflow rate.
1	0	Mode2, 9-bit UART, baud rate fixed to: Fsys/128@SMOD=0, Fsys/32@SMOD=1.
1	1	Mode3, 9-bit UART, baud rate = variable by timer1 or timer2 overflow rate.

In mode1 and mode3, UART0 baud rate is generated by T1 when RCLK=0 and TCLK=0. Set T1 in mode2 auto reload 8-bit timer, clear bT1_CT and bT1_GATE, as follow:

Table 13.2.1.2 Calculation formula of UART0 baud rate

bTMR_CLK	bT1_CLK	SMOD	Description
1	1	0	TH1 = 256 - Fsys / 32 / baud rate
1	1	1	TH1 = 256 - Fsys / 16 / baud rate
0	1	0	TH1 = 256 - Fsys / 4 / 32 / baud rate
0	1	1	TH1 = 256 - Fsys / 4 / 16 / baud rate
X	0	0	TH1 = 256 - Fsys / 12 / 32 / baud rate
X	0	1	TH1 = 256 - Fsys / 12 / 16 / baud rate

In mode1 and3, UART0 baud rate is generated by T2 when RCLK=1 and TCLK=1. Set T2 in mode2 auto reload 16-bit timer, clear C_T2 and CP_RL2, as follow:

Table 13.2.1.3 Calculation formula of UART0 baud rate

bTMR_CLK	bT2_CLK	Description
1	1	RCAP2 = 65536 - Fsys / 16 / baud rate
0	1	RCAP2 = 65536 - Fsys / 2 / 16 / baud rate
X	0	RCAP2 = 65536 - Fsys / 4 / 16 / baud rate

UART0 data buffer register (SBUF):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF	RW	UART0 data buffer: reading for receiving, writing for transmittal.	xxh

13.2.2 UART1 register description

SER1_FIFO consists of 2 physical-separated registers: receive buffer SER1_RBR and transmit buffer SER1_THR.

UART1 receiver buffer register (SER1_RBR), valid when bLCR_DLAB=0:

Bit	Name	Access	Description	Reset value
[7:0]	SER1_RBR	RO	UART1 receiver buffer register. Read data from the register when bLSR_DATA_RDY = 1. If bFCR_FIFO_EN = 1, data in shift register will be stored in receiver first and may be read from this register.	xxh

Data transmitter hold register (SER1_THR), valid when bLCR_DLAB=0:

Bit	Name	Access	Description	Reset value
[7:0]	SER1_THR	WO	Transmit hold register, include FIFO. Data written will be stored in FIFO first and send through SER1_THR one by one if bFCR_FIFO_EN = 1.	xxh

UART1 interrupt enable register (SER1_IER), valid when bLCR_DLAB=0:

Bit	Name	Access	Description	Reset value
7	bIER_RESET	RW	UART1 software reset control, high action, auto cleared.	0
6	bIER_EN_MODEM_O	RW	Enable UART1 modem output signal, DTR connect P0.0, RTS connect P0.1	0
5	bIER_PIN_MOD1	RW	UART1 pin mode high bit	0
4	bIER_PIN_MOD0	RW	UART1 pin mode low bit	0
3	bIER_MODEM_CHG	RW	UART1 interrupt enable for modem status change: 1 = Enable. 0 = Disable.	0
2	bIER_LINE_STAT	RW	UART1 interrupt enable for receiver line status: 1 = Enable. 0 = Disable.	0
1	bIER_THR_EMPTY	RW	UART1 interrupt enable for THR empty: 1 = Enable. 0 = Disable.	0
0	bIER_RECV_RDY	RW	UART1 interrupt enable for receiver data ready: 1 = Enable. 0 = Disable.	0

UART1 PIN mode is set by the combination of bIER_PIN_MOD1, bIER_PIN_MOD0, bUH1_DISABLE, bXBUS_CS_OE, bXBUS_AL_OE and bALE_CLK_EN. The last four may combine RS485EN:
RS485EN = bUH1_DISABLE & ~ (bXBUS_CS_OE & ~ bXBUS_AL_OE | bALE_CLK_EN)

RS485EN	bIER_PIN_MOD1	bIER_PIN_MOD0	Mode description
x	0	0	RXD1 connect P4.0, disable TXD1
0	1	0	RXD1/TXD1 connect P2.6/P2.7
0	0	1	RXD1/TXD1 connect P4.0/P4.4
0	1	1	RXD1/TXD1/TNOWconnect P2.6/P2.7/P2.5
1	1	0	RXD1/TXD1 connect iRS485 pins XA/XB
1	0	1	RXD1/TXD1 connect iRS485 pins XA/XB, TNOW connect P4.4
1	1	1	RXD1/TXD1 connect iRS485 pins XA/XB, TNOW connect P2.5

The last 3 configurations in the above table are iRS485 half-duplex communication modes. In this case, RS485EN=1, RXD1/TXD1 connect iRS485 pins XA/XB, and directly support simple long-distance multi-device communication like RS485 bus through built-in half-duplex differential transceiver. In iRS485 half-duplex mode, set as follow:

(1). Set bMCR_HALF in SER1_MCR to 1 to enable half-duplex mode;

(2). Set bUH1_DISABLE in UHUB1_CTRL to 1 to disable HP/HM.

UART1 interrupt identification register (SER1_IIR):

Bit	Name	Access	Description	Reset value
[7:6]	MASK_U1_IIR_ID	R0	Bit mask of UART1 IIR, FIFO enable flag	00b
[5:4]	Reserved	RO	Reserved	00b
[3:0]	MASK_U1_IIR_INT	R0	Bit mask of UART1 interrupt flag	0001b
0	bIIR_NO_INT	RO	1 = No UART1 interrupt. 0 = Interrupt.	1

UART1 interrupt status consists of 4 bits: bIIR_INT_FLAG3, bIIR_INT_FLAG2, bIIR_INT_FLAG1, and bIIR_INT_FLAG0, details as follows:

Name	Value	Type	Source	Clear interrupt
U1_INT_SLV_ADDR	0Eh	UART1 interrupt by slave address match	Receive a data of UART address which match pre-address or broadcast address	Read SER1_IIR or disable multi-device communication
U1_INT_LINE_STAT	06h	UART1 interrupt by receiver line status	bLSR_OVER_ERR, bLSR_PAR_ERR, bLSR_FRAME_ERR, bLSR_BREAK_ERR	Read SER1_LSR
U1_INT_RECV_RDY	04h	UART1 interrupt by receiver data available	Receive number reach FIFO trigger level	Read SER1_RBR
U1_INT_RECV_TOUT	0Ch	UART1 interrupt by	Receive data already and not receive next data over 4-byte	Read SER1_RBR

		receiver FIFO timeout	time	
U1_INT_THR_EMPTY	02h	UART1 interrupt by THR empty	UART1 interrupt by THR empty, bIER_THR_EMPTY changing from 0 to 1 may re-enable this interrupt.	Read SER1_IIR or write SER1_THR
U1_INT_MODEM_CHG	00h	UART1 interrupt by modem status change	△CTS, △DSR, △RI, △DCD	Read SER1_MSR
U1_INT_NO_INTER	01h	No UART interrupt	No interrupt	

FIFO control register (SER1_FCR):

Bit	Name	Access	Description	Reset value
7	bFCR_FIFO_TRIG1	W0	UART1 receiver FIFO trigger level high bit	0
6	bFCR_FIFO_TRIG0	W0	UART1 receiver FIFO trigger level low bit	0
[5:3]	Reserved	RO	Reserved	000b
2	bFCR_T_FIFO_CLR	W0	1 = clear UART1 transmitter FIFO, high action, auto cleared.	0
1	bFCR_R_FIFO_CLR	W0	1 = clear UART1 receiver FIFO, high action, auto cleared	0
0	bFCR_FIFO_EN	W0	1 = UART1 FIFO enable. 0 = disable	0

MASK_U1_FIFO_TRIG consists of bFCR_FIFO_TRIG1 and bFCR_FIFO_TRIG0, which is used to set receive FIFO interrupt and hardware flow control trigger level:
00 = 1 byte,
01 = 2 bytes,
10 = 4 bytes,
11 = 7 bytes.

Line control register (SER1_LCR):

Bit	Name	Access	Description	Reset value
7	bLCR_DLAB	RW	UART1 divisor latch access bit enable. 0 = SER1_RBR,SER1_THR,SER1_IER,SER1_ADR. 1 = SER1_DLL,SER1_DLM,SER1_DIV.	0
6	bLCR_BREAK_EN	RW	UART1 break control enable: 0 = No BREAK output. 1 = For make BREAK output.	0
5	bLCR_PAR_MOD1	RW	UART1 parity mode high bit	0
4	bLCR_PAR_MOD0	RW	UART1 parity mode low bit	0

3	bLCR_PAR_EN	RW	UART1 parity bit enable: 0 = Disable. 1 = Enable.	0
2	bLCR_STOP_BIT	RW	UART1 stop bit length: 0 = 1 bit. 1 = 2 bits.	0
1	bLCR_WORD_SZ1	RW	UART1 word size high bit	0
0	bLCR_WORD_SZ0	RW	UART1 word size low bit	0

The combination of bLCR_PAR_MOD1 and bLCR_PAR_MOD0 is used to set parity mode when bLCR_PAR_EN = 1:
00 = odd parity;
01 = even parity;
10 = mark bit parity;
11 = space parity.

The combination of bLCR_WORD_SZ1 and bLCR_WORD_SZ0 is used to set data length:
00 = 5 bits;
01 = 6 bits;
10 = 7 bits;
11 = 8 bits.

UART1 modem control register (SER1_MCR):

Bit	Name	Access	Description	Reset value
7	bMCR_HALF	RW	1 = Enable UART1 half-duplex mode 0 = Disable	0
6	bMCR_TNOW	RW	UART1 RTS Pin mode selection: 0 = Standard RTS output. 1 = Enable TNOW output on RTS pin.	0
5	bMCR_AUTO_FLOW	RW	UART1 enable auto flow control by CTS & RTS pin: 1 = Enable. 0 = Disable.	0
4	bMCR_LOOP	RW	UART1 enable local loop back for testing: 1 = Enable. 0 = Disable.	0
3	bMCR_OUT2	RW	1 = Enable interrupt request output, 0 = Disable.	0
2	bMCR_OUT1	RW	UART1 control OUT1, not real pin	0
1	bMCR_RTS	RW	UART1 RTS output control: 0 = Invalid (high -level). 1 = Valid (low-level).	0
0	bMCR_DTR	RW	UART1 DTR output control bit: 0 = Invalid (high -level). 1 = Valid (low-level).	0

UART1 line status register (SER1_LSR):

Bit	Name	Access	Description	Reset value
7	bLSR_ERR_R_FIFO	R0	Error in UART1 receiver FIFO, read to clear	0
6	bLSR_T_ALL_EMP	R0	UART1 transmitter all empty status	1
5	bLSR_T_FIFO_EMP	R0	UART1 transmitter FIFO empty status	1
4	bLSR_BREAK_ERR	R0	UART1 receiver break error, read to clear	0
3	bLSR_FRAME_ERR	R0	UART1 receiver frame error, read to clear	0
2	bLSR_PAR_ERR	R0	UART1 receiver parity error, read to clear	0
1	bLSR_OVER_ERR	R0	UART1 receiver overflow error, read to clear	0
0	bLSR_DATA_RDY	R0	UART1 receiver FIFO data ready status, auto cleared	0

UART1 modem status register (SER1_MSR):

Bit	Name	Access	Description	Reset value
7	bMSR_DCD	R0	UART1 DCD action status:1 = Valid (low-level)	1
6	bMSR_RI	R0	UART1 RI action status:1 = Valid (low-level)	1
5	bMSR_DSR	R0	UART1 DSR action status:1 = Valid (low-level)	1
4	bMSR_CTS	R0	UART1 CTS action status: 1 = Valid (low-level)	1
3	bMSR_DCD_CHG	R0	UART1 DCD changed status, high action, read to clear	0
2	bMSR_RI_CHG	R0	UART1 RI changed status, high action, read to clear	0
1	bMSR_DSR_CHG	R0	UART1 DSR changed status, high action, read to clear	0
0	bMSR_CTS_CHG	R0	UART1 CTS changed status, high action, read to clear	0

UART1 slave address preset register (SER1_ADDR), valid when bLCR_DLAB=0:

Bit	Name	Access	Description	Reset value
[7:0]	SER1_ADDR	RW	UART1 bus address preset register	FFh

SER_ADDR preset local address for multi-device communication in slave mode, interrupt when address match or receive broadcast address and allow receiving the following data. Not allow to receive any data before it receives matching address, and stop receiving when start to send or rewrite SER1_ADDR until address match or receive broadcast address.

Bus address auto-compare function is disabled when SER1_ADDR = 0FFH, or bLCR_PAR_EN = 0.

Bus address auto-compare function is enabled when SER1_ADDR != 0FFH and bLCR_PAR_EN = 1, and configure as follow: set bLCR_WORD_SZ1, bLCR_WORD_SZ0 and bLCR_PAR_MOD1 to 1, set bLCR_PAR_MOD0 to 1 when address bit is 0, and clear bLCR_PAR_MOD0 when address bit is 1.

UART1 baud rate divisor latch LSB (SER1_DLM, SER1_DLL), valid when bLCR_DLAB=1:

Bit	Name	Access	Description	Reset value
[7:0]	SER1_DLL	RW	Baud rate divisor consists of SER1_DLL (low byte) and DLM (high byte), and valid when bLCR_DLAB = 1. Baud rate divisor = Fsys * 2 / SER1_DIV / 16 / baud rate	xxh
[7:0]	SER1_DLM	RW		80h

UART1 predivisor latch register (SER1_DIV), valid when bLCR_DLAB=1:

Bit	Name	Access	Description	Reset value
[7:0]	SER1_DIV	RW	Generate internal base clock for baud rate generator after Fsys multiplier and divisor. Valid when bLCR_DLAB = 1	xxh

13.3 UART application

UART0 application:

(1). Select UART0 baud rate generator from T1 or T2 and set counter.

(2). Enable timer.

(3). Set SM0, SM1, SM2 in SCON to select UART0 work mode. Set REN 1 and enable UART0 receiver,

(4). Set UART interrupt or query RI and TI interrupt status.

(5). Write SBUF to send and read SBUF to receive data, and the allowed receive baud rate error should be less than 2%.

UART1 application:

(1). Set bLCR_DLAB in SER1_LCR to 1, set SER1_DIV, count the baud rate divisor and write into SER1_DLM and SER1_DLL.

(2). Set SER_LCR to select data length and parity bit.

(3). Set SER_IER to select interrupt (optional).

(4). Set bMCR_OUT2 in SER1_MCR to enable interrupt output when interrupt enabled, otherwise query the interrupt status

(5). Read or write SER_FIFO to receive or transmit data, and the allowed receive baud rate error should be less than 2%.

14. Synchronous serial interface SPI

14.1 SPI introduction

The CH559 provides 2 SPI interfaces which are used for high-speed synchronous data transmission between peripheral devices.

SPI0 features:

(1). Supports master mode and slave mode;

(2). Supports mode0 and mode3 clock mode;

(3). 3-line full duplex mode or 2-line half-duplex mode is optional;

(4). MSB or LSB is optional to send first;

(5). Clock frequency is variable and can be maximum half of system frequency;

(6). 3-byte receiver FIFO and 1-byte transmitter FIFO inside;

(7). Supports different kinds of interrupts.

SPI1 features:

(1). Supports master mode only, MSB send in first;

(2). Supports clock mode0 and mode3;

(3). 3-line full duplex mode or 2-line half-duplex modes is optional;

(4). Clock frequency is variable and can be maximum half of system frequency.

14.2 SPI register

Table 14.2.1 List of SPI registers

Name	Address	Description	Reset value
SPI0_SETUP	FCh	SPI0 setup register	00h
SPI0_S_PRE	FBh	SPI0 slave mode preset data register	20h
SPI0_CK_SE	FBh	SPI0 clock divisor setting register	20h
SPI0_CTRL	FAh	SPI0 control register	02h
SPI0_DATA	F9h	SPI0 data register	xxh
SPI0_STAT	F8h	SPI0 status register	08h
SPI1_CK_SE	B7h	SPI1 clock divisor setting register	20h
SPI1_CTRL	B6h	SPI1 control register	02h
SPI1_DATA	B5h	SPI1 data register	xxh
SPI1_STAT	B4h	SPI1 status register	08h

14.2.1 SPI0 register description

SPI0 setup register (SPI0_SETUP):

Bit	Name	Access	Description	Reset value
7	bS0_MODE_SLV	RW	SPI0 master/slave mode select: 0 = Master mode. 1 = Slave mode/device mode	0
6	bS0_IE_FIFO_OV	RW	FIFO overflow interrupt enable in slave mode: 1 = FIFO overflow interrupt is enabled. 0 = FIFO overflow will not result in interrupt	0
5	bS0_IE_FIRST	RW	The first receive byte interrupt in slave mode enable: 1 = The first receive byte will trigger interrupt in slave mode. 0 = The first receive byte will not trigger interrupt	0
4	bS0_IE_BYTE	RW	Data byte transfer completion interrupt enable: 1 = Byte transfer completion interrupt is enabled. 0 = Byte transfer completion interrupt will not result in interrupt	0
3	bS0_BIT_ORDER	RW	Data byte bit order control: 0 = MSB in first. 1 = LSB in first.	0
2	Reserved	RO	Reserved	0

1	bS0_SLV_SELT	R0	CS activation status in slave mode: 0 = Not selected at present. 1 = Selected at present.	0
0	bS0_SLV_PRELOAD	R0	Preload data state in slave mode 1 = It is in preload state before data transmission while CS is valid	0

SPI0 clock divisor setting register (SPI0_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_CK_SE	RW	SPI0 clock divisor setting in master mode	20h

SPI0 slave mode preset data register (SPI0_S_PRE)

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_S_PRE	RW	Pre-load the first transfer data in slave mode	20h

SPI0 control register (SPI0_CTRL):

Bit	Name	Access	Description	Reset value
7	bS0_MISO_OE	RW	SPI0 MISO output enable: 1 = Enable output. 0 = Disable output.	0
6	bS0_MOSI_OE	RW	SPI0 MOSI output enable: 1 = Enable output. 0 = Disable output.	0
5	bS0_SCK_OE	RW	SPI0 SCK output enable: 1 = Enable output. 0 = Disable output.	0
4	bS0_DATA_DIR	RW	SPI0 data direction: 0 = Output data, only regard FIFO writing as valid operation, start a SPI transmission 1 = Input data, reading or writing FIFO are all valid, start a SPI transmission	0
3	bS0_MST_CLK	RW	SPI0 master clock mode: 0 = Mode0, default low level when SCK is free. 1 = Mode3, SCK default high level	0
2	bS0_2_WIRE	RW	SPI0 2 line half duplex mode enable: 0 = 3 line full duplex mode, including SCK, MOSI, and MISO. 1 = 2 line half duplex mode, including SCK, MISO	0
1	bS0_CLR_ALL	RW	1 = Clear SPI0 interrupt flag and FIFO. Reset by software.	1
0	bS0_AUTO_IF	RW	Clear byte receiving completion interrupt flag	0

			automatically by FIFO valid operation enable bit: 1 = It will clear byte receiving completion interrupt flag S0_IF_BYTE automatically when there is valid FIFO read/write operation.	

SPI0 data register (SPI0_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_DATA	RW	Consist of physically separated receive FIFO and transmit FIFO. The receive FIFO is used for read operation. The transmit FIFO is used for write operation. SPI transmission can be started by valid read and write operation	xxh

SPI0 status register (SPI0_STAT):

Bit	Name	Access	Description		Reset value
7	S0_FST_ACT	R0	1 = First byte has been received in slave mode		0
6	S0_IF_OV	RW	FIFO overflow flag in slave mode: 1 = FIFO overflow interrupt. 0 = No interrupt Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset. Transmit FIFO empty triggers interrupt when bS0_DATA_DIR = 0. Receive FIFO full triggers interrupt when bS0_DATA_DIR = 1.		0
5	S0_IF_FIRST	RW	The first byte received completion interrupt flag in slave mode: 1 = The first byte has been received. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.		0
4	S0_IF_BYTE	RW	Data byte transfer completion interrupt flag 1 = one byte has been transferred. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset. Valid FIFO operation while bS0_AUTO_IF = 1 can also reset it.		0
3	S0_FREE	R0	SPI0 empty flag: 1 = No SPI shifting at present, usually in idle period between data bytes		1
2	S0_T_FIFO	R0	SPI0 transmit FIFO count, the valid value is 0 or 1		0
1	S0_R_FIFO1	R0	SPI receive FIFO count bit 1	Valid value is 0, 1, 2 or 3	0
0	S0_R_FIFO0	R0	SPI receive FIFO count bit 0		0

14.2.2 SPI1 register description

SPI1 status register (SPI1_STAT)

Bit	Name	Access	Description	Reset value
[7:5]	Reserved	RO	Reserved	000b
4	bS1_IF_BYTE	RW	Data byte transfer completion interrupt flag: 1 = One byte has been transferred,. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset. Valid FIFO operation while bS0_AUTO_IF = 1 can also reset it.	0
3	bS1_FREE	R0	SPI1 empty flag: 1 = No SPI shifting at present, usually in idle period between data bytes	1
[2:0]	Reserved	RO	Reserved	000b

SPI1 data register (SPI1_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	SPI1_DATA	RW	SPI1 data shift register in actual, reading is data receiving, writing is data sending, SPI transmission can be started once by valid read and write operation	xxh

SPI1 control register (SPI1_CTRL):

Bit	Name	Access	Description	Reset value
7	bS1_MISO_OE	RW	SPI1 MISO output enable: 1 = Enable output. 0 = Disable output.	0
6	Reserved	RO	Reserved	0
5	bS1_SCK_OE	RW	SPI1 SCK output enable: 1 = Enable SCK1 output, MOSI1 output can also be enabled in the meantime if bS1_2_WIRE = 0. 0 = Disable output	0
4	bS1_DATA_DIR	RW	SPI1 data direction control: 0 = Otput data, only regard writing SPI1_DATA as valid operation, start SPI transmission once. 1 = Iput data, writing or reading SPI1_DATA are all valid operation and can trigger SPI1 transmission once	0
3	bS1_MST_CLK	RW	SPI1 clock mode control: 0 = Mde0, default low level when SCK1 is free. 1 = Mde3,default high level when SCK1 is free	0
2	bS1_2_WIRE	RW	SPI1 2 line half duplex mode enable bit: 0 = 3 line full duplex mode, including SCK1, MOSI1, and MISO1. 1 = 2 line half duplex mode, including SCK1, MISO1.	0
1	bS1_CLR_ALL	RW	1 = Cear SPI1 interrupt flag and FIFO.	1

			Reset by software.	
0	bS1_AUTO_IF	RW	Clear byte receiving completion interrupt flag automatically by SPI1_DATA valid operation enable bit: 1 = I will clear byte receiving completion interrupt flag bS1_AUTO_IF automatically when there is valid SPI1_DATA read/write operation	0

SPI1 clock divisor setting register (SPI1_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	SPI1_CK_SE	RW	SPI1 clock divisor setting	20h

14.3 SPI transfer format

SPI host mode support 2 transfer formats, including mode0 and mode3 ,which can be selected by setting bSn_MST_CLK in SPIn_CTRL. CH559 always samples MISO data during CLK rising edge. The data transfer formats are shown below:

Mode0: bSn_MST_CLK = 0

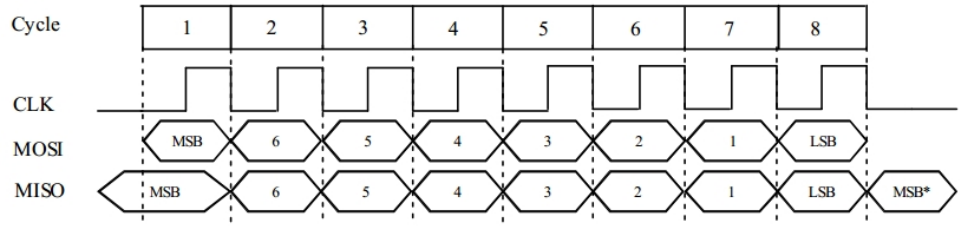


Figure 14.3.1 SPI mode0 timing diagram

Mode3: bSn_MST_CLK = 1

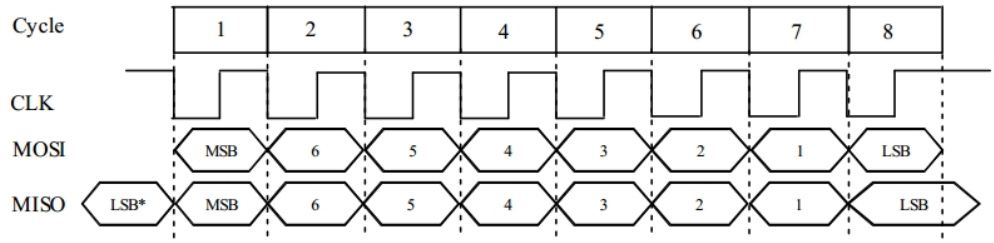


Figure 14.3.2 SPI mode3 timing diagram

14.4 SPI configuration

14.4.1 SPI host mode configuration

SCK pin outputs serial clock, CS output pin can be assigned as any I/O pin in SPI host mode.

SPI0 configuration steps:

(1). Configure SPI clock frequency by setting SPI clock divisor setting register SPI0_CK_SE.

(2). Configure SPI host mode by setting bS0_MODE_SLV in SPI setup register SPI0_SETUP0.

(3). Set bS0_MST_CLK in SPI control register SPI0_CTRL, configuration as mode0 or mode3 according

to the demand

(4). Set bS0_SCK_OE and bS0_MOSI_OE in SPI control register SPI0_CTRL as 1 , bS0_MISO_OE as 0, set P1 direction bSCK and bMOSI as output, bMISO as input ,and CS pin as output.

Data transmission:

(1). Write SPI0_DATA register, write data ready for sending to FIFO and start SPI transmission once automatically.

(2). Wait for S0_FREE until it is 1, indicating that data transmission is over, and can continue to send next byte.

Data reception:

(1). Write SPI0_DATA register, start SPI transmission once by writing any data such as 0FFh to FIFO.

(2). Wait for S0_FREE until it is 1, indicating that data reception is over, and can get data by reading SPI0_DATA

(3). The operation above can also start SPI transmission once while bS0_DATA_DIR has been 1, otherwise no SPI transmission starts.

14.4.2 SPI slave mode configuration

Only SPI0 supports slave mode. In the slave configuration, the serial clock is received on the SCK pin from the master device.

(1). Set the bS0_MODE_SLV bit in the SPI0_SETUP register for slave mode.

(2). Clear the bS0_SCK_OE bit and bS0_MOSI_OE bit (both in the SPI0_CTRL register), and set bS0_MISO_OE bit, and configure bSCK pin, bMOSI pin, bMISO pin and CS pin direction for input. It will enable MISO pin output automatically if CS pin is effective (low level). In addition, it is recommended to set MISO pin high-impedance input mode (bP1_OC=0, P1_DIR[6]=0, P1_PU[6]=0), so that the MISO does not output when CS pin is not effective (high level), which is conducive to sharing the SPI bus.

(3). Optionally, configure SPI0_S_PRE register for the first data output after the CS pin is effective. After the 8 serial clocks, that is the first data byte exchanged, the CH559 slave device gets the first byte from SPI host, and the external SPI host gets the data byte in the SPI0_S_PRE register. The bit 7 in the SPI0_S_PRE register will be sent to the MISO pin during SCK is low after the CS pin is effective. In SPI mode 0, if set the bit 7 in the SPI0_S_PRE register, the external SPI host will get the state of bit 7 in the SPI0_S_PRE register by reading MISO pin when the CS pin is effective but not transmitted data.

Data transmission:

(1) Wait for S0_IF_BYTE bit setting or interrupt for a byte data exchanged event.

(2) Write the SPI0_DATA register for sending data to the FIFO.

(3) Or wait the S0_FREE bit changed from 0 to 1, continue to send next byte.

Data reception:

(1) Wait for S0_IF_BYTE bit setting or interrupt for a byte data exchanged event.

(2) Read the SPI0_DATA register for receiving data from the FIFO.

(3) Query MASK_S0_RFIFO_CNT register (that consists of S0_R_FIFO1 bit and S0_R_FIFO0 bit) to obtain the number of bytes remaining in FIFO.

15. Analog to Digital Converter (ADC)

15.1 ADC introduction

The optional 10-bit or 11-bit ADC of the CH559 MCU is a successive approximation analog-to-digital converter. It has up to 8 multiplexed for time-sharing sampling.

ADC main features:

(1). Optional 10-bit or 11-bit resolution.

(2). ADC input range: 0≤VIN≤VDD33.

(3). Sampling rate up to 1MSPS.

(4). Scan mode for automatic conversion of two channels.

(5). Built-in 2-level FIFO, support automatic sampling and DMA.

15.2 ADC register

Table 15.2.1 List of ADC registers

Name	Address	Description	Reset value
ADC_EX_SW	F7h	ADC extend switch control register	00h
ADC_SETUP	F6h	ADC setup register	08h
ADC_FIFO_H	F5h	ADC FIFO high byte (read-only)	0xh
ADC_FIFO_L	F4h	ADC FIFO low byte (read-only)	xxh
ADC_FIFO	F4h	ADC FIFO word (Read-only), little-endian	0xxxh
ADC_CHANN	F3h	ADC channel selection register	00h
ADC_CTRL	F2h	ADC control register	00h
ADC_STAT	F1h	ADC status register	04h
ADC_CK_SE	EFh	ADC clock divisor setting register	10h
ADC_DMA_CN	EEh	DMA remainder word count register	00h
ADC_DMA_AH	EDh	DMA address high byte	0xh
ADC_DMA_AL	ECh	DMA address low byte	xxh
ADC_DMA	ECh	DMA address word, must even address, little-endian	0xxxh

DMA address word (ADC_DMA):

Bit	Name	Access	Description	Reset value
[7:0]	ADC_DMA_AH	RW	High byte of DMA 16-bit address. This byte is the initial value of the high byte of the DMA 16-bit address and then the DMA address is increased automatically. Only the low 4 bits are valid, and high 4 bits is always 0. Only supports the previous 4K of xRAM	0xh
[7:0]	ADC_DMA_AL	RW	Low byte of DMA address. This byte is the initial value of the low byte of the DMA 16-bit address and then the DMA address is increased automatically. Only the high 7 bits are valid, and the low bit is always 0.	xxh

			Only supports the even address	

DMA remainder word count register (ADC_DMA_CN):

Bit	Name	Access	Description	Reset value
[7:0]	ADC_DMA_CN	RW	DMA remainder word count. This byte is the initial value of the DMA remainder count and then the DMA remainder count is decreased automatically.	00h

ADC clock divisor setting register (ADC_CK_SE):

Bit	Name	Access	Description	Reset value
7	bADC_CHK_CLK_SEL	RW	AIN7 level check delay clock frequency selection bit: 0 = Sow (1xfsys) 1 = Fst (4xfsys)	0
[6:0]	MASK_ADC_CK_SE	RW	ADC clock divisor for ADC working clock	10h

ADC status register (ADC_STAT):

Bit	Name	Access	Description	Reset value
7	bADC_IF_DMA_END	RW	DMA complete flag. This bit is set to 1 via hardware while DMA complete. This bit must be cleared via software. Write 1 to clear or write ADC_DMA_CN to clear.	0
6	bADC_IF_FIFO_OV	RW	FIFO overflow flag. This bit is set when FIFO overflows. Software can write 1 to clear.	0
5	bADC_IF_AIN7_LOW	RW	AIN7 low level flag. This bit is set when checking AIN7 low level. Write 1 to clear by software.	0
4	bADC_IF_ACT	RW	ADC finished flag. This bit is set when an ADC conversion complete. Software can write 1 to clear.	0
3	bADC_AIN7_INT	R0	1 = Crrent AIN7 low level delay status	0
2	bADC_CHANN_ID	R0	Current channel ID in channel automatic switch mode: 0 = AIN0 or AIN6. 1 = AIN1 or AIN4 or AIN7.	0
2	bADC_DATA_OK	RO	ADC end and data ready flag in channel manual selection mode: 0 = Dta not ready. 1 = Dta ready.	1

[1:0]	MASK_ADC_FIFO_CNT	R0	Current ADC FIFO count.	00b

The size of MASK_ADC_FIFO_CNT is 2 bits, indicating the current count of ADC FIFO.

MASK_ADC_FIFO_CNT	Description
00b	Epty FIFO, return current ADC result if reading FIFO
01b	1 result in FIFO
10b	2 results in FIFO, and FIFO full
11b	Unknown error

ADC control register (ADC_CTRL):

Bit	Name	Access	Description	Reset value
7	bADC_SAMPLE	RW	In manual sample mode, this bit is for sampling pulse control. High level pulse action. In automatic sample mode, this bit is sample pulse state.	0
6	bADC_SAMP_WIDTH	RW	In automatic sample mode, sample pulse width: 0 = 1 ADC clock. 1 = 2 ADC clocks.	0
5	bADC_CHANN_MOD1	RW	ADC channel control mode high bit.	0
4	bADC_CHANN_MOD0	RW	ADC channel control mode low bit.	0
[3:0]	MASK_ADC_CYCLE	RW	ADC automatic sample cycle: 0 = Mnual sample. Others = set cycle number for automatic sample	0000b

MASK_ADC_CHANN consists of bADC_CHANN_MOD1 and bit bADC_CHANN_MOD0, indicating the current channel control mode.

MASK_ADC_CHANN	Description
00b	Cannel manual selection mode by SFR ADC_CHANN
01b	Atomatic switch mode between AIN0 and AIN1
10b	Atomatic switch mode between AIN6 and AIN4
11b	Atomatic switch mode between AIN6 and AIN7

ADC channel selection register (ADC_CHANN):

Bit	Name	Access	Description	Reset value
[7:0]	ADC_CHANN	RW	ADC channel selection: Set ADC current sample channel, bit0 to bit7 correspond to channels AIN0 to AIN7. Cannot select multiple bits simultaneously.	00h

ADC FIFO register (ADC_FIFO):

Bit	Name	Access	Description	Reset value
[7:0]	ADC_FIFO_H	RO	High byte of 16-bit ADC FIFO. Only the low 4 bits are valid, and high 4 bits are always 0.	0xh
[7:0]	ADC_FIFO_L	RO	Low byte of 16-bit ADC FIFO.	xxh

ADC setup register (ADC_SETUP):

Bit	Name	Access	Description	Reset value
7	bADC_DMA_EN	RW	DMA and DMA interrupt enable for ADC: 0 = Disable DMA and DMA interrupt. 1 = Enable DMA and DMA interrupt.	0
6	bADC_IE_FIFO_OV	RW	0 = Disable FIFO overflow interrupt. 1 = Enable FIFO overflow interrupt.	0
5	bADC_IE_AIN7_LOW	RW	0 = Disable interrupt for AIN7 low level checking. 1 = Enable interrupt for AIN7 low level checking.	0
4	bADC_IE_ACT	RW	0 = Disable interrupt for a ADC finished. 1 = Enable interrupt for a ADC finished.	0
3	bADC_CLOCK	RO	Current level of internal ADC clock	0
2	bADC_POWER_EN	RW	ADC power control: 0 = Shut down ADC power. 1 = Enable power for ADC	0
1	bADC_EXT_SW_EN	RW	Extend switch module power control: 0 = Shut down. 1 = Enable power for extend switch.	0
0	bADC_AIN7_CHK_EN	RW	AIN7 level check module power control: 0 = Shut down. 1 = Enable power for AIN7 level check.	0

ADC extend switch control register (ADC_EX_SW):

Bit	Name	Access	Description	Reset value
7	bADC_SW_AIN7_H	RW	Internal AIN7 extend switch control: 0 = Float AIN7. 1 = Tie AIN7 to high level VDD33.	0
6	bADC_SW_AIN6_L	RW	Internal AIN6 extend switch control: 0 = Float AIN6. 1 = Tie AIN6 to low level GND.	0
5	bADC_SW_AIN5_H	RW	Internal AIN5 extend switch control: 0 = Float AIN5 1 = Tie AIN5 to high level VDD33.	0

4	bADC_SW_AIN4_L	RW	Internal AIN4 extend switch control: 0 = Float AIN4. 1 = Tie AIN4 to low level GND.	0
3	bADC_EXT_SW_SEL	RW	Extend switch resistor selection: 0 = High resistor, about 800Ω. 1 = Low resistor, about 300Ω.	0
2	bADC_RESOLUTION	RW	ADC resolution: 0 = 10 bits. 1 = 11 bits.	0
1	bADC_AIN7_DLY1	RW	AIN7 level check delay control bit 1	0
0	bADC_AIN7_DLY0	RW	AIN7 level check delay control bit 0	0

MASK_ADC_AIN7_DLY consists of bADC_AIN7_DLY1 and bADC_AIN7_DLY0, for setting the delay time after detection AIN7 level change:

00 = No delay time

01 = Maximum delay time

10 = Long delay time

11 = Short delay time.

15.3 ADC functional description

ADC configuration steps:

(1) Setting the bADC_POWER_EN bit in the ADC_SETUP register, enable ADC module.

(2) Setting ADC_CK_SE register for ADC clock frequency (fADC≤12 MHz), recommend no less than 1MHz.

(3) Clear FIFO by reading ADC_FIFO register. If interrupt or DMA function needed, enable them according to the above register description.

(4) Sampling:

In automatic conversion mode:

Configure the MASK_ADC_CYCLE in ADC_CTRL register for sampling cycles in automatic conversion mode. Select input channel by settingADC_CHANN register.

In manual conversion mode:

Configure the MASK_ADC_CYCLE in ADC_CTRL register for manual conversion mode. Select input channel by setting ADC_CHANN register. To start a sampling pulse which is a high level pulse. Set the bADC_SAMPLE bit in the ADC_CTRL register and then continue for at least 1 ADC clock cycles and then clear to 0. Each ADC conversion needs a manual sampling pulse.

(5) Waiting for bADC_IF_ACT bit in the ADC_STAT register equal to 1 which means that the end of ADC conversion, read the ADC_FIFO register for the conversion data.

(6) Another way, read ADC_FIFO several times according to the value of MASK_ADC_FIFO_CNT in the ADC_STAT register. It is advisable to discard the first conversion data in FIFO.

(7) If use DMA, set buffer start address by writing ADC_DMA first. Second, set DMA remainder word count by writing ADC_DMA_CN, and finally set bADC_DMA_EN bit in the ADC_SETUP register for enabling DAM.

(8) There are 12 valid bits in the ADC FIFO. bit0~bit10 are conversion value and bit11 is flag which is always 0 in manual channel selection mode and is a marker equivalent to bADC_CHANN_ID bit in auto channel selection mode.

16. Universal serial bus interface (USB)

16.1 USB introduction

The CH559 is built-in USB controller and dual USB transceiver. USB main features:

(1). USB host and USB device

(2). Compatible with USB specification version 2.0 full-speed (12Mbps) or low-speed (1.5Mbps)

(3). Support control transfers, Bulk transfers, Interrupt, Isochronous transfers

(4). Dual port Root-HUB for USB host

(5). Support up to 64 bytes of USB data packets, built-in FIFO, and interrupt and DMA

There are 3 parts for USB registers, and some registers are multiplexed in host and device mode.

(1). USB global registers.

(2). USB device control registers.

(3). USB host control registers.

16.2 Global registers

Table 16.2.1 List of USB global registers

Name	Address	Description	Reset value
USB_RX_LEN	D1h	USB receiving data length (Read-only)	0xxx xxxxb
USB_INT_FG	D8h	USB interrupt flag	0010 0000b
USB_INT_ST	D9h	USB interrupt status (read only)	00xx xxxxb
USB_MIS_ST	DAh	USB miscellaneous status (read only)	xx10 1000b
USB_INT_EN	E1h	USB interrupt enable	0000 0000b
USB_CTRL	E2h	USB base control	0000 0110b
USB_DEV_AD	E3h	USB device address	0000 0000b
USB_DMA_AH	E7h	Low byte of 16-bit DMA address (read-only)	000x xxxxb
USB_DMA_AL	E6h	High byte of 16-bit DMA address (read-only)	xxxx xxx0b
USB_DMA	E6h	16-bit DMA address (consists of USB_DMA_AL and USB_DMA_AH)	xxxxh

USB receiving data length (USB_RX_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	bUSB_RX_LEN	RO	The number of bytes received by the current USB endpoint	xxh

USB interrupt flag (USB_INT_FG):

Bit	Name	Access	Description	Reset value
7	U_IS_NAK	RO	In USB device mode, (Read-only): 1 = Current the host receives the USB response is NAK. 0 = Current the host receives the USB response is not NAK.	0
6	U_TOG_OK	RO	Current USB transmit data toggle flag status: 1 = Current USB DATA0/1 toggle is OK.	0

			0 = Current USB DATA0/1 toggle is not OK.	
5	U_SIE_FREE	RO	USB SIE free status: 1 = SIE is free. 0 = SIE is busy, USB transfer	1
4	UIF_FIFO_OV	RW	FIFO overflow interrupt flag: 1 = FIFO is overflow. 0 = No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
3	UIF_HST_SOF	RW	In USB host mode, SOF timer interrupt flag: 1 = SOF packet transfer completes. 0 = No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
2	UIF_SUSPEND	RW	USB suspend or resume event interrupt flag: 1 = Suspend or resume event. 0 = No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
1	UIF_TRANSFER	RW	USB transfer complete interrupt flag: 1 = USB transfer complete. 0 = No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
0	UIF_DETECT	RW	In USB host mode, checking device connect or disconnect: 1 = Device connection or disconnection event. 0 = No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
0	UIF_BUS_RST	RW	In USB device mode, USB bus reset flag: 1 = USB bus reset event. 0 = No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0

USB interrupt status (USB_INT_ST):

Bit	Name	Access	Description	Reset value
7	bUIS_IS_NAK	RO	In USB device mode: 1 = Current received the USB response is NAK, (be equal to U_IS_NAK).	0
6	bUIS_TOG_OK	RO	USB transfer toggle state, (be equal to U_TOG_OK): 1 = Current USB DATA0/1 toggle is OK. 0 = Current USB DATA0/1 toggle is not OK.	0

5	bUIS_TOKEN1	RO	In USB device mode, current token PID code bit 1.	x
4	bUIS_TOKEN0	R0	In USB device mode, current token PID code bit 0.	x
[3:0]	MASK_UIS_ENDP	RO	In USB device mode, current endpoint number of a transaction. 0000 = Endpoint 0. …, 1111 = Endpoint 15.	xxxxb
[3:0]	MASK_UIS_H_RES	RO	In USB host mode, current token PID code. 0000 = No response or timeout. Others = Respond PID.	xxxxb

MASK_UIS_TOKEN consists of bUIS_TOKEN1 bit and bUIS_TOKEN0 bit which is used to indicate the current host transmission PID to USB device:

00 = OUT Packet

01 = SOF Packet

10 = IN Packet

11 = SETUP Packet.

USB miscellaneous status (USB_MIS_ST):

Bit	Name	Access	Description	Reset value
7	bUMS_SOF_PRES	RO	SOF timer presage status in host mode: 1 = SOF packet will be sent. 0 = No SOF packet will be sent.	x
6	bUMS_SOF_ACT	RO	SOF timer action status in host mode: 1 = Sending SOF packet. 0 = Free.	x
5	bUMS_SIE_FREE	RO	USB SIE free status, (be equal to U_SIE_FREE): 1 = SIE is free. 0 = SIE is busy, USB transfer	1
4	bUMS_R_FIFO_RDY	RO	USB receiving FIFO ready status : 1 = Receiving FIFO is not empty. 0 = Receiving FIFO is empty.	0
3	bUMS_BUS_RESET	RO	USB bus reset status: 1 = Bus reset. 0 = Bus not reset.	1
2	bUMS_SUSPEND	RO	USB suspend status : 1 = Bus suspend. 0 = Bus not suspend.	0
1	bUMS_H1_ATTACH	RO	In host mode, device attached status on USB hub1 HP/HM: 1 = There is USB device being connected to Hub1. 0 = No device connecting.	0
0	bUMS_H0_ATTACH	RO	In host mode, device attached status USB hub0 DP/DM:	0

			1 = There is USB device being connected to Hub0. 0 = No device connecting.	

USB interrupt enable (USB_INT_EN):

Bit	Name	Access	Description	Reset value
7	bUIE_DEV_SOF	RW	1 = Enable interrupt for SOF received for USB device mode. 0 = Disable interrupt.	0
6	bUIE_DEV_NAK	RW	1 = Enable interrupt for NAK responded for USB device mode. 0 = Disable interrupt.	0
5	Reserved	RO	Reserved	0
4	bUIE_FIFO_OV	RW	1 = Enable interrupt for FIFO overflow. 0 = Disable interrupt.	0
3	bUIE_HST_SOF	RW	1 = Enable interrupt for host SOF timer action for USB host mode. 0 = Disable interrupt.	0
2	bUIE_SUSPEND	RW	1 = Enable interrupt for USB suspend or resume event. 0 = Disable interrupt.	0
1	bUIE_TRANSFER	RW	1 = Enable interrupt for USB transfer completion. 0 = Disable interrupt.	0
0	bUIE_DETECT	RW	1 = Enable interrupt for USB device detected event for USB host mode; 0 = Disable interrupt.	
0	bUIE_BUS_RST	RW	1 = Enable interrupt for USB bus reset event for USB device mode; 0 = Disable interrupt.	0

USB base control (USB_CTRL)

Bit	Name	Access	Description	Reset value
7	bUC_HOST_MODE	RO	USB mode selection: 1 = Host mode. 0 = Device mode.	0
6	bUC_LOW_SPEED	RW	USB bus speed selection: 1 = Low speed (1.5Mbps). 0 = Full speed (12Mbps).	0
5	bUC_DEV_PU_EN	RW	In USB device mode: 1 = Enable USB device function and enable internal pull-up resistor. 0 = Disable USB device function.	0
5	bUC_SYS_CTRL1	RW	USB system control high bit	0
4	bUC_SYS_CTRL0	RW	USB system control low bit	0
3	bUC_INT_BUSY	RW	1 = Automatic responding busy (NAK) for device mode or automatic pause for host mode during interrupt flag	0

			UIF_TRANSFER valid. 0 = No pause.	
2	bUC_RESET_SIE	RW	1 = Force reset USB SIE. Reset by software.	1
1	bUC_CLR_ALL	RW	Force clear FIFO and count of USB. Reset by software.	1
0	bUC_DMA_EN	RW	1 = DMA enable and DMA interrupt enable for USB 0 = Disable DMA.	0

USB system control consists of bUC_HOST_MODE, bUC_SYS_CTRL1 and bUC_SYS_CTRL0.

bUC_HOST_MODE	bUC_SYS_CTRL1	bUC_SYS_CTRL0	USB system control description
0	0	0	Disable USB device function and disable internal pull-up resistor
0	0	1	Enable USB device and disable internal pull-up resistor, need external pull-up resistor
0	1	0	Enable USB device and enable internal pull-up resistor
0	1	1	Enable USB device and enable internal weak pull-up resistor
1	0	0	Enable USB host and normal status
1	0	1	Enable USB host and force DP/DM output SE0 state
1	1	0	Enable USB host and force DP/DM output J state
1	1	1	Enable USB host and force DP/DM output resume or K state

USB device address (USB_DEV_AD):

Bit	Name	Access	Description	Reset value
7	bUDA_GP_BIT	RW	General purpose bit. User-defined. Can be set and reset by software.	0
[6:0]	MASK_USB_ADDR	RW	In host mode, this address is the operated device address. In device mode, it is the address of device.	00h

16-bit DMA address (USB_DMA):

Bit	Name	Access	Description	Reset value
[7:0]	USB_DMA_AH	RO	High byte of 16-bit DMA address. the low 5 bits are effective and the high 3 bits are always 0.	xxh
[7:0]	USB_DMA_AL	R0	Low byte of 16-bit DMA address.	xxh

16.3 USB device control registers

CH559 can configure number of bidirectional endpoints from 0 to 4 and the maximum data packet size for all endpoints is 64 bytes.

Endpoint0 is for default control pipe as a message pipe and control transfers are carried only through message pipe. There is a group of 64 bytes buffer shared by endpoint0 sending and receiving.

Endpoint1 and endpoint2 and endpoint3 each have a sending pipe (IN) and a receiving pipe (OUT), and the transmitter and receiver each have a single 64-byte buffer or a double 64-byte buffer for USB transfers.

Endpoint4 has a sending pipe (IN) and a receiving pipe (OUT), and the transmitter and receiver each have a single 64-byte buffer for USB transfers.

Each endpoint has a control register (UEPn_CTRL) and a transmittal length register (UEPn_T_LEN) (n = 0/1/2/3/4) to configure the data toggle flag, handshake response, transmittal length, etc.

The pull-up resistor of the USB device port is enabled or disabled by the software settings. If you set the bUC_DEV_PU_EN bit in the USB_CTRL register, the USB device function start. At this time, the CH559 internal DP or DM pin connected to the pull-up resistor according to the bUD_LOW_SPEED bit. When the event of bus reset, suspend or resume is detected or USB transfer completion, the USB SIE will generate the corresponding interrupt flag and interrupt request. The use program can directly query USB interrupt flag register (USB_INT_FG) or query in the interrupt service routine (ISR). If UIF_TRANSFER bit is valid, you should also do the corresponding processing according to the value of interrupt status register (USB_INT_ST) and MASK_UIS_ENDP and MASK_UIS_TOKEN. If you configure the bUEP_R_TOG bit for each endpoint OUT transaction, you can query the U_TOG_OK bit or bUIS_TOG_OK bit to determine whether the current received data toggle match with the expected, and if the toggle is OK, the data is valid otherwise the data should be discarded. After processing the send or receive data, you need to correct the toggle of the endpoint for the next data packet to send or receive data packet match-detect. Setting the bUEP_AUTO_TOG bit may enable toggle turn automatically after transfer completion.

The prepared data to send by each endpoint are placed in the buffer of each endpoint, and the length of data should be written to the transmittal length register of each endpoint (UEPn_T_LEN). The receive data by each endpoint are placed in the buffer of each endpoint, and the length of receive data of each endpoint is all placed in the USB receiving data length register (USB_RX_LEN).

Table 16.3.1 List of USB device registers

Name	Address	Description	Reset value
UEP1_CTRL	D2h	Endpoint1 control	0000 0000b
UEP1_T_LEN	D3h	Endpoint1 transmittal length	0xxx xxxxb
UEP2_CTRL	D4h	Endpoint2 control	0000 0000b
UEP2_T_LEN	D5h	Endpoint2 transmittal length	0000 0000b
UEP3_CTRL	D6h	Endpoint3 control	0000 0000b
UEP3_T_LEN	D7h	Endpoint3 transmittal length	0xxx xxxxb
UEP0_CTRL	DCh	Endpoint0 control	0000 0000b
UEP0_T_LEN	DDh	Endpoint0 transmittal length	0xxx xxxxb
UEP4_CTRL	DEh	Endpoint4 control	0000 0000b
UEP4_T_LEN	DFh	Endpoint4 transmittal length	0xxx xxxxb
UDEV_CTRL	E4h	USB device physical port control	0100 x000b

UEP4_1_MOD	2446h	Endpoint4/1 mode control	0000 0000b
UEP2_3_MOD	2447h	Endpoint2/3 mode control	0000 0000b
UEP0_DMA_H	2448h	High byte of 16-bit endpoint 0/4 buffer start address	0000 xxxxb
UEP0_DMA_L	2449h	Low byte of 16-bit endpoint 0/4 buffer start address	xxxx xxx0b
UEP0_DMA	2448h	16-bit endpoint 0/4 buffer start address, (consists of UEP0_DMA_L and UEP0_DMA_H).	xxxxh
UEP1_DMA_H	244Ah	High byte of 16-bit endpoint1 buffer start address	000x xxxxb
UEP1_DMA_L	244Bh	Low byte of 16-bit endpoint1 buffer start address	xxxx xxx0b
UEP1_DMA	244Ah	16-bit endpoint1 buffer start address, (consists of UEP1_DMA_L and UEP1_DMA_H)	xxxxh
UEP2_DMA_H	244Ch	High byte of 16-bit endpoint2 buffer start address	000x xxxxb
UEP2_DMA_L	244Dh	Low byte of 16-bit endpoint2 buffer start address	xxxx xxx0b
UEP2_DMA	244Ch	16-bit endpoint2 buffer start address, (consists of UEP2_DMA_L and UEP2_DMA_H)	xxxxh
UEP3_DMA_H	244Eh	High byte of 16-bit endpoint3 buffer start address	000x xxxxb
UEP3_DMA_L	244Fh	Low byte of 16-bit endpoint3 buffer start address	xxxx xxx0b
UEP3_DMA	244Eh	16-bit endpoint 3 buffer start address, (consists of UEP3_DMA_L and UEP3_DMA_H)	xxxxh
pUEP*	254*h	After setting bXIR_XSFR, the pdata will be addressed in xSFR, which is faster than xdata adderssing.	

Endpoint n control (UEPn_CTRL):

Bit	Name	Access	Description	Reset value
7	bUEP_R_TOG	RW	Expected data toggle flag of USB endpoint n receiving (SETUP/OUT): 1 = Expected DATA1. 0 = Expected DATA0.	0
6	bUEP_T_TOG	RW	Prepared data toggle flag of USB endpoint n transmittal (IN): 1 = Send DATA1. 0 = Send DATA0.	0
5	Reserved	RO	Reserved	0
4	bUEP_AUTO_TOG	RW	Enable automatic toggle after successful transfer completion on endpoint 1/2/3: 1 = Automatic toggle. 0 = Manual toggle.	0
3	bUEP_R_RES1	RW	High bit of handshake response type for USB endpoint n receiving (SETUP/OUT).	0
2	bUEP_R_RES0	RW	Low bit of handshake response type for USB endpoint n receiving (SETUP/OUT).	0
1	bUEP_T_RES1	RW	High bit of handshake response type for USB endpoint n transmittal (IN).	0
0	bUEP_T_RES0	RW	Low bit of handshake response type for USB endpoint n transmittal (IN).	0

MASK_UEP_R_RES consists of bUEP_R_RES1 bit and bUEP_R_RES0 bit, used to indicate handshake response type for USB endpoint n receiving (SETUP/OUT):
00 = ACK
01 = timeout/ no response (for isochronous transfers)
10 = NAK
11 = STALL

MASK_UEP_T_RES consist of bUEP_T_RES1 bit and bUEP_T_RES0 bit, used to indicate handshake response type for USB endpoint n transmittal (IN):
00 = DATA0/DATA1 and expected host ACK
01 = DATA0/DATA1 and expected host no response (for Isochronous transfers)
10 = NAK
11 = STALL

Endpoint n transmittal length (UEPn_T_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	bUEPn_T_LEN	RW	Endpoint n transmittal length, (n = 0/1/3/4).	xxh
	bUEP2_T_LEN		Endpoint2 transmittal length.	00h

USB device physical port control (UDEV_CTRL):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bUD_RECV_DIS	RW	Disable USB physical port receiver: 1 = Disable receiver. 0 = Enable receiver.	1
5	bUD_DP_PD_DIS	RW	Disable USB DP pull-down resistor: 1 = Disable. 0 = Enable pull-down.	0
4	bUD_DM_PD_DIS	RW	Disable USB DM pull-down resistor: 1 = Disable. 0 = Enable pull-down.	0
3	bUD_DIFF_IN	R0	Current DP/DM difference input status.	x
2	bUD_LOW_SPEED	RW	Enable USB physical port low speed: 1 = Low speed (1.5Mbps). 0 = Full speed (12Mbps).	0
1	bUD_GP_BIT	RW	General purpose bit. User-defined. Can be set and reset by software.	0
0	bUD_PORT_EN	RW	Enable USB physical port I/O: 1 = Enable. 0 = Disable.	0

Endpoint 4/1 mode control (UEP4_1_MOD):

Bit	Name	Access	Description	Reset value
7	bUEP1_RX_EN	RW	Enable USB endpoint1 receiving (OUT): 1 = Enable. 0 = Disable.	0
6	bUEP1_TX_EN	RW	Enable USB endpoint1 transmittal (IN): 1 = Enable. 0 = Disable.	0
5	Reserved	RO	Reserved	0
4	bUEP1_BUF_MOD	RW	Buffer mode control of USB endpoint1	0
3	bUEP4_RX_EN	R0	Enable USB endpoint4 receiving (OUT): 1 = Enable. 0 = Disable.	0
2	bUEP4_TX_EN	RW	Enable USB endpoint4 transmittal (IN): 1 = Enable. 0 = Disable.	0
[1:0]	Reserved	RO	Reserved	00b

Configuration of buffer mode of endpoint 0 and 4 by bUEP4_RX_EN bit and bUEP4_TX_EN bit. Refer to the following table.

Table 16.3.2 Buffer mode of endpoint 0 and 4

bUEP4_RX_EN	bUEP4_TX_EN	Description: buffer start address is UEP0_DMA
0	0	Single 64 bytes buffer for endpoint 0 receiving & transmittal (OUT & IN endpoint).
1	0	Single 64 bytes buffer for endpoint 0 receiving & transmittal (OUT & IN endpoint) and for endpoint 4 receiving (OUT endpoint), total = 128 bytes
0	1	Single 64 bytes buffer for endpoint 0 receiving & transmittal (OUT & IN endpoint) and for endpoint 4 transmittal (IN endpoint), total = 128 bytes
1	1	Single 64 bytes buffer for endpoint 0 receiving & transmittal (OUT & IN endpoint) + 64 bytes buffer for endpoint 4 receiving (OUT endpoint) + 64 bytes buffer for endpoint 4 transmittal (IN endpoint), total is 192bytes. Start address UEP0_DMA+0: endpoint 0 receiving & transmittal. Start address UEP0_DMA+64: endpoint 4 receiving. Start address UEP0_DMA+128: endpoint 4 transmittal.

Endpoint 2/3 mode control (UEP2_3_MOD):

Bit	Name	Access	Description	Reset value
7	bUEP3_RX_EN	RW	Enable USB endpoint3 receiving (OUT): 1 = Enable.	0

			0 = Disable.	
6	bUEP3_TX_EN	RW	Enable USB endpoint3 transmittal (IN): 1 = Enable. 0 = Disable.	0
5	Reserved	RO	Reserved	0
4	bUEP3_BUF_MOD	RW	Buffer mode control of USB endpoint3.	0
3	bUEP2_RX_EN	R0	Enable USB endpoint2 receiving (OUT): 1 = Enable. 0 = Disable.	0
2	bUEP2_TX_EN	RW	Enable USB endpoint2 transmittal (IN): 1 = Enable. 0 = Disable.	0
1	Reserved	RO	Reserved	0
0	bUEP2_BUF_MOD	RW	Buffer mode control of USB endpoint 2.	0

Configuration buffer mode of endpoint 1 or 2 or 3 by bUEPn_RX_EN bit and bUEPn_TX_EN bit and bUEPn_BUF_MOD bit, (n = 1/2/3). Refer to the following table.

Table 16.3.3 Buffer mode of endpoint n (n=1/2/3)

bUEPn_RX_EN	bUEPn_TX_EN	bUEPn_BUF_MOD	Description: buffer start address is UEPn_DMA
0	0	x	Disable endpoint and disable buffer.
1	0	0	Single 64 bytes buffer for receiving (OUT)
1	0	1	Dual 64 bytes buffer by toggle bit bUEP_R_TOG selection for receiving (OUT), total = 128bytes.
0	1	0	Single 64 bytes buffer for transmittal (IN).
0	1	1	Dual 64 bytes buffer by toggle bit bUEP_T_TOG selection for transmittal (IN), total = 128bytes.
1	1	0	Single 64 bytes buffer for receiving (OUT) + Single 64 bytes buffer for transmittal (IN), total = 128bytes.
1	1	1	Dual 64 bytes buffer by bUEP_R_TOG selection for receiving (OUT) + dual 64 bytes buffer by bUEP_T_TOG selection for transmittal (IN), total = 256bytes. Start address UEPn_DMA+0: endpoint receiving when bUEP_R_TOG bit is 0. Start address UEPn_DMA+64: endpoint receiving when bUEP_R_TOG bit is 1. Start address UEPn_DMA+128: endpoint transmittal when bUEP_T_TOG bit is 0. Start address UEPn_DMA+192: endpoint transmittal when bUEP_T_TOG bit is 1.

16-bit endpoint n buffer start address (UEPn_DMA)(n=0/1/2/3):

Bit	Name	Access	Description	Reset value
[7:0]	UEPn_DMA_H	RW	High byte of 16-bit endpoint n buffer start address. Among them, the low 5 bits are effective, and the high 3 bits are always 0.	xxh
[7:0]	UEPn_DMA_L	RW	Low byte of 16-bit endpoint n buffer start address. Among them, the high 7 bits are effective, and the low 1 bit is always 0, and only even address.	xxh

Note: receiving data length > = min(maximum packet length possible+2 bytes, 64 bytes)

16.4 USB host control registers

CH559 provides a set of bidirectional host endpoints in host mode, including a transmittal endpoint (OUT) and a receiver endpoint (IN). The maximum data packet size for all endpoints is 64 bytes for control / interrupt / bulk / isochronous transactions.

After processing the USB things initiated by the host, CH559 will automatically set the interrupt flag UIF_TRANSFER bit. The user program can read the interrupt flag register (USB_INT_FG) by the way of query or interrupt, and deal with according to the interrupt flags. If the UIF_TRANSFER bit is valid, it also needs to analyze the interrupt status register (USB_INT_ST) and deal with based on the current handshake response PID (MASK_UIS_H_RES) for USB host transmittal.

If you configure the bUEP_R_TOG bit for host receiver endpoint (IN), you can query the U_TOG_OK bit or bUIS_TOG_OK bit to determine whether the current received data toggle match the expected, and if the toggle is OK, the data is valid otherwise the data should be discarded. After processing the send or receive data, you need to correct the toggle of the endpoint for the next data packet to send or receive data packet to match-detect. Setting the bUEP_AUTO_TOG bit can be achieved toggle turn automatically after transfer completion.

The UH_EP_PID register for host mode is alternate-function of the UEP2_T_LEN register for device mode, which is used to configure the endpoint number of the target device and the PID of USB packet. The data buffer start address for USB data packet following SETUP/OUT packet is filled in UH_TX_DMA register and the length of data should be written to the transmit length register of host endpoint (UH_TX_LEN). The receiving data packet start address by host endpoint is placed in the UH_RX_DMA register, and the length of receive data of host endpoint is placed in the USB receiving data length register (USB_RX_LEN).

Table 16.4.1 List of USB host registers

Name	Address	Description	Reset value
UH_SETUP	D2h	Host auxiliary setup	0000 0000b
UH_RX_CTRL	D4h	Host receiver endpoint control	0000 0000b
UH_EP_PID	D5h	Host endpoint and token PID	0000 0000b
UH_TX_CTRL	D6h	Host transmittal endpoint control	0000 0000b
UH_TX_LEN	D7h	Host endpoint transmittal length	0xxx xxxxb
USB_HUB_ST	DBh	USB host hub status (Read-only)	0000 0000b
UHUB0_CTRL	E4h	USB hub0 control	0100 x000b
UHUB1_CTRL	E5h	USB hub1 control	1100 x000b

UH_EP_MOD	2447h	Host endpoint mode control	0000 0000b
UH_RX_DMA_H	244Ch	High byte of host receiving endpoint buffer start address	000x xxxxb
UH_RX_DMA_L	244Dh	Low byte of host receiving endpoint buffer start address	xxxx xxx0b
UH_RX_DMA	244Ch	16-bit host receiving endpoint buffer start address (consists of UH_RX_DMA_L and UH_RX_DMA_H)	xxxxh
UH_TX_DMA_H	244Eh	High byte of host transmittal endpoint buffer start address	000x xxxxb
UH_TX_DMA_L	244Fh	Low byte of host transmittal endpoint buffer start address	xxxx xxx0b
UH_TX_DMA	244Eh	16-bit host transmittal endpoint buffer start address (consists of UH_TX_DMA_L and UH_TX_DMA_H).	xxxxh
pUH_*	254*h	After setting bit bXIR_XSFR, the pdata will be addressed in xSFR, which is faster than xdata addressing.	

Host auxiliary setup (UH_SETUP):

Bit	Name	Access	Description	Reset value
7	bUH_PRE_PID_EN	RW	USB host PRE PID enable for low speed device via hub: 1 = Enable PRE. 0 = Disable. Cannot operate low device via hub.	0
6	bUH_SOF_EN	RW	USB host automatic SOF enable: 1 = Enable. 0 = Disable. Send SOF manually.	0
[5:0]	Reserved	RO	Reserved	00h

Host receiver endpoint control (UH_RX_CTRL):

Bit	Name	Access	Description	Reset value
7	bUH_R_TOG	RW	Expected data toggle flag of host receiving (IN): 1 = DATA1. 0 = DATA0.	0
[6:5]	Reserved	RO	Reserved	00b
4	bUH_R_AUTO_TOG	RW	Enable automatic toggle after successful transfer completion: 1 = Automatic toggle. 0 = Manual toggle.	0
3	Reserved	RO	Reserved	0
2	bUH_R_RES	RW	Prepared handshake response type for host receiving (IN): 1 = No response, time out to device, for isochronous transactions (not for endpoint 0). 0 = ACK (ready).	0
[1:0]	Reserved	RO	Reserved	00b

Host endpoint and token PID (UH_EP_PID):

Bit	Name	Access	Description	Reset value
[7:4]	MASK_UH_TOKEN	RW	Token PID for USB host transfer	0000b
[3:0]	MASK_UH_ENDP	RW	Endpoint number for USB host transfer.	0000b

Host transmittal endpoint control (UH_TX_CTRL):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bUH_T_TOG	RW	Prepared data toggle flag of host transmittal (SETUP/OUT): 1 = DATA1. 0 = DATA0.	0
5	Reserved	RO	Reserved	0
4	bUH_T_AUTO_TOG	RW	Enable automatic toggle after successful transfer completion: 1 = Automatic toggle. 0 = Manual toggle.	0
[3:1]	Reserved	RO	Reserved	000b
0	bUH_T_RES	RW	Expected handshake response type for host transmittal (SETUP/OUT): 1 = No response, time out from device, for isochronous transactions (not for endpoint 0). 0 = ACK (ready).	0

Host endpoint transmittal length (UH_TX_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	UH_TX_LEN	RW	Host endpoint transmittal length.	xxh

USB host hub status (USB_HUB_ST):

Bit	Name	Access	Description	Reset value
7	bUHS_H1_ATTACH	RO	Device attached status on USB hub1 HP/HM, (equal to bUMS_H1_ATTACH): 1 = Connect. 0 = Disconnect.	0
6	bUHS_HM_LEVEL	RO	HM level saved at device attached to USB hub1: 1 = High level. 0 = Low level.	0
5	bUHS_HP_PIN	RO	Current HP pin level:	0

			1 = High level. 0 = Low level.	
4	bUHS_HM_PIN	RO	Current HM pin level: 1 = High level. 0 = Low level.	0
3	bUHS_H0_ATTACH	RO	Device attached status on USB hub0 DP/DM, (equal to bUMS_H0_ATTACH): 1 = Connect. 0 = Disconnect.	0
2	bUHS_DM_LEVEL	RO	DM level saved at device attached to USB hub0: 1 = High level. 0 = Low level.	0
1	bUHS_DP_PIN	RO	Current DP pin level: 1 = High level. 0 = Low level.	0
0	bUHS_DM_PIN	RO	Current DM pin level: 1 = High level. 0 = Low level.	0

USB hub n control (UHUBn_CTRL) (n = 0.1)

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved for SFR UHUB0_CTRL	0
7	bUH1_DISABLE	RW	Disable USB hub1 pin: 1 = Disable hub1 and releasing HP/HM pin. 0 = Enable hub1 and using HP/HM pin.	1
6	bUH_RECV_DIS	RW	Disable USB HUBn receiver: 1 = Disable hub receiver. 0 = Enable hub receiver.	1
5	bUH_DP_PD_DIS	RW	Disable USB DP or HP pull-down resistor: 1 = Disable. 0 = Enable pull-down.	0
4	bUH_DM_PD_DIS	RW	Disable USB DM or HM pull-down resistor: 1 = Disable. 0 = Enable pull-down.	0
3	bUH_DIFF_IN	R0	Current DP/DM or HP/HM difference input status	x
2	bUH_LOW_SPEED	RW	Enable USB hub low speed: 1 = Low speed (1.5Mbps). 0 = Full speed (12Mbps).	0
1	bUH_BUS_RESET	RW	Control USB hub bus reset: 1 = Force bus reset. 0 = Normal.	0

0	bUH_PORT_EN	RW	Enable USB hub port: 1 = Enable port, automatic disabled if USB device detached. 0 = Disable.	0

Host endpoint mode control (UH_EP_MOD):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bUH_EP_TX_EN	RW	Enable USB host endpoint transmittal: 1 = Enable. 0 = Disable.	0
5	Reserved	RO	Reserved	0
4	bUH_EP_TBUF_MOD	RW	Buffer mode control of USB host transmittal endpoint	0
3	bUH_EP_RX_EN	RO	Enable USB host endpoint receiving: 1 = Enable. 0 = Disable.	0
[2:1]	Reserved	RO	Reserved	00b
0	bUH_EP_RBUF_MOD	RW	Buffer mode of USB host receiving endpoint	0

Configuration buffer mode of USB host transmittal endpoint by bUH_EP_TX_EN bit and bUH_EP_TBUF_MOD bit. Refer to the following table.

Table 16.4.2 List of USB host transmittal endpoint buffer

bUH_EP_TX_EN	bUH_EP_TBUF_MOD	Description : buffer start address is UH_TX_DMA
0	x	Disable endpoint and disable buffer.
1	0	Single 64 bytes buffer for transmittal (OUT endpoint).
1	1	Dual 64 bytes buffer by toggle bit bUH_T_TOG selection for transmittal (OUT endpoint), total = 128bytes. Select the first 64 bytes of buffer if bUH_T_TOG bit is 0. Select the last 64 bytes of buffer if bUH_T_TOG bit is 1.

Configuration buffer mode of USB host receiving endpoint by bUH_EP_TX_EN bit and bUH_EP_TBUF_MOD bit. Refer to the following table.

Table 16.4.3 USB host receiving endpoint buffer list

bUH_EP_RX_EN	bUH_EP_RBUF_MOD	Description : buffer start address is UH_ RX _DMA
0	x	Disable endpoint and disable buffer.
1	0	Single 64 bytes buffer for receiving (IN endpoint).
1	1	Dual 64 bytes buffer by toggle bit bUH_R_TOG selection for receiving (IN endpoint), total = 128bytes. Select the first 64 bytes of buffer if bUH_R_TOG bit is 0.

		Select the last 64 bytes of buffer if bUH_R_TOG bit is 1.

16-bit host receiving endpoint buffer start address (UH_RX_DMA)

Bit	Name	Access	Description	Reset value
[7:0]	UH_RX_DMA_H	RW	High byte of host receiving endpoint buffer start address. Among them, the low 5 bits are effective and the high 3 bits are fixed to 0.	xxh
[7:0]	UH_RX_DMA_L	RW	Low byte of host receiving endpoint buffer start address. Among them, the high 7 bits are effective and the low 1 bit are fixed to 0, and only even address.	xxh

16-bit host transmittal endpoint buffer start address (UH_TX_DMA):

Bit	Name	Access	Description	Reset value
[7:0]	UH_TX_DMA_H	RW	High byte of host transmittal endpoint buffer start address. Among them, the low 5 bits are effective and the high 3 bits are fixed to 0.	xxh
[7:0]	UH_TX_DMA_L	RW	Low byte of host transmittal endpoint buffer start address. Among them, the high 7 bits are effective and the low 1 bit is fixed to 0, and only even address.	xxh

17. LED display control interface

17.1 LED control card

CH559 provides LED display control interface, built-in 4-level FIFO, It supports DMA and interrupt, which saves the processing time for CPU. It also supports 1/2/4 data line.

Table 17.1.1 List of LED display interface registers

Name	Address	Description	Reset value
LED_STAT	2880h	LED status	010x 0000b
LED_CTRL	2881h	LED control	0000 0010b
LED_FIFO_CN	2882h	LED FIFO count (read-only)	0000 0000b
LED_DATA	2882h	LED data (write-only)	xxxx xxxxb
LED_CK_SE	2883h	LED clock divisor setting	0001 0000b
LED_DMA_AH	2884h	High byte of 16-bit DMA address	000x xxxxb
LED_DMA_AL	2885h	Low byte of 16-bit DMA address	xxxx xxx0b
LED_DMA	2884h	16-bit DMA address (consists of LED_DMA_AL and LED_DMA_AH)	xxxxh
LED_DMA_CN	2886h	DMA remainder word count	xxxx xxxxb
LED_DMA_XH	2888h	High byte of 16-bit auxiliary buffer DMA address	000x xxxxb
LED_DMA_XL	2889h	Low byte of 16-bit auxiliary buffer DMA address	xxxx xxx0b
LED_DMA_X	2888h	16-bit auxiliary buffer DMA address (consists of	xxxxh

		LED_DMA_XL and LED_DMA_XH)	
pLED_*	298*h	After setting bXIR_XSFR, the pdata will be addressed in xSFR, which is faster than xdata addressing.	

LED status register (LED_STAT):

Bit	Name	Access	Description	Reset value
7	bLED_IF_DMA_END	RW	DMA complete interrupt flag. 1 = DMA completion. 0 = No interrupt. Write 1 to clear or write LED_DMA_CN to clear.	0
6	bLED_FIFO_EMPTY	RO	FIFO empty flag: 1 = FIFO is empty. 0 = FIFO is not empty.	0
5	bLED_IF_FIFO_REQ	RW	Request FIFO data flag(FIFO < = 2): 1 = FIFO is not full. 0 = FIFO is full. Write 1 to clear.	0
4	bLED_CLOCK	R0	Current LED clock level.	x
3	Reserved	RO	Reserved	0
[2:0]	MASK_LED_FIFO_CNT	R0	Current LED FIFO count.	000b

LED control register (LED_CTRL):

Bit	Name	Access	Description	Reset value
7	bLED_CHAN_MOD1	RW	LED channel mode high bit	0
6	bLED_CHAN_MOD0	RW	LED channel mode low bit	0
5	bLED_IE_FIFO_REQ	RW	Enable interrupt for FIFO < = 2: 1 = Enable interrupt for FIFO < = 2. 0 = Disable.	0
4	bLED_DMA_EN	RW	DMA enable and DMA interrupt enable for LED: 1 = Enable. 0 = Disable.	0
3	bLED_OUT_EN	RW	LED output enable: 1 = Enable. 0 = Disable.	0
2	bLED_OUT_POLAR	RW	LED output polarity: 1 = Invert. 0 = Passthrough.	0
1	bLED_CLR_ALL	RW	Force clear FIFO and count of LED, need software clear.	1
0	bLED_BIT_ORDER	RW	LED bit data order: 1 = MSB first. 0 = LSB first.	0

Table 16.1.2 LED channel mode

bLED_CHAN_MOD1	bLED_CHAN_MOD0	Description
0	0	Single channel output, LED0
0	1	Dual channels output, LED0/1
1	0	4 channels output, LED0 to 3. The data from LED_DMA buffer take turns to LED0 to LED3.
1	1	4 channels output and LED2/3 from auxiliary buffer, LED0~3. LED0 and LED1 data are from LED_DMA buffer. LED2 and LED3 data are from LED_DMA_X buffer.

LED FIFO count (LED_FIFO_CN):

Bit	Name	Access	Description	Reset value
[7:0]	LED_FIFO_CN	RO	Current FIFO count. Only the low 3 bits are effective and the high 5 bits are fix to 0.	00h

LED data (LED_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	LED_DATA	WO	LED data port for FIFO.	xxh

LED clock divisor setting (LED_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	LED_CK_SE	RW	Set LED output clock divisor	10h

16-bit DMA address (LED_DMA):

Bit	Name	Access	Description	Reset value
[7:0]	LED_DMA_AH	RW	SFR high byte of 16-bit DAM address. This byte is the initial value of the high byte of the 16-bit DMA address and then the DMA address is increased automatically. Only the low 5 bits are valid, and high 3 bits are fixed to 0.	xxh
[7:0]	LED_DMA_AL	RW	SFR low byte of 16-bit DAM address. This byte is the initial value of the high byte of the 16-bit DMA address and then the DMA address is increased automatically. The high 7 bits are valid, and the low bit is fixed to 0. Only for even address.	xxh

16-bit auxiliary buffer DMA address (LED_DMA_X):

Bit	Name	Access	Description	Reset value
[7:0]	LED_DMA_XH	RW	SFR high byte of 16-bit DAM address. This byte is the initial value of the high byte of the 16-bit auxiliary buffer DMA address and then the DMA address is increased automatically. Only the low 5 bits are valid, and high 3 bits are fixed to 0.	xxh
[7:0]	LED_DMA_XL	RW	SFR low byte of 16-bit DAM address. This byte is the initial value of the high byte of the 16-bit auxiliary buffer DMA address and then the DMA address is increased automatically. The high 7 bits are valid, and the low bit is fixed to 0. Only for even address.	xxh

DMA remainder word counter (LED_DMA_CN):

Bit	Name	Access	Description	Reset value
[7:0]	LED_DMA_CN	RW	DMA remainder word count, just main buffer and exclude auxiliary buffer, automatic decreasing after DMA	00h

17.2 LED display control application

(1) Configure the LEDC and LED0~LED3 pins for the output mode and set the I/O port drive capability.
(2) Configure the LED_CK_SE register, selecting LED output clock divisor.
(3) Write the LED_DMA register as DMA data buffer start address which is main buffer.
(4) If the channel mode of LED is 3, you need write LED_DMA_X register, which auxiliary buffer.
(5) Configure the LED_CTRL register, select channel mode, output polarity, bit data order, interrupt and DMA, etc...For example, LED_CTRL = bLED_CHAN_MOD0 | bLED_DMA_EN | bLED_OUT_EN.
(6) Configure DMA remainder word count, and enable DMA. Or you can send data by FIFO.
(7) You can use the query or interrupt mode to deal with the corresponding flag status.

18. Parameters

18.1 Absolute maximum ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Symbol	Parameter description	Min.	Max.	Unit
TA	Operating temperature	-40	85	℃
TS	Storage temperature	-55	125	℃
VDD33	Internal operating supply voltage (VCC33 is connected to power, GND is connected to ground)	-0.4	3.6	V
VIN5	External input supply voltage (VIN5 is connected to power, GND is connected to ground)	-0.4	5.6	V
VIO5	Voltage on the input or output pins support 5V	-0.4	5.5	V

VIO3	Voltage on the input or output pins not support 5V	-0.4	VDD33+0.4	V

18.2 Electrical characteristics

Test conditions: TA=25℃, VIN5=5V or 3.3V, VDD33=3.3V, Fsys=12MHz.

Symbol	Parameter description		Min.	Typ.	Max.	Unit
VDD33	Internal power voltage		2.85	3.3	3.6	V
VIN5	External input supply voltage	External capacitor connected to VDD33 pin	3.6	5	5.5	V
		VDD33 pin shorted to VIN5 pin	2.85	3.3	3.6	V
ICC	Total operating current		4	8	50	mA
ISLP	Total sleep current			0.1	0.2	mA
VIL	Input low voltage		-0.4		0.8	V
VIH	Input high voltage		2.0		VDD33+0.4	V
VOL	Output low voltage (I_{IL} = 4mA)				0.4	V
VOH	Output highvoltage (I_{OH} = 4mA)		VDD33-0.4			V
IIN	The input current without pull-up resistor		-5	0	5	uA
IUP	The input current with pull-up resistor		20	40	80	uA
IDN	The input current with pull-down resistor		-20	-40	-80	uA
IUPX	The input current with pull-up resistor from low to high		200	300	500	uA
Vpot	Power on reset threshold		2.4	2.55	2.7	V

Note: All the current of pull-up are pulled up to VDD33, not VIN5.

18.3 AC electrical characteristics

Test conditions: TA=25℃, VIN5=5V or 3.3V, VDD33=3.3V, Fsys=12MHz.

Symbol	Parameter description	Min.	Typ.	Max.	Unit
Fxt	External clock input frequency	4	12	20	MHz
Fosc	Internal clock frequency	11.82	12	12.18	MHz
Fpll	Frequency after PLL	24	288	350	MHz
Fusb4x	USB sampling clock frequency for the USB host	47.98	48	48.02	MHz
	USB sampling clock frequency for the USB device	47.04	48	48.96	MHz
Fsys	System frequency (VDD33>=3V)	1	12	56	MHz
	System frequency (VDD33<3V)	1	12	50	MHz
Tpor	Power on reset delay	15	17	20	mS
Trst	External input valid reset signal width	70	100	200	nS
Trdl	Thermal reset delay	35	60	100	uS
Twdc	Watchdog overflow/ Timer calculation formula	262144 * (0x100 - WDOG_COUNT) / Fsys			
Tusp	Automatically hang up time in USB host mode	2	3	4	mS
	Automatically hang up time in USB device mode	4	5	6	mS
Twak	Time to wake up from sleep mode	1	40	100	uS

19. Revision history

Version	Date	Description
V1.0	September 26, 2014	Initial release
V1.1	August 14, 2015	Update: Section 12.5.2, Section 14.4
V1.2	September 25, 2015	Update: Chapter 1, Chapter 4, Section 16.3, Chapter 17, Section 18.3
V1.3	July 22, 2016	Update: Section 12.5
V1.4	February 10, 2017	Update: Chapter 2, Section 6.7, Section 14.4.2
V1.5	November 22, 2017	Update: RCAP2H in Table 5.1, Table 6.7.1
V1.6	January 05, 2022	Typo corrected: P3 direction control register. Note that USB pins are not connected to external resistors in series. Expression optimized: Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.