WD7910/LP

ISA-Based System Controller

with Cache for 80386SX and 80286

Desktop and Portable Compatibles

WESTERN DIGITAL

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1.0 INTRODUCTION

The WD7910 is the second generation single chip AT solution based on the WD76C10A core. It is fabricated in 0.9 micron CMOS. The WD7910 provides 8 Kbytes of direct-mapped or two-way set associative lookaside caching, a page-interleaved memory controller, and enhanced power management features. Figure 1-1 shows the block diagram of the WD7910-based system.

The standard version of the WD7910 operates from 5 VDC (±10%) supplies. An extended low-power version, the WD7910LP, can operate with 3.3 VDC (±0.3V) or 5 VDC (±0.5V).

1.1 DOCUMENT SCOPE

This document describes the function and operation of the WD7910 and WD7910LP System Controller devices. It includes the description of external logic necessary for efficient use of these devices. In most instances the WD7910 and WD7910LP operate similarly and are referred to in this document as the System Controller. Where there are differences, the devices are identified specifically.

1.2 FEATURES

- Software compatible with WD76C10A
- 8Kbyte on-chip cache for 80386SX
  - Direct map or 2 way set-associative
  - Self timed Integrated RAM arrays
  - Programmable non-cacheable regions
  - Diagnostic mode to test Tag and Data Ram
  - Flush command
  - 25 Mhz zero wait state cache hit
- ROM may be shadowed and/or cached
- Supports Static CPU for power savings in sleep mode
- Supports extra wait state for page mode
- Supports VLBI for high-speed video access
- Operates at speeds of 16 MHz, 20 MHz and 25 MHz.
- Interfaces with 80286, or 80386SX CPUs.
- Supports memory in four banks with 64 Kbits, 256 Kbits, 1 Mbits or 4 Mbits DRAMs. Also supports new 512k x 8, 1M x 16 and 2M x 8 DRAM configurations.
- Page mode zero wait state access at 25 MHz with 70 ns DRAM.
- Supports up to 16 Mbyte of real memory, or 32 Mbyte of EMS memory.
- Maintains controlled propagation delay for 80386SX reset.
- Employs an internal self-tuning delay line for DRAM control.
- Self-adjusting output drivers minimize output rise/fall time variations and reduces EMI and ground noise.
- DRAM address multiplexer drives 350 pF with adjustable strength drivers.
- Main and VGA BIOS may be mapped into one physical PROM.
- Advanced 64 Kbyte and 128 Kbyte ROM shadowing allows main BIOS and video BIOS shadowing along with 320 Kbyte and 256 Kbyte remap to extended or expanded memory.
- Offers additional power saving modes:
  - Slow Refresh
  - Stop DMA Clock
- Parity generation and checking.
- 160-pin PQFP package
- 3.3V low power operation
- I/O Pin mapping for testability
- Low power 0.9 micron CMOS technology.

Additional features of WD7910LP only:

- Supports System Management Interrupt (SMI)
- Provides I/O trapping
- Provides System Activity Monitor (SAM).
- Provides power control with suspend and resume.
- Provides processor stop clock.
- Features CAS before RAS slow refresh for portable applications.
- Offers automatic processor clock speed switching.
- 3V Suspend to hard disk

1.3 GENERAL DESCRIPTION

The WD7910 is designed for use in a high performance desktop AT computer using an 80286 or 80386SX processor up to 25 MHz. The WD7910LP has the features of the WD7910 and is designed to operate in a high-performance notebook/laptop AT compatible computer using an 80286 or 80386SX processor.

1.3.1 WD7910

The WD7910 contains a high performance memory controller with programmable modes of operation. It supports non-page, zero wait state read and write memory control. A maximum of four banks of 64 Kbit, 256 Kbit, 1 Mbit, 4 Mbit or 16 Mbit DRAM may be controlled, allowing up to 16 Mbytes of real or 32 Mbytes EMS (Expanded Memory Specification) memory. Any combination of DRAM sizes may be used. In addition, the WD7910 controls page mode DRAM or static column DRAM with page mode operation.

The on-board memory can be allocated either to extended or EMS memory in 128 Kbyte increments. Forty EMS registers support EMS 4.0 multitasking.

An internal self-tuning delay line is used for DMA and Bus Master memory cycles. Delay line information is also used to adjust the strength of the output drivers. This stabilizes the output rise and fall times, which reduces ground noise and electromagnetic interference (EMI).

EMS access to external RAM or ROM may be used to support Kanji or other extended character sets.

The WD7910 interfaces with either an 80286 or 80386SX processor. The processor type is automatically sensed at power-up. No extra logic is required to interface with the 80386SX. The variation in processor reset propagation delay is controlled to meet the strict reset timing of the 80386SX.

1.3.2 WD7910LP

In addition to supporting all the features of the WD7910, the WD7910LP also supports portable notebook/laptop computers. To provide this support, the WD7910LP makes use of Power Management Control (PMC) for powering down peripherals or the processor, which includes processor stop clock, slow clock, automatic processor clock speed switching modes and CAS before RAS slow refresh. Suspend and resume is supported when low power DRAM is refreshed while the processor and other power consuming devices are turned off. The power drain for the core logic and VGA controller is less than 5 mA in this mode. Power and clock speed may be controlled by the keyboard processor, transparently to the 80286 or 80386SX.

The System Activity Monitor (SAM) provided by WD7910LP is a transparent feature that replaces the functions previously performed by software. It determines when the system has been idle for a previously programmed period of time and determines a clean break point in which to perform powerdown activities such as suspend.

The WD7910LP also supports System Management Interrupt (SMI) with complete I/O trapping of up to six separate I/O ranges.

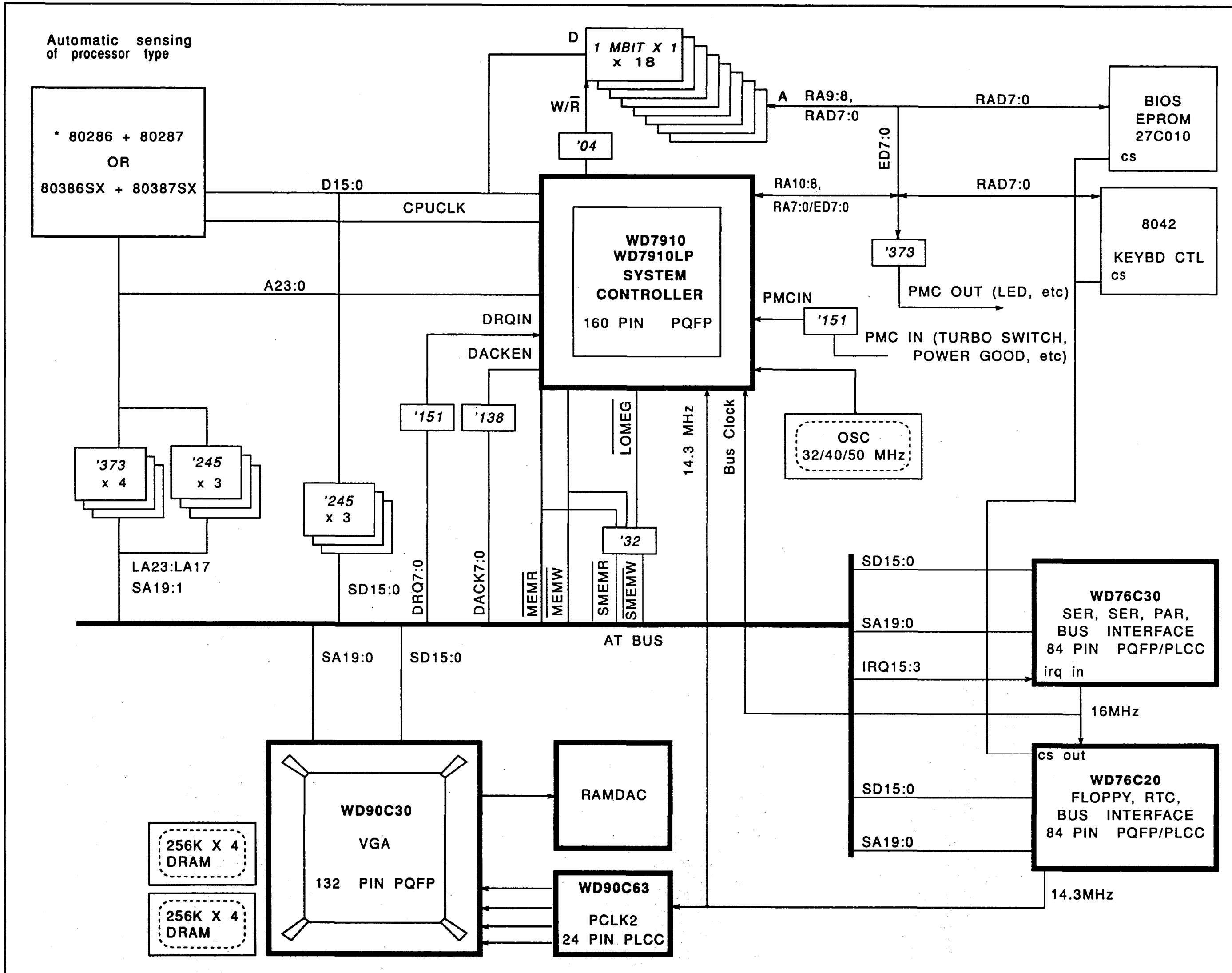

FIGURE 1-1. SYSTEM BLOCK DIAGRAM FOR DESKTOP

2.0 ARCHITECTURE

All versions of the System Controller are comprised of eight major blocks:

- Initialization and clocking
- AT bus
- 80286/80387SX processor control
- 80287/80387SX numeric processor control
- Data bus
- Memory and EMS control
- Power Management Control (WD7910LP only)
- Register File
- Video Local Bus Interface (VLBI) control
- Cache control

Sections 2.1 through 2.10 provide an overview of these blocks and are described in more detail in sections 4 through 11.

2.1 INITIALIZATION AND CLOCKING

At power up, the System Controller receives the $\overline{\text{RSTIN}}$ signal, which it uses to reset the AT bus and assert CPURES and NPRST to reset the main and numeric processors. The processor and AT bus resets are held for 84 processor clocks beyond the removal of the $\overline{\text{RSTIN}}$ signal. It is at this time that the type of processor in use (80286, 80287 or 80386SX, 80387SX) is determined by examining the $\overline{\text{S1}}$[W/R#] signal.

CLK14 is a 14.318 MHz clock for the 8254 compatible timers and is switched by the WD76C20 to 32 KHz during a suspend and resume operation.

BCLK2 is used to generate an 8 MHz or 10 MHz bus clock and may also be used as the source for the main processor clock, CPUCLK.

2.2 AT BUS

The AT bus provides the logic necessary to control the system clock, memory read and write access, I/O read and write cycles, data bus direction, data and interrupt requests and speaker driver.

2.3 MAIN PROCESSOR CONTROL

At the termination of reset, this block determines whether the local processor is an 80286 or 80386SX by examining the $\overline{\text{S1}}$[W/R#] signal. This block also controls whether the CPUCLK is to be an input or output. While both devices have the ability to reduce the processor clock rate, only the WD7910LP has the ability to stop the clock to the processor. The WD7910LP also has the ability to power down the processor, at which time it tristates the CPUCLK, $\overline{\text{READY}}$, HOLD, INTRQ and NMI signals.

2.4 NUMERIC PROCESSOR CONTROL

Both System Controllers support an 80287 or 80387SX processor.

2.5 DATA BUS

The Data Bus is a 16-bit (two bytes) bidirectional bus that connects to the processor's, System Controller, DRAM, and to AT data bus transceivers. The parity of each DRAM byte is indicated by DPL and DPH.

2.6 MEMORY AND EMS CONTROL

This block controls the access to 16 Mbytes of real memory or 32 Mbytes of expanded memory. Both versions of the System Controller supports non-page mode memory and independent two-way interleave page mode access to the DRAM banks.

2.7 POWER MANAGEMENT CONTROL

The Power Management Control (PMC) is internal logic which interfaces with external multiplexers and latches. Only the WD7910LP makes full use of the PMC. It has the ability to power down only the main processor or the main processor and peripherals, conserving power essential to portable notebook/laptop computers. When in a power down state, the WD7910LP tristates the CPUCLK, READY, HOLD, INTRQ and NMI output signals to the main processor. Also contained within this functional block are the SMI and SAM logic.

2.8 REGISTER FILE

The register file provides software control of the interface signals. The function of each register is described in the same section as the logic block which it controls. Some registers, such as the Bus Timing and Power Down Control Register at Port 1872H, serve more than one area. In this instance the register description appears only in one section but is referred to in all appropriate sections.

The registers, and the section in which they are described, are listed in Table 2-1.

In most cases, the registers are addressed by all 16 address bits, A15 through A00. Within the text, when the address is expressed as a three digit number, i.e., 092H - ALT A20 GATE and HOT RESET, only address bits A09 through A00 are used, A15 through A10 are ignored. If the address is expressed as a four digit number, all 16 address bits are used.

With the exception of the EMS Registers at port E072H and E872H and Port 70H Shadow Register at E472H, all registers located at Ports 1072H through FC72H are locked and inaccessible until unlocked by performing an eight bit I/O write of DA to the Lock/Unlock Register at Port F073H. Writing anything other than DA locks the registers. The lock/unlock status can be determined by reading the Lock/Unlock Status Register at Port FC72H twice. If the T bit (bit 15) toggles, the registers are unlocked. If the registers are locked, the read cycle is directed to the AT bus, and the data is undetermined.

2.8.1 Lock Status Register

Port Address FC72H - Read only

Bits 11 through 03 are particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board devices.

15	14	13	12	11	10	09	08
T	Not Used			DMA #2			
				CH3	CH2	CH1	CH0

07	06	05	04	03	02	01	00
DMA #1				P4	Not Used		
CH3	CH2	CH1	CH0				

Signal Name	Default At RSTIN
All signals	None

Bit 15 - T, Toggle

Changes state after every read of this port.

Bits 14-12 - Not used, state is ignored

Bits 11-08 - DMA #2, Channel Enable

This field represents the state of the Enable Bit (Mask) for channels 3 through 0 of DMA Controller #2. For a description of the Mask Registers, refer to section 5.4.11.

1 = Channel enabled

0 = Channel disabled

Bits 07-04 - DMA #1, Channel Enable

This field represents the state of the Enable Bit (Mask) for channels 3 through 0 of DMA Controller #1. For a description of the Mask Registers, refer to section 5.4.11.

1 = Channel enabled

0 = Channel disabled

Bit 03 - P, Parallel Port Direction

The P bit represents the state of the Direction Bit (bit 5) of the parallel port Write Control Register. For a description of this bit, refer to the WD76C30 Data Book, section 4.3

Bits 02-00 - Not used, state is ignored

2.8.2 Lock/Unlock Register

Port Address F073H - Write only

15	14	13	12	11	10	09	08
Not Used							

07	06	-5	04	03	02	01	00
L/UL = DA-							

Signal Name	Default At RSTIN
All signals	None

Bits 15-08 - Not used, state is ignored

Bits 07-00 - L/UL, Lock/Unlock

L/UL = DA -

11011010 unlocks the registers, allowing read and write access to the registers. Refer to Table 2-1 for the registers capable of being locked.

L/UL ≠ DA -

Anything other than 11011010 locks the registers. Any attempt to access a locked register I/O port address goes to the AT bus rather than the locked register.

2.9 VLBI Control

The Video Local Bus Interface (VLBI) control is internal logic which interfaces with the WD90C56 VLBI controller. It has the ability to determine whether the current CPU cycle should be processed by the WD90C56 or the WD7910LP.

2.10 Cache Control

This functional block contains the 8Kbyte integrated cache (both tag and data RAM) as well as cache control logic.

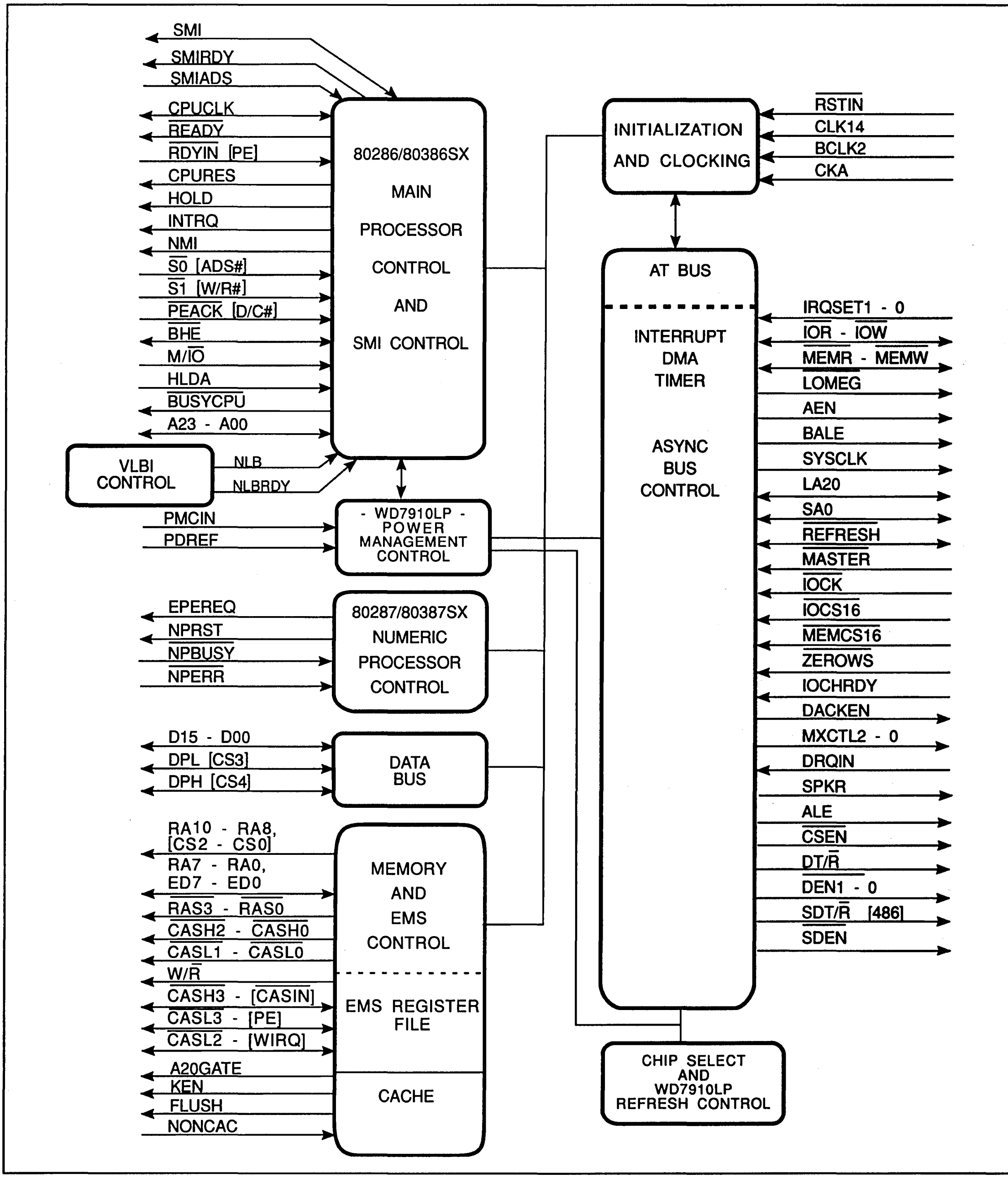

FIGURE 2-1. WD7910 AND WD7910LP BLOCK DIAGRAM

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PORT ADDRESS (HEX)	REGISTER NAME	LOCK/ UNLOCK	SECTION
000 - 00F ①	DMA Control #1 (Channel 0:3)	No	5.4, 5.6,
020 - 021 ②	Interrupt Controller #1	No	5.5
040	Timer 0, Time Of Day	No	5.7
041	Timer 1, Refresh	No	5.7
042	Timer 2, Speaker	No	5.7
043	Control Word	No	5.7
060 - 06E even	Keyboard Controller	No	8.5, Table 8-1
061 - 06F odd	Port B Parity Error And I/O Channel Check	No	5.9
070 - 07E even	Real-Time Clock Address Register	No	5.8.1
071 - 07F odd	Real-Time Clock Data Register	No	5.8.2
080 - 09F	(except 092H) DMA Page Registers	No	5.6.4
092	ALT A20 Gate and Hot Reset	No	5.8.3
0A0 - 0A1 ②	Interrupt Control Slave #2	No	5.4, 5.6
0C0 - 0DE ①	DMA Control #2 (Channel 4:7)	No	5.4
00F0	Clear 287 Busy	No	5.3.2
00F1	Reset 287/387SX	No	5.3.3
1072	CPU Clock Control	Yes	4.2.4
1872	Bus Timing And Power Down Control	Yes	5.3.1
2072	Refresh Control, Serial And Parallel Chip Selects	Yes	8.1
2872	Chip Selects	Yes	8.2
3072	Programmable Chip Select Address	Yes	8.3
3872	Memory Control	Yes	6.2.1
3C72	DMA Shadow Register 1	Yes	9.14
4072	Non-page Mode DRAM Memory Timing	Yes	6.3.1
4472	DMA Shadow Register 2	Yes	9.14
4872	Bank 1 And Bank 0 Start Address	Yes	6.2.2
4C72	DMA Shadow Register 3	Yes	9.14
5072	Bank 3 And Bank 2 Start Address	Yes	6.2.2
5872	Split Start Address	Yes	6.2.3
5C72	Programmable CS2 and CS3 Control Register	Yes	10.11
6072	RAM Shadow And Write Protect	Yes	6.2.4
6472	Programmable CS2 Address Register	Yes	10.11
6872	EMS Control And Lower EMS Boundary	Yes	6.4.1
6C72	Programmable CS3 Address Register	Yes	10.13
7072	PMC Output Control 7:0	Yes	9.3
7472	DRAM Size and SMI RAM Register	Yes	10.14
7872	PMC Output Control 15:8	Yes	9.3
7C72	SMI I/O Trap Control Register	Yes	10.2
8072	PMC Timers	Yes	9.4
8872	PMC Inputs 7:0	Yes	9.5
8C72	I/O Data/Memory Address Capture Register Low	Yes	10.4
9072	NMI Status	Yes	9.7
9472	I/O Data/Memory Address Capture Register High	Yes	10.7
9872	Diagnostic	Yes	11.1
9C72	SMI I/O Timeout Control Register	Yes	10.5
A072	Delay Line	Yes	11.2

TABLE 2-1. REGISTER INDEX

PORT ADDRESS (HEX)	REGISTER NAME	LOCK/ UNLOCK	SECTION
A472	SMI I/O Timeout Count Register 1	Yes	10.8
A872	Test Enable	Yes	11.3
AC72	SMI I/O Timeout Count Register 2	Yes	10.9
B072	Activity Monitor Control	Yes	9.11
B872	DMA Control Shadow	Yes	5.4.15
C072	High Memory Write Protect Boundary	Yes	6.2.5
C872	PMC Interrupt Enables	Yes	9.6
D072	Serial/Parallel Shadow Register	Yes	9.8
D472	Interrupt Controller Shadow	Yes	9.9
D872	Activity Monitor Mask	Yes	9.12
DC72	Test Status	Yes	11.4
E072	EMS Page Register Pointer	No	6.4.2
E472	Port 70H Shadow	No	9.10
E872	EMS Page Register	No	6.4.3
F072	48 MHz Oscillator Disable	Yes	8.5, Table 8-1
F472	48 MHz Oscillator Enable	Yes	8.5, Table 8-1
F872	Cache Flush	Yes	8.4
FC72	Lock Status	Yes	2.8.1
F073	Lock/Unlock	No	2.8.2

① See Table 5-4. DMA Controller/Channel Function Map
② See Table 5-6. Interrupt Controller Function Map

TABLE 2-1. REGISTER INDEX (cont.)

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3.0 SIGNAL DESCRIPTION

The signals are listed according to their pin number in Table 3-1. The signals are grouped according to their application and described in Table 3-2.

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	CLK14	41	PDREF	81	DRQIN	121	CLKA
2	NPBUSY	42	PMCIN	82	IOCHRDY	122	CPUCLK
3	BLE	43	WNRDRAM	83	ZEROWS	123	BUSYCPU
4	A1	44	CASH0	84	IOCS16	124	NMI
5	NC	45	NC	85	A20GATE	125	NA
6	A20	46	CASL0	86	MEMCS16	126	INTRQ
7	A19	47	RAS0	87	SPKR	127	D0
8	A18	48	CASH1	88	SA0	128	D1
9	A17	49	CASL1	89	LA20	129	D2
10	NC	50	NC	90	KEN	130	VSS
11	A16	51	RAS1	91	MASTER	131	D3
12	A15	52	RA10	92	ALE	132	D4
13	A14	53	RA9	93	AEN	133	D5
14	A13	54	RA8	94	SDEN	134	D6
15	NC	55	NC	95	LBRDY	135	VSS
16	A12	56	VSS	96	SDTR	136	D7
17	A11	57	RA7	97	VCC	137	D8
18	VSS	58	RA6	98	REFRESH	138	D9
19	VSS	59	VSS	99	VSS	139	D10
20	RA11	60	NC	100	LB	140	NC
21	A10	61	RA5	101	EPEREQ	141	VSS
22	VCC	62	VCC	102	PRST	142	D11
23	A9	63	RA4	103	LOMEG	143	VCC
24	A8	64	RA3	104	MEMW	144	D12
25	NONCAC	65	NC	105	SMI	145	NC
26	A7	66	VSS	106	MEMR	146	D13
27	A6	67	RA2	107	IOW	147	D14
28	A5	68	RA1	108	IOR	148	D15
29	A4	69	RA0	109	BHE	149	DTR
30	FLUSH	70	NC	110	SMIRDY	150	VSS
31	A3	71	CASH2	111	NPERR	151	DEN1
32	A2	72	CASL2	112	DNC	152	DEN0
33	IRQSET1	73	RAS2	113	MIO	153	SYSCLK
34	IRQSET0	74	CASH3	114	ADS	154	CPURES
35	MXCTL0	75	CASL3	115	SMIADS	155	BALE
36	NC	76	NC	116	WNR	156	NC
37	MXCTL1	77	RAS3	117	READY	157	A23
38	MXCTL2	78	DPH	118	HLDA	158	A22
39	CSEN	79	DPL	119	HOLD	159	A21
40	DACKEN	80	RSTIN	120	BCLK2	160	IOCK

TABLE 3-1. PIN ASSIGNMENTS

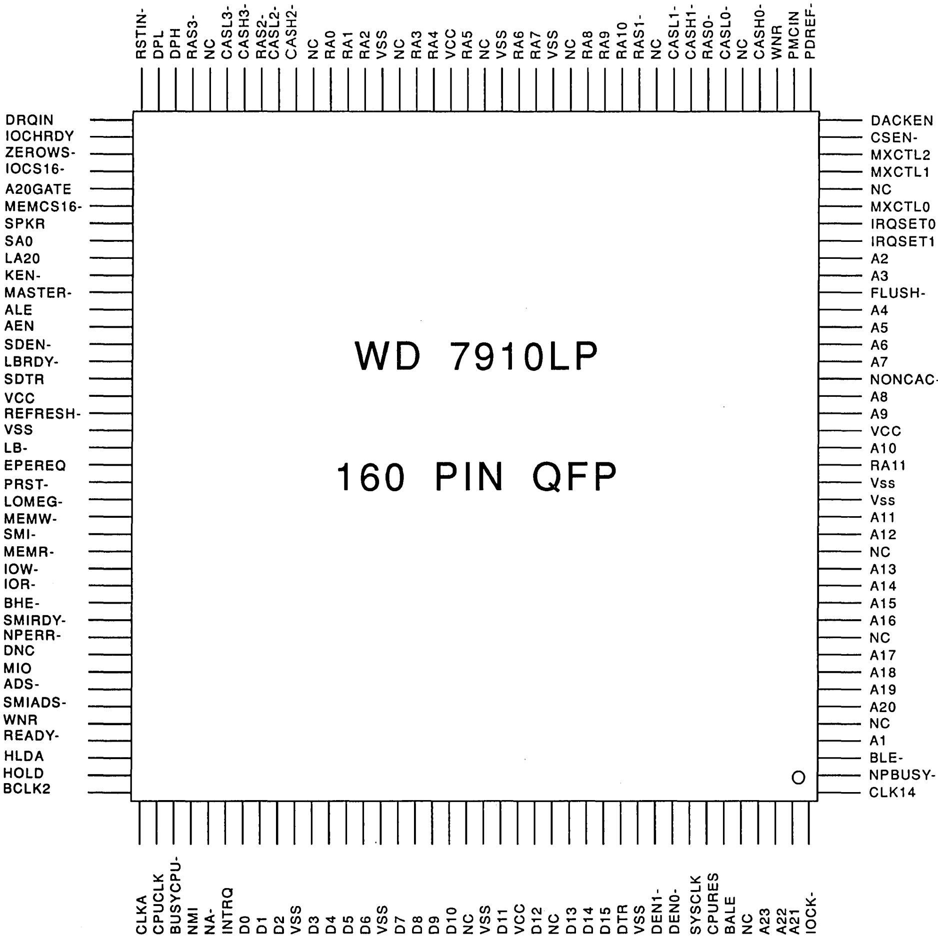

FIGURE 3-1. WD7910 PINOUT DIAGRAM

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PIN	MNEMONIC	I/O	DESCRIPTION
INITIALIZATION AND CLOCKING			
1	CLK14	I	**Clock 14** CLK14 is derived from a 14.318 MHz crystal and is used internally for the 8254 compatible timers. CLK14 is externally switched to 32 KHz during a suspend and resume.
80	RSTIN	I	**System Reset In** RSTIN drives a CMOS input level Schmitt Trigger and is used to reset the entire system at powerup. For a detailed description, see Section 4, Initialization and Clocking.
120	BCLK2	I	**Bus Clock** BCLK2 is used to generate an 8 MHz or 10 MHz expansion bus clock. For an 8 MHz bus, BCLK2 is a 16 MHz or 32 MHz input signal. For a 10 MHz bus clock, BCLK2 is a 20 or 40 MHz input signal. BCLK2 may also be used to drive the processor clock.
121	CLKA	I	**Clock A** Source for CPU clock.
AT BUS			
33	IRQSET1	I	**Interrupt Request Set 1** IRQSET1, along with MXCTL2 - 0, selects one of the of the following: A20GT, IRQ1, IRQ3 - IRQ7, IRQ12. Refer to Table 5-1 and Figure 5-1.
34	IRQSET0	I	**Interrupt Request Set 0** IRQSET0, along with MXCTL2 - 0, selects one of the following: ROM8, RESCPU, IRQ8, IRQ9 - IRQ11, IRQ14 and IRQ15. Refer to Table 5-1 and Figure 5-1.
35, 37, 38	MXCTL2:0	O	**Multiplexer Control 2-0** MXCTL2 - MXCTL0, along with DRQIN, DACKEN, IRQSET1, IRQSET0 and PMCIN, control the external multiplexer for the selection of DRQs, DACKs, IRQs, ROM8, A20GT and RESCPU. Refer to Table 5-1 and Figure 5-1.
39	CSEN	O	**Chip Select Enable** When CSEN is asserted, DPH, DPL, and RA10-RA8 are used to generate one of 28 different chip selects. Refer to Table 8-1.
40	DACKEN	O	**DACK Enable** When DACKEN is asserted, MXCTL2-0 are used to generate DACK7-5, 3-0 and BUS_RST. Refer to Table 5-1 and Figure 5-1.
81	DRQIN	I	**Multiplexed DRQ Inputs** DRQIN, along with MXCTL2 - 0, selects one of the DRQs or CLOCK_DIR_IN. Refer to Table 5-1 and Figure 5-1
82	IOCHRDY	I/O	**I/O Channel Ready** Indicates extra wait states are required for the AT bus cycles.

TABLE 3-2. SIGNAL DESCRIPTION

PIN	MNEMONIC	I/O	DESCRIPTION
83	$\overline{\text{ZEROWS}}$	I	**Zero Wait States** Indicates the current AT bus cycle can be finished in zero wait state.
84	$\overline{\text{IOCS16}}$	I	**16-Bit I/O Cycle** Inicates the I/O device on the AT bus is a 16-bit slave.
86	$\overline{\text{MEMCS16}}$	I	**16-Bit Memory Cycle** Indicates that the memory device on the AT bus is a 16-bit slave.
87	SPKR	O	**Speaker** SPKR drives the speaker transistor.
88	SA0	I/O	**System Address 0** When not in Master Mode, SA0 is an output and is asserted by the System Controller to place address 00 on the AT Bus SA0 line.When in Master Mode, SA0 is an input and is asserted by the Bus Master to place address on A0.
89	LA20	I/O	**Early Address 20** When not in Master Mode, LA20 is an output and is asserted by the System Controller to place address 20 on the AT Bus LA20 line. When in Master Mode, LA20 is an input and is asserted by the Bus Master to place address on A20.
91	$\overline{\text{MASTER}}$	I	**Master** $\overline{\text{MASTER}}$ is asserted by the Bus Master to indicate that a Bus Master cycle is occurring. This causes LA20, SA0, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$, and $\overline{\text{IOW}}$ to be selected as input signals.
92	ALE	O	**Address Latch Enable** ALE is used to clock the SA1 - SA19 address latches.
93	AEN	O	**Address Enable** AEN is asserted by the System Controller while performing DMA and Refresh cycles.
94	$\overline{\text{SDEN}}$	O	**Swap Data Enable** $\overline{\text{SDEN}}$ enables the data transfer between high and low bytes of the AT Bus.
96	SDT/$\overline{\text{R}}$	I/O	**Swap Data Transmit/Receive** SDT/$\overline{\text{R}}$ controls the direction of the buffer between the low byte and high byte of the AT bus. SDT/$\overline{\text{R}}$ is tristated by a 50K pullup resistor internal to the WD7910 when $\overline{\text{RSTIN}}$ at pin 80 is low. **SDT/$\overline{\text{R}}$ Mode - Output** When SDT/$\overline{\text{R}}$ is high, it directs data from the low byte of the AT Bus to the high byte. When SDT/$\overline{\text{R}}$ is low, it directs data from the high byte of the AT bus to the low byte. Forcing SDT/$\overline{\text{R}}$ high while $\overline{\text{RSTIN}}$ is low selects the SDT/$\overline{\text{R}}$ mode. Holding SDT/R high as $\overline{\text{RSTIN}}$ goes high maintains the SDT/$\overline{\text{R}}$ mode.

TABLE 3-2. SIGNAL DESCRIPTION (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
98	REFRESH	I/O	**Refresh** As an output, REFRESH is asserted by the System Controller to refresh memory on the AT Bus. As an input, REFRESH is asserted by the Bus Master in conjunction with MEMR to refresh memory on the AT Bus and DRAM controlled by the System Controller.
103	LOMEG	O	**First Megabyte** LOMEG is asserted when the AT bus address is below 1 Mbyte.
104	MEMW	I/O	**Memory Write** MEMW is an output and it is asserted by the System Controller when a memory write access to the AT bus is to take place. It is an input during Master mode.
106	MEMR	I/O	**Memory Read** MEMR is an output and it is asserted by the System Controller when a memory read access to the AT bus is to take place. It is an input during Master mode.
107	IOW	I/O	**I/O Write** IOW is an output and it is asserted by the System Controller during processor or DMA access to indicate that an I/O write operation is to take place on the AT bus. IOW is an input during Master Mode.
108	IOR	I/O	**I/O Read** IOR is an output and iit s asserted by the System Controller during processor or DMA access to indicate that an I/O read operation is to take place on the AT bus. IOR is an input during Master Mode.
149	DT/R	O	**Data Transmit/Receive** DT/R controls the direction of the AT Data Bus D00 through D15. When DT/R is high, data is directed to the AT Bus. When DT/R is low, data is transferred from the AT bus.
151	DEN1	O	**Data Bus Enable 1** When asserted, DEN1 enables the high order byte data buffer.
152	DEN0	O	**Data Bus Enable 0** When asserted, DEN0 enables the low order byte data buffer.
153	SYSCLK	O	**System Clock** In asynchronous bus mode, SYSCLK is equal to BCLK2 divided by two when BCLK2 is less than 28 MHz, and divided by four when BCLK2 is greater than 28 MHz. In synchronous bus mode, SYSCLK is equal to CPUCLK divided by two or four, depending on the programming.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
155	BALE	O	**AT Bus Address Latch Enable** Address Latch Enable for the AT bus. BALE is synchronous with the Bus Clock (BCLK2).
160	$\overline{IOCK}$	I	**I/O Channel Check** When asserted, $\overline{IOCK}$ indicates a bus or memory error is on the AT bus and generates an NMI to the processor.
			MAIN PROCESSOR CONTROL
95	LBRDY	I	**Local Bus Ready** Local bus cycle ready signal
100	$\overline{LB}$	I	**Local Bus** Local bus cycle request signal
105	$\overline{SMI}$	I/O	**SMI Request** SMI request to the processor.
109	$\overline{BHE}$	I/O	**Bus High Enable** As an input, $\overline{BHE}$ indicates a transfer of the high byte on the processor data bus. $\overline{BHE}$ is an output during DMA transfers.
110	$\overline{SMIRDY}$	O	**SMI Ready** SMI Ready signal to the processor
112	DNC	I	Processor DNC signal.
113	M/IO	I	**Memory or I/O** Processor Memory cycle or $\overline{I/O}$ Status cycle.
114	$\overline{ADS}$	I	$\overline{ADS}$ signal from the processor.
115	$\overline{SMIADS}$	I	**SMI Address** $\overline{SMIADS}$ signal from the processor.
116	W/$\overline{NR}$	I	When W/$\overline{NR}$ is high, a write to memory occurs; when low, a read from memory occurs.
117	$\overline{READY}$	O	**Processor Ready** $\overline{READY}$ is an output to the processor
118	HLDA	I	**Hold Acknowledge** Processor hold acknowledge.
119	HOLD	O	**Hold Request** Processor hold cycle request.
122	CPUCLK	I/O	**Processor Clock** CPUCLK speed and whether it is to be an input or output, is selected by the CPU Clock Control Register at Port Address 1072H. It is normally selected as an output to drive the processor but may be selected as an input from an external processor clock driver.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
124	NMI	O	**Non-maskable Interrupt** Processor non-maskable interrupt cycle request.
125	$\overline{NA}$	O	**Next Address** Next address request to the processor.
126	INTRQ	O	**Interrupt Request** Processor interrupt cycle request.
154	CPURES	O	**Main Processor Reset** CPURES is a synchronous processor reset signal.
157-159, 6-9, 11-14, 16, 17, 21, 23, 24, 26-29, 31, 32, 4, 3	A23:1, $\overline{BLE}$	I/O	**Processor Address A23-A00[$\overline{BLE}$]** A23 through A1 are address lines from the 80286 or 80386SX.
NUMERIC PROCESSOR CONTROL			
2	$\overline{NPBUSY}$	I	**Numeric Processor Busy** Busy signal from the numeric processor 80287 or 80387SX.
101	EPERQ	O	**Extend PERQ** PERQ extend signal to the 80386SX for IRQ13 handling. Used only for the 80386SX.
102	NPRST	O	**Numeric Processor Reset** Reset to the numeric processor 80287 or 80387SX.
111	$\overline{NPERR}$	I	**Numeric Processor Error** Error signal from the numeric processor 80287 or 80387SX.
123	$\overline{BUSYCPU}$	O	**Coprocessor Busy** Coprocessor Busy signal to the processor.
DATA BUS			
78	DPH[CS4]	I/O	**Data Parity High Byte [Chip Select 4]** For DRAM cycles, DPH is the high byte parity bit. For I/O cycle, CS4 is bit four of the encoded chip select bus.
79	DPL[CS3]	I/O	**Data Parity Low Byte [Chip Select 3]** For DRAM cycles, DPL is the low byte parity bit. For I/O cycle, CS3 is bit three of the encoded chip select bus.

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
148-146, 144, 142, 139-136, 134-131, 129-127	D15-D13 D12, D11, D10-D7 D6-D3 D2-D0	I/O	**Data Bits 15 through 0** The Data Bits are connected directly to the Local and Numeric processors, DRAM data and AT Bus data transceivers.
			MEMORY AND EMS CONTROL
25	NONCAC	I	**Noncacheable** External noncacheable signal.
30	FLUSH	O	**Flush** Flush signal to external cache controller.
43	NWR	O	**Write Not Read** Write Not Read signal to DRAM.
20 52 53 54	RA11 RA10/CS2 RA9/CS1 RA8/CS0	O	**DRAM Address Bits 11 through 8** **Chip Select Bits 2 through 0** The DRAM Address Bus is multi-functional. During DRAM cycles, RA11 through RA0 select the DRAM row and column.
57 58 61 63 64 67 68 69	RA7/ED7 RA6/ED6 RA5/ED5 RA4/ED4 RA3/ED3 RA2/ED2 RA1/ED1 RA0/ED0	I/O	**DRAM Address Bits 7 through 0** **EDATA Bits 7 through 0** During I/O cycles, CS2 through CS0, along with CS4 and CS3, are decoded by external logic to one of 32 possible Chip Selects. ED7 through ED0 represents the data from such devices as the Keyboard Controller on the EDATA bus.
77 73 51 47	RAS3 thru RAS0	O	**Row Address Select Bits 3 through 0** RAS3 through RAS0 are designed to access the DRAM without the use of external drivers.
74	CASH3 [CASIN]	I/O	CASH3 [CASIN] is tristated by a 50K pullup resistor internal to the WD76C10A when RSTIN at pin 17 is low.
71 48 44	CASH2 CASH1 CASH0	O O O	**CAS Output Mode** CASH3 through CASH0 operate as output signals and are designed to accessthe DRAM without the use of external drivers. Forcing CASH3[CASIN] high while RSTIN is low, selects the CASH3 Output Mode. Holding CASH3[CASIN] high as RSTIN goes high, maintains the CASH3 Output Mode.
75 72 49 46	CASL3 thru CASL0	O	**Column Address Select Low 3 through 0** CASL3 through CASL0 are designed to access the DRAM without the use of external drivers.
85	A20GATE	O	**A20 Gate** A20 Gate signal to external cache controller

TABL 3-2. SIGNAL DESCRIPTIONS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
90	$\overline{KEN}$	O	**Cache Enable** Noncacheable signal to external cache controller.
			POWER MANAGEMENT CONTROL
41	NPDREF	I	**Power-down Refresh** NPDREF is a 64 KHz signal from the WD7910. During power-down, NPDREF is passed internally to pin 98 ($\overline{REFRESH}$).
42	PMCIN	I	**Power Management Control Input** PMCIN is used to sample eight PMC inputs. See Table 5-1 and Figure 5-1.
			MISCELLANEOUS
18, 19, 56, 59, 66, 99, 141	VSS	I	**Ground**
22, 62, 97, 143	VCC	I	**+5 Volts**

TABLE 3-2. SIGNAL DESCRIPTIONS (Continued)

4.0 INITIALIZATION AND CLOCKING

This section describes the system Master Reset (RSTIN) operation, control of internal clock (CLK14), bus clock (SYSCLK) and the processor clock (CPUCLK).

4.1 POWER UP RESET

The system reset signal, NRSTIN, is generated externally at power up and is used to reset the entire system. When asserted, the System Controller outputs the CPURES signal to reset the Main Processor. At this time the System Controller also resets the AT bus by asserting DACKEN and MXCTL2-0 = 100, which are decoded externally as BUS_RST (DACK4), see sections 5.1, 5.1.1, Table 5-1 and Figure 5-1. An external RC circuit can be used to extend the time that RSTIN is asserted until the power supply reaches a proper level. CPURES and the AT bus reset signals are de-asserted 84 clock pulses after RSTIN reaches its switching threshold. It is during the reset period that the type of processor is detected by examining the state of the S1 signal. If S1 is asserted, the System Controller enters the 80386SX mode. If S1 is de-asserted, it enters the 80286 mode. If an 80386SX has been detected, BUSYCPU is asserted so that the processor may perform its self-test operation immediately following the power up reset.

4.2 CLOCKING

The System Controller makes use of five clocks, CLK14, BCLK2, CPUCLK, CKA and SYSCLK. Figure 4-1 shows how the clocks interact with each other and the register used to select the clock and speed.

4.2.1 Internal Clock (CLK14)

CLK14 is an input signal from a 14.318 MHz crystal and is used for the control of the 8254 compatible timers. CLK14 is switched by the WD7910 to 32 KHz during save and resume operations.

4.2.2 System Bus Clock (SYSCLK)

The AT bus is driven by the SYSCLK, which is derived from either the BCLK2 or CPUCLK, as selected by the Bus Timing Register at Port Address 1872H. SYSCLK is always one half or one fourth the value of the selected input clock (refer to Figure 4-1).

4.2.3 Processor Clock (CPUCLK)

The processor clock may be an output or input, depending on whether the System Controller generates CPUCLK or an external oscillator is used. At speeds higher than 50 MHz, CPUCLK may need to be generated by an external oscillator, making it possible to control the processor duty cycle more closely. At lower speeds, the System Controller may use BCLK2 to generate CPUCLK or, in a system without discrete cache, the System Controller may use CKA to generate CPUCLK.

During reset, CPUCLK is an output.

If the CPUCLK is initially placed in the input mode, it may be changed to the output mode by writing to the PMC Control Register at Port Address 7872H. The PMC control output 0 tristates the external clock oscillator. A processor reset (CPURES) is automatically generated during the clock switching process.

When the CPUCLK is an output, it may be stopped by SCHH or SCH (CPU Clock Control Register - bits 01 or 00, at Port Address 1072H) or divided down by CLK_SPD (bits 14-12). Only the WD7910LP supports the CPUCLK stop function. When CPUCLK is stopped, it is in phase two of the 80C286. CPUCLK is restarted by an NMI or IRQ interrupt, qualified by the normal NMI and IRQ masking circuitry or by an NMI generated PMC logic.

There are two methods for slowing the processor execution rate to provide software compatibility with programs expecting a particular CPU speed, such as game software. One method is to divide the CPUCLK by a factor of 2, 4 or 8. Dividing the clock rate may also have an effect on the CPU power consumption, so CLK_SPD also provides some choices of clock duty cycle. The other method can be used when the CPUCLK is an

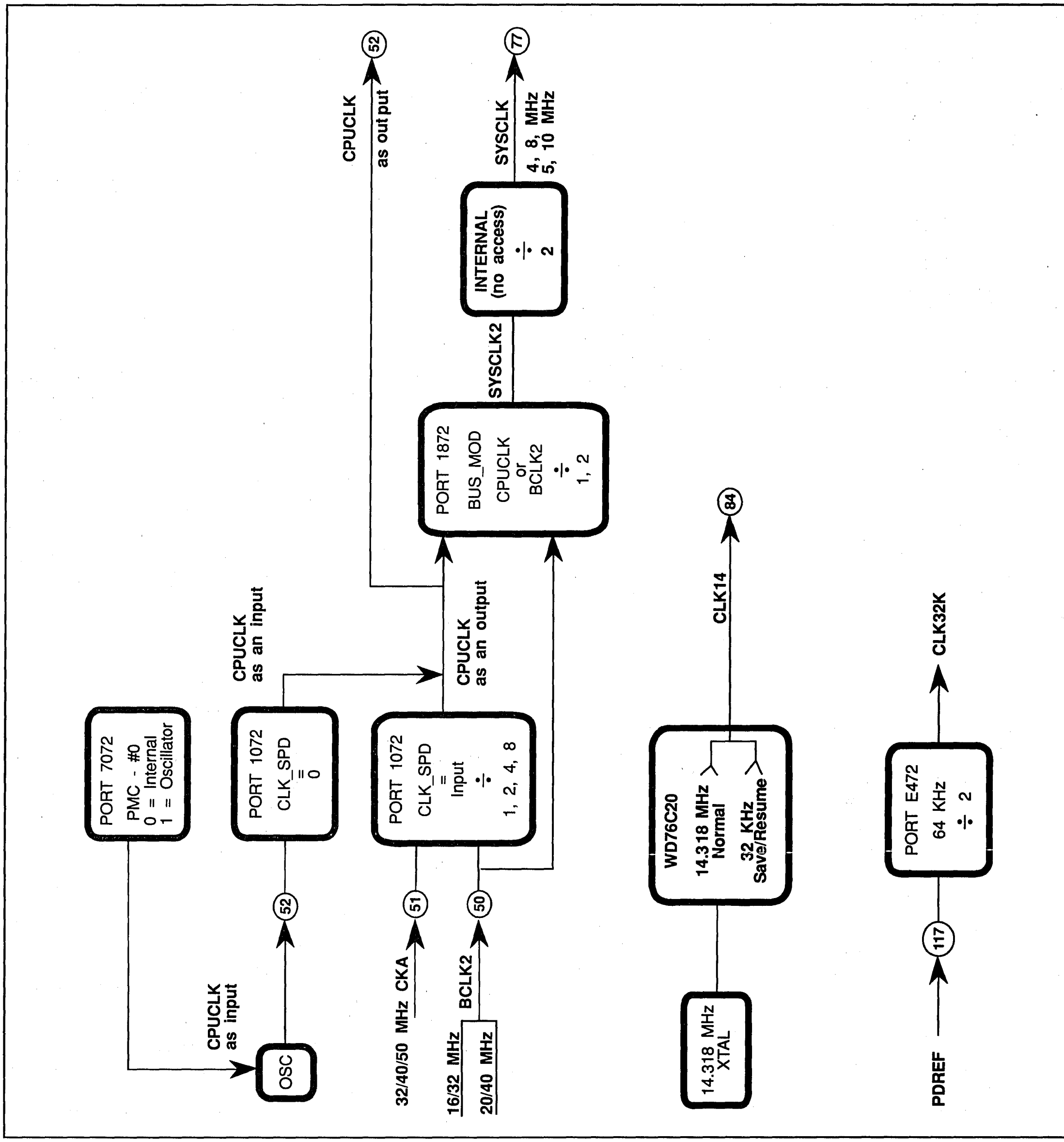

FIGURE 4-1. CLOCK CONTROL

output or input and generated by an external oscillator. In this case, EXT_HOLD is used to extend the hold request time to the processor after every refresh.

In a system without a cache or external memory controller, pin 51 can be defined as Clock A (CKA) and used in place of the BCLK2. This choice is determined by SRC (CPU Clock Control Register bit 15 at Port Address 1072H). SRC is set automatically at power up reset, if a clock source is present at pin 51 (CKA).

4.2.4 CPU Clock (CPUCLK) Control Register

Port Address 1072H - Read and Write

15	14	13	12	11	10	09	08
SRC	CLK_SPD			AUT_ FST	ALT_CLK_SPD		

07	06	05	04	03	02	01	00
EXT_HOLD						SCHH	SCH

Signal Name	Default At RSTIN
SRC	0/1
CLK_SPD	000/001
AUT FST †	0
ALT CLK SPD †	000
EXTEND HOLD	0000
Bits 03, 02	None
SCH †	0
SCHH †	0

† Featured only in the WD7910LP

Bit 15 - SRC, CPUCLK Clock Source

When CPUCLK is selected as an output by bits 14 - 12, SRC determines whether it is to be driven by BCLK2 or CKA.

Default Value

SRC is set to 0 and BLCK2 is used as the CPUCLK clock source if CKA does not change state within 64 clocks after RSTIN is de-asserted.

SRC is set to 1 and CKA is used as the CPUCLK clock source if CKA changes state within 64 clocks after RSTIN is de-asserted, or when operating in the 80486 Mode. The 80486 Mode is selected by holding SDT/R low during RSTIN transition from low to high.

SRC = 0 -
BCK2 is the CPUCLK source.

SRC = 1 -
CKA is the CPUCLK source.

Bits 14-12 - CLK_SPD, CPUCLK Clock Speed

CLK_SPD determines whether CPUCLK is to be an input or output. When selecting CPUCLK as an output, CLK_SPD also determines the divisor and duty cycle values. The CLK_SPD *defaults to 000 or 001 at power up. Changing the CPUCLK from an input (CLK_SPD = 000) to an output automatically asserts the processor reset (CPURES) and the CPUCLK Driver Enable from the PMC latch is forced low, tristating the external clock oscillator. One millesecond later, CPUCLK becomes active as an output. One millesecond and 16 CPUCLK clocks (or one millesecond) later, the CPURES is de-asserted. This method allows switching the clock source while tolerating glitches in the CPUCLK, generated due to the clock driver not being able to synchronously switch the clock. The one millesecond and 16 clocks or one millesecond selection is made through the Diagnostic Register at Port 9872H.

CLK_SPD
14 13 12

- 0 0 0 - CPUCLK pin is an input, speed determined by external driving source (* Default value).
- 0 0 1 - CPUCLK pin is an output, source divided by 1 (* Default value).
- 0 1 0 - OUT, source divided by 2.
- 0 1 1 - OUT, source divided by 4, 25% duty cycle.
- 1 0 0 - OUT, source divided by 4, 75% duty cycle.
- 1 0 1 - OUT, source divided by 8, 12% duty cycle.
- 1 1 0 - OUT, source divided by 8, 88% duty cycle.

* Based upon the value of CLOCK_DIR_IN at power up (refer to Table 5-1, Figure 5-1 and section 5.1.2).

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Bit 11 - AUT_FST, Automatic Processor Clock Speed Switching
Featured only in the WD7910LP

When automatic CPUCLK switching is enabled, the processor clock is switched between high and low clock speeds, depending upon activity. If the external TURBO signal is de-asserted when auto switching is enabled, the CPUCLK is normally at the alternate clock or slower rate. When speedup activity occurs, the clock speed switches to the nominal clock rate, normally the higher, for a period of time determined by Table 4-2. When no further activity occurs, the clock speed switches back down to the alternate speed. If the external TURBO signal is asserted, the clock rate is set to the nominal clock rate specified by the CLK_SPD field.

A halt state also causes the clock rate to slow, unless the SCHH or SCH field is programmed to stop the clock. The clock restarts or returns to the faster rate when any interrupt occurs.

Table 4-2 shows the activity that triggers a higher clock rate.

AUT_FST = 0 -
Automatic Clock Switching is disabled. TURBO determines whether CLK_SPD or ALT_CLK_SPD is to be used as the CPU clock. Refer to Table 4-1 for the appropriate selection, as determined by TURBO.

AUT_FST = 1 -
Automatic CPUCLK Switching between CLK_SPD and ALT_CLK_SPD is enabled when TURBO is de-asserted. CLK_SPD is selected when TURBO is asserted. Refer to Table 4-1. The EXT_HOLD field must be 0000 when AUT_FST = 1.

TURBO	AUTO_FST	CPU CLOCK SPEED
0	0	CLK_SPD
0	1	CLK_SPD
1	0	ALT_CLK_SPD
1	1	CLK_SPD or ALT_CLK_SPD

TABLE 4-1. CLOCK SWITCH SELECTION

SPEEDUP ACTIVITY	TIME PERIOD
Hard disk interrupt, Hard disk or numeric processor I/O, SCSI, floppy, port B I/O	1 second
Keyboard interrupt	1 second or until next video access
Video access or processor reset	1 millisecond
Any NMI or IRQ interrupt, except keyboard or hard disk	1 millisecond

TABLE 4-2. SPEEDUP ACTIVITY

Bits 10-08 - ALT_CLK_SPD, Alternate Clock Speed
Featured only in the WD76C10ALP

ALT_CLK_SPD
10 09 08

0 0 0 - CPUCLK unchanged from CLK_SPD (Default value).

0 0 1 - Equals source.

0 1 0 - Equals source div by 2.

0 1 1 - Equals source div by 4, 25% duty cycle.

1 0 0 - Equals source div by 4, 75% duty cycle.

1 0 1 - Equals source div by 8, 12% duty cycle.

1 1 0 - Equals source div by 8, 88% duty cycle.

Bits 07-04 - EXT_HOLD, Extend Processor Hold

Processor execution may be slowed for software compatibility by extending the processor hold request after refresh cycles. If the external TURBO signal is asserted, EXT_HOLD is forced to 0000. When the external TURBO signal is de-asserted, the EXT_HOLD returns to its programmed value, allowing an external TURBO switch to slow the processing speed.

EXT_HOLD
07 06 05 04

0 0 0 0 - No hold extension, (Default value).

0 0 0 1 - 1 μs hold after refresh.

0 0 1 0 - 2 μs hold after refresh.

0 0 1 1 - 3 μs hold after refresh.

0 1 0 0 - 4 μs hold after refresh.

↕

1 1 0 1 - 13 μs hold after refresh.

1 1 1 0 - 14 μs hold after refresh.

1 1 1 1 - 15 μs hold after refresh.

Bits 03-02 - Reserved for future use, must be set to zero

Bit 01 - SCHH, Stop CPUCLK at next Halt and Hold.
Featured only in the WD76C10ALP

SCHH is applicable only for 80C286 or Am386SXL type processors in which the clock may be stopped. This option should only be used when the clock source is the WD7910LP rather than an external oscillator.

Any unmasked processor interrupt, or NMI, restarts the CPUCLK. The SCHH bit remains set and the clock will be stopped again if a halt and hold condition is detected. The refresh rate may be as programmed by the Refresh Timer at Port Address 041H, or at the slower rate selected by the Refresh Control Register at Port 2072H.

SCHH = 0 -
Normal processor clock (default value).

SCHH = 1 -
Stop processor clock at next halt and hold cycle.

Bit 00 - SCH, Stop CPUCLK at next Hold
Featured only in the WD7910LP

SCH is applicable only for 80C286 or Am386SXL type processors in which the clock may be stopped. This option should only be used when the clock source is the WD7910LP instead of an external oscillator.

Any unmasked processor interrupt, or NMI, restarts the CPUCLK and sets the SCH bit to zero. DRAM refresh continues while the processor clock is stopped. The refresh rate may be as programmed by the Refresh Timer at Port Address 041H, or at the slower rate as selected by the Refresh Control Register at Port 2072H.

SCH = 0 -
Normal processor clock (Default value).

SCH = 1 -
Stop processor clock at next processor hold cycle.

5.0 AT BUS

This section describes the logic required to control the interrupts and timing between the AT bus and the System Controller.

5.1 INTERRUPT MULTIPLEXING

To reduce the number of pins required, the System Controller generates and outputs the MXCTL2-0 and DACKEN signals used by external logic to multiplex the DACKs, DRQs and IRQs down to single inputs. See Figure 5-1.

MXCTL2-0 are set to 100 during a System Reset (RSTIN) to provide a Bus Reset (BUS_RST), and to determine the ROM width (ROM8) and processor clock (CPUCLK) pin direction. See Table 5-1.

5.1.1 Data Acknowledge DACK7-5, 3-0

An external 74F138, 3 to 8 Decoder for desktop systems, or 74ACT138, 3 to 8 Decoder for laptop systems, uses MXCTL2-0 to generate the DACK7-5 and DACK3-0, which are applied to the AT bus. The unused combination develops the AT BUS_RST (bus reset). The decoder is enabled by the DACKEN signal from the System Controller.

5.1.2 Data Request DRQIN

The MXCTL2-0 signals are also used by an external 74F151, 8 to 1 Multiplexer for desktop systems, or 74ACT151, 8 to 1 Multiplexer for laptop systems, to develop the DRQIN signal received by the System Controller. The MXCLT2-0 signals are held stable during DMA transfers.

Immediately following a System Reset (RSTIN), DRQIN input 100 is sampled. If low, the processor clock (CPUCLK) pin is an output. If high, the CPUCLK starts as an output but is switched to an input shortly after RSTIN is de-asserted. See Table 5-1 and Figure 5-1. This controls the default value of CLK_SPD in the CPU Clock (CPUCLK) Control Register at Port 1072H. See section 4.2.4.

5.1.3 Interrupt Requests

The Interrupt Requests are multiplexed by the WD76C30. The multiplexing is performed as shown in Table 5-1 and Figure 5-1, and provides the System Controller with the IRQSET1 and IRQSET0 signals.

DRQIN, IRQSET1 and IRQSET0 are sampled by the System Controller at every rising edge of SYSCLK2. This allows all DMA, DRQ and IRQ lines to be sampled within 500 ns, when SYSCLK is 8 MHz.

The ROM8 input is sampled at the completion of a NRSTIN to determine ROM data width (ROM8). The RESCPU and A20GT inputs come from the 8042 keyboard controller.

5.1.4 AT Address Bus, Data Bus and Terminal Count (TC) Signal

The AT Address Bus SA19-00 and NBLE are generated from A19-00 with external latches and tristate buffers.

The AT Data Bus SD15-00 uses D15-00 and external bidirectional buffers.

The TC signal is generated by an external gate when DACKEN and CSEN are both asserted.

5.2 POWER MANAGEMENT CONTROL PMCIN

The power control signals are placed on the PMCIN input pin by way of an eight to one multiplexer, controlled by the MXCTL2-0 signals from the System Controller. In the WD7910, the TURBO signal may be connected directly to PMCIN. In the WD7910LP, the external 8:1 MUX is always used. See Figure 5-1. Bits 14 and 13 of Port 1872H (Section 5.3) control the power down of the processor and peripheral.

MXCTL 2 1 0	DRQIN	DACKEN	IRQSET0	IRQSET1	PMCIN
0 0 0	DRQ0	DACK0	$\overline{\text{IRQ8}}$	IRQ12	$\overline{\text{TURBO}}$
0 0 1	DRQ1	DACK1	IRQ9	IRQ1	PROC_PWR_GOOD
0 1 0	DRQ2	DACK2	IRQ10	A20GT	LCL_RQ or USER DEF.
0 1 1	DRQ3	DACK3	IRQ11	IRQ3	USER DEF.
1 0 0	CLOCK_ DIR_IN	BUS_RST	ROM8	IRQ4	USER DEF.
1 0 1	DRQ5	DACK5	$\overline{\text{RESCPU}}$	IRQ5	USER DEF.
1 1 0	DRQ6	DACK6	IRQ14	IRQ6	USER DEF.
1 1 1	DRQ7	DACK7	IRQ15	IRQ7	USER DEF.

TABLE 5-1. MXCTL2 - 0 DECODING

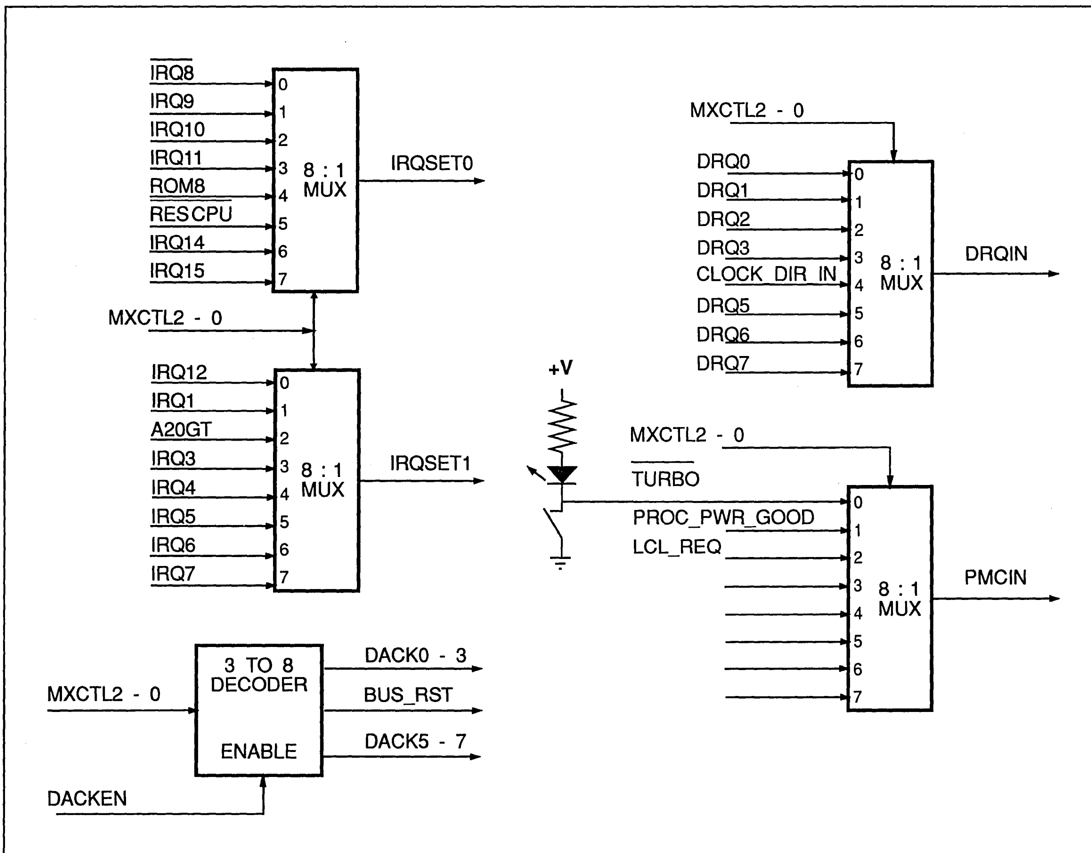

FIGURE 5-1. MXCTL2-0 MULTIPLEXING

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5.3 NUMERIC PROCESSOR

5.3.1 Numeric Processor Busy, Bus Timing, And Power Down Register

Port Address 1872H - Read and Write

15	14	13	12	11	10	09	08
NP_BSY	PRO_PD	FPD		BUS_MOD		BRQ_DEL	

07	06	05	04	03	02	01	00
BAK_DEL		WSI 16	WSM_16	WSI8		WSM8	

Signal Name	Default At NRSTIN
NP_BSY	0
PRO_PD †	0
Bit 12	None
FPD †	0
BUS_MOD	00
BRQ_DEL	00
BAK_DEL	11
WSI_16	0
WSM_16	0
WS18	10
WSM8	10

† Featured only in the WD7910LP

Bit 15 - NP_BSY, Numeric Processor Busy

NP_BSY must be set for systems using an 80286 CPU where the CPU runs faster than the AT bus. The causes BUSYCPU to be asserted early during any CPU write to I/O ports F8H through FFH. BUSYCPU is de-asserted at the end of the I/O write if the coprocessor has not asserted its own NPBUSY by this time. Early assertion of BUSYCPU is necessary to prevent a loss of synchronization between the 80286 and 80287. Bit 15 is ignored when an 80386SX is used.

NP_BSY = 0 -
Force an early BUSYCPU for I/O writes to coprocessor addresses F8H through FFH. (Default value).

NP_BSY = 1 -
Normal BUSYCPU assertion.

Bit 14 - PRO_PD, Processor Power Down
Featured only in the WD7910LP

When PRO_PD has been changed from zero to one, a power down sequence for the 80286 or 80386SX processor will be initiated at the next Halt State and the expansion bus will continue to operate normally. The processor should not be powered down if DMA cycles are likely to occur. When PRO_PD is set and a halt state occurs, the processor inputs are ignored and appear to the WD7910LP to be in the passive state.

The input buffers connected to the processor signals do not consume power even if the processor signals do not reach ground. The internal pullups on inputs connecting to the processor are disabled to reduce power. PMC output 5 from Port 7072H (Processor Power Down) is set. This can be used to control the power transistor and turn off the power to the processor. All outputs going to the processor will be tristated.

When an unmasked interrupt, DRQ or NMI occurs, PMC output 5 is reset, re-powering the processor. A voltage comparator should be used to generate a Processor Power Good (PPG) signal. The PPG signal is sampled by bit 01 of the PMC Input Register at Port Address 8872H. When PPG is high, the outputs to the processor are driven and the processor is reset.

PRO_PD = 0 -
Normal processor power (Default value).

PRO_PD = 1 -
Start processor power down sequence.

Bit 13 - FPD, Full Powerdown
Featured only in the WD7910LP

When FPD equals one and a halt state occurs, all processor and peripheral outputs except the PMC, DRAM controls and RA/ED bus are tristated and all inputs except NRSTIN, CLK14 and PMC inputs are ignored. CAS before RAS refresh will be performed if enabled by Port 2072H. All circuitry except the PMC and refresh timer logic is stopped and PMC output 7 (Full Powerdown) from Port 7072H is set. This enables the powering down of all chips except DRAM, WD7910LP, WD76C20, WD76C30 and WD90C20. The WD76C20 provides NPDREF (a 64 KHz refresh signal on input pin 117) during the power down mode. This signal is then gated by the System Controller to the NREFRESH signal as an output on pin 32.

When a PMC interrupt occurs, PMC output 7 at Port 7072H is reset, enabling the power up sequence. A CPURES and BUS_RST (see Figure 5-1) are asserted until the PMCIN 01 PPG at Port 8872H input is high. The tristated outputs are restored and the inputs are no longer masked.

FPD remains a 1 until replaced by a 0.

FPD = 0 -
No power down (Default value).

FPD = 1 -
Full power down and in standby mode.

Bit 12 - Ignored by the System Controller, may be 0 or 1.

Bits 11, 10 - BUS_MOD, Bus Mode

The System Controller defaults to mode 00 at power up. Therefore, the bus clock (SYSCLK) is controlled by BCLK2 and is asynchronous with CPUCLK (see Figure 4-1). This allows CPUCLK to be faster than SYSCLK and vary without affecting the bus timing. Normally, BCLK2 is either 16 MHz or 32 MHz. SYSCLK is divided by two regardless of the mode selected by BUS_MOD, and if BCLK2 is 16 MHz at power up, it is divided by two again, providing a SYSCLK clock rate of 4 MHz until programmed to mode 01. In mode 01, the SYSCLK rate is 8 MHz for a BCLK2 of 16 MHz. Both mode 00 and 01 are asynchronous and require the appropriate synchronization delays to be established by BRQ_DEL and BAK_DEL of this register.

In modes 10 and 11, the SYSCLK is synchronous with the CPUCLK and synchronization delays are not needed. The bus clock mode may need to be reprogrammed when the processor clock changes.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BUS_MOD
11 10
0 0 - Bus logic uses BCLK2 divided by 2 (Default value).
0 1 - Bus logic uses BCLK2 divided by 1.
1 0 - Bus logic uses CPUCLK divided by 2.
1 1 - Bus logic uses CPUCLK divided by 1.

Bits 09, 08 - BRQ_DEL, Bus Request Delay

An asynchronous AT bus state machine requires a synchronization delay at the start of the bus cycle.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BRQ_DEL
09 08
0 0 - 1 Bus clock delay (Default value).
0 1 - .5 Bus clock delay.
1 0 - No clock delay.
1 1 - Reserved.

Bits 07, 06 - BAK_DEL, Bus Acknowledge Delay

The AT bus state machine has several options available for signaling the CPU control logic that an AT bus cycle has completed. The timing of this signal determines AT bus hold time for the data and address. Proper timing is determined by the CPU speed, AT bus speed and whether they are synchronous or asynchronous. The delay settings listed here are referenced to the trailing edge of the AT command strobe.

Refer to Table 5-2 for the appropriate choices according to the CPU type and speed and AT bus speed employed.

BAK_DEL
07 06
0 0 - No delay.
0 1 - -.5 Bus clock delay.
1 0 - -1 Bus clock delay.
1 1 - +.5 Bus clock delay (Default value)

Bit 05 - WSI16, Wait State for 16 bit I/O

WSI16 = 0 -
1 Bus clock wait state (Default value).

WSI16 = 1 -
2 Bus clock wait state

Bit 04 - WSM16, Wait State for 16 bit Memory

WSM16 = 0 -
1 Bus clock wait state (Default value).

WSM16 = 1 -
2 Bus clock wait state.

Bits 03, 02 - WSI8, Wait State for 8 bit I/O

WSI8
03 02

0 0 - 2 Bus clock wait state.

0 1 - 3 Bus clock wait state.

1 0 - 4 Bus clock wait state (Default value).

1 1 - 5 Bus clock wait state.

Bits 01, 00 - WSM8, Wait State for 8 bit Memory

WSM8
01 00

0 0 - 2 Bus clock wait state.

0 1 - 3 Bus clock wait state.

1 0 - 4 Bus clock wait state (Default value).

1 1 - 5 Bus clock wait state.

5.3.2 Numeric Processor Busy (NPBUSY) Reset

Port Address 0F0H - Write only

Writing any data to this port resets the 80287 busy signal (de-asserts NPBUSY). The data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

5.3.3 Numeric Processor Reset (NPRST)

Port Address 0F1H - Write only

Writing any data to this port asserts NPRST and resets the 80287. The main processor is wait stated for 128 clocks when writing to this port. The data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

CPU TYPE	CPU SPEED	AT BUS SPEED	AT BUS MODE	BUS MOD	BRQ DEL	BAK DEL
80286	25 MHz	8 MHz	ASYNC	0X	00	00
	20 MHz	8 MHz	ASYNC	0X	01	01
	20 MHz	10 MHz	SYNC	10	10	10
	16 MHz	8 MHz	SYNC	10	10	10
	12.5 MHz	8 MHz	ASYNC	0X	01	10
	10 MHz	10 MHz	SYNC	11	10	10
	8 MHz	8 MHz	SYNC	11	10	10
80386SX	25 MHz	8 MHz	ASYNC	0X	01	00
	20 MHz	10 MHz	SYNC	10	10	10
	20 MHz	8 MHz	ASYNC	0X	01	00
	16 MHz	8 MHz	SYNC	10	10	10
	12.5 MHz	8 MHz	ASYNC	0X	01	10

TABLE 5-2. BUS TIMING PARAMETERS

5.4 DMA CONTROL

The System Controller contains two DMA controllers. DMA Controller 1 is in the I/O address space from 000H to 00FH and is used for 8-bit transfers. DMA Controller 2 is in the I/O space from 0C0H to 0DEH and is used for 16-bit transfers. Channel 0 of DMA Controller 2 is used to cascade DMA controller #1. Table 5-4 indentifies the Controller/-Channel location and function.

AT Bus DMA Channel	DMA Controller	Transfer Type
0	#1 Channel 0	8-bit
1	#1 Channel 1	8-bit
2	#1 Channel 2	8-bit
3	#1 Channel 3	8-bit
4	#2 Channel 0	Cascade DMA Cont. #1
5	#2 Channel 1	16-bit
6	#2 Channel 2	16-bit
7	#2 Channel 3	16-bit

TABLE 5-3. DMA TRANSFER TYPES

5.4.1 Transfer Modes

Each DMA channel may be programmed in Single Transfer Mode, Block Transfer Mode, Demand Transfer Mode or Cascade Mode.

Refer to Section 5.4.12 - Mode Register, bits 7 and 6 for programming.

Demand Mode - 00

In demand mode, a transfer continues to take place until DRQ is de-asserted or a Terminal Count (TC) is reached. If the DRQ is de-asserted, the bus will be released. If DRQ is re-asserted, the transfer will resume. The address and word count behave as in single mode.

Single Transfer Mode - 01

In single transfer mode, the channel makes one transfer for each request. The word count is decremented, and the address is incremented or decremented at the end of each transfer. When the word count goes from 0000H to FFFFH, a Terminal Count (TC) is generated. To start a transfer, the DRQ should be asserted until a DACK is received. If the DRQ is asserted through the cycle, only one transfer will take place. The DRQ must be de-asserted and then re-asserted to start another transfer. The bus is released between transfers.

Block Transfer Mode - 10

A transfer is started in block mode by a DRQ and continues until a TC is reached. The DRQ should be held active until DACK is asserted. Block mode should be used with caution since refresh is locked out. The address and word count behave as in single mode.

Cascade Mode - 11

Cascade mode is used to cascade DMA controller #2 to DMA controller #1, and for bus master transfers. A channel in cascade mode gets the bus when a DRQ is asserted, but the word count and address are ignored. The channel holds the bus until DRQ is de-asserted. The $\overline{\text{IOR}}$, $\overline{\text{IOW}}$, $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ signals must be generated by the bus master device. The addresses from the System Controller are tristated when the $\overline{\text{MASTER}}$ signal is asserted.

5.4.2 Transfer Types

There are three types of transfers: verify, write and read.

Refer to Section 5.4.12 - Mode Register, bits 3 and 2 for programming.

Verify - 00

A verify transfer is a pseudo transfer that does not generate $\overline{\text{IOR}}$, $\overline{\text{IOW}}$, $\overline{\text{MEMR}}$ or MEMW signals.

Write - 01

A write transfers data from an I/O device to memory.

Read - 10

A read transfers data from memory to an I/O device.

5.4.3 Autoinitialize

A channel may be programmed to autoinitialize for any transfer type. In this mode, when a TC is reached, the channel is loaded with the original word count and address and is ready to start another transfer.

Refer to Section 5.4.12 - Mode Register, bit 4 for programming.

5.4.4 Priority

Each DMA controller has two types of priority, fixed and rotating. For fixed priority, channel 0 has the highest priority and channel 3 has the lowest. In rotating priority, the last channel to be serviced has the lowest priority.

5.4.5 Extended Write

In normal timing, the $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$ pulse is two clock cycles and the $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ is one clock cycle. If extended write is selected, the $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ will be the same as the $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$.

5.4.6 Base and Current Address

Each channel has a 16-bit base and current address register. The current address register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current address register is incremented or decremented during a transfer.

Addresses are driven to the bus while $\overline{\text{REFRESH}}$ is asserted, indicating a refresh cycle. Only address bits A23-A16 (from the page register) and bits A10-A0 (from the refresh counter) are meaningful during refresh. The address counter is incremented on the rising edge of $\overline{\text{REFRESH}}$.

5.4.7 Base and Current Word Count

Each channel has a 16-bit base and current word count register. The current word count register is loaded from the base register when the base register is loaded or when in autoinitialize mode. The current word count is decremented during a transfer.

I/O Address Hex	Read/Write	DMA Controller	Function
000	Read/Write	1	Channel 0 Address
001	Read/Write	1	Channel 0 Word Count
002	Read/Write	1	Channel 1 Address
003	Read/Write	1	Channel 1 Word Count
004	Read/Write	1	Channel 2 Address
005	Read/Write	1	Channel 2 Word Count
006	Read/Write	1	Channel 3 Address
007	Read/Write	1	Channel 3 Word Count
008	Read	1	Status
008	Write	1	Command Register
009	Write	1	Request Register
00A	Write	1	Single Mask
00B	Write	1	Mode Register
00C	Write	1	Clear Pointer
00D	Write	1	Master Clear
00E	Write	1	Clear Mask
00F	Write	1	Mask All
080-09F			DMA Page Register
0C0	Read/Write	2	Channel 0 Address
0C2	Read/Write	2	Channel 0 Word Count
0C4	Read/Write	2	Channel 1 Address
0C6	Read/Write	2	Channel 1 Word Count
0C8	Read/Write	2	Channel 2 Address
0CA	Read/Write	2	Channel 2 Word Count
0CC	Read/Write	2	Channel 3 Address
0CE	Read/Write	2	Channel 3 Word Count
0D0	Read	2	Status
0D0	Write	2	Command Register
0D2	Write	2	Request Register
0D4	Write	2	Single Mask
0D6	Write	2	Mode Register
0D8	Write	2	Clear Pointer
0DA	Write	2	Master Clear
0DC	Write	2	Clear Mask
0DE	Write	2	Mask All
B872	Read	1, 2	DMA Mode Shadow

TABLE 5-4. DMA CONTROLLER/CHANNEL FUNCTION MAP

5.4.8 Command Register

Port Addresses 008H, 0D0H - Write only

The Command Register is reset by RSTIN or by writing any data to Port Address 00DH or 0DAH (see section 5.4.14).

7	6	5	4	3	2	1	0
		EX_ WR	RO_ PRI	0	CO_ DIS		

Signal Name	Default At RSTIN
All signals	0

Bits 7, 6 - Not used, state is ignored

Bit 5 - EX_WR, Extended Write

Bit 4 - RO_PRI, Rotating Priority

Bit 3 - Must be set to 0

Bit 2 - CO_DIS, Controller Disabled

Bits1, 0 - Not used, state is ignored

5.4.9 Status Register

Port Addresses 008H, 0D0H - Read only

Bits 3-0 are reset by NRSTIN, writing any data to Port Address 00DH or 0DAH (see section 5.4.14) or when read by a Status Read Command.

7	6	5	4	3	2	1	0
CH3_ DRQ	CH2_ DRQ	CH1_ DRQ	CH0_ DRQ	CH3_ TC	CH2_ TC	CH1_ TC	CH0 TC

Signal Name	Default At RSTIN
CH3_DRQ - CH0_DRQ	None
CH3_TC - CH0_TC	0

Bit 7 - CH3_DRQ, Channel 3 DRQ active

Bit 6 - CH2_DRQ, Channel 2 DRQ active

Bit 5 - CH1_DRQ, Channel 1 DRQ active

Bit 4 - CH0_DRQ, Channel 0 DRQ active

Bit 3 - CH3_TC, Channel 3 has reached TC

Bit 2 - CH2_TC, Channel 2 has reached TC

Bit 1 - CH1_TC, Channel 1 has reached TC

Bit 0 - CH0_TC, Channel 0 has reached TC

5.4.10 Request Register

Port Addresses 009H, 0D2H - Write only

Each channel may be started by a software request. These requests are not affected by the Mask Register. The Request Register is reset by RSTIN or by writing any data to Port Address 00DH or 0DAH (see section 5.4.14).

7	6	5	4	3	2	1	0
					CRQ	CH#	

Signal Name	Default At RSTIN
All signals	0

Bits 7-3 - Not used, state is ignored

Bit 2 - CRQ, Channel Requested

Bits 1, 0 - CH#, Channel Number Requested

CH# 1	0	
0	0	- Channel 0
0	1	- Channel 1
1	0	- Channel 2
1	1	- Channel 3

5.4.11 Mask Registers

Each channel has a mask bit associated with it If it is set, the channel is disabled. The bits may be set or reset by software, or set by a Terminal Count (TC) if the channel is not in autoinitialize mode. All the bits are set by a RSTIN, or by writing any data to Port Address 00DH or 0DAH (see section 5.4.14).

5.4.11.1 Single Mask Register

Port Addresses 00AH, 0D4H - Write only

7	6	5	4	3	2	1	0
					SE_MA	CH#	

Signal Name / **Default At RSTIN**

All signals 1

Bits 7-3 - Not used, state is ignored

Bit 2 - SE_MA, Set Mask

SE_MA = 0 - Clear Mask

SE_MA = 1 - Set Mask

Bits 1, 0 - CH#, Channel Number Requested

CH# 1 0

0 0 - Channel 0

0 1 - Channel 1

1 0 - Channel 2

1 1 - Channel 3

5.4.11.2 Clear Mask Register

Port Addresses 00EH, 0DCH - Write only

Writing any data to this register resets all Masks. The data is ignored.

7	6	5	4	3	2	1	0

Signal Name / **Default At RSTIN**

All signals . . . . None

Bits 7-0 - Not used, state is ignored

5.4.11.3 Mask Multiple Register

Port Addresses 00FH, 0DEH - Write only

7	6	5	4	3	2	1	0
				CH3_MA	CH2_MA	CH1_MA	CH0_MA

Signal Name / **Default At RSTIN**

All signals 1

Bits 7-4 - Not used, state is ignored

Bit 3 - CH3_MA, Channel 3 Mask

Bit 2 - CH2_MA, Channel 2 Mask

Bit 1 - CH1_MA, Channel 1 Mask

Bit 0 - CH0_MA, Channel 0 Mask

5.4.12 Mode Register

Port Addresses 00BH, 0D6H - Write only

This register selects the mode and type of transfer for each channel. Refer to sections 5.4.1 through 5.4.1.4 for a description of the Transfer Modes, sections 5.4.2 through 5.4.2.3 for a description of the Transfer Types and section 5.4.3 for a description of Autoinitialize.

7	6	5	4	3	2	1	0
TRA_MOD		AD_DEC	AUTO	TRA_TYP		CHA#SEL	

Signal Name / **Default At RSTIN**

All signals . . . . None

Bits 7, 6 - TRA_MOD, Transfer Mode

TRA_MOD
7 6

0 0 - Demand

0 1 - Single

1 0 - Block

1 1 - Cascade

Bit 5 - AD_DEC, Address Decrement

AD_DEC = 0
Address is incremented.

AD_DEC = 1
Address is decremented after each DMA cycle.

Bit 4 - AUTO, Autoinitialize

AUTO = 0
Autoinitialization is disabled.

AUTO = 1
Autoinitialization is enabled.

Bits 3, 2 - TRA_TYP, Transfer Type

TRA_TYP

3	2
0	0 - Verify
0	1 - Write
1	0 - Read
1	1 - Not used

Bits 1, 0 - CHA#_SEL, Channel Select

CHA#_SEL

1	0
0	0 - Channel 0
0	1 - Channel 1
1	0 - Channel 2
1	1 - Channel 3

5.4.13 Clear Pointer Register

Port Addresses 00CH, 0D8H - Write only

Each DMA controller has a pointer flip-flop that indicates which half of the word count or address is being accessed. Each time a word count or address is written or read, the pointer changes state. When the flip-flop is reset, bits 7-0 are accessed, and when it is set, bits 15-8 are accessed. The pointer is reset by writing any data to the Clear Pointer Register, or to Port Address 00DH or 0DAH (see section 5.4.14). In either case, the data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

Bits 7-0 - Not used, state is ignored

5.4.14 Master Clear Rgister

Port Addresses 00DH, 0DAH - Write only

Writing any data to the Master Clear Register will:

1. Clear the Command Register
2. Clear the Status Register
3. Clear the Request Register
4. Set the Mask Register
5. Clear the Pointer Flip-Flop

All data is ignored.

7	6	5	4	3	2	1	0

Signal Name	Default At RSTIN
All signals	None

Bits 7-0 - Not used, state is ignored

5.4.15 DMA Mode Shadow Register

Port Address B872H - Read only

This register is particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board devices.

15	14	13	12	11	10	09	08
DMA1 MODE							

07	06	05	04	03	02	01	00
DMA2 MODE							

Signal Name	Default At RSTIN
DMA1 MODE	0
DMA 2 MODE	0

Bits 15-08 - DMA1 MODE

DMA 1 MODE contains a copy of the data written into the DMA1 Mode Register located at I/O address 00BH (see Table 5-4).

Bits 07-00 - DMA 2 MODE

DMA 2 MODE contains a copy of the data written into the DMA2 Mode Register located at I/O address 0D6H (see Table 5-4).

5.5 SYSTEM CONTROLLER 8259 INTERRUPT CONTROLLERS

The System Controller contains two interrupt controllers. Interrupt Controller 1 is in the I/O space of 020H to 021H and Interrupt Controller 2 is in the I/O space of 0A0H to 0A1H. Interrupt 2 of Interrupt Controller 1 is used to cascade Interrupt Controller 2.

5.5.1 Interrupt Sequence

1. When an interrupt arrives from a peripheral device, the interrupt may only be programmed to be edge sensitive. In this mode, the interrupt must go low and high for each interrupt.

The interrupt sets the appropriate bit in the Interrupt Request Register (IRR).

System Interrupt	Interrupt Controller	Use
0	#1 Level 0	Timer
1	#1 Level 1	Keyboard
2	#1 Level 2	Cascade
3-7	#1 Level 3 - 7	AT Bus
8	#2 Level 0	RTC
9-12	#2 Level 1-4	AT Bus
13	#2 Level 5	Co-Processor
14-15	#2 Level 6-7	AT Bus

TABLE 5-5. INTERRUPT SEQUENCE

2. If the interrupt has not been masked off, it is passed to the priority circuit. There are three types of priority.

Fixed

In fixed priority, interrupt 0 has the highest priority and interrupt 7 has the lowest.

Automatic Rotation

In automatic rotation, the last interrupt serviced has the lowest priority.

Specific Rotation

In this mode, the lowest priority interrupt can be set by software. The next interrupt will have the highest priority. For example if interrupt 4 is set to the lowest level, the priority will be 5, 6, 7, 0, 1, 2, 3 and 4.

3. The interrupt controller sends an IRQ to the CPU.

4. The CPU responds with an INTA cycle that freezes priority.

5. The CPU sends another INTA, causing the interrupt controller to send a vector to the CPU, set the appropriate bit in the Interrupt Service Register (ISR) and clear the corresponding bit in the IRR, if it is in the edge triggered mode. As long as the bit in the ISR is set, all interrupts at the same level or lower are inhibited unless programmed for special mask mode.

6. An EOI is issued to end the interrupt. This clears the appropriate bit in the Interrupt Service Register. For the slave adapter (interrupt controller #2), two EOI's must be issued. There are three types of EOI's, Specific, Non-specific and Automatic.

Specific

An EOI is issued by software for a specific interrupt.

Non-Specific

A non-specific EOI is also issued by software. The hardware generates an EOI for the highest level active interrupt.

Automatic

An automatic EOI is a non-specific EOI that is caused by the second INTA.

The interrupt controllers may also be operated in a polled mode. In this mode, the CPU is set to disable the interrupt input. In this case, software must issue a poll command. This takes the place of an INTA, and the software can then read the interrupt level to determine the interrupt to be serviced.

When cascading is used and the slave has issued an interrupt, other interrupts from the slave are locked out. If it is desired to preserve priority in the slave (i.e., allow higher interrupts to occur when a lower interrupt is being serviced), Special Fully Nested Mode should be programmed in the master. After a non-specific EOI has been sent to the slave, the ISR should be checked to see whether any other interrupts are active. If there are no interrupts active, a non-specific EOI should be sent to the master.

Interrupt Controller	Address Hex	Function	Read/Write
1	020	ICW1	Write
1	021	ICW2	Write
1	021	ICW3	Write
1	021	ICW4	Write
1	021	OCW1	Write
1	020	OCW2	Write
1	020	OCW3	Write
1	020	IRR	Read
1	020	ISR	Read
1	021	Mask	Read
1	020, 021	Interrupt Level	Read
2	0A0	ICW1	Write
2	0A1	ICW2	Write
2	0A1	ICW3	Write
2	0A1	ICW4	Write
2	0A1	OCW1	Write
2	0A0	OCW2	Write
2	0A0	OCW3	Write
2	0A0	IRR	Read
2	0A0	ISR	Read
2	0A1	Mask	Read
2	0A0, 0A1	Interrupt Level	Read

TABLE 5-6. INTERRUPT CONTROLLER FUNCTION MAP

5.5.2 Setup - Initialization Command Words (ICW)

The interrupt controllers are set up by writing a series of Initialization Command Words (ICW). The sequence is started by writing a one to bit 4 of ICW1. If ICW4 is to be included in the sequence, a one must also be written to bit 0 of the ICW1.

5.5.2.1 ICW1 - Initialization Command Word 1

Port Addresses 020H, 0A0H - Write only

Bit 4 of this register must be set to 1 or it will be interrpreted as OCW2 or OCW3.

7	6	5	4	3	2	1	0
			S_S	L_T		N C_M	ICW 4

Signal Name	Default At RSTIN
All signals	None

Bit 7-5 - Not used, state is ignored

Bit 4 - S_S, Start Sequence

S_S Must be set to 1

Bit 3 - L_T, Level Trigger

The Interrupt Controller may be programmed to support Level Sensitive Mode for diagnostic adapters which may need to test this capability.

L_T = 0 -
Edge Triggered Mode is selected.

L_T = 1 -
Level Triggered Mode is selected. EN_LVL (bit 00) in Port A872H must first be set to 1.

Bit 2 - Not Used, state is ignored

Bit 1 - N C_M, Not Cascade Mode

N C_M = 0 -
Cascade Mode selected

N C_M = 1 -
Single Mode selected

Bit 0 - ICW4, Initialization Control Word 4

ICW4 = 0 -
ICW4 not included in sequence

ICW4 = 1 -
ICW4 is included in sequence

5.5.2.2 ICW2 - Initialization Command Word 2

Port Addresses 021H, 0A1H - Write only

7	6	5	4	3	2	1	0
Interrupt Vector							

Signal Name	Default At RSTIN
All signals	None

Bits 7-3 - Interrupt Vector

Bits 2-0 - Not used, state is ignored

5.5.2.3 ICW3 - Initialization Command Word 3

Port Addresses 021H - Write only

This address accesses only Interrupt Controller 1.

7	6	5	4	3	2	1	0
0	0	0	0	0	I2 H_L	0	0

Signal Name	Default At RSTIN
All signals	None

Bits 7-3 - Not used, must be set to 0

Bit 2 - I2 H_L, Interrupt 2 Has Slave

I2 H_L = 0 -
Interrupt 2 does not have the Slave

I2 H_L = 1 -
Interrupt 2 has the Slave

Bits 1-0 - Not used, must be set to 0

8

Port Addresses 0A1H - Write only

This address accesses only Interrupt Controller 2.

7	6	5	4	3	2	1	0
0	0	0	0	0	Slave ID		

Signal Name	Default At RSTIN
All signals	None

Bits 7-3 - Not used, must be set to 0

Bits 2-0 - Slave ID

5.5.2.4 ICW4 - Initialization Command Word 4

Port Addresses 021H, 0A1H - Write only

A Slave does not have ICW4.

7	6	5	4	3	2	1	0
0	0	0	S F N M	0	0	AUT EOI	1

Signal Name	Default At RSTIN
All signals	None

Bits 7-5 - Not used, must be set to 0

Bit 4 - S F N M, Special Fully Nested Mode

S F N M = 0 -
Not Special Fully Nested Mode

S F N M = 1 -
Special Fully Nested Mode

Bits 3-2 - Not used, must be set to 0

Bit 1 - AUT_EOI, Auto End Of Interrupt

AUT_EOI = 0 -
Normal End Of Interrupt

AUT_EOI = 1 -
Automatic End Of Interrupt

Bit 0 - Not used, must be set to 1

5.5.3 Operation

Once the interrupt controllers are set up, they may be programmed by Operation Control Words One through Three (OCW1:3).

5.5.3.1 OCW1 - Operation Control Word 1

Port Address 021H, 0A1H - Write only

7	6	5	4	3	2	1	0
INT 7_M	INT 6_M	INT 5_M	INT 4_M	INT 3_M	INT 2_M	INT 1_M	INT 0_M

Signal Name	Default At RSTIN
All signals	None

Bit 7 - Interrupt 7 Mask

Bit 6 - Interrupt 6 Mask

Bit 5 - Interrupt 5 Mask

Bit 4 - Interrupt 4 Mask

Bit 3 - Interrupt 3 Mask

Bit 2 - Interrupt 2 Mask

Bit 1 - Interrupt 1 Mask

Bit 0 - Interrupt 0 Mask

5.5.3.2 OCW2 - Operation Control Word 2

Port Address 020H, 0A0H - Write only

7	6	5	4	3	2	1	0
EOI_CONT			0	0	INT_LEV		

Signal Name	Default At RSTIN
All signals	None

Bits 7-5 - EOI_CONT, End Of Interrupt

EOI_CONT

7	6	5
0	0	0 - Clear Rotate On Automatic EOI
0	0	1 - Non-specific EOI
0	1	0 - Not used
0	1	1 - Specific EOI
1	0	0 - Set Rotate on Automatic EOI
1	0	1 - Rotate on Non-Specific EOI
1	1	0 - Set Priority
1	1	1 - Rotate on Specific EOI

Bits 4, 3 - Must be set to 0

Bits 2-0 - INT_LEV, Interrupt Level

To enable the setting of the interrupt level (INT_LEV), EOI_CONT must be set to 1 1 0 (Set Priority).

INT_LEV

2	1	0
0	0	0 - Interrupt Level 0
	↕	
1	1	1 - Interrupt Level 7

5.5.3.3 OCW3

Port Address 020H, 0A0H - Write only

7	6	5	4	3	2	1	0
0	SMM		0	1	P_C	IRR_ISR	

Signal Name	Default At RSTIN
All signals	None

Bit 7 - Must be set to 0

Bits 6, 5 - SMM, Special Mask Mode

SMM

6	5	
0	0	Not used
0	1	Not used
1	0	Reset Special Mask Mode
1	1	Set Special Mask Mode

Bit 4 - Must be set to 0

Bit 3 - Must be set to 1

Bit 2 - P_C, Poll Command

P_C = 0 -
No Poll Command

P_C = 1 -
Poll Command

Bits 1-0 - IRR_ISR, Interrupt Request Register and Interrupt Service Register

IRR_ISR

1	0
0	0 - Not used
0	1 - Not used
1	0 - Read Interrupt Request Register
1	1 - Read Interrupt Service Register

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5.6 SYSTEM CONTROLLER 8254 TIMER

The System Controller contains an 8254 equivalent timer containing three independent counters. All the timers run off of a 1.19 MHz clock derived from the 14.318 MHz clock input. The GATE0 and GATE1 signals are tied high. The GATE2 signal is tied to register 61H, bit 0. The counters decrement when counting. The largest possible count is 0.

Each counter may be programmed for different counting modes and the count may be read back. To initialize a counter, the Control Word must be written, followed by one or two bytes of count if needed. Refer to Table 5-7 for the correct Control Word Format. Each counter may be programmed to count in BCD or binary.

I/O Address	Use	Read/Write
040H	Timer 0 Count/Status	Read/Write
041H	Timer 1 Count/Status	Read/Write
042H	Timer 2 Count/Status	Read/Write
043H	Control Word	Write

Timer Channel	Use
0	Time of Day (Interrupt)
1	Refresh Request
2	Speaker

CONTROL WORD (FORMAT 1) - I/O Address 043H - Counter Latch Command			
0	BCD		
1-3	Mode	000	Mode 0
		001	Mode 1
		X10	Mode 2
		X11	Mode 3
		100	Mode 4
		101	Mode 5
4-5	Function	00	Counter Latch Command
		01	Read/Write Low Byte
		10	Read/Write High Byte
		11	Read/Write Low Byte then High Byte
6-7	Counter	00	Counter 0
		01	Counter 1
		10	Counter 2

CONTROL WORD (FORMAT 2) - I/O Address 043H - Read Back Command		
0		0
1		Select Counter 0
2		Select Counter 1
3		Select Counter 2
4		Latch Status
5		Latch Count
6-7		11

TABLE 5-7. CONTROL WORD FORMAT

5.6.1 Setup

Each counter may be set in one of six modes by writing a Control Word (format 1). The Control Word must specify the counter and the number of count bytes to be written. A new count may be written at any time.

5.6.1.1 Mode 0 Interrupt on Terminal Count

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting.

OUT goes low when the counter starts. It goes high when the count = 0, and stays high until a new count or mode is written.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

5.6.1.2 Mode 1 Hardware Retriggerable One Shot

The counter starts when GATE goes from low to high. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode.

Any time GATE goes from low to high, the counter is reloaded with the original count and the counter started.

OUT goes low when GATE goes from low to high. It goes high when the count = 0. If a new count is written while the counter is counting, it will be loaded the next time GATE goes from low to high.

5.6.1.3 Mode 2 Rate Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter is started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

OUT is initially high. When the count = 1, OUT goes low for one clock.

If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.1.4 Mode 3 Square Wave Generator

The counter starts when the count is loaded. When the count = 0, the counter is reloaded and the counter started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded.

When the counter starts, OUT is high. When the count is half done, OUT goes low. If GATE goes low then OUT will go high.

If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.1.5 Mode 4 Software Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. OUT is initially high. When the count = 0, OUT goes low for one clock.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

5.6.1.6 Mode 5 Hardware Triggered Strobe

The counter starts when the count is loaded. When the count = 0, the counter continues counting from FFFFH in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high, the counter is reloaded. OUT is high when the counter starts. When count = 0, OUT goes low for one clock. If a new count is written while the counter is counting, it will be loaded the next time the count = 0 or when GATE goes from low to high.

5.6.2 Reading The Counter

There are three ways of reading the counters:

1. The count is read directly. This mode can cause false readings due to the fact that the counter may be changing while it is read.

2. The count may be read via a Counter Latch Command. (See Control Word format 1). This command latches the count so that it may be read without changing.

3. The count may be read via a Read Back Command. (See Control Word format 2). This command is the equivalent of multiple Counter Latch Commands.

5.6.3 Reading Status

The status of a counter may be read by issuing a Read Back Command with data bit 4 = 0. (See Control Word format 2). Bits 0-5 are the same as the command word for the counter. Bit 6 tells whether the last count that was written has been loaded into the counter. Bit 7 reflects the state of the OUT pin.

STATUS WORD	
0	BCD
1-3	Mode
4-5	Function
6	New Count Written
7	Out Status

5.6.4 Page

The page register is an 8-bit by 16-byte dual-ported RAM. It is used during refresh cycles and to generate address bits 16 to 23 for 8-bit DMA transfers and address bits 17 to 23 for 16-bit DMA transfers. One port of the RAM is a read-only port for DMA or refresh cycles and the other is a read/write port for the 80286 CPU.

5.6.5 Refresh Address

This block contains an 11-bit counter that is used for the address during a refresh.

5.7 SYSTEM CONTROLLER DECODE

Address 9	8	7	6	5	4	3	2	1	0	Decodes	Hex
0	0	0	0	0	X	X	X	X	X	DMA Controller 1 (Ch 0-3)	000-00F
0	0	0	0	1	X	X	X	X	X	Interrupt Controller Master	020-03F
0	0	0	1	0	X	X	X	X	X	Timer	040-05F
0	0	0	1	1	0	X	X	X	1	Port B (PIO)	061-06F (odd)
0	0	0	1	1	1	X	X	X	0	Real-Time Clock (Address)	070-07E (even)
0	0	0	1	1	1	X	X	X	1	Real-Time Clock (Data)	071-07F (odd)
0	0	1	0	0	X	X	X	X	X	Page Register (except 092H)	080-09F
0	0	1	0	0	1	0	0	1	0	ALT 20 GATE, Hot Reset	092
0	0	1	0	1	X	X	X	X	X	Interrupt Controller Slave	0A0-0BF
0	0	1	1	0	X	X	X	X	X	DMA Controller 2 (Ch 4-7)	0C0-0DF

TABLE 5-8. DECODE ADDRESSES

5.7.1 Page Register Decodes

Address	Decode
0087H	DMA Channel 0
0083H	DMA Channel 1
0081H	DMA Channel 2
0082H	DMA Channel 3
008BH	DMA Channel 5
0089H	DMA Channel 6
008AH	DMA Channel 7
008FH	Refresh

TABLE 5-9. PAGE REGISTER DECODES

NOTE

Page register data appears on address bits A23-A16 during refresh and 8-bit DMA cycles. For 16-bit DMA cycles (channels 5-7), the LSB of the page register does not appear.

8

5.8 NMI AND REAL TIME CLOCK

5.8.1 Real Time Clock Address Register

Port Address 070H-07EH even - Write only

There is only one RTC Address Register. All even number addresses from 070H through 07EH access this register.

7	6	5	4	3	2	1	0
D_ NMI	RTC A6	RTC A5	RTC A4	RTC A3	RTC A2	RTC A1	RTC A0

Signal Name	Default At RSTIN
D_NMI	1
RTC6 - RTC0	None

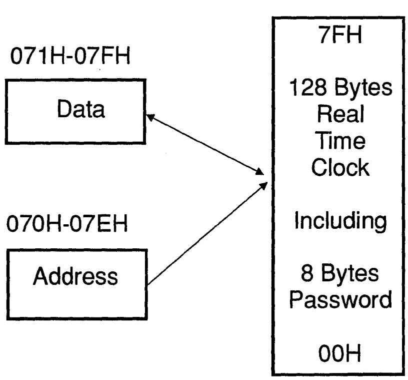
Bit 7 - D_NMI, Disable Non-Maskable Interrupt

D_NMI = 0 -
Non-Maskable Interrupt enabled

D_NMI = 1 -
Non-Maskable Interrupt disabled (Default value)

Bits 6-0 - RTCA6 through RTCA0, Real-Time Clock Address

RTCA6 through RTCA0 provide the 128 addresses of the Real-Time Clock area. The data selected by this address is available by reading the RTC Data Register at the odd numbered locations, 071H-07FH.



5.8.2 Real-Time Clock Data Register

Port Address 071H-07FH odd - Read and Write

There is only one RTC Data Register. All odd number addresses from 071H through 07FH access this register.

Data is transferred between this register and the memory location selected by the RTC Address Register. The data bus used is selected by bit 15 of the register at Port Address 2872H (refer to section 7.2).

7	6	5	4	3	2	1	0
Real-Time Clock Data							

5.8.3 Lock Pass, Alternate A20G And Hot Reset

Port Address 092H - Read and Write

7	6	5	4	3	2	1	0
				LOCK_ PASS		ALT_ A20G	HOT_ RST

Signal Name	Default At RSTIN
Bits 7-4, 2	None
LOCK_PASS	0
ALT_A20G	0
HOT_RST	0

Bit 3 - LOCK_PASS

LOCK_PASS is used to prevent access to the eight byte password located in the Real-Time Clock area. The protected addresses are 38H through 3FH. Before LOCK_PASS can be set, bit 02 of the register at Port Address 2872H must be set to 0. Once LOCK_PASS is set, it can only be reset by NRSTIN.

LOCK_PASS = 0 -
The eight byte password area is accessible.

LOCK_PASS = 1 -
The eight byte password area is not accessible.

Bit 1 - ALT_A20G, Alternate A20 Gate

Normally, the state of ALT_A20G is ORed with the external A20GT signal. If either ALT_A20G or A20GT is high, the A20 line is ungated. If both ALT-A20G and A20GT are low, A20 will be gated low.

As an option, ALT_A20G may be programmed by the Diagnostic Register at Port Address 9872H to automatically change state to match that of the Keyboard's A20GATE.

Bit 0 - HOT_RST, Hot Reset

A processor reset (CPURES) is generated 128 CPUCLKs after the HOT_RST changes from a 0 to 1. The CPURES is 16 clock pulses wide.

5.9 PARITY ERROR AND I/O CHANNEL CHECK

Port Address 061H- 06FH odd
Bits 7-4 - Read only, Bits 3-0 - Read and Write

Odd numbered Port Addresses 061H through 06FH provide access to parity error and I/O Channel Check of the expansion bus.

7	6	5	4	3	2	1	0
PE	IOCK	OUT 2	REF DT	D_ IOC	D_ PE	ENS PK	TMR 2G

Signal Name	Default At RSTIN
PE	0
IOCK	0
OUT2	NA
REFDT	1
D_IOC	0
D_PE	0
ENSPK	0
TMR2G	0

Bit 7 - PE, Parity Error (read only)

PE = 0 -
No Parity Error

PE = 1 -
Parity Error

Bit 6 - IOCK, I/O Channel Check from the expansion bus (read only)

IOCK = 0 -
No I/O Channel Check Error

IOCK = 1 -
I/O Channel Check Error

Bit 5 - OUT2, from timer channel 2 (read only)

OUT2 represents the state of the Timer 2 output.

Bit 4 - REFDT, changes state on each refresh (read only)

Bit 3 - D_IOC, Disable I/O Channel Check (read and write)

D_IOC = 0 -
I/O channel check from the expansion bus is not disabled.

D_IOC = 1 -
I/O channel check from the expansion bus is disabled.

Bit 2 - D_PE, Disable Parity Error Check (read and write)

D_PE = 0 -
Parity error checking not disabled. This may be overridden by Port Address register 6072H, bit 10 for systems without parity RAM.

D_PE = 1 -
Parity error checking disabled

Bit 1 - ENSPK, Enable Speaker

ENSPK = 0 -
Speaker is not enabled

ENSPK = 1 -
Speaker is enabled

Bit 0 - TMR2G, Gate for Timer Channel 2

TMR2G = 0 -
Timer Channel 2 gated low

TMR2G = 1 -
Timer Channel 2 output enabled

8

6.0 MEMORY AND EMS CONTROL

This section describes the DRAM address bus and the EMS memory configuration and control registers.

6.1 DRAM ADDRESS AND DATA BUS

The memory address bus is multi-functional. During DRAM cycles, the DRAM row and column addresses are present on RA11 through RA0. During I/O cycles, RA11 through RA08 (CS3-CS0)are used to decode 16 possible Chip Selects. Also, during I/O cycles to devices such as the Keyboard Controller, RA7 through RA0 become the Data Bus bits ED7 through ED0.

The RAS and CAS lines are designed to drive the DRAM array directly without the use of external drivers. RA11 through RA0 are capable of driving 350 pF, the equivalent load of two banks of one bit wide RAM, plus two banks of four bit wide RAM (48 DRAMs).

The W/$\overline{R}$ signal at pin 119 should be buffered before use. Write protection is accomplished by not asserting CAS to the local DRAM while $\overline{NMEMW}$ at pin 37 is asserted.

The on-board DRAM may be disabled so that external cards such as EMS may provide memory. The DRAM may be disabled in three stages, from 128 Kbyte to 640 Kbyte, 256 Kbyte to 640 Kbyte and 512 Kbyte to 640 Kbyte.

When disabling any on-board DRAM, the register at Port Address 6872H must not be programmed to enable the on-board Lower EMS Page Frame.

The WD7910 and WD7910LP provide support for DRAM banks to be independent or two-way page interleaved. DRAM banks that are interleaved must be of the same DRAM size.

6.2 MEMORY CONFIGURATION

6.2.1 Memory Control

Port Address 3872H - Read and Write

15	14	13	12	11	10	09	08
PG_CAS		CA		PG	ILV		

07	06	05	04	03	02	01	00
SIZE BNK3		SIZE_ BNK2		SIZE_ BNK1		SIZE_ BNK0	

Signal Name	Default At RSTIN
PG_CAS	0
CA	00
PG	0
ILV	00
SIZE_BNK3	00
SIZE_BNK2	00
SIZE_BNK1	00
SIZE_BNK0	00

Bit 15 - PG_CAS, Page Mode CAS Width

PG_CAS = 0 - Read CAS pulse width is 2.5 CPUCLK clocks (Default value).

PG_CAS = 1 - Read CAS pulse width is 2 CPUCLK clocks. This is required for 80386SX Pipeline mode.

Bit 14 - Reserved for future use, should be set to 0.

Bits 13, 12 - CA, Cache Mode

Enabling the Cache Mode adds an additional wait state to the beginning of on-board read cycles. On-board read cycles occur only for cache misses. If the RDYIN signal indicates that the external cache has experienced a zero wait state read hit, the DRAM read cycle is aborted.

Pin 51 of the System Controller serves one of three functions, depending upon the mode selected by CA. Pin 51 may represent the RDYIN (Ready In), CKA (Alternate Clock) or PE (Parity Error).

When CA is changed, a hold acknowledge cycle is required before the change goes into effect.

CA 13 12

- 0 0 - Cache Mode not enabled. Pin 51 may be used as the alternate clock CKA. (Default value)
- 0 1 - Cache Mode enabled.
- 1 0 - External Memory Controller. Pin 51 becomes PE and is connected to the parity error line of the external memory controller.
- 1 1 - Pin 51 may be used as the alternate clock CKA. When CAS Input Mode is enabled, PE on pin 111 becomes an input and represents an error. (See pin 12 description in Table 3-2 on selecting CAS Mode.)

Bit 11 - PG, Page Mode

PG = 0 - Non-page mode (Default value) Word interleaving is employed when bank interleaving is enabled by ILV. Non-page mode *is not supported* in 1Mbit x 16 chips and 2Mbits x 16 configurations.

PG = 1 - Page mode Page mode interleaving is performed when bank interleaving is enabled by ILV.

Bits 10-08 - ILV, Interleave

In Non-page Mode (PG = 0), word interleaving is employed. In Page Mode (PG = 1), Page Mode interleaving is used. Four-way interleave is only supported in Page Mode when four banks are installed using one of the following DRAM configurations: 4 Mbits x 16; 512Kbits x 16; 1Mbit x 16 chips; or 2Mbits x 16. Interleave of 64 Kbits x 16 DRAM is not supported by any of the System Controllers.

DRAM banks must be of the same size and assigned the same starting address when they are interleaved together.

8

ILV 10 09 08

- 0 0 0 - No interleaving performed
- 0 0 1 - Banks 0 and 1 are interleaved
  Banks 2 and 3 are not interleaved
  Banks 0 and 1 must be the same size
- 0 1 0 - Banks 0 and 1 are not interleaved
  Banks 2 and 3 are interleaved
- 0 1 1 - Banks 0 and 1 are interleaved
  Banks 2 and 3 are interleaved
  (Each pair must be the same size. Banks 0 and 1 may be a different size from Banks 2 and 3.)
- 1 0 0 - Page Mode four-way interleave (Banks 0, 1, 2 and 3 must have one of the following DRAM configurations installed: 4 Mbits x 16; 512 Kbits x 16; 2Mbits x 16; or 1 Mbit x 16 chips.)

DRAM Banks 3 through 0

The WD7910 and WD76910LP support all DRAM sizes. The DRAM sizes may be mixed. See section 10.14, DRAM Size and SMI RAM Register.

Bits 07, 06 - SIZE_BNK3, Size of Bank 3

PORT 7472	PORT 3872		BANK 3 SIZE
BIT 15	BIT 7	BIT 6	
0	0	0	64Kbits x 16
0	0	1	256Kbits x 16
0	1	0	1Mbits x 16
0	1	1	4Mbits x 16
1	0	0	512Kbits x 16
1	0	1	1 Mbits x 16 chip
1	1	0	2 Mbits x 16
1	1	1	Reserved

Bits 05, 04 - SIZE_BNK2, Size of Bank 2

PORT 7472	PORT 3872		BANK 2 SIZE
BIT 14	BIT 5	BIT 4	
0	0	0	64Kbits x 16
0	0	1	256Kbits x 16
0	1	0	1Mbits x 16
0	1	1	4Mbits x 16
1	0	0	512Kbits x 16
1	0	1	1 Mbits x 16 chip
1	1	0	2 Mbits x 16
1	1	1	Reserved

Bits 03, 02 - SIZE_BNK1, Size of Bank 1

PORT 7472	PORT 3872		BANK 1 SIZE
BIT 13	BIT 3	BIT 2	
0	0	0	64Kbits x 16
0	0	1	256Kbits x 16
0	1	0	1Mbits x 16
0	1	1	4Mbits x 16
1	0	0	512Kbits x 16
1	0	1	1 Mbits x 16 chip
1	1	0	2 Mbits x 16
1	1	1	Reserved

Bits 01, 00 - SIZE_BNK0, Size of Bank 0

PORT 7472	PORT 3872		BANK 0 SIZE
BIT 12	BIT 1	BIT 0	
0	0	0	64Kbits x 16
0	0	1	256Kbits x 16
0	1	0	1Mbits x 16
0	1	1	4Mbits x 16
1	0	0	512Kbits x 16
1	0	1	1 Mbits x 16 chip
1	1	0	2 Mbits x 16
1	1	1	Reserved

6.2.2 Memory Bank 3 Through Bank 0 Starting Address

Port Address 4872H - Read and Write

15	14	13	12	11	10	09	08
A24	A23	A22	A21	A20	A19	A18	A17
Bank 1 start address							

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17
Bank 0 start address							

Port Address 5072H - Read and Write

15	14	13	12	11	10	09	08
A24	A23	A22	A21	A20	A19	A18	A17
Bank 3 start address							

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17
Bank 2 start address							

The starting address of the bank must be programmed on boundaries corresponding to the bank size. Smaller banks must be placed at a higher starting address than larger banks. The size of the bank is automatically set by the type and size of the RAM. When banks are interleaved, in either page or non-page mode, the interleaved banks should be enabled and programmed to the same starting address.

The bank size is doubled for two-way interleave and quadrupled for four-way interleave. For example, if bank 0 has 256 Kbit DRAMs and banks 2 and 3 have 1 Mbit DRAMs, the starting address for banks 2 and 3 should be zero. Both banks should be enabled. The size of the combined banks is 4 Mbytes, double the size of the individual banks. The starting address for bank 0 should then be at 4 Mbytes. For three banks of the same size, in which two are interleaved, the two interleaved banks must be placed at a lower starting address than the third bank.

RAM SIZE	PAGE SIZE	BANK SIZE
64Kbits x 16	512 Bytes	128 Kbytes
256 Kbits x 16	1024 Bytes	512 Kbytes
1 Mbits x 16	2048 Bytes	2048 Kbytes
4 Mbits x 16	4096 Bytes	8192 Kbytes
512 Kbits x 16	1024 Bytes	1024 Kbytes
1 Mbit x 16 chips	512 Bytes	2048 Kbytes
2 Mbits x 16	1024 Bytes	4096 Kbytes

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6.2.3 Split Starting Address

Port Address 5872H - Read and Write

15	14	13	12	11	10	09	08
EN_ BK3	EN_ BK2	EN_ BK1	EN_ BK0	DRAM_ DRV		SPLIT SIZE	

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19		

Signal Name	Default At RSTIN
EN_BK3	0
EN_BK2	0
EN_BK1	0
EN_BK0	0
DRAM_DRV	00
SPLIT_SIZE	00
Bits 01, 00	None

Bit 15 - EN_BK3, Enable Bank 3

EN_BK3 = 0 -
Bank 3 is disabled (Default value)

EN_BK3 = 1 -
Bank 3 is enabled

Bit 14 - EN_BK2, Enable Bank 2

EN_BK2 = 0 -
Bank 2 is disabled (Default value)

EN_BK2 = 1 -
Bank 2 is enabled

Bit 13 - EN_BK1, Enable Bank 1

EN_BK1 = 0 -
Bank 1 is disabled (Default value)

EN_BK1 = 1 -
Bank 1 is enabled

Bit 12 - EN_BK0, Enable Bank 0

EN_BK0 = 0 -
Bank 0 is disabled (Default value)

EN_BK0 = 1 -
Bank 0 is enabled

Bits 11, 10 - DRAM_DRV, DRAM Driver Strength

The DRAM address driver strength may be adjusted for capacitive load. When adjusted properly, output overshoot and undershoot is minimized while still meeting worst case DRAM timing. The DRAM RAS, CAS and address buffers also automatically compensate for variations in temperature, voltage and manufacturing process.

DRAM_DRV
11 10

0 0 - Full strength DRAM address drive, up to 350 pF (Default value)

0 1 - Low strength DRAM address drive, up to 100 pF

1 0 - Medium strength DRAM address drive, up to 180 pF

1 1 - High strength DRAM address drive, up to 260 pF

Bits 09, 08 - SP SIZE, Split Size

The split is implemented by moving the block of memory between 0A0000H through 0FFFFFH to another area. The destination area must start on a 512 Kbyte boundary. If BIOS is to be shadowed, the split size must be 320 Kbyte for a 64 Kbyte shadow or 256 Kbyte for a 128 Kbyte shadow, and the RAM Shadow And Write Protect Register (Port 6072H) must also be programmed.

Figure 6-1 illustrates that the memory from 0A0000H (640 Kbyte) to 100000H (1024 Kbyte) is available for remapping. The remapping may start at 100000H, providing 384 Kbyte of extended memory, or may start at 0F0000H to allow BIOS shadowing, with 320 Kbyte of extended memory. Only a single bank may be split. The bank to be split must be at least 512 Kbyte or larger.

SPLIT SIZE

09 08

0 0 - No split (Default value)

0 1 - 256 Kbyte split, memory moved from 0A0000H to 0DFFFFH

1 0 - 320 Kbyte split, memory moved from 0A0000H to 0EFFFFH

1 1 - 384 Kbyte split, memory moved from 0A0000H to 0FFFFFH

Bits 07-02 - A24-A19, Split Starting Address

Bits 01, 00 - Not used, state is ignored

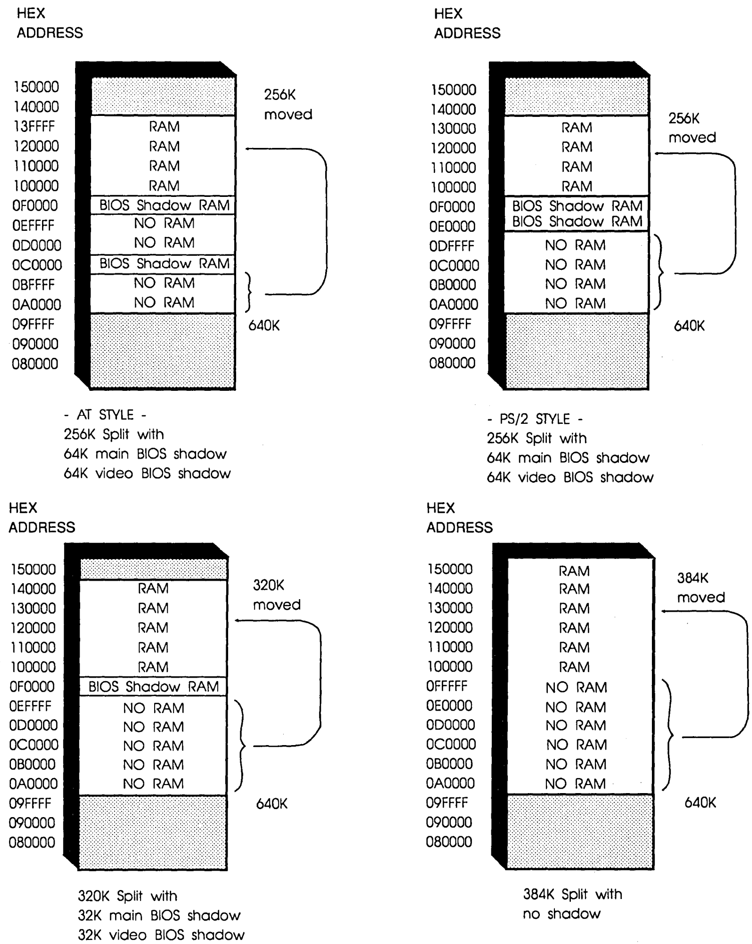

FIGURE 6-1. SPLIT SIZE

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6.2.4 RAM Shadow And Write Protect

Port Address 6072H - Read and Write

15	14	13	12	11	10	09	08
DIS_MEM		HM_ WP	WP	INV_ PAR	PAR_ DIS	SHD	

07	06	05	04	03	02	01	00
X_ MEM		VB_SIZ		ROM_ TYP		BL_MOU	

Signal Name	Default At RSTIN
DIS_MEM	00
HM_WP	0
WP	0
INV_PAR	0
PAR_DIS	0
SHD	00
X_MEM	0
Bit 06	None
VB_SIZ	00
ROM_TYP	00
BL_MOU †	00

→ Featured only in the WD7910LP

Bit 15, 14 - DIS_MEM, Disable On-board Memory

DIS_MEM
15 14

0 0 - On-board memory from 128 KB to 640 KB not disabled (Default value).

0 1 - On-board memory from 512 KB to 640 KB disabled.

1 0 - On-board memory from 256 KB to 640 KB disabled.

1 1 - On-board memory from 128 KB to 640 KB disabled.

Bit 13 - HM_WP, High Memory Write Protect Enable

This bit enables the write protection for the memory boundary established by the register at Port C072H.

HM_WP = 0 -
High memory write protect not enabled (Default value).

HM_WP = 1 -
High memory write protect enabled.

Bit 12 - WP, Shadowed BIOS Write Protect Enable

WP = 0 -
Write protect for shadowed BIOS not enabled (Default value).

WP = 1 -
Write protect for shadowed BIOS enabled.

Bit 11 - INV_PAR, Invert Parity

INV_PAR = 0 -
Normal parity when writing to on-board DRAM (Default value).

INV_PAR = 1 -
Invert parity when writing to on-board DRAM.

Bit 10 - PAR_DIS, Parity Checking Disabled

Parity checking is normally enabled or disabled by Port 061H. Setting PAR_DIS overrides the Port 061H setting and disables parity checking. This ability is provided for systems without parity RAM.

PAR_DIS = 0 -
Parity checking as selected by Port 061H (Default value).

PAR_DIS = 1 -
Parity checking disabled.

Bits 09, 08 - SHD, Shadow BIOS

Before the BIOS can be shadowed, the SPLIT_SIZE field in the Split Starting Address Register at Port 5872H must be programmed to non-zero.

ROM at FE0000H - FFFFFFH, the top of 16 MByte address space is never shadowed.

Option SHD 11 should be used when Video Remap Function is desired (i.e. Video BIOS in the lower half of EPROM shows up at C0000H).

64 Kbyte of system BIOS at 0F0000H - 0FFFFFH, and up to 64 Kbyte of video BIOS at 0C0000H - 0CFFFFH, may be shadowed. This type of shadowing is accomplished by setting SHD = 10 and then writing the system and video BIOS into 0E0000H - 0FFFFFH. When SHD is set to 11, the video BIOS appears at 0C0000H - 0CFFFFH rather than 0E0000H - 0EFFFFH.

The video shadow size at 0C0000H - 0CFFFFH is determined by VB_SIZ, the video BIOS size field.

SHD
09 08

- † 0 0 - No BIOS shadowing, allows 384 KB remap (Default value).
- 0 1 - 64 KB system BIOS shadow, 0F0000H - 0FFFFFH, allows 320 KB remap.
- 1 0 - 128 KB system BIOS shadow, 0E0000H - 0FFFFFH, allows 256 KB remap.
- † 1 1 - 64 KB system BIOS shadow, 0F0000 - 0FFFFF and video BIOS shadow, allows 256 KB remap.

† See note following bits 01, 00.

Bit 07 - X_MEM, Shadow BIOS for Read/Write Memory

When SHD (bits 09 and 08) equals 11, X_MEM provides the means of using RAM from E8000H through EFFFFH not being used for video BIOS shadowing, to be used as read/write memory.

X_MEM = 0 - SHD = 11
ROM_TYP = 10 - VB_SIZ = 01

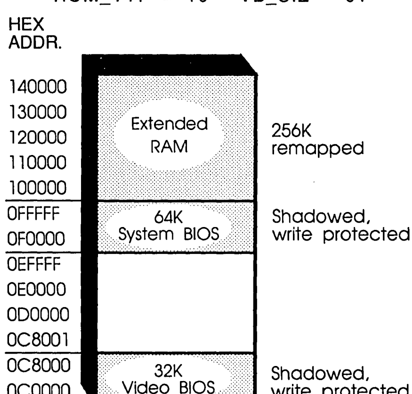

FIGURE 6-2. X_MEM = 0

X_MEM = 1 - SHD = 11
ROM_TYP = 10 - VB_SIZE = 01

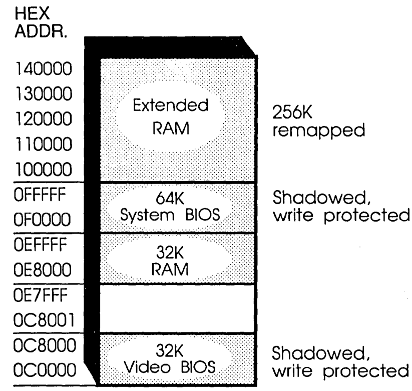

FIGURE 6-3. X_MEM = 1

Bit 06 - Not used, state is ignored

Bits 05, 04 - VB_SIZ, Video BIOS Size

VB_SIZ †
05 04

- 0 0 - 16 KB video BIOS (Default value)
- 0 1 - 32 KB video BIOS
- 1 0 - 48 KB video BIOS
- 1 1 - 64 KB video BIOS

† See note following bits 01, 00.

Bits 03, 02 - ROM_TYP, ROM Type

For ROM type 00, $\overline{\text{CSPROM}}$ is asserted when the address is 0E0000H - 0FFFFFH or FE0000H - FFFFFFH.

For ROM type 01, $\overline{\text{CSPROM}}$ is asserted when the address is 0F0000H - 0FFFFFH or FF0000H - FFFFFFH.

For ROM type 10, CSPROM is asserted when the address is 0F0000H - 0FFFFFH, FF0000H - FFFFFFH or 0C0000H - 0CXFFFH where X is determined by VB_SIZ. This allows either a 128 Kbyte BIOS with a 64 Kbyte system BIOS and a 64 Kbyte video BIOS, or a 64 Kbyte BIOS with a 32 Kbyte system BIOS and a 32 Kbyte video BIOS. The 32 Kbyte video BIOS portion must be in the bottom half of the EPROM and is accessed both at C0000H - CX000H and F0000H - FX000H. A

64 Kbyte EPROM needs addresses SA15 - SA0. A 128 Kbyte EPROM needs addresses SA16 - SA0. Neither EPROM needs translated addresses.

CSPROM is CS4 through CS0, decoded as the value of 00.

ROM_TYP
03 02

0 0 - 128 KB system BIOS, located at E0000H - FFFFFH

0 1 - 64 KB system BIOS, located at F0000H - FFFFFH (Default value)

† 1 0 - 64 KB or 128 KB shared BIOS System BIOS located at F0000H - FFFFFH, video BIOS located at C0000H - CX000H

1 1 - Reserved

† See note following bits 01, 00.

Bits 01, 00 - BL_MOU, Backlight Mouse Control
Featured only in the WD7910LP

Enabling the Backlight Mouse Control increases the CPU speed for one second if Auto Clock Switching is on. The AUT_FST bit is located at Port 1072H bit 11. Enabling the Backlight Mouse Control also affects the Back/light and LCD timers in the PMC Timer Register at Port Address 8072H.

BL_MOU
01 00

0 0 - No mouse control (Default value)

0 1 - INT12 mouse

1 0 - INT4 mouse

1 1 - INT3 mouse

† NOTE

When SHD = 11 and X_MEM = 0, or SHD = 00 and ROM_TYP = 10, the portion of 0E0000H DRAM memory that is not mapped to 0C0000H (as determined by VB_SIZ) is not accessible. Once a portion of 0E0000H segment is mapped to 0C0000H, all 0E0000H accesses go to the expansion bus without generation of CSPROM. This allows AT bus plug-in boards and/or drivers to access the E0000H segment.

6.2.5 High Memory Write Protect Boundary

Port Address C072H - Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
A24	A23	A22	A21	A20	A19	A18	A17

Signal Name	Default At RSTIN
Bits 15-08	None
A24 - A17	00

Bits 15-08 - Not used, state is ignored

Bits 07-00 - A24-A17, Boundary Address

Memory above the high memory write protect boundary is write protected when enabled by the HM_WP, bit 13 of the RAM Shadow And Write Protect Register at Port 6072H. This provides an additional write protect region for disk caching.

6.3 MEMORY TIMING

The DRAM timing is determined by an internal delay line for DMA and Master Mode transfers. The RAS leading edge becomes active from the active level of MEMR and MEMW. The delay line is automatically tuned to fixed delays, using the 14.318 MHz clock CLK14 as reference.

When writing to the DRAM memory timing register at Port 4072H, the memory timing mode changes immediately. The code that programs this register should be in ROM and not shadowed in RAM.

6.3.1 Non-page Mode DRAM Memory Timing

Port Address 4072H - Read and Write

15	14	13	12	11	10	09	08
	NP_MODE		NP_RAW	NP_WCAS		_NP_RCAS	

07	06	05	04	03	02	01	00
	NP_RAS_HLD		NP_PWE			NP_WS	

Signal Name	Default At RSTIN
Bits 15, 07	None
NP_MODE	00
NP_RAW	0
NP_WCAS	00
NP_RCAS	00
NP_RAS_HLD	00
NP_PWE	000
NP_WS	00

Bit 15 - Not used, state is ignored

Bits 14, 13 - NP_MODE, Non-Page Mode

There are two non-page modes available, Mode-00 and Mode-01. Mode-00 provides one processor clock of row address hold time and is used for 1, 2 or 3 wait state memory cycles. Mode-01 provides a half processor clock of row address hold time and is used for 0 wait state memory cycles. Because the memory timing may be adjusted in increments of half a processor clock, Mode-00 is suited for all DRAM and processor speeds.

Mode-01 provides a half processor clock row address hold time, which is usually sufficient for system speeds of 12.5 MHz and slower. This compressed timing allows zero wait state operation.

Table 6-1A shows typically required DRAM speeds and register programming values for various processor speeds. Because DRAM timing varies among manufacturers, the required DRAM speed may differ from those listed in the table.

NP_MODE
14 13

0 0 - Minimum 1 wait state.

0 1 - Minimum 0 wait state.

PROCESSOR SPEED	NP_MODE	DRAM SPEED	WAIT STATES	REGISTER 4072H
12.5 MHz	01	80 ns	0	3560H
16 MHz	01	53 ns	0	3560H
16 MHz	00	80 ns	1	1025H
20 MHz	00	80 ns	1	1025H
20 MHz	00	100 ns	2	107AH

TABLE 6-1A. TYPICAL DRAM SPEEDS

Bit 12 - NP_RAW, Non-page disable Read After Write

EMS accesses and interleave miss cycles (I/O cycle to device on RAD) may add one additional wait state.

NP_RAW = 0 -
Memory read cycles immediately following a write cycle causes an automatic wait state to be added before initiating the read cycle.

NP_RAW = 1 -
Read after write cycles do not have additional wait states.

Bit 11, 10 - NP_WCAS, Non-page Write CAS Delay

NP_WCAS
11 10

0 0 - CAS write delay 1.0 CLK2
0 1 - CAS write delay 1.5 CLK2
1 0 - CAS write delay 2.0 CLK2
1 1 - CAS write delay 2.5 CLK2

Bit 09, 08 - NP_RCAS, Non-page Read CAS Delay

NP_RCAS
11 10

0 0 - CAS read delay 1.0 CLK2
0 1 - CAS read delay 1.5 CLK2
1 0 - CAS read delay 2.0 CLK2
1 1 - CAS read delay 2.5 CLK2

Bit 07 - Not used, state is ignored

Bits 06, 05 - NP_RAS_HLD, Non-page CAS to RAS Hold Time

The RAS active delay is reduced by half a clock during writes if NP_WCAS is set to 1X, or during reads if NP_RCAS is set to 1X.

NP_RAS_HLD
06 05

0 0 - RAS active until 1.0 clock after CAS.
0 1 - RAS active until 1.5 clock after CAS.
1 0 - RAS active until 2.0 clock after CAS.
1 1 - RAS active until 2.5 clock after CAS.

Bits 04-02 - NP_PWE, Non-page CAS Pulse Width Extension

The pulse width is reduced by half a clock during writes if NP_WCAS is set to X1, or during reads if NP_RCAS is set to 1X.

NP_PWE
04 03 02

0 0 0 - No extension (2 CLK2 normal)
0 0 1 - Extended by 0.5 CLK2
0 1 0 - Extended by 1.0 CLK2
0 1 1 - Extended by 1.5 CLK2
1 0 0 - Extended by 2.0 CLK2
1 0 1 - Extended by 2.5 CLK2
1 1 0 - Extended by 3.0 CLK2
1 1 1 - Extended by 3.5 CLK2

Bits 01, 00 - NP_WS, Non-page Wait States

NP_WS makes it possible to unconditionally add wait states to all DRAM cycles. Condional wait states may be added to read after write cycles, EMS accesses and interleave miss cycles, with NP_RAW (bit 12).

NP_WS
01 00

0 0 - No wait states added
0 1 - 1 Wait state added
1 0 - 2 Wait states added
1 1 - 3 Wait states added

TIMING	NUMBER OF CLK2'S	
	MODE-00	MODE-01
Row address to RAS	2	2
RAS width	3 + NPH + NPHB / 2	1 + NPH + NPHB / 2
Row address hold	1	0.5
Column address setup (read)	1 + NPRF / 2	0.5 + NPRF / 2
Column address setup (write)	1 + NPWF / 2	1 + NPWF / 2
RAS hold (read from CAS)	1 + NPHB / 2 - NPRF / 2 + NPH	0.5 - NPRF / 2 + NPH
RAS hold (write)	1 + NPHB / 2 - NPWF / 2 + NPH	0.5 - NPWF / 2 + NPH
CAS width (read)	① + NPCAS + NPCB / 2 - NPRF / 2	① + NPCAS + NPCB / 2 - NPRF / 2
CAS width (write)	① + NPCAS + NPCB / 2 - NPWF / 2	① + NPCAS + NPCB / 2 - NPWF / 2
RAS precharge	2 × (2 + NP_WS) - RAS width	2 × (2 + NP_WS) - RAS width
Column address hold	1 - NPCB / 2	1 - NPCB / 2

① 2 if NPCAS = 0 or 1
1 if NPCAS = 2 or 3

NPWF = Bit 10 NPRF = Bit 08 NPH = Bit 06 NPHB = Bit 05
NPCAS = Bits 04, 03 NPCB = Bit 02 NP_WS = Bits 01, 00

TABLE 6-1B. NON-PAGE MODE TIMING

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6.3.2 Page Mode

Table 6-2. identifies the type of DRAM cycle and number of wait states for the 80286 and 80386SX processors.

	PAGE MODE DRAM CYCLE	WAIT STATES
80286	Write page hit	0
	Write page first access †	1
	Write page miss	2
	Read page hit	0
	Read after write page hit	1
	Read page first access †	2
	Read page miss	3
80286 With Discrete Cache	Write page hit	0
	Write page first access †	1
	Write page miss	2
	Read cache hit	0
	Read cache miss, page hit	1
	Read cache miss, page first access †	3
	Read cache miss, page miss	4
80386SX	Write page hit, pipeline mode	0
	Write page hit, non-pipeline mode	1
	Write page first access, pipline mode †	1
	Write page miss, pipeline mode	2
	Write page miss, non-pipeline mode	3
	Read page hit, pipeline mode	0
	Read page hit, non-pipeline mode	1
	Read after write page hit, pipeline mode †	1
	Read page first access non-pipeline mode †	3
	Read page miss, pipeline mode	3
	Read page miss, non-pipeline mode	4
80386SX With Discrete Cache, Non-pipe	Write page hit	0
	Write page first access †	1
	Write page miss	2
	Read cache hit	0
	Read cache miss, page hit	1
	Read cache miss, page first access †	3
	Read cache miss, page miss	4

† Equal Bank sizes, non-EMS cycle

First access is a page mode memory cycle which immediately follows a refresh, DMA or master cycle. It is not necessary for the DRAMs to be precharged for a first access cycle, since all RAS signals have been high in the previous cycle. This shortens a first access page mode cycle by one wait state. For example, a read page miss, non-pipeline mode in 80386SX mode is four wait states. A read page miss, non-pipeline mode, first access in 80386SX mode is three wait states. All installed DRAMs must be the same size and configuration and the memory cycle cannot be an EMS cycle for a first access to occur.

TABLE 6-2. PAGE MODE WAIT STATES

6.3.3 Memory Address Multiplexer

The memory address multiplexer generates the DRAM row and column address. The DRAM address multiplexer is designed so that the same type socket may be used for 64 Kbyte, 256 Kbyte, 1 Mbyte or 4 Mbyte SIMM memory modules.

	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
	64 KBITS NON-INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A9
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	64 KBITS 2-WAY INTERLEAVE OR 256K NON-INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	64 KBITS 4-WAY INTERLEAVE, 256K 2-WAY INTERLEAVE, 1MBITS NON-INTERLEAVE OR 512 KBITS X 8 2-WAY INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	256 KBITS 4-WAY INTERLEAVE, 1 MBITS 2-WAY INTERLEAVE, 4 MBITS NON-INTERLEAVE OR 512 KBITS X 8 4-WAY INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	1 MBITS 4-WAY OR 4 MBITS 2-WAY INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A13	A23	A21	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	4 MBITS 4-WAY INTERLEAVE											
ROW	A13	A22	A20	A18	A16	A15	A14	A24	A23	A21	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	512K X 8 DRAM: NON-INTERLEAVE											
ROW	A13	A22	A19	A18	A16	A15	A14	A13	A12	A11	A10	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	1M X 16 DRAM: NON-INTERLEAVE											
ROW	A13	A9	A19	A18	A16	A15	A14	A20	A12	A11	A10	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	1M X 16 DRAM: 2-WAY INTERLEAVE											
ROW	A13	A10	A21	A18	A16	A15	A14	A20	A12	A11	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	1M X 16 DRAM: 4-WAY INTERLEAVE											
ROW	A13	A22	A21	A18	A16	A15	A14	A20	A12	A11	A19	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1

TABLE 6-3. PAGE MODE DRAM ADDRESS MULTIPLEXER CONFIGURATION

	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
	2M X 8 DRAM: NON-INTERLEAVE											
ROW	A13	A21	A19	A18	A16	A15	A14	A20	A12	A11	A10	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	2M X 8 DRAM: 2-WAY INTERLEAVE											
ROW	A13	A21	A19	A18	A16	A15	A14	A20	A12	A11	A22	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	2M X 8 DRAM: 4-WAY INTERLEAVE											
ROW	A13	A21	A19	A18	A16	A15	A14	A20	A12	A23	A22	A17
COL	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	REFRESH ADDRESS											
ROW		A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

TABLE 6-3. PAGE MODE DRAM ADDRESS MULTIPLEXER (Continued)

	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	
ROW	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	ALL
COL	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A9	64 Kb
COL	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A10	A17	256 Kb
COL	A13	A22	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17	1 Mb or 512 Kb x 8
COL	A13	A22	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17	4 Mb

TABLE 6-4. NON-PAGE, NON-INTERLEAVE ADDRESS CONFIGURATION

	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	
ROW	A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A13	ALL
COL	A13	A22	A20	A18	A16	A15	A14	A17	A12	A11	A10	A9	64 Kb
COL	A13	A22	A20	A18	A16	A15	A14	A19	A12	A11	A10	A17	256 Kb
COL	A13	A22	A20	A18	A16	A15	A14	A21	A12	A11	A19	A17	1 Mb or 512 Kb x 8
COL	A13	A22	A20	A18	A16	A15	A14	A12	A23	A21	A19	A17	4 Mb

TABLE 6-5. NON-PAGE, NON-INTERLEAVE ADDRESS CONFIGURATION

6.4 EMS

6.4.1 EMS Control And Lower EMS Boundary

Port Address 6872H - Read and Write

15	14	13	12	11	10	09	08
INC	PF_LOC			EMS_EN			

07	06	05	04	03	02	01	00
EN_RES	A23	A22	A21	A20	A19	A18	A17
	LOWER_EMS_BOUNDARY						

Signal Name	Default At RSTIN
INC	0
PF_LOC	00
Bits 12, 09, 08	None
EMS_EN	00
EN_RES	0
A23-A17	0

Bit 15 - INC, Increment EMS Pointer

The INC bit controls whether or not the EMS Pointer at Port E072H is to be incremented after each read or write of the EMS Page Register at Port E872H.

INC = 0 -
The EMS pointer does not increment (Default value).

INC = 1 -
EMS pointer increments after access to EMS Page Register.

Bits 14-13 - PF_LOC, Upper Page Frame Location

PF_LOC determines the starting location of a block eight frames. See Table 6-6 for the upper page frame assignments.

PF_LOC
14 13

0 0 - Upper page frame starts at C4000H (Default value)

0 1 - Upper page frame starts at C8000H

1 0 - Upper page frame starts at CC000H

1 1 - Upper page frame starts at D0000H

Bit 12 - Not used, state is ignored

Bits 11, 10 - EMS_EN, EMS Enable

EMS_EN determines whether all EMS frames are to be enabled, only the upper page frames or no page frames. Tables 6-6 and 6-7 show the upper and lower page frame assignments.

EMS_EN
11 10

0 0 - Disable EMS (Default value)

0 1 - Enable EMS Register programming without having to enable a Page Frame. This is useful for initializing the lower Page Frame.

1 0 - Enable upper Page Frame assignments and EMS register programming.

1 1 - Enable upper and lower Page Frame assignments and EMS register programming.

Bits 09, 08 - Not used, state is ignored

Bits 07 - EN_RES, Enable Lower Boundary

EN_RES determines whether A23 through A17 (bits 06 through 00 of this register) are to be used as the lower EMS boundary or ignored.

When the LOWER_EMS_BOUNDARY is enabled, the memory above the boundary is removed from the extended memory and reserved for EMS.

EN_RES = 0 -
Ignore LOWER_EMS_BOUNDARY (Default value)

EN_RES = 1 -
Enable LOWER_EMS_BOUNDARY

Bits 06-00 - A23-A17, LOWER_EMS_BOUNDARY

The lower_EMS_boundary provides address bits A23 through A17 and determines the starting address.

This address must be set to 128 Kbyte below the actual start address. For example, to start EMS at the 1 Mbyte boundary, this field should be set to 07H.

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6.4.2 EMS Page Register Pointer

Port Address E072H - Bits 15-06 Read only,
Bits 05-00 Read and Write

15	14	13	12	11	10	09	08
DLT							
16	15	15	13	12	11	10	9

07	06	05	04	03	02	01	00
DLT		POINTER					
8	7						

Signal Name	Default At RSTIN
DLT	0-0
POINTER	0

The EMS Page Register Pointer is used as an indirect address register. It is loaded with the EMS Page Register Number, ranging from 00 to 39 decimal. If the INC bit is set in Port 6872H, the EMS Page Register Pointer is incremented after each read or write of the EMS Page Register at Port E872H. Tables 6-6 and 6-7 shows the EMS Page Register Pointer value and the page frame assignments.

Bits 15-06 - DLT, Delay Line Test

In the Delay Line Test Mode, these bits represent the state of internal Delay Line signals.

The Delay Line Test is initiated by bit 8 (TDL) in the Test Enable Register at Port Address A872H.

Bits 05-00 - POINTER, EMS Page Register Number

Decimal number, 00 through 39. When programming this field, the hex equivalent 00 through 27H should be used.

EMS REG NUM	PF_LOC = 00	EMS REG NUM	PF_LOC = 01	EMS REG NUM	PF_LOC = 10	EMS REG NUM	PF_LOC = 11
32	E0000-E3FFF	33	E4000-E7FFF	34	E8000-EBFFF	35	EC000-EFFFF
39	DC000-DFFFF	32	E0000-E3FFF	33	E4000-E7FFF	34	E8000-EBFFF
38	D8000-DBFFF	39	DC000-DFFFF	32	E0000-E3FFF	33	E4000-E7FFF
37	D4000-D7FFF	38	D8000-DBFFF	39	DC000-DFFFF	32	E0000-E3FFF
36	D0000-D3FFF	37	D4000-D7FFF	38	D8000-DBFFF	39	DC000-DFFFF
35	CC000-CFFFF	36	D0000-D3FFF	37	D4000-D7FFF	38	D8000-DBFFF
34	C8000-CBFFF	35	CC000-CFFFF	36	D0000-D3FFF	37	D4000-D7FFF
33	C4000-C7FFF	34	C8000-CBFFF	35	CC000-CFFFF	36	D0000-D3FFF
EMS registers 32 through 39 (decimal) can be individually enabled or disabled by the EN (bit 15) of the EMS Page Register. See Port E872H description.							

TABLE 6-6. UPPER PAGE FRAME ASSIGNMENTS

EMS REG NUM	HEX	DEC	EMS REG NUM	HEX	DEC
23	5C000-5FFFF	368K-384K	7	9C000-9FFFF	624K-640K
22	58000-5BFFF	352K-368K	6	98000-9BFFF	608K-624K
21	54000-57FFF	336K-352K	5	94000-97FFF	592K-608K
20	50000-53FFF	320K-336K	4	90000-93FFF	576K-592K
19	4C000-4FFFF	304K-320K	3	8C000-8FFFF	560K-576K
18	48000-4BFFF	288K-304K	2	88000-8BFFF	544K-560K
17	44000- 47FFF	272K-288K	1	84000-87FFF	528K-544K
16	40000-43FFF	256K-272K	0	80000-83FFF	512K-528K
15	3C000-3FFFF	240K-256K	31	7C000-7FFFF	496K-512K
14	38000-3BFFF	224K-240K	30	78000-7BFFF	480K-496K
13	34000-37FFF	208K-224K	29	74000-77FFF	464K-480K
12	30000-33FFF	192K-208K	28	70000-73FFF	448K-464K
11	2C000-2FFFF	176K-192K	27	6C000-6FFFF	4320-448K
10	28000-2BFFF	160K-176K	26	68000-6BFFF	416K-432K
9	24000-27FFF	144K-160K	25	64000-67FFF	400K-416K
8	20000-23FFF	128K-144K	24	60000-63FFF	384K-400K

EMS registers 0 through 31 (decimal) are enabled or disabled as a block. If the EMS_EN field of Port 6872H is 11, the EMS registers 0 through 31 are enabled and the EN (bit 15) of the EMS Page Register is treated as a one. See Port E872H description.

TABLE 6-7. LOWER PAGE FRAME ASSIGNMENTS

6.4.3 EMS Page Register

Port Address E872H - Bits 14-12 Read only, Bits 15, 11-00 Read and Write

There are 40 EMS Page Registers accessible through Port E872H. Only EMS registers 32 through 39 are initialized to zero. EMS registers 0 through 31 are not initialized. The EMS Page Register Pointer at Port E072H provides the offset location for Port E872H.

15	14	13	12	11	10	09	08
EN	0	0	0	P11	P10	P9	P8

07	06	05	04	03	02	01	00
P7	P6	P5	P4	P3	P2	P1	P0

Signal Name	Default At RSTIN
EN	0
Bits 14-12	0
P11-P0	0

Bit 15 - EN, Enable EMS Page Register

EMS Page Registers 32 through 39 can be individually enabled or disabled by the EN bit. EMS Page Registers 0 through 31 are enabled or disabled as a block by the setting of the EMS_EN field in the EMS Control Register at Port 6872H. When EMS_EN equals 11, the EN bit in this register is treated as a one for the lower Page Frame.

EN = 0 -
This EMS Page Register is disabled

EN = 1 -
This EMS Page Register is enabled

Bits 14-12 - Read only, not used by the System Controller

Bits 11-00 - P11 through P00, EMS Page Number

EMS page numbers 8 through 39 and 64 through 2047 are supported for on-board memory, equal to 31.5 MBytes of EMS memory. The memory address is generated by reading the EMS page number from the System Controller and multiplying it by 16 Kbytes, then adding the lower 14 bits of the processor address to the product. This results in EMS page numbers zero through seven being mapped to the lower 128 Kbytes of memory and On-board extended memory being able to be accessed in real mode via the EMS logic.

EMS page numbers 2048 through 2303, equal to 4 MBytes, are used for external EMS memory, providing a method of accessing plug-in RAM or ROM cards. If P11 is 1 when an external EMS access occurs, EMS page number bits P7 through P0 are output on RA0-7/ED0-7 and the EMS chip select is asserted. The RAM/ROM card should access data on the expansion data bus, using $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{MEMCS16}}$ and IOCHRDY to make the transfer.

NOTE

When using external EMS memory with P11 = 1, EN (bit 15) must be 0.

7.0 CACHE CONTROLLER

The Cache Controller provides an effective way to increase the memory bandwidth by storing the most frequently used data in the internal Cache DATA RAM. The WD7910 provides both software and hardware mechanisms to assure coherency of the data between CPU, DMA and Bus Master cycles. During DMA/Master write cycles, the controller will compare the system address and the tag contents. If the address matches, the data will be written into the data RAM. The cache can also be flushed by writing to the flush register.

7.1 CACHE ARCHITECTURE

The cache controller contains of eight functional blocks.

- Processor Interface
- TAG RAM
- DATA RAM
- SNOOP Interface
- Non-cacheable Control
- Diagnostic Control Logic
- LRU
- Flush

Figure 7-1 shows a block diagram of the cache.

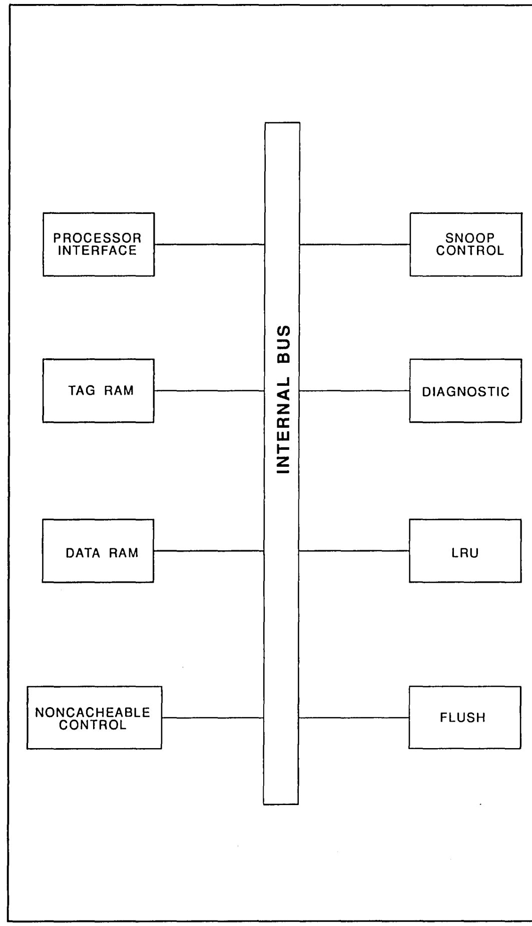

FIGURE 7-1. CACHE CONTROLLER FUNCTIONAL DIAGRAM

7.1.1 Processor Interface

The processor interface supports the 80386SX in both pipeline and non-pipeline mode. It keeps track of the 80386SX processor states a generates READY for read hit cycles. It ignores all the I/O and co-processor cycles.

7.1.2 TAG RAM

BIST (Built-In-Self-Test)logic is included in the TAG RAM to reduce test time.

The internal TAG RAM is organized as two sets of 256 x 21 self-timed synchronous static RAM. Twelve bits are used to store A12:23 from the processor; 8 bits are used to store the demultiplexed A1:3 as line valid, and 1 bit is used as block valid. The block valid bit can be cleared by the FLUSH function which flushes the cache contents and causes block miss for all the subsequent cycles.

A4 through A11 from the 80386SX selects one of the entries from each set. The output from the TAG RAM is compared against the address (A12:23,A1:A3) from the processor. If the address is the same and the corresponding line valid and block valid bits are set, a cache hit cycle is activated. If an address match occurs when the block valid bit is set, and the line valid is clear, it is a line miss. On the other hand, if the address does not compare or the block valid bit is clear, it is a block miss cycle.

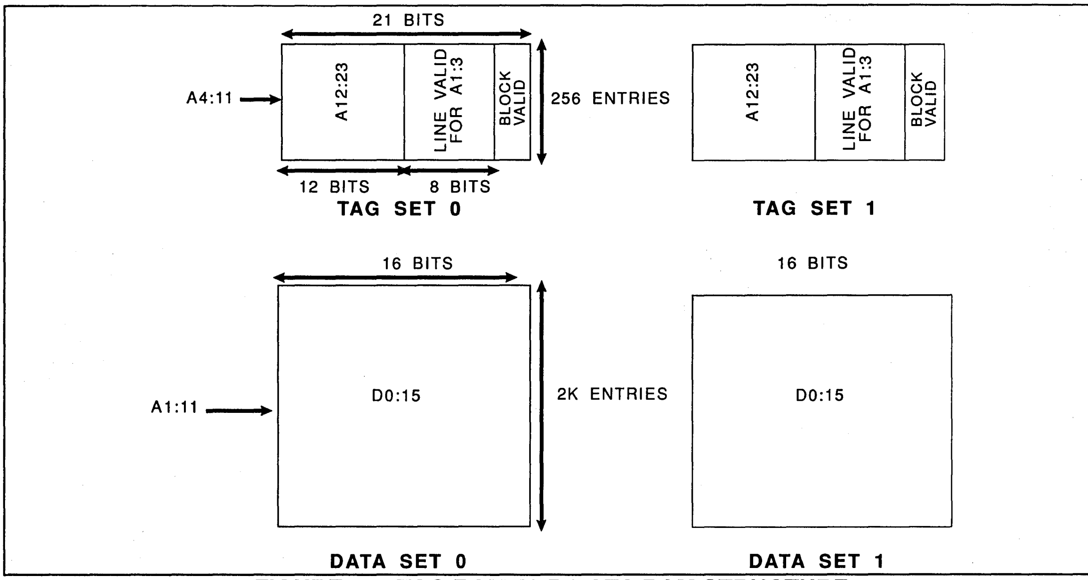

FIGURE 7-2. TAG RAM AND DATA RAM STRUCTURE

During the read block miss cycle, the address is written into the TAG RAM, the block valid bit is set, and the corresponding line valid bit is set.

During the read line miss cycle, the corresponding line valid bit is set, and all other bits are not altered.

Address Compare	Line Valid	Block Valid	
X	X	0	Block Miss
0	X	1	Block Miss
1	0	1	Line Miss
1	1	1	Hit

During a memory write cycle, the contents of the TAG RAM is not affected. The Block size of the TAG RAM is eight lines and each line is 2 bytes. The TAG RAM enters low power mode during Full Power Down to conserve power.

7.1.3 Data RAM

The internal DATA RAM is organized as 2 sets of 2K x 16. During a read hit cycle, the data is provided by one of the sets of DATA RAM to the processor. During a read miss cycle, the data is provided by the DRAM to the processor and is written into the DATA RAM. If the read cycle is a page hit, it will be a one wait state cycle. If it is a page miss, it will be a four wait states cycle. See Section 13.4, Cache Controller Timing.

During a write hit cycle, the data from the processor is written into the DATA RAM to maintain data coherency. In a write miss cycle, either block miss or line miss, no action is taken and DATA RAM contents are not affected. See Section 13.4, Cache Controller Timing.

The DATA RAM enters low power mode during Full Power Down to conserve power. BIST logic is included in the DATA RAM to reduce test time.

7.1.4 Snoop Interface

The Snoop interface maintains the data coherency when DMA or Master cycles take place. When a DMA or Bus Master write cycle occurs, the Snoop logic will update the data in the DATA RAM if the address from DMA or the Bus Master is the same as the corresponding TAG address(Hit cycle). If no match is indicated (Miss cycle), the DATA RAM will not be updated. See Section 13.4, Cache Controller Timing.

7.1.5 Non-cacheable Control

Two user definable and twelve standard non-cacheable regions are provided. Ten of the twelve standard regions are 16KB increments from C8000H - EFFFFH. These regions can be used as EMS memory or for DOS 5.0 Upper Memory Blocks and can be enabled or disabled individually. The other two standard non-cacheable regions are the video BIOS area (C0000-CXFFF or E0000-EFFFF) and the system BIOS area (F0000-FFFFF). The Non-cacheable control logic allows cacheing of these regions to be enabled or disabled individually.

The two user definable non-cacheable regions can also be enabled individually. The non-cacheable regions are set by the upper and lower limit registers. These regions are assigned on 4Kbyte boundaries anywhere in the 16MB physical address space of the 80386SX.

The typical applications of these user defined noncacheable areas are the memory between 512KB and 640KB, and the memory accessed on the AT bus. When powered up, the WD7910 assumes all the memory from 0KB to 640KB and 1M to 16MB are cacheable. It is necessary to have the BIOS to program the noncacheable region registers.

7.1.6 Diagnostic Control Logic

The function of the diagnostic control logic, when enabled, is to map the internal TAG RAM and LRU RAM to address 20000H and DATA RAM to address 40000H. In this mode, memory accesses to these address ranges are diverted to the internal TAG RAM and DATA RAM. This permits the system BIOS to test the internal DATA RAM and TAG RAM.

During Diagnostic Access, the 21-bit TAG RAM (D20:0) and the 2-bit LRU RAM (L1:0) are concatenated to 23 bits and mapped into the Address Space by using A1 to determine whether the data presented is TAG RAM bits D20-D9 (A1 Low) or TAG RAM bits {L1:0,D8:0} (A1 high). Since the LRU RAM has 128 entries (See Section 3.1.7) whereas the TAG RAM has 256 entries, so address A4 has no effect on the selection of the LRU RAM.

7.1.7 LRU

The LRU section has 128 entries and each entry has 2 bits. Addresses 11:5 are used to select one of the entries and Address 4 is used to select one of the two bits. In the event of a read miss, either group can be updated with new data. The LRU bit of the corresponding entry flags the candidate for replacement. Once the replacement is done, LRU bit of the corresponding entry is changed and pointed to the other set. In the event of read hit, the LRU bit of the corresponding entry points to the other set. During a write hit cycle, the corresponding LRU bit is changed and pointed to the other set. The LRU bit is not changed for write miss cycles. All the entries are reset to zero by NRESIN.

7.1.8 Flush

Flush is used to clear all the block valid bits in the TAG RAM and to clear all the LRU bits. This force the cache controller to rebuild the cache contents and force all the subsequent fetch to the DRAM. This is used after an EMS page change.

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7.2 CACHE CONTROL REGISTER

Port Address C472 Read / Write

15	14	13	12	11	10	09	08
C_ ENBL	C_ SSB	C_ DIAG	C_ SVB	MFR	C_M	HI_ME M9	HI_ME M8

07	06	05	04	03	02	01	00
HI_ME M7	HI_ME M6	HI_ME M5	HI_ME M4	HI_ME M3	HI_ME M2	HI_ME M1	HI_ME M0

Bit 15 - C_ENBL, Cache Enable

This bit is used to enable the cache controller. Before writing to this bit, the memory controller must be programmed to support the cache mode. This can be done by writing (01) to bit 13 and 12 of register 3872. When this bit is changed, a hold acknowledge cycle is required before the change goes into effect.

C_ENBL= 1 Cache Enable
C_ENBL= 0 Cache Disable (Default)

Bit 14 - C_SSB, Cache Shadowed System BIOS at F0000H through FFFFFH

When the System BIOS is shadowed, it can also be cached to increase the system BIOS performance.When this bit is changed, a hold acknowledge cycle is required before the change goes into effect.

C_SSB = 1 Enable caching of shadow RAM. When Custom mode is enabled, the address from 0F0000H - 0F0FFFH is not cached.

C_SSB = 0 Disable caching of shadow RAM (Default)

Bit 13 - C_DIAG, Cache Diagnostic Mode

Enabling the cache and this bit puts the cache into diagnostic mode as described in section 7.1.6. When this bit is changed, a hold acknowledge cycle is required before the change goes into effect.

C_DIAG = 1 Cache is in diagnostic mode

C_DIAG = 0 Standard cache mode (Default)

Bit 12 - C_SVB, Cache Shadowed Video BIOS at E0000H through EFFFFH or C0000H through CXXXXH

When the Video BIOS is shadowed, it can also be cached to increase the Video BIOS performance.When this bit is changed, a hold acknowledge cycle is required before the change goes into effect.

C_SVB = 1 Enable Cacheing Video BIOS

C_SVB = 0 Disable Cacheing Video BIOS (Default)

Bit 11 - C_MFR, Manufacturing Test Bit

Bit 10 - C, Cache Mode

C = 1 2-way set associative
C = 0 Direct-mapped (Default)

Bits 9:0 - HI-MEM, High memory region caching control. Setting these bits enables the caching of the HI-MEM region. Default after reset is 0.

BIT 9 EC000H - EFFFFH
BIT 8 E8000H - EBFFFH
BIT 7 E4000H - E7FFFH
BIT 6 E0000H - E3FFFH
BIT 5 DC000H - DFFFFH
BIT 4 D8000H - DBFFFH
BIT 3 D4000H - D7FFFH
BIT 2 D0000H - D3FFFH
BIT 1 CC000H - CFFFFH
BIT 0 C8000H - CBFFFH

Bits 9:0 = 1, Enable caching
Bits 9:0 = 0, Disable caching

7.2.1 Noncacheable Region 1 Upper Boundary

Port Address BC72. Read/Write

15	14	13	12	11	10	09	08
A23	A22	A21	A20	A19	A18	A17	A16

07	06	05	04	03	02	01	00
A15	A14	A13	A12	S_ REF	INT_ DIS	INT_ ST	S_ IO RDY

This register determines the upper address boundary of the user defineable noncacheable region 1. Default after reset is zero.

Bits 15:4, = A23: 12 of the upper address boundary

Bit 3, Slow Refresh

When this bit is set, the DRAM refresh rate is slowed down to 120µs. This bit does not affect the refresh toggle bit in Port 61.

Bit 3 = 1, Enable Slow Refresh

Bit 3 = 0, Disable Slow Refresh (Default)

Bit 2, Interrupt Disable

When this bit is set, the interrupt from the interrupt controller is disabled. The command will not take effect immediately if the interrupt request signal from the interrupt controller is active. The command will take effect immediately if the interrupt request signal is inactive. This allows control of the interrupt regardless of the Operating system privilege level.

Bit 2 = 1, Disable the hardware interrupt from the interrupt Controller

Bit 2 = 0, Enable hardware interrupt.

Bit 1, Interrupt Disable Status (Read Only)

This enables reading of Interrupt Status regardless of Operating System privilege Level.

Bit 1 = 1, Indicates the Interrupt Disable command is pending

Bit 1= 0, Indicates the Interrupt Disable command is processed

Bit 0, SNOOP with IOCHRDY active

During periods when the CPU Clock is slower than the AT BUS clock (slowed for power savings), the Snoop Logic may be unable to properly track the memory cycle during DMA or BUS Master Cycles. Setting this bit enables the WD7910 to use the IOCHRDY signal to lengthen the cycle.

Bit 0 = 1, Enable IOCHRDY for DMA/Master cycle

Bit 0 = 0, Disable IOCHRDY for DMA/Master cycle (Default)

7.2.2 Noncacheable Region 1 Lower Boundary

Port Address B472. Read/Write

15	14	13	12	11	10	09	08
A23	A22	A21	A20	A19	A18	A17	A16

07	06	05	04	03	02	01	00
A15	A14	A13	A12	S DMA_ CLK	X_ WS	S_ BIST	BIST _S

This register determines the lower address boundary of the user defineable noncacheable region 1. Noncacheable region 1 is disabled when the upper boundary is set below the lower boundary. Default after reset is zero.

Bits 15:4, A23: 12 of the lower address boundary.

Bit 3, Stop DMA Clock

Setting this bit causes the DMA clock to stop while there is no DMA activity. Upon any DMA request (DRQn), the DMA clock starts up again and continues to run until 16 DMA clocks after the end of the DMA Acknowledge (DACKn).

Bit 3 = 1, Enable Stop DMA Clock

Bit 3 = 0, Disable Stop DMA Clock (Default)

Bit 2, Extra Wait State for Page Mode

If this bit is active, it adds an extra wait state to all the memory cycles. With this featury system manufacturer can use slower DRAM for WD7910 system without loss of huge performance and achieve saving since the majority of the memory access are directly to the internal cache.

Bits 1, Start BIST

Setting bit 1 forces the BIST to check the TAG RAM and DATA RAM. The result can be checked by reading BIT 0. Bit 0 is a read only register.

Bit 0, BIST Status

Bit 0 = 1, RAM error.

Bit 0 = 0, No error found.

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7.2.3 Noncacheable Region 2 Lower Boundary

Port Address CC72 Read/Write

15	14	13	12	11	10	09	08
A23	A22	A21	A20	A19	A18	A17	A16

07	06	05	04	03	02	01	00
A15	A14	A13	A12				NR 2C

This is used to determine the lower address boundary of the user defineable noncacheable region 2. Any address above or equal to this address is considered non-cacheable. Default after reset is zero.

Bits 15:4, A23: 12 of the lower address boundary

Bits 3:1, Test Register

For Factory use only.

Bit 0, Non-cacheable Region 2

Bit 0 = 1, enables non-cacheable Region 2
Bit 0 = 0, disables non-cacheable Region 2 (default)

7.2.4 Flush

Port Address F872H Write Only

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00

Signal Name	Default At RSTIN
All signals	None

Writing to this I/O port with any data will clear all the valid bits in the TAG RAM. This is ordinarily used to clear the cache when there is a change to the EMS page register and also causes the WD7910 to output Chip Select number 13H.

8.0 PORT CHIP SELECT AND WD7910LP REFRESH

This section describes refresh control logic peculiar to the WD7910LP and used by the power down feature. This section also describes the registers used to control the following functions:

- Port chip select and control
- High speed hard disk access
- AT hard disk IDE mode
- 8/16 bit 80287 bus timing
- Real-Time Clock bus location
- Access to the CMOS RAM password

Table 8-1 identifies the ports, their Chip Select number, I/O address and function.

8.1 REFRESH CONTROL, SERIAL AND PARALLEL CHIP SELECTS

Port Address 2072H - Read and Write

15	14	13	12	11	10	09	08
M_REF	V_REF	CBR_REF	CBR_SR	SCSI	PAR		PAR_L

07	06	05	04	03	02	01	00
SER_A			SER_AL	SER_B			SER_BL

Signal Name	Default At RSTIN
M_REF †	0
V_REF †	0
CBR_REF †	0
CBR_SR	0
SCSI	0
PAR	00
PAR_L	0
SER_A	000
SER_AL	0
SER_B	000
SER_BL	0

† Featured only in the WD7910LP

Bit 15 - M_REF, Memory Refresh Power Down Mode
Featured only in the WD7910LP

The refresh period may be lengthened for extended refresh DRAM while maintaining bus compatibility. When slow refresh is selected, main on-board memory is refreshed at one eighth the normal rate. In the Full Power Down mode, selected by the FPD bit in the register at Port 1872H, and M_REF = 1, the on-board DRAM is refreshed with every eighth NPDREF. NPDREF is a 64 KHz input signal supplied by the WD76C20.

M_REF = 0 -
Normal refresh period for main on-board memory (Default value).

M_REF = 1 -
Slow refresh main on-board memory.

Bit 14 - V_REF, Video Refresh Power Down Mode
Featured only in the WD7910LP

The refresh period may be lengthened for extended refresh DRAM while maintaining bus compatibility. When slow refresh is selected, main on-board memory is refreshed at one eighth the normal rate. In the Full Power Down mode, selected by the FPD bit in the register at Port 1872H, and V_REF = 1, the on-board DRAM is refreshed with every eighth NPDREF. NPDREF is a 64 KHz input signal supplied by the WD76C20.

V_REF = 0 -
Normal refresh period for video memory (Default value)

V_REF = 1 -
Slow refresh video memory

Bit 13 - CBR_REF, CAS Before RAS Refresh For On-board DRAM
Featured only in the WD7910LP

Most standard DRAMs support this type of CAS before RAS refresh, while special DRAMs do not.

CBR_REF = 0 -
Normal refresh for on-board DRAM (Default value)

CBR_REF = 1 -
CAS before RAS refresh

Bit 12 - CBR_SR, CAS Before RAS Self Refresh

CAS before RAS self refresh is supported only by special DRAMs.

CBR_SR = 0 -
No CAS before RAS self refresh (Default value)

CBR_SR = 1 -
CAS before RAS self refresh of DRAM is supported during suspend and resume, where CAS is held low continuously while in suspend.

Bit 11 - SCSI, Small Computer System Interface Chip Select

The SCSI is selected by chip select number 12. See Table 8-1.

SCSI = 0 -
SCSI chip select disabled (Default value)

SCSI = 1 -
SCSI chip select at I/O port 353XH

Bits 10, 09 - PAR, Parallel Port Chip Select

The parallel port is selected by chip select number 0FH and may be located at I/O address 278H through 27FH, 378H through 37FH, or 3BCH through 3BFH. Bits 10 and 09 may disable the chip select or locate it at one of three areas. See Table 8-1.

PAR
10 09

0 0 - PAR chip select disabled (Default value)

0 1 - PAR chip select at I/O port 3BCH - 3BFH

1 0 - PAR chip select at I/O port 378H - 37FH

1 1 - PAR chip select at I/O port 278H - 27FH

Bit 08 - PAR_L, Parallel Port Bus Location

PAR_L = 0 -
Parallel port is located on the RA0-7/ED0-7 bus. This is typical when the WD76C30 is used.

PAR_L = 1 -
Parallel port is located on the expansion data bus.

Bits 07, 06, 05 - SER_A, Serial Port A Chip Select

The serial port A is selected by chip select number 0EH and may be located at I/O address 2E8H through 2EFH, 2F8H through 2FFH, 3E8H through 3EFH or 3F8H through 3FFH. Bits 07, 06, and 05 may disable the chip select or locate it at one of the four areas. See Table 8-1.

It is possible to select the same I/O port address for serial port A and serial port B. Selecting the same address for both ports results in an unpredictable response and should not be done.

SER_A
07 06 05

0 0 0 - Serial port A chip select disabled (Default value)

0 0 1 - Serial port A chip select at I/O port 3F8H - 3FFH

0 1 0 - Serial port A chip select at I/O port 2F8H - 2FFH

0 1 1 - Serial port A chip select at I/O port 3E8H - 3EFH

1 0 0 - Serial port A chip select at I/O port 2E8H - 2EFH

Bit 04 - SER_AL, Serial A Port Bus Location

SER_AL = 0 -
Serial port A is located on the RA0-7/ED0-7 bus. This is typical when the WD76C30 is used.

SER_AL = 1 -
Serial port A is located on the expansion data bus.

Bits 03, 02, 01 - SER_B Serial Port B Chip Select

The serial port B is selected by chip select number 10 and may be located at I/O address 2E8H through 2EFH, 2F8H through 2FFH, 3E8H through 3EFH or 3F8H through 3FFH. Bits 03, 02 and 01 may disable the chip select or locate it at one of the four areas. See Table 8-1.

It is possible to select the same I/O port address for serial port B and serial port A. Selecting the same address for both ports results in an unpredictable response and should not be done.

SER_B
03 02 01

0 0 0 - Serial port B chip select disabled (Default value)

0 0 1 - Serial port B chip select at I/O port 3F8H - 3FFH

0 1 0 - Serial port B chip select at I/O port 2F8H - 2FFH

0 1 1 - Serial port B chip select at I/O port 3E8H - 3EFH

1 0 0 - Serial port B chip select at I/O port 2E8H - 2EFH

Bit 00 - SER_BL, Serial B Port Bus Location

SER_BL = 0 -
Serial port B is located on the RA0-7/ED0-7 bus. This is typical when the WD76C30 is used.

SER_BL = 1 -
Serial port B is located on the expansion data bus

8.2 RTC, PVGA, 80287 TIMING, AND DISK CHIP SELECTS

Port Address 2872H - Read and Write

Bits 12 through 07 and Port Address 3072H control the use and location of the Programmable Chip Select.

15	14	13	12	11	10	09	08
RTC_L	FST_VGA	FST_SCSI	EN_PCS1	U_MSK1	L_MSK1		

07	06	05	04	03	02	01	00
PRG_L	HS_HD		P/S	HS_287	LK_PSW	DS_HD	DS FLP

Signal Name	Default At RSTIN
RTC_L	0
FST_VGA	0
FST_SCSI	0
EN_PCS	0
U_MSK1	00
L_MSK1	00
PRG L	0
HS HD	000
P/S	000
HS 287	0
LK PSW	0
DS HD	0
DS FLP	0

Bit 15 - RTC_L, Real-Time Clock

The Real-Time Clock is normally on the RA0-7/ED0-7 bus but may be placed on the expansion data bus.

RTC_L = 0 -
Real-Time Clock is on the RA0-7/ED0-7 bus (Default value).

RTC_L = 1 -
Real-Time Clock is on the expansion data bus. This is the required setting when the WD76C20 is used.

Bit 14 - FST_VGA, Fast VGA Video

The performance of Western Digital Imaging PVGA display controllers may be enhanced by reducing wait states for access to video I/O. This feature should only be used with Western Digital Imaging PVGA1A, WD90C90, WD90C30, WD90C20, WD90C11 and WD90C10 devices. I/O cycles to eight-bit ports 3C0H - 1H, 3C4H - 5H and 3CEH - FH are made with one wait state cycles.

FST_VGA = 0 -
Normal PVGA control (Default value)

FST_VGA = 1 -
One wait state I/O cycle to PVGA

Bit 13 - FST_SCSI, Fast SCSI

The performance of the WD33C93 SCSI Contoller is enhanced by performing eight-bit accesses with one wait state rather than four wait states.

FST_SCSI = 0 -
Four Wait States (Default value)

FST_SCSI = 1 -
One Wait State

Bit 12 - EN_PCS1, Enable Programmable Chip Select 1

The Programmable Chip Select logic is selected with chip select 11 and may be disabled or enabled. See Table 8-1.

EN_PCS = 0 -
Disable Programmable Chip Select (Default value)

EN_PCS = 1 -
Enable Programmable Chip Select

Bit 11 - U_MSK1, Upper Address Bits Masked

U_MSKI determines whether or not the upper address bits A15 through A10 are to be used as designated in the Programmable Chip Select Address Register at Port 3072H.

U_MSKI = 0 -
A15 through A10 are ignored (Default value).

U_MSKI = 1 -
A15 through A10 are included in the address.

Bits 10, 09, 08 - L_MSK1, Lower Address Bits Masked

L_MSK1 determines whether the lower four address bits A03 through A00 are to be used as designated in the Programmable Chip Select Address Register at Port 3072H.

L_MSK1
10 09 08

0 0 0 - A09 through A00 are included in the address (Default value).

0 0 1 - A00 is ignored.

0 1 0 - A00, A01 are ignored.

0 1 1 - A00, A01, A02 are ignored.

1 0 0 - A00, A02, A03 are ignored, A01 is not ignored, ver. A-F. A00, A01, A02 A03 are ignored, WD76C10A and newer.

Bit 07 - PRG_L, Programmable Chip Select Bus Location

PRG_L = 0 -
Programmable Chip Select is on the RA0-7/ED0-7 bus (Default value).

PRG_L = 1 -
Programmable Chip Select is on the expansion bus.

Bit 06 - HS_HD, High Speed Hard Disk Data Transfer Rate

Enabling the high speed data transfers results in hard disk, 16-bit data transfers to be performed at a compressed timing rate rather than at the compatible bus rate. When operating in the high speed mode, the first data transfer is made at the compatible bus rate. Subsequent accesses to the hard disk port are made at high speed, with $\overline{\text{IOCS16}}$ ignored and the WD76C20 hard disk chip select remaining stable.

NOTE

This feature requires the use of the WD76C20 and should only be used with Western Digital IDE drives WD-AC280, WD-AC140, WD-AC160, WD-AC2120, WD-AP4200, WD-AB130 and WD-AH260.

HS_HD = 0 -
Compatible bus timing enabled (Default value).

HS_HD = 1 -
High speed hard disk accesses enabled.

Bit 05 - Not used, the state is ignored

Bit 04 - P/S, Primary Or Secondary Disk

The P/S bit is only used to select the floppy disk chip select address in the IDE mode. See Table 8-1, chip select numbers 08H through 0BH.

P/S = 0 -
Primary hard disk and Floppy address selected (Default value).

P/S = 1 -
Secondary hard disk and Floppy address selected.

Bit 03 - HS_287, Co-processor 80287 High Speed Timing

Normal I/O read and write access to the 80287 is made with eight bit bus timing. Setting HS_287 results in 16-bit bus timing.

HS_287 = 0 -
Normal 80287 timing (Default value).

HS_287 = 1 -
Fast 80287 timing.

Bit 02 - LK_PSW, Prevent Locking Password

Port 092H bit 3 (Lock_Pass) is used to prevent access to the CMOS RAM password area located at 38H through 3FH. Setting LK_PSW before attempting to set Lock_Pass, inhibits the setting of Lock_Pass. In this instance, it is possible to access the CMOS RAM password area. If Lock_Pass is set before LK_PSW, LK_PSW will have no effect.

LK_PSW = 0 -
Port 092H bit 3, Lock_Pass can be set (Default value).

LK_PSW = 1 -
Port 092H bit 3, Lock_Pass can not be set.

Bit 01 - DS_HD, Hard Disk Chip Select 0CH, 0DH

DS_HD = 0 -
Hard disk chip select is enabled (Default value).

DS_HD = 1 -
Hard disk chip select is not generated.

Bit 00 - DS_FLP, Floppy Disk Chip Select 08H, 09H, 0AH, 0BH

DS_FLP = 0 -
Floppy disk chip select is enabled (Default value).

DS_FLP = 1 -
Floppy disk chip select is not generated.

8.3 PROGRAMMABLE CHIP SELECT ADDRESS

Port Address 3072H - Read and Write

15	14	13	12	11	10	09	08
A15	A14	A13	A12	A11	A10	A09	A08

07	06	05	04	03	02	01	00
A07	A06	A05	A04	A03	A02	A01	A00

Signal Name	Default At RSTIN
All signals	None

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8.4 I/O PORT ADDRESSES AND CHIP SELECT ASSIGNMENTS

Table 8-1 lists the I/O addresses and chip selects generated for each fixed port type. Address bits A15 through A10 are ignored for the I/O addresses listed with three digits. The ports are listed in the sequence of the chip select value.

PORT	I/O ADDRESS (HEX)	CHIP SELECT NUMBER (HEX)	FUNCTION
ROM Chip Select	N/A	00	Chip select for BIOS ROM
Keyboard Control	060 - 06E even	01	Chip select for 8042
80287	00E0 - 00FF	02	Chip select for numeric processor
Power Control	7072	03	PMC Write Strobe 0
Reserved		04	Reserved
Real-time Clock	070	05	RTC ALE
Real-time Clock	071	06	RTC Write Strobe
Real-time Clock	071	07	RTC Read Strobe
Floppy Operation Chip Select	3F2 372	08	Primary address Secondary address
Floppy Chip Select	3F4, 3F5 374, 375	09	Primary address Secondary address
Floppy Control Chip Select	3F7 377	0A	Primary address Secondary address (Floppy enabled, HD disabled)
Floppy and HD Control Chip Select	3F7 377	0B	Primary address Secondary address (Floppy enabled, HD enabled)
Hard Disk Chip Select	1F0, 1F1 - 1F7 170, 171 - 177	0C	Primary address Secondary address
Hard Disk Chip Select	3F6 3F7 † 376 377 †	0D	Primary Address Secondary address
Serial Port A Chip Select	2E8 - 2EF 2F8 - 2FF 3E8 - 3EF 3F8 - 3FF	0E ††	
Parallel Port 0 Chip Select	278 - 27F 378 - 37F 3BC - 3BF	0F	

TABLE 8-1. I/O PORT ADDRESSES AND CHIP SELECT ASSIGNMENTS

PORT	I/O ADDRESS (HEX)	CHIP SELECT NUMBER (HEX)	FUNCTION
Serial Port B Chip Select	2E8 - 2EF 2F8 - 2FF 3E8 - 3EF 3F8 - 3FF	10 ††	
Program Chip Select 1	PROG 1	11	
SCSI	3530 - 353X	12	
Cache Flush	F872	13	
EMS	 F072 F472	14 15 16	External EMS 48 MHz Clock Disabled 48 MHz Clock Enabled
Power Control	7872	17	PMC Write Strobe 1
Floppy Chip Select	3F0 - 3F1 370 - 371	18	Primary address Secondary address
Floppy Chip Select	3F3 373	19	Primary address Secondary address
Program Chip Select2	PROG 2	1A	
Program Chip Select 3	PROG 3	1B	
Reserved		1E	Reserved
Reserved		1F	Reserved

† IDE Hard disk enabled, floppy disabled

†† The Chip Select Number is the decoded value of CS4 - CS0. If the Programmed Chip Select corresponds to any other decode, the Programmed Chip Select is suppressed. If Serial Port A and B are programmed for the same address, Serial Port B Chip Select is suppressed.

TABLE 8-1. I/O PORT ADDRESSES (Continued)

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9.0 POWER MANAGEMENT CONTROL

The WD7910LP supports all PMC inputs, output and interrupt functions.

9.1 SYSTEM ACTIVITY MONITOR (SAM)

The System Activity Monitor (SAM) found in the WD7910LP is a hardware solution to monitoring system activity. SAM was conceived to solve the problems associated with system activity detection in various operating environments such as DOS, Windows, OS/2 and VCPI.

With the WD7910LP a software approach was employed to determine system activity. This software approach was accomplished using a watchdog timer. As a part of the watchdog timer service, the sources of activity are checked and a determination is then made on the state of system activity. This approach does not consider the state of the system activity between watchdog timer interrupts. However, with SAM, the system activity state is continuously monitored through hardware, thus providing a more universal approch to activity detection.

With the help of SAM it is now possible to:

- Provide a trigger when a pre-programmed period of system inactivity time elapses.
- Enable/disable the sources that constitute system activity.
- Select either coarse or fine timeout values for system inactivity period.

System Activity
System activity denotes periods of time in which the system performs useful tasks. The sources Of System Activity are:

- Unmasked pending interrupts.
- Unmasked interrupts in service.
- Access to hard disk data port.
- I/O Access to programmable chip select port.
- DMA transfers.
- Coprocessor cycles.
- A programmable PCU input.
- NMI.

SAM allows for excluding the following interrupt sources from contributing to system activity:

- IRQ 0, used by DOS to keep track of the system time.
- IRQ7, used for spurious interrupts and parallel port interrupts.
- IRQ 8, used by Windows, OS/2 and other multitasking environments to keep the scheduler running.
- A progammable interrupt level used as a power management interrupt.

SAM also takes into account programs such as MOUSE.COM which, in an attempt to locate a mouse on a communication port, generates interrupts on interrupt levels 3 and 4, and leaves them pending. To overcome this problem, SAM allows only the unmasked pending interrupts on 3 and 4 to constitute system activity.

Using SAM for System Power Management:

a) System Timeout Capability

SAM can be programmed to determine coarse periods of inactivity, with the minimum period as one minute, four seconds, up to a maximum period of 16 minutes. It is also possible to extend the maximum limit to any value by reading the Activity Before bit (ACTBEF) in the Activity Monitor Control Register at Port Address B072H.

On reaching the programmed period, SAM generates a Local Attention signal. Typically, the Local Attention is tied to a power management interrupt. In response to Local Attention, the power management interrupt handler makes it possible to prepare the system for a Suspend operation.

b) Responding to a Suspend Request

SAM can be programmed to determine a clean breakpoint for suspending the system upon receiving the Suspend request. At the time the Suspend request is received, it is possible that the system is busy performing an indivisible operation, and it is necessary to wait for the system to finish this indivisible operation before initiating suspend. In order to do this, control to the CPU must be relinquished for just enough time for the CPU to complete the operation. This is referred as Suspend arbitration.

In addition to performing Suspend arbitration, SAM is also responsible for determining the earliest opportunity to initiate the Suspend sequence. For instance, if a Suspend request is caused by a low battery condition, it is imperative that the system be placed in the suspend state as soon as possible. Here the fine granularity of SAM may be used to determine brief periods of inactivity from as low as 7.8 milliseconds to as high as 117.2 milliseconds, and establish a clean breakpoint for Suspending the system.

Advantages of SAM:

1. SAM is a reliable and consistent approach to detecting system activity.

2. SAM is hardware based making it truly non-obtrusive.

3. SAM is independent of the operating environment and the execution mode of the processor.

4. SAM can perform in two modes:

- Detection of system activity for extended periods of time, for the purposes of system timeout.
- Detection of brief periods of inactivity for initiating Suspend.

5. Programmability allows for the control of sources of system activity and setting up coarse and fine timeout values.

6. SAM generates a signal called Local Attention (LCL_ATN) on reaching programmed periods of timeout. This signal is generally tied to an unused IRQ level to invoke the Power Management program.

7. SAM also carries information on DMA activity state. This is used for determining whether it is appropriate to place the processor in the Sleep Mode.

8. SAM makes it possible to read the state of the interrupt controllers and, if needed, reprogram them on Resume. This is provided to handle the spurious interrupts that are generated by devices at powerup time on Resume.

NOTE

SAM cannot be used for determining when the processor should be placed in the Sleep Mode. This determination is intimately tied to the operating environment and is handled by Western Digital's Power Management drivers DOS/VCPI, Windows and OS/2.

9.2 PROCESSOR POWER DOWN MODE

The Processor Power Down Mode is initiated by setting bit 13 of the register at Port Address 1872H to one. The CPURES signal is asserted, then tristated. An internal 200K pullup resistor holds the CPURES active. The Processor Power Down (PMC # 5) signal from the PMC Control Register is used to control the power converter from the processor. The WD7910LP holds CPUCLK, $\overline{\text{READY}}$, HOLD, INTRQ and NMI low to the processor.

The same conditions used to restart a stopped clock also initiate the Power Up Mode. The Power Up Mode is entered by an unmasked DRQ, unmasked IRQ interrupt or a PMC input change, resulting in an unmasked NMI to Port 9072H. A Processor Power Good signal is then input on the PMCIN pin. After 1 ms., PMC Processor Power Good signal is checked for a logic 1 state. At this time, CPURES is driven high and the CPUCLK, $\overline{\text{READY}}$, HOLD, INTRQ and NMI signals are driven to their correct states. CPURES remains asserted for 64 additional CPUCLKs.

The PMC unit is composed of two external chips, 74HCT273 octal latch used for the eight PMC outputs from data bus ED0 - ED7 and a 74HCT151 8:1 multiplexer used for the PMCIN signal. The PMC output latches are cleared at power up (see Figure 5-1).

The keyboard processor may access the WD7910LP's internal registers by way of the PMC logic. The keyboard processor starts a local ac-

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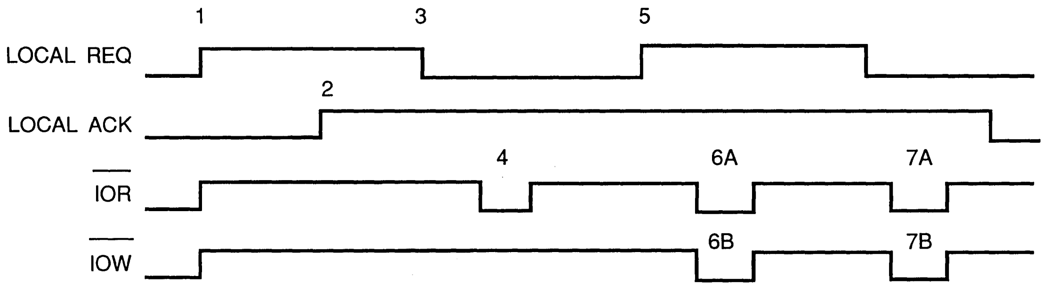
cess by asserting LCL_REQ, which causes PMCIN 2 to be asserted and written in the PMC input register at Port 8872H (see Figure 5-1 and Table 9-2). The WD7910LP arbitrates with refresh, DMA and master for a hold cycle from the processor. When the processor returns a hold acknowledge (HLDA), the WD7910LP asserts LCL_ACK (PMC output 3 from Port 7072H) on the ED0 - ED7 data bus. The keyboard processor then passes the opcode/address byte to the WD7910LP on the data bus and drops the LCL_REQ. The WD7910LP responds by de-asserting LCL_ACK.

If the opcode specified a register write, data high (D15 through D08) and data low (D07 through D00), bytes are passed to the WD7910LP. If the opcode specified an I/O read, the data high and data low bytes are sent from the WD7910LP to the keyboard processor.

All special operation registers within the WD7910LP may be accessed in this manner without first unlocking the register. See section 2.8.2, Port Address F073H, for Lock/Unlock Register. This method allows the keyboard processor to control speed switching and other parameters without host processor intervention.

Figure 9-1 shows the handshake procedure, followed by the keyboard controller and the WD7910LP.

Figures 9-2 and 9-3 represents the powerdown and powerup sequence and control.



1 8042 Requests local data transfer

2 WD7910LP returns LOCAL_ACK after receiving HLDA from the host processor

3 8042 loads address and OPCODE into data register, then drops LOCAL_REQ

4 WD7910LP reads address and OPCODE

5 8042 Reloads data register with high byte, then asserts LOCAL_REQ

6A WD7910LP Reads high byte

7A WD7910LP Read low byte, writes to internal register

FOR READ CYCLE OF WD7910LP INTERNAL REGISTER:

6B WD7910LP Writes high byte to 8042

7B WD7910LP writes low byte to 8042

OP_CODE FORMAT

7	6	5	4	3	2	1	0
DIR	RSV	A15	A14	A13	A12	A11	A10

DIR = 1 - Read register (generates IOW to 8042)

DIR = 0 - Write register (generates IOR to 8042)

FIGURE 9-1. REGISTER ACCESS BY KEYBOARD CONTROLLER

9.3 PMC OUTPUT CONTROL REGISTERS

Port Address 7072H - Bits 07-00 are Read only

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
OUT 7	OUT 6	OUT 5	OUT 4	OUT 3	OUT 2	OUT 1	OUT 0

Signal Name	Default RSTIN
All signals	None

PMC Output Control Bits 7:0

Featured only in the WD7910LP

Port Address 7872H - Bits 07-00 are Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
OUT F	OUT E	OUT D	OUT C	OUT B	OUT A	OUT 9	OUT 8

Signal Name	Default RSTIN
All signals	None

PMC Output Control Bits 15:08

Featured only in the WD7910LP

PMC	PMC OUTPUT SIGNAL PORT 7072H	PMC	PMC OUTPUT SIGNAL PORT 7872H
0H	CPU Clock Driver Enable	8H	User Defined
1H	LCD Enable	9H	User Defined
2H	Backlight Enabled	AH	User Defined
3H	LCL_ACK	BH	User Defined
4H	LCL_ATN	CH	User Defined
5H	Processor powerdown	DH	User Defined
6H	Gate A20	EH	User Defined
7H	Full Powerdown	FH	User Defined

TABLE 9-1. PMC OUTPUT SIGNALS

9.4 PMC TIMERS

Port Address 8072H - Read and Write

When no keyboard or Mouse interrupts have occurred for the time specified by BL_TIMEOUT or LCD_TIMEOUT, PMC Output 1 or 2 is written to the PMC OUTPUT CONTROL 7:0 register at Port Address 7072H (see Table 9-1) to disable the LCD or Backlight. The timer is reset and the Backlight and LCD control re-enabled at the refresh cycle following a Keyboard or Mouse interrupt. The Mouse Interrupts are programmed by bits 01 and 00 (BL_MOU) in the RAM Shadow And Write Protect Register at Port Address 6072H. The same timer is used for the Backlight and LCD timeout.

The timeout delay may be programmed in increments of five seconds, to a maximum of 1,270 seconds, or 21 minutes and 10 seconds.

15	14	13	12	11	10	09	08
BL_TIMEOUT							

07	06	05	04	03	02	01	00
LCD_TIMEOUT							

Signal Name	Default RSTIN
BL_TIMEOUT †	0
LCD_TIMEOUT †	0

† Featured only in the WD7910LP

Bits 15-08 - BL_TIMEOUT, Backlight Time Out

00H - Backlight always disabled
01H - Enabled for 5 seconds
02H - Enabled for 10 seconds

↕

FEH - enabled for 254 x 5 seconds
FFH - Backlight enabled

Bits 07-00 - LCD_TIMEOUT, LCD Time Out

00H - LCD always disabled
01H - Enabled for 5 seconds
02H - Enabled for 10 seconds

↕

FEH - enabled for 254 x 5 seconds
FFH - LCD enabled

9.5 PMC INPUTS

Port Address 8872H - Read and Write

15	14	13	12	11	10	09	08
PMC_UPD	EN_LCL	AF 7	AF 6	AF 5	AF 4	AF 3	AF 2

07	06	05	04	03	02	01	00
IN 7	IN 6	IN 5	IN 4	IN 3	IN 2	IN 1	IN 0

Signal Name	Default At RSTIN
PMC_UPD	0
EN_LCL †	0
AF7-AF2 †	0
IN7-IN0	None

† Featured only in the WD7910LP

Bit 15 - PMC_UPD, Enable PMC Update

PMC_UPD = 0 -
No update cycles occur.

PMC_UPD = 1 -
A change of state of PMC outputs 7 through 0 (Port Address 7072H) or the internal A20 GATE, causes an update cycle of the PMC 7:0 output latch.

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Bit 14 - EN_LCL, Enable Local Request - Featured only in the WD7910LP

EN_LCL enables the PMCIN 2 to initiate a local access of the WD7910LP internal registers from the keyboard controller.

EN_LCL = 0 -
PMCIN 2 is user defined.

EN_LCL = 1 -
PMCIN 2 is LOCAL_REQ.

Bits 13-08 - AF7-AF2, Local Attention Flags Featured only in the WD7910LP

Local attention flags AF7 through AF2 are set to indicate which PMC input(s) have caused LCL_ATN in PMC Interrupt Enable Register at Port C872H to be asserted. To clear the flag and corresponding IN bit in the PMC Inputs Register, it is necessary to clear the corresponding EA bit in PMC Interrupt Enable Register. If both an EA bit and EI bit in the PMC Interrupt Enable Register are set, both must be reset to clear the corresponding IN status and AF flag.

AF7 - AF2 = 0 -
This PMC input did not cause LCL_ATN to be asserted.

AF7 - AF2 = 1 -
This PMC input caused LCL_ATN to be asserted.

Bits 07-00 - IN7-IN0, PMC Inputs 7-0

The Activity Monitor Mask Register at Port Address D872H may be used to select one of the PMC inputs IN7 through IN2 as a source of activity for power management purposes.

IN7 through IN0 are status flags which provide information about the corresponding PMC input IN7 through IN0. IN1 and IN0 represent the current state of the input, while IN7 through IN2 represent either the current state or a latched transition. An IN7 through IN2 status is unlatched when both the corresponding EI and EA bits in the PMC Interrupt Enable Register at Port C872H are reset. It becomes a latched status when either the corresponding EI or EA bit is set. See Table 9-2.

9.6 PMC INTERRUPT ENABLE

Port Address C872H - Read and Write

15	14	13	12	11	10	09	08
EI7	EI6	EI5	EI4	EI3	EI2		
	Non-maskable Interrupt Enable						

07	06	05	04	03	02	01	00
EA7	EA6	EA5	EA4	EA3	EA2		
	Local Attention Enable						

Signal Name	Default At RSTIN
EI7-EI2 †	0
EA7-EA2 †	0

† Featured only in the WD7910LP

Bits 15-10 - EI7-EI2, Non-maskable Interrupt Enable 7 through 2 - Featured only in the WD7910LP

EI7 through EI2 enable the generation of an NMI when the corresponding PMC inputs IN_7 through IN_2 in Port 8872H change state. For example, when EI7 is a 1 and IN_7 changes from a 0 to 1 an NMI will be generated.

EI7-EI2 = 0 -
Non-maskable Interrupt not enabled

EI7-EI2 = 1 -
Non-maskable Interrupt is enabled

Bits 09, 08 - Not used, state is ignored

Bits 07-02 - EA7-EA2, Local Attention Enable Featured only in the WD7910LP

EA7 through EA2 enable the assertion of LCL_ATN by the corresponding IN_7 through IN_2. LCL_ATN is PMC output number 4.

EA7-EA2 = 0 -
LCL_ATN is not enabled

EA7-EA2 = 1 -
LCL_ATN is enabled

Bits 01, 00 - Not used, state is ignored

9.7 NMI STATUS

Port Address 9072H - Read and Write

15	14	13	12	11	10	09	08
0	0	0	0	0	0	0	0

07	06	05	04	03	02	01	00
IF7	IF6	IF5	IF4	IF3	IF2	0	0
Non-maskable Interrupt Flags							

Signal Name	Default At RSTIN
IF7-IF2 †	0-0

† Featured only in the WD7910LP

Bits 15-08 - Not used, must be 0

Bits 07-02 - IF7-IF2, Non-maskable Interrupt Flags 7 through 2 - Featured only in the WD7910LP

NMI interrupt flags IF7 through IF2 are set to indicate which PMC input(s), if any, have caused NMI to be asserted. To reset the flag and corresponding IN status bit in the PMC Input Register at Port 8872H, it is necessary to reset the corresponding bit in the PMC Interrupt Enable Register at Port C872H. If both an EA bit and EI bit in the PMC Interrupt Enable Register are set, both must be reset to clear the corresponding IN status and IF flag.

Bits 01, 00 - Not used, must be 0

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PMC INPUT NUMBER[1]	PMC INPUT NAME	INTERRUPT ON	SETS FLAG NUMBER[2]
00H	$\overline{\text{TURBO}}$		
01H	PROC_PWR_GOOD		
02H	LCL_REQ or User Defined	Transition	IF2 or AF2
03H	User Defined	Transition	IF3 or AF3
04H	User Defined	Transition	IF4 or AF4
05H	User Defined	Transition	IF5 or AF5
06H	User Defined	Transition	IF6 or AF6
07H	User Defined	Active Edge	IF7 or AF7

1 Port Address 8872H, section 9.5
2 Port Address 9072H, section 9.7
Port Address 8872H, section 9.5

TABLE 9-2. PMCIN INPUTS

9.8 SERIAL/PARALLEL SHADOW REGISTER

Port Address D072H - Read only

The Shadow Register is particularly useful in laptop applications by allowing the suspend/resume software to restore correct status to on-board serial and parallel devices.

15	14	13	12	11	10	09	08
SP_A		SP_B		PP_2			

07	06	05	04	03	02	01	00
PP_0							

Signal Name	Default At RSTIN
All signals	None

Bits 15, 14 - SP_A, Serial Port A Register 2

This field represents bits 7 and 6 of Serial Port A Register 2.

Bits 13, 12 - SP_B, Serial Port B Register 2

This field represents bits 7 and 6 of Serial Port B Register 2.

Bits 11-08 - PP_2, Parallel Port Register 2

This field represents bits 3-0 of Parallel Port Register 2

Bits 07-00 - PP_0, Parallel Port Register 0

This field represents bits 7-0 of Parallel Port Register 0.

9.9 INTERRUPT CONTROLLER SHADOW REGISTER

Port Address D472H - Read only

When performing a resume operation, it may be advantageous to reset and reinitialize the interrupt controllers in the WD7910. Since many of the interrupt control registers are write only, it is impossible to determine the state of the interrupt controllers at suspend time. This register makes it possible to determine the state of selected signals internal to the master and slave interrupt controllers. With this information, when the interrupt control registers are reinitialized during resume, they can be returned to the state in which they were before suspend.

ICW2, ICW4, OCW2 and OCW3 referred to in this text is further defined in sections 5.5.2.2, 5.5.2.4, 5.5.3.2 and 5.5.3.3.

15	14	13	12	11	10	09	08
AMT OUT	DEV		TM7	TS7	S F N M	AUT_ EOI	RA_ EOI

07	06	05	04	03	02	01	00
PLM2	PLM1	PLM0	PLS2	PLS1	PLS0	SMM M	SMM S
Priority Level Master			Priority Level Slave				

Signal Name	Default At RSTIN
Bits 15, 12-00	None
Bits 14, 13	00

Bit 15 - AMTOUT, Activity Monitor Timeout

AMTOUT represents the current state of the timeout comparator in the activity monitor. It is for test purposes only

Bit 14, 13 - DEV, Device

DEV identifies the device as WD7910 or WD7710 and is used in conjunction with VER at Port Address 9872H and SVER at Port Address A872H. DEV, VER and SVER are defined in Table 10.1.

Bit 12 - TM7, Master Interrupt Vector Bit 7

TM7 represents bit 7 of the Interrupt Vector in the Master Interrupt Controller as set by ICW2. Bits 6 through 3 of the Interrupt Vector may be read from D6 through D3 by a Poll Command to the Master Interrupt Controller. The Poll Command is implemented by P_C = 1 (bit 2 of OCW3).

Bit 11 - TS7, Slave Interrupt Vector Bit 7

TS7 represents bit 7 of the Interrupt Vector in the Slave Interrupt Controller as set by ICW2. Bits 6 through 3 of the Interrupt Vector may be read from D6 through D3 by a Poll Command to the Slave Interrupt Controller. The Poll Command is implemented by P_C = 1 (bit 2 of OCW3).

Bit 10 - SFNM, Special Fully Nested Mode

SFNM represents the state of ICW4 - bit 4 in the Master Interrupt Controller. The WD7910 does not require SFNM for the slave interrupt controller and ignores its state.

Bit 09 - AUT_EOI, Auto End Of Interrupt

AUT_EOI represents the state of ICW4 - bit 1 in the Master Interrupt Controller. The WD7910 does not require AUT_EOI for the slave interrupt controller and ignores its state.

Bit 08 - RA_EOI, Rotate Auto End Of Interrupt

RA_EOI indicates whether or not Rotate On Automatic End Of Interrupt has been selected in the Master Interrupt Controller by EOI_CONT (bits 7 through 5 of OCW2). The WD7910 does not require Rotate On End Of Interrupt for the slave interrupt controller and ignores its state.

RA_EOI = 0 -
Rotate On Auto End Of Interrupt has not been selected.

RA_EOI = 1-
Rotate On Auto End Of Interrupt has been selected.

Bits 07-05 - PLM2-PLM0, Priority Level Master

PLM2-PLM0 represent the bottom priority level programmed into the Master Interrupt Controller by INT_LEV (OCW2 bits 2 through 0).

Bits 04-02 - PLS2-PLS0, Priority Level Slave

PLS2-PLS0 represent the bottom priority level programmed into the Slave Interrupt Controller by INT_LEV (OCW2 bits 2 through 0).

Bit 01 - SMMM, Special Mask Mode Master

SMMM indicates whether Special Mask Mode has been set in the Master Interrupt Controller by a write to SMM in OCW3.

SMMM = 0 -
Special Mask Mode is not enabled.

SMMM = 1 -
Special Mask Mode is enabled.

Bit 00 - SMMS, Special Mask Mode Slave

SMMS indicates whether Special Mask Mode has been set in the Slave Interrupt Controller by a write to SMM in OCW3.

SMMS = 0 -
Special Mask Mode is not enabled.

SMMS = 1 -
Special Mask Mode is enabled.

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9.10 PORT 70 SHADOW REGISTER

Port Address E472

15	14	13	12	11	10	09	08
CLK 32K	REF DET	INTR	NOD MA	TOD UN	RSVD	RSVD	RSVD

07	06	05	04	03	02	01	00
NMI MSK	RTC IR6	RTC IR5	RTC IR4	RTC IR3	RTC IR2	RTC IR1	RTC IR0

This register provides read-only information on the status of interrupts and DMA which is useful for determining when the processor may be put to sleep. Two bits are also provided for generating software delays without incurring the operating system traps that would result from accessing I/O port 0061 in virtual 86 mode. This register also contains a shadow of the real time clock address register, a write only I/O port. It is necessary to access the real-time clock CMOS RAM during Suspend/Resume operations. This shadow of Port 0070 allows it to be restored to the same state it was in at suspend time.

This register can be read without first unlocking the WD7910. This is important since the CLK32K, REFDET, and TODUN bits may need to be read frequently.

Bit 15 - CLK32K

This read-only bit is a divide by 2 of the PDREF input. It can be read to provide a stable timing reference, not subject to reprogramming of the refresh rate. CLK32K has a 30.5 microsecond period with a 50% duty cycle.

Bit 14 - REFDET

This read-only bit is a copy of the REFDET bit available from I/O Port 0061, Bit 4.

Bit 13 - INTR

This read-only bit gives the state of the INTR output pin to the CPU.

Bit 12 - NODMA, No DMA

This read-only bit is set whenever it has been at least 30.5 microseconds since the last DMA or bus master cycle occurred.

Bit 11 - TODUN, Time of Day Update Needed (R/W)

This is a general purpose storage bit which can be written and read but has no effect on internal logic. Its purpose is to allow an SMI handler to signal the operating system that the time of day has been corrupted. This bit is checked by the Timer 0 Interrupt Handler. Note that although this bit is readable without unlocking the WD7910, it cannot be written unless the WD7910 is unlocked.

Bits 10:8 - RSVD

These read-only bits are reserved for future use. They currently are read back as a 0.

Bit 7 - NMIMSK, NMI Mask

This read-only bit gives the state of the NMI mask bit as it was set the last time I/O port 0070 was written.

Bits 6:0 - RTCIR6-0

These read-only bits give the state of the real time clock address register as it was set the last time I/O port 0070 was written.

9.11 ACTIVITY MONITOR CONTROL REGISTER

Port Address B072H - Bits 15, 13-11, 08-00 Read and Write Bits 14, 10, 09 Read only

For an overview of the Activity Monitor Register, see the general description of the Activity Monitor Mask Register in section 9.12.

15	14	13	12	11	10	09	08
IRR AE	CB12	AM TM	ACT LCH	IND ET	ACT AFT	ACT BEF	AM EN

07	06	05	04	03	02	01	00
Coarse Timeout Count				Fine Timeout Count			
AMC7	AMC6	AMC5	AMC4	AMC3	AMC2	AMC1	AMC0

Signal Name	Default At RSTIN
IRRAE	0
CB12	None
AMTM	0
ACTLCH	None
INDET	None
ACTAFT	None
ACTBEF	None
AMEN	0
AMC7-AMC0	0-0

Bit 15 - IRRAE, Interrupt Request Register Activity Enable

IRRAE controls whether or not the IRR (Interrupt Request Register) bits from the Interrupt Controller at Port Address 020H, 0A0H may be a source of activity (refer to section 5.5).

IRRAE = 0 -
No IRR bits can be used as an activity source.

IRRAE = 1 -
IRR bits can be a source of activity. IRR8, IRR7 and IRR0 may still be masked by Port Address D872H.

Bit 14 - CB12, Counter Bit 12

For factory use only.

The activity monitor circuitry contains a 17-bit timeout counter for generating long timeouts. For test purposes, CB12 represents the twelfth bit of that counter.

Bit 13 - AMTM, Activity Monitor Test Mode

AMTM = 0 -
Activity Monitor functions normally.

AMTM = 1 -
Activity Monitor is in Test Mode. Activity Monitor State Machine is clocked faster than normal and nine stages of the 17-bit timeout counter are bypassed.

Bit 12 - ACTLCH, Activity Latch

This latch is always enabled, regardless of other enable bit settings. Writing a 1 to ACTLCH has no effect.

ACTLCH = 0 -
The Activity Latch is reset by writing 0 to ACTLCH.

ACTLCH = 1 -
Activity by an unmasked source has occurred.

Bit 11 - INDET, Inactivity Detect

Writing a 1 to INDET has no effect.

INDET = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

INDET = 1 -
System is idle and the Activity Monitor has requested the local attention output be set. This occurs when there has been no unmasked activity, allowing the predetermined timeout (bits 07-00) to be reached.

NOTE

PMCIN transitions may also cause the local attention (LCL_ATN PMC 4) output to be set.

Bit 10 - ACTAFT, Activity After INDET

ACTAFT is a read only bit and its state is ignored during writes.

ACTAFT = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

ACTAFT = 1 -
Activity has occurred after INDET had been set. This would happen when activity occurs during the time it takes to reach the interrupt service routine invoked by the local attention output request.

Bit 09 - ACTBEF, Activity Before INDET

ACTBEF is a read only bit and its state is ignored during writes.

ACTBEF = 0 -
Writing 0 to INDET, or placing the Activity Monitor in the idle state by writing 0 to AMEN (bit 8), resets INDET, ACTAFT and ACTBEF.

ACTBEF = 1 -
Activity did occur and reset the timeout counter before INDET was set. This is important if consecutive timeout periods are being counted in a service routine to obtain a system timeout period other than that available using AMC7-AMC0 (bits 07-00). It would be necessary for the routine to clear the software counter if ACTBEF were set, since there would have been no activity only for the period of time programmed in AMC7-AMC0.

Bit 08 - AMEN, Activity Monitor Enable

This is the master enable for the Activity Monitor.

AMEN = 0 -
Writing 0 to AMEN places the Activity Monitor in the idle state.

AMEN = 1 -
Writing 1 to AMEN causes the Activity Monitor to start clocking the timeout counter. Each time an unmasked source of activity is detected, the counter is cleared. If no unmasked source of activity is detected before the timeout counter reaches the value programmed by ACM7 through ACM0, INDET and the local attention output are set. The timeout counter is then cleared and a new timeout sequence begins.

Bits 07-04 - AMC7-AMC4, Activity Monitor Counter Coarse

AMC7-AMC4 establish the timeout values from 64 seconds to 16 minutes in 64-second increments. These bits must only be written when the Activity Monitor is disabled (AMEN = 0). They may be read at any time.

AMC7	AMC6	AMC5	AMC4	
0	0	0	0	0 seconds
0	0	0	1	1 min., 4s
0	0	1	0	2 min., 8s
0	0	1	1	3 min., 12s
0	1	0	0	4 min., 16s
0	1	0	1	5 min., 20s
0	1	1	0	6 min., 24s
0	1	1	1	7 min., 28s
1	0	0	0	8 min., 32s
1	0	0	1	9 min., 36s
1	0	1	0	10 min., 40s
1	0	1	1	11 min., 44s
1	1	0	0	12 min., 48s
1	1	0	1	13 min., 52s
1	1	1	0	14 min., 56s
1	1	1	1	16 min., 0s

Bits 03-00 - AMC3-AMC0, Activity Monitor Counter Fine

AMC3-AMC0 establish the timeout values from 7.8 milliseconds to 117.2 milliseconds in 7.8 millisecond increments. Tolerance on time delays is -0, +3.9 milliseconds. These bits must only be written when the Activity Monitor is disabled (AMEN = 0). They may be read at any time.

AMC3	AMC2	AMC1	AMC0	
0	0	0	0	0 ms
0	0	0	1	7.8 ms
0	0	1	0	15.6 ms
0	0	1	1	23.4 ms
0	1	0	0	31.3 ms
0	1	0	1	39.1 ms
0	1	1	0	46.9 ms
0	1	1	1	54.7 ms
1	0	0	0	62.5 ms
1	0	0	1	70.3 ms
1	0	1	0	78.1 ms
1	0	1	1	85.9 ms
1	1	0	0	93.8 ms
1	1	0	1	101.6 ms
1	1	1	0	109.4 ms
1	1	1	1	117.2 ms

NOTE

The fine timeout delay (AMC3 through AMC0) is added to the coarse timeout delay (AMC7 through AMC4) to obtain the total timeout delay.

9.12 ACTIVITY MONITOR MASK REGISTER

Port Address D872H - Read and Write

The activity monitor provides a hardware solution for determining inactivity in a system. Knowing when a system is inactive is key to performing such power reduction activities as suspend. When the Activity Monitor is enabled by the Activity Monitor Control Register at Port Address B072H, the Activity Monitor clocks a counter and invokes a service routine using local attention when the counter reaches a programmed timeout value. However, while the counter is being clocked, the Activity Monitor continuously monitors for any of several events that would indicate that the system is active. If any of these events occur, the counter is reset and the timeout starts over. Thus the service routine is only invoked when the system has been inactive for a programmed period of time.

To provide a high degree of flexibility in determining what is active and what is not, many sources are routed to the Activity Monitor. These include the IRR (Interrupt Request Register) and ISR (In Service Register) bits from the Interrupt Controller, the PMC inputs, NMI output, DMA (or AT Master) cycles and I/O accesses to either the numeric coprocessor, hard disk data port or programmable chip select. All of these sources are considered activity unless masked.

The interrupt input masks are controlled in the lower byte. All ISR and IRR bits are detected as activity except those specifically masked. Note, however, that ISR2 and IRR2 are not examined since they are cascade interrupts only. Also, IRR3 and IRR4 are qualified by the Mask Register in the Interrupt Controller before being passed to the Activity Monitor. The master mask for all IRR bits is the IRRAE bit in the register at Port Address B072H.

15	14	13	12	11	10	09	08
PCSM	PMCILS	PMCIS2	PMCIS1	PMCIS0	NMIM	HDDM	COPM

07	06	05	04	03	02	01	00
IMS1	IMS0	IRR8M	IRR7M	IRR0M	ISR8M	ISR7M	ISR0M

Signal Name	Default RSTIN
All signals	0

Bit 15 - PCSM, Programmable Chip Select Mask

PCSM = 0 -
Read or write I/O accesses to the ports defined by the programmable chip select in the WD7910LP are considered activity.

PCSM = 1 -
Read or write I/O accesses to the ports defined by the programmable chip select in the WD7910LP are ignored.

Bit 14 - PMCILS, Power Management Control Input Level Select

PMCILS determines which logic level on the selected PMC input is to be considered active. (See bits 13-11, PMCIS2-0.)

PMCILS = 0 -
PMCIN is active low.

PMCILS = 1 -
PMCIN is active high.

Bits 13-11 - PMCIS2-PMCIS0, Power Management Control Input Select

One of the PMC inputs IN7 through IN2 at Port Address 8872H may be selected for detection as a source of activity.

NOTE

The EI and EA bits at Port Address C872H, corresponding to the selected IN signal, should be cleared to prevent the IN signal from being latched internally.

PMCIS 2	1	0	
0	0	0	- PMC input 2 selected
0	0	1	- PMC input 3 selected
0	1	0	- PMC input 4 selected
0	1	1	- PMC input 5 selected
1	0	0	- PMC input 6 selected
1	0	1	- PMC input 7 selected
1	1	0	- Reserved
1	1	1	- Disabled, no PMC inputs checked

Bit 10 - NMIM, Non-maskable Interrupt Mask

NMIM = 0 -
The NMI output is used as a source of activity.

NMIM = 1 -
The NMI output is ignored.

Bit 9 - HDDM, Hard Disk Data Port Mask

HDDM = 0 -
If the hard disk chip select has been enabled by bit 01 at Port Address 2872H, I/O read and write operations to the 16-bit hard disk data port are allowed as a source of activity.

HDDM = 1 -
The hard disk data port I/O is ignored.

Bit 8 - COPM, Coprocessor Mask

COPM = 0 -
I/O cycles to the coprocessor are treated as a source of activity. For an 80286 system, this is I/O address range 00F8H through 00FFH. For an 80386SX system, this is when A23 is high and M/$\overline{IO}$ is low.

COPM = 1 -
I/O to the coprocessor is ignored.

Bits 07, 06 - IMS1-0, Interrupt Mask Select

The local attention generated by the Activity Monitor will be routed to an available interrupt input to invoke a service routine. That interrupt is not to be detected as a source of activity. IMS1 through 0 provide a selection of four possible inputs to be used for this function and masks the corresponding IRR and ISR bits as sources of activity.

IMS 1	0	
0	0	- IRQ5 masked
0	1	- IRQ10 masked
1	0	- IRQ11 masked
1	1	- IRQ15 masked

Bit 05 - IRR8M, Interrupt Request Register 8 Mask

IRR8M = 0 -
Real-Time Clock Interrupt (IRR8) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register

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at Port Address B072H must also be set.

IRR8M = 1 -
Real-Time Clock Interrupt (IRR8) is ignored.

NOTE

See Test Enable Register (A872), Section 11.3 for information about IRQ9 enable control.

See SMI Auxillary Control Register (5472), Section 10.10, for a definition of the activity masks for PCS2 and PCS3.

Bit 04 - IRR7M, Interrupt Request Register 7 Mask

IRR7M = 0 -
Parallel Port or Spurious Interrupt (IRR7) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register at Port Address B072H must also be set.

IRR7M = 1 -
Parallel Port or Spurious Interrupt (IRR7) is ignored.

Bit 03 - IRR0M, Interrupt Request Register 0 Mask

IRR0M = 0 -
Time Of Day Interrupt (IRR0) may be detected as a source of activity. Bit 15 in the Activity Monitor Control Register at Port Address B072H must also be set.

IRR0M = 1 -
Time Of Day Interrupt (IRR0) is ignored.

Bit 02 - ISR8M, Interrupt Service Register 8 Mask

ISR8M = 0 -
Real-Time Clock Interrupt (ISR8) may be detected as a source of activity.

ISR8M = 1 -
Real-Time Clock Interrupt (ISR8) is ignored.

Bit 01 - ISR7M, Interrupt Service Register 7 Mask

ISR7M = 0 -
Parallel Port or Spurious Interrupt (ISR7) may be detected as a source of activity.

ISR7M = 1 -
Parallel Port or Spurious Interrupt (ISR7) is ignored.

Bit 00 - ISR0M, Interrupt Service Register 0 Mask

ISR0M = 0 -
Time of Day Interrupt (ISR0) may be detected as a source of activity.

ISR0M = 1 -
Time Of Day Interrupt (ISR0) is ignored.

9.13 3V Suspend Shadow Registers

The 3V suspend mode provides maximum power savings for the system. The contents of the DRAM, chip set registers, CPU registers and video RAM are all written to the hard disk and then all voltages are shut down, including the power supply. The only logic left on in this mode is the real-time clock and a 3V suspend controller. The real-time clock and the 3V suspend controller run off of the real-time clock battery. When the resume request is sampled by the suspend controller, the suspend controller enables the power supply and resumes the system.

To maintain compatibility with the IBM AT, the timer and DMA registers cannot be read back. To overcome this, these registers are shadowed and read back through other registers. (See descriptions for registers 3C72, 4472 and 4C72.)

9.13.1 DMA Shadow Register 1

Port Address 3C72H (R)

15	14	13	12	11	10	09	08
AD_ DEC	AUTO	TRA_ TYP	TRA_ TYP	TRA_ MOD	TRA_ MOD	AD_ DEC	AUTO

07	06	05	04	03	02	01	00
TRA_ TYP	TRA_ TYP	TRA_ MOD	TRA_ MOD	AD_ DEC	AUTO	TRA_ TYP	TRA_ TYP

Bit 15, the AD_DEC bit of register 0B for DMA channel 2.

Bit 14, the AUTO bit of register 0B for DMA channel 2.

Bits 13:12, the TRA_TYP bits of registers 0B for DMA channel 1.

Bits 11:10, the TRA_MOD bits of register 0B for DMA channel 1.

Bit 9, the AD_DEC bit of register 0B for DMA channel 1.

Bit 8, the AUTO bit of register 0B for DMA channel 1.

Bits 7:6, the TRA_TYP bits of register 0B for DMA channel 1.

Bits 5:4, the TRA_MOD bits of register 0B for DMA channel 0.

Bit 3, the AD_DEC bit or register 0B for DMA channel 0.

Bit 2, the AUTO bit of register 0B for DMA channel 0.

Bits 1:0, the TRA_TYP bits of register 0B for DMA channel 0.

9.13.2 DMA Shadow Register 2

Port Address 4472H (R)

15	14	13	12	11	10	09	08
TRA_ TYP	TRA_ TYP	TRA_ MOD	TRA_ MOD	AD_ DEC	AUTO	TRA_ TYP	TRA_ TYP

07	06	05	04	03	02	01	00
TRA_ MOD	TRA_ MOD	AD_ DEC	AUTO	TRA_ TYP	TRA_ TYP	TRA_ MOD	TRA_ MOD

Bits 15:14, the TR_TYP bits of register 0D6 for channel 6.

Bits 13:12, the TRA_MOD bits of register 0D6 for channel 5.

Bit 11, the AD_DEC bit of register 0D6 for channel 5.

Bit 10, the AUTO bit of register 0D6 for channel 5.

Bits 9:8, the TRA_TYP bits of register 0D6 for channel 5.

Bits 7:6, the TRA_MOD bits of register 0B for channel 3.

Bit 5, the AD_DEC bit of register 0B for channel 3.

Bit 4, the AUTO bit of register 0B for channel 3.

Bit 3:2, the TRA_TYP bits of register 0B for channel 3.

Bits 1:0, the TRA_MOD bits of register 0B for channel 2.

9.13.3 DMA Shadow Register 3

Port Address 4C72H (Read only for bits 14:0)

15	14	13	12	11	10	09	08
SCB		EX_ WR	RO_ PRI		CO_ DIS	TRA_ MOD	TRA_ MOD

07	06	05	04	03	02	01	00
AD_ DEC	AUTO	TRA_ TYP	TRA_ TYP	TRA_ MOD	TRA_ MOD	AD_ DEC	AUTO

Bit 15, Shadow Control BIT (SCB)

Bit 14, Reserved

Bit 13, When SCB is low, this bit represents the EX_WR bit of register 08. When SCB is high, this bit represents the EX_WR bit of register of register 0D0.

Bit 12, When SCB is low, this bit represents the RO_PRI bit of register 08. When SCB is high, this bit represents the RO_PRI bit of register 0D0.

Bit 11, Reserved.

Bit 10, When SCB is low, this bit represents the CO_DIS bit of register 08. When SCB is high, this bit represents the CO_DIS bit of register 0D0.

Bits 9:8, These bits represent the TRA_MOD bits of register 0D6 for channel 7.

Bit 7, AD_DEC bit of register 0D6 for channel 7.

Bit 6, AUTO bit of register 0D6 for channel 7.

Bits 5:4, the TRA_TYP bits of register 0D6 for channel 7.

Bits 3:2, the TRA_MOD bits of register 0D6 for channel 6.

Bit 1, the AD_DEC bit of register 0D6 for channel 6.

Bit 0, the AUTO bit of register 0D6 for channel 6

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9.13.4 DMA Base Address and Count Register

When the SCB is high, the DMA base aaddress and base count can be read back from register 0 to 7. When SCB is low, register 0 to 7 represents the current address and current count.

9.13.5 Timer Count

When SCB is high, the timer base count can be read back from register 40:43. When SCB is low, the register 40:43 represents the timer current count.

9.14 SAVE AND RESUME

When the WD7910LP is in the Save And Resume Mode, it typically draws less than 500 µA. Figures 9-2 and 9-3 illustrate the steps that the WD7910LP goes through during power down and power up.

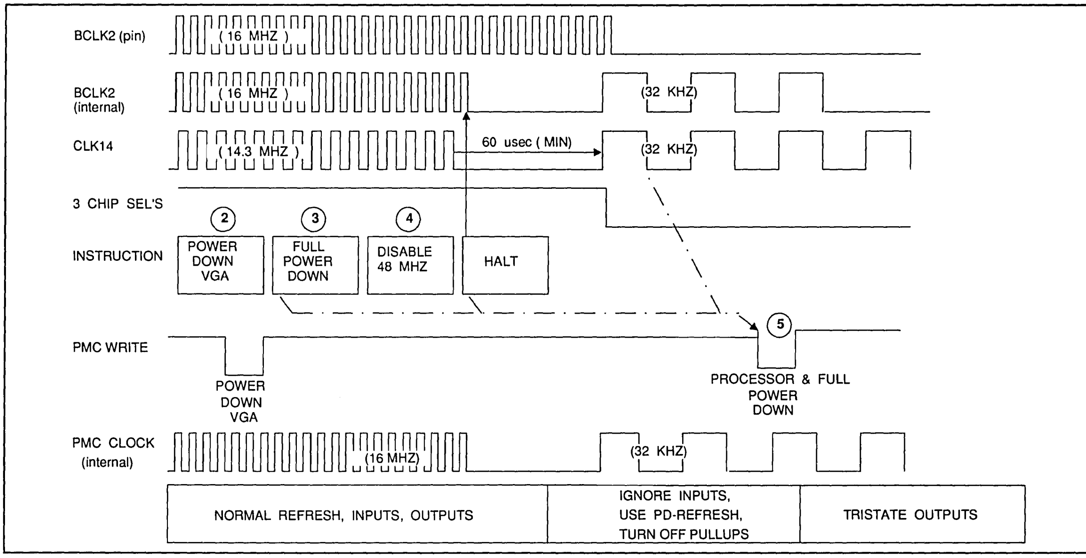

FIGURE 9-2. POWER DOWN

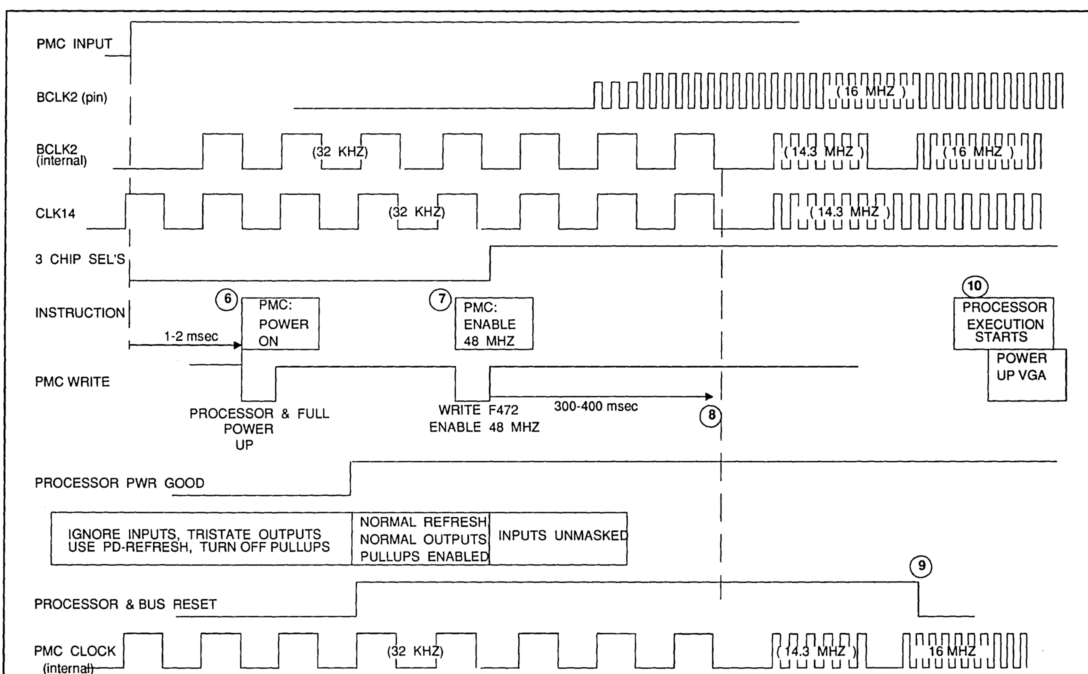

FIGURE 9-3. POWER UP

10.0 SYSTEM MANAGEMENT INTERRUPT (SMI)

10.1 I/O TRAPS

In order to conserve power, certain I/O peripherals can be put to sleep when they are not in use. To accomplish this in a transparent manner, hardware must intercept (trap) any accesses made to the sleeping device and wake it up before allowing the access to proceed. The WD7910 can trap accesses to I/O devices controlled by the following chip selects:

- Programmable Chip Select 1
- Programmable Chip Select 2
- Programmable Chip Select 3
- Serial Port A Chip Select
- Serial Port B Chip Select
- Parallel Port Chip Select

When access to an I/O device is trapped, the WD7910 asserts the SMI pin to the AM386SX. Control is transferred to the SMI handler routine which determines which I/O access caused the SMI handler to be invoked. The handler looks at Registers 7C72 and 8472 to determine the I/O address accessed and how many bytes have been read or written. If the I/O access was unaligned, up to three I/O transfers may have taken place since SMI only breaks AM386SX execution on an instruction boundary. A memory write can also occur if the AM386SX is executing a string input instruction. If unaligned, the memory write can also involve up to three transfers.

Registers 8C72 and 9472 contain either the data written to the I/O device or the memory address written while trapping a string input instruction. Using this information allows the SMI handler to reconstruct the events causing the I/O trap. The handler can then wake up the I/O device, repeat the I/O instruction, rewrite memory if needed, and finally exit to allow normal code execution to continue.

The SMI handler is located in SMI RAM. SMI RAM consists of 64 Kbytes of DRAM space taken from the top of the DRAM space specified by Register 7472. Once the SMI service routine is loaded into SMI RAM space, the SMI RAM space can be hidden from system access and remapped to SMI address space 6000:0H. The only way to access the SMI address space after remap is to put the AM80386SX in SMI mode.

Support for I/O trapping and the generation of SMI is only available on the WD7910LP.

10.2 SMI I/O TRAP CONTROL REGISTER

Port Address 7C72

15	14	13	12	11	10	09	08
LAEN	NAC1	NAC0	PCS TPE	PC2 TPE	SPA TPE	SPB TPE	PAR TPE

07	06	05	04	03	02	01	00
TRPS	IOWS	IOS2	IOS1	IOS0	MS2	MS1	MS0

Bit 15 - LAEN, Local Attention Enable (R/W)

There are three sources that can cause the Local Attention PMC output to be asserted. One is a transition on an unmasked PMC input pin (see description for registers 8872 and C872). The second is a signal from the system activity monitor (see description for registers B072 and D872). The third is a watch dog timer. These sources will also cause an SMI if LAEN is set high. The SMI is based on an internal version of Local Attention and occurs even if PMC updates are disabled.

Bit 15 = 1, Enables SMI to be caused by a Local Attention

Bit 15 = 0, Disables generation of SMI by a Local Attention (Default)

Bits 14:13 - NAC1-0, Next Address Control 1-0 (R/W)

These bits control the function of the NA output pin.

NAC1	NAC0	FUNCTION
0	0	NA is always deasserted (inactive), forcing all 386SX cycles to be nonpipelined. (default)
0	1	NA is always asserted (active), allowing the 386SX to run pipelined whenever possible.
1	0	Reserved setting. Do not use.
1	1	NA is normally asserted allowing pipelined cycles. However, NA is deasserted during T1P (pipelined cycle) or the first T2 (nonpipelined cycle) of all I/O cycles, except coprocessor cycles. NA is asserted again in the next T state unless SMI is active. This setting must be used if pipelining is allowed when I/O traps are enabled.

Bit 12 - PCSTPE, Programmable Chip Select Trap Enable (R/W)

This bit, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the Programmable Chip Select (See registers 2872 and 3072).

Bit 12 = 1, Enable Trap

Bit 12 = 0, Disable Trap (Default)

Bit 11 - PC2TE, Programmable Chip Select 2 Trap Enable (R/W)

This bit, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the second programmable chip select (see registers 5C72 and 6472). This trap occurs even if the ENPCS2 bit in register 5C72 is not set.

Bit 11 = 1, Enable Trap

Bit 11 = 0, Disable Trap (Default)

Bit 10 - SPATPE, Serial Port A Chip Select Trap Enable (R/W)

This bit, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the Serial Port A Chip Select (see register 2072).

Bit 10 = 1, Enable Trap

Bit 10 = 0, Disable Trap (Default)

Bit 9 - SPBTPE, Serial Port B Chip Select Trap Enable (R/W)

This bit, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the Serial Port B Chip Select (see register 2072)

Bit 9 = 1, Enable Trap

Bit 9 = 0, Disable Trap (Default)

Bit 8 - PARTPE, Parallel Port Chip Select Trap Enable (R/W)

This bit, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the Parallel Port Chip Select (see register 2072).

Bit 8 = 1, Enable Trap

Bit 8 = 0, Disable Trap (Default)

Bit 7 - TRPS, Trap Status (R/Clear)

When read as a 1, this bit indicates an I/O trap has occurred. If read as a zero, then no I/O trap has occurred. The SMI handler can poll this status bit to determine if an I/O trap caused the SMI. When this bit is written as a zero, the TRPS, IORD, IOS2-0, and MS2-0 status bits are all reset to 0, readying the I/O trap state machines to capture future I/O and memory cycles. This should be done by the SMI handler each time it services an I/O trap. Writing a 1 to TRPS has no effect.

Bit 6 - IOWS, I/O Write Status (R)

This read only bit is set when the I/O cycle that caused the trap is a write operation. This tells the SMI handler that the contents of Registers 8C72 and 9472 hold the data that was written to the I/O device. This bit is cleared during reset or when TRPS is written with a 0.

Bits 5:2 - IOS2-0, I/O Address Status 2-0 (R)

These read-only bits provide information about the the I/O Cycles captured by the I/O trap (See Table 10-1). This information, along with the I/O address of the first transfer stored in Register 8472, can be used to reconstruct the complete sequence that may have occurred due to an unaligned transfer. These bits are cleared during reset or when TRPS is written with a 0.

Bits 2:0 - MS2-0, Memory Address Status 2-0 (R)

These read-only bits provide information about memory write cycles, if any, captured by the I/O trap (See Table 10-2). Memory write cycles will only be captured if an indivisible string input instruction is being executed. The status information from MS2-0, along with the memory address of the first transfer stored in registers 8C72 and 9472, can be used to reconstruct the complete sequence that may have occurred due to an unaligned transfer. These bits are cleared during reset or when TRPS is written with a 0.

10.3 SMI I/O ADDRESS CAPTURE REGISTER

Port Address 8472

15	14	13	12	11	10	09	08
CIOA 15	CIOA 14	CIOA 13	CIOA 12	CIOA 11	CIOA 10	CIOA 9	CIOA 8

07	06	05	04	03	02	01	00
CIOA 7	CIOA 6	CIOA 5	CIOA 4	CIOA 3	CIOA 2	CIOA 1	CIOA 0

Bits 15:0 - CIOA15-0, Captured I/O Address (R)

These read only bits hold the I/O address being written or read which caused the I/O trap to occur. If multiple I/O cycles were required due to an unaligned transfer, then this is the first address and may need to be adjusted as discussed in the description of the ISO2-0 bits in register 7C72. These bits are cleared during reset or when TRPS (Register 7C72) is written with a 0.

IOS2	IOS1	IOS0	BIT 0 of REG. 8472	TRANSFER TYPE	ADJUSTMENT TO REG. 8472 TO OBTAIN ACTUAL I/O ADDRESS
0	0	0	X	None	Only occurs after a clear
0	0	1	X	16-bit	No adjustment needed
0	1	0	X	32-bit	No adjustment needed
0	1	1	X	32-bit	Subtract 2
1	0	0	X	32-bit	Subtract 1
1	0	1	X	8-bit	No adjustment needed
1	1	0	0	16-bit	Subtract 1
1	1	0	1	16-bit	No adjustment needed
1	1	1	X	32-bit	Subtract 3
X = Don't Care					

TABLE 10-1. I/O ADDRESS STATUS

10.4 I/O DATA/MEMORY ADDRESS CAPTURE REGISTER LOW

Port Address 8C72 (R)

15	14	13	12	11	10	09	08
MAID 15	MAID 14	MAID 13	MAID 12	MAID 11	MAID 10	MAID 9	MAID 8

07	06	05	04	03	02	01	00
MAID 7	MAID 6	MAID 5	MAID 4	MAID 3	MAID 2	MAID 1	MAID 0

Bits 15:0 - MAID 15-0, Memory Address or I/O Data Bits

This read only register holds 16 bits of either the memory address being written after SMI was asserted or the I/O data being written to the I/O address which caused the I/O trap to occur. The IOWS bit in Register 7C72 indicates the type of data. If IOWS is a 1, then this register holds data being written to the I/O device. If IOWS is 0, then this register holds the address of the memory being written, if any. This register is cleared during reset or when TRPS (Register 7C72) is written with a 0.

When capturing the memory write address, this register holds the 16 least significant bits of the address of the first memory write cycle (register 9472 holds the eight most significant bits). More cycles will be completed if the transfer was unaligned. Status bits MS2 through 0 in register 7C72 show how many bytes were written and indicate how to adjust the captured address to get the actual address.

When capturing I/O write data, this register holds up to 16 bits of data, and Register 9472 holds the rest, if any. The data bytes may be stored in a jumbled order if it was an unaligned transfer. The format of the stored data bytes can be obtained from the IOS2-0 bits in Register 7C72 using Table 10-3.

10.5 I/O DATA/MEMORY ADDRESS CAPTURE REGISTER HIGH

Port Address 9472 (R)

15	14	13	12	11	10	09	08
MAID 31	MAID 30	MAID 29	MAID 28	MAID 27	MAID 26	MAID 25	MAID 24

07	06	05	04	03	02	01	00
MAID 23	MAID 22	MAID 21	MAID 20	MAID 19	MAID 18	MAID 17	MAID 16

Bits 15:0 - MAID 31-16, Memory Address or I/O Data Bits

This read-only register holds either: (1) 8 bits of the memory address being written after

IOS2	IOS1	IOS0	BIT 0 of REG. 8472	TRANSFER TYPE	ADJUSTMENT TO REG. 8C72 and 9472 TO OBTAIN ACTUAL MEMORY ADDRESS
0	0	0	X	None	No memory write cycles occurred
0	0	1	X	16-bit	No adjustment needed
0	1	0	X	32-bit	No adjustment needed
0	1	1	X	32-bit	Subtract 2
1	0	0	X	32-bit	Subtract 1
1	0	1	X	8-bit	No adjustment needed
1	1	0	0	16-bit	Subtract 1
1	1	0	1	16-bit	No adjustment needed
1	1	1	X	32-bit	Subtract 3
X = Don't Care					

TABLE 10-2. MEMORY ADDRESS STATUS

SMI is asserted; or (2) the 16 bits of I/O data being written to the I/O address which caused the I/O trap to occur. The IOWS bit in register 7C72 indicates the type of information. If IOWS is a 1, then this register holds data being written to the I/O device. If IOWS is 0, then this register holds the address of the memory being written, if any. This register is cleared during reset or when TRPS (register 7C72) is written with a 0.

When capturing the memory write address, MAID 23 through MAID 16 holds the eight most significant bits of the address of the first memory write cycle (register 8C72 holds the 16 least significant bits). More cycles will be done if the transfer is unaligned. Status bits MS2 through MS0 in register 7C72 show how many bytes were written and indicate how to adjust the captured address to get the actual address.

When capturing I/O write data, this register holds 16 bits of data if it is a 32-bit I/O write. Register 8C72 holds the rest of the data. See the data format description table for register 8C72.

10.6 SMI I/O TIMEOUT

As a power conservation measure, it is desirable to put some I/O peripherals to sleep when they are not in use. This may involve shutting off clocks or removing power. In order to do this, there must be a mechanism for determining that a device is not in use. In the 7910, timers are included for each I/O device that is a candidate for power reduction measures. Each timer causes an SMI when no access is made to an I/O device for a programmable amount of time. The timers are reset by I/O read or write operations to any address which falls within the range of its chip select.

When an SMI is generated, the SMI handler takes whatever action is appropriate to power down the I/O peripheral. The handler then enables the I/O trap for that device so that it can be awakened the next time it is accessed.

IOS2	IOS1	IOS0	BIT 0 of REG. 8472	DATA SIZE	REGISTER 9472 HI BYTE	REGISTER 9472 LO BYTE	REGISTER 8C72 HI BYTE	REGISTER 8C72 LO BYTE
0	0	0	X	None				
0	0	1	X	16-bit			B1	B0
0	1	0	X	32-bit	B3	B2	B1	B0
0	1	1	X	32-bit	B1	B0	B3	B2
1	0	0	X	32-bit	B0	B3	B2	B1
1	0	1	0	8-bit			-	B0
1	0	1	1	8-bit			B0	-
1	1	0	X	16-bit			B0	B1
1	1	1	X	32-bit	B2	B1	B0	B3

Where:
B0 = least significant byte
B1 = next most significant byte (MSB for 16-bit data)
B2 = next most significant byte (32-bit data only)
B3 = most significant byte (32-bit data only)
X = Don't Care

TABLE 10-3. MEMORY ADDRESS OR I/O DATA CAPTURE

10.7 SMI I/O TIMEOUT CONTROL REGISTER

Port Address 9C72

15	14	13	12	11	10	09	08
FSMI	PCS ADS	PC2 ADS	SPA ADS	SPB ADS	PAR ADS	PCS TOS	PC2 TOS

07	06	05	04	03	02	01	00
SPA TOS	SPB TOS	PAR TOS	PCS TOE	PC2 TOE	SPA TOE	SPB TOE	PAR TOE

Bit 15 - FSMI, Force SMI (R/W)

This bit provides a means to invoke the SMI handler through software. When this bit is set to 1, the SMI pin is asserted. FSMI should be cleared by the SMI handler before it exits to prevent another SMI.

Bit 15 = 1, Force SMI Enable

Bit 15 = 0, Force SMI Disable (Default)

Bit 14 - PCSADS, Programmable Chip Select Activity Detect Status (R)

This bit can be polled by the SMI handler to see if the programmable chip select I/O address range has been accessed since PCSTOS was set. If PCSADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. PCSADS is cleared by reset or when PCSTOE is cleared.

Bit 13 - PC2ADS, Programmable Chip Select 2 Activity Detect Status (R)

This bit can be polled by the SMI handler to see if the second Programmable Chip Select's I/O address range has been accessed since PC2TOS was set. If PC2ADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. PC2ADS is cleared by reset or when PC2TOE is cleared.

Bit 12 - SPAADS, Serial Port A Chip Select Activity Detect Status (R)

This bit can be polled by the SMI handler to see if the Programmable Chip Select's I/O address range has been accessed since SPATOS was set. If SPAADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. SPAADS is cleared by reset or when SPATOE is cleared.

Bit 11 - SPBADS, Serial Port B Chip Select Activity Detect Status (R)

This bit can be polled by the SMI handler to see if the Programmable Chip Select's I/O address range has been accessed since SPBTOS was set. If SPBADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. SPBADS is cleared by reset or when SPBTOE is cleared.

Bit 10 - PARADS, Parallel Port Chip Select Activity Detect Status (R)

This bit can be polled by the SMI handler to see if the programmable chip select I/O address range has been accessed since PARTOS was set. If PARADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI handler ignores the timeout and restarts the timeout counter. PARADS is cleared by reset or when PARTOE is cleared.

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Bit 9 - PCSTOS, Programmable Ship Select Timeout Status (R)

This bit is set to a 1 when an I/O access timeout has occurred for the Programmable Chip Select I/O address range. It can be polled by the SMI handler to determine the source of the SMI. PCSTOS is cleared by reset or when PCSTOE is cleared.

Bit 8 - PC2TOS, Programmable Chip Select 2 Timeout Status (R)

This bit is set to a 1 when an I/O access timeout has occurred for the second programmable chip select I/O address range. It can be polled by the SMI handler in determining the source of the SMI. PC2TOS is cleared by reset or when PC2TOE is cleared.

Bit 7 - SPATOS, Serial Port A Chip Select Timeout Status (R)

This bit is set to a 1 when an I/O access timeout has occurred for the Serial Port A Chip Select I/O address range. It can be polled by the SMI handler in determining the source of the SMI. SPATOS is cleared by reset or when SPATOE is cleared.

Bit 6 - SPBTOS, Serial Port B Chip Select Timeout Status (R)

This bit is set to a 1 when an I/O access timeout has occurred for the Serial Port B Chip Select's I/O address range. It can be polled by the SMI handler in determining the source of the SMI. SPBTOS is cleared by reset or when SPBTOE is cleared.

Bit 5 - PARTOS, Parallel Port Chip Select Timeout Status (R)

This bit is set to a 1 when an I/O access timeout has occurred for the Parallel Port Chip Select I/O address range. It can be polled by the SMI handler in determining the source of the SMI. PARTOS is cleared by reset or when PARTOE is cleared.

Bit 4 - PCSTOE, Programmable Chip Select Timeout Enable (R/W)

This bit, when written with a 1, enables an I/O access timeout for the Programmable Chip Select I/O address range. When written with a 0, this bit disables programmable chip select timeouts and clears PCSTOS.

Bit 4 = 1, Timeout Enable

Bit 4 = 0, Timeout Disable (Default)

Bit 3 - PCSTOE, Programmable Chip Select 2 Timeout Enable (R/W)

This bit, when written with a 1, enables an I/O access timeout for the second Programmable Chip Select I/O address range. When written with a 0, this bit disables programmable chip select 2 timeouts and clears PC2TOS.

Bit 3 = 1, Timeout Enable

Bit 3 = 0, Timeout Disable (Default)

Bit 2 - SPATOE, Serial Port A Chip Select Timeout Enable (R/W)

This bit, when written with a 1, enables an I/O access timeout for the Serial Port A Chip Select I/O address range. When written with a 0, this bit disables serial port A chip select timeouts and clears SPATOS.

Bit 2 = 1, Timeout Enable

Bit 2 = 0, Timeout Disable (Default)

Bit 1 - SPBTOE, Serial Port B Chip Select Timeout Enable (R/W)

This bit, when written with a 1, enables an I/O access timeout for the Serial Port B Chip Select I/O address range. When written with a 0, this bit disables serial port B chip select timeouts and clears SPBTOS.

Bit 1 = 1, Timeout Enable

Bit 1 = 0, Timeout Disable (Default)

Bit 0 - PARTOE, Parallel Chip Select Timeout Enable (R/W)

This bit, when written with a 1, enables an I/O access timeout for the Parallel Port Chip Select I/O address range. When written with a zero, this bit disables parallel port chip select timeouts and clears PARTOS.

Bit 0 = 1, Timeout Enable

Bit 0 = 0, Timeout Disable (Default)

10.8 SMI I/O TIMEOUT COUNT REGISTER 1

Port Address A472

15	14	13	12	11	10	09	08
SMI WUE	PCS TC4	PCS TC3	PCS TC2	PCS TC1	PCS TC0	PC2 TC4	PC2 TC3

07	06	05	04	03	02	01	00
PC2 TC2	PC2 TC1	PC2 TC0	SPA TC4	SPA TC3	SPA TC2	SPA TC1	SPA TC0

Bit 15 - SMIWUE, SMI Wake Up Enable (R/W)

This bit, when set to a 1, causes the assertion of SMI to wake up the processor from a powerdown or stop clock state. An INTR, NMI, or DMA request continues to wake up the processor as in the WD76C10, regardless of the state of this bit. Note that setting this bit does not enable SMI to initiate a resume from suspend.

Bit 15 = 1, Enable SMI Wakeup

Bit 15 = 0, Disable SMI Wakeup (Default)

Bits 14:10 - PCSTC 4-0, Programmable Chip Select Timeout Count (R/W)

These bits, along with the timeout clock select PCSTCS (Register AC72), determine the time period during which an I/O peripheral (selected by the Programmable Chip Select) must not be accessed in order to be considered inactive. The timeout setting is computed as follows:

PCSTCS = 0, (Count in PCSTC4-0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

PCSTCS = 1, (Count in PCSTC4-0) x 4 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Default after reset is 00000.

Bits 9:5 - PC2TC 4-0, Programmable Chip Select 2 Timeout Count (R/W)

These bits, along with the timeout clock select PC2TCS (Register AC72), determine the time period during which an I/O peripheral (selected by Programmable Chip Select 2) must not be accessed in order to be considered inactive. The timeout setting is computed as follows:

PC2TC = 0, (Count in PC2TC4-0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

PC2TC = 1, (Count in PC2TC4-0) x 4 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Default after reset is 00000.

Bits 4:0 - SPATC4-0, Serial Port A Chip Select Timeout Count (R/W)

These bits, along with the timeout clock select SPATCS (Register AC72), determine the time period during which Serial Port A must not be accessed in order to be considered inactive. The timeout setting is computed as follows:

SPATCS = 0, (Count in SPATC4-0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

SPATCS = 1, (Count in SPATC4-0) x 4 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Default after reset is 00000.

10.9 SMI I/O TIMEOUT COUNT REGISTER 2

Port Address AC72

15	14	13	12	11	10	09	08
IOT CTM	SPB TC4	SPB TC3	SPB TC2	SPB TC1	SPB TC0	PAR TC4	PAR TC3

07	06	05	04	03	02	01	00
PAR TC2	PAR TC1	PAR TC0	PCS TCS	PC2 TCS	SPA TCS	SPB TCS	PAR TCS

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Bit 15 - IOTCTM, I/O Timeout Counter Test Mode (R/W)

This bit, when written as a 1, puts the timeout counters into test mode. For factory use only.

Bits 14:10 - SPBTC4-0, Serial Port B Chip Select Timeout Count (R/W)

These bits, along with the timeout clock select SPBTCS (Register AC72), determine the time period during which Serial Port B must not be accessed in order to be considered inactive. The timeout setting is computed as follows:

SPBTCS = 0, (Count in SPBTC4-0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

SPBTCS = 1, (Count in SPBTC4-0) x 4 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Default after reset is 00000.

Bits 9:5 - PARTC4-0, Parallel Port Chip Select Timeout Count (R/W)

These bits, along with the timeout clock select PARTCS (Register AC72), determine the time period during which the parallel port must not be accessed in order to be considered inactive. The timeout setting is computed as follows:

PARTCS = 0, (Count in PARTC4-0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

PARTCS = 1, (Count in PARTC4-0) x 4 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Default after reset is 00000.

Bit 4 - PCSTCS, Programmable Chip Select Timeout Clock Select (R/W)

This bit selects the clock to be used for the Programmable Chip Select Timeout Counter. When it is set to 0, a high-speed clock is used to obtain 4 second timing resolution for timeout periods of 2 minutes or less. When it is set to 1, a low-speed clock is used to obtain 40 second timing resolution but a longer timeout period of over 20 minutes. See the description of PCSTC4-0 (Register A472) for more details. Default after reset is 0.

Bit 3 - PC2TCS, Programmable Chip Select 2 Timeout Clock Select (R/W)

This bit selects the clock to be used for the second Programmable Chip Select Timeout Counter. When it is set to 0, a high-speed clock is used to obtain 4 second timing resolution for timeout periods of 2 minutes or less. When it is set to 1, a low-speed clock is used to obtain 40 second timing resolution, but a longer timeout period of over 20 minutes. See the description of PC2TC4-0 (Register A472) for more details. Default after reset is 0.

Bit 2 - SPATCS, Serial Port A Chip Select Timeout Clock Select (R/W)

This bit selects the clock to be used for the Serial Port A Timeout Counter. When it is set to 0, a high-speed clock is used to obtain 4 second timing resolution for timeout periods of 2 minutes or less. When it is set to 1, a low-speed clock is used to obtain 40 second timing resolution, but a longer timeout period of over 20 minutes. See the description of SPATC4-0 (Register A472) for more details. Default after reset is 0.

Bit 1 - SPBTCS, Serial Port B Chip Select Timeout Clock Select (R/W)

This bit selects the clock to be used for the Serial Port B Timeout Counter. When it is set to 0, a high-speed clock is used to obtain 4 seconds timing resolution for timeout periods of 2 minutes or less. When it is set to 1, a low-speed clock is used to obtain 40 second timing resolution, but a longer timeout period of over 20 minutes. See the description of SPBTC4-0 (Register A472) for more details. Default after reset is 0.

Bit 0 - PARTCS, Parallel Port Chip Select Timeout Clock Select

This bit selects the clock to be used for the Parallel Port Timeout Counter. When it is set to 0, a high-speed clock is used to obtain 4 seconds timing resolution for timeout periods of 2 minutes or less. When it is set to 1, a low-speed clock is used to obtain 40 second timing resolution, but a longer timeout period of over 20 minutes. See the description of PARTC4-0 (Register A472) for more details. Default after reset is 0.

10.10 SMI AUXILIARY CONTROL REGISTER

Port 5472

15	14	13	12	11	10	09	08
TOM SK	7910	WDO GEN	WDO GS	PCS 3M	PCS 2M	PC3 TPE	PC3 TOE

07	06	05	04	03	02	01	00
PC3 TOS	PC3 ADS	PC3 TC4	PC3 TC3	PC3 TC2	PC3 TC1	PC3 TC0	PC3 TCS

Bit 15 - TOMSK, Timeout Mask (R/W)

When set to one, TOMSK masks I/O device timeouts from causing assertion of the SMI output. The I/O device timers continue to count down, if enabled, and, if a timeout occurs, the SMI output is asserted after TOMSK is cleared. Also, when TOMSK is set, the I/O device timers will not detect I/O activity, thus preventing the timer from being reset.

Bit 14 - 7910 (R)

This read only bit is set to 1 if the device is a WD7910 or WD7910LP. It is set to 0 if the device is a WD7710 or WD7710LP.

Bit 13 - WDOGEN, Watchdog Timer Interrupt Enable (R/W)

This bit, when set to a 1, enables a periodic interrupt to be generated every 125 ms. Each interrupt causes LCL_ATN to be set, so that it is useful both with or without SMI suppport. The interrupt is cleared either by writing WDOGST with a zero or by writing WDOGEN with a zero to disable further watchdog interrupts. Note that the first interrupt after the watchdog timer is enabled can occur anytime from 62.5 ms to 125 ms later.

Bit 12 - WDOGS, Watchdog Timer Interrupt Status (Read/Clear)

This bit is read as a 1 when LCL_ATN has been set due to a Watchdog Timer Interrupt Request. WDOGST is cleared by writing it with a zero, although the watchdog timer continues to run and will set WDOGST at 125 ms intervals. WDOGST is also cleared when WDOGEN is set to a zero. Writing WDOGST with a 1 has no effect.

Bit 11 - PCS3M, Programmable Chip Select 3 Mask (R/W)

This bit is an extension to register D872. When zero, PCS3M allows I/O accesses to the third Programmable Chip Select address range (see registers 5C72 and 6C72) to be observed as a source of activity by the system activity monitor. When set, it masks I/O accesses to the third Programmable Chip Select from being seen by the system activity monitor. Note that the setting of ENPCS3 in register 5C72 has no effect on I/O activity detection.

Bit 10 - PCS2M, Programmable Chip Select 2 Mask (R/W)

This bit is an extension to register D872. When set to 0, PCS2M allows I/O accesses to the second Programmable Chip Select address range (see registers 5C72 and 6472) to be observed as a source of activity by the system activity monitor. When set, it masks I/O accesses to the second Programmable Chip Select from being seen by the system activity monitor. Note that the setting of ENPCS2 in register 5C72 has no effect on I/O activity detection.

Bit 9 - PC3TPE, Programmable Chip Select 3 Trap Enable (R/W)

This bit, when set to 1, enables an I/O trap to occur whenever an I/O read or write occurs at an address within the range covered by the third Programmable Chip Select (see registers 5C72 and 6C72). This trap occurs even if the ENPCS3 bit in register 5C72 is not set.

Bit 8 - PC3TOE, Programmable Chip Select 3 Timeout Enable (R/W)

This bit, when written with a 1, enables an I/O access timeout for the third Programmable Chip Select I/O address range. The timeout count will be reset by I/O to the Programmable Chip Select 3 address range even if the ENPCS3 bit in register 5C72 is not set. When written with a 0, PC3TOE disables Programmable Chip Select 3 timeouts and clears PC3TOS.

Bit 7 - PC3TOS, Programmable Chip Select 3 Timeout Status (R)

This bit is set to a 1 when an I/O access timeout has occurred for the third Programmable Chip Select I/O address range. It can be polled by the SMI handler in determining the source of the SMI. PC3TOS is cleared by reset or when PC3TOE is cleared.

Bit 6 - PC3ADS, Programmable Chip Select 3 Activity Detect Status (R)

This bit can be polled by the SMI Handler to see if the third Programmable Chip Select I/O address range has been accessed since PC3TOS was set. If PC3ADS is set, then an I/O access has occurred since the inactivity timeout was triggered. The SMI Handler would ignore the timeout and restart the timeout counter. PC3ADS is cleared by reset or when PC3TOE is cleared.

Bit 5:1 - PC3TC4-0, Programmable Chip Select 3 Timeout Count (R/W)

These bits, along with the timeout clock select PC3TCS, determine the time period during which an I/O peripheral (selected by Programmable Chip Select 3) must not be accessed in order to be considered inactive. The timeout setting is computed as follows:

PC3TCS = 0, (Count in PC3TC4-0) x 4 seconds
Range: from 4 seconds to 2 minutes, 4 seconds
Error: -0, +2 seconds.

PC3TCS = 1, (Count in PC3TC4-0) x 4 seconds
Range: from 40 seconds to 20 minutes, 40 seconds
Error: -0, +20 seconds.

Default after reset is 00000.

Bit 0 - PC3TCS, Programmable Chip Select 3 Timeout Clock Select (R/W)

This bit selects the clock to be used for the third Programmable Chip Select timeout counter. When it is set to 0, a high-speed clock is used to obtain 4 second timing resolution for timeout periods of 2 minutes or less. When it is set to 1, a low-speed clock is used to obtain 40 second timing resolution but a longer timeout period of over 20 minutes. See the description of PC3TC4-0 for more details.

10.11 PROGRAMMABLE CS2 AND CS3 CONTROL REGISTER

Port 5C72

15	14	13	12	11	10	09	08
PCS 2L	ENP CS2	UMS K2	2LM SK4	2LM SK3	2LM SK2	2LM SK1	2LM SK0

07	06	05	04	03	02	01	00
PCS 3L	ENP CS3	UMS K3	3LM SK4	3LM SK3	3LM SK2	3LM SK1	3LM SK0

Bit 15 - PCS2L, Programmable Chip Select 2 Location (R/W)

When this bit is set to a 1, the I/O device selected by the second Programmable Chip Select is located on the expansion bus. When this bit is low, the device is located on the RA0-7/ED0-7 bus.

Bit 14 - ENPCS2, Enable Programmable Chip Select 2 (R/W)

When this bit is set to a 1, the second Programmable Chip Select is enabled. When set to a 0, the second Programmable Chip Select is not enabled.

Bit 13 - UMSK2, Upper Address Bits Mask 2 (R/W)

When this bit is set to a 1, then A15 through A10 from register 6472 are compared against CPU address Bits 15 through 10 when qualifying the second programmable chip select. When UMSK2 is set to a 0, then Bits A15 through A10 are ignored.

Bits 12:8 - 2LMSK4-0, Programmable CS2 Lower Address Bits MASK 4-0 (R/W)

These mask bits allow individual qualification of the lower five address bits in register 6472. When a mask bit is set to 1, the corresponding bit in register 6472 is compared against that CPU address bit. When a mask bit is set to 0, the corresponding bit in register 6472 is ignored in the comparison. This allows address ranges of up to 32 bytes to be supported (2LMSK4-0 would all be zeroes), as well as unusual requirements such as odd addresses only.

Bit 7 - PCS3L, Programmable Chip Select 3 Location (R/W)

When this bit is set to a 1, the I/O device selected by the third Programmable Chip Select is located on the expansion bus. When this bit is low, the device is located on the RA0-7/ED0-7 bus.

Bit 6 - ENPCS3, Enable Programmable Chip Select 3 (R/W)

When this bit is set to a 1, the third Programmable Chip Select is enabled. When set to a 0, the third Programmable Chip Select is not enabled.

Bit 5 - UMSK3, Upper Address Bits Mask 3 (R/W)

When this bit is set to a 1, then A15 through A10 from register 6C72 are compared against CPU address bits 15 through 10 when qualifying the third Programmable Chip Select. When UMSK3 is set to a zero, then Bits A15 through A10 are ignored.

Bits 4:0 - 3LMSK4-0, Programmable CS3 Lower Address Bits Mask (R/W)

These mask bits allow individual qualification of the lower five address bits in Register 6C72. When a mask bit is set to 1, the corresponding bit in Register 6C72 is compared against that CPU address bit. When a mask bit is set to 0, the corresponding bit in Register 6C72 is ignored in the comparison. This allows address ranges of up to 32 bytes to be supported (3LMSK4-0 would all be zeroes), as well as unusual requirements such as odd addresses only.

10.12 PROGRAMMABALE CS2 ADDRESS REGISTER

Port 6472

15	14	13	12	11	10	09	08
PC2 A15	PC2 A14	PC2 A13	PC2 A12	PC2 A11	PC2 A10	PC2 A9	PC2 A8

07	06	05	04	03	02	01	00
PC2 A7	PC2 A6	PC2 A5	PC2 A4	PC2 A3	PC2 A2	PC2 A1	PC2 A0

Bits 15:0 - PC2A15-0, Programmable Chip Select 2 Address (R/W)

These bits determine the base address of the I/O device corresponding to the second programmable chip select. Register 5C72 provides the enable for Programmable Chip Select 2 and allows selective masking of some of the address bits.

10.13 PROGRAMMABLE CS3 ADDRESS REGISTER (R/W)

Port 6C72

15	14	13	12	11	10	09	08
PC3 A15	PC3 A14	PC3 A13	PC3 A12	PC3 A11	PC3 A10	PC3 A9	PC3 A8

07	06	05	04	03	02	01	00
PC3 A7	PC3 A6	PC3 A5	PC3 A4	PC3 A3	PC3 A2	PC3 A1	PC3 A0

Bits 15:0 - PC3A15-0, Programmable Chip Select 3 Address (R/W)

These bits determine the base address of the I/O device corresponding to the third Programmable Chip Select. Register 5C72 provides the enable for Programmable Chip Select 3 and allows selective masking of some of the address bits.

10.14 DRAM SIZE AND SMI RAM REGISTER

Port Address 7472

15	14	13	12	11	10	09	08
Bank 3	Bank 2	Bank 1	Bank 0				SMI_R ENB

07	06	05	04	03	02	01	00
SMI_RAM							

This register is used to set up the starting address of the SMI DRAM and support extra DRAM types.

Bits 15:12 - DRAM Type

These four bits are used with Bits 7:0 of Register 3872 to determine the DRAM sizes.

Bit 15 is the MSB of DRAM size for bank 3

Bit 14 is the MSB of DRAM size for bank 2

Bit 13 is the MSB of DRAM size for bank 1

Bit 12 is the MSB of DRAM size for bank 0

See Section 6.2, Memory Configuration.

Bits 11:10, Reserved

These bits should be programmed to zero.

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Bit 9 - HSRPD, Holdoff SMI When Reset Pending Disable (R/W)

When HSRPD is set to 0, then all SMI sources, except I/O traps, are held off whenever a reset-pending condition is detected. The sources remain active internally, but do not cause the SMI output to be asserted until the reset-pending condition is cleared. When HSRPD is set to a 1, the reset pending condition does not gate off the assertion of SMI. Reset pending is defined as: (1) Port 92 reset pending; or (2) KB controller ports 60 or 64 have been written within the last 14 µs or (3) the CPU is in a halt state.

Bit 9 = 1, SMI is not held off.

Bit 9 = 0, SMI is held off when reset is pending (Reset default).

Bit 8, SMI RAM Enable

Setting this bit enables the SMI RAM remapping and protection. The system BIOS should load the SMI service routine into the SMI RAM before setting this bit.

Bit 8 = 0, SMI RAM disable (default)

Bit 8 = 1, SMI RAM enable

Bits 7:0, SMI RAM Starting Address

These bits determine the physical location of the SMI DRAM. These are also used to read/write protect the SMI RAM when the SMI RAM Enable bit is set.

11.0 DIAGNOSTIC MODE

Simultaneously asserting MASTER, MEMR and MEMW while RSTIN is asserted, causes all output pins to become tristated. The outputs remain tristated if RSTIN is de-asserted while MASTER, MEMR and MEMW are asserted. The outputs become active drivers when RSTIN is asserted and any of the MASTER, MEMR or MEMW are not asserted. The output tristate mode allows an in-circuit board tester to drive the WD7910's output pins.

I/O Pin Mapping Mode

The I/O Pin Mapping Mode provides the in-circuit tester for evaluating the connectivity of the WD7910 to the printed circuit board. Simultaneously asserting MASTER, MEMR, MEMW when A1 is high, A2 is low, and RSTIN is asserted, causes the WD7910 to switch to I/O Mapping Mode. The WD7910 stays in this mode if RSTIN is deasserted while MASTER, MEMR, and MEMW are asserted.

Full Tristate Mode

Simultaneously asserting MASTER, MEMR, and MEMW with A1 low and A2 high while RSTIN is asserted, causes all the output pins of the WD7910 to tristate and disablesall the pullup and pulldown register. The WD7910 stays in this mode if RSTIN is deasserted while MASTER, MEMR and MEMW are asserted. The outputs become active drivers when RSTIN is asserted with any of the MASTER, MEMR or MEMW is deasserted. This allows the tester to test for leakage current of the device.

Pullup and Pulldown Test Mode

Simultaneously asserting MASTER, MEMR, MEMW with A1 and A2 high while RSTIN is asserted, causes all the output pins of the WD7910 to become tristated and enables all the pullup and pulldown resistors. The WD7910 stays in this mode if RSTIN is deasserted while MASTER, MEMR and MEMW are asserted. The outputs become active drivers when RSTIN is asserted with any of the MASTER, MEMR or MEMW is deasserted. This allows the tester to test the pullup and pulldown resistors of the device.

11.1 DIAGNOSTIC REGISTER

Port Address 9872H - Read and Write

15	14	13	12	11	10	09	08
RSVD			CLK_ TST	REF_ MAS	AUT_ A20		CLK SW

07	06	05	04	03	02	01	00
SX	DS	DIAG					

Signal Name	Default RSTIN
VER	VER #
CLK_TST	0
REF_MAS	0
AUT_A20	0
Bit 09	None
CLK_SW	0
SX	None
DS	0
DIAG	0-0

Bit 12 - CLK_TST, Clock Test

Diagnostics for factory use only.

Bit 11 - REF_MAS, Bus Master Refresh

Additional external logic may be required to support the bus master initiated refresh.

REF_MAS = 0 -
Does not support bus master initiated refresh (Default value).

REF_MAS = 1 -
Supports bus master initiated refresh.

Bit 10 - AUT_A20, Automatic Gate A20

Normally, the Alternate Gate A20 signal from Port 092H is OR'ed with the 8042 Gate A20.

When the AUT_A20 bit is set, the Alternate Gate A20 control bit automatically changes state to match the keyboard's Gate A20. Bit 1 (ALT_A20G) of Port 092H is set or reset according to the way 8042 is programmed. When the keyboard data port is read using the D1 keyboard controller command, the state of the Gate A20 status bit is replaced by that of AUT_A20.

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The state of the A20 gating signal is available on PMC output 6 by reading Port 7072H (see Table 9-1).

AUT_A20 = 0 -
Normal Alternate Gate A20 (Default value).

AUT_A20 = 1 -
Automatic Gate A20

Bit 09 - Not used, state is ignored.

Bit 08 - CLK_SW, Clock Switch

The short clock switch reset pulse width is 1 µs plus 16 CPUCLKs. The 80486 processor requires a 1 ms clock switch.

CLK_SW = 0 -
Short clock switch reset width (Default value)

CLK_SW = 1 -
1 ms clock switch reset width

Bit 07 - SX, 80386SX Processor

At power up the System Controller samples the type of processor in the system.

SX = 0 -
80286 processor was detected.

SX = 1 -
80386SX processor was detected.

Bit 06 - DS, Diagnostic Signal

DS represents the state of the diagnostic signal selected by DIAG (bits 05 through 00).

Bits 05-00 - DIAG, Diagnostic Function

DIAG selects the diagnostic function to be performed. The DS bit represents the state of the signal selected. Table 11-2. lists the tests available.

DIAG = 00000 - Diagnostic output disabled, speaker normal.

DIAG = 00001 - Diagnostic output disabled, speaker disabled.

DIAG	FUNCTION	DIAG	FUNCTION
00000	Normal Speaker	10000	Reserved
00001	Speaker Disabled	10001	Reserved
00010	Reserved	10010	Reserved
00011	Reserved	10011	Reserved
00100	Reserved	10100	Reserved
00101	Reserved	10101	Reserved
00110	Reserved	10110	Reserved
00111	Reserved	10111	Reserved
01000	Reserved	11000	Reserved
01001	Reserved	11001	Reserved
01010	Reserved	11010	Reserved
01011	Reserved	11011	Reserved
01100	Reserved	11100	Reserved
01101	Reserved	11101	Reserved
01110	Reserved	11110	Reserved
01111	Reserved	11111	Reserved

TABLE 11-1. DIAGNOSTIC TESTS

11.2 DELAY LINE DIAGNOSTIC REGISTER

Port Address A072H - Read and Write

15	14	13	12	11	10	09	08

07	06	05	04	03	02	01	00
LAT	DL	DELAY					

Signal Name	Default RSTIN
Bits 15-08	None
LAT	0
DL	0
DELAY	None

Bit 07 - LAT, Latch Output Strength

The delay line count value (bits 05-00) is used to control the output buffer strength. The output buffer strength is normally adjusted every time the delay count changes. LAT may be used to lock the buffer strength at its present value.

LAT = 0 -
The output buffer strength is adjusted when the delay count changes.

LAT = 1 -
The output buffer strength is locked at its present value.

Bit 06 - DL, Delay Freeze

The internal self tuning delay line normally is updated by one delay element during every refresh cycle. For test purposes, the delay may be forced to stop generating calibration cycles. When delay line updates are frozen, the tester may write different delay line counter values in bits 05-00.

DL = 0 -
Normal delay line operation (Default value)

DL = 1 -
Freeze delay line

Bits 05-00 - DELAY, Delay Counter Value

The delay line counter value is used to control the output buffer strength.

This register may be written to when DL is set to one.

11.3 TEST ENABLE REGISTER

Port Address A872H - Bits 15-10 Read only
Bits 09-00 Read and Write

The test function bits 07-03 are for factory use only.

15	14	13	12	11	10	09	08
SVER				BF40	BC40	IRQ9 EN	TDL

07	06	05	04	03	02	01	00
OLD IHLD	BFC 3	BIST 3	BFC 40	BIST 40	EN_ PLD	DISFA	EN_ LVL

Signal Name	Default At RSTIN
All signals	0-0

Bits 15-12 - SVER, Secondary Version Number.

See VER at Port Address 9872H.

PORT ADDRESS D472H DEVICE - Bits 14, 13			PORT ADDRESS A872H SECONDARY VERSION - Bits 15-12				
14	13	Device	15	14	13	12	Rev
0	0	WD76C10	0	0	0	0	A
0	1	WD7710/7910	0	0	0	1	B
1	0	Reserved	0	0	1	0	C
1	1	Reserved	-	-	-	-	-
			1	1	1	1	P

Bit 11 - BF40, EMS Register Self Test Status

Bit 10 - BC40, EMS Register Self Test Status

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Bit 09 - IRQ9EN = 0, Masks IRR9 and ISR9 so that the System Activity Monitor does not detect these signals. This prevents vertical retrace from being a source of activity for SAM.

IRQ9EN = 0 ,
Masking of IRR9 and ISR9 enabled

IRQ9EN = 1,
Masking disabled

Bit 08 - TDL, Test Delay Line.

Bit 07 - OLD_IHLD,

OLD_IHLD = 0 -
SX test not enabled

OLD_IHLD = 1 -
SX test enabled

Bit 06 - BFC3,

BFC3 = 0 -
DMA register file test

BFC3 = 1 -
DMA register file test

Bit 05 - BIST3,

BIST3 = 0 -
DMA register file test

BIST3 = 1 -
DMA register file test

Bit 04 - BFC40,

BFC40 = 0 -EMS mapping RAM

BFC40 = 1 -EMS mapping RAM

Bit 03 - BIST40,

BIST40 = 0 -
EMS mapping RAM

BIST40 = 1 -
EMS mapping RAM

Bit 02 - EN_PLD, Enable Pulldown

EN_PLD = 0 -
Pulldown resistors are not enabled.

EN_PLD = 1 -
40K to 100K internal pulldown resistors will be enabled during processor power down or full power down on processor address lines A23 through A00, and on processor data lines D15 through D00.

Bit 01 - DISFA, Disable First Access

DISFA = 0 -
First access Page Mode cycles are not disabled.

DISFA = 1 -
First access Page Mode cycles are disabled. Page Miss cycles occur instead.

Bit 00 - EN_LVL, Enable Level

The Interrupt Controller may be programmed to support Level Sensitive Mode for diagnostic adapters which may need to test this capability.

EN_LVL = 0 -
Level Sensitive Interrupt Mode in the 8259 Interrupt Controller is not supported. L_T (bit 3) at Port 020H has no effect.

EN_LVL = 1 -
Level Sensitive Interrupt Mode in the 8259 Interrupt Controller is supported. L_T (BIT 3) at Port 020H now controls the selection of edge-sensed or level-sensed interrupts.

11.4 TEST STATUS REGISTER

Port Address DC72H - Read only

For factory use only.

15	14	13	12	11	10	09	08
Delay Line Status CAL	MED	SLOW	DLT6	DLT5	DLT4	DLT3	DLT2

07	06	05	04	03	02	01	00
DLT1	DLT0	BF34	BF33	BF32	BF31	BF30	BC

Signal Name	Default RSTIN
All signals	None

Bit 15 - CAL, Calibration

CAL = 0 -
Internal delay line has not completed initial calibration.

CAL = 1 -
Internal delay line has completed initial calibration.

Bits 14, 13 - MED, SLOW, Medium and Slow

These bits provide information regarding the output buffer strength.

MEDIUM	SLOW	
0	0	Output buffers are set to low strength (fast WD7910/7910LP).
0	1	Invalid
1	0	Output buffers are set to medium strength (medium speed WD7910/7910LP).
1	1	Output buffers are set to full strength (slow WD7910/7910LP).

Bits 12-06 - DLT6-DLT0,

These bits provide information about internal nodes and are for test purposes only. Their state is dependent upon the test mode selected and the speed of the WD7910/7910LP.

Bits 05-01 - BF34-BF30,

These bits provide information about internal nodes and are for test purposes only. Their state is dependent upon the test mode selected and the speed of the WD7910/7910LP.

Bit 00 - BC

This bit provides information about internal nodes and are for test purposes only. Its state is dependent upon the test mode selected and the speed of the WD7910/7910LP.

12.0 DC ELECTRICAL SPECIFICATIONS

12.1 MAXIMUM RATINGS

Supply Voltage (Vcc) with respect to Vss (ground) . . . . . . Vcc - Vss ≤ 7.0 Volts

Voltage on any pin with respect to Vss (ground) . . . . Vss -0.3 Volts to Vdd +0.3 Volts

Operating Temperature . . . . 0°C (32°F) to 70°C (158°F)

Storage Temperature . . . . -40°C (-40°F) to 125°C (257°F)

Power Dissipation . . . . 600 mW

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

12.2 DC OPERATING CHARACTERISTICS

TA = 0°C (32°F) to 70°C (158°F)
Vcc = +5V ±.25V (5%) for WD7910 and WD7910LP

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Leakage		± 10	µA	Vin = .4 to Vcc
IOZ	Tristate And Open Drain Output Leakage		± 10	µA	Vout = .4 to Vcc
VIH	Input High Voltage	2.0		V	
VIL	Input Low Voltage		.8	V	
VIHC	CPUCLK Input High	3.6		V	
VIL	CPUCLK Input Low		.6	V	
ICC	Supply Current		200 150	mA mA	Inputs at 2.0V Inputs at 5.0V Outputs Open, CPUCLK = 32 MHz
ICCSB	Typical Supply Current, Power Down Mode For WD7910LP	.5		mA	Typical, CPUCLK Off, CLK14 = 32 KHz

TABLE 12-1. DC OPERATING CHARACTERISTICS

FOR PINS WITH INTERNAL PULLUPS:

MASTER, IOCK, IOCS16, MEMCS16, ZEROWS, IOCHRDY, RDYIN, PDREF

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-30	-110	µA	Not suspend and resume mode

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

M/IO, PEACK, NPERR, NPBUSY, S0, S1, NPRST, CPURES, DPH, DPL

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-30	-110	µA	Not processor down or suspend mode

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

PMCIN, IOCHRDY, ZEROWS, IOCS16, MEMCS16, MASTER, PDREF, REFRESH, BHE, IOR, IOW, MEMR, MEMW

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-30	-110	µA	Not suspend mode

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

CASL3, CASL2, CASH3, SDT/R

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pullup Current	-30	-110	µA	RESET IN = 0

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

FOR PINS WITH INTERNAL PULLDOWNS:

A23-A0, D15-D0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
IIL	Input Pulldown Current	-30	-110	µA	Processor power down or suspend mode

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

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FOR OUTPUTS:

DACK2-0, DACKEN, D15-D0, READY, CPURES, HOLD, INTRQ, A23-A0, NMI, DPH, DPL, RA10-RA8, RA7/ED7-RA0/ED0, BHE, RAS3-RAS0, CASL3-CSL0, CASH3-CASH0, W/R, DT/R, DEN1, DEN0, SDT/R, SDEN, CSEN, LOMEG

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	Vcc -.8		V	IOUT = -100 µA
VOH	Output High Voltage	2.4		V	IOUT = -2 mA
VOL	Output Low Voltage		.4	V	IOUT = 2 mA

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

MXCTL2-0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	Vcc - .8		V	IOUT = -200 µA
VOH	Output High Voltage	2.4		V	IOUT = -4 mA
VOL	Output Low Voltage		.4	V	IOUT = 4 mA

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUTS:

IOR, IOW, MEMR, MEMW, AEN, SYSCLK, BALE, LA20, SA0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOUT = -3 mA
VOL	Output Low Voltage		.5	V	IOUT = 24 mA

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

FOR OUTPUT:

REFRESH

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITIONS
VOL	Output Low Voltage		.5	V	IOUT = 24 mA

TABLE 12-1. DC OPERATING CHARACTERISTICS cont.

13.0 AC OPERATING CHARACTERISTICS

The AC Operating Characteristics are divided into three major categories: Memory Timing (Section 13.1), AT Bus Timing (Section 13.2), Processor Timing (Section 13.3), and Cache Controller Timing (Section 13.4).

Table 13-1 lists the timing tables and figures, and their section location.

TABLE NUMBER	FIGURE NUMBER	TITLE	SECTION
13-3		80286 - Page Mode Memory Timing	13.1.1
	13-1	80286 - Page Mode First Access Read/Write	13.1.1
	↕		
	13-6	80286 - Page Mode Read Hit Followed By Write Hit	13.1.1
13-4		80286 - Non-Page Mode 00 Memory Timing	13.1.2
	13-7	80286 - Non-Page Mode 00 1 Wait State Write	13.1.2
	13-8	80286 - Non-Page Mode 00 1 Wait State Read	13.1.2
	13-9	80286 - Non-Page Mode 00 2 Wait States Read After Write	13.1.2
13-5		80286 - Non-Page Mode 01 Memory Timing	13.1.3
	13-10	80286 - Non-Page Mode 01 0 Wait State Write	13.1.3
	13-11	80286 - Non-Page Mode 01 0 Wait State Read	13.1.3
13-6		80386SX - Page Mode Memory Timing	13.1.4
	13-12	80386SX - Page Mode, First Access Read/Write	13.1.4
	↕		
	13-17	80386SX - Page Mode, Write Miss Following A Write	13.1.4
13-7		80386SX - Non-Page Mode 00 And Mode 01	13.1.5
	13-18	80386SX - Non-Page Mode 00 1 Wait State Read	13.1.5
	↕		
	13-21	80386SX - Non-Page Mode 00 1 Wait State Read	13.1.5
13-8		CPU Initiated AT Bus Cycles	13.2.1
	13-22	AT Bus I/O Or Memory Read: 8-Bit, Default Timing	13.2.1
	↕		
	13-31	AT Bus I/O Or Memory Write: 16-Bit, Default Timing	13.2.1
13-9		Entering The AT Bus	13.2.2
	13-32	80286 CPU - Asysnchronous CPUCLK To SYSCLK, BREQ Delay = 1/2 Clock	13.2.2
	↕		
	13-37	80386SX CPU - Synchronous CPUCLK To SYSCLK	13.2.2
13-10		Exiting The AT Bus	13.2.3
	13-38	Synchronous AT Bus Cycle Completion, AT Bus Clock = 1/2 CPUCLK	13.2.3
	↕		
	13-41	Asynchronous AT Bus Cycle Completion, BAK_DEL = 0 Or +0.5 AT Bus Cycles	13.2.3
13-11		DMA Entering And Exiting The AT Bus	13.2.4
	13-42	Basic DMA Cycle, Default Timing	13.2.4
	13-43	DMA Cycle, 8-Bit I/O To On-board Memory	13.2.4
	13-44	DMA Cycle, On-board Memory To 8-Bit I/O	13.2.4
13-12		AT Bus Master Cycle	13.2.5
	13-45	AT Bus Master, Bus Acquisition/Release	13.2.5
	13-46	AT Bus Master, Write To On-board Memory	13.2.5
	13-47	AT Bus Master, Read From On-board Memory	13.2.5
13-13		AT Bus Refresh Cycle, Default Timing	13.2.5
	13-48	AT Bus Refresh Cycle, Default Timing	13.2.5

TABLE 13-1. TIMING FIGURE/TABLE NUMBERS

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TABLE NUMBER	FIGURE NUMBER	TITLE	SECTION
13-14		80286 CPU TIMING	13.3
	13-49	80286 - CPURES AND NPRST DURING POWER UP	13.3
	↕		
	13-54	80286 - MISCELLANEOUS TIMING	13.3
13-15		80386SX CPU TIMING	13.3
	13-55	80386SX - CPURES AND NPRST DURING POWER UP	13.3
	↕		
	13-62	80386SX - OUTPUT DELAY TIMING	13.3

TABLE 13-1. TIMING FIGURE/TABLE NUMBERS cont.

SIGNAL	LOAD	SIGNAL	LOAD	SIGNAL	LOAD
CPURES	50 pF	NPRST	50 pF	$\overline{\text{BHE}}$	50 pF
W/$\overline{\text{R}}$	50 pF	ALE	50 pF	$\overline{\text{DEN1}}$, $\overline{\text{DEN0}}$	50 pF
$\overline{\text{SDEN}}$	50 pF	DT/$\overline{\text{R}}$	50 pF	SDT/$\overline{\text{R}}$	50 pF
MXCTL2 - 0	50 pF	DACKEN	50 pF	$\overline{\text{CSEN}}$	50 pF
$\overline{\text{LOMEG}}$	50 pF	SPKR	50 pF	$\overline{\text{READY}}$	50 pF
HOLD	50 pF	INTRQ	50 pF	NMI	50 pF
$\overline{\text{BUSYCPU}}$	50 pF	EPEREQ	50 pF	A23 - A0	60 pF
CPUCLK	70 pF	SYSCLK	75 pF	$\overline{\text{CASH3}}$ - $\overline{\text{0}}$	75 pF
$\overline{\text{CASL3}}$ - $\overline{\text{0}}$	75 pF	D15 - D0	100 pF	DPH	100 pF
DPL	100 pF	$\overline{\text{RAS3}}$ - $\overline{\text{RAS0}}$	150 pF	$\overline{\text{IOW}}$	200 pF
$\overline{\text{IOR}}$	200 pF	$\overline{\text{MEMW}}$	200 pF	$\overline{\text{MEMR}}$	200 pF
LA20	200 pF	SA0	200 pF	AEN	200 pF
BALE	200 pF	$\overline{\text{REFRESH}}$	200 pF	RA10 - RA0	350 pF

TABLE 13-2. SIGNAL LOADING

13.1 MEMORY TIMING

Sections 13.1.1 through 13.1.5 present the memory timing for Page Mode and Non-Page Mode, for the 80286 and 80386SX processors.

Categories are grouped as follows:

- 80286
  - Page Mode
  - Non-Page Mode 00
  - Non-Page Mode 01
- 80386SX
  - Page Mode
  - Non-Page Mode 00 and 01

Mnemonics used in the timing diagrams and tables are defined as:

- TC - Command Cycle
- TW - Wait State Cycle
- TS - Status Cycle
- WNRDRAM - Write Not Read DRAM (W/R̄ pin 119).

13.1.1 80286 Page Mode Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz
T220	Processor address to RAM address valid, Page Hit	32	30
T221	CPUCLK fall to CAS fall, 2.5 CLK CAS	36	34
T222	CPUCLK rise to CAS rise	29	27
T223	CPUCLK rise to CAS fall, 2.0 CLK CAS	30	26
T224	Processor data to parity valid	25	22
T225	CPUCLK fall to RAM address valid, Page Miss	39	36
T226	CPUCLK fall to WNRDRAM rise	34	31
T227	CPUCLK rise to RAS fall, first access	28	26
T228	CPUCLK fall to column address valid	44	41
T229	CPUCLK fall to WNRDRAM fall	34	31
T232	CPUCLK fall to RAS rise, Page Miss	29	27
T233	CPUCLK rise to RAS fall, Page Miss	28	26
T234	CPUCLK rise to READY rise	24	22
T235	CPUCLK rise to READY fall	24	22

TABLE 13-3. 80286 - PAGE MODE MEMORY TIMING

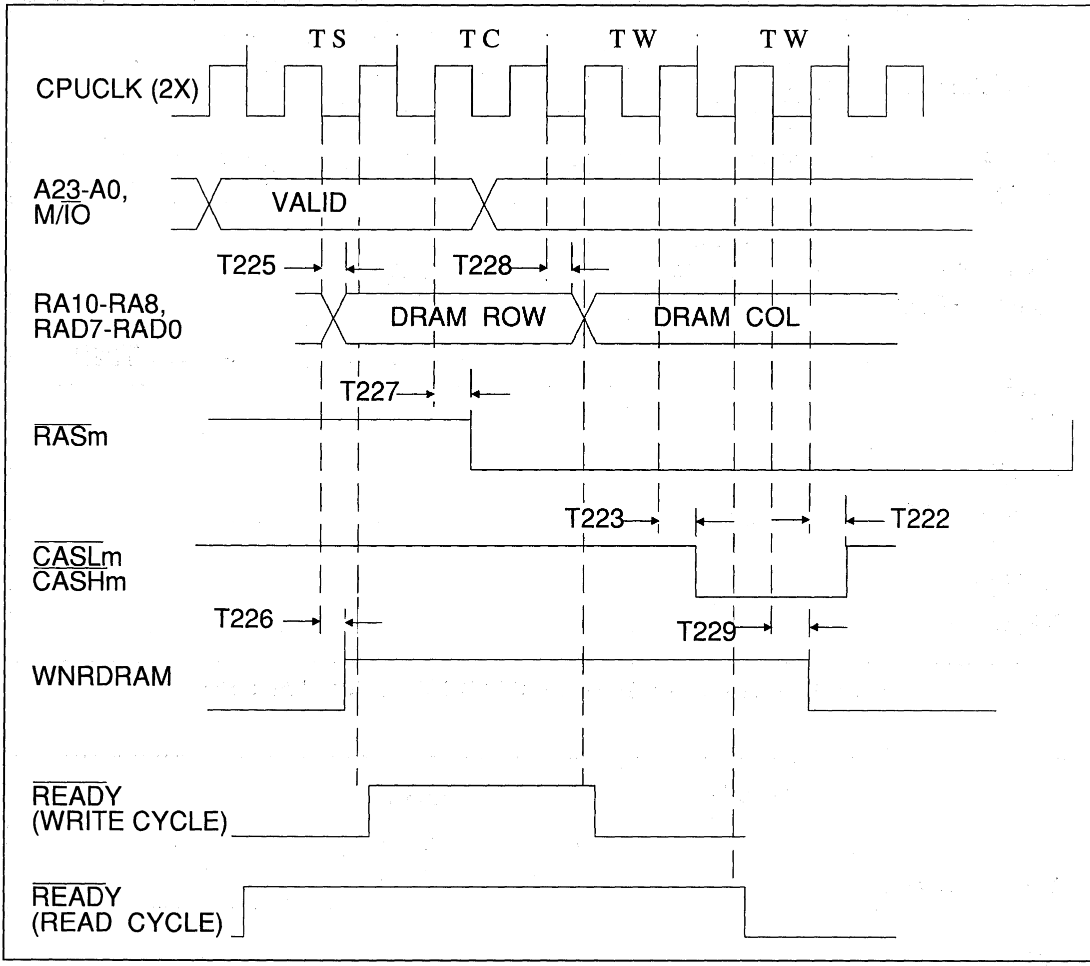

FIGURE 13-1. 80286 - PAGE MODE FIRST ACCESS READ/WRITE

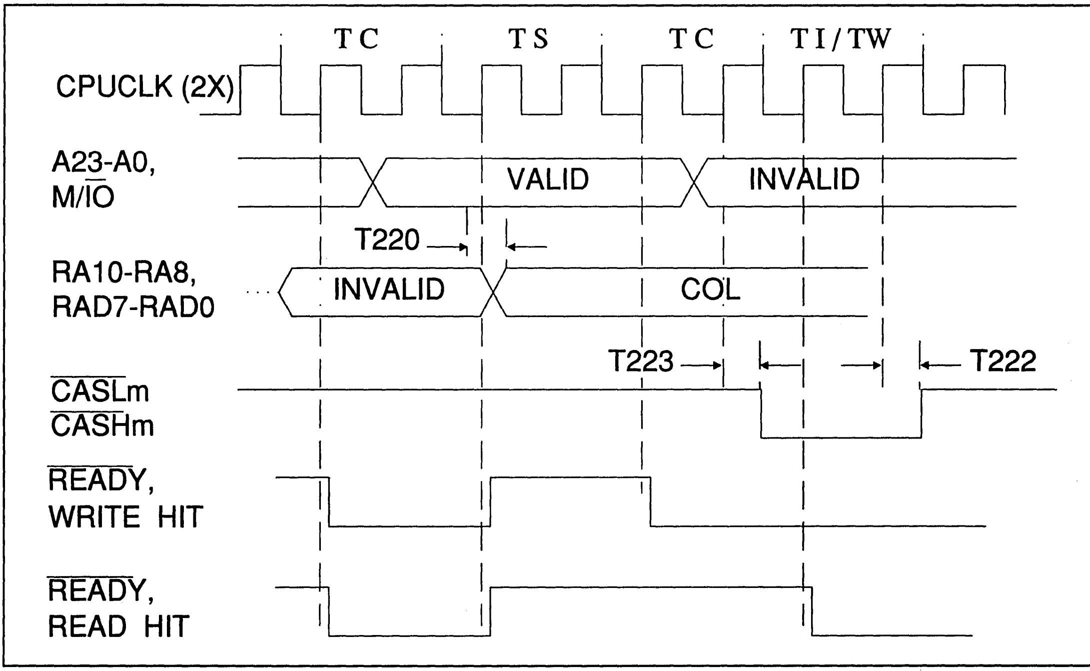

FIGURE 13-2. 80286 - PAGE MODE READ CYCLE AND PAGE HIT

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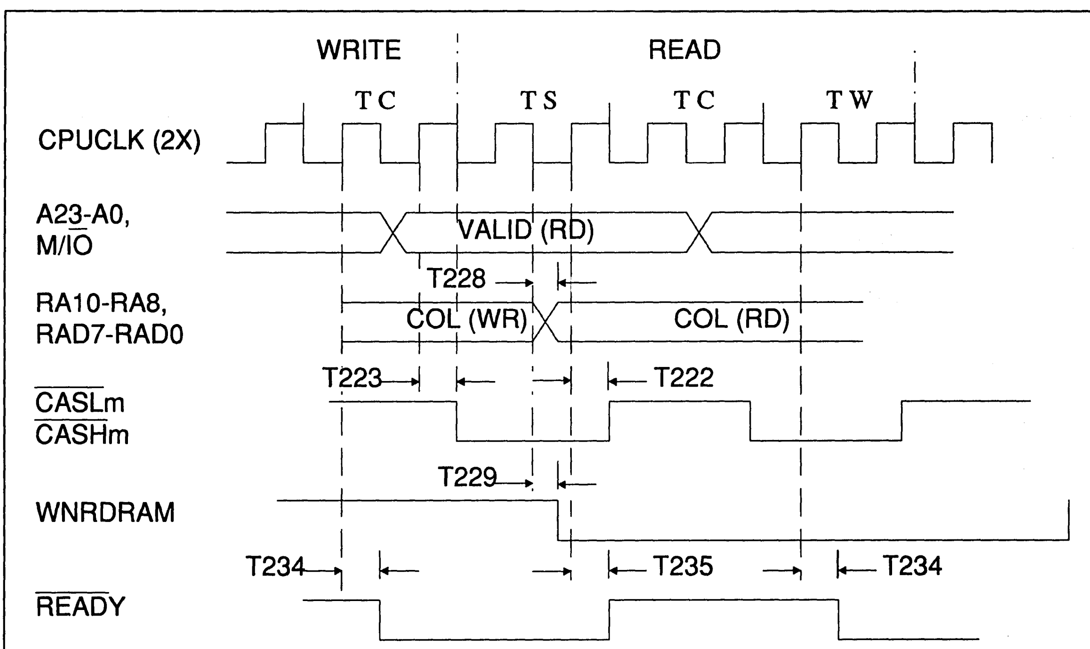

FIGURE 13-3. 80286 - PAGE MODE READ AFTER WRITE

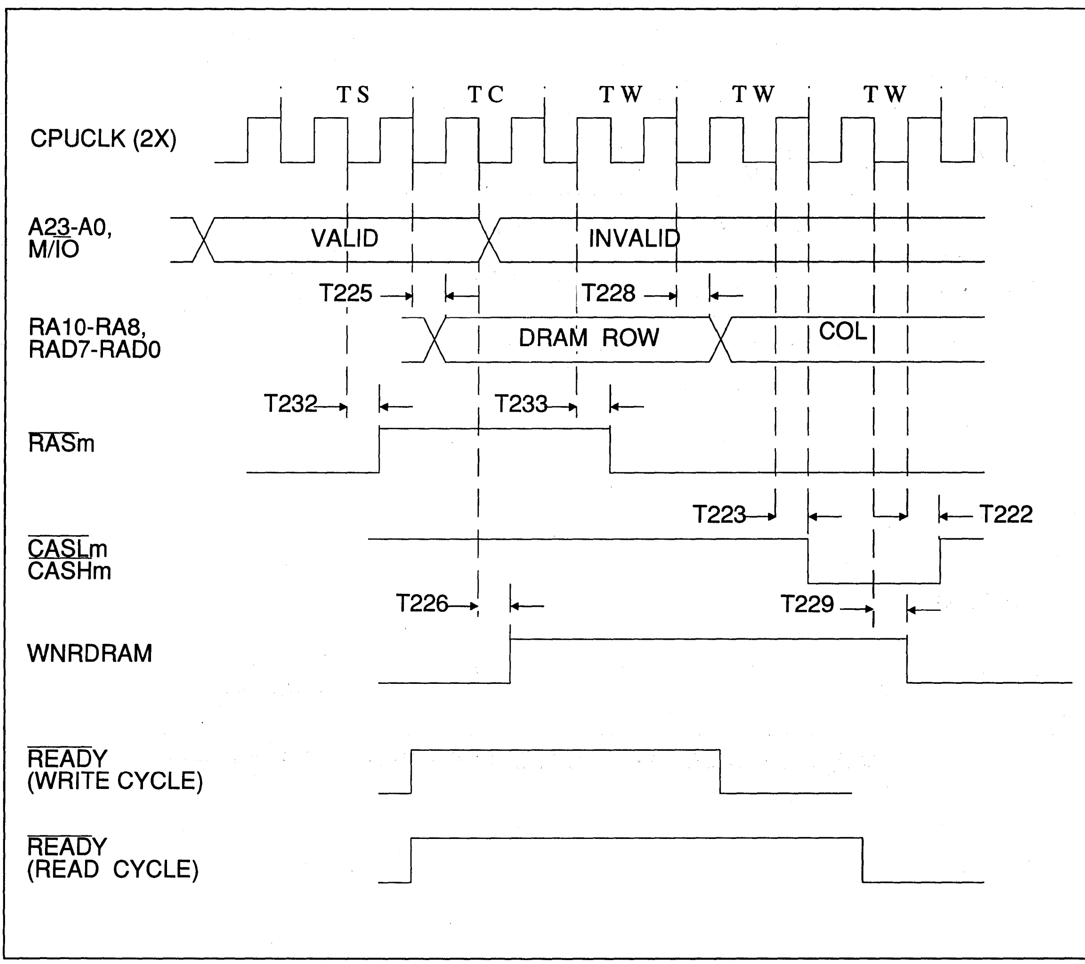

FIGURE 13-4. 80286 - PAGE MODE, PAGE MISS READ/WRITE

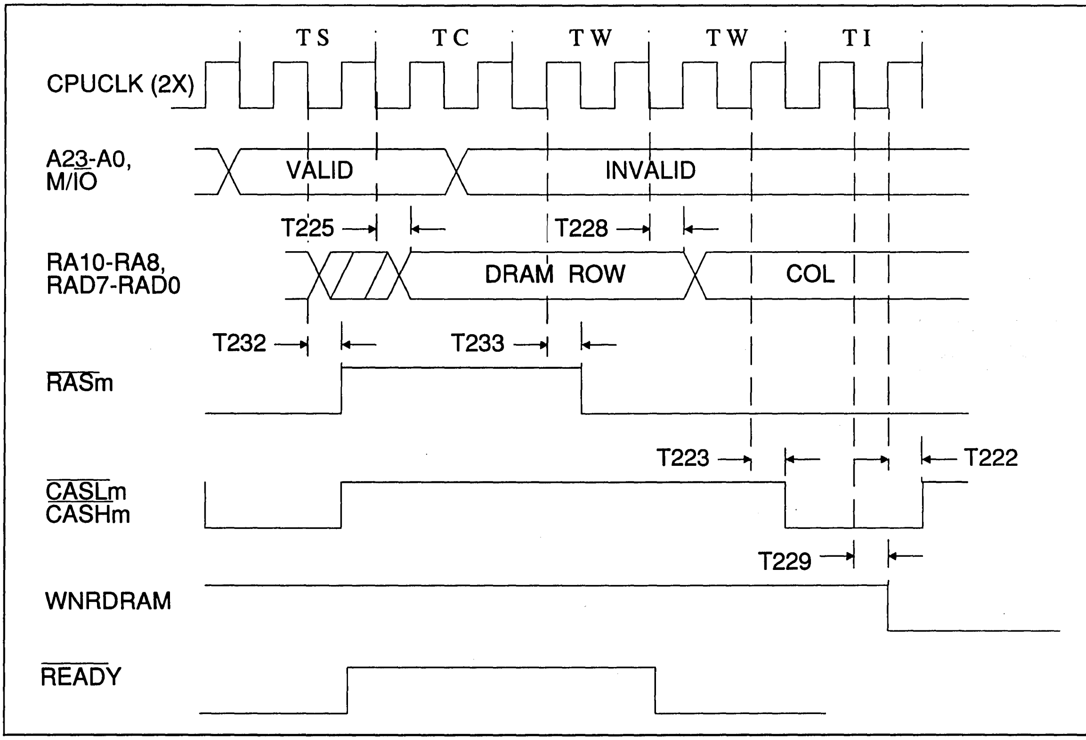

FIGURE 13-5. 80286 - PAGE MODE, WRITE MISS AFTER WRITE

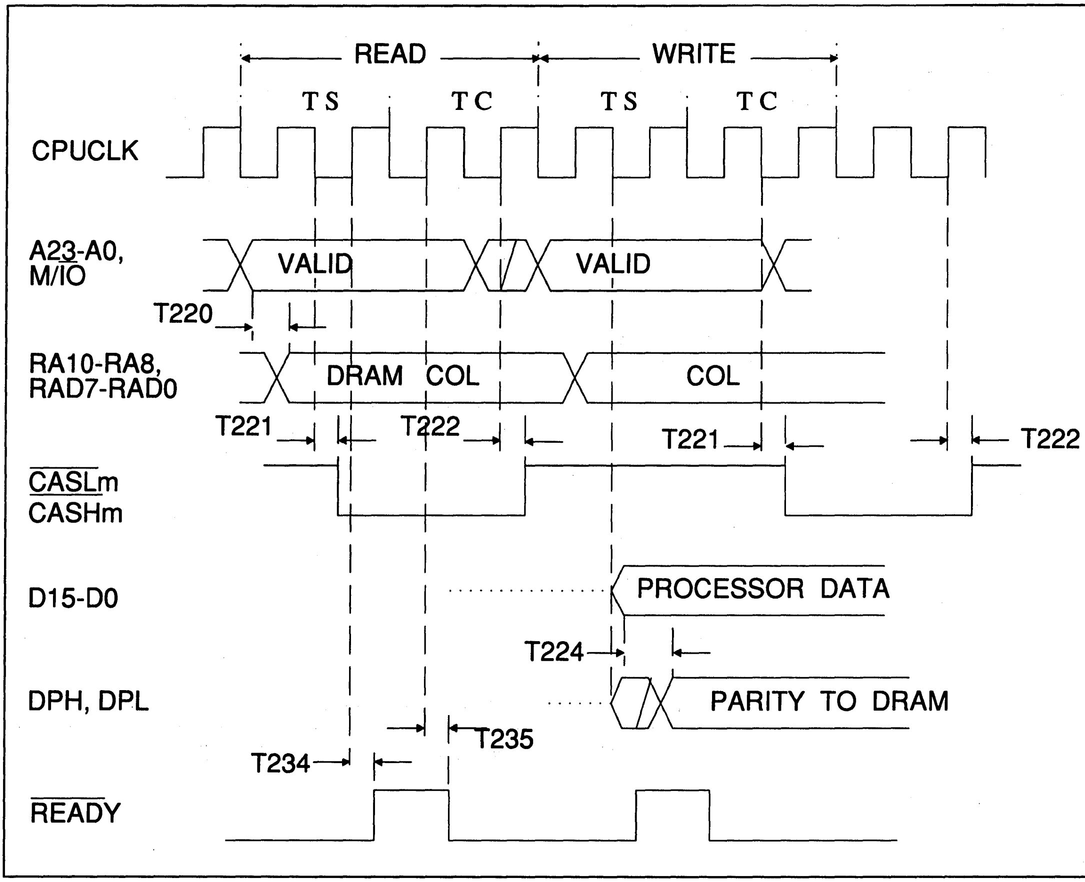

FIGURE 13-6. 80286 - PAGE MODE READ HIT AND WRITE HIT

13.1.2 80286 Non-Page Mode 00 Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz
T234	See Table 13-3		
T235	See Table 13-3		
T252	CPUCLK fall to $\overline{\text{CAS}}$ rise	33	30
T255	CPUCLK fall to $\overline{\text{RAS}}$ fall	35	32
T270	CPUCLK fall to ROW address	46	42
T271	CPUCLK fall to CAS fall	37	34
T273	CPUCLK fall to WNRDRAM fall	33	31
T274	CPUCLK fall to WNRDRAM rise	33	31
T275	Data holding tristate. ①	12	12
T276	Clock fall to parity valid	30	27
T277	CPUCLK fall to RAS rise	30	28
T278	CPUCLK fall to COLUMN address valid	41	38
T279	Processor address to ROW address	32	30

① Tristate times are not tested. Timing specifications are derived from simulation.

TABLE 13-4. 80286 - NON-PAGE MODE 00 MEMORY TIMING

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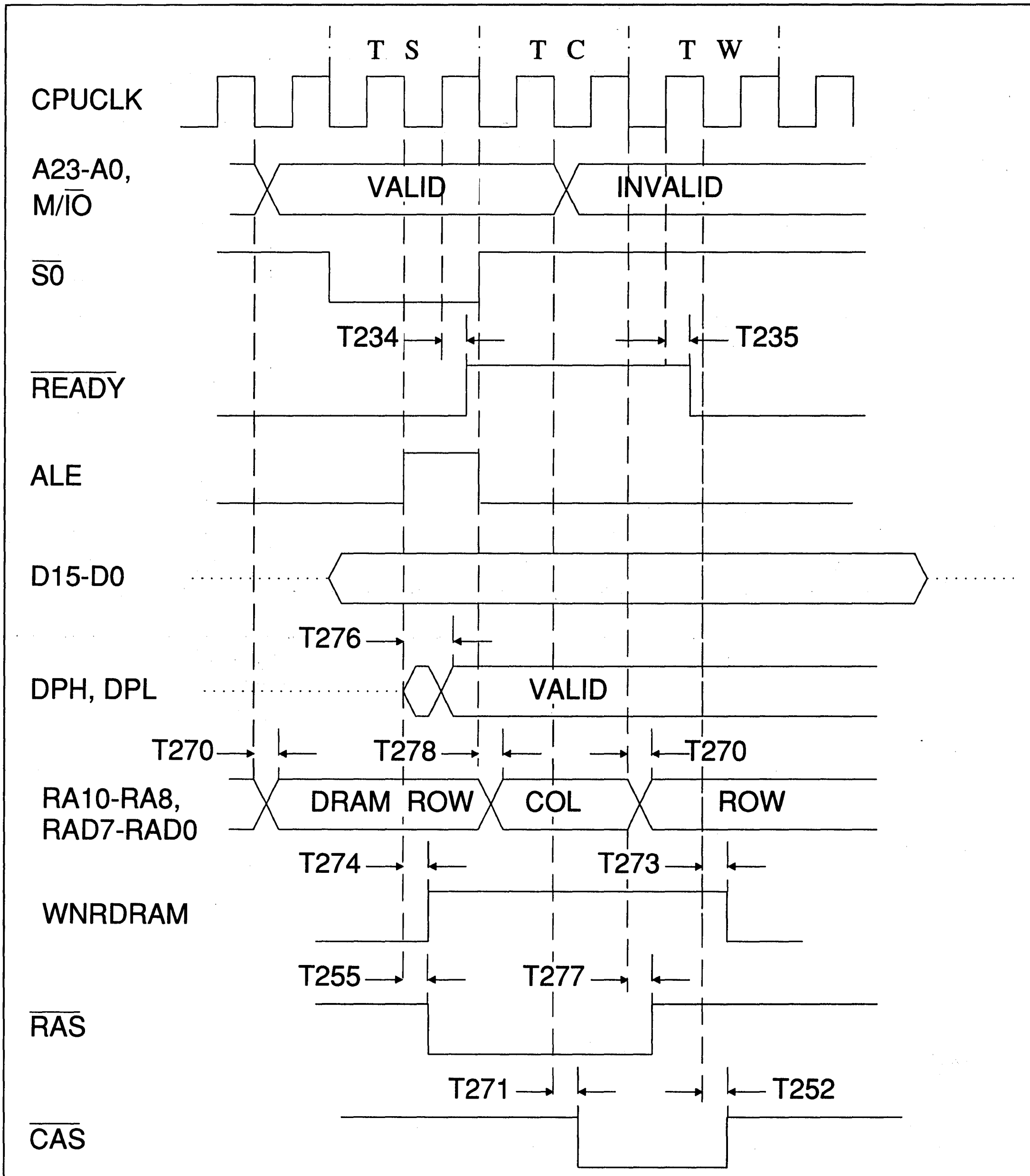

FIGURE 13-7. 80286 - NON-PAGE MODE 00, 1 WAIT STATE WRITE (4072H = 0001)

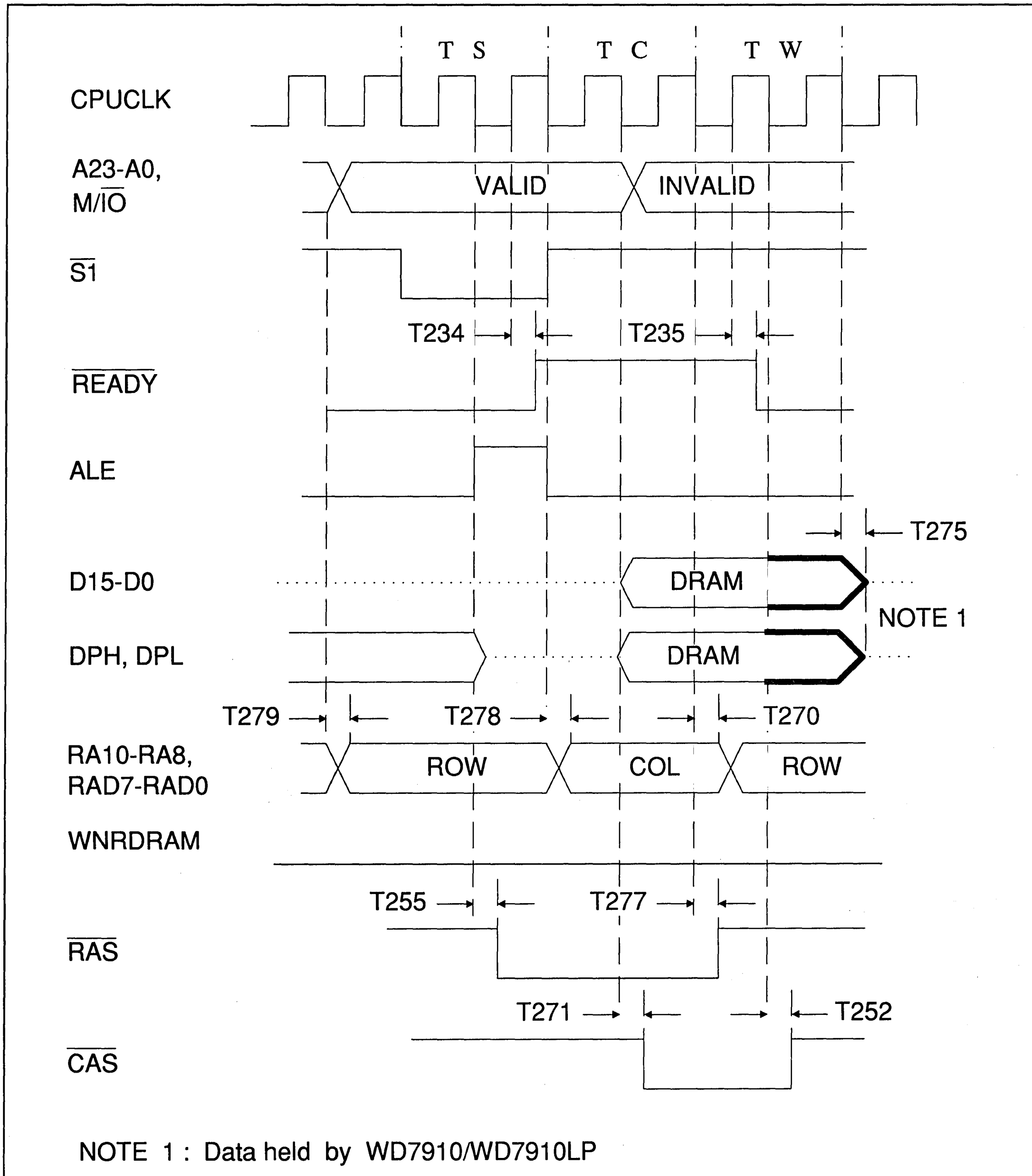

FIGURE 13-8. 80286 - NON-PAGE MODE 00, 1 WAIT STATE READ (4072H = 0001)

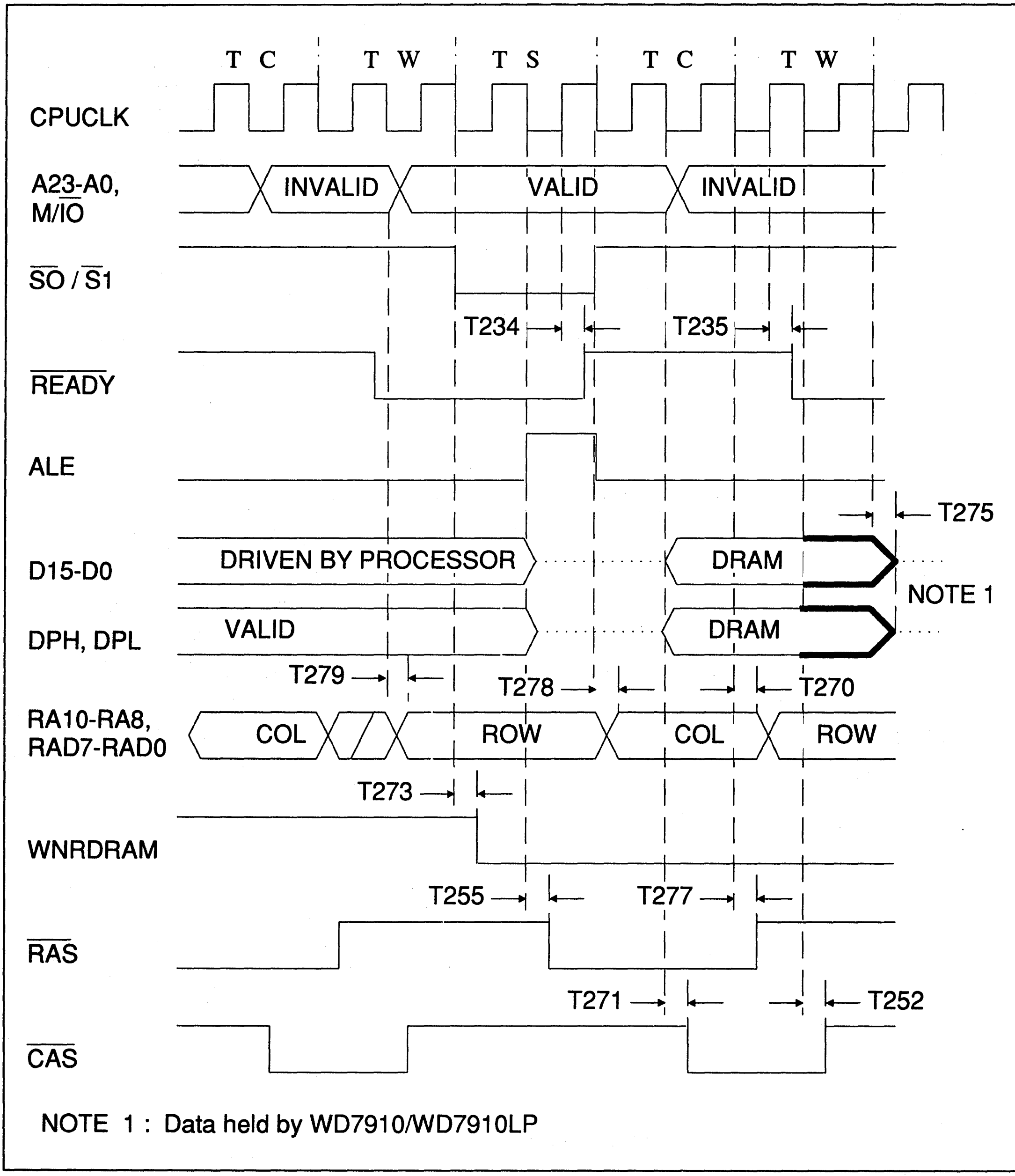

FIGURE 13-9. 80286 - NON-PAGE MODE MODE 00, 2 WAIT STATES READ AFTER WRITE (4072H = 0001)

13.1.3 80286 Non-Page Mode 01 Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz
T224	See Table 13-3		
T234	See Table 13-3		
T235	See Table 13-3		
T252	See Table 13-4		
T253	CPUCLK fall to WNRDRAM fall	34	31
T254	CPUCLK fall to WNRDRAM rise	34	31
T255	See Table 13-4		
T257	CPUCLK rise to $\overline{RAS}$ rise	35	32
T258	CPUCLK rise to COLUMN address valid	44	40
T276	See Table 13-4		

TABLE 13-5. 80286 - NON-PAGE MODE 01 MEMORY TIMING

8

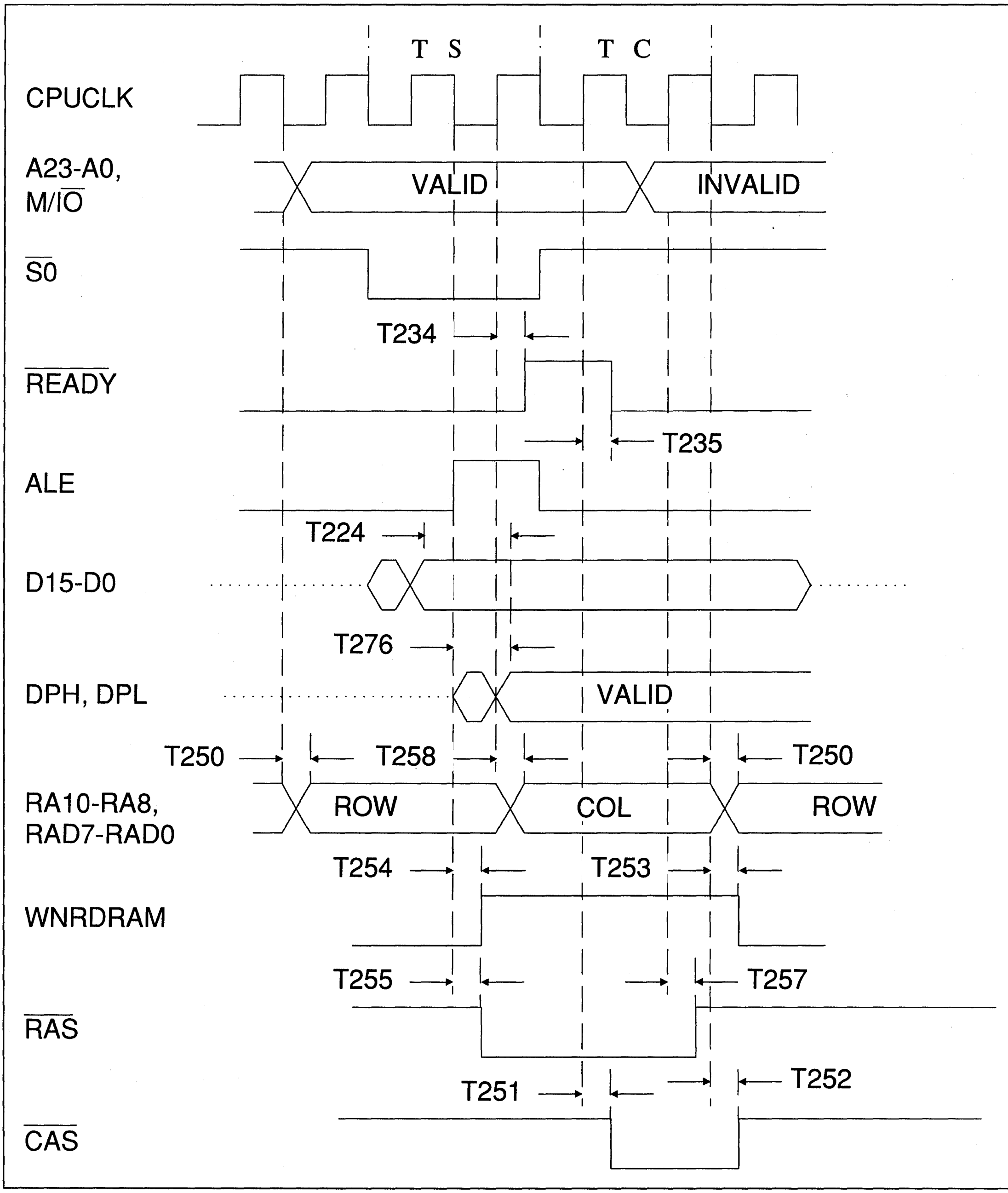

FIGURE 13-10. 80286 - NON-PAGE MODE 01, 0 WAIT STATE WRITE (4072H = 3560H)

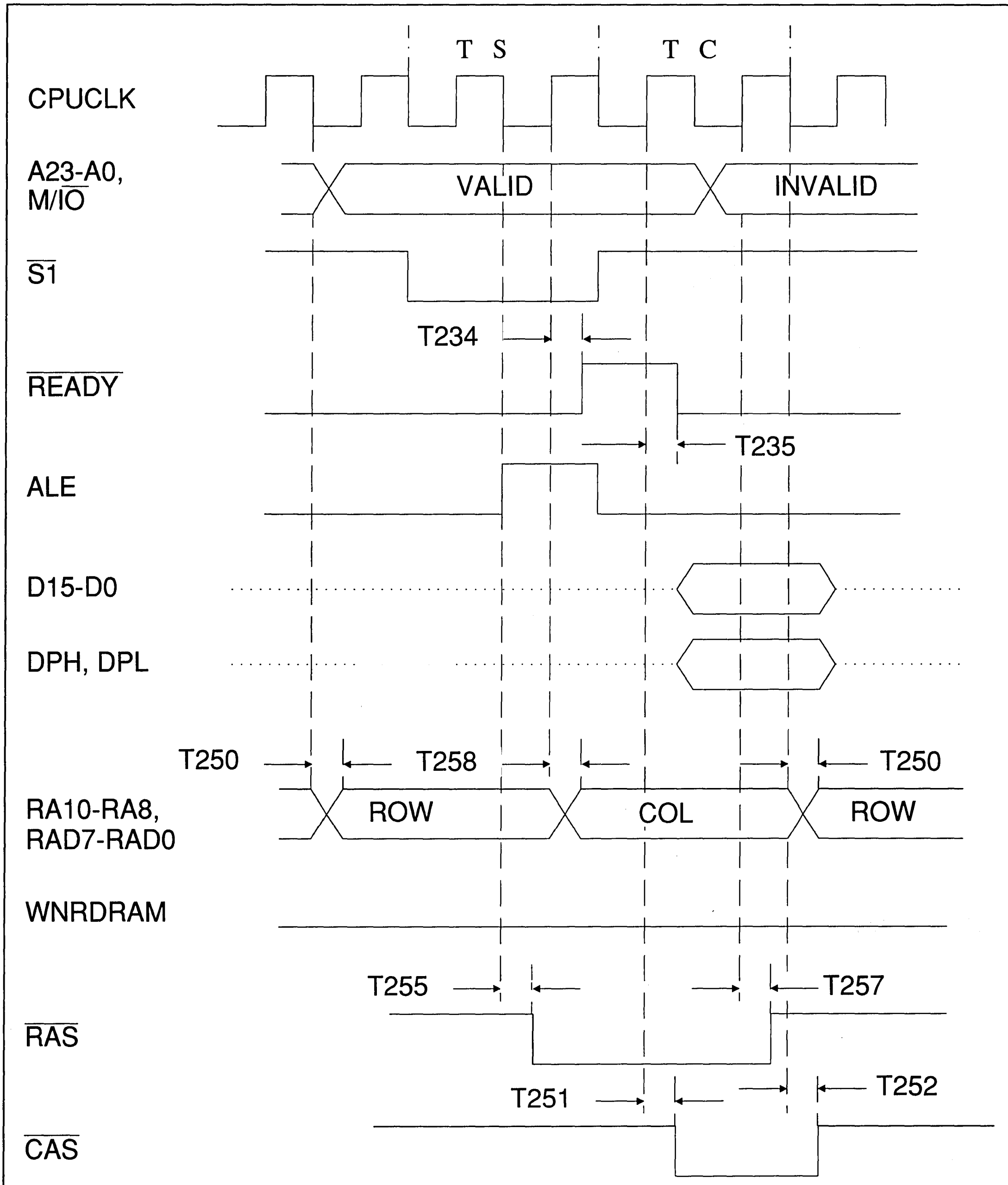

FIGURE 13-11. 80286 - NON-PAGE MODE 01, 0 WAIT STATE READ (4072H = 3560H)

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13.1.4 80386SX Page Mode Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz	MAX 25 MHz
T200	Processor ADDRESS to RAM address valid, Page Hit		34	27
T201	CPUCLK rise to CAS fall, 2.5 CLK CAS		31	25
T202	CPUCLK fall to CAS rise		24	21
T203	CPUCLK fall to CAS fall, 2.0 CLK CAS		27	22
T204	Processor data to parity valid		25	20
T205	CPUCLK rise to RAM address valid, Page Miss		48	43
T206	CPUCLK rise to WNRDRAM rise		31	28
T207	CPUCLK fall to RAS fall, first access		27	21
T208	CPUCLK rise to COLUMN address valid		49	33
T209	CPUCLK rise to WNRDRAM fall		31	28
T212	CPUCLK rise to RAS rise, Page Miss		27	24
T213	CPUCLK fall to RAS fall, Page Miss		27	24
T214	CPUCLK rise to READY fall		19	18
T215	CPUCLK rise to READY rise		19	18

TABLE 13-6. 80386SX - PAGE MODE MEMORY TIMING

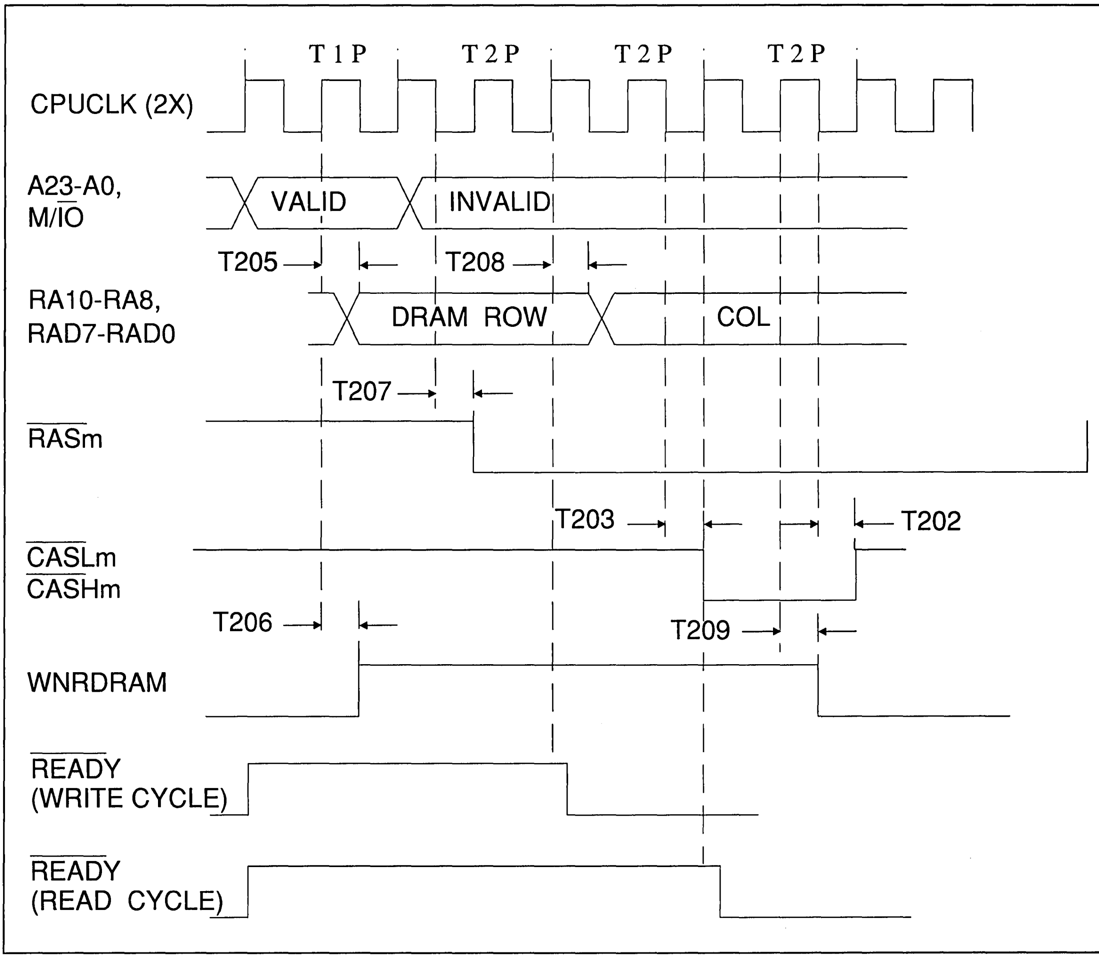

FIGURE 13-12. 80386SX - PAGE MODE, FIRST ACCESS READ/WRITE

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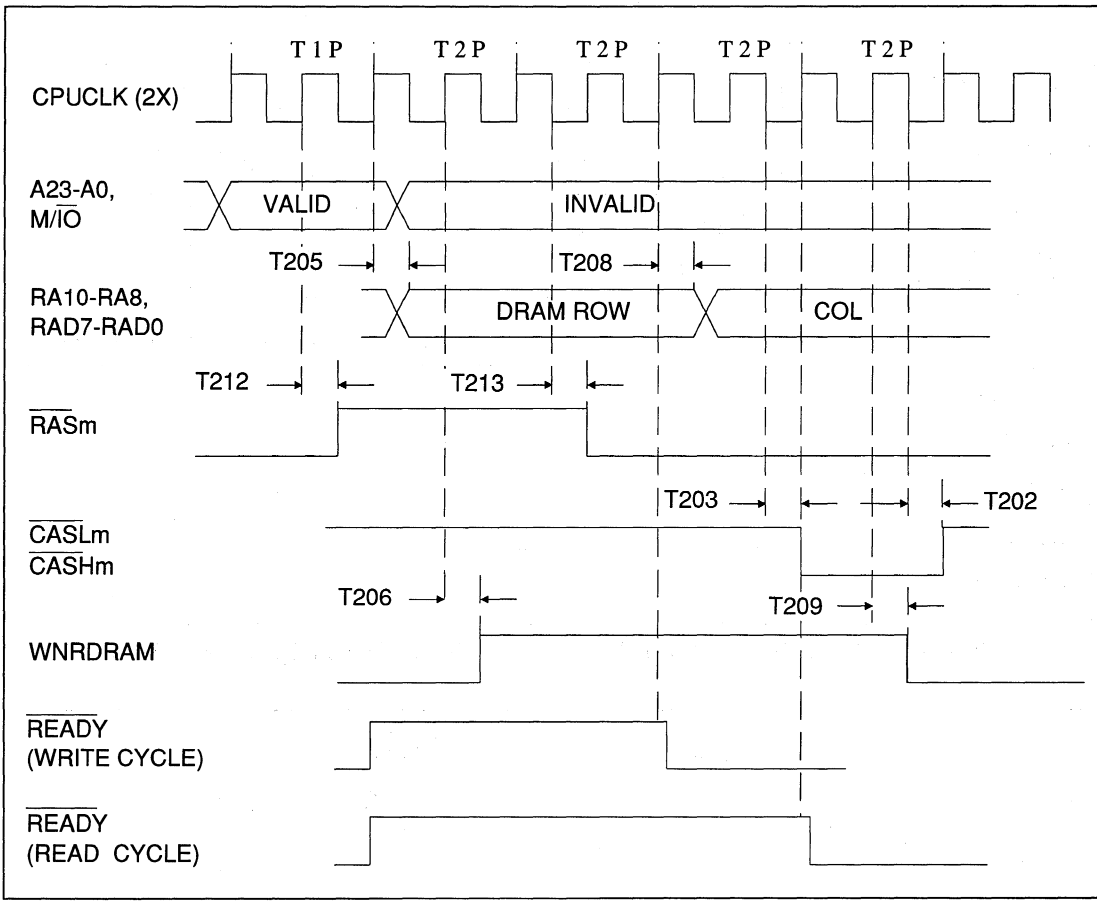


FIGURE 13-13. 80386SX - PAGE MODE, PAGE MISS READ/WRITE

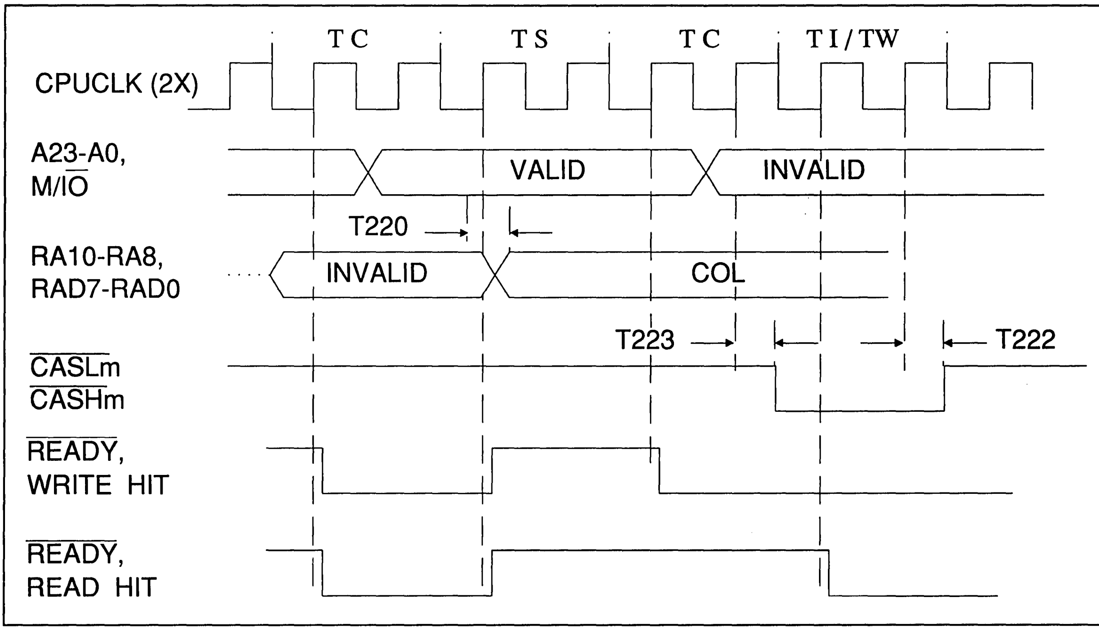


FIGURE 13-14. 80386SX - PAGE MODE, RAD CYCLE FOLLOWED BY A PAGE HIT

8

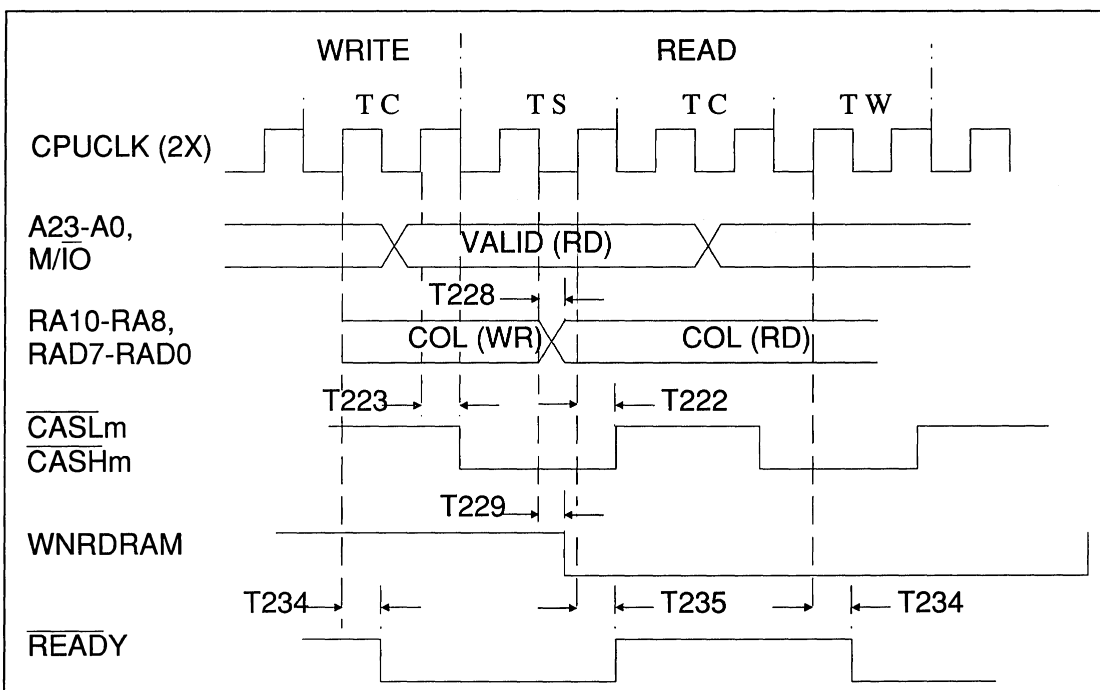


FIGURE 13-15. 80386SX - PAGE MODE, READ AFTER WRITE

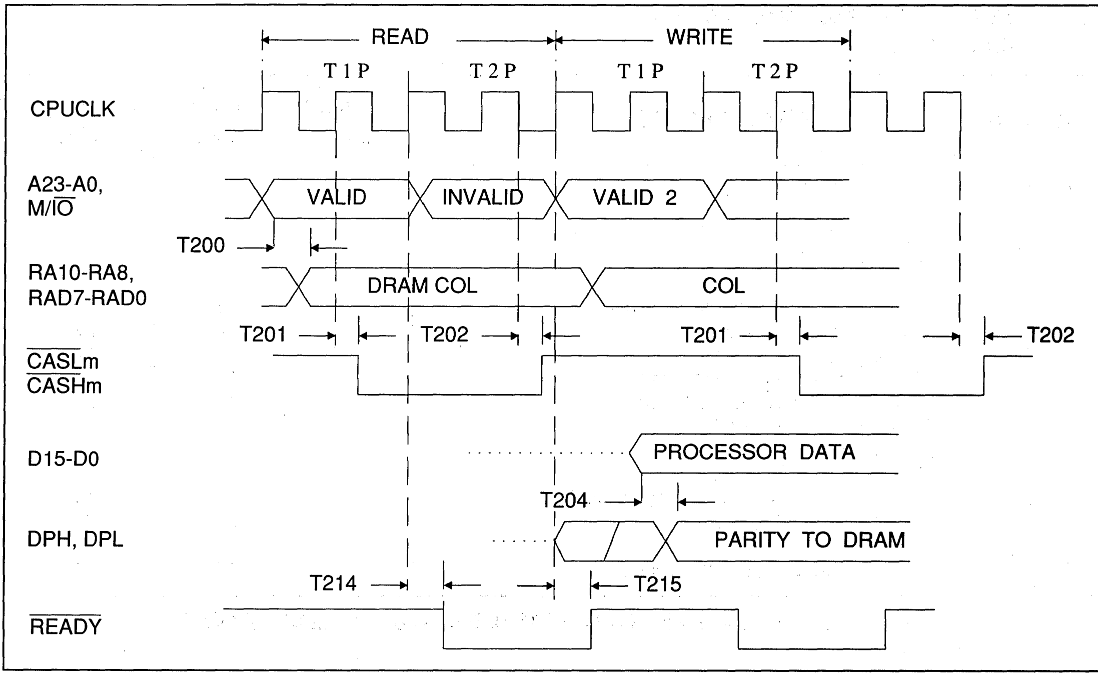


FIGURE 13-16. 80386SX - PAGE MODE, READ HIT FOLLOWED BY A WRITE HIT

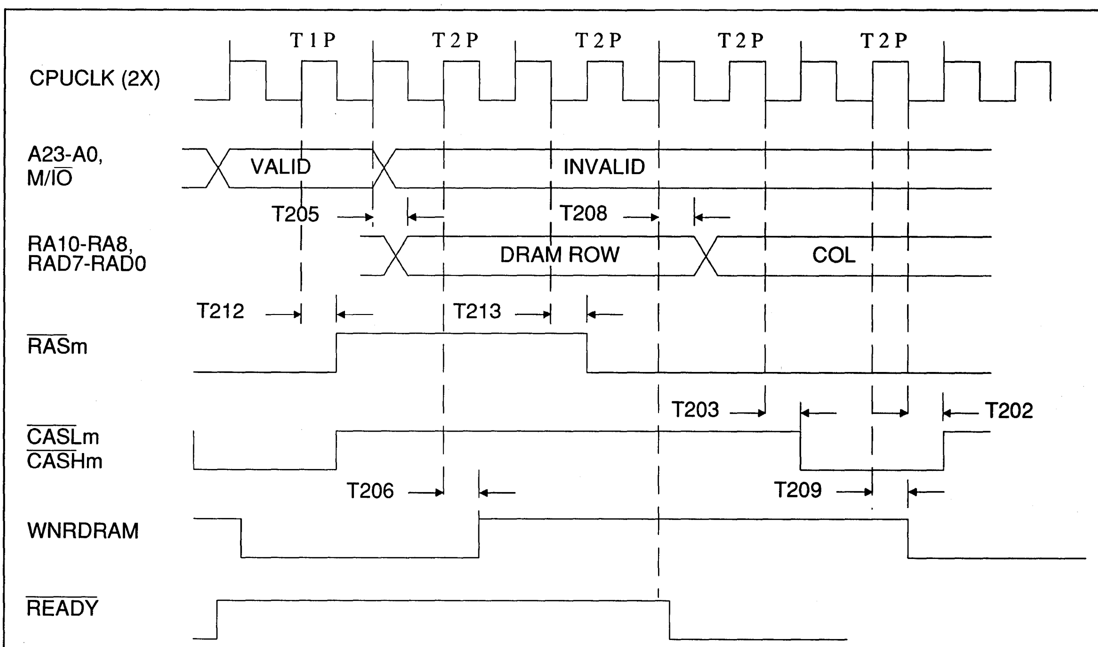


FIGURE 13-17. 80386SX - PAGE MODE, WRITE MISS CYCLE FOLLOWING A WRITE CYCLE

13.1.5 80386SX Non-Page Mode 00 And Mode 01 Timing

SYMBOL	CHARACTERISTIC	MAX 12.5 MHz	MAX 20 MHz	MAX 25 MHz
T204	See Table 13-6			
T214	See Table 13-6			
T215	See Table 13-6			
T240	CPUCLK rise to ROW address valid		42	42
T241	CPUCLK fall to CAS fall		27	27
T242	CPUCLK rise to CAS rise		28	24
T243	CPUCLK rise to WNRDRAM fall		28	28
T244	CPUCLK rise to WNRDRAM rise		28	28
T245	CPUCLK rise to RAS fall		25	23
T246	CPUCLK rise to RAS rise		25	23
T247	CPUCLK fall to RAS rise		29	29
T248	CPUCLK fall to COLUMN address valid		44	44
T249	CPUCLK rise to CAS fall		29	29
T260	CPUCLK rise to COLUMN address		43	41

TABLE 13-7. 80386SX - NON-PAGE MODE 00 & 01 MEMORY TIMING

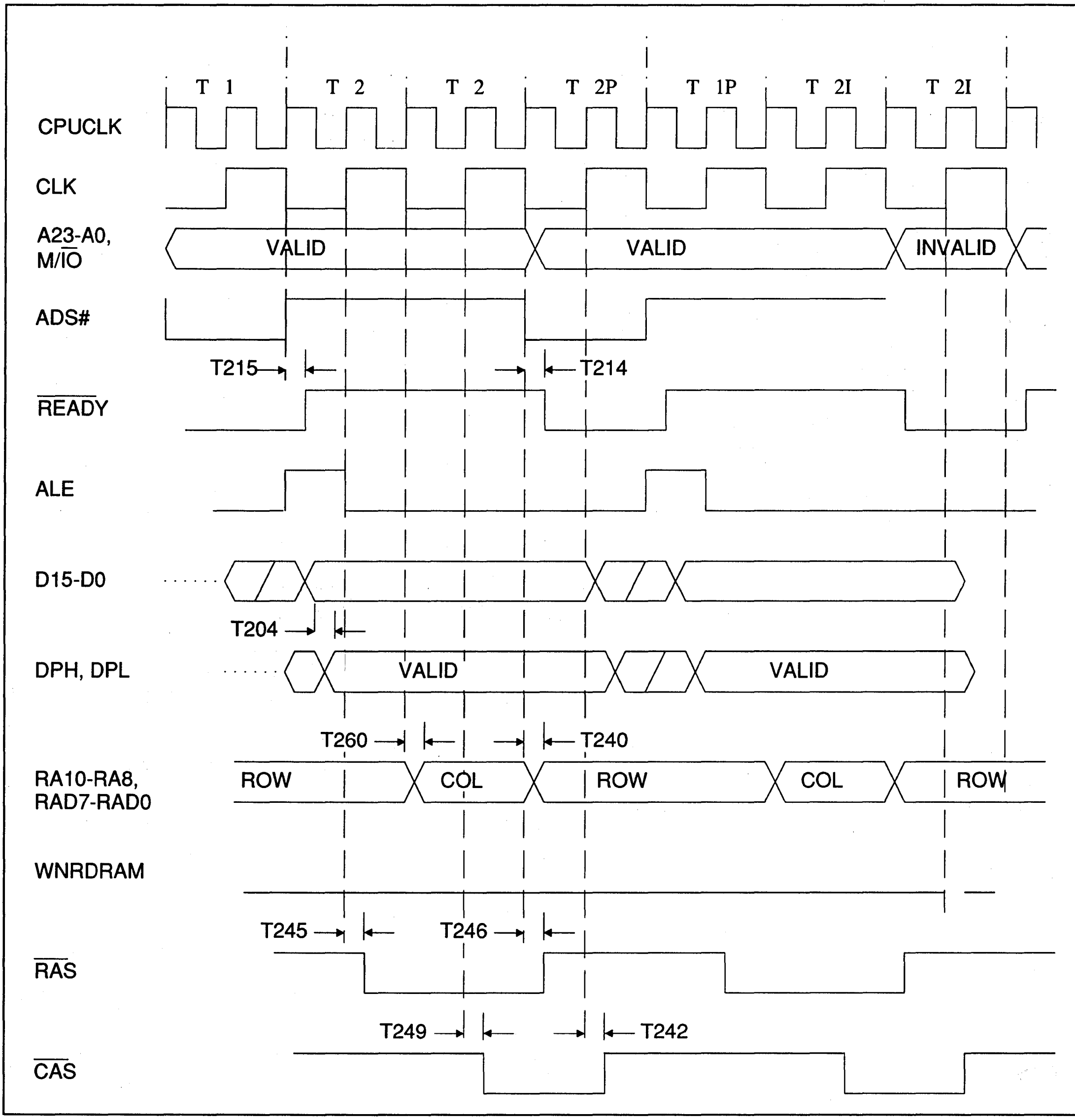


FIGURE 13-18. 80386SX - NON-PAGE MODE 00, 1 WAIT STATE READ (PIPELINE) (4072H = 0001)

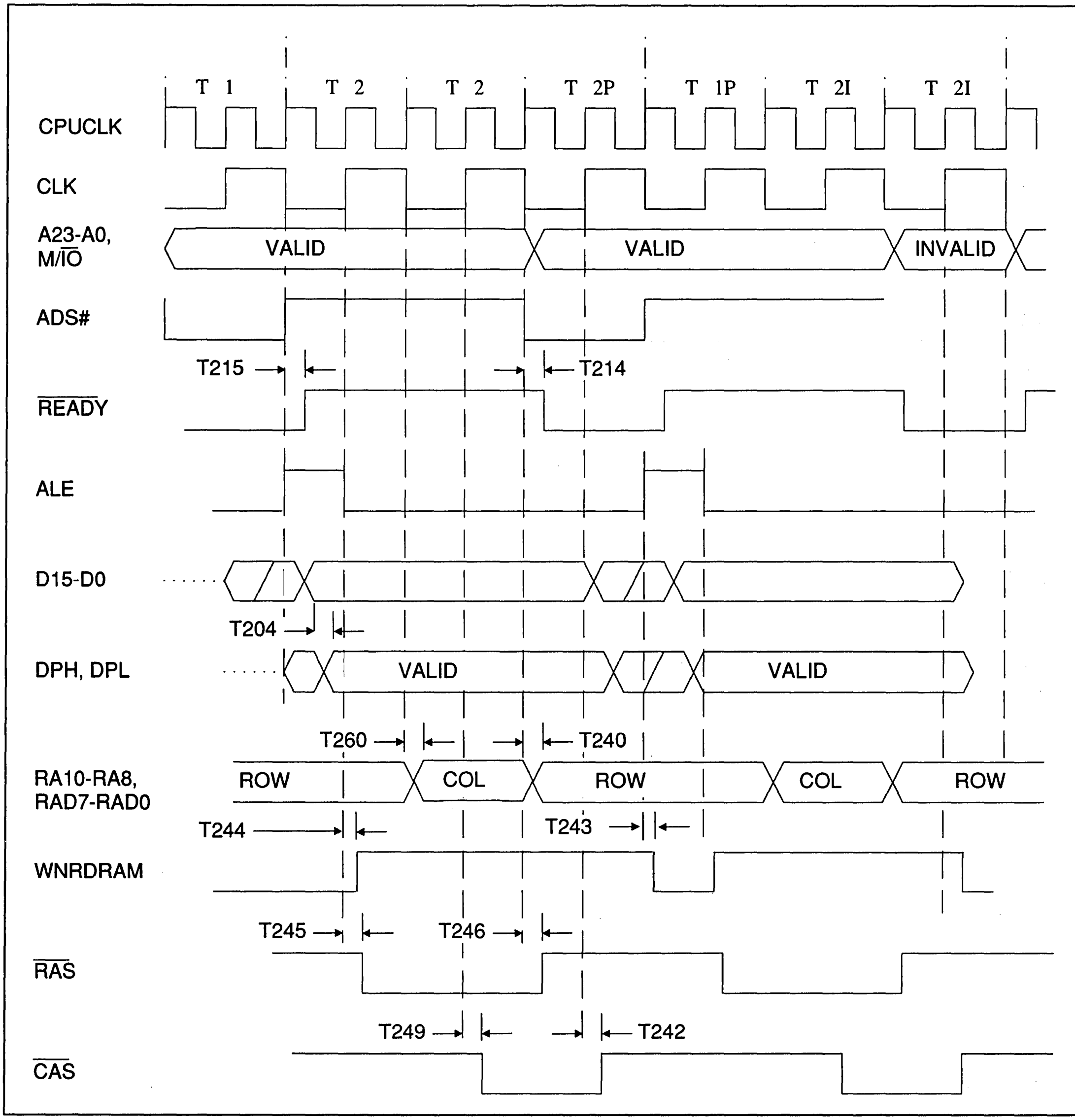


FIGURE 13-19. 80386SX - NON-PAGE MODE 00, 1 WAIT STATE WRITE (PIPELINE) (4072H = 0001)

8

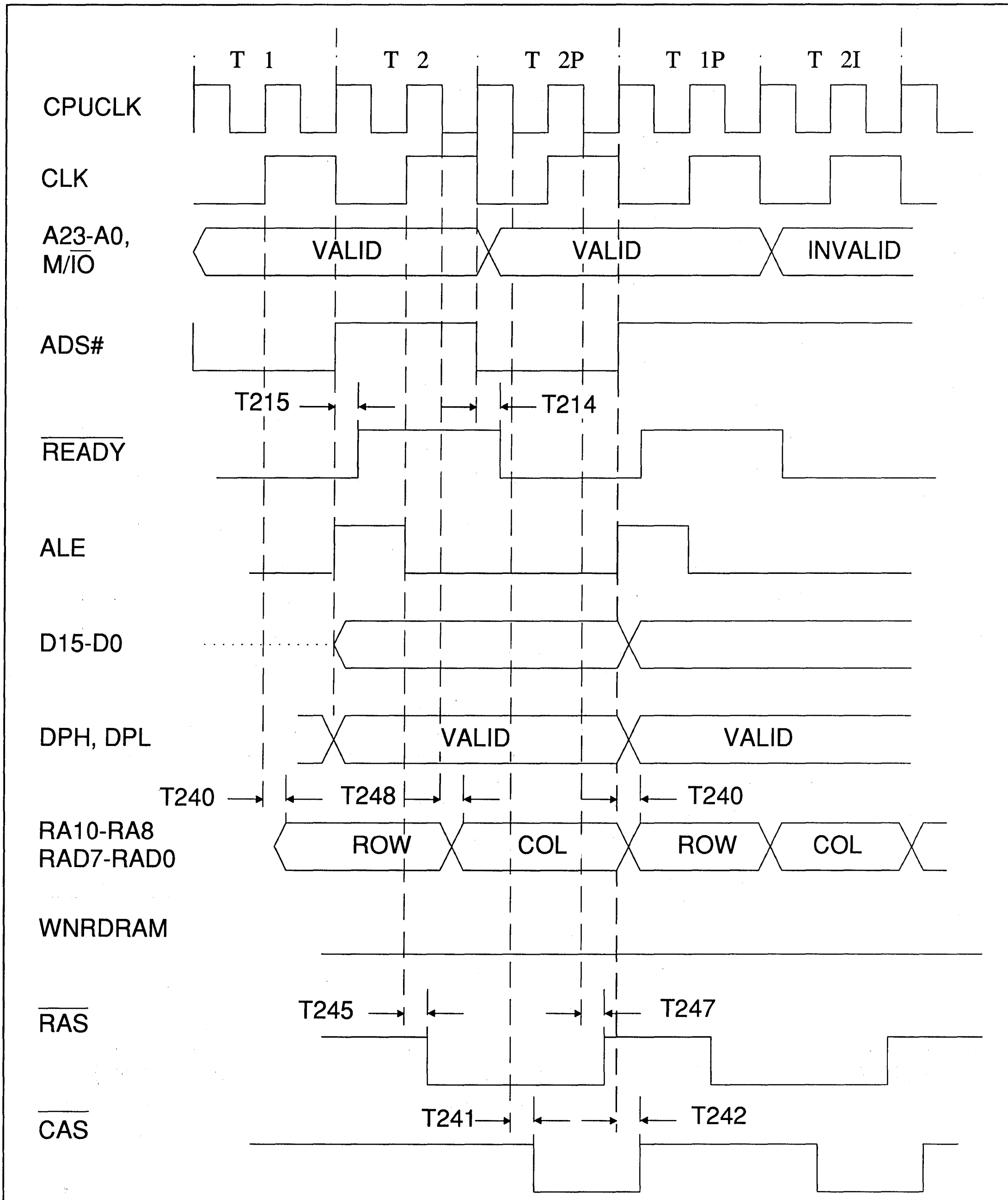


FIGURE 13-20. 80386SX - NON-PAGE MODE 01, 0 WAIT STATE READ (PIPELINE) (4072H = 3560H)

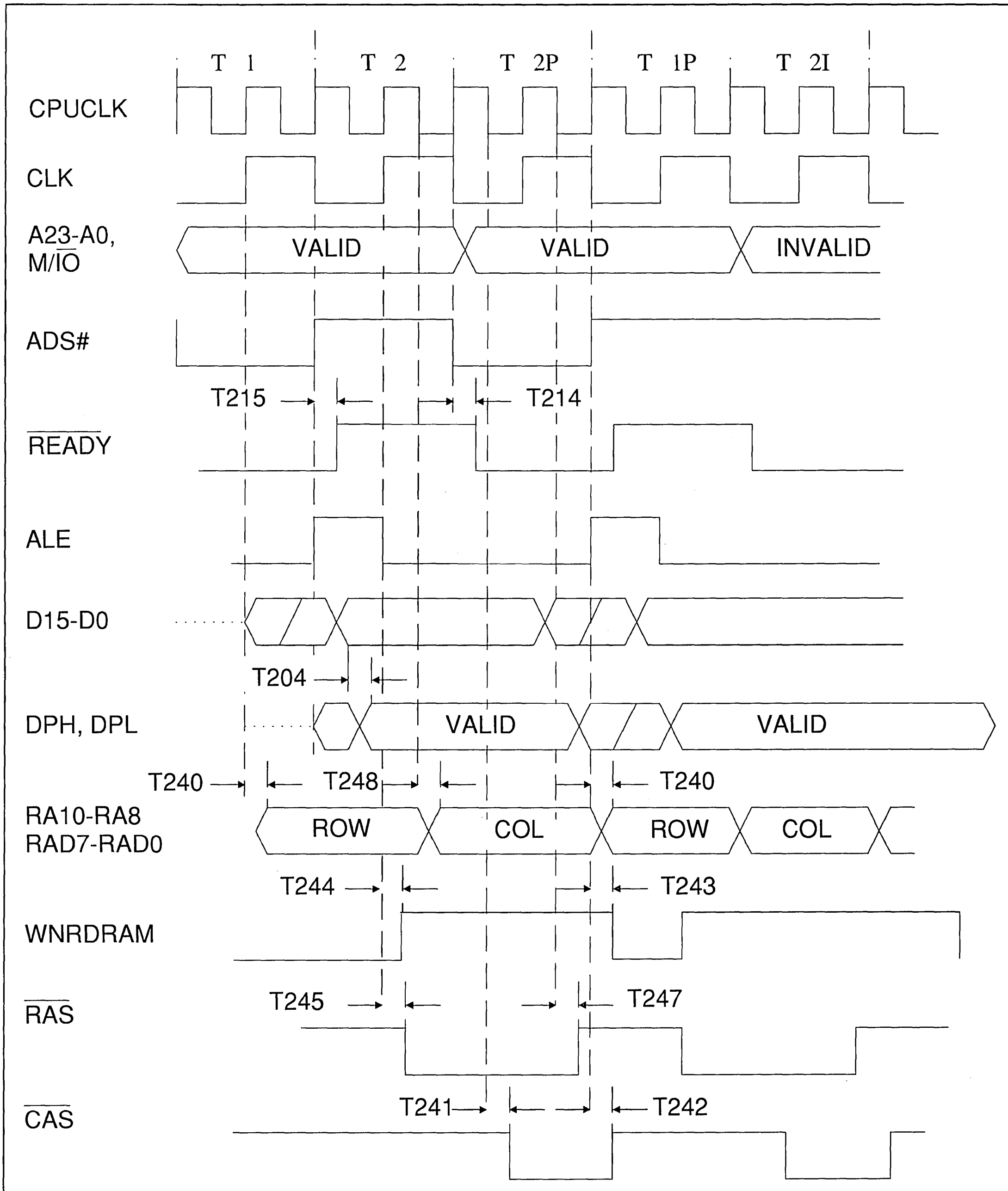


FIGURE 13-21. 80386SX - NON-PAGE MODE 01, 0 WAIT STATE READ (PIPELINE) (4072H = 3560H)

8

13.2 AT BUS TIMING

The AT Bus timing is divided into six major categories:

1. CPU initiated AT Bus cycles.
2. Entering the AT Bus.
3. Exiting the AT Bus.
4. DMA cycles.
5. AT Bus Master cycles.
6. AT Bus refresh cycle

Some figures in this section are included only to show the sequence of the signals during certain operations. In these figures, no timing parameters are provided.

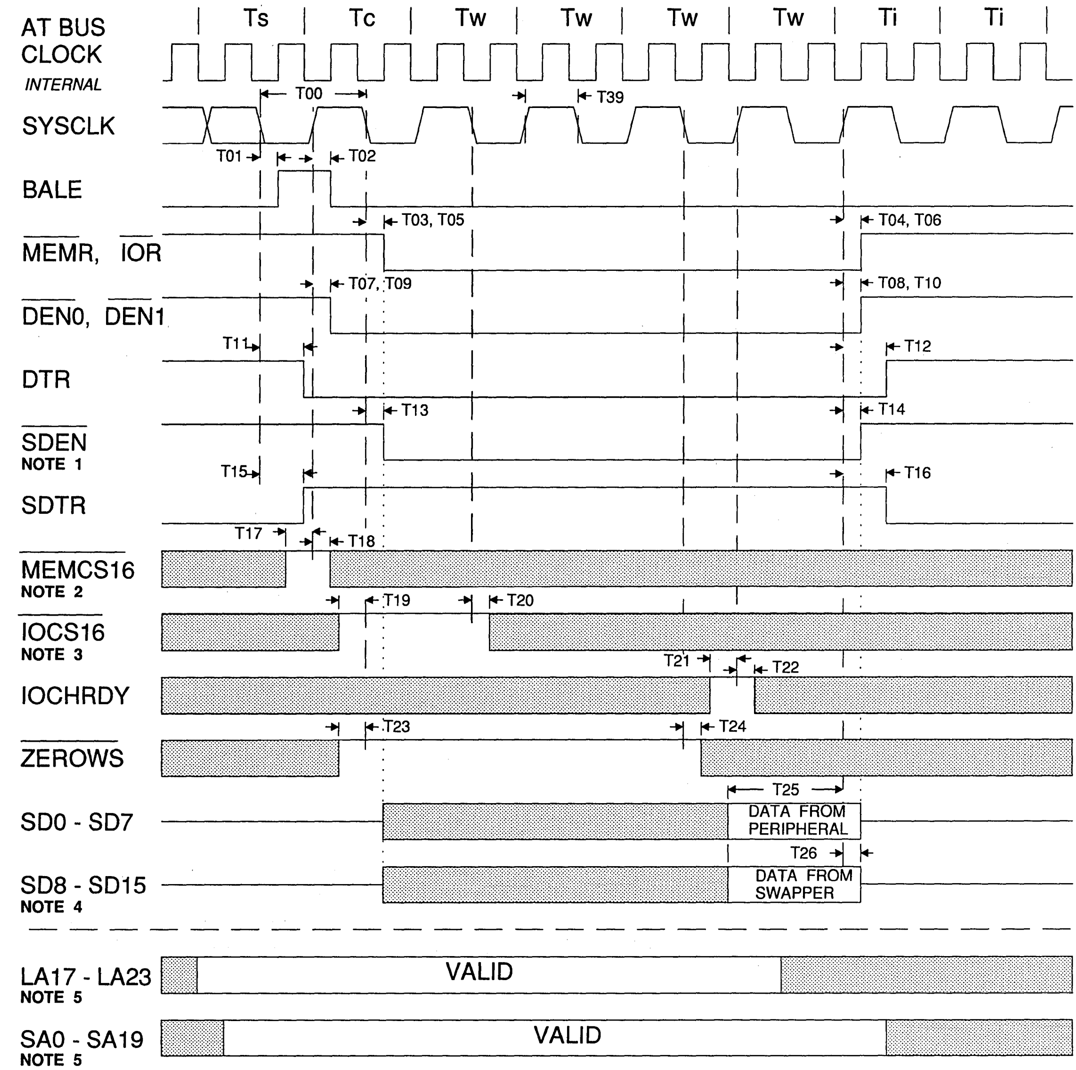
13.2.1 CPU Initiated AT Bus Cycles

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T00	SYSCLK Cycle Time	100		ns	
T01	SYSCLK fall to BALE rise		12	ns	
T02	SYSCLK rise to BALE fall		9	ns	
T03	SYSCLK fall to $\overline{\text{MEMR}}$ fall		9	ns	8-bit cycle
T04	SYSCLK rise to $\overline{\text{MEMR}}$ rise		6	ns	
T05	SYSCLK fall to $\overline{\text{IOR}}$ fall		10	ns	
T06	SYSCLK rise to $\overline{\text{IOR}}$ rise		7	ns	
T07	SYSCLK rise to $\overline{\text{DEN0}}$ fall		7	ns	Read Cycle
T08	SYSCLK rise to $\overline{\text{DEN0}}$ rise		11	ns	Read Cycle
T09	SYSCLK rise to $\overline{\text{DEN1}}$ fall		7	ns	Read Cycle
T10	SYSCLK rise to $\overline{\text{DEN1}}$ rise		9	ns	Read Cycle
T11	SYSCLK fall to DTR fall		19	ns	Delay is number given plus (T00 × 0.25)
T12	SYSCLK rise to DTR rise		14	ns	Delay is number given plus (T00 × 0.25)
T13	SYSCLK fall to $\overline{\text{SDEN}}$ fall		10	ns	
T14	SYSCLK rise to $\overline{\text{SDEN}}$ rise		8	ns	
T15	SYSCLK fall to SDTR rise		14	ns	Delay is number given plus (T00 × 0.25)
T16	SYSCLK rise to SDTR fall		11	ns	Delay is number given plus (T00 × 0.25)
T17	$\overline{\text{MEMCS16}}$ setup time to SYSCLK rise	25		ns	
T18	$\overline{\text{MEMCS16}}$ hold time from SYSCLK rise	0		ns	
T19	$\overline{\text{IOCS16}}$ setup time to SYSCLK fall	23		ns	
T20	$\overline{\text{IOCS16}}$ hold time from SYSCLK fall	0		ns	8-bit cycle

TABLE 13-8. CPU INITIATED AT BUS CYCLES

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T21	IOCHRDY setup time to SYSCLK rise	22		ns	
T22	IOCHRDY hold time from SYSCLK rise	0		ns	
T23	ZEROWS setup time to SYSCLK fall	24		ns	
T24	ZEROWS hold time from SYSCLK fall	0		ns	
T25	AT Bus data setup time to SYSCLK rise	22		ns	Total setup time is number given plus delay through AT Bus data buffers.
T26	AT Bus data hold time from SYSCLK rise	0		ns	
T27	SYSCLK fall to MEMW fall		9	ns	
T28	SYSCLK rise to MEMW rise		5	ns	
T29	SYSCLK fall to IOW fall		10	ns	
T30	SYSCLK rise to IOW rise		8	ns	
T31	SYSCLK fall to DEN0 fall		10	ns	Write cycle
T32	SYSCLK fall to DEN0 rise		9	ns	Write cycle
T33	SYSCLK fall to DEN1 fall		10	ns	Write cycle
T34	SYSCLK fall to DEN1 rise		9	ns	Write cycle
T35	SYSCLK fall to SDEN rise		11	ns	
T36	SYSCLK fall to SA0 rise		16	ns	Word to byte conversion cycle
T37	SYSCLK rise to MEMR fall		6	ns	16-bit cycle
T38	IOCS16 hold time from SYSCLK rise	0		ns	16-bit cycle
T39	SYSCLK high time	-4	0	ns	(T00 ÷ 2) plus number given

TABLE 13-8. CPU INITIATED BUS CYCLES cont.



NOTE 1: SDEN is asserted only when SA0 is high.

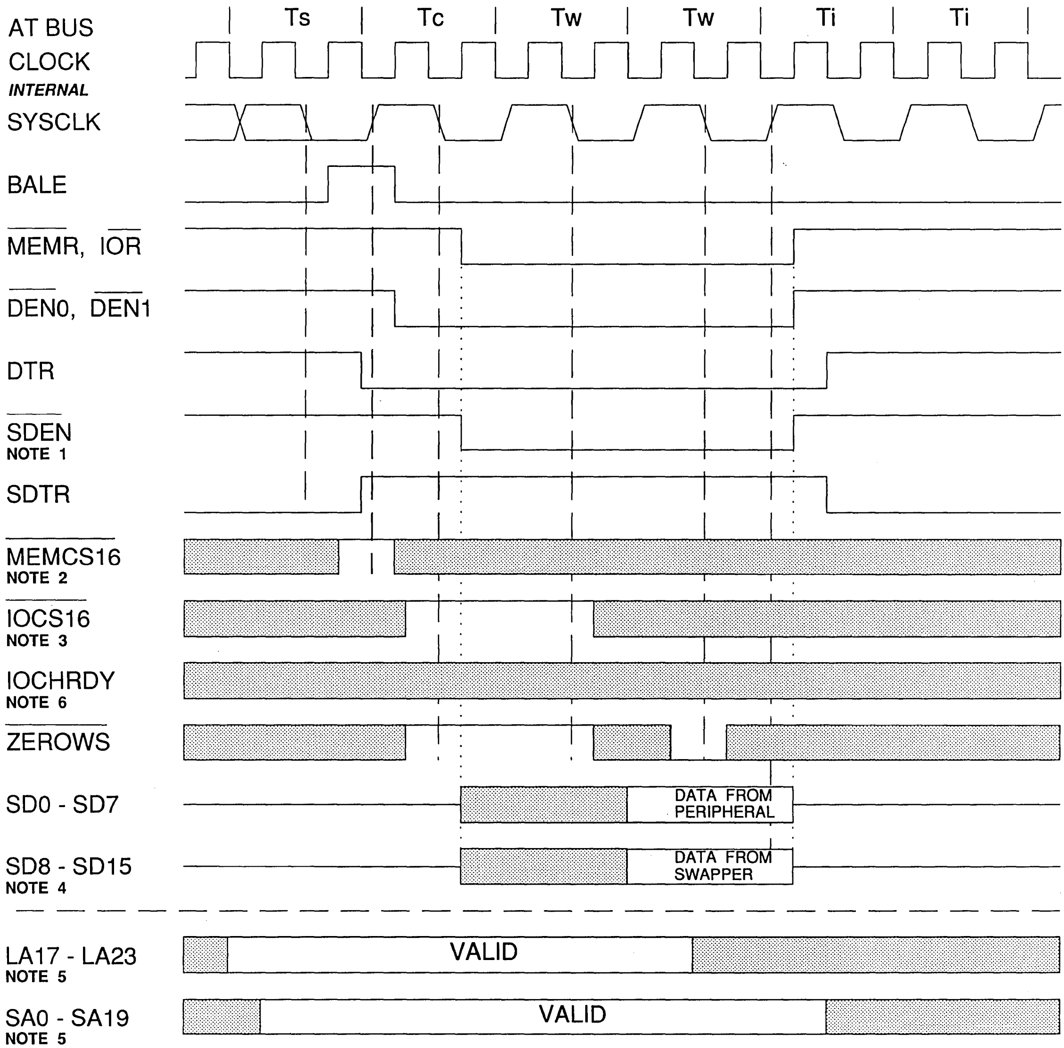
NOTE 2: MEMCS16 is sampled only during memory cycles.

NOTE 3: IOCS16 is sampled only during I/O cycles.

NOTE 4: SD8 - 15 are driven by the data swapper only when SA0 is high (SDEN asserted).

NOTE 5: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 13-22. AT BUS I/O OR MEMORY READ: 8-BIT, DEFAULT TIMING



NOTE 1: SDEN is asserted only when SA0 is high.

NOTE 2: MEMCS16 is sampled only during memory cycles.

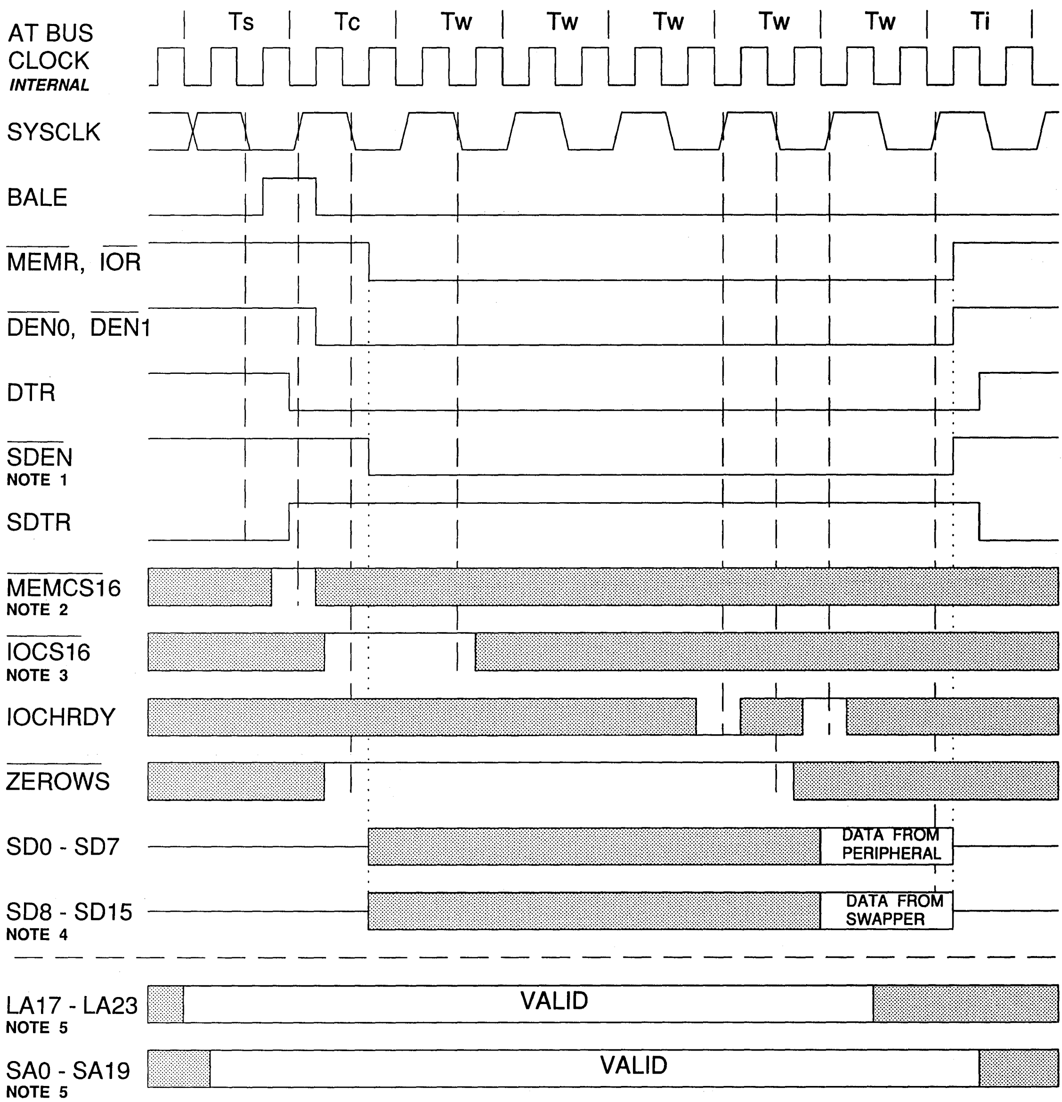
NOTE 3: IOCS16 is sampled only during I/O cycles.

NOTE 4: SD8 - 15 are driven by the data swapper only when SA0 is high (SDEN asserted).

NOTE 5: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

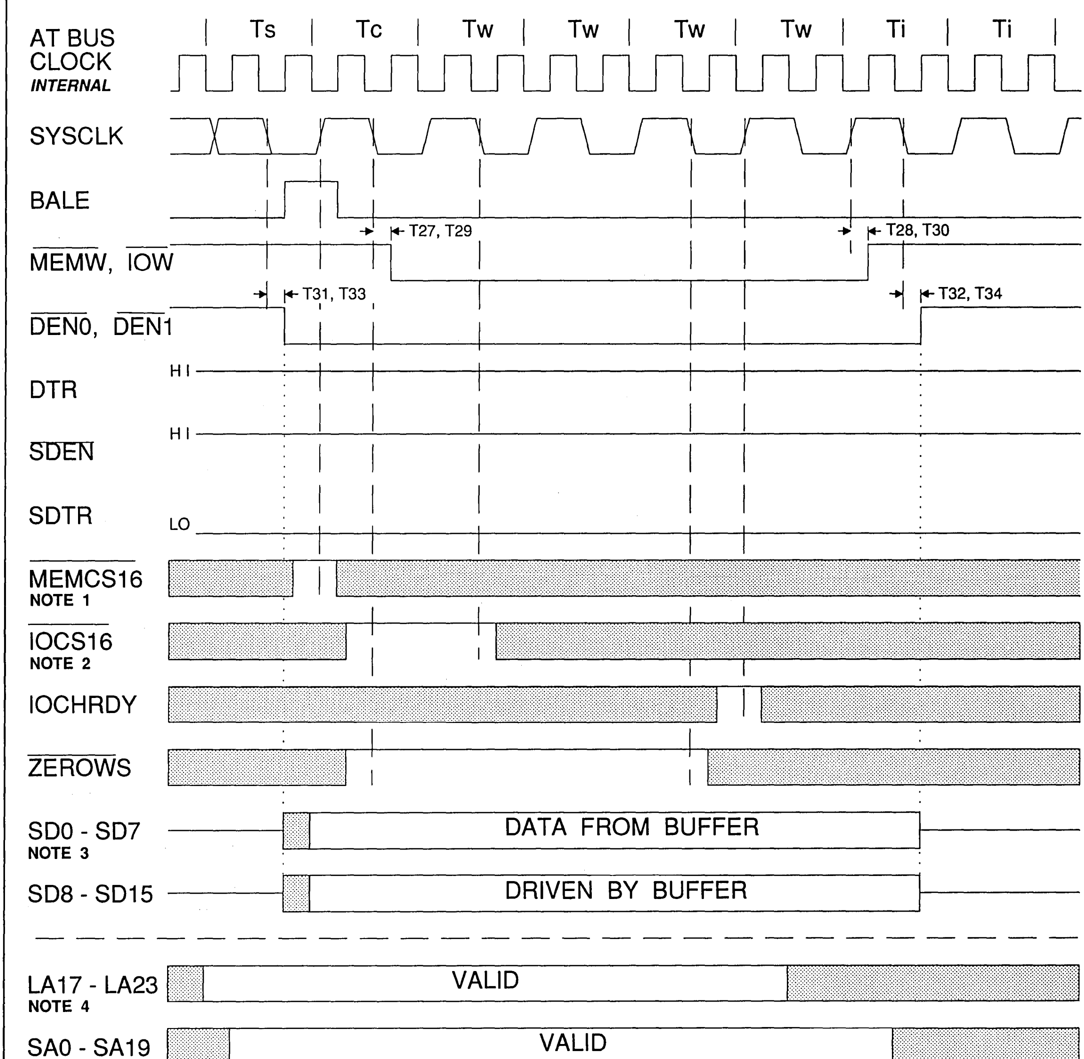
NOTE 6: IOCHRDY overrides ZEROWS only during the first cycle of a word to byte conversion.

FIGURE 13-23. AT BUS I/O OR MEMORY READ: 8-BIT, ZEROWS ASSERTED



NOTE 1: $\overline{\text{SDEN}}$ is asserted only when SA0 is high.
NOTE 2: $\overline{\text{MEMCS16}}$ is sampled only during memory cycles.
NOTE 3: $\overline{\text{IOCS16}}$ is sampled only during I/O cycles.
NOTE 4: SD8 - 15 are driven by data swapper only when SA0 is high ($\overline{\text{SDEN}}$ asserted).
NOTE 5: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 13-24. AT BUS I/O OR MEMORY READ: 8-BIT, EXTRA WAIT STATE ADDED



NOTE 1: MEMCS16 is sampled only during memory cycles.

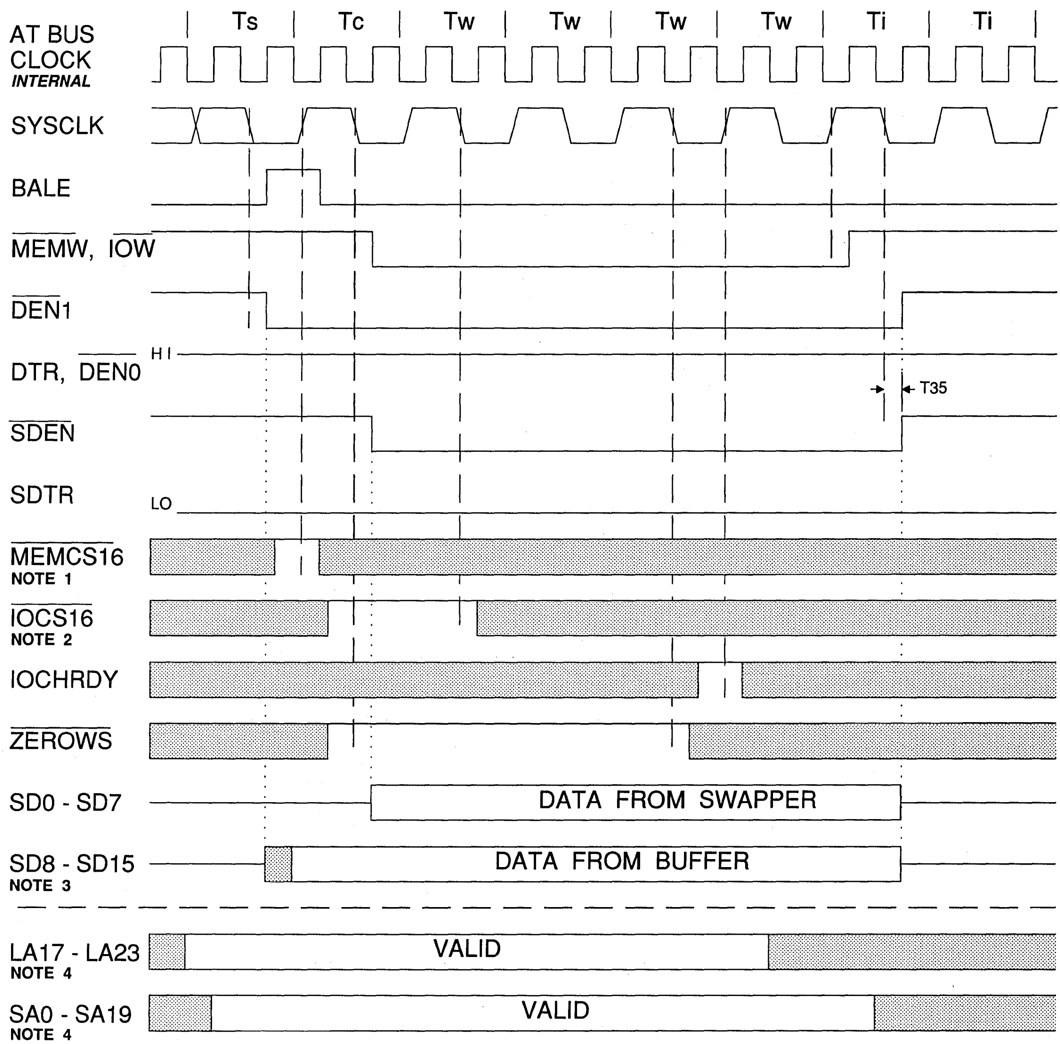
NOTE 2: IOCS16 is sampled only during I/O cycles.

NOTE 3: The small period of unknown data on SD0 - 7 when DEN0 is asserted is dependent on register settings and may be asynchronous. Minimum valid time is shown for reference.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 13-25. AT BUS I/O OR MEMORY WRITE: 8-BIT, EVEN BYTE, DEFAULT TIMING

8



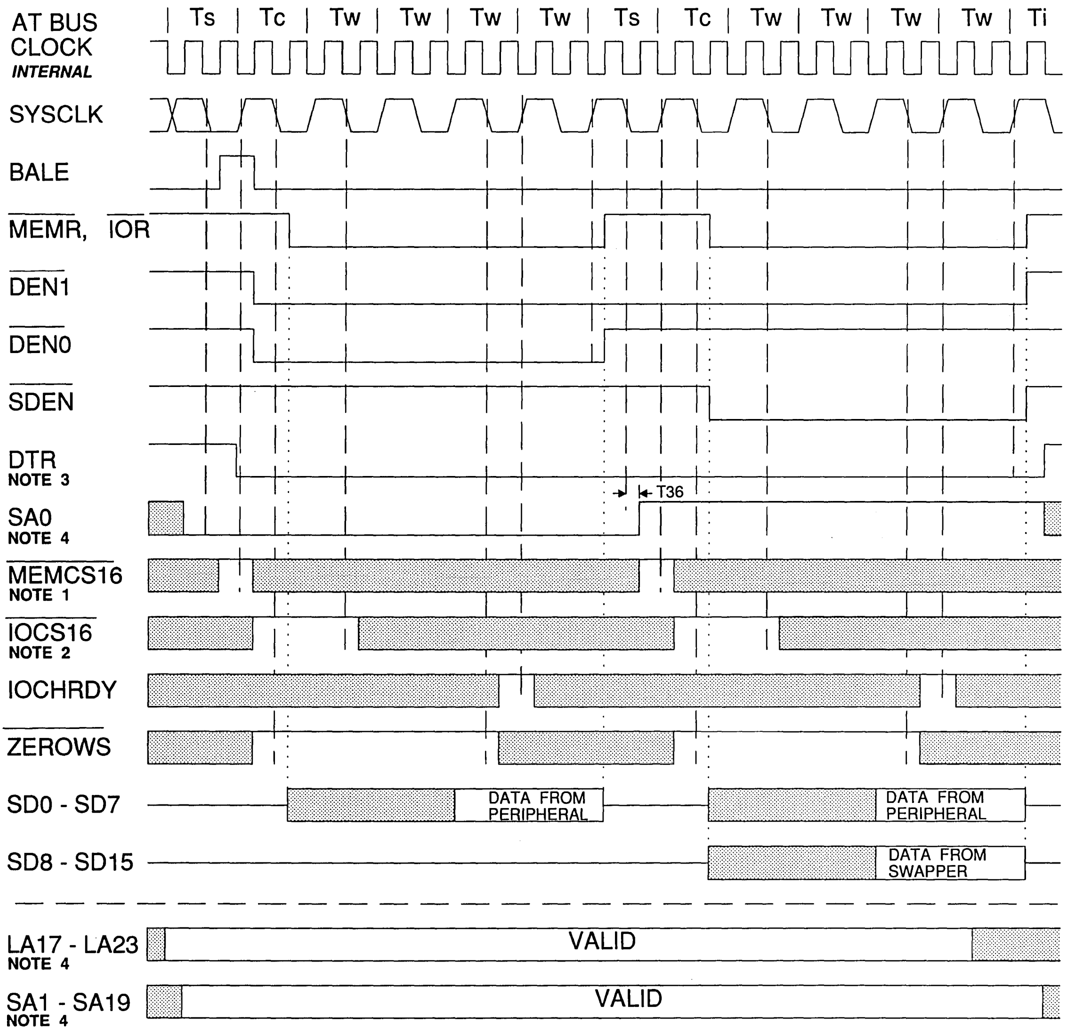
NOTE 1: MEMCS16 is sampled only during memory cycles.

NOTE 2: IOCS16 is sampled only during I/O cycles.

NOTE 3: The small period of unknown data on SD8 - 15 when DEN1 is asserted is dependent on register settings and may be asynchronous. Minimum valid time is shown for reference.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 13-26. AT BUS I/O OR MEMORY WRITE: 8-BIT, ODD BYTE, DEFAULT TIMING



NOTE 1: MEMCS16 is sampled only during memory cycles.

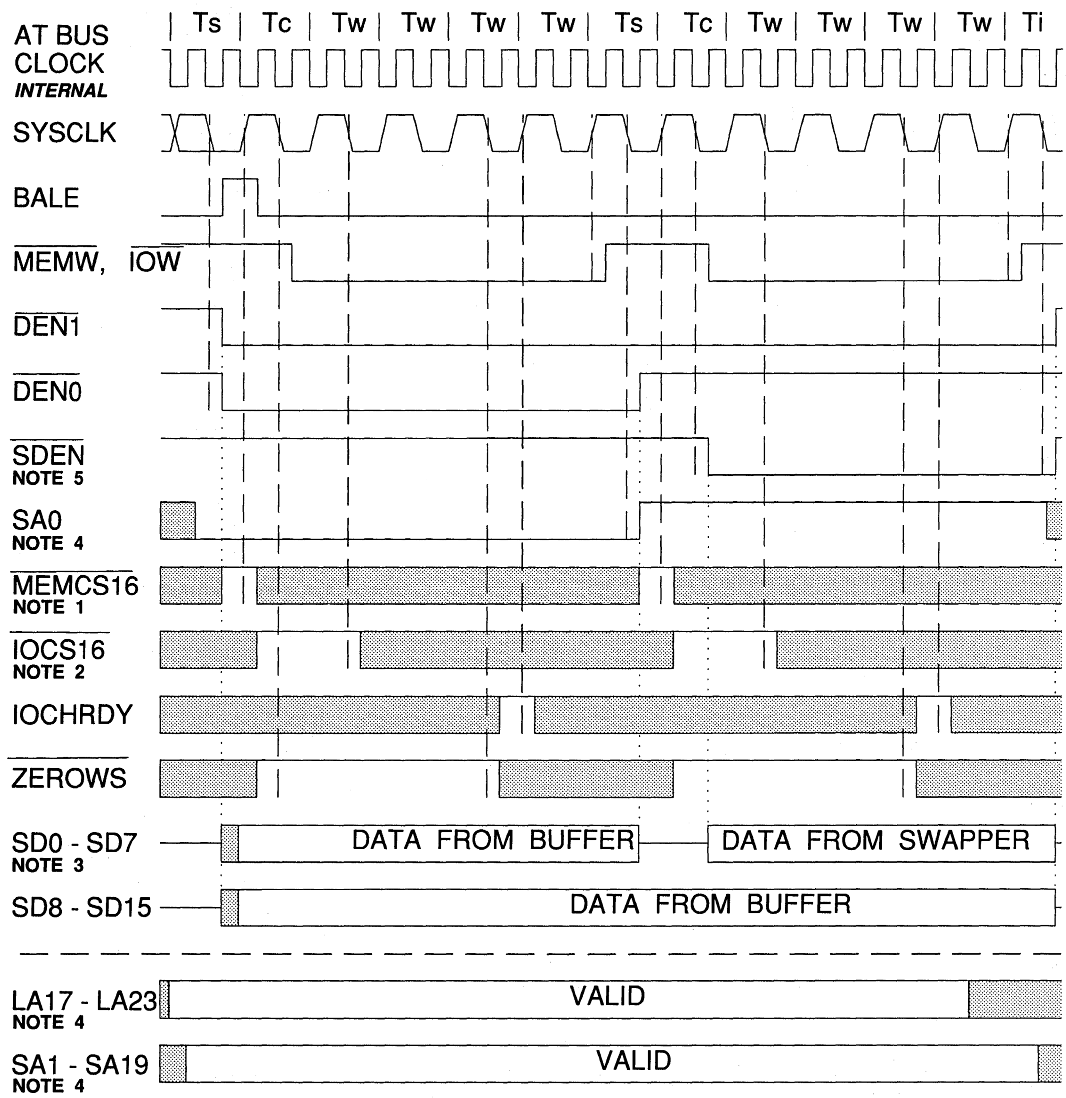
NOTE 2: IOCS16 is sampled only during I/O cycles.

NOTE 3: SDTR is the inversion of DTR during CPU transfer cycles.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 13-27. AT BUS I/O OR MEMORY READ: 8-BIT, WORD TO BYTE CONVERSION, DEFAULT TIMING

8



NOTE 1: MEMCS16 is sampled only during memory cycles.

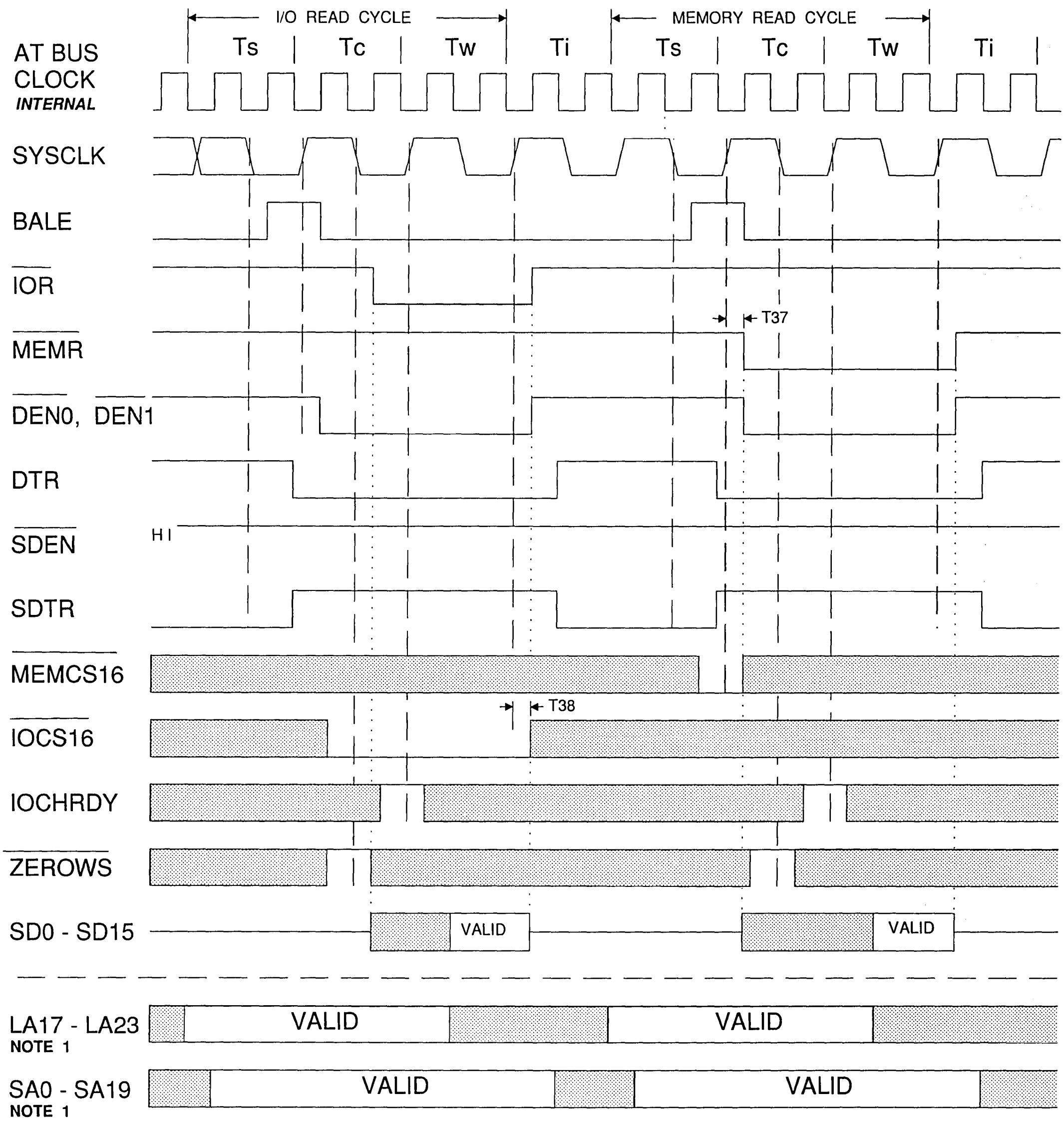
NOTE 2: IOCS16 is sampled only during I/O cycles.

NOTE 3: The small period of unknown data on SD0 - 7 when DEN0 is asserted is dependent on register settings and may be synchronous. Minimum valid time is shown for reference.

NOTE 4: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

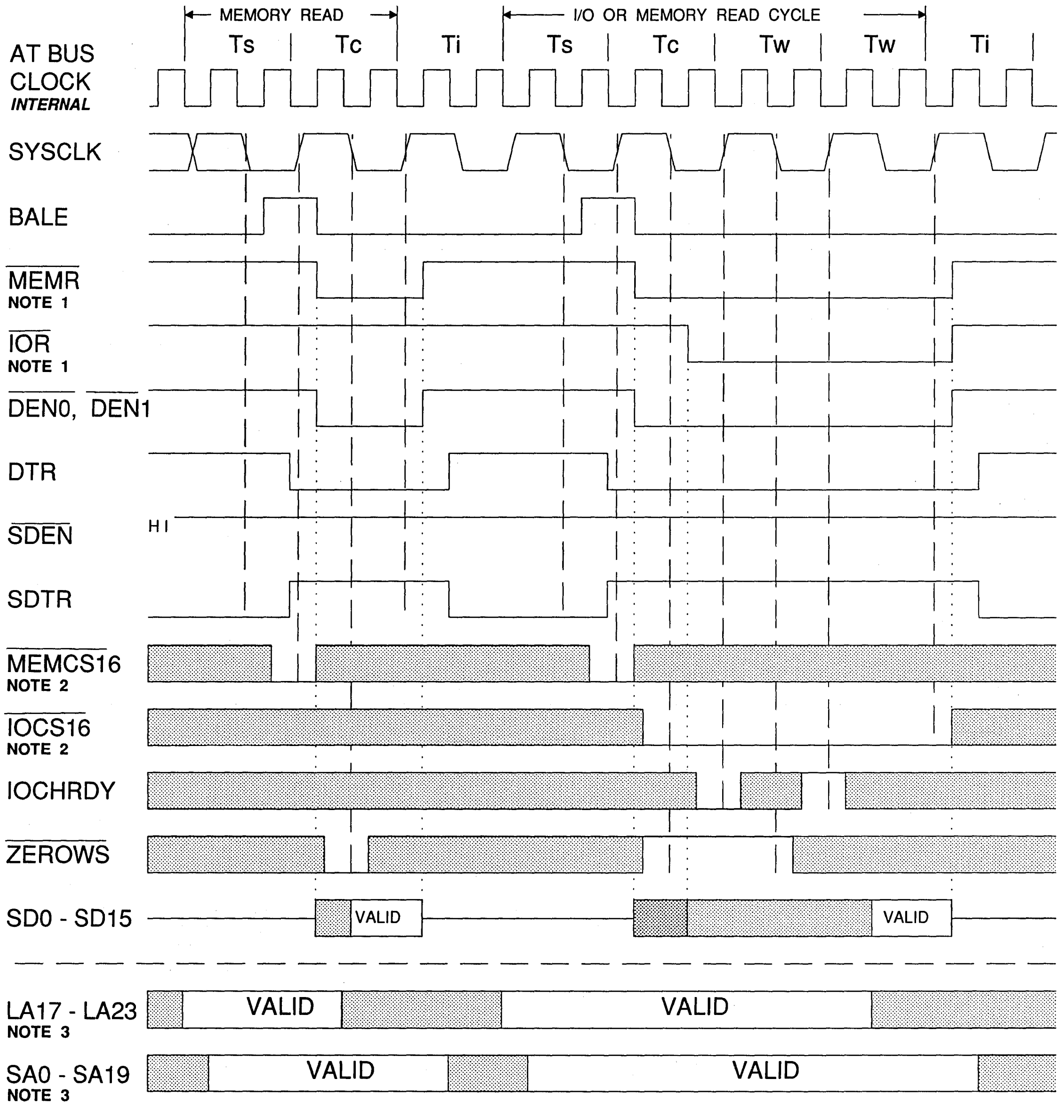
NOTE 5: SDTR remains low and DTR remains high for this cycle.

FIGURE 13-28. AT BUS I/O OR MEMORY WRITE: 8-BIT, WORD TO BYTE CONVERSION, DEFAULT TIMING



NOTE 1: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 13-29. AT BUS I/O OR MEMORY READ: 16-BIT, DEFAULT TIMING

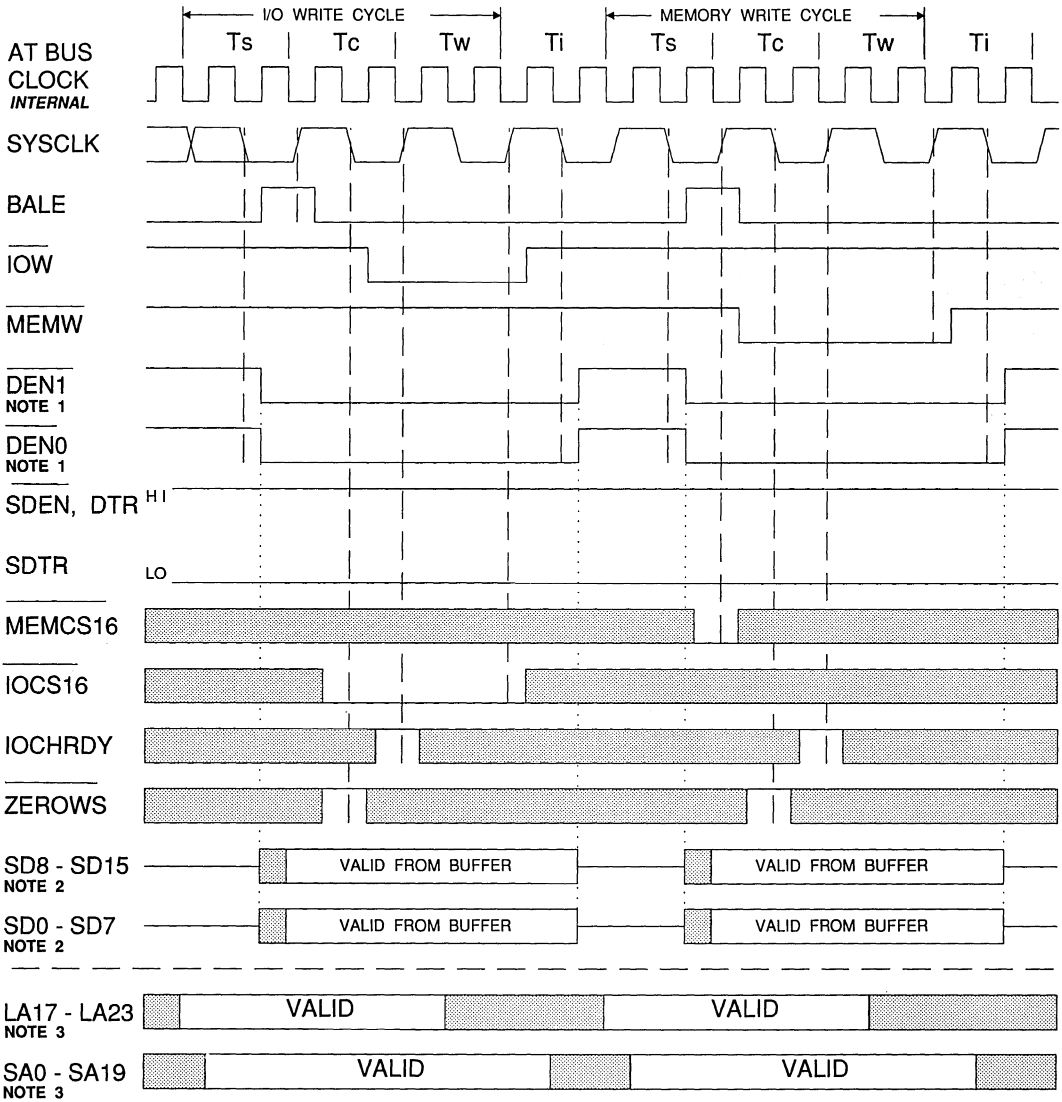


NOTE 1: $\overline{MEMR}$ and $\overline{IOR}$ will not be asserted simultaneously. The first cycle must be to memory, as zero wait state I/O cycles are not supported.

NOTE 2: $\overline{MEMCS16}$ is sampled only during memory cycles. $\overline{IOCS16}$ is sampled only during I/O cycles.

NOTE 3: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 13-30. AT BUS I/O OR MEMORY READ: 16-BIT, 0WS ASSERTED AND EXTRA WAIT STATE ADDED



NOTE 1: $\overline{DEN0}$ is asserted only in cycles where SA0 is low. $\overline{DEN1}$ is asserted only in cycles where $\overline{SBHE}$ is low.

NOTE 2: SD8 - SD15 are driven when $\overline{DEN1}$ is low. SD0 - SD7 are driven when $\overline{DEN0}$ is low. The small period of unknown data is dependent on register settings and may be asynchronous. Minimum valid time is shown for reference.

NOTE 3: Timing for LA17 - 23 and SA0 - 19 is dependent on register settings and may be asynchronous. Minimum valid windows are shown for reference.

FIGURE 13-31. AT BUS I/O OR MEMORY WRITE: 16-BIT, DEFAULT TIMING

13.2.2 Entering the AT Bus

The timing in this section is presented in the following sequence:

80286 CPU

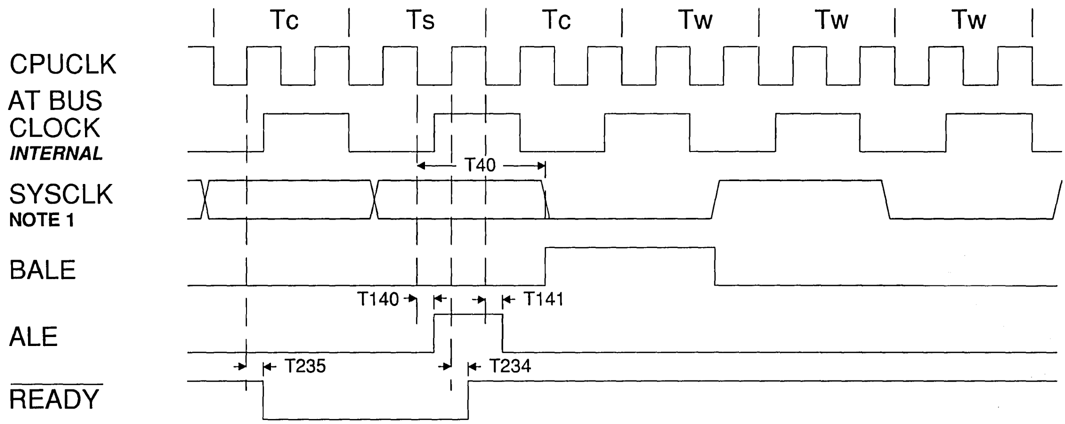
Asysnchronous CPUCLK to SYSCLK
Synchronous CPUCLK to SYSCLK

80386SX CPU

Asysnchronous CPUCLK to SYSCLK
Synchronous CPUCLK to SYSCLK

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T40	CPUCLK fall to SYSCLK fall 80286 CPU mode. CPUCLK rise to SYSCLK fall 80386SX CPU mode.	4		ns	Register 1872H: BRQ_DEL = 01 BUS_MOD = 0X Delay is number given plus (T00 × 0.25)
T41	CPUCLK fall to SYSCLK fall 80286 CPU mode. CPUCLK rise to SYSCLK fall 80386SX CPU mode.	9		ns	Register 1872H: BRQ_DEL = 00 BUS_MOD = 0X Delay is number given plus (T00 × 0.5)
T42	CPUCLK fall to SYSCLK fall 80386SX CPU mode.		29	ns	Register 1872H: BRQ_DEL = 10 BUS_MOD = 11
T43	CPUCLK rise to SYSCLK fall 80386SX CPU mode.		35	ns	Register 1872H: BRQ_DEL = 10 BUS_MOD = 10
T44	CPUCLK rise to SYSCLK fall 80286 CPU mode.		29	ns	Register 1872H: BRQ_DEL = 10 BUS_MOD = 11
T45	CPUCLK fall to SYSCLK fall 80286 CPU mode.		36	ns	Register 1872H: BRQ_DEL = 10 BUS_MOD = 10
T140	CPUCLK fall to ALE rise 80286 CPU mode. CPUCLK rise to ALE rise 80386SX CPU mode.		20	ns	
T141	CPUCLK fall to ALE fall 80286 CPU mode. CPUCLK rise to ALE fall 80386SX CPU mode.		20	ns	
T214	See TABLE 13-6				
T215	See TABLE 13-6				
T234	See TABLE 13-3				
T235	See TABLE 13-3				

TABLE 13-9. ENTERING THE AT BUS

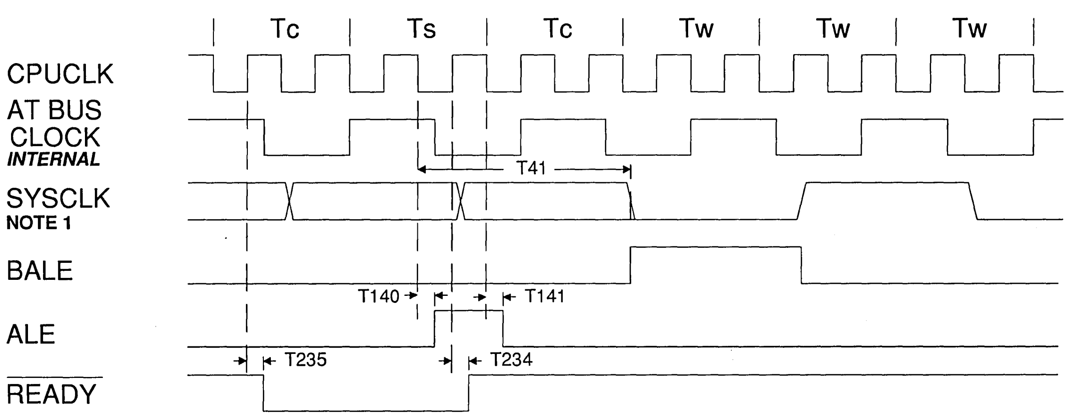


NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

NOTE 2: Register 1872H: BRQ_DEL = 01, BUS_MOD = 00 or 01.

FIGURE 13-32. 80286 CPU - ASYNCHRONOUS CPUCLK TO SYSCLK, BREQ DELAY = 1/2 CLOCK

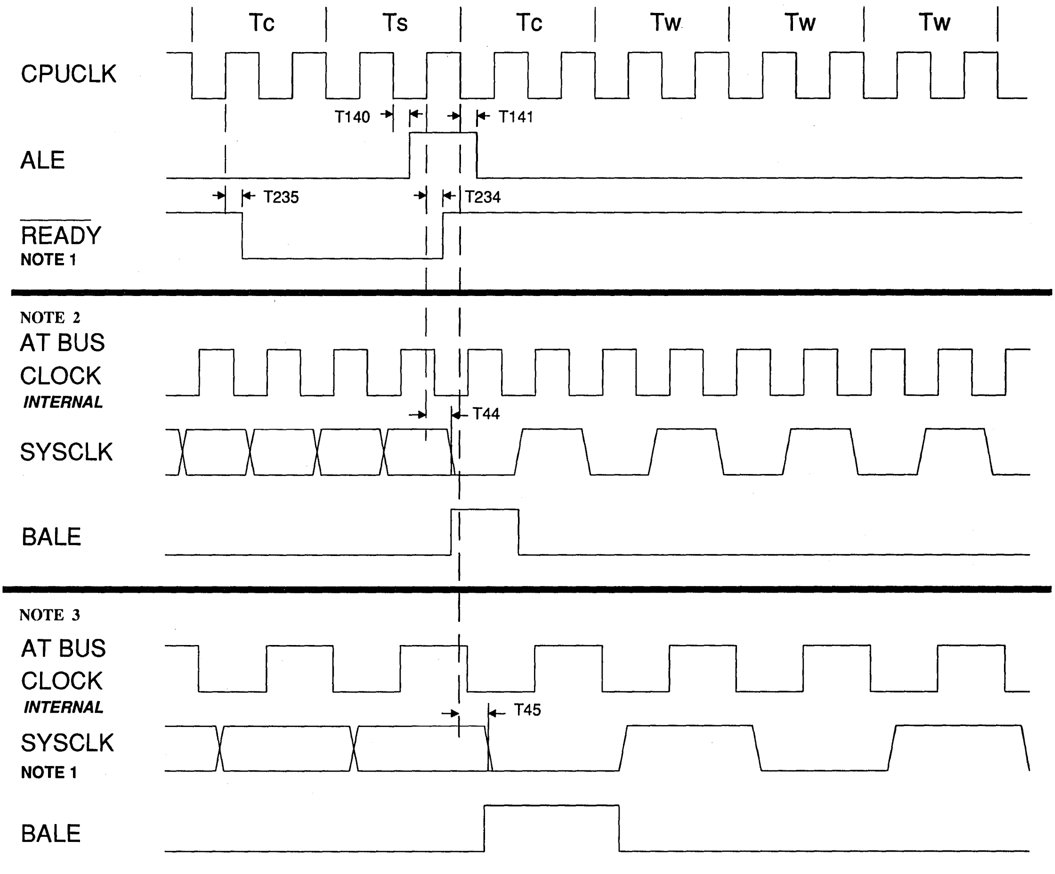
8



NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

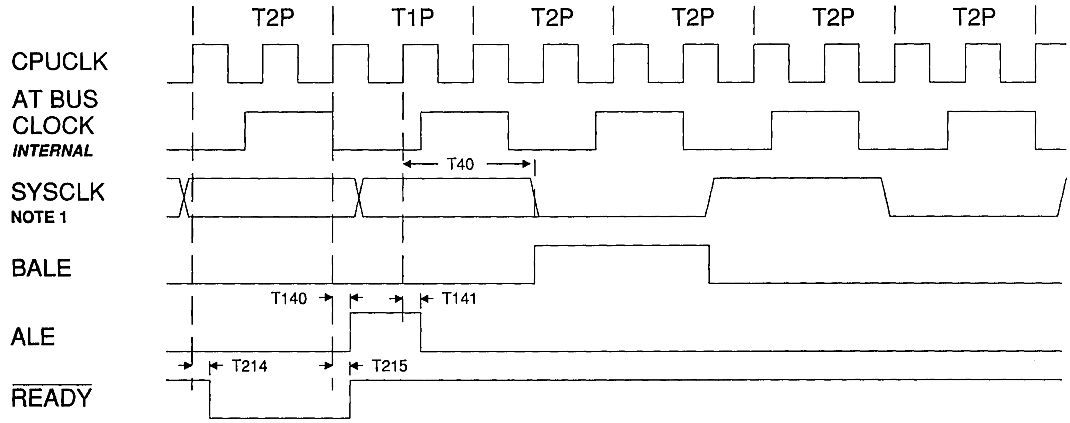
NOTE 2: Register 1872H: BRQ_DEL = 00, BUS_MOD = 00 or 01.

FIGURE 13-33. 80286 CPU - ASYNCHRONOUS CPUCLK TO SYSCLK, BREQ DELAY = 1 CLOCK



NOTE 1: $\overline{\text{READY}}$ timing is shown for when the previous cycle was not an AT bus cycle.
NOTE 2: AT bus clock = CPUCLK ÷ 1. Register 1872H: BRQ_DEL = 10, BUS_MOD = 11.
NOTE 3: AT bus clock = CPUCLK ÷ 2. Register 1872H: BRQ_DEL = 10, BUS_MOD = 10.

FIGURE 13-34. 80286 CPU - SYCNHRONOUS CPUCLK TO SYSCLK

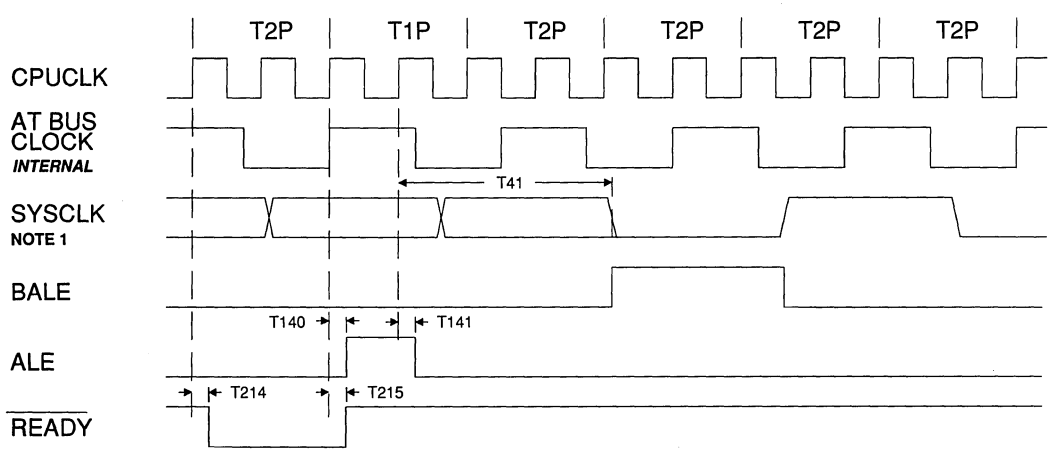


NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

NOTE 2: Register 1872H: BRQ_DEL = 01, BUS_MOD = 00 or 01.

FIGURE 13-35. 80386SX CPU - BREQ DELAY = 1/2 CLOCK

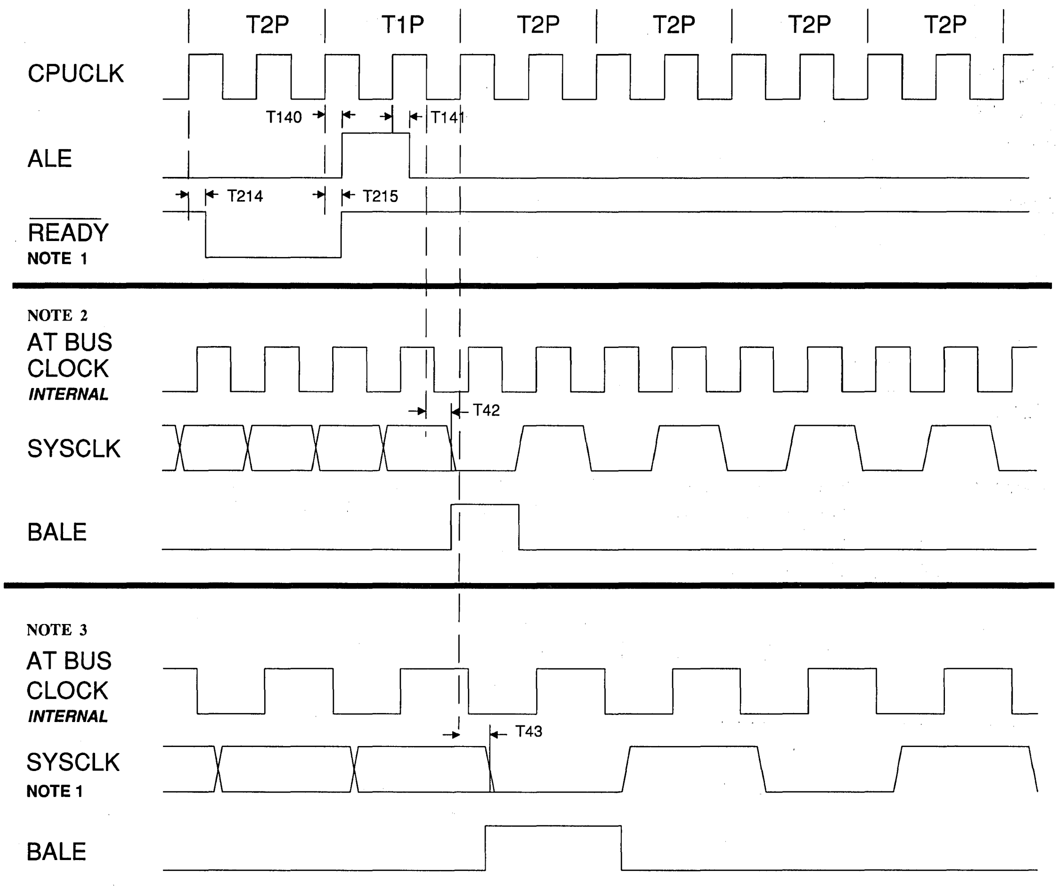
8



NOTE 1: SYSCLK is asynchronous to CPUCLK. The minimum delay between CPUCLK and SYSCLK for an AT bus cycle to be started is shown here. Reducing the delay further would cause the AT cycle to start 1/2 SYSCLK period later.

NOTE 2: Register 1872H: BRQ_DEL = 00, BUS_MOD = 00 or 01.

FIGURE 13-36. 80386SX - BREQ DELAY = 1 CLOCK



NOTE 1: If this AT bus cycle is immediatly preceded by another bus cycle and the BUS_MOD field in register 1872 = 11, READY will fall 1 CPUCLK later than shown.

NOTE 2: AT bus clock = CPUCLK ÷ 1. Register 1872H: BRQ_DEL = 10, BUS_MOD = 11.

NOTE 3: AT bus clock = CPUCLK ÷ 2. Register 1872H: BRQ_DEL = 10, BUS_MOD = 10.

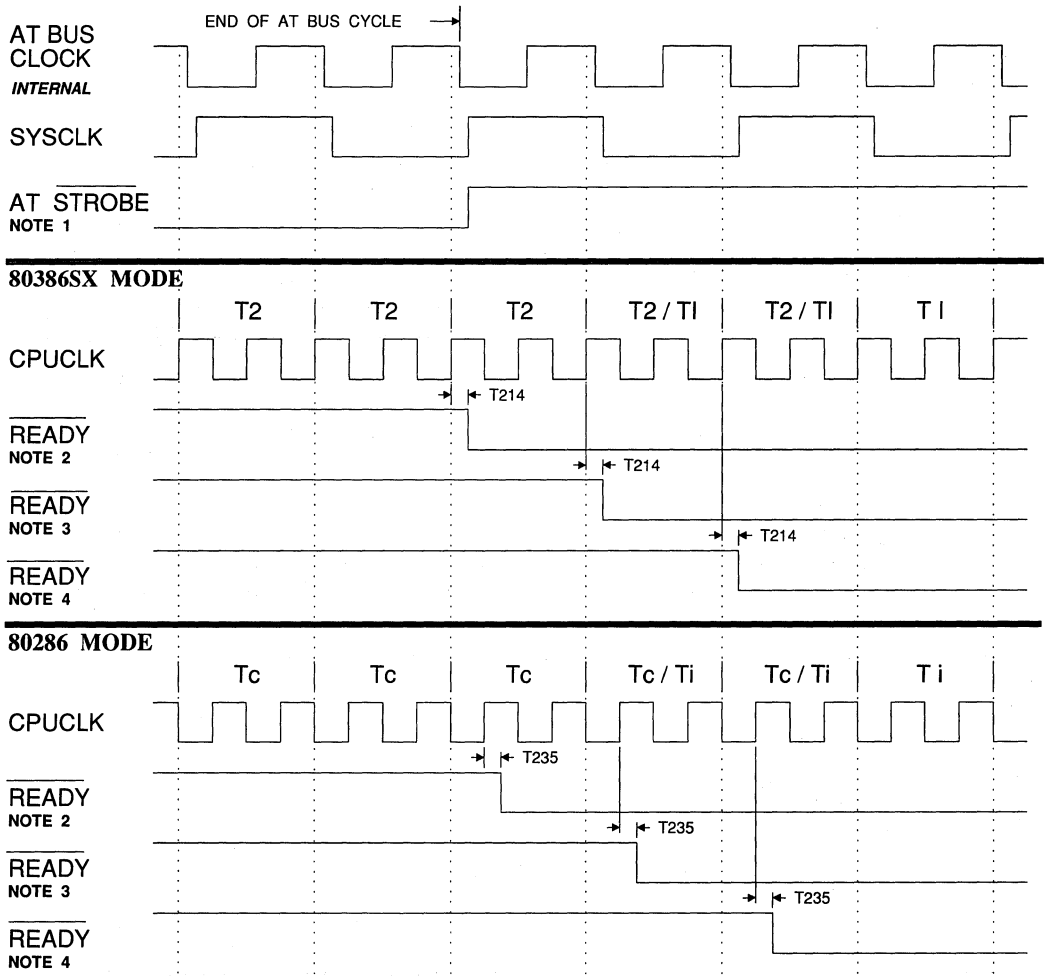
FIGURE 13-37. 80386SX CPU - SYCNHRONOUS CPUCLK TO SYSCLK

13.2.3 Exiting The AT Bus

Exiting a synchronous AT bus is covered first, followed by the asynchronous bus.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T46	SYSCLK fall to CPUCLK	-5		ns	Register 1872H: BAK_DEL = 10 BUS_MOD = 0X
T47	SYSCLK fall to CPUCLK	-15		ns	Register 1872H: BAK_DEL = 01 BUS_MOD = 0X Delay is number given plus (T00 × 0.25)
T48	SYSCLK rise to CPUCLK	-10		ns	Register 1872H: BAK_DEL = 00 BUS_MOD = 0X
T49	SYSCLK rise to CPUCLK	-15		ns	Register 1872H: BAK_DEL = 11 BUS_MOD = 0X Delay is number given plus (T00 × 0.25)
T144	CPUCLK fall to $\overline{\text{READY}}$ fall, 80286 CPU mode.		24	ns	Register 1872H: BUS_MOD = 11 AT cycles only
T145	CPUCLK fall to $\overline{\text{READY}}$ rise, 80286 CPU mode.		26	ns	Register 1872H: BUS_MOD = 11 AT cycles only
T214	See TABLE 13-6				
T215	See TABLE 13-6				
T234	See TABLE 13-3				
T235	See TABLE 13-3				

TABLE 13-10. EXITING THE AT BUS



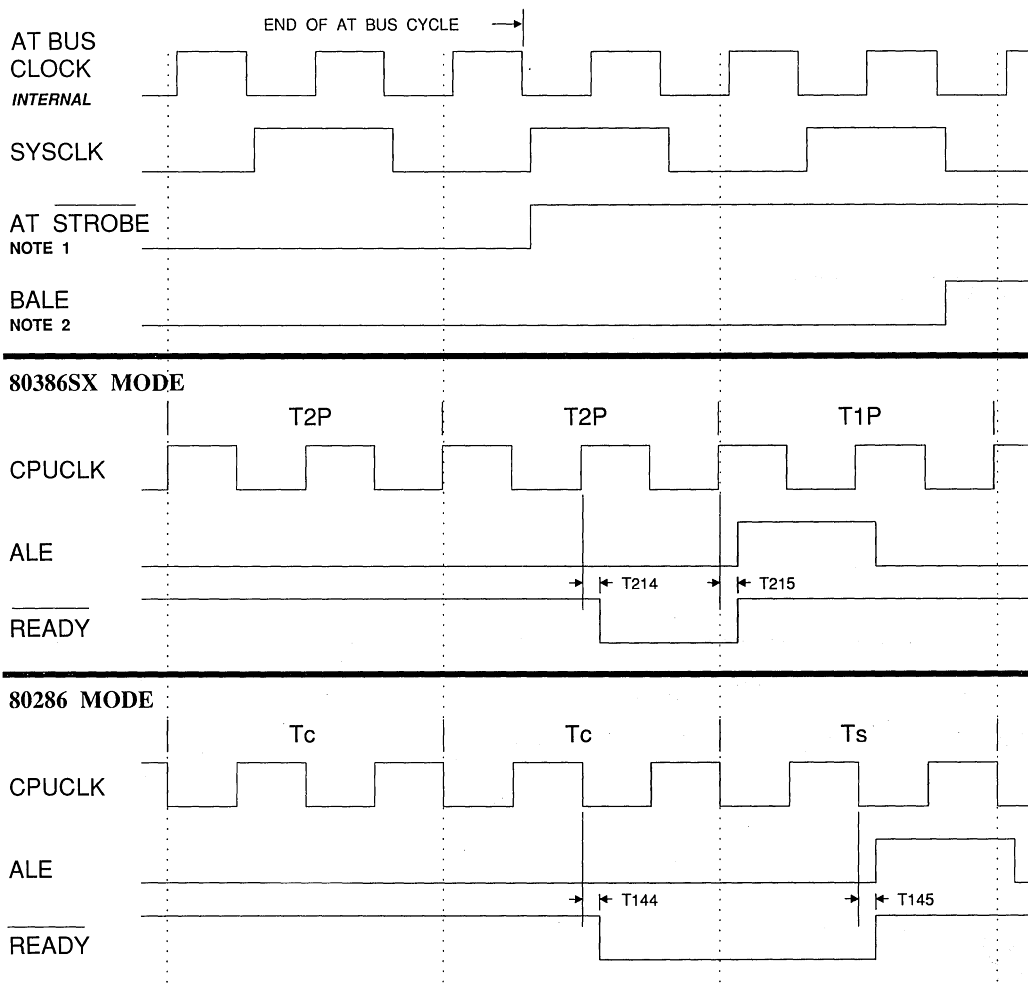
NOTE 1: AT STROBE is either MEMR, MEMW, IOR or IOW.

NOTE 2: Register 1872H: BUS_MOD = 10, BAK_DEL = 10 (-1 AT bus clock).

NOTE 3: Register 1872H: BUS_MOD = 10, BAK_DEL = 01 or 00 (-0.5 AT bus clock or no delay).

NOTE 4: Register 1872H: BUS_MOD = 10, BAK_DEL = 11 (+0.5 AT bus clock).

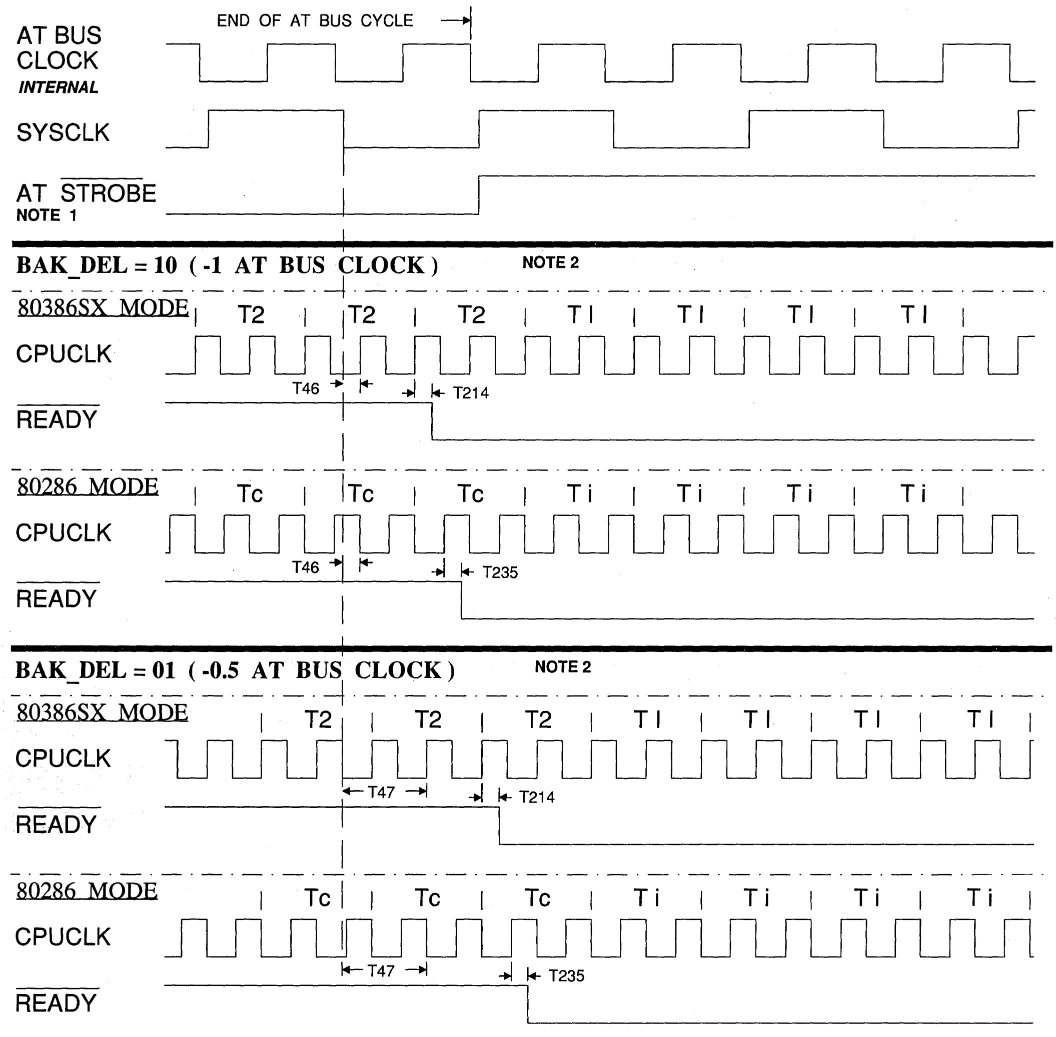
FIGURE 13-38. SYNCHRONOUS AT BUS CYCLE COMPLETION, AT BUS CLOCK = CPUCLK ÷ 2



NOTE 1: AT STROBE is either MEMR, MEMW IOR or IOW.

NOTE 2: Register 1872H: BRQ_DEL = 10, BUS_MOD = 11, BAK_DEL = XX.

FIGURE 13-39. SYNCHRONOUS AT BUS CYCLE COMPLETION, AT BUS CLOCK = CPUCLK ÷ 1

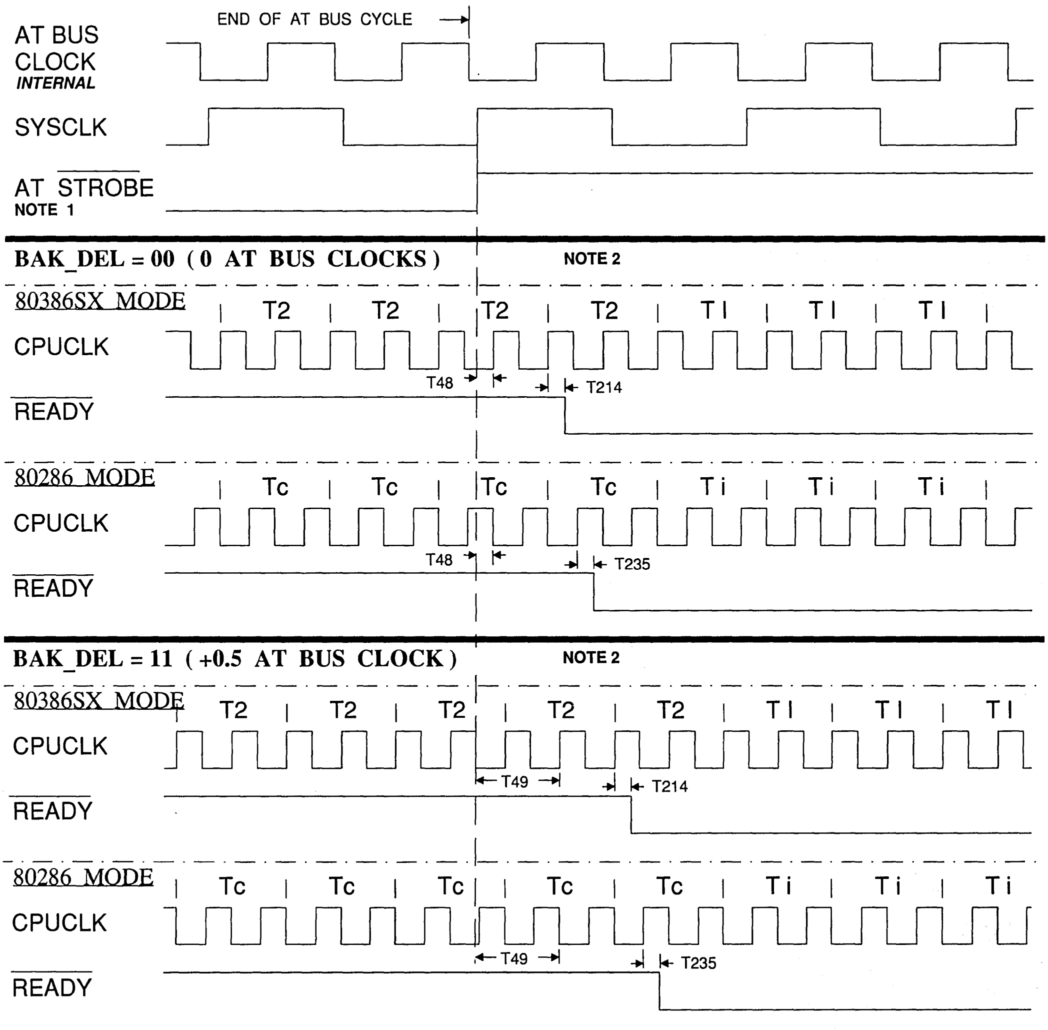


NOTE 1: AT STROBE is either MEMR, MEMW, IOR or IOW.

NOTE 2: Register 1872H: BUS_MOD = 00 or 01 (asynchronous AT bus), BAK_DEL set as indicated.

NOTE 3: SYSCLK is asynchronous to CPUCLK. The minimum delay between SYSCLK and CPUCLK for READY to be asserted is shown here. Reducing the delay further would cause READY to be asserted one CPU "T" state later.

FIGURE 13-40. ASYNCHRONOUS AT BUS CYCLE COMPLETION, BAK_DEL = -1 OR -0.5 AT BUS CLOCKS



NOTE 1: AT STROBE is either MEMR, MEMW, IOR or IOW.

NOTE 2: Register 1872H: BUS_MOD = 00 or 01 (asynchronous AT bus), BAK_DEL set as indicated.

NOTE 3: SYSCLK is asynchronous to CPUCLK. The minimum delay between SYSCLK and CPUCLK for READY to be asserted is shown here. Reducing the delay further would cause READY to be asserted one CPU "T" state later.

FIGURE 13-41. ASYNCHRONOUS AT BUS CYCLE COMPLETION, BAK_DEL = 0 OR +0.5 AT BUS CLOCKS

8

13.2.4 DMA Cycles

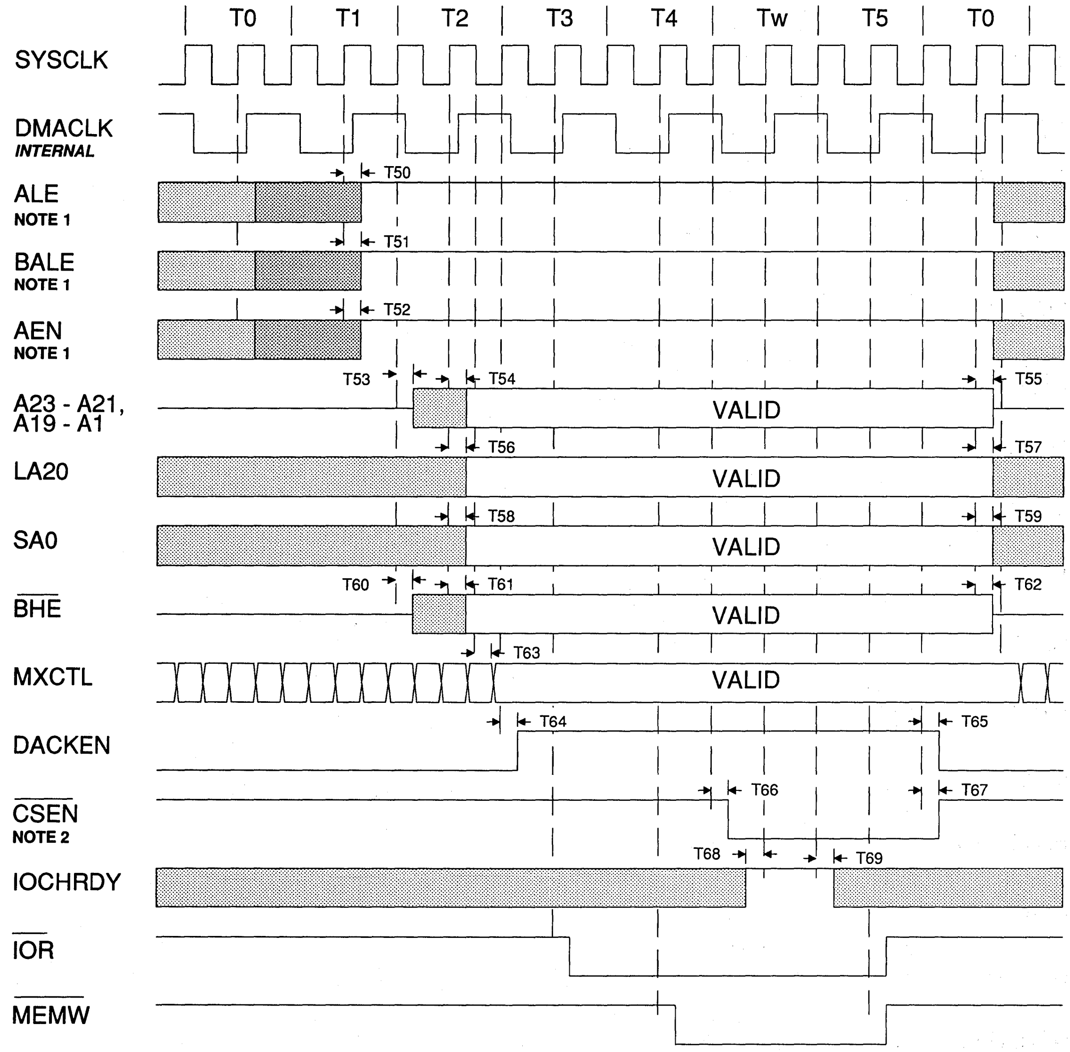
Basic default timing is covered first, followed by 8-bit I/O to onboard memory, then onboard memory to 8-bit I/O.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T50	SYSCLK rise to ALE valid high		15	ns	
T51	SYSCLK rise to BALE valid high		15	ns	
T52	SYSCLK rise to AEN valid high		15	ns	
T53	SYSCLK rise to Address driven	0		ns	
T54	SYSCLK rise to Address valid		60	ns	
T55	Address hold from SYSCLK rise	0		ns	
T56	SYSCLK rise to LA20 valid		49	ns	
T57	LA20 hold from SYSCLK rise	0		ns	
T58	SYSCLK rise to SA0 valid		40	ns	
T59	SA0 hold from SYSCLK rise	0		ns	
T60	SYSCLK rise to $\overline{BHE}$ driven	0		ns	
T61	SYSCLK rise to $\overline{BHE}$ valid		36	ns	
T62	$\overline{BHE}$ hold from SYSCLK rise	0		ns	
T63	SYSCLK fall to MXCTL valid		2	ns	
T64	SYSCLK rise to DACKEN rise		28	ns	
T65	SYSCLK rise to DACKEN fall		31	ns	
T66	SYSCLK rise to $\overline{CSEN}$ fall		32	ns	
T67	SYSCLK rise to $\overline{CSEN}$ rise		33	ns	
T68	IOCHRDY setup to SYSCLK rise	12		ns	
T69	IOCHRDY hold from SYSCLK rise	0		ns	
T70	SYSCLK rise to $\overline{IOR}$ fall		28	ns	
T71	SYSCLK rise to $\overline{IOR}$ rise		35	ns	
T72	SYSCLK rise to $\overline{MEMW}$ fall		47	ns	
T73	SYSCLK rise to $\overline{MEMW}$ rise		35	ns	
T74	SYSCLK rise to $\overline{DEN1}$ fall		32	ns	I/O to memory
T75	SYSCLK rise to $\overline{DEN1}$ rise		42	ns	I/O to memory
T76	SYSCLK rise to $\overline{DEN0}$ fall		32	ns	I/O to memory
T77	SYSCLK rise to $\overline{DEN0}$ rise		42	ns	I/O to memory
T78	SYSCLK rise to $\overline{SDEN}$ fall		21	ns	
T79	SYSCLK rise to $\overline{SDEN}$ rise		37	ns	I/O to memory

TABLE 13-11. DMA CYCLES

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T80	SYSCLK rise to SDTR rise		30	ns	
T81	SYSCLK rise to SDTR fall		20	ns	
T82	SYSCLK rise to $\overline{\text{IOW}}$ fall		53	ns	
T83	SYSCLK rise to $\overline{\text{IOW}}$ rise		37	ns	
T84	SYSCLK rise to $\overline{\text{MEMR}}$ fall		17	ns	
T85	SYSCLK rise to $\overline{\text{MEMR}}$ rise		38	ns	
T86	SYSCLK rise to $\overline{\text{DEN1}}$ fall		22	ns	Memory to I/O
T87	SYSCLK rise to $\overline{\text{DEN1}}$ rise		116	ns	Memory to I/O
T88	SYSCLK rise to $\overline{\text{DEN0}}$ fall		22	ns	Memory to I/O
T89	SYSCLK rise to $\overline{\text{DEN0}}$ rise		116	ns	Memory to I/O
T90	SYSCLK rise to $\overline{\text{SDEN}}$ rise		116	ns	Memory to I/O
T91	SYSCLK rise to DTR rise		31	ns	
T92	SYSCLK rise to DTR fall		22	ns	
T100	$\overline{\text{MEMW}}$ fall to $\overline{\text{RASn}}$ fall		27	ns	
T101	$\overline{\text{MEMW}}$ rise to $\overline{\text{RASn}}$ rise		29	ns	
T102	$\overline{\text{MEMW}}$ fall to $\overline{\text{CASn}}$ fall		108	ns	
T103	$\overline{\text{MEMW}}$ rise to $\overline{\text{CASn}}$ rise		30	ns	
T105	$\overline{\text{MEMW}}$ fall to RA10 - RA0 valid		100	ns	
T107	$\overline{\text{MEMW}}$ fall to W/$\overline{\text{R}}$ high		29	ns	
T108	$\overline{\text{MEMW}}$ rise to W/$\overline{\text{R}}$ low	10		ns	
T120	$\overline{\text{MEMR}}$ fall to $\overline{\text{RASn}}$ fall		28	ns	
T121	$\overline{\text{MEMR}}$ rise to $\overline{\text{RAS}}$ rise		29	ns	
T122	$\overline{\text{MEMR}}$ fall to $\overline{\text{CASn}}$ fall		110	ns	
T123	$\overline{\text{MEMR}}$ rise to $\overline{\text{CAS}}$ rise		31	ns	
T125	$\overline{\text{MEMR}}$ fall to RA10 - RA0 valid		100	ns	
T126	$\overline{\text{MEMR}}$ fall to DPH, DPL float		25		
T127	$\overline{\text{MEMR}}$ rise to DPH, DPL driven	35			
T303	D15 - D0 valid to DPH, DPL valid		27	ns	
T305	D15 - D0 setup to $\overline{\text{MEMR}}$ rise	18		ns	
T306	DPH, DPL setup to $\overline{\text{MEMR}}$ rise	10		ns	

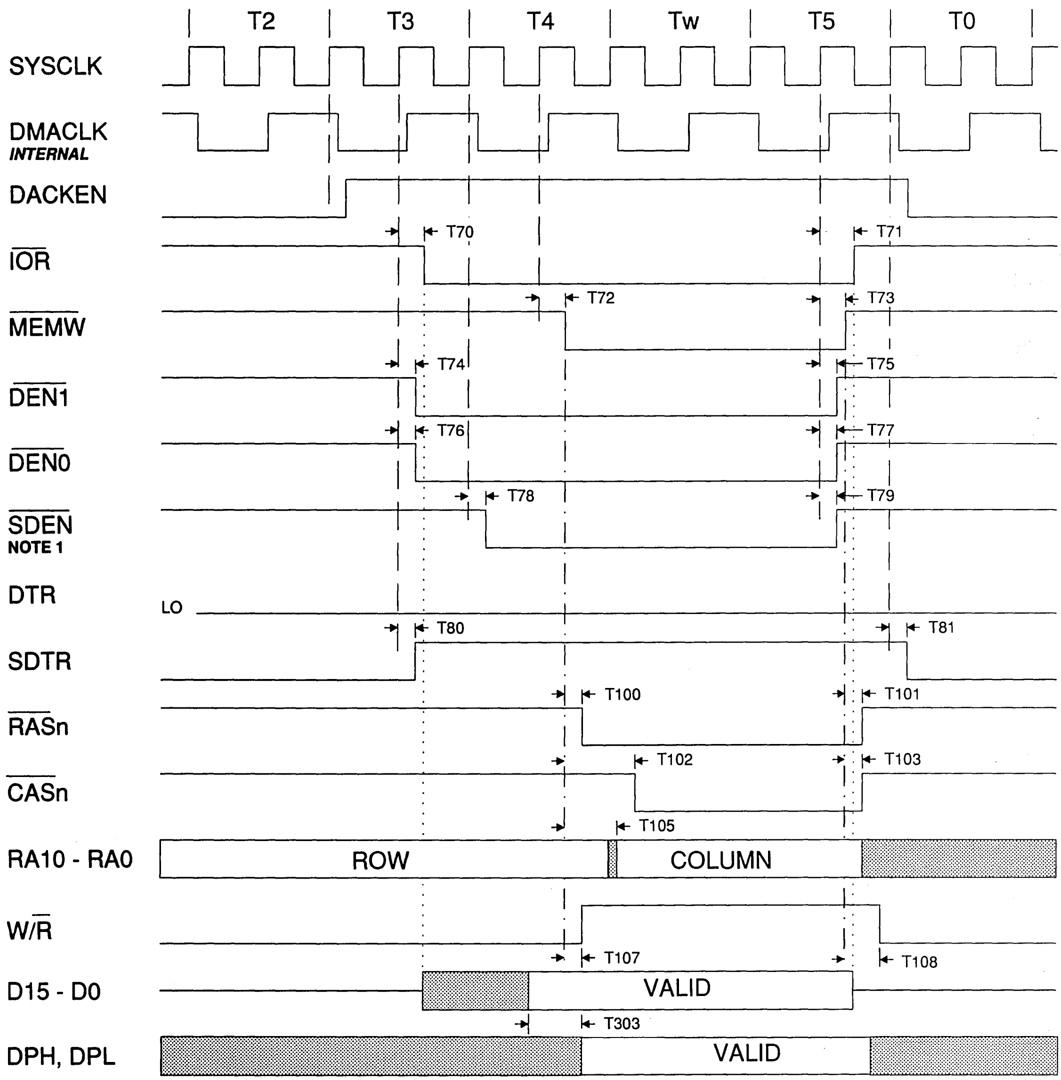
TABLE 13-11. DMA CYCLES cont.



NOTE 1: ALE, BALE and AEN may be asynchronous. Minimum valid time is shown. DMA channels 0, 1, 2, and 3 will have two additional SYSCLK periods of valid time as shown by the alternate shaded region.

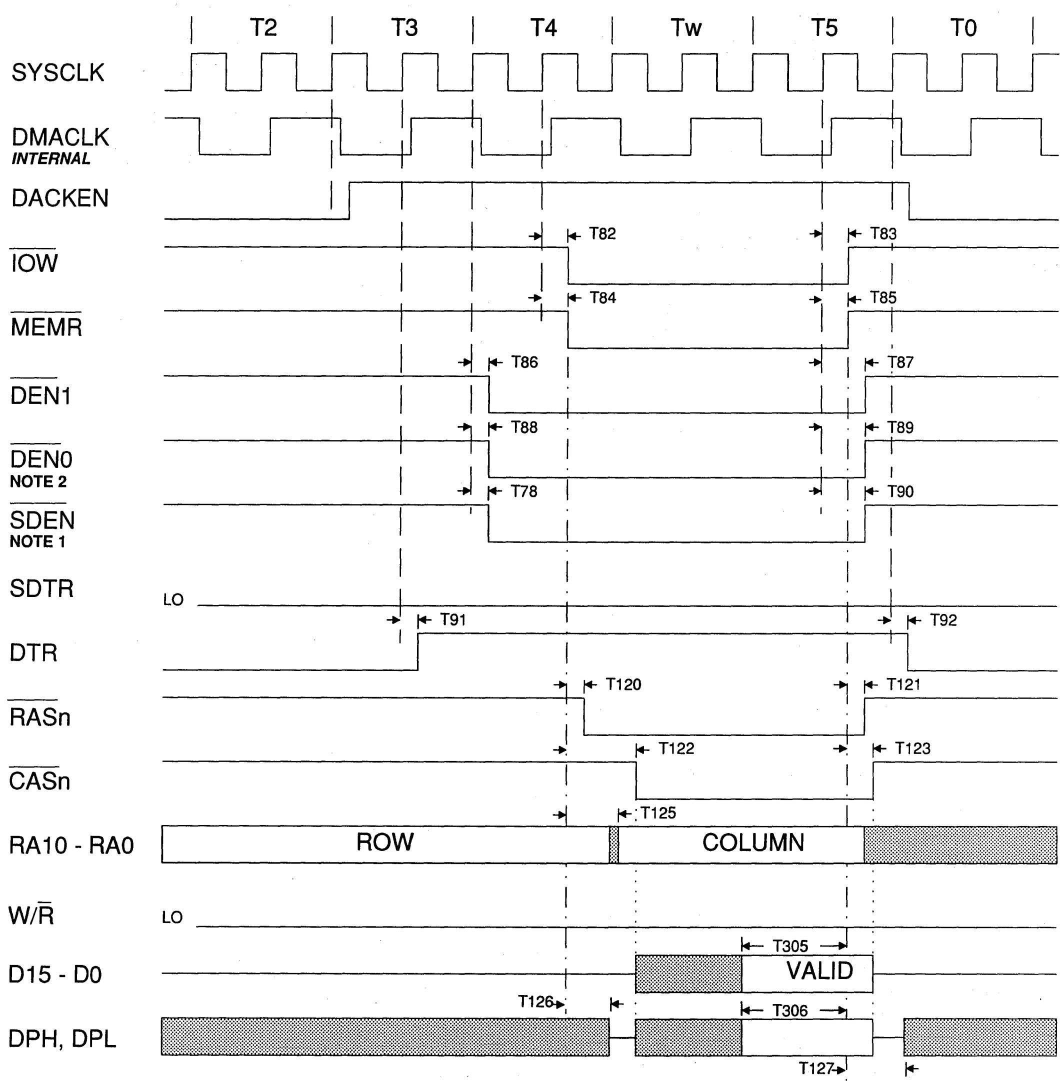
NOTE 2: $\overline{CSEN}$ is used to generate the terminal count signal and pulses low only during the last transfer in a block.

FIGURE 13-42. BASIC DMA CYCLE, DEFAULT TIMING



NOTE 1: SDEN is asserted only in cycles with an odd numbered address.

FIGURE 13-43. DMA CYCLE, 8-BIT I/O TO ON-BOARD MEMORY



NOTE 1: SDEN is asserted only in cycles with an odd numbered address.
NOTE 2: DEN0 is asserted only in cycles with an even numbered address.

FIGURE 13-44. DMA CYCLE, ON-BOARD MEMORY TO 8-BIT I/O

13.2.5 AT Bus Master

The AT bus master timing is covered in the following sequence:

- Bus acquisition and release
- Writing to the onboard memory
- Reading from the onboard memory

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T50	SYSCLK rise to ALE valid high		15	ns	
T51	SYSCLK rise to BALE valid high		15	ns	
T52	SYSCLK rise to AEN valid high		15	ns	
T53	SYSCLK rise to Address driven	0		ns	
T55	Address hold from SYSCLK rise	0		ns	
T60	SYSCLK rise to $\overline{\text{BHE}}$ driven	0		ns	
T61	SYSCLK rise to $\overline{\text{BHE}}$ valid		36	ns	
T62	$\overline{\text{BHE}}$ hold from SYSCLK rise	0		ns	
T63	SYSCLK fall to MXCTL valid		2	ns	
T64	SYSCLK rise to DACKEN rise		28	ns	
T65	SYSCLK rise to DACKEN fall		31	ns	
T150	$\overline{\text{MASTER}}$ fall to AEN fall		30	ns	
T151	$\overline{\text{MASTER}}$ rise to AEN rise		30	ns	
T152	$\overline{\text{MASTER}}$ fall to A23 - A21, A19 - A1 float		30	ns	
T153	$\overline{\text{MASTER}}$ rise to A23 - A21, A19 - A1 driven	15		ns	
T154	$\overline{\text{MASTER}}$ fall to LA20 float		23	ns	
T155	$\overline{\text{MASTER}}$ rise to LA20 driven	10		ns	
T156	$\overline{\text{MASTER}}$ fall to SA0 float		24	ns	
T157	$\overline{\text{MASTER}}$ rise to SA0 driven	10		ns	
T158	$\overline{\text{MASTER}}$ fall to $\overline{\text{BHE}}$ float		30	ns	
T159	$\overline{\text{MASTER}}$ rise to $\overline{\text{BHE}}$ driven	10		ns	
T160	$\overline{\text{MASTER}}$ fall to $\overline{\text{CSEN}}$ fall		32	ns	
T161	$\overline{\text{MASTER}}$ rise to $\overline{\text{CSEN}}$ rise		35	ns	
T162	$\overline{\text{MASTER}}$ fall to $\overline{\text{MEMR}}$ float		24	ns	
T163	$\overline{\text{MASTER}}$ rise to $\overline{\text{MEMR}}$ driven	10		ns	
T164	$\overline{\text{MASTER}}$ fall to MEMW, $\overline{\text{IOR}}$, $\overline{\text{IOW}}$, float		23	ns	
T165	$\overline{\text{MASTER}}$ rise to $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$, $\overline{\text{IOW}}$ driven	10		ns	

TABLE 13-12. AT BUS MASTER CYCLE

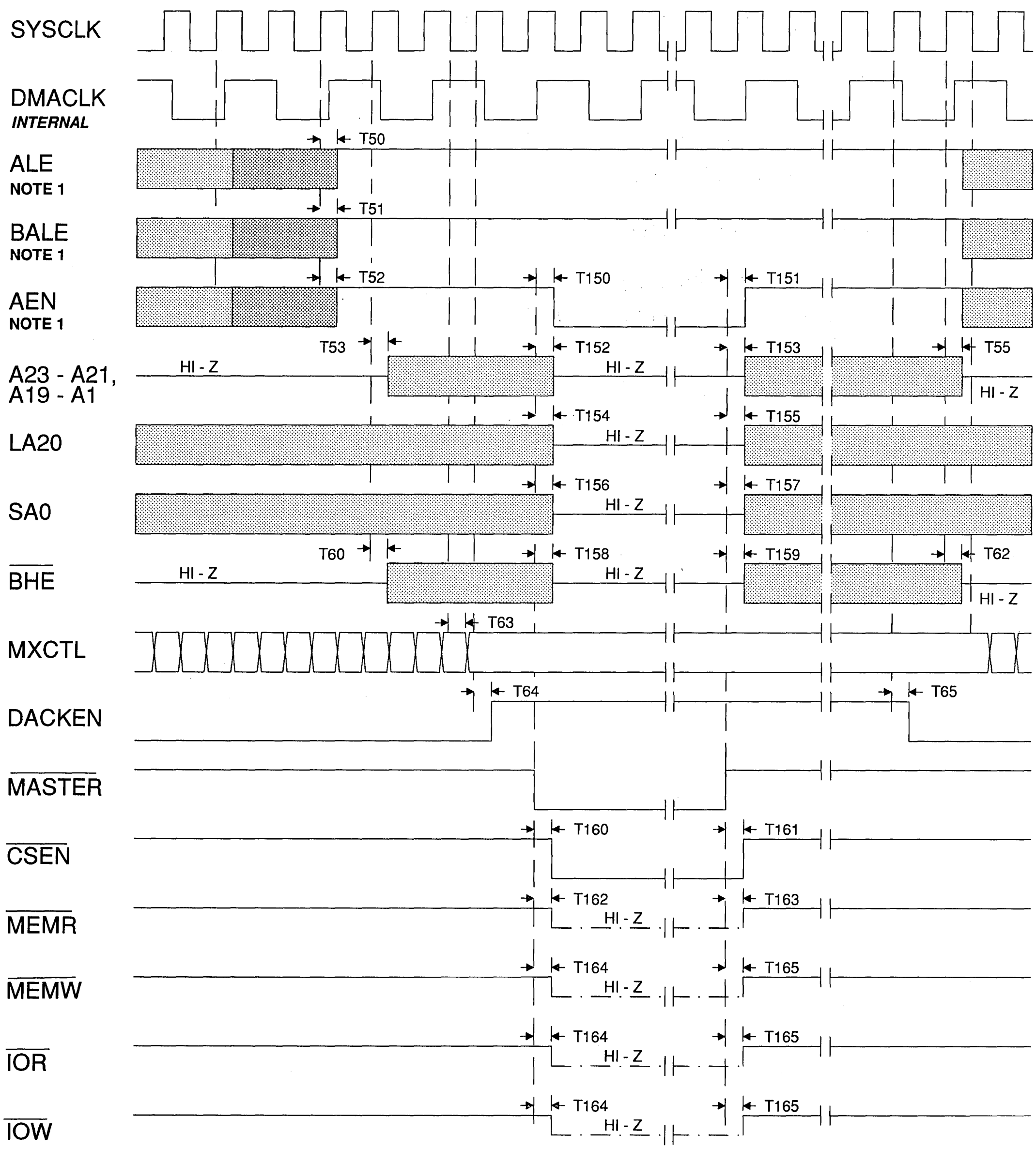
8

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T166	A23 - A21, A19 - A1 setup to MEMR, MEMW	45		ns	
T167	LA20 setup to MEMR, MEMW	50		ns	
T168	BHE setup to MEMR, MEMW	0		ns	
T169	SA0 setup to MEMR, MEMW	0		ns	
T170	A23 - A21, A19 - A1 hold from MEMR, MEMW	15		ns	
T171	LA20 hold from MEMR, MEMW	15		ns	
T172	BHE hold from MEMR, MEMW	15		ns	
T173	SA0 hold from MEMR, MEMW	15		ns	
T174	SA0 in to A0 out delay		45	ns	
T175	MEMW fall to DEN1 fall		30	ns	
T176	MEMW fall to DEN0 fall		30	ns	
T177	MEMW rise to DEN1 rise		83	ns	
T178	MEMW rise to DEN0 rise		83	ns	
T179	MEMR fall to DEN1 fall		85	ns	
T180	MEMR fall to DEN0 fall		85	ns	
T181	MEMR rise to DEN1 rise		32	ns	
T182	MEMR rise to DEN0 rise		32	ns	
T183	MEMR fall to DTR rise		29	ns	
T184	MEMR rise to DTR fall		82	ns	
T190	MEMR, MEMW fall to RASn fall		83	ns	
T191	MEMR, MEMW rise to RASn rise		33	ns	
T192	MEMR, MEMW fall to CASn fall		126	ns	
T193	MEMR, MEMW rise to CASn rise		33	ns	
T194	MEMR, MEMW fall to RA10 - RA0 column address valid		120	ns	
T196	MEMR, MEMW fall to RA10 - RA0 row address valid		42	ns	
T197	RA10 - RA0 column address hold from MEMR, MEMW rise	5		ns	

TABLE 13-12. AT BUS MASTER CYCLE cont.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T300	$\overline{\text{MEMW}}$ fall to W/$\overline{\text{R}}$ rise		33	ns	
T301	$\overline{\text{MEMW}}$ rise to W/$\overline{\text{R}}$ fall	10		ns	
T302	$\overline{\text{MEMW}}$ fall to DPH, DPL valid		32	ns	
T303	D15 - D0 valid to DPH, DPL valid		27	ns	
T304	DPH, DPL hold from $\overline{\text{MEMW}}$ rise	5		ns	
T305	D15 - D0 setup to $\overline{\text{MEMR}}$ rise	18		ns	
T306	DPH, DPL setup to $\overline{\text{MEMR}}$ rise	10		ns	
T307	$\overline{\text{MEMR}}$ fall to DPH, DPL float		35	ns	
T308	$\overline{\text{MEMR}}$ rise to DPH, DPL driven	58		ns	

TABLE 13-12. AT BUS MASTER CYCLE cont.



NOTE 1: The shaded regions of ALE, BALE and AEN show a possible asynchronous relarionship. Minimum valid time is shown. DMA channels 0, 1, 2 and 3 will have two additional SYSCLK periods of valid HI time as shown by the alternate shading.

FIGURE 13-45. AT BUS MASTER, BUS ACQUISITION/RELEASE

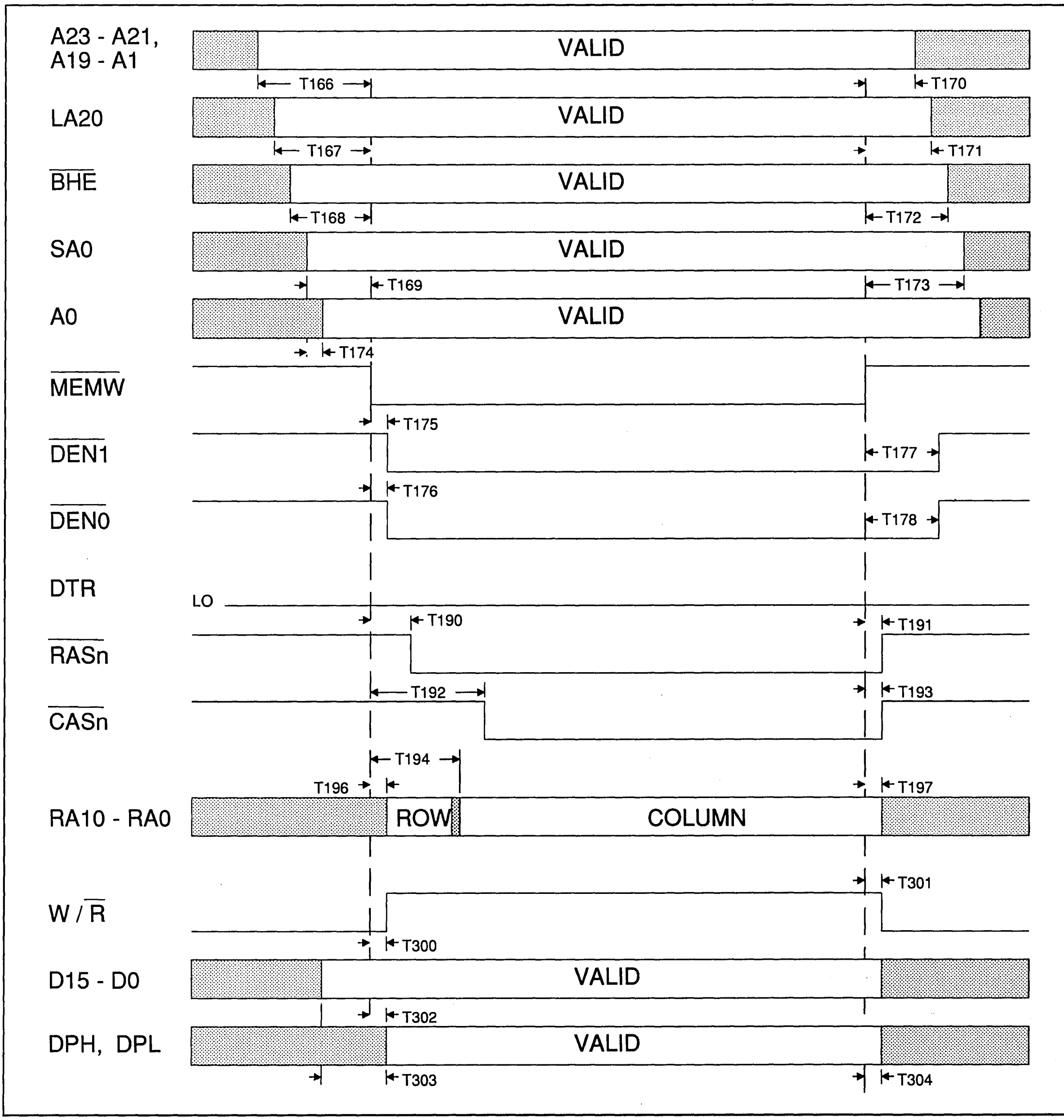


FIGURE 13-46. AT BUS MASTER, WRITE TO ON-BOARD MEMORY

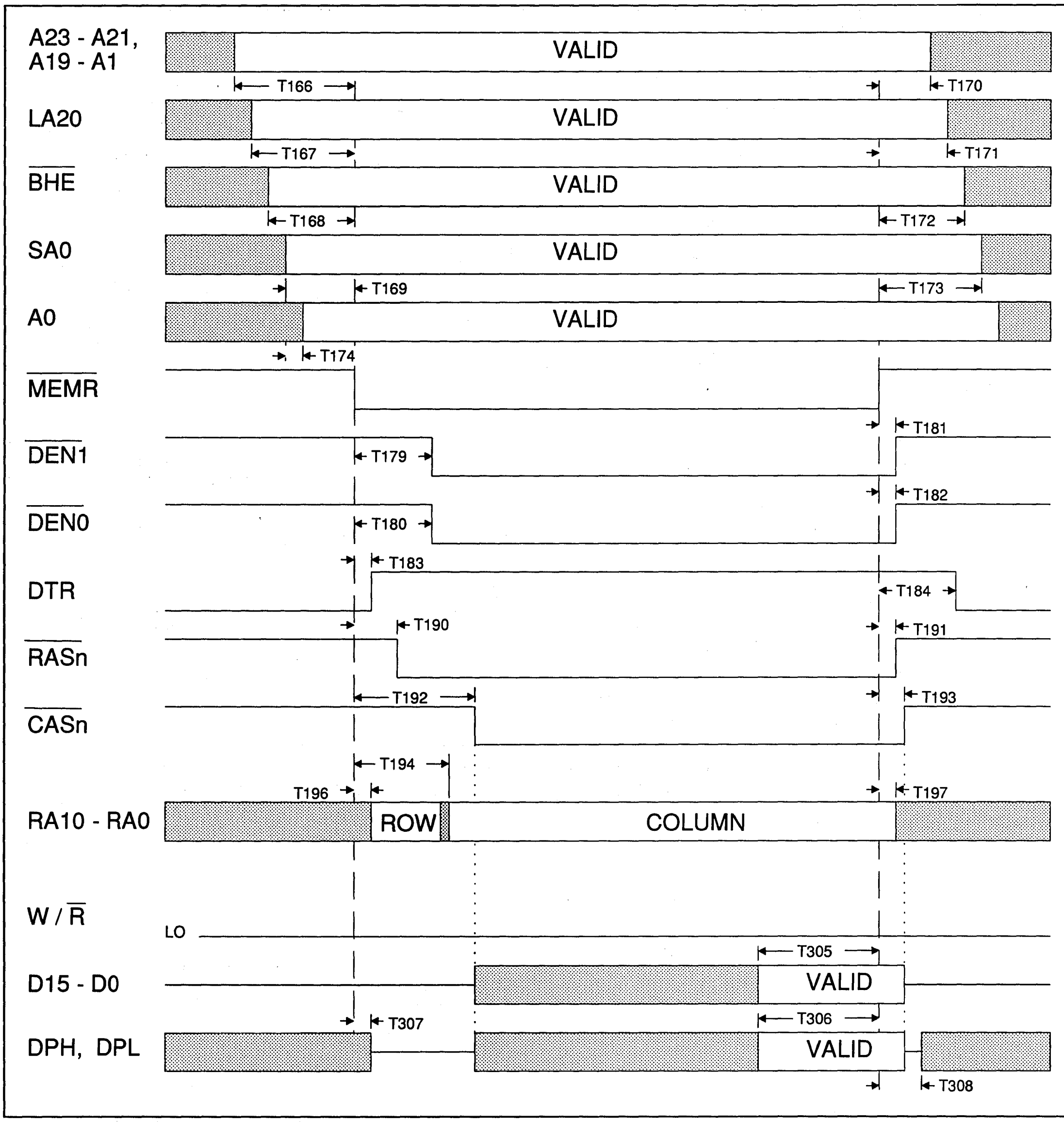


FIGURE 13-47. AT BUS MASTER, READ FROM ON-BOARD MEMORY

13.2.6 AT Bus Refresh

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T320	$\overline{\text{REFRESH}}$ low before SYSCLK rise	4		ns	$\overline{\text{REFRESH}}$ setup is number given plus (T00 × 0.25)
T321	SYSCLK fall to $\overline{\text{REFRESH}}$ rise		16	ns	
T325	SYSCLK rise to A23 - A21, A19 - A16 and A7 - A1 valid		35	ns	
T326	SYSCLK fall to A23 - A21, A19 - A16 and A7 - A1 invalid	2		ns	
T327	SYSCLK rise to A20, A15 - A8 valid		45	ns	
T328	SYSCLK fall to A20, A15 - A8 invalid	2		ns	
T329	SYSCLK rise to LA20 valid		30	ns	
T330	SYSCLK fall to LA20 invalid	2		ns	
T331	SYSCLK rise to SA0 valid		30	ns	
T332	SYSCLK fall to SA0 invalid	2		ns	
T333	SYSCLK rise to $\overline{\text{MEMR}}$ low		8	ns	
T334	SYSCLK rise to $\overline{\text{MEMR}}$ high		7	ns	
T335	IOCHRDY setup to SYSCLK rise	23		ns	
T336	IOCHRDY hold time from SYSCLK rise	0		ns	

TABLE 13-13. AT BUS REFRESH CYCLE, DEFAULT TIMING

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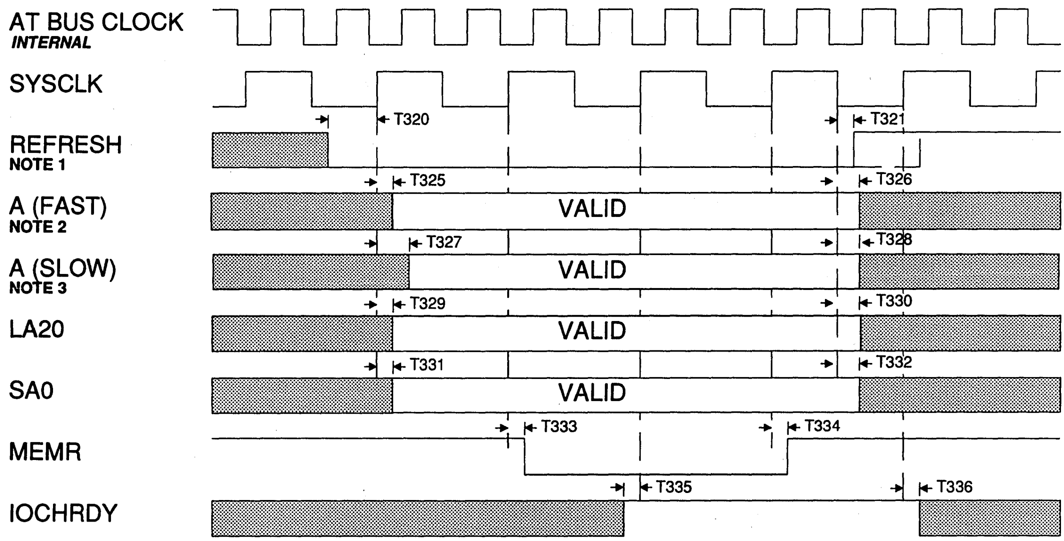


NOTE 1: REFRESH rises 1/2 SYSCLK period later (dashed line) if there is a pending hold cycle (DMA, local access).

NOTE 2: (FAST) is address lines A23 - A21, A19 - A16 and A7 - A1.

NOTE 3: (SLOW) is address lines A20, and A15 - A8

FIGURE 13-48. AT BUS REFRESH CYCLE, DEFAULT TIMING

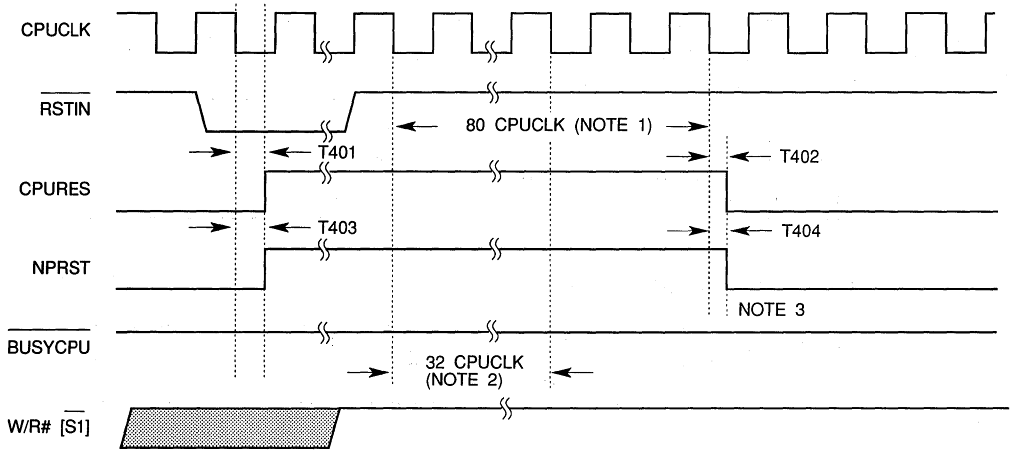
13.3 PROCESSOR TIMING

This section covers the 80286 CPU timing, followed by the 80386SX.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T140	See Table 13-9				
T141	See Table 13-9				
T143	See Table 13-9				
T401	CPUCLK fall to CPURES rise delay		14	ns	
T402	CPUCLK fall to CPURES fall delay		13	ns	
T403	CPUCLK fall to NPRST rise delay		14	ns	
T404	CPUCLK fall to NPRST fall delay		13	ns	
T405	CPUCLK fall to $\overline{\text{BUSYCPU}}$ fall delay		35	ns	①
T406	$\overline{\text{NPBUSY}}$ rise to $\overline{\text{BUSYCPU}}$ rise delay		35	ns	①
T408	$\overline{\text{SO}}$, $\overline{\text{S1}}$ setup time to CPUCLK	9		ns	
T409	$\overline{\text{SO}}$, $\overline{\text{S1}}$ hold time to CPUCLK	1		ns	
T410	M/$\overline{\text{IO}}$ setup time to CPUCLK	26		ns	
T411	M/$\overline{\text{IO}}$ hold time to CPUCLK	1		ns	
T412	Address setup time to CPUCLK	26		ns	
T413	Address hold time to CPUCLK	1		ns	
T414	$\overline{\text{PEACK}}$ setup time to CPUCLK	7		ns	
T415	$\overline{\text{PEACK}}$ hold time to CPUCLK	1		ns	
T416	DPH, DPL setup time to CPUCLK fall	5		ns	
T417	DPH, DPL hold time from CPUCLK fall	19		ns	
T418	D15 - D0 setup time to CPUCLK fall	5		ns	
T419	D15 - D0 hold time from CPUCLK fall	19		ns	

① T405 and T406 are for reference only since $\overline{\text{BUSYCPU}}$ is an asynchronous signal to the 80286. These two parameters are guaranteed by design and will not be tested.

TABLE 13-14. 80286 CPU TIMING

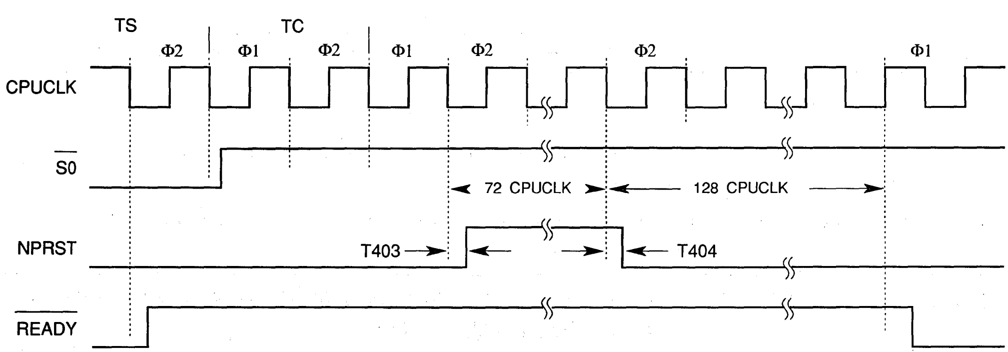


NOTE 1: Minimum of 80 CPUCLKs are asserted before the removal of CPURES.

NOTE 2: W/R# [S1] is sampled 32 CPUCLKs after RSTIN is de-asserted to determine the processor type.

NOTE 3: If, by sampling W/R# [S1], the processor type detected is an 80386SX, BUSYCPU is asserted for a minimum of 10 CPUCLKs before and after the trailing edge of CPURES to perform 80386SX self test.

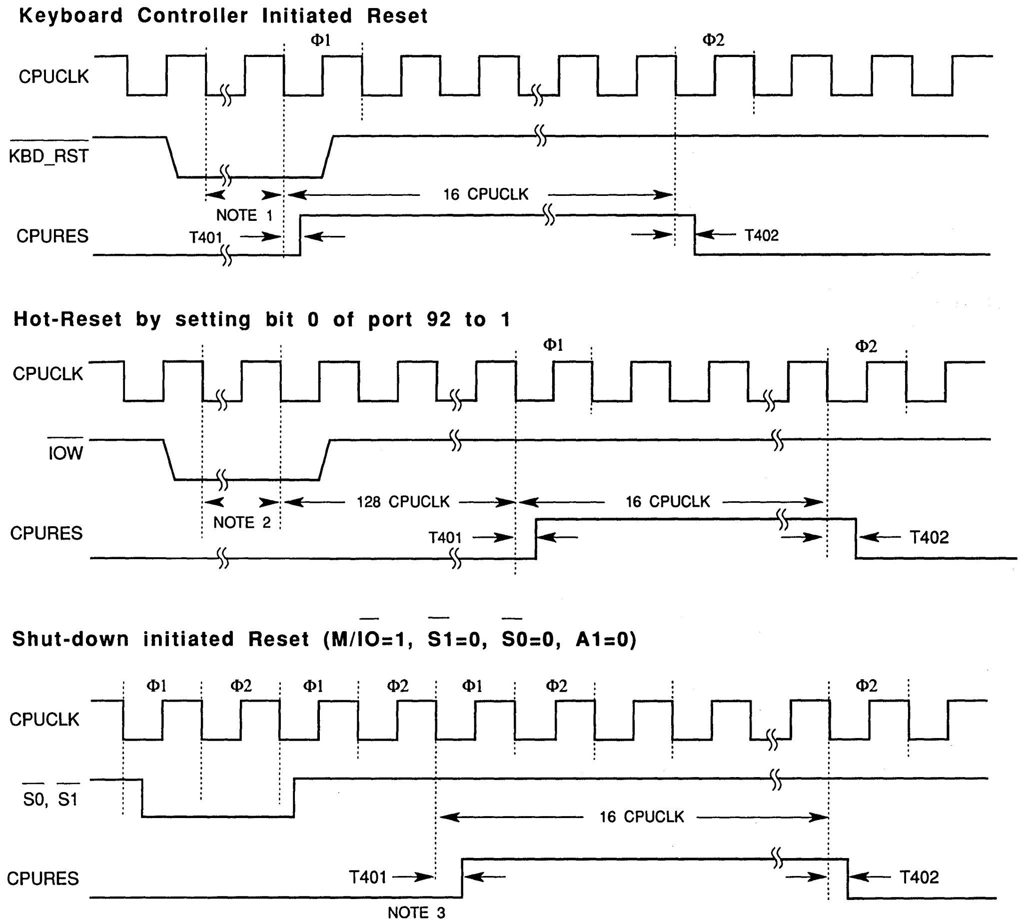
FIGURE 13-49. 80286 - CPURES AND NPRST DURING POWER UP



NOTE 1: NPRST is asserted for 72 CPUCLKs to fulfill the requirements of the 80287 and 80387SX.

NOTE 2: READY is de-asserted for an additional 128 CPUCLKs to prevent the coprocessor from being accessed before it is allowed. This covers up to 25 MHz 80286 working with 12.5 MHz Intel's C287A.

FIGURE 13-50. 80286 - COPROCESSOR RESET (NPRST) INITIATED BY IOW TO PORT F1



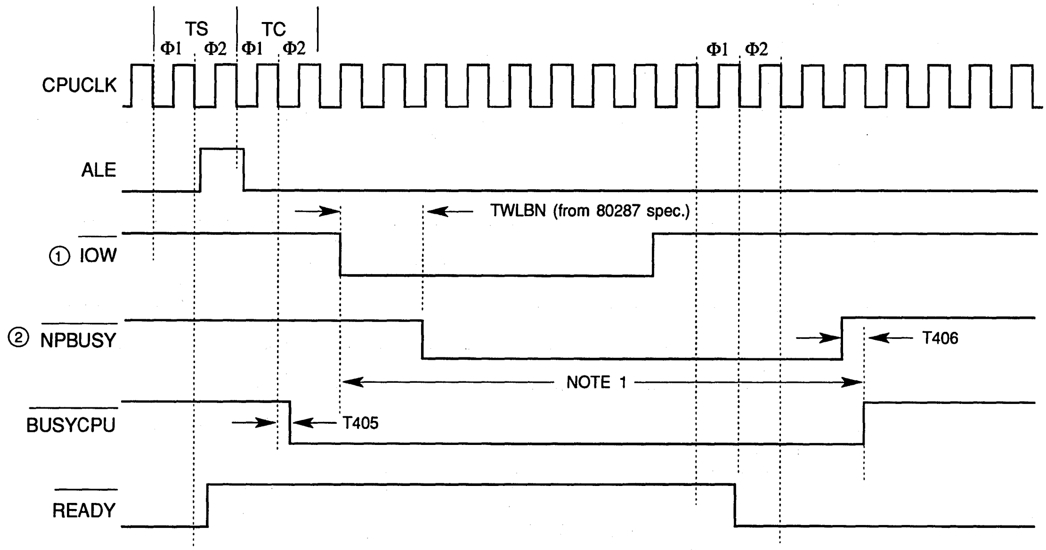
NOTE 1: This time can be as long as 8 MXCTL clocks (~4 SYSCLK) plus 2 CPUCLKs for synchronization.

NOTE 2: 1 SYSCLK, plus 2 CPUCLKs for synchronization.

NOTE 3: CPURES is asserted at the beginning of phase 1 to maintain the phase relationship with the 80286.

FIGURE 13-51. 80286 - PROCESSOR RESET (CPURES) INITIATED BY SOURCES OTHER THAN POWER UP RESET

8

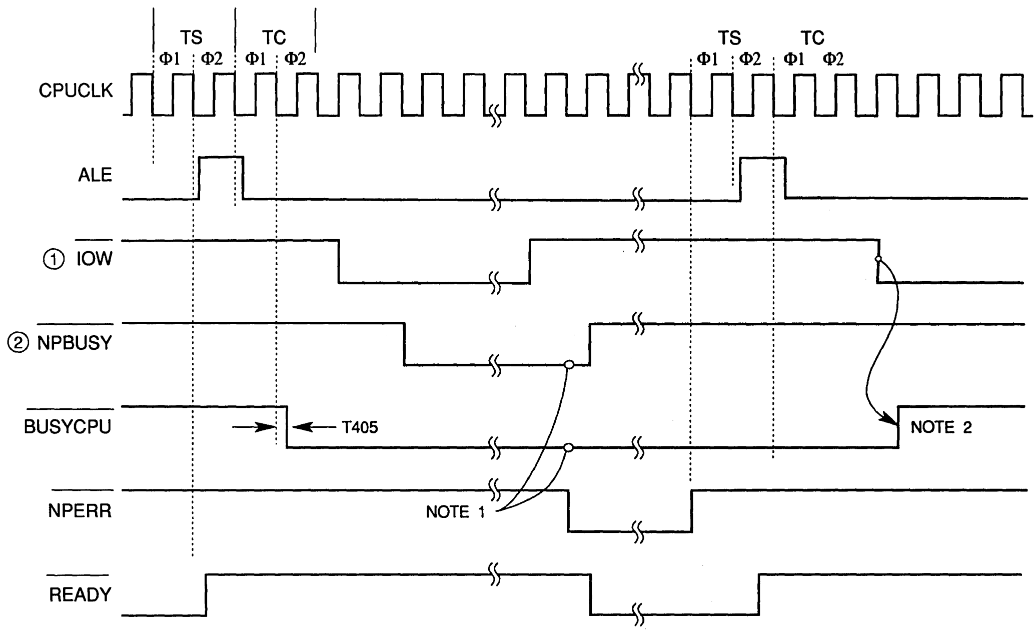


① *TO COPROCESSOR*

② *FROM COPROCESSOR*

NOTE 1: During a write to the 80287, BUSYCPU is asserted at the middle of the first Tc and continues for one SYSCLK plus two CPUCLKs beyond the active edge of IOW, then follows the NPBUSY from the 80287. This early assertion of BUSYCPU is required to maintain compatibility with the 80287.

FIGURE 13-52. 80286 - BUSYCPU ASSERTED DURING COPROCESSOR ACCESS



① *TO COPROCESSOR*

② *FROM COPROCESSOR*

NOTE 1: BUSYCPU is latched by the leading edge of the NPERR signal from the coprocessor while NPBUSY from the coprocessor is still active.

NOTE 2: BUSYCPU is de-asserted by the leading edge of IOW, delayed by a low half of SYSCLK, when any data is written to port F0. BUSYCPU can be an asynchronous signal to the processor and is shown for reference only.

FIGURE 13-53. 80286 - LATCHING BUSYCPU WHEN AN ERROR OCCURS AND CLEARING IT WITH A WRITE TO PORT F0

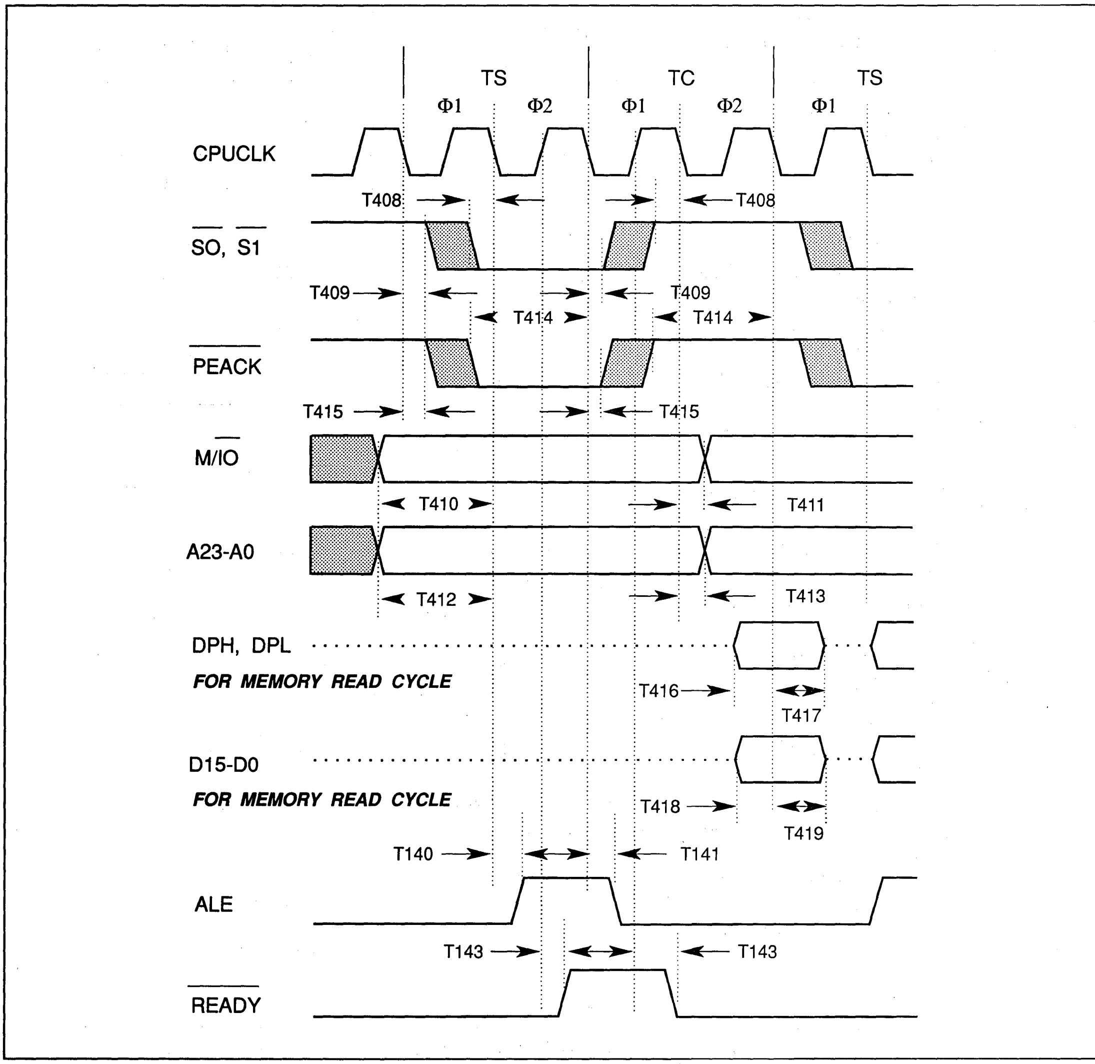


FIGURE 13-54. 80286 - MISCELLANEOUS TIMING

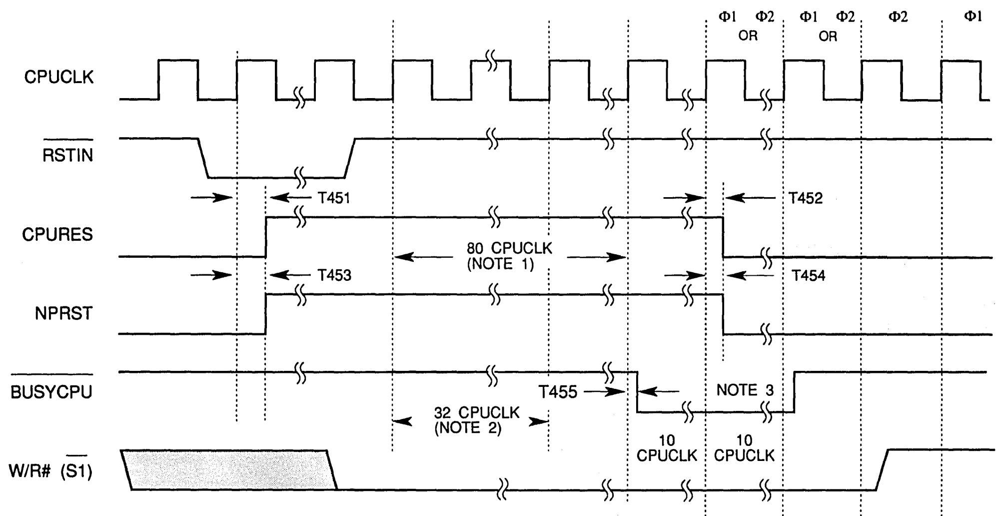
SYMBOL	CHARACTERISTIC	20 MHz MIN	20 MHz MAX	25 MHz MIN	25 MHz MAX	UNITS
T140	See Table 13-9					
T141	See Table 13-9					
T204	See Table 13-6					
T214	See Table 13-6					
T215	See Table 13-6					
T451	CPUCLK rise to CPURES rise delay		14		10	ns
T452	CPUCLK rise to CPURES fall delay		13		10	ns
T453	CPUCLK rise to NPRST rise delay		14		10	ns
T454	CPUCLK rise to NPRST fall delay		13		10	ns
T455	CPUCLK rise to $\overline{\text{BUSYCPU}}$ fall delay		35		35	ns
T456	CPUCLK rise to $\overline{\text{BUSYCPU}}$ rise delay		35		30	ns
T457	$\overline{\text{NPBUSY}}$ fall to $\overline{\text{BUSYCPU}}$ fall delay		30		30	ns
T458	$\overline{\text{NPBUSY}}$ rise to $\overline{\text{BUSYCPU}}$ rise delay		35		35	ns
T460	$\overline{\text{NPERR}}$ fall to EPEREQ rise delay		30		30	ns
T462	ADS# setup time to CPUCLK rise	14		10		ns
T463	ADS# hold time from CPUCLK rise	5		4		ns
T464	W/R# setup time to CPUCLK rise	14		8		ns
T465	W/R# hold time from CPUCLK rise	5		4		ns
T466	D/C# setup time to CPUCLK rise	14		6		ns
T467	D/C# hold time from CPUCLK rise	5		4		ns
T468	M/$\overline{\text{IO}}$ setup time to CPUCLK rise	17		15		ns
T469	M/$\overline{\text{IO}}$ hold time from CPUCLK rise	5		4		ns
T470	$\overline{\text{BHE}}$ setup time to CPUCLK rise	17		15		ns
T471	$\overline{\text{BHE}}$ hold time from CPUCLK rise	3		4		ns

TABLE 13-15. 80386SX CPU TIMING

8

SYMBOL	CHARACTERISTIC	20 MHz MIN	20 MHz MAX	25 MHz MIN	25 MHz MAX	UNITS
T472	HLDA setup time to CPUCLK rise	10		6		ns
T473	HLDA hold time from CPUCLK rise	3		4		ns
T474	HOLD valid delay from CPUCLK rise		26		20	ns
T475	DPH setup time to CPUCLK rise	5		5		ns
T476	DPH hold time from CPUCLK rise	19		19		ns
T477	D15-D0 setup time to CPUCLK rise	5		5		ns
T478	D15-D0 hold time from CPUCLK rise	19		19		ns
T479	A23-A1, BLE# setup time to CPUCLK rise	40		38		ns
T480	A23-A1, BLE# hold time from CPUCLK rise	3		4		ns

TABLE 13-15. 80386SX CPU TIMING cont.

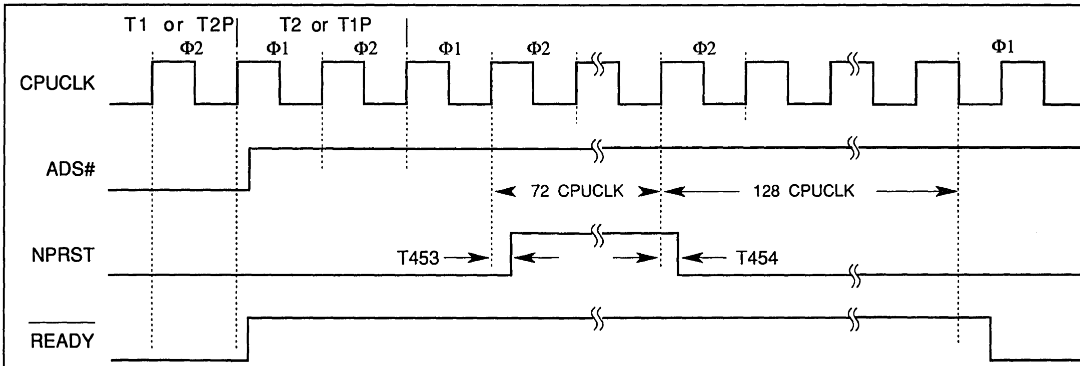


NOTE 1: Minimum of 80 CPUCLKs are asserted before the removal of CPURES.

NOTE 2: W/R# [S1] is sampled 32 CPUCLKs after RSTIN is de-asserted to determine the processor type.

NOTE 3: If, by sampling W/R# [S1], the processor type detected is an 80386SX, BUSYCPU is asserted for a minimum of 10 CPUCLKs before and after the trailing edge of CPURES to perform 80386SX self test.

FIGURE 13-55. 80386SX - CPURES AND NPRST DURING POWER UP



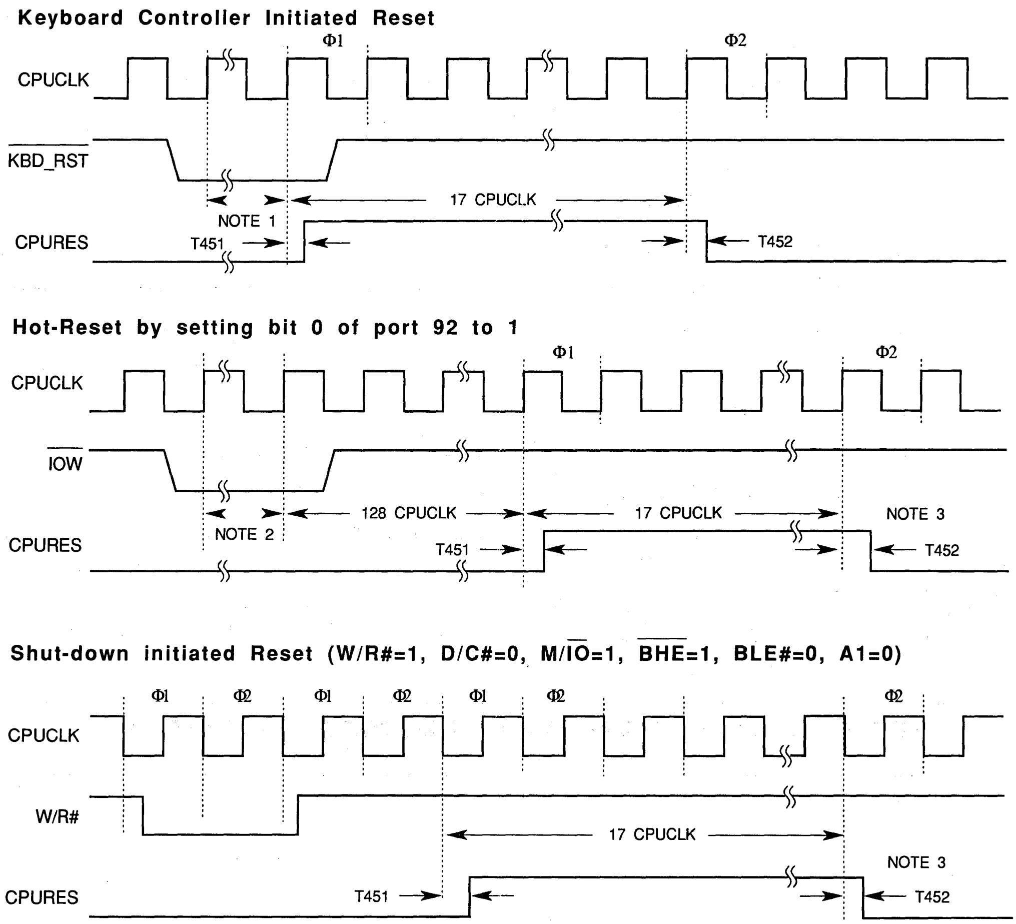
NOTE 1: The trailing edge of NPRST occurs during phase 2 to maintain the correct phase of 80387SX with the 80386SX.

NOTE 2: NPRST is asserted for 72 CPUCLKs to fulfill the requirements of the 80287 and 80387SX.

NOTE 3: READY is de-asserted for an additional 128 CPUCLKs to prevent the coprocessor from being accessed before it is allowed. This covers up to 25 MHz 80286 working with 12.5 MHz Intel's 80C287A.

NOTE 4: 25 MHz operation requires a minimum of 8 MHz for AT Bus Clock.

FIGURE 13-56. 80386SX - COPROCESSOR RESET (NPRST) INITIATED BY IOW TO PORT F1

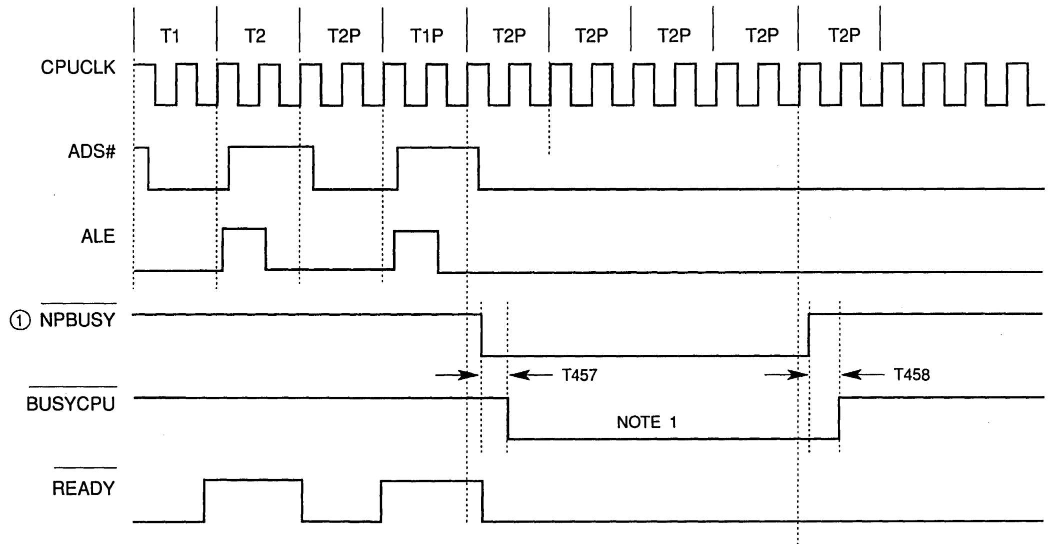


NOTE 1: This time can be as long as 8 MXCTL clocks (~4 SYSCLK) plus 2 CPUCLKs for synchronization.

NOTE 2: 1 SYSCLK, plus 2 CPUCLKs for synchronization.

NOTE 3: CPURES is de-asserted at the beginning of phase 1 to maintain the phase relationship with the 80386SX.

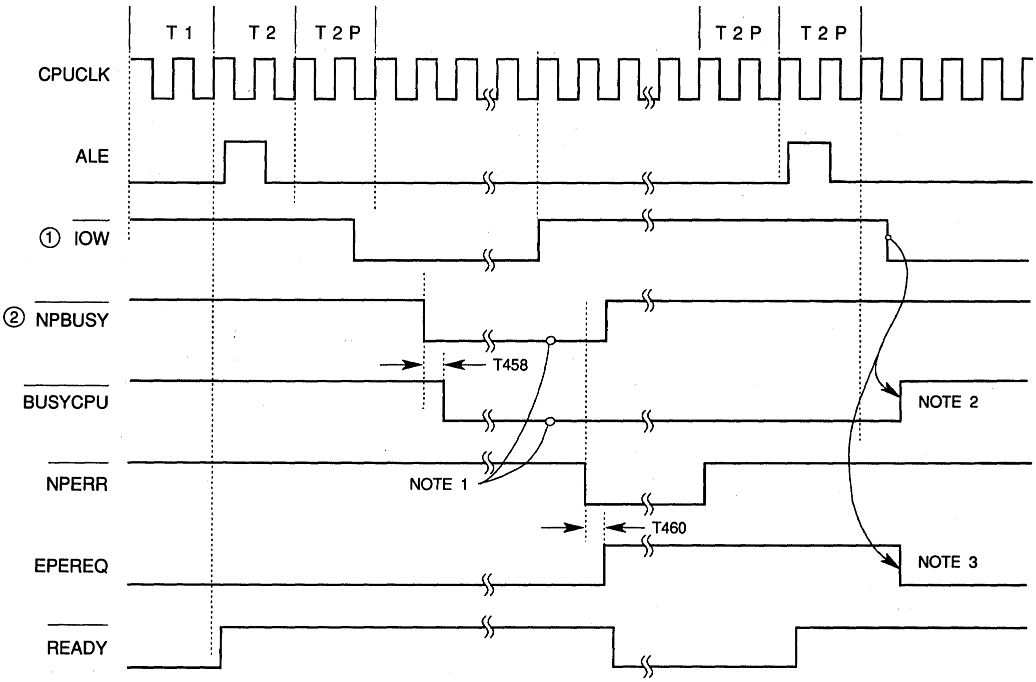
FIGURE 13-57. 80386SX - PROCESSOR RESET (CPURES) INITIATED BY SOURCES OTHER THAN POWER UP RESET



① ***FROM COPROCESSOR***

NOTE 1: BUSYCPU follows NPBUSY from the 80387SX.

FIGURE 13-58. BUSYCPU ASSERTION DURING COPROCESSOR ACCESS



① *TO COPROCESSOR*

② *FROM COPROCESSOR*

NOTE 1: BUSYCPU is latched by the leading edge of the NPERR signal from the coprocessor while NPBUSY from the coprocessor is active.

NOTE 2: BUSYCPU is de-asserted by the leading edge of IOW delayed by a low half of SYSCLK when any data is written to port F0. BUSYCPU can be an asynchronous signal to the processor and is shown for reference only.

NOTE 3: EPEREQ is asserted if NPERR occurs while NPBUSY from the coprocessor is active. EPEREQ is de-asserted by the leading edge of IOW delayed by the low half of SYSCLK when any data is written to port F0. EPEREQ can be asynchronous to the processor and is shown for reference only.

FIGURE 13-59. 80386SX - LATCHING BUSYCPU WHEN AN ERROR OCCURS AND CLEARING IT WITH A WRITE TO PORT F0

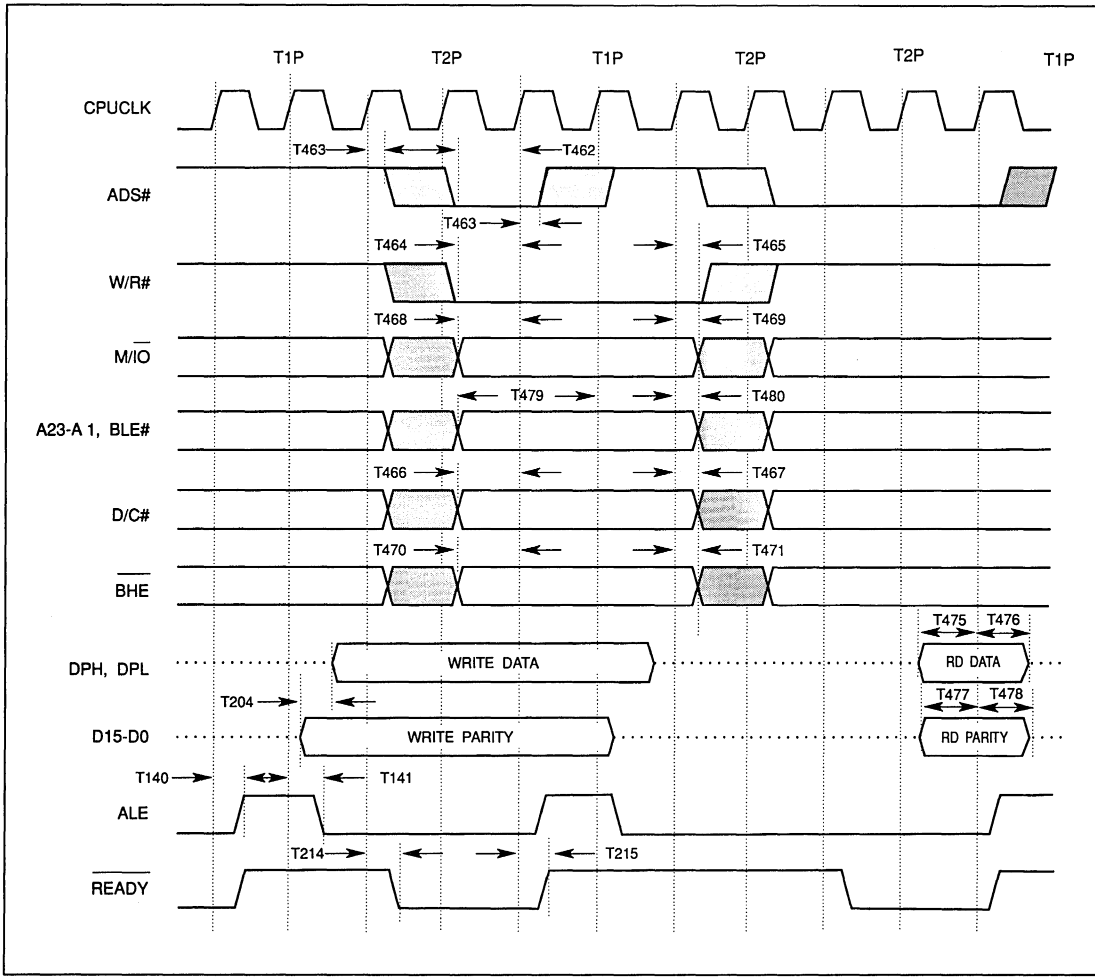


FIGURE 13-60. 80386SX - MISCELLANEOUS TIMING

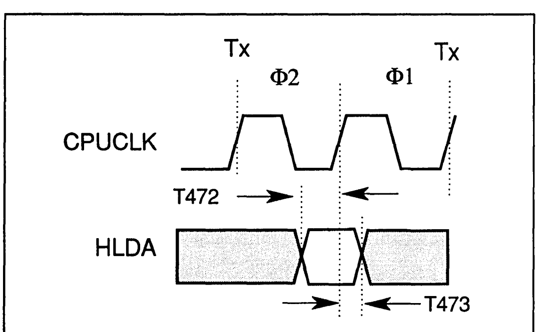


FIGURE 13-61. 80386SX - INPUT SETUP AND HOLD TIMING

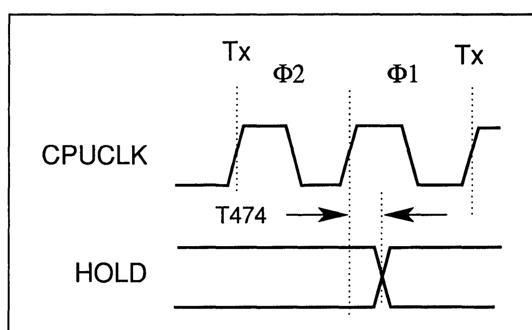


FIGURE 13-62. 80386SX - OUTPUT DELAY TIMING

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13.4 CACHE CONTROLLER TIMING

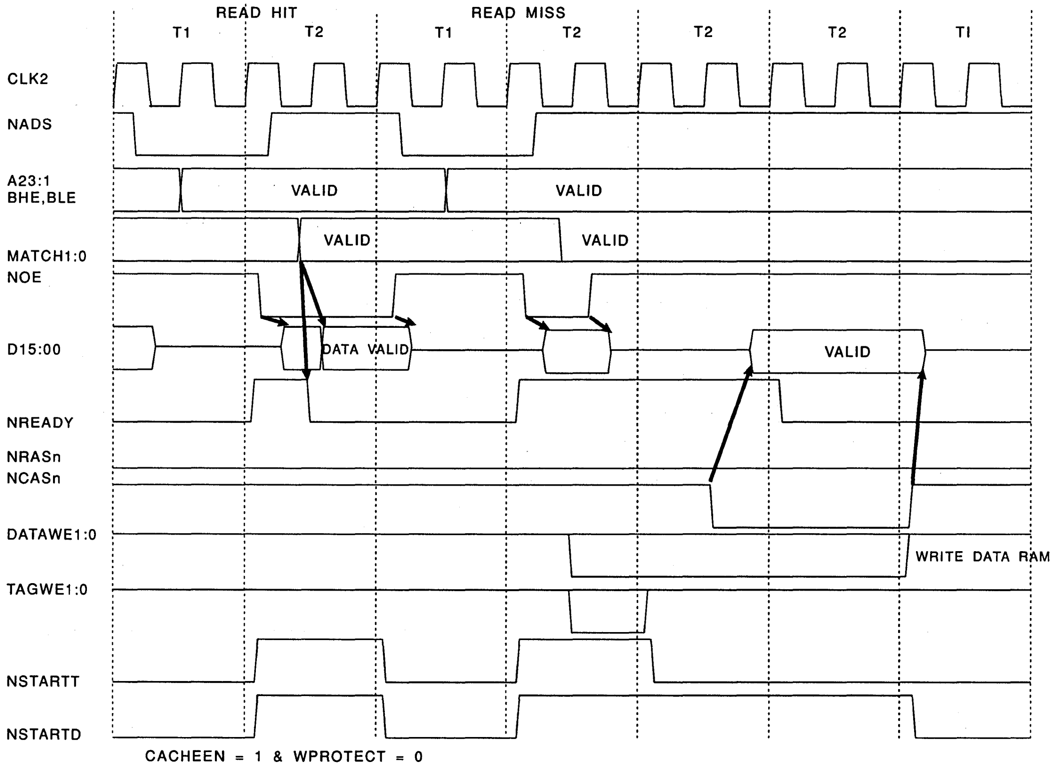

FIGURE 13-63. READ HIT/READ MISS CYCLE

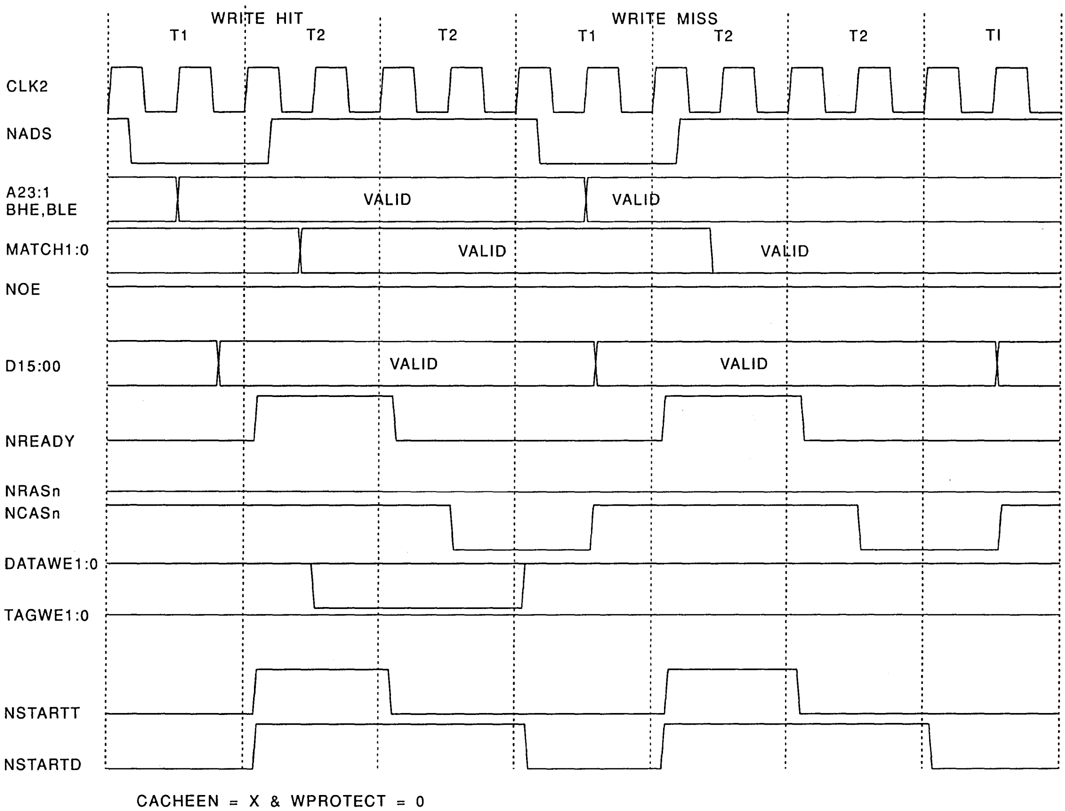

FIGURE 13-64. WRITE HIT/WRITE MISS CYCLE

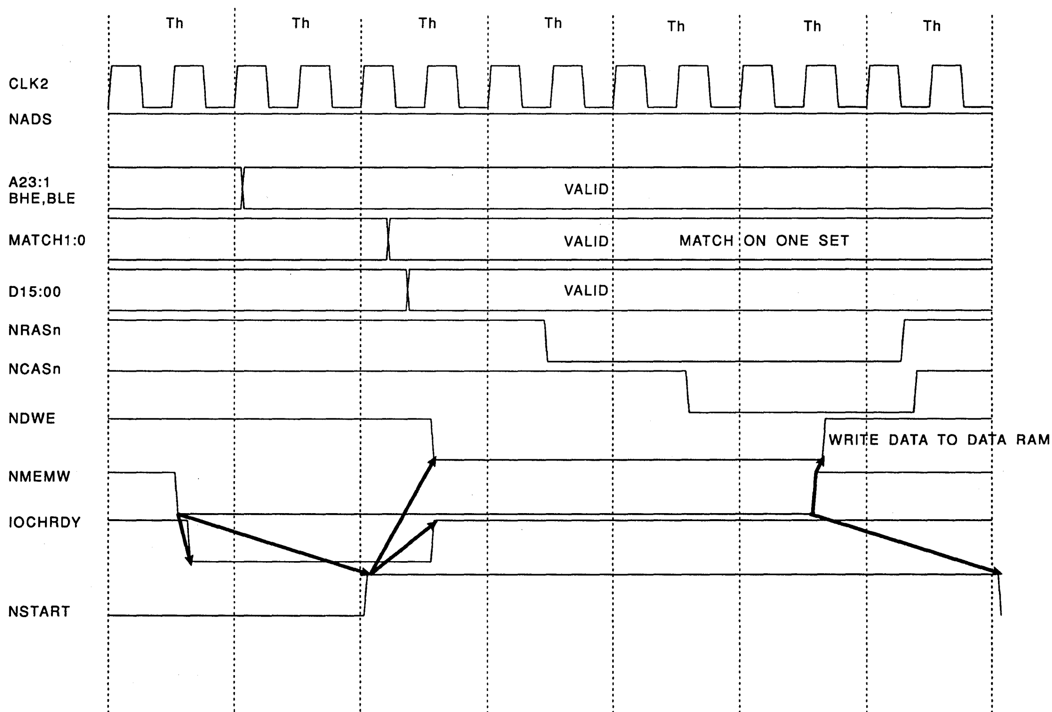

FIGURE 13-65. DMA/MASTERMEMORY WRITE HIT CYCLE

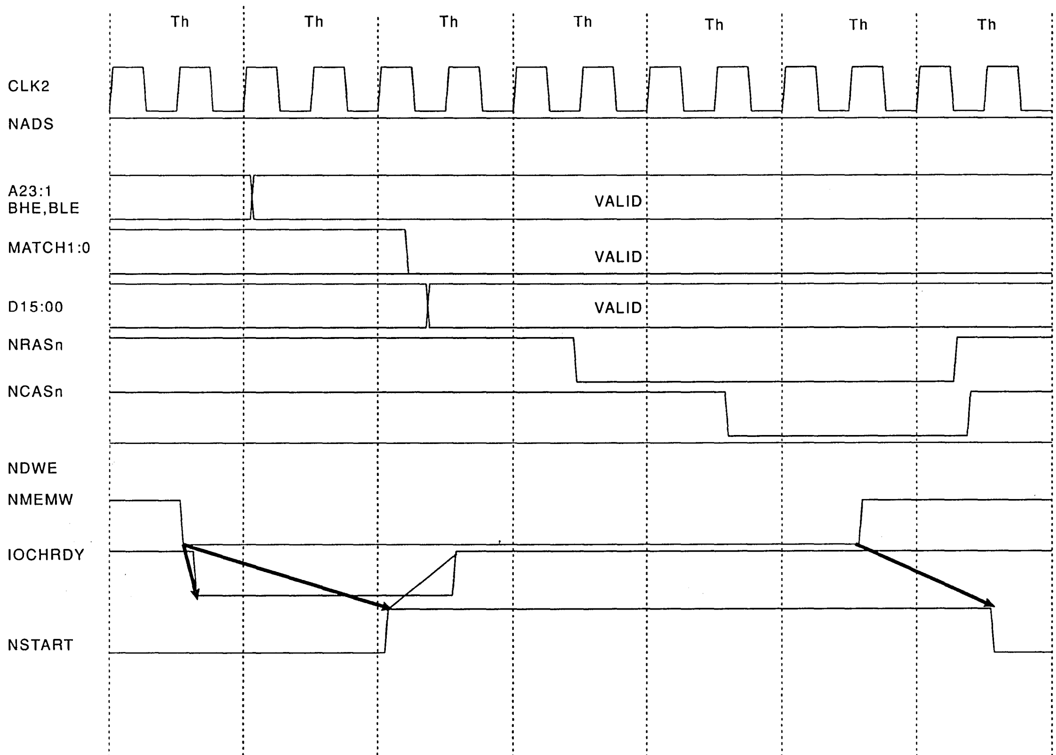

FIGURE 13-66. DMA/MASTER MEMORY WRITE MISS CYCLE

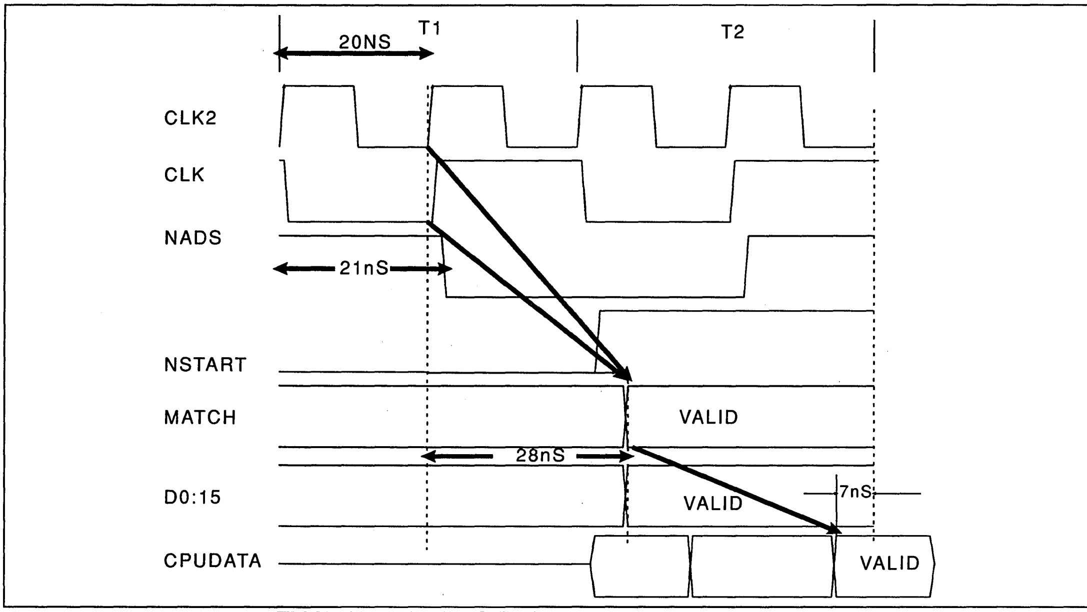

FIGURE 13-67. TAG RAM AND DATA RAM TIMING