

PC87384

Legacy-Reduced SuperI/O with Serial Port, Parallel Port and GPIOs for Notebook and Docking Applications

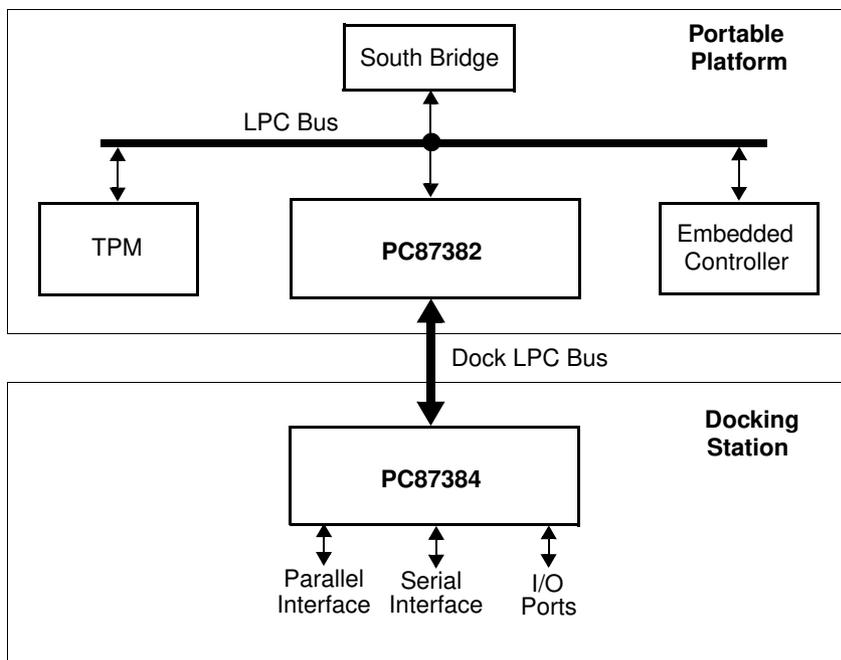
General Description

The PC87384, a member of the Winbond LPC SuperI/O family, is targeted for a wide range of notebook and docking applications where an FIR port is not required. The PC87384 is PC2001 and ACPI compliant, and features Serial Port, Parallel Port and General-Purpose Input/Output (GPIO) support for a total of 21 ports.

Outstanding Features

- LPC bus interface, based on Intel's *LPC Interface Specification* Revision 1.1, August 2002 (supports CLKRUN and LPCPD signals)
- PC2001 and ACPI Revision 3.0 compliant
- Serial IRQ support (15 options)
- Protection features, including GPIO lock and pin configuration lock
- 21 GPIO ports, including 14 with "assert IRQ" capability
- XOR Tree and TRI-STATE[®] device pins (for ICT) testability modes.
- 5V tolerant and back-drive protected pins (except LPC bus pins)
- 64-pin TQFP package

System Block Diagram

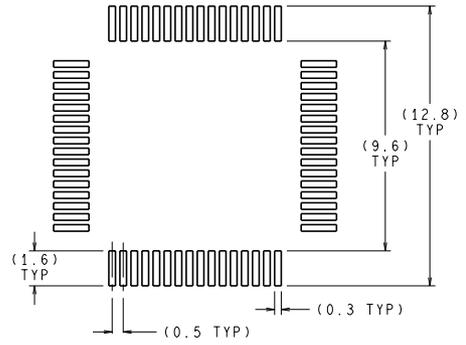
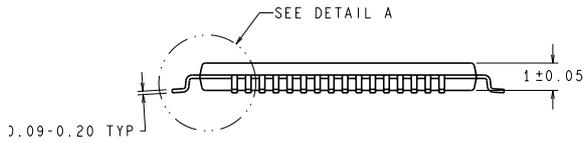
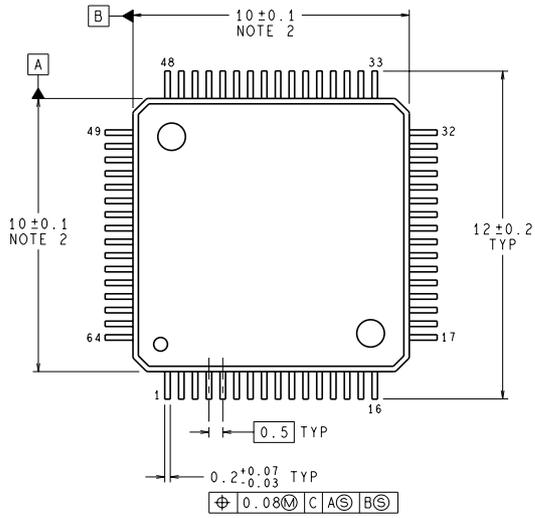


Features

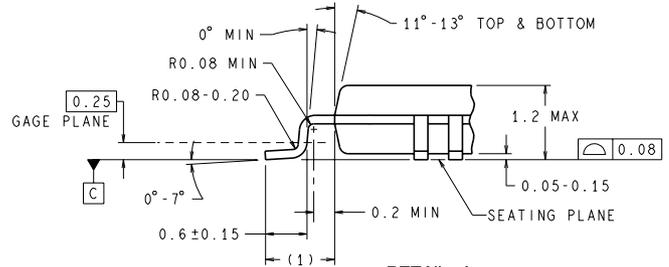
- **LPC System Interface**
 - Synchronous cycles, up to 33 MHz bus clock
 - 8-bit I/O cycles
 - Up to four 8-bit DMA channels
 - LPCPD and CLKRUN support
 - Implements PCI mobile design guide recommendation (*PCI Mobile Design Guide 1.1, Dec. 18, 1998*)
- **PC2001 and ACPI Compliant**
 - PnP Configuration Register structure
 - Flexible resource allocation for all logical devices
 - Relocatable base address
 - 15 IRQ routing options
 - Three optional 8-bit DMA channels (where applicable) selected from four possible DMA channels
 - Supports ACPI Specification Revision 3.0 September 2, 2004
- **Clock Sources**
 - 14.318 MHz or 48 MHz clock input
 - LPC clock, up to 33 MHz
- **Power Supply**
 - 3.3V supply operation
 - All pins are 5V tolerant, except LPC bus pins
 - All pins are back-drive protected, except LPC bus pins
- **21 General-Purpose I/O (GPIO) Ports**
 - 14 support assert IRQ
 - Programmable drive type for each output pin (open-drain, push-pull or output disable)
 - Programmable option for internal pull-up resistor on each input pin
 - Output lock option
 - Programmable option for input debounce mechanism
- **Serial Port**
 - Software compatible with the 16550A and the 16450
 - Shadow register support for write-only bit monitoring
 - UART data rates up to 1.5 Mbaud
- **IEEE 1284-compliant Parallel Port**
 - ECP, with Level 2 (14 mA sink and source output buffers)
 - Software or hardware control
 - Enhanced Parallel Port (EPP) compatible with EPP 1.7 and EPP 1.9
 - Supports EPP as mode 4 of the Extended Control Register (ECR)
 - Selection of internal pull-up or pull-down resistor for Paper End (PE) pin
 - Supports a demand DMA mode mechanism and a DMA fairness mechanism for improved bus utilization
 - Protection circuit that prevents damage to the parallel port when a printer connected to it is powered up or is operated at high voltages (in both cases, even if the PC87384 is in power-down state)
- **Strap Configuration**
 - Base Address (BADDR) strap to determine the base address of the Index-Data register pair
 - Strap Inputs to select testability mode
- **Testability**
 - XOR Tree
 - TRI-STATE device pins

Physical Dimensions

All dimensions are in millimeters



LAND PATTERN RECOMMENDATION



DETAIL A
TYP. SCALE: 25X

64-Pin Thin Quad Flatpack (TQFP)
Order Number 87384MG/K1

Important Notice

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