Design Manager/ Flow Engine Guide

About This Manual

This manual describes the Xilinx Design Manager and Flow Engine, tools that manage and process your design implementation. This manual describes the use of these tools with the Xilinx Alliance Series software. Because the Design Manager and Flow Engine are closely integrated in the Alliance Series, this manual covers both software applications in detail and also covers how to access other tools from the Design Manager.

In the Xilinx Foundation Series software, the Project Manager, rather than the Design Manager, is the top level software tool that is closely integrated with the Flow Engine. For information on the Foundation Series Flow Engine, refer to this manual. For information on the Project Manager, see the *Foundation Series User Guide*.

Note: The Design Manager software documented in this manual is available as a standalone tool from the Foundation Series software. Use the Xilinx Foundation Series → Accessories → Design Manager command to access the standalone Design Manager.

Additional Resources

For additional information, go to http://support.xilinx.com. The following table lists some of the resources you can access from this

page. You can also directly access some of these resources using the provided URLs.

Resource	Description/URL
Tutorial	Tutorials covering Xilinx design flows, from design entry to verification and debugging http://support.xilinx.com/support/techsup/tutorials/index.htm
Answers Database	Current listing of solution records for the Xilinx software tools Search this database using the search function at http://support.xilinx.com/support/searchtd.htm
Application Notes	Descriptions of device-specific design techniques and approaches http://support.xilinx.com/apps/appsweb.htm
Data Book	Pages from *The Programmable Logic Data Book*, which describe device-specific information on Xilinx device characteristics, including read-back, boundary scan, configuration, length count, and debugging http://support.xilinx.com/partinfo/databook.htm
Xcell Journals	Quarterly journals for Xilinx programmable logic users http://support.xilinx.com/xcell/xcell.htm
Tech Tips	Latest news, design tips, and patch information on the Xilinx design environment http://support.xilinx.com/support/techsup/journals/index.htm

Manual Contents

This manual covers the following topics.

- Chapter 1, “Introduction,” describes the Design Manager and Flow Engine main functions, place in the Xilinx design flow, key features, inputs and outputs, and the architectures with which they work. It also outlines the basic procedure for using the tools.
- Chapter 2, “Getting Started,” describes how to start and exit the Design Manager and Flow Engine; how to use the menus, icons, and dialog boxes; and how to use online help.
- Chapter 3, “Using the Design Manager and Flow Engine,” explains how to perform Design Manager and Flow Engine functions.
- Chapter 4, “Menu Commands,” describes the Design Manager and Flow Engine menu commands and options.

- Chapter 5, “Implementation Flow Options,” describes the options you can set to control the implementation flow.
- Appendix A, “Glossary,” defines important words, terms, concepts, and ideas used in this manual.
- Appendix B, “Legacy Information,” describes major changes to the software since the previous release.

Conventions

This manual uses the following typographical and online document conventions. An example illustrates each typographical convention.

Typographical

The following conventions are used for all documents.

- `Courier font` indicates messages, prompts, and program files that the system displays.

  ```
  speed grade: -100
  ```

- **`Courier bold`** indicates literal commands that you enter in a syntactical statement. However, braces "{ }" in Courier bold are not literal and square brackets "[ ]" in Courier bold are literal only in the case of bus specifications, such as bus [7:0].

  `rpt_del_net=`

  `Courier bold` also indicates commands that you select from a menu.

  `File` → **`Open`**

- *Italic font* denotes the following items.

  - Variables in a syntax statement for which you must supply values

    `edif2ngd` *design_name*

  - References to other manuals

    See the *Development System Reference Guide* for more information.

- Emphasis in text

  If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

- Square brackets "[ ]" indicate an optional entry or parameter. However, in bus specifications, such as bus [7:0], they are required.

  edif2ngd [*option_name*] *design_name*

- Braces "{ }" enclose a list of items from which you must choose one or more.

  lowpwr ={**on** | **off**}

- A vertical bar " | " separates items in a list of choices.

  lowpwr ={**on** | **off**}

- A vertical ellipsis indicates repetitive material that has been omitted.

```
IOB #1: Name = QOUT'
IOB #2: Name = CLKIN'
.
.
.
```

- A horizontal ellipsis ". . ." indicates that an item can be repeated one or more times.

  allow block *block_name loc1 loc2* . . . *locn;*

Online Document

The following conventions are used for online documents.

- Red-underlined text indicates an interbook link, which is a cross-reference to another book. Click the red-underlined text to open the specified cross-reference.
- Blue-underlined text indicates an intrabook link, which is a cross-reference within a book. Click the blue-underlined text to open the specified cross-reference.

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Chapter 3 Using the Design Manager and Flow Engine

Chapter 5 Implementation Flow Options

Appendix A Glossary

Appendix B Legacy Information

Chapter 1

Introduction

This chapter briefly describes the Design Manager and Flow Engine. It describes their main functions, place in the design flow, major features, inputs and outputs, and the device architectures with which they work. It also outlines the basic procedure for using these tools. This chapter contains the following sections.

- "Overview"
- "Design Flow"
- "Inputs and Outputs"
- "Architectures"
- "Design Manager Fundamentals"
- "Flow Engine Fundamentals"

Overview

The Design Manager is the top level software module in the Xilinx Alliance Series Development System. Use the Xilinx Development System tool suite to implement a design into a Xilinx device. The Design Manager provides access to all the tools you need to read a design file from a design entry tool and implement it in a Xilinx device. The Design Manager performs the following functions.

- Organizes and manages your design implementation data
- Creates multiple design versions for management of design changes
- Creates multiple implementation revisions for management of implementation strategies
- Provides access to reports

- Manages data for and provides access to the following tools. The tools differ for FPGA and CPLD families.
  - Flow Engine (FPGA and CPLD)
  - Timing Analyzer (FPGA and CPLD)
  - Floorplanner (All XC4000 families, Virtex, Spartan / XL, and Spartan2 FPGA families only)
  - PROM File Formatter (FPGA)
  - Hardware Debugger (FPGA)
  - FPGA Editor (FPGA)
  - Chip Viewer (CPLD)
  - JTAG Programmer (All XC4000 families, XC5200, Virtex, Spartan / XL, and Spartan2 FPGA families and CPLD families)

The Design Manager manages your Xilinx designs. The Flow Engine implements your designs. The Flow Engine is closely integrated with the Design Manager, sharing many of the same menus and dialog boxes. You can use the Design Manager and Flow Engine together to perform the following functions.

- Target different devices
- Generate and export timing simulation data for external simulation tools
- Generate and export configuration data

Design Flow

You can use a variety of schematic and HDL tools for design entry. The netlist formats supported as inputs to the Design Manager are listed in the “Inputs and Outputs” section.

After design entry, you can use the Design Manager and Flow Engine to process your design in the following basic steps.

1. Implementation of your design for a specific target device
2. Report generation showing the status of your design
3. Timing analysis for design verification

4. Export of your design for timing simulation and programming

The following figure illustrates the processing steps and the flow of files in and out of the Design Manager and Flow Engine.

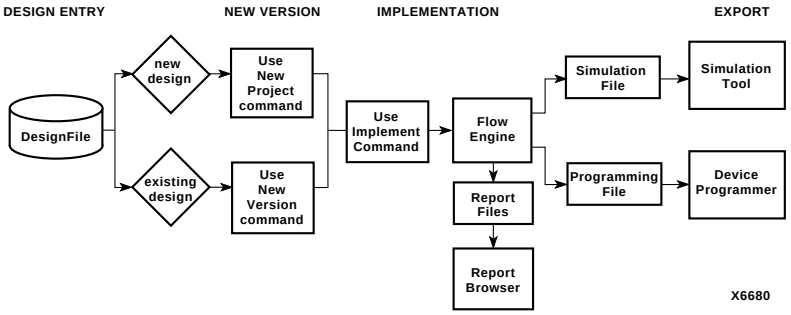


Figure 1-1 Design Manager/Flow Engine Design Flow

Inputs and Outputs

The Design Manager accepts the following file types as inputs.

.edf, .edn, .edif, .sedif	EDIF netlist file
.pld	PLUSASM file (CPLD only)
.xnf, .xtf, .sxnf	Xilinx hierarchical netlist file

The Design Manager and Flow Engine output report, timing simulation, and programming files.

Architectures

You can use the Design Manager and Flow Engine with the following Xilinx device families.

- XC3000A™ / L™
- XC3100A™ / L™
- XC4000E™ / L™
- XC4000EX™ / XL™ / XV™ / XLA™
- XC5200™
- Spartan™ / XL™
- Spartan2™
- Virtex™
- XC9500™ / XL™ / XV™

The Spartan, Virtex, XC3000, XC4000, and XC5200 families compose the FPGA families. The XC9500 families compose the CPLD families.

Design Manager Fundamentals

You can perform multiple functions from within the Design Manager, such as launching Xilinx tools and managing your projects, design versions, and implementation revisions.

Projects

The Design Manager window displays all Xilinx data related to a single project. When you create a project, a design version and implementation revision are automatically created so you always have a revision on which to run the software tools. A project includes all design versions and implementation revisions that are created as you implement your design. You can work with multiple projects, but only one is active at a time. The hierarchical structure in the Design Manager project view shows the relationships of the data elements to each other.

Design Versions

You create your design using third party front-end tools that support schematic and Hardware Description Language (HDL) entry. The Design Manager reads in the design netlist and creates a design version in the Design Manager project view. If the design netlist changes, the Design Manager reads in the modified design and creates a new design version.

You can try modified versions of your design and easily keep track of them. Each new set of changes becomes a new design version and is assigned a design version name by the Design Manager. You can choose any one of the available design versions for processing.

When you create a new design version, a new implementation revision is automatically created. Each design version can contain multiple implementation revisions.

Note: The Design Manager saves design versions in the Xilinx database format, not in the format of the front-end editor.

Implementation Revisions

After you create a design version, you can try different implementation strategies on your design. The data associated with each of these implementation strategies is called an implementation revision. Each implementation revision contains the data files and reports that are created based on a specific set of implementation strategies.

This method allows you to vary how your design is implemented in order to achieve your design objectives. For example, you can maximize speed and density in your design by controlling the implementation settings or by targeting a different device family better suited for your design.

Note: If you are using an HDL flow, it is strongly recommended that you create a new synthesis netlist when you change FPGA or CPLD families. This ensures that the tools make the best use of the target device.

When you create a new revision either manually or automatically, the data from the “last” revision is copied to the new revision by default. The “last” revision is bottommost in the Design Manager project view. You can copy data from other revisions by setting options in the Copy Persistent Data field of the New Version or New Revision

dialog box. You can also copy data from other revisions by using the Set Constraint File, Set Guide File(s), and Set Floorplan File(s) menu commands after the revision is created. If you want to change any of the implementation options, use the Options command.

Note: Because you must always have an implementation revision on which to run the tools, at least one revision must always exist for each version in the Design Manager. If only one revision exists inside a version, you can only delete the revision by deleting the version.

Design Management Basic Procedure

The typical procedure for managing a design is as follows.

1. In your design entry tool, create a design.
2. In your design entry tool, output your design as an EDF, EDIF, EDN, SEDIF, PLD, SXNF, XNF, or XTF file. The PLD format is supported for CPLDs only.
3. In the Design Manager, open an existing project or create a new project in which to implement your logic design.
4. Implement your design.
   - If necessary, choose a different target device in which to implement your design. The initial target device is specified in the input design or when you create a new implementation revision.
   - Select implementation, simulation, and configuration options. You can use the default settings, an existing set of options, or set new options.
   - Run your design implementation and create timing simulation files and a device programming file.
5. Review your design reports to verify that your design fits within the target device and that your timing requirements are met.

6. If your design requirements are not met, you can do any of the following and process your design again.
   - Change your logic design.
   - Choose a different target device, package, or speed grade.
   - Define a different set of implementation, simulation, or configuration options.

Flow Engine Fundamentals

The Flow Engine allows you to easily process and control the implementation of your design.

Design Implementation

When you process your design, the Flow Engine translates the design file into the Xilinx Native Generic Database (NGD) format. The Flow Engine then implements your design and generates bitstream data.

The Flow Engine allows you to control the implementation of your design in different ways. For example, if you are new to Xilinx software or want to quickly check your design, you can run the Flow Engine automatically using the Design Manger Design → Implement command. However, if you are an experienced user, you can open the Flow Engine from the Design Manger Tools menu and use the interactive Flow Engine to execute steps separately. You can also fine tune your design by modifying your implementation, simulation, and configuration options. You can access these options through the Design Manager's Design → Options command or the Flow Engine's Setup → Options command. Use the Design Manager Options command with the automatic Flow Engine and the Flow Engine Options command with the interactive Flow Engine.

If you use the interactive Flow Engine, you can control how far to process your design using the Flow Engine's Setup → Stop After command. In the Stop After dialog box, select a step as your target break point. For example, if you want to map, place, and route your design but not create device programming file, select Stop After Place&Route. A stop sign indicates where the process flow will stop.

Following are the steps run by the Flow Engine.

Translate

During this step, the Flow Engine merges all of the input netlists. You can control aspects of the Translate step by setting implementation options using the Options command from the Design Manager or Flow Engine. The Flow Engine accomplishes this step by running NGDBuild, which is described in the "NGDBuild" chapter of the *Development System Reference Guide*.

Map (FPGA)

During this step, the Flow Engine maps a logical design to a Xilinx FPGA. The input is an NGD file, which contains a logical description of the design and macro library (NMC) files. The Flow Engine first performs a logical Design Rule Check (DRC) on the design in the NGD file. It then maps the logic to the components in the target Xilinx FPGA. The output design is an Native Circuit Description (NCD) file that physically represents the design mapped to the components in the Xilinx FPGA. You can control aspects of the Map step by setting implementation options using the Options command from the Design Manager or Flow Engine. The Flow Engine accomplishes the Map step by running the MAP program, which is described in the "MAP—The Technology Mapper" chapter of the *Development System Reference Guide*.

Place&Route (FPGA)

During this step, the Flow Engine takes the NCD file produced during Map and places and routes the design to produce a routed NCD file. The output NCD file can also act as a guide file if you place and route the design again. You can control aspects of the Place and Route step by setting implementation options using the Options command from the Design Manager or Flow Engine. To accomplish this step, the Flow Engine runs the PAR program, which is described in the "PAR—Place and Route" chapter of the *Development System Reference Guide*.

Fit (CPLD)

During Fit, the Flow Engine launches the CPLD Fitter to minimize and collapse the combinational logic of your design so that it requires

the least number of macrocell and product term resources. It also partitions and maps your design to fit within the architecture of the CPLD. You can control aspects of this step by setting implementation options using the Options command from the Design Manger or Flow Engine.

Timing (Sim)

The Flow Engine runs this step to produce timing simulation data. The data that is produced depends on the simulation options you set using the Options command from the Design Manager or Flow Engine. To accomplish this step, the Flow Engine runs NGDAnno and one of the following tools, all of which are described in the *Development System Reference Guide.*

- NGD2EDIF
- NGD2VER
- NGD2VHDL

Configure (FPGA)

After the design has been completely routed, the Flow Engine configures the device so that it can execute the desired function. Using a fully routed NCD file as input, it produces a configuration bitstream, a binary file with a .bit extension. The BIT file contains all of the configuration information from the NCD file defining the internal logic and interconnections of the FPGA, plus device-specific information from other files associated with the target device. The binary data in the BIT file can then be downloaded into the FPGA's memory cells, or it can be used to create a PROM file. You can control aspects of this step by setting configuration options using the Options command from the Design Manager or Flow Engine. The Flow Engine accomplishes this step by running BitGen, which is described in the “BitGen” chapter of the *Development System Reference Guide*.

Bitstream (CPLD)

During this step, the Flow Engine produces a JED programming file. The JTAG Programmer uses this file to configure CPLD devices. You can control aspects of this step by setting implementation options using the Options command from the Design Manager or Flow Engine.

Note: For more information on setting implementation, simulation, and configuration options, see the "Specifying Implementation Flow Options" section of the "Using the Design Manager and Flow Engine" chapter.

Smart Flow Engine

When the Flow Engine is first invoked, it automatically looks for changes made to certain files. If the Flow Engine detects changes, it restarts the flow for the implementation revision as follows. This feature is called the Smart Flow Engine.

- If a previously set target break point has already been reached at the time you launch the Flow Engine, the Smart Flow Engine removes the break point and implements the next process in the flow.
- If any of the following changes are made, the Smart Flow Engine determines which process to rerun.
  - Changes to implementation flow options from the Options dialog box or Template Manager
  - Changes to design, constraints, guide, or output files

    The following table shows which flow process the Flow Engine reruns if you make changes to a particular file.

Table 1-1 Smart Flow Engine Change Detection

File Changed	Process Rerun
design_name.ucf	Translate
design_name.ngd *design_name*.mfp	Map (FPGA)
map.ncd guide.ncd	Place&Route (FPGA)
design_name.ngd *design_name*.gyd	Fit (CPLD)
design_name.ncd	Timing (Sim) (FPGA)
design_name.vm6	Timing (Sim) (CPLD)
design_name.ncd	Configure (FPGA)
design_name.vm6	Bitstream (CPLD)

The Smart Flow Engine notifies the Design Manager of the state and status of your implementation revision and the Design Manager updates the information in the main window.

Note: The Flow Engine checks for changes related to successfully completed processes. If a process did not complete successfully, the Flow Engine does not look for changes related to this process but automatically restarts the flow at this process or, if appropriate, at a previous process. If the Flow Engine is already open and you want to check for changes, use the Setup → Update Flow command.

Chapter 2

Getting Started

This chapter leads you through the basic operation of the Design Manager and Flow Engine. This chapter contains the following sections.

- "Preparing the Input Design File"
- "Starting and Exiting the Design Manager"
- "Starting and Exiting the Flow Engine"
- "Using the Interface"
- "Using Help"

Preparing the Input Design File

Create the input design in your design entry tool and save it in one of acceptable formats described in the "Inputs and Outputs" section of the "Introduction" chapter.

Starting and Exiting the Design Manager

The Design Manager runs on PCs and workstations. You can start the Design Manager as a standalone tool on the PC or from the command line. Use the following procedures to start and exit the Design Manager.

Starting as a Standalone Tool

If you installed the Design Manager as a standalone tool on a PC, click the Design Manager icon (shown in the following figure) on the Windows desktop or select dsgnmgr.exe from the Windows 95®, Windows 98®, or Windows NT® Start button.

Starting from the Command Line

To start the Design Manager from the UNIX® or DOS™ command prompt, enter one of the following commands.

- **`dsgnmgr`**
- **`xilinx`**

Exiting the Design Manager

To exit the Design Manager, select the **`File`** → **`Exit`** menu command. A confirmation box appears. Click **`Yes`** to exit the Design Manager.

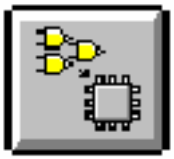
Starting and Exiting the Flow Engine

The Flow Engine runs on PCs and workstations. Use the following procedures to start and exit the Design Manager.

Starting from the Alliance Series

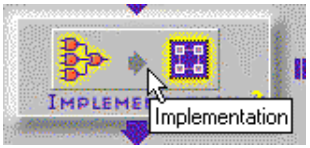
To launch the Flow Engine from the Alliance Design Manager, select an implementation revision and do one of the following.

- Select **Tools** → **Flow Engine**.
- Click the Flow Engine toolbox button, shown in the following figure.



Starting from the Foundation Series

To launch the Flow Engine from the Foundation Project Manager, select the Implementation phase button on the project flow chart, shown in the following figure.



Note: For more information about accessing and using the Flow Engine from the Foundation Project Manager, see the "Design Implementation" chapter of the *Foundation Series User Guide*.

Exiting the Flow Engine

To exit the Flow Engine, select the **Flow** → **Close** command.

Using the Interface

This section describes the elements that compose the Design Manager and Flow Engine interfaces and how to use them.

Note: Menus, dialog boxes, and parts of the application window are documented as they appear on a UNIX workstation. Differences between the PC and the workstation applications are documented if there is a difference in operation between the two platforms.

Main Window

This section describes the Design Manager and Flow Engine main windows, their menus, toolbar, and status bar. By default, the main window displays a menu bar and toolbar at the top and status bar at the bottom of the window. You can hide the toolbar or status bar from view by selecting the Toolbar or the Status Bar commands, respectively, from the View menu. In the Design Manager, the toolbox also appears by default. You can hide it from view by selecting the Toolbox command from the View menu.

Design Manager Window

To work with the Design Manager, you must create a project. See the "Creating a New Project" section of the "Using the Design Manager and Flow Engine" chapter for information. After you create a project, the Design Manager window appears configured for the loaded design, as shown in the following figure.

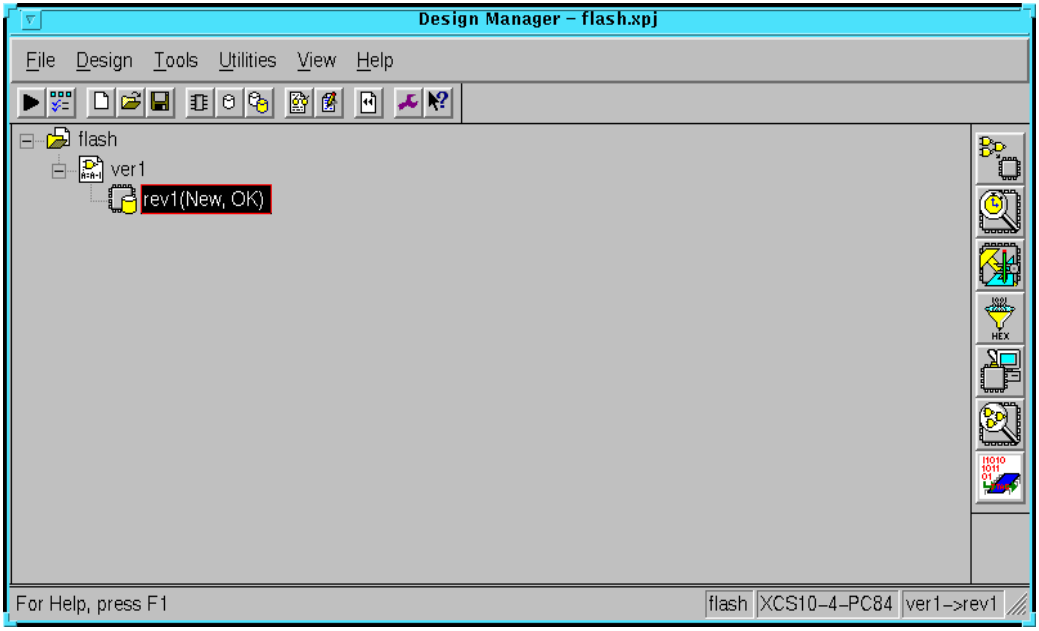


Figure 2-1 Design Manager Window

The Design Manager project view displays design version and implementation revision icons. The toolbox allows you to launch Xilinx

tools. You can select Design Manager commands from the menus and toolbar.

Flow Engine Window

You can open the Flow Engine automatically through the Design Manager implementation process or manually from the Design Manager Tools menu or toolbox. See the “Implementing a Design from the Design Manager” or “Implementing a Design from the Flow Engine” section of the “Using the Design Manager and Flow Engine” chapter for descriptions of the different ways to open the Flow Engine and implement a design. When you open the Flow Engine, the Flow Engine window appears as shown in the following figures.

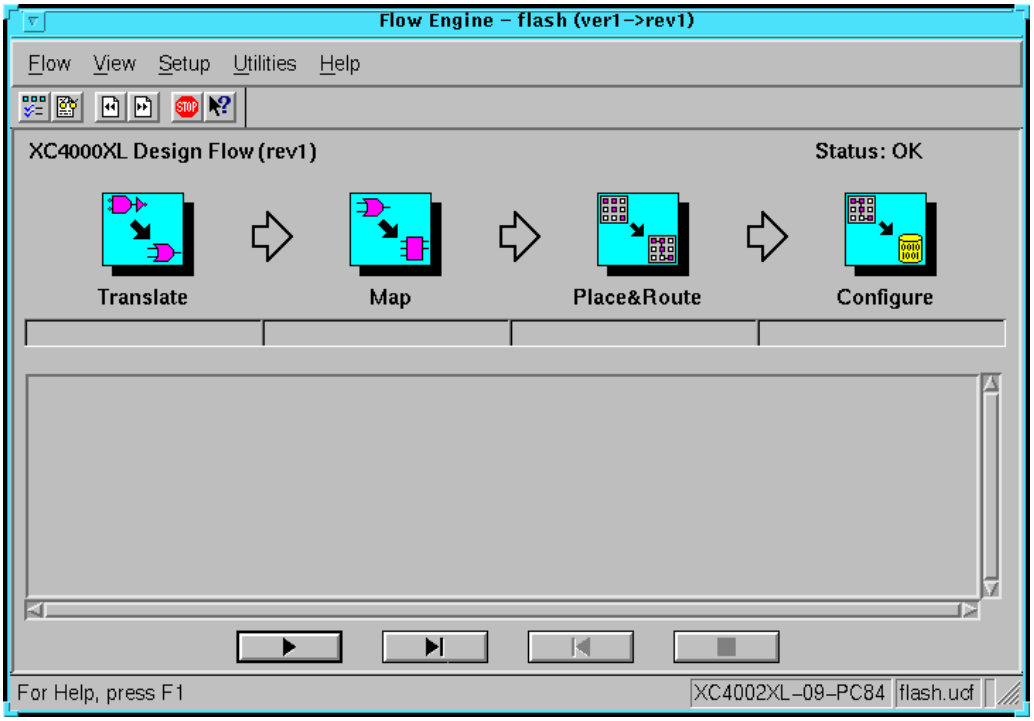


Figure 2-2 Flow Engine Window (FPGA)

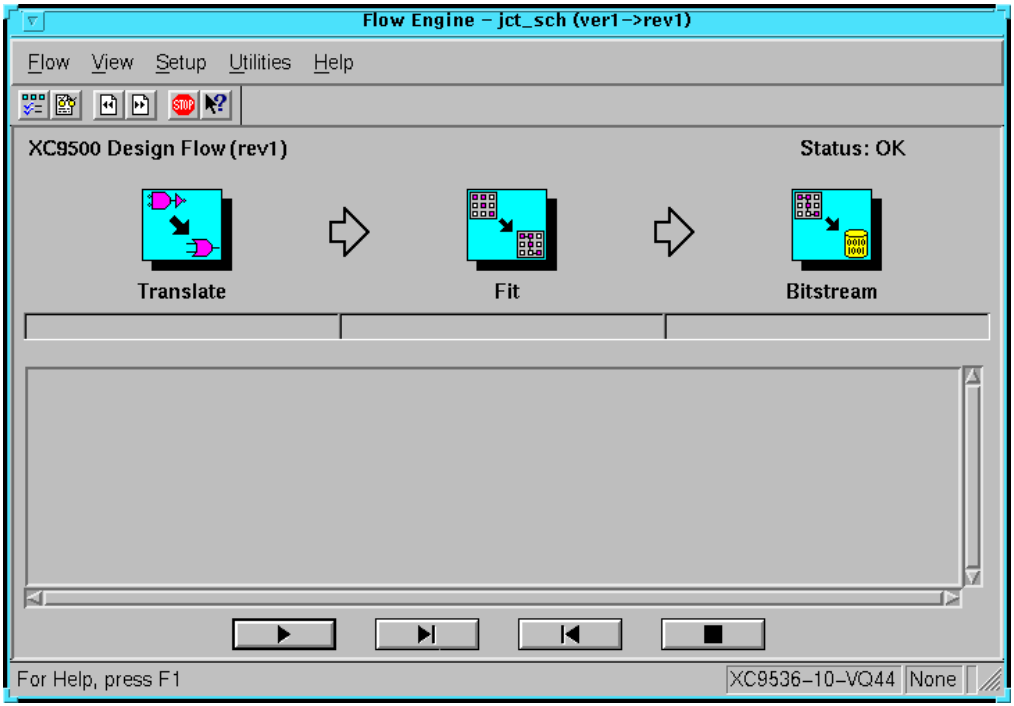


Figure 2-3 Flow Engine Window (CPLD)

Process indicators in the Flow Engine main window show which step in the design flow is currently processing. The arrows between each step turn black after the previous step is completed. Below each process indicator, a progress bar shows the status of each processing step, whether Running, Completed, Aborted, or Failed. You can control each step in the processing of your design by using the run control buttons at the bottom of the Flow Engine main window. Select Flow Engine commands from the menus and toolbar.

Title Bar

The title bar displays the program name and the name of the currently loaded design.

Menu Bar

All of the Design Manager commands are available in the pull-down menus of the Design Manager window after a design is loaded. Flow

Engine commands are available in the pull-down menus of the Flow Engine window.

All menu commands and keyboard combinations for certain commands are described in the “Menu Commands” chapter.

Toolbar Buttons

You can access frequently used commands by clicking the appropriate toolbar button. See the “Toolbars” section of the “Menu Commands” chapter for an explanation of each toolbar button.

The toolbar can either be docked (that is, attached to the main window) or floating (that is, contained in its own window). You can position the toolbar as follows.

- To move the toolbar, point to a spot between toolbar buttons (or to the title bar, if the toolbar is floating), then drag and drop the toolbar to the desired location. If you drop the toolbar near an edge of the main window, it will be docked on that edge. If you drag the toolbar away from the window edge, it will float instead of being docked.
- To toggle between a floating toolbar and a docked toolbar, double-click on a spot between toolbar buttons (or on the title bar, if the toolbar is floating).
- To prevent the toolbar from being docked, press the **`Ctrl`** key as you move the toolbar.

Toolbox Buttons

You can access the available set of Xilinx interactive tools from the Design Manager Tools menu or from the toolbox. To launch a tool from the toolbox, click the appropriate toolbox button. See the “Toolbox” section of the “Menu Commands” chapter for a detailed explanation of the toolbox. The toolbox can be arranged in the ways described in the preceding section.

Status Bar

By default, the status bar appears at the bottom of the main window. When you select a menu command, a brief description of the command’s function appears in the status bar. As the software processes, status messages are dynamically updated and displayed.

Dialog Boxes

Many menu commands display dialog boxes in which you can enter information and set options.

Common Fields

The fields shown in the following table are common to most dialog boxes.

Table 2-1 Common Dialog Box Fields

Dialog Box Field	Function
OK	Closes the dialog box and implements the intended action according to the settings in the dialog box
Cancel	Closes the dialog box without effecting any action
Help	Displays information on that particular dialog box

Using Help

The Design Manager and Flow Engine contain context-sensitive help and a Help menu. You can obtain help on commands and procedures through the Help menus or by selecting the Help toolbar button. In addition, the dialog boxes associated with many commands have a Help button that you can click to obtain context-sensitive help.

Help Menu

Use the following Help menu commands to obtain help.

- The Help Topics command opens Help and lists the online help topics available. From the Contents page, you can jump to command information or step-by-step instructions. After you open Help, you can click the Help Topics button in the Help window whenever you want to return to the help topic list.
- The Online Documentation command provides access to the Software Manuals Online.

- The Xilinx on the Web command provides access to the support.xilinx.com page and the Xilinx home page on the Web.
- The About Design Manager command opens a popup window that displays the serial and version number of the Design Manager software and a copyright notice.
- The About Flow Engine command opens a popup window that displays the serial and version number of the Flow Engine software and a copyright notice.

Toolbar Help Button

You can obtain context-sensitive help from the toolbar as follows.

1. Click the Help button in the toolbar.

The cursor changes to a question mark.

2. With the left mouse button, click the menu item or toolbar button for which you want help.

Help appears for the selected command or option.

Note: You can also press **`Shift F1`** to obtain context-sensitive help.

F1 Key

Pressing the F1 key on a dialog box displays help on that dialog box. Pressing the F1 key is the same as selecting Help → Help Topics, if no dialog boxes are displayed.

Help Button in Dialog Boxes

Many of the dialog boxes have a Help button that you can click to obtain help for the dialog box with which you are working. You can also press **`Alt H`** on your keyboard while positioned over the dialog box to obtain help.

Chapter 3

Using the Design Manager and Flow Engine

This chapter shows you how to perform common design tasks in the Design Manager and Flow Engine. These procedures are described in the following sections.

- “Creating a New Project”
- “Creating a New Design Version”
- “Creating a New Implementation Revision”
- “Setting a Part”
- “Deleting Items from the Project View”
- “Specifying Implementation Flow Options”
- “Implementing a Design from the Design Manager”
- “Copying Constraints, Guide, and Floorplan File Data”
- “Viewing Reports”
- “Producing Timing Reports”
- “Generating Pin Locking Constraints”
- “Producing Timing Simulation Data”
- “Exporting Design Data”

Following are advanced procedures you can use after you are comfortable with the preceding basic procedures. The advanced procedures may help improve your runtime and design performance.

- “Implementing a Design from the Flow Engine”
- “Placing and Routing Non-Timing Driven Designs”
- “Running Multiple Place and Route Passes”

- "Running Re-Entrant Routing on FPGAs"
- "Working with Templates"

Note: Most commands run from the Design Manager require that an implementation revision be selected.

Creating a New Project

When you open the Design Manager for the first time, you must create a new project for your design before you can use the Design Manager. A project includes all design versions, implementation revisions, reports, and any other Xilinx data created while you work with a design.

The Design Manager graphically displays information about these items in the project view. When you create a new project, you specify a design to open and a directory for the project. You can create as many projects as you want, but you can only work with one at a time. The following procedure explains how to create a new project by importing a design.

1. In the Design Manager, select **`File`** → **`New Project`** or click the New Project toolbar button.

The dialog box shown in the following figure appears.

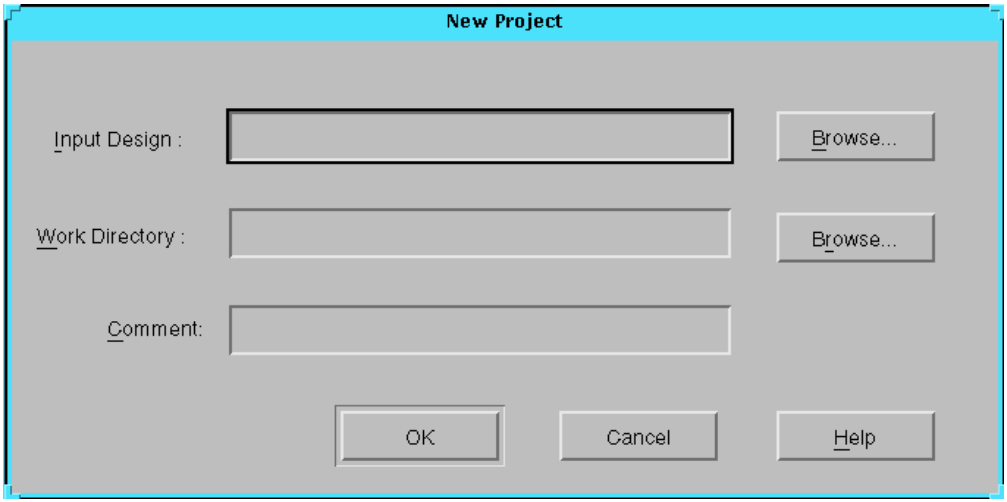


Figure 3-1 New Project Dialog Box

2. In the Input Design field, type the name of a design file to open, or click the **Browse** button to select a file from the Open dialog box. Use only the file formats listed in the "Inputs and Outputs" section of the "Introduction" chapter.

3. If you want to change the default work directory, type a path in the Work Directory field or use **Browse** to select a directory.

Note: The Design Manager automatically creates a subdirectory named xproj under the input design directory and uses it as the work directory. The Design Manager uses the xproj subdirectory to store all the data files for the project.

4. Enter any comments in the Comment field. Use this field to note options and strategies.

5. In the New Project dialog box, click **OK**.

   After your design is loaded, the Design Manager is configured for the loaded design.

Creating a New Design Version

While working on a project, you may need to modify the initial input design and bring these changes into an existing project in the Design Manager. You can do this with the New Version command. The

Design Manager automatically assigns a name for the design version, but you can enter a different name in the New Version dialog box. A new implementation revision is automatically created when you create a new version.

Note: When implementing your design, the New Version dialog box appears automatically if you made changes to your design netlist.

1. In the Design Manager, select **Design** → **New Version**.

   The dialog box shown in the following figure appears.

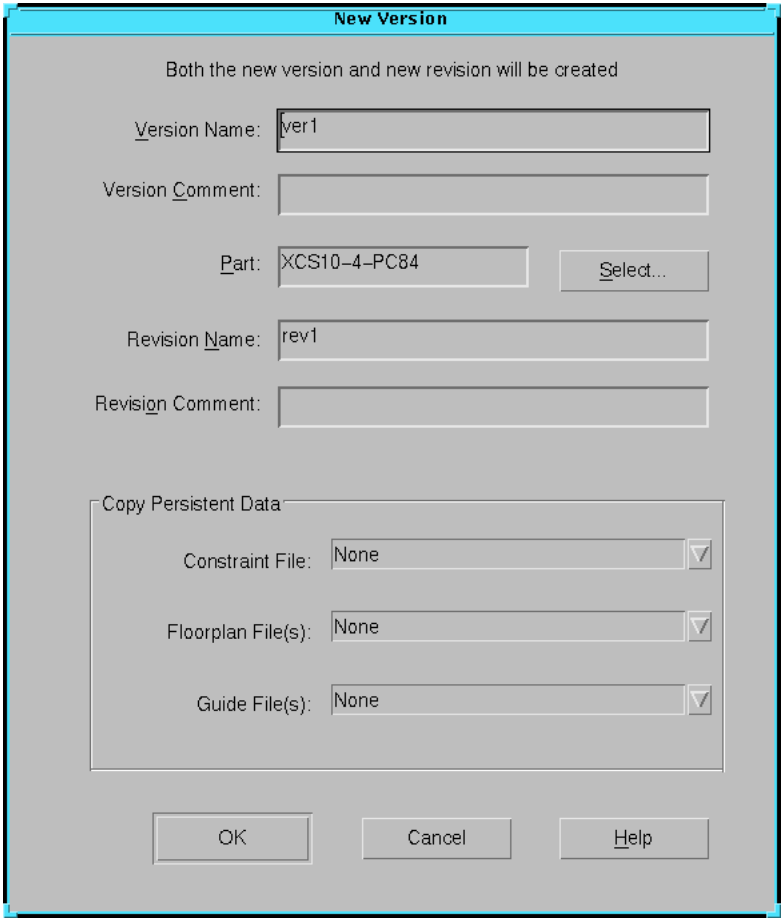


Figure 3-2 New Version Dialog Box

2. Enter a name in the Version Name field if you do not want to use the default name. Use the characters A through Z, a through z, 0 through 9, period (.), underscore (_), or hyphen (-) only. The name should be unique within the project.
3. Enter any comments in the Version Comment field. Use this field to note options and strategies.
4. To choose a device from the Part Selector, click **Select**.

   The dialog box shown in the following figure appears.

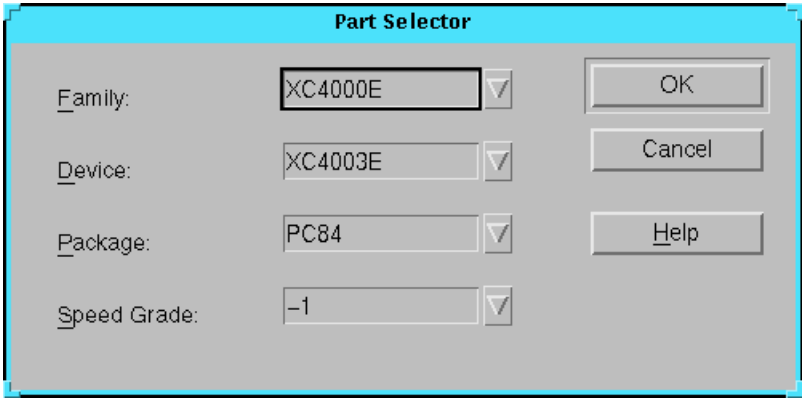


Figure 3-3 Part Selector

5. Specify the desired settings in the Family, Device, Package, and Speed Grade pulldown menus. For more information on these settings, see the "Part Selector Dialog Box" section of the "Menu Commands" chapter.
6. Click **OK**.
7. Enter the name for the new implementation revision in the Revision Name field. Use the characters A through Z, a through z, 0 through 9, period (.), underscore (_), or hyphen (-) only. The name should be unique within the design version.
8. Enter any comments in the Revision Comment field. Use this field to note options and strategies.
9. If you want to copy data to your new revision from another revision or from a custom file, use the settings in the **Copy Persistent Data** field. Select **None** if you do not want to copy data.

Note: By default, the Design Manager copies floorplan and constraints file data from the "last" revision. The "last" revision is the bottommost revision in the Design Manager project view. When initially creating a project, the Design Manager copies constraints file data from the project directory to the revision directory.

10. Click **OK** in the New Version dialog box.

    The Design Manager displays a new design version and implementation revision icon in the project view.

Creating a New Implementation Revision

After you create a design version, you can try different implementation strategies on that design. For instance, you can reduce area, increase speed, and vary placement effort. Each set of implementation strategies makes up a new implementation revision. Generating new implementation revisions allows you to vary how your design is implemented in order to achieve your design objectives.

You can select new options or target a new device to change the way your design is implemented. Targeting a new device allows you to try your design in various devices to determine the most suitable fit. For example, if a particular device proves to be too large or too slow for your needs, you can select a smaller or faster target device from a different family.

Note: If you are using an HDL flow, it is strongly recommended that you create a new synthesis netlist when you change FPGA or CPLD families. This ensures that the tools make the best use of the target device.

When you create an implementation revision, an implementation revision icon is placed in the Design Manager project view. Each time you create a new implementation revision, a default revision name and the part used in the "last" revision are automatically selected. If you want to change these default values, you can enter your own revision name and change the target part. The implementation revision name, implementation state, implementation status, and any user comments for the implementation revision are indicated next to its icon in the project view when you process the implementation. Replace or delete implementation revisions that are no longer useful.

1. In the Design Manager project view, select a design version icon.
2. Choose **Design** → **New Revision** from the Design Manager menu or click the New Revision toolbar button.

The dialog box shown in the following figure appears.

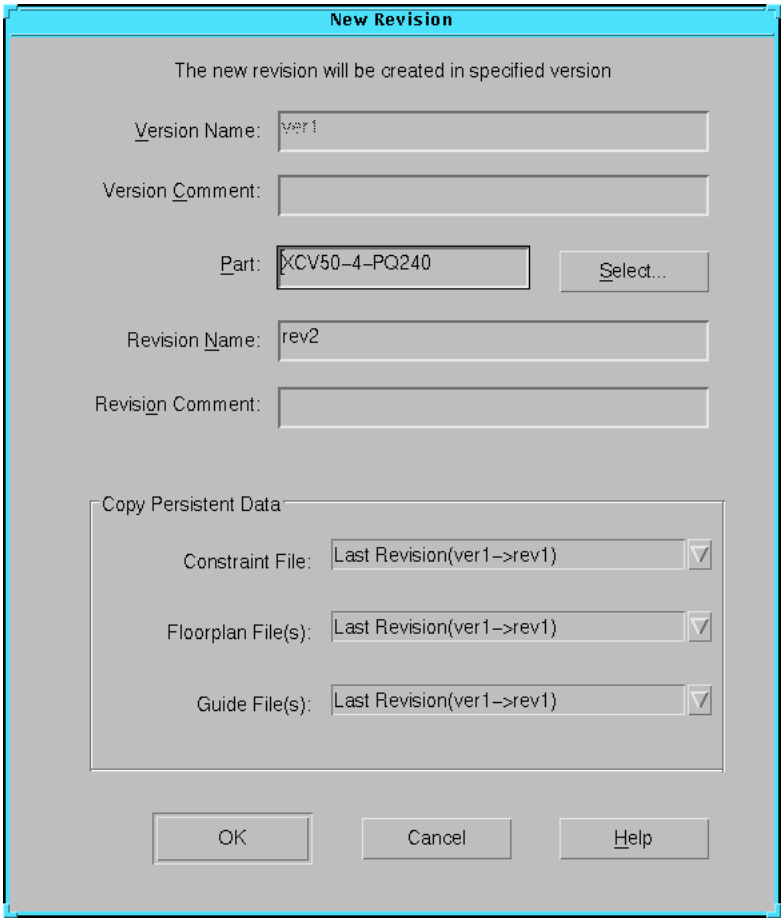


Figure 3-4 New Revision Dialog Box

3. To choose a device from the Part Selector, click **Select**.

   The dialog box shown in the following figure appears.

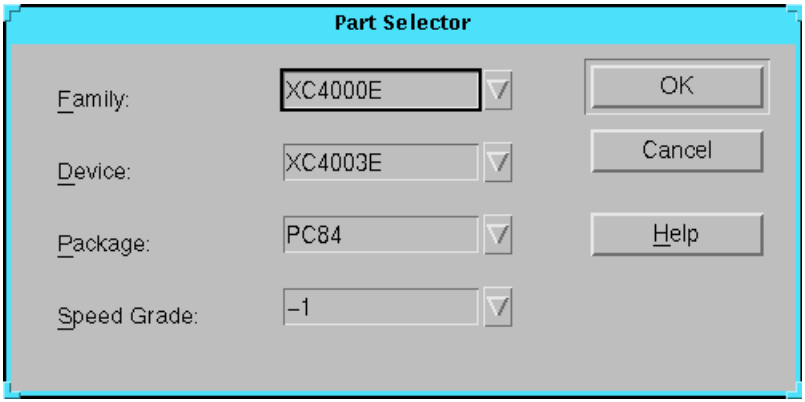


Figure 3-5 Part Selector

4. Specify the desired settings in the Family, Device, Package, and Speed Grade pulldown menus. For more information on these settings, see the "Part Selector Dialog Box" section of the "Menu Commands" chapter.
5. Click **OK**.
6. Enter the name for the new implementation revision in the Revision Name field. Use the characters A through Z, a through z, 0 through 9, period (.), underscore (_), or hyphen (-) only. The name should be unique within the design version.
7. Enter any comments in the Revision Comment field. Use this field to note options and strategies.
8. If you want to copy data to your new revision from another revision or from a custom file, use the settings in the **Copy Persistent Data** field. Select **None** if you do not want to copy data.

Note: By default, the Design Manager copies floorplan and constraints file data from the "last" revision. The "last" revision is the bottommost revision in the Design Manager project view. When initially creating a project, the Design Manager copies constraints file data from the project directory to the revision directory.

9. In the New Revision dialog box, click **OK**.

The Design Manager creates a new implementation revision and displays its icon in the project view.

Setting a Part

Use the Set Part command to set the part number for a new implementation revision. Changing the part number allows you to select the device best suited for your design.

Note: You cannot change the part number of an existing implementation revision.

1. Choose **Design** → **Set Part** from the Design Manager menu or click the Set Part toolbar button.

The dialog box shown in the following figure appears.

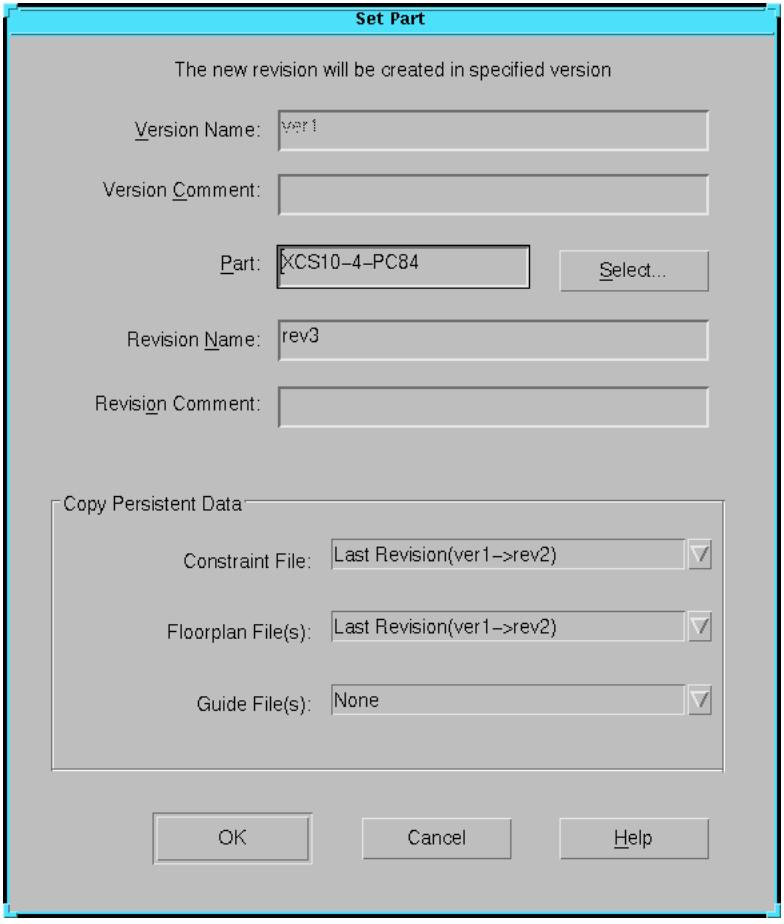


Figure 3-6 Set Part Dialog Box

2. Click **Select** to choose a device from the Part Selector.

   The dialog box shown in the following figure appears.

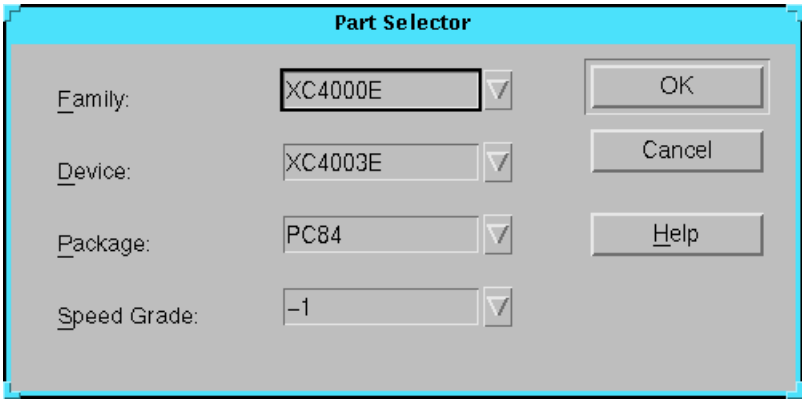


Figure 3-7 Part Selector

3. Specify the desired settings in the Family, Device, Package, and Speed Grade pulldown menus. For more information on these settings, see the "Part Selector Dialog Box" section of the "Menu Commands" chapter.
4. Click **OK**.
5. In the Set Part dialog box, click **OK**.

   The Design Manager displays the new implementation revision in the project view and the part number in the status bar.

Deleting Items from the Project View

Warning: When deleting an item from the project view, the Design Manager deletes the item and all accompanying data. Deleted data cannot be recovered.

Use the Delete command to delete a project, design version, or implementation revision from the project view.

1. In the Design Manager project view, select the icon of the project, design version, or implementation revision that you want to delete.
2. Select **Design** → **Delete**.
3. A confirmation box appears asking if you want to delete the selected item. Click **OK**.

Specifying Implementation Flow Options

You can specify options that control how the Flow Engine implements a design, configures a device, creates netlist files, and generates reports, timing data, and configuration data. The available options depend on the target device family.

You can specify these options by choosing settings within the Options dialog box. You can set implementation, simulation, and configuration options. The implementation options control how the software translates, maps, places, routes, and optimizes an FPGA design and how it translates and fits a CPLD design. The simulation options control the creation of netlists in terms of Xilinx primitives, allowing you to perform simulation and back-annotation. The configuration options define the initial configuration parameters of a device, the startup sequence, and readback capabilities. See the "Implementation Flow Options" chapter for information on each implementation, simulation, and configuration option.

Changes you make in the Options dialog box are applied to the implementation revision that was selected when you invoked the dialog box. The Flow Engine picks up changes after the currently running step is finished if a flow is running, or when you implement your design if no flow is running.

1. Open the Options dialog box using one of the following methods.
   - From the Design Manager, select **Design** → **Options**.
   - From the Flow Engine, select **Setup** → **Options**.
   - Click the Set Options toolbar button.

If you are targeting an FPGA, the dialog box shown in the following figure appears.

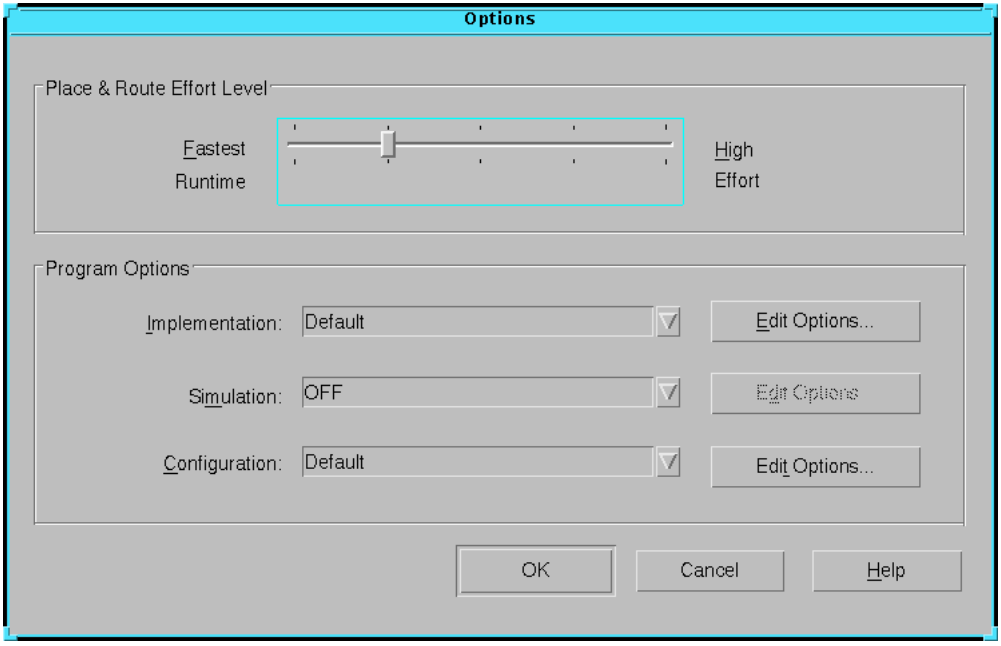


Figure 3-8 Options Dialog Box (FPGA)

If you are targeting a CPLD, the dialog box shown in the following figure appears.

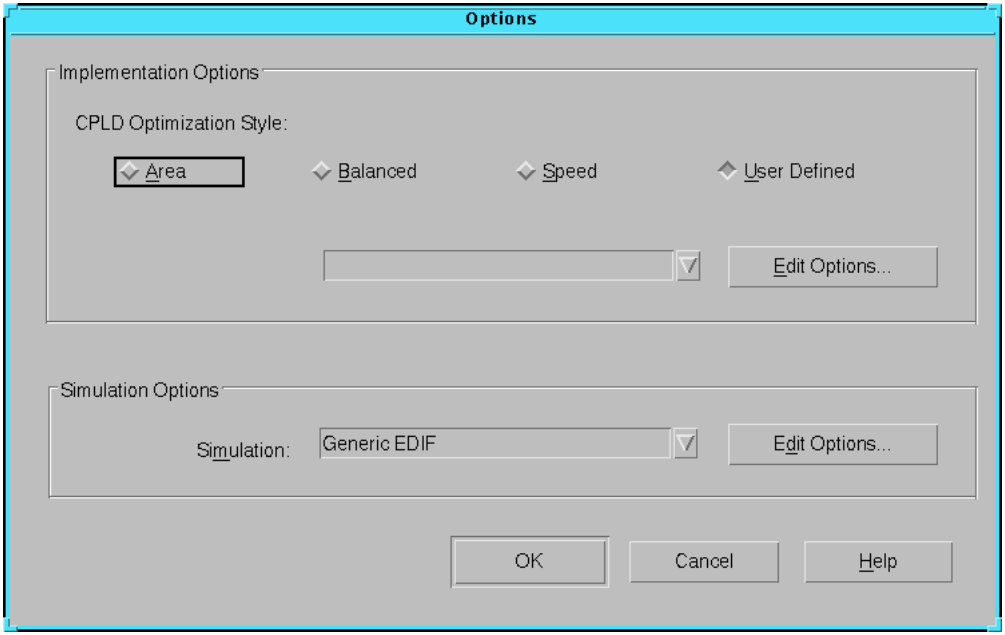


Figure 3-9 Options Dialog Box (CPLD)

2. If you are targeting an FPGA, do the following.

   a) Select a Place & Route Effort Level setting. A setting closer to High Effort provides better place and route results at the expense of longer run times.

   b) If you want to modify the default implementation options, click the **Edit Options** button to the right of the Implementation field. These options affect the Translate, Map, and Place&Route steps in the implementation flow.

   c) If you want to create timing simulation data, select one of the simulators in the drop-down list box next to the Simulation field. If you want to edit the default option settings, click the **Edit Options** button to the right of the Simulation field. Select **OFF** if you do not want to generate simulation data.

Note: The Edit Options button is disabled if you set Simulation to OFF.

d) If you want to modify the default configuration options, click the **Edit Options** button to the right of the Configuration field. These options affect the Configure step in the implementation flow. Select **OFF** if you do not want to generate configuration data.

Note: The Edit Options button is disabled if you set Configuration to OFF.

e) Click **OK**.

3. If you are targeting a CPLD, do the following.

a) In the Implementation Options field, select **Area**, **Balanced**, or **Speed** for the CPLD Optimization Style, or if you have your own option templates, select **User Defined** and select a template from the drop-down list. For information on creating your own templates see the "Working with Templates" section.

b) If you want to edit your User Defined options, click the **Edit Options** button. These options affect the Translate, Fit, and Bitstream steps in the implementation flow.

c) If you want to create timing simulation data, select one of the simulators in the drop-down list box next to the Simulation field. If you want to edit the default option settings, click the **Edit Options** button to the right of the Simulation field. Select **OFF** if you do not want to generate simulation data.

Note: The Edit Options button is disabled if you set Simulation to OFF.

d) Click **OK**.

4. Click **OK** to maintain your settings and exit the Options dialog box.

Implementing a Design from the Design Manager

You can implement your design in an automatic step from the Design Manager. When you implement your design automatically, the Flow Engine implements your design to completion.

You can implement your design with default values set for copying guide, floorplan, and constraint file data and default values for implementation flow options, or you can set your own values. If you

want to set your own values, follow the procedures described in the "Specifying Implementation Flow Options" and "Copying Constraints, Guide, and Floorplan File Data" sections before implementing your design.

Implementing a Design Automatically

The following procedure describes how to implement a design automatically from the Design Manager.

1. Select **Design** → **Implement** or click the Implement toolbar button.

   One of the following occurs.

   - If you altered your source design, the software opens the New Version dialog box. See the "Creating a New Design Version" section for information on setting the options in this dialog box.

     The Design Manager creates a new version and revision and the Flow Engine implements this new revision.

   - If you did not alter the source design or part type, the Smart Flow Engine appears and implements your design starting with the appropriate step.

   When processing is complete, the Smart Flow Engine closes and the Implement Status dialog box appears.

Note: The Flow Engine is run on the "last" revision regardless of the currently selected revision. To implement a revision other than the "last" one, follow the procedure in "Re-Implementing a Design."

2. In the Implement Status dialog box, click **Reports** to view the reports generated by the Flow Engine or click **View Log File** to view the implementation log file.

Note: At this point you can also perform timing simulation, if you set options as described in the "Producing Timing Simulation Data" section, and program the device. Timing simulation is described in

the interface user guide for your system. Device programming is described in the programmer user guide for your system.

Re-Implementing a Design

If you want to automatically implement an implementation revision that is *not* your "last" revision, use the following procedure.

1. Select an implementation revision.
2. Right-click on the revision.
3. Select **`Re-Implement`**.

   The Flow Engine determines where it should start running in the flow and implements your revision to completion.

Copying Constraints, Guide, and Floorplan File Data

You can copy constraints, guide, and floorplan file data to an existing implementation revision. Copy this data to your implementation revision to control the implementation of your design. Specify the data you want to copy using the Design Manager. The following sections describe how to copy this data to an existing revision.

- "Setting a Constraints File"
- "Setting a Guide File"
- "Setting Floorplan Files"

Note: The following procedures describe how to copy data to an existing implementation revision. If you want to copy data to a new design version or implementation revision, use the Copy Persistent Data option described in the "Creating a New Design Version" or "Creating a New Implementation Revision" section.

Setting a Constraints File

You can use a user constraints file (*design_name*.ucf) to control the implementation of your design. The user constraints file can contain information on where to place I/O pins and blocks of logic and timing requirements for the design.

If you want to control the implementation of your design with a user constraints file, you can specify this file in the Set Constraints File

dialog box. The software tries to implement your design to meet the specified timing requirements and other constraints.

1. In the Design Manager, select **Design** → **Set Constraints File** to open the dialog box shown in the following figure.

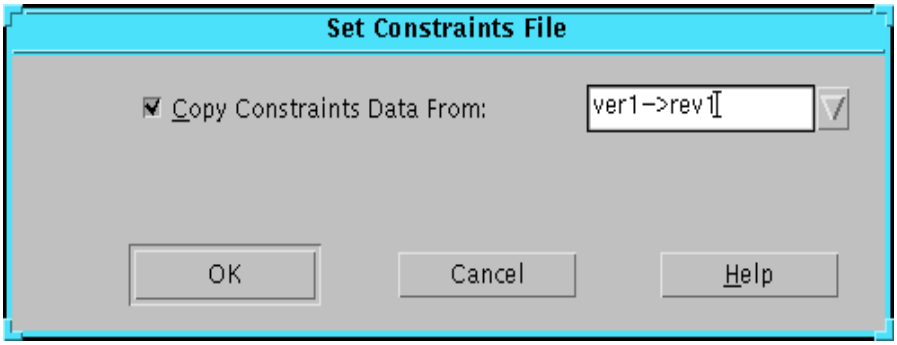


Figure 3-10 Set Constraints File Dialog Box

2. Make sure **Copy Constraints Data From** is selected.
3. In the drop-down list box, choose one of the following.
   - A revision that contains the user constraints file (UCF) you want to use for this implementation
   - **None** if you do not want to copy constraints data
   - **Custom** to guide from a specific file

     If you select **Custom**, the following dialog box appears. Type the name of a specific file in the Constraints File field, or click **Browse** to open a file selection dialog box in which you can choose an existing UCF file.

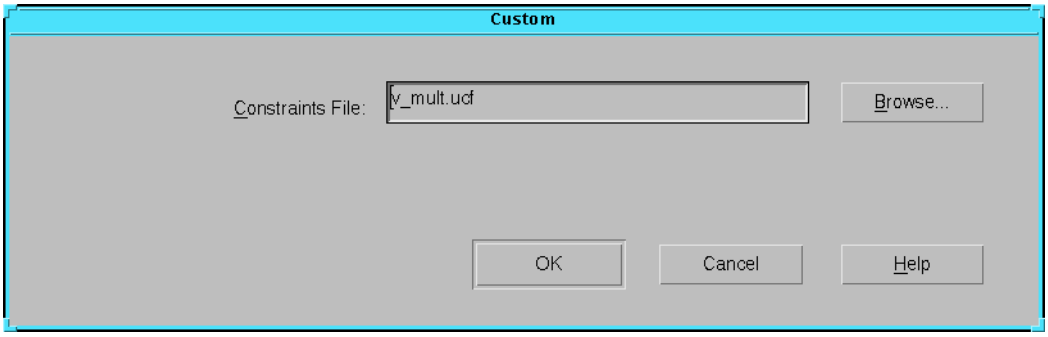


Figure 3-11 Set Constraints File Custom Dialog Box

4. In the Set Constraints File dialog box, click **OK**.

   When you implement the design, the Flow Engine uses the copied data to constrain the implementation.

Setting a Guide File

You can select a previously routed or fitted implementation revision or a guide file to use as a guide for implementation. The procedure for guiding your implementation is the same for FPGAs and CPLDs. However, the way the design is guided differs between the two.

When guiding an FPGA design, the software attempts to use the guide for placing logic and routing signals for the current implementation revision of the design. This can reduce the amount of time the software takes to place and route. Guiding a design for an FPGA works as follows.

- If a component in the new design has the same name as that of the guide design or file, it is placed as in the guide.
- If an unnamed component in the new design is the same type as a component within the guide, it is placed as in the guide.
- If the signals attached to a component in the new design match the signals attached to the component of the guide, the pins are swapped to match the guide, where possible.
- If the signal names in the input design match the guide, and have the same sources and loads, the routing information from the guide design is copied to the new design.

After these components and signals are placed and routed, the remainder of the logic is placed and routed. If you have made only minor changes to your design and want the remaining logic placed and routed exactly as in your guide design, select the Match Guide Design Exactly option. This option locks the placement and routing of the matching logic so that it cannot change to accommodate additional logic.

Note: Setting the Match Guide Design Exactly option is not recommended for synthesis based designs.

For CPLDs, each time you implement your design, a guide file is created (*design_name*.gyd) which contains your pinout information. You can reuse this file in subsequent iterations of your design if you want to keep the same pinouts. If you select a valid implementation revision or guide file name, the pinouts from that file will be used when the design is processed.

Note: You can override guide file locations by assigning locations in your design file or constraints file.

1. In the Design Manager, select **`Design`** → **`Set Guide File(s)`** to open the dialog box shown in the following figure.

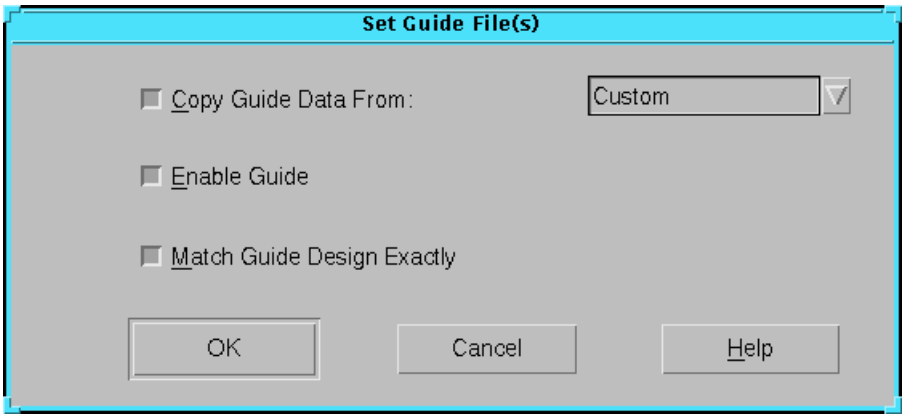


Figure 3-12 Set Guide File(s) Dialog Box

2. Make sure **`Copy Guide Data From`** is selected.
3. In the drop-down list box, choose one of the following.
   - A revision that contains the guide file you want to use for this implementation

- **None** if you do not want to copy a guide file
- **Custom** to guide from any mapped or routed file for FPGAs or fitted file for CPLDs, including designs not generated from within the Design Manager

  If you select **Custom**, the following dialog box appears. Type the name of a mapped, routed, or fitted file in the Guide File field, or click **Browse** to open a file selection dialog box in which you can choose an existing file. Choose an NCD file for FPGAs or a GYD file for CPLDs. You can also specify a mapping guide file for FPGAs.

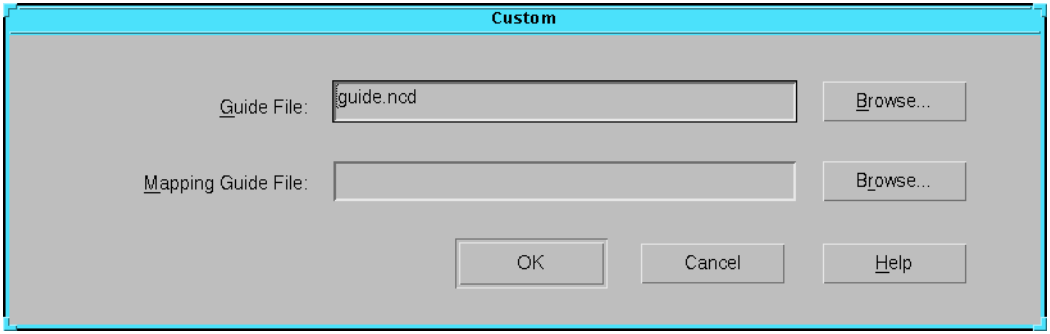


Figure 3-13 Set Guide File(s) Custom Dialog Box

Note: The implementation revision or revision data is based on a placed and routed design. Guide from a placed and routed file rather than a mapped file to reduce runtime. To guide from a mapped file, you must use the Custom option. If you use this option, you cannot guide mapping using the Set Floorplan File(s) command. Guided mapping is not supported for Virtex devices.

4. In the Set Guide File(s) dialog box, make sure **Enable Guide** is selected.

   By default, this option is enabled and instructs the software to use the specified guide file. If you do not want to guide your design but want to keep your guide file intact, disable this option.

5. For FPGA devices, select **Match Guide Design Exactly** if you want to lock the placement and routing of matching logic.

   If you do *not* select this option, the guide files are used as a starting point only. This allows the mapper, placer, and router

greater flexibility in accommodating design modifications, often resulting in greater overall success.

Note: For synthesis-based designs, use the Match Guide Design Exactly option only if the guide file is from the same design version.

6. Click **OK**.

   When you implement the design, the Flow Engine uses the copied data to guide the implementation.

Setting Floorplan Files

When you use the Floorplanner, an MFP file is generated that contains mapping information. You can instruct the Design Manager to use this file as a guide for mapping an implementation revision using the Set Floorplan File(s) command. To use this command, you must select an implementation revision that has been mapped and modified using the Floorplanner. For information on using the Floorplanner, see the *Floorplanner Guide*.

Note: If you use the Set Floorplan File(s) command you cannot guide mapping using the Set Guide File(s) command Custom option. The Set Floorplan File(s) command is available for the XC4000, Virtex, Spartan, and Spartan2 device families only.

1. From the Design Manager, select **Design** → **Set Floorplan File(s)** to open the dialog box shown in the following figure.

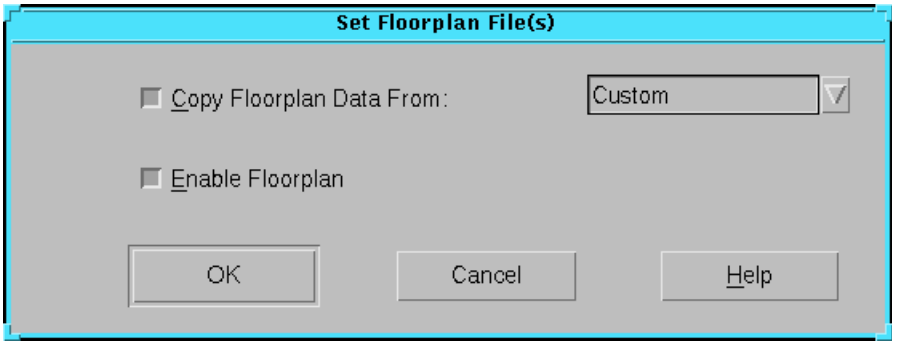


Figure 3-14 Set Floorplan File(s) Dialog Box

2. Make sure **Copy Floorplan Data From** is selected.
3. In the drop-down list box, choose one of the following.

- A revision that contains the floorplan files you want to use for this implementation
- **None** if you do not want to copy floorplan data
- **Custom** to guide from any mapped file in your file system, including designs not generated from within the Design Manager

  If you select **Custom**, the following dialog box appears. Type the name of a specific file in the Floorplanning File field, or click **Browse** to open a file selection dialog box in which you can choose an existing file. Specify an FNF file for the Floorplanning File field and an MFP file for the Floorplanned Guide File field.

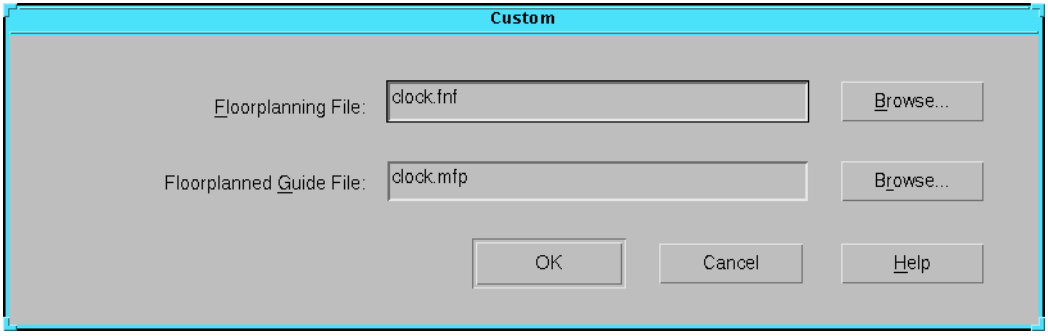


Figure 3-15 Set Floorplan File(s) Custom Dialog Box

4. In the Set Floorplan File(s) dialog box, make sure **Enable Floorplan** is selected.

Note: By default, this option is enabled and instructs the software to use the specified floorplan file. If you do not want to guide your design but want to keep your floorplan file intact, disable this option.

5. Click **OK**.

   The Flow Engine uses the copied data to guide the implementation.

Viewing Reports

The Flow Engine generates various reports which you can view in the Report Browser. The Report Browser opens reports for the selected implementation revision.

1. Select **`Utility`** → **`Report Browser`** or click the Browse Reports button.

   The Report Browser window opens and displays reports for the active implementation revision.

2. In the Report Browser window, double-click the report icon for the report you want to view.

   The report is displayed in the standard text editor that you specified with the **`File`** → **`Preferences`** command.

Note: The icons change appearance to indicate whether or not you have read a report. A yellow mark in the upper left corner of the report icon indicates that the report has been generated but not read. A report icon without this mark indicates that the report has been generated and read.

Producing Timing Reports

You can generate timing reports after you implement your design using the Produce Timing Reports command. You can use this command if Map for FPGAs or Fit for CPLDs has completed successfully. The timing report created is based on the state of your design when you run the command.

Note: If you select the appropriate options in the Timing Reports tab of the Implementation Options dialog box before you implement your design, the software automatically generates timing reports with the Map and Place&Route steps. See the “Specifying Implementation Flow Options” section for information on making settings in the Implementation Options dialog box.

1. Select **`Utilities`** → **`Produce Timing Reports`**.

   The following dialog box appears if you are targeting an FPGA.

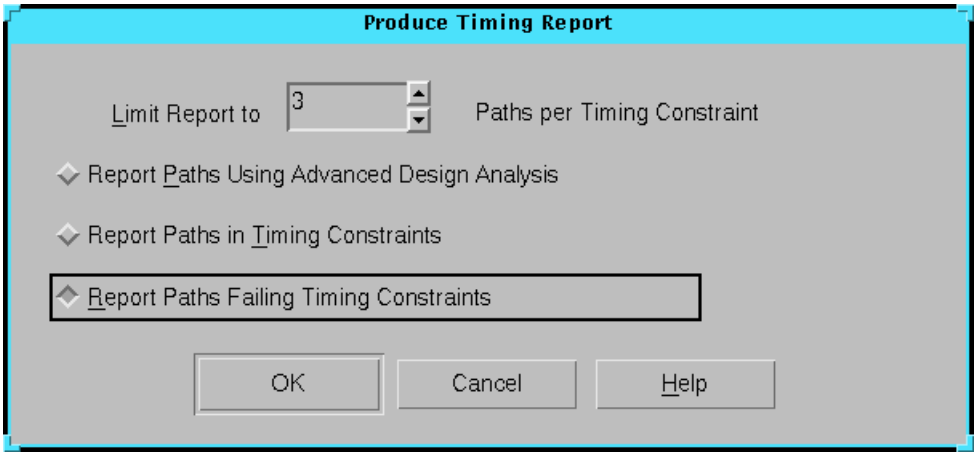


Figure 3-16 Produce Timing Reports Dialog Box (FPGA)

The following dialog box appears if you are targeting a CPLD.

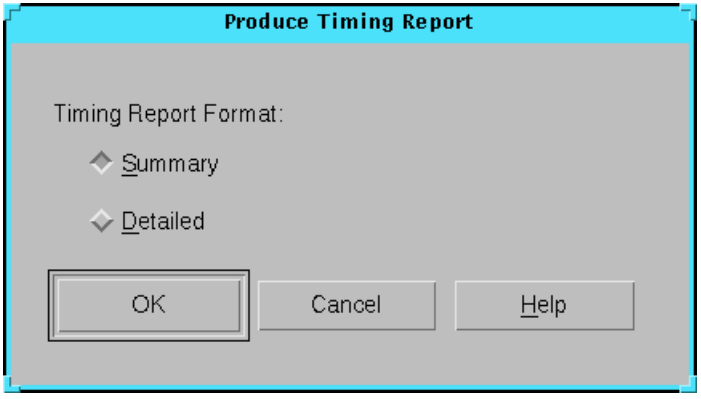


Figure 3-17 Produce Timing Reports Dialog Box (CPLD)

2. Select a timing report format. For information on these formats, see the “Produce Timing Report Dialog Box (FPGA)” or “Produce Timing Report Dialog Box (CPLD)” section of the “Menu Commands” chapter.

The timing report is created and placed in the Report Browser. See the "Viewing Reports" section for information on viewing reports.

Generating Pin Locking Constraints

You can generate pin locking constraints in your UCF file for use with other Xilinx implementation tools. Pinout information is taken from a placed NCD file for FPGAs or a fitted GYD file for CPLDs.

1. In the Design Manager, select **Design** → **Lock Pins**.
2. In the confirmation dialog box, click **Yes**.

   Pin locking constraints that you created with this command are added to your UCF file in the PINLOCK section.
3. After the constraints are added, the dialog box shown in the following figure appears. Click **View Lock Pins Report** to view the report.

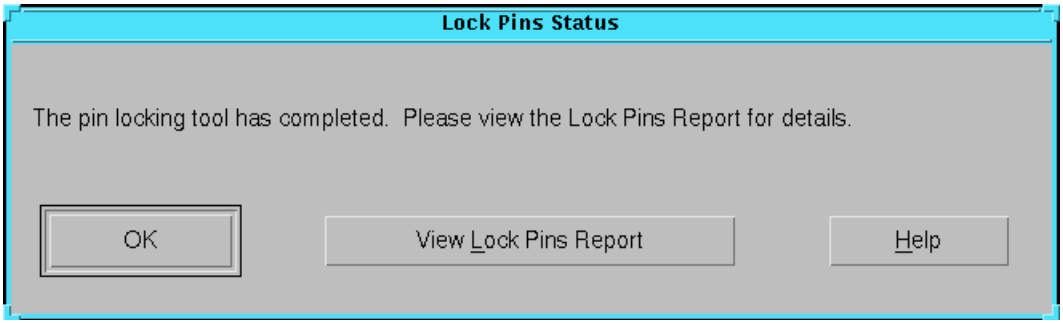


Figure 3-18 Lock Pins Status Dialog Box

You can view the pinouts using the Constraints Editor. See the *Constraints Editor Guide* for more information.

Note: If you want to view the report after you have dismissed the Lock Pins Status dialog box, use the **Utilities** → **Lock Pins Report** from the Design Manager.

Producing Timing Simulation Data

The Flow Engine can produce timing simulation data for use in a third party simulation tool. This data is produced for the selected implementation revision.

1. Open the Options dialog box using one of the following methods.
   - From the Design Manager, select **`Design`** → **`Options`**.
   - From the Flow Engine, select **`Setup`** → **`Options`**.
   - Click the Set Options toolbar button.

If you are targeting an FPGA, the dialog box shown in the following figure appears.

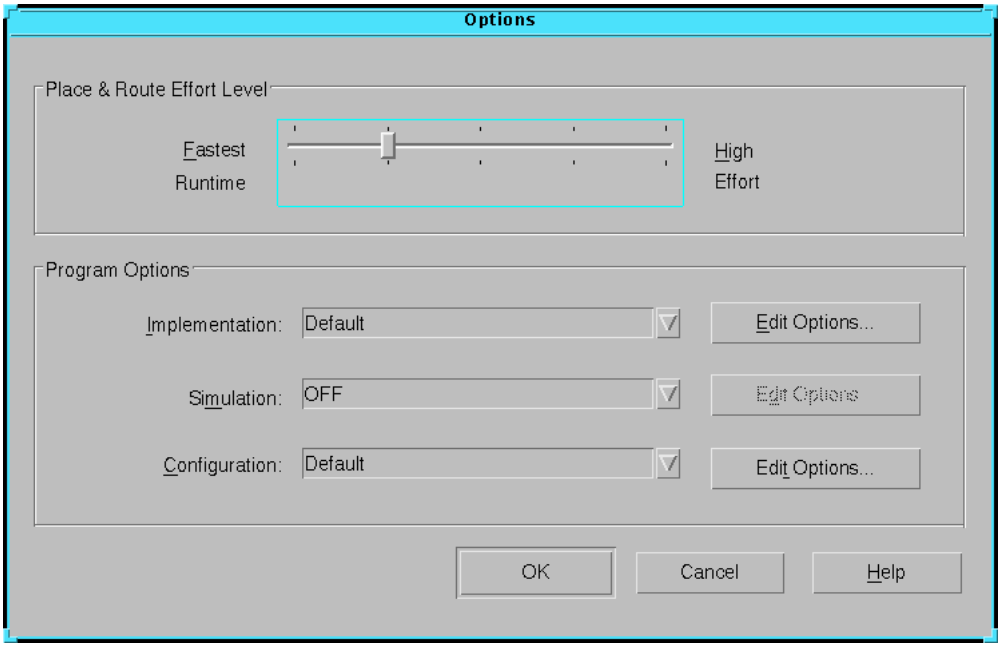


Figure 3-19 Options Dialog Box (FPGA)

If you are targeting a CPLD, the dialog box shown in the following figure appears.

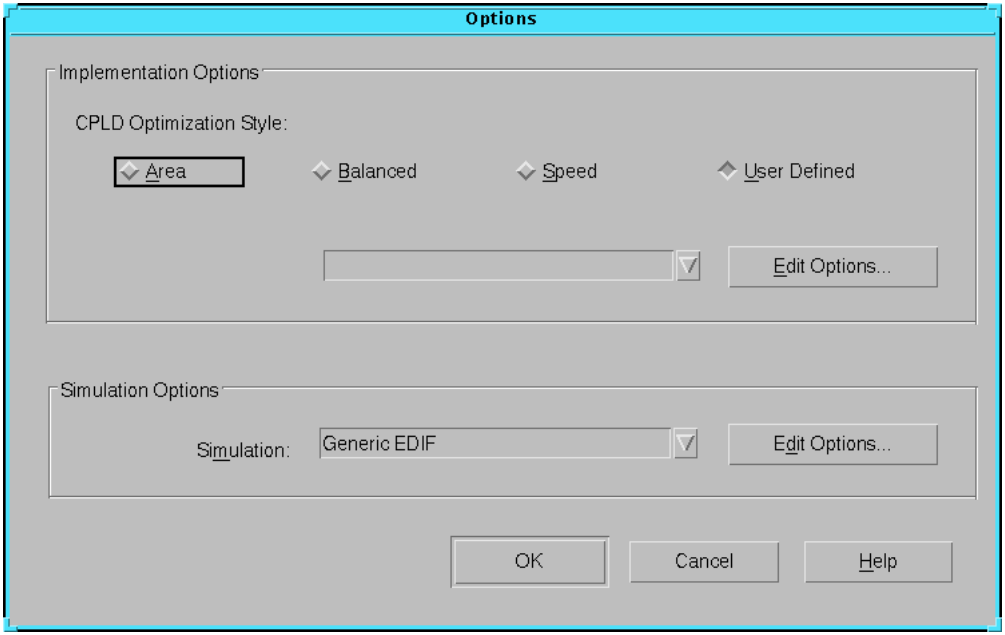


Figure 3-20 Options Dialog Box (CPLD)

2. Select one of the simulators in the drop-down list box next to the Simulation field.
3. If you want to edit the default option settings, click the **Edit Options** button to the right of the Simulation field.

Note: If you set Simulation to OFF, no timing simulation data is created and the Edit Options button is disabled.

4. Make settings in the Simulation Options dialog box and click **OK**. See the "Implementation Flow Options" chapter for information on each simulation option.
5. Click **OK**.

   When you implement the design, the Flow Engine produces timing simulation data files. Each time the data is produced, it is automatically exported to your design directory. You can use

these files to simulate the design with a supported third party simulation tool.

Exporting Design Data

You can export design data created in the Design Manager to other environments. The Design Manger exports design data for the selected implementation revision.

1. In the Design Manager, select **Design** → **Export** to open the dialog box shown in the following figure.

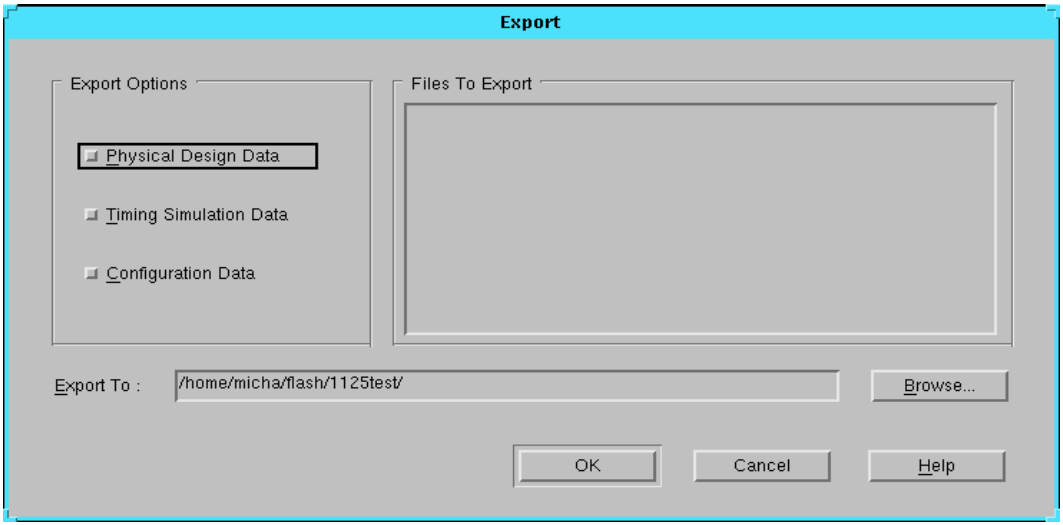


Figure 3-21 Export Dialog Box

2. In the Export Options field, select the type or types of data to export, whether **Physical Design Data**, **Timing Simulation Data**, or **Configuration Data**.

   The associated files appear in the Files to Export field.

3. Enter a directory path in the Export To field or click **Browse** to browse for a directory.

4. Click **OK**.

Implementing a Design from the Flow Engine

If you want to control the implementation processes, you can implement your design in separate steps from the Flow Engine. Implementing your design from the Flow Engine allows you to control aspects of the flow such as updating the implementation status, enabling flashing icons, and setting run targets. You can implement your design with default implementation flow options set, or you can set your own values. This section contains the following procedures.

- "Implementing a Design in Separate Steps"
- "Setting the State of the Flow"
- "Enabling Flashing Icons"
- "Setting a Run Target"
- "Updating the Flow"

Implementing a Design in Separate Steps

The following procedure describes how to implement your design in separate steps. Follow this procedure according to how you want to implement your design.

1. If you want to set implementation flow options or specify constraint, floorplan, and guide file data for copying, follow the procedures in the "Specifying Implementation Flow Options" and "Copying Constraints, Guide, and Floorplan File Data" sections.
2. If you want to set a run target, enable flashing icons, or update the implementation status or flow, use the procedures in the following sections.
3. Do one of the following.
   - In the Flow Engine window, select **Flow** → **Run** to run through the entire implementation process.
   - Select **Flow** → **Step** to single step through the implementation process.

Note: If you stop processing while the Flow Engine is running the Place&Route step, the Flow Engine asks whether you want to save

the data that has processed to this point or exit immediately without saving the data.

Setting the State of the Flow

Use the Advanced command in the Flow Engine Setup menu to set the state of the implementation flow.

Note: This procedure is not used in normal Flow Engine use. It is used if some processing on the design was performed outside of the Design Manager or Flow Engine, such as in the FPGA Editor. It can also be used if you ran the Flow Engine Step Back button by mistake and want to reset the implementation state to its original state.

1. Select **Setup** → **Advanced** to open the dialog box shown in the following figure.

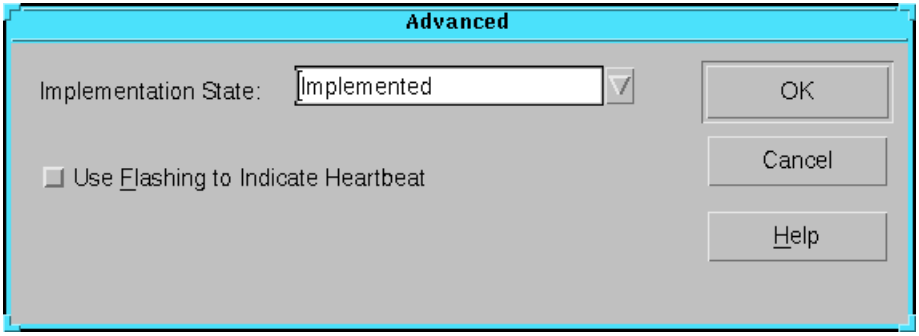


Figure 3-22 Advanced Dialog Box

2. Select a state from the Implementation State list box to update the Design Manager and Flow Engine as to which implementation state was last completed.
3. Click **OK**.

Enabling Flashing Icons

You can enable flashing icons to indicate that a process step is being processed. A trade-off of this feature is that flashing icons slow down the implementation process.

1. Select **Setup** → **Advanced** to open the Advanced dialog box shown in the preceding figure.
2. Select **Use Flashing to Indicate Heartbeat**
3. Click **OK**.

Setting a Run Target

The Flow Engine flow includes several process steps. You can specify that the flow stop at a certain point with the Stop After command. When specified, the Flow Engine does not process beyond that point. You do not need to set a run target for typical Flow Engine use. By default, the Flow Engine processes all the steps.

1. Select **Setup** → **Stop After** or click the Set Target toolbar button.

The dialog box shown in the following figure appears.

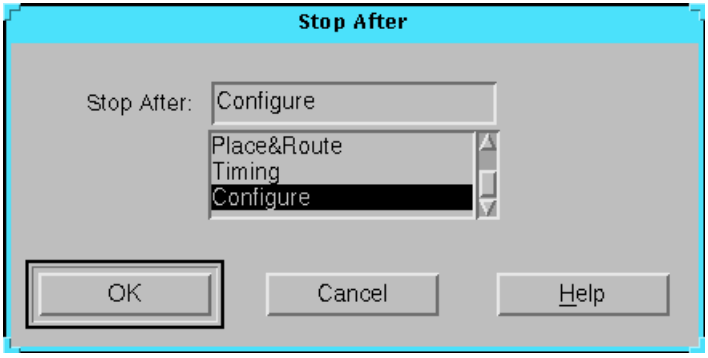


Figure 3-23 Stop After Dialog Box

2. Select the desired run target from the Stop After drop-down list box.
3. Click **OK**.

   The Flow Engine stops processing after the specified point. A red stop sign visually indicates the run target.

Updating the Flow

When the Flow Engine is first invoked, it automatically looks for changes made to certain files. If changes are detected, the Flow Engine resets the flow for the implementation revision. For information on which file changes cause the flow to be reset, see the "Smart Flow Engine" section of the "Introduction" chapter. If you want to check for changes and the Flow Engine is already open, use the Setup → Update Flow command.

1. Select **Setup** → **Update Flow**.

   The Flow Engine resets the flow if certain file changes are detected.

2. Do one of the following.

   - In the Flow Engine window, select **Flow** → **Run** to run through the entire implementation process.
   - Select **Flow** → **Step** to single step through the implementation process.

Placing and Routing Non-Timing Driven Designs

When targeting the Virtex and Spartan2 device families on designs that are run without timing constraints, you may notice lower design performance results from the Place and Route process. To get a more realistic estimate of how your design will perform without timing constraints applied, do the following.

1. In the Flow Engine, set your run target to Place&Route.

   See the "Setting a Run Target" section for more information.

2. Select **Flow** → **Run**.

3. After the Flow Engine has finished routing your design, select **Setup** → **FPGA Re-entrant Route** to open the dialog box shown in the following figure.

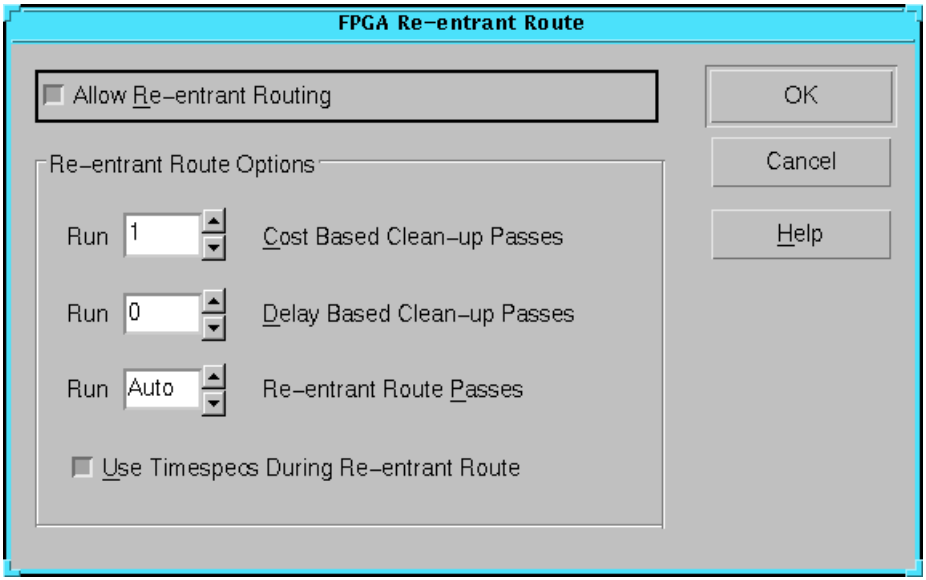


Figure 3-24 FPGA Re-entrant Route Dialog Box

4. Specify the number of Clean-up Passes to run. For information on clean-up passes, see the "FPGA Re-entrant Route Dialog Box" section of the "Menu Commands" chapter.
5. Click **OK**.
6. Select **Flow** → **Step Back**.
7. Select **Flow** → **Run**.
8. Check the P&R Report and Post Layout Timing Report in the Report Browser for improved performance results. See the "Viewing Reports" section for information on viewing the report.

Running Multiple Place and Route Passes

Running multiple place and route passes allows you to automatically generate multiple place and route solutions for a design. The Place and Route process offers both the ability to generate a determinate,

repeatable solution by using the same starting point, or cost table, and the ability to generate a range of unique solutions by using different cost tables.

The FPGA Multi-Pass Place & Route command automates the ability to run Place and Route several times with different cost tables. It scores each place and route pass and uses the score to determine the best passes to save. Scores are based on factors such as the number of unrouted nets, the delays on nets, and conformity to your timing constraints. The passes you save appear as implementation revisions in the Design Manager project view.

On average, design speed from an arbitrary multiple pass place and route will vary plus or minus 5 to 10% from the median design speed across all cost tables. About 1/3 of the cost tables will result in speeds within 5% of the median, 1/3 in the 5 to 10% range, and 1/3 in the 10-15% range. When comparing performance from the absolute worst cost table to the absolute best, a spread of 25 to 30% is possible.

Note: Ranges are narrower for Virtex devices and higher for XC4000 devices.

Use the FPGA Multi-Pass Place & Route command in the following situations.

- You want to evaluate whether worse than expected results are due to a poor starting point or cost table.

  In this case, run multiple place and route passes at any time during the design cycle by running 3 or 4 cost tables.

- You made small changes to a design at the end of the design cycle and performance falls 5 to 10% as a result of these changes.

  In this case, run 5 to 10 cost tables.

If you are working on a workstation, you can use the Nodelist File option to execute the place and route process on multiple machines. This significantly reduces the run time.

Note: The FPGA Multi-Pass Place & Route command is supported for the FPGA device families only. Using the FPGA Multi-Pass Place & Route command is not recommended for every design iteration. If you need the top performing cost tables to meet design performance, your design should be modified to remove one or more logic levels.

1. In the Design Manager, select **Design** → **FPGA Multi-Pass Place & Route** to open the dialog box shown in the following figure.

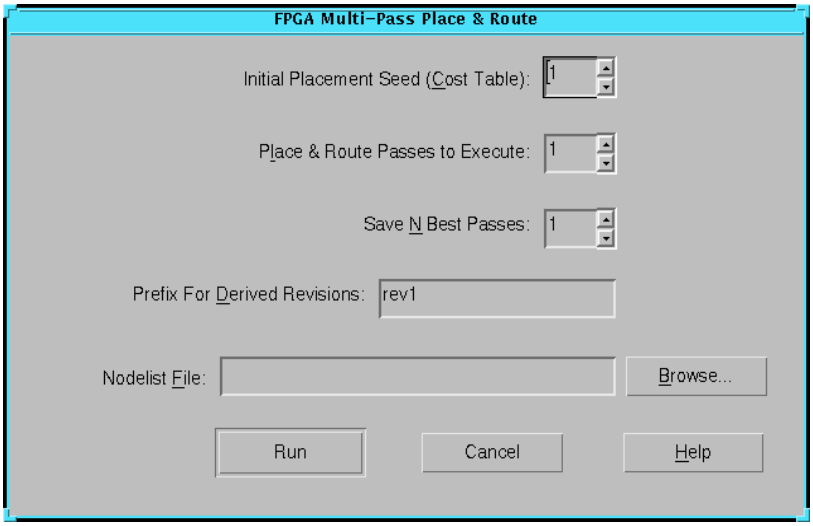


Figure 3-25 FPGA Multi-Pass Place & Route Dialog Box

The options in this dialog box are described in the "FPGA Multi-Pass Place & Route Dialog Box" section of the "Menu Commands" chapter.

2. In the Initial Placement Seed (Cost Table) field, specify a placement initialization value.

   The placement initialization value sets the number with which to begin the place and route attempts. Each pass receives an incremental value. The value you choose corresponds to a cost table index which initializes the place and route algorithms.

3. In the Place & Route Passes to Execute field, specify the number of place and route passes to attempt.

4. In the Save N Best Passes field, specify the number of place and route passes to save.

   The software saves the best passes based on the iteration design scores.

5. If you want to change the default prefix of the pass names, enter a new name in the Prefix for Derived Revisions field. The default prefix is rev#.

6. If you are working on a workstation, you can click the Nodelist File **Browse** button to choose a nodelist file that you generated.

   This file allows you to use multiple machine (nodes) that are networked together to run the place and route passes. For more information on generating a nodelist file and setting up environment variables, see the "Turns Engine (PAR Multi-Tasking Option)" section of the *Development System Reference Guide*.

7. In the FPGA Multi-Pass Place & Route dialog box, click **Run**.

   The Design Manager creates implementation revisions for the number of passes you specified in the Save N Best Passes field. After the passes are complete, the dialog box shown in the following figure appears. Click **View Log File** to view the log file or click **View Summary Report** to view the summary report.

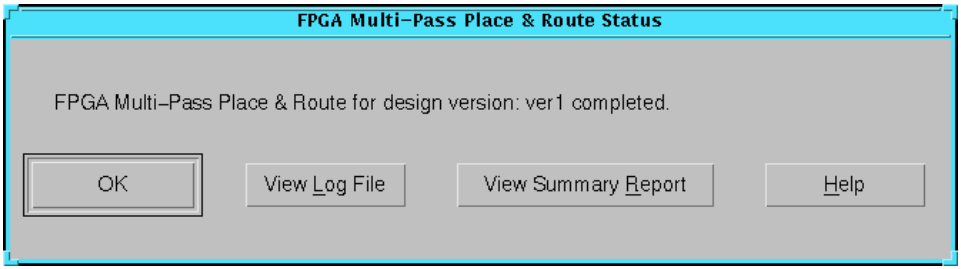


Figure 3-26 FPGA Multi-Pass Place & Route Status Dialog Box

Running Re-Entrant Routing on FPGAs

Use re-entrant routing to further route an already routed design. The design maintains its current routing and additional routing is added.

You can reroute connections by running cost-based cleanup, delay-based cleanup, and additional re-entrant route passes. Cleanup passes attempt to minimize the delays on all nets and decrease the number of routing resources used. Cost-based cleanup routing is faster while delay-based cleanup is more intensive.

Re-entrant routing offers the following advantages.

- Cleanup passes significantly reduce delays, especially on non-timing driven runs.
- For timing-driven runs, cleanup passes can improve timing on elements not covered by timing constraints.
- For designs which do not meet timing goals by a narrow margin, delay-based cleanup passes can reorganize routing so that additional re-entrant route passes enable the design to meet timing goals.

Note: The FPGA Re-entrant Route command is supported for the FPGA device families only.

1. In the Flow Engine, select **Setup** → **FPGA Re-entrant Route** to open the dialog box shown in the following figure.

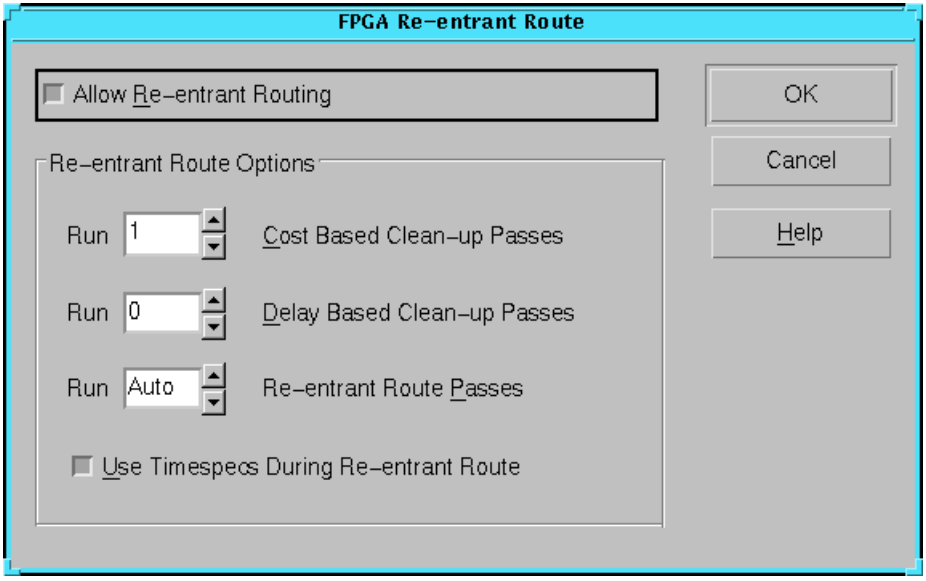


Figure 3-27 FPGA Re-Entrant Route Dialog Box

2. Select **Allow Re-entrant Routing** to route the previously routed design again.
3. Select a number between 1 and 5 for the **Run _ Cost-Based Cleanup Passes** field.

These cleanup passes reroute nets if the new routing uses less costly resources than the original configuration. Cost is based on pre-determined cost tables. Cost-based cleanup usually has a faster runtime than the delay-based cleanup, but does not reduce delays as significantly.

Note: If you run both cost-based and delay-based cleanup passes, the cost-based passes run first.

4. Select a number between 1 and 5 for the **Run _ Delay-Based Cleanup Passes** field.

   These cleanup passes reroute nets if new routing will minimize the delay for a given connection. Delay-based cleanup usually produces faster in-circuit performance.

5. Select a number between 1 to 2000 for the **Run _ Re-entrant Route Passes** field to run additional re-entrant routing passes.

   These passes are either timing driven or non-timing driven depending on whether you specified timing constraints.

6. Select **Use Timespecs During Re-entrant Route** if you want to reroute the design within the specified timing constraints in your design file.

7. Click **OK**.

Working with Templates

An option template is a group of implementation flow option settings. Instead of setting options each time you create an implementation revision, templates provide a convenient way to have several groups of option settings that you can select from when you implement a design. For example, you can have a template for quick place and route and another one for maximum placement effort.

Note: If you want to set the implementation flow options without using templates, follow the procedure in the “Specifying Implementation Flow Options” section.

The three types of option templates are implementation, simulation, and configuration templates. The implementation templates control how the software translates, maps, places, routes, and optimizes an FPGA design and how it translates and fits a CPLD design. The simulation templates control the creation of netlists in terms of Xilinx

primitives, allowing you to perform simulation and back-annotation. The configuration templates set options which define the initial configuration parameters of a device, the startup sequence, and read-back capabilities.

Xilinx provides default option templates with the software. You can create your own implementation, simulation, and configuration templates with the Template Manager utility. This utility also allows you to set advanced options using the Customize Options dialog box. The following sections describe these procedures.

- "Starting the Template Manager"
- "Creating a Template"
- "Editing a Template"
- "Setting Custom Template Options"
- "Using the Template"

Starting the Template Manager

Use the following procedure to start the Template Manager. You must complete this procedure before using the procedures in the following sections.

1. In the Design Manager, select **`Utilities`** → **`Template Manager`** to open the dialog box shown in the following figure.

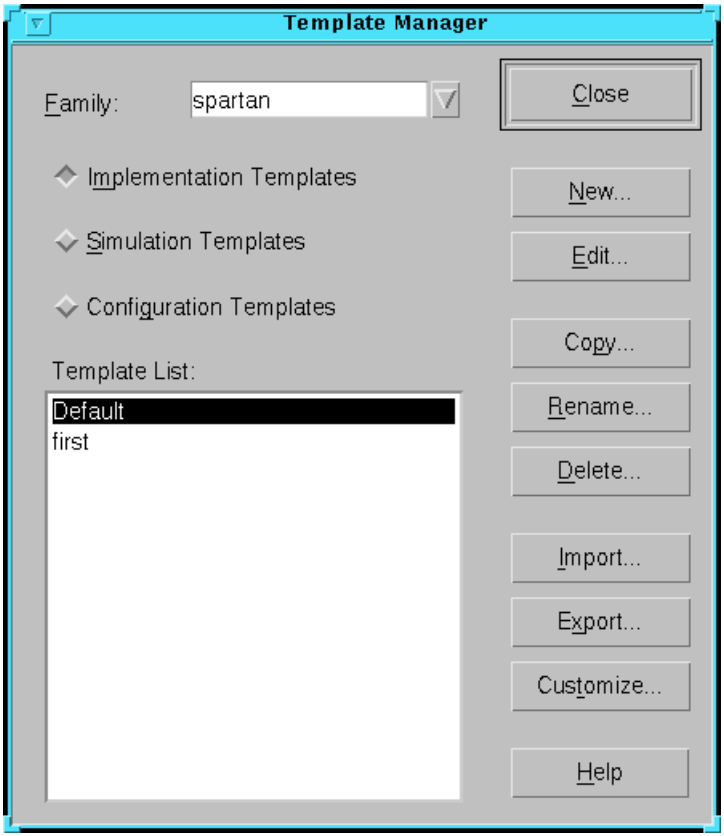


Figure 3-28 Template Manager Dialog Box

2. Select the appropriate device family in the Family drop-down list.

The following table shows which template family to select based on the FPGA or CPLD family you are targeting.

Table 3-1 Template Manager Family Usage

Targeted Device Family	Template Family
XC3000A / L	xc3000
XC3100A / L	xc3000
XC4000E / L	xc4000
XC4000EX / XL / XV / XLA	xc4000
XC5200	xc5200
Spartan / XL	spartan
Spartan2	spartan2
Virtex	virtex
XC9500 / XL / XV	xc9500

3. Select either **Implementation Templates**, **Simulation Templates**, or **Configuration Templates** to specify the type of template with which to work.

Note: Configuration options are supported for the FPGA device families only. There are no configuration options for the CPLD family.

4. Create and modify templates from the Template Manager dialog box as described in the following sections.

Creating a Template

Use the following procedure to create a new template.

1. In the Template Manager dialog box, click **New** to open the dialog box shown in the following figure.

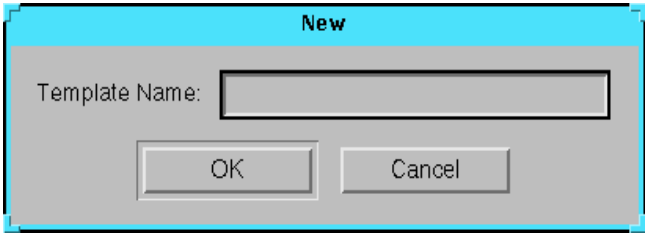


Figure 3-29 New Dialog Box

2. Type a name for the new template.
3. Click **OK**.

   The name of the new template is added to the option templates list in the Template Manager dialog box.

Editing a Template

After you create an option template as described in the preceding section, you can edit the template using the following procedure.

1. In the Template List of the Template Manager dialog box, click the name of the template you want to edit.
2. Click **Edit**.

   The Implementation, Simulation, or Configuration Options dialog box opens, depending on which type of template you are working with.
3. Select the desired settings.

   The available settings depend on the device family and the template type. See the “Implementation Flow Options” chapter for information on the options in the Implementation, Simulation, and Configuration Options dialog boxes.
4. Click **OK**.

   The Template Manager saves the options settings and closes the Implementation, Simulation, or Configuration Options dialog box.

Setting Custom Template Options

The options available in the option templates permit you to set the most commonly used options. If you want to set more advanced options, use the Customize feature in the Template Manager.

1. Select a template from the Template List in the Template Manager dialog box.
2. Click **Customize** to open the dialog box shown in the following figure.

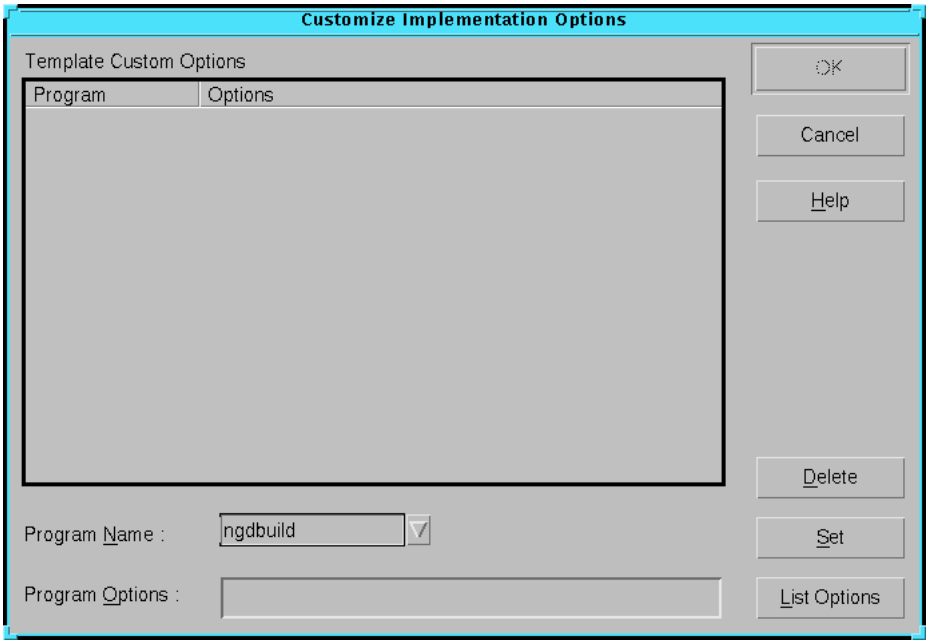


Figure 3-30 Customize Options Dialog Box

Note: The title of this dialog box changes based on whether you are working with implementation, simulation, or configuration options. Any program options you have entered previously are saved and appear the next time you open this dialog box.

3. Select the program name from the Program Name drop down list box.
4. Enter the option names in the Program Options field. Enter the options as they would appear on the command line. To open a file that lists the options and usage messages associated with the selected program name, click **List Options**.

5. Click **Set**.

   The program and option names are added to the Template Custom Options list box.

6. Repeat steps 3 through 5 for each program and option you want to enter.

7. To remove a program, click the program name in the Template Custom Options field and click **Delete**.

8. Click **OK** in the Customize Options dialog box.

Note: It is possible to enter options in the Custom Template dialog box that can conflict with normal Flow Engine options. It is beyond the scope of this manual to explain all the possible conflicts.

Using the Template

After you create a template, you must specify the template to use in the Options dialog box before you implement your design.

1. Open the Options dialog box using one of the following methods.
   - From the Design Manager, select **Design** → **Options**.
   - From the Flow Engine, select **Setup** → **Options**.
   - Click the Set Options toolbar button.

If you are targeting an FPGA, the dialog box shown in the following figure appears.

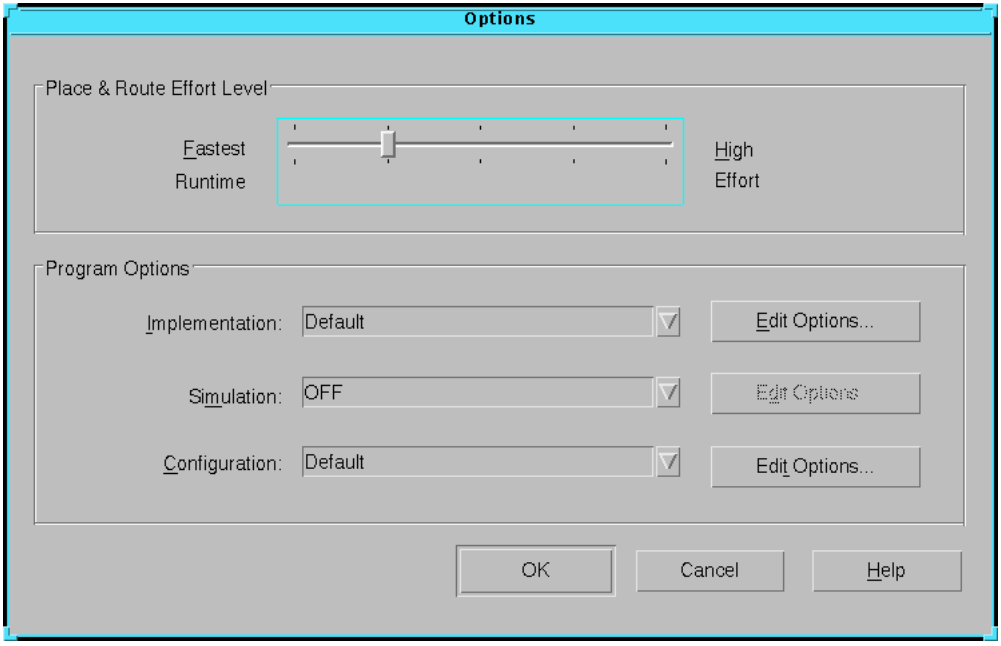


Figure 3-31 Options Dialog Box (FPGA)

If you are targeting a CPLD, the dialog box shown in the following figure appears.

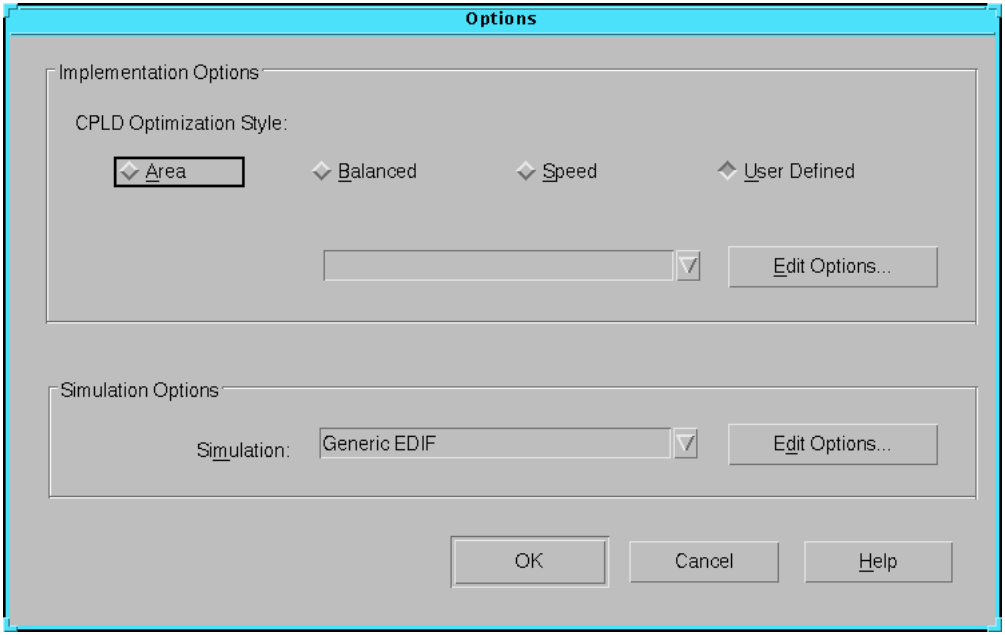


Figure 3-32 Options Dialog Box (CPLD)

2. If you are targeting an FPGA, do the following.

   a) If you created an implementation option template, select the appropriate template name from the drop-down list box next to the Implementation field.

   b) If you created a simulation option template, select the appropriate template name from the drop-down list box next to the Simulation field.

   c) If you created a configuration option template, select the appropriate template name from the drop-down list box next to the Configuration field.

3. If you are targeting a CPLD, do the following.

   a) If you created an implementation option template, select **`User Defined`** in the Implementation Options group box

and select the appropriate template name from the drop-down list box.

b) If you created a simulation option template, select the appropriate template name from the drop-down list box next to the Simulation field.

4. Click **OK** to maintain your settings and exit the Options dialog box.

5. Implement your design as described in the "Implementing a Design from the Design Manager" or "Implementing a Design from the Flow Engine" section.

Chapter 4

Menu Commands

This chapter describes the Design Manager and Flow Engine commands. It contains the following sections.

- “Design Manager Menus”
- “Flow Engine Menus”
- “Design Manager and Flow Engine Menu Commands”
- “Toolbars”
- “Toolbox”
- “Run Control”
- “Popup Menus”
- “Keyboard Shortcuts”

Design Manager Menus

The Design Manager has six menus, which are described in the following sections.

File Menu

The File menu contains commands that create and modify a project, control preferences for working with a project, and exit the Design Manager. The following are the File menu commands and a brief explanation of each.

New Project	Creates a new project
Open Project	Selects an existing project and opens it
Save Project	Saves the current project
Delete Project	Selects an existing project and deletes it

Preferences	Customizes the program settings
1, 2, 3, 4	Displays up to four of the most recently used projects
Exit	Quits the Design Manager

Design Menu

The Design menu contains commands that implement the design and manipulate the design versions and implementation revisions. The following are the Design menu commands and a brief explanation of each.

Implement	Launches the Flow Engine and runs the implementation flow on the “last” revision
Options	Sets options for the implementation flow
Set Part	Sets the device part
Set Constraints File	Sets the UCF file for constraining a design
Set Guide File(s)	Sets the file for guiding a design
Set Floorplan File(s)	Sets the files generated by the Floorplanner for guiding a design
FPGA Multi-Pass Place & Route	Runs multiple place and route passes on a selected design version
Lock Pins	Generates pin locking constraints in the UCF file
New Version	Creates a new design version of the design data
New Revision	Creates a new implementation revision of the design data
Copy Revision	Copies the selected implementation revision into a new implementation revision
Export	Exports the data for the selected implementation revision
Properties	Displays the properties of the selected object
Delete	Deletes the selected object

Tools Menu

The Tools menu contains commands that launch various tools to run on the selected implementation revision. The following are the Tools menu commands and a brief explanation of each.

Flow Engine	Runs the Flow Engine, which maps, places, and routes your design
Timing Analyzer	Runs the Timing Analyzer, which analyzes paths in your design and compares them against your timing constraints
Floorplanner	Runs the Floorplanner, which allows you to graphically place your design into certain FPGAs
PROM File Formatter	Runs the PROM File Formatter, which creates a PROM file or series of PROM files
Hardware Debugger	Runs the Hardware Debugger, which downloads your design to an in-circuit part and interactively debugs your design
FPGA Editor	Runs the FPGA Editor, which allows you to graphically examine your placed and routed design
Chip Viewer	Runs the Chip Viewer, which allows you to graphically view the final fitting report for CPLDs
JTAG Programmer	Runs the JTAG Programmer, which allows you to program certain FPGAs or CPLDs while the device is on a circuit board

Utilities Menu

The Utilities menu contains commands that run utilities to gain information about the selected project or implementation revision and to set options for the design implementation flow. The following are the Utilities menu commands and a brief explanation of each.

Report Browser	Opens the Report Browser for the selected implementation revision
Constraints Editor	Runs the Constraints Editor, which allows you to create and edit constraints

Command History	Displays the command and option history for the selected implementation revision
Template Manager	Manages option templates for the current project
Produce Timing Report	Generates specified timing reports
Lock Pins Report	Opens the report generated by the Design → Lock Pins command
Flow Log File	Opens the Flow Engine log file for the selected revision in a separate window
Project Notes	Edits notes for the current project

View Menu

The View menu contains commands that control the visibility of the toolbar, status bar, and toolbox in the Design Manager main window. The following are the View menu commands and a brief explanation of each.

Toolbar	Shows or hides the toolbar
Status Bar	Shows or hides the status bar
Toolbox	Shows or hides the toolbox

Help Menu

The Help menu contains commands that invoke online help and display information about the Design Manager. The following are the Help menu commands and a brief explanation of each.

Help Topics	Displays help topics
Online Documentation	Starts the online documentation viewer
Xilinx on the Web → Support and Services	Opens the Xilinx technical support page on the Web
Xilinx on the Web → Xilinx Home Page	Opens the Xilinx home page on the Web
About Design Manager	Displays the program information and copyright

Flow Engine Menus

The Flow Engine has five menus, which are described in the following sections.

Flow Menu

The Flow menu contains commands that process the design implementation flow. The following are the Flow menu commands and a brief explanation of each.

Run	Executes the implementation flow until complete or until target process is complete
Step	Executes one process in the implementation flow
Step Back	Moves one step back in the implementation flow execution process
Abort	Aborts the currently executing process
Close	Closes the Flow Engine

View Menu

The View menu contains commands that control the font type of the Flow Engine message log window and the visibility of the toolbar and status bar in the Flow Engine main window. The following are the View menu commands and a brief explanation of each.

Toolbar	Shows or hides the toolbar
Status Bar	Shows or hides the status bar
Font	Modifies the font type of the message log window

Setup Menu

The Setup menu contains commands that control and configure the design implementation flow. The following are the Setup menu commands and a brief explanation of each.

Options	Sets options for the implementation flow
Stop After	Sets the processing break point

FPGA Re-entrant Route	Sets the re-entrant route options for a previously routed design
Update Flow	Detects if any changes have been made that may cause a process to be rerun
Advanced	Configures the implementation flow

Utilities Menu

The Utilities menu contains commands that run utilities useful for gaining information about the selected project or implementation revision. The following are the Utilities menu commands and a brief explanation of each.

Report Browser	Opens the Report Browser on the current implementation revision
Produce Timing Report	Generates specified timing reports
Command History	Displays the command and option history for the current implementation revision
Command Preview	Displays a preview of commands and options to be run for the current implementation revision
Project Notes	Edits notes for the current project

Help Menu

The Help menu contains commands that invoke online help and display information about the Flow Engine. The following are the Help menu commands and a brief explanation of each.

Help Topics	Displays help topics
Online Documentation	Starts the online documentation viewer
About Flow Engine	Displays the program information and copyright

Design Manager and Flow Engine Menu Commands

This section describes all of the menu commands for the Design Manager and Flow Engine combined. The commands are presented in alphabetical order.

1, 2, 3, 4 (File Menu)

The File menu display up to four of the most recently used projects. To open a project, click on the appropriate file listed in the menu.

Abort (Flow Menu)

Warning: The Abort command is an immediate abort. When you select this command, all data produced by the currently running process is lost.

Use this command to terminate the current Flow Engine execution.

Note: To set a run target, use the Setup → Stop After command.

About Design Manager (Help Menu)

Use this command to display program information, including the software version and serial number, and the copyright notice. A dialog box displays this information.

About Flow Engine (Help Menu)

Use this command to display program information, including the software version and serial number, and the copyright notice. A dialog box displays this information.

Advanced (Setup Menu)

Use this command to open the Advanced dialog box, shown in following figure. Set the options in this dialog box to configure the implementation flow and control aspects of the Flow Engine interface.

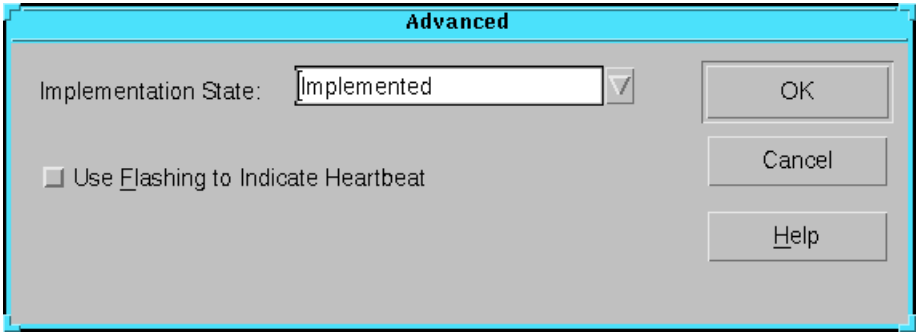


Figure 4-1 Advanced Dialog Box

Advanced Dialog Box

The following options are available in this dialog box.

- Implementation State

  Use this option to update the Flow Engine to which implementation state was last completed. Most users will not need to modify this setting.

  In normal Flow Engine use, do not use this setting to change the implementation state. This setting is typically used if some processing on the design was performed outside of the Design Manager or Flow Engine. For example, if the design was routed using the FPGA Editor, the Implementation State option should be set to Routed to inform the Design Manager and Flow Engine that this implementation state is complete.

- Use Flashing to Indicate Heartbeat

  Use this option to show flashing process icons that indicate processing activity in the Flow Engine. This option is useful for providing feedback that the Flow Engine is running. However, using this option may slow the implementation process. This option is off by default.

Chip Viewer (Tools Menu)

Use this command to launch the Chip Viewer. This tool presents a graphical view of the final fitting report for CPLDs. You can use the Chip Viewer before or after the Fitting process.

If you run the Chip Viewer before Fitting, the viewer reads from the design netlist. Select a device to get basic design information, set I/O assignments and pin-locking, and modify the UCF file.

If you run it after Fitting, the viewer reads the fitting results in the .vm6 file. It allows you to view the final fit and all pin assignments, connections between macrocells and details about macrocell use, and power settings and slew rates.

Note: The Chip Viewer is supported for CPLD device families only.

Close (Flow Menu)

Use this command to close the Flow Engine window. Use this command when you are finished implementing the design or no longer need the Flow Engine.

Command History (Utilities Menu)

Use this command to open the Command History utility and display the commands and options that have been run in the flow for the current implementation revision. This utility is useful for reviewing the commands and options that were used while executing the flow. This utility is shown in the following figure.

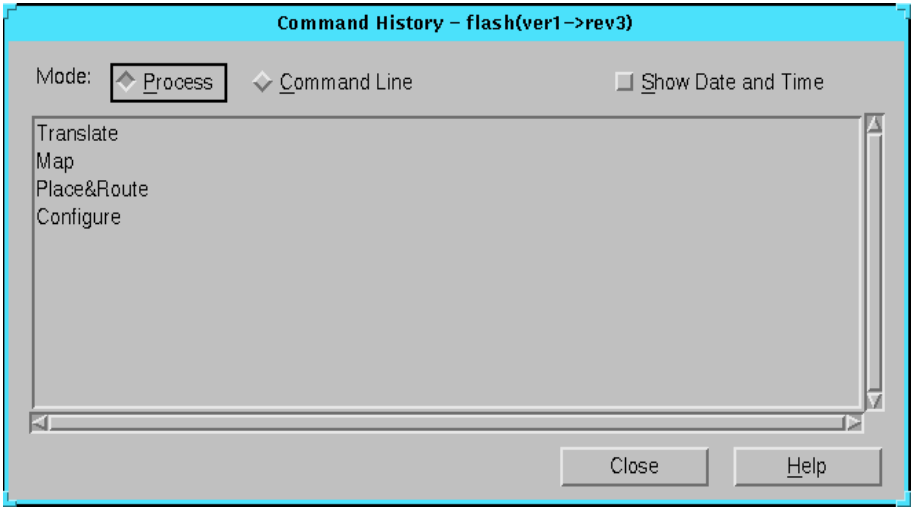


Figure 4-2 Command History Utility

Command History Utility

The following options are available.

- Mode

  Select a view mode.

  - Process

    This mode displays high level flow information about the executed commands, such as optimize, map, place, and route.

  - Command Line

    This mode displays the executed operating system commands and command line options.

  - Show Date and Time

    This mode displays the date and time that the commands were run on the selected implementation revision.

- Close

  Click **Close** to exit the utility.

Command Preview (Utilities Menu)

Use this command to open the Command Preview utility and display the commands and options that remain to be run in the flow for the current implementation revision. This utility is useful for determining which commands will be executed in the flow and whether the correct options have been set. This utility is shown in the following figure.

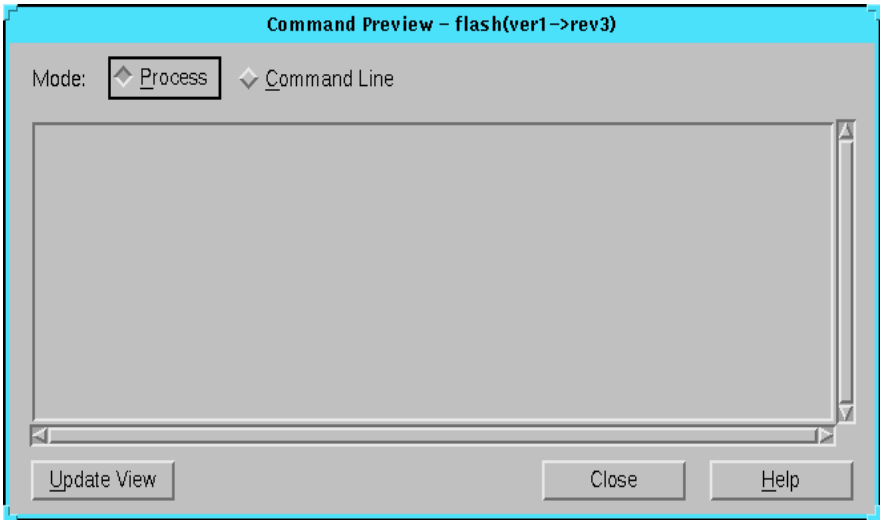


Figure 4-3 Command Preview Utility

Command Preview Utility

The following options are available.

- Mode

  Select a view mode.

  - Process

    This mode displays high level flow information about the commands, such as optimize, map, place, and route, that will be executed.

  - Command Line

    This mode displays the operating system commands and command line options that will be executed.

- Update View

  Click this button to update the command preview information to reflect any changes made in Flow Engine option settings since opening the Command Preview window.

- Close

  Click **`Close`** to exit the utility.

Constraints Editor (Utilities Menu)

Use this command to launch the Constraints Editor. This tool allows you to create new constraints and edit existing ones after running the Translate step in the Flow Engine.

The Constraints Editor accepts NGD and, optionally, UCF files as input and writes out a valid UCF file. You can use this valid UCF file as input to an automatic implementation of a revision or to the Translate step, if you are implementing a revision in separate steps.

For additional information, see the *Constraints Editor Guide*.

Copy Revision (Design Menu)

Use this command to make a copy of the currently selected implementation revision. The new implementation revision contains the same data as the selected implementation revision. When you use the Copy Revision command, the Copy As dialog box appears, as shown in the following figure. After the Design Manager creates the copy, it displays a new implementation revision icon in the project view.

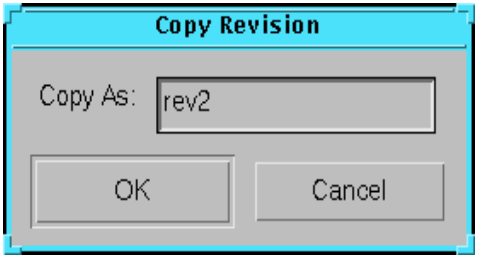


Figure 4-4 Copy As Dialog Box

Copy Revision Dialog Box

Type a name for the implementation revision copy in the Copy As field.

Delete (Design Menu)

Warning: When deleting an item from the project view, the Design Manager deletes the item and all accompanying data. Deleted data cannot be recovered.

Use this command to delete the currently selected project, design version, or implementation revision. Select the appropriate icon and select **Design** → **Delete** or press the **Delete** key on your keyboard. You are prompted to confirm that you really want to delete the selected data.

Delete Project (File Menu)

Warning: When deleting a project, the Design Manager deletes the project and all accompanying data. Deleted data cannot be recovered.

Use this command to delete a project along with all its associated files in the project directory. This command opens the Delete Project dialog box, shown in the following figure. You are presented with a list of projects from which you can select a project to delete. To delete a project, select a project and click **Delete**.

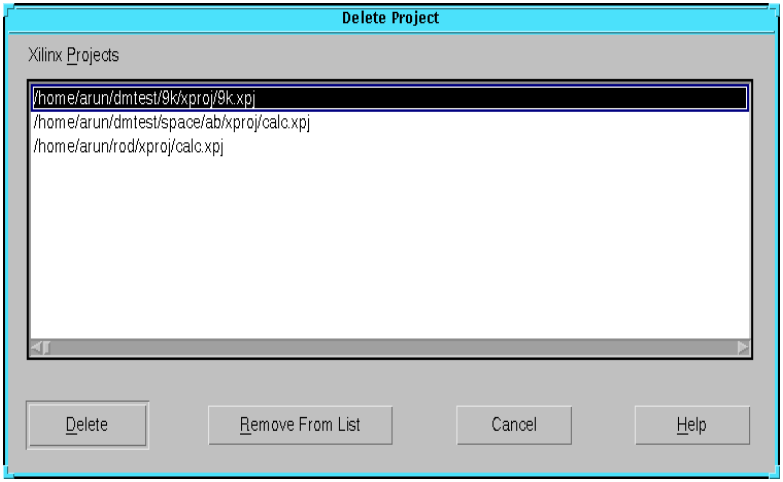


Figure 4-5 Delete Project Dialog Box

Delete Project Dialog Box

The following options are available in this dialog box.

- Xilinx Projects

  Select a project to delete.

- Delete

  Click **Delete** to exit the dialog box and delete the selected project.

- Remove From List

  Click **Remove From List** to exit the dialog box and remove the project from the most recently used project list in the File menu. This option removes the project from the list but does *not* delete the project and all accompanying data.

Exit (File Menu)

Use this command to close the current project and exit the Design Manager. All data is saved automatically upon exit. You are prompted to confirm that you really want to quit.

Export (Design Menu)

Use this command to export your design data. It opens the Export dialog box, shown in the following figure. This command is useful for transferring design data created in the Design Manager to other environments.

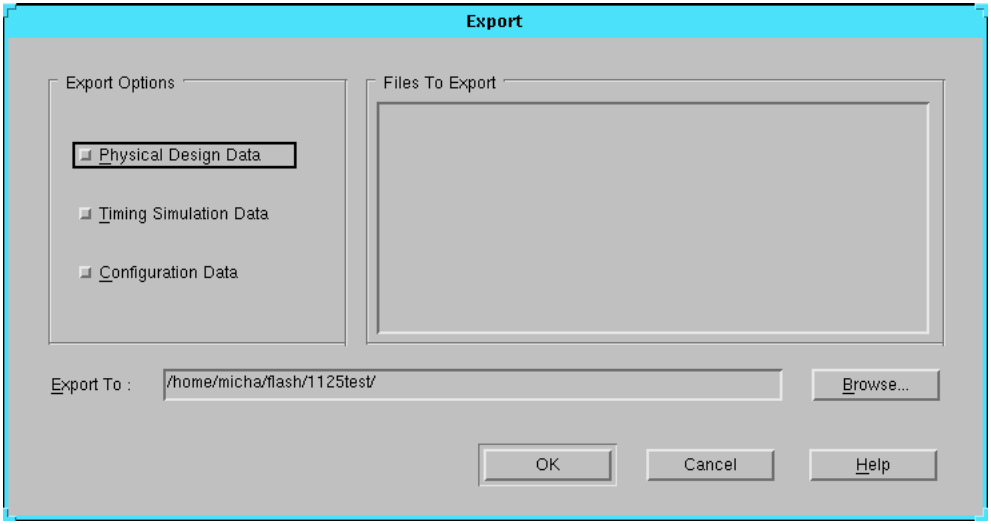


Figure 4-6 Export Dialog Box

Note: The Flow Engine automatically exports certain files to your design directory based on the targets selected in the Options dialog box.

Export Dialog Box

The following options are available in this dialog box.

- Export Options

  Choose the types of data to export.

  - Physical Design Data

    Select this option to export physical design data (*design_name*.ncd file for FPGAs and *design_name*.vm6 or *design_name*.gyd file for CPLDs).

  - Timing Simulation Data

    Select this option to export timing simulation data (*time_sim*.edn, *time_sim*.sdf, *time_sim*.v, *time_sim*.vhd, and *time_sim*.xmm files).

  - Configuration Data

    Select this option to export configuration data (*design_name*.bit or *design_name*.ll file for FPGAs and *design_name*.jed file for CPLDs).

- Files To Export

  This list box shows the files to be exported based on the selections made in the Export Options area.

- Export To

  Type the directory path and name in which to save the exported data. Click the **Browse** button to open a directory selection dialog box in which you can select a directory for the exported data.

Floorplanner (Tools Menu)

Use this command to launch the Floorplanner from the Design Manager. The Floorplanner is a graphical placement tool that gives you control over placing a design into a target FPGA using a “drag and drop” paradigm with the mouse pointer.

The Floorplanner displays a hierarchical representation of the design in the Design window using hierarchy structure lines and colors to distinguish the different hierarchical levels. The Floorplan window displays the floorplan of the target device into which you place logic from the hierarchy.

For online help for this tool, obtain Help from within the Floorplanner.

Note: The Floorplanner is supported for all XC4000 families, Virtex, Spartan/XL, and Spartan2 FPGA device families only.

Flow Engine (Tools Menu)

Use this command to launch the Flow Engine. You can use the Flow Engine to implement a design. You can set compile and flow options from within the Flow Engine.

For additional online help for this tool, obtain Help from within the Flow Engine.

Flow Log File (Utilities Menu)

Use this command to view the Flow Engine log file in a separate window. The log file contains all of the messages displayed for the programs run during the implementation process.

Font (View Menu)

Use this command to specify the font type and font size for the text displayed in the Flow Engine message log window. This command opens a standard font dialog box in which you can make these settings.

FPGA Editor (Tools Menu)

Use this command to launch the FPGA Editor from the Design Manager. The FPGA Editor is a graphical tool that allows you to display and configure FPGAs. You can use the FPGA Editor to edit design logic, logic placement, and signal routing.

Use the FPGA editor before the Place&Route step to place and route critical components. You can also use the editor to manually finish

placement and routing if the Route process does not completely route your design.

For online help for this tool, obtain Help from within the FPGA Editor.

Note: The FPGA Editor is supported for the FPGA device families only.

FPGA Multi-Pass Place & Route (Design Menu)

Use this command to run multiple place and route passes on an implementation revision. You can indicate the number of place and route passes the software should run and the number of passes you want to save. Each pass you save is added as an implementation revision in the Design Manager project view. When you use this command, the dialog box shown in the following figure appears, in which you can make these settings.

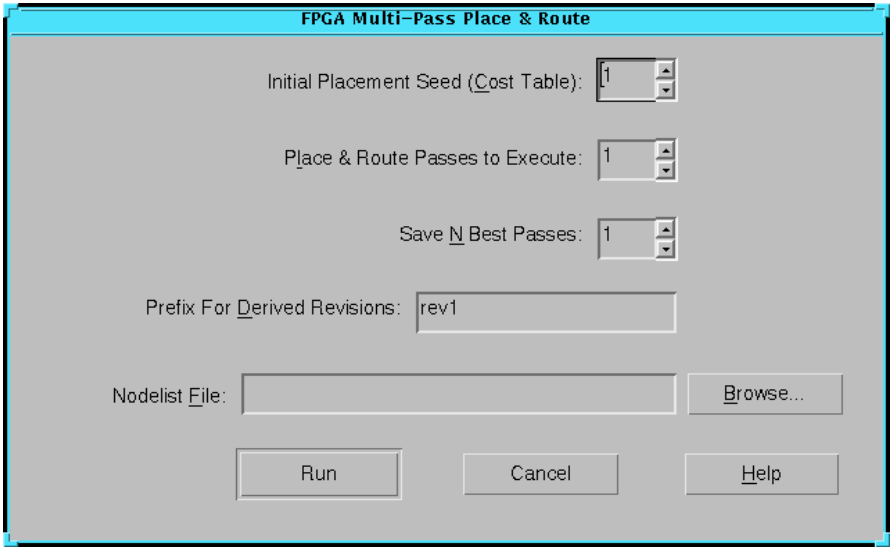


Figure 4-7 FPGA Multi-Pass Place & Route Dialog Box

After you run the place and route passes, the FPGA Multi-Pass Place & Route Status dialog box appears. This dialog box shows the design version name and the status of your placed and routed design, as shown in the following figure.

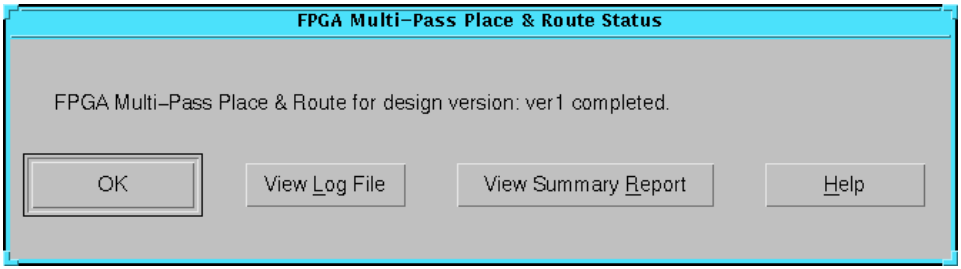


Figure 4-8 FPGA Multi-Pass Place & Route Status Dialog Box

For more information on cost tables, best passes, and on generating a nodelist file and setting up environment variables, see the "Turns Engine (PAR Multi-Tasking Option)" section of the *Development System Reference Guide*.

Note: This command is supported for the FPGA device families only. In order to accomplish the MPPR runs, the Flow Engine generates temporary (tmp) files in your working directory. If MPPR does not complete successfully, the tmp files remain in the Design Manager project view.

FPGA Multi-Pass Place & Route Dialog Box

The following options are available in this dialog box.

- Initial Placement Seed (Cost Table)

  Specify a placement initialization value with which to begin the place and route attempts. Each subsequent attempt is assigned an incremental value based on the placement initialization value.

  The number you choose corresponds to a cost table index and results in different place and route strategies. Cost tables assign weighted values to relevant factors such as constraints specified in the input file (for example, certain components must be in certain locations), the length of connections, and the available routing resources. Choose a number from 1 to 100. The default is 1.

Note: Cost tables are fixed from one run to the next; however, cost tables are not an ordered set. There is no correlation between a cost table's number and its relative value.

- Place & Route Passes to Execute

  Specify the number of place and route passes to attempt. Choose a number from 1 to 100. The default is 1.

- Save N Best Passes

  Specify the number of place and route passes to save. The software saves the specified number of passes. Choose a number from 1 to 100. The default is 1.

  This option compares every result to every other result and leaves you with the best passes. The best outputs are determined by a score assigned to each output design. This score takes into account such factors as the number of unrouted nets, the delays on nets, and conformance to your timing constraints. The lower the score, the better the design.

- Prefix for Derived Revisions

  Enter a prefix for the name of the passes to be run, if you do not want to use the default, rev#. Passes saved as revisions in the Design Manager project view follow different default naming conventions than normal revisions. By default, the passes are named rev#_p#_#_#_#.

  The default prefix, rev#, indicates the number of the revision on which the pass was based. The rest of the pass name is fixed, that is you cannot alter it. The second number, p#, indicates the number of the Multi-Pass Place & Route (MPPR) run within a given version. For example, if you run MPPR once, p will be followed by a 1. If you run MPPR a second time on a different revision within the same version, p is followed by 2. The last three numbers are based on the initial cost table, the pass number, and the number of passes saved.

- Nodelist File

  Click the **Browse** button to the right of this field to choose a nodelist file that you have generated. Choosing a nodelist file allows you to use multiple machines (nodes) that are networked together for a multi-run place and route job, significantly reducing the total amount of elapsed time to completion. The nodelist file contains a list of the node names, one per line.

Note: The Nodelist File option is only available on UNIX workstations.

- Run

  Click **Run** to exit the dialog box and launch the FPGA Multi-Pass Place & Route Flow Engine.

FPGA Multi-Pass Place & Route Status Dialog Box

The following options are available in this dialog box.

- OK

  Click OK to exit the dialog box.

- View Log File

  Click this button to view the log file.

- View Summary Report

  Click this button to launch the Report Browser and view the summary report generated by the FPGA Multi-Pass Place & Route Flow Engine.

FPGA Re-entrant Route (Setup Menu)

Use this command to reroute a previously routed design. This command opens the Re-entrant Route dialog box, shown in the following figure, which allows you to set up the conditions for your re-entrant routing. You can set the number of re-entrant routing and cleanup passes and set whether to use timing constraints for the re-entrant route process.

Note: This command is supported for FPGA device families only.

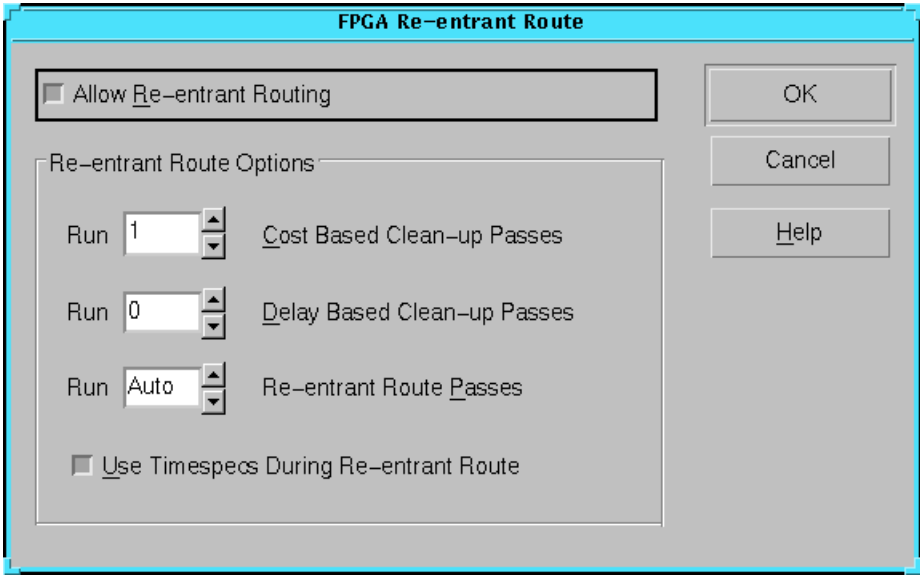


Figure 4-9 FPGA Re-entrant Route Dialog Box

FPGA Re-entrant Route Dialog Box

The following options are available in this dialog box.

- Allow Re-entrant Routing

  Use this option to further route an already routed design. The router reroutes some connections to improve the timing score or to finish routing unrouted nets. This option is useful if you want to manually route a portion of the design and then automatically route the design or if you want to run additional delay reduction passes.

- Re-entrant Route Options

  You can set the number of re-entrant routing and cleanup passes. If you run both cost-based and delay-based cleanup passes, the cost-based passes will run before the delay-based passes. Running more than two cleanup passes rarely provides improved results. You can also specify whether you want to use timing constraints during the re-entrant routing process.

- Run _ Cost-Based Cleanup Passes

  Cost-based cleanup makes rerouting decisions by assigning weighted values to the factors affecting delay times between sources and nets. Set the number of cost-based cleanup passes you want to run by choosing a number from 1 to 5. The default is 1.

- Run _ Delay-Based Cleanup Passes

  Delay-based cleanup makes rerouting decisions based on computed delay times between sources and loads on the routed nets, and reroutes to minimize the delays. Set the number of delay-based cleanup passes you want to run by choosing a number from 1 to 5. The default is 0.

- Run _ Re-entrant Route Passes

  Re-entrant routing runs additional timing driven or non-timing driven routing passes, depending on whether you specified timing constraints. Placement and routing from previous place and route runs are preserved. Set the number of re-entrant route passes by choosing a number from 1 to 2000. The default is Auto.

- Use Timespecs During Re-entrant Route

  The Flow Engine uses timing constraints in the design file to route the design within the specified constraints. By default, this option is on.

Hardware Debugger (Tools Menu)

Use this command to launch the Hardware Debugger. Use the Hardware Debugger to download a design to a device, verify the downloaded configuration, and display the internal states of the programmed device.

For online help for this tool, obtain Help from within the Hardware Debugger.

Note: The Hardware Debugger is supported for FPGA device families only.

Help Topics (Help Menu)

Use this command to display the opening screen of Design Manager or Flow Engine Help. From the opening screen, you can jump to step-by-step instructions and to various types of reference information.

After you open Help, you can click the Help Topics button in the Help window whenever you want to return to the opening screen of Help.

For more information about online help, see the "Using Help" section of the "Getting Started" chapter.

Implement (Design Menu)

Use this command to start the implementation process. This command opens the Flow Engine and begins an automatic implementation on the "last" implementation revision. The "last" revision is the bottommost revision in the Design Manager project view. However, if you changed your source design for the "last" revision, the New Version dialog box appears. You must set options in this dialog box before implementation can take place. See the "New Version Dialog Box" section for information on these options.

If you want to set implementation, simulation, and configuration options before you implement your design, set them in the Options dialog box. For more information on this dialog box, see the "Options Dialog Box (FPGA)" or "Options Dialog Box (CPLD)" section.

Note: If you want to implement a revision that is not the "last" revision, right-click on a revision and select Re-implement. See the "Re-Implementing a Design" section of the "Using the Design Manager and Flow Engine" chapter for information.

After you implement a design, the Implement Status dialog box appears. This dialog box is shown in the following figure.

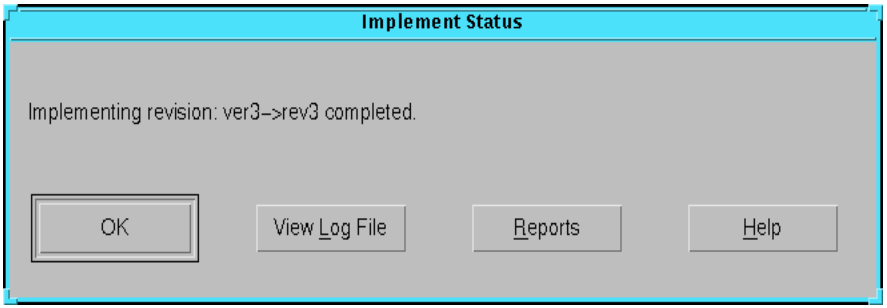


Figure 4-10 Implement Status Dialog Box

Implement Status Dialog Box

The following options are available in this dialog box.

- OK

  Click OK to exit the dialog box.

- View Log File

  Click this button to view the log file for this implementation.

- Reports

  Click this button to launch the Report Browser and view reports generated by the Flow Engine.

JTAG Programmer (Tools Menu)

Use this command to launch the JTAG Programmer. Use the JTAG Programmer to download your design and configure a device from the XC4000, XC5200, Virtex, Spartan / XL, or Spartan2 FPGA families or XC9500 CPLD family.

For online help for this tool, obtain Help from within the JTAG Programmer.

Lock Pins (Design Menu)

Use this command to perform pin locking by placing pinout information in the user constraints file (UCF). This command allows you to use pinout information with other Xilinx implementation tools. For FPGAs, pin locations and logical pad names are read from a placed NCD file. For CPLDs, this information is read from a fitted GYD file.

This command creates a UCF file if one does not exist. If one exists, the existing user constraints are maintained, but additional pin locking constraints are added to the file. All pin locking constraints created by this command are written in a PINLOCK section within the UCF file.

After the constraints are generated, you can review the Lock Pins report by clicking View Report in the status dialog box, shown in the following figure, or by using the Utilities → Lock Pins Report command.

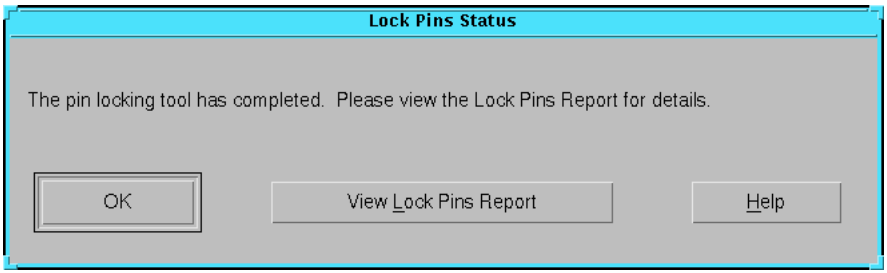


Figure 4-11 Lock Pins Status Dialog Box

Lock Pins Status Dialog Box

The following options are available in this dialog box.

- OK

  Click OK to exit the dialog box.

- View Lock Pins Report

  Click this button to view the report generated during the creation of pin locking constraints in your UCF file.

Lock Pins Report (Utilities Menu)

Use this command to open the report file generated during the execution of the Design → Lock Pins command. This report contains information on the constraint conflicts between the pin locking constraints in the UCF file and the design file.

New Project (File Menu)

Use this command to create a new project. This command opens the New Project dialog box, shown in the following figure. In this dialog box, you can specify the design file for creating your new project.

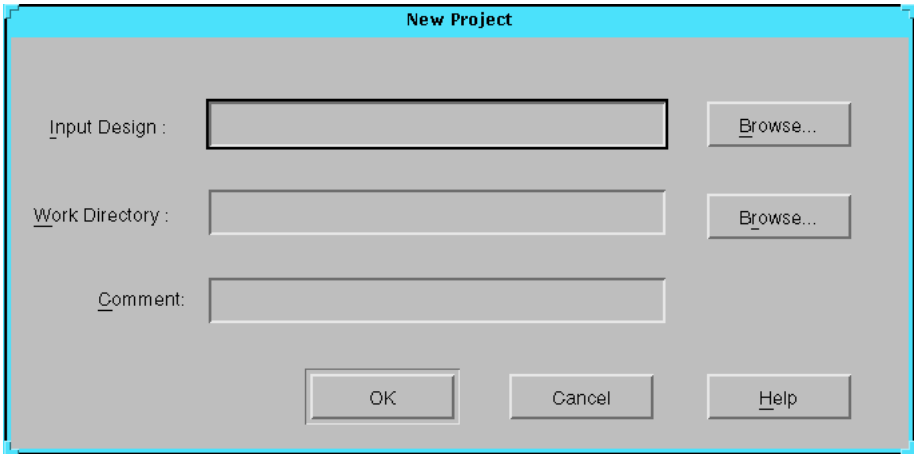


Figure 4-12 New Project Dialog Box

Note: To open an existing project, use the **File** → **Open Project** command.

New Project Dialog Box

The following options are available in this dialog box.

- Input Design

  Specify the name of the design file you want to open. You can either type the name or click the **Browse** button to the right of the Design field. Clicking the Browse button opens a file selection dialog box in which you can select a design file to open. See the "Inputs and Outputs" section of the "Introduction" chapter for information on the input design file types accepted by the Design Manager.

- Work Directory

  Specify the name of the directory in which to put the project data files. To modify the work directory, type the path or click the **Browse** button to open a directory selection dialog box. The

software automatically appends the subdirectory xproj to the selection made in the directory selection dialog box. The xproj subdirectory stores all of the data files for the project.

If you want to change the name of the work directory, type over the name using the characters A through Z, a through z, 0 through 9, period (.), underscore (_), or hyphen (-) only.

Note: When you browse for the input design, the software automatically fills the Work Directory field with the input design directory followed by the xproj subdirectory.

- Comment

  Type any comments, including options and strategies. Comments appear in the main window next to the project icon.

New Revision (Design Menu)

Use this command to create a new implementation revision. A new implementation revision allows you to attempt a new implementation of the design using different compile options or a different target part. When you use the New Revision command, you must make settings in the dialog box shown in the following figure. After the new implementation revision is created, a new implementation revision icon is displayed in the Design Manager project view.

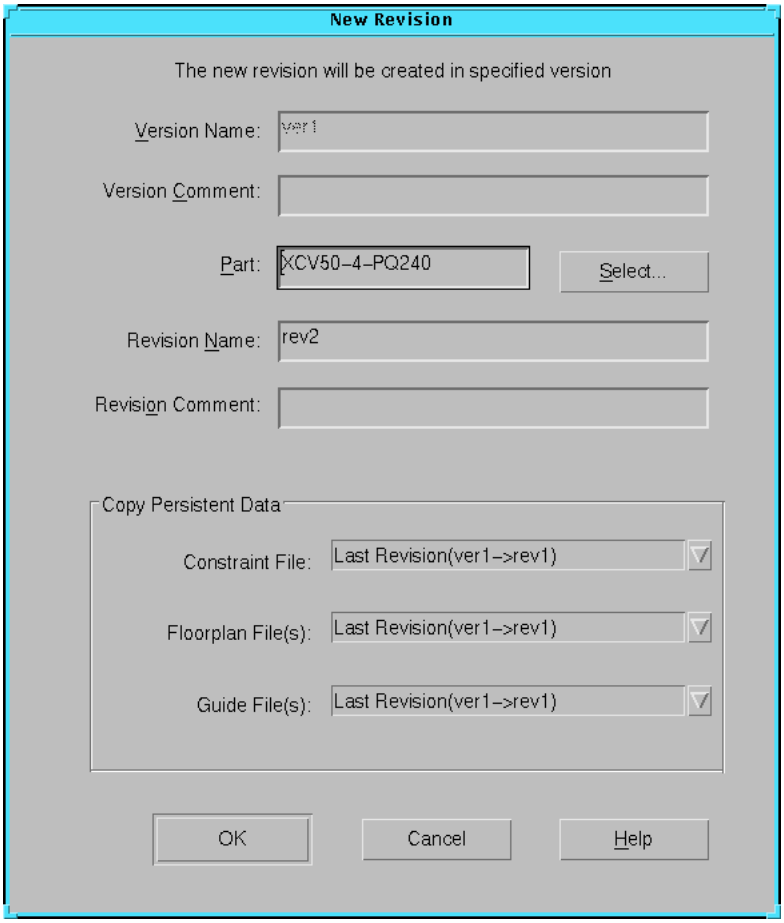


Figure 4-13 New Revision Dialog Box

New Revision Dialog Box

The following options are available in this dialog box.

- Version Name

  This option is disabled when creating a revision.

- Version Comment

  This option is disabled when creating a revision.

- Revision Name

  Enter the revision name for your implementation revision.

Note: When naming revisions, use the characters A through Z, a through z, 0 through 9, period (.), underscore (_), or hyphen (-) only.

- Revision Comment

  Type any comments, including options and strategies. Comments appear in the main window next to the implementation revision icon.

- Part

  Click the **Select** button to the right of the Part field to select a part type from the Part Selector. See the "Part Selector Dialog Box" for details.

- Copy Persistent Data

  Use the drop down list boxes to the right of the following options to copy constraint, guide, and floorplan data to the new revision.

  - Constraints File
  - Guide File
  - Floorplan File

  When initially creating a project, the Design Manager copies constraints file data from the project directory to the revision directory. By default, floorplan and constraint file data is copied from the "last" revision, that is the bottommost revision in the project view. Guide file data is copied based on your previous setting. You can choose to copy data from a previous revision or a custom file or choose **None** if you do not want to copy data.

New Version (Design Menu)

Use this command to create a new design version. A new design version allows you to manage changes to the input design or logic of your design. For instance, any time your netlist data or schematic changes, you must generate a new design version.

When you use the New Version command, the New Version dialog box appears, as shown in the following figure. In the New Version dialog box, enter the information necessary to define the new design

version. After the new design version is created, a new design version icon is immediately added and displayed in the Design Manager project view.

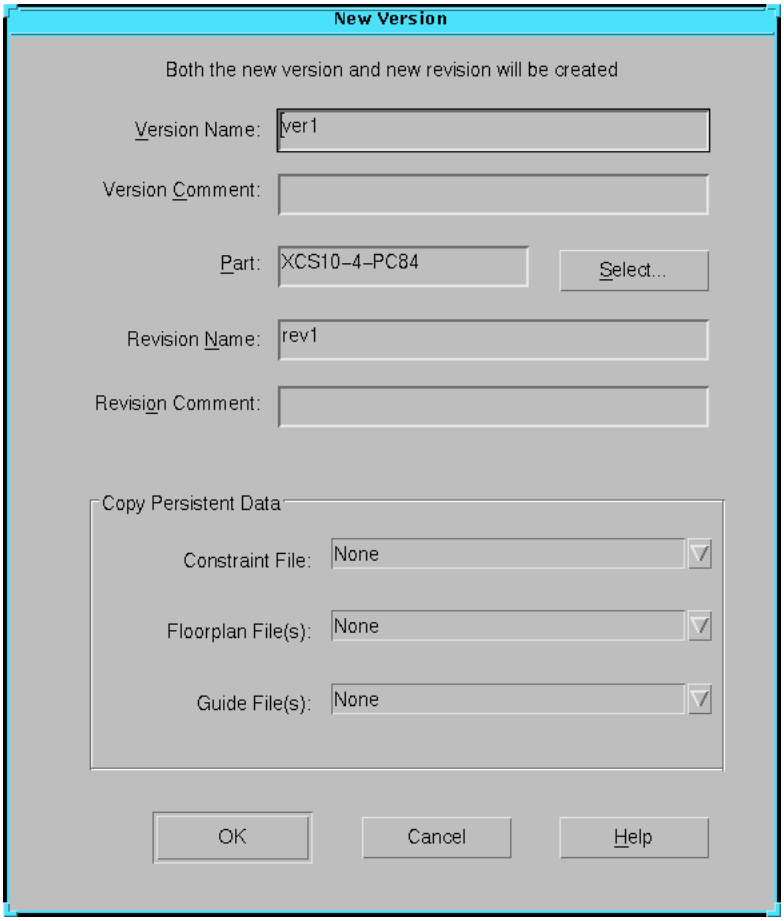


Figure 4-14 New Version Dialog Box

New Version Dialog Box

The following options are available in this dialog box.

Note: When naming versions and revisions, use the characters A through Z, a through z, 0 through 9, period (.), underscore (_), or hyphen (-) only.

- Version Name

  Enter the design version name.

- Version Comment

  Type any comments, including options and strategies. Comments appear in the main window next to the design version icon.

- Revision Name

  Enter the revision name for your implementation revision.

- Revision Comment

  Type any comments, including options and strategies. Comments appear in the main window next to the implementation revision icon.

- Part

  Click the **Select** button to the right of the Part field to select a part type from the Part Selector. See the "Part Selector Dialog Box" section for details.

- Copy Persistent Data

  Use the drop down list boxes to the right of the following options to copy constraint, guide, and floorplan data to the new revision.

  - Constraints File
  - Guide File
  - Floorplan File

  When initially creating a project, the Design Manager copies constraints file data from the project directory to the revision directory. By default, floorplan and constraint file data is copied from the "last" revision, that is the bottommost revision in the project view. Guide file data is copied based on your previous setting. You can choose to copy data from a previous revision or a custom file or choose **None** if you do not want to copy data.

Online Documentation (Help Menu)

Use this command to open the software manuals on the Web. If you do not have Web access, you can still access the documentation, either from the copy you installed on your local hard drive or from the CD.

The manuals are opened in the default Web browser. You can set your default browser using the File → Preferences command.

Open Project (File Menu)

Use this command to open an existing project. The project consists of several files but is represented in the Xilinx Project dialog box as a single file with the .xpj extension. The Open Project command opens the Open Project dialog box, as shown in the following figure. Select a project from this dialog box.

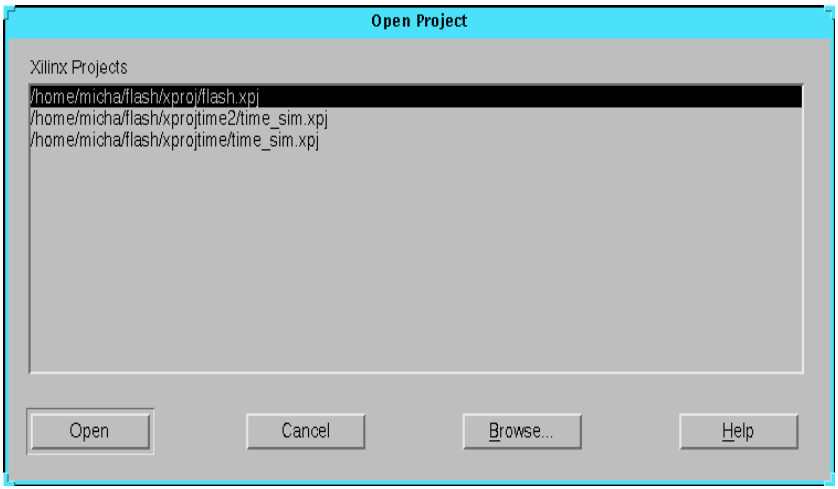


Figure 4-15 Open Project Dialog Box

To open one of the four most recently used projects, select a project from the project name list in the Design Manager File menu.

Note: To create a new project, use the **`File`** → **`New Project`** command.

Open Project Dialog Box

The following options are available in this dialog box.

- Xilinx Projects

  Select the project file you want to open.

- Open

  Click **Open** to exit the dialog box and open the selected project file.

- Browse

  Click **Browse** to search for a project file. The project file you choose is appended to the Xilinx Projects list.

Options (Design and Setup Menus)

Use this command to open the dialog box shown in the following figures. This dialog box allows you to set options used in the implementation flow. Changes made in this dialog box apply to the selected implementation revision. The following dialog box appears if you are targeting an FPGA.

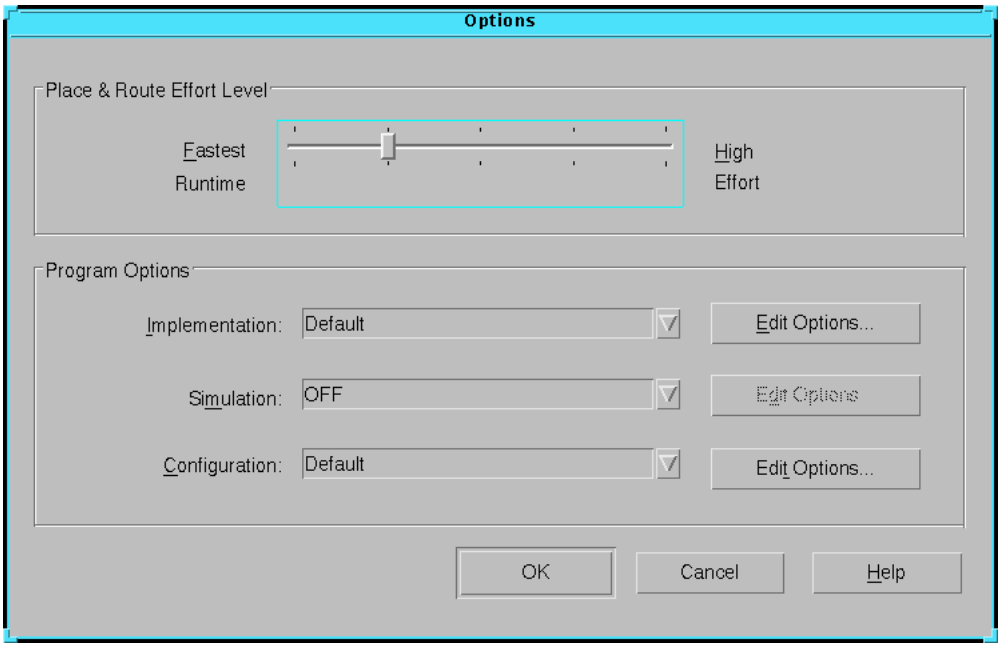


Figure 4-16 Options Dialog Box (FPGA)

The following dialog box appears if you are targeting a CPLD.

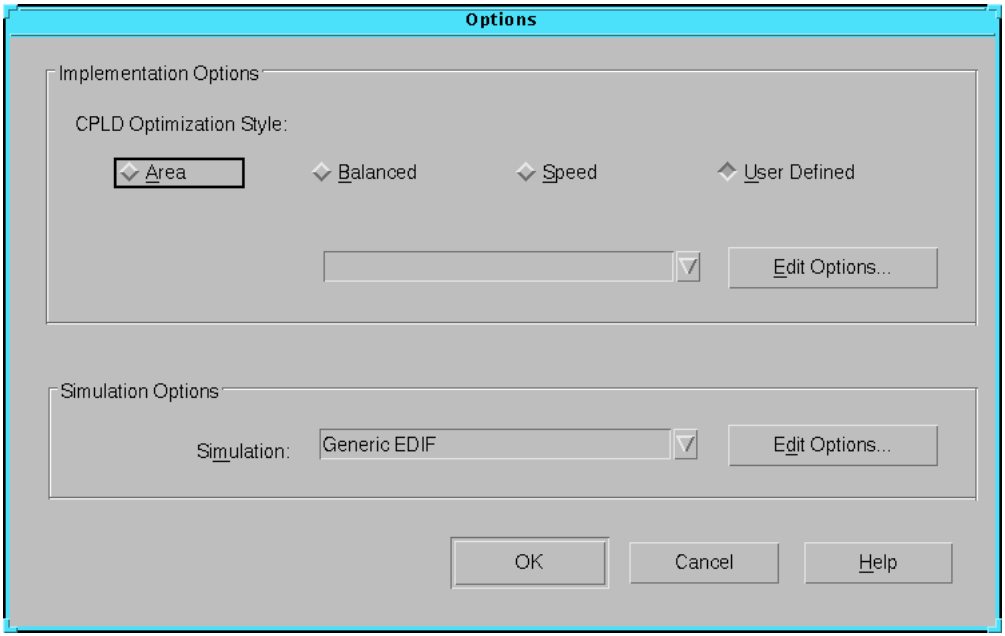


Figure 4-17 Options Dialog Box (CPLD)

Note: If you open this dialog box from the Flow Engine while a step is running, the changes are picked up when the step is done. Subsequent steps are run with the changes you made.

Options Dialog Box (FPGA)

This dialog box allows you to set implementation, configuration, and simulation options. It also allows you to set the Place and Route Effort Level.

- Place & Route Effort Level

  Use this option to specify the algorithms that the placer and router use to place and route a design. Use the Place & Route Effort Level slider bar to select an effort level setting. A setting closer to High Effort provides better place and route results at the expense of longer run times. The default value is 2.

- Implementation

  Select a set of implementation options to use from the Implementation drop-down list. Implementation options control how the

software translates, maps, places, routes, and optimizes a design. These options affect the Translate, Map, and Place&Route steps in the implementation flow. A set of default implementation options and any option templates you created with the Template Manager appear when you click this drop-down list.

Click the **Edit Options** button to the right of the Implementation drop-down list to open the Implementation Options dialog box. The options in this box depend on the target device family. For more information on the implementation options, see one of the following sections in the "Implementation Flow Options" chapter.

- "Spartan Implementation Options"
- "Spartan2 Implementation Options"
- "Virtex Implementation Options"
- "XC3000 Implementation Options"
- "XC4000 Implementation Options"
- "XC5200 Implementation Options"

- Simulation

  To produce timing simulation data, select one of the simulators or a template you created with the Template Manager from the drop-down list box. This data is produced after the design is placed and routed. See the "Producing Timing Simulation Data" section of the "Using the Design Manager and Flow Engine" chapter for more information. If you do not want to produce timing simulation data, select **OFF**.

  Click the **Edit Options** button to the right of the Simulation drop-down list to open the Simulation Options dialog box. Simulation options control the creation of netlists in terms of the Xilinx primitive set, which allow you to simulate and back-annotate your design. In back-annotation, physical design data is distributed back to the logic design to perform back-end simulation. You can perform front and back-end simulation on both pre- and post-routed designs. For information on the simulation options, see one of the following sections in the "Implementation Flow Options" chapter.

- "Spartan Simulation Options"
- "Spartan2 Simulation Options"
- "Virtex Simulation Options"
- "XC3000 Simulation Options"
- "XC4000 Simulation Options"
- "XC5200 Simulation Options"

- Configuration

  Select a set of configuration options to use in this implementation from the Configuration drop-down list. Configuration options control the configuration parameters of a device, the startup sequence, and readback capabilities. These options affect the Configure step in the implementation flow. A set of default configuration options and any option templates you created with the Template Manager appear when you click this drop-down list. Selecting a set of options produces configuration data after design implementation. The configuration data is used to program a device. Select **OFF** if you do not want to produce configuration data.

  Click the **Edit Options** button to the right of the Configuration drop-down list to open the Configuration Options dialog box. The options in this dialog box depend on the target device family. For information on the configuration options, see one of the following sections in the "Implementation Flow Options" chapter.

  - "Spartan Configuration Options"
  - "Spartan2 Configuration Options"
  - "Virtex Configuration Options"
  - "XC3000 Configuration Options"
  - "XC4000 Configuration Options"
  - "XC5200 Configuration Options"

Options Dialog Box (CPLD)

This dialog box allows you to set implementation and simulation options.

- Implementation Options

  Select a CPLD Optimization Style, whether optimized for area, a balance of both area and speed, or speed. Implementation options control how the software translates and fits a design. These options affect the Translate, Fit, and Bitstream steps in the implementation flow.

  If you created an option template using the Template Manager, click **User Defined** as your CPLD Optimization Style and select your template from the drop-down list box. If you want to edit these user defined options, click the **Edit Options** button to the right of the drop-down list to open the Implementation Options dialog box. See the "XC9500 Implementation Options" section of the "Implementation Flow Options" chapter for information on this dialog box.

- Simulation

  To produce timing simulation data, select one of the simulators or a template you created with the Template Manager from the drop-down list box. This data is produced after the design is fitted. See the "Producing Timing Simulation Data" section of the "Using the Design Manager and Flow Engine" chapter for more information. If you do not want to produce timing simulation data, select **OFF**.

  Click the **Edit Options** button to the right of the Simulation drop-down list to open the Simulation Options dialog box. Simulation options control the creation of netlists in terms of the Xilinx primitive set, which allow you to simulate and back-annotate your design. In back-annotation, physical design data is distributed back to the logic design to perform back-end simulation. You can perform front and back-end simulation on both pre- and post-fitted designs. For information on the simulation options, see the "XC9500 Simulation Options" section of the "Implementation Flow Options" chapter.

Preferences (File Menu)

Use this command to open the dialog box shown in the following figure. Use this dialog box to customize program settings, such as specifying the text editor for viewing reports. The settings you make in this dialog box are applied to all projects.

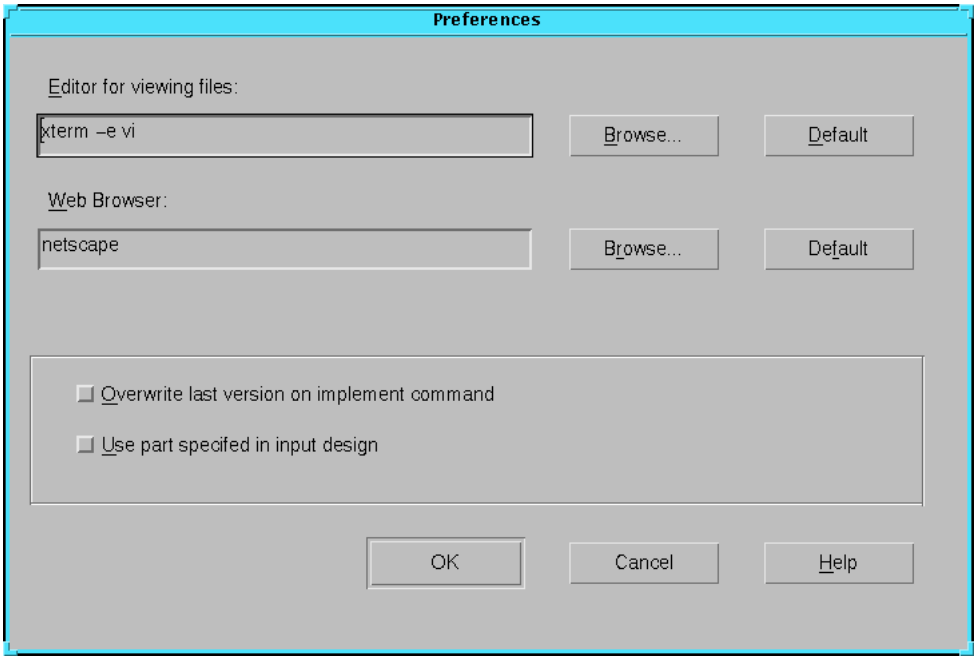


Figure 4-18 Preferences Dialog Box

Note: The text that specifies the editor and web browser is not validated and is sent directly to the operating system. Verify the text before sending it.

Preferences Dialog Box

The following options are available in this dialog box.

- Editor for Viewing Files

  Specify the text editor you want to use. This option sets the text editor for all tools in the Xilinx tool suite. Click **Browse** to search for an executable to use as your text editor. Click **Default** to select the default text editor.

- Web Browser

  Specify the Web browser you want to use. Click **Browse** to search for an executable to use as your browser. Click **Default** to select the default browser.

- Overwrite Last Version on Implement Command

  Select this option to overwrite the “last” version when you select Design → Implement. The “last” version is the bottommost version in the Design Manager project view. By default, this option is off.

- Use Part Specified in Input Design

  By default, the Design Manager reads the part you set using the Part Selector. Select this option if you want the Design Manager to read the part from the input design instead. By default, this option is off.

Produce Timing Report (Utilities Menu)

Use this command to generate timing reports. You can use this command if at least Map (for FPGAs) or Fit (for CPLDs) has completed successfully. The type, title, and file name of the report depend on the state of your design when you run this command. You cannot change the file name of the report. The following table shows the report that is generated given a particular state. The timing reports are placed in the Report Browser when complete.

Table 4-1 Timing Report Titles and File Names

State	File Name	Title
Mapped (FPGA)	map_*number*.twr	Logic Level Timing Report #*number*
Routed (FPGA)	*design_name_number*.twr	Post Layout Timing Report #*number*
Fitted (CPLD)	*design_name_number*.twr	Post Fitting Timing Report #*number*
Timed	*design_name_number*.twr	Post Layout Timing Report #*number* (FPGA) Post Fitting Timing Report #*number* (CPLD)
Implemented	*design_name_number*.twr	Post Bitgen Timing Report #*number* (FPGA) Post Fitting Timing Report #*number* (CPLD)

This command opens a dialog box in which you can set the report format. The dialog box shown in the following figure appears if you are targeting an FPGA.

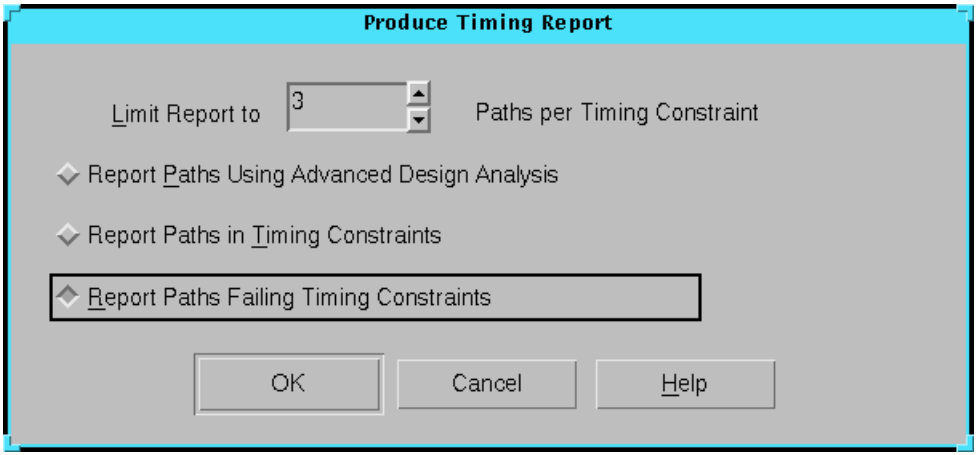


Figure 4-19 Produce Timing Reports Dialog Box (FPGA)

The dialog box shown in the following figure appears if you are targeting a CPLD.

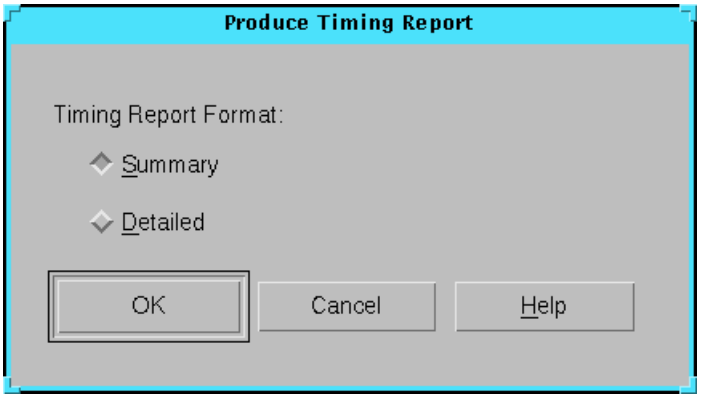


Figure 4-20 Produce Timing Reports Dialog Box (CPLD)

Note: If you step back over a state that was necessary to generate a report, the report associated with that state is removed from the Report Browser. To restore the state and the associated reports, use the Flow → Step command in the Flow Engine.

Produce Timing Report Dialog Box (FPGA)

Select a timing report format. The default is Report Paths Failing Timing Constraints.

- Limit Report to _ Paths per Timing Constraint

  Use this option to set the maximum number of reported paths for each timing constraint. The report displays worst-case paths. Choose Summary, No Limit, or a value from 1 to 10. The Summary report indicates whether your timing constraints are being met and the maximum frequency for your clocks. It also indicates if errors exist. The default setting is 3.

- Report Paths Using Advanced Design Analysis

  Select this option only if you are not supplying any timing constraints in a PCF file. This report contains an analysis that enumerates all clocks and the required OFFSETs for each clock. It also contains an analysis of paths having only combinatorial logic, ordered by delay.

- Report Paths in Timing Constraints

  Select this option to generate a report of the paths and path delays covered by the timing constraints that you specified in your design or UCF file. The number of paths per constraint is limited to the number you specify with the Limit Report to _ Paths per Timing Constraint option.

- Report Paths Failing Timing Constraints

  Select this option to generate an error report. The error report lists timing errors and associated net / path delay information. Failed paths appear listed from worst-case to best-case.

  If a constraint is not met, the report gives the number of items scored, the number of errors encountered, and a detailed break-down of the error. For errors in which the path delays are broken down into individual net and component delays, the report lists each physical element and the logic element from which the physical element was generated. If a constraint is met, the report states the number of items scored, reports no timing errors detected, and issues a brief report line.

The number of errors listed for each constraint is limited to the number you specify with the Limit Report to _ Paths per Timing Constraint option.

Produce Timing Report Dialog Box (CPLD)

Select a timing report format.

- Summary

  Select **`Summary`** to generate a report that contains summary information and design statistics.

- Detailed

  Select **`Detailed`** to generate a report that lists delay information for all nets and paths.

Project Notes (Utilities Menu)

Use this command to open a standard text editor window in which to make notes for the current project. Use the **`File`** → **`Preferences`** command to specify the text editor of your choice.

PROM File Formatter (Tools Menu)

Use this command to launch the PROM File Formatter. Use the PROM File Formatter to format BIT files into a PROM file compatible with Xilinx and third party PROM programmers. You can also use it to concatenate multiple bitstreams into a single PROM file for daisy chain applications.

For online help for this tool, obtain Help from within the PROM File Formatter.

Note: The PROM File Formatter is supported for the FPGA device families only.

Properties (Design Menu)

Use this command to display information about a selected project, design version, or implementation revision. This command opens a dialog box containing information that varies depending on the selected object.

All dialog boxes contain the object name and directory, and a comment field with noted options and strategies. In addition, the Project Properties dialog box contains the input design name and path. The Revision Properties dialog box contains the part type used.

The Project Properties dialog box also contains two buttons, Version List or Revision List. If you click one of these buttons, the Files List dialog box opens, as shown in the following figure. From this dialog box, you can specify files you want to copy to your version or revision directory or a specified subdirectory.

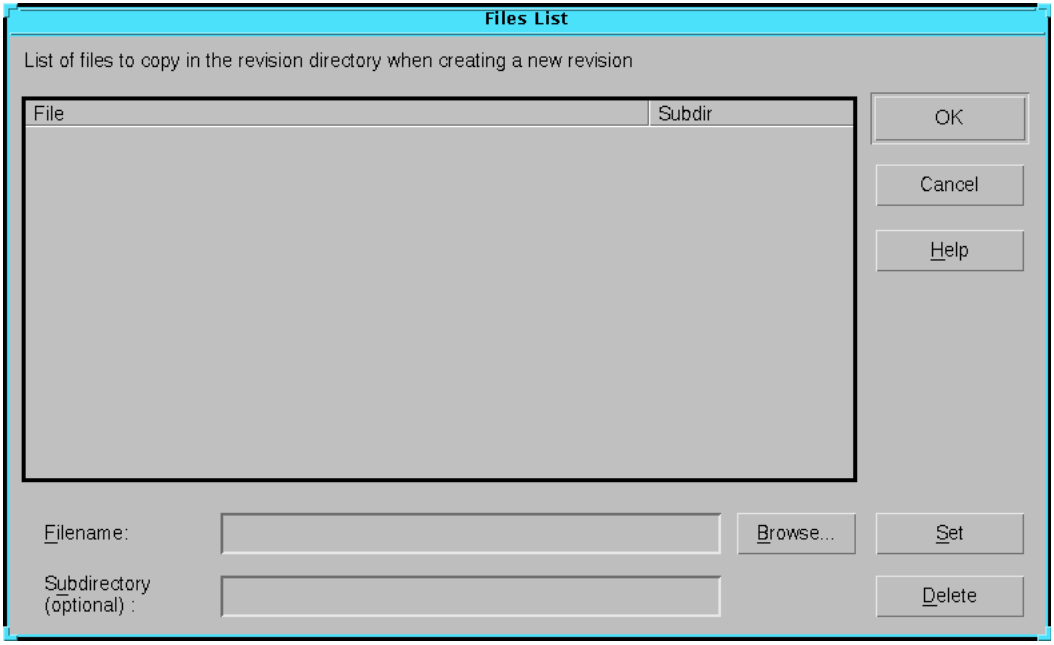


Figure 4-21 Files List Dialog Box

Files List Dialog Box

- File

  This area lists the files you specify in the Filename field.

- Subdir

  This area lists the subdirectories you specify in the Subdirectory field.

- Filename

  Specify the file or files you want to copy to the version or revision directory or subdirectory you specify. Use wildcard characters to specify a multiple file names. Click **Browse** to search for a file.

- Subdirectory (optional)

  Specify the subdirectory into which you want to copy files. The subdirectory is created under the version or revision directory.

- Set

  Click **Set** to set the files and subdirectories you specify.

- Delete

  Click **Delete** to remove the selected file or subdirectory.

Report Browser (Utilities Menu)

Use this command to view reports. The Report Browser command opens the Report Browser utility. This utility contains icons that represent the reports that have been generated by the Flow Engine.

The icons change appearance to indicate whether or not you have read a report. A yellow mark in the upper left corner of the report icon indicates that the report has been generated but not read. A report icon without this mark indicates that the report has been generated and read.

To read a report, double-click the report icon. The report opens in the text editor that you specified with the **File** → **Preferences** command.

Run (Flow Menu)

Use this command to start the Flow Engine. The Flow Engine processes until it completes the target process or finishes implementing the design.

Save Project (File Menu)

Use this command to save the current project. Using this command ensures that all comments and the state of the project and design version icons are saved.

Note: The Design Manager saves frequently so that data is almost always up to date.

Set Constraints File (Design Menu)

Use this command to bring up the Set Constraints dialog box shown in the following figure. This dialog box allows you to identify a UCF file to constrain your design. You can specify logic placement and timing requirements in the UCF file.

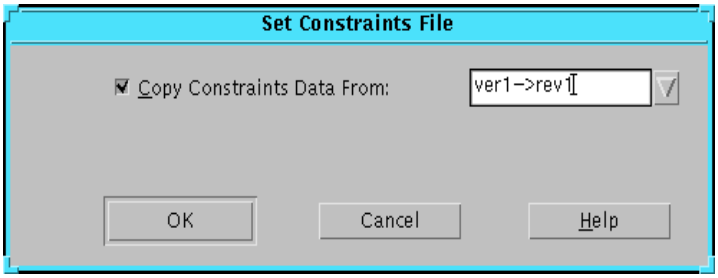


Figure 4-22 Set Constraints Dialog Box

Set Constraints File Dialog Box

This dialog box contains the Copy Constraints Data From option. Select this option to copy a constraints file into the selected implementation revision. The software uses this file to implement the design.

From the drop-down list box, select a revision that contains the UCF file you want to use, or select Custom to open the Custom dialog box and select a specific file. See the following section for information on the Custom dialog box. Select **None** if you do not want to constrain your design based on a previous revision or custom file.

Set Constraints File Custom Dialog Box

This dialog box is shown in the following figure.

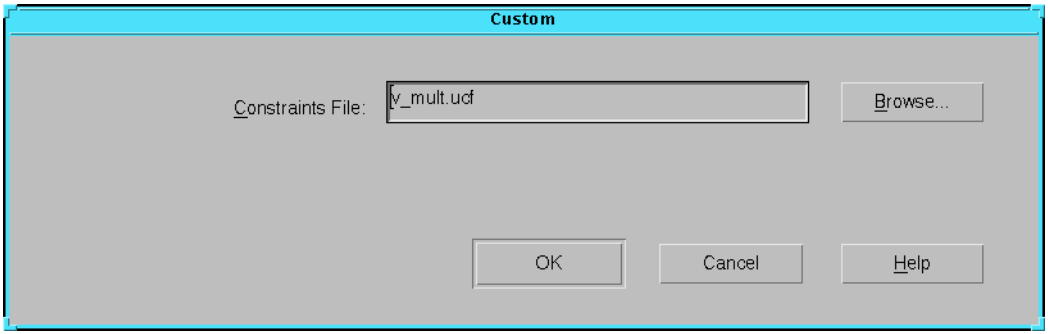


Figure 4-23 Set Constraint File Custom Dialog Box

In the Constraints File field, type the name of a specific file, or click **Browse** to open a file selection dialog box in which you can select an existing UCF file.

Set Floorplan File(s) (Design Menu)

Use this command to open the Set Floorplan File(s) dialog box, shown in the following figure. Use this dialog box to instruct the Design Manager to use information generated by the Floorplanner as a guide for mapping. The Design Manager obtains this information from the Floorplanner MFP file. For information on how to create the MFP file, refer to the *Floorplanner Guide*.

Note: This command is available for the XC4000, Virtex, Spartan, and Spartan2 device families only. If you use this command, you cannot guide mapping using the Design → Set Guide File(s) command Custom option.

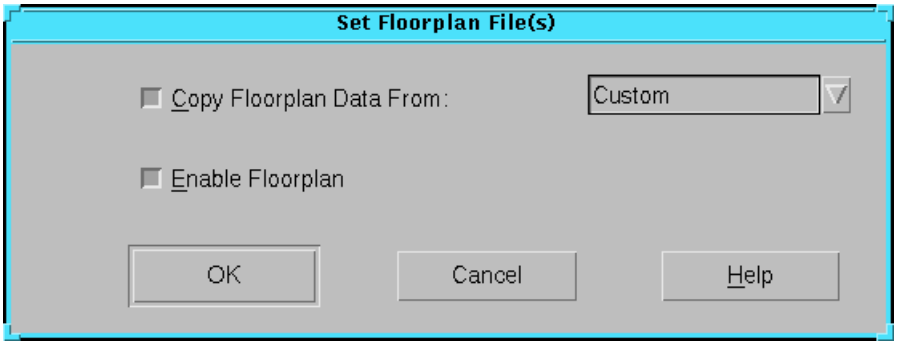


Figure 4-24 Set Floorplan File(s) Dialog Box

Set Floorplan File(s) Dialog Box

This dialog box contains the following options.

- Copy Floorplan Data From

  Select this option to copy a floorplan file into the selected implementation revision. If the Enable Floorplan option is selected, the software uses this file to implement the design.

  From the drop-down list box, select a revision that contains the floorplan files you want to use, or select Custom to open the Custom dialog box and guide from a specific file. See the following section for information on the Custom dialog box. Select **None** if you do not want to copy floorplan data from a previous revision or custom file.

- Enable Floorplan

  By default, this option is enabled and instructs the software to use the specified floorplan file. If you do not want to guide your design in this revision but want to keep your floorplan file intact, disable this option.

Set Floorplan File(s) Custom Dialog Box

This dialog box is shown in the following figure. It contains the following options.

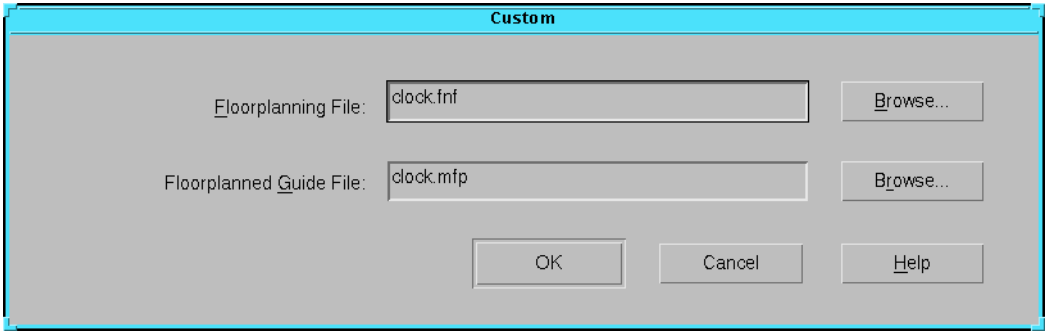


Figure 4-25 Set Floorplan File(s) Custom Dialog Box

- Floorplanning File

  Select an FNF file. Click **Browse** to search for a file.

- Floorplanned Guide File

  Select an MFP file. Click **Browse** to search for a file.

Set Guide File(s) (Design Menu)

Use this command to open the Set Guide File(s) dialog box, shown in the following figure, in which you can specify a guide file. A guide file is created each time you implement your design and you can reuse this data to maintain mapping, placing, and routing consistency for FPGAs and fitting consistency for CPLDs. You can guide from an implementation revision or from a custom guide file. Guiding your design can reduce the amount of time taken for implementation.

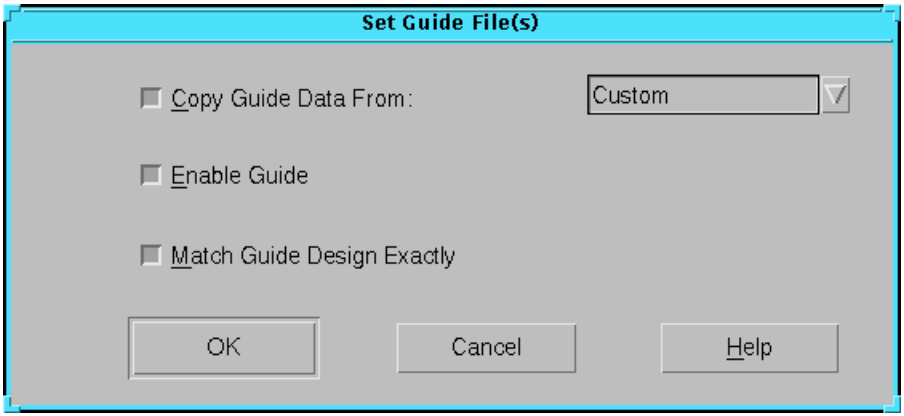


Figure 4-26 Set Guide File(s) Dialog Box

Set Guide File(s) Dialog Box

The following options are available in this dialog box.

- Copy Guide Data From

  Select this option to copy a guide file into the selected implementation revision. If the Enable Guide option is selected, the software uses this file to implement the design.

  From the drop-down list box, select a revision that contains the guide files you want to use, or select Custom to open the Custom dialog box and guide from a specific file. See the following section for information on the Custom dialog box. Select **None** if you do not want to guide from a previous revision or custom file.

Note: If you select a revision, it must be a placed and routed revision. If you want to guide from a mapped file, you must use the Custom option.

- Enable Guide

  By default, this option is enabled and instructs the software to use the specified guide file. If you do not want to guide your design in this revision but want to keep your guide file intact, disable this option.

- Match Guide Design Exactly

  Select this option to lock the placement and routing of the matching logic. This option is useful when you have made minor changes to the design and want to ensure that matching logic is not changed to accommodate additional logic.

  If you do not select this option, the guide files are used as a starting point only. This allows the mapper, placer, and router greater flexibility in accommodating design modifications.

Note: This option is not recommended for synthesis based designs. This option is supported for the FPGA device families only.

Set Guide File(s) Custom Dialog Box

This dialog box is shown in the following figure. It contains the following options.

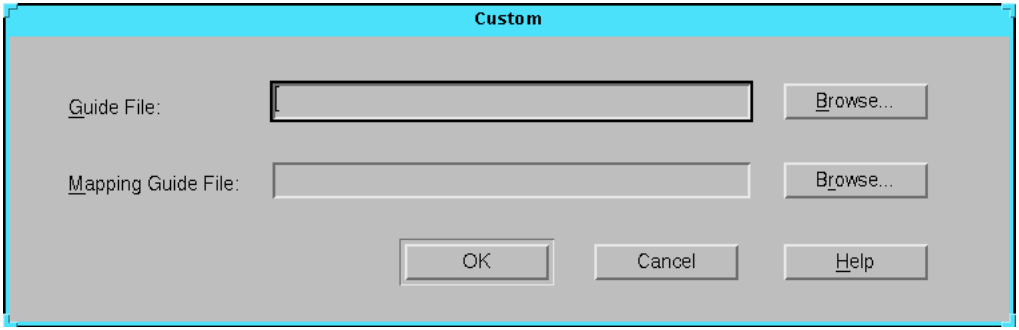


Figure 4-27 Set Guide File(s) Custom Dialog Box

- Guide File

  Specify an NCD file to guide placing and routing for FPGAs. Specify a GYD file to guide fitting for CPLDs. Click **Browse** to search for a file.

- Mapping Guide File

  Specify a file to guide mapping for FPGAs. This option is not supported for CPLDs. Click **Browse** to search for a file.

Note: If you use this option, you cannot guide mapping using the Design → Set Floorplan File(s) command.

Set Part (Design Menu)

Use this command to open the Set Part dialog box shown in the following figure. This command allows you to create a new implementation revision targeted for the part you choose.

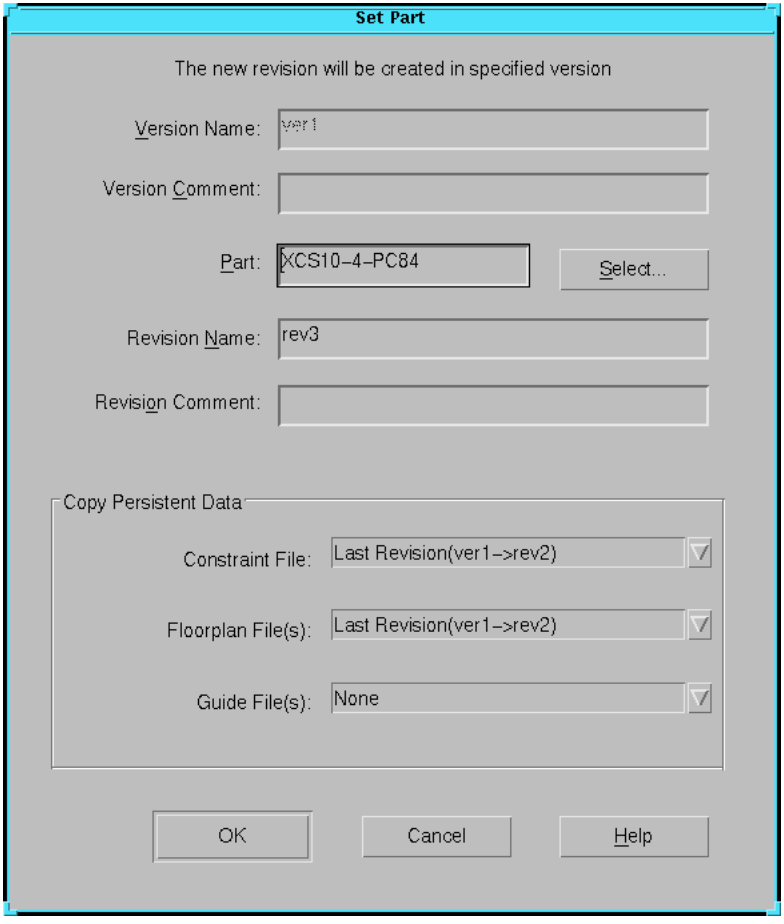


Figure 4-28 Set Part Dialog Box

Note: After the implementation revision is created, the part cannot be changed.

Set Part Dialog Box

The following options are available in this dialog box.

- Version Name

  This option is disabled when setting the part.

- Version Comment

  This option is disabled when setting the part.

- Revision Name

  Enter the revision name for your implementation revision.

Note: When naming revisions, use the characters A through Z, a through z, 0 through 9, period (.), underscore (_), or hyphen (-) only.

- Revision Comment

  Type any comments, including options and strategies. Comments appear in the main window next to the implementation revision icon.

- Part

  Click the **Select** button to the right of the Part field to select a part type from the Part Selector. See the following section for details.

- Copy Persistent Data

  Use the drop down list boxes to the right of the following options to copy constraint, guide, and floorplan data to the new revision.

  - Constraints File
  - Guide File
  - Floorplan File

  When initially creating a project, the Design Manager copies constraints file data from the project directory to the revision directory. By default, floorplan and constraint file data is copied from the “last” revision, that is the bottommost revision in the project view. Guide file data is copied based on your previous setting. You can choose to copy data from a previous revision or a custom file or choose **None** if you do not want to copy data.

Part Selector Dialog Box

This dialog box is shown in the following figure. Set the following options in the Part Selector.

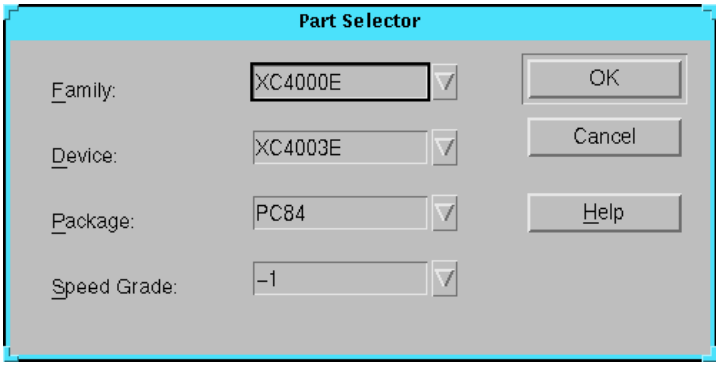


Figure 4-29 Part Selector Dialog Box

- Family

  Specify the family type.

- Device

  Specify the device type. Only the devices that are in the family that you specify in the Family field are displayed in the Devices field.

- Package

  Specify the package type such as PC84, PQ100, or BGA225.

- Speed Grade

  Specify the speed grade of the device.

Status Bar (View Menu)

Use this command to show or hide the status bar.

In the Design Manager, the status bar shows the project name, the part name if an implementation revision is selected, and the name of the selected item.

In the Flow Engine, the status bar shows the target part name for the current implementation revision, the name of the user specified constraints file, and the name of the user specified guide file.

Step (Flow Menu)

Use this command to run the next step in the processing flow. This command allows you to single-step through the implementation process.

Note: You can use the Implementation State option in the Advanced dialog box to restore an implementation state when you have stepped forward too far.

Step Back (Flow Menu)

Use this command to go back one step in the processing flow. You can use this command to back up and rerun a step using different options. The data is not deleted until you overwrite it by rerunning the step.

Note: You can use the Implementation State option in the Advanced dialog box to restore an implementation state when you have stepped back too far.

Stop After (Setup Menu)

Use this command to specify a target break point where the Flow Engine will stop processing. Choose a process from the Stop After dialog box, shown in the following figure. For instance, if you want to map, place, and route your design but not create a timing simulation file or device programming file, select Stop After Place&Route.

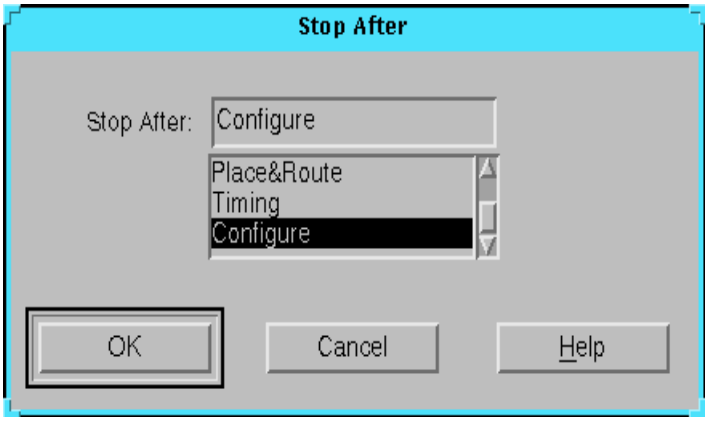


Figure 4-30 Stop After Dialog Box

Stop After Dialog Box

Select a target break point from the Stop After list box. When working with an FPGA the available targets are Translate, Map, Place & Route, Timing (Sim), and Configure. When working with a CPLD the available targets are Translate, Fit, Timing (Sim), and Bitstream. The selected target appears in the Stop After field.

Template Manager (Utilities Menu)

Use this command to create or modify your implementation, simulation, and configuration option templates. Templates provide a convenient way to have several groups of option settings that you can select from when you implement a design. Implementation and simulation options are supported for FPGAs and CPLDs. Configuration options are supported for FPGAs.

The Template Manager command opens the dialog box shown in the following figure. For more information on how to use the Template Manager, see the “Working with Templates” section of the “Using the Design Manager and Flow Engine” chapter.

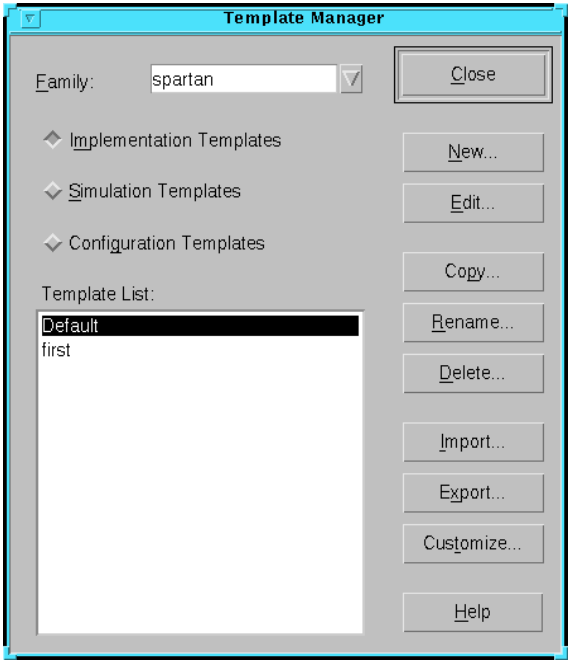


Figure 4-31 Template Manager Dialog Box

Template Manager Dialog Box

The following options are available in this dialog box.

- Family

  Select the device family of the option templates you want to create or modify.

- Implementation Templates

  Select this option to work with implementation option templates. Implementation options control how an FPGA design is translated, mapped, optimized, placed, and routed and how a CPLD design is translated and fitted.

- Simulation Templates

  Select this option to work with simulation option templates. Simulation options control the creation of netlists for front and

back-end simulation. Simulation can be performed on both pre- and post-routed designs.

- Configuration Templates

  Select this option to work with configuration option templates. Configuration options control the configuration startup, read-back, and parameters for the device.

Note: Configuration options are available for FPGA devices only.

- Template List

  Select an option template with which to work. If you are working with simulation options, select the name of your simulator.

- Close

  Click **Close** to close the Template Manager.

- New

  Click **New** to add a new option template. This allows you to create multiple templates with different settings.

- Edit

  Click **Edit** to open the Implementation, Simulation, or Configuration Options dialog box to view and modify the settings for a particular option template.

- Copy

  Click **Copy** to make a copy of the selected option template.

- Rename

  Click **Rename** to rename the selected option template. You cannot rename the default set of options.

- Delete

  Click **Delete** to delete the selected option template. You cannot delete the default set of options.

- Import

  Click **Import** to import a template file. A template file contains one or more option templates. Clicking Import opens a standard file selection dialog box in which you can choose a template file to import. The templates read from the file appear in the

Template List area of the Template Manager. You can transfer a template from one Design Manager project to another by using the Export option followed by the Import option.

- Export

  Click **Export** to export option templates to a template file. A template file contains one or more option templates. You can select the templates you want to export from the Template List area of the Template Manager. Clicking Export opens a standard file selection dialog box in which you can specify the template file name. You can transfer a template from one Design Manager project to another by using the Export option followed by the Import option.

- Customize

  Click **Customize** to open the Customize Options dialog box. Use this dialog box to specify custom template options that are provided by other programs but are not supported by the standard options provided in the Design Manager. You can use any options that the programs support. For more information on the commands and options for the programs, refer to their user manuals.

Customize Options Dialog Box

This dialog box is shown in the following figure. The following options are available in this dialog box.

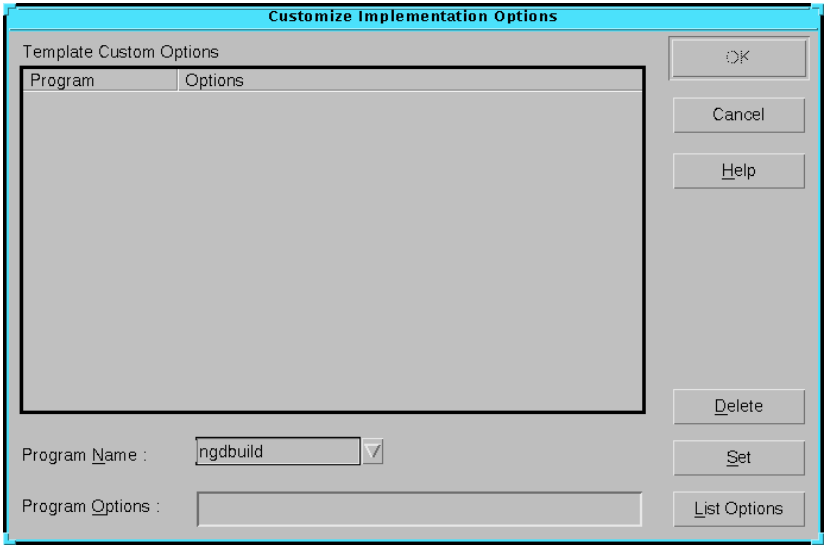


Figure 4-32 Customize Options Dialog Box

Note: The title of this dialog box changes based on whether you are working with implementation, simulation, or configuration options.

- Template Custom Options

  This area lists the programs and options you specify in the Program Name and Program Options fields.

- Program Name

  Select the name of the program or programs that you want to use from the drop-down list box. This list box contains only the programs that apply for the template type and part family that you chose.

- Program Options

  Specify the program options that you want to use. Enter the options as they would appear on the command line.

Note: Any options you have entered previously are saved and appear the next time you open this dialog box.

- List Options

  Click **List Options** to open a file that lists the options and usage messages associated with the selected program. If the options differ according to a device family, the options are listed broken into families. The file opens in the text editor you set using the File → Preferences command.

- Set

  Click **Set** to set the programs and options that you specify.

- Delete

  Click **Delete** to remove the selected program or option.

Note: It is possible to enter options in the Customize Options dialog box that can conflict with normal Flow Engine options. It is beyond the scope of this manual to explain all the possible conflicts.

Timing Analyzer (Tools Menu)

Use this command to launch the Timing Analyzer. Use the Timing Analyzer after a design has been mapped, routed, or fitted. The Timing Analyzer performs a static timing analysis of a mapped or routed FPGA or fitted CPLD design. A static timing analysis is a point-to-point analysis of a design network. It does not include insertion of stimulus vectors.

The Timing Analyzer verifies that the delay along a given path or paths meets your specified timing requirements. It organizes and displays data that indicate the critical paths in your circuit, the cycle time of the circuit, the delay along any specified paths, and the paths with the greatest delay. It also provides a quick analysis of the effect of different speed grades on the design.

The Timing Analyzer works with synchronous systems composed of flip-flops and combinatorial logic. In a synchronous design, signals must be stable long enough to allow the clocks to change so that setup and hold violations are avoided.

For online help for the this tool, obtain Help from within the Timing Analyzer.

Toolbar (View Menu)

Use this command to show or hide the toolbar.

Toolbox (View Menu)

Use this command to show or hide the toolbox.

Update Flow (Setup Menu)

Use this command to determine whether a change has been made that would cause a successfully run step to be rerun. If the Flow Engine determines that a process needs to be rerun, it presents a confirmation dialog box. Click **Yes** and the flow is reset to run the appropriate step next. See the "Smart Flow Engine Change Detection" table of the "Introduction" chapter for information on which file changes cause steps to be rerun.

Note: The Flow Engine will not automatically begin processing the appropriate step, you must select **Flow** → **Run** or **Flow** → **Step** to begin the implementation process.

Xilinx on the Web (Help Menu)

This cascading menu command allows you to access Xilinx web pages through a Web browser. Use the File → Preferences command to set the Web browser of your choice. You must have Web access to use these commands.

Use the **Support and Services** command to open the Xilinx technical support page. Use this page to access the latest design information, to search across various resources, and to access online resources directly.

Use the **Xilinx Home Page** command to open the Xilinx home page. This page contains links to the latest Xilinx announcements, technical support, and information on the company, its products, and investor relations.

Toolbars

Toolbars provide convenient access to frequently used commands. Click once on a toolbar button to execute a command.

If you position the mouse pointer over a toolbar button, a short description, called a tool tip, appears next to the button and a longer description appears in the status bar at the bottom of the main window.

Design Manager Toolbar Buttons

This section briefly describes the function of each Design Manager toolbar button and includes a graphic of each button.

Implement

The Implement button runs the implementation flow. It is equivalent to the Design → Implement command.

Set Options

The Set Options button opens the Options dialog box. It is equivalent to the Design → Options command.

New Project

The New Project button creates a new project. It is equivalent to the File → New Project command.

Open Project

The Open Project button opens an existing project. It is equivalent to the File → Open Project command.

Save Project

The Save Project button saves the current project. It is equivalent to the File → Save Project command.

Set Part

The Set Part button allows you to select the device to use in creating a new implementation revision. It is equivalent to the Design → Set Part command.

New Revision

The New Revision button creates a new implementation revision. It is equivalent to the Design → New Revision command.

Copy Revision

The Copy Revision button makes a copy of the selected implementation revision. It is equivalent to the Design → Copy Revision command.

Browse Reports

The Browse Reports button opens the Report Browser for viewing reports. It is equivalent to the Utilities → Report Browser command.

Edit Project Notes

The Edit Project Notes button opens a text editor window in which to enter notes for the project. It is equivalent to the Utilities → Project Notes command.

View Command History

The View Command History button opens a command history utility which displays the command history for the selected implementation revision. It is equivalent to the Utilities → Command History command.

Online Support

The Online Support button opens the Xilinx technical support page. Use this page to access the latest design information, to search across various resources, and to access online resources directly. It is equivalent to the Help → Xilinx on the Web → Support and Services command. You must have Web access to use this toolbar button.

Help

The Help button opens context-sensitive help.

Flow Engine Toolbar Buttons

This section briefly describes the function of each Flow Engine toolbar button and includes a graphic of each button.

Set Options

The Set Options button opens the Options dialog box. It is equivalent to the Setup → Options command.

Browse Reports

The Browse Reports button opens the Report Browser tool for viewing reports. It is equivalent to the Utilities → Report Browser command.

Command History

The Command History button opens a command history utility which displays commands that have been run for the current implementation revision. It is equivalent to the Utilities → Command History command.

Preview Commands

The Preview Commands button opens a utility which displays the commands that will be run on the current implementation revision. It is equivalent to the Utilities → Command Preview command.

Set Target

The Set Target button opens the Stop After dialog box from which you specify a processing break point. It is equivalent to the Setup → Stop After command.

Help

The Help button opens context-sensitive help.

Toolbox

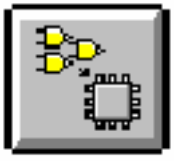
The toolbox provides buttons to access the tools in the Xilinx Development System. Click a toolbox button once to launch a tool. You can also launch these tools from the Tools menu.

The toolbox contents depend on the selected implementation revision. Each time you select an implementation revision, the toolbox changes automatically. The toolbox contents differ for FPGAs and CPLDs as indicated in the following sections.

If you position the mouse pointer over a toolbox button, a tool tip appears next to the button and a longer description appears in the status bar at the bottom of the Design Manager window.

Flow Engine

The Flow Engine button launches the Flow Engine, which implements a design. It is equivalent to the Tools → Flow Engine command and is supported for FPGAs and CPLDs.



Timing Analyzer

The Timing Analyzer button launches the Timing Analyzer, which performs timing analysis on a design. It is equivalent to the Tools → Timing Analyzer command and is supported for FPGAs and CPLDs.

Floorplanner

The Floorplanner button launches the Floorplanner, which allows you to graphically place your design into a target FPGA. It is equivalent to the Tools → Floorplanner command and is supported for all XC4000 families and the Virtex, Spartan/XL, and Spartan2 device families only.

PROM File Formatter

The PROM File Formatter button launches the PROM File Formatter, which creates a PROM file or series of PROM files. It is equivalent to the Tools → PROM File Formatter command and is supported for FPGAs only.

Hardware Debugger

The Hardware Debugger button launches the Hardware Debugger, which downloads a design to a device and interactively debugs the design while in circuit. It is equivalent to the Tools → Hardware Debugger command and is supported for FPGAs only.

FPGA Editor

The FPGA Editor button launches the FPGA Editor, which allows you to graphically examine your placed and routed designs. It is equivalent to the Tools → FPGA Editor command and is supported for FPGAs only.

Chip Viewer

The Chip Viewer button launches the Chip Viewer, which allows you to graphically examine your fitted designs. It is equivalent to the Tools → Chip Viewer command and is supported for CPLDs only.

JTAG Programmer

The JTAG Programmer button launches the JTAG Programmer, which downloads a design and configures a device from the XC4000, XC5200, Virtex, Spartan / XL, or Spartan2 FPGA families or XC9500 CPLD family. It is equivalent to the Tools → JTAG Programmer command.

Run Control

The Flow Engine contains run control buttons that provide convenient access to the Flow menu commands. Click once on a run control button to execute a command.

If you position the mouse pointer over a run control button, a short description, called a tool tip, appears next to the button.

Run

Use this command to start the Flow Engine. It is equivalent to the Flow → Run command.

Step

Use this command to run the next operation in the processing flow. It is equivalent to the Flow → Step command.

Step Back

Use this command to go back one step in the processing flow. It is equivalent to the Flow → Step Back command.

Abort

The Abort button aborts the currently running process. All data from the currently running process is lost. It is equivalent to the Flow → Abort command.

Popup Menus

The right mouse button provides quick access to frequently used commands.

Design Manager Popup Menus

The following commands are active in the project view of the Design Manager main window. To access a command, select a project, design version, or implementation revision icon, press the right mouse button while positioned in the horizontal line of the selected object, and choose the appropriate command from the popup menu. The following commands are available.

- Collapse/Expand

  Select this command to expand or collapse the project or design version hierarchy. This command is the same as double-clicking the project or design version icon. There is no equivalent menu command.

Note: The Collapse/Expand command only applies to selected projects and design versions.

- Re-Implement

  Select **Re-Implement** to launch the Flow Engine on the selected implementation revision. The Flow Engine determines where it should start running in the flow and implements your revision to completion. There is no equivalent menu command.

Note: This command is only available when positioned over an implementation revision.

- Implement

  Select **Implement** to implement the "last" implementation revision, that is the bottommost revision in the Design Manager project view. See the "Implement (Design Menu)" section of this chapter.

Note: This command is only available when positioned over a project or design version.

- Delete

  Select **Delete** to delete the selected project, design version, or implementation revision. See the "Delete (Design Menu)" section of this chapter.

- Properties

  Select **Properties** to display information about a selected project, design version, or implementation revision. See the "Properties (Design Menu)" section of this chapter.

Flow Engine Popup Menus

The following mouse menu commands are active in the Flow Engine message log window. To access a command, press the right mouse button in the Flow Engine message log window and choose the appropriate command from the popup menu. There are no equivalent menu commands for these mouse commands.

- Copy

  Select **Copy** to copy selected text to the clipboard.

- Find

  Select **Find** to search for a text string.

Keyboard Shortcuts

You can use the following keyboard shortcuts in the Design Manager.

- Ctrl N

  In the Design Manager, press **Ctrl N** to access the File → New Project command.

- Ctrl O

  In the Design Manager, press **Ctrl O** to access the File → Open Project command.

- Ctrl S

  In the Design Manager, press **Ctrl S** to access the File → Save Project command.

Chapter 5

Implementation Flow Options

This chapter describes the Flow Engine implementation flow options, which control how the Flow Engine implements a design. This chapter contains the following sections.

- “Spartan Implementation Options”
- “Spartan Simulation Options”
- “Spartan Configuration Options”
- “Spartan2 Implementation Options”
- “Spartan2 Simulation Options”
- “Spartan2 Configuration Options”
- “Virtex Implementation Options”
- “Virtex Simulation Options”
- “Virtex Configuration Options”
- “XC3000 Implementation Options”
- “XC3000 Simulation Options”
- “XC3000 Configuration Options”
- “XC4000 Implementation Options”
- “XC4000 Simulation Options”
- “XC4000 Configuration Options”
- “XC5200 Implementation Options”
- “XC5200 Simulation Options”
- “XC5200 Configuration Options”

- "XC9500 Implementation Options"
- "XC9500 Simulation Options"

Spartan Implementation Options

Click the Translate, Optimize and Map, Place and Route, or Timing Reports tab to access the different options within the Implementation Options dialog box. These options affect the Translate, Map, and Place&Route steps in the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

- "Spartan Translate Tab"
- "Spartan Optimize and Map Tab"
- "Spartan Place and Route Tab"
- "Spartan Timing Reports Tab"

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

Spartan Translate Tab

Use this tab, shown in the following figure, to set the following options.

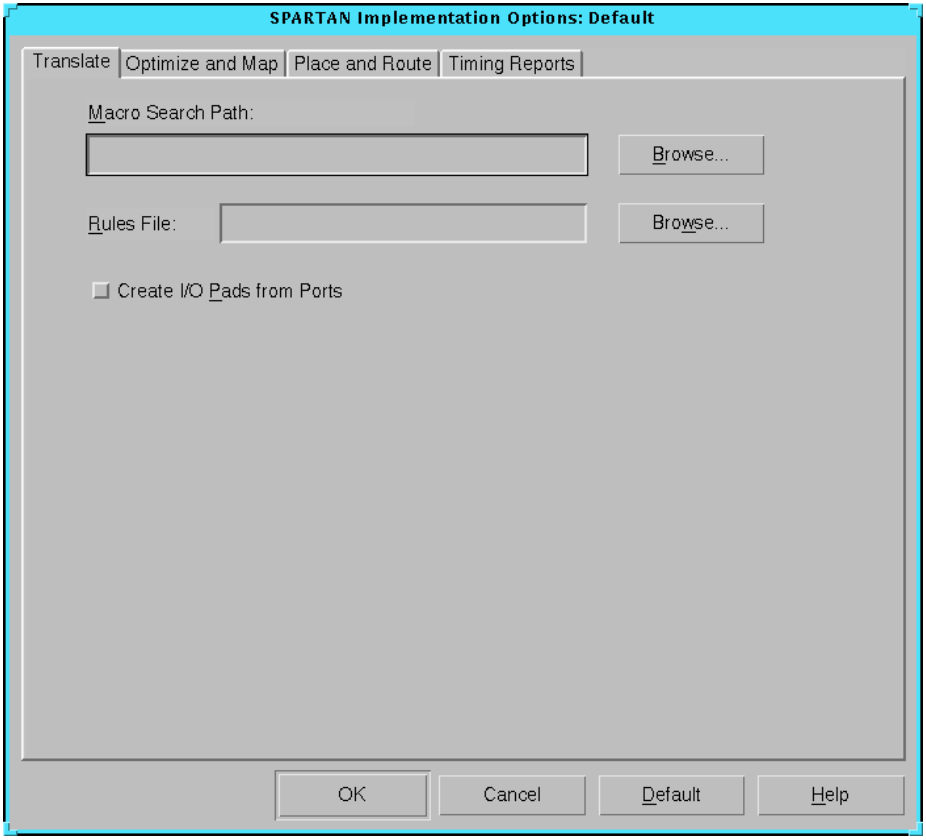


Figure 5-1 Spartan Translate Tab

Macro Search Path

Use this option to add the specified search path to the list of directories to search when resolving file references (that is, files specified in the schematic with FILE=*filename* property). This option also supplies paths for macros (*design_name*.nmc) or other directories containing NGO files. Specify a macro search path or click **Browse** to look for a path to add as a macro search path.

To specify multiple search paths, type in each directory name separated by a semicolon (;). A semicolon is automatically appended when you use the Browse button to select multiple search paths.

Rules File

Use this option to specify which executables are used to convert outside netlists to NGO netlists. Specify a rules file or click **Browse** to look for a file to add as a rules file.

Create I/O Pads from Ports

This option adds PAD properties to all top level port signals. Select this option if your simulation netlist format is an EDIF file in which PAD symbols were translated into ports. If you do not select this option for one of these EDIF files, the mapper reads the design incorrectly. By default, this option is off.

Note: PAD symbols are translated into ports in all Mentor Graphics and Cadence EDIF files. This option is set automatically for EDIF files from either of these vendors.

Spartan Optimize and Map Tab

Use this tab, shown in the following figure, to set the following options.

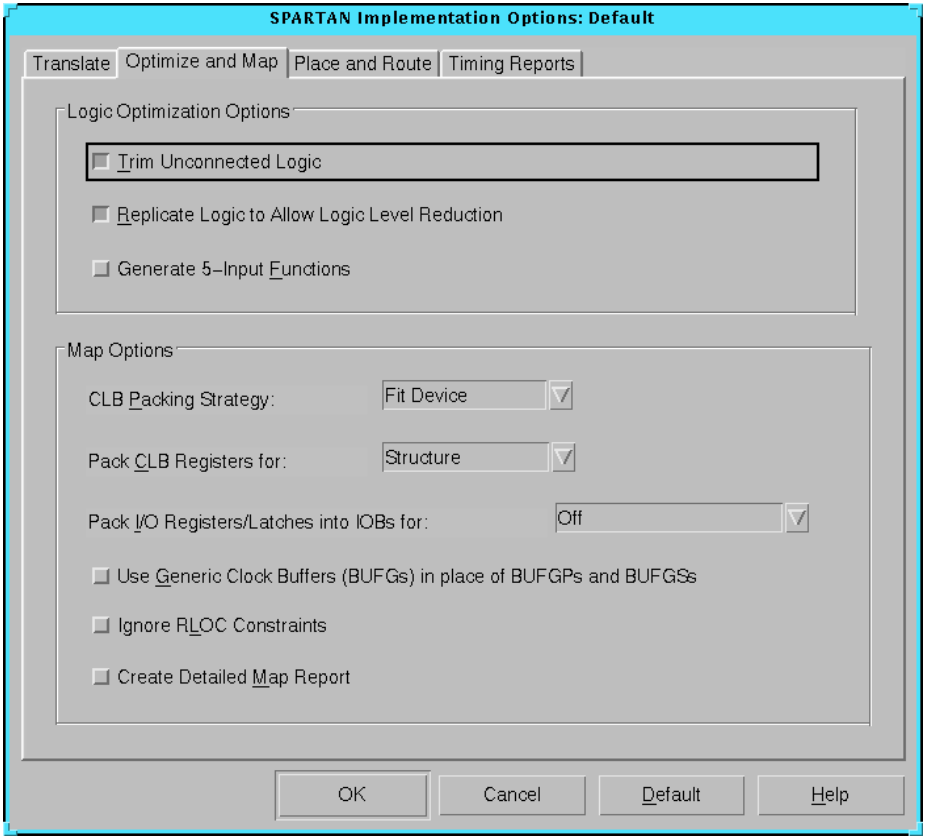


Figure 5-2 Spartan Optimize and Map Tab

Logic Optimization Options

The Logic Optimization Options group box contains the following options.

- Trim Unconnected Logic

  Select this option to trim unconnected components and nets from the design before mapping occurs. Deselect this option to map unconnected components and nets. Deselecting this option is

useful for estimating the logic resources required for a design and for obtaining timing information on partially finished designs. When implementing an unfinished design, deselect this option to prevent partial logic from being trimmed. By default, this option is on.

- Replicate Logic to Allow Logic Level Reduction

  Use this option to replicate a single driver that drives multiple loads and map it as separate components that drive individual loads. This option is useful for creating a mapping strategy that may more readily meet your timing constraints. It reduces the number of logic elements through which a signal must pass, thereby eliminating path delays. By default, this option is on.

- Generate 5-Input Functions

  Select this option to map each five-input logic function to a single CLB. This option can sometimes reduce the number of cell-to-cell delays at the expense of increased CLB count. By default, this option is off.

Map Options

The Map Options group box contains the following options.

- CLB Packing Strategy

  This option partitions logic more densely. Normally, the mapper partitions logic to maximize signal sharing within CLBs and to minimize routing congestion. The CLB Packing Strategy option optimizes density by relaxing the requirement for a high degree of signal sharing between logic elements in a CLB, using the DI (direct flip-flop input) pins on CLBs, and reducing minimum signal combining requirements. The default is Fit Device.

Note: Although the CLB Packing Strategy option makes a design denser, it can also adversely affect place and route performance, resulting in higher delays and more unrouted nets. Use this option if you are willing to trade performance for density.

- Fit Device

  Select **`Fit Device`** to pack logic elements that do not share common signals into the CLBs. The mapper continues packing until the design fits into the selected device or no further packing is possible.

- Off

  Select **Off** to disable the CLB Packing Strategy option. Disabling this option causes only related logic (logic with common inputs) to be packed together. This is useful for increasing speed in high speed designs. However, the design may overflow the selected part due to the increase in CLBs used.

- Pack CLB Registers for

  This option controls register ordering. When you map a design containing registers, the mapper can optimize the way the registers are grouped into CLBs. This optimized mapping is called register ordering. For more information on register ordering, see the "Register Ordering" section of the *Development System Reference Guide*. The default is Structure.

  - Structure

    Select **Structure** to enable register ordering. The mapper will look at the register bit names for similarities and try to map register bits in an ordered manner.

  - Minimum Area

    Select **Minimum Area** to disable register ordering for a denser design. Register bit names will be ignored when registers are mapped, and the bits will not be mapped in any special order.

- Pack I/O Registers/Latches into IOBs for

  This option controls the packing of flip-flops or latches within an I/O cell. Normally, the mapper packs flip-flops or latches within an I/O cell only if such packing is specified by your design entry method. This option allows you to control packing after the design entry phase. The default is Off.

  - Inputs Only

    Select **Inputs Only** to pack flip-flops or latches into input I/O cells.

  - Outputs Only

    Select **Outputs Only** to pack flip-flops or latches into output I/O cells.

- Inputs and Outputs

  Select **`Inputs and Outputs`** to pack flip-flops or latches into both input and output I/O cells.

- Off

  Select **`Off`** to pack flip-flops or latches as specified by your design entry method.

- Use Generic Clock Buffers (BUFGs) in place of BUFGPs and BUFGSs

  Select this option to replace primary and secondary clock buffers with generic clock buffers before mapping occurs. This option is useful when working with design entry tools that generate only BUFGPs or BUFGSs. By default, this option is off.

- Ignore RLOC Constraints

  Select this option to cause Map to ignore the RLOC information that contains the relative placement of one CLB to another. This option also causes Map to ignore any invalid RLOC information that would result in a Map error. By default, this option is off.

Note: To ensure CLBs containing carry logic are aligned properly, Map retains the RLOC information that dictates what is packed into an individual CLB.

- Create Detailed Map Report

  Select this option to create a detailed Map report that includes signal and symbol cross-reference information. By default, this option is off.

Spartan Place and Route Tab

Use this tab, shown in the following figure, to set the following options.

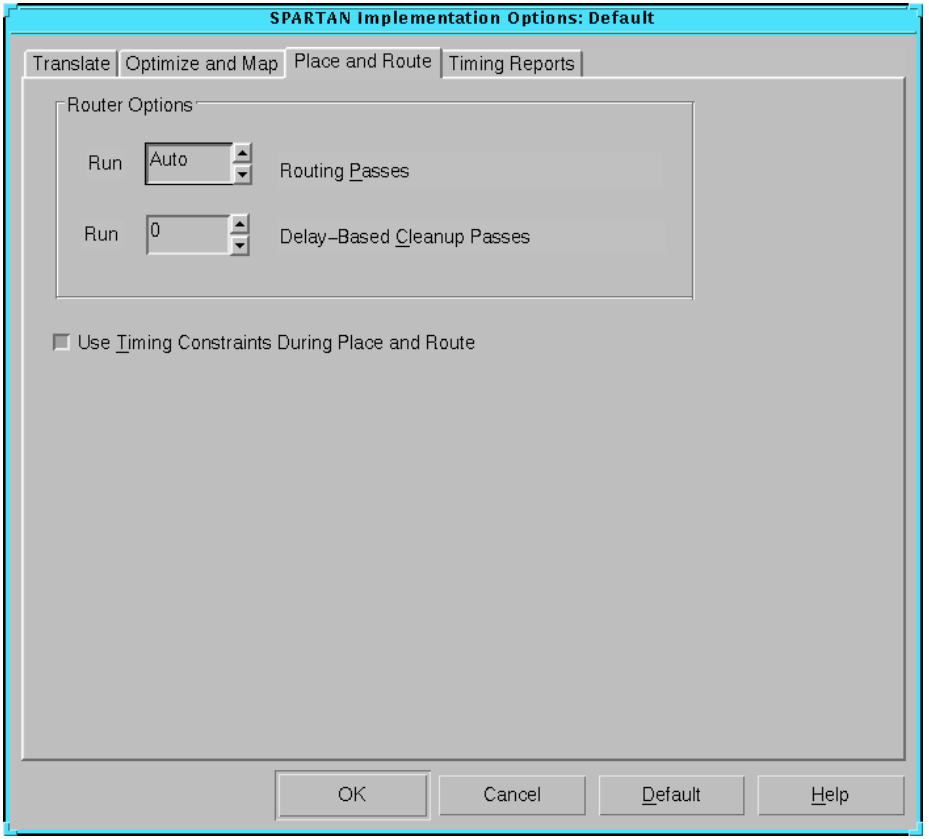


Figure 5-3 Spartan Place and Route Tab

Router Options

The Router Options group box contains the following options.

- Run _ Routing Passes

  Use this option to set the maximum number of routing passes that the router runs in a design. The router attempts to

completely route a placement with each pass. You can set the number of passes to a value from 1 to 1000 or to Auto.

Auto runs the router until specific exit conditions are met. At place and route effort levels of 3, 4, or 5, the router runs until it routes to 100% completion and meets all timing constraints or until it determines it cannot complete the routing. At levels of 1 or 2, the router stops after a predetermined number of passes. With all settings, the router exits immediately after it routes all connections and meets all timing constraints. A higher number of passes provides better routing results at the expense of longer run times. The default is Auto.

- Run _ Delay-Based Cleanup Passes

  Use this option to further optimize routing of an already routed design. The router makes routing decisions based on computed delay times between sources and loads on the routed nets, and reroutes to minimize the delays. Set the number of delay-based cleanup passes you want to run by choosing a number from 1 to 5. The default is 0.

Use Timing Constraints During Place and Route

Select this option to produce a high-performance implementation of the design. The router uses the timing constraints in the design file to place and route the design within the specified constraints. Deselect this option to ignore timing constraints. This reduces implementation time at the expense of timing performance. By default, this option is on.

Spartan Timing Reports Tab

Use this tab, shown in the following figure, to set the following options.

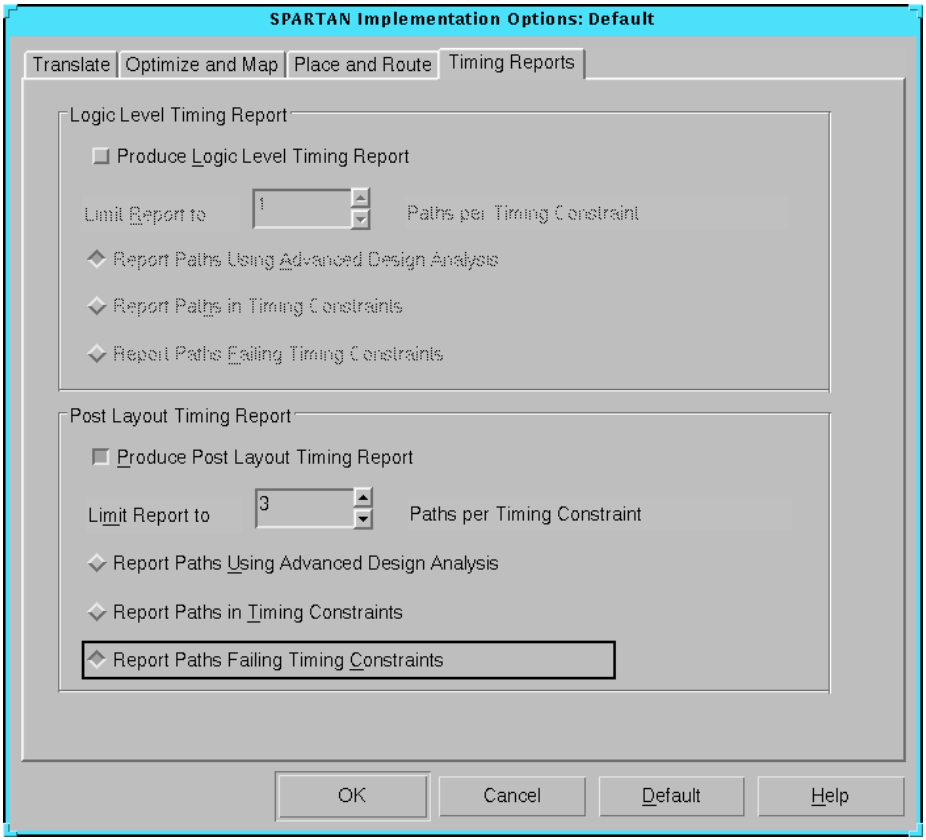


Figure 5-4 Spartan Timing Reports Tab

Logic Level Timing Report/Post Layout Timing Report

Choose whether you want to generate a logic level timing report, a post layout timing report, or both.

Note: When the Logic Level Timing Report option is enabled, the report is automatically generated as part of the Map step. When the

Post Layout Timing Report option is enabled, the report is automatically generated as part of the Place and Route steps.

- Produce Logic Level Timing Report

  Select this option to produce a timing report prior to place and route but after map. The timing report provides a summary analysis of your timing constraints based on block delays and estimates of route delays. You can use this report to determine whether you need to revise the timing constraints in your design or create more efficient logic. This feature provides a useful analysis of your timing constraints without the wait required for place and route. To obtain a detailed analysis, use the Timing Analyzer tool after you place and route the design. By default, this option is off.

- Produce Post Layout Timing Report

  Select this option to produce a timing report. The timing report provides a brief analysis of the maximum clock speed for the design after it is placed and routed. To obtain a detailed analysis, use the Timing Analyzer tool. By default, this option is on.

Both the Logic Level Timing Report and Post Layout Timing Report group boxes contain the following options, which control the number of reported paths for each timing constraint and the format of the report. The default timing report format is Report Paths Failing Timing Constraints.

At the top of each type of report, there is descriptive information such as the software version of the application, the name of the design file, the input physical constraints (PCF) file name, the device speed and the report level. A timing summary always appears at the end of the report. For error and path reports, entries are ordered by constraint and, within constraints, by slack (the difference between the constraint and the analyzed value, with a negative slack indicating an error condition). Error and path reports also contain a list of all time groups defined in the PCF file and all of the members defined within each group.

- Limit Report to _ Paths per Timing Constraint

  Use this option to set the maximum number of reported paths for each timing constraint. The report displays worst-case paths. Choose Summary, No Limit, or a value from 1 to 10. The Summary report indicates whether your timing constraints are

being met and the maximum frequency for your clocks. It also indicates if errors exist.

The default setting is 1 for the Logic Level Timing Report and 3 for the Post Layout Timing Report.

- Report Paths Using Advanced Design Analysis

  Select this option only if you are not supplying any timing constraints in a PCF file. This report contains an analysis that enumerates all clocks and the required OFFSETs for each clock. It also contains an analysis of paths having only combinatorial logic, ordered by delay.

- Report Paths in Timing Constraints

  Select this option to generate a report of the paths and path delays covered by the timing constraints that you specified in your design or UCF file. The number of paths per constraint is limited to the number you specify with the Limit Report to _ Paths per Timing Constraint option.

- Report Paths Failing Timing Constraints

  Select this option to generate an error report. The error report lists timing errors and associated net / path delay information. Failed paths appear listed from worst-case to best-case.

  If a constraint is not met, the report gives the number of items scored, the number of errors encountered, and a detailed break-down of the error. For errors in which the path delays are broken down into individual net and component delays, the report lists each physical element and the logic element from which the physical element was generated. If a constraint is met, the report states the number of items scored, reports no timing errors detected, and issues a brief report line.

  The number of errors listed for each constraint is limited to the number you specify with the Limit Report to _ Paths per Timing Constraint option.

Spartan Simulation Options

Click the General, VHDL / Verilog, or EDIF tab to access the different options within the Simulation Options dialog box. These options affect the timing simulation data produced during the Timing (Sim)

step of the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

- "Spartan General Tab"
- "Spartan VHDL / Verilog Tab"
- "Spartan EDIF Tab"

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

Spartan General Tab

Use this tab, shown in the following figure, to set the following options.

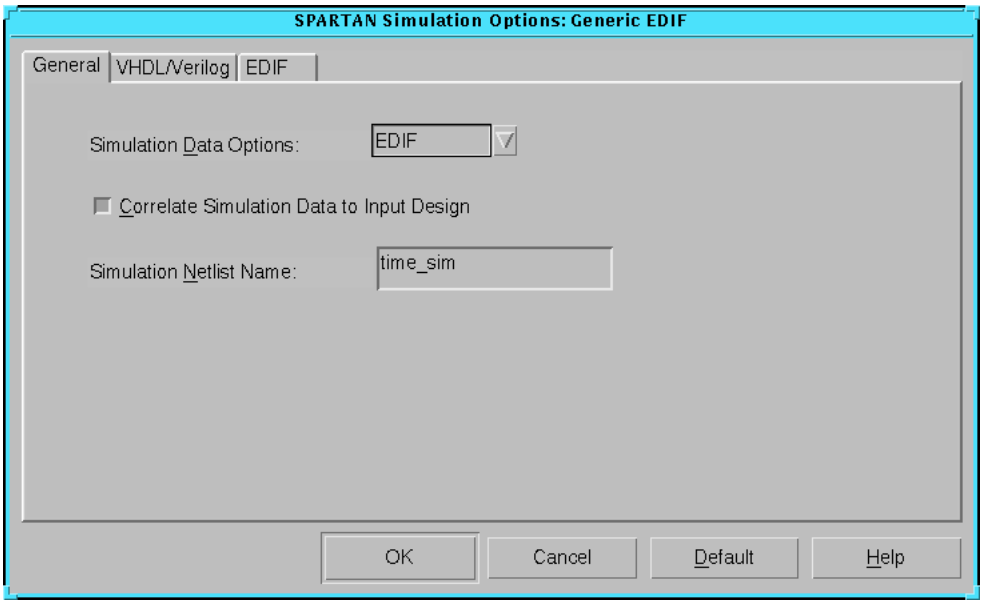


Figure 5-5 Spartan General Tab

Simulation Data Options

Specify the netlist format to use for simulation. The following formats are available.

- EDIF
- VHDL
- Verilog

Correlate Simulation Data to Input Design

Select this option to create a timing simulation netlist that contains the same logic gates and net names as those in the original schematic. Deselect this option to create a timing simulation netlist that contains the same logic gates and net names as those in the optimized implemented netlist.

Simulation Netlist Name

Select this option to specify the name of the output file. This allows you to control the output netlist name to avoid overwriting any files. The default name is time_sim.

Spartan VHDL/Verilog Tab

Use this tab, shown in the following figure, to set the following options.

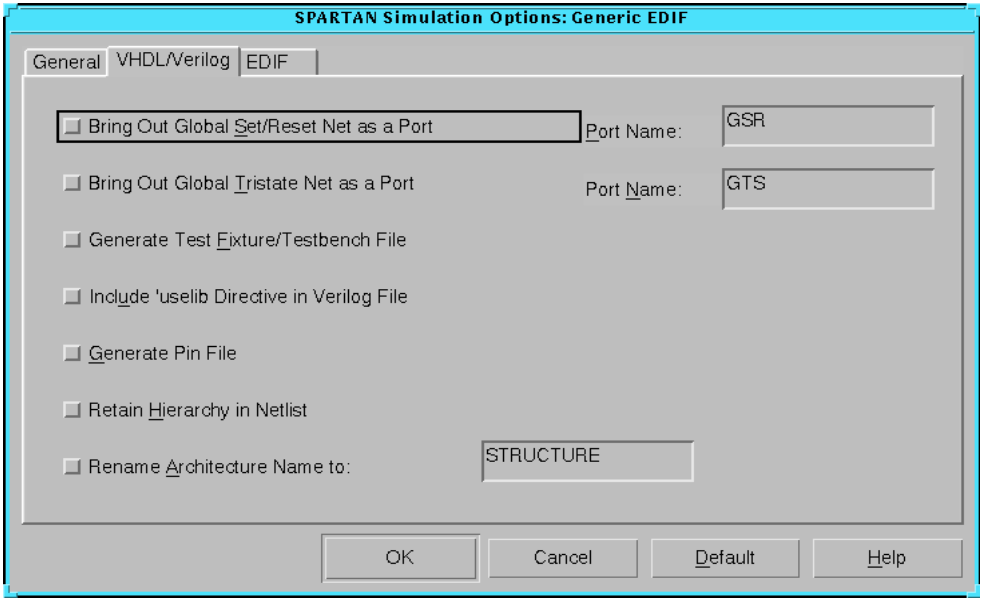


Figure 5-6 Spartan VHDL/Verilog Tab

Bring Out Global Set/Reset Net as a Port

This option creates a Global Set/Reset port on the top-level simulation module (entity). This port is connected to all flip-flop and latch primitives in the design. Stimulating this port automatically sets or resets every flip-flop and latch to its initial state, as determined in the

design. The default name of the Global Set/Reset port depends on the target device family as described in the following table.

Table 5-1 Global Set/Reset Port Information

Device Family	Port Name	When Top-Level Global Set/Reset Port Appears	Polarity
Spartan	GSR	per design or when option is used	active-High
Spartan2	GSR	per design or when option is used	active-High
Virtex	GSR	per design or when option is used	active-High
XC3000	GR	always	active-Low
XC4000	GSR	per design or when option is used	active-High
XC5200	GR	per design or when option is used	active-High
XC9500	PRLD	when option is used	active-High

Use the **`Port Name`** field to change the default port name. Specifying the port name allows you to match the port name you used in the front end.

Bring Out Global Tristate Net as a Port

This option creates a global tristate signal (which forces all device outputs to the high-impedance state) as a port on the top-level entity in the output file.

Use the **`Port Name`** field to change the default port name. Specifying the port name allows you to match the port name you used in the front end. The default name is GTS.

Note: This option is only used if the global tristate net is not driven.

Generate Test Fixture/Testbench File

This option writes out a Verilog test fixture file or a VHDL testbench file. The test fixture file has a .tv extension. The testbench file has a .tvhd extension.

Include ‘uselib Directive in the Verilog File

This option writes a library path pointing to the SimPrim library into the output Verilog (.v) file. The path is written as follows, where *$XILINX* is the location of the Xilinx software.

```
‘uselib dir=$XILINX/verilog/data libext=.vmd
```

Note: This option is supported for Verilog only.

Generate Pin File

This option writes out a signal-to-pin mapping file. The file has a .pin extension.

Retain Hierarchy in Netlist

This option writes out a Verilog HDL or VHDL file that retains the hierarchy in the original design. The option groups logic based on the original design hierarchy.

Rename Architecture Name to

This option allows you to rename the architecture name generated in your VHDL file. The default architecture name for each entity in the netlist is STRUCTURE.

Spartan EDIF Tab

Use this tab, shown in the following figure, to set the following options.

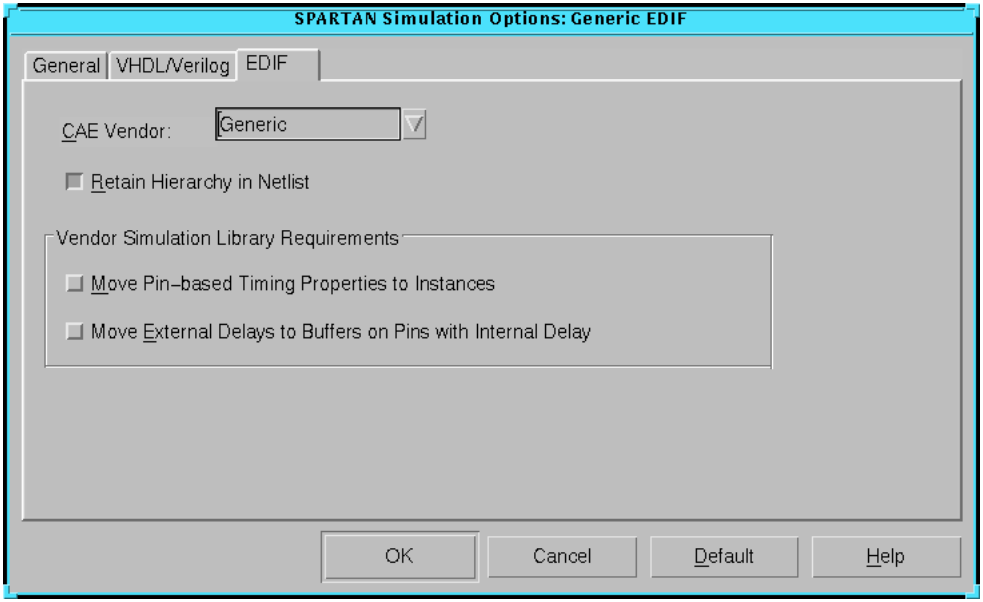


Figure 5-7 Spartan EDIF Tab

CAE Vendor

Specify the vendor name of your simulation tool in the CAE Vendor drop-down list. This ensures that the correct dialect of EDIF is chosen.

Retain Hierarchy in Netlist

This option writes out a flattened netlist.

Vendor Simulation Library Requirements

The following options apply only if you specify Generic as the CAE Vendor.

- Move Pin-Based Timing Properties to Instances

  This option annotates all timing properties to instances.

- Move External Delays to Buffers on Pins with Internal Delay

  This option models certain delays using buffers.

Spartan Configuration Options

Click the Configuration, Startup, Readback, or Tie tab to access the different options within the Configuration Options dialog box. These options affect the Configure step in the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

- "Spartan Configuration Tab"
- "Spartan Startup Tab"
- "Spartan Readback Tab"
- "Spartan Tie Tab"

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

Spartan Configuration Tab

Use this tab, shown in the following figure, to set the following options.

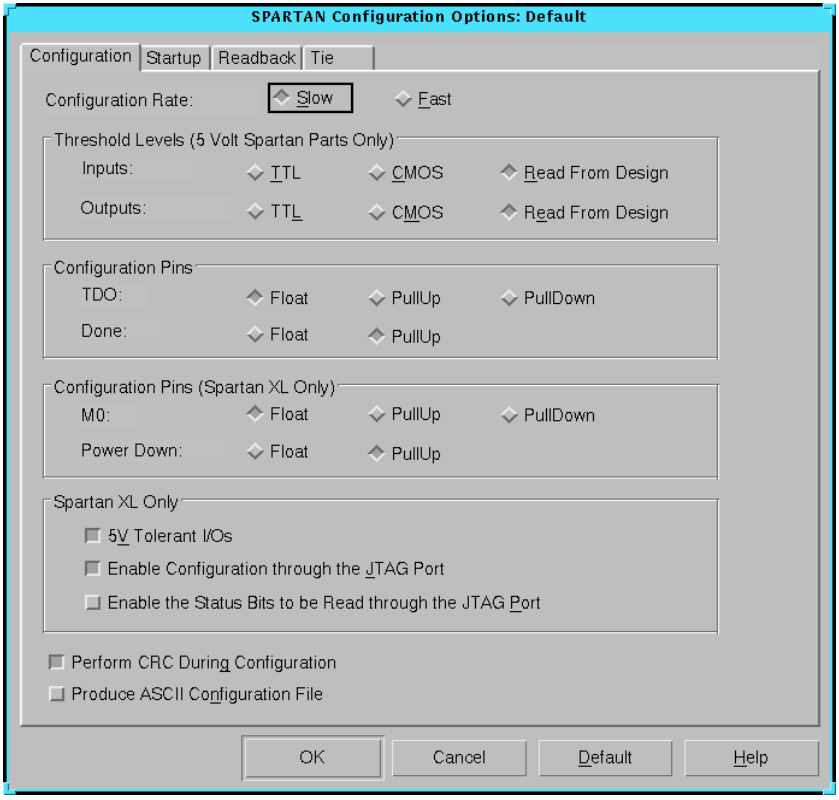


Figure 5-8 Spartan Configuration Tab

Configuration Rate

The Spartan device uses an internal configuration clock, CCLK, when configuring in a master mode. The configuration rate option allows you to select the rate for this clock. The following options are available. The default is Slow.

- Slow

  Select **`Slow`** to set the configuration clock rate to 1 MHz (nominal).

- Fast

  Select **Fast** to set the configuration clock rate to 8 MHz (nominal).

Threshold Levels (5 Volt Spartan Parts Only)

The Threshold Levels group box contains the following options.

Note: These options are supported for the Spartan family only. They are not supported for the SpartanXL family.

- Inputs

  Specify one of the following input options. The default is Read from Design.

  - TTL

    Select **TTL** to specify TTL-compatible inputs.

  - CMOS

    Select **CMOS** to specify CMOS-compatible inputs.

  - Read from Design

    Select **Read from Design** to specify the TTL/CMOS input level included in the physical contraints (PCF) file.

- Outputs

  Specify one of the following output options. The default is Read from Design.

  - TTL

    Select **TTL** to specify TTL-compatible output.

  - CMOS

    Select **CMOS** to specify CMOS-compatible outputs.

  - Read from Design

    Select **Read from Design** to specify the TTL/CMOS output level included in the PCF file.

Configuration Pins

The Configuration Pins group box contains the following options.

Note: You cannot use these pins to set the configuration mode or use them as user I/Os.

- TDO

  The value of the pull-up and pull-down resistors is 50 to 100 kilohms. The following options are available. The default is Float.

  - Float

    Select **`Float`** to disable both the pull-up resistor and pull-down resistor on the TDO pin.

  - PullUp

    Select **`PullUp`** to enable a pull-up on the TDO pin.

  - PullDown

    Select **`PullDown`** to enable a pull-down on the TDO pin.

- Done

  The DONE pin configures an open-drain driver that requires a pull-up resistor to indicate the end of the configuration. The value of the pull-up resistor is 2 to 8 kilohms. The following options are available. The default is PullUp.

  - Float

    Select **`Float`** to disable the pull-up resistor on the DONE pin. If you select this option, be sure you have connected an external pull-up resistor to this pin.

  - PullUp

    Select **`PullUp`** to enable an internal pull-up resistor on the DONE pin in Spartan devices. Select this option only if you do not connect an external pull-up resistor to this pin.

Configuration Pins (Spartan XL Only)

The Configuration Pins (Spartan XL Only) group box contains the following options. These options are supported for SpartanXL devices only.

- M0

  The M0 pin is used to determine the configuration mode. The value of the pull-up and pull-down resistors is 50 to 100 kilohms. The following options are available. The default is Float.

  - Float

    Select **Float** to disable both the pull-up resistor and pull-down resistor on the M0 pin.

  - PullUp

    Select **PullUp** to enable a pull-up on the M0 pin.

  - PullDown

    Select **PullDown** to enable a pull-down on the M0 pin.

- Power Down

  The Power Down pin allows the FPGA to exist in a standby mode which consumes less power. The FPGA enters this standby mode when the Power Down pin is driven Low. The default is PullUp.

  - Float

    Select **Float** to disable the pull-up resistor on the Power Down pin. Use this option if you will use the Power Down pin but will not tristate it.

  - PullUp

    Select **PullUp** to enable an internal pull-up resistor on the Power Down pin. You must use this option if the Power Down pin is not connected in your design, or if the signal driving this pin could be in a tristate condition.

Spartan XL Only

This group box contains the following options.

- 5V Tolerant I/Os

  This option allows a 3.3 V device circuitry to tolerate 5 V operation. For any device that operates on a mixed circuit environment with 3.3V and 5V, use this option. For any circuitry that operates exclusively on 3.3 V, such as in a laptop computer, turn this

option off. Turning off this option reduces power consumption. By default, this option is on.

Note: Enabling this option allows the device's clamping diodes to clamp ringing transients back to the 3.3 V supply rail. A clamping diode is connected from each output to VCC. This option affects all I/O pins.

- Enable Configuration Through the JTAG Port

  This option allows BSCAN-based configuration after the device is successfully configured. By default, this option is on.

- Enable the Status Bits to be Read Through the JTAG Port

  This option allows direct sensing of the DONE configuration state after performing a BSCAN-based configuration. This allows you to determine if a BSCAN-based configuration was successful. By default, this option is off.

Perform CRC During Configuration

This option enables Cyclic Redundancy Checking (CRC) error checking during configuration. If enabled, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each data frame in the configuration bitstream. This allows the device to perform a CRC check on the bitstream during the configuration process. If disabled, the device performs a simple check for the 0110 pattern at the end of each frame in the configuration data. By default, this option is on.

Produce ASCII Configuration File

This option creates a rawbits (RBT) file in addition to the binary BIT file. The RBT file is a text file that contains ASCII 1s and 0s. These characters represent the actual bits in the configuration bitstream that are downloaded to the FPGA. By default, this option is off.

Spartan Startup Tab

Use this tab, shown in the following figure, to set the following options.

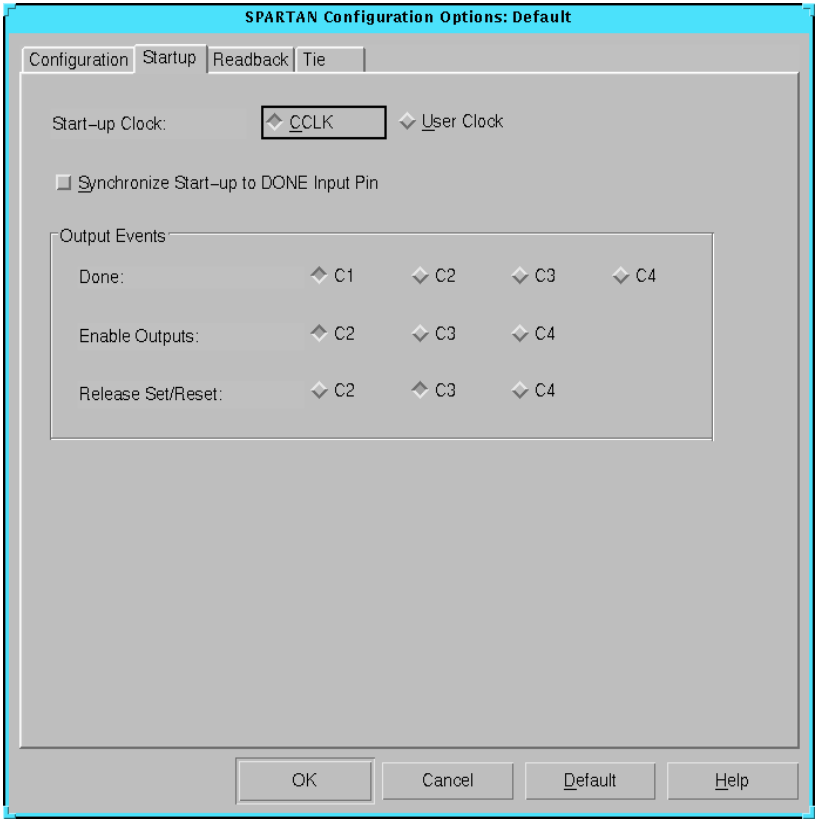


Figure 5-9 Spartan Startup Tab

Start-up Clock

The startup sequence following the configuration of a device can be synchronized to either CCLK or a User Clock. The default is CCLK.

- CCLK

  Select **CCLK** to synchronize to an internal clock provided in the FPGA device.

- User Clock

  Select **`User Clock`** to synchronize to a user-defined signal connected to the CLK pin of the startup symbol. You must select this option if your design contains a user clock net that drives the CLK pin on startup.

Synchronize Start-up to DONE Input Pin

The startup sequence of the device can be synchronized with the signal on the DONE pin. Deselect this option to begin the startup sequence when the configuration memory is full. Select this option to begin the startup sequence when the signal on the DONE pin goes High. By default, this option is off.

Output Events

There are three major output events which occur during a device startup.

- Done (DONE pin going High)
- Enable Outputs (device outputs no longer tristated)
- Release Set/Reset (Global Set/Reset signal deasserted)

Depending on the settings for Startup Clock and Synchronize Start-up to Done Input pin, the output events can be set to occur as shown in the following table. For more information, see *The Programmable Logic Data Book.*

Table 5-2 Output Events Options Matrix

	CCLK		User Clock	
	Sync	**No Sync**	**Sync**	**No Sync**
DONE	C1-C3	C1-C4	C1, U2	C1, U2-U4
Enable Outputs	C2, C3, DI, DI+1	C2-C4	U2, DI, DI+1, DI+2	U2-U4
Release Set/Reset	C2, C3, DI, DI+1	C2-C4	U2, DI, DI+1, DI+2	U2-U4

The definitions of the possible output events settings are as follows.

`C1` — first-Cclk rising edge after the length count is met

`C2` — second-Cclk rising edge after the length count is met

`C3` — third-Cclk rising edge after the length count is met

`C4` — fourth-Cclk rising edge after the length count is met

`U2` — second-valid-user-clock rising edge after C1 (first-Cclk rising edge after length count is met)

`U3` — third-valid-user-clock rising edge after C1 (first-Cclk rising edge after length count is met)

`U4` — fourth-valid-user-clock rising edge after C1 (first-Cclk rising edge after length count is met)

`DI` — when the DoneIn signal goes High

`DI+1` — first-Cclk or valid-user-clock rising edge, depending on the selection of startup-Clk, after DoneIn goes High

`DI+2` — second-Cclk or valid-user-clock rising edge, depending on the selection of startup-Clk, after DoneIn goes High

Spartan Readback Tab

Use this tab, shown in the following figure, to set the following options.

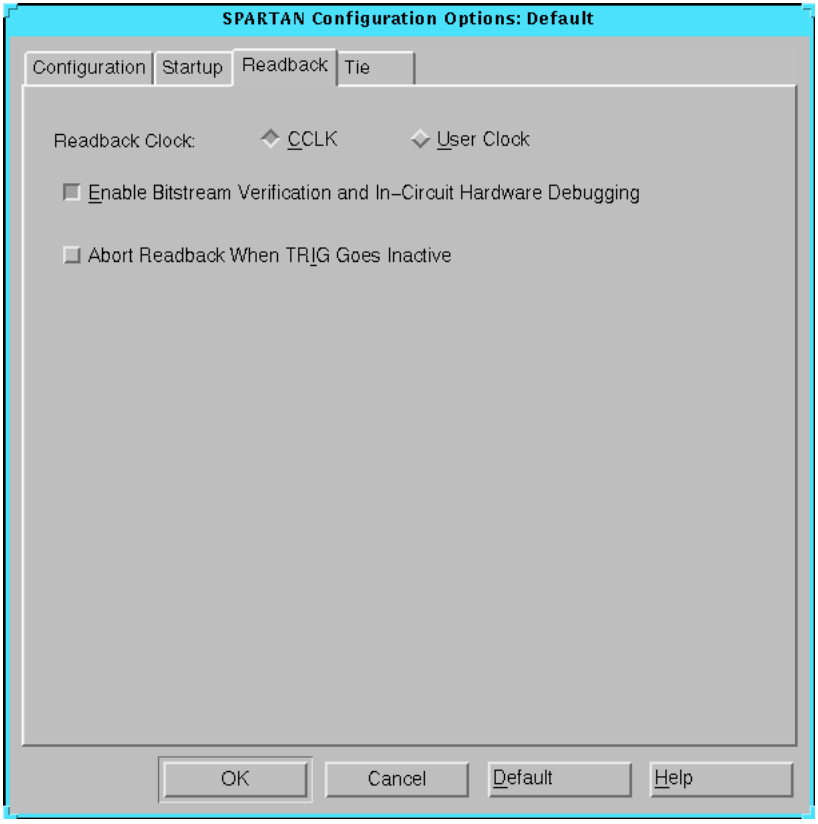


Figure 5-10 Spartan Readback Tab

Readback Clock

The readback data can be clocked out by either CCLK or a User Clock. The default is CCLK.

- CCLK

  Select **CCLK** to clock out the readback data through an internal clock provided in the FPGA device.

- User Clock

  Select **User Clock** to clock out the readback data through a user-defined signal connected to the CLK pin of the READBACK symbol.

Enable Bitstream Verification and In-Circuit Hardware Debugging

Use this option to activate or deactivate the readback capability of the configuration bitstream. To activate this feature, select this option and include the READBACK symbol in your design. Enabling this option generates a .ll file. By default, this option is on.

Abort Readback When TRIG Goes Inactive

Use this option to abort the readback sequence. Select this option to terminate the readback sequence when the device detects a High-to-Low transition on the TRIG pin of the READBACK symbol. By default, this option is off.

Spartan Tie Tab

Use this tab, shown in the following figure, to set the following options.

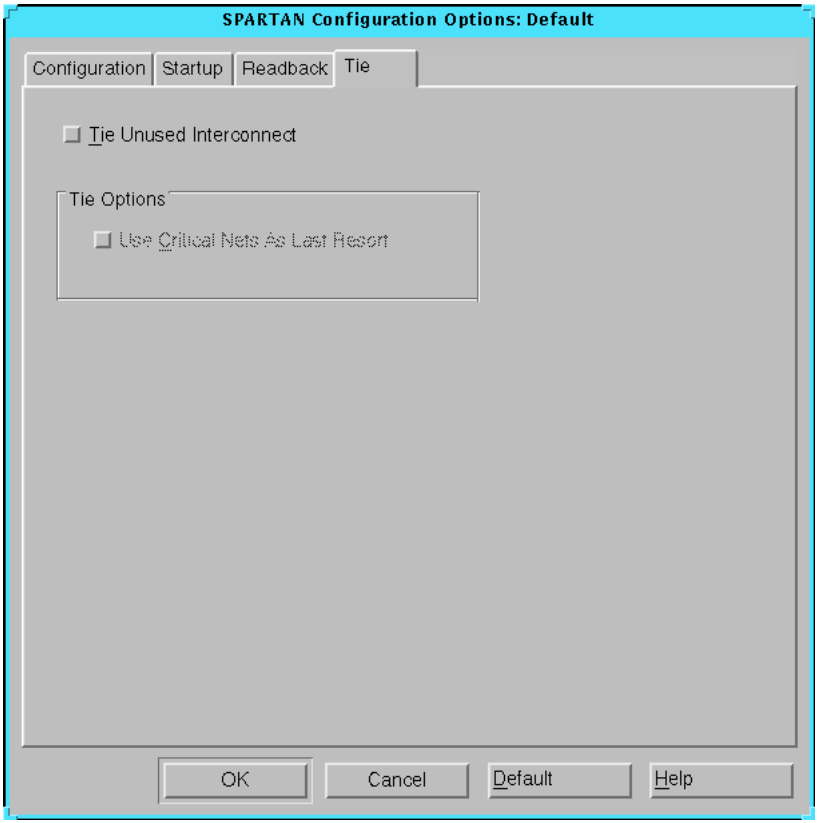


Figure 5-11 Spartan Tie Tab

Tie Unused Interconnect

Select this option to cause all unused interconnect to be tied to a logic Low or to a known level, keeping internal noise and power consumption to a minimum. When you use this option, Design Rule Check (DRC) runs first. After DRC, this option does the following.

- Ties all possible unused interconnect to unused CLB outputs and configures those outputs with a logic Low (F=0 or G=0)

- Attempts to tie any remaining interconnect to CLB outputs which have not been designated as critical
- Attempts to tie remaining interconnect to the global primary or secondary clock buffer outputs

By default, this option is off.

Tie Options — Use Critical Nets as Last Resort

Select this option to use the nets marked as critical to complete the tiedown process if necessary. Use this option as a last resort after an attempt is made to use nets not marked critical. By default, this option is off.

Spartan2 Implementation Options

Click the Translate, Optimize and Map, Place and Route, or Timing Reports tab to access the different options within the Implementation Options dialog box. These options affect the Translate, Map, and Place&Route steps in the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

- "Spartan2 Translate Tab"
- "Spartan2 Optimize and Map Tab"
- "Spartan2 Place and Route Tab"
- "Spartan2 Timing Reports Tab"

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

Spartan2 Translate Tab

Use the tab shown in the following figure, to set the translate options.

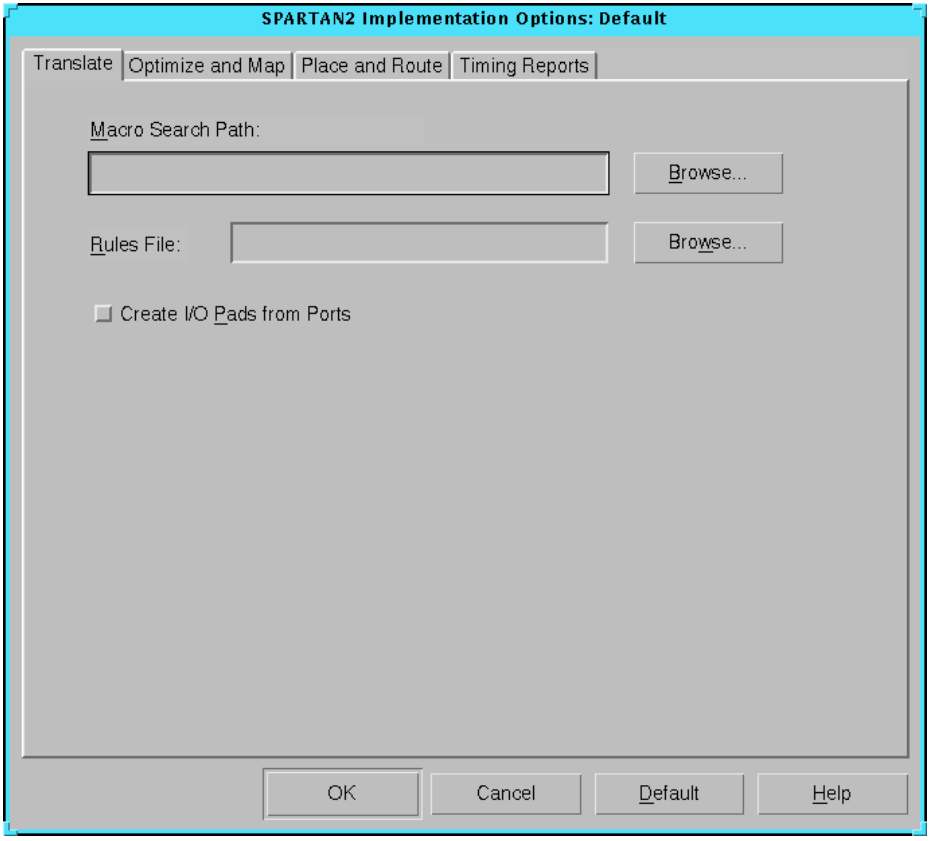


Figure 5-12 Spartan2 Translate Tab

The Spartan2 Translate tab is identical to the tab described in the "Spartan Translate Tab" section.

Spartan2 Optimize and Map Tab

Use this tab, shown in the following figure, to set the optimize and map options.

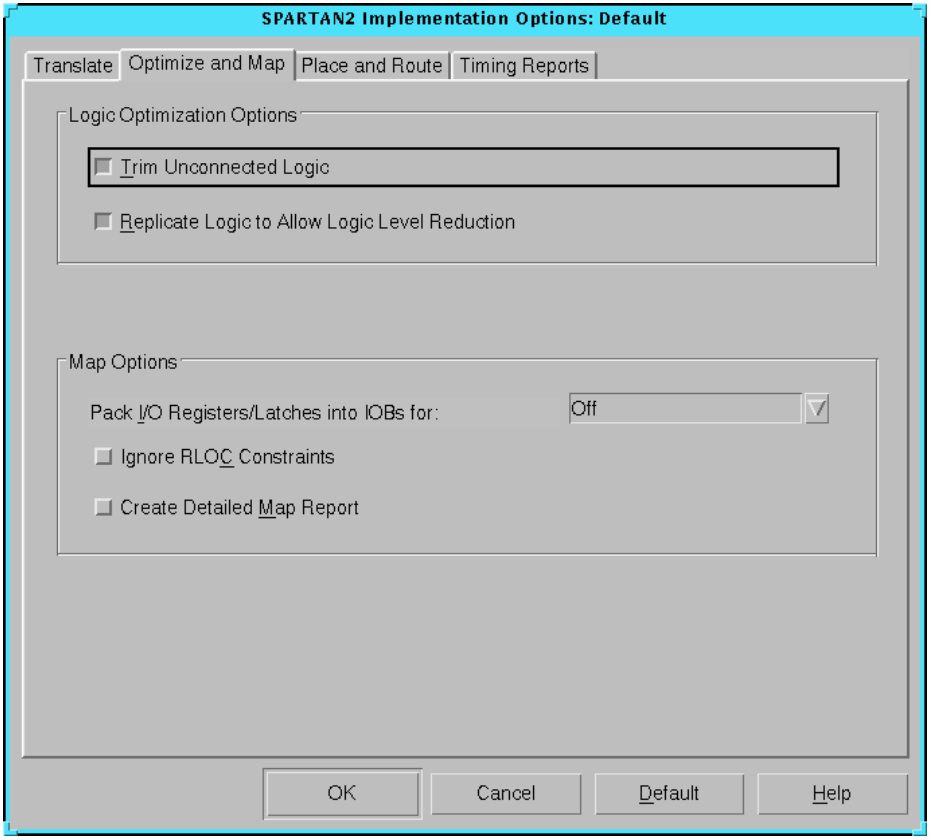


Figure 5-13 Spartan2 Optimize and Map Tab

The Spartan2 Optimize and Map tab is identical to the tab described in the “Virtex Optimize and Map Tab” section.

Spartan2 Place and Route Tab

Use this tab, shown in the following figure, to set the place and route options.

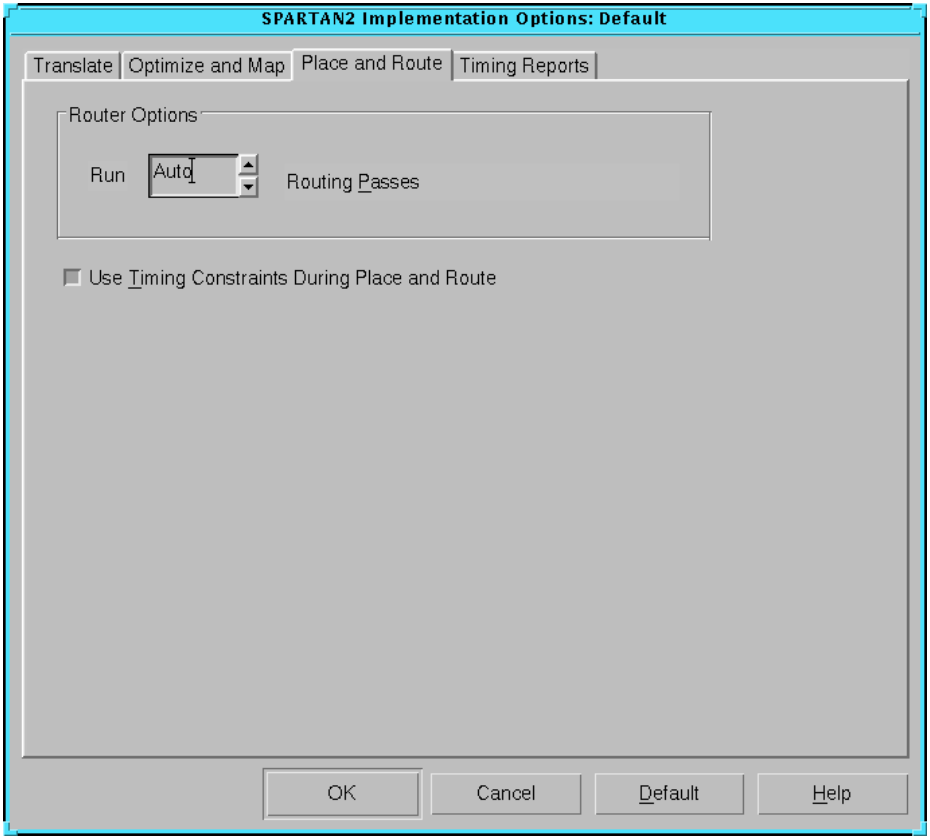


Figure 5-14 Spartan2 Place and Route Tab

The Spartan2 Place and Route tab is identical to the tab described in the “Virtex Place and Route Tab” section.

Spartan2 Timing Reports Tab

Use the tab shown in the following figure, to set the timing reports options.

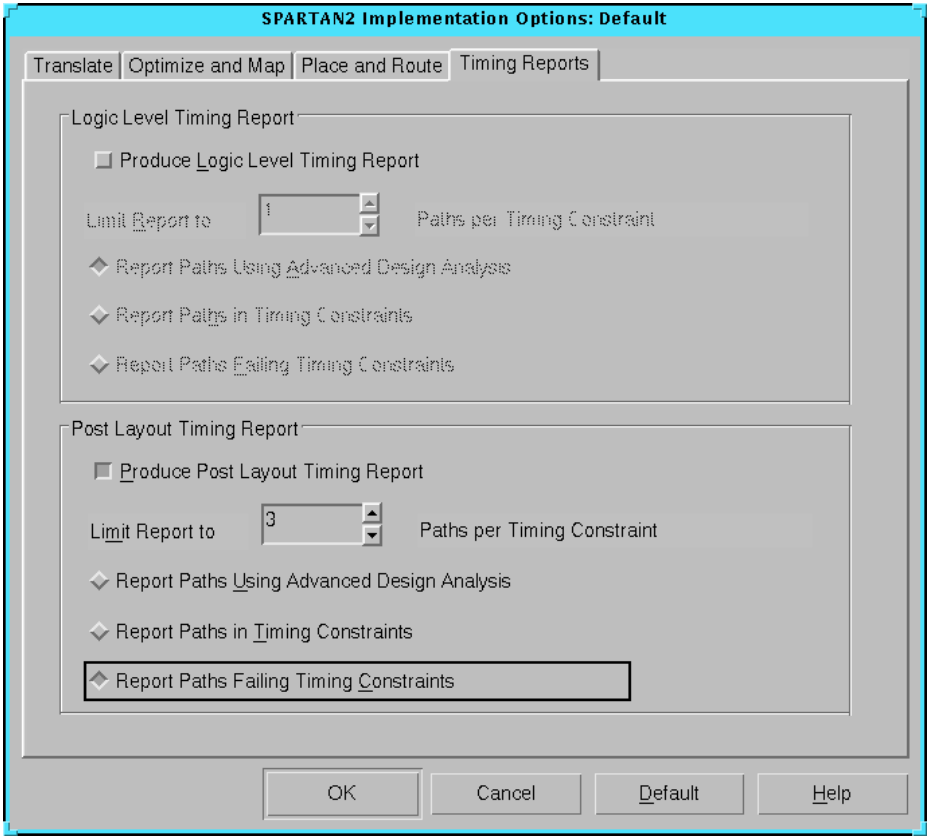


Figure 5-15 Spartan2 Timing Reports Tab

The Spartan2 Timing Reports tab is identical to the tab described in the “Spartan Timing Reports Tab” section.

Spartan2 Simulation Options

Click the General, VHDL / Verilog, or EDIF tab to access the different options within the Simulation Options dialog box. These options affect the timing simulation data produced during the Timing (Sim)

step of the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

Spartan2 General Tab

Use this tab, shown in the following figure, to set the general simulation options.

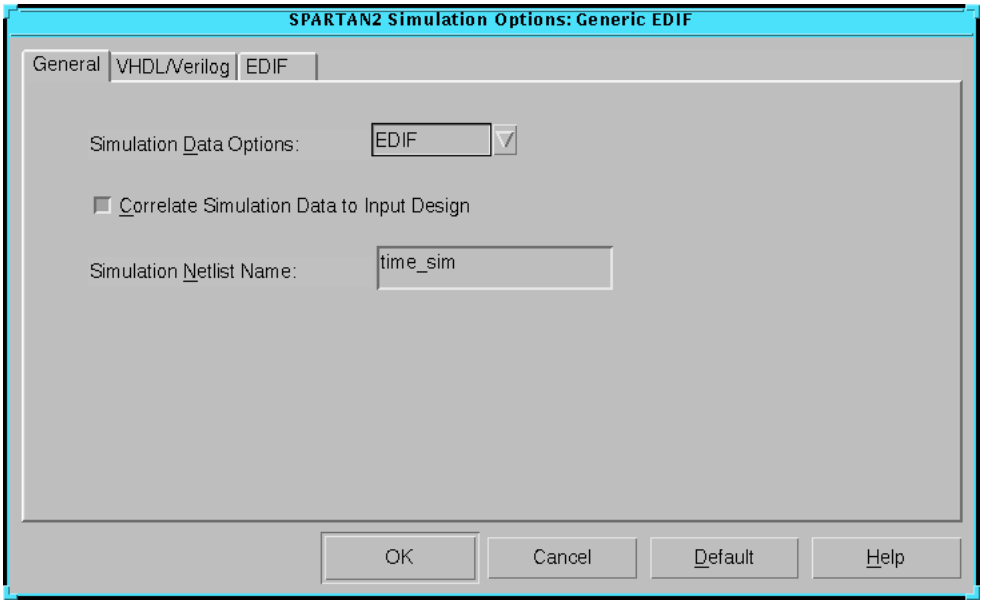


Figure 5-16 Spartan2 General Tab

The Spartan2 General tab is identical to the tab described in the "Virtex General Tab" section.

Spartan2 VHDL/Verilog Tab

Use this tab, shown in the following figure, to set the VHDL or Verilog options.

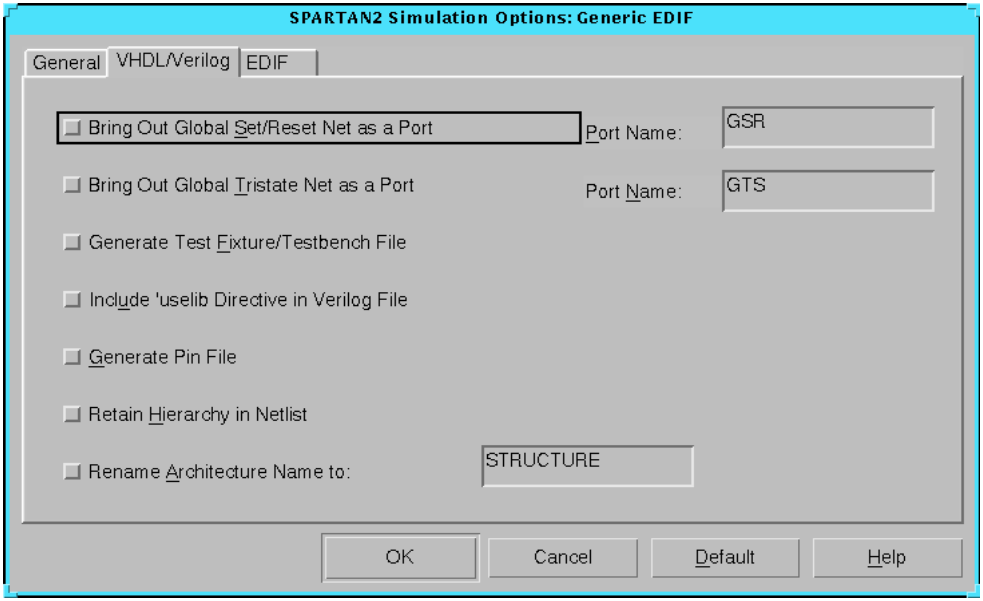


Figure 5-17 Spartan2 VHDL/Verilog Tab

The Spartan2 VHDL / Verilog tab is identical to the tab described in the "Spartan VHDL / Verilog Tab" section.

Note: In Spartan2 devices, the following components are *not* reset by the GSR signal: LUT RAM, Block RAM content, DLL, and SRL.

Spartan2 EDIF Tab

Use this tab, shown in the following figure, to set the EDIF options.

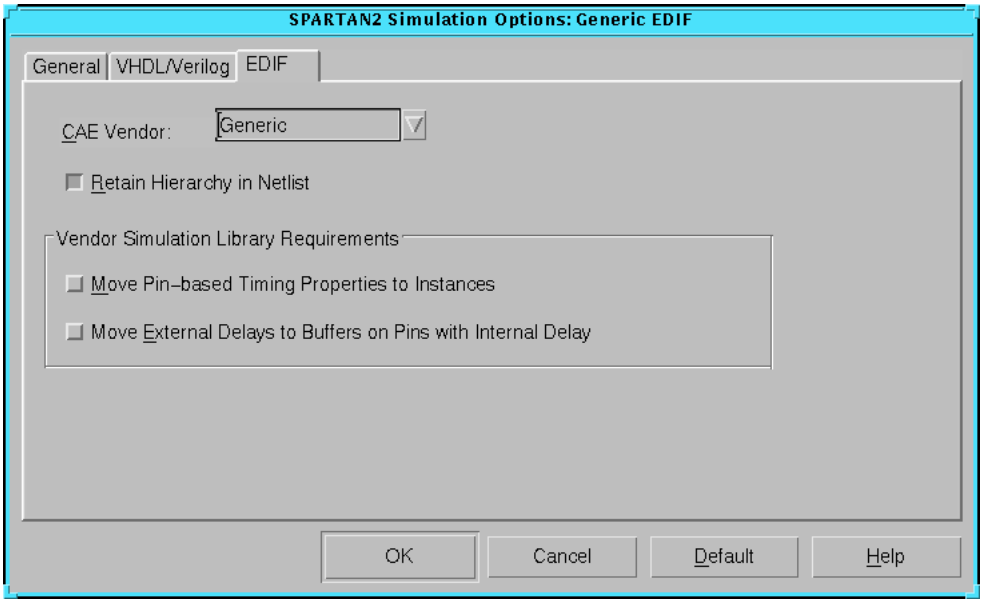


Figure 5-18 Spartan2 EDIF Tab

The Spartan2 EDIF tab is identical to the tab described in the “Spartan EDIF Tab” section.

Spartan2 Configuration Options

Click the Configuration, Startup, or Readback tab to access the different options within the Configuration Options dialog box. These options affect the Configure step in the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

Spartan2 Configuration Tab

Use this tab, shown in the following figure, to set the configuration options.

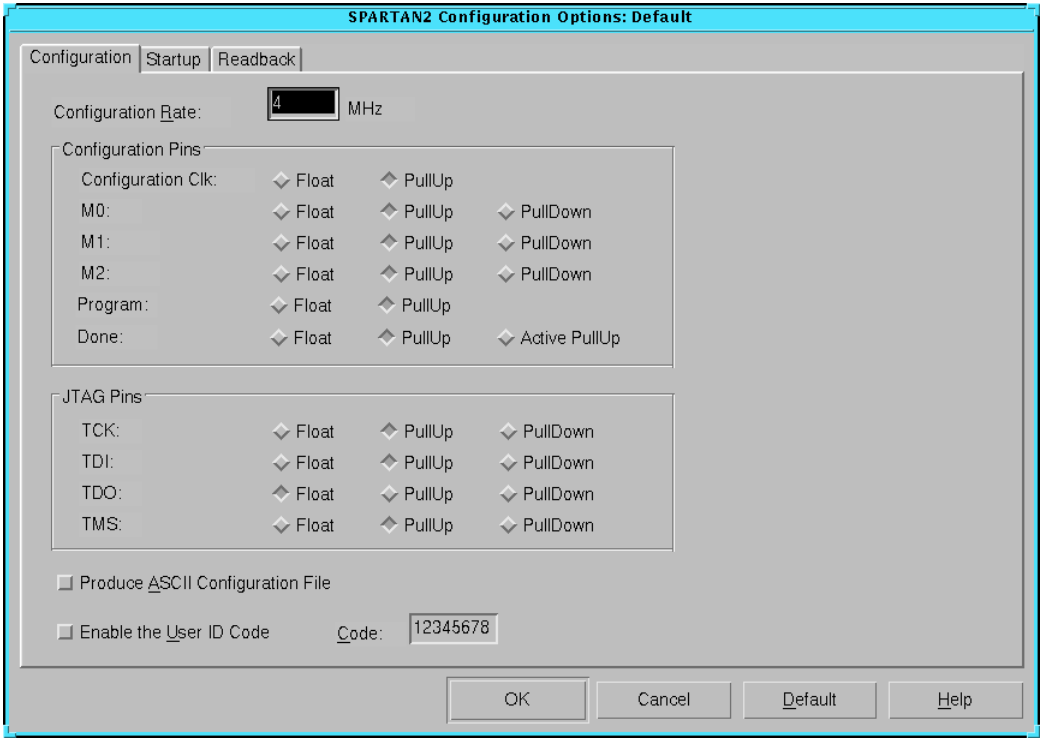


Figure 5-19 Spartan2 Configuration Tab

The Spartan2 Configuration tab is identical to the tab described in the "Virtex Configuration Tab" section.

Spartan2 Startup Tab

Use this tab, shown in the following figure, to set the configuration startup options.

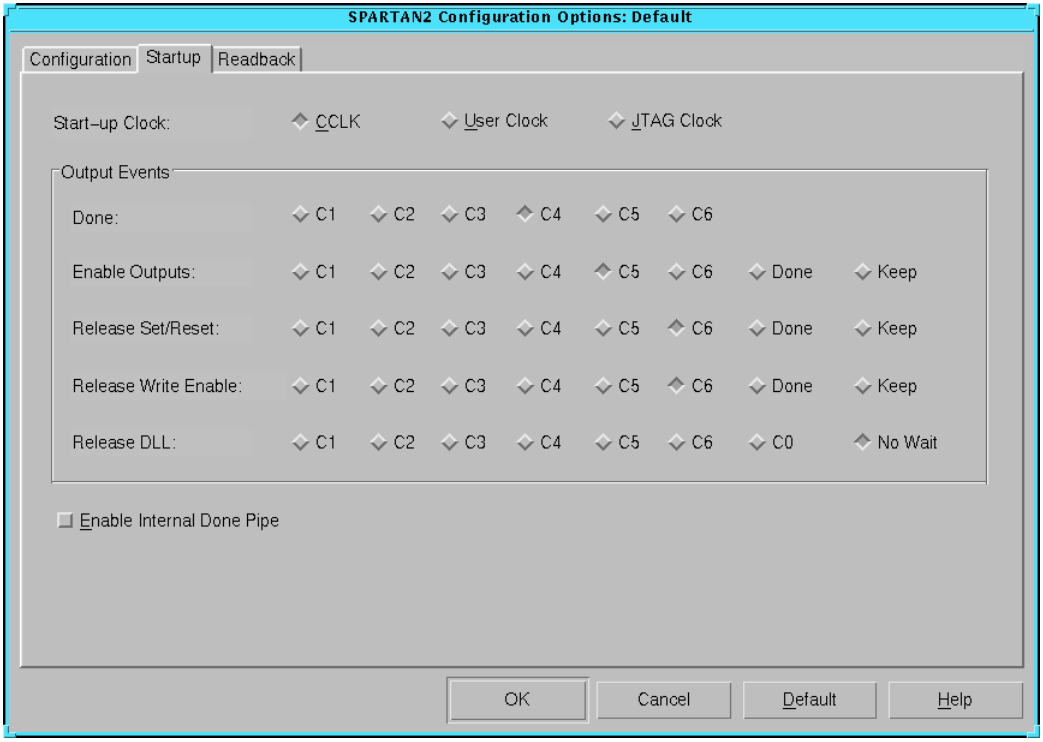


Figure 5-20 Spartan2 Startup Tab

The Spartan2 Startup tab is identical to the tab described in the "Virtex Startup Tab" section.

Spartan2 Readback Tab

Use this tab, shown in the following figure, to set the configuration readback options.

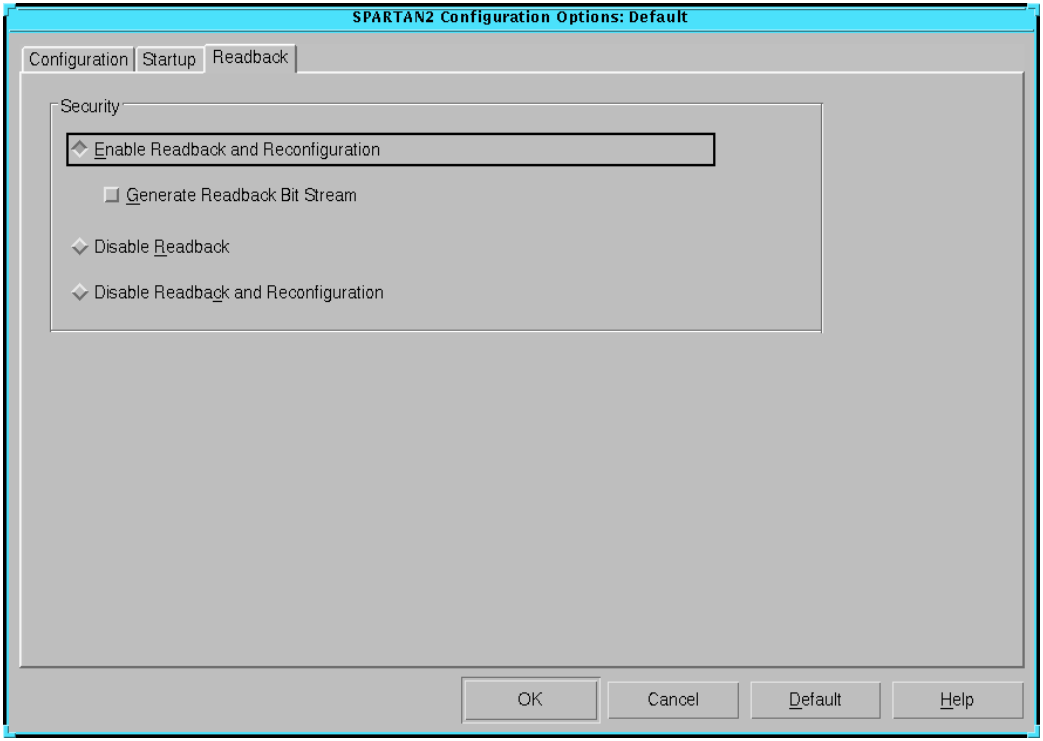


Figure 5-21 Spartan2 Readback Tab

The Spartan2 Readback tab is identical to the tab described in the "Virtex Readback Tab" section.

Virtex Implementation Options

Click the Translate, Optimize and Map, Place and Route, or Timing Reports tab to access the different options within the Implementation Options dialog box. These options affect the Translate, Map, and Place&Route steps in the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

- "Virtex Translate Tab"
- "Virtex Optimize and Map Tab"
- "Virtex Place and Route Tab"
- "Virtex Timing Reports Tab"

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

Virtex Translate Tab

Use this tab, shown in the following figure, to set the translate options.

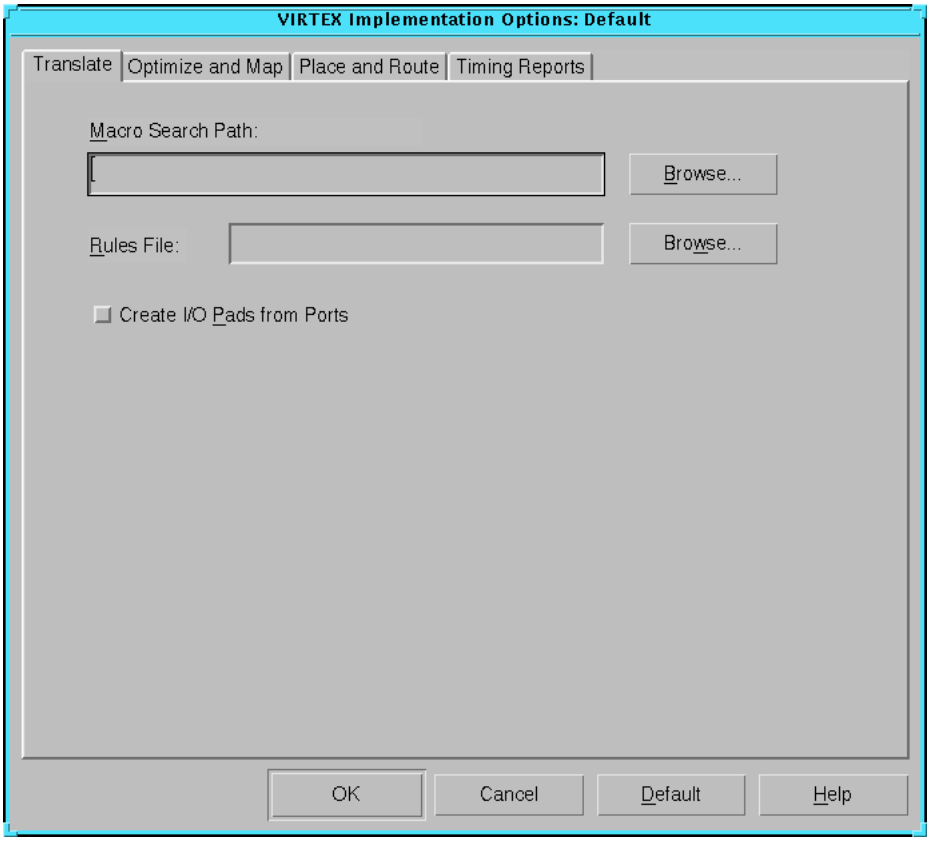


Figure 5-22 Virtex Translate Tab

The Virtex Translate tab is identical to the tab described in the "Spartan Translate Tab" section.

Virtex Optimize and Map Tab

Use this tab, shown in the following figure, to set the following options.

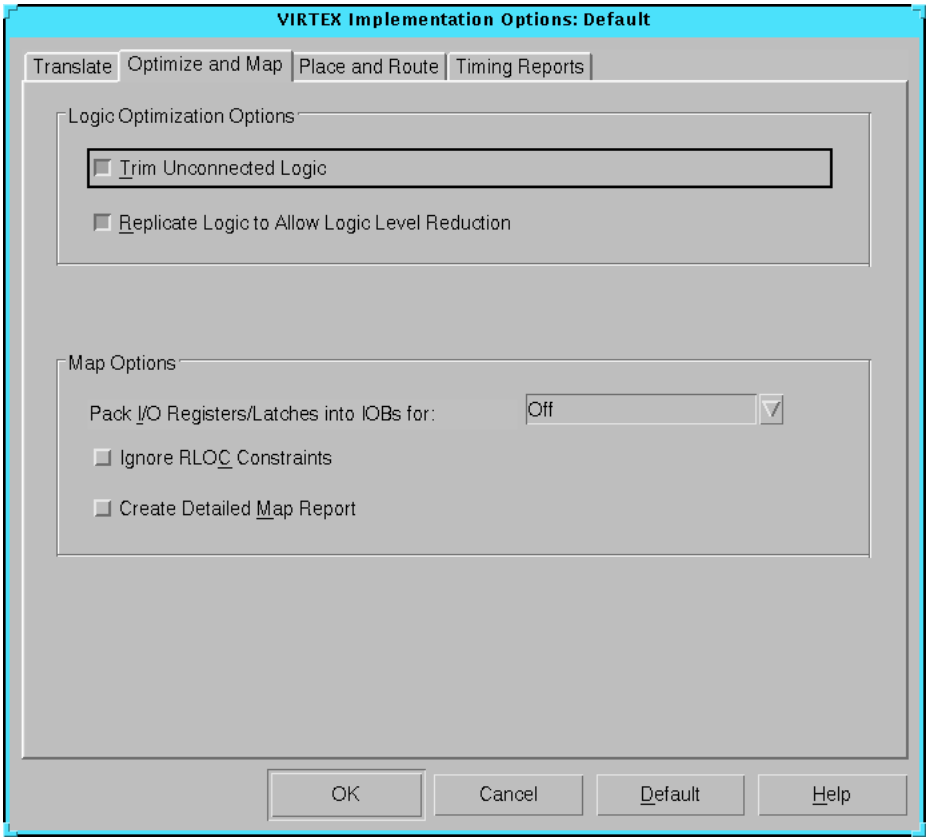


Figure 5-23 Virtex Optimize and Map Tab

Logic Optimization Options

The Logic Optimization Options group box contains the following options.

- Trim Unconnected Logic

  Select this option to trim unconnected components and nets from the design before mapping occurs. Deselect this option to map unconnected components and nets. Deselecting this option is useful for estimating the logic resources required for a design and for obtaining timing information on partially finished designs. When implementing an unfinished design, deselect this option to prevent partial logic from being trimmed. By default, this option is on.

- Replicate Logic to Allow Logic Level Reduction

  Use this option to replicate a single driver that drives multiple loads and map it as separate components that drive individual loads. This option is useful for creating a mapping strategy that may more readily meet your timing constraints. It reduces the number of logic elements through which a signal must pass, thereby eliminating path delays. By default, this option is on.

Map Options

- Pack I/O Registers/Latches into IOBs for

  This option controls the packing of flip-flops or latches within an I/O cell. Normally, the mapper packs flip-flops or latches within an I/O cell only if such packing is specified by your design entry method. This option allows you to control packing after the design entry phase. The default is Off.

  - Inputs Only

    Select **`Inputs Only`** to pack flip-flops or latches into input I/O cells.

  - Outputs Only

    Select **`Outputs Only`** to pack flip-flops or latches into output I/O cells.

  - Inputs and Outputs

    Select **`Inputs and Outputs`** to pack flip-flops or latches into both input and output I/O cells.

- Off

  Select **`Off`** to pack flip-flops or latches as specified by your design entry method.

- Ignore RLOC Constraints

  Select this option to cause Map to ignore the RLOC information that contains the relative placement of one CLB to another. This option also causes Map to ignore any invalid RLOC information that would result in a Map error. By default, this option is off.

Note: To ensure CLBs containing carry logic are aligned properly, Map retains the RLOC information that dictates what is packed into an individual CLB.

- Create Detailed Map Report

  Select this option to create a detailed Map report that includes signal and symbol cross-reference information. By default, this option is off.

Virtex Place and Route Tab

Use this tab, shown in the following figure, to set the following options.

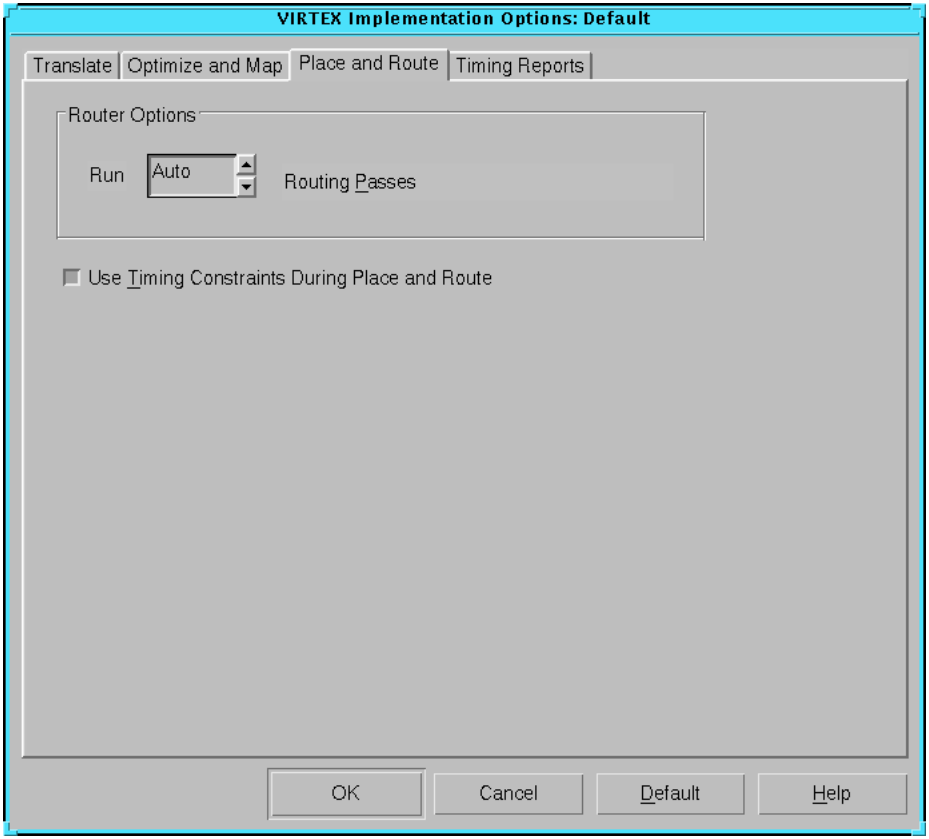


Figure 5-24 Virtex Place and Route Tab

Router Options

Use the Run _ Routing Passes option to set the maximum number of routing passes that the router runs in a design. The router attempts to completely route a placement with each pass. You can set the number of passes to a value from 1 to 1000 or to Auto.

Auto runs the router until specific exit conditions are met. At place and route effort levels of 3, 4, or 5, the router runs until it routes to

100% completion and meets all timing constraints or until it determines it cannot complete the routing. At levels of 1 or 2, the router stops after a predetermined number of passes. With all settings, the router exits immediately after it routes all connections and meets all timing constraints. A higher number of passes provides better routing results at the expense of longer run times. The default is Auto.

Use Timing Constraints During Place and Route

Select this option to produce a high-performance implementation of the design. The router uses the timing constraints in the design file to place and route the design within the specified constraints. Deselect this option to ignore timing constraints. This reduces implementation time at the expense of timing performance. By default, this option is on.

Virtex Timing Reports Tab

Use this tab, shown in the following figure, to set the timing report options.

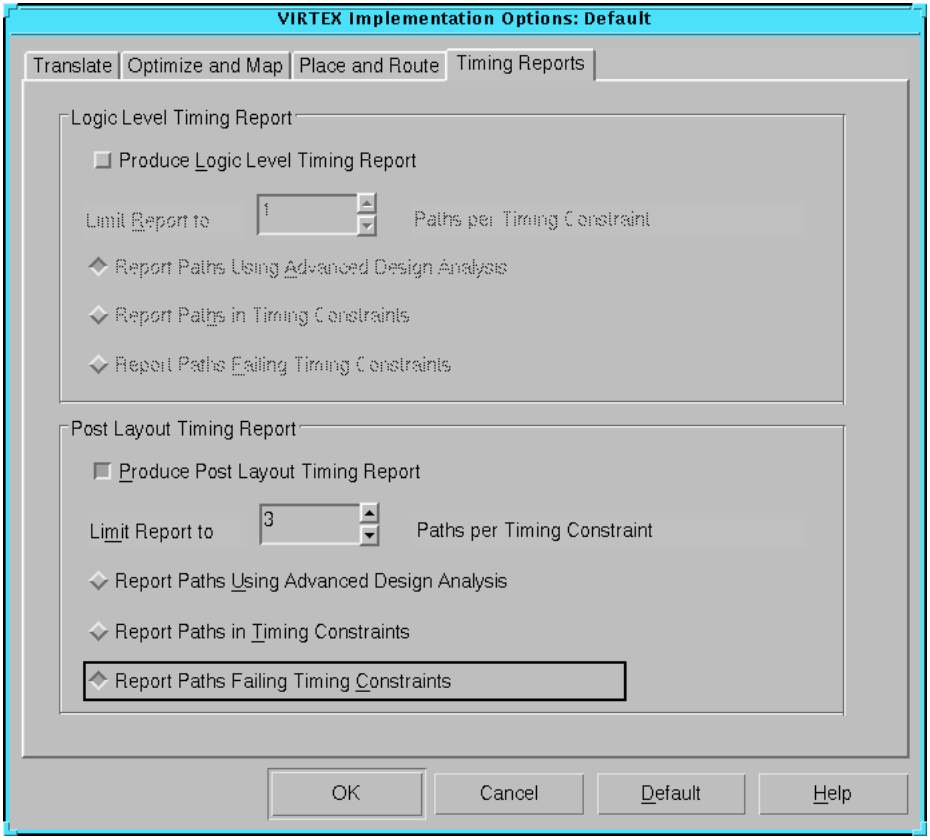


Figure 5-25 Virtex Timing Reports Tab

The Virtex Timing Reports tab is identical to the tab described in the "Spartan Timing Reports Tab" section.

Virtex Simulation Options

Click the General, VHDL / Verilog, or EDIF tab to access the different options within the Simulation Options dialog box. These options affect the timing simulation data produced during the Timing (Sim)

step of the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

Virtex General Tab

Use this tab, shown in the following figure, to set the following options.

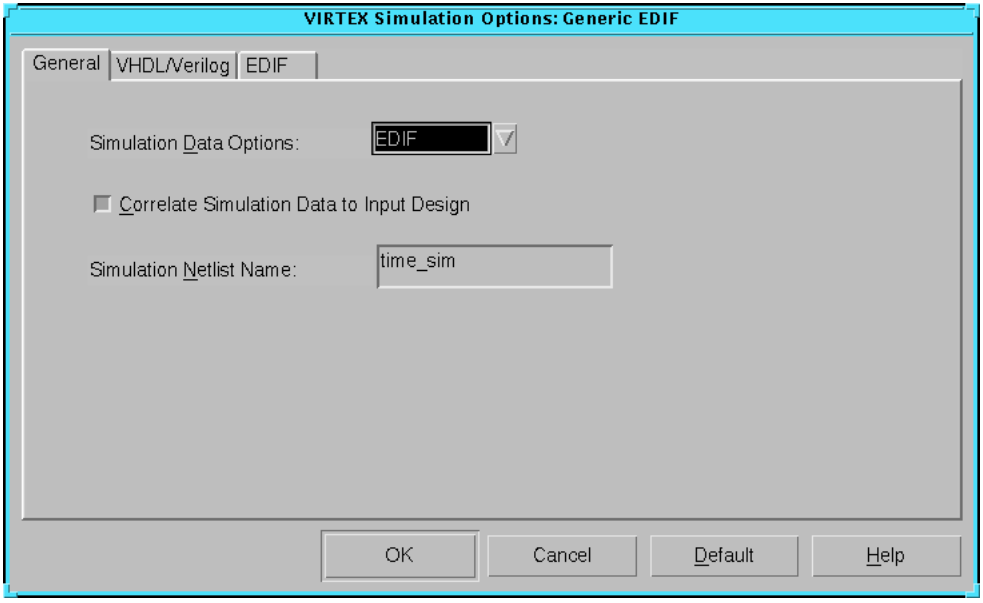


Figure 5-26 Virtex General Tab

Simulation Data Options

Specify the netlist format to use for simulation. The following formats are available.

- EDIF
- VHDL
- Verilog

Correlate Simulation Data to Input Design

Select this option to create a timing simulation netlist that contains the same logic gates and net names as those in the original schematic. Deselect this option to create a timing simulation netlist that contains the same logic gates and net names as those in the optimized implemented netlist.

Simulation Netlist Name

Select this option to specify the name of the output file. This allows you to control the output netlist name to avoid overwriting any files. The default name is time_sim.

Virtex VHDL/Verilog Tab

Use this tab, shown in the following figure, to set the VHDL or Verilog options.

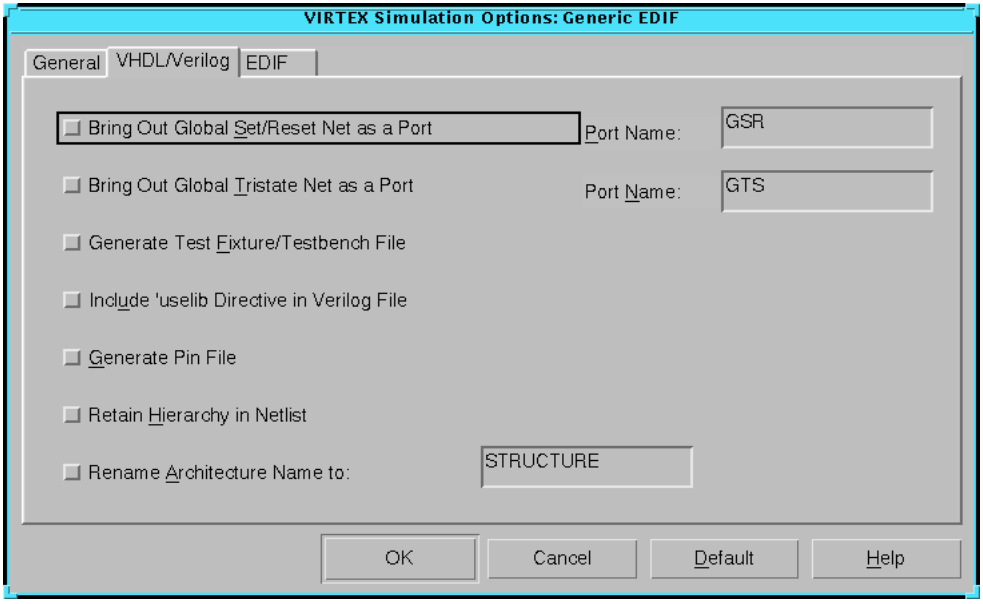


Figure 5-27 Virtex VHDL/Verilog Tab

The Virtex VHDL / Verilog tab is identical to the tab described in the "Spartan VHDL / Verilog Tab" section.

Note: In Virtex devices, the following components are *not* reset by the GSR signal: LUT RAM, Block RAM content, DLL, and SRL.

Virtex EDIF Tab

Use the Virtex EDIF tab, shown in the following figure, to set the EDIF options.

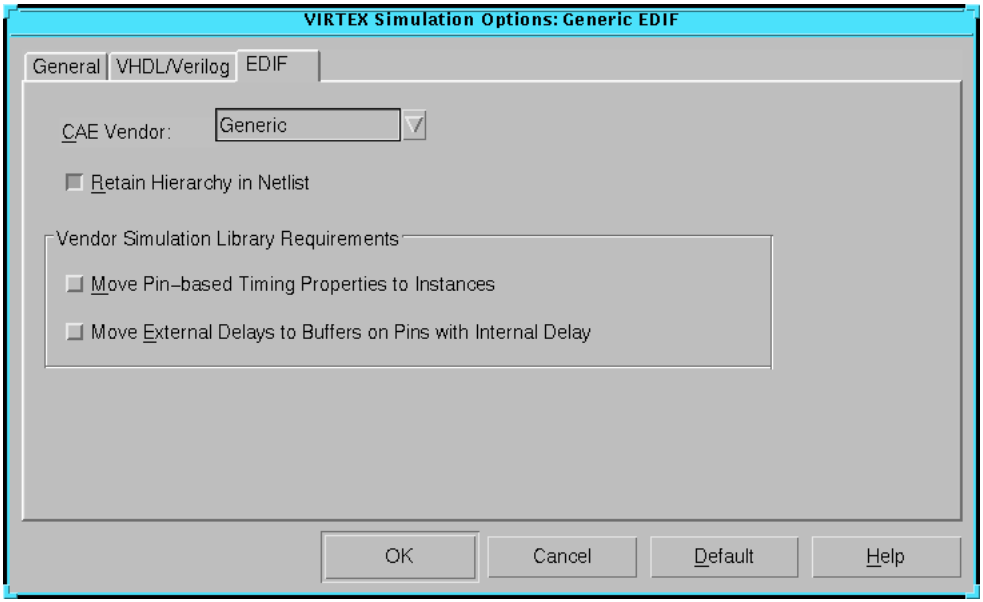


Figure 5-28 Virtex EDIF Tab

The Virtex EDIF tab is identical to the tab described in the “Spartan EDIF Tab” section.

Virtex Configuration Options

Click the Configuration, Startup, or Readback tab to access the different options within the Configuration Options dialog box. These options affect the Configure step in the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

- “Virtex Configuration Tab”
- “Virtex Startup Tab”
- “Virtex Readback Tab”

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

Virtex Configuration Tab

Use this tab, shown in the following figure, to set the following options.

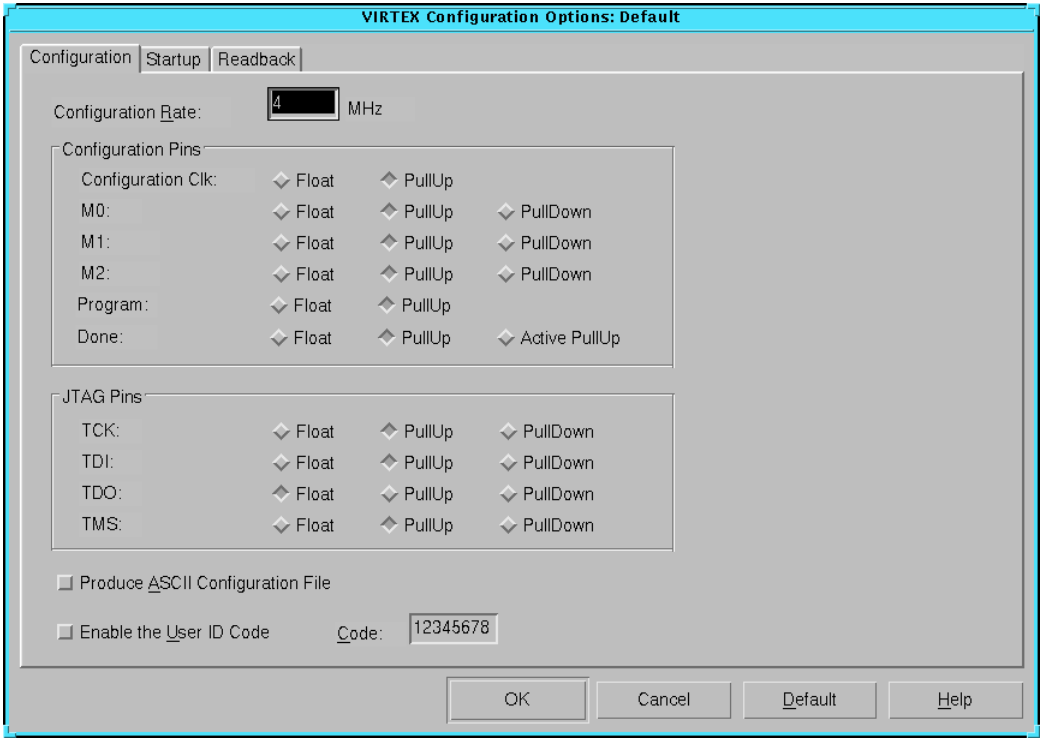


Figure 5-29 Virtex Configuration Tab

Configuration Rate

Virtex uses an internal configuration clock, CCLK, when configuring in a master mode. Use the configuration rate option to select the rate in megahertz (MHz) for this clock. The default is 4MHz.

Configuration Pins

The Configuration Pins group box contains the following options.

- Configuration Clk

  This pin is used to synchronize to an internal clock provided in the FPGA device. The default is PullUp.

  - Float

    Select **`Float`** to disable the pull-up resistor on the Configuration Clk pin.

  - PullUp

    Select **`PullUp`** to enable a pull-up on the Configuration Clk pin.

- M0

  The M0 pin is used to determine the configuration mode. The value of the pull-up and pull-down resistors is 50 to 100 kilohms. The following options are available. The default is PullUp.

  - Float

    Select **`Float`** to disable both the pull-up resistor and pull-down resistor on the M0 pin.

  - PullUp

    Select **`PullUp`** to enable a pull-up on the M0 pin.

  - PullDown

    Select **`PullDown`** to enable a pull-down on the M0 pin.

- M1

  The M1 pin can be used as tristatable output pin. The value of the pull-up and pull-down resistors is 50 to 100 kilohms. The following options are available. The default is PullUp.

- Float

  Select **Float** to disable both the pull-up resistor and pull-down resistor on the M1 pin.

- PullUp

  Select **PullUp** to enable a pull-up on the M1 pin.

- PullDown

  Select **PullDown** to enable a pull-down on the M1 pin.

- M2

  The M2 pin is used to determine the configuration mode. The value of the pull-up and pull-down resistors is 50 to 100 kilohms. The following options are available. The default is PullUp.

  - Float

    Select **Float** to disable both the pull-up resistor and pull-down resistor on the M2 pin.

  - PullUp

    Select **PullUp** to enable a pull-up on the M2 pin.

  - PullDown

    Select **PullDown** to enable a pull-down on the M2 pin.

- Program

  The $\overline{\text{PROG}}$ pin allows device reprogramming. The value of the pull-up resistor is 50 to 100 kilohms. The default is PullUp.

  - Float

    Select **Float** to disable both the pull-up resistor and pull-down resistor on the $\overline{\text{PROG}}$ pin.

  - PullUp

    Select **Pullup** to enable a pull-up on the $\overline{\text{PROG}}$ pin.

- Done

  The DONE pin configures an open-drain driver that requires a pull-up resistor to indicate the end of the configuration. The value of the pull-up resistor is 2 to 8 kilohms. The following options are available. The default is PullUp.

- Float

  Select **Float** to disable the pull-up resistor on the DONE pin. If you select this option, be sure you have connected an external pull-up resistor to this pin.

- PullUp

  Select **PullUp** to enable an internal pull-up resistor on the DONE pin. Select this option only if you do not connect an external pull-up resistor to this pin.

- Active PullUp

  Select **Active PullUp** to drive the DONE pin High with a CMOS driver.

JTAG Pins

The JTAG group box contains the following options. For more information on the following pins, see the *JTAG Programmer Guide*.

- TCK

  This pin is the JTAG test clock.The default is PullUp.

  - Float

    Select **Float** to disable both the pull-up resistor and pull-down resistor on the TCK pin.

  - PullUp

    Select **PullUp** to enable a pull-up on the TCK pin.

  - PullDown

    Select **PullDown** to enable a pull-down on the TCK pin.

- TDI

  This pin is the serial data input to all JTAG instructions and JTAG registers. The default is PullUp.

  - Float

    Select **Float** to disable both the pull-up resistor and pull-down resistor on the TDI pin.

  - PullUp

    Select **PullUp** to enable a pull-up on the TDI pin.

- PullDown

  Select **`PullDown`** to enable a pull-down on the TDI pin.

- TDO

  The TDO pin is the serial data output for all JTAG instruction and data registers. The default is Float.

  - Float

    Select **`Float`** to disable both the pull-up resistor and pull-down resistor on the TDO pin.

  - PullUp

    Select **`PullUp`** to enable a pull-up on the TDO pin.

  - PullDown

    Select **`PullDown`** to enable a pull-down on the TDO pin.

- TMS

  This pin is the mode input signal to the TAP controller. The TAP controller provides the control logic for JTAG. The default is PullUp.

  - Float

    Select **`Float`** to disable both the pull-up resistor and pull-down resistor on the TMS pin.

  - PullUp

    Select **`PullUp`** to enable a pull-up on the TMS pin.

  - PullDown

    Select **`PullDown`** to enable a pull-down on the TMS pin.

Produce ASCII Configuration File

This option creates a rawbits (RBT) file in addition to the binary BIT file. The RBT file is a text file that contains ASCII 1s and 0s. These characters represent the actual bits in the configuration bitstream that are downloaded to the FPGA. By default, this option is off.

Enable the User ID Code

Use this option to assign a code in the User Identification Register. Enter an ID code in the Code field. This code comprises eight hexadecimal digits that are placed in the User ID Register. By default, this option is off.

Virtex Startup Tab

Use this tab, shown in the following figure, to set the following options.

Figure 5-30 Virtex Startup Tab

Start-up Clock

The startup sequence following the configuration of a device can be synchronized to either CCLK, a User Clock, or the JTAG Clock. The default is CCLK.

- CCLK

  Select **CCLK** to synchronize to an internal clock provided in the FPGA device.

- User Clock

  Select **User Clock** to synchronize to a user-defined signal connected to the CLK pin of the startup symbol. You must select this option if your design contains a user clock net that drives the CLK pin on startup.

- JTAG Clock

  Select **JTAG Clock** to synchronize to the clock provided by JTAG. This clock sequences the TAP controller which provides the control logic for JTAG.

Output Events

There are five major output events which occur during a device startup.

- Done (CFG_DONE pin going High)
- Enable Outputs (device outputs no longer tristated)
- Release Set/Reset (Global Set/Reset signal deasserted)
- Release Write Enable (Global Write Enable signal deasserted)
- Release DLL (DLL allowed to synchronize)

Depending on the settings for Startup Clock, the output events can be set to occur as shown in the following table. For more information, see *The Programmable Logic Data Book.*

Table 5-3 Output Events Options Matrix

	CCLK	User Clock	JTAG Clock
DONE	C1-C6	C1, U2-U6	C1, J2-J6
Enable Outputs	C1-C6, Done, Keep	C1, U2-U6, Done, Keep	C1, J2-J6, Done, Keep
Release Set/ Reset	C1-C6, Done, Keep	C1, U2-U6, Done, Keep	C1, J2-J6, Done, Keep
Release Write Enable	C1-C6, Done, Keep	C1, U2-U6, Done, Keep	C1, J2-J6, Done, Keep
Release DLL	C0-C6, No Wait	C0-C1, U2-U6, No Wait	C0-C1, J2-J6, No Wait

The definitions of the possible output events settings are as follows.

`C0` — before the Cclk rising edge after the length count is met

`C1` — first-Cclk rising edge after the length count is met

`C2` — second-Cclk rising edge after the length count is met

`C3` — third-Cclk rising edge after the length count is met

`C4` — fourth-Cclk rising edge after the length count is met

`C5` — fifth-Cclk rising edge after the length count is met

`C6` — sixth-Cclk rising edge after the length count is met

`U2` — second-valid-user-clock rising edge after C1 (first-Cclk rising edge after length count is met)

`U3` — third-valid-user-clock rising edge after C1 (first-Cclk rising edge after length count is met)

`U4` — fourth-valid-user-clock rising edge after C1 (first-Cclk rising edge after length count is met)

`U5` — fifth-valid-user-clock rising edge after C1 (first-Cclk rising edge after length count is met)

`U6` — sixth-valid-user-clock rising edge after C1 (first-Cclk rising edge after length count is met)

`J2` — second-valid-JTAG-clock rising edge after C1 (first-Cclk rising edge after length count is met)

`J3` — third-valid-JTAG-clock rising edge after C1 (first-Cclk rising edge after length count is met)

`J4` — fourth-valid-JTAG-clock rising edge after C1 (first-Cclk rising edge after length count is met)

`J5` — fifth-valid-JTAG-clock rising edge after C1 (first-Cclk rising edge after length count is met)

`J6` — sixth-valid-JTAG-clock rising edge after C1 (first-Cclk rising edge after length count is met)

`Done` — when the CFG_DONE signal goes High

Keep — holds the pin at whatever level (High or Low) the pin is when the CFG_DONE signal goes High

No Wait — not synchronized to the startup clock; DLL synchronizes as soon as possible

Enable Internal Done Pipe

Select this option when the startup clock is running at high speeds. If you select this option, the FPGA waits for the CFG_DONE signal that is delayed by one clock cycle instead of waiting for the pin itself. By default, this option is off.

Virtex Readback Tab

Use the Readback tab, shown in the following figure, to set the configuration readback options.

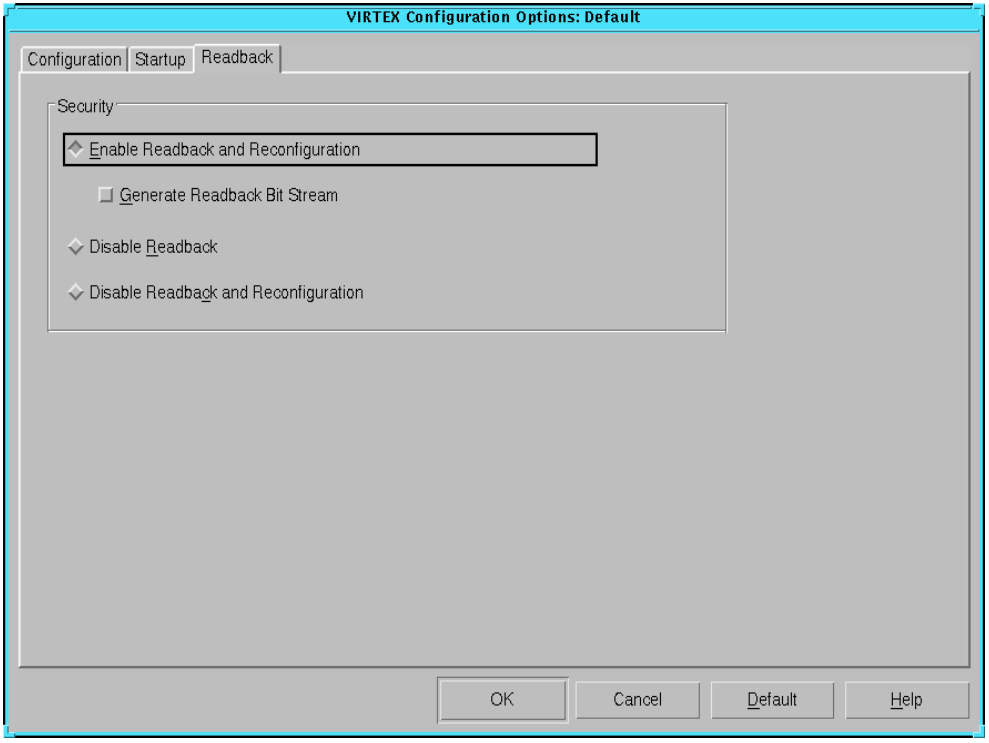


Figure 5-31 Virtex Readback Tab

Security

- Enable Readback and Reconfiguration

  This option specifies readback options. After the FPGA design has been configured, the FPGA configuration data can be read back and compared with the original configuration data. Readback is initiated by a Low-to-High transition on the M0/RTRIG pin. After this option is run, external logic must drive the Cclk input to read back each data bit. The readback data appears on the $\overline{\text{RDATA}}$ pin.

Select **Generate Readback Bitstream** to create a byte wide readback bitstream file. By default, this option is off.

- Disable Readback

  This option disables readback. Use this option for design security. By disabling readback, configuration data is secure from being read from the FPGA. By default, this option is off.

- Disable Readback and Reconfiguration

  This option disables both readback and reconfiguration. Use this option for design security. By disabling readback and reconfiguration, configuration and reconfiguration data is secure from being read from the FPGA. By default, this option is off.

XC3000 Implementation Options

Click the Translate, Optimize and Map, Place and Route, or Timing Reports tab to access the different options within the Implementation Options dialog box. These options affect the Translate, Map, and Place&Route steps in the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

- "XC3000 Translate Tab"
- "XC3000 Optimize and Map Tab"
- "XC3000 Place and Route Tab"
- "XC3000 Timing Reports Tab"

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

XC3000 Translate Tab

Use this tab, shown in the following figure, to set the translate options.

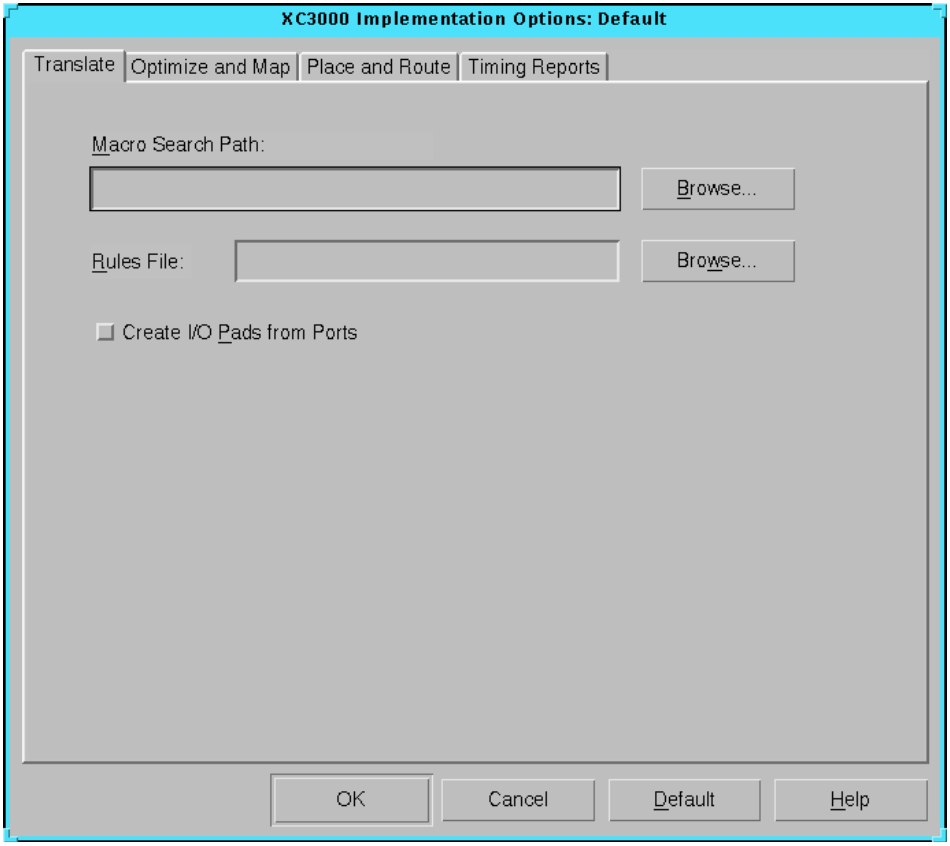


Figure 5-32 XC3000 Translate Tab

The XC3000 Translate tab is identical to the tab described in the "Spartan Translate Tab" section.

XC3000 Optimize and Map Tab

Use this tab, shown in the following figure, to set the following options.

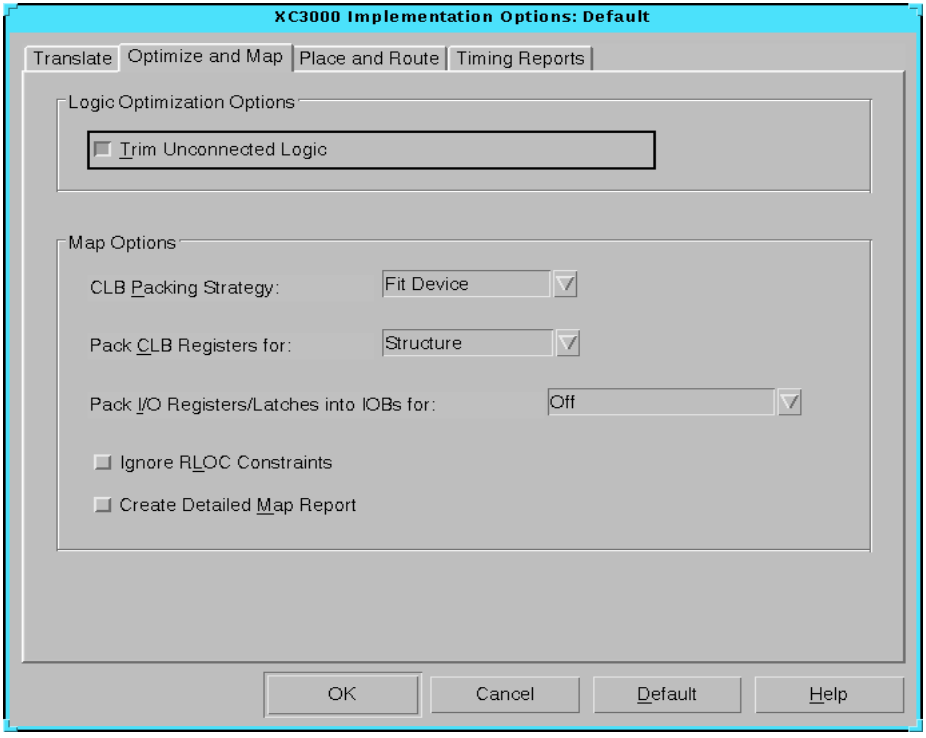


Figure 5-33 XC3000 Optimize and Map Tab

Logic Optimization Options

Select **`Trim Unconnected Logic`** to trim unconnected components and nets from the design before mapping occurs. Deselect this option to map unconnected components and nets. Deselecting this option is useful for estimating the logic resources required for a design and for obtaining timing information on partially finished designs. When implementing an unfinished design, deselect this option to prevent partial logic from being trimmed. By default, this option is on.

Map Options

The Map Options group box contains the following options.

- CLB Packing Strategy

  This option partitions logic more densely. Normally, the mapper partitions logic to maximize signal sharing within CLBs and to minimize routing congestion. The CLB Packing Strategy option optimizes density by relaxing the requirement for a high degree of signal sharing between logic elements in a CLB, using the DI (direct flip-flop input) pins on CLBs, and reducing minimum signal combining requirements. The default is Fit Device.

Note: Although the CLB Packing Strategy option makes a design denser, it can also adversely affect place and route performance, resulting in higher delays and more unrouted nets. Use this option if you are willing to trade performance for density.

  - Fit Device

    Select **`Fit Device`** to pack logic elements that do not share common signals into the CLBs. The mapper continues packing until the design fits into the selected device or no further packing is possible.

  - Off

    Select **`Off`** to disable the CLB Packing Strategy option. Disabling this option causes only related logic (logic with common inputs) to be packed together. This is useful for increasing speed in high speed designs. However, the design may overflow the selected part due to the increase in CLBs used.

- Pack CLB Registers for

  This option controls register ordering. When you map a design containing registers, the mapper can optimize the way the registers are grouped into CLBs. This optimized mapping is called register ordering. For more information on register ordering, see the “Register Ordering” section of the *Development System Reference Guide*. The default is Structure.

- Structure

  Select **Structure** to enable register ordering. The mapper will look at the register bit names for similarities and try to map register bits in an ordered manner.

- Minimum Area

  Select **Minimum Area** to disable register ordering for a denser design. Register bit names will be ignored when registers are mapped, and the bits will not be mapped in any special order.

- Pack I/O Registers/Latches into IOBs for

  This option controls the packing of flip-flops or latches within an I/O cell. Normally, the mapper packs flip-flops or latches within an I/O cell only if such packing is specified by your design entry method. This option allows you to control packing after the design entry phase. The default is Off.

  - Inputs Only

    Select **Inputs Only** to pack flip-flops or latches into input I/O cells.

  - Outputs Only

    Select **Outputs Only** to pack flip-flops or latches into output I/O cells.

  - Inputs and Outputs

    Select **Inputs and Outputs** to pack flip-flops or latches into both input and output I/O cells.

  - Off

    Select **Off** to pack flip-flops or latches as specified by your design entry method.

- Ignore RLOC Constraints

  Select this option to cause Map to ignore the RLOC information that contains the relative placement of one CLB to another. This option also causes Map to ignore any invalid RLOC information that would result in a Map error. By default, this option is off.

Note: To ensure CLBs containing carry logic are aligned properly, Map retains the RLOC information that dictates what is packed into an individual CLB.

- Create Detailed Map Report

  Select this option to create a detailed Map report that includes signal and symbol cross-reference information. By default, this option is off.

XC3000 Place and Route Tab

Use this tab, shown in the following figure, to set the place and route options.

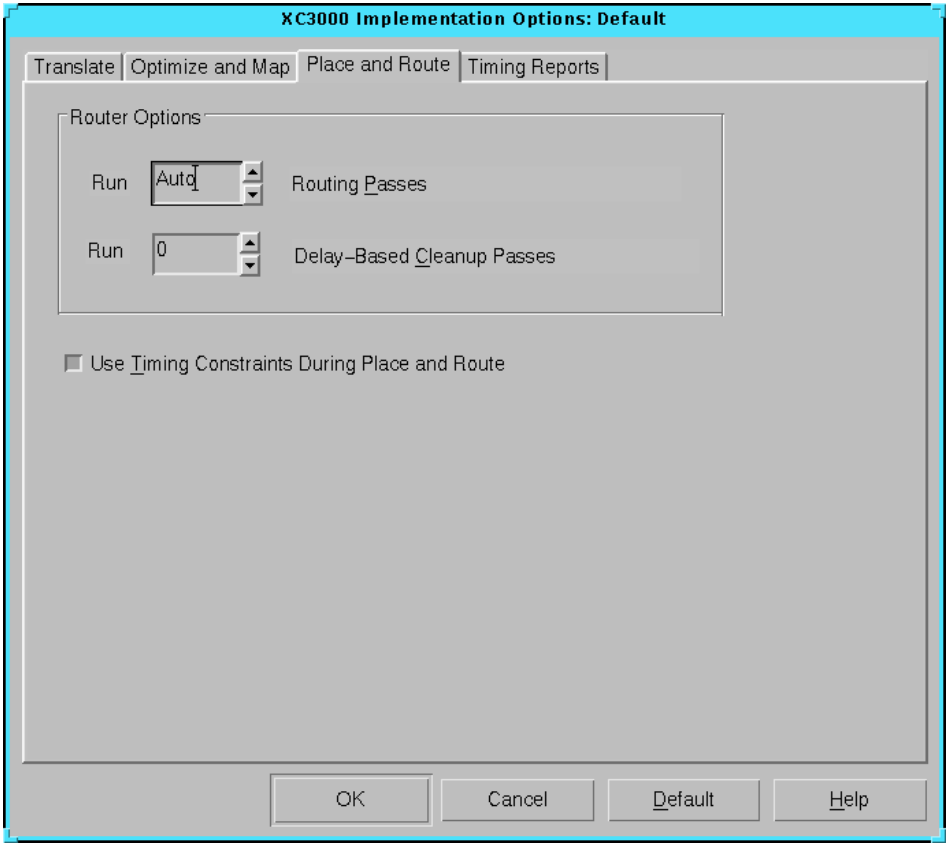


Figure 5-34 XC3000 Place and Route Tab

The XC3000 Place and Route tab is identical to the tab described in the “Spartan Place and Route Tab” section.

XC3000 Timing Reports Tab

Use this tab, shown in the following figure, to set the timing report options.

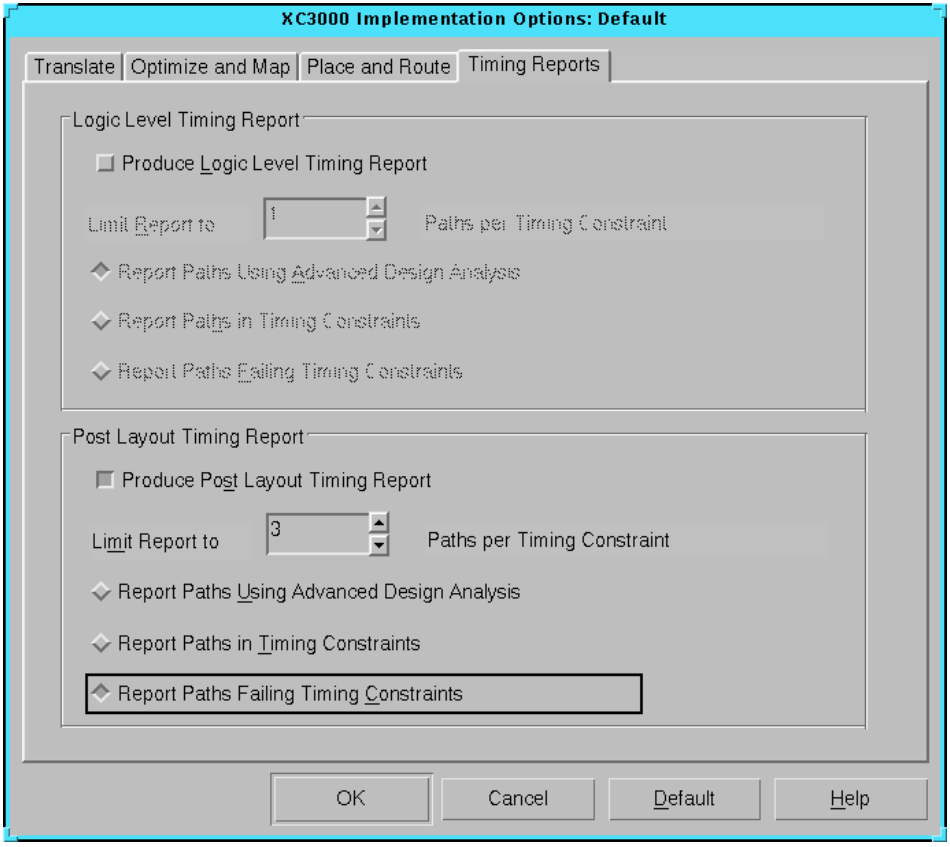


Figure 5-35 XC3000 Timing Reports Tab

The XC3000 Timing Reports tab is identical to the tab described in the “Spartan Timing Reports Tab” section.

XC3000 Simulation Options

Click the General, VHDL / Verilog, or EDIF tab to access the different options within the Simulation Options dialog box. These options affect the timing simulation data produced during the Timing (Sim) step of the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

XC3000 General Tab

Use this tab, shown in the following figure, to set the general simulation options.

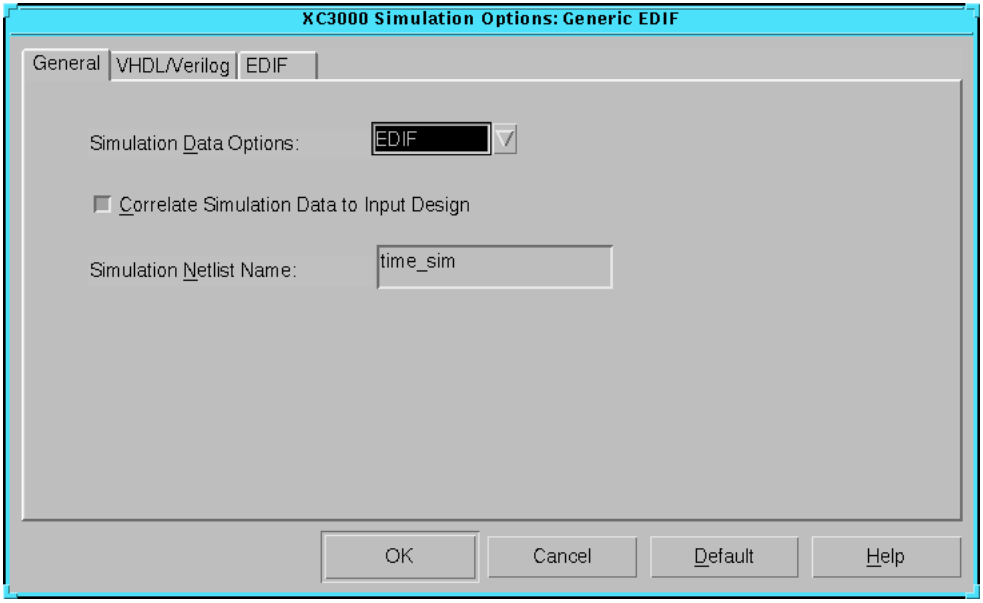


Figure 5-36 XC3000 General Tab

The XC3000 General tab is identical to the tab described in the "Spartan General Tab" section.

XC3000 VHDL/Verilog Tab

Use this tab, shown in the following figure, to set the VHDL or Verilog options.

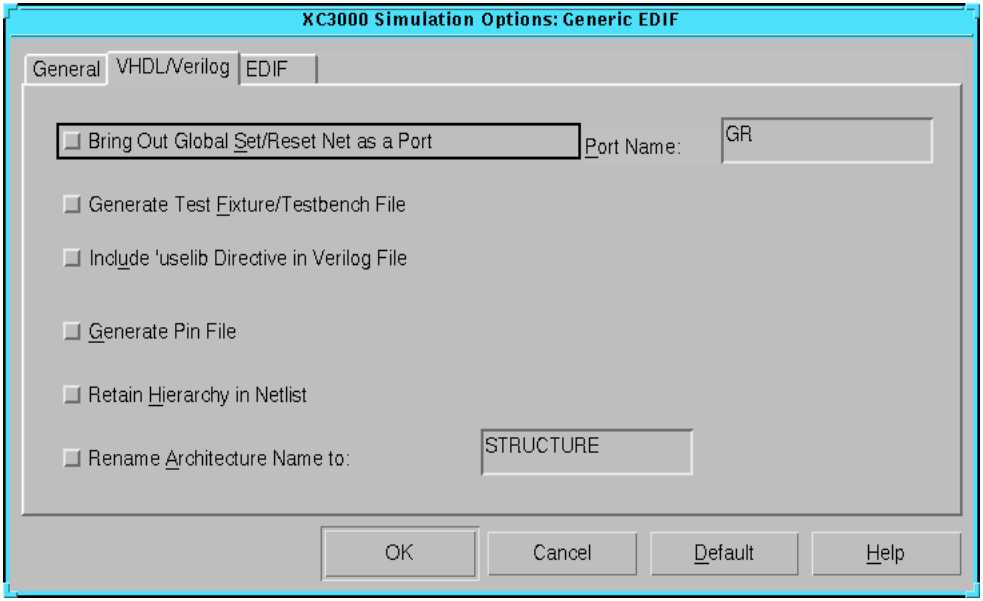


Figure 5-37 XC3000 VHDL/Verilog Tab

Bring Out Global Set/Reset Net as a Port

This option creates a Global Set/Reset port on the top-level simulation module (entity). This port is connected to all flip-flop and latch primitives in the design. Stimulating this port automatically sets or resets every flip-flop and latch to its initial state, as determined in the design. The default name of the Global Set/Reset port depends on the target device family as described in the "Global Set/Reset Port Information" table.

Use the **`Port Name`** field to change the default port name. Specifying the port name allows you to match the port name you used in the front end.

Generate Test Fixture/Testbench File

This option writes out a Verilog test fixture file or a VHDL testbench file. The test fixture file has a .tv extension. The testbench file has a .tvhd extension.

Include ‘uselib Directive in the Verilog File

This option writes a library path pointing to the SimPrim library into the output Verilog (.v) file. The path is written as follows, where *$XILINX* is the location of the Xilinx software.

```
‘uselib dir=$XILINX/verilog/data libext=.vmd
```

Note: This option is supported for Verilog only.

Generate Pin File

This option writes out a signal-to-pin mapping file. The file has a .pin extension.

Retain Hierarchy in Netlist

This option writes out a Verilog HDL or VHDL file that retains the hierarchy in the original design. The option groups logic based on the original design hierarchy.

Rename Architecture Name to

This option allows you to rename the architecture name generated in your VHDL file. The default architecture name for each entity in the netlist is STRUCTURE.

XC3000 EDIF Tab

Use this tab, shown in the following figure, to set the EDIF options.

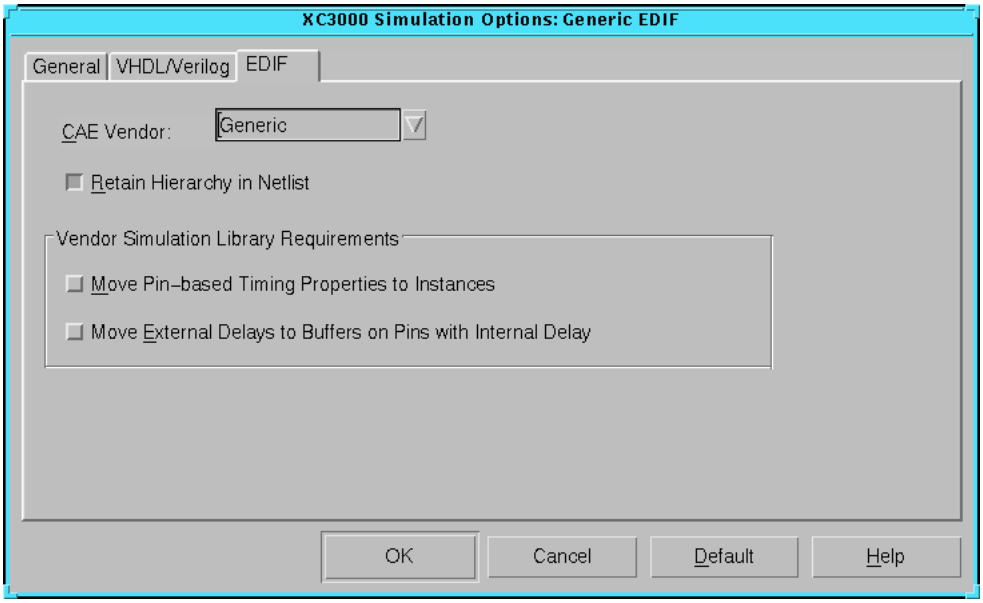


Figure 5-38 XC3000 EDIF Tab

The XC3000 EDIF tab is identical to the tab described in the "Spartan EDIF Tab" section.

XC3000 Configuration Options

Click the Configuration, Startup / Readback, or Tie tab to access the different options within the Configuration Options dialog box. These options affect the Configure step in the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

- "XC3000 Configuration Tab"
- "XC3000 Startup / Readback Tab"
- "XC3000 Tie Tab"

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

XC3000 Configuration Tab

Use this tab, shown in the following figure, to set the following options.

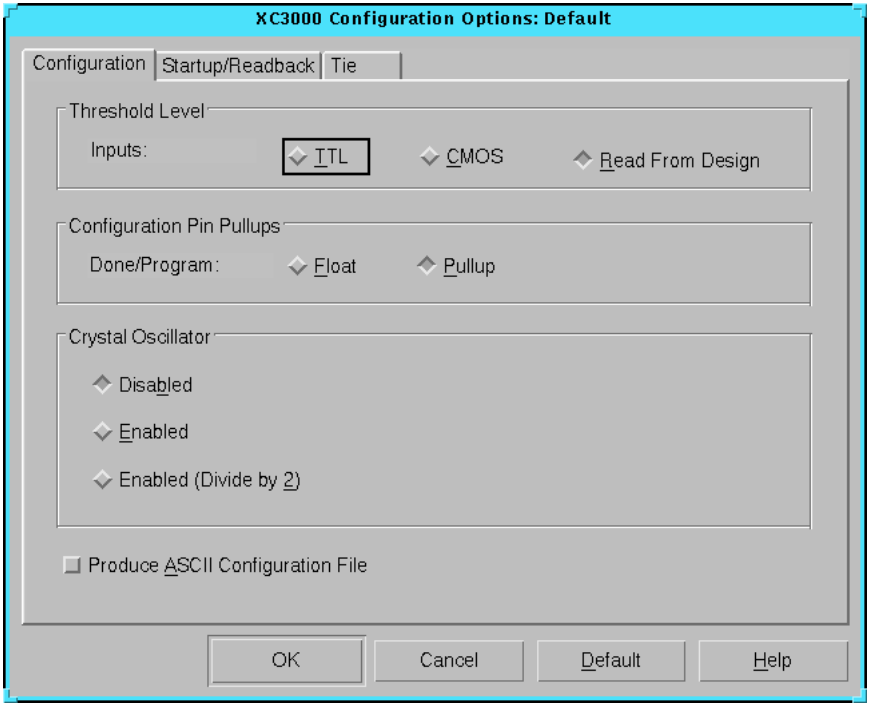


Figure 5-39 XC3000 Configuration Tab

Threshold Level — Inputs

Specify one of the following input options. The default is Read from Design.

- TTL

  Select **TTL** to specify TTL-compatible inputs except for the special purpose clocks, Tclkin, Bclkin, and Pwrdwn which require CMOS input signals.

- CMOS

  Select **CMOS** to specify CMOS compatible inputs.

- Read from Design

  Select **Read from Design** to specify the TTL/CMOS input level included in the physical contraints (PCF) file.

Configuration Pin Pullups — Done/Program

Specify one of the following options. The default is Pullup.

- Float

  This option disables an internal pull-up resistor on the Done/Program (D/$\overline{P}$) pin. The D/$\overline{P}$ pin is an open-drain output that requires a pull-up resistor to indicate the end of the configuration. If this option is selected, an external pull-up resistor should be connected to the D/$\overline{P}$ pin.

- Pullup

  This option enables an internal pull-up resistor on the Done/Program (D/$\overline{P}$) pin. This resistor has a value of 2 to 8 kilohms. The D/$\overline{P}$ pin configures an open-drain driver that requires a pull-up resistor to indicate the end of the configuration. Turn off this option only if you intend to connect an external pull-up resistor to this pin.

Crystal Oscillator

The XC3000 family of devices contains an internal high-speed inverting amplifier which you can use to implement an on-chip crystal oscillator. To use this feature, you must include either the GXTL or OSC library element in your design and connect the appropriate external R-C crystal circuit to the amplifier. See the Xilinx *Libraries Guide* and *The Programmable Logic Data Book* for more information.

Select one of the following options. The default is Disabled.

- Disabled

  Select **Disabled** to disable the crystal oscillator.

- Enabled

  Select **Enabled** to enable the crystal oscillator.

- Enabled (Divide by 2)

  Select **`Enabled (Divide by 2)`** to divide the crystal oscillator frequency by two to generate a symmetrical clock signal.

Produce ASCII Configuration File

This option creates a rawbits (RBT) file in addition to the binary BIT file. The RBT file is a text file that contains ASCII 1s and 0s. These characters represent the actual bits in the configuration bitstream that are downloaded to the FPGA. By default, this option is off.

XC3000 Startup/Readback Tab

Use this tab, shown in the following figure, to set the following options.

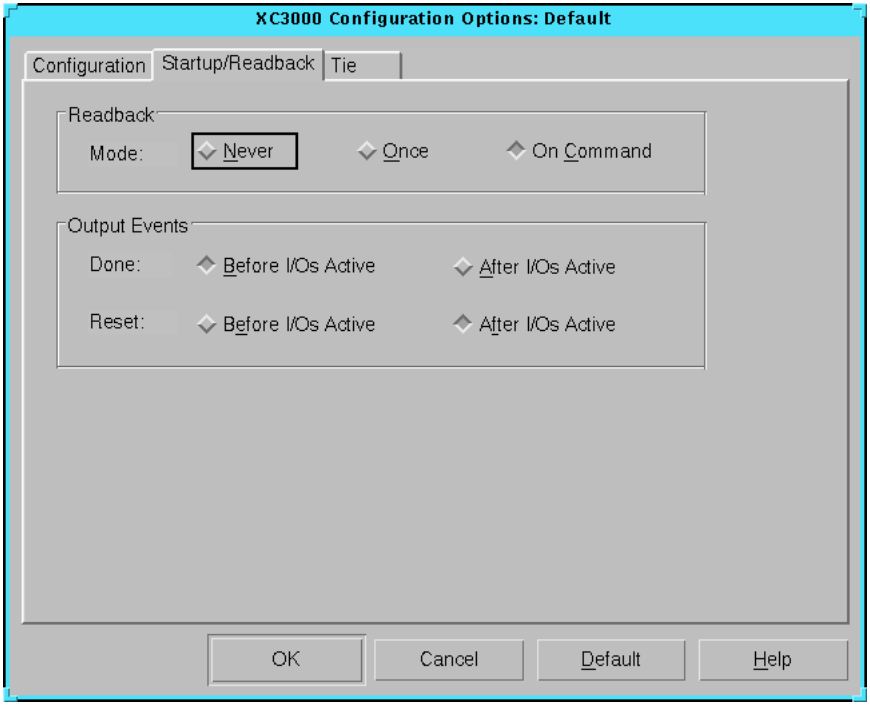


Figure 5-40 XC3000 Startup/Readback Tab

Readback — Mode

After an FPGA is configured, data can be read back and compared with the original configuration data. For security reasons it is sometimes desirable to disable or limit readback capability. The following options control readback. The default is On Command.

- Never

  Select **`Never`** to disable readback.

- Once

  Select **`Once`** to enable a one-time readback.

- On Command

  Select **`On Command`** to enable readback on command. This option generates a .ll file.

Output Events

The Output Events group box contains the following options.

- Done

  The DONE signal indicates the completion of the configuration sequence. You can program this signal to be asserted before or after I/Os go active. The default is Before I/Os Active.

  - Before I/Os Active

    Select **`Before I/Os Active`** to release the DONE signal one Cclk period before the outputs go active.

  - After I/Os Active

    Select **`After I/Os Active`** to release the DONE signal one Cclk period after the outputs go active.

- Reset

  A global reset signal is asserted while the device is configuring during the startup sequence. You can program the release of this signal to occur before or after I/Os go active. The default is After I/Os Active.

- Before I/Os Active

  Select **`Before I/Os Active`** to release the Internal Reset one Cclk period before the outputs go active.

- After I/Os Active

  Select **`After I/Os Active`** to release the Internal Reset one Cclk period after the outputs go active.

XC3000 Tie Tab

Use this tab, shown in the following figure, to set the tie options.

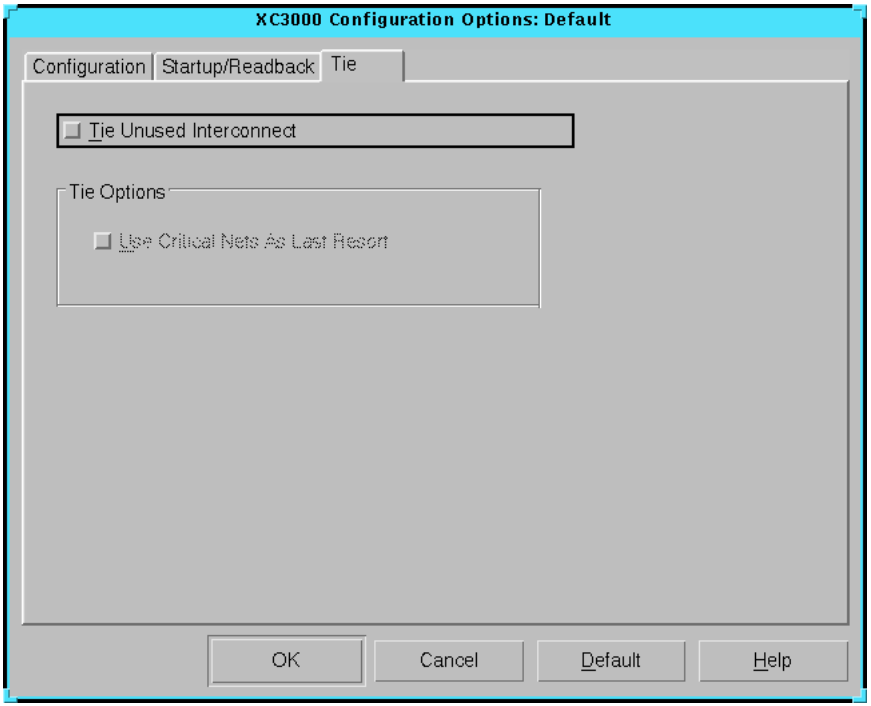


Figure 5-41 XC3000 Tie Tab

The XC3000 Tie tab is identical to the tab described in the “Spartan Tie Tab” section.

XC4000 Implementation Options

Click the Translate, Optimize and Map, Place and Route, or Timing Reports tab to access the different options within the Implementation Options dialog box. These options affect the Translate, Map, and Place&Route steps in the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

XC4000 Translate Tab

Use this tab, shown in the following figure, to set the translate options.

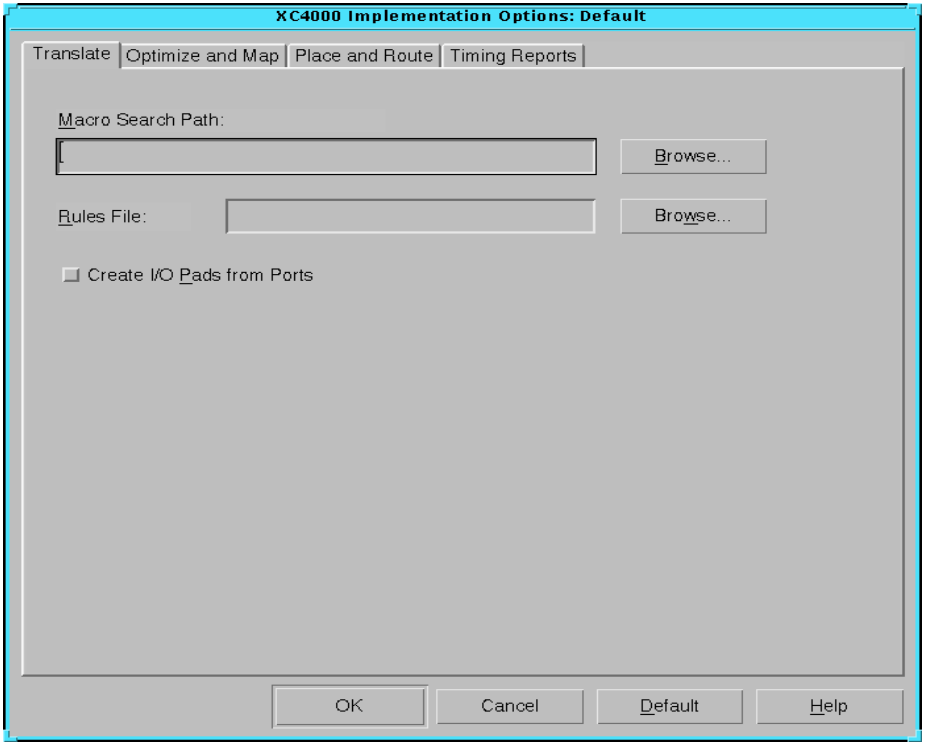


Figure 5-42 XC4000 Translate Tab

The XC4000 Translate tab is identical to the tab described in the "Spartan Translate Tab" section.

XC4000 Optimize and Map Tab

Use this tab, shown in the following figure, to set the optimize and map options.

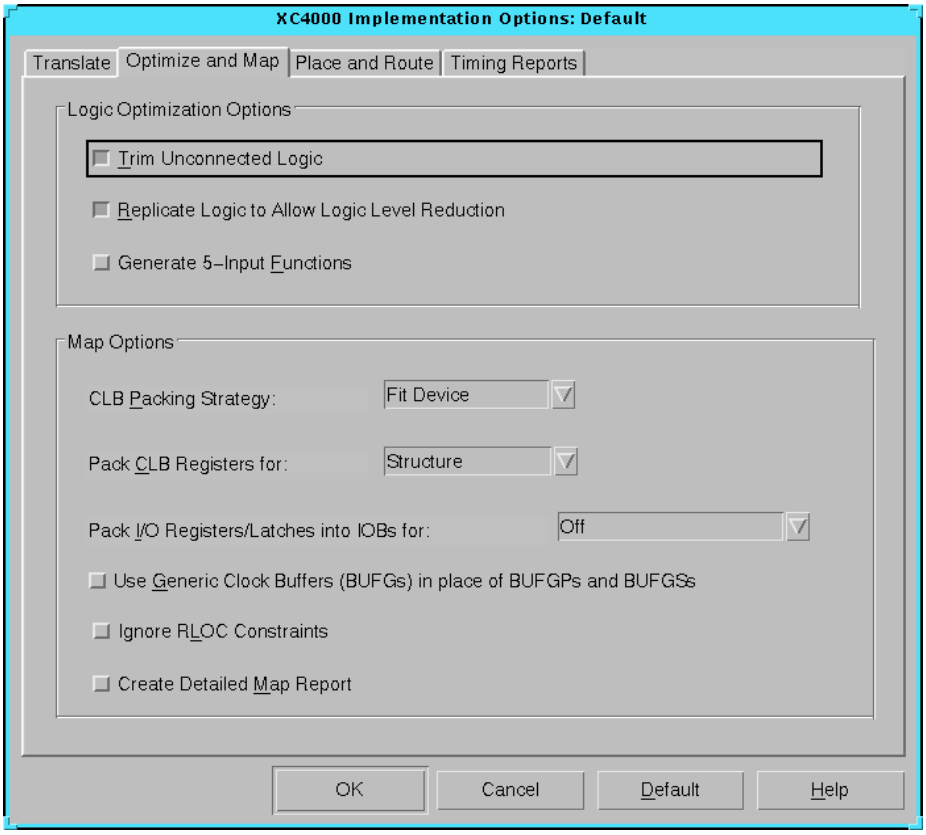


Figure 5-43 XC4000 Optimize and Map Tab

The XC4000 Optimize and Map tab is identical to the tab described in the "Spartan Optimize and Map Tab" section.

XC4000 Place and Route Tab

Use this tab, shown in the following figure, to set the place and route options.

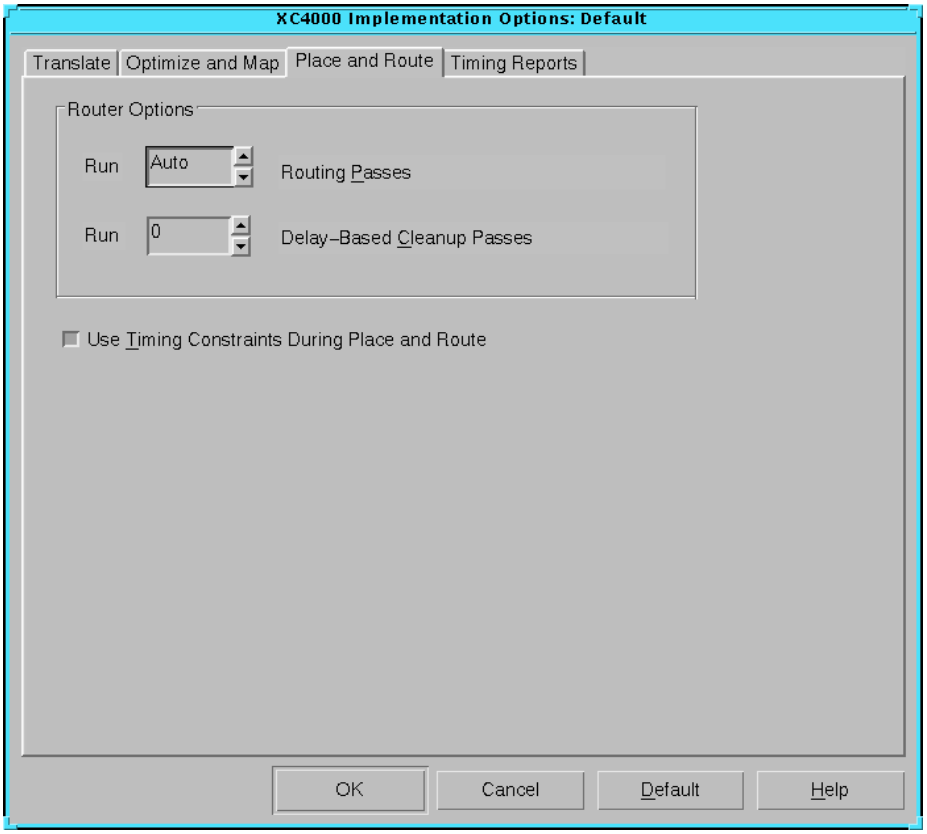


Figure 5-44 XC4000 Place and Route Tab

The XC4000 Place and Route tab is identical to the tab described in the “Spartan Place and Route Tab” section.

XC4000 Timing Reports Tab

Use this tab, shown in the following figure, to set the timing reports options.

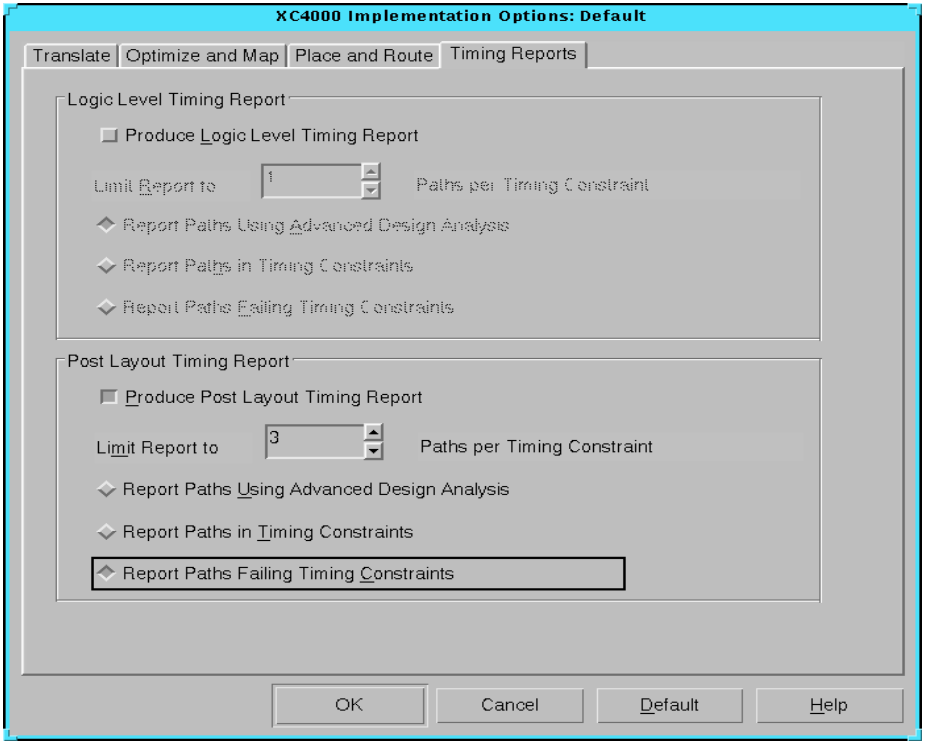


Figure 5-45 XC4000 Timing Reports Tab

The XC4000 Timing Reports tab is identical to the tab described in the "Spartan Timing Reports Tab" section.

XC4000 Simulation Options

Click the General, VHDL / Verilog, or EDIF tab to access the different options within the Simulation Options dialog box. These options affect the timing simulation data produced during the Timing (Sim) step of the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

XC4000 General Tab

Use this tab, shown in the following figure, to set the general simulation options.

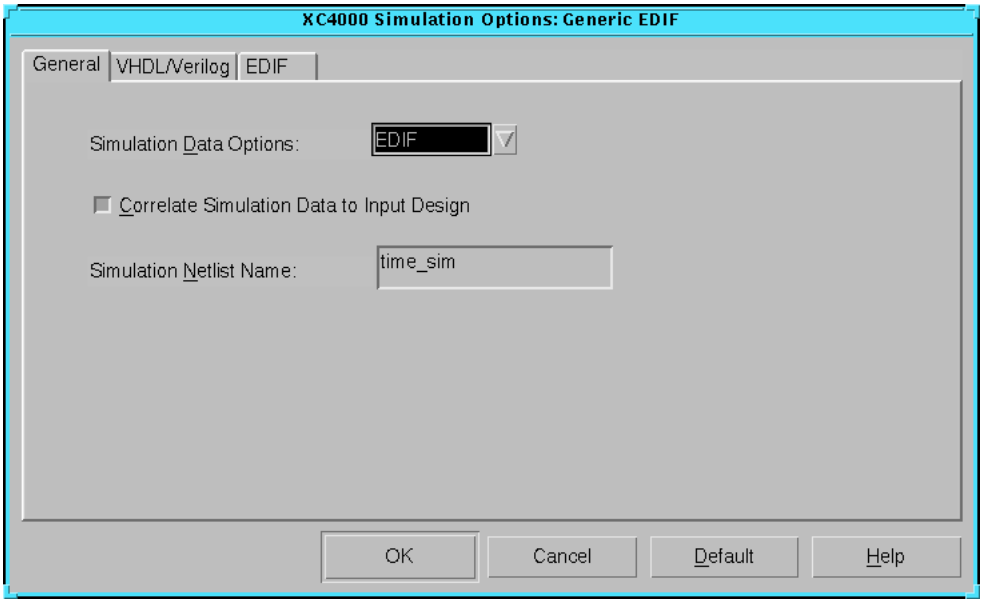


Figure 5-46 XC4000 General Tab

The XC4000 General tab is identical to the tab described in the "Spartan General Tab" section.

XC4000 VHDL/Verilog Tab

Use this tab, shown in the following figure, to set the VHDL or Verilog options.

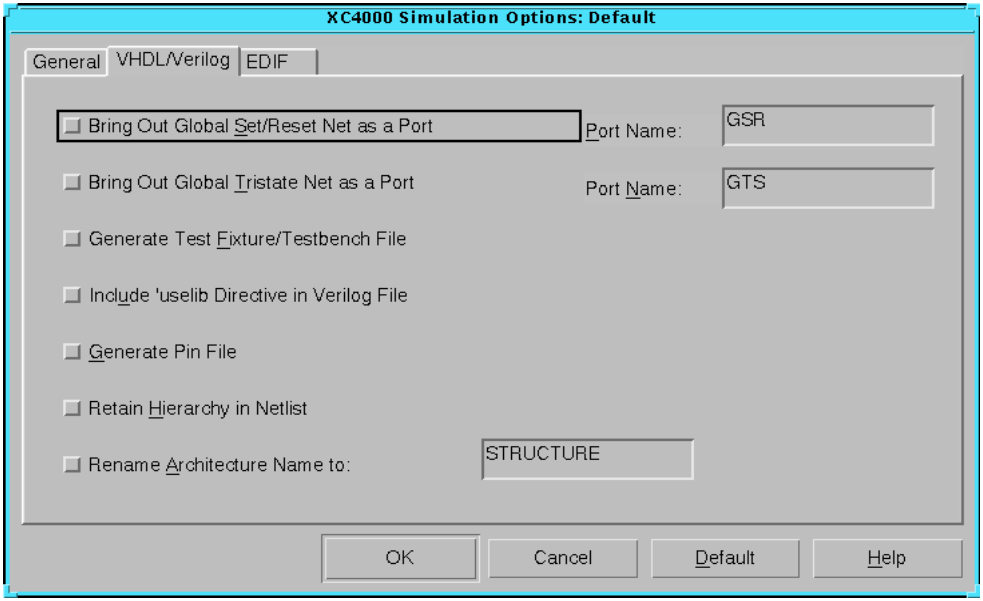


Figure 5-47 XC4000 VHDL/Verilog Tab

The XC4000 VHDL / Verilog tab is identical to the tab described in the "Spartan VHDL / Verilog Tab" section.

XC4000 EDIF Tab

Use this tab, shown in the following figure, to set the EDIF options.

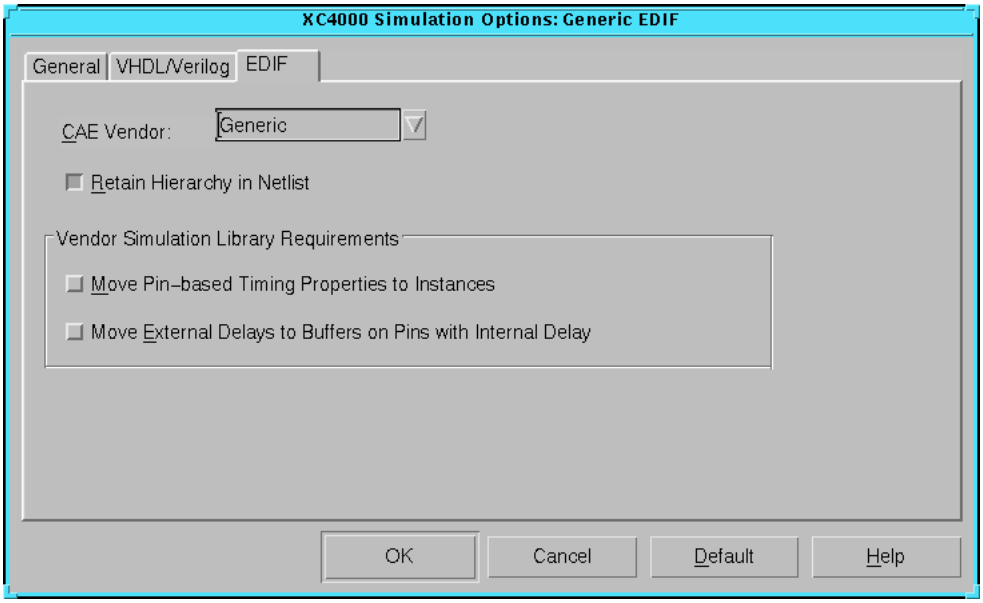


Figure 5-48 XC4000 EDIF Tab

The XC4000 EDIF tab is identical to the tab described in the "Spartan EDIF Tab" section.

XC4000 Configuration Options

Click the Configuration, Startup, Readback, Tie, or Advanced tab to access the different options within the Configuration Options dialog box. These options affect the Configure step in the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

- "XC4000 Configuration Tab"
- "XC4000 Startup Tab"
- "XC4000 Readback Tab"
- "XC4000 Tie Tab"
- "XC4000 Advanced Tab"

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

XC4000 Configuration Tab

Use this tab, shown in the following figure, to set the following options.

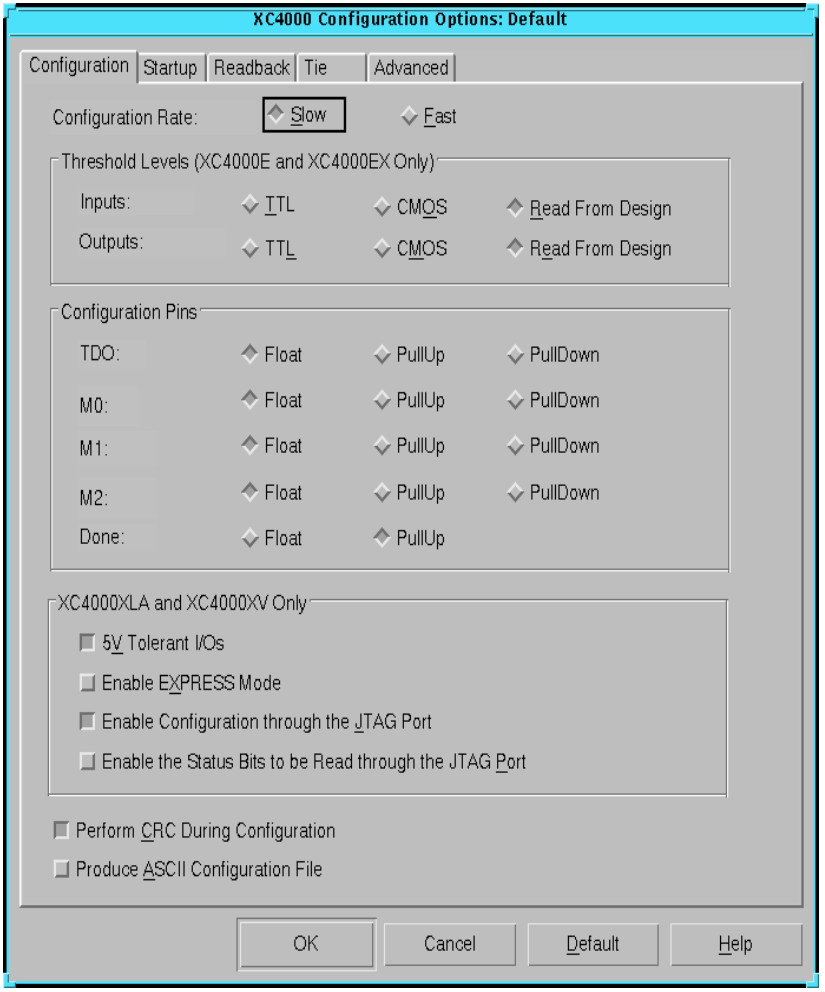


Figure 5-49 XC4000 Configuration Tab

Configuration Rate

The XC4000 uses an internal configuration clock, CCLK, when configuring in a master mode. The configuration rate option allows you to select the rate for this clock. The following options are available. The default is Slow.

- Slow

  Select **Slow** to set the configuration clock rate to 1 MHz (nominal).

- Fast

  Select **Fast** to set the configuration clock rate to 8 MHz (nominal).

Threshold Levels (XC4000E and XC4000EX Only)

The Threshold Levels group box contains the following options.

Note: These options are supported for the XC4000E and XC4000EX subfamilies only.

- Inputs

  Specify one of the following input options. The default is Read from Design.

  - TTL

    Select **TTL** to specify TTL-compatible inputs.

  - CMOS

    Select **CMOS** to specify CMOS-compatible inputs.

  - Read from Design

    Select **Read from Design** to specify the TTL / CMOS input level included in the physical contraints (PCF) file.

- Outputs

  Specify one of the following output options. The default is Read from Design.

  - TTL

    Select **TTL** to specify TTL-compatible output.

- CMOS

  Select **CMOS** to specify CMOS-compatible outputs.

- Read from Design

  Select **Read from Design** to specify the TTL/CMOS output level included in the PCF file.

Configuration Pins

The Configuration Pins group box contains the following options.

- TDO

  The TDO pin can be used as tristatable output pin. The value of the pull-up and pull-down resistors is 50 to 100 kilohms. The following options are available. The default is Float.

  - Float

    Select **Float** to disable both the pull-up resistor and pull-down resistor on the TDO pin.

  - PullUp

    Select **PullUp** to enable a pull-up on the TDO pin.

  - PullDown

    Select **PullDown** to enable a pull-down on the TDO pin.

- M0

  The M0 pin is used to determine the configuration mode. The value of the pull-up and pull-down resistors is 50 to 100 kilohms. The following options are available. The default is Float.

  - Float

    Select **Float** to disable both the pull-up resistor and pull-down resistor on the M0 pin.

  - PullUp

    Select **PullUp** to enable a pull-up on the M0 pin.

  - PullDown

    Select **PullDown** to enable a pull-down on the M0 pin.

- M1

  The M1 pin can be used as tristatable output pin. The value of the pull-up and pull-down resistors is 50 to 100 kilohms. The following options are available. The default is Float.

  - Float

    Select **`Float`** to disable both the pull-up resistor and pull-down resistor on the M1 pin.

  - PullUp

    Select **`PullUp`** to enable a pull-up on the M1 pin.

  - PullDown

    Select **`PullDown`** to enable a pull-down on the M1 pin.

- M2

  The M2 pin is used to determine the configuration mode. The value of the pull-up and pull-down resistors is 50 to 100 kilohms. The following options are available. The default is Float.

  - Float

    Select **`Float`** to disable both the pull-up resistor and pull-down resistor on the M2 pin.

  - PullUp

    Select **`PullUp`** to enable a pull-up on the M2 pin.

  - PullDown

    Select **`PullDown`** to enable a pull-down on the M2 pin.

- Done

  The DONE pin configures an open-drain driver that requires a pull-up resistor to indicate the end of the configuration. The value of the pull-up resistor is 2 to 8 kilohms. The following options are available. The default is PullUp.

  - Float

    Select **`Float`** to disable the pull-up resistor on the DONE pin. If you select this option, be sure you have connected an external pull-up resistor to this pin.

- PullUp

  Select **PullUp** to enable an internal pull-up resistor on the DONE pin in XC4000 devices. Select this option only if you do not connect an external pull-up resistor to this pin.

XC4000XLA and XC4000XV Only

This group box contains the following options.

- 5V Tolerant I/Os

  This option allows a 3.3 V device circuitry to tolerate 5 V operation. For any device that operates on a mixed circuit environment with 3.3V and 5V, use this option. For any circuitry that operates exclusively on 3.3 V, such as in a laptop computer, turn this option off. Turning off this option reduces power consumption. By default, this option is on.

Note: Enabling this option allows the device's clamping diodes to clamp ringing transients back to the 3.3 V supply rail. A clamping diode is connected from each output to VCC. This option affects all I/O pins.

- Enable EXPRESS Mode

  This option enables express mode configuration. In this mode, configuration data is presented to the device in parallel format, and each new byte is clocked into the target device with every rising edge of the CCLK. This mode is eight times as fast as other configuration modes because data is processed at the rate of one byte per CCLK rather than one bit per CCLK. By default, this option is off.

- Enable Configuration Through the JTAG Port

  This option allows BSCAN-based configuration after the device is successfully configured. This feature allows board testing without the risk of reconfiguring XLA devices by toggling the TCK/TMS/TDI/TDO lines. By default, this option is on.

- Enable the Status Bits to be Read Through the JTAG Port

  This option allows direct sensing of the DONE configuration state after performing a BSCAN-based configuration. This allows you to determine if a BSCAN-based configuration was successful. By default, this option is off.

Perform CRC During Configuration

This option enables Cyclic Redundancy Checking (CRC) error checking during configuration. If enabled, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each data frame in the configuration bitstream. This allows the device to perform a CRC check on the bitstream during the configuration process. If disabled, the device performs a simple check for the 0110 pattern at the end of each frame in the configuration data. By default, this option is on.

Produce ASCII Configuration File

This option creates a rawbits (RBT) file in addition to the binary BIT file. The RBT file is a text file that contains ASCII 1s and 0s. These characters represent the actual bits in the configuration bitstream that are downloaded to the FPGA. By default, this option is off.

XC4000 Startup Tab

Use this tab, shown in the following figure, to set the configuration startup options.

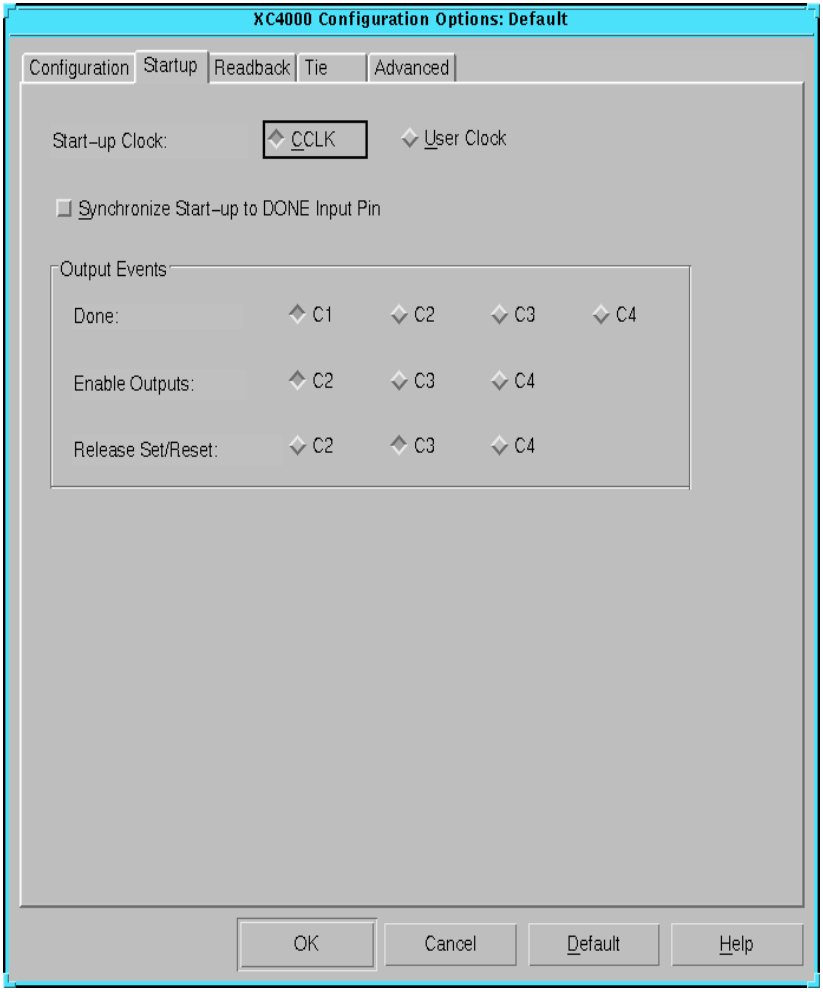


Figure 5-50 XC4000 Startup Tab

The XC4000 Startup tab is identical to the tab described in the "Spartan Startup Tab" section.

XC4000 Readback Tab

Use this tab, shown in the following figure, to set the configuration readback options.

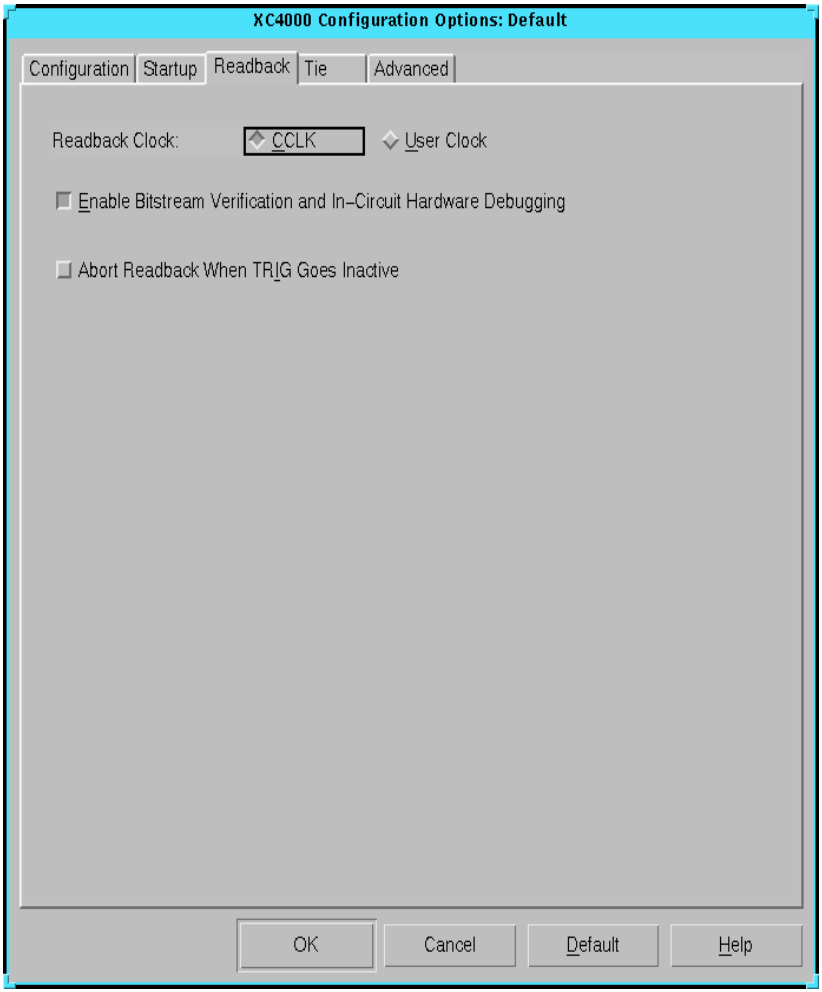


Figure 5-51 XC4000 Readback Tab

The XC4000 Readback tab is identical to the tab described in the "Spartan Readback Tab" section.

XC4000 Tie Tab

Use this tab, shown in the following figure, to set the tie options.

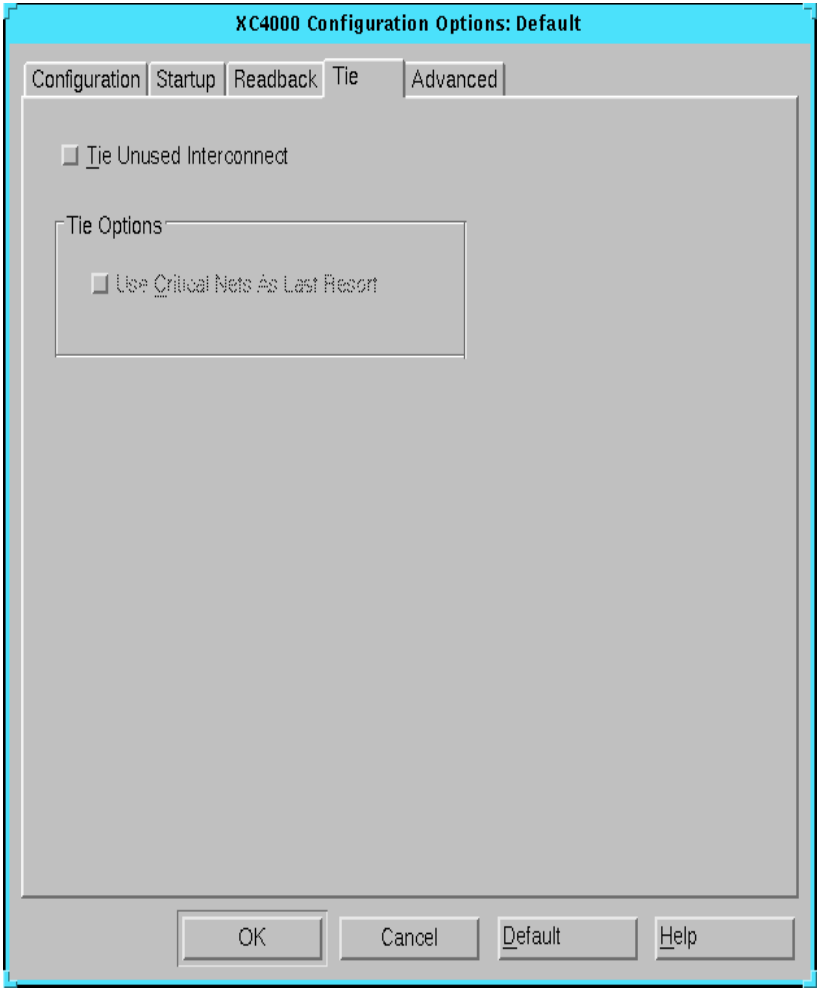


Figure 5-52 XC4000 Tie Tab

The X4000 Tie tab is identical to the tab described in the “Spartan Tie Tab” section.

XC4000 Advanced Tab

Use this tab, shown in the following figure, to set the following options.

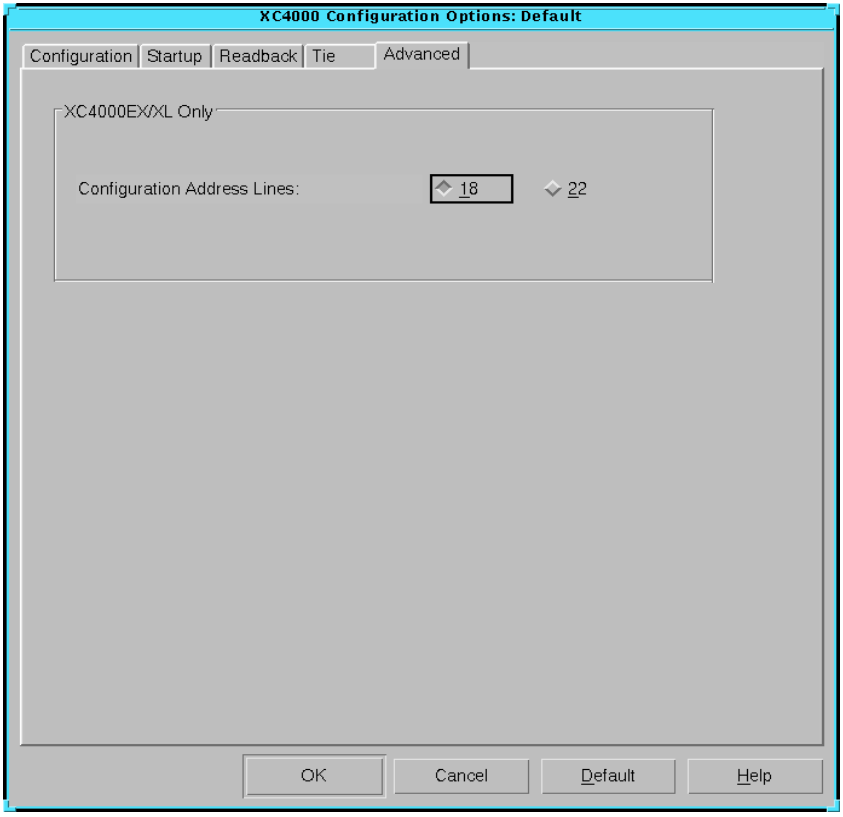


Figure 5-53 XC4000 Advanced Tab

XC4000EX/XL Only — Configuration Address Lines

Use the Configuration Address Lines option to set the number of address lines that will be used by the FPGA during device configuration. Address lines are used to address data from a parallel PROM or flash memory device. Select either 18 or 22. If you choose 22, four extra device pins are activated as configuration address lines. The default is 18.

This option only applies to master parallel mode configuration. You must set this option in addition to setting the mode pins. Refer to the *Programmable Logic Data Book* for more information on address lines and master parallel mode configuration.

XC5200 Implementation Options

Click the Translate, Optimize and Map, Place and Route, or Timing Reports tab to access the different options within the Implementation Options dialog box. These options affect the Translate, Map, and Place&Route steps in the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

- "XC5200 Translate Tab"
- "XC5200 Optimize and Map Tab"
- "XC5200 Place and Route Tab"
- "XC5200 Timing Reports Tab"

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

XC5200 Translate Tab

Use this tab, shown in the following figure, to set the translate options.

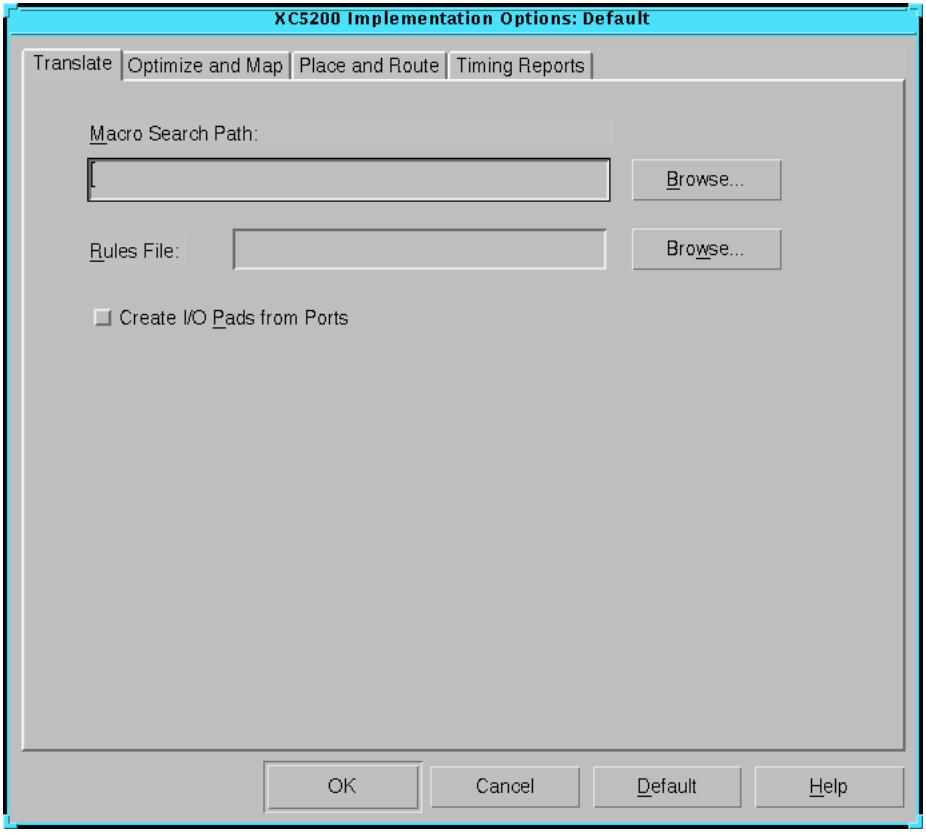


Figure 5-54 XC5200 Translate Tab

The XC5200 Translate tab is identical to the tab described in the "Spartan Translate Tab" section.

XC5200 Optimize and Map Tab

Use the Optimize and Map tab, shown in the following figure, to set these options.

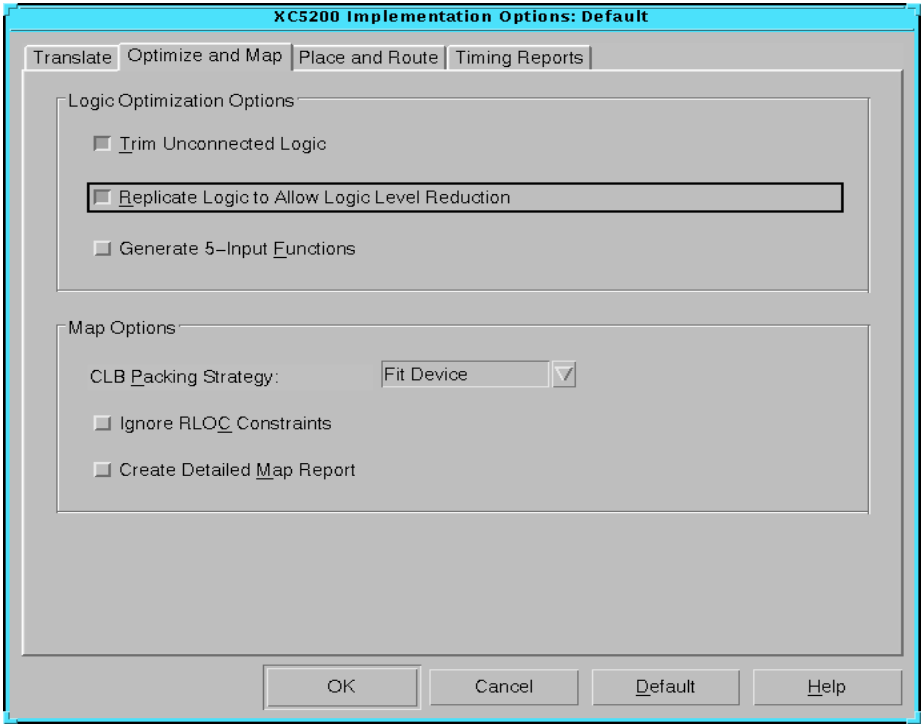


Figure 5-55 XC5200 Optimize and Map Tab

Logic Optimization Options

The Logic Optimization Options group box contains the following options.

- Trim Unconnected Logic

  Select this option to trim unconnected components and nets from the design before mapping occurs. Deselect this option to map unconnected components and nets. Deselecting this option is useful for estimating the logic resources required for a design and for obtaining timing information on partially finished designs. When implementing an unfinished design, deselect this option to

prevent partial logic from being trimmed. By default, this option is on.

- Replicate Logic to Allow Logic Level Reduction

  Use this option to replicate a single driver that drives multiple loads and map it as separate components that drive individual loads. This option is useful for creating a mapping strategy that may more readily meet your timing constraints. It reduces the number of logic elements through which a signal must pass, thereby eliminating path delays. By default, this option is on.

- Generate 5-Input Functions

  Select this option to map each five-input logic function to a single CLB. This option can sometimes reduce the number of cell-to-cell delays at the expense of increased CLB count. By default, this option is off.

Map Options

The Map Options group box contains the following options.

- CLB Packing Strategy

  This option partitions logic more densely. Normally, the mapper partitions logic to maximize signal sharing within CLBs and to minimize routing congestion. The CLB Packing Strategy option optimizes density by relaxing the requirement for a high degree of signal sharing between logic elements in a CLB, using the DI (direct flip-flop input) pins on CLBs, and reducing minimum signal combining requirements. The default is Fit Device.

Note: Although the CLB Packing Strategy option makes a design denser, it can also adversely affect place and route performance, resulting in higher delays and more unrouted nets. Use this option if you are willing to trade performance for density.

- Fit Device

  Select **`Fit Device`** to pack logic elements that do not share common signals into the CLBs. The mapper continues packing until the design fits into the selected device or no further packing is possible.

- Off

  Select **Off** to disable the CLB Packing Strategy option. Disabling this option causes only related logic (logic with common inputs) to be packed together. This is useful for increasing speed in high speed designs. However, the design may overflow the selected part due to the increase in CLBs used.

- Ignore RLOC Constraints

  Select this option to cause Map to ignore the RLOC information that contains the relative placement of one CLB to another. This option also causes Map to ignore any invalid RLOC information that would result in a Map error. By default, this option is off.

Note: To ensure CLBs containing carry logic are aligned properly, Map retains the RLOC information that dictates what is packed into an individual CLB.

- Create Detailed Map Report

  Select this option to create a detailed Map report that includes signal and symbol cross-reference information. By default, this option is off.

XC5200 Place and Route Tab

Use this tab, shown in the following figure, to set the place and route options.

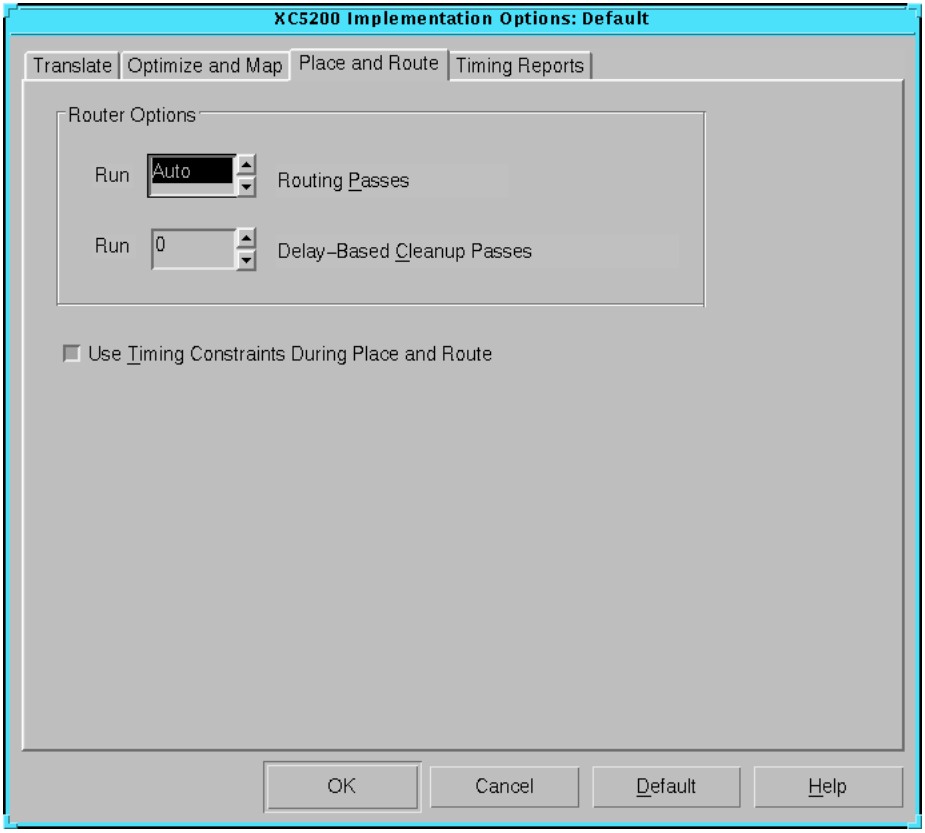


Figure 5-56 XC5200 Place and Route Tab

The XC5200 Place and Route tab is identical to the tab described in the “Spartan Place and Route Tab” section.

XC5200 Timing Reports Tab

Use the Timing Reports tab, shown in the following figure, to set the timing reports options.

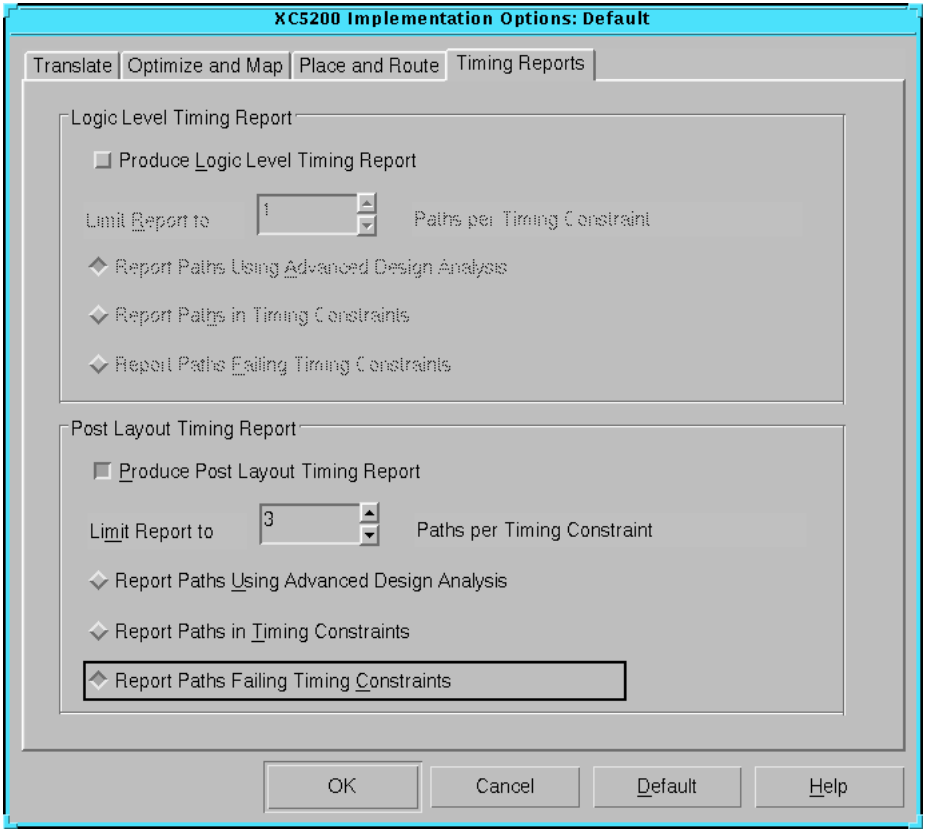


Figure 5-57 XC5200 Timing Reports Tab

The XC5200 Timing Reports tab is identical to the tab described in the "Spartan Timing Reports Tab" section.

XC5200 Simulation Options

Click the General, VHDL / Verilog, or EDIF tab to access the different options within the Simulation Options dialog box. These options affect the timing simulation data produced during the Timing (Sim)

step of the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

XC5200 General Tab

Use this tab, shown in the following figure, to set the general simulation options.

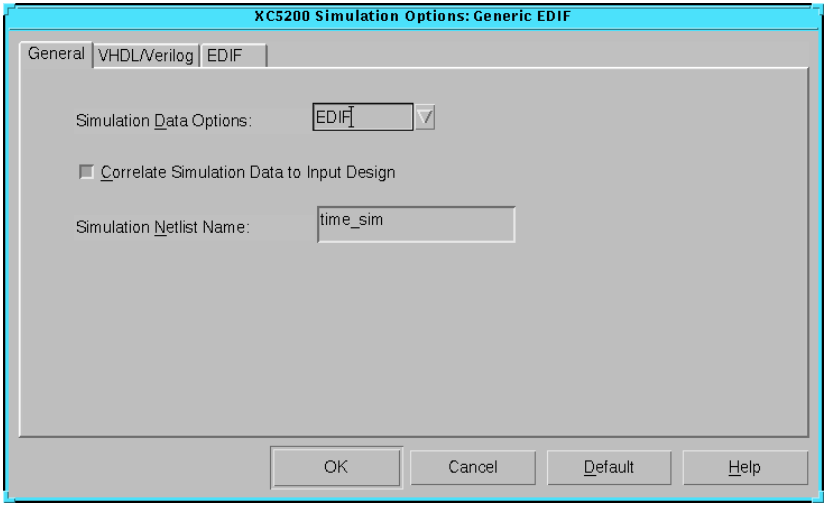


Figure 5-58 XC5200 General Tab

The XC5200 General tab is identical to the tab described in the "Spartan General Tab" section.

XC5200 VHDL/Verilog Tab

Use this tab, shown in the following figure, to set the VHDL or Verilog options.

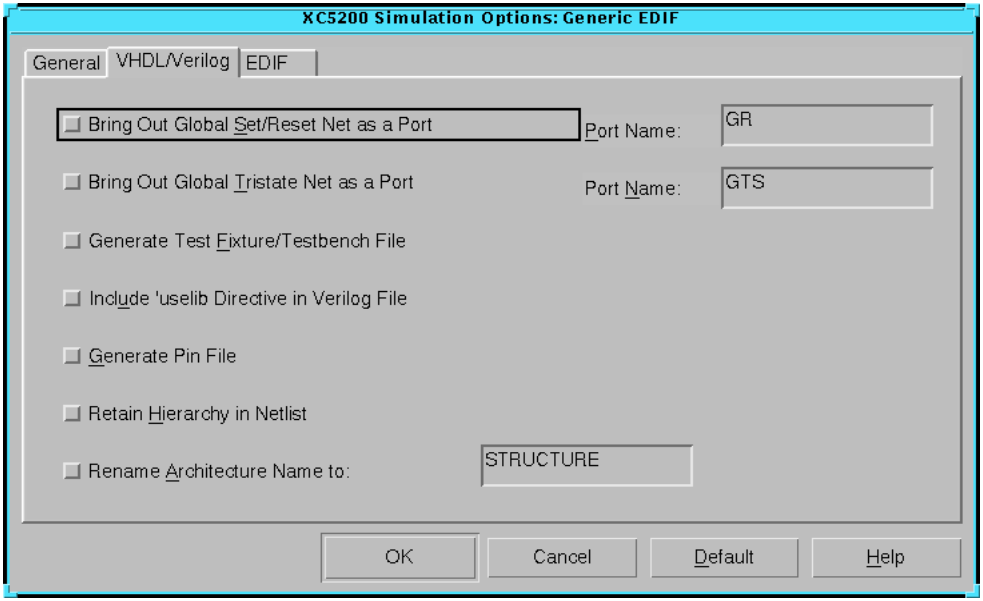


Figure 5-59 XC5200 VHDL/Verilog Tab

The XC5200 VHDL / Verilog tab is identical to the tab described in the "Spartan VHDL / Verilog Tab" section.

XC5200 EDIF Tab

Use this tab, shown in the following figure, to set the EDIF options.

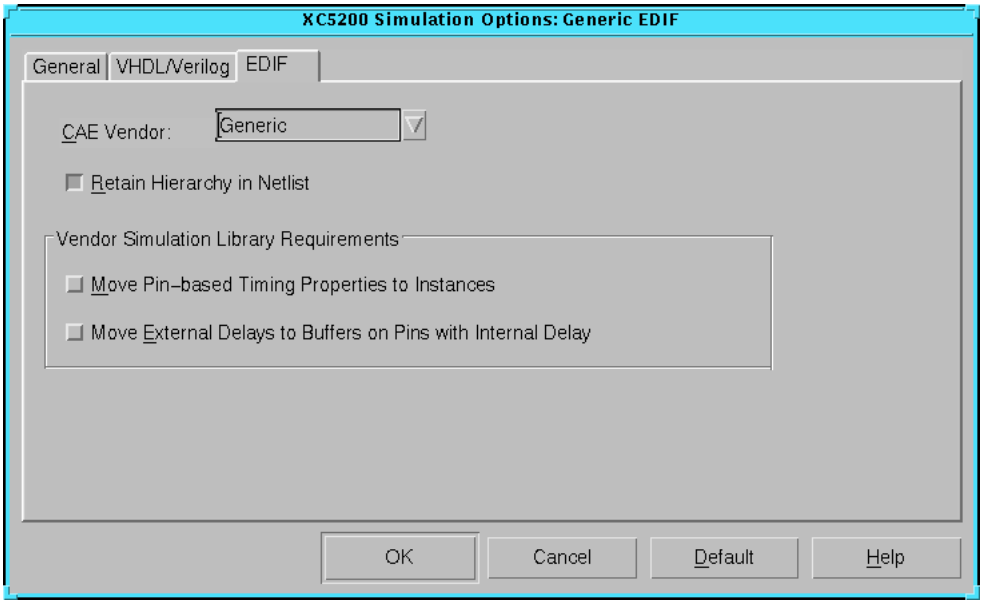


Figure 5-60 XC5200 EDIF Tab

The XC5200 EDIF tab is identical to the tab described in the "Spartan EDIF Tab" section.

XC5200 Configuration Options

Click the Configuration, Startup, Readback, or Tie tab to access the different options within the Configuration Options dialog box. These options affect the Configure step in the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

- "XC5200 Configuration Tab"
- "XC5200 Startup Tab"
- "XC5200 Readback Tab"
- "XC5200 Tie Tab"

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

XC5200 Configuration Tab

Use this tab, shown in the following figure, to set the following options.

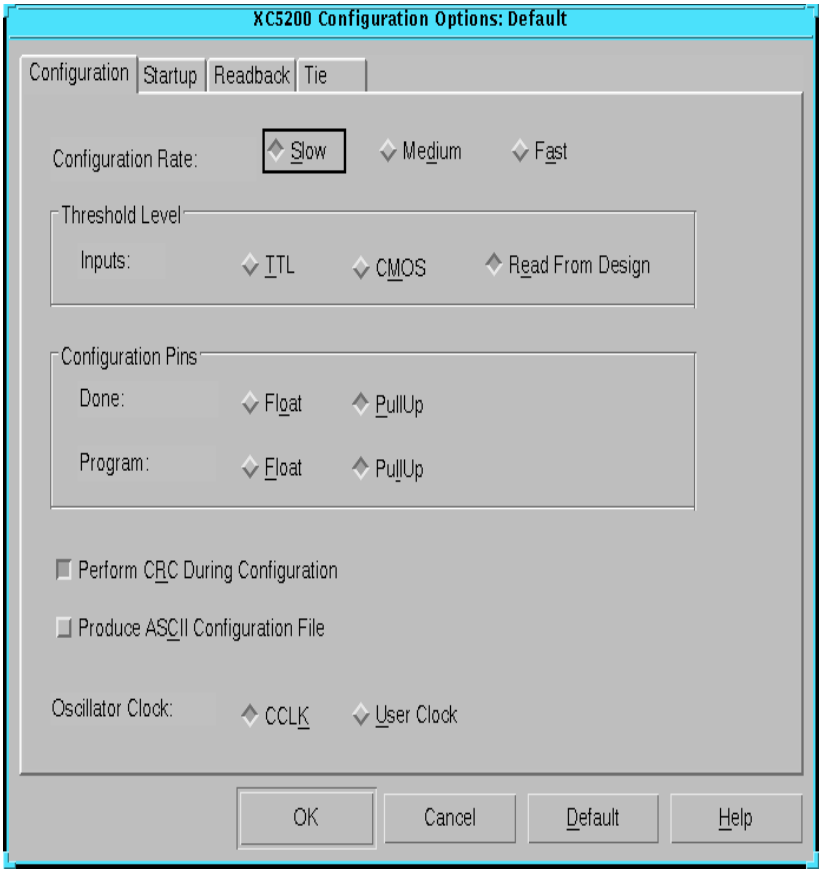


Figure 5-61 XC5200 Configuration Tab

Configuration Rate

The XC5200 uses an internal configuration clock, CCLK, when configuring in a master mode. The configuration rate option allows you to select the rate for this clock. The following options are available. The default is Slow.

- Slow

  Select **Slow** to set the configuration clock rate to 0.75 MHz (nominal).

- Medium

  Select **Medium** to set the configuration clock rate to 6 MHz (nominal).

- Fast

  Select **Fast** to set the configuration clock rate to 12 MHz (nominal).

Threshold Level — Inputs

Select one of the following input options. The default is Read from Design.

- TTL

  Select **TTL** to specify TTL-compatible inputs.

- CMOS

  Select **CMOS** to specify CMOS-compatible inputs.

- Read from Design

  Select **Read from Design** to specify the TTL / CMOS input level included in the physical contraints (PCF) file.

Configuration Pins

The Configuration Pins group box contains the following options.

- Done

  The DONE pin configures an open-drain driver that requires a pull-up resistor to indicate the end of the configuration. The following options are available. The default is PullUp.

- Float

  Select **Float** to disable the pull-up resistor on the DONE pin. If you select this option, be sure you have connected an external pull-up resistor to this pin.

- PullUp

  Select **PullUp** to enable an internal pull-up resistor on the DONE pin. This resistor has a value of 2 to 8 kilohms. Select this option only if you do not connect an external pull-up resistor to this pin.

- Program

  The $\overline{\text{PROG}}$ pin allows device reprogramming. The value of the pull-up resistor is 50 to 100 kilohms. The following options are available. The default is PullUp.

  - Float

    Select **Float** to disable the pull-up resistor on the $\overline{\text{PROG}}$ pin.

  - PullUp

    Select **PullUp** to enable an internal pull-up resistor on the $\overline{\text{PROG}}$ pin.

Perform CRC During Configuration

This option enables Cyclic Redundancy Checking (CRC) error checking during configuration. If enabled, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each data frame in the configuration bitstream. This allows the device to perform a CRC check on the bitstream during the configuration process. If disabled, the device performs a simple check for the 0110 pattern at the end of each frame in the configuration data. By default, this option is on.

Produce ASCII Configuration File

This option creates a rawbits (RBT) file in addition to the binary BIT file. The RBT file is a text file that contains ASCII 1s and 0s. These characters represent the actual bits in the configuration bitstream that are downloaded to the FPGA. By default, this option is off.

Oscillator Clock

This option determines whether the XC5200 oscillator will be driven by the internal clock or by a user clock. The default is CCLK.

- CCLK

  Select **CCLK** to drive the oscillator with the internal 16 MHz clock.

- User Clock

  Select **User Clock** to drive the oscillator with a user clock. If you specify User Clock, the clock must be connected to the OSC.CK pin of the device's OSC component.

XC5200 Startup Tab

Use this tab, shown in the following figure, to set the configuration startup options.

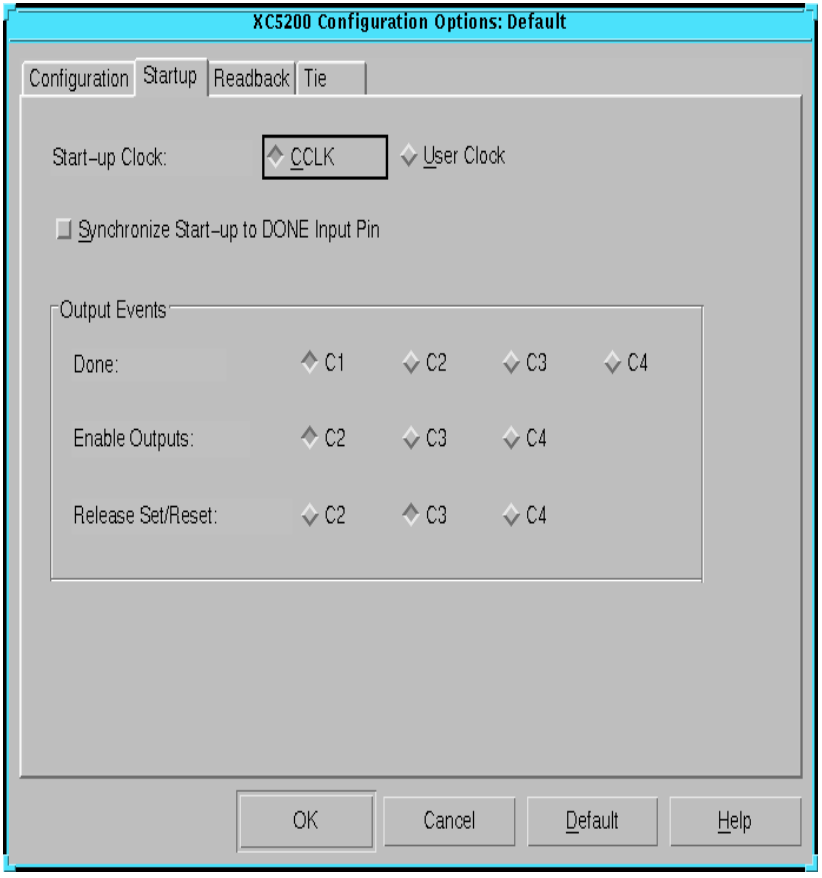


Figure 5-62 XC5200 Startup Tab

The XC5200 Startup tab is identical to the tab described in the "Spartan Startup Tab" section.

XC5200 Readback Tab

Use this tab, shown in the following figure, to set the configuration readback options.

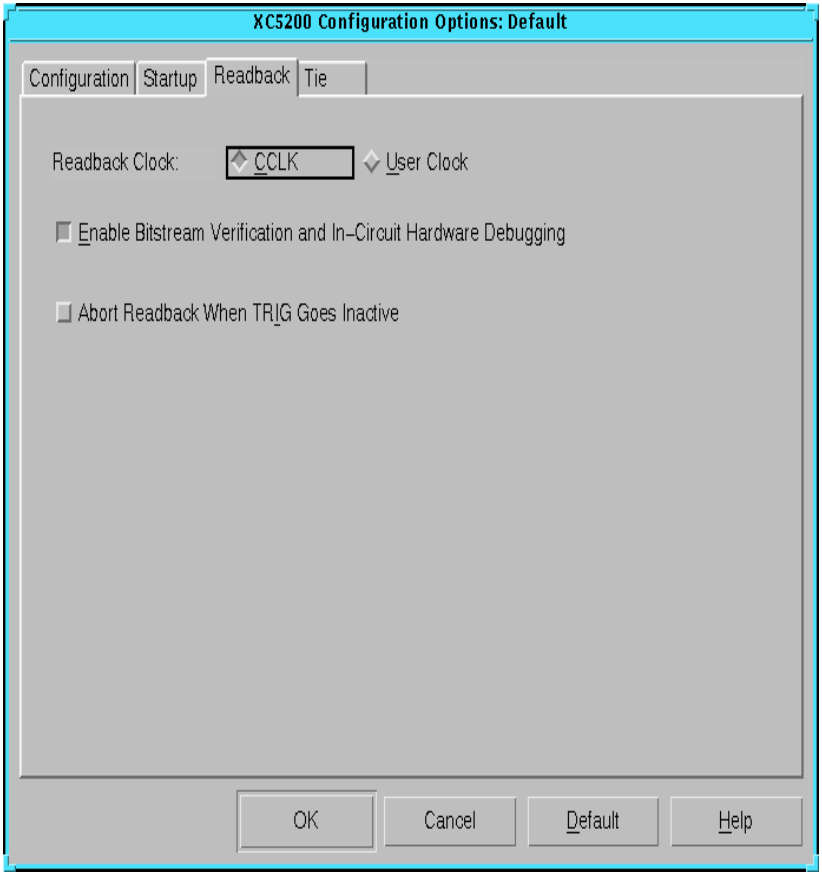


Figure 5-63 XC5200 Readback Tab

The XC5200 Readback tab is identical to the tab described in the "Spartan Readback Tab" section.

XC5200 Tie Tab

Use this tab, shown in the following figure, to set the tie options.

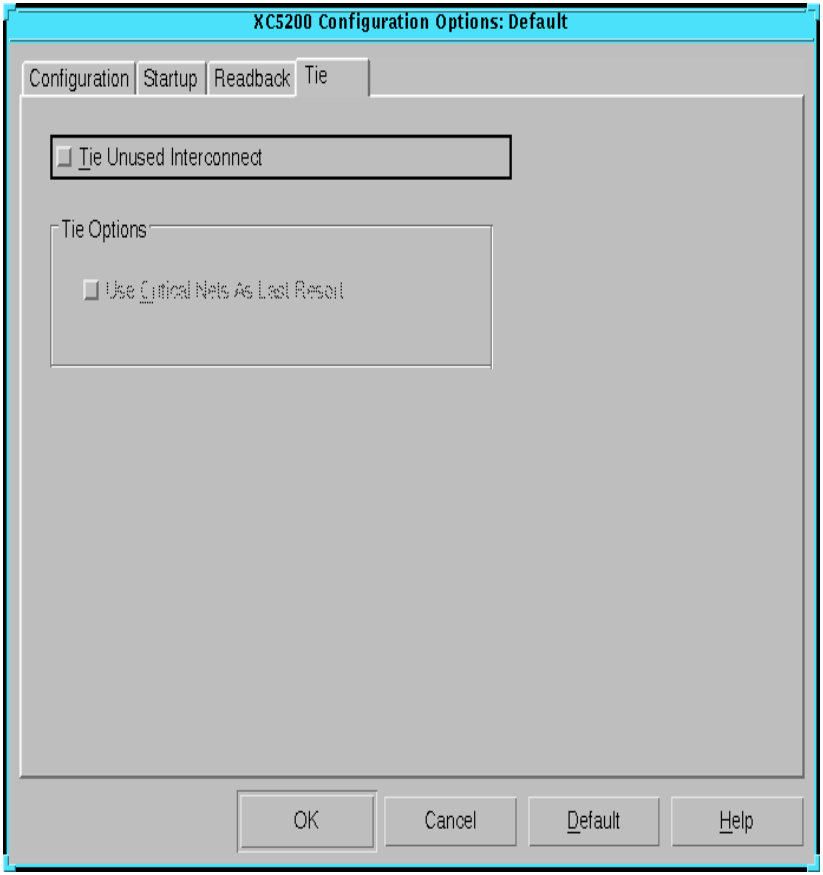


Figure 5-64 XC5200 Tie Tab

The XC5200 Tie tab is identical to the tab described in the “Spartan Tie Tab” section.

XC9500 Implementation Options

Click the Translate, Basic, Advanced, Timing Reports, or Programming tab to access the different options within the Implementation Options dialog box. These options affect the Translate, Fit, and

Bitstream steps in the implementation flow. Use the different tabs of this dialog box to set the options described in the following sections.

- "XC9500 Translate Tab"
- "XC9500 Basic Tab"
- "XC9500 Advanced Tab"
- "XC9500 Programming Tab"

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options which are optimized for speed, or click **Help** to obtain online help.

Note: In addition to the Balanced optimization default options, there are two preset implementation option templates: Speed optimization and Area optimization. The defaults described in the following sections only apply to the Balanced optimization options.

XC9500 Translate Tab

Use this tab, shown in the following figure, to set the translate options.

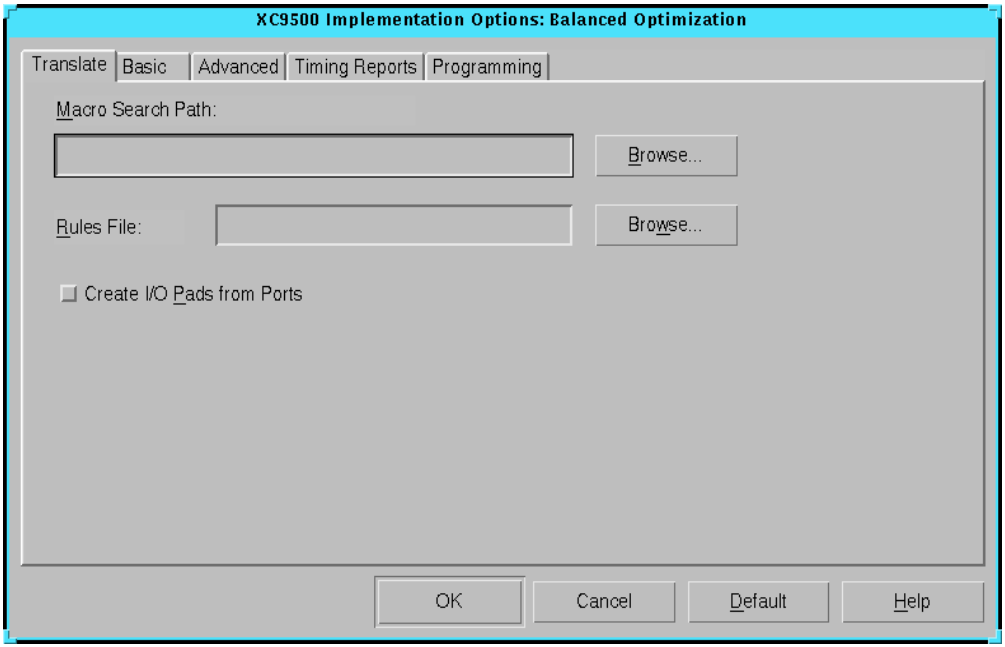


Figure 5-65 XC9500 Translate Tab

The XC9500 Translate tab is identical to the tab described in the "Spartan Translate Tab" section.

XC9500 Basic Tab

Use this tab, shown in the following figure, to set the following options.

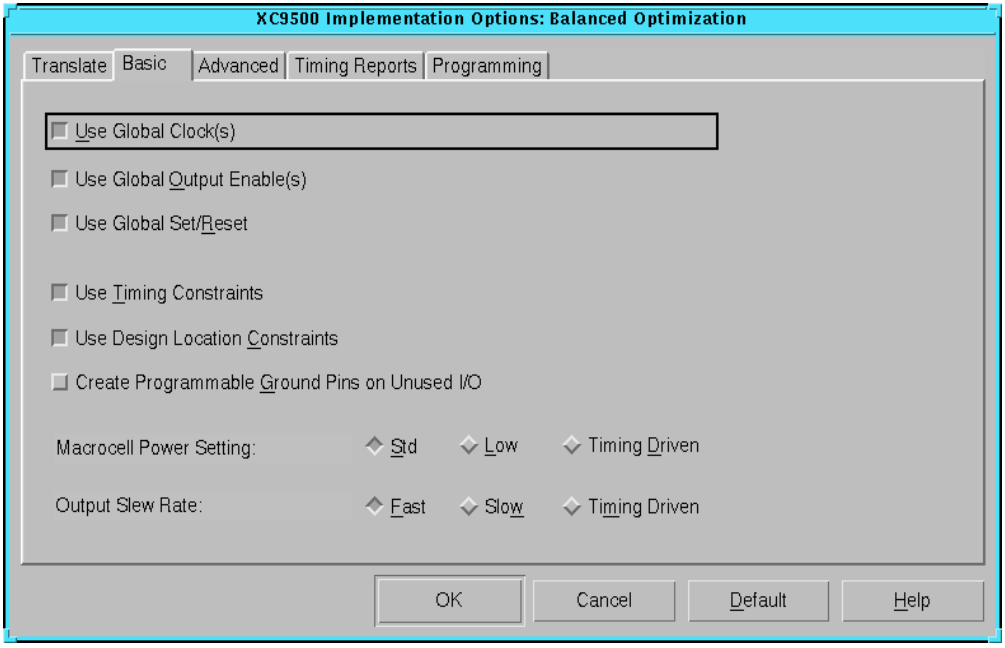


Figure 5-66 XC9500 Basic Tab

Use Global Clock(s)

Select this option to convert the p-term clock to a global clock. The global clock may allow you to meet your timing constraints more easily. By default, this option is on.

Use Global Output Enable(s)

Select this option to convert the p-term output enable to global output enable. Global output enable may allow you to meet your timing constraints more easily. By default, this option is on.

Use Global Set/Reset

Select this option to convert the p-term set/reset to global set/reset. Global set/reset may allow you to meet your timing constraints more easily. By default, this option is on.

Use Timing Constraints

Select this option to indicate that you want the software to use your timing constraints to perform timing-driven optimization in the fitting of your design. For this option to be useful, you must have previously created a timing constraints file or you must have included timing constraints in your design. By default, this option is on.

Use Design Location Constraints

Select this option to indicate that you want to use pinout and macrocell location information in the design file or in a constraint file. Deselect this option to allow the fitter to place pins and logic anywhere or as specified in the guide file. By default, this option is on.

Create Programmable Ground Pins on Unused I/O

Select this option to indicate that you want all unused I/O pads to be configured as ground pins. This may reduce ground bounce. By default, this option is off.

Macrocell Power Setting

Use this option to control device power consumption. Select **`Std`** (standard), **`Low`**, or **`Timing Driven`** to set the default power mode for the macrocells used to implement the design. The default is Std.

Note: Any explicit power control statements in the design or constraints file have precedence over the Default Power Setting.

- Std

  Select **`Std`** to set the power mode for the macrocells to higher speed and higher power.

- Low

  Select **`Low`** to reduce power consumption and reduce speed.

- Timing Driven

  Select **`Timing Driven`** to set the power consumption based on your timing constraints.

Output Slew Rate

Use this option to modify the output slew rate. Limiting the slew rate reduces output switching surges in the device. You can control the transition time of device output pins by setting the slew rate to Fast, Slow, or Timing Driven. The default is Fast.

Note: Any explicit slew rate control statements in the design or constraints file have precedence over the Output Slew Rate. This setting has no effect on third-party tools that create explicit slew rate statements.

- Fast

  Select **`Fast`** to use more current and enable faster logic responses.

- Slow

  Select **`Slow`** to use less current and avoid ground bounce.

- Timing Driven

  Select **`Timing Driven`** to control the transition time based on your timing constraints.

XC9500 Advanced Tab

Use this tab, shown in the following figure, to set the following options.

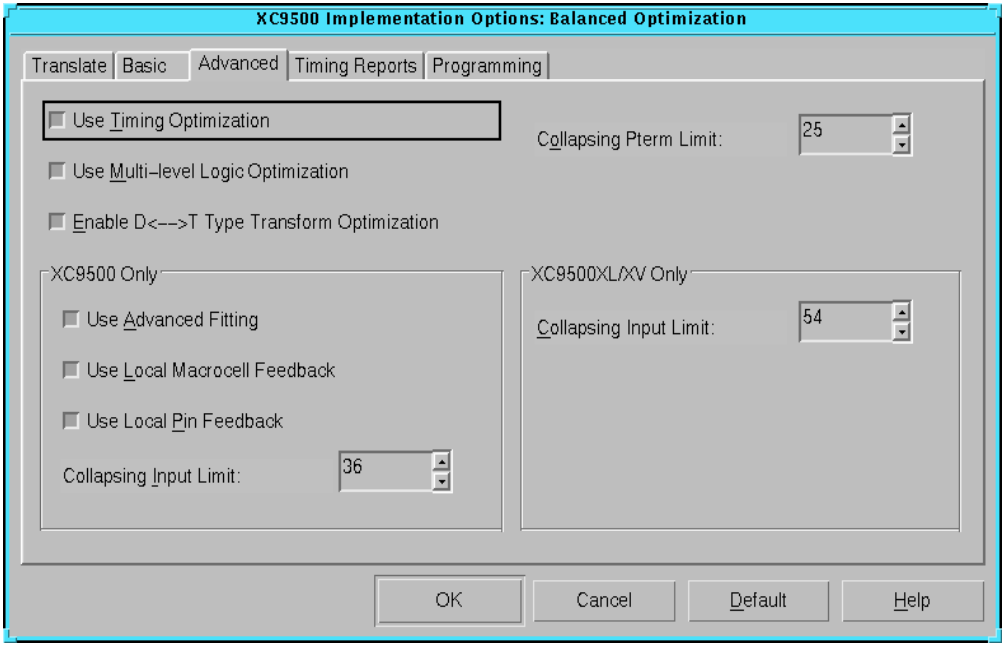


Figure 5-67 XC9500 Advanced Tab

Use Timing Optimization

Select this option to perform timing optimization. Timing optimization shortens the critical paths and allocates the fastest resources for a design, assuming that all paths are equally critical. In some cases, timing optimization will trade density for speed. By default, this option is on.

Use Multi-level Logic Optimization

This option simplifies the total number of logic expressions in a design, and then collapses the logic in order to meet user objectives such as density, speed and timing constraints. This optimization targets CPLD architecture, making it possible to collapse to the

macrocell limits, reduce levels of logic, and minimize the total number of p-terms.

Multi-level Logic Optimization optimizes combinatorial logic from your design. Combinatorial logic includes the following types of logic.

- Register-to-register logic
- Pad-to-register logic
- Register-to-pad logic
- Pad-to-pad logic

Multi-level Logic Optimization operates on combinatorial logic according to the following rules.

- If timing constraints are set, the program optimizes for speed to meet timing constraints.
- If timing constraints are not set, the program optimizes either for speed or density, depending on the user setting for the Use Timing Optimization option.
    - If Use Timing Optimization is turned on, the combinatorial logic will be mapped for speed.
    - If Use Timing Optimization is turned off, the combinatorial logic will be mapped for density. The goal of optimization will then be to reduce the total number of p-terms.
- Logic marked with the attribute **`MINIMIZE=OFF`** will not be extracted or optimized.

By default, this option is on.

Enable D <--> T Type Transform Optimization

Select this option to allow the software to convert D-type flip-flops to T-type flip-flops. This option allows the software to choose the implementation that requires the smaller amount of logic resources. By default, this option is on.

Collapsing Pterm Limit

This option controls the degree to which a design netlist is flattened. A logic gate can collapse forward into a subsequent gate only if the

number of product terms in the resulting logic function does not exceed the p-term limit. If the path delay of a logic function is not acceptable, increase the p-term limit to allow the larger functions to be further flattened. Choose a number from 2 to 90. The default p-term limit for the XC9500 device family is 25 p-terms.

XC9500 Only — Use Advanced Fitting

Select this option to enable an advanced fitting strategy that favors placing signals with common inputs in the same function block. This usually allows you to pack more logic into the same device. Disable this option if the software has trouble fitting a design that used to fit with an older version of software. By default, this option is on.

XC9500 Only — Use Local Macrocell Feedback

Select this option to enable the software to use local macrocell feedback whenever possible. The local feedback path (from a macrocell-output to an input of the same function block) takes less time than the global feedback path. Using local feedback can speed up your design but can also make it difficult to keep the same timing after a design change.

To take maximum advantage of local feedback, control the placement to group appropriate signals into the same function block. In order to fit a design, the software may require wire-ANDing in the interconnect which can prevent local feedback use. However, you can force a local feedback by applying a timing constraint and assigning the signals to the same function block. This method prevents wire-ANDing of local feedback signal and works even if you disable the Use Local Macrocell Feedback option. By default, this option is on.

Note: The XC9536 device does not have local feedback.

XC9500 Only — Use Local Pin Feedback

Select this option to enable the software to use local I/O pin feedback whenever possible. The pin feedback path takes less time than the FastCONNECT™ path. The software uses the pin feedback path instead of the FastCONNECT path for output pin signals that do not have 3-state control or Slow slew rate. By default, this option is on.

XC9500 Only and XC9500XL/XV Only — Collapsing Input Limit

This option controls the degree to which a design netlist is flattened. A logic gate can collapse forward into a subsequent gate only if the number of inputs in the resulting logic function does not exceed the input limit. If the path delay of a logic function is not acceptable, increase the input limit to allow the larger functions to be further flattened. For XC9500 devices, choose a number from 2 to 36. The default is 36. For XC9500XL and XC9500XV devices, choose a number from 2 to 54. The default is 54.

XC9500 Timing Reports Tab

Use this tab, shown in the following figure, to set the following options.

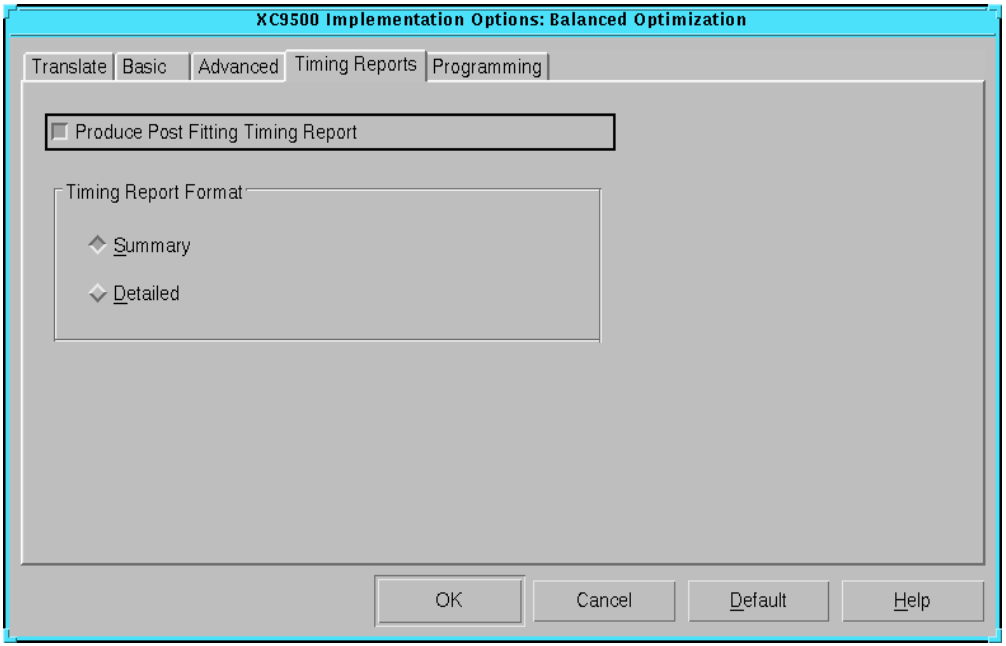


Figure 5-68 XC9500 Timing Reports Tab

Produce Post Fitting Timing Report

Select this option to produce a timing report. The timing report provides a brief analysis of the maximum clock speed for the design after it is fitted. To obtain a detailed analysis, use the Timing Analyzer tool. By default, this option is on.

Note: If you select this option, the report is automatically generated during the Fit step.

Timing Report Format

This option allows you to choose the level of detail given in your timing report. The default is Summary.

- Summary

  Select **`Summary`** to generate a report that contains summary information and design statistics.

- Detailed

  Select **`Detailed`** to generate a report that lists delay information for all nets and paths.

XC9500 Programming Tab

Use this tab, shown in the following figure, to set the following options.

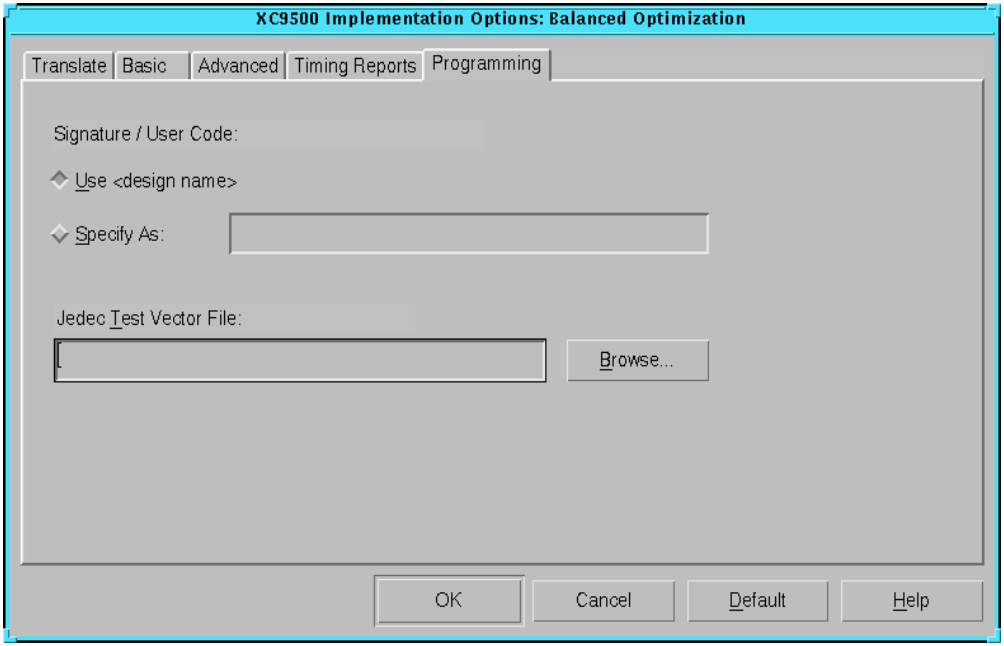


Figure 5-69 XC9500 Programming Tab

Signature/User Code

Select **Use <design name>** or enter a unique text string in the **Specify As** field to identify the configuration data. You can enter a string of up to four alphanumeric characters. The device programmer can read the signature, and the person running the device programmer can verify that the correct configuration data file is loaded. Use the JTAG Programmer to identify the configuration data signature (usercode) of a programmed XC9500 or XC9500XL device. The default is Use <design name>.

Jedec Test Vector File

Use this option to include a TMV file in your JEDEC file. The TMV file is a test vector file generated when ABEL compiles a design containing user test vectors. Click **Browse** to look for a TMV file.

XC9500 Simulation Options

Click the General, VHDL / Verilog, or EDIF tab to access the different options within the Simulation Options dialog box. Use the different tabs of this dialog box to set the options described in this section.

Click **OK** to accept the options, click **Cancel** to exit the dialog box without changing any settings, click **Default** to set the default options, or click **Help** to obtain online help.

XC9500 General Tab

Use this tab, shown in the following figure, to set the following options.

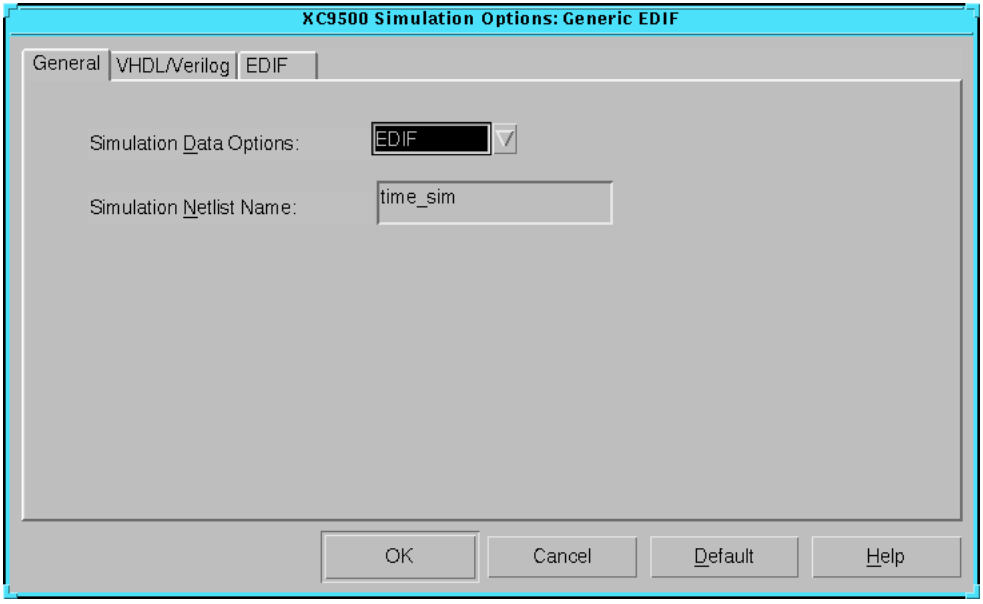


Figure 5-70 XC9500 General Tab

Simulation Data Options

Specify the netlist format to use for simulation. The following formats are available.

- EDIF
- VHDL
- Verilog

Simulation Netlist Name

Select this option to specify the name of the output file. This allows you to control the output netlist name to avoid overwriting any files. The default name is time_sim.

XC9500 VHDL/Verilog Tab

Use this tab, shown in the following figure, to set the VHDL or Verilog options.

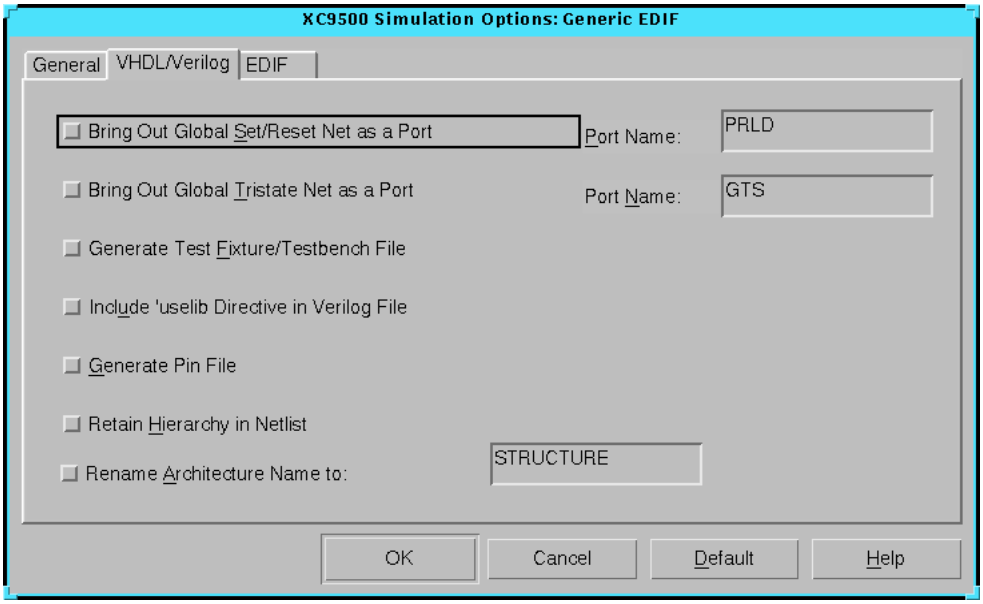


Figure 5-71 XC9500 VHDL/Verilog Tab

The XC9500 VHDL / Verilog tab is identical to the tab described in the "Spartan VHDL / Verilog Tab" section.

XC9500 EDIF Tab

Use this tab, shown in the following figure, to set the EDIF options.

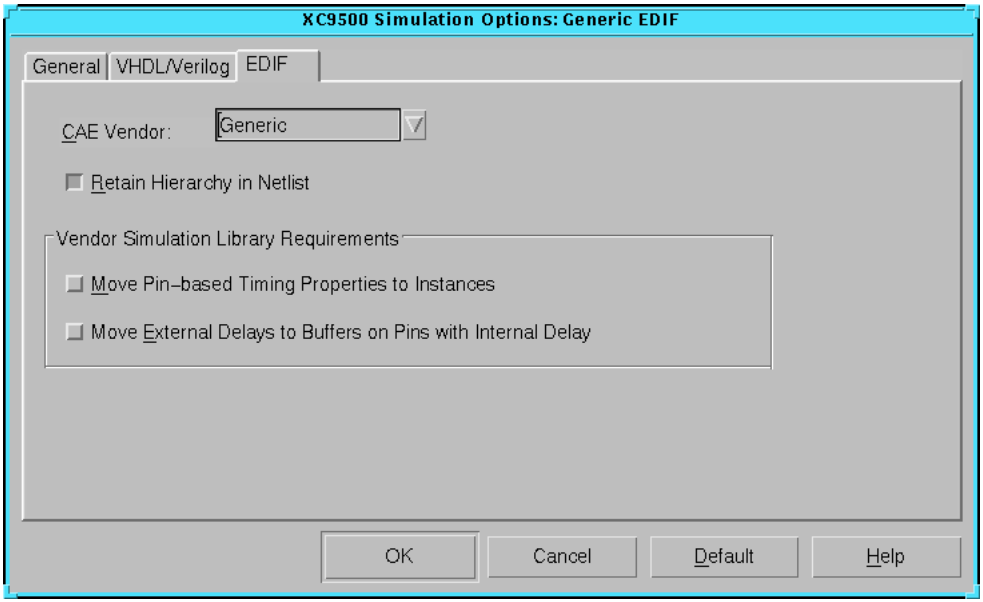


Figure 5-72 XC9500 EDIF Tab

The XC9500 EDIF tab is identical to the tab described in the “Spartan EDIF Tab” section.

Appendix A

Glossary

This appendix contains definitions and explanations for terms used in this manual.

asynchronous debugging

Asynchronous debugging is a debugging mode in which you capture data without controlling your system clock.

BIT file

BIT file is the same as a bitstream file. See bitstream.

bitstream (BIT file)

A bitstream file is a stream of data that contains location information for logic on a device, that is, the placement of Configurable Logic Blocks (CLBs), Input / Output Blocks (IOBs), TBUFs, pins, and routing elements. The bitstream also includes empty placeholders that are filled with the logical states sent by the device during a readback. Only the memory elements, such as flip-flops, RAMs, and CLB outputs, are mapped to these placeholders, because their contents are likely to change from one state to another. When downloaded to a device, a bitstream configures the logic of a device and programs the device so that the states of that device can be read back.

A bitstream file has a .bit extension.

block

A block is a group of one or more logic functions.

bottom-up design

Bottom-up design is an HDL design methodology where already defined HDL blocks are merged into one overall desired design behavior. The lowest level portion of your design is completed first. Only after the low-level building blocks are complete do you finish higher-level hierarchical blocks in your design. This methodology is typically used with schematic capture programs.

BUFT

A BUFT is a tristate buffer.

byte-wide PROM

A byte-wide PROM is a byte-wide programmable read-only memory (PROM) supplies data one byte at a time.

CCLK pin

The CCLK pin is the XChecker pin that provides the configuration clock for the device or daisy chain of devices during a download.

CLKI pin

The CLKI pin is the clock input pin to XChecker. CLKI provides an external clock to the Hardware Debugger so that in conjunction with the CLKO pin, the Debugger can control the application of the external clock to the device being debugged.

CLKO pin

The CLKO pin is the XChecker clock output pin. CLKO supplies the Hardware Debugger controlled clock to the device being debugged. The source of CLKO is one of the following: CLKI, logic 1, logic 0, or the internal XChecker clock.

clock input path

A clock input path starts at either an input of the chip or at the output of a flip-flop, latch, or RAM, and ends at any clock pin on a flip-flip or latch enable. The clock input path time is the maximum time required

for the signal to arrive at the flip-flop clock input. Clock input paths help to determine system-level design timing.

clock skew

Clock skew is the difference between the time a clock signal arrives at the source flip-flop in a path and the time it arrives at the destination flip-flop. It is also referred to as clock delay.

critical path

A critical path is a signal in a section of combinatorial logic that limits the speed of the logic. Storage elements begin and end a critical path, which may include I/O pads.

daisy chain

A daisy chain is a series of bitstream files concatenated in one file. It can be used to program several FPGAs connected in a daisy chain board configuration.

debugging

Debugging is the process of reading back or probing the states of a configured device to ensure that the device is behaving as expected while in circuit.

DIN pin

In an FPGA, the DIN pin loads a bitstream in serial mode. On the XChecker cable, it provides the bitstream data and connects to the DIN pin of the target FPGA.

DONE pin (Spartan/XC4000/XC5200)

The DONE pin is a dual function pin. As an input, it can be configured to delay the global logic initialization or the enabling of outputs. As an output, it indicates the completion of the configuration process.

Note: For Virtex devices, this pin is called DONE_CFG.

downloading

Downloading is the process of configuring or programming a device by sending bitstream data to the device.

D/P pin (XC3000)

The D/P pin is dual-function pin. As an input, it initiates a reconfiguration of a configured device. As an output, it signals the end of configuration.

EDIF

EDIF is an acronym for Electronic Data Interchange Format, an industry standard file format for specifying a design netlist. It is generated by a third-party design-entry tool.

EXORmacs (Motorola)

This is a PROM format supported by the Xilinx tools. Its maximum address is 16 777 216. This format supports PROM files of up to (8 x 16 777 216) = 134 217 728 bits.

external clock

The external clock is the system clock that XChecker uses from the target board during synchronous mode debugging. To use an external clock, connect the system clock to the XChecker cable using the CLKI pin and the XChecker clock to the FPGA device using the CLKO pin.

fitting

Fitting is the process of putting logic from your design into physical macrocell locations in the CPLD. Routing is performed automatically, and because of the UIM architecture, all designs are routable.

GND pin

A GND pin is Ground (0 volts).

group

A group is a collection of common signals to form a bus. In the case of a counter, for example, the different signals that produce the actual counter values can be combined to form an alias, or group.

guide file

A guide file is a previously placed and routed FPGA or fitted CPLD file that can be used in a subsequent place and route or fitting operation.

HDL

HDL is an acronym for Hardware Description Language. The most common HDLs in use today are Verilog and VHDL. They describe designs in a technology-independent manner using a high level of abstraction.

HEX

HEX refers to a simple text dump of the PROM data in HEX format. It has unlimited data capacity.

hold time

Hold time is the time following a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct.

INIT pin

The INIT pin is a device pin indicating when a device is ready to receive configuration data after power-up.

instance

An instance is one specific gate or hierarchical element in a design or netlist. The term “symbol” often describes instances in a schematic drawing. Instances are interconnected by pins and nets. Pins are ports through which connections are made from an instance to a net. A

design that is flattened to the lowest level constituents is described using primitive instances.

internal XChecker clock

The internal XChecker clock is internal to XChecker and can be applied by the XChecker CLKO pin to a device being debugged.

IOB (input/output block)

An IOB is a collection or grouping of basic elements that implement the input and output functions of an FPGA device.

.ll file

The .ll file is the logic allocation file, which indicates the bitstream position of storage elements such as latches, flip-flops, and IOB inputs and outputs. The Hardware Debugger uses this file to locate signal values inside a readback bitstream.

loading direction

Loading direction is the direction of the addresses in which data is stored on your PROM. In the Up direction, the data is stored in ascending order. In the Down direction, the data is stored in descending order.

logic icon

A logic icon is a graphical representation of a logic resource, such as a flip-flop, buffer, or register.

logic synthesis

Logic synthesis is a process that starts from a high level of logic abstraction (typically Verilog or VHDL) and automatically creates a lower level of logic abstraction using a library containing primitives.

mapping

Mapping is the process of assigning a design's logic elements to the specific physical elements that actually implement logic functions in a device.

MCS-86 (Intel)

MCS-86 is a PROM format supported by the Xilinx tools. Its maximum address is 1 048 576. This format supports PROM files of up to (8 x 1 048 576) = 8 388 608 bits.

net

A net is a logical connection between two or more symbol instance pins. After routing, the abstract concept of a net is transformed to a physical connection called a wire.

number of clock cycles

The number of clock cycles is the number of clocks that occur between snapshots during synchronous mode debugging. When capturing multiple snapshots, the number of snapshots is used as a trigger for capturing each snapshot.

one-to-one logic

In the context of Xilinx FPGA devices, one-to-one logic is the exact correspondence between the logic specified in the design entry phase and the logic implemented in the device. For example, if you draw three inverters in your design, there are three corresponding inverters in the programmed device. This correspondence makes back-annotation of timing delays very straightforward and ensures that there are no differences between your original design and the finished device.

optimization

Optimization is the process that decreases the area or increases the speed of a design.

pad

A pad is the physical bonding pad on an integrated circuit. All signals on a chip must enter and leave by way of a pad. Pads are connected to package pins in order for signals to enter or leave an integrated circuit package.

pin

A pin can be a symbol pin or package pin. A package pin is a physical connector on an integrated circuit package that carries signals into and out of an integrated circuit. A symbol pin, also referred to as an instance pin, is the connection point of an instance to a net.

place effort

Place effort is a user-controlled parameter that balances run-time with placement efficiency for the Flow Engine.

placer

The placer is a utility that maps logic from your design into specific locations in the target FPGA chip.

placing

Placing is the process of assigning physical device cell locations to the logic in a design.

primitive

A primitive is a logic element that directly corresponds, or maps, to a basic silicon component.

probing

Probing is the process of examining the states of an FPGA device.

$\overline{\text{PROG}}$ pin

A $\overline{\text{PROG}}$ pin is an XChecker pin that provides a reprogram pulse to XC4000, XC5200, and Virtex devices when connected to the $\overline{\text{PROG}}$ pin of the device.

programming

Programming is the process of configuring the programmable interconnect in the FPGA.

PROM

PROM is an acronym for programmable read-only memory.

PROM file

A PROM file consists of one or more BIT files (bitstreams) formed into one or more datastreams. The file is formatted in one of four industry-standard formats: Intel MCS-86, Tektronics TEKHEX, Motorola EXORmacs, or HEX. The PROM file includes headers that specify the length of the bitstreams, as well as all the framing and control information necessary to configure the FPGAs. It can be used to program one or more devices.

RBT file

An RBT file is a raw BIT format file; the ASCII version of the BIT file.

RD pin

The RD pin is the XChecker readback data pin.

readback

Readback is the process of reading the logic downloaded to an FPGA device. There are two types of readbacks.

- A readback with a filter that extracts the configuration bits to verify that a design was downloaded in its entirety.

- A readback with a filter that extracts the state of design storage elements, CLB outputs, and IOB outputs to ensure that the device is behaving as expected.

route effort

Route effort is the user-controlled parameter that balances run-time with routing efficiency for the Flow Engine.

router

The router connects all appropriate pins to create the design's nets.

routing

Routing is the process of assigning logical nets to physical wire segments in the FPGA that interconnect logic cells.

RPM

A Relationally Placed Macro (RPM) defines the spatial relationship of the primitives that constitute its logic. An indivisible block of logic elements that are placed as a unit into a design.

RST pin

An RST pin is an XChecker pin that can be driven Low after configuration to reset the target FPGA internal latches and flip-flops.

RT pin

The RT pin is the XChecker readback trigger pin.

schematic

A schematic is a hierarchical drawing representing a design in terms of user and library components.

script

A script is a series of commands that automatically execute a complex operation such as the steps in a design flow.

SDF

Standard Delay Format (SDF) is an industry-standard file format for specifying timing information. It is usually used for simulation.

serial PROM

A serial PROM is a PROM that is read one bit at a time.

setup time

Setup time is the time prior to a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct.

snapshot

A snapshot is the readback data that contains the values of all storage elements, CLB outputs, and IOB inputs and outputs of a design at a point in time.

state

A state is a set of values stored in the memory elements of a device (flip-flops, latches, RAMs, CLB outputs, and IOBs) that represent the state of that device for a particular readback. To each state there corresponds a specific set of logical values.

static timing analysis

Static timing analysis is a point-to-point delay analysis of a design network.

status bar

The status bar is an area located at the bottom of a window that provides information about the commands that you are about to select or that are being processed.

synchronous debugging

Synchronous debugging is a debugging mode in which you use the XChecker cable to have full control of the clock.

synthesis

See logic synthesis.

TCK pin

A TCK pin is an XChecker pin. This output supplies clocks for a boundary scan port on an XC9500 device. The JTAG software must be used to drive the boundary scan port on the XChecker cable.

TDI pin

A TDI pin is an XChecker pin. This input receives data from the boundary scan chain. The JTAG software must be used to drive the boundary scan port on the XChecker cable.

TEKHEX (Tektronix)

TEKHEX is a PROM format supported by Xilinx. Its maximum address is 65 536. This format supports PROM files of up to (8 x 65 536) = 524 288 bits.

timing

Timing is the process that calculates the delays associated with each of the routed nets in the design.

timing constraints

Timing constraints are user specifications of the maximum allowable delay on any given set of paths in a design. Timing constraints can be entered on a schematic or in a user constraints file (UCF).

TMS pin

A TMS pin is an XChecker pin. This output drives the mode of the boundary scan state machine. The JTAG software must be used to drive the boundary scan port on the XChecker cable.

toolbar

The toolbar is a field located under the menu bar at the top of a window. It contains a series of buttons that you click to execute some of the most commonly used commands. These buttons are an alternative to the menu commands.

toolbox

The toolbox is a field located in the Design Manager main window. It contains a series of buttons that you click to invoke tools such as the Flow Engine, Timing Analyzer, Floorplanner, Hardware Debugger, PROM File Formatter, FPGA Editor, Chip Viewer, and JTAG Programmer.

top-down design

Top-down design starts a design with the highest level of abstraction and gradually designs underlying blocks until the complete design is implemented in the target technology. Top-down design is often technology-independent at the highest levels of design abstraction.

TRIG pin

A TRIG pin is an XChecker external trigger pin that causes the Hardware Debugger to initiate a readback of the device being debugged.

trigger

A trigger is an external signal that tells the Hardware Debugger to start the readback operation. It applies the clock to the bitstream.

TTY

TTY is a textual command line interface.

universal interconnect matrix (UIM)

The UIM is the routing matrix for CPLD devices. This fully populated switching matrix allows any output to be routed to any input, guaranteeing 100% routability of all designs. The UIM can also function as a very wide AND gate, which can allow more logic to be placed in macrocells.

VCC pin

The VCC pin is Power (5 volts). It is the supply voltage.

verification

Verification is the process of reading back the configuration data of a device and comparing it to the original design to ensure that all of the design was correctly received by the device.

Verilog

Verilog is a commonly used Hardware Description Language (HDL) that can be used to model a digital system at many levels of abstraction ranging from the algorithmic level to the gate level. It is IEEE standard 1364-1995. Verilog was originally developed by Cadence Design Systems and is now maintained by OVI.

A Verilog file has a .v extension.

VHDL

VHDL is an acronym for VHSIC Hardware Description Language (VHSIC an acronym for Very High-Speed Integrated Circuits). It can be used to describe the concurrent and sequential behavior of a digital system at many levels of abstraction ranging from the algorithmic level to the gate level. VHDL is IEEE standard 1076-1993.

A VHDL file has a .vhd or .vhdl extension.

waveform

A waveform is a graphical representation of a set of simulation transitions that depicts the digital or electrical values of a node on the schematic.

WIR file

Viewlogic netlist files built by ViewDraw, PROcapture, or ViewSynthesis.

A WIR file is an intermediate design file generated by the Viewlogic design tools.

workspace

In the PROM File Formatter, the workspace is a frame and an empty datastream. When you add files into the datastream, the horizontal arrows indicate the concatenation of files.

Appendix B

Legacy Information

This appendix provides information for Design Manager and Flow Engine legacy users. It describes changes that have occurred to the following in this release.

- “Implementation Revisions”
- “Place and Route Effort Level”
- “Option Location”
- “Clipboard Data”

Implementation Revisions

In this release, option data is stored at the revision level. Implementation revisions from the previous release do not have option data stored at the revision level. If you attempt to open an implementation revision from the previous release with the Design Manger in this release, the Design Manager copies the option information from the project area to each revision.

To keep your old revision intact, make a copy of your entire project tree, or do not attempt to open it with the Design Manger in this release.

Place and Route Effort Level

To enhance ease of use, the Place & Route Effort Level setting has moved from the Place and Route tab of the Implementation Options dialog box to the Options dialog box. When you open a project from the previous release with the new software, the Place & Route Effort Level setting from the Implementation Options dialog box is not retained. Instead, the software uses the default value of 2 from the Place & Route Effort Level setting in the Options dialog box.

Option Location

Some of the options from the previous release have been moved to enhance ease of use. The following table shows these options with their old and new locations.

Table B-1 Option Locations

Option	Previous Release	This Release
Part Select	Implement Dialog Box	New Version Dialog Box New Revision Dialog Box Set Part Dialog Box
Copy Guide Data to Project Clipboard	Implement Dialog Box	N / A[a]
Copy Floorplan Data to Project Clipboard	Implement Dialog Box	N / A[a]
Overwrite Last Version	Implement Dialog Box	Preferences Dialog Box
Overwrite Last Revision	Implement Dialog Box	Automatic
New Version Name	Implement Dialog Box	New Version Dialog Box
New Revision Name	Implement Dialog Box	New Version Dialog Box New Revision Dialog Box Set Part Dialog Box
User Constraints	Options Dialog Box	New Version Dialog Box New Revision Dialog Box Set Part Dialog Box Set Constraints Dialog Box

a. See the following section for more information.

Clipboard Data

In this release, the project clipboard is no longer used. If you want to use the clipboard data from an old implementation revision, copy the old revision data to the new revision as follows.

- If you have not yet created your new revision, adjust settings in the Copy Persistent Data field of the New Version, New Revision, or Set Part dialog box

- If you have already created your new revision, adjust settings in the Set Floorplan File(s) or Set Guide File(s) dialog box