

Features

- Complete line of four related Field Programmable Gate Array product families
 - XC3000A, XC3000L, XC3100A, XC3100L
- Ideal for a wide range of custom VLSI design tasks
 - Replaces TTL, MSI, and other PLD logic
 - Integrates complete sub-systems into a single package
 - Avoids the NRE, time delay, and risk of conventional masked gate arrays
- High-performance CMOS static memory technology
 - Guaranteed toggle rates of 70 to 370 MHz, logic delays from 9 to 1.5 ns
 - System clock speeds over 80 MHz
 - Low quiescent and active power consumption
- Flexible FPGA architecture
 - Compatible arrays ranging from 1,000 to 7,500 gate complexity
 - Extensive register, combinatorial, and I/O capabilities
 - High fan-out signal distribution, low-skew clock nets
 - Internal 3-state bus capabilities
 - TTL or CMOS input thresholds
 - On-chip crystal oscillator amplifier
- Unlimited reprogrammability
 - Easy design iteration
 - In-system logic changes
- Extensive packaging options
 - Over 20 different packages
 - Plastic and ceramic surface-mount and pin-grid-array packages
 - Thin and Very Thin Quad Flat Pack (TQFP and VQFP) options
- Ready for volume production
 - Standard, off-the-shelf product availability
 - 100% factory pre-tested devices
 - Excellent reliability record

- Complete XACTstep Development System
 - Schematic capture, automatic place and route
 - Logic and timing simulation
 - Interactive design editor for design optimization
 - Timing calculator
 - Interfaces to popular design environments like Viewlogic, Cadence, Mentor Graphics, and others

Description

XC3000-Series Field Programmable Gate Arrays (FPGAs) provide a group of high-performance, high-density, digital integrated circuits. Their regular, extendable, flexible, user-programmable array architecture is composed of a configuration program store plus three types of configurable elements: a perimeter of I/O Blocks (IOBs), a core array of Configurable Logic Blocks (CLBs) and resources for interconnection. The general structure of an FPGA is shown in **Figure 2**. The XACTstep development system provides schematic capture and auto place-and-route for design entry. Logic and timing simulation, and in-circuit emulation are available as design verification alternatives. The design editor is used for interactive design optimization, and to compile the data pattern that represents the configuration program.

The FPGA user logic functions and interconnections are determined by the configuration program data stored in internal static memory cells. The program can be loaded in any of several modes to accommodate various system requirements. The program data resides externally in an EEPROM, EPROM or ROM on the application circuit board, or on a floppy disk or hard disk. On-chip initialization logic provides for optional automatic loading of program data at power-up. The companion XC17XX Serial Configuration PROMs provide a very simple serial configuration program storage in a one-time programmable package.

The XC3000 Field Programmable Gate Array families provide a variety of logic capacities, package styles, temperature ranges and speed grades.

Device	Max Logic Gates	Typical Gate Range	CLBs	Array	User I/Os Max	Flip-Flops	Horizontal Longlines	Configuration Data Bits
XC3020A, 3020L, 3120A	1,500	1,000 - 1,500	64	8 x 8	64	256	16	14,779
XC3030A, 3030L, 3130A	2,000	1,500 - 2,000	100	10 x 10	80	360	20	22,176
XC3042A, 3042L, 3142A, 3142L	3,000	2,000 - 3,000	144	12 x 12	96	480	24	30,784
XC3064A, 3064L, 3164A	4,500	3,500 - 4,500	224	16 x 14	120	688	32	46,064
XC3090A, 3090L, 3190A, 3190L	6,000	5,000 - 6,000	320	16 x 20	144	928	40	64,160
XC3195A	7,500	6,500 - 7,500	484	22 x 22	176	1,320	44	94,984

XC3000 Series Overview

Introduced in 1987/88, the XC3000 series is the industry's most successful family of FPGAs, with over 10 million devices shipped. In 1992/93, Xilinx introduced three additional families, offering more speed, functionality, and a new supply-voltage option.

There are now four distinct family groupings within the XC3000 Series of FPGA devices, with emphasis on those listed below:

- XC3000A Family
- XC3000L Family
- XC3100A Family
- XC3100L Family

All six families share a common architecture, development software, design and programming methodology, and also common package pin-outs. An extensive Product Description covers these common aspects.

The much shorter individual Product Specifications then provide detailed parametric information for the XC3000A, XC3000L, XC3100A, and XC3100L product families. (The XC3000 and XC3100 families are not recommended for new designs, and their individual product specifications are not included in this book.)

Here is a simple overview of those XC3000 products currently emphasized:

- **XC3000A Family** — The XC3000A is an enhanced version of the basic XC3000 family, featuring additional interconnect resources and other user-friendly enhancements. The ease-of-use of the XC3000A family makes it the obvious choice for all new designs that do not require the speed of the XC3100A or the 3-V operation of the XC3000L.
- **XC3000L Family** — The XC3000L is identical in architecture and features to the XC3000A family, but operates at a nominal supply voltage of 3.3 V. The XC3000L is the right solution for battery-operated and low-power applications.
- **XC3100A Family** — The XC3100A is a performance-optimized relative of the XC3000A family. While both families are bitstream and footprint compatible, the

XC3100A family extends toggle rates to 370 MHz and in-system performance to over 80 MHz. The XC3100A family also offers one additional array size, the XC3195A. The XC3100A is best suited for designs that require the highest clock speed or the shortest net delays.

- **XC3100L Family** — The XC3100L is identical in architectures and features to the XC3100A family, but operates at a nominal supply voltage of 3.3V.

Figure 1 illustrates the relationships between the families. Compared to the original XC3000 family, XC3000A offers additional functionality and, coming soon, increased speed. The XC3000L family offers the same additional functionality, but reduced speed due to its lower supply voltage of 3.3 V. The XC3100A family offers substantially higher speed and higher density with the XC3195A.

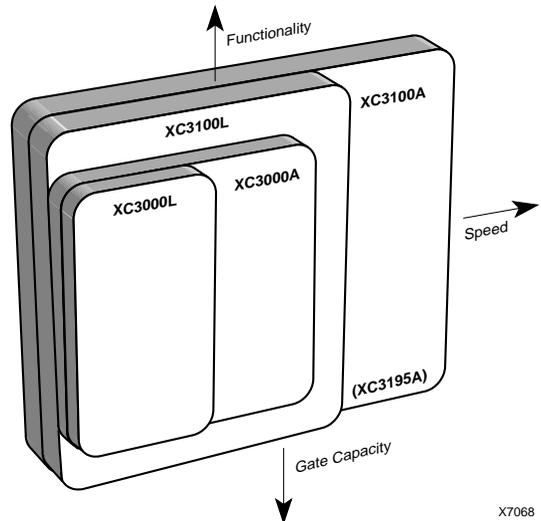


Figure 1: XC3000 FPGA Families

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Detailed Functional Description

The perimeter of configurable Input/Output Blocks (IOBs) provides a programmable interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks, carrying logic signals among blocks, analogous to printed circuit board traces connecting MSI/SSI packages.

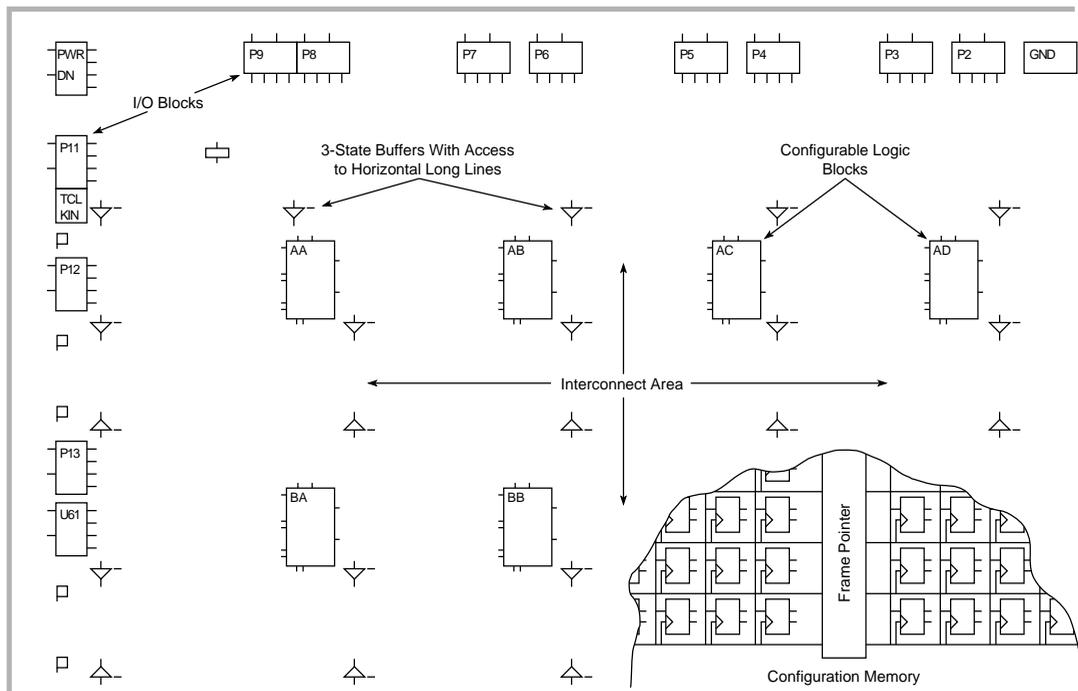
The block logic functions are implemented by programmed look-up tables. Functional options are implemented by program-controlled multiplexers. Interconnecting networks between blocks are implemented with metal segments joined by program-controlled pass transistors.

These FPGA functions are established by a configuration program which is loaded into an internal, distributed array of configuration memory cells. The configuration program is loaded into the device at power-up and may be reloaded on command. The FPGA includes logic and control signals to implement automatic or passive configuration. Program data may be either bit serial or byte parallel. The XACT^{step} development system generates the configuration program

bitstream used to configure the device. The memory loading process is independent of the user logic functions.

Configuration Memory

The static memory cell used for the configuration memory in the Field Programmable Gate Array has been designed specifically for high reliability and noise immunity. Integrity of the device configuration memory based on this design is assured even under adverse conditions. As shown in **Figure 3**, the basic memory cell consists of two CMOS inverters plus a pass transistor used for writing and reading cell data. The cell is only written during configuration and only read during readback. During normal operation, the cell provides continuous control and the pass transistor is off and does not affect cell stability. This is quite different from the operation of conventional memory devices, in which the cells are frequently read and rewritten.



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Figure 2: Field Programmable Gate Array Structure.

It consists of a perimeter of programmable I/O blocks, a core of configurable logic blocks and their interconnect resources. These are all controlled by the distributed array of configuration program memory cells.

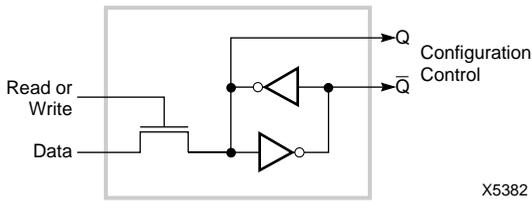


Figure 3: Static Configuration Memory Cell.
It is loaded with one bit of configuration program and controls one program selection in the Field Programmable Gate Array.

The memory cell outputs Q and \bar{Q} use ground and V_{CC} levels and provide continuous, direct control. The additional capacitive load together with the absence of address decoding and sense amplifiers provide high stability to the cell. Due to the structure of the configuration memory cells, they are not affected by extreme power-supply excursions or very high levels of alpha particle radiation. In reliability

testing, no soft errors have been observed even in the presence of very high doses of alpha radiation.

The method of loading the configuration data is selectable. Two methods use serial data, while three use byte-wide data. The internal configuration logic utilizes framing information, embedded in the program data by the XACTstep development system, to direct memory-cell loading. The serial-data framing and length-count preamble provide programming compatibility for mixes of various FPGA device configurations in a synchronous, serial, daisy-chain fashion.

I/O Block

Each user-configurable IOB shown in Figure 4, provides an interface between the external package pin of the device and the internal user logic. Each IOB includes both registered and direct input paths. Each IOB provides a programmable 3-state output buffer, which may be driven by a registered or direct output signal. Configuration options allow each IOB an inversion, a controlled slew rate and a high impedance pull-up. Each input circuit also provides input clamping diodes to provide electrostatic protection, and circuits to inhibit latch-up produced by input currents.

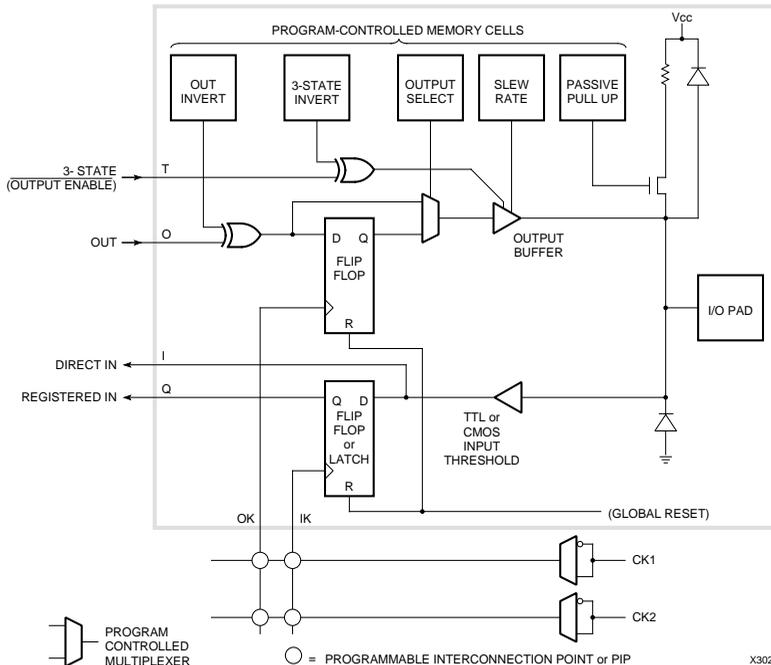


Figure 4: Input/Output Block.
Each IOB includes input and output storage elements and I/O options selected by configuration memory cells. A choice of two clocks is available on each die edge. The polarity of each clock line (not each flip-flop or latch) is programmable. A clock line that triggers the flip-flop on the rising edge is an active Low Latch Enable (Latch transparent) signal and vice versa. Passive pull-up can only be enabled on inputs, not on outputs. All user inputs are programmed for TTL or CMOS thresholds.

The input-buffer portion of each IOB provides threshold detection to translate external signals applied to the package pin to internal logic levels. The global input-buffer threshold of the IOBs can be programmed to be compatible with either TTL or CMOS levels. The buffered input signal drives the data input of a storage element, which may be configured as either a flip-flop or a latch. The clocking polarity (rising/falling edge-triggered flip-flop, High/Low transparent latch) is programmable for each of the two clock lines on each of the four die edges. Note that a clock line driving a *rising* edge-triggered flip-flop makes any latch driven by the same line on the same edge Low-level transparent and vice versa (*falling* edge, *High* transparent). All Xilinx primitives in the supported schematic-entry packages, however, are positive edge-triggered flip-flops or High transparent latches. When one clock line must drive flip-flops as well as latches, it is necessary to compensate for the difference in clocking polarities with an additional inverter either in the flip-flop clock input or the latch-enable input. I/O storage elements are reset during configuration or by the active-Low chip RESET input. Both direct input (from IOB pin I) and registered input (from IOB pin Q) signals are available for interconnect.

For reliable operation, inputs should have transition times of less than 100 ns and should not be left floating. Floating CMOS input-pin circuits might be at threshold and produce oscillations. This can produce additional power dissipation and system noise. A typical hysteresis of about 300 mV reduces sensitivity to input noise. Each user IOB includes a programmable high-impedance pull-up resistor, which may be selected by the program to provide a constant High for otherwise undriven package pins. Although the Field Programmable Gate Array provides circuitry to provide input protection for electrostatic discharge, normal CMOS handling precautions should be observed.

Flip-flop loop delays for the IOB and logic-block flip-flops are short, providing good performance under asynchronous clock and data conditions. Short loop delays minimize the probability of a metastable condition that can result from assertion of the clock during data transitions. Because of the short-loop-delay characteristic in the Field Programmable Gate Array, the IOB flip-flops can be used to synchronize external signals applied to the device. Once synchronized in the IOB, the signals can be used internally without further consideration of their clock relative timing, except as it applies to the internal logic and routing-path delays.

IOB output buffers provide CMOS-compatible 4-mA source-or-sink drive for high fan-out CMOS or TTL- com-

patible signal levels (8 mA in the XC3100A family). The network driving IOB pin O becomes the registered or direct data source for the output buffer. The 3-state control signal (IOB) pin T can control output activity. An open-drain output may be obtained by using the same signal for driving the output and 3-state signal nets so that the buffer output is enabled only for a Low.

Configuration program bits for each IOB control features such as optional output register, logic signal inversion, and 3-state and slew-rate control of the output.

The program-controlled memory cells of [Figure 4](#) control the following options.

- Logic inversion of the output is controlled by one configuration program bit per IOB.
- Logic 3-state control of each IOB output buffer is determined by the states of configuration program bits that turn the buffer on, or off, or select the output buffer 3-state control interconnection (IOB pin T). When this IOB output control signal is High, a logic one, the buffer is disabled and the package pin is high impedance. When this IOB output control signal is Low, a logic zero, the buffer is enabled and the package pin is active. Inversion of the buffer 3-state control-logic sense (output enable) is controlled by an additional configuration program bit.
- Direct or registered output is selectable for each IOB. The register uses a positive-edge, clocked flip-flop. The clock source may be supplied (IOB pin OK) by either of two metal lines available along each die edge. Each of these lines is driven by an invertible buffer.
- Increased output transition speed can be selected to improve critical timing. Slower transitions reduce capacitive-load peak currents of non-critical outputs and minimize system noise.
- An internal high-impedance pull-up resistor (active by default) prevents unconnected inputs from floating.

Summary of I/O Options

- Inputs
 - Direct
 - Flip-flop/latch
 - CMOS/TTL threshold (chip inputs)
 - Pull-up resistor/open circuit
- Outputs
 - Direct/registered
 - Inverted/not
 - 3-state/on/off
 - Full speed/slew limited
 - 3-state/output enable (inverse)

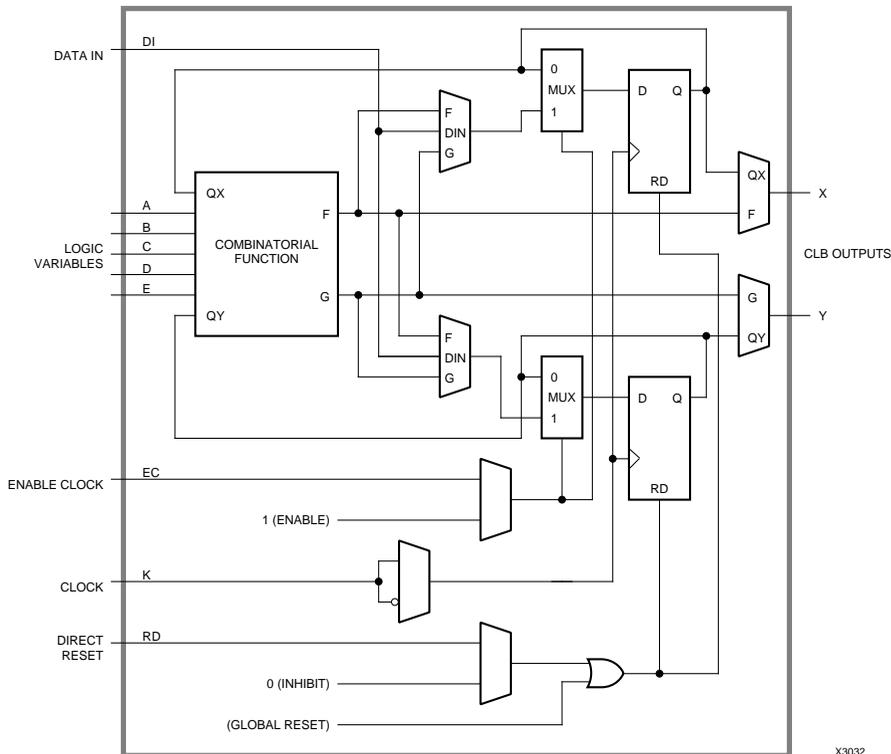
Configurable Logic Block

The array of CLBs provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. For example, the XC3020A has 64 such blocks arranged in 8 rows and 8 columns. The XACT^{step} development system is used to compile the configuration data which is to be loaded into the internal configuration memory to define the operation and interconnection of each block. User definition of CLBs and their interconnecting networks may be done by automatic translation from a schematic-capture logic diagram or optionally by installing library or user macros.

Each CLB has a combinatorial logic section, two flip-flops, and an internal control section. See Figure 5. There are: five logic inputs (A, B, C, D and E); a common clock input (K); an asynchronous direct RESET input (RD); and an enable clock (EC). All may be driven from the interconnect

resources adjacent to the blocks. Each CLB also has two outputs (X and Y) which may drive interconnect networks.

Data input for either flip-flop within a CLB is supplied from the function F or G outputs of the combinatorial logic, or the block input, DI. Both flip-flops in each CLB share the asynchronous RD which, when enabled and High, is dominant over clocked inputs. All flip-flops are reset by the active-Low chip input, RESET, or during the configuration process. The flip-flops share the enable clock (EC) which, when Low, recirculates the flip-flops' present states and inhibits response to the data-in or combinatorial function inputs on a CLB. The user may enable these control inputs and select their sources. The user may also select the clock net input (K), as well as its active sense within each CLB. This programmable inversion eliminates the need to route both phases of a clock signal throughout the device. Flexible routing allows use of common or individual CLB clocking.



X3032

Figure 5: Configurable Logic Block.

Each CLB includes a combinatorial logic section, two flip-flops and a program memory controlled multiplexer selection of function. It has the following:

- five logic variable inputs A, B, C, D, and E
- a direct data in DI
- an enable clock EC
- a clock (invertible) K
- an asynchronous direct RESET RD
- two outputs X and Y

The combinatorial-logic portion of the CLB uses a 32 by 1 look-up table to implement Boolean functions. Variables selected from the five logic inputs and two internal block flip-flops are used as table address inputs. The combinatorial propagation delay through the network is independent of the logic function generated and is spike free for single input variable changes. This technique can generate two independent logic functions of up to four variables each as shown in Figure 6a, or a single function of five variables as shown in Figure 6b, or some functions of seven variables as shown in Figure 6c. Figure 7 shows a modulo-8 binary counter with parallel enable. It uses one CLB of each type. The partial functions of six or seven variables are implemented using the input variable (E) to dynamically select between two functions of four different variables. For the two functions of four variables each, the independent results (F and G) may be used as data inputs to either flip-flop or either logic block output. For the single function of five variables and merged functions of six or seven variables, the F and G outputs are identical. Symmetry of the F and G functions and the flip-flops allows the interchange of CLB outputs to optimize routing efficiencies of the networks interconnecting the CLBs and IOBs.

Programmable Interconnect

Programmable-interconnection resources in the Field Programmable Gate Array provide routing paths to connect inputs and outputs of the IOBs and CLBs into logic networks. Interconnections between blocks are composed of a two-layer grid of metal segments. Specially designed pass transistors, each controlled by a configuration bit, form programmable interconnect points (PIPs) and switching matrices used to implement the necessary connections between selected metal segments and block pins. Figure 8 is an example of a routed net. The XACTstep development system provides automatic routing of these interconnections. Interactive routing (Editnet) is also available for design optimization. The inputs of the CLBs or IOBs are multiplexers which can be programmed to select an input network from the adjacent interconnect segments. **Since the switch connections to block inputs are unidirectional, as are block outputs, they are usable only for block input connection and not for routing.** Figure 9 illustrates routing access to logic block input variables, control inputs and block outputs. Three types of metal resources are provided to accommodate various network interconnect requirements.

- General Purpose Interconnect
- Direct Connection
- Longlines (multiplexed busses and wide AND gates)

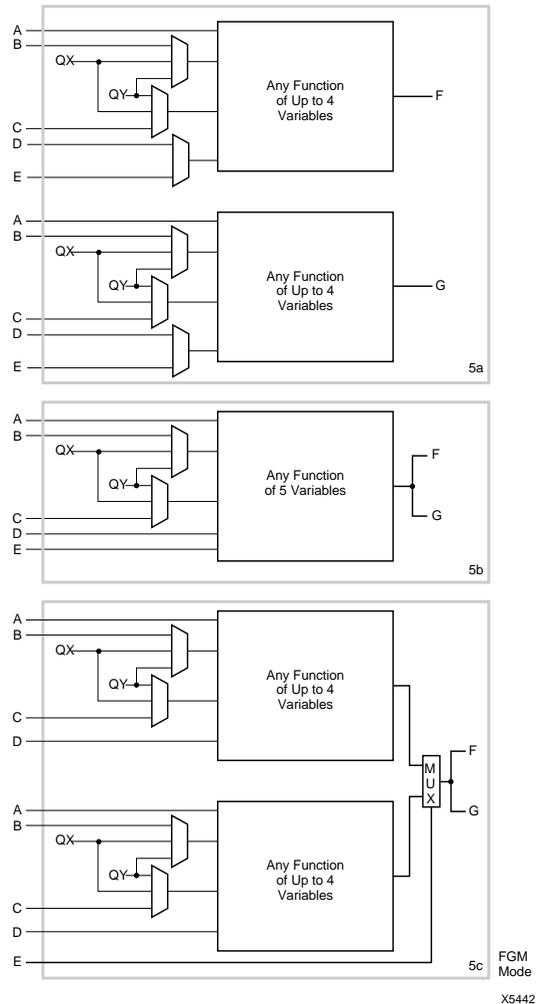


Figure 6: Combinational Logic Options

6a. Combinatorial Logic Option FG generates two functions of four variables each. One variable, A, must be common to both functions. The second and third variable can be any choice of B, C, QX and QY. The fourth variable can be any choice of D or E.

6b. Combinatorial Logic Option F generates any function of five variables: A, D, E and two choices out of B, C, QX, QY.

6c. Combinatorial Logic Option FGM allows variable E to select between two functions of four variables: Both have common inputs A and D and any choice out of B, C, QX and QY for the remaining two variables. Option 3 can then implement some functions of six or seven variables.

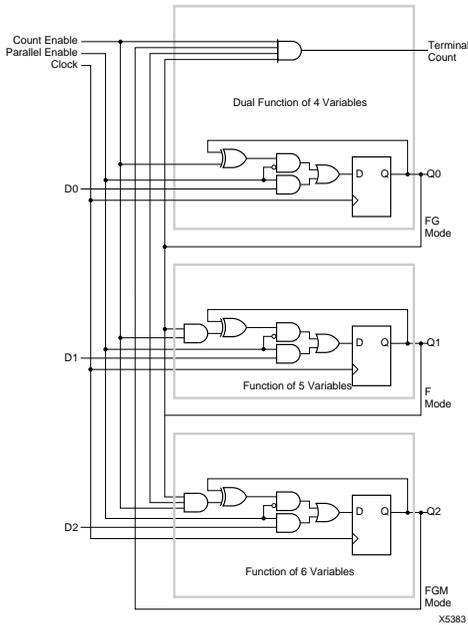


Figure 7: C8BCP Macro.

The C8BCP macro (modulo-8 binary counter with parallel enable and clock enable) uses one combinatorial logic block of each option.

General Purpose Interconnect

General purpose interconnect, as shown in Figure 10, consists of a grid of five horizontal and five vertical metal segments located between the rows and columns of logic and IOBs. Each segment is the height or width of a logic block. Switching matrices join the ends of these segments and allow programmed interconnections between the metal grid segments of adjoining rows and columns. The switches of an unprogrammed device are all non-conducting. The connections through the switch matrix may be established by the automatic routing or by using Editnet to select the desired pairs of matrix pins to be connected or disconnected. The legitimate switching matrix combinations for each pin are indicated in Figure 11 and may be highlighted by the use of the Show-Matrix command in the XACT Design Editor.

Special buffers within the general interconnect areas provide periodic signal isolation and restoration for improved performance of lengthy nets. The interconnect buffers are available to propagate signals in either direction on a given general interconnect segment. These bidirectional (bidi) buffers are found adjacent to the switching matrices, above

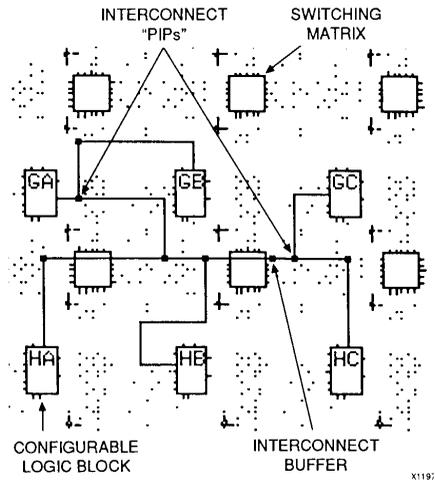


Figure 8: An XACT Design Editor view of routing resources used to form a typical interconnection network from CLB GA.

and to the right and may be highlighted by the use of the Show BIDI command in the XACT Design Editor. The other PIPs adjacent to the matrices are accessed to or from Longlines. The development system automatically defines the buffer direction based on the location of the interconnection network source. The delay calculator of the XACTstep development system automatically calculates and displays the block, interconnect and buffer delays for any paths selected. Generation of the simulation netlist with a worst-case delay model is provided by an XACT option.

Direct Interconnect

Direct interconnect, shown in Figure 12, provides the most efficient implementation of networks between adjacent CLBs or I/O Blocks. Signals routed from block to block using the direct interconnect exhibit minimum interconnect propagation and use no general interconnect resources. For each CLB, the X output may be connected directly to the B input of the CLB immediately to its right and to the C input of the CLB to its left. The Y output can use direct interconnect to drive the D input of the block immediately above and the A input of the block below. Direct interconnect should be used to maximize the speed of high-performance portions of logic. Where logic blocks are adjacent to IOBs, direct connect is provided alternately to the IOB inputs (I) and outputs (O) on all four edges of the die. The right edge provides additional direct connects from CLB outputs to adjacent IOBs. Direct interconnections of IOBs with CLBs are shown in Figure 13.

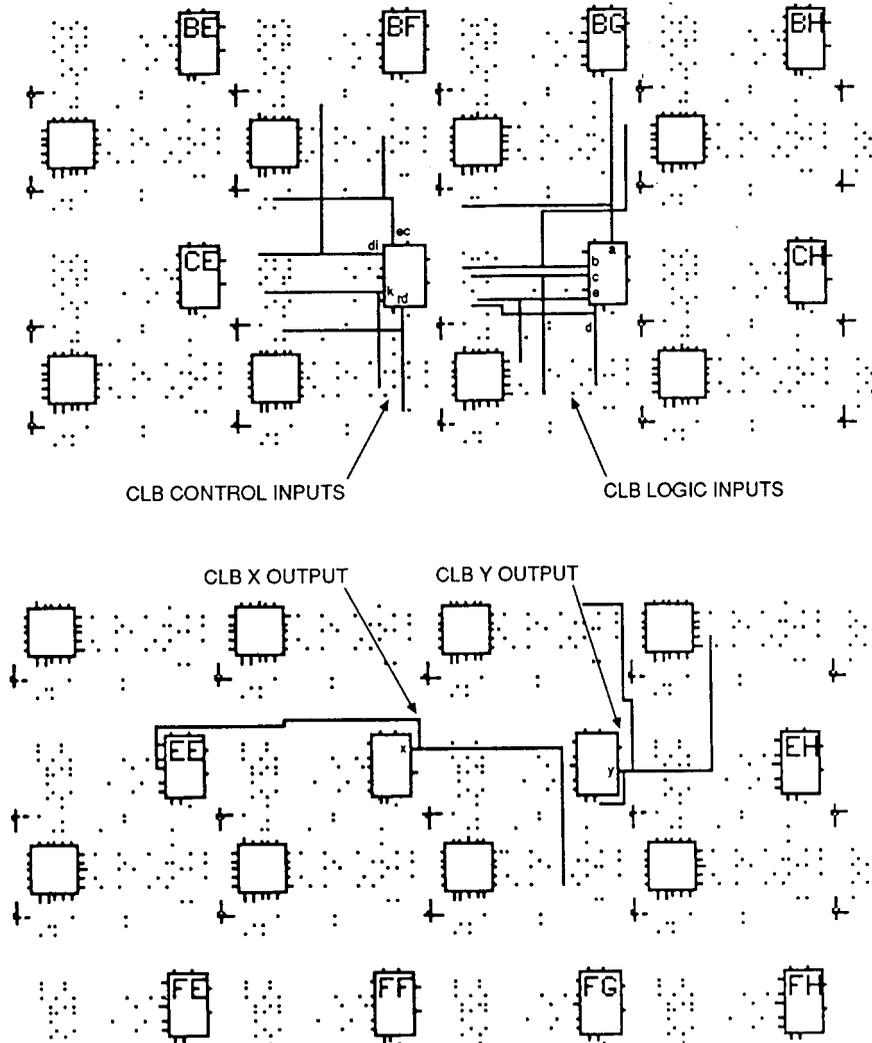


Figure 9: XACT Design Editor Locations of interconnect access, CLB control inputs, logic inputs and outputs. The dot pattern represents the available programmable interconnection points (PIPs).

Some of the interconnect PIPs are directional. This is indicated on the XACT Design Editor status line:

- ND is a nondirectional interconnection.
- D:H->V is a PIP that drives from a horizontal to a vertical line.
- D:V->H is a PIP that drives from a vertical to a horizontal line.
- D:C->T is a "T" PIP that drives from a cross of a T to the tail.
- D:CW is a corner PIP that drives in the clockwise direction.
- P0 indicates the PIP is non-conducting, P1 is on.

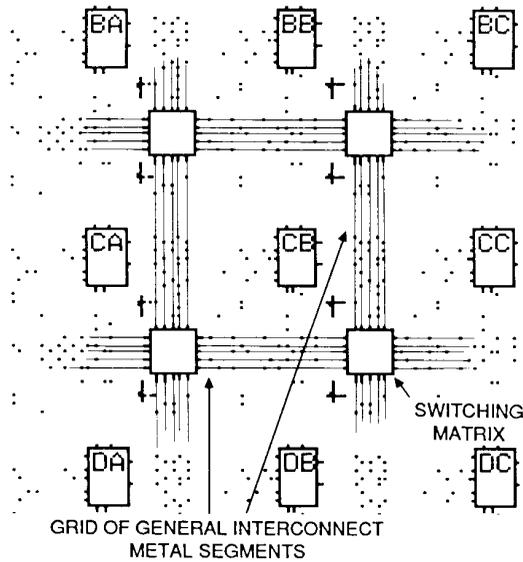


Figure 10: FPGA General-Purpose Interconnect.
Composed of a grid of metal segments that may be interconnected through switch matrices to form networks for CLB and IOB inputs and outputs.

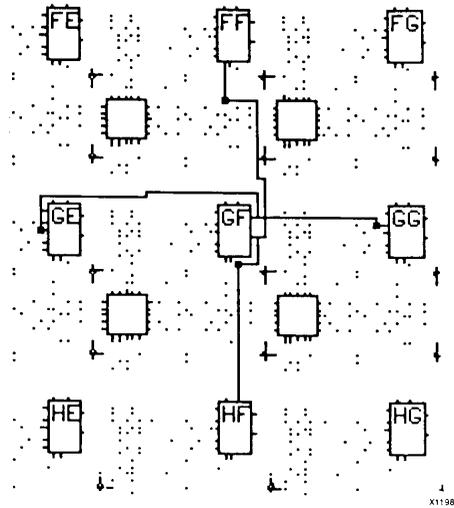
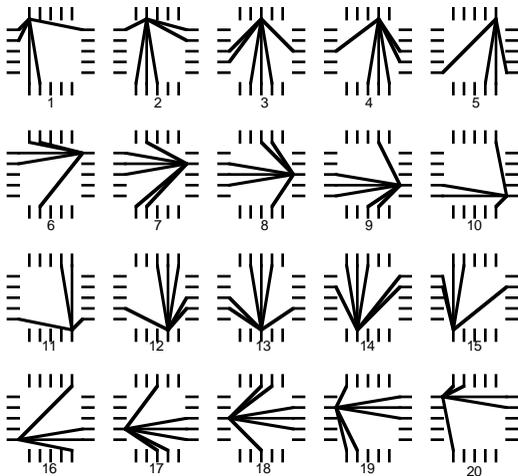


Figure 12: CLB X and Y Outputs.
The X and Y outputs of each CLB have single contact, direct access to inputs of adjacent CLBs



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Figure 11: Switch Matrix Interconnection Options for Each Pin.

Switch matrices on the edges are different. Use Show Matrix menu option in the XACT Design Editor.

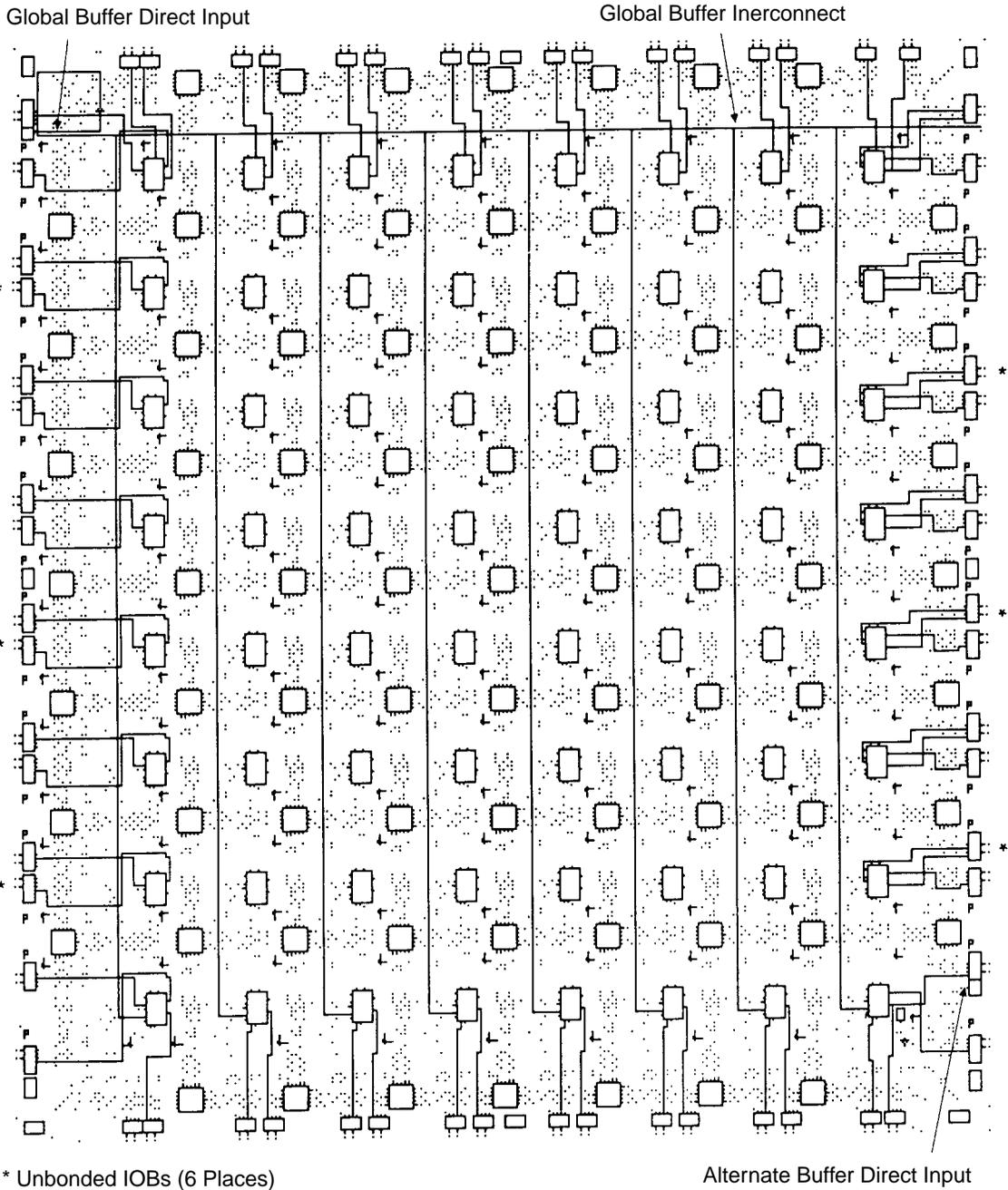


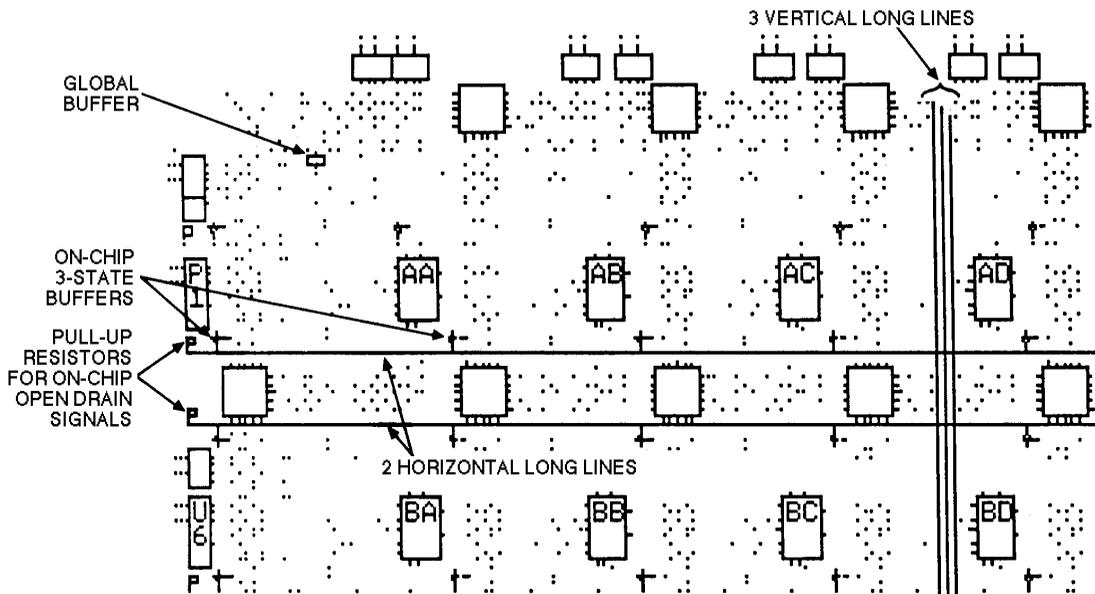
Figure 13: XC3020A Die-Edge IOBs. The XC3020A die-edge IOBs are provided with direct access to adjacent CLBs.

Longlines

The Longlines bypass the switch matrices and are intended primarily for signals that must travel a long distance, or must have minimum skew among multiple destinations. Longlines, shown in **Figure 14**, run vertically and horizontally the height or width of the interconnect area. Each interconnection column has three vertical Longlines, and each interconnection row has two horizontal Longlines. Two additional Longlines are located adjacent to the outer sets of switching matrices. In devices larger than the XC3020A,

two vertical Longlines in each column are connectable half-length lines. On the XC3020A, only the outer Longlines are connectable half-length lines.

Longlines can be driven by a logic block or IOB output on a column-by-column basis. This capability provides a common low skew control or clock line within each column of logic blocks. Interconnections of these Longlines are shown in **Figure 15**. Isolation buffers are provided at each input to a Longline and are enabled automatically by the development system when a connection is made.



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Figure 14: Horizontal and Vertical Longlines. These Longlines provide high fan-out, low-skew signal distribution in each row and column. The global buffer in the upper left die corner drives a common line throughout the FPGA.

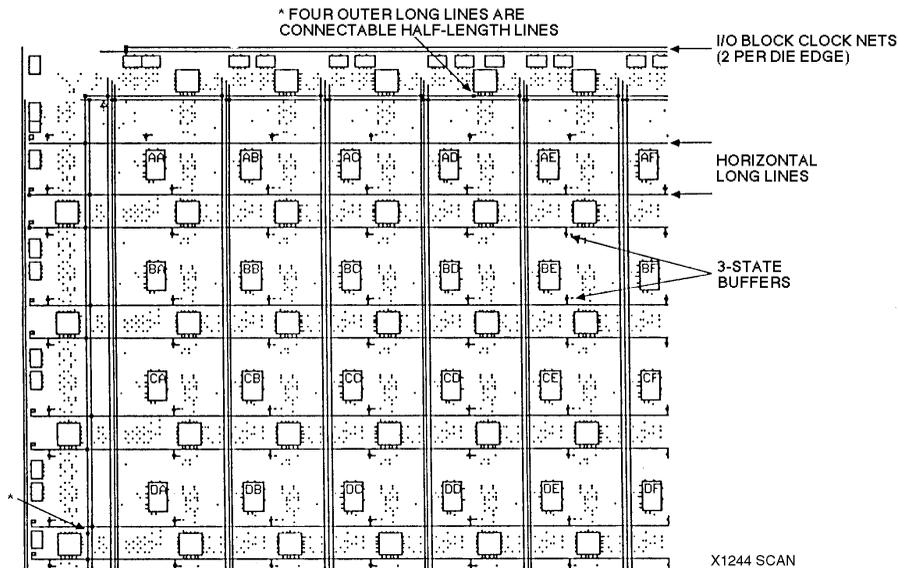


Figure 15: Programmable Interconnection of Longlines. This is provided at the edges of the routing area. Three-state buffers allow the use of horizontal Longlines to form on-chip wired AND and multiplexed buses. The left two non-clock vertical Longlines per column (except XC3020A) and the outer perimeter Longlines may be programmed as connectable half-length lines.

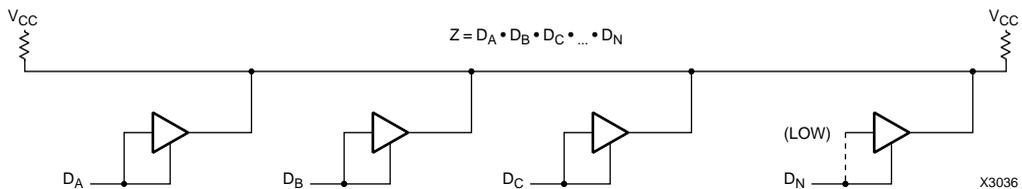


Figure 16: 3-State Buffers Implement a Wired-AND Function. When all the buffer 3-state lines are High, (high impedance), the pull-up resistor(s) provide the High output. The buffer inputs are driven by the control signals or a Low.

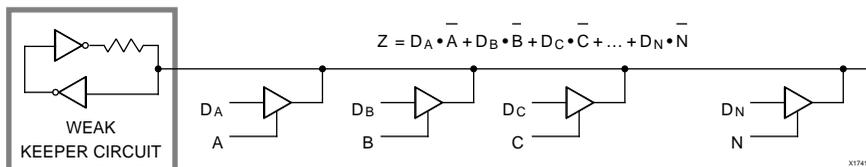


Figure 17: 3-State Buffers Implement a Multiplexer. The selection is accomplished by the buffer 3-state signal.

A buffer in the upper left corner of the FPGA chip drives a global net which is available to all K inputs of logic blocks. Using the global buffer for a clock signal provides a skew-free, high fan-out, synchronized clock for use at any or all of the IOBs and CLBs. Configuration bits for the K input to each logic block can select this global line or another routing resource as the clock source for its flip-flops. This net may also be programmed to drive the die edge clock lines for IOB use. An enhanced speed, CMOS threshold, direct access to this buffer is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal Longline that can drive programmed connections to a vertical Longline in each interconnection column. This alternate buffer also has low skew and high fan-out. The network formed by this alternate buffer's Longlines can be selected to drive the K inputs of the CLBs. CMOS threshold, high speed access to this buffer is available from the third pad from the bottom of the right die edge.

Internal Busses

A pair of 3-state buffers, located adjacent to each CLB, permits logic to drive the horizontal Longlines. Logic operation

of the 3-state buffer controls allows them to implement wide multiplexing functions. Any 3-state buffer input can be selected as drive for the horizontal long-line bus by applying a Low logic level on its 3-state control line. See Figure 16. The user is required to avoid contention which can result from multiple drivers with opposing logic levels. Control of the 3-state input by the same signal that drives the buffer input, creates an open-drain wired-AND function. A logic High on both buffer inputs creates a high impedance, which represents no contention. A logic Low enables the buffer to drive the Longline Low. See Figure 17. Pull-up resistors are available at each end of the Longline to provide a High output when all connected buffers are non-conducting. This forms fast, wide gating functions. When data drives the inputs, and separate signals drive the 3-state control lines, these buffers form multiplexers (3-state buses). In this case, care must be used to prevent contention through multiple active buffers of conflicting levels on a common line. Each horizontal Longline is also driven by a weak keeper circuit that prevents undefined floating levels by maintaining the previous logic level when the line is not driven by an active buffer or a pull-up resistor. Figure 18 shows 3-state buffers, Longlines and pull-up resistors.

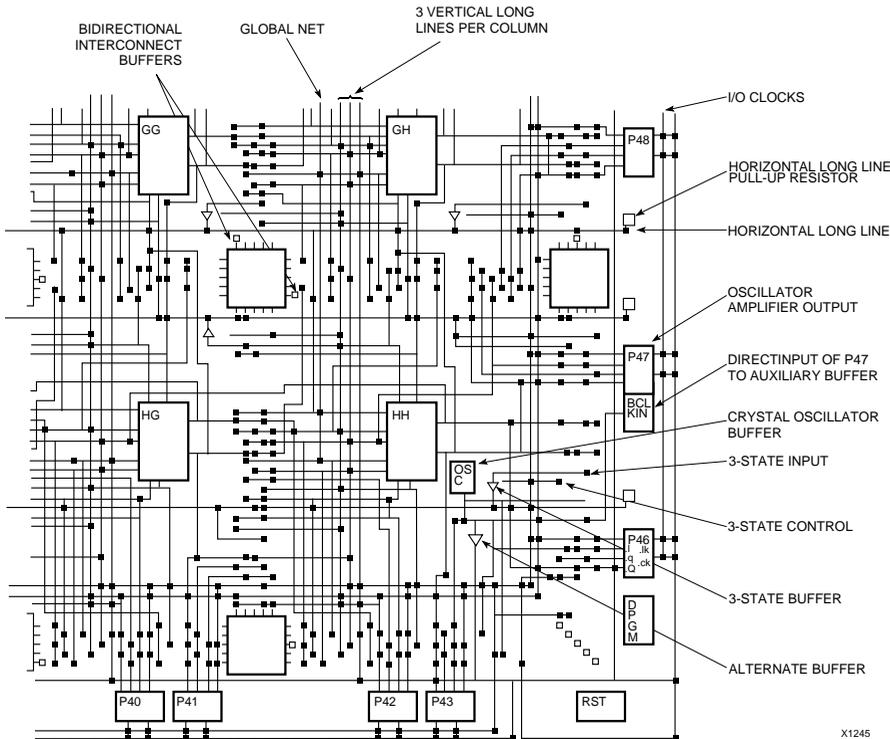


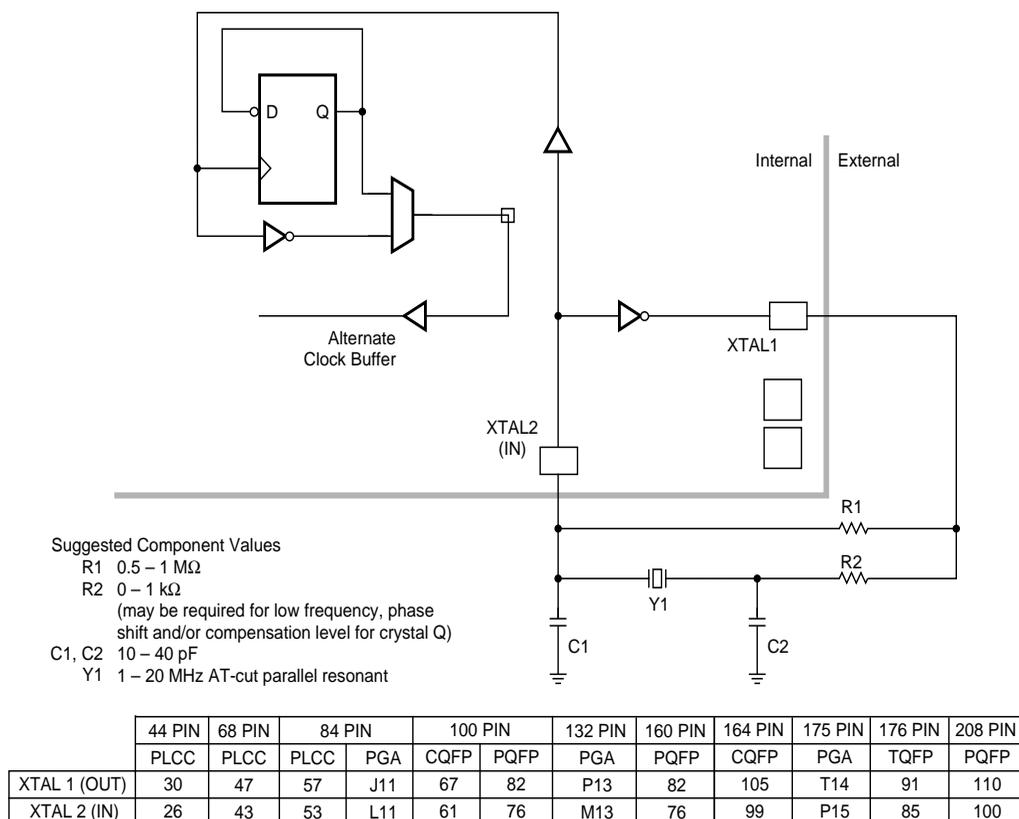
Figure 18: XACT Design Editor.

An extra large view of possible interconnections in the lower right corner of the XC3020A.

Crystal Oscillator

Figure 18 also shows the location of an internal high speed inverting amplifier that may be used to implement an on-chip crystal oscillator. It is associated with the auxiliary buffer in the lower right corner of the die. When the oscillator is configured by MakeBits and connected as a signal source, two special user IOBs are also configured to connect the oscillator amplifier with external crystal oscillator components as shown in Figure 19. A divide by two option is available to assure symmetry. The oscillator circuit becomes active early in the configuration process to allow the oscillator to stabilize. Actual internal connection is delayed until completion of configuration. In Figure 19 the feedback resistor R1, between the output and input, biases the amplifier at threshold. The inversion of the amplifier, together with the R-C networks and an AT-cut series resonant crystal, produce the 360-degree phase shift of the

Pierce oscillator. A series resistor R2 may be included to add to the amplifier output impedance when needed for phase-shift control, crystal resistance matching, or to limit the amplifier input swing to control clipping at large amplitudes. Excess feedback voltage may be corrected by the ratio of C2/C1. The amplifier is designed to be used from 1 MHz to about one-half the specified CLB toggle frequency. Use at frequencies below 1 MHz may require individual characterization with respect to a series resistance. Crystal oscillators above 20 MHz generally require a crystal which operates in a third overtone mode, where the fundamental frequency must be suppressed by an inductor across C2, turning this parallel resonant circuit to double the fundamental crystal frequency, i.e., 2/3 of the desired third harmonic frequency network. When the oscillator inverter is not used, these IOBs and their package pins are available for general user I/O.



X7064

Figure 19: Crystal Oscillator Inverter. When activated in the MakeBits program and by selecting an output network for its buffer, the crystal oscillator inverter uses two unconfigured package pins and external components to implement an oscillator. An optional divide-by-two mode is available to assure symmetry.

Configuration

Initialization Phase

An internal power-on-reset circuit is triggered when power is applied. When V_{CC} reaches the voltage at which portions of the FPGA device begin to operate (nominally 2.5 to 3 V), the programmable I/O output buffers are 3-stated and a high-impedance pull-up resistor is provided for the user I/O pins. A time-out delay is initiated to allow the power supply voltage to stabilize. During this time the power-down mode is inhibited. The Initialization state time-out (about 11 to 33 ms) is determined by a 14-bit counter driven by a self-generated internal timer. This nominal 1-MHz timer is subject to variations with process, temperature and power supply. As shown in Table 1, five configuration mode choices are available as determined by the input levels of three mode pins; M0, M1 and M2.

Table 1: Configuration Mode Choices

M0	M1	M2	CCLK	Mode	Data
0	0	0	output	Master	Bit Serial
0	0	1	output	Master	Byte Wide Addr. = 0000 up
0	1	0	—	reserved	—
0	1	1	output	Master	Byte Wide Addr. = FFFF down
1	0	0	—	reserved	—
1	0	1	output	Peripheral	Byte Wide
1	1	0	—	reserved	—
1	1	1	input	Slave	Bit Serial

In Master configuration modes, the device becomes the source of the Configuration Clock (CCLK). The beginning of configuration of devices using Peripheral or Slave modes must be delayed long enough for their initialization to be completed. An FPGA with mode lines selecting a Master configuration mode extends its initialization state using four times the delay (43 to 130 ms) to assure that all daisy-chained slave devices, which it may be driving, will be ready even if the master is very fast, and the slave(s) very slow. Figure 20 shows the state sequences. At the end of Initialization, the device enters the Clear state where it clears the configuration memory. The active Low, open-drain initialization signal \overline{INIT} indicates when the Initialization and Clear states are complete. The FPGA tests for the absence of an external active Low \overline{RESET} before it makes a final sample of the mode lines and enters the Configuration state. An external wired-AND of one or more \overline{INIT} pins can be used to control configuration by the assertion of the active-Low \overline{RESET} of a master mode device or to signal a processor that the FPGAs are not yet initialized.

If a configuration has begun, a re-assertion of \overline{RESET} for a minimum of three internal timer cycles will be recognized and the FPGA will initiate an abort, returning to the Clear state to clear the partially loaded configuration memory words. The FPGA will then resample \overline{RESET} and the mode lines before re-entering the Configuration state.

A re-program is initiated when a configured XC3000 series device senses a High-to-Low transition and subsequent >6 μ s Low level on the DONE/ $\overline{PROGRAM}$ package pin, or, if this pin is externally held permanently Low, a High-to-Low transi-

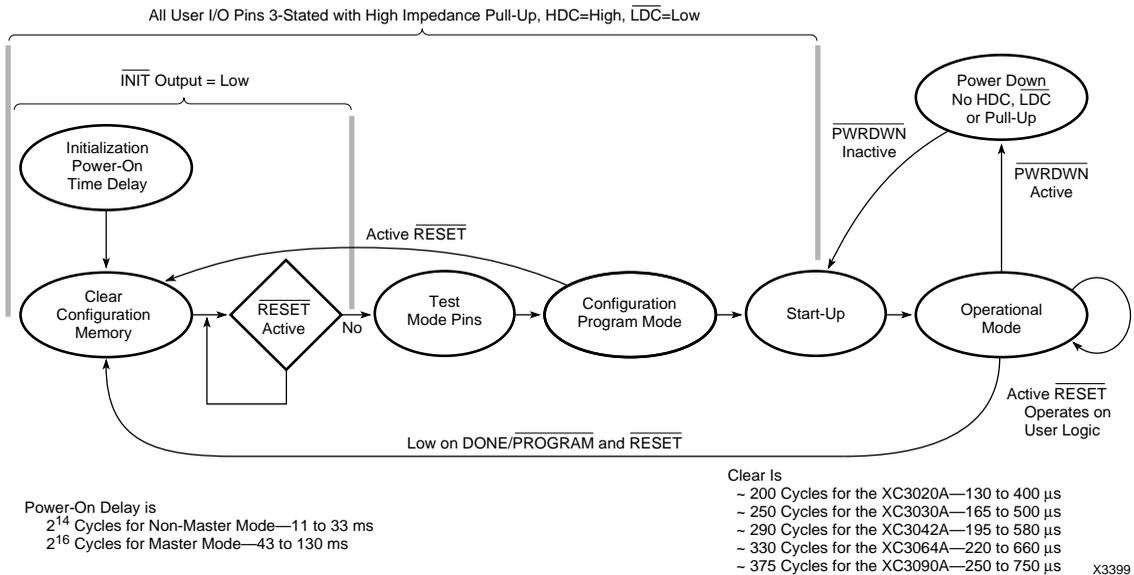


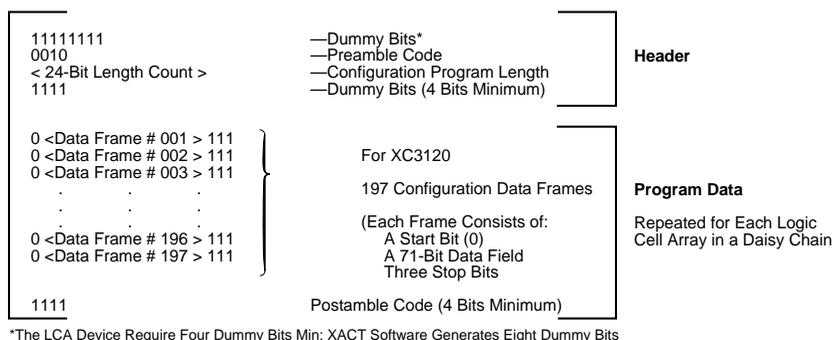
Figure 20: A State Diagram of the Configuration Process for Power-up and Reprogram.

tion and subsequent >6 μ s Low time on the $\overline{\text{RESET}}$ package pin.

The device returns to the Clear state where the configuration memory is cleared and mode lines re-sampled, as for an aborted configuration. The complete configuration program is cleared and loaded during each configuration program cycle.

Length count control allows a system of multiple Field Programmable Gate Arrays, of assorted sizes, to begin operation in a synchronized fashion. The configuration program generated by the MakePROM program of the XACTstep development system begins with a preamble of

11111110010 followed by a 24-bit length count representing the total number of configuration clocks needed to complete loading of the configuration program(s). The data framing is shown in Figure 21. All FPGAs connected in series read and shift preamble and length count in on positive and out on negative configuration clock edges. A device which has received the preamble and length count then presents a High Data Out until it has intercepted the appropriate number of data frames. When the configuration program memory of an FPGA is full and the length count does not yet compare, the device shifts any additional data through, as it did for preamble and length count. When the F{GA configuration memory is full and the length count



Device	XC3020A XC3020L XC3120 XC3120A	XC3030A XC3030L XC3130A	XC3042A XC3042L XC3142A XC3142L	XC3064A XC3064L XC3164A	XC3090A XC3090L XC3190A XC3190L	XC3195A
Gates	1,000 to 1,500	1,500 to 2,000	2,000 to 3,000	3,500 to 4,500	5,000 to 6,000	6,500 to 7,500
CLBs	64	100	144	224	320	484
Row x Col	(8 x 8)	(10 x 10)	(12 x 12)	(16 x 14)	(20 x 16)	(22 x 22)
IOBs	64	80	96	120	144	176
Flip-flops	256	360	480	688	928	1,320
Horizontal Longlines	16	20	24	32	40	44
TBUFs/Horizontal LL	9	11	13	15	17	23
Bits per Frame (including 1 start and 3 stop bits)	75	92	108	140	172	188
Frames	197	241	285	329	373	505
Program Data = Bits x Frames + 4 bits (excludes header)	14,779	22,176	30,784	46,064	64,160	94,944
PROM size (bits) = Program Data + 40-bit Header	14,819	22,216	30,824	46,104	64,200	94,984

Figure 21: Internal Configuration Data Structure for an FPGA. This shows the preamble, length count and data frames generated by the XACTstep Development System.

The Length Count produced by the MakeBits program = [(40-bit preamble + sum of program data + 1 per daisy chain device) rounded up to multiple of 8] - (2 ≤ K ≤ 4) where K is a function of DONE and RESET timing selected. An additional 8 is added if roundup increment is less than K. K additional clocks are needed to complete start-up after length count is reached.

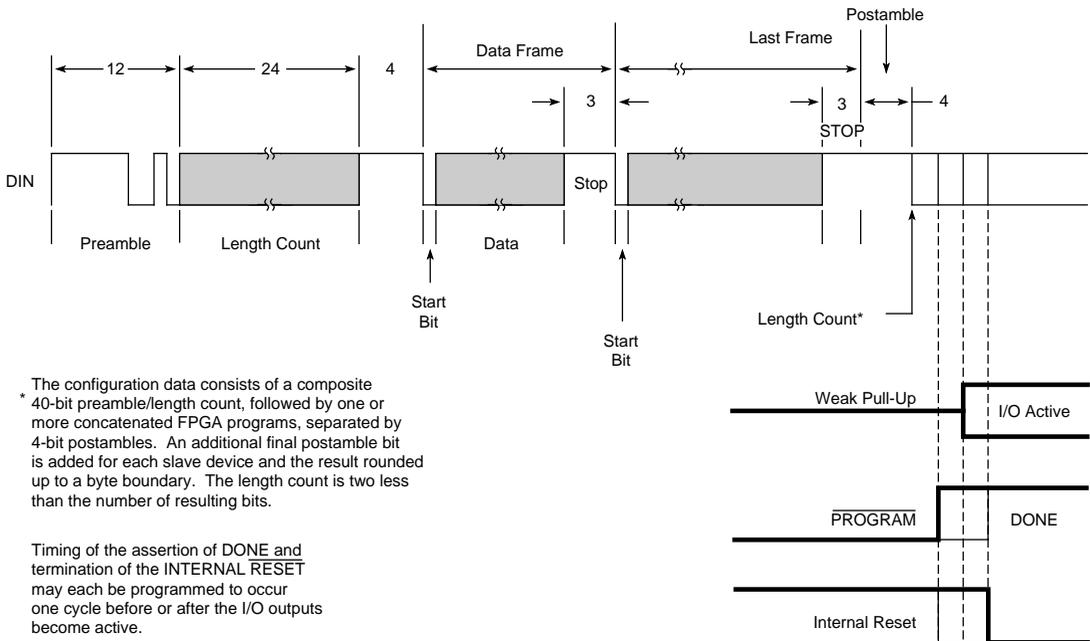
compares, the device will execute a synchronous start-up sequence and become operational. See Figure 22. Two CCLK cycles after the completion of loading configuration data, the user I/O pins are enabled as configured. As selected in MakeBits, the internal user-logic RESET is released either one clock cycle before or after the I/O pins become active. A similar timing selection is programmable for the DONE/PROG output signal. DONE/PROG may also be programmed to be an open drain or include a pull-up resistor to accommodate wired ANDING. The High During Configuration (HDC) and Low During Configuration (LDC) are two user I/O pins which are driven active while an FPGA is in its Initialization, Clear or Configure states. They and DONE/PROG provide signals for control of external logic signals such as RESET, bus enable or PROM enable during configuration. For parallel Master configuration modes, these signals provide PROM enable control and allow the data pins to be shared with user logic signals.

User I/O inputs can be programmed to be either TTL or CMOS compatible thresholds. At power-up, all inputs have TTL thresholds and can change to CMOS thresholds at the completion of configuration if the user has selected CMOS thresholds. The threshold of PWRDWN and the direct clock inputs are fixed at a CMOS level.

If the crystal oscillator is used, it will begin operation before configuration is complete to allow time for stabilization before it is connected to the internal circuitry.

Configuration Data

Configuration data to define the function and interconnection within a Field Programmable Gate Array is loaded from an external storage at power-up and after a re-program signal. Several methods of automatic and controlled loading of the required data are available. Logic levels applied to mode selection pins at the start of configuration time determine the method to be used. See Table 1. The data may be either bit-serial or byte-parallel, depending on the configuration mode. The different FPGAs have different sizes and numbers of data frames. To maintain compatibility between various device types, the Xilinx product families use compatible configuration formats. For the XC3020A, configuration requires 14779 bits for each device, arranged in 197 data frames. An additional 40 bits are used in the header. See Figure 22. The specific data format for each device is produced by the MakeBits command of the development system and one or more of these files can then be combined and appended to a length count preamble and be transformed into a PROM format file by the MakePROM command of the XACTstep development system. A compatibility exception precludes the use of an XC2000-series device as the master for XC3000-series devices if their DONE or RESET are programmed to occur after their outputs become active. The Tie Option of the MakeBits program defines output levels of unused blocks of a design and connects these to unused routing resources. This prevents indeterminate levels that might produce parasitic



Heavy lines indicate the default condition

X5988

Figure 22: Configuration and Start-up of One or More FPGAs.

supply currents. If unused blocks are not sufficient to complete the tie, the Flagnet command of EditLCA can be used to indicate nets which must not be used to drive the remaining unused routing, as that might affect timing of user nets. Norestore will retain the results of tie for timing analysis with Querynet before Restore returns the design to the untied condition. Tie can be omitted for quick breadboard iterations where a few additional milliamps of Icc are acceptable.

The configuration bitstream begins with eight High preamble bits, a 4-bit preamble code and a 24-bit length count. When configuration is initiated, a counter in the FPGA is set to zero and begins to count the total number of configuration clock cycles applied to the device. As each configuration data frame is supplied to the device, it is internally assembled into a data word, which is then loaded in parallel into one word of the internal configuration memory array. The configuration loading process is complete when the current length count equals the loaded length count and the required configuration program data frames have been written. Internal user flip-flops are held Reset during configuration.

Two user-programmable pins are defined in the unconfigured Field Programmable Gate Array. High During Configuration (HDC) and Low During Configuration (LDC) as well as DONE/ $\overline{\text{PROG}}$ may be used as external control signals during configuration. In Master mode configurations it is convenient to use LDC as an active-Low EPROM Chip Enable. After the last configuration data bit is loaded and the length count compares, the user I/O pins become active. Options in the MakeBits program allow timing choices of one clock earlier or later for the timing of the end of the internal logic RESET and the assertion of the DONE signal. The open-drain DONE/ $\overline{\text{PROG}}$ output can be AND-tied with multiple devices and used as an active-High READY, an active-Low PROM enable or a RESET to other portions of the system. The state diagram of Figure 20 illustrates the configuration process.

Configuration Modes

Master Mode

In Master mode, the FPGA automatically loads configuration data from an external memory device. There are three Master modes that use the internal timing source to supply the configuration clock (CCLK) to time the incoming data. Master Serial mode uses serial configuration data supplied to Data-in (DIN) from a synchronous serial source such as the Xilinx Serial Configuration PROM shown in Figure 23. Master Parallel Low and High modes automatically use parallel data supplied to the D0–D7 pins in response to the 16-bit address generated by the FPGA. Figure 25 shows an example of the parallel Master mode connections required. The HEX starting address is 0000 and increments for Master Low mode and it is FFFF and decrements for

Master High mode. These two modes provide address compatibility with microprocessors which begin execution from opposite ends of memory.

Peripheral Mode

Peripheral mode provides a simplified interface through which the device may be loaded byte-wide, as a processor peripheral. Figure 27 shows the peripheral mode connections. Processor write cycles are decoded from the common assertion of the active low Write Strobe ($\overline{\text{WS}}$), and two active low and one active high Chip Selects ($\overline{\text{CS0}}$, $\overline{\text{CS1}}$, CS2). The FPGA generates a configuration clock from the internal timing generator and serializes the parallel input data for internal framing or for succeeding slaves on Data Out (DOUT). A output High on READY/ $\overline{\text{BUSY}}$ pin indicates the completion of loading for each byte when the input register is ready for a new byte. As with Master modes, Peripheral mode may also be used as a lead device for a daisy-chain of slave devices.

Slave Serial Mode

Slave Serial mode provides a simple interface for loading the Field Programmable Gate Array configuration as shown in Figure 29. Serial data is supplied in conjunction with a synchronizing input clock. Most Slave mode applications are in daisy-chain configurations in which the data input is driven from the previous FPGA's data out, while the clock is supplied by a lead device in Master or Peripheral mode. Data may also be supplied by a processor or other special circuits.

Daisy Chain

The XACTstep development system is used to create a composite configuration for selected FPGAs including: a preamble, a length count for the total bitstream, multiple concatenated data programs and a postamble plus an additional fill bit per device in the serial chain. After loading and passing-on the preamble and length count to a possible daisy-chain, a lead device will load its configuration data frames while providing a High DOUT to possible down-stream devices as shown in Figure 25. Loading continues while the lead device has received its configuration program and the current length count has not reached the full value. The additional data is passed through the lead device and appears on the Data Out (DOUT) pin in serial form. The lead device also generates the Configuration Clock (CCLK) to synchronize the serial output data and data in of down-stream FPGAs. Data is read in on DIN of slave devices by the positive edge of CCLK and shifted out the DOUT on the negative edge of CCLK. A parallel Master mode device uses its internal timing generator to produce an internal CCLK of 8 times its EPROM address rate, while a Peripheral mode device produces a burst of 8 CCLKs for each chip select and write-strobe cycle. The internal timing generator continues to operate for general timing and synchronization of inputs in all modes.

Special Configuration Functions

The configuration data includes control over several special functions in addition to the normal user logic functions and interconnect.

- Input thresholds
- Readback disable
- DONE pull-up resistor
- DONE timing
- RESET timing
- Oscillator frequency divided by two

Each of these functions is controlled by configuration data bits which are selected as part of the normal *XACTstep* development system bitstream generation process.

Input Thresholds

Prior to the completion of configuration all FPGA input thresholds are TTL compatible. Upon completion of configuration, the input thresholds become either TTL or CMOS compatible as programmed. The use of the TTL threshold option requires some additional supply current for threshold shifting. The exception is the threshold of the $\overline{\text{PWRDWN}}$ input and direct clocks which always have a CMOS input. Prior to the completion of configuration the user I/O pins each have a high impedance pull-up. The configuration program can be used to enable the IOB pull-up resistors in the Operational mode to act either as an input load or to avoid a floating input on an otherwise unused pin.

Readback

The contents of a Field Programmable Gate Array may be read back if it has been programmed with a bitstream in which the Readback option has been enabled. Readback may be used for verification of configuration and as a method of determining the state of internal logic nodes during debugging. There are three options in generating the configuration bitstream.

- “Never” inhibits the Readback capability.
- “One-time,” inhibits Readback after one Readback has been executed to verify the configuration.
- “On-command” allows unrestricted use of Readback.

Readback is accomplished without the use of any of the user I/O pins; only M0, M1 and CCLK are used. The initiation of Readback is produced by a Low to High transition of the M0/RTRIG (Read Trigger) pin. The CCLK input must then be driven by external logic to read back the configuration data. The first three Low-to-High CCLK transitions clock out dummy data. The subsequent Low-to-High CCLK transitions shift the data frame information out on the M1/ $\overline{\text{RDATA}}$ (Read Data) pin. Note that the logic polarity is always inverted, a zero in configuration becomes a one in Readback, and vice versa. Note also that each Readback frame has one Start bit (read back as a one) but, unlike in configuration, each Readback frame has only one Stop bit (read back as a zero). The third leading dummy bit men-

tioned above can be considered the Start bit of the first frame. All data frames must be read back to complete the process and return the Mode Select and CCLK pins to their normal functions.

Readback data includes the current state of each CLB flip-flop, each input flip-flop or latch, and each device pad. These data are imbedded into unused configuration bit positions during Readback. This state information is used by the *XACTstep* development system In-Circuit Verifier to provide visibility into the internal operation of the logic while the system is operating. To readback a uniform time-sample of all storage elements, it may be necessary to inhibit the system clock.

Reprogram

To initiate a re-programming cycle, the dual-function pin DONE/ $\overline{\text{PROG}}$ must be given a High-to-Low transition. To reduce sensitivity to noise, the input signal is filtered for two cycles of the FPGA internal timing generator. When reprogram begins, the user-programmable I/O output buffers are disabled and high-impedance pull-ups are provided for the package pins. The device returns to the Clear state and clears the configuration memory before it indicates ‘initialized’. Since this Clear operation uses chip-individual internal timing, the master might complete the Clear operation and then start configuration before the slave has completed the Clear operation. To avoid this problem, the slave $\overline{\text{INIT}}$ pins must be AND-wired and used to force a $\overline{\text{RESET}}$ on the master (see [Figure 25](#)). Reprogram control is often implemented using an external open-collector driver which pulls DONE/ $\overline{\text{PROG}}$ Low. Once a stable request is recognized, the DONE/ $\overline{\text{PROG}}$ pin is held Low until the new configuration has been completed. Even if the re-program request is externally held Low beyond the configuration period, the FPGA will begin operation upon completion of configuration.

DONE Pull-up

DONE/ $\overline{\text{PROG}}$ is an open-drain I/O pin that indicates the FPGA is in the operational state. An optional internal pull-up resistor can be enabled by the user of the XACT development system when MakeBits is executed. The DONE/ $\overline{\text{PROG}}$ pins of multiple FPGAs in a daisy-chain may be connected together to indicate all are DONE or to direct them all to reprogram.

DONE Timing

The timing of the DONE status signal can be controlled by a selection in the MakeBits program to occur either a CCLK cycle before, or after, the outputs going active. See [Figure 22](#). This facilitates control of external functions such as a PROM enable or holding a system in a wait state.

RESET Timing

As with DONE timing, the timing of the release of the internal reset can be controlled by a selection in the MakeBits program to occur either a CCLK cycle before, or after, the outputs going active. See [Figure 22](#). This reset keeps all user programmable flip-flops and latches in a zero state during configuration.

Crystal Oscillator Division

A selection in the MakeBits program allows the user to incorporate a dedicated divide-by-two flip-flop between the crystal oscillator and the alternate clock line. This guarantees a symmetrical clock signal. Although the frequency stability of a crystal oscillator is very good, the symmetry of its waveform can be affected by bias or feedback drive.

Bitstream Error Checking

Bitstream error checking protects against erroneous configuration.

Each Xilinx FPGA bitstream consists of a 40-bit preamble, followed by a device-specific number of data frames. The number of bits per frame is also device-specific; however, each frame ends with three stop bits (111) followed by a start bit for the next frame (0).

All devices in all XC3000 families start reading in a new frame when they find the first 0 after the end of the previous frame. XC3000 device does not check for the correct stop bits, but XC3000A/XC3100A/XC3000L and XC3100L devices check that the last three bits of any frame are actually 111.

Under normal circumstances, all these FPGAs behave the same way; however, if the bitstream is corrupted, an XC3000 device will always start a new frame as soon as it finds the first 0 after the end of the previous frame, even if the data is completely wrong or out-of-sync. Given sufficient zeros in the data stream, the device will also go Done,

but with incorrect configuration and the possibility of internal contention.

An XC3000A/XC3100A/XC3000L/XC3100L device starts any new frame only if the three preceding bits are all ones. If this check fails, it pulls INIT Low and stops the internal configuration, although the Master CCLK keeps running. The user must then start a new configuration by applying a $>6 \mu\text{s}$ Low level on RESET.

This simple check does not protect against random bit errors, but it offers almost 100 percent protection against erroneous configuration files, defective configuration data sources, synchronization errors between configuration source and FPGA, or PC-board level defects, such as broken lines or solder-bridges.

Reset Spike Protection

A separate modification slows down the RESET input before configuration by using a two-stage shift register driven from the internal clock. It tolerates submicrosecond High spikes on RESET before configuration. The XC3000 master can be connected like an XC4000 master, but with its RESET input used instead of INIT. (On XC3000, INIT is output only).

Soft Start-up

After configuration, the outputs of all FPGAs in a daisy-chain become active simultaneously, as a result of the same CCLK edge. In the original XC3000/3100 devices, each output becomes active in either fast or slew-rate limited mode, depending on the way it is configured. This can lead to large ground-bounce signals. In XC3000A/XC3000L/XC3100A/XC3100L devices, all outputs become active first in slew-rate limited mode, reducing the ground bounce. After this soft start-up, each individual output slew rate is again controlled by the respective configuration bit.

Configuration Timing

This section describes the configuration modes in detail.

Master Serial Mode

In Master Serial mode, the CCLK output of the lead FPGA drives a Xilinx Serial PROM that feeds the DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. This puts the next data bit on the SPROM data output, connected to the DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

The lead FPGA then presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that

DOUT changes on the falling CCLK edge, and the next device in the daisy-chain accepts data on the subsequent rising CCLK edge.

The SPROM CE input can be driven from either \overline{LDC} or DONE. Using \overline{LDC} avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but \overline{LDC} is then restricted to be a permanently High user output. Using DONE also avoids contention on DIN, provided the early DONE option is invoked.

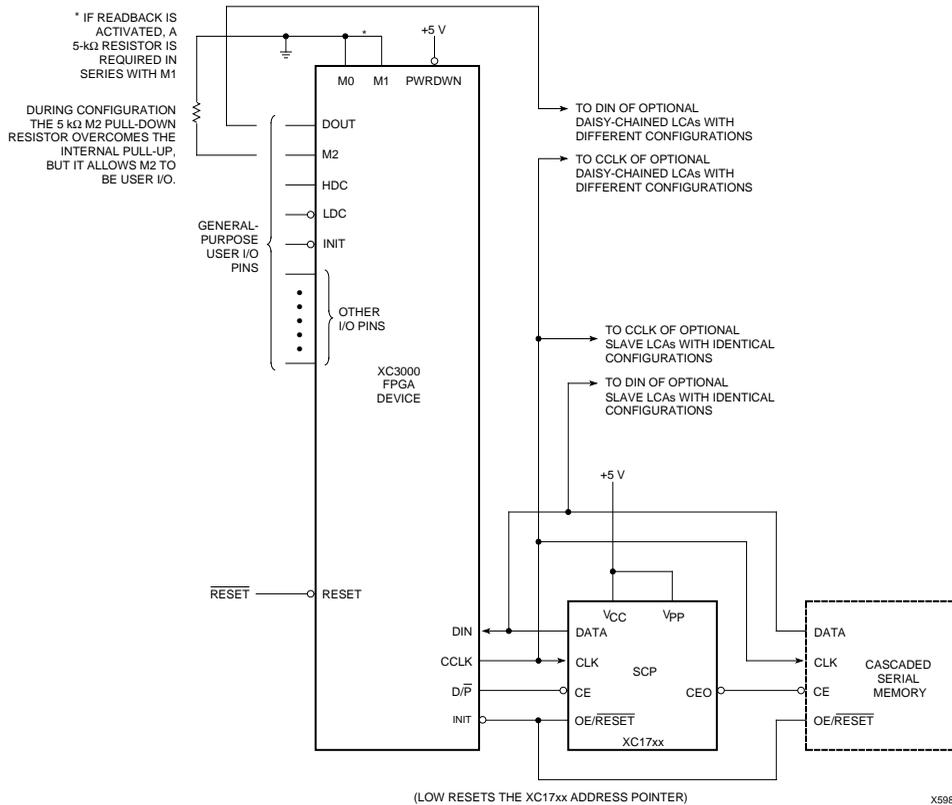
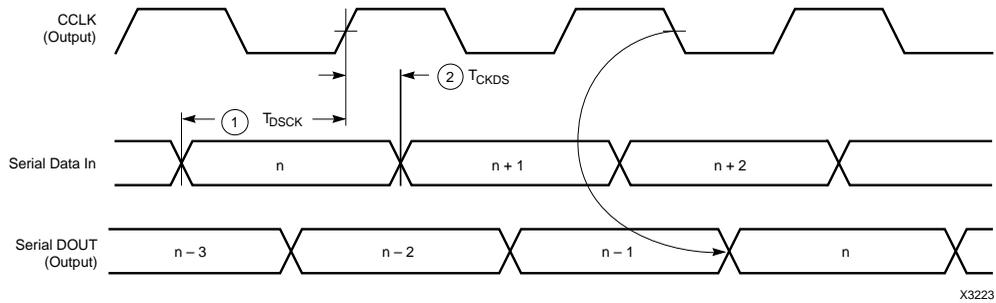


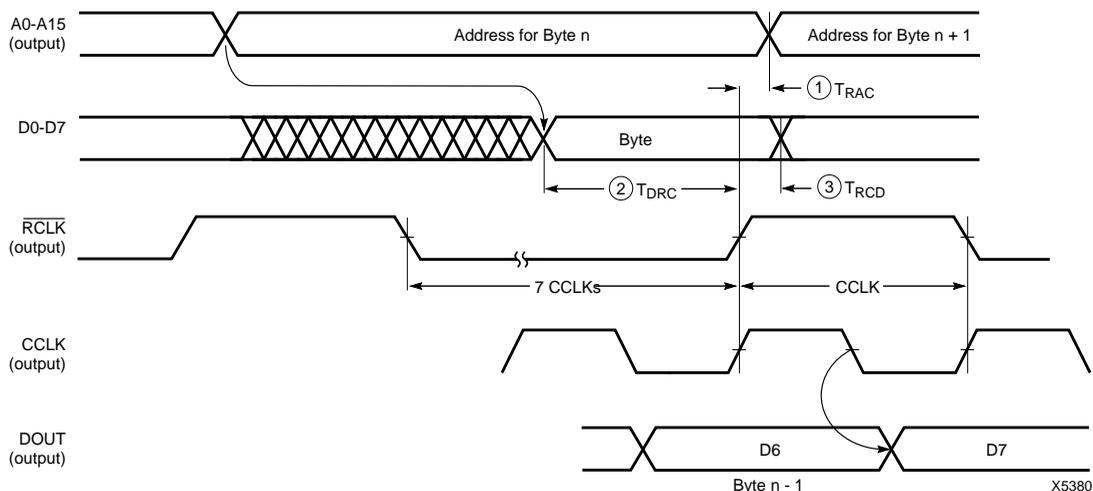
Figure 23: Master Serial Mode Circuit Diagram



	Description		Symbol	Min	Max	Units
CCLK	Data In setup	1	T_{DSCK}	60		ns
	Data In hold	2	C_{KDS}	0		ns

- Notes:
1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding \overline{RESET} Low until V_{CC} has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require >6- μ s High level on \overline{RESET} , followed by a >6- μ s Low level on \overline{RESET} and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).
 2. Configuration can be controlled by holding \overline{RESET} Low with or until after the \overline{INIT} of all daisy-chain slave-mode devices is High.
 3. Master-serial-mode timing is based on slave-mode testing.

Figure 24: Master Serial Mode Programming Switching Characteristics



	Description	Symbol	Min	Max	Units
RCLK	To address valid	1 T_{RAC}	0	200	ns
	To data setup	2 T_{DRC}	60		ns
	To data hold	3 T_{RCD}	0		ns
	RCLK High	T_{RCH}	600		ns
	RCLK Low	T_{RCL}	4.0		μ s

- Notes:
1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding \overline{RESET} Low until V_{CC} has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6- μ s High level on \overline{RESET} , followed by a >6- μ s Low level on \overline{RESET} and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).
 2. Configuration can be controlled by holding \overline{RESET} Low with or until after the \overline{INIT} of all daisy-chain slave-mode devices is High.

This timing diagram shows that the EPROM requirements are extremely relaxed: EPROM access time can be longer than 4000 ns. EPROM data output has no hold time requirements.

Figure 26: Master Parallel Mode Programming Switching Characteristics

Peripheral Mode

Peripheral mode uses the trailing edge of the logic AND condition of the $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, and \overline{WS} inputs to accept byte-wide data from a microprocessor bus. In the lead FPGA, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic. The lead FPGA presents the preamble data (and all data that overflows the lead device) on the DOUT pin.

The Ready/Busy output from the lead device acts as a handshake signal to the microprocessor. RDY/BUSY goes Low when a byte has been received, and goes High again

when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. The length of the \overline{BUSY} signal depends on the activity in the UART. If the shift register had been empty when the new byte was received, the \overline{BUSY} signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the \overline{BUSY} signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with DOUT equal to bit 6 (the next-to-last bit) of the last byte entered.

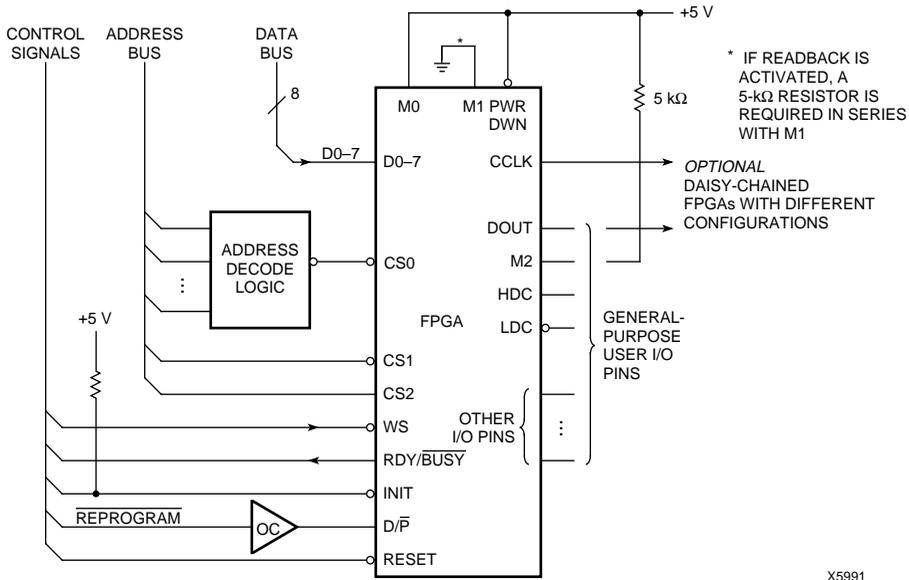
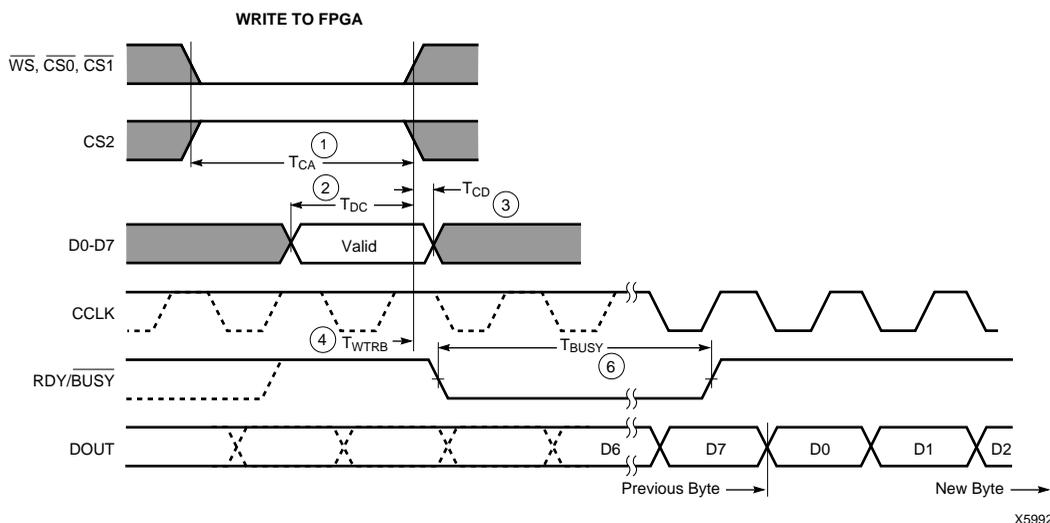


Figure 27: Peripheral Mode Circuit Diagram



X5992

	Description	Symbol	Min	Max	Units
WRITE	Effective Write time required (Assertion of $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, \overline{WS})	1 T_{CA}	100		ns
	DIN Setup time required	2 T_{DC}	60		ns
	DIN Hold time required	3 T_{CD}	0		ns
	RDY/BUSY delay after end of \overline{WS}	4 T_{WTRB}		60	ns
RDY	Earliest next \overline{WS} after end of \overline{BUSY}	5 T_{RBWT}	0		ns
	\overline{BUSY} Low time generated	6 T_{BUSY}	2.5	9	CCLK periods

- Notes:
- At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding \overline{RESET} Low until V_{CC} has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6- μ s High level on \overline{RESET} , followed by a >6- μ s Low level on \overline{RESET} and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).
 - Configuration must be delayed until the \overline{INIT} of all FPGAs is High.
 - Time from end of \overline{WS} to CCLK cycle for the new byte of data depends on completion of previous byte processing and the phase of the internal timing generator for CCLK.
 - CCLK and DOUT timing is tested in slave mode.
 - T_{BUSY} indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest T_{BUSY} occurs when a byte is loaded into an empty parallel-to-serial converter. The longest T_{BUSY} occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

Note: This timing diagram shows very relaxed requirements: Data need not be held beyond the rising edge of \overline{WS} . \overline{BUSY} will go active within 60 ns after the end of \overline{WS} . \overline{BUSY} will stay active for several microseconds. \overline{WS} may be asserted immediately after the end of \overline{BUSY} .

Figure 28: Peripheral Mode Programming Switching Characteristics

Slave Serial Mode

In Slave Serial mode, an external signal drives the CCLK input(s) of the FPGA(s). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short set-up time before each rising CCLK edge. The lead device then presents the preamble data (and all data that over-

flows the lead device) on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next device in the daisy-chain accepts data on the subsequent rising CCLK edge.

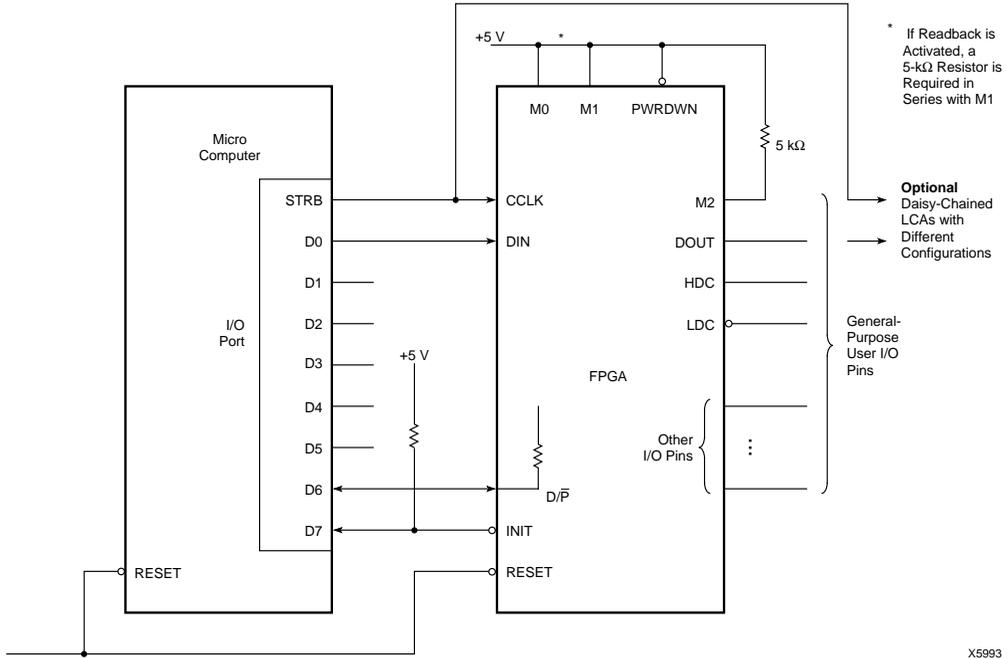
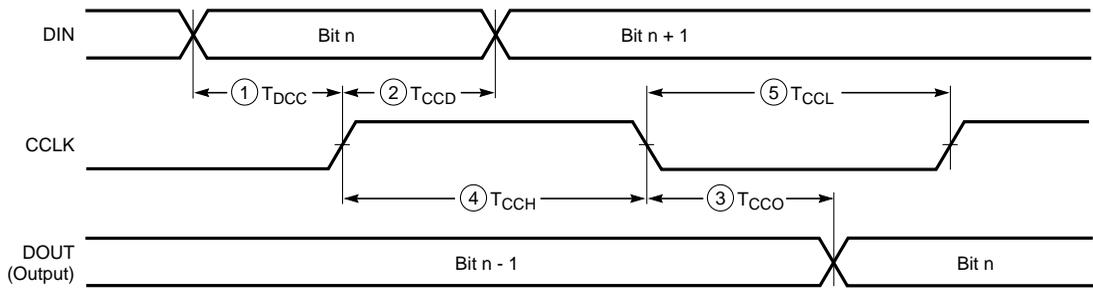


Figure 29: Slave Serial Mode Circuit Diagram

X5993



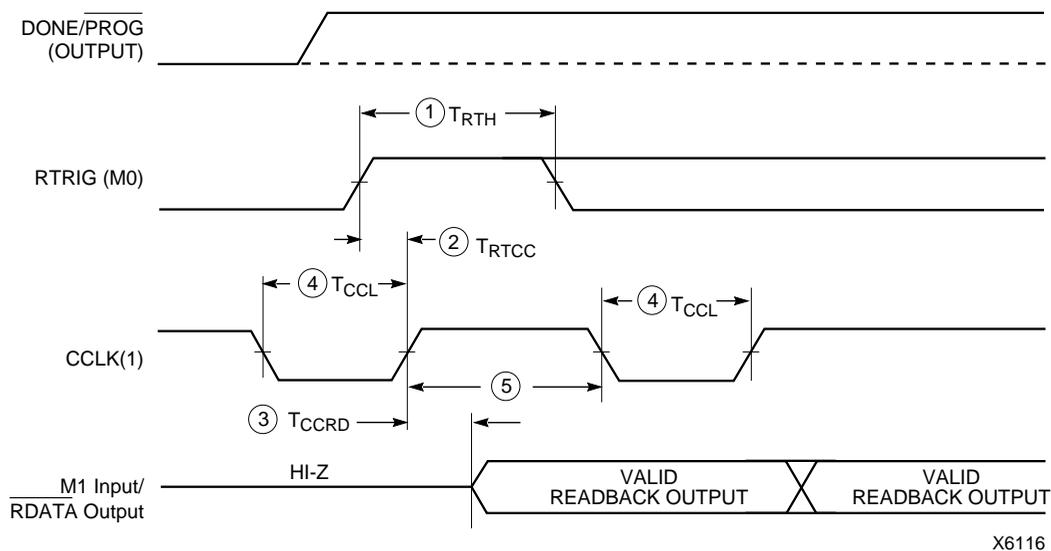
X5379

	Description	Symbol	Min	Max	Units
CCLK	To DOUT	3 T_{CCO}		100	ns
	DIN setup	1 T_{DCC}	60		ns
	DIN hold	2 T_{CCD}	0		ns
	High time	4 T_{CCH}	0.05		ns
	Low time (Note 1)	5 T_{CCL}	0.05	5.0	μ s
	Frequency	F_{CC}		10	MHz

- Notes:
1. The max limit of CCLK Low time is caused by dynamic circuitry inside the FPGA.
 2. Configuration must be delayed until the \overline{INIT} of all FPGAs is High.
 3. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding \overline{RESET} Low until V_{CC} has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6- μ s High level on \overline{RESET} , followed by a >6- μ s Low level on \overline{RESET} and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).

Figure 30: Slave Serial Mode Programming Switching Characteristics

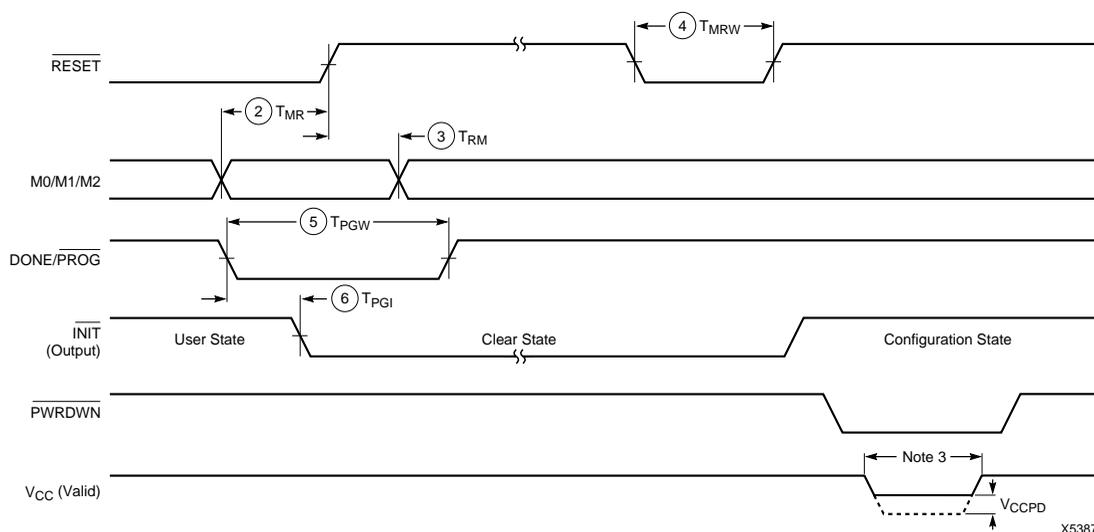
Program Readback Switching Characteristics



	Description		Symbol	Min	Max	Units
RTRIG	RTRIG High	1	T_{RTH}	250		ns
CCLK	RTRIG setup	2	T_{RTCC}	200		ns
	RDATA delay	3	T_{CCRD}		100	ns
	High time	4	T_{CCHR}	0.5		μ s
	Low time	5	T_{CCLR}	0.5	5	μ s

- Notes:
1. During Readback, CCLK frequency may not exceed 1 MHz.
 2. RETRIG (M0 positive transition) shall not be done until after one clock following active I/O pins.
 3. Readback should not be initiated until configuration is complete.
 4. T_{CCLR} is 5 μ s min to 15 μ s max for XC3000L.

General XC3000 Series Switching Characteristics



X5387

	Description		Symbol	Min	Max	Units
$\overline{\text{RESET}}$ (2)	M0, M1, M2 setup time required	2	T_{MR}	1		μs
	M0, M1, M2 hold time required	3	T_{RM}	4.5		μs
	RESET Width (Low) req. for Abort	4	T_{MRW}	6		μs
$\overline{\text{DONE/PROG}}$	Width (Low) required for Re-config.	5	T_{PGW}	6		μs
	INIT response after D/P is pulled Low	6	T_{PGI}		7	μs
$\overline{\text{PWRDWN}}$ (3)	Power Down V_{CC}		V_{CCPD}	2.3		V

- Notes:
- At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding $\overline{\text{RESET}}$ Low until V_{CC} has reached 4.0 V (2.5 V for XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >1- μs High level on $\overline{\text{RESET}}$, followed by a >6- μs Low level on $\overline{\text{RESET}}$ and $\overline{\text{D/P}}$ after V_{CC} has reached 4.0 V (2.5 V for XC3000L).
 - $\overline{\text{RESET}}$ timing relative to valid mode lines (M0, M1, M2) is relevant when $\overline{\text{RESET}}$ is used to delay configuration. The specified hold time is caused by a shift-register filter slowing down the response to $\overline{\text{RESET}}$ during configuration.
 - $\overline{\text{PWRDWN}}$ transitions must occur while $V_{CC} > 4.0$ V (2.5 V for XC3000L).

Device Performance

The XC3000 families of FPGAs can achieve very high performance. This is the result of

- A sub-micron manufacturing process, developed and continuously being enhanced for the production of state-of-the-art CMOS SRAMs.
- Careful optimization of transistor geometries, circuit design, and lay-out, based on years of experience with the XC3000 family.
- A look-up table based, coarse-grained architecture that can collapse multiple-layer combinatorial logic into a single function generator. One CLB can implement up to four layers of conventional logic in as little as 1.5 ns.

Actual system performance is determined by the timing of critical paths, including the delay through the combinatorial and sequential logic elements within CLBs and IOBs, plus the delay in the interconnect routing. The AC-timing specifications state the worst-case timing parameters for the various logic resources available in the XC3000-families architecture. **Figure 31** shows a variety of elements involved in determining system performance.

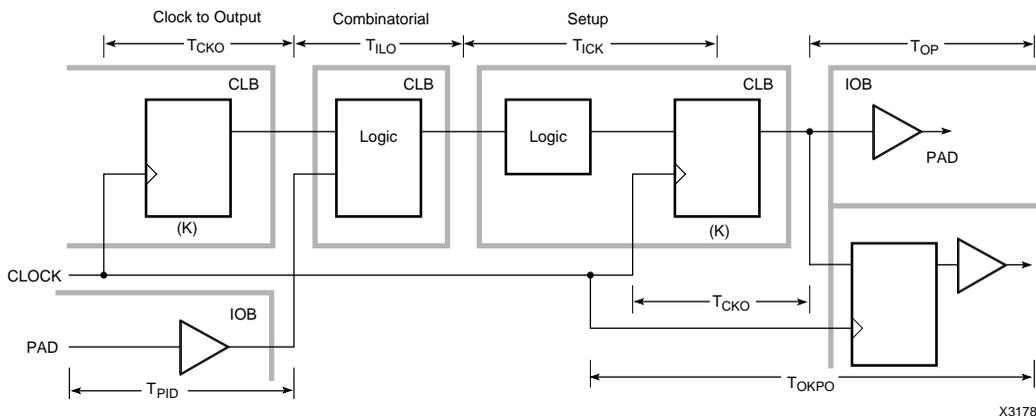
Logic block performance is expressed as the propagation time from the interconnect point at the input to the block to the output of the block in the interconnect area. Since combinatorial logic is implemented with a memory lookup table within a CLB, the combinatorial delay through the CLB, called T_{ILO} , is always the same, regardless of the function being implemented. For the combinatorial logic function driving the data input of the storage element, the critical timing is data set-up relative to the clock edge provided to the flip-flop element. The delay from the clock source to the output of the logic block is critical in the timing signals produced by storage elements. Loading of a logic-block output is limited only by the resulting propagation delay of the larger interconnect network. Speed performance of the

logic block is a function of supply voltage and temperature. See **Figure 32**.

Interconnect performance depends on the routing resources used to implement the signal path. Direct interconnects to the neighboring CLB provide an extremely fast path. Local interconnects go through switch matrices (magic boxes) and suffer an RC delay, equal to the resistance of the pass transistor multiplied by the capacitance of the driven metal line. Longlines carry the signal across the length or breadth of the chip with only one access delay. Generous on-chip signal buffering makes performance relatively insensitive to signal fan-out; increasing fan-out from 1 to 8 changes the CLB delay by only 10%. Clocks can be distributed with two low-skew clock distribution networks.

The tools in the *XACTstep* Development System used to place and route a design in an XC3000 FPGA automatically calculate the actual maximum worst-case delays along each signal path. This timing information can be back-annotated to the design's netlist for use in timing simulation or examined with X-Delay, a static timing analyzer.

Actual system performance is applications dependent. The maximum clock rate that can be used in a system is determined by the critical path delays within that system. These delays are combinations of incremental logic and routing delays, and vary from design to design. In a synchronous system, the maximum clock rate depends on the number of combinatorial logic layers between re-synchronizing flip-flops. **Figure 33** shows the achievable clock rate as a function of the number of CLB layers.



X3178

Figure 31: Primary Block Speed Factors. Actual timing is a function of various block factors combined with routing factors. Overall performance can be evaluated with the XDelay timing calculator or by an optional simulation.

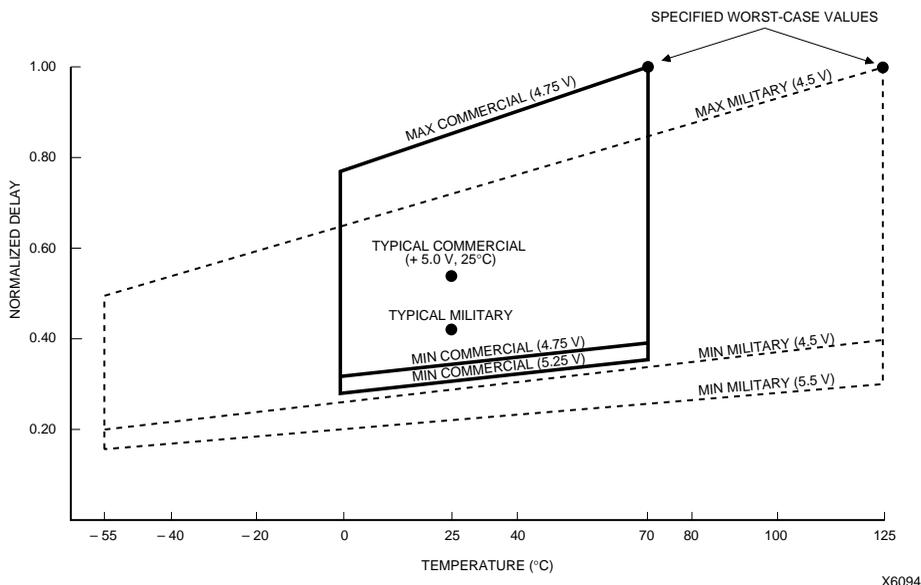


Figure 32: Relative Delay as a Function of Temperature, Supply Voltage and Processing Variations

X6094

Power

Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated V_{CC} and ground ring surrounding the logic array provides power to the I/O drivers. An independent matrix of V_{CC} and groundlines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1- μ F capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 4- or 8-mA loads under worst-case conditions may be capable of driving as much as 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise.

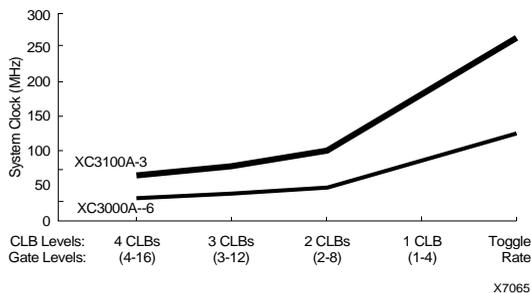


Figure 33: Clock Rate as a Function of Logic Complexity (Number of Combinational Levels between Flip-Flops)

X7065

Dynamic Power Consumption

	XC3042A	XC3042L	XC3142A	
One CLB driving three local interconnects	0.25	0.17	0.25	mW per MHz
One global clock buffer and clock line	2.25	1.40	1.70	mW per MHz
One device output with a 50 pF load	1.25	1.25	1.25	mW per MHz

Power Consumption

The Field Programmable Gate Array exhibits the low power consumption characteristic of CMOS ICs. For any design, the configuration option of TTL chip input threshold requires power for the threshold reference. The power required by the static memory cells that hold the configuration data is very low and may be maintained in a power-down mode.

Typically, most of power dissipation is produced by external capacitive loads on the output buffers. This load and frequency dependent power is 25 $\mu\text{W}/\text{pF}/\text{MHz}$ per output. Another component of I/O power is the external dc loading on all output pins.

Internal power dissipation is a function of the number and size of the nodes, and the frequency at which they change. In an FPGA, the fraction of nodes changing on a given clock is typically low (10-20%). For example, in a long binary counter, the total activity of all counter flip-flops is equivalent to that of only two CLB outputs toggling at the clock frequency. Typical global clock-buffer power is between 2.0 mW/MHz for the XC3020A and 3.5 mW/MHz for the XC3090A. The internal capacitive load is more a function of interconnect than fan-out. With a typical load of three general interconnect segments, each CLB output requires about 0.25 mW per MHz of its output frequency.

Because the control storage of the FPGA is CMOS static memory, its cells require a very low standby current for data retention. In some systems, this low data retention current characteristic can be used as a method of preserving configurations in the event of a primary power loss. The FPGA

has built in powerdown logic which, when activated, will disable normal operation of the device and retain only the configuration data. All internal operation is suspended and output buffers are placed in their high-impedance state with no pull-ups. Different from the XC3000 family which can be powered down to a current consumption of a few microamps, the XC3100A draws 5 mA, even in power-down. This makes power-down operation less meaningful. In contrast, I_{CCPD} for the XC3000L is only 10 μA .

To force the FPGA into the Powerdown state, the user must pull the $\overline{\text{PWRDWN}}$ pin Low and continue to supply a retention voltage to the V_{CC} pins. When normal power is restored, V_{CC} is elevated to its normal operating voltage and $\overline{\text{PWRDWN}}$ is returned to a High. The FPGA resumes operation with the same internal sequence that occurs at the conclusion of configuration. Internal-I/O and logic-block storage elements will be reset, the outputs will become enabled and the DONE/PROG pin will be released.

When V_{CC} is shut down or disconnected, some power might unintentionally be supplied from an incoming signal driving an I/O pin. The conventional electrostatic input protection is implemented with diodes to the supply and ground. A positive voltage applied to an input (or output) will cause the positive protection diode to conduct and drive the V_{CC} connection. This condition can produce invalid power conditions and should be avoided. A large series resistor might be used to limit the current or a bipolar buffer may be used to isolate the input signal.

Pin Descriptions

Permanently Dedicated Pins

V_{CC}

Two to eight (depending on package type) connections to the positive V supply voltage. All must be connected.

GND

Two to eight (depending on package type) connections to ground. All must be connected.

PWRDWN

A Low on this CMOS-compatible input stops all internal activity, but retains configuration. All flip-flops and latches are reset, all outputs are 3-stated, and all inputs are interpreted as High, independent of their actual level. When PWRDWN returns High, the FPGA becomes operational with DONE Low for two cycles of the internal 1-MHz clock. Before and during configuration, PWRDWN must be High. If not used, PWRDWN must be tied to V_{CC} .

RESET

This is an active Low input which has three functions.

Prior to the start of configuration, a Low input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle. When the time-out and RESET are complete, the levels of the M lines are sampled and configuration begins.

If RESET is asserted during a configuration, the FPGA is re-initialized and restarts the configuration at the termination of RESET.

If RESET is asserted after configuration is complete, it provides a global asynchronous RESET of all IOB and CLB storage elements of the FPGA.

CCLK

During configuration, Configuration Clock is an output of an FPGA in Master mode or Peripheral mode, but an input in Slave mode. During Readback, CCLK is a clock input for shifting configuration data out of the FPGA.

CCLK drives dynamic circuitry inside the FPGA. The Low time may, therefore, not exceed a few microseconds. When used as an input, CCLK must be "parked High". An internal pull-up resistor maintains High when the pin is not being driven.

DONE/PROG (D/P)

DONE is an open-drain output, configurable with or without an internal pull-up resistor of 2 to 8 k Ω . At the completion of configuration, the FPGA circuitry becomes active in a synchronous order; DONE is programmed to go active High one cycle either before or after the outputs go active.

Once configuration is done, a High-to-Low transition of this pin will cause an initialization of the FPGA and start a reconfiguration.

M0/RTRIG

As Mode 0, this input is sampled on power-on to determine the power-on delay (2^{14} cycles if M0 is High, 2^{16} cycles if M0 is Low). Before the start of configuration, this input is again sampled together with M1, M2 to determine the configuration mode to be used.

A Low-to-High input transition, after configuration is complete, acts as a Read Trigger and initiates a Readback of configuration and storage-element data clocked by CCLK. By selecting the appropriate Readback option when generating the bitstream, this operation may be limited to a single Readback, or be inhibited altogether.

M1/RDATA

As Mode 1, this input and M0, M2 are sampled before the start of configuration to establish the configuration mode to be used. If Readback is never used, M1 can be tied directly to ground or V_{CC} . If Readback is ever used, M1 must use a 5-k Ω resistor to ground or V_{CC} , to accommodate the RDATA output.

As an active-Low Read Data, after configuration is complete, this pin is the output of the Readback data.

User I/O Pins That Can Have Special Functions

M2

During configuration, this input has a weak pull-up resistor. Together with M0 and M1, it is sampled before the start of configuration to establish the configuration mode to be used. After configuration, this pin is a user-programmable I/O pin.

HDC

During configuration, this output is held at a High level to indicate that configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin.

LDC

During Configuration, this output is held at a Low level to indicate that the configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin. LDC is particularly useful in Master mode as a Low enable for an EPROM, but it must then be programmed as a High after configuration.

INIT

This is an active Low open-drain output with a weak pull-up and is held Low during the power stabilization and internal clearing of the configuration memory. It can be used to indicate status to a configuring microprocessor or, as a wired

AND of several slave mode devices, a hold-off signal for a master mode device. After configuration this pin becomes a user-programmable I/O pin.

BCLKIN

This is a direct CMOS level input to the alternate clock buffer (Auxiliary Buffer) in the lower right corner.

XTL1

This user I/O pin can be used to operate as the output of an amplifier driving an external crystal and bias circuitry.

XTL2

This user I/O pin can be used as the input of an amplifier connected to an external crystal and bias circuitry. The I/O Block is left unconfigured. The oscillator configuration is activated by routing a net from the oscillator buffer symbol output and by the MakeBits program.

CS0, CS1, CS2, WS

These four inputs represent a set of signals, three active Low and one active High, that are used to control configuration-data entry in the Peripheral mode. Simultaneous assertion of all four inputs generates a Write to the internal data buffer. The removal of any assertion clocks in the D0-D7 data. In Master-Parallel mode, WS and CS2 are the A0 and A1 outputs. After configuration, these pins are user-programmable I/O pins.

RDY/BUSY

During Peripheral Parallel mode configuration this pin indicates when the chip is ready for another byte of data to be written to it. After configuration is complete, this pin becomes a user-programmed I/O pin.

RCLK

During Master Parallel mode configuration, each change on the A0-15 outputs is preceded by a rising edge on RCLK, a redundant output signal. After configuration is complete, this pin becomes a user-programmed I/O pin.

D0-D7

This set of eight pins represents the parallel configuration byte for the parallel Master and Peripheral modes. After configuration is complete, they are user-programmed I/O pins.

A0-A15

During Master Parallel mode, these 16 pins present an address output for a configuration EPROM. After configuration, they are user-programmable I/O pins.

DIN

During Slave or Master Serial configuration, this pin is used as a serial-data input. In the Master or Peripheral configuration, this is the Data 0 input. After configuration is complete, this pin becomes a user-programmed I/O pin.

DOUT

During configuration this pin is used to output serial-configuration data to the DIN pin of a daisy-chained slave. After configuration is complete, this pin becomes a user-programmed I/O pin.

TCLKIN

This is a direct CMOS-level input to the global clock buffer. This pin can also be configured as a user programmable I/O pin. However, since TCLKIN is the preferred input to the global clock net, and the global clock net should be used as the primary clock source, this pin is usually the clock input to the chip.

Unrestricted User I/O Pins**I/O**

An I/O pin may be programmed by the user to be an Input or an Output pin following configuration. All unrestricted I/O pins, plus the special pins mentioned on the following page, have a weak pull-up resistor of 50 k Ω to 100 k Ω that becomes active as soon as the device powers up, and stays active until the end of configuration.

Note: *Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a 50 k Ω to 100 k Ω pull-up resistor.*

Pin Functions During Configuration

Configuration Mode <M2:M1:M0>					***														***			
SLAVE SERIAL <1:1:1>	MASTER-SERIAL <0:0:0>	PERIPH <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>	44 PLCC	64 VQFP	68 PLCC	84 PLCC	84 PGA	100 PQFP	100 VQFP	132 PGA	144 TQFP	160 PQFP	175 PGA	176 TQFP	208 PQFP	223 PGA	User Function			
POWR DWN (I)	POWER DWN (I)	POWER DWN (I)	POWER DWN (I)	POWER DWN (I)	7	17	10	12	B2	29	26	A1	1	159	B2	1	3	B2	POWER DWN (I)			
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	16	31	25	31	J2	52	49	B13	36	40	B14	45	48	C16	RDATA			
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	17	32	26	32	L1	54	51	A14	38	42	B15	47	50	B17	RTRIG (I)			
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	18	33	27	33	K2	56	53	C13	40	44	C15	49	56	A17	I/O			
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	19	34	28	34	K3	57	54	B14	41	45	E14	50	57	A18	I/O			
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	20	36	30	36	L3	59	56	D14	45	49	D16	54	61	E16	I/O			
INIT*	INIT*	INIT*	INIT*	INIT*	22	40	34	42	K6	65	62	G14	65	59	H15	65	77	J16	I/O			
GND	GND	GND	GND	GND	23	41	35	43	J6	66	63	H12	55	19	J14	67	79	K15	GND			
					26	47	43	53	L11	76	73	M13	69	76	P15	85	100	V18	XTL2 OR I/O			
RESET (I)	RESET (I)	RESET (I)	RESET (I)	RESET (I)	27	48	44	54	K10	78	75	P14	71	78	R15	87	102	U17	RESET (I)			
DONE	DONE	DONE	DONE	DONE	28	49	45	55	J10	80	77	N13	73	80	R14	89	107	V17	PROGRAM (I)			
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)		50	46	56	K11	81	78	M12	74	81	N13	90	109	T16	I/O			
					30	51	47	57	J11	82	79	P13	75	82	T14	91	110	U16	XTL1 OR I/O			
		DATA 6 (I)	DATA 7 (I)	DATA 6 (I)		52	48	58	H10	83	80	N11	78	86	P12	96	115	U15	I/O			
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)		53	49	60	F10	87	84	M9	84	92	T11	102	122	U12	I/O			
		CS0 (I)				54	50	61	G10	88	85	N9	85	93	R10	103	123	V11	I/O			
		DATA (4)	DATA (4)	DATA (4)		55	51	62	G11	89	86	N8	88	96	R9	108	128	U10	I/O			
		DATA (3)	DATA (3)	DATA (3)		57	53	65	F11	92	89	N7	92	102	P8	112	132	T9	I/O			
		CS1 (I)				58	54	66	E11	93	90	P6	93	103	R8	113	133	V9	I/O			
		DATA (2)	DATA (2)	DATA (2)		59	55	67	E10	94	91	M6	96	106	R7	118	138	V8	I/O			
		DATA (1)	DATA (1)	DATA (1)		60	56	70	D10	98	95	M5	102	114	R5	124	145	U5	I/O			
		RDY/BUSY	RCLK	RCLK		61	57	71	C11	99	96	N4	103	115	P5	125	146	U4	I/O			
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	38	62	58	72	B11	100	97	N2	106	119	R3	130	151	U3	I/O			
DOUT	DOUT	DOUT	DOUT	DOUT	39	63	59	73	C10	1	98	M3	107	120	N4	131	152	V2	I/O			
CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	CCLK (O)	40	64	60	74	A11	2	99	P1	108	121	R2	132	153	U2	CCLK (I)			
		WS (I)	A0	A0		1	61	75	B10	5	2	M2	111	124	P2	135	161	T3	I/O			
		CS2 (I)	A1	A1		2	62	76	B9	6	3	N1	112	125	M3	136	162	V1	I/O			
			A2	A2		3	63	77	A10	8	5	L2	115	128	P1	140	165	R2	I/O			
			A3	A3		4	64	78	A9	9	6	L1	116	129	N1	141	166	T1	I/O			
			A15	A15			65	81	B6	12	9	K1	119	132	M1	146	172	N2	5			
			A4	A4		5	66	82	B7	13	10	J2	120	133	L2	147	173	M4	I/O			
			A14	A14		6	67	83	A7	14	11	H1	123	136	K2	150	178	L4	I/O			
			A5	A5		7	68	84	C7	15	12	H2	124	137	K1	151	179	L2	I/O			
			A13	A13		9	2	2	A6	17	14	G2	128	141	H2	156	184	K3	I/O			
			A6	A6		10	3	3	A5	18	15	G1	129	142	H1	157	185	J1	I/O			
			A12	A12		11	4	4	B5	19	16	F2	133	147	F2	164	192	G1	I/O			
			A7	A7		12	5	5	C5	20	17	E1	134	148	E1	165	193	G4	I/O			
			A11	A11		13	6	6	A3	23	20	D1	137	151	D1	169	199	F4	I/O			
			A8	A8		14	7	9	A2	24	21	D2	138	152	C1	170	200	E2	I/O			
			A10	A10		15	8	10	B3	25	22	B1	141	155	E3	173	203	E3	I/O			
			A9	A9		16	9	11	A1	26	26	C2	142	156	C2	174	204	B1	I/O			
																			All Others			
							X	X	X	X									XC3x20A etc.			
						X	X	X	X	X									XC3x30A etc.			
							X	X	X	X	X	X	X						XC3x42A etc.			
							X**					X	X						XC3x64A etc.			
							X**					X	X	X	X	X	X	X	XC3x90A etc.			
							X**							X	X		X	X	XC3195A			

Notes:

Generic I/O pins are not shown.

For a detailed description of the configuration modes, see [page 310](#) through [page 319](#).

For pinout details, see [page 327](#) through [page 338](#).

Represents a 50-kΩ to 100-kΩ pull-up before and during configuration.

* INIT is an open drain output during configuration.

(I) Represents an input.

** Pin assignment for the XC3064A/XC3090A and XC3195A differ from those shown.

*** Peripheral mode and master parallel mode are not supported in the PC44 package.

**** Pin assignments for the XC3195A PQ208 differ from those shown.

Pin assignments of PGA Footprint PLCC sockets and PGA packages are not identical.

The information on this page is provided as a convenient summary. For detailed pin descriptions, see the preceding two pages.

Note: Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a 50-kW to 100-kW pull-up resistor.

XC3000 Series Pin Assignments

Xilinx offers the six different array sizes in the XC3000 families in a variety of surface-mount and through-hole package types, with pin counts from 44 to 223.

Each chip is offered in several package types to accommodate the available PC board space and manufacturing technology. Most package types are also offered with different chips to accommodate design changes without the need for PC board changes.

Note that there is no perfect match between the number of bonding pads on the chip and the number of pins on a package. In some cases, the chip has more pads than there are pins on the package, as indicated by the information (“unused” pads) below the line in the following table. The IOBs of the unconnected pads can still be used as storage elements if the specified propagation delays and set-up times are acceptable.

In other cases, the chip has fewer pads than there are pins on the package; therefore, some package pins are not connected (n.c.), as shown above the line in the following table.

Number of Unbounded or Unconnected Pins

Device	Pads	Number of Package Pins											
		44	64	68	84	100	132	144	160	175	176	208	223
3020A	74	—	—	6 u	10 n.c.	26 n.c.	—	—	—	—	—	—	—
3030A	98	54 u	34 u	30 u	14 u	2 n.c.	—	—	—	—	—	—	—
3042A	118	—	—	—	34 u	18 u	14 n.c.	26 n.c.	—	—	—	—	—
3064A	142	—	—	—	50 u	—	10 u	2 u	18 n.c.	—	—	—	—
3090A	166	—	—	—	82 u	—	—	—	6 u	9 n.c.	10 n.c.	42 n.c.	—
3195A	198	—	—	—	114 u	—	—	—	—	9 n.c. 32 u	—	10 n.c.	25 n.c.

n.c. = Unconnected package pin
u = Unbonded device pad

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Number of Available I/O Pins

	Max I/O	Number of Package Pins																	
		44	64	68	84	100	120	132	144	156	160	164	175	176	191	196	208	223	240
XC3020A/XC3120A	64			58	64	64													
XC3030A/XC3130A	80	34	54	58	74	80													
XC3042A/XC3142A	96				74	82		96	96										
XC3064A/XC3164A	120				70			110	110		120								
XC3090A/XC3190A	144				70				120		138	144	144	144			144		
XC3195A	176				70						138		144				176	176	

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XC3000 Series 44-Pin PLCC Pinouts

XC3000A, XC3000L, and XC3100A families have identical pinouts

Pin No.	XC3030A
1	GND
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	PWRDWN
8	TCLKIN-I/O
9	I/O
10	I/O
11	I/O
12	VCC
13	I/O
14	I/O
15	I/O
16	M1-RDATA
17	M0-RTRIG
18	M2-I/O
19	HDC-I/O
20	LDC-I/O
21	I/O
22	INIT-I/O

Pin No.	XC3030A
23	GND
24	I/O
25	I/O
26	XTL2(IN)-I/O
27	RESET
28	DONE-PGM
29	I/O
30	XTL1(OUT)-BCLK-I/O
31	I/O
32	I/O
33	I/O
34	VCC
35	I/O
36	I/O
37	I/O
38	DIN-I/O
39	DOOUT-I/O
40	CCLK
41	I/O
42	I/O
43	I/O
44	I/O

Peripheral mode and Master Parallel mode are not supported in the PC44 package

XC3000 Series 64-Pin Plastic VQFP Pinouts

XC3000A, XC3000L, and XC3100A families have identical pinouts

Pin No.	XC3030A
1	A0-WS-I/O
2	A1-CS2-I/O
3	A2-I/O
4	A3-I/O
5	A4-I/O
6	A14-I/O
7	A5-I/O
8	GND
9	A13-I/O
10	A6-I/O
11	A12-I/O
12	A7-I/O
13	A11-I/O
14	A8-I/O
15	A10-I/O
16	A9-I/O
17	$\overline{\text{PWRDN}}$
18	TCLKIN-I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	VCC
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1-RDATA
32	M0-RTRIG

Pin No.	XC3030A
33	M2-I/O
34	HDC-I/O
35	I/O
36	$\overline{\text{LDC}}$ -I/O
37	I/O
38	I/O
39	I/O
40	$\overline{\text{INIT}}$ -I/O
41	GND
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	XTAL2(IN)-I/O
48	$\overline{\text{RESET}}$
49	DONE- $\overline{\text{PG}}$
50	D7-I/O
51	XTAL1(OUT)-BCLKIN-I/O
52	D6-I/O
53	D5-I/O
54	$\overline{\text{CS0}}$ -I/O
55	D4-I/O
56	VCC
57	D3-I/O
58	$\overline{\text{CS1}}$ -I/O
59	D2-I/O
60	D1-I/O
61	$\overline{\text{RDY}}/\overline{\text{BUSY}}-\overline{\text{RCLK}}$ -I/O
62	D0-DIN-I/O
63	DOUT-I/O
64	CCLK

XC3000 Series 68-Pin PLCC, 84-Pin PLCC and PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC	84 PGA	68 PLCC XC3030A XC3020A	XC3020A, XC3030A, XC3042A	84 PLCC	84 PGA	XC3020A
XC3030A	XC3020A								
10	10	PWRDN	12	B2	44	RESET	54	K10	44
11	11	TCLKIN-I/O	13	C2	45	DONE- \overline{PG}	55	J10	45
12	—	I/O*	14	B1	46	D7-I/O	56	K11	46
13	12	I/O	15	C1	47	XTL1(OUT)-BCLKIN-I/O	57	J11	47
14	13	I/O	16	D2	48	D6-I/O	58	H10	48
—	—	I/O	17	D1	—	I/O	59	H11	—
15	14	I/O	18	E3	49	D5-I/O	60	F10	49
16	15	I/O	19	E2	50	CS0-I/O	61	G10	50
—	16	I/O	20	E1	51	D4-I/O	62	G11	51
17	17	I/O	21	F2	—	I/O	63	G9	—
18	18	VCC	22	F3	52	VCC	64	F9	52
19	19	I/O	23	G3	53	D3-I/O	65	F11	53
—	—	I/O	24	G1	54	CST-I/O	66	E11	54
20	20	I/O	25	G2	55	D2-I/O	67	E10	55
—	21	I/O	26	F1	—	I/O	68	E9	—
21	22	I/O	27	H1	—	I/O*	69	D11	—
22	—	I/O	28	H2	56	D1-I/O	70	D10	56
23	23	I/O	29	J1	57	RDY/BUSY-RCLK-I/O	71	C11	57
24	24	I/O	30	K1	58	D0-DIN-I/O	72	B11	58
25	25	M1-RDATA	31	J2	59	DOUT-I/O	73	C10	59
26	26	M0-RTRIG	32	L1	60	CCLK	74	A11	60
27	27	M2-I/O	33	K2	61	A0- \overline{WS} -I/O	75	B10	61
28	28	HDC-I/O	34	K3	62	A1-CS2-I/O	76	B9	62
29	29	I/O	35	L2	63	A2-I/O	77	A10	63
30	30	LDC-I/O	36	L3	64	A3-I/O	78	A9	64
—	31	I/O	37	K4	—	I/O*	79	B8	—
—	—	I/O*	38	L4	—	I/O*	80	A8	—
31	32	I/O	39	J5	65	A15-I/O	81	B6	65
32	33	I/O	40	K5	66	A4-I/O	82	B7	66
33	—	I/O*	41	L5	67	A14-I/O	83	A7	67
34	34	INIT-I/O	42	K6	68	A5-I/O	84	C7	68
35	35	GND	43	J6	1	GND	1	C6	1
36	36	I/O	44	J7	2	A13-I/O	2	A6	2
37	37	I/O	45	L7	3	A6-I/O	3	A5	3
38	38	I/O	46	K7	4	A12-I/O	4	B5	4
39	39	I/O	47	L6	5	A7-I/O	5	C5	5
—	40	I/O	48	L8	—	I/O*	6	A4	—
—	41	I/O	49	K8	—	I/O*	7	B4	—
40	—	I/O*	50	L9	6	A11-I/O	8	A3	6
41	—	I/O*	51	L10	7	A8-I/O	9	A2	7
42	42	I/O	52	K9	8	A10-I/O	10	B3	8
43	43	XTL2(IN)-I/O	53	L11	9	A9-I/O	11	A1	9

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

This table describes the pinouts of three different chips in three different packages. The pin-description column lists 84 of the 118 pads on the XC3042A (and 84 of the 98 pads on the XC3030A) that are connected to the 84 package pins. Ten pads, indicated by an asterisk, do not exist on the XC3020A, which has 74 pads; therefore the corresponding pins on the 84-pin packages have no connections to an XC3020A. Six pads on the XC3020A and 16 pads on the XC3030A, indicated by a dash (—) in the 68 PLCC column, have no connection to the 68 PLCC, but are connected to the 84-pin packages.

XC3064A/XC3090A/XC3195A 84-Pin PLCC Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PLCC Pin Number	XC3064A, XC3090A, XC3195A
12	PWRDN
13	TCLKIN-I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	GND*
22	VCC
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1-RDATA
32	M0-RTRIG
33	M2-I/O
34	HDC-I/O
35	I/O
36	LDC-I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	INIT/I/O*
42	VCC*
43	GND
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	XTL2(IN)-I/O

PLCC Pin Number	XC3064A, XC3090A, XC3195A
54	RESET
55	DONE- \overline{PG}
56	D7-I/O
57	XTL1(OUT)-BCLKIN-I/O
58	D6-I/O
59	I/O
60	D5-I/O
61	CS0-I/O
62	D4-I/O
63	I/O
64	VCC
65	GND*
66	D3-I/O*
67	CS1-I/O*
68	D2-I/O*
69	I/O
70	D1-I/O
71	RDY/BUSY-RCLK-I/O
72	D0-DIN-I/O
73	DOUT-I/O
74	CCLK
75	A0- \overline{WS} -I/O
76	A1-CS2-I/O
77	A2-I/O
78	A3-I/O
79	I/O
80	I/O
81	A15-I/O
82	A4-I/O
83	A14-I/O
84	A5-I/O
1	GND
2	VCC*
3	A13-I/O*
4	A6-I/O*
5	A12-I/O*
6	A7-I/O*
7	I/O
8	A11-I/O
9	A8-I/O
10	A10-I/O
11	A9-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* In the PC84 package, XC3064A, XC3090A and XC3195A have additional VCC and GND pins and thus a different pin definition than XC3020A/XC3030A/XC3042A.

XC3000 Series 100-Pin QFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin No.			XC3020A XC3030A XC3042A	Pin No.			XC3020A XC3030A XC3042A	Pin No.			XC3020A XC3030A XC3042A
CQFP	PQFP	TQFP VQFP		CQFP	PQFP	TQFP VQFP		CQFP	PQFP	TQFP VQFP	
1	16	13	GND	35	50	47	I/O*	69	84	81	I/O*
2	17	14	A13-I/O	36	51	48	I/O*	70	85	82	I/O*
3	18	15	A6-I/O	37	52	49	M1-RD	71	86	83	I/O
4	19	16	A12-I/O	38	53	50	GND*	72	87	84	D5-I/O
5	20	17	A7-I/O	39	54	51	MO-RT	73	88	85	CS0-I/O
6	21	18	I/O*	40	55	52	VCC*	74	89	86	D4-I/O
7	22	19	I/O*	41	56	53	M2-I/O	75	90	87	I/O
8	23	20	A11-I/O	42	57	54	HDC-I/O	76	91	88	VCC
9	24	21	A8-I/O	43	58	55	I/O	77	92	89	D3-I/O
10	25	22	A10-I/O	44	59	56	LDC-I/O	78	93	90	CS1-I/O
11	26	23	A9-I/O	45	60	57	I/O*	79	94	91	D2-I/O
12	27	24	VCC*	46	61	58	I/O*	80	95	92	I/O
13	28	25	GND*	47	62	59	I/O	81	96	93	I/O*
14	29	26	PWRDN	48	63	60	I/O	82	97	94	I/O*
15	30	27	TCLKIN-I/O	49	64	61	I/O	83	98	95	D1-I/O
16	31	28	I/O**	50	65	62	INIT-I/O	84	99	96	RDY/BUSY-RCLK-I/O
17	32	29	I/O*	51	66	63	GND	85	100	97	DO-DIN-I/O
18	33	30	I/O*	52	67	64	I/O	86	1	98	DOOUT-I/O
19	34	31	I/O	53	68	65	I/O	87	2	99	CCLK
20	35	32	I/O	54	69	66	I/O	88	3	100	VCC*
21	36	33	I/O	55	70	67	I/O	89	4	1	GND*
22	37	34	I/O	56	71	68	I/O	90	5	2	AO-WS-I/O
23	38	35	I/O	57	72	69	I/O	91	6	3	A1-CS2-I/O
24	39	36	I/O	58	73	70	I/O	92	7	4	I/O**
25	40	37	I/O	59	74	71	I/O*	93	8	5	A2-I/O
26	41	38	VCC	60	75	72	I/O*	94	9	6	A3-I/O
27	42	39	I/O	61	76	73	XTL2-I/O	95	10	7	I/O*
28	43	40	I/O	62	77	74	GND*	96	11	8	I/O*
29	44	41	I/O	63	78	75	RESET	97	12	9	A15-I/O
30	45	42	I/O	64	79	76	VCC*	98	13	10	A4-I/O
31	46	43	I/O	65	80	77	DONE-PG	99	14	11	A14-I/O
32	47	44	I/O	66	81	78	D7-I/O	100	15	12	A5-I/O
33	48	45	I/O	67	82	79	BCLKIN-XTL1-I/O				
34	49	46	I/O	68	83	80	D6-I/O				

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* This table describes the pinouts of three different chips in three different packages. The pin-description column lists 100 of the 118 pads on the XC3042A that are connected to the 100 package pins. Two pads, indicated by double asterisks, do not exist on the XC3030A, which has 98 pads; therefore the corresponding pins have no connections. Twenty-six pads, indicated by single or double asterisks, do not exist on the XC3020A, which has 74 pads; therefore, the corresponding pins have no connections. (See table on [page 326](#).)

XC3000 Series 132-Pin Ceramic and Plastic PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PGA Pin Number	XC3042A XC3064A						
C4	GND	B13	M1-RD	P14	RESET	M3	DOUT-I/O
A1	PWRDN	C11	GND	M11	VCC	P1	CCLK
C3	I/O-TCLKIN	A14	M0-RT	N13	DONE-PG	M4	VCC
B2	I/O	D12	VCC	M12	D7-I/O	L3	GND
B3	I/O	C13	M2-I/O	P13	XTL1-I/O-BCLKIN	M2	A0-WS-I/O
A2	I/O*	B14	HDC-I/O	N12	I/O	N1	A1-CS2-I/O
B4	I/O	C14	I/O	P12	I/O	M1	I/O
C5	I/O	E12	I/O	N11	D6-I/O	K3	I/O
A3	I/O*	D13	I/O	M10	I/O	L2	A2-I/O
A4	I/O	D14	LDC-I/O	P11	I/O*	L1	A3-I/O
B5	I/O	E13	I/O*	N10	I/O	K2	I/O
C6	I/O	F12	I/O	P10	I/O	J3	I/O
A5	I/O	E14	I/O	M9	D5-I/O	K1	A15-I/O
B6	I/O	F13	I/O	N9	CS0-I/O	J2	A4-I/O
A6	I/O	F14	I/O	P9	I/O*	J1	I/O*
B7	I/O	G13	I/O	P8	I/O*	H1	A14-I/O
C7	GND	G14	INIT-I/O	N8	D4-I/O	H2	A5-I/O
C8	VCC	G12	VCC	P7	I/O	H3	GND
A7	I/O	H12	GND	M8	VCC	G3	VCC
B8	I/O	H14	I/O	M7	GND	G2	A13-I/O
A8	I/O	H13	I/O	N7	D3-I/O	G1	A6-I/O
A9	I/O	J14	I/O	P6	CS1-I/O	F1	I/O*
B9	I/O	J13	I/O	N6	I/O*	F2	A12-I/O
C9	I/O	K14	I/O	P5	I/O*	E1	A7-I/O
A10	I/O	J12	I/O	M6	D2-I/O	F3	I/O
B10	I/O	K13	I/O	N5	I/O	E2	I/O
A11	I/O*	L14	I/O*	P4	I/O	D1	A11-I/O
C10	I/O	L13	I/O	P3	I/O	D2	A8-I/O
B11	I/O	K12	I/O	M5	D1-I/O	E3	I/O
A12	I/O*	M14	I/O	N4	RDY/BUSY-RCLK-I/O	C1	I/O
B12	I/O	N14	I/O	P2	I/O	B1	A10-I/O
A13	I/O*	M13	XTL2(IN)-I/O	N3	I/O	C2	A9-I/O
C12	I/O	L12	GND	N2	D0-DIN-I/O	D3	VCC

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

*Indicates unconnected package pins (14) for the XC3042A.

XC3000 Series 144-Pin Plastic TQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin Number	XC3042A XC3064A XC3090A	Pin Number	XC3042A XC3064A XC3090A	Pin Number	XC3042A XC3064A XC3090A
1	PWRDN	49	I/O	97	I/O
2	I/O-TCLKIN	50	I/O*	98	I/O
3	I/O*	51	I/O	99	I/O*
4	I/O	52	I/O	100	I/O
5	I/O	53	INIT-I/O	101	I/O*
6	I/O*	54	VCC	102	D1-I/O
7	I/O	55	GND	103	RDY/BUSY-RCLK-I/O
8	I/O	56	I/O	104	I/O
9	I/O*	57	I/O	105	I/O
10	I/O	58	I/O	106	D0-DIN-I/O
11	I/O	59	I/O	107	DOUT-I/O
12	I/O	60	I/O	108	CCLK
13	I/O	61	I/O	109	VCC
14	I/O	62	I/O	110	GND
15	I/O*	63	I/O*	111	A0-WSI/O
16	I/O	64	I/O*	112	A1-CS2-I/O
17	I/O	65	I/O	113	I/O
18	GND	66	I/O	114	I/O
19	VCC	67	I/O	115	A2-I/O
20	I/O	68	I/O	116	A3-I/O
21	I/O	69	XTL2(IN)-I/O	117	I/O
22	I/O	70	GND	118	I/O
23	I/O	71	RESET	119	A15-I/O
24	I/O	72	VCC	120	A4-I/O
25	I/O	73	DONE-PG	121	I/O*
26	I/O	74	D7-I/O	122	I/O*
27	I/O	75	XTL1(OUT)-BCLKIN-I/O	123	A14-I/O
28	I/O*	76	I/O	124	A5-I/O
29	I/O	77	I/O	125	I/O (XC3090 only)
30	I/O	78	D6-I/O	126	GND
31	I/O*	79	I/O	127	VCC
32	I/O*	80	I/O*	128	A13-I/O
33	I/O	81	I/O	129	A6-I/O
34	I/O*	82	I/O	130	I/O*
35	I/O	83	I/O*	131	I/O (XC3090 only)
36	M1-RD	84	D5-I/O	132	I/O*
37	GND	85	CS0-I/O	133	A12-I/O
38	MO-RT	86	I/O*	134	A7-I/O
39	VCC	87	I/O*	135	I/O
40	M2-I/O	88	D4-I/O	136	I/O
41	HDC-I/O	89	I/O	137	A11-I/O
42	I/O	90	VCC	138	A8-I/O
43	I/O	91	GND	139	I/O
44	I/O	92	D3-I/O	140	I/O
45	LDC-I/O	93	CS1-I/O	141	A10-I/O
46	I/O*	94	I/O*	142	A9-I/O
47	I/O	95	I/O*	143	VCC
48	I/O	96	D2-I/O	144	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* Indicates unconnected package pins (24) for the XC3042A.

XC3000 Series 160-Pin PQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PQFP Pin Number	XC3064A, XC3090A, XC3195A	PQFP Pin Number	XC3064A, XC3090A, XC3195A	PQFP Pin Number	XC3064A, XC3090A, XC3195A	PQFP Pin Number	XC3064A, XC3090A, XC3195A
1	I/O*	41	GND	81	D7-I/O	121	CCLK
2	I/O	42	M0-RTRIG	82	XTL1-I/O-BCLKIN	122	VCC
3	I/O	43	VCC	83	I/O*	123	GND
4	I/O	44	M2-I/O	84	I/O	124	A0-WS-I/O
5	I/O	45	HDC-I/O	85	I/O	125	A1-CS2-I/O
6	I/O	46	I/O	86	D6-I/O	126	I/O
7	I/O	47	I/O	87	I/O	127	I/O
8	I/O	48	I/O	88	I/O	128	A2-I/O
9	I/O	49	$\overline{\text{LDC}}$ -I/O	89	I/O	129	A3-I/O
10	I/O	50	I/O*	90	I/O	130	I/O
11	I/O	51	I/O*	91	I/O	131	I/O
12	I/O	52	I/O	92	D5-I/O	132	A15-I/O
13	I/O	53	I/O	93	CS0-I/O	133	A4-I/O
14	I/O	54	I/O	94	I/O*	134	I/O
15	I/O	55	I/O	95	I/O*	135	I/O
16	I/O	56	I/O	96	I/O	136	A14-I/O
17	I/O	57	I/O	97	I/O	137	A5-I/O
18	I/O	58	I/O	98	D4-I/O	138	I/O*
19	GND	59	INIT-I/O	99	I/O	139	GND
20	VCC	60	VCC	100	VCC	140	VCC
21	I/O*	61	GND	101	GND	141	A13-I/O
22	I/O	62	I/O	102	D3-I/O	142	A6-I/O
23	I/O	63	I/O	103	CS1-I/O	143	I/O*
24	I/O	64	I/O	104	I/O	144	I/O*
25	I/O	65	I/O	105	I/O	145	I/O
26	I/O	66	I/O	106	I/O*	146	I/O
27	I/O	67	I/O	107	I/O*	147	A12-I/O
28	I/O	68	I/O	108	D2-I/O	148	A7-I/O
29	I/O	69	I/O	109	I/O	149	I/O
30	I/O	70	I/O	110	I/O	150	I/O
31	I/O	71	I/O	111	I/O	151	A11-I/O
32	I/O	72	I/O	112	I/O	152	A8-I/O
33	I/O	73	I/O	113	I/O	153	I/O
34	I/O	74	I/O	114	D1-I/O	154	I/O
35	I/O	75	I/O*	115	RDY/BUSY-RCLK-I/O	155	A10-I/O
36	I/O	76	XTL2-I/O	116	I/O	156	A9-I/O
37	I/O	77	GND	117	I/O	157	VCC
38	I/O*	78	RESET	118	I/O*	158	GND
39	I/O*	79	VCC	119	D0-DIN-I/O	159	PWRDWN
40	M1-RDATA	80	DONE/PG	120	DOUT-I/O	160	TCLKIN-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed IOBs are default slew-rate limited.

*Indicates unconnected package pins (18) for the XC3064A.

XC3000 Series 175-Pin Ceramic and Plastic PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PGA Pin Number	XC3090A, XC3195A	PGA Pin Number	XC3090A, XC3195A	PGA Pin Number	XC3090A, XC3195A	PGA Pin Number	XC3090A, XC3195A
B2	PWRDN	D13	I/O	R14	DONE-PG	N4	DOUT-I/O
D4	TCLKIN-I/O	B14	M1-RDATA	N13	D7-I/O	R2	CCLK
B3	I/O	C14	GND	T14	XTL1(OUT)-BCLKIN-I/O	P3	VCC
C4	I/O	B15	M0-RTRIG	P13	I/O	N3	GND
B4	I/O	D14	VCC	R13	I/O	P2	A0-WS-I/O
A4	I/O	C15	M2-I/O	T13	I/O	M3	A1-CS2-I/O
D5	I/O	E14	HDC-I/O	N12	I/O	R1	I/O
C5	I/O	B16	I/O	P12	D6-I/O	N2	I/O
B5	I/O	D15	I/O	R12	I/O	P1	A2-I/O
A5	I/O	C16	I/O	T12	I/O	N1	A3-I/O
C6	I/O	D16	LDC-I/O	P11	I/O	L3	I/O
D6	I/O	F14	I/O	N11	I/O	M2	I/O
B6	I/O	E15	I/O	R11	I/O	M1	A15-I/O
A6	I/O	E16	I/O	T11	D5-I/O	L2	A4-I/O
B7	I/O	F15	I/O	R10	CS0-I/O	L1	I/O
C7	I/O	F16	I/O	P10	I/O	K3	I/O
D7	I/O	G14	I/O	N10	I/O	K2	A14-I/O
A7	I/O	G15	I/O	T10	I/O	K1	A5-I/O
A8	I/O	G16	I/O	T9	I/O	J1	I/O
B8	I/O	H16	I/O	R9	D4-I/O	J2	I/O
C8	I/O	H15	INIT-I/O	P9	I/O	J3	GND
D8	GND	H14	VCC	N9	VCC	H3	VCC
D9	VCC	J14	GND	N8	GND	H2	A13-I/O
C9	I/O	J15	I/O	P8	D3-I/O	H1	A6-I/O
B9	I/O	J16	I/O	R8	CS1-I/O	G1	I/O
A9	I/O	K16	I/O	T8	I/O	G2	I/O
A10	I/O	K15	I/O	T7	I/O	G3	I/O
D10	I/O	K14	I/O	N7	I/O	F1	I/O
C10	I/O	L16	I/O	P7	I/O	F2	A12-I/O
B10	I/O	L15	I/O	R7	D2-I/O	E1	A7-I/O
A11	I/O	M16	I/O	T6	I/O	E2	I/O
B11	I/O	M15	I/O	R6	I/O	F3	I/O
D11	I/O	L14	I/O	N6	I/O	D1	A11-I/O
C11	I/O	N16	I/O	P6	I/O	C1	A8-I/O
A12	I/O	P16	I/O	T5	I/O	D2	I/O
B12	I/O	N15	I/O	R5	D1-I/O	B1	I/O
C12	I/O	R16	I/O	P5	RDY/BUSY-RCLK-I/O	E3	A10-I/O
D12	I/O	M14	I/O	N5	I/O	C2	A9-I/O
A13	I/O	P15	XTL2(IN)-I/O	T4	I/O	D3	VCC
B13	I/O	N14	GND	R4	I/O	C3	GND
C13	I/O	R15	RESET	P4	I/O		
A14	I/O	P14	VCC	R3	D0-DIN-I/O		

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

Pins A2, A3, A15, A16, T1, T2, T3, T15 and T16 are not connected. Pin A1 does not exist.

XC3000 Series 176-Pin TQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin Number	XC3090A	Pin Number	XC3090A	Pin Number	XC3090A	Pin Number	XC3090A
1	PWRDWN	45	M1-RDATA	89	DONE-PG	133	VCC
2	TCLKIN-I/O	46	GND	90	D7-I/O	134	GND
3	I/O	47	M0-RTRIG	91	XTAL1(OUT)-BCLKIN-I/O	135	A0-WS-I/O
4	I/O	48	VCC	92	I/O	136	A1-CS2-I/O
5	I/O	49	M2-I/O	93	I/O	137	–
6	I/O	50	HDC-I/O	94	I/O	138	I/O
7	I/O	51	I/O	95	I/O	139	I/O
8	I/O	52	I/O	96	D6-I/O	140	A2-I/O
9	I/O	53	I/O	97	I/O	141	A3-I/O
10	I/O	54	LDC-I/O	98	I/O	142	–
11	I/O	55	–	99	I/O	143	–
12	I/O	56	I/O	100	I/O	144	I/O
13	I/O	57	I/O	101	I/O	145	I/O
14	I/O	58	I/O	102	D5-I/O	146	A15-I/O
15	I/O	59	I/O	103	CS0-I/O	147	A4-I/O
16	I/O	60	I/O	104	I/O	148	I/O
17	I/O	61	I/O	105	I/O	149	I/O
18	I/O	62	I/O	106	I/O	150	A14-I/O
19	I/O	63	I/O	107	I/O	151	A5-I/O
20	I/O	64	I/O	108	D4-I/O	152	I/O
21	I/O	65	INIT-I/O	109	I/O	153	I/O
22	GND	66	VCC	110	VCC	154	GND
23	VCC	67	GND	111	GND	155	VCC
24	I/O	68	I/O	112	D3-I/O	156	A13-I/O
25	I/O	69	I/O	113	CS1-I/O	157	A6-I/O
26	I/O	70	I/O	114	I/O	158	I/O
27	I/O	71	I/O	115	I/O	159	I/O
28	I/O	72	I/O	116	I/O	160	–
29	I/O	73	I/O	117	I/O	161	–
30	I/O	74	I/O	118	D2-I/O	162	I/O
31	I/O	75	I/O	119	I/O	163	I/O
32	I/O	76	I/O	120	I/O	164	A12-I/O
33	I/O	77	I/O	121	I/O	165	A7-I/O
34	I/O	78	I/O	122	I/O	166	I/O
35	I/O	79	I/O	123	I/O	167	I/O
36	I/O	80	I/O	124	D1-I/O	168	–
37	I/O	81	I/O	125	RDY/BUSY-RCLK-I/O	169	A11-I/O
38	I/O	82	–	126	I/O	170	A8-I/O
39	I/O	83	–	127	I/O	171	I/O
40	I/O	84	I/O	128	I/O	172	I/O
41	I/O	85	XTAL2(IN)-I/O	129	I/O	173	A10-I/O
42	I/O	86	GND	130	D0-DIN-I/O	174	A9-I/O
43	I/O	87	RESET	131	DOUT-I/O	175	VCC
44	–	88	VCC	132	CCLK	176	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

XC3000 Series 208-Pin PQFP Pinouts

XC3000A, and XC3000L families have identical pinouts

Pin Number	XC3090A	Pin Number	XC3090A	Pin Number	XC3090A	Pin Number	XC3090A
1	–	53	–	105	–	157	–
2	GND	54	–	106	VCC	158	–
3	PWRDWN	55	VCC	107	D/P	159	–
4	TCLKIN-I/O	56	M2-I/O	108	–	160	GND
5	I/O	57	HDC-I/O	109	D7-I/O	161	WS-A0-I/O
6	I/O	58	I/O	110	XTL1-BCLKIN-I/O	162	CS2-A1-I/O
7	I/O	59	I/O	111	I/O	163	I/O
8	I/O	60	I/O	112	I/O	164	I/O
9	I/O	61	LDC-I/O	113	I/O	165	A2-I/O
10	I/O	62	I/O	114	I/O	166	A3-I/O
11	I/O	63	I/O	115	D6-I/O	167	I/O
12	I/O	64	–	116	I/O	168	I/O
13	I/O	65	–	117	I/O	169	–
14	I/O	66	–	118	I/O	170	–
15	–	67	–	119	–	171	–
16	I/O	68	I/O	120	I/O	172	A15-I/O
17	I/O	69	I/O	121	I/O	173	A4-I/O
18	I/O	70	I/O	122	D5-I/O	174	I/O
19	I/O	71	I/O	123	CS0-I/O	175	I/O
20	I/O	72	–	124	I/O	176	–
21	I/O	73	–	125	I/O	177	–
22	I/O	74	I/O	126	I/O	178	A14-I/O
23	I/O	75	I/O	127	I/O	179	A5-I/O
24	I/O	76	I/O	128	D4-I/O	180	I/O
25	GND	77	INIT-I/O	129	I/O	181	I/O
26	VCC	78	VCC	130	VCC	182	GND
27	I/O	79	GND	131	GND	183	VCC
28	I/O	80	I/O	132	D3-I/O	184	A13-I/O
29	I/O	81	I/O	133	CS1-I/O	185	A6-I/O
30	I/O	82	I/O	134	I/O	186	I/O
31	I/O	83	–	135	I/O	187	I/O
32	I/O	84	–	136	I/O	188	–
33	I/O	85	I/O	137	I/O	189	–
34	I/O	86	I/O	138	D2-I/O	190	I/O
35	I/O	87	I/O	139	I/O	191	I/O
36	I/O	88	I/O	140	I/O	192	A12-I/O
37	–	89	I/O	141	I/O	193	A7-I/O
38	I/O	90	–	142	–	194	–
39	I/O	91	–	143	I/O	195	–
40	I/O	92	–	144	I/O	196	–
41	I/O	93	I/O	145	D1-I/O	197	I/O
42	I/O	94	I/O	146	RDY/BUSY-RCLK-I/O	198	I/O
43	I/O	95	I/O	147	I/O	199	A11-I/O
44	I/O	96	I/O	148	I/O	200	A8-I/O
45	I/O	97	I/O	149	I/O	201	I/O
46	I/O	98	I/O	150	I/O	202	I/O
47	I/O	99	I/O	151	DIN-D0-I/O	203	A10-I/O
48	M1-RDATA	100	XTL2-I/O	152	DOUT-I/O	204	A9-I/O
49	GND	101	GND	153	CCLK	205	VCC
50	M0-RTRIG	102	RESET	154	VCC	206	–
51	–	103	–	155	–	207	–
52	–	104	–	156	–	208	–

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

*In PQ208, XC3090A and XC3195A have different pinouts.

XC3195A PQ208 and PG223 Pinouts

Pin Description	PG223	PQ208	Pin Description	PG223	PQ208	Pin Description	PG223	PQ208	Pin Description	PG223	PQ208
A9-I/O	B1	206	D0-DIN-I/O	U3	154	I/O	U18	102	I/O	A16	48
A10-I/O	E3	205	I/O	V3	153	I/O	P15	101	I/O	D14	47
I/O	E4	204	I/O	R5	152	I/O	T17	100	I/O	C15	46
I/O	C2	203	I/O	T4	151	I/O	T18	99	I/O	B15	45
I/O	C1	202	I/O	V4	150	I/O	P16	98	I/O	A15	44
I/O	D2	201	RDY/BUSY-RCLK-I/O	U4	149	I/O	R17	97	I/O	C14	43
A8-I/O	E2	200	D1-I/O	U5	148	I/O	N15	96	I/O	D13	42
A11-I/O	F4	199	I/O	R6	147	I/O	R18	95	I/O	B14	41
I/O	F3	198	I/O	T5	146	I/O	P17	94	I/O	C13	40
I/O	D1	197	I/O	U6	145	I/O	N17	93	I/O	B13	39
I/O	F2	196	I/O	T6	144	I/O	N16	92	I/O	B12	38
I/O	G2	194	I/O	V7	141	I/O	M15	89	I/O	D12	37
A7-I/O	G4	193	I/O	R7	140	I/O	M18	88	I/O	A12	36
A12-I/O	G1	192	I/O	U7	139	I/O	M17	87	I/O	B11	35
I/O	H2	191	D2-I/O	V8	138	I/O	L18	86	I/O	C11	34
I/O	H3	190	I/O	U8	137	I/O	L17	85	I/O	A11	33
I/O	H1	189	I/O	T8	136	I/O	L15	84	I/O	D11	32
I/O	H4	188	I/O	R8	135	I/O	L16	83	I/O	A10	31
I/O	J3	187	I/O	V9	134	I/O	K18	82	I/O	B10	30
I/O	J2	186	CS1-I/O	U9	133	I/O	K17	81	I/O	C10	29
A6-I/O	J1	185	D3-I/O	T9	132	I/O	K16	80	I/O	C9	28
A13-I/O	K3	184	GND	R9	131	GND	K15	79	VCC	D10	27
VCC	J4	183	VCC	R10	130	VCC	J15	78	GND	D9	26
GND	K4	182	I/O	T10	129	INIT	J16	77	I/O	B9	25
I/O	K2	181	D4-I/O	U10	128	I/O	J17	76	I/O	A9	24
I/O	K1	180	I/O	V10	127	I/O	J18	75	I/O	C8	23
A5-I/O	L2	179	I/O	R11	126	I/O	H16	74	I/O	D8	22
A14-I/O	L4	178	I/O	T11	125	I/O	H15	73	I/O	B8	21
I/O	L3	177	I/O	U11	124	I/O	H17	72	I/O	A8	20
I/O	L1	176	CS0-I/O	V11	123	I/O	H18	71	I/O	B7	19
I/O	M1	175	D5-I/O	U12	122	I/O	G17	70	I/O	A7	18
I/O	M2	174	I/O	R12	121	I/O	G18	69	I/O	D7	17
A4-I/O	M4	173	I/O	V12	120	I/O	G15	68	I/O	B6	14
A15-I/O	N2	172	I/O	T13	119	I/O	F16	67	I/O	C6	13
I/O	N3	171	I/O	U13	118	I/O	F17	66	I/O	B5	12
I/O	P2	169	I/O	T14	117	I/O	E17	63	I/O	A4	11
I/O	R1	168	I/O	R13	116	I/O	C18	62	I/O	D6	10
I/O	N4	167	I/O	U14	115	I/O	F15	61	I/O	C5	9
A3-I/O	T1	166	D6-I/O	U15	114	I/O	D17	60	I/O	B4	8
A2-I/O	R2	165	I/O	V15	113	LDC-I/O	E16	59	I/O	B3	7
I/O	P3	164	I/O	T15	112	I/O	C17	58	I/O	C4	6
I/O	T2	163	I/O	R14	111	I/O	B18	57	I/O	D5	5
I/O	P4	162	I/O	V16	110	I/O	E15	56	I/O	C3	4
I/O	U1	161	XTLX1(OUT)BCLKN-I/O	U16	109	HDC-I/O	A18	55	I/O	A3	3
A1-CS2-I/O	V1	160	D7-I/O	T16	108	M2-I/O	A17	54	TCLKIN-I/O	A2	2
A0-WS-I/O	T3	159	D/P	V17	107	VCC	D16	53	PWRDN	B2	1
GND	R3	158	VCC	R15	106	M0-RTIG	B17	52	GND	D4	208
VCC	R4	157	RESET	U17	105	GND	D15	51	VCC	D3	207
CCLK	U2	156	GND	R16	104	M1/RDATA	C16	50			
DOUT-I/O	V2	155	XTL2(IN)-I/O	V18	103	I/O	B16	49			

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

In the PQ208 package, pins 15, 16, 64, 65, 90, 91, 142, 143, 170 and 195 are not connected.

In the PG223 package, the following pins are not connected: A5, A6, A13, A14, D18, E1, E18, F1, F18, N1, N18, P1, P18, V5, V6, V13, and V14.

*In PQ208, XC3090A and XC3195A have different pinouts.

Product Availability

Pins		44	64	68	84		100				132		144	160	164	175		176	208	223	
Type		Plast. PLCC	Plast. VQFP	Plast. PLCC	Plast. PLCC	Cer. PGA	Plast. P QFP	Plast. TQFP	Plast. VQFP	Top-Brazed CQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Top-Brazed CQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Cer. PGA	
Code		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100	PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223	
XC3020A	-7			CI	CI	CI	CI														
	-6			C	C	C	C														
XC3030A	-7	CI	CI	CI	CI	CI	CI		CI												
	-6	C	C	C	C	C	C		C												
XC3042A	-7				CI	CI	CI		CI		CI	CI	CI								
	-6				C	C	C		C		C	C	C								
XC3064A	-7				CI						CI	CI	CI	CI							
	-6				C						C	C	C	C							
XC3090A	-7				CI								CI	CI			CI	CI	CI	CI	
	-6				C								C	C		C	C	C	C	C	
XC3020L	-8				C																
XC3030L	-8		C		C				C												
XC3042L	-8				C				C				C								
XC3064L	-8				C								C								
XC3090L	-8				C								C						C		
XC3120A	-5			CI	CI	CI	CI														
	-4			CI	CI	CI	CI														
	-3			CI	CI	CI	CI														
	-2			CI	CI	CI	CI														
	-1			C	C	C	C														
	-09			C	C	C	C														
XC3130A	-5	CI	CI	CI	CI	CI	CI		CI												
	-4	CI	CI	CI	CI	CI	CI		CI												
	-3	CI	CI	CI	CI	CI	CI		CI												
	-2	CI	CI	CI	CI	CI	CI		CI												
	-1	C	C	C	C	C	C		C												
	-09	C	C	C	C	C	C		C												
XC3142A	-5				CI	CIMB	CI		C	MB	C	CIMB	CI								
	-4				CI	CI	CI		C		C	CI	CI								
	-3				CI	CI	CI		CI		CI	CI	CI								
	-2				CI	CI	CI		CI		CI	CI	CI								
	-1				C	C	C		C		C	C	C								
	-09				C	C	C		C		C	C	C								
XC3164A	-5				CI						CI	CI	CI	CI							
	-4				CI						CI	CI	CI	CI							
	-3				CI						CI	CI	CI	CI							
	-2				CI						CI	CI	CI	CI							
	-1				C						C	C	C	C							
	-09				C						C	C	C	C							
XC3190A	-5				CI									CI	MB	CI	CIMB	CI	CI	CI	
	-4				CI									CI		CI	CI	CI	CI	CI	
	-3				CI									CI		CI	CI	CI	CI	CI	
	-2				CI									CI		CI	CI	CI	CI	CI	
	-1				C									C		C	C	C	C	C	
	-09				C									C		C	C	C	C	C	
XC3195A	-5				CI									CI	MB	CI	CIMB			CI	CIMB
	-4				CI									CI		CI	CI			CI	CI
	-3				CI									CI		CI	CI			CI	CI
	-2				CI									CI		CI	CI			CI	CI
	-1				C									C		C	C			C	C
	-09				C									C		C	C			C	C

Pins		44	64	68	84		100				132		144	160	164	175		176	208	223	
Type		Plast. PLCC	Plast. VQFP	Plast. PLCC	Plast. PLCC	Cer. PGA	Plast.P QFP	Plast. TQFP	Plast. VQFP	Top-Brazed CQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Top-Brazed CQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Cer. PGA	
Code		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100	PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223	
XC3142L	-3*				C				C				C								
	-2*				C				C				C								
XC3190L	-3*				C								C						C		
	-2*				C								C						C		

Notes: * Advance Information

C = Commercial, T_J = 0° to +85°C

I = Industrial, T_J = -40° to +100°C

M = Military Temp, T_C = -55° to +125°C

B = MIL-STD-883C Class B

Ordering Information

Example: XC3030A-3 PC44C

