

Xcell journal

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SOLUTIONS FOR A PROGRAMMABLE WORLD

4G Wireless Networks Poised for Multimode Flexibility

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Designs for Biomedical
Applications

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Solving FPGA I/O Pin
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Replacing Obsolete
Video Game Circuits
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Xcell to New Heights

Xcell Wants You!

Welcome to the new version of *Xcell Journal*. I'm Mike Santarini, *Xcell's* new publisher. I joined Xilinx in March of this year after working 13 years as an editor covering the EDA, FPGA, ASIC, IP, and memory industries for EE trade publications *EDN*, *EE Times*, and *Integrated System Design*.

I've dedicated my entire professional career to keeping the IC and systems design communities informed of new design developments and challenges. Now I'm bringing that mission to the ever-expanding Xilinx® user community. When Xilinx approached me for this job, I jumped at the chance.

Over the last 25 years, FPGAs have evolved from their glue logic beginnings to become a fundamental element of just about every digital design project. Indeed, today FPGAs boast multi-million-gate counts, MPUs, DSPs, and embedded functionality, and are starting to play a more central role in the world's most advanced products.

Even if FPGAs are not in your end product, chances are you've used at least one FPGA to develop that product. And what's beautiful about FPGAs – and at the same time a bit daunting – is their versatility. You can use them for any number of applications, but perhaps what's under-marketed is the “field-programmable” part of FPGAs. Yes, FPGAs are reprogrammable, meaning that you can change your design in the lab and even reuse the chips for other design projects. But you can also change the logic of your design in the field – after you've deployed your product.

The “FP” makes FPGAs the building blocks, Erector Set, Legos, ball of clay – you pick the analogy – of electronic design. We provide the renewable canvas (silicon) and the brushes and paint (tools and IP); you create the masterpieces. And as an editor walking through your gallery for the last 14 years, what beautiful, diverse and wonderful works of art you are creating. You are literally changing the world.

In my role as publisher here at *Xcell Journal*, I want to help you develop those masterpieces by keeping you informed of what the extremely hard-working folks at Xilinx are developing and what your peers are doing as well.

As you give this issue a read, you'll notice a number of new sections and a broad range of content, reflecting FPGA versatility. You'll notice that each issue contains a cover story examining the high-level challenges of a given application area. From there, the content becomes progressively more technical: from application articles that will appear in regularly featured sections, to how-to articles, to walkthroughs from our FAE staff. And to break it up a bit, we'll also profile one of our customers and take a look at new tool, IP, and board offerings from our growing list of partners.

This issue is a first of many steps to make *Xcell Journal* a technical Xilinx user community magazine. To reach its true potential, *Xcell Journal* needs your help; I encourage all of you to submit articles. Even if you are a bit pen-shy, I'll work with you to get your content in the magazine and out to your peers.

I hope you enjoy reading this issue of *Xcell* – a lot of people worked very hard to make this publication what it is. I'm hoping you will also pitch in to help it become what it can be. Please feel free to send me your articles and feedback to make *Xcell* excel to new heights.



Mike Santarini
Publisher

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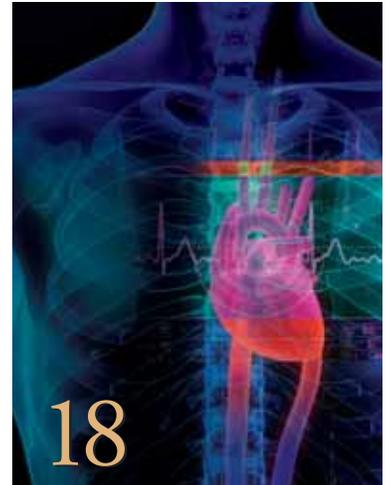
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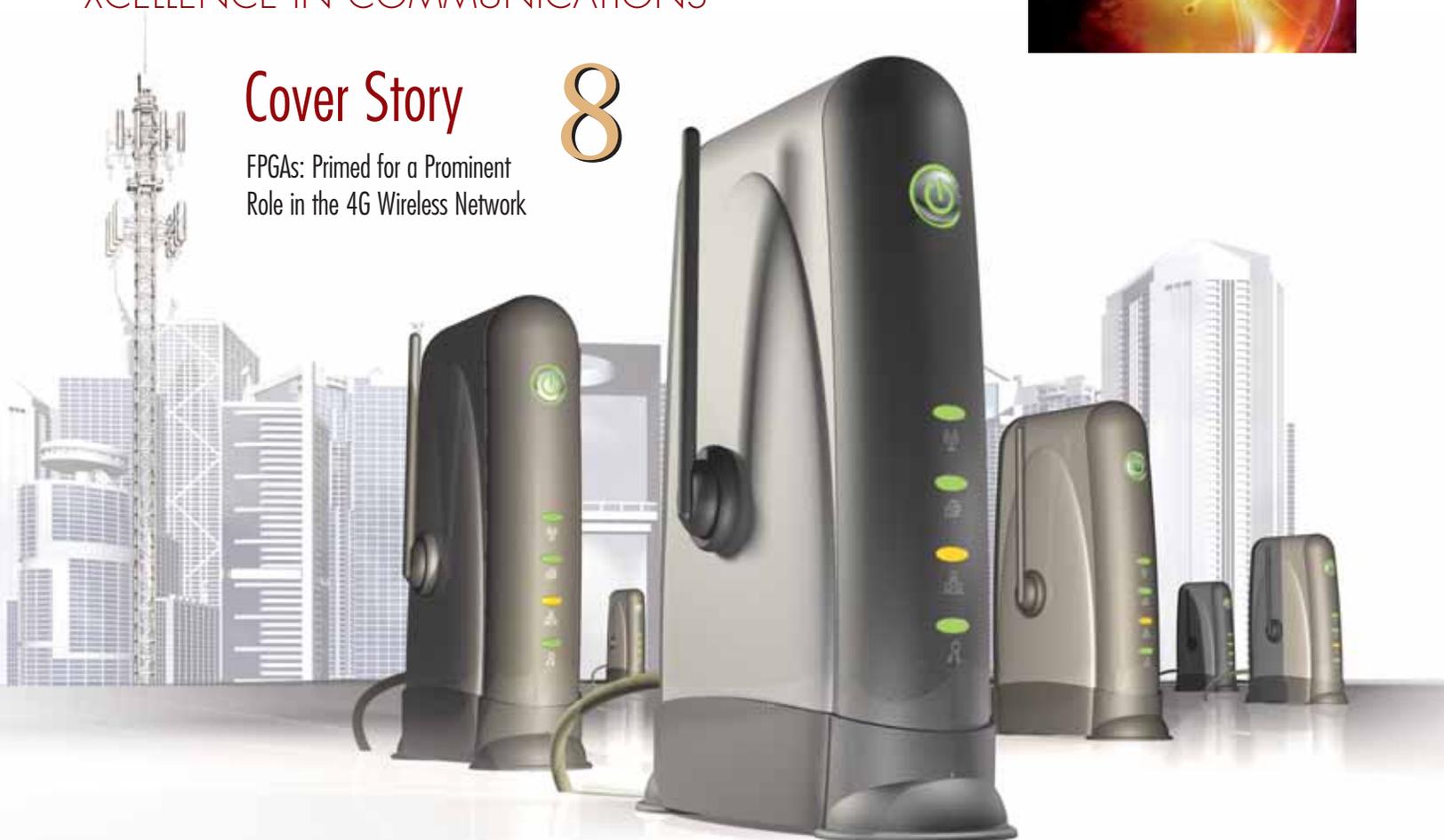


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FPGAs: Primed for a Prominent Role in the 4G Wireless Network



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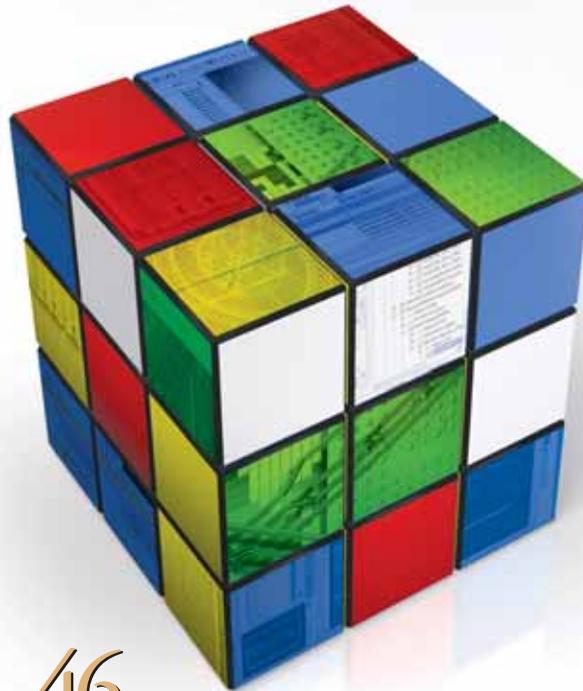
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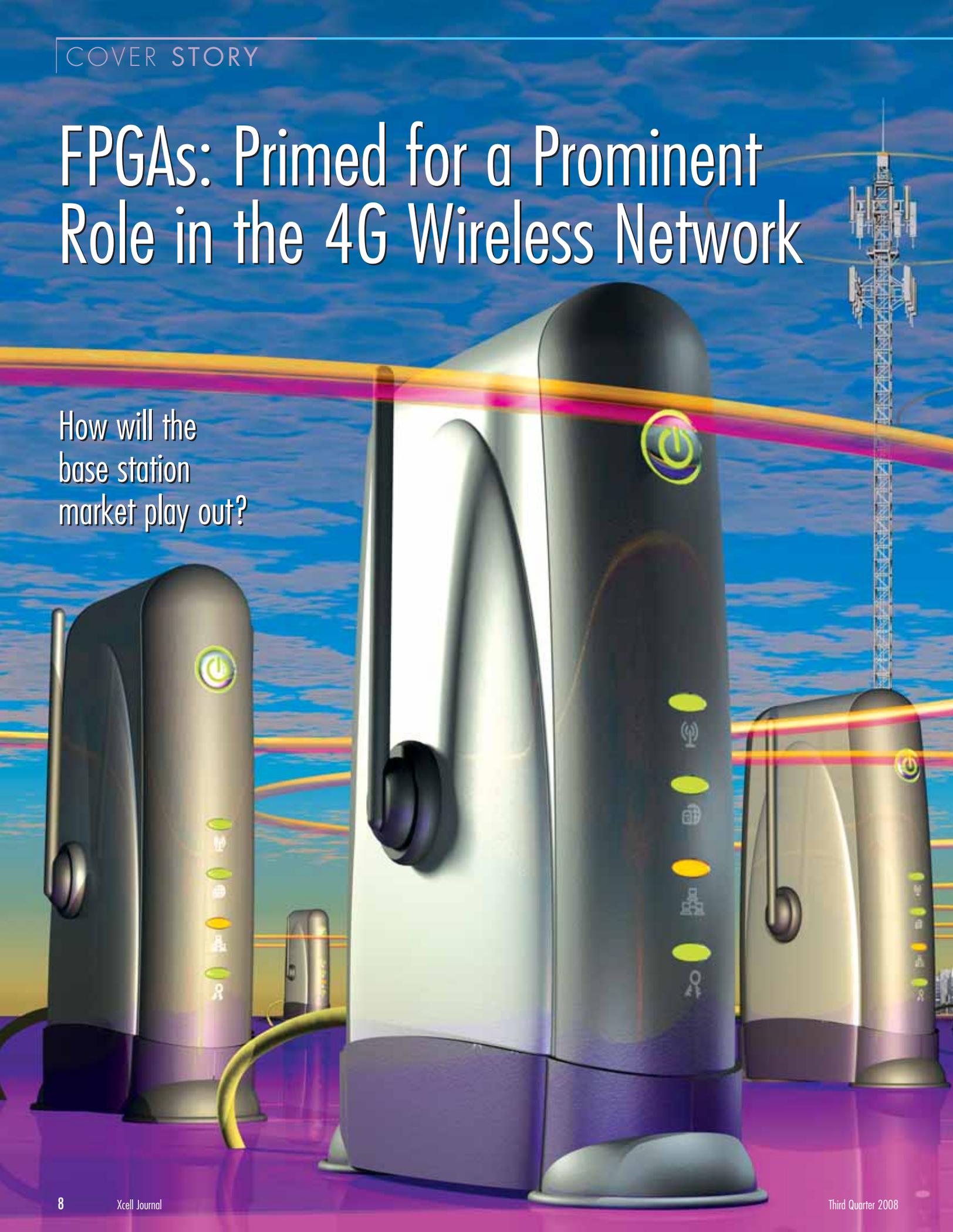
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FPGAs: Primed for a Prominent Role in the 4G Wireless Network

How will the base station market play out?



by Mike Santarini
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The impending convergence of third-generation (3G) CDMA2000 and WCDMA/GSM wireless network standards into the 4G LTE (Long Term Evolution) wireless network standard presents developers of next-generation base stations with a bit of a challenge. How do you create a next-generation base station that will support current 3G communication standards as well as next-generation standards, and perhaps go the extra mile to outpace your competition and offer a solution that can accommodate whatever successive standard(s) the communications industry picks after LTE?

Stepping up to this challenge, many design groups are now in the process of creating multimode (also known as multi-standard) base stations that will support 3G and 4G standards – perhaps multiple variants of these standards – while being flexible enough to adapt to any changes that may arise in the design specifications or even the wireless standards the design targets. Many are giving FPGAs a more central role in multimode base station design (see Figure 1).

The Promise of 4G: LTE and WiMAX

LTE promises to bring wireless customers data rates of 100 Mbps or higher, which is a 10x improvement in performance over current 3G networks. This data-rate increase paves the way for carriers and mobile handset makers to offer customers more advanced features on their respective networks and mobile devices, such as mobile TV, advanced video, and even gaming in addition to Internet, e-mail, and voice.

This means that mobile device makers will be able to sell more advanced phones to carriers, while carriers will be able to offer more expensive mobile phone plans and increase their average revenue per user (ARPU).

But of course, carriers must install a wireless network infrastructure before all that can happen.

Currently, 70% of the world uses GSM-based networks (in particular 3G WCDMA), while North America and

South Korea primarily use 3G CDMA2000 networks. Carriers in Japan are scheduled to conduct a trial run later this year of the Orthogonal Frequency Division Multiple Access (OFDM) modulation scheme underlying LTE, essentially kicking off LTE adoption.

Manuel Uhm, senior marketing manager for the Wireless business at Xilinx, notes that carriers currently employing CDMA2000 networks will likely move to LTE as well, because Qualcomm's proposal for a follow-on to CDMA2000, UMB, didn't gain industry support.

Indeed, one of those CDMA2000 carriers, Verizon, recently announced that it will be installing LTE in the 700-MHz spectrum in North America. It recently won the 700-MHz spectrum in a Federal Communications Commission auction.

Still, the industry doesn't expect LTE to be in large-scale deployment until the 2012 time frame, so many wireless carriers shopping for next-generation base stations will be looking for hardware that will allow them to offer customers support for their current networks while providing an upgrade path to a faster 4G wireless network. Simultaneously, they will want to minimize the operational expenses of each system and the entire network, including reducing the base station power and thus utility costs.

Although CDMA2000 and WCDMA seem likely to converge on LTE, it's uncertain whether the rest of the world will also adopt LTE networks. Carriers in some countries are embracing data-centric networks such as WiMAX and WiBro (South Korea), which carriers can enhance to carry voice over packet. WiMAX and WiBro will compete with LTE.

But Loring Wirbel, director of *EE Times'* market intelligence unit and longtime communications editor, points out that LTE and WiMAX standards are very similar – reportedly 80% percent of the baseband functionality is the same – which opens the door for base station vendors to attempt to build one base station that can support 4G standards while still supporting legacy 3G networks.

But even if the world converges on LTE, it isn't likely to be the last network carriers

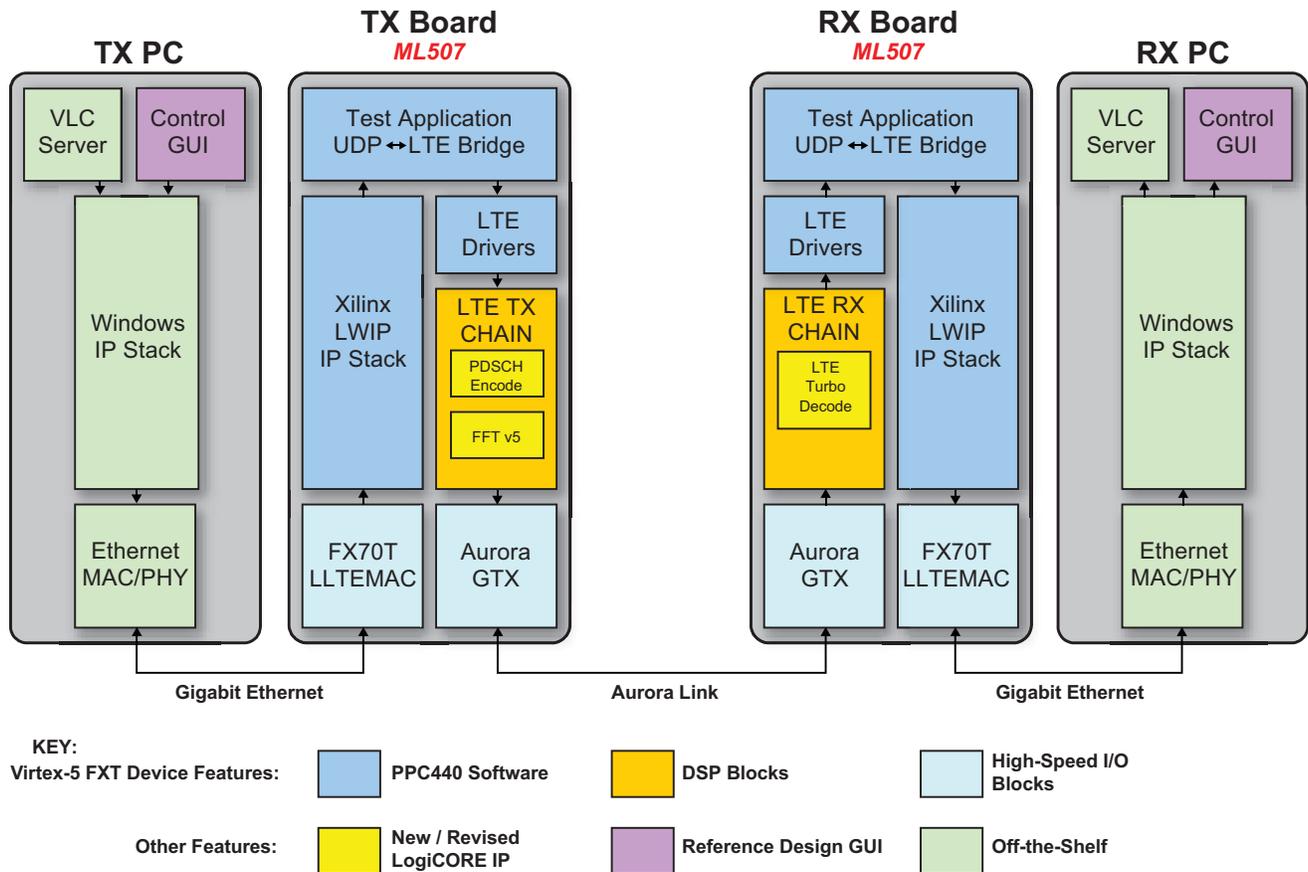


Figure 1 – Xilinx LTE baseband reference design

install. “WCDMA was supposed to be the convergence of air interface standards, but that wasn’t the case,” Uhm noted.

Indeed, if history is any indication of future behavior, it likely means that as soon as LTE gets established, some new need – be it network performance, new functionality/services, or even something political – will spur the need for a 5G solution, or perhaps an intermittent tweak to extend the life of LTE.

In fact, the industry is already laying the groundwork for 5G networks such as LTE advanced, even though the 3GPP (the international body that defines GSM network standards, including LTE) hasn’t fully completed its definition of LTE, and the industry is only starting to roll out LTE equipment.

This uncertainty – which network will be best, what standard will really materialize (and in what form), and what new

applications will it need to support – has to make carriers a bit more apt to hedge their bets and lean toward systems that are more adaptable, more expandable, and easily and ultimately less expensively modified to suit changes in 4G standards. In short, next-generation base stations need to be flexible, though to what degree is debatable.

Undefined Standards and Multimode Opportunity

Because the 3GPP has yet to fully define the standard, companies building base stations today, especially those trying to be first to market, must build flexibility into their designs. The question is: how much flexibility?

Traditionally, flexibility has come in the form of sending out maintenance crews to replace entire cards in each base station and then tweaking the software running on

those cards. But carriers shopping for 4G are looking for a greater degree of flexibility.

Indeed, wireless network standards (and wireless networks for that matter) comprise two fundamental layers: hardware (PHY) and software. The PHY layer, or physical layer, defines the performance and functionality requirements of the hardware the network will need to support the standard. The software layer defines the functionality that various software applications will need in order to adhere to the basic network standard.

Carriers can add software and even enhanced hardware (above and beyond the basic PHY and software requirements of the standard) to woo customers to their particular network. But with 4G, many believe base stations need to be more flexible than ever.

Some are anticipating that this will be the era where the industry produces the Holy Grail in base station technology: soft-

[uncertainty] has to make carriers a bit more apt to hedge their bets and lean toward systems that are more adaptable, more expandable, and easily and ultimately less expensively modified to suit changes in 4G standards. In short, next-generation base stations need to be flexible...

ware defined radio (SDR), in which one system can support every standard simply by software reprogramming the base station hardware on the fly to adapt to any incoming signals.

Wirbel noted that in the dawning of the 3G era, several startups offered specialty chips with programmable logic cores and hard-wired high-performance blocks. These devices, however, “were insanely hard to program and insanely expensive.” SDR has yet to fully deliver on its Holy Grail vision, but some vendors are starting to produce innovative SDR subsystems using commercial FPGAs. Perhaps sometime in the near future those subsystems will debut in base stations.

Still, some analysts (Wirbel among them) are not easily convinced that next-generation base stations will truly be as expandable and as multimode as many developers in the market predict (or hope).

“4G promises to make life easier than 3G, because what they want to do is harmonize WiMAX and LTE into one set of standards that both support OFDM. Then it’s just a little software shim as to whether it supports WiMAX or LTE at the end of the day,” Wirbel said. “At the same time, they have to support all of the RF chains and baseband issues for GSM and CDMA2000. At some point, you’ve got to make decisions about what to support or your base station becomes too complex.”

“What happens in the RF component is just as important as the baseband. It’s not the glamour part necessarily,” said Gabriel Brown, Heavy Reading’s senior analyst, who specializes in the wireless market. “You could in theory have multimode, upgradable baseband, but it doesn’t really do you any good if you don’t have the whole RF chain with either the right power output or bandwidth or frequency. Quite often you don’t; this point gets glossed over quite often.

“Yes, it’s software and it is upgradable, but you need to have the RF chain to support it. When folks typically say things are upgradable, they usually mean that it’s upgradable within the same technology stream. For example, you can upgrade from WCDMA to HSPA to HSPA+ on the same baseband hardware by upgrading the software. But the idea of jumping from generations of technologies with different modulations is a bit of nirvana – it isn’t really how things work.”

Battle at the Heart of the Base Station

At the heart of a base station’s hardware is a series of electronic systems that control much of the wireless network functions. Traditionally, these systems have mainly comprised ASICs/ASSPs and standard products such as DSPs. But those technologies are limited in how design groups can modify them to suit late changes in standards or even upgrade the hardware in the field.

Therefore, as base station vendors begin designing 4G base stations that must support the as-yet-not-fully defined LTE standard while also supporting 3G networks, they are increasingly giving FPGA technology a more prominent role in controlling those systems.

“If you looked in a base station five years ago, you wouldn’t find many FPGAs,” Uhm said. “Today they are a prominent part of the radio and channel cards.” One of the reasons, Uhm added, is that FPGAs fulfill the need for base station designs to be much more flexible than in the past.

To make changes to traditional 3G base stations, companies typically had few options. They could try to implement a software patch to rectify a problem in software or a shortcoming in hardware, but doing that often slows down the hardware and thus the overall computation of the base

station, which if anything in the emerging days of LTE needs to be faster. Or they could send a technician out to the site to physically replace a defective or older PCB containing those devices with a newer one (and possibly add a software patch as well).

If there’s a drastic change, like the need to support an extra standard, carriers may have to install new base stations, much like AT&T did a few years ago when it moved from GSM to WCDMA. Of course, sending out technicians to sites around the world to swap out hardware and program software – on top of mountains, on top of buildings, on the edges of cliffs – adds great maintenance costs to a carrier’s network. Adding new base stations and securing leasing for those sites is exponentially more expensive.

“Base station vendors would love to sell carriers a network of base stations for each of the standards, but carriers can’t afford to do forklift upgrades anymore,” Uhm said. “They are looking for the flexibility to add new revenue-generating services, higher data rates, lower power, lower maintenance costs, and of course, a great price.”

Analysts point out that many years ago, base stations cost around \$250,000, but new base stations will likely be in the \$15,000 to \$25,000 range. They note that the unit price of base station hardware is only a fraction of the overall cost, and that leasing space and maintenance costs can be exponentially higher than the base station itself.

What’s more, if a base station needs to support multiple standards, designers typically have to create an ASIC and associated PCB for each of those standards, as well as extra circuitry to negotiate how those boards will interact with the existing antennae.

In particular, ASICs are increasingly more expensive at relatively low volumes (and at volumes typical for the base station market) and are difficult to produce on

leading-edge processes, making them increasingly less attractive for the macrocell, microcell, and picocell base station markets.

A single 65-nm ASIC mask runs around \$1.5 million, and a 45-nm mask is double that. Adding EDA and IP costs tacks a few million more onto design costs. ASSPs are similarly expensive for silicon vendors, complicated to produce, and typically modifiable only on a software level. Given the choice of ASICs, ASSPs, or DSPs, DSPs are the most versatile for base station applications and will likely maintain a secure position in 4G base stations. But only the software is modifiable, limiting flexibility if designers want to make changes to their designs in the field.

“When the issue was just GSM vs. CDMA for voice, it was best to do everything in DSP. But when people started adding data services such as EDGE and HSDPA, it really made a lot more sense to look at an FPGA solution,” Wirbel said. “That transition started to take place around 2002 or 2003.”

It’s for all of these reasons that designers are starting to give FPGAs a more central role in the era of multimode base stations. Some are even making FPGAs the primary devices for software defined radio implementations of multimode base stations.

“FPGAs add another level of flexibility and performance to a base station that ASICs, ASSPs, and DSPs cannot, enabling operators to increase ARPU by adding new bandwidth-intensive applications,” Uhm said. “FPGAs are attractive for multimode base stations because they have a mix of reconfigurable resources for high-performance signal processing.”

Joe Byrne, a senior analyst with the Linley Group, notes that one reason the FPGA is looking more attractive in the base station market is because LTE employs OFDM modulation. “The downstream modulation scheme in LTE is OFDM, which is a different scheme than WCDMA,” Byrne said. “It’s conceivable that next-generation base stations will essentially be one piece of equipment with two different processing modules: one that does the legacy protocol and another that does the new protocol.

But I think the opportunity is to create equipment that does both, and for that you need something that is programmable. The programmability can come from FPGAs or something with more traditional software programmability, such as a DSP.

“The thing with OFDM is that instead of being a signal carrier, there are a lot of signals conveyed on a lot of carriers in parallel. That means the processing

has to be done in parallel. So from an FPGA perspective, if you have these thousands of carriers to process, you can take your big FPGA and partition it into these processing units in parallel and do the processing of each carrier. That is something that an FPGA would be well suited for, instead of doing it in sequence.

“There’s an opportunity for doing it with a logic-based approach, such as an FPGA, as opposed to a software-based

Base Station 101

To date, wireless network carriers have traditionally employed two types of base stations (commonly referred to as cells). The first is the macrocell (see Figure 1), which usually consists of a tall tower with transmit and receive radio antennae at the top of the tower (receive is usually at the very top).

These antennae run signals, through fiber-optic cable, down the tower to electronics systems traditionally located at the base. The electronic systems coordinate the transmit and receive functions up to the antennae, negotiate coverage with other base stations, and transmit call data to the rest of the network as customers move from one base station’s coverage area to another, racking up billable minutes. Macrocells typically have large coverage areas; carriers deploy them in rural areas or along long stretches of highway.

The second type of traditional base station is called a microcell. Wireless carriers typically deploy these in densely populated areas like cities. The coverage area of a microcell is smaller than the coverage area of macrocell, but a cluster of microcells allows more people to access their carrier’s wireless network.

In recent years, the industry has produced two other types of base stations: the picocell and femtocell. The picocell is for smaller, even more densely populated areas such as airports, conference centers, and sporting venues. The femtocell targets home and small office use, whereas the macrocell, microcell and picocell are traditionally sold to networks. Femtocells will likely be sold at retail directly to consumers or perhaps bundled in with services such as cable or satellite TV.

“So far, femto has been over-hyped and under-delivered,” Wirbel said. “We don’t even know if it will be a real market and what the price points will be.” Still, it could be an interesting play as more devices in the home become wireless.

Analyst Richard Wawrzyniak addresses the promises and challenges of the picocell market as the “Xpert Opinion” in this issue of *Xcell Journal* (see page 8).



Figure 1 – A typical macrocell base station with receive antennae at the top, transmit antennae below the receive antennae, and the control system at the base.

approach, such as a DSP. Some fine tuning will always take place. The physical layer may be pretty well understood but the actual algorithm to extract the best performance out of the physical layer may change. It's good to have some flexibility, especially in the early days of the market.”

Wirbel agrees with Byrne and believes that next-generation base stations will

likely have a healthy mix of DSPs and FPGAs. “I think that the future lies in mixing and matching major DSP architectures on the top, with separate channels for multiple FPGAs in the middle. I think that's where the base station market is going,” said Wirbel.

Designers are considering several architectures for 4G base stations. Figures 2

and 3 illustrate two of the many uses for FPGAs in those architectures. Analysts point out that in addition to flexibility, performance will also be a key to 4G networks. In fact, it's such an issue that many next-generation base station designers are moving more of the compute power up the base station tower, closer to the antennae, to physically shorten the amount of time it takes for the antennae and base station control system to communicate.

Uhm said that the latest generation FPGAs are up to the performance requirements and many employ high-speed I/O.

5G and Beyond

While analysts seem to agree that FPGAs will play a stronger role in 4G networks, they all doubt that any manufacturer will be able to build a multimode base station that will also be able to anticipate and handle the data rates and feature set requirements of 5G base stations.

“Carriers have been doing incremental upgrades to their 3G base stations for several years now,” Byrne said. “They've upgraded from 7.2 Mbps to 10 Mbps with a software upgrade to the baseband processor, which is now a DSP or FPGA. I think that with LTE, we will see a lot of incremental upgrades. If you do a bigger upgrade than that, you'll essentially need new hardware.”

Byrne and others note that by the time 5G makes it to mainstream, there will likely be some crazy new hardware performance and functionality requirement. That means more challenges and opportunities for designers along the full spectrum of the wireless network.

Uhm said that Xilinx is investing heavily in developing not only FPGAs for the base station market but also tools, IP, and embedded software. Xilinx is also working with its many IP and software partners to help designers meet challenges and create innovations for the 4G wireless network, especially those base stations at the heart of worldwide wireless communications. For more information about Xilinx silicon and solutions for the base station market, visit www.xilinx.com/esp/wireless. 

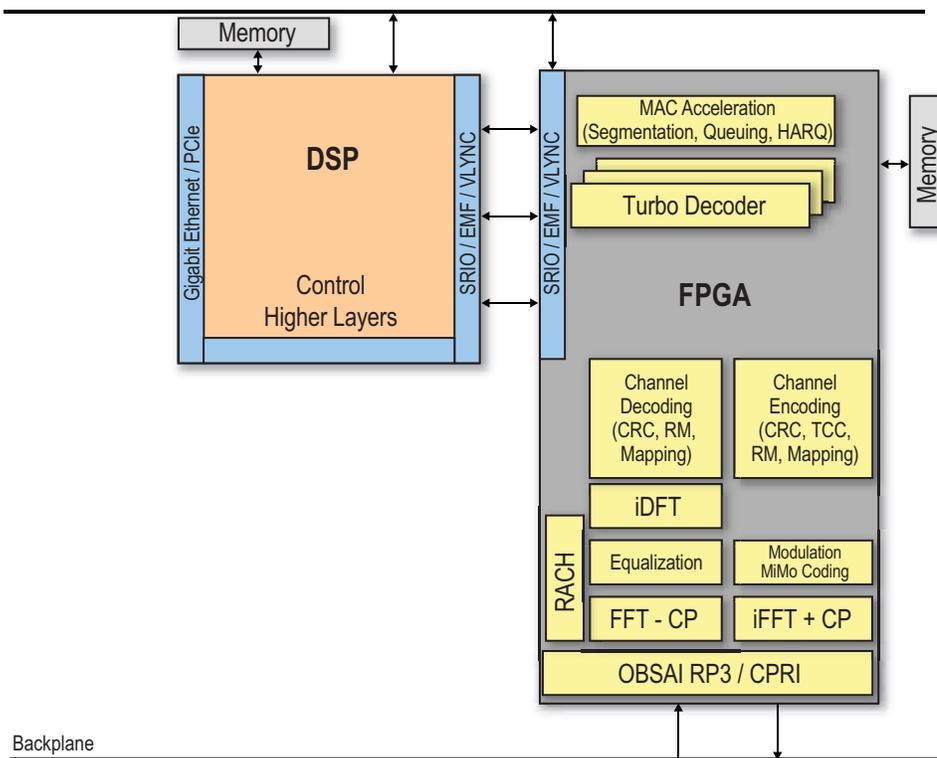


Figure 2 – FPGA preprocessing with DSP architecture

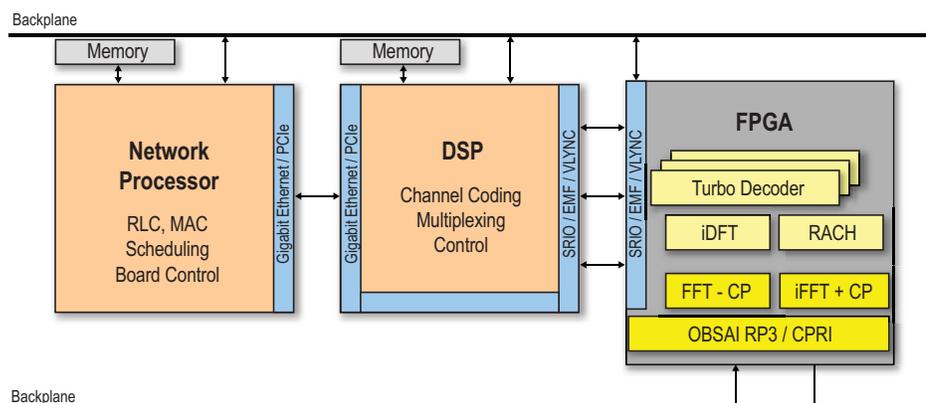


Figure 3 – FPGA as coprocessor for LTE

What Role Will FPGAs Play in the Pico-cell Base Station Market?

Airports outfitted with a comprehensive set of pico-cell base stations could give their customers much better experiences while traveling.



by Richard Wawrzyniak
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As we enter the second half of 2008, a sad fact of life is that airline travel is becoming harder and more uncomfortable with each passing week. This is due in large part to increased fuel costs for airlines and the cutbacks in service enacted to help offset these costs. Plus, some airlines are instituting additional fees for checked baggage and are also taking planes out of service, making the number of seats available fewer at any given time.

Undeniably, the life of the casual airline traveler is becoming more complicated. This is doubly true for the business traveler.

What does the FPGA have to do with all this? Please bear with me while I explain.

Traveler's Tension

Picture a large airport anywhere in the world, with many gates. Numerous planes are taking off and landing. Large masses of people are coming and going; the corridors are packed. Everyone is either trying to make a connecting flight, heading toward baggage claim, or looking for a place to rest weary bones.

Let's say that your flight has just arrived. You could be traveling by yourself, with other colleagues, or even with your family. This airport is unfamiliar to you and the people in it may be speaking a foreign language. The signs may also be in an unfamiliar language. Your flight has landed late (of course) and you need to make decisions about several things simultaneously:

- Where is the gate for my next flight?
- How far away is the gate from where I'm at now? Do I have enough time to get there without running?
- Do I have enough time to get something to eat (preferably at a reasonably good restaurant) along the way?
- What types of food are available along the way? Do any of them interest me, my colleagues, or my other family members?
- My colleagues were sitting in seats somewhere behind me on the plane. If I obtain the necessary information about shops, restaurants, gates, and flight times, how do I easily communicate this to them without losing any time?
- I need to connect to my office to send/download a file necessary for my next customer visit. Will my cell phone reception provide a data rate sufficient to accomplish this in a reasonable amount of time so I still have time to eat? (Don't forget, you're still hungry.)
- What other shops are along the way? Will I need to pick up a birthday present, which I didn't have time to do at my point of departure. Am I limited to just the shops I can see along the way? Does more information exist somewhere that I can access easily?
- Finally, where is the closest restroom?

I'm sure the list of questions above pretty much outlines the experiences of most airline travelers today. It is a set of decision points that we travelers review each time we fly – especially if our arrival airport is new or unfamiliar to us.

But given the press of humanity on all sides, all trying to do essentially the same thing at the same time, how will you collect all of this data in the short amount of time you have? This can be a daunting and stressful situation for most people. It definitely takes most of the fun out of flying today.

Smooth Skies

I'd like to lay out the following scenario of what I think is a possible solution to solving some of these issues for airline travelers.

As the cell phone market continues to evolve, new types of technologies are becoming available. This includes commu-

nication interface solutions such as WiMAX and WiFi for broader, faster coverage. A new technology has also come along: the picocell base station.

A picocell base station is similar to a cellular base station, except that it is intended to function in large municipal buildings and large commercial spaces such as airports and sports stadiums. Unlike its larger cousin, the cellular base station, each picocell base station is intended to service a far smaller number of users – possibly only several hundred to 1,000 users at one time, as the range of a picocell base station is only 100 to 200 feet.

Because of these restrictions, it would take still many picocell base stations to fully cover one facility (think O'Hare Airport or any large sports stadium). The main idea for this type of solution is to make very fast data rates available to users and to increase the quality of services offered to them.

One possible scenario, given the increase in capabilities, is to offer good quality mobile TV, for example. Another is some form of video conferencing, which business travelers would surely pay for, as it would give them the opportunity to be more productive while traveling.

I must point out that at the time of this writing, many details for picocell base sta-

tions have yet to be worked out. Areas like which communications protocol to use – WiMAX or WiFi – are as yet undetermined. How many users each base station will support is still undetermined. In addition, who will pay for these stations and how much access to these services will cost are also as yet undecided.

Changes will also have to occur on the cell phone handset side for these types of services to be accessed. In fact, several vendors (Intel being one of them) are planning to create semiconductor solutions that incorporate several air interfaces – all simultaneously active.

Airline travelers might start to see some of the fun come back into flying, with services enabled by picocell base stations.

These solutions will begin entering the market toward the end of 2008 and into 2009. Much work still needs to be done to arrive at the right mix of features and capabilities. However, it would seem that there is definitely some value to this type of solution.

Airports outfitted with a comprehensive set of picocell base stations could give their customers much better experiences while traveling. Vendors could offer a wider set of products and sell these products to a broader set of customers. Most airport vendors today do not really do much advertising, depending instead on foot traffic.

Imagine a situation where vendors allow access to their products and services over the Internet through picocell base stations. Potential customers could access airport restaurant menus remotely, order meals, and reserve table space if necessary. They could pay for their meal and have it ready as they move toward their connecting gate.

The same solutions could apply for the other basic questions I outlined previously: where is the next gate, how much time does it take to get there, what shops and restaurants are along the way, and how do I communicate this information to my colleagues. All of these questions can be answered by putting such a system in place.

To make such a scenario real, additional middleware must be written with the appropriate level of security for financial transactions. This presents opportunities for both software companies and facility owners to jointly participate in improving the level of service available to the traveling public.

FPGAs in Picocell Base Stations

Back to the FPGA. For the type of system outlined in this article, the number of picocell base stations would need to be substantial, since the range of each system will be fairly limited. This increases the number of systems needed to offer full coverage.

Given the range of capabilities inherent in such systems, the types of services offered must change very fast to meet changing consumer preferences. Programmable logic is a perfect fit given these parameters.

Picocell base stations will be fitted in relatively small enclosures, probably high up toward the ceiling in any given large commercial space. In this situation, there will be little opportunity to do an extensive installation of new fixtures, since the space around these installations will most likely remain in service during the installation process. Although the systems will have access to building power, they won't have extensive cooling systems, which means operating in ambient conditions. This lends itself well to the direction programmable logic is heading in today;

namely, lower power silicon that still delivers relatively high performance.

Finally, because the number of systems in any of these environments will be large, the ability to swap out circuit boards for upgrades will be limited. This is another area where programmable logic can shine, given its ability to be reprogrammed as needs dictate.

Semico Research Corp. has looked at this market and has concluded that a real potential exists both for the picocell base station concept and for the role programmable logic can play within it.

The forecast shown in Figure 1 is for the semiconductor content in the entire picocell base station market, including programmable logic. It is reasonable to expect that programmable logic will represent at least 15% of these revenues. It is also likely that each system will include at least one programmable logic device and that larger systems will include more than one programmable logic device.

If, as Semico believes, this market does in fact come to fruition, it can represent a significant growth potential and revenue stream to the programmable logic industry in the coming years.

The future is indeed bright for programmable logic. Airline travelers might start to see some of the fun come back into flying, with services enabled by picocell base stations.

Now if airports could do something to make their seats more comfortable ...

Source: Semico Research Corp.

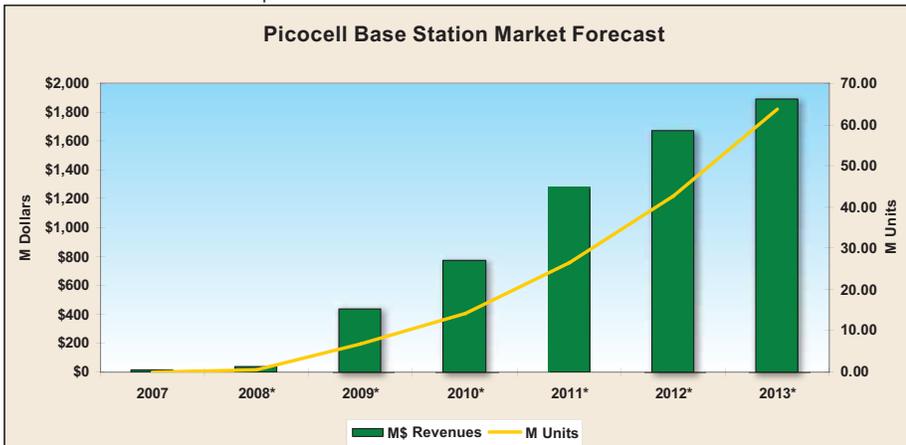


Figure 1 – Picocell base station market forecast



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Exploring and Prototyping Designs for Biomedical Applications

Researchers at the University of Hawaii at Manoa have implemented ECG analysis algorithms with Xilinx System Generator.

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Many physicians use electrocardiogram (ECG) machines to monitor the electrical activity of the heart and the heart condition in general. But today, there is a lengthy delay in the time it takes to transfer data from ECG monitoring machines to trained physicians.

Here at the University of Hawaii at Manoa, we are researching ways to transfer – in real time – preprocessed ECG data from the patient's heart to physicians. As a first step toward this goal, we implemented two variants of a well-known software detection algorithm for ECG in hardware and explored the design choices using Xilinx® FPGA tools and hardware.

Many biological instrumentation-based designs require designers to combine filtering stages and customized logic such as finite state machines in the same system. But now it is easier for researchers to design filters in the Xilinx System Generator environment by simply connecting the various blocks from the Xilinx blockset (included with the System Generator blockset library) instead of creating these modules from scratch using a hardware description language like Verilog or VHDL.

Using System Generator to create most of the blocks allows you to concentrate on the critical parts of the design and delegate the details of the implementation of those standard modules to the tool. You can then import your custom logic modules into the System Generator environment; the tool will integrate those custom logic blocks with the rest of the design.

Because noise contamination is an inherent problem in ECG monitoring and we cannot completely remove it, we had to come up with a way to suppress noise contamination.

Automated ECG System Analysis

A heart's natural pacemaker, composed of special self-exciting cells, generates and propagates a polarization and depolarization electrical signal that regulates the proper contraction of the heart muscle. This electrical activity is recorded as an electrocardiogram (ECG) by a machine called an electrocardiograph, which provides physicians with a wealth of information on heartbeats and the heart's condition in general [1].

The QRS complex – a wave structure that corresponds to the depolarization of ventricles and has a spiked shape in the ECG – is often the most telling waveform found in an ECG signal. The morphology, duration, and amplitude of the QRS complex in an ECG signal provides significant information to physicians diagnosing various arrhythmias and other cardiac ailments.

Health professionals can best judge the state of a patient's heart by monitoring the heart's activity (and the QRS complex) during stress or physical activity. Therefore, health professionals often connect ECG monitors to their patients for many hours (generally 24 hours at a time).

Currently, most health professionals use Holter System monitors for this purpose. But Holter System monitors have an inherent battery power and processing power constraint that limits their functionality to data acquisition systems.

A Holter System's heart monitors record the patient's ECG data to flash memory or to a tape attached to the system. A technician then removes the drive from the Holter System and sends it to the lab, where technicians analyze the data. Once the lab technicians complete their analysis, they send the ECG report to the physician. Of course, this means that there is a delay between hooking up the monitor to the patient and getting the ECG data to the patient's physician, thus delaying treatment, possibly with tragic consequences.

Here at the University of Hawaii at Manoa, we are researching how to create ECG analysis systems that will reduce the amount of time it takes to transfer data from the patient's heart to the physician by carrying out the analysis in real time. We hope to achieve this by integrating the ECG analysis system into portable ECG monitors, which physicians can use directly and thus eliminate the technician translation/analysis step.

To aid us in this effort, we have implemented real-time ECG analysis on a Xilinx Spartan™ XC3S500 device in the Spartan-3E starter kit, which allows the system to perform this analysis much faster than previous software-based methods. FPGAs offer many advantages for this and other applications because they support rapid prototyping, are less expensive than ASICs at low volume, and are quickly reprogrammable.

Furthermore, their fast and efficient testing option, combined with System Generator software, makes them a great choice for algorithm exploration as well as hardware implementation and prototyping.

Implementation of the Algorithm in Hardware

In our research, we are implementing a well-known algorithm by Tompkins and Hamilton for QRS detection in hardware ([2], [3], [4], [5]). To help us with this effort, we took advantage of the fast prototyping features included in the Xilinx toolset.

In our system, the processing of the ECG signal begins with a number of filtering stages through which a signal must pass before the system accurately detects a QRS complex. We divided the design into two main stages. The first stage, or pre-processing stage, comprises four linear filters and one non-linear filter. The second stage, or peak detection stage, identifies the peak signal in the QRS complex and applies decision rules to qualify a feature as a QRS complex.

Filtering Stage

The ECG recording is very sensitive to even the smallest body movement or noise, such as electrical muscle (myographic) signals and the system's own electrical power-line interference. Because noise contamination is an inherent problem in ECG monitoring and we cannot completely remove it, we had to come up with a way to suppress noise contamination. We achieved this by employing filtering during the preprocessing stage (as in [4], [5]).

To do this, we first pass an ECG signal through an infinite impulse response (IIR) low-pass filter, which suppresses the high frequency noise in the signal. Then the signal passes through an IIR high-pass filter, which attenuates the P and T waves in the signal and suppresses the DC offset present in the signal.

The low-pass and high-pass filter together form a bandpass filter. It then feeds the output of the high-pass filter to a finite impulse response (FIR) derivative filter, which further emphasizes the QRS complex. This typically presents a more pronounced slope variation compared to the other signal features, making it somewhat easier for observers to identify [1].

The FIR derivative filter step also helps further reduce the noise content of the signal. After filtering, we employ a squaring stage that carries out non-linear amplification of the QRS complex and makes all data points positive.

Finally, we use the output of the squaring stage as the input to a moving window integrator. Each sample output from this filter is an average of the previous 32 values. We implemented all these filtering stages directly in the Simulink environment using the System Generator tool. Then we tried out two different approaches for the next stage, which is a moving window integrator.

The first approach involved the connection of a number of register, delay, and adder blocks to implement the filter as a



Figure 1 — Input ECG and filtering stages output, from top to bottom: original signal, low-pass output, high-pass output, derivative output, squaring stage output, moving window integrator output. The arrow indicates the position of the QRS complex.

direct Form I structure. With this approach, however, we ended up using 31 adders and an equally large number of delay or register blocks.

We investigated further and later came up with a more resource-efficient structure that uses the block RAM resources in the Spartan-3 FPGA. This final structure uses a

small RAM of 32 40-bit words and just two adders and is also very efficient in timing. Figure 1 shows a typical ECG input, with results of the various filtering operations.

Peak Detection Stage

In the peak detection stage, we are trying to find the peak in the output of the moving

window integrator. The peak detection process depends on the calculation of the threshold value, and we can locate a peak among the sample values that are greater than the threshold value. But the algorithm does not report a peak until a sample appears in the falling slope of the moving window integrator signal with a value less than half of the peak value.

We use this method because it reduces the number of false peak detections caused by noise. Once the algorithm locates the maximum point of the QRS signal in the moving window integrator output, we search for a peak in an appropriately delayed copy of the output of the high-pass filter and use it as a fiducial point for the position of the QRS complex.

Essentially, we are finding the peak of the QRS complex in the output of the bandpass signal instead of the original signal, because the original signal is highly contaminated by noise. We achieved this using a memory module, which records the previous 60 samples from the high-pass filter and sends a fixed interval of samples

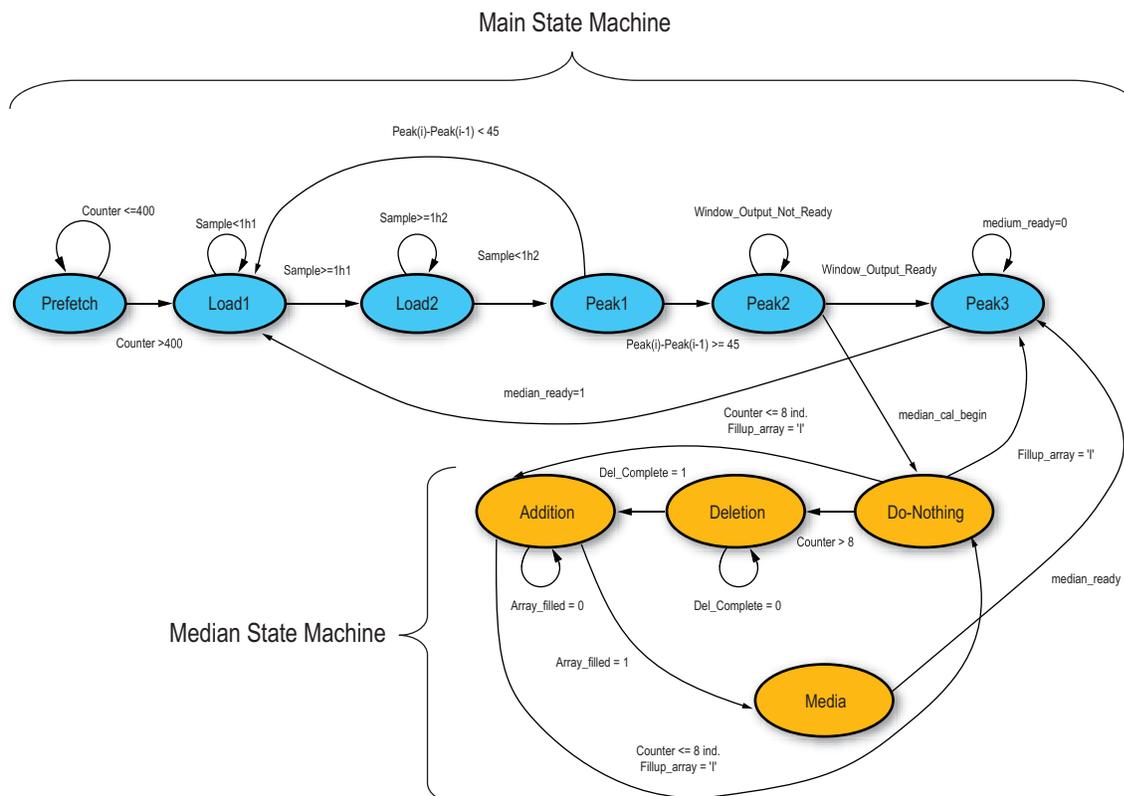


Figure 2 – State machine for the complete design

containing the QRS complex as an input to the window module. The window module finds the maximum QRS signal.

We based the threshold for the next peak detection process in the moving window integrator output on the median of the eight previously detected peaks.

To calculate the running median calculation, the system maintains an updated, sorted list of such peaks. The computation is supervised by a median calculation FSM (called the median state machine) communicating with a separate peak detection FSM (called the main state machine) (see Figure 2). The main state machine finds the peak in the moving window output (as discussed); then the median state machine sets up the threshold value for the next detection.

We implemented the entire peak detection stage in VHDL. It contains the memory, window, main, and median state machines and the median RAM modules. Later, we imported these VHDL modules into the System Generator environment as black boxes and simulated the design (Figure 3).

Programming and Testing the Hardware Implementation

We programmed the FPGA through the JTAG port. To test the design, we used System Generator's JTAG co-simulation feature, which allowed us to pass data from the Simulink environment through the USB cable to the board (the Xilinx Spartan-3E starter kit) containing the downloaded design.

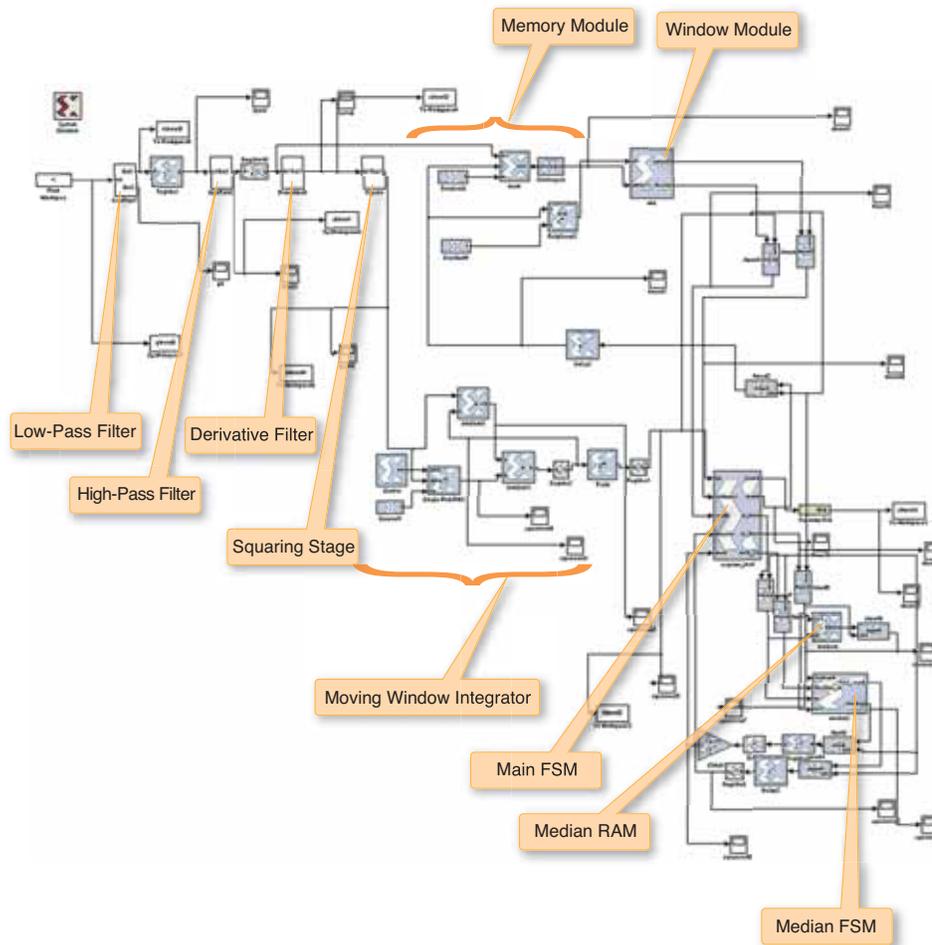


Figure 3 – Complete design in the System Generator environment

The design implemented in the FPGA processes the data and sends the output back to the MATLAB environment so that we can compare it to the simulation output. This feature was very convenient and helped us establish the accuracy of the design implementation in hardware. It also allowed us to run tests on complete sets of benchmark ECG data (from www.physionet.org) in a fraction of the time we previously needed to test the software version of the algorithm.

Overall, we found System Generator to be very useful for implementing designs for biomedical instrumentation applications. The tool provides easy filter design options and simplifies design implementation by accepting imported custom modules as black boxes. It also provides a fast and efficient way to test a design on hardware, with easy interfacing options between the board and the user's workstation. 🌈

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Taking Designs to New Heights with Space-Grade Virtex-4QV FPGAs

Special processing, packaging, and SEU mitigation techniques enable designers to perform system-level integration with reconfigurable FPGAs in space-based systems.

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Designing high-performance electronic systems for space presents designers with a slew of unique challenges. Designers must meet tight power and weight budgets while under enormous pressure to get designs completed on time and with zero flaws.

Companies and government agencies set rocket launch schedules years in advance of actual launch dates. Missing a launch date can delay programs until, literally, planets align; some delays can even lead to project cancellations.

But while space applications have power, weight, and time-to-launch challenges, by far the most stringent requirement is ultra-high reliability. If a component fails in space, you can't send the Geek Squad out to fix it (unless you have astronauts on board).

To make things worse, as spacecraft rise to higher altitudes – and especially as they move beyond the protective blanket of Earth's atmosphere – they are bombarded by increasing levels of radiation that can upset or even disable delicate electronic components.

As a viable solution to these challenges, you can try to integrate functions into an ASIC, which can meet your performance, capacity, and power requirements. But designing an ASIC is increasingly complex, and if the design requires new functionality or if you find a bug late in the design cycle, you may have to re-spin the design or even create a new mask, causing you to miss launch windows.

Some silicon vendors offer radiation-hardened anti-fuse FPGAs, but those devices have limited capacity and performance, which means most of them are unsuitable for achieving SOC-type integration goals.

Increasingly, designers are turning to space-qualified Xilinx® Virtex™ FPGAs, which allow them to achieve performance, power, and integration targets while enjoying flexibility and productivity benefits previously available only in the commercial arena.

Let's examine our latest space-grade offering, the Virtex-4QV FPGA family, and some design techniques and tools that you can use in your design projects to tailor the devices for your space deployment requirements.

The Xilinx Space Heritage

Xilinx has provided uninterrupted support to the aerospace and defense (A&D) community since 1989. Our company pioneered the application of SRAM-based FPGAs in high radiation environments, beginning with the XQR4036XL FPGA, which first flew in FedSat, an Australian satellite.

Quad-redundant XQR4062XL FPGAs performed mission-critical landing duties (pyro control) on the Mars Exploration Rover (MER) 2003 landers, which delivered the Spirit and Opportunity MERs to the surface of Mars. Virtex XQRV1000 FPGAs handle motor control functions on both MERs as they explore the Martian landscape.

To accelerate the adoption of reconfigurable FPGAs for aerospace applications, in 2002 Xilinx joined forces with the Jet Propulsion Laboratory, Los Alamos National Labs, Sandia, Aerospace Corp., and SEAKR Engineering to found the Single-Event Effects (SEE) Consortium. Fostering an environment of openness and collaboration, the SEE Consortium leverages the collective talents and financial resources of its member companies to perform exhaustive analysis of complex FPGAs.

The SEE Consortium subjects FPGAs to in-beam radiation testing and then reports peer-reviewed results to the industry. As a result of those efforts, Venus Express, the Mars Reconnaissance Orbiter, GRACE, OPTUS, TACSAT2, CIBOLA, and a number of classified programs have included Xilinx FPGAs. Many more Virtex FPGAs will soon be

orbiting overhead, as our customers have more than 50 new programs currently under development.

Virtex-4QV FPGA Family Overview

To bring the benefits of advanced FPGAs to designers of in-orbit, space-based, or extraterrestrial systems, Xilinx recently launched a space-grade variant of its Virtex-4 family. The new Virtex-4QV family of radiation-tolerant FPGAs meets the military's MIL-PRF-38535 Class V screening requirements and offers design groups a compelling alternative to ASIC and one-

time programmable logic technologies. The lineup comprises four of the configurations from the commercial Virtex-4 device family (see Table 1).

High-performance logic, processing, and DSP capabilities make Virtex-4QV FPGAs ideal for demanding applications such as video processing, radar, and encryption. In addition, their packet processing capabilities are enabling a new generation of networked space-based communication systems, such as the IRIS program, to put reconfigurable network routing in orbit.

		Virtex-4QV FPGAs Optimized for:			
		Logic	DSP	Embedded Processing	
Part Number		XQR4VLX200	XQR4VSX55	XQR4VFX60	XQR4VFX140
Logic Cells		200,448	55,296	56,880	142,128
CLB Flip-Flops		178,176	49,152	50,560	126,336
Maximum Distributed RAM (Kb)		1,392	384	395	987
Block RAM/FIFO w/ECC (18 Kb each)		336	320	232	552
Total Block RAM (Kb)		6,048	5,760	4,176	9,936
Digital Clock Managers (DCMs)		12	8	12	20
Maximum Single-Ended I/Os		960	640	576	896
DSP Slices		96	512	128	192
10/100/1000 Ethernet MAC Blocks		–	–	4	4
PowerPC Processor Blocks		–	–	2	2
Total Ionizing Dose (krad)		300	300	300	300
SEL Immunity (MeV-cm ² /mg)		>125	>125	>125	>125
Package	Area	Available User I/Os			
CFA Packages (CF): Flip-Chip Ceramic Column Grid Array (1.0-mm Column Spacing)					
CF1140	35 x 35 mm		640		
CF1144	35 x 35 mm			576	
CF1509	40 x 40 mm	960			768

Table 1 – Xilinx 90-nm Virtex-4QV FPGA family

The combination of the XTMR methodology and configuration memory scrubbing provides an elegant and cost-effective method to ensure reliable operation for almost all critical space applications.

To enable design teams to use reconfigurable FPGAs in space, Xilinx tackled multiple technical challenges:

- Make the CMOS silicon immune to latchup induced by strikes of heavy ions (a.k.a., “cosmic rays”)
- Create a high pin-count package that meets the unique requirements of space deployment
- Screen all devices to MIL-PRF-38535 Class V requirements
- Develop a range of upset mitigation techniques backed up by tools and IP

Ionizing particles in space can strike the electronic systems of a spacecraft and produce currents in a device’s silicon junctions that can induce latchup of the parasitic transistors inherent in all CMOS integrated circuits. Latchup is a significant concern for designers because it results in high current that can kill the device.

To provide immunity against destructive latchup, Xilinx fabricates radiation-tolerant Virtex-4QV FPGAs on special wafers that incorporate a thin, lightly doped epitaxial layer. In the event of a particle strike, the doped substrate effectively limits the length of the charge trail that can contribute to a current spike in active nodes (Figure 1).

For each Virtex-4QV device type, the SEE Consortium verifies latchup immunity at maximum V_{CC} and operating temperature, subjected to a heavy ion fluence exceeding 1×10^7 particles/cm², with an effective linear energy transfer (LET) exceeding 125 MeV-cm²/mg.

Packaging Considerations

Space applications impose special requirements on device packaging with regard to thermal cycling and hermeticity. Xilinx has developed a column-grid array (CGA) surface-mount package that meets these requirements while supporting the high pin count of Virtex-4 FPGAs.

For reliable operation in the vacuum of space, semiconductor devices require packaging that can withstand the extreme temperature ranges and thermal cycles encountered outside the thermal conduction of the Earth’s atmosphere.

It isn’t uncommon for one side of a satellite to broil under the searing radiation of the sun, while the other side suffers the deepest chill of space. Components in an orbiting and spinning satellite can find themselves rapidly cycling between these temperature extremes. In such an environment, differences in the coefficients of thermal expansion between PCB and device pack-

ing point than the solder paste that companies typically use to attach the device to the circuit board. The solder columns flex to absorb the difference in expansion rates of the package and board to greatly extend the operating life of the device.

Hermetic packages encapsulate die, which electrically connect to the package pins through wire bonds. Virtex-4 FPGAs are high pin-count devices and thus can’t employ wire-bond packaging. Instead, they use flip-chip packaging, in which solder bumps on the die make direct contact with the package substrate.

For Virtex-4QV FPGAs, we reengineered the device’s flip-chip package to

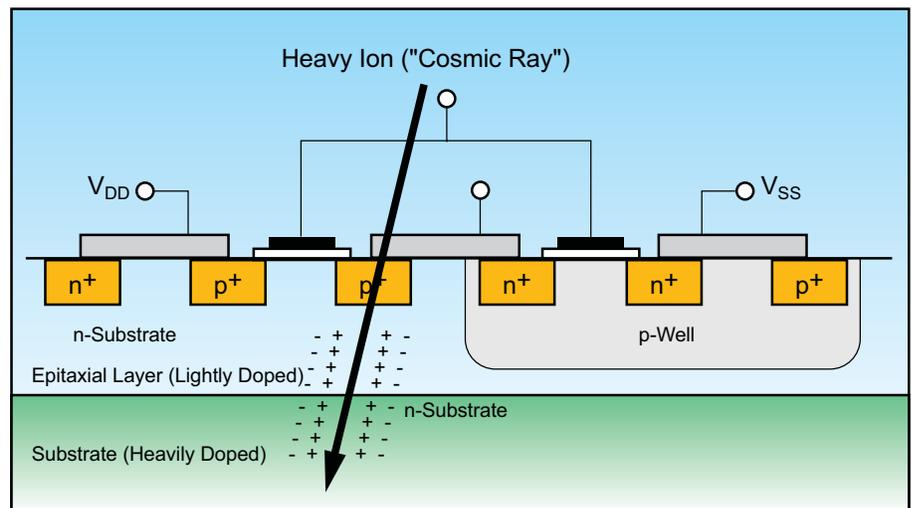


Figure 1 – A mobile charge produced by a heavy ion strike can induce SEU in an FPGA.

age materials can lead to failures in the solder joints that bind the packaged device to its PCB.

To avoid this problem, we package our Virtex-4QV FPGAs with CGA packaging, which addresses the thermal cycling shortcomings of traditional surface-mount technologies. An enhancement of BGA technology, CGA packaging uses solder columns, rather than balls, made of a more flexible low-tin solder with a higher melt-

address the thermal cycle-induced stress where the die attaches to the package, as well as to meet the reliability requirements of a hermetic package. Through judicious choice of solder bump and underfill materials, lid material, and lid-attach adhesive, we made sure that Virtex-4QV devices satisfy JEDEC moisture sensitivity level 1, NASA outgassing requirements, and corrosion specs, plus first- and second-level thermal cycle reliability requirements.

To ensure that our Virtex-4QV FPGAs meet reliability standards for space deployment, Xilinx performs conformance certification of each manufacturing lot. Following military performance specifications, we perform a full test suite across the full military temperature range, including dynamic and static burn-in.

In addition, we perform full TCI/QCI screening to MIL-STD-883 test method 5004 (screening 100% of units) and 5005 (destructive stress testing) on a lot-by-lot basis. We subject every assembly lot to destructive physical analysis (DPA) to comply with MIL-STD-1580 requirement 16, which involves the construction analysis of die fabrication, package fabrication, and assembly.

Design Techniques for Upset Mitigation

In addition to making the silicon more resilient to radiation, Xilinx has developed a range of mitigation techniques that designers can employ to further reduce the likelihood that a charged particle strike will affect the operation of our FPGAs in high-radiation environments.

When developing systems that will operate in hostile radiation environments, you must consider the effects of charged particles such as heavy ions or reaction products from neutrons or protons. As these charged particles travel through the FPGA (Figure 1), they can alter the logic state of any static memory element, resulting in single-event upsets (SEUs). An SEU in the configuration memory array can have adverse effects on expected FPGA functionality.

By thoroughly analyzing your system’s operating environment and radiation-tolerance requirements, you can choose an approach that economically delivers the required reliability. For example, for a mission-critical application in a harsh environment, you could use a mitigation scheme that combines redundant FPGAs with radiation-hardened configuration management hardware.

On the other hand, consider an orbiting satellite carrying an image processing circuit that powers up only periodically to capture scenes of interest. If the statistical risk of an upset during that short window of operation is acceptably small, you might choose

to forego any special mitigation techniques, especially if the worst-case outcome is the corruption of single frame of image data. In this case, the standard configuration process of loading fresh configuration data on each power-up cycle could be a sufficient approach to fixing upsets.

Answering the following questions and understanding the trade-offs between these application requirements will guide you in selecting the appropriate mitigation scheme:

- Is the application error-tolerant?
- What is the expected operating time window?
- What is the FPGA performance requirement?
- What is the FPGA power requirement?
- How cost-sensitive is the application?
- Can the application withstand any possible FPGA downtime? If so, does the single-event functionality interrupt (SEFI) cross section specified in the data sheet meet the application requirement?

Based on your answers to these questions, you can employ a series of mitigation techniques and IP in your design to reduce the risks that a particle strike will affect the operation of Xilinx FPGAs when they are in high-radiation environments. Figure 2 provides an overview for a mitigation scheme selection based on application requirements and environmental constraints.

Reconfiguration and Memory Scrubbing

A complete FPGA reconfiguration (or, alternatively, power-cycling the FPGA) is the simplest form of mitigation, as it reloads the configuration memory contents. You can use the FPGA’s configuration memory readback function to determine whether the contents have been corrupted by an ion strike and then initiate reconfiguration. Although readback does not interfere with the device’s operation, a complete reconfiguration interrupts design function for anywhere from a fraction of a second to a few seconds, depending on clock rates and device size.

Because a given design uses only a fraction of the configuration memory cells in an FPGA, an SEU will likely have no effect on system operation. To avoid unnecessary interruptions caused by complete reconfiguration, you can employ the partial reconfiguration capabilities built into Virtex-4QV FPGAs to reset corrupted bits. The FPGA performs this process (called memory scrubbing) automatically, without hindering the operation of the system.

Hardware Redundancy

Designers can also fall back on a well-known technique called hardware redundancy, which is critical for high-availability systems – those that can only have minimal unplanned downtime. By employing hardware redundancy, you create two copies of a system so that one copy can keep running

Data Criticality		Low		High	
		No		Yes	
SEU Rate	System Duty Cycle	Low	Hours	No Mitigation	XTMR
		High	Weeks	Configuration Management (Scrubbing)	Configuration Management Plus XTMR
			Years		
			Continuous		

Figure 2 – Mitigation scheme matrix

if the other fails. However, the overall system may not be able to distinguish which of the two systems has failed.

To resolve this dilemma, you can add a third copy of the system – known as triplication – to act as a tie breaker. Logic triplication, plus the addition of special voter circuits at key locations in the design, enables your system to continue running even in the presence of an upset.

You'll find that the ample logic and routing resources available in Virtex FPGAs enable you to implement logic triplication within a single device. This capability is the cornerstone of the Xilinx Triple Modular Redundancy (XTMR) methodology. We offer software called the TMRTool that automates the process of building triple redundancy into your designs to simplify this tedious and poten-

design to periodically scrub the circuits and prevent errors from accumulating. Indeed, the combination of the XTMR methodology and configuration memory scrubbing provides an elegant and cost-effective method to ensure reliable operation for almost all critical space applications.

There are extremely rare cases where the combination of XTMR and scrubbing is not enough. For example, if several ions simultaneously (during a single scrub cycle) strike the device's configuration memory and change the logic function on two signals going into the same voter circuit, the voter circuit will misinterpret the false signal as a valid signal and propagate the false signal through the rest of the circuit.

However, for a reasonable scrub rate, even during the most severe space radia-

Redundant Devices

Depending on the mission criticality of your design and the orbit in which it will be operating, you might choose to use an even more robust mitigation scheme. For example, you can expect that a triplicated design with full-blown configuration management in geosynchronous orbit will experience only one SEFI per device-century. Thus, if the FPGA's SEFI detection and device reconfiguration requires only one second, the result is one second of device outage per 3 billion seconds of operation.

In the unlikely event that your system requires even higher availability (must have extremely short or no downtime), you should employ a design that involves redundant FPGAs plus dedicated configuration management, as well as voting on

Mitigation Scheme	Mitigation Strength	Board Layout Complexity	Ease in Meeting Timing Constraints	Power Consumption	Component Cost
No Mitigation (Power Cycling)	Weak	Low	Normal	Typical	Low
Configuration Management (Scrubbing)	Medium	Low	Normal	Typical	Low
XTMR	Medium	High	Reduced	~3x Typical	Medium
XTMR + Configuration Management	Strong	High	Reduced	~3x Typical	Medium
Redundant Devices + Configuration Management	Strongest	Medium	Normal	~2-4x Typical	High

Table 2 – Performance overview of mitigation schemes

tially error-prone task. Used in conjunction with the ISE™ software design tool suite, the TMRTool will partially or fully triplicate a design, insert voters, and synchronize feedback path loops. TMRTool also enables the insertion of custom-triplicated design modules.

XTMR by itself is not completely fool-proof. As systems fly through space, they will accumulate errors that will adversely affect their operation. During system operation, the probability of system error increases exponentially as upsets accumulate in the system and defeat the device's voter circuits.

To address error accumulation before it becomes a problem, use a combination of XTMR and memory scrubbing in the

tion conditions (a 90% worst-case solar flare), the probability of this happening is lower than the likelihood of a SEFI – the upset of a control bit that results in the persistent interference of the normal operation of the circuit.

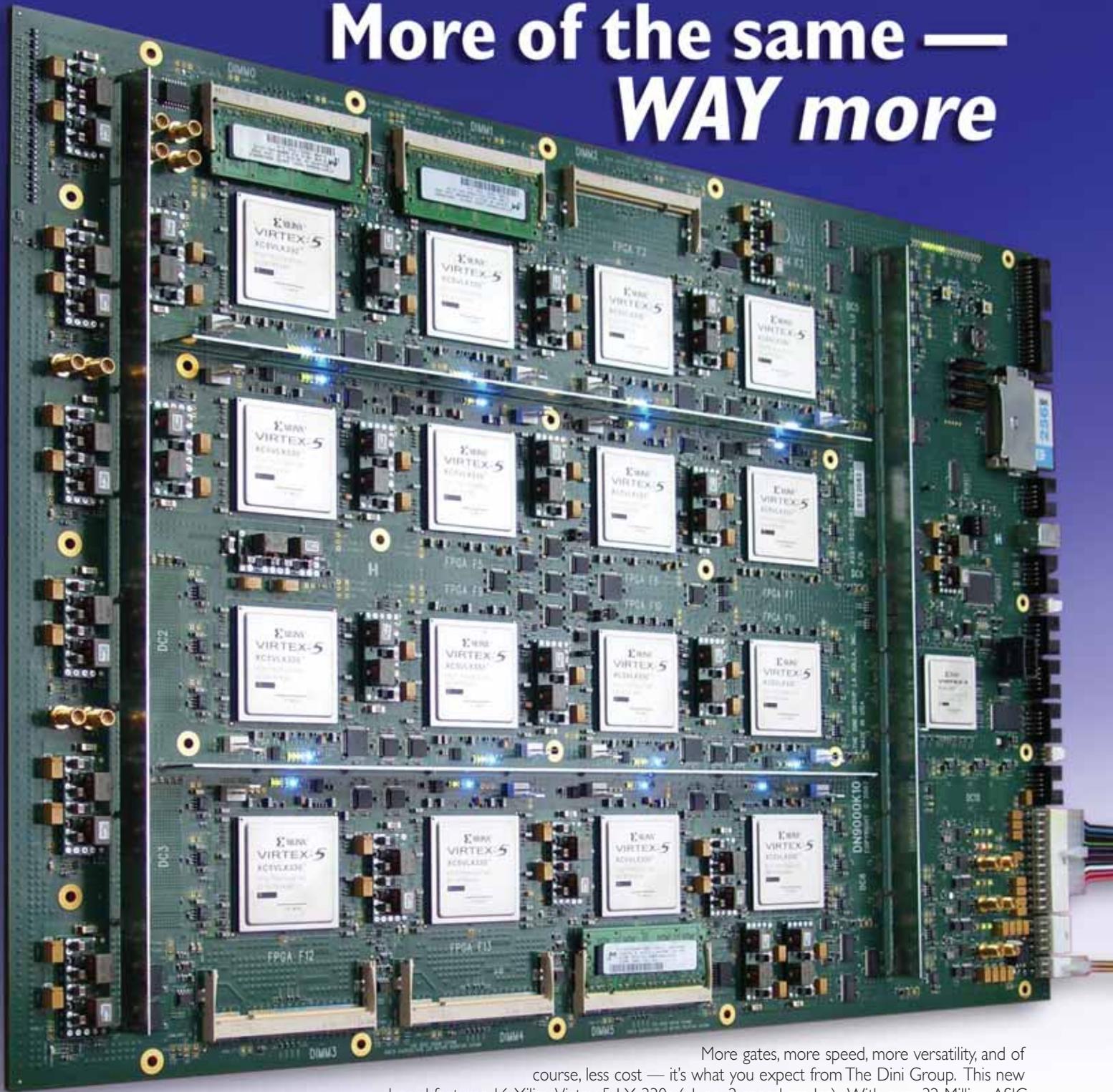
A SEFI typically results in the loss of one or more of the following: configuration capability, power on reset ability, JTAG functionality, a region of configuration memory, or the entire configuration. Recovering from a SEFI requires reconfiguring your FPGA.

You can improve scrubbing by adding the ability to detect SEFIs. Thus, full-blown configuration management combines transparent readback and scrubbing plus SEFI detection.

the outputs of the FPGAs. Table 2 shows the trade-offs that can guide your choice of mitigation schemes.

Xilinx takes great pride in introducing space-grade variants of our commercial devices to bring advanced functionality to designers in the aerospace and defense industries. This functionality allows you to meet payload and power requirements and integrate more advanced functionality into your designs. It also gives you the unique flexibility to make changes to your designs late in the development process and even in space, if required. And as you plan to expand the possibilities of space exploration, Xilinx continues its commitment to helping you make those possibilities a reality. 

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CERN Scientists Use Virtex-4 FPGAs for Big Bang Research

How 120 Xilinx FPGAs help scientists understand the big bang and gain insight into the fundamental building blocks of matter.



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In a tunnel underneath the French-Swiss border, scientists at CERN, the European laboratory for particle physics, are on the verge of conducting an experiment called ALICE (A Large Ion Collider Experiment).

They will use the world's most powerful particle accelerator to accelerate two streams of heavy lead (Pb) ions very close to the speed of light and make them collide head-on, attempting to recreate conditions believed to exist shortly after the big bang.

CERN scientists expect that each collision will release an enormous amount of energy and create a local temperature of 10^{12} °C – a hundred thousand times higher than the core of our sun.

When the heavy ions collide, CERN scientists expect the collision will also generate a vast number of subatomic particles flying in all directions. CERN scientists hope that by tracing the paths of these particles, they can discover answers to many of the deepest questions in physics.

Scheduled to begin in 2008, CERN scientists will observe collisions in the ALICE experiments with the help of Xilinx® FPGAs, which will allow them to map and disentangle the trajectories of the thousands of subatomic particles emerging from the collision. Powerful data-reduction algorithms in the FPGAs eliminate redundant information and send only the important data to the CERN data bank.

In April 2008, Xilinx accepted the ALICE Industrial Collaboration Award for its contributions in support of research into particle physics. Professor Volker Lindenstruth of the University of Heidelberg presented the award on behalf of the ALICE collaboration in recognition of the central role played by Xilinx FPGAs in the core measurement instrumentation (see Figure 1).



Figure 1 – Pictured from left to right: Marc Defossez, Peter Alfke, Volker Lindenstruth, and Patrick Lysaght

The Large Hadron Collider and ALICE

Considered the “most ambitious scientific undertaking on earth,” the Large Hadron Collider (LHC) is the world's largest and most complex scientific instrument. It is housed in a 27-km tunnel 100m below

ground, straddling the French-Swiss border near Geneva (Figure 2). It is the latest and most powerful in a series of particle accelerators physicists are using to study quark gluon plasma, the smallest known particles that are the fundamental building blocks of all matter.

The Large Haldron Collider accelerates protons and heavy ions close to the speed of light and smashes them together, thus recreating conditions that existed a fraction of a second after the big bang.

The scientific community generally assumes that the universe has been cooling down ever since the big bang, and that all matter familiar to us evolved out of this event. The particle collisions in the LHC

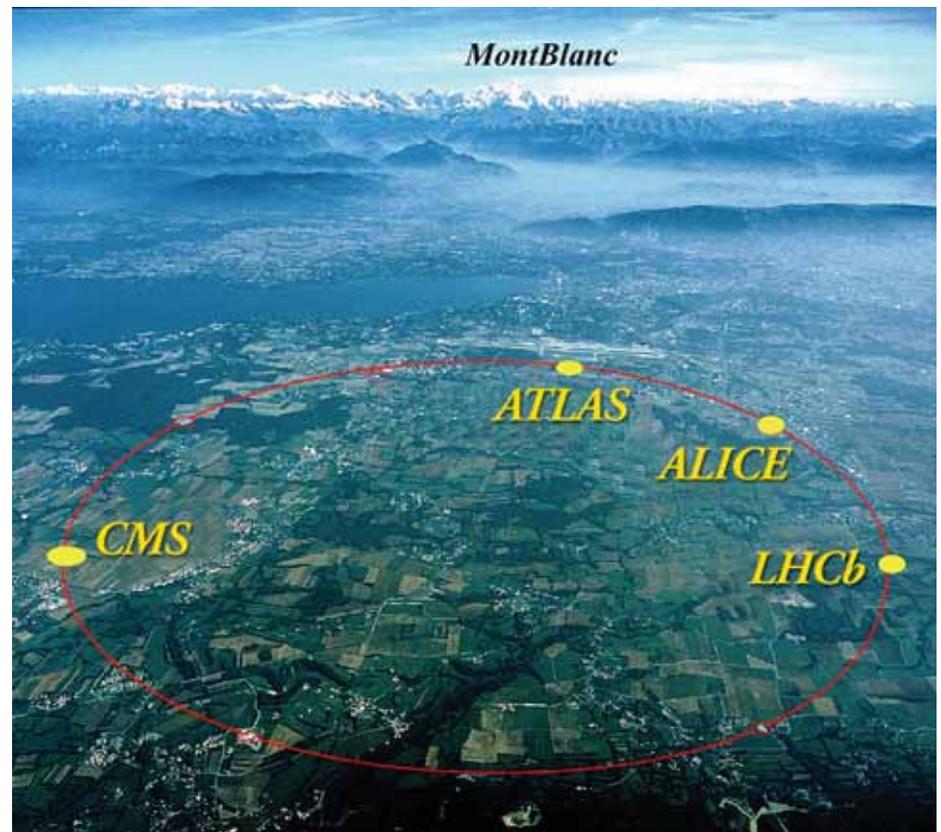


Figure 2 – The CERN Large Haldron Collider is located underground, straddling the border between France and Switzerland near Geneva.

Each XC4VFX100 device performs the first-level data reduction simultaneously and independently, and processes and classifies the trajectory data on the fly. The combined data rate of 2.7 terabits per second is processed by the collection of 120 Xilinx FPGAs...

will emulate that energy density and thus provide a look at conditions very early in the evolution of the universe. These experiments might uncover new facts about matter, and promise to revolutionize our understanding of the miniscule world deep within atoms to the vastness of the universe.

Two beams of atomic particles called “hadrons” – either protons or lead ions – will travel in opposite directions inside the circular accelerator, gaining energy with every lap. Physicists will then make

the beams collide head-on. Teams of scientists from around the world will analyze the particles created in the collisions using special detectors in a number of experiments performed in the LHC.

The Role of Xilinx Virtex-4 FX FPGAs

When the counter-rotating beams of hadrons collide at extremely high speed they create a storm of subatomic particles. To monitor the particles generated by the collisions, the ALICE experiment

uses special photo-detectors that can measure the position of thousands of particle trajectories generated in every collision to a fraction of a millimeter.

The Transition Radiation Detector (TRD) has 1.2 million analog detectors. The system converts each analog signal to a 10-MHz, 10-bit data stream. The 540 individual detectors are combined into 18 super-modules. Their individual analog signals are pre-processed by 67,000 front-end chips. This generates a total

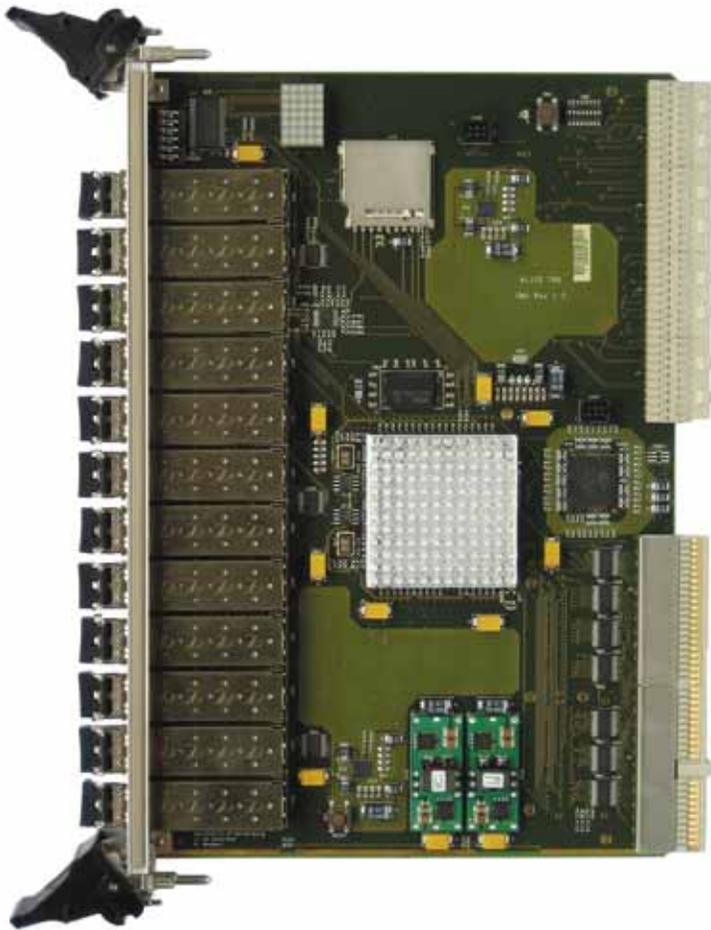


Figure 3 – A track matching unit card with the Xilinx XC4VFX100 Virtex-4 FPGA



Figure 4 – One of many racks containing the TMU cards that filter and track trajectory data from the lead ion collision.

data stream of 120 terabits per second of raw data.

The system preprocesses and compresses this data locally so that it can be sent out on 1080 optical links, each carrying data at a rate of 2.5 Gbps. These optical cables run to racks filled with 90 Track Matching Unit (TMU) cards. Each of these cards, shown in Figure 3, has 12 optical-to-electrical converters connected to the 12 multi-gigabit transceiver inputs of a single Xilinx Virtex™-4 FPGA.

Each XC4VFX100 device performs the first-level data reduction simultaneously and independently, and processes and classifies the trajectory data on the fly. The combined data rate of 2.7 terabits per second is processed by the collection of 120 Xilinx FPGAs, 90 of them in racks of TMUs (Figure 4).

The ALICE designers connected the remaining 30 FPGAs in a tree structure to higher level modules, where the final trigger decision (capturing the important content and filtering out redundant content) is performed by the FPGA at the top of the tree. With the help of powerful algorithms that eliminate repetitive, redundant, or unimportant data, the complete system is capable of fitting and selecting more than 20,000 track parameters within a microsecond, while preventing information overload in the CERN data processing and storage system.

Each XC4VFX100 FPGA has two embedded IBM PowerPC microprocessors, one of which runs the Linux operat-

ing system to perform system verification and housekeeping.

The Higgs Boson

The ALICE experiment is the most ambitious effort to date from CERN, but it is certainly not the last one they plan to conduct. Indeed, CERN scientists hope that ALICE's sister projects ATLAS and CMS will be able to produce the elusive Higgs boson.

In 1964, physicist Peter Higgs and his colleagues hypothesized the existence of a massive scalar elementary particle, now dubbed the Higgs boson. Physicists have added the Higgs boson to the Standard Model of particle physics, but no experiment to date has been able to confirm its existence.

CERN scientists hope that the Higgs boson particle might explain how elementary particles acquire properties such as mass. This would then be a significant step in the formation of the Grand Unified Theory and research of the nature of dark matter and dark energy. ●●

CERN and the Six-Billion Dollar Experiment

CERN is the French acronym for the European Organization for Nuclear Research, more appropriately called the European Laboratory for Particle Physics. CERN is the world's largest institution dedicated to high-energy research in subatomic particles.

CERN was founded in 1954 and is located near Geneva, Switzerland. Its annual budget of nearly U.S. \$1 billion is provided by 20 European member states plus eight observers, including the U.S. Almost 8,000 scientists and engineers – about half of the world's particle physics community – work on experiments conducted at CERN and analyze the results. Work at CERN was honored twice with Nobel Prizes in Physics in 1984 and 1992.

Most of the activities at CERN are currently directed toward building the Large Hadron Collider (LHC) and developing experiments for it. CERN expects to start its experiments in mid-2008.

Scientists expect to run several experiments on the LHC and have already scheduled six: CMS, ATLAS, LHCb, TOTEM, LHC-forward, and ALICE.

CERN is famous not only for its basic research in subatomic physics but also for a variety of technological breakthroughs. The best known is Tim Berners-Lee's invention of the World Wide Web in 1989, originally intended to improve communication between scientists associated with CERN.

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Using the JTAG Chain for Accurate System and Intra-Die Power and Thermal Analysis

New boundary scan techniques using Xilinx System Monitor test more aspects of system behavior.

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Engineers typically use the boundary scan chain to program devices such as CPLDs or flash memories. But more engineers should be tapping into the power of boundary scan as a way of extracting detailed information about how boards or systems are functioning.

With the recent introduction of the Xilinx® System Monitor function inside the latest Virtex™-5 FPGAs, you can now collect voltage and temperature information from within the FPGA using the same Joint Test Action Group (JTAG) test access port (TAP) traditionally used for boundary scan functions and programming devices.

And by using equipment and test scripts provided by Xilinx partner XJTAG, or by writing your own scripts, you can more easily verify analog signals at various points in the circuit from within the boundary scan

test environment. XJTAG's boundary scan test system helps engineers test devices such as discrete temperature sensors, DACs, or VGA ports.

System Monitor: A Device-Level Test Probe

The System Monitor is analog circuitry within the Xilinx Virtex-5 FPGA architecture that samples on-chip temperature and voltage (Figure 1). The dedicated System Monitor circuitry – which is built around a 200-kps ADC by default – performs a continuous sequence of measurements on the FPGA die temperature, as well as V_{CCINT} and V_{CCAUX} supply voltage levels. This feature in Virtex-5 devices eliminates the added complexity and cost of implementing external monitoring components to a system.

Moreover, the System Monitor feature allows you to take power supply measurements from the die itself (inside the package), which is not possible using an external ADC.

You can also use System Monitor to get accurate thermal readings. Traditionally, engineers used thermal diodes to monitor die temperatures, but they had to pay careful attention to the PCB layout because diode measurements are highly sensitive to

noise from other devices and features on the PCB, as well as other implementation details such as signal offsets and tolerances. The new System Monitor gets around that issue. It incorporates a temperature sensor on the FPGA die to allow you to take accurate temperature readings from the die itself (Figure 2).

These power and thermal monitoring capabilities allow for the implementation of safety functions such as power-on self-check or over-temperature power down. System Monitor's internal power supply measurements are accurate to within $\pm 1\%$, while monitoring of the on-chip temperature sensor is accurate to $\pm 4^\circ\text{C}$ in the -40°C to 125°C range.

The System Monitor circuitry also includes an integrated multiplexer that not only supports inputs for the two on-chip voltage-sensing channels and temperature sensor, but also accepts inputs from as many as 17 additional analog sources external to the FPGA. This means that you can use System Monitor to monitor various off-chip analog signals. It supports off-chip inputs that are single-ended or differential signals, up to 1.0V in amplitude; thus, you can connect to many types of sensors, including shunt resistor-based current sen-

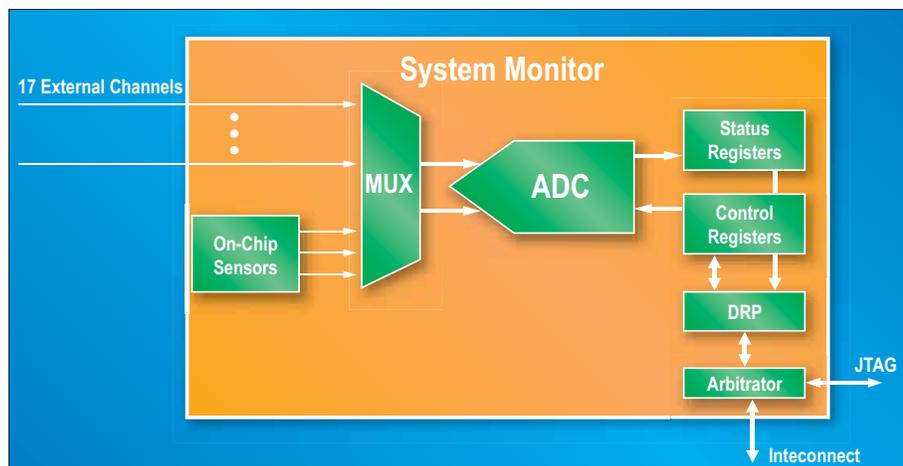


Figure 1 – System Monitor allows you to monitor voltages and temperature of a Virtex-5 FPGA die and as many as 17 other analog sources that can impact overall system performance.

sors, accelerometers, position sensors, and external temperature sensors.

The System Monitor control system also includes an automatic channel sequencer that allows you to define which parameters you want to monitor. You configure System Monitor by setting up its control registers. To do this, simply instantiate System Monitor in your design or write to the control registers over JTAG. The Xilinx ISE™ software tool suite also includes a utility called the System Monitor architecture wizard to walk you through the instantiation process.

Turning on the TAP

By designing System Monitor to deliver this data directly to the FPGA's JTAG TAP, Xilinx has opened up many new opportunities for extracting detailed information from prototype or production systems. Moreover, you can import the data into boundary scan test gear that operates at a high level of abstraction.

Although most engineers are familiar with using boundary scan to program devices in situ, many remain unaware of its power as an unobtrusive debugging and test solution. Applying tests through the JTAG TAP means that you no longer need to physically attach test probes to a development board or production assembly. Attaching probes is time-consuming and leaves the test strategy vulnerable to errors.

More importantly, it is impossible to physically probe modern BGA- and CSP-

type device packages because the ball pitch is so fine and is located under the device's body. And as the industry increasingly uses these packages in new ICs, it is effectively reducing the amount of test coverage you can achieve using conventional test techniques.

Boundary scan testing, as defined by the Joint Test Action Group and ratified as IEEE1149.1, specifies a four-wire TAP and boundary scan architecture that engineers can implement in their IC designs to facilitate product testing later in the IC development cycle. The four-wire TAP interface allows engineers to read values into and out of pins or internal registers of JTAG devices. And with access to these pins, you can debug and test other devices on the circuit board, such as FPGAs, EEPROMs, RAMs, and flash memory.

Using boundary scan test equipment, you can perform quick net-level diagnostics without having to rely on embedded test software or functional tests. The PCB doesn't need to be running for you to use it, so you can quickly verify basic functionality as soon as first prototypes return from assembly, even if the board will not boot up. You can also carry out basic checks, toggling individual pins or buses

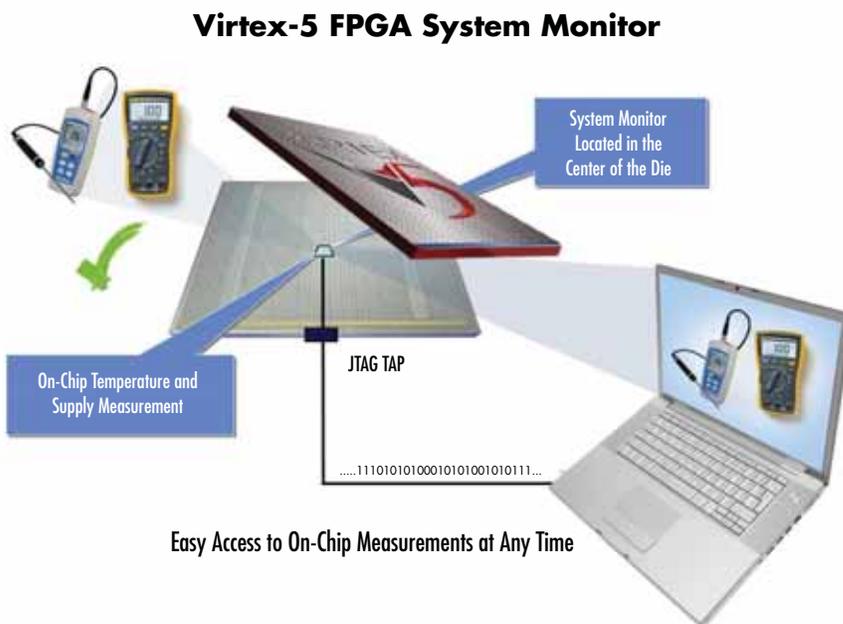


Figure 2 – The System Monitor sensor, located in the center of the Virtex-5 device die, provides valuable on-chip voltage and temperature data accessible during product development, when the device is in mass production, or even after deployment in the field.

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Engineers at XJTAG, working with Xilinx and the Virtex-5 LXT ML505 development board, developed several turnkey test scripts that allow XJTAG boundary scan test solution users to access data from System Monitor.

to locate shorts, breaks, poor joints, or incorrect connections.

The test ports of all JTAG devices in the system are interconnected at the board level, setting up a serial scan chain that you can access through a single connector at the edge of the board. As the numbers of JTAG-compliant devices per board increase, emerging JTAG testers can access a greater proportion of the total nets, thereby increasing overall test coverage.

By manipulating the scan chain to set up suitable test patterns, you can also collect

modern boundary scan equipment, such as the XJTAG system, has raised achievable test coverage by using the JTAG chain to its maximum potential. In practice, XJTAG customers are now achieving more than 90% test coverage for complex boards.

Extending Boundary Scan Capabilities

Now that Xilinx System Monitor allows you to easily collect analog values from inside Virtex-5 FPGAs, those of you already familiar with boundary scan testing can apply yet another valuable set of tests

information using the boundary scan chain even before configuring the FPGA. This allows development engineers, for example, to verify system power rails and assess basic cooling provisions before finalizing the FPGA configuration.

Because Xilinx implemented the sampling circuitry in hardware on the FPGA silicon, you can apply the System Monitor functions at any time in the product lifecycle. For example, if a system exhibits persistent overheating or if a power supply starts to exhibit signs that it is defective in the lab or even in the field, you can immediately apply a test to read the System Monitor data through the JTAG TAP without reconfiguring the FPGA.

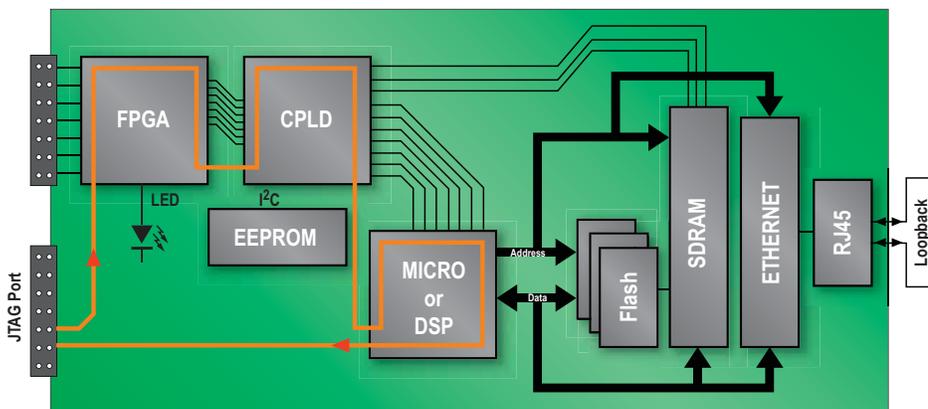


Figure 3 – Thanks to the growing JTAG compliance in modern PCB design, you can use boundary scan to perform many more types of tasks and tests.

responses from components that do not offer a boundary scan test interface, provided that the components you want to access are connected to the same net as a compliant device. This technique is sometimes referred to as cluster testing, and provides a way to test non-JTAG devices such as external connectors, video chips, IIC devices, Ethernet controllers, LEDs, or switches.

For example, you can also use the JTAG chain to drive an Ethernet test packet to a non-JTAG Ethernet controller on the board and verify its response (Figure 3). Similarly, it is possible to test SRAM devices, as well as SDRAM, DDR, and DDR2 chips – even though these are not JTAG-enabled. These examples show how

through the TAP. Virtex-5 device users can import data from the 17 external analog channels into the boundary scan test environment through System Monitor.

The use of the Virtex-5 System Monitor feature requires PCB design engineers to follow a certain minimal set of design guidelines. These guidelines are documented in the applications section of the Virtex-5 System Monitor User Guide (www.xilinx.com/support/documentation/user_guides/ug192.pdf).

Once the PCB support is in place, it's time to take advantage of System Monitor's many capabilities. For example, because the System Monitor ADC is operational on power-up, you can extract valuable system

XJTAG Simplifies Emerging Uses of Boundary Scan

Engineers at XJTAG, working with Xilinx and the Virtex-5 LXT ML505 development board, developed several turnkey test scripts that allow XJTAG boundary scan test solution users to access data from System Monitor. XJTAG can display die temperature, supply voltages, and off-chip analog values directly onto a workstation, and it allows you to verify that the values System Monitor and XJTAG collect are within specified tolerances.

Figure 4 is a code snippet of a simple set of tests that users can generate in XJTAG's high-level scripting language, XJEase, to check the operating parameters of the Virtex-5 FPGA. In the function call `Test`, you first configure System Monitor. The test then reads individual inputs and checks them.

Figure 5 shows code that checks the device's temperature. If the temperature is out of tolerances, the test displays an error. This example shows how you can access Virtex-5 System Monitor using simple functions provided on the XJTAG website.

XJTAG also supports customized tests that can, for example, record System

Monitor data for fault detection or traceability purposes. You can also write scripts to have XJTAG check for peak values, respond to thresholds, or apply an averaging algorithm to the data from System Monitor.

```
//-----
Test() (INT result)
//-----
INT temp;
  result := 0;

  Config_SysMon() ();

  Read_Internal_Temp() (result);
  Read_VAUX() (result);
  Read_VINT() (result);
  Read_RefP() (result);
  Read_RefN() (result);

  IF (result != 0) THEN
    result := RESULT_FAIL;
  ELSE
    result := RESULT_PASS;
  END;

END;
```

Figure 4 – Code snippet showing how to set up and test some of the System Monitor inputs using the XJEase scripting language.

You can create scripts using XJEase, which XJTAG includes as part of the XJTAG environment. XJEase allows you to work at a high level of abstraction from the raw boundary scan data. You can also write test scripts specifically for devices, whether or not the devices are in the boundary scan chain. You can store these scripts and even reuse them for future projects.

XJTAG will generate a new test sequence automatically each time the netlist data indicates a change to the board, which saves you from manually rewriting the test routine. In contrast, older types of boundary scan test equipment typically produce board-centric test sequences that are laborious to update with each design change.

As this device-centric scan approach to test development increases in popularity within the engineering community, many XJTAG users have begun posting their proven pre-written scripts on XJTAG's website. Customers who have current support contracts with XJTAG can download these scripts from www.xjtag.com free of charge and incorporate them into their test routines. And if the website does not have the exact device you are looking for, simply download a similar script and customize it for the device you want to test.

Scanning the Future

The scope of the interactions possible between System Monitor and XJTAG highlights the potential for boundary scan test systems to support innovative on-chip features supporting verification, debugging, parameterization, and calibration. By accessing silicon features implemented in the core of FPGAs – or other devices such as processors, memories, or control ICs – it becomes possible for boundary scan to perform functions such as virtualizing DIP switches, calibrating digital filters, or adjusting analog settings or threshold values. Plus, you can now achieve this quickly, whether the product is at the development stage, in volume production, or operating in the field.

For engineers already using the boundary scan chain to test the functional nets of prototype or production assemblies, System Monitor now allows vital-signs monitoring from within the boundary scan environment. Those of you who are more ambitious will certainly step up and take advantage of this new ability to see even more deeply into the system. And in the future, as the technique becomes more mainstream, expect to see customized test scripts that reach into even the most inaccessible aspects of product designs. 🌈

```
//-----
Read_Internal_Temp() (INT result)
//-----
  INT temp;
  Read_Temp() (temp);
  IF ((temp < (Die_Temp - Temp_Margin)) || (temp > (Die_Temp + Temp_Margin))) THEN
    PRINT("Die temperature = ",temp,"C. ** OUTSIDE LIMITS **\n");
    result := result + 1;
  ELSIF (DEBUG) THEN
    PRINT("Die temperature = ",temp,"C\n");
  END;
END;

//-----
Read_Temp() (INT temp)
//-----
  Read_Channel(0) (temp);
  temp := ((temp * 20159) / 40960) - 273;
END;
```

Figure 5 – Code snippet for testing the temperature of the Virtex-5 FPGA

Solving FPGA I/O Pin Assignment Challenges

Here's a step-by-step methodology to help you pinout complex FPGAs.



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I/O pin assignment is one of the main challenges facing designers integrating large FPGA devices onto PCBs. Many designers find the process of defining the I/O pin configuration, or “pinout,” of large FPGA devices and their advanced BGA packages an increasingly difficult task for a seemingly ever-expanding number of reasons. But with a mix of smart I/O planning and new tools, you can remove the pain from the pinout process.

The task of defining an I/O pinout from FPGA to PCB is a major design chal-

lenge that can make or break a design. You must balance requirements from both the FPGA and PCB perspectives while designing both sides in parallel. If you prematurely optimize a pinout specifically for the PCB or the FPGA, it can lead to design issues in the other domain.

You need to be able to visualize both the PCB placement and FPGA physical device pins, along with the internal FPGA I/O pads and related resources, to understand the ramifications of your pin assignment choices. Unfortunately, as of today there isn't just one tool or methodology to address all of these co-design concerns.

What you can do, however, is combine various techniques and strategies to optimize the pin-planning process and add

new co-design tools like Xilinx® PinAhead technology to devise an effective pinout methodology. Xilinx includes PinAhead in the ISE™ software design suite 10.1.

At Xilinx, we have developed a rule-driven methodology in which we define an initial pinout that considers both the PCB and FPGA requirements, allowing each design group to begin their respective design processes as early as possible by using a pinout that should be very close to the finalized version. If the design requires changes because of PCB routability or internal FPGA performance issues late in the process, this methodology is such that those issues are typically localized, requiring you to make only small changes in either design domain.

Step 1: Evaluating the Design Parameters

So where should you start? You should begin to formulate an I/O strategy as early as possible. But you may find this task difficult in the absence of an optimal tool for the job or a complete netlist.

First, let's examine the PCB physical parameters and limitations by answering a few questions:

- What is the preferred layer count, trace width, and via size?
- Do the PCB parameters limit the FPGA package types that you can use, such as BGA?
- Are there any fixed interface locations for the FPGA on the PCB? Other chips, connectors, or placement restrictions?
- Which high-speed interfaces need special attention?
- Can you visualize a placement strategy to enable the shortest interconnect?

You may find it helpful to draw a diagram of the proposed PCB placement – including all major components with critical interfaces and buses – to determine

the best FPGA pin assignment locations. Make sure that you draw the components on the side of the board where you plan to mount those components. Make note of interfaces that will require special attention, such as high-speed buses and differential pairs (Figure 1).

Next, examine the layout of the FPGA device to understand where the physical resources exist on the silicon. List the various voltages and clocks you are using in the design to begin to isolate the interfaces the design will require. Then determine if your design uses specific I/O interface resources such as giga transceivers (GTs), BUFRRs, IODELAY, and digital clock managers that require you to define and route I/O pins in close proximity to each other.

Now it's time to locate the FPGA resources, such as PowerPCs, DSP48s, and RAM16s, in the design. It makes sense for you to target any related I/Os to the I/O banks closest to those resources. See if you can group any of the I/O signals into interfaces; this will help during pin assignment. Finally, determine the configuration mode for the FPGA.

Step 2: Defining Pinout Requirements

Once you understand the main FPGA interfaces and have created a mockup of the physical layout, you can start to define the pinout. Some designers like to use a spreadsheet containing all of the I/O signals to keep track of the pins. You can group them by voltage, by clocks, by interface, or by bus. This method is really quite valuable because it helps you begin to formulate the groups of signals you will assign in close proximity. At this stage, you should also identify critical interfaces that must exit the device on a particular edge or use outside physical pins for optimal PCB routing.

After examining both the FPGA and PCB requirements and defining the major interface locations, the next step is to begin assigning pins to I/O banks based on all of the preceding criteria. This is where the real work begins. In the current flow, pin assignment is a time-consuming task that can involve a lot of trial and error to solve any performance and signal integrity concerns. Designers have traditionally performed this task freehand, because EDA and chip ven-

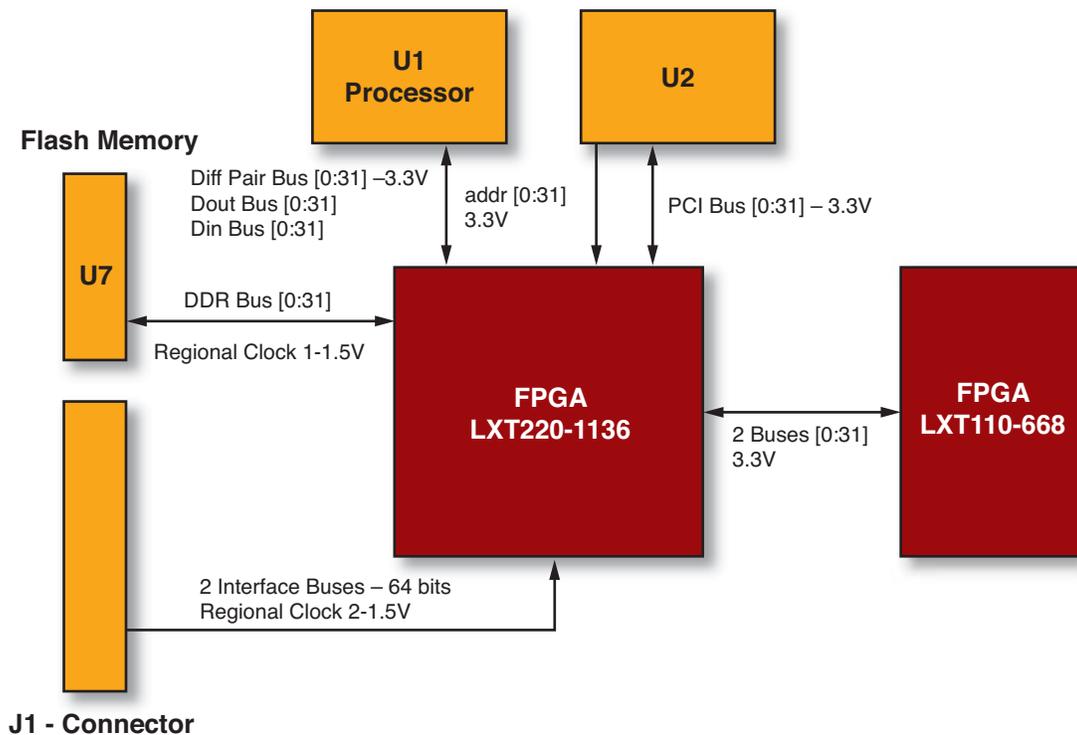


Figure 1 – Create a PCB connectivity diagram

dors didn't offer tools to effectively help designers visualize the two domains.

But now, Xilinx has a tool for the job. PlanAhead Lite, which we've included in the 10.1 release of the ISE Foundation™ software toolset, is a subset of the PlanAhead™ software design, analysis, and floorplanning tool. It includes a tool called PinAhead, which addresses both PCB and FPGA design concerns and makes I/O pinout configuration much easier for designers.

Rather than go into detail about every feature of the tool, let's see how we can use it in the context of an I/O pin assignment methodology. If you want more detailed information about PinAhead, including a video demonstration and tutorial, visit www.xilinx.com/planahead.

Step 3: Using PinAhead for Assigning the Pinout

The PinAhead environment displays a set of views applicable to the task of exploring and assigning I/O port signals to physical package pins or I/O pads on the die (Figure 2).

PinAhead has virtually the same graphical environment as PlanAhead software, clearly displaying the silicon I/O pads and related resources in the "Device" view and the physical device pins in the "Package" view. The views present both I/O port and physical pin information so that you can cross-select to explore the logical design and physical device resources.

You can use PinAhead in the absence of a design netlist to explore device resources or to start the I/O pin planning process. The "Package Pins" view lists device package specifications according to the device data sheets, so in most cases you won't have to cross-reference the device data sheet when configuring the pinout. The Package Pins view table categorizes I/O banks, allowing you to cross-select and highlight I/O banks in both the Device and Package views. The view clearly shows the relationship between the physical pin location and the I/O pad location on the die, which simplifies optimal I/O bank selection. The Package Pins' "Pin" view also displays information for each pin in the I/O bank.

You can begin creating I/O ports from scratch using the PinAhead interface or by importing them from a comma separated

value (CSV) format spreadsheet, HDL source file headers, or a synthesized netlist and UCF format constraints file. The "I/O Ports" view displays all of the I/O port signals you have currently defined in the design, and the bus folders display the grouped buses and differential pair signals.

You can sort the Package Pins and I/O Ports views in a variety of ways. You can toggle the list views to display a category-based list or a flat list, and with just a mouse click, sort the Package Pins view to display all available global clock- or regional clock-capable pins. You can also export the information to a CSV format spreadsheet to use as a starting point for pinout configuration.

PinAhead also has an interface to allow you to selectively prohibit I/O pins, groups of I/O pins, or I/O banks from having I/O ports assigned to them by PinAhead. You can select and prohibit pins in the Package Pins, Device or Package views. For example, you can sort the Package Pins view and prohibit all VREF pins.

PinAhead allows you to group related I/O ports and buses into an "interface." This grouping simplifies I/O port management and assignment tasks by allowing you to handle related I/O ports as a single entity. The interface grouping makes it much easier for you to visualize and manage all of the signals associated with a particular logic interface.

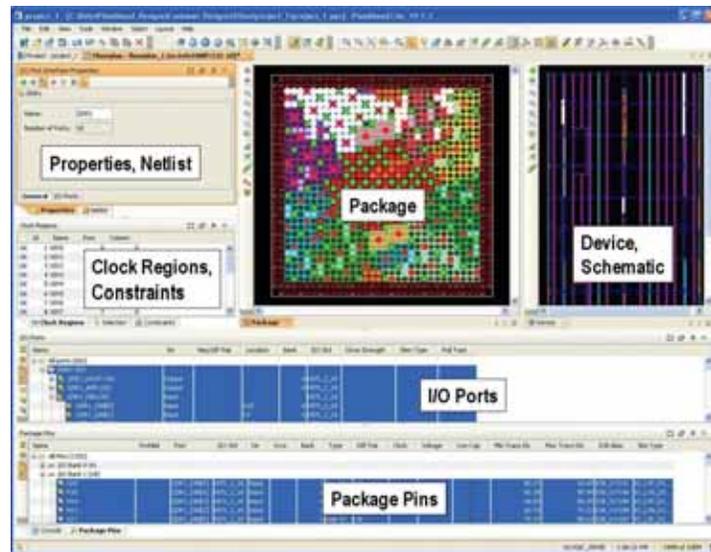


Figure 2 – The PinAhead environment

You can easily copy interfaces from design to design or use them to generate interface-specific PCB schematic symbols. The interfaces appear as expandable folders in the I/O Ports view, and you can add additional I/O ports to the interface by selecting them in that view and dragging them into the interface folder.

As you create the I/O ports, you can assign them to package pins or I/O pads. Before you do this, it pays to examine the I/O ports' initial PCB interconnect sketch and consult with the PCB designer to understand the desired locations and other considerations for placing the various I/O port interfaces. Proper bus order and edge proximity can aid PCB routing significantly and save design time.

You can assign individual pins, buses, and interfaces to I/O pins by dragging them into either the Device or Package views. You can assign the entire group of pins to the selected I/O pins using various assignment pattern modes. The available modes include "Place I/O Ports in an I/O Bank," "Place I/O Ports in Area," and "Place I/O Ports Sequentially."

Each mode offers a different assignment pattern for the I/O ports you are assigning to pins. Using these modes, you will see information about the number of ports you are placing by looking at the pop-up window on your mouse cursor's tip. This mode remains active until you have placed all of the selected I/O ports.

The Device view graphically displays all clock regions and clock-related logic objects, making I/O assignment based on clocks much easier and intuitive. Selecting a clock region will display all of the I/O banks, clock-related resources, and device resources associated with it.

PlanAhead software attempts to maintain your correct-by-assignment rules. With your guidance, the tool will assign differential pair ports into proper pin pairs. As you interactively assign I/O ports with the tool, the tool runs design rule checking (DRC) to ensure legal placement.

The tool's default setting runs in interactive DRC mode, but you can toggle it off if you choose. The tool checks for conflicting voltages, VREF pins, or I/O standards, as well as noise-sensitive pins located near GT devices. When it finds an error, the tool displays a Tooltip indicating why you can't assign an I/O port to a specific pin.

You can activate PinAhead's "Autoplace" command to direct the tool to automatically place all or any selected I/O ports to package pins. The Autoplace command will obey all I/O standard and differential pair rules and will place global clock pins appropriately. The command will also attempt to group interfaces as much as possible.

The Device view graphically displays all clock regions and clock-related logic objects, making I/O assignment based on clocks much easier and intuitive. Selecting a clock region will display all of the I/O banks, clock-related resources, and device resources associated with it. This makes the process of regional clock planning much easier by allowing exploration of the available resources along with their physical relationship.

You can also use PinAhead to place other I/O related logic in your design, such as BUFs, BUFRs, IODELAYS, IDELAYCTRLs, and DCMs. You can easily locate these objects and placement sites in PlanAhead by using the "Find" command. To selectively explore and expand logic and logic connectivity, use the tool's "Schematic" view.

You can also lock the placement of specific I/O-related logic with PlanAhead software by selecting the logic in any view and dragging it onto sites in the Device view.

PlanAhead software will only allow you to place logic on appropriate sites. A dynamic cursor identifies the proper site locations as you are dragging a logic object over the design.

Step 4: Running DRC and WASSO for Legal Sign-Off

Once you've completed your pin assignment, you can use PinAhead's vast set of DRC rules to run a sign-off DRC and ensure that the design is error-free before running the PlanAhead software implementation tools. The tool has many I/O and clock-related rules to ensure that I/O placement is legal. You can select rules using the PlanAhead software DRC dialog.

If the tool finds rule violations, it displays a DRC results table with the errors. You can select the errors to investigate them further.

PlanAhead software also includes weighted average simultaneous switching output (WASSO) analysis to help you identify potential signal integrity issues with the pinout configurations. You feed the tool the parasitic characteristics of your PCB design; PlanAhead software will analyze the various I/O banks and their neighbors and report back the utilization and status of each I/O bank.

Step 5: Exporting the I/O Pinout

You can export the I/O port list and package pin information from PlanAhead software into a CSV format file, HDL header, or UCF file. The CSV file includes information about all of the package pins in the device, as well as design-specific I/O port assignments and their configurations. The package pin section of the list makes a great starting point for defining I/O port definitions in the spreadsheet.

You can also use the spreadsheet to automatically generate the PCB schematic symbols your group needs to begin the PCB layout. Sometimes, however, these symbols

are too large for the schematic; you'll have to break them up into several symbols. You can do this quite effectively using the interface groups created in PinAhead.

Providing this I/O pinout configuration in the form of a schematic symbol gives PCB designers a good foundation to start developing an effective PCB layout. Because you developed the initial pinout with the PCB interfaces in mind, it should be fairly close to the final pinout configuration.

And if you do need to swap pins during layout to facilitate routing, you should be able to make those changes easily – because more likely than not the pins that require swapping are conveniently located within the I/O banks. And the methodology shouldn't affect the FPGA design too drastically. You can transfer revised pinout spreadsheets or UCF files between your PCB and FPGA designers to keep in sync with any modifications you've made.

You may also wish to tie the unused pins or certain configuration pins to either VCC or GND (ground) to help with signal noise concerns and facilitate proper FPGA functionality. At Xilinx, we are currently working on a function for the next version of PinAhead that will provide an interface for FPGA designers to specify these pins and include the pins' connections in the output CSV spreadsheet. This will allow PCB designers to more easily identify pins and connect them appropriately.

Moving forward, as FPGAs employ more complex functions and use more advanced packages, devising a solid FPGA and PCB pinout methodology will become imperative. Although we think you'll find PinAhead Lite a great help in executing your co-design-savvy pinout strategies today, we are already working on improvements to the tool to better help you tackle pinout challenges and get the job done. 🌟

Replacing Obsolete Video Game Circuits with Xilinx CPLDs

Replacing obsolete parts with a Xilinx XC9536XL CPLD gives new life to a Vectrex video game system.

In this article, designer In Choi describes a project for his home business in which he replaces a defective part in a 1980s game system to show his full-time employer that they can adopt a methodology using Xilinx® programmable devices to replace a range of parts that other semiconductor vendors are no longer producing.



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Parts obsolescence is nothing new, but it has attracted more attention recently, particularly in the semiconductor industry. Sometimes chip companies no longer produce parts for older products; others go out of business.

Although no single optimal solution exists, you can typically manage parts obsolescence using one of three methods:

- Find a form, fit, and functional substitute.
- Redesign the subsystem containing the obsolete part.
- Replace or redesign the entire system.

From a practical perspective, the last two methods are generally too expensive; it would probably be more cost-effective to replace the subsystem or the entire system.

Thus, the first method is the most practical, and we'll show how we at Retro Devices Technology did it using a Xilinx® XC9536XL CPLD – specifically targeted for 5-V transistor-to-transistor logic (TTL) gates and digital logic functions – to replace a 74LS32 microcircuit in the PCB of a 1980s video game system called Vectrex. For the sake of this project, we are assuming that the 74LS32 is obsolete.

Vectrex System Overview

The Vectrex video game system was originally licensed and distributed by General Consumer Electric (GCE) in the early 1980s. It was a self-contained game unit much like the full-sized game machines in arcades but scaled down for home use. It was somewhat portable as long as you could plug it into an AC outlet.

The Vectrex system comprises an 8-bit 6809 microprocessor running at 1.5 MHz, an AY-3-8912 sound chip from General Instruments, a 9 x 11-inch monochrome monitor, and a game controller with four buttons, as shown in Figure 1. The Vectrex uses a vector graphics system as opposed to a pixel-based raster graphics system.

[The Vectrex video game system] was a self-contained game unit much like the full-sized game machines in arcades but scaled down for home use. It was somewhat portable as long as you could plug it into an AC outlet.



Figure 1 – The Vectrex gaming system

In this design, we used the XC9536XL CPLD to replace a part called the 74LS32 Quad-OR gate in the Vectrex video game system. The original designers used this part as decoding logic to perform read and write access to the RAM by the processor in the Vectrex (more information is available from the Vectrex website at www.vectrex.nl). I chose to replace the 74LS32 with the XC9536XL CPLD to minimize development cost and to prove out my scalable design methodology simultaneously.

Design Description

Our design requirements were to keep the physical size of the replacement part as small as possible, meet all of the electrical specifications, keep the power level at least equal to the obsolete part, and use a replacement part that is configurable to replace as many 5-V TTL 74LS series gates and digital functions as possible.

I created the customized functions using VHDL, then synthesized the code into a configuration file and programmed the design into the CPLD. For the sake of this

article, I'll refer to the replacement part as the retro logic device (RLD). Figure 2 shows the fully operational RLD device next to the 74LS32.

The design footprint of the RLD is a little larger than the 74LS32 because of the PCB vendor's manufacturing limitations, but there was sufficient room in the original game circuit board to accommodate the RLD.

The electrical performance of the RLD was a non-issue, since the Xilinx XC9536XL CPLD already has TTL I/O compatibility. You can read the XC9536XL data sheet if you are not familiar with the specifications or how to properly power the I/O for TTL compatibility.



Figure 2 – The RLD (left) and the original 74LS32 part it replaced (right)

The power of the RLD is also comparable to many 74LS series functions. I achieved this power compliance by using a 3.3-V low power voltage regulator on the RLD's PCB. I placed a bypass capacitor at the output of the voltage regulator to provide filtering for the CPLD.

From a signal integrity perspective, it is typically best to place the capacitor directly under the board and attach it to the CPLD's voltage and ground planes to provide the shortest (lowest inductance) path. However, the Vectrex circuit board didn't require a high level of performance.

I then placed a 6-pin JTAG connector on the RLD to configure the CPLD. Finally, I created a custom mating connec-

tor for the RLD for configuring the RLD. I attached this custom connector to the platform cable USB using flying leads.

Design Operation

I needed to find the right power source to configure the RLD. Therefore, I used a breadboard to power the RLD configuration before applying the design to the Vectrex circuit board. I achieved the power regulation using a 6-V power adapter from a development kit that was lying around. Experimenting with several capacitors and resistors, I came up with the appropriate current and voltage settings to properly operate the RLD.

The cost of low-end laptop computers has dropped significantly and their performance is quite good, so I did not need a high-performance modeling environment for this project. Therefore, I used a cheap laptop running Windows XP, loads of vendor trial software, and Xilinx WebPACK software, which is freely available for downloading from the Xilinx website. The laptop proved more than sufficient to run the software.

I used the Xilinx WebPACK to create the 74LS32 project, which essentially consisted of creating four concurrent statements in VHDL. VHDL is a simple code

for OR-ing two inputs to a single output, and I repeated the step three times to different I/O ports, making sure to use the proper I/O constraints file for the design.

I attached the laptop to the RLD with the cable. I then synthesized the 74LS32 VHDL code and downloaded the design into the RLD using the Impact tool integrated into Xilinx WebPACK.

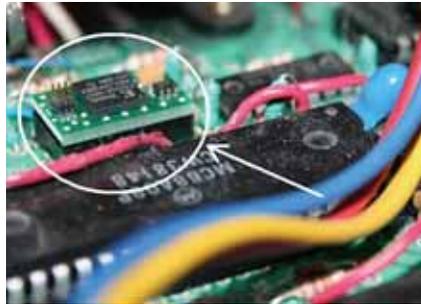


Figure 3 – The RLD placed on the Vectrex board

I then physically removed the 74LS32 part from the Vectrex circuit board. To make maintenance easier, I soldered a 14-pin socket onto the circuit board. I then inserted the RLD into the Vectrex game circuit board, as shown in Figure 3. I switched the Vectrex game system to “on” and played a game.

I created the RLD so that I could configure it while it was on the Vectrex circuit board. In general, using this method can often prove unpredictable and may even be catastrophic in some designs. If you are planning to use the method I’ve described here, be prepared to have a lot of sacrificial hardware on hand in case something doesn’t go as planned. If your configuration is successful and passes the no-smoke test, push the reset button on the Vectrex unit and everything should work fine. But do this at your own risk – and don’t call me if you smell or see smoke.

There will always be some degree of parts obsolescence, but this procedure serves as an alternate solution to manage it more effectively. If anything, it allows more time for managers to make economical business decisions. With further research and development, this scalable solution can be retargeted to replace other legacy devices of varying technologies and complexities, thus providing a truly unified solution to parts obsolescence.

Please visit our website at www.retrodevices.com for more technical information about the RLD, including purchasing information. 🌈

Design Notes

You may be wondering why I did this exercise. Wouldn’t it have been easier to buy a video game console from this or even the last decade? I didn’t do the design simply to restore the video game – I did it for a number of reasons.

First off, I think logic design is fun (and I’m lucky enough to get paid to do it). Second, I wanted to show that I could create the RLD to directly replace a failed part. But my main reason for doing the project was to create a methodology with an FPGA to show that there are indeed practical ways to overcome chip obsolescence.

The approach I demonstrated in this article is scalable. Although this article focuses on the configuration of an XC9500XL series CPLD to replace 74LS series devices, I could have conceivably applied the same method to replace even more complex devices in this system, even the 6809 microprocessor on the Vectrex game board. The 6809 VHDL IP core is readily available from multiple sources and can fit within a Xilinx Spartan™-II FPGA.

In fact, with the resources available to us today through the Internet, a designer could conceivably add more functionality to the processor and actually improve the Vectrex system, or develop their own version of the microprocessor. If you do a search on the Internet, you will be amazed at how many people have developed their own processors.

This isn’t the first time I’ve used an FPGA to replace an obsolete part. Indeed, over my long career I’ve done many of these projects. I’m currently working on a project at my full-

time job, in which my employer has asked me to port a series of 12-year-old FPGA designs that were originally implemented on one-time programmable FPGA technology – technology that is now obsolete – to a newer series of one-time-programmable FPGAs from the same manufacturer. The design files comprise EDIF files, logic schematics, Abel code, and circuit diagrams (Does anyone remember Abel?).

To get around the challenges of moving the design from an obsolete OTP FPGA to a newer OTP FPGA, I am currently trying to work with my managers to run a pilot project based on the RLD methodology demonstrated in this article.

For the pilot project, I’ve outlined a new methodology in which I’ll review all the circuit boards and identify and create a list of obsolete parts. From the list, we’ll group the parts based on packaging and find the largest design in the list using the same package. We can then select a Xilinx FPGA that can fit the largest design.

Better yet, we can select the largest Xilinx part possible that fits comfortably within the package footprint and use the extra resources to add functionality from other FPGAs on one device, add new functionality, or simply avoid any unanticipated design problems. We can then create a custom circuit board with the FPGA and mass-produce it. This methodology is repeatable for any other parts that are now obsolete, so long as they have a suitable package footprint.

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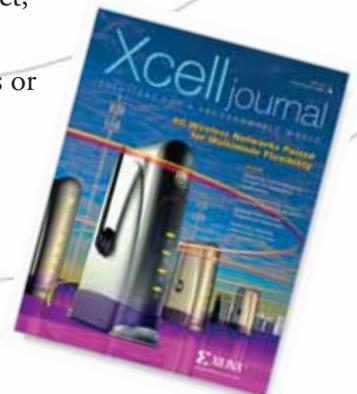
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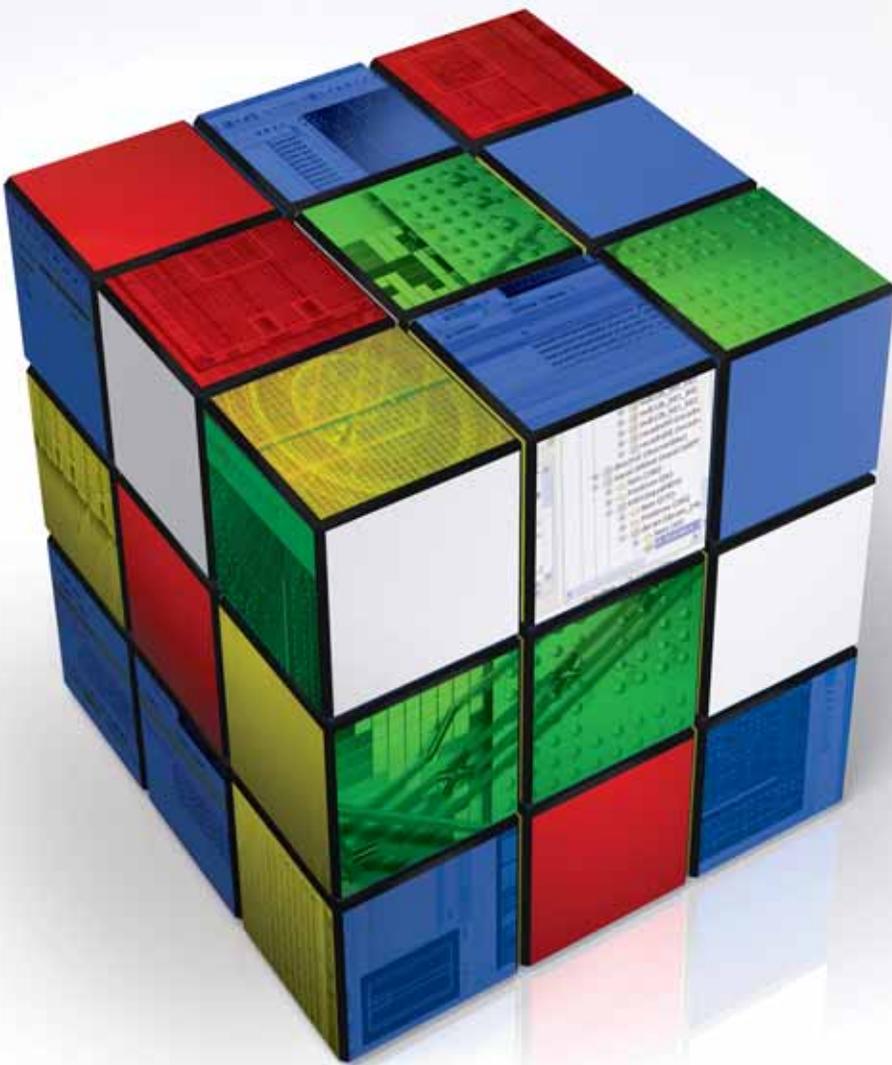


Identifying and Solving Timing Problems in Xilinx FPGA Designs

In this first edition of Ask FAE-X, the all-knowing, all-seeing FAE-X gives advice on finding and fixing timing constraint problems.

Welcome to Xcell Journal's new column, "Ask FAE-X." In each issue going forward, one of our many field application engineers worldwide will assume the identity of the FAE-X and answer one of your questions or a question that users commonly ask our field support team.

If you have a question that you would like the FAE-X to answer in Xcell, send your question to Ask FAE-X's minion, mike.santarini@xilinx.com.



by Chris Dunlap
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It is heartbreaking to spend months on a design and then not meet your timing constraints. It can be almost as heartbreaking trying to figure out how to properly constrain the design to make sure that your design meets timing. Finding and fixing timing constraints is a common yet very tricky problem.

The frustrating thing about timing problems is that no one single cure solves every type of timing problem. The good news is that we can solve most timing problems by pushing the limits of the software, optimizing RTL code, or a little of both.

Because customers are usually very wary of sharing source code with FAEs, we generally try to solve their timing problems by helping them push the limits of their tools.

But before I get into that, the first thing we need to do is a basic analysis of the timing problem. The goal here is to root out anything obvious such as a clock pin at the top of the device, driving a digital clock

manager (DCM) at the bottom of the device, which in turn drives a global buffer (BUFG) at the top of the device.

Sometimes you can place pins in such a way that makes it impossible to meet timing. Usually you can discover obvious timing problems by inspecting the delays in the timing report. In any case, you will need to use a floorplanner to solve obvious problems by locking down the offending instance(s) to proper locations. A floorplanner will also help to visually understand the timing problem.

Use Current Software Tools

Assuming that the problem isn't an obvious one, to zero in on the cause we need to understand which device family and software version you are using. In general, each device family tends to have a single optimal software release. The best software for Xilinx® Virtex™-4 devices is ISE™ software version 9.2i, while the best software to date for Virtex-5 FPGAs is ISE software 10.1. (For this month's column, I used ISE software v10.1 and PlanAhead™ software v10.1.)

Synthesis tool versions matter as well, so when using the latest device architectures, it is really important to make sure that you have downloaded and are using the latest software builds. Software development almost always lags behind the hardware capabilities, so using old software with new device families is not something I advocate.

Unfortunately, some customers shy away from upgrading software for fear of dealing with new or unknown bugs. However, if you want to deal with timing challenges properly when using the latest device family, I strongly recommend downloading the latest software.

Once you have the best software release for the device family you are targeting for your design, you need to find the best set of implementation options. Unfortunately, there is no such thing as a magic set of options. There are thousands of different combinations that you can apply to implementation tools. The timing score – that is, the summation of total failed timing paths in picoseconds – will vary greatly depending on what implementation options you use.

Xilinx has several tools to help you find the best set of options for your design. ISE software now includes two tools: Xplorer, and more recently, SmartXplorer. SmartXplorer can take advantage of multiple processors to run multiple implementations with different options.

SmartXplorer requires Linux but is very easy to use. The command line is simple: `smartxplorer designname.edn -p xc5v1x110t-1ff1136`.

As long as the user constraints file (UCF) and netlist constraints file (NCF) have the same name, SmartXplorer will use the correct options automatically. The only other thing you'll need is the host list file.

Options	Timing Score	Run Time
Map : -timing -ol high -xe n -global_opt on -retiming on	651262	6h 26m
Par : -ol high		
Map : -timing -ol high -xe n	0	4h 25m
Par : -ol high		
Map : -cm area	380834	5h 19m
Par : -ol high -xe n		
Map : -timing -ol high -xe n -register_duplication -logic_opt on	0	5h 46m
Par : -ol high -xe n		
Map : -timing -ol high -xe n -global_opt on -retiming on -ignore_keep_hierarchy	666567	12h 34m
Par : -ol high -xe n		
Map : -cm balanced	172171	4h 4m
Par : -ol high		
Map : -timing -ol high -xe n -pr b -cm balanced	7235	6h 33m
Par : -ol high		

Table 1 – A SmartXplorer 10.1 example on Virtex-5 FPGA-based design

SmartXplorer can log in to other machines through secure shell/remote shell (SSH/rsh). Just add each machine name on a separate line in a file called `smartxplorer.hostlist`. If a machine has two processors, list that machine twice. Table 1 shows a set of results from SmartXplorer.

PlanAhead software also includes a feature similar to SmartXplorer called ExploreAhead, which supports distributed processing of place-and-route jobs across multiple Linux machines at the same time. The point of all of these tools is similar: to find a set of options in the implementation tools that will get the best timing score.

Notice how the options can have a drastic effect on the timing score and run times. It is also important to play with synthesis options. For instance, turning off hierarchy in synthesis often signifi-

cantly improves performance. Good constraints in synthesis can also make a difference in meeting timing.

PlanAhead Software

After you have played around with implementation options to come up with the best timing score, you can now start to effectively analyze the timing problem. PlanAhead software is a very valuable tool at this point because it allows you to visualize the post place-and-route design. You can also import the timing constraints and cross-probe the failed path to the placed component window.

When the tools make bad decisions, you can correct them by floorplanning modules

or hand-placing components. This can be – and often is – an iterative task that requires multiple runs to find the best way to floorplan the design to optimize timing. PlanAhead software's visual capabilities really do make that job much easier.

Using PlanAhead software, first create a project, importing either the HDL or netlist files into the tool. Once you've created a project, choose **File** → **Import Placement**. Select the post PAR (ncd) file from the best run to import the placement into the PlanAhead software project.

The tool will organize the PlanAhead software project into several windows. The top left window is the physical hierarchy, which describes the current area groups in the design. The selection window is beneath that and contains details on whatever data you have currently selected. The middle

Timing problems will vary, and the solutions to tackle them in PlanAhead software will also vary. Solving timing problems inside PlanAhead design tools requires practice.

window is the netlist window, which outlines the full netlist hierarchy. The far-right-side window is the Device view, which will now be populated with logic you've implemented in your design.

Next, import the timing analyzer report (TWR/TWX) into the tool. Choose **File → Import TRCE Report**. This step will add the timing report data in the bottom window. You should sort this window by worst-case timing slack to focus on the worst-case offenders first. Fixing the worst-case offenders will often solve timing problems in the whole design.

Once you select a failing path, PlanAhead software will select the instances and the connections in that failed path. Hit **F9** to zoom into that selection (see Figure 1).

This is where things might get a bit complicated. You must do some amount of inspection to understand why the place-and-route tool placed the primitives the way it did, and whether there is a better method for your particular design.

You can zoom into any of the highlighted primitives. Left-click a primitive and move it around to understand the connectivity. In the netlist window, you can also move up to the top-level block, which has the selected instance in it. Right-click the block name and choose a color for those selected instances. This will now show how this block was placed in the chip and if the grouping is close together or spread out.

Sometimes you will see that you need to lock down particular primitives better. Block RAM and DSP auto-block placements tend to be common problems in timing failures. In Figure 1, it is easy to see that PAR placed the Mult18 in a non-optimal location. The failing path has a block RAM, which feeds a Mult18, which in turn feeds a carry chain. The block RAM is high, the Mult18 is low, and the logic is high. If the routing didn't have to go up and down as well as sideways, it would have met timing.

Timing problems will vary, and the solutions to tackle them in PlanAhead software will also vary. Solving timing problems inside PlanAhead design tools requires practice. Let's tackle the timing problem in Figure 1 as an example. Following these steps will lead us to a solution:

1. Select the failed timing path so that the essential path is highlighted.
2. Right-click on one of the instances and choose **Highlight With** → color of choice.
3. In the left column, unplace the Mult18 that is second from the bottom. Right-click **Unplace**. This will open up room for the block RAM that is failing timing.
4. Move the Mult18 on the bottom left up one location by clicking and dragging.
5. Click and drag the block RAM on the right to the free block RAM location at the bottom left.
6. Select the failed timing path and verify that the path looks optimal (see Figure 2).
7. Choose **Tools → Clear Placement Constraints**. Click **Next** through the first option.
8. Select **Unplace All But Selected Instances**. Click **Next** through the remaining wizard.
9. If you wish to run implementation outside of PlanAhead software, choose **File → Export Floorplan**.
10. The tool will write out a new UCF called top.ucf. You can either use that or take the constraints in the file and add them to your original UCF.
11. Another option is to run implementation inside PlanAhead software.

Choose **Tool → Run ISE Place & Route** with ExploreAhead.

ExploreAhead has a couple of nice features, including:

- a) Automatic importing of constraints from the Device view to the UCF.
- b) Simplified importing of placement and timing results from runs implemented inside ExploreAhead.

Pblocks and Floorplanning

If you find a lot of timing failures in your layout, hand-placing typically won't solve these timing issues. Instead, you should create area groups.

One of several ways to create an area group (Pblock) is to right-click the block name in the Netlist window and choose **Draw Pblock**. Then draw a rectangle in the Device view where you would like to place that area group.

The tool will create a Pblock, and you'll be able to see a lot of information about it. The properties window will display the logic resources the Pblock requires and the resources available in the drawn group.

It can be quite an iterative process to floorplan a design. You'll find that you may have to do several runs to tune the area groups before they start working well. Also remember that less is sometimes more. You do not always need to area group the entire block. Focus on the failing primitives; you can group those and floorplan them alone.

You should use metrics on Pblocks to better understand functionality, such as how well-utilized the configurable logic blocks (CLBs) are in that area group (to see the available metrics, click on the **Metrics** tab in the top left window of PlanAhead software). This can help you determine if a lot of congestion exists in a particular area that is inhibiting routing. If there is a lot of congestion, you'll need to spread the logic out through floorplanning.

Once you've used PlanAhead software to squeeze out the best timing score, the last remaining task is to optimize the code. PlanAhead design tools now support HDL source. You can cross-probe timing problems back to the netlist or HDL, depending on what sources you imported.

Using the Schematic view, you can view the entire timing path. Just select the timing path from the timing results and hit F4. Watch out for logic that fans in and out of other modules. The tools must often spread out modules over the chip because of external interface requirements. If this happens,

you'll probably need to use pipelining in your design.

Block RAM or DSP output timing will commonly contribute to timing failures. You can often recover a full nanosecond or more by registering the output of these blocks.

Final Recommendations

If you are having problems with timing closure and you don't have PlanAhead software, I strongly recommend that you get it. This tool allows you to manage every aspect of solving a timing problem.

Using PlanAhead design tools, you can run ExploreAhead to find the best set of options. And because PlanAhead software is not tied to a particular ISE software release, you can also try different ISE software versions if you have multiple versions installed on your workstation. PlanAhead software's cross-probing features allow you to fully understand both the source and implementation of a design.

Timing closure can be a pretty tricky problem, but with the right versions of the right tools and a comprehensive timing closure plan, you should be able to locate timing problems in your designs quickly and get the job done. And with that, FAE-X bids you happy designing. 🎯

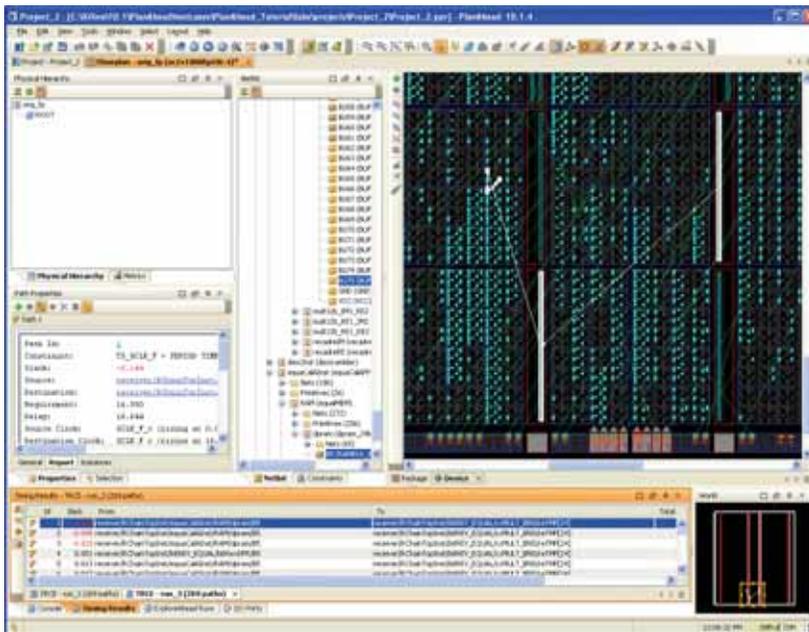


Figure 1 – PlanAhead software 10.1 shows an implemented run with a failed timing path highlighted

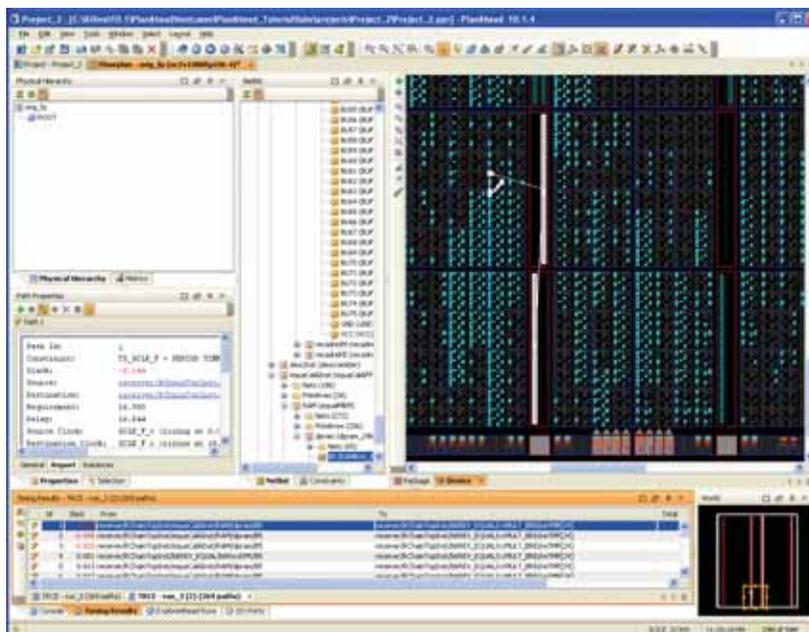


Figure 2 – PlanAhead software 10.1 shows a corrected path after locking down DSP48 and block RAM

Chris Dunlap is an FAE in the Xilinx Santa Clara sales office in California. He originally joined Xilinx in 1999, working in the technical support group.

What Chris enjoys most about his job as an FAE is helping customers in need. He enjoys the diversity of his position, as well as the variety of challenges he faces on a daily basis. In his spare time, he lets off steam on the ice, playing hockey. At home, he loves to spend time with his wife and son, while anxiously awaiting a newborn daughter.

If you need assistance, be sure to check in with your local FAE, contact Xilinx tech support at (800) 255-7778, or visit www.xilinx.com/support/clearexpress/web support.htm.

Application Notes

If you want to do a bit more reading about how our FPGAs lend themselves to a broad number of applications, we recommend these application notes.



XAPP1106: Using and Creating Flash Files for the MicroBlaze Development Kit – Spartan-3A DSP 1800A Starter Platform

www.xilinx.com/support/documentation/application_notes/xapp1106.pdf

In this application note, Sundararajan Ananthkrishnan describes the files for programming the serial flash memory and the StrataFlash memory for the MicroBlaze™ Development Kit – Spartan™-3A DSP 1800A Starter Platform.

The reference system executes the HelloWorld software application (running from serial flash) using the SPI configuration mode and the BlueCat Linux image (from StrataFlash) in BPI configuration mode. Ananthkrishnan includes the files you need to run the BlueCat Linux reference system from StrataFlash memory and the HelloWorld application from the serial flash. The application note also describes how to use the files – as well as create new files – to run the reference system successfully from flash memories.

XAPP514: Audio/Video Connectivity Solutions for Virtex-II Pro and Virtex-4 FPGAs: Reference Designs for the Broadcast Industry: Volume 1

www.xilinx.com/support/documentation/application_notes/xapp514.pdf

This is a comprehensively updated collection of reference designs for designers tackling applications in the broadcast industry.

Xilinx updated XAPP514 earlier this year, adding among other things a new chapter (Chapter 9), entitled “Introduction to the SMPTE High-Definition Serial Digital Interface Standards.” The new chapter describes how the SMPTE 3G-SDI standard is emerging to replace dual-link HD-SDI, to accommodate higher bandwidth video formats running at 3 Gbps and higher. The standard uses the same electrical characteristics and scrambling as HD-SDI, but doubles the bit rate to almost 3 Gbps.

This document also discusses why 3G-SDI is an attractive alternative to dual-link HD-SDI because it uses a single cable instead of a pair of cables.

XAPP860: 16-Channel, DDR LVDS Interface with Real-Time Window Monitoring

www.xilinx.com/support/documentation/application_notes/xapp860.pdf

In this application note, Greg Burton describes a 16-channel, source-synchronous LVDS interface operating at double data rate (DDR). The transmitter (TX) requires 16 LVDS pairs for data and one LVDS pair for the forwarded clock. The transmitter operates at 6:1 serialization on each of the 16 data channels.

The receiver (RX) also requires 16 LVDS pairs for data and one LVDS pair for the source-synchronous clock input. The receiver operates at 1:6 deserialization on each of the 16 data channels. Burton describes the timing of the receiver in depth and characterizes it in hardware.

This application note has a sister note, XAPP855, entitled “16-Channel DDR LVDS Interface with Per Channel Alignment” (www.xilinx.com/support/documentation/application_notes/xapp855.pdf). The design technique discussed in XAPP860 has all of the same features, as well as an additional window monitoring circuit, boosting the performance above that of the design described in XAPP855. But the added performance comes at the expense of additional logic utilization.

XAPP453: Spartan-3 FPGA Family Advanced Configuration Architecture

www.xilinx.com/support/documentation/application_notes/xapp453.pdf

This 14-page application note presents an approach to configure Spartan-3 FPGAs from a 3.3-V interface. It provides a set of connection diagrams for each configuration mode. These diagrams are complete, ready-to-implement solutions.

You can also apply the approach outlined in this paper to the Spartan-3E family, although pin names and banks are different. The Spartan-3A/3AN/3A DSP families allow V_{CCAUX} to be 3.3V, simplifying the interface. ●●

The Path to Successful Design

The Xilinx Customer Education group can help you gain the knowledge and skills you need to innovate with Xilinx FPGAs.

by Stuart Elston
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With an ever-increasing number of electronics companies turning to Xilinx® FPGAs, our company has made it a top priority to make world-class training available to designers.

Today, our Customer Education group offers comprehensive curriculum paths, including our popular “FPGA Design Curriculum Path,” comprising three core classes:

1. “Fundamentals of FPGA Design”
2. “Designing for Performance”
3. “Advanced implementation Techniques”

In the “Fundamentals of FPGA Design” course, we focus on the use of Xilinx Project Navigator to implement and simulate an FPGA design. We’ll show you how to read reports to determine whether you have met your design goals, and how to use the architecture wizard to create digital clock manager (DCM) instantiations.

We’ll also use the Floorplan Editor and PinAhead tools to help you with pin assignment, and the Constraints Editor to enter global timing constraints, locating and modifying implementation options as necessary.

In the “Designing for Performance” course, we build on the fundamentals by describing a flow to help you obtain timing closure. In this course, we also describe the architectural features of the Virtex™-5 FPGA and review the features of the DCM and phase-locked loop (PLL), explaining how you can use them to improve performance.

We’ll also look at how you can increase design performance through duplicating registers and pipelining, and describe different synthesis options and how they improve performance. We look at how to create cores and

integrate them into your design flow using CORE Generator™ software, and how to run behavioral simulation on an FPGA design that contains cores.

We’ll show you how to pinpoint design bottlenecks with timing analyzer reports and how to apply advanced timing constraints to your design to meet your performance goals. We’ll also show you how to use advanced implementation options to increase design performance.

Finally, if you are an advanced user, we offer a course on “Advanced Implementation Techniques.” In this course, we create and edit timing constraints in the UCF file and use Tcl-based scripting to implement a design.

We’ll also show you how to analyze I/O interface timing and implement timing

constraints and design modifications to meet system and source-synchronous I/O interface timing. We’ll demonstrate how to use partitions and SmartGuide™ technology to preserve timing results, and discuss floorplanning techniques to enhance timing and optimize the post-place and route design in the FPGA Editor for more efficient in-circuit testing.

This quarter, we are featuring all three of these classes at multiple North American locations. To see a schedule, visit www.xilinx.com/support/training/abstracts/Class-Schedule-by-Course.pdf.

In addition, our network of authorized training providers is dedicated to helping you become successful. To find your local authorized training provider, visit www.xilinx.com/support/training/atp.htm. 🌟

Upcoming Conferences

In addition to offering training at multiple locations, we exhibit our technologies at several conferences.

Conference	Date	Location
NI Week 2008	August 5-7, 2008	Austin, TX
IBC2008	September 11-16, 2008	Amsterdam, Netherlands
MAPLD Conference 2008	September 15-18, 2008	Annapolis, MD
Convergence 2008	October 20-22, 2008	Detroit, MI
SDR Forum	October 26-30, 2008	Washington, DC
Electronica 08	November 11-14, 2008	Munich, Germany
MILCOM 2008	November 17-19, 2008	San Diego, CA
Embedded Technology 2008	November 19-21, 2008	Yokohama, Japan
InterBEE	November 19-21, 2008	Chiba City, Japan
CES 2009	January 8-11, 2009	Las Vegas, NV
Mobile World Congress 2009	February 16-19, 2009	Barcelona, Spain
Embedded World 2009	March 3-5, 2009	Nuremburg, Germany
Embedded Systems Conference	April 1-5, 2009	San Jose, CA

Xcuse Us

To err is human...

Welcome to a new section in Xcell Journal called “Xcuse Us: To err is human ...” If you use software of any kind, chances are you’ve encountered a software glitch or bug and had to locate a patch to fix the problem (if you haven’t used software of any kind, chances are you are an analog designer).

Imagine how hard it is to develop a conventional software program; now imagine how hard it is to develop a program that allows you to design and program IC technology, which is ever-changing. Here at Xilinx, our Solutions Group is constantly developing software and flows for new silicon and is even creating multi-discipline design tools by developing tools for embedded software and DSP development, as well as logic design.

As you can imagine, it isn’t easy task. We try to proactively catch issues with our tools, but sometimes a bug or 10 slips through our detection ... and we’re sorry. Fixing issues is a top priority as they arise.

Other times, we update tools simply to add new features to help you design more efficiently. Therefore, in each issue of Xcell Journal we’ll keep you up-to-date on our latest patches, updates, and service packs. You can also visit the Xilinx® Download Center at www.xilinx.com/download to see and download the latest patches developed between issues of Xcell Journal.

Here are the most current updates to Xilinx design products and IP as of June 30, 2008.

The Xilinx flagship FPGA development environment is ISE™ Foundation™ software, which is a configurable suite of individual design tools. You can select (and purchase) which tools in the suite are best suited to your specific design requirements; you don’t have to purchase tools you don’t need.

The ISE design suite includes logic tools: ISE Foundation software, ChipScope™ Pro analyzer, ChipScope Pro serial I/O toolkit, and PlanAhead™ design tools. It also includes the Embedded Development Kit for embedded software development, and System Generator for DSP and the AccelDSP™ synthesis tool for DSP programming.

Logic Design Tools

ISE Foundation Software

Description: The industry’s most complete programmable logic design solution

Latest Version Number: 10.1

Date of Latest Release: June 2008

Previous Release: 9.2i

Download the Latest Patch:

www.xilinx.com/download

Revision Highlights: In addition to significant quality improvements, Service Pack 2 reduces simulation run times with improvements in the models for GTP transceivers in the Virtex™-5 FPGA family. You can expect 2x-7x faster simulation run times.

Service Pack 2 also provides support in the XPower estimator for the Virtex-5 FXT FPGA family; updated power modeling for the Spartan™-3A FPGA family; and numerous updates to the Xilinx power estimator spreadsheets for Spartan-3 Generation FPGAs.

ISE Software Simulator

Description: A complete, full-featured HDL simulator integrated with ISE Foundation software

Latest Version Number: 10.1

Date of Latest Release: June 2008

Previous Release: 9.2i

Download the Latest Patch:

www.xilinx.com/download

Revision Highlights: Quality improvements

ModelSim Xilinx Edition III (MXE-III)

Description: A low-cost version of the industry’s most popular simulation environment

Latest Version Number: 6.3c

Date of Latest Release: March 2008

Previous Release: 6.2g

Download the Latest Patch: N/A

Revision Highlights: No new updates since the release of ISE software design suite 10.1

PlanAhead Design Tools

Description: A faster, more efficient FPGA design solution to help achieve your performance goals in less time

Latest Version Number: 10.1

Date of Latest Release: June 2008

Previous Release: 9.2i

Download the Latest Patch:

www.xilinx.com/download

Revision Highlights: Quality improvements

ChipScope Pro Analyzer and the ChipScope Pro Serial I/O Toolkit

Description: Real-time debugging and verification tools for Xilinx FPGAs

Latest Version Number: 10.1

Date of Latest Release: June 2008

Previous Release: 9.2i

Download the Latest Patch:

www.xilinx.com/download

Revision Highlights: Quality improvements

ISE WebPACK™ Software

Description: A free solution for your Xilinx CPLD or medium-density FPGA designs

Latest Version Number: 10.1

Date of Latest Release: June 2008

Previous Release: 9.2i

Download the Latest Patch:

www.xilinx.com/webpack

Revision Highlights: See the revision highlights for ISE Foundation software; these improvements apply to all devices supported in ISE WebPACK software.

Embedded Design and DSP Tools

Platform Studio and EDK (Embedded Development Kit)

Description: An integrated development environment comprising embedded processing tools, a MicroBlaze™ embedded processor, IP, software libraries, and design generators

Latest Version Number: 10.1

Date of Latest Release: June 2008

Previous Release: 9.2i

Download the Latest Patch:

www.xilinx.com/download

Revision Highlights: In addition to quality improvements, Service Pack 2 provides full access to the Virtex-5 FXT family of FPGAs and new support for the automotive versions of the Spartan-3A and Spartan-3A DSP FPGA families.

Base System Builder, included in the EDK, provides support for the ML507, a general-purpose FPGA, RocketIO™ GTX transceivers, and an embedded system development board.

A new floating-point unit core is now available for designs targeting Virtex-5 FPGA families. This new core includes an APU interface and is supported in the Base System Builder.

System Generator DSP Tool Kit

Description: Enables the development of high-performance DSP systems using products from The MathWorks

Latest Version Number: 10.1

Date of Latest Release: June 2008

Previous Release: 9.2i

Download the Latest Patch:

www.xilinx.com/download

Revision Highlights: In addition to quality improvements and support for MATLAB 2008a from The MathWorks, Service Pack 2 introduces a new clocking option to automatically include a digital clock manager (DCM), allowing designs to have more than three clocks and clock rates.

Service Pack 2 also includes two new DSP block set enhancements with the addition of the FIR Compiler 4.0 – with all of the features supported by the FIR Compiler LogiCORE IP v4.0 – and Divider Generator 2.0, which generates arithmetic division algorithms for integer division.

AccelDSP Synthesis Tool

Description: Option for System Generator for DSP, enabling a top-down MATLAB language-based DSP design methodology

Latest Version Number: 10.1

Date of Latest Release: June 2008

Previous Release: 9.2i

Download the Latest Patch:

www.xilinx.com/download

Revision Highlights: In addition to quality improvements and support for MATLAB 2008a from The MathWorks, Service Pack 2 allows the use of Xilinx-optimized LogiCORE IP in generated HDL for all supported operators.

Xilinx IP Updates

Name of IP: ISE Software IP Update 10.1.2

Type of IP: All

Targeted Application: Xilinx develops IP cores and partners with third-party IP providers to decrease customer time to market. The powerful combination of Xilinx FPGAs and IP cores provides functionality and performance similar to ASSPs, but with flexibility not possible with ASSPs.

Latest Version Number: 10.1.2

Date of Latest Release: March 2008

Previous Release/Release Date: 10.1.1i (April 2008)

Access the Latest Version:

www.xilinx.com/download

Revision Highlights: Xilinx IP cores, including LogiCORE IP cores, are delivered through software updates available from the Xilinx Download Center. The latest versions of IP products have been tested and delivered with the current IP release.

In addition to quality improvements, Service Pack 2 for ISE software IP update 10.1.2 provides new features, functionality, and examples for many Xilinx LogiCORE IP cores.

Here is a partial list of significant changes in Service Pack 2:

- Endpoint block plus wrapper for PCI Express v1.8. Added new dual-core example design for Virtex-5 FX70T devices and Fast Functional Simulation model support for Virtex-5 FPGA GTP-based transceiver configurations.
- Virtex-5 FPGA RocketIO GTX wizard v4.1. Enhanced with new OBSAI and PCI Express Gen2 protocol templates and support for the GTX-DUAL Fast Functional Simulation model.

- Virtex-5 FPGA RocketIO GTP wizard v1.9. Added TX phase alignment updates, selectable PPM offset, support for the GTP_DUAL FAST Functional Simulation Model, and support for Synplicity's Synplify 9.2.
- Serial RapidIO v4.4. VHDL wrapper support for Virtex-5 FPGA families. Two new ports added to support capture and retransmission of request packet original destination IDs.
- FIR Compiler v4.0. Distributed architecture support for Virtex-5 FPGAs/Spartan-3A DSP devices, extended data and coefficient bit widths to 49 bits, polyphase filter bank for channelizer applications, and support for as many as 16 parallel data paths. System Generator 10.1.2 supports all features of FIR Compiler v4.0.
- Divider Generator v2.0. Added support for Virtex-5 FPGAs/Spartan-3A DSP devices. A new high radix divider algorithm supports as many as 54 bit operands, also supported in System Generator 10.1.2.

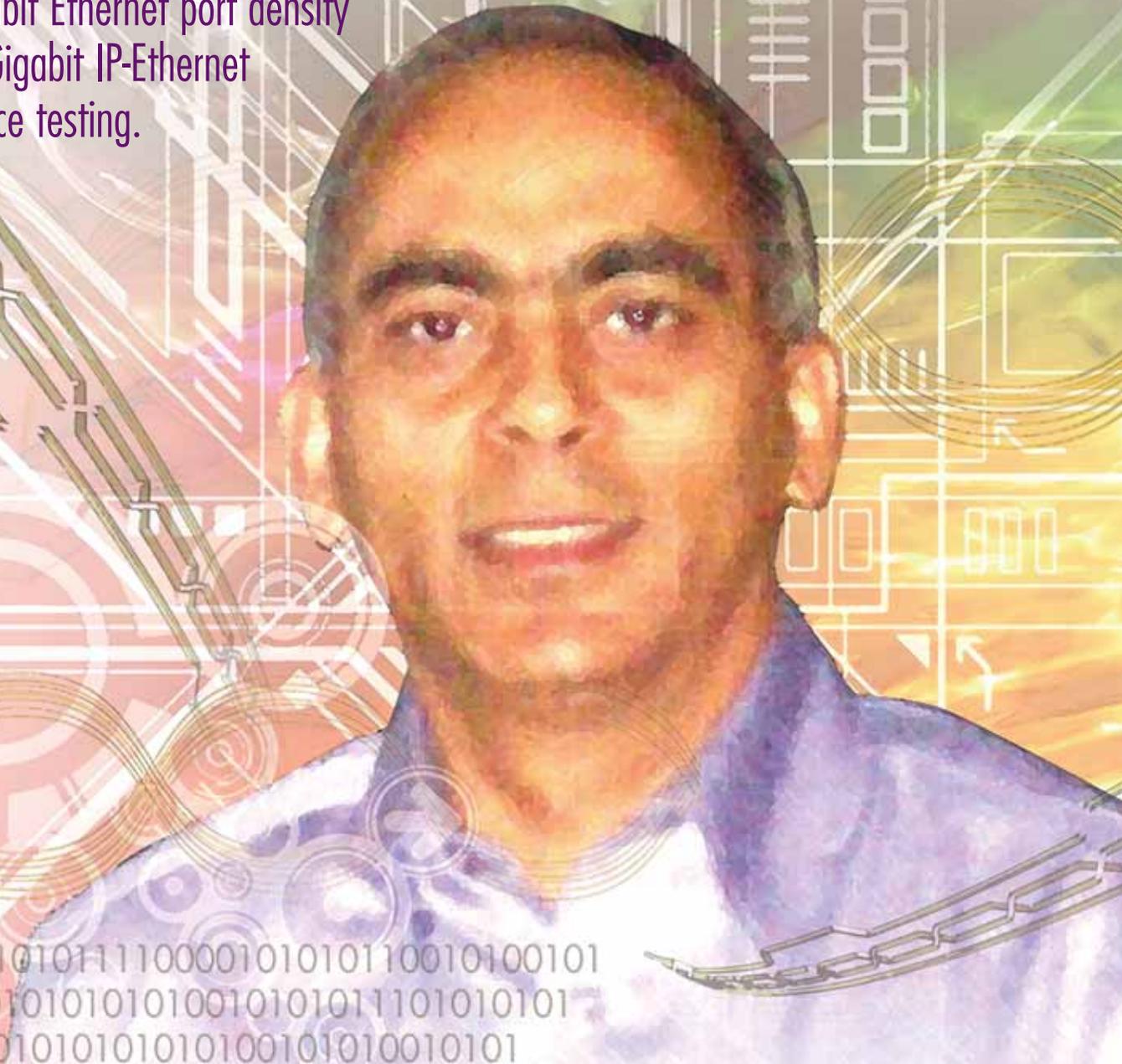
In addition:

- OBSAI v2.1. Added support for the Virtex-5 FXT family of FPGAs.
- SPI-4.2 Lite v4.3. Verilog support for the Synopsys VCS simulator.
- Aurora 64b/66b v1.2. Enhanced frame generator and frame checker, updated GTX attributes, and support for multiple lanes.
- Aurora v3.0 for Virtex-5 FPGA families. Xilinx ISE software simulator and Cadence NCSim simulator support, SecureIP encrypted model support for MTI ModelSim, and support for changing lane assignments within a tile.
- Discrete Fourier transform v3.0. Addition of 1296- and 1536-point sizes for 3GPP-LTE wireless systems and the option to trade off between area resources or speed performance. 🌈

Xcell Journal would like to thank Mark Goosman for compiling this data.

Ixia CEO Atul Bhatnagar: Calm in the Storm

Xilinx customer Ixia is pushing the limits of 10 Gigabit Ethernet port density and 100 Gigabit IP-Ethernet performance testing.



by Mike Santarini
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 Xilinx, Inc.
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Imagine the stress of having to design IP, high-speed Ethernet network devices, or an entirely new network before a standards body has even fully defined the next-generation network standard.

Now imagine that your company has to develop test equipment to help network design companies ensure that their designs comply with this not-yet-fully-defined next-generation network standard.

Ixia is one of those companies, but if its business is stressful, it certainly doesn't show on the face or in the demeanor of its president and CEO, Atul Bhatnagar.

Keys to the (iSim)City

Bhatnagar sits on a leather sofa in an ultra-modern meeting room in Ixia's Santa Clara, Calif., sales offices. The meeting room is adjacent to another glass-encased room, with several racks of testing equipment labeled "iSimCity."

During our meeting, he calmly pointed to the room full of racks and said, "That's where we can simulate an entire city of a quarter of a million users of multimedia services. A service provider or network equipment manufacturer can bring their gear into this center and we'll hammer it with the load of a quarter million users – it will tell you if your gear can handle the load.

"We do a very realistic simulation of end users: a kid playing Halo on Xbox Live, a wife surfing the Internet, while you are watching HDTV. We can simulate all those end-user services per user and multiply that a quarter of a million times. Customers find it very useful." His customers are a who's who in the network infrastructure business: Cisco, Juniper, Nortel, and multiple worldwide carriers too.

"Learning Different Functions"

Bhatnagar originally hails from India, where in 1978 he received his bachelor's degree in electrical engineering from the Birla Institute of Technology and Science in Pilani. He came to United States in

1981 to obtain a master's degree, also in electrical engineering, from the University of New Mexico, and landed a job at Tektronix developing networking gear.

In 1985, he joined Hewlett-Packard (HP) and worked in the field of open systems networking for eight years. "One of the things I did at Hewlett-Packard was try to diversify myself by learning different functions," said Bhatnagar. "I worked at first in engineering; in product management and product marketing; and then in the quality groups. That's where I learned about software engineering, software quality, processes, and process management."

Bhatnagar then took an overseas assignment in Singapore, where he led HP's network management group. "I came back to

solutions, WLAN mobility solutions, Metro Ethernet technologies, and enterprise routers.

Bhatnagar's next position was head of product development at mobile convergence startup DiVitas Networks. In 2006, Ixia's board of directors tapped the well-spoken and broadly experienced comms veteran to be their new president and COO. Bhatnagar was named president and CEO in March 2008.

100 Gigabit Ethernet

Ixia specializes in Internet Protocol (IP) performance testing, 1 to 100 Gigabit Ethernet network simulation, and has recently entered the service verification business. "Ten years ago, when Ixia started,

"We showcased the first 100 Gigabit Ethernet line rate implementation – the first ever in the industry – with tremendous support and help from Xilinx. Together, Xilinx and Ixia are stretching the limits of technology and showcasing innovations, which will really further Ethernet penetration into carriers and network equipment manufacturers."

the U.S. and started working on a lot of innovative programs: next-generation Internet communications and new ways of using the Internet." In his last five years at HP, he worked as the division GM.

Over a span of 15 years at HP, Bhatnagar led the creation of the operation support systems (OSS) and business support systems (BSS) solutions for wireless service providers based on HP's OpenView architecture. His team was also responsible for networking services for all HP-UX-based workstations and minicomputers.

He left HP in 2000 and joined a company called Alteon Web Systems, creating next-generation Web Switches and security acceleration products. Alteon was acquired by Nortel in October of that same year. Bhatnagar served as vice president and general manager of the Enterprise Data Networks division of Nortel, where he was responsible for the design and marketing of a full range of Ethernet switches, security

we bet that IP and Ethernet would become dominant in communications," said Bhatnagar. "There were gobs of things we could have focused on, but we focused on this area, and as a result, we are the market-share leader in 1 and 10 Gigabit Ethernet testing solutions." Ixia intends to stay on top for the foreseeable future.

At NXTcomm08 in Las Vegas, Ixia announced the industry's first 100 Gigabit Ethernet implementation. "That's where Xilinx has been a very close partner," said Bhatnagar. "We showcased the first 100 Gigabit Ethernet line rate implementation – the first ever in the industry – with tremendous support and help from Xilinx. Together, Xilinx and Ixia are stretching the limits of technology and showcasing innovations, which will really further Ethernet penetration into carriers and network equipment manufacturers."

Why 100 Gigabit Ethernet? Bhatnagar explained that the proliferation of video

“Data centers are now deploying significant 10 Gigabit Ethernet switching and connectivity. The convergence of storage, data, voice, and video flowing over common plumbing is driving the adoption of 10 Gigabit Ethernet in data centers. The adoption of 10 Gigabit Ethernet will in turn drive the adoption of 100 Gigabit Ethernet in data centers.”

and multimedia over wired and wireless networks is escalating at such a pace that every carrier and large enterprise knows they will be running out of bandwidth every few years.

“The revolution continues,” Bhatnagar said. “Data centers are now deploying significant 10 Gigabit Ethernet switching and connectivity. The convergence of storage, data, voice, and video flowing over common plumbing is driving the adoption of 10 Gigabit Ethernet in data centers. The adoption of 10 Gigabit Ethernet will in turn drive the adoption of 100 Gigabit Ethernet in data centers.

“At the same time, carriers are also looking at what will be the next-generation infrastructure technologies. 100 Gigabit Ethernet will play there as well. That’s a breakthrough project where Xilinx and Ixia worked together.”

The Four “E”s

Ixia’s continued success, said Bhatnagar, is driven by a company-wide adherence to four key values: energy, edge, execution, and ethics.

“Without energy, you don’t have the wherewithal to be a leader,” said Bhatnagar. “Whatever you do, you have to have a superior edge over your competition – you have to do it with excellence. Our third value is execution – you can have the best plans in the world, but if you don’t execute them, those plans are no good. And fourth is ethics: not just ethics in business dealings, but ethics in interpersonal relationships as well.”

Bhatnagar said that the company focuses on direct communications “to put all issues on the table and be direct in communications.” “We are very customer-focused and strive to create customer delight,” said Bhatnagar. “It’s encouraged all the way from engineering

to system testing to support to sales. We are very responsive to customers and our engineers go the extra mile if there is a way to make things happen.”

Growth Chart

Ixia’s adherence to these values has been key to making Ixia top in Gigabit Ethernet performance testing and analytics market share. But Bhatnagar said the company is not simply content to be

number one in 1 to 100 Gigabit Ethernet pre-deployment testing.

“Our priority now is to grow the company,” said Bhatnagar. “Up until now, we’ve been primarily focused on pre-deployment testing. Now we are going toward post-deployment service verification. How do we help customers run networks with quality? How do we bulletproof the networks with good monitoring and the right diagnostic tools?”

From Engineer to CEO and Many Roles in Between

Over Bhatnagar’s long career, he has played many roles in many companies, from engineer to CEO. He said during our interview that he made it a point to be open to taking on new roles and responsibilities throughout his career.

So what’s it like to be a CEO?

“As a CEO, you are a coach. Your goal is to develop all of the teams around you in such a way that there isn’t a weak spot,” said Bhatnagar. “You cannot do everything yourself and you have to surround yourself with people who in each function are better than you.

“As a CEO, I know how to do many functions, but you really want to hire people that are far superior in each of those functions. Then you have to make sure the team is working well, the employees are energized, the value system is in place, and that you have a sense of urgency in execution. By and large, the stronger the team, the more you can execute.

“It really comes down to all the key values. In our industry, you also have to have people believing in the mission. You have to constantly adapt and look at the trends, but the more you communicate and share your vision, the more it becomes your employees’ vision as well.”

Bhatnagar also notes that the job of CEO, like many other jobs, is very demanding on many fronts. And so when he does get time to unwind, he likes to hike. “I like to hike early in the morning before the family wakes up; it’s good exercise and it’s good thinking time,” said Bhatnagar. “I do it in the morning because it doesn’t take away time with the family. It’s important to spend time with your family – kids grow up too soon.”

Case in point: the company recently released a new technology called IxRave, which is a service verification product. “We’re already deploying it at a couple of carriers to provide diagnostics tools for the service professionals of these networks,” said Bhatnagar.

But while Ixia is investing in 100 Gigabit Ethernet-generation network testing, it’s also strengthening its play in 10 Gigabit Ethernet network testing, expecting that to continue to grow for the company. “We recently announced, with Xilinx cooperation, the industry’s highest density 10 Gigabit Ethernet testing solution, the IxYukon,” said Bhatnagar.

IxYukon has eight 10 Gigabit Ethernet ports per blade and 12 blades per chassis, totaling 96 layer 2 through 7 testing ports.

“It’s another example of our long partnership with Xilinx,” said Bhatnagar. “We are very proud of this partnership. We push the technology quite a bit and we admire and appreciate the help of Xilinx engineers in creating world-class solutions.

“As a company focused on network performance testing, we have to have our products ready to go three or four quarters before customers release their products. So we are always on the bleeding edge of the technology. We always adopt standards at an early stage to make sure that our testing tools are ready by the time customers are beginning to design their products.”

Ixia’s business is seemingly also a risky one, because sometimes it has to develop IP-Ethernet test tools before standards bodies have solidified the standards. “That’s where

FPGAs come into play,” said Bhatnagar. “With FPGA-based designs, we have the flexibility of adapting as markets are changing and as technology is changing and yet maintain the first-to-market advantage. And of course in our industry, the first-to-market advantage is a significant advantage.

“It’s amazing the amount of marketing you pick up when you move first. It’s always a good strategy to move first, pick up industry marketing, and be a thought leader – or at least viewed as such by the industry – versus spending gobs of marketing dollars later. If you are first, the industry does the marketing for you.”

The key to that, said Bhatnagar, is not being the first to promise the technology, but delivering the technology. And Ixia’s delivered. ●●

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Tools of Xcellence

News and the latest products from Xilinx partners.

Welcome to the “Tools of Xcellence” section. In each issue, our staff will interview tool, IP, and development board vendors about their latest product introductions and upgrades. From time to time, we’ll also include write-ups of significant business moves that could impact the Xilinx user community.

by Mike Santarini
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Combined Synopsys/Synplicity Holds Potential for FPGA Tool Innovations

Synopsys Inc.’s \$223 million acquisition of its longtime FPGA synthesis rival Synplicity in May has left many Synplicity tool users wondering how the acquisition will affect them.

George Zafiroopoulos, vice president of solutions marketing at Synopsys, said to only expect good things: no Synplicity tools are going away. Additionally, Ken McElvain, the cofounder of Synplicity and designer of Synplify, is staying at Synopsys indefinitely. The company will function as an independent business unit within Synopsys, developing tools leveraging the strengths of both companies.

In the early 1990s, McElvain and his wife Alisa Yaffa left Mentor Graphics to found Synplicity. The company’s first product, the Synplify FPGA synthesis tool, was an instant success. In those days, FPGA synthesis tools were typically complex and had very long run times. In contrast, Synplicity users reported being stunned by Synplify’s speedy run times – many users reported hitting the “synthesize my design” button more than once before figuring out that Synplify had actually synthesized their designs very quickly.

This success led to dominant market share in FPGA synthesis, an IPO in 2000, and product launches of Synplify variants and new tools like the Identify debugger, the Certify ASIC prototyping/partitioning tool, and Amplify ASIC/structured ASIC synthesis (Synplicity shelved the latter tool in 2007).

Synplicity even acquired Hardi Electronics to bolster its play in FPGA-based ASIC prototyping (see info about the new HAPS 51T prototyping board later in this article), leading to the release of the Confirma ASIC/ASSP platform, which combines Certify, Hardi boards, and Identify in one package.

Meanwhile, Synopsys – hoping to leverage its dominant position in ASIC synthesis tools – made three attempts to swipe market share from Synplicity over the last decade, first launching FPGA Compiler in the early 1990s, FPGA Express in the mid ’90s, and FPGA Compiler II in the late ’90s. All of these tools were fairly short-lived (FPGA Compiler II was “end of life” at the end of 2006), as Synplicity continued to innovate its tools with each new generation of FPGA silicon.

Indeed, Synopsys’s acquisition is, in a way, an “if you can’t beat ’em, buy ’em,” acquisition.

Zafiroopoulos said that Synplicity will now function as Synopsys’s sixth business unit, headed by Gary Meyers, Synplicity’s president and CEO, now GM of the Synplicity business unit. Ken McElvain, said Zafiroopoulos, is essentially serving as the group’s CTO, developing next-generation tools.

“Synplicity is extremely well-known for its FPGA synthesis tools, but over the years [the company] expanded into verification

and they've done some great work there," said Zafiropoulos. "Before the acquisition, our two companies had been collaborating on flows in the verification area and now we've stepped up development." Zafiropoulos declined to elaborate on future tool or flow offerings.

Verification Tools and Methodologies

Although Synopsys may not have had the greatest record competing against Synplicity in the FPGA space, Synopsys does own a full suite of verification tools, including the popular VCS simulator. It also has formal analysis, debugging, and test bench generation, all supporting advanced assertion-based verification.

Zafiropoulos points out that many FPGA designers today use VCS for simulating their code, but as FPGAs become more complex and reach into the millions of gates, FPGA designers are starting to apply

ASIC verification methodologies to their FPGA verification flows.

A few years ago, Synopsys acquired SystemVerilog inventor Co-Design Automation. SystemVerilog is just finding traction in mainstream ASIC design, and it's just now starting to gain traction in FPGA design. It's possible that the combined Synopsys/Synplicity could accelerate usage of SystemVerilog methodologies in the FPGA design community.

A key to success in these endeavors will be making sure that the new technologies are suited to the varying skill levels of FPGA users. Indeed, over the last few years, the FPGA user base has expanded beyond traditional hardware designers to include embedded system developers and DSP programmers. Zafiropoulos points out that Synplicity has also been serving that growing user base, having released Synplify DSP in 2004, a DSP synthesis tool for both FPGA and ASIC end implementations.

Aldec Upgrades Active-HDL, Releases ALINT Design Rule Checker

Aldec Inc. (Henderson, Nevada) has released the 8.1 version of its flagship product, Active-HDL, adding various functionality and performance improvements to the tool. At the Design Automation Conference (DAC) in June, the company also announced a new design rule checker called ALINT.

Lori Nguyen, Aldec's director of marketing, said that with the 8.1 release, Active-HDL performs VHDL simulation faster than competing tools and simulates SystemVerilog with the same performance as competing tools. "And we're about 30% less expensive," Nguyen added.

Igor Tsapenko, manager of applications engineering, said that with version 8.1 Aldec is now making its SLP-enhanced Verilog simulation engine the default simulation engine for the tool. Previously, Aldec offered SLP as an option to the tool.

Active-HDL has included various coverage tools such as code coverage and expression coverage for several years now, but each tool used a separate database. In version 8.1, Aldec has added a unified code coverage database to Active-HDL.

The company also improved the performance of Active-HDL's waveform viewer and made general improvements to the tool, in particular Active-HDL's graphical entry tool. This tool allows designers to build designs with either a block diagram editor or finite state machine editor instead of hand-coding their designs using HDL. In the 8.1 release, the company is adding a code coverage engine to the FSM editor.

Nguyen said that in March 2009, the company plans to issue the 8.2 version of Active-HDL, which will add to the tool graphical entry support for SystemVerilog.

ALINT

At DAC, the company also announced a new linting product, ALINT. Linting tools essentially allow designers to check that their code complies with various styles and standards.

"What's unique about our tool is that we support the 2006 STARC rules set, where most other tools on the market today only currently support STARC's 2002 rules set," said Nguyen. "And we also support clock domain crossing rules sets."

The Semiconductor Technology Academic Research Center (STARC) in Japan specifies, among other things, a 250-rule synthesizable subset for HDL coding. This helps ensure that its member companies create code that can they effectively and efficiently synthesize with commercial EDA ASIC and FPGA synthesis and FPGA vendor synthesis tools.

In addition to support for various synthesis rules, ALINT also supports coding style rules as well as rules for various verification techniques.

The tool features two application interfaces: Configuration Manager and Violation Viewer. Configuration Manager allows you to specify what rules sets you'd like the tool to check. Violation Viewer allows you to locate violations in your source code so you can fix them.

Currently, the tool only supports Verilog, but the company expects to make full VHDL support available by October 2008, with complete Verilog, SystemVerilog, and VHDL mixed-language support by February 2009.

Nguyen said that ALINT currently includes several customization features that allow users to modify existing rules and policies to make sure designers are coding to their company's best practices guidelines. It plans to expand that feature in a future release to allow users to create their own rules. Plus, the company plans to add an Aldec rules set as well as rules sets from FPGA vendors to that release.

Nguyen claims that ALINT is more robust than other commercial tools, and at a starting price of \$7,500 for a simulator upgrade and a stand-alone version for \$13,000, roughly half the cost.

Aldec offers several versions of Active-HDL. The single-language version of the tool starts at \$3,500, while the full-featured mixed language version is \$20,000.

Synfora Launches PICO Extreme FPGA, a C-to-FPGA Algorithmic Synthesis Tool

At DAC, tool vendor Synfora Inc. (Mountain View, California) announced the availability of its new C-to-RTL algorithmic synthesis tool targeted for FPGAs, PICO Extreme FPGA.

In February 2008, Synfora and Xilinx announced that the two companies were beta-testing the new Synfora technology, specifically on Virtex™-5 devices and low-cost Spartan™-3A DSP FPGAs. The tool is now out of the testing phase, so Synfora is making it available (for a licensing fee) to the mass market supporting Spartan-3, Virtex-4, and Virtex-5 device platforms.

“If you look at an FPGA, it has certain fabric components like the MicroBlaze™ embedded processor, DMA, USB, PCIe ... these cores don’t fully define the device,” said Synfora’s CEO, Simon Napper. “What defines the functionality is what we call the application engine: the wireless modem, the video codec, imaging pipeline. And increasingly, designers are specifying this type of functionality in C.”

In the Synfora scheme of things, customers will typically use PICO Extreme FPGA at the beginning of a design project (see Figure 1). Users start a project by first creating an architecture template with the tool, which Napper said requires some knowledge of hardware but is essentially an untimed C file that you run in a GNU compiler, or the C compiler of your choice. “The architecture template is a C file that captures the hardware properties you desire (shared memory, streaming data),” said Napper. “To validate that this is correct, PICO Extreme FPGA generates a block diagram of the hardware it will create based on the C code.”

After that, said Napper, you populate the diagram with C code and run the PICO Extreme FPGA compiler, which generates RTL. PICO Extreme FPGA also creates all of the scripts necessary to run the XST/Synplicity tool flows. “You don’t really need to know anything about the hardware,” Napper said. And if your design requires any optimizations, you can implement those in C as well, he added.

As with the ASIC version of Synfora’s PICO Extreme, PICO Extreme FPGA also allows more advanced users to reduce the area of certain blocks in the FPGA using Synfora’s tightly coupled accelerator blocks (TCABs). “TCABs are user-definable procedures that the compiler can encapsulate and reuse as a fundamental building blocks in your design,” Napper explained. “If you have a function that the compiler calls many times, you can build it as a TCAB and reduce area. It will also improve the run time of PICO Extreme FPGA.”

The maiden release of PICO Extreme FPGA is primarily focused on video for high-end TVs, video analytics, and imaging applications. “What we’ve done is work with Xilinx to integrate with their fixed fabric for video applications. There’s essentially a slot where users insert their unique video algorithms,” said Napper. At DAC, Synfora demonstrated the system running a Sobel algorithm on a Xilinx Spartan-3 device. “You could do the same thing with a deblocking filter algorithm or an image enhancement algorithm,” said Napper. “Once you’ve created the fabric, you have a script file that just builds it.”

Napper believes that Xilinx® users will find the tool especially useful if they are moving a design they’ve traditionally implemented in a DSP to an FPGA.

Xilinx customers can also use the tool complementary to The MathWorks’s MATLAB-Simulink flow. “Many designers use MATLAB to create an executable specification of their functions,” said Napper. “They can also now rewrite that specification in C using PICO Extreme FPGA and then do equivalence checking to make sure that the MATLAB specification and C are the same. It’s easy to do equivalence at that level because MATLAB can accommodate C models.”

PICO Extreme FPGA comes pre-characterized for Spartan-3, Virtex-4, and Virtex-5 devices and with an existing board support package for the Spartan-3E Development Kit. Pricing for PICO Extreme starts at \$210,000. ●●●

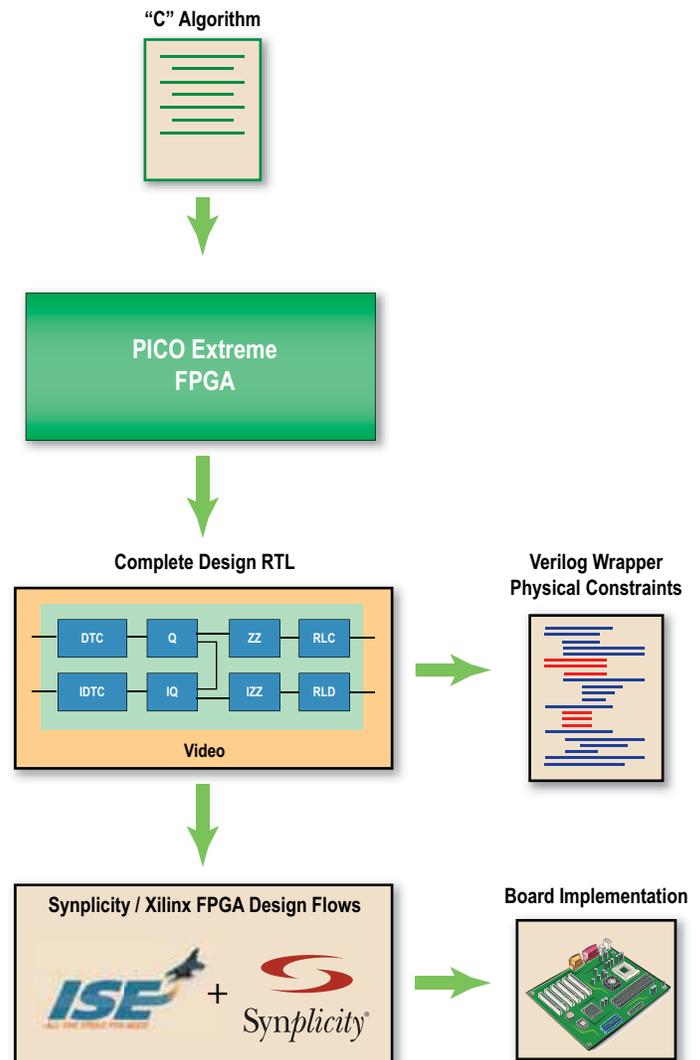


Figure 1 – The PICO Extreme flow synthesis tool generates RTL from C.

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“Persona-Based Design”: Tailoring our Flows to Your Needs

The Xilinx Solutions Development group is developing next-generation tool flows with customer guidance.



by Vin Ratford
Sr. Vice President,
Xilinx Solutions Development Group
Xilinx, Inc.
vin.ratford@xilinx.com

It’s absolutely amazing how far programmable logic has come over the last couple of years. With gate counts rivaling advanced ASICs and with hard-wired processors, DSPs, and high-speed I/O blocks, today’s FPGAs are a far cry from the glue logic PALs and ASIC prototyping vehicles of yesteryear.

A few years ago FPGAs were in embedded systems; now they *are* embedded systems.

As our customers, you have put Xilinx® FPGAs at the heart of a dazzling array of applications: from network cards, to 4G wireless base stations, to medical and broadcast devices, to the world’s most advanced supercomputers. We’re in the depths of the ocean and on board the Mars rover.

And as the applications have grown, so too have the types of engineers using our FPGA platforms. A few years ago, our user base was primarily hardware designers; today systems integrators, DSP developers, and even embedded software engineers are creating innovations with our FPGA platforms.

Persona-Based Design

The broadening of our customer base wasn’t a fluke. Indeed, over the last few years, our tools group, now called the Solutions Development Group, has been busy developing and acquiring tools and



IP to expand the value of FPGAs to a wider audience beyond the hardware designers at your company.

We are now stepping up efforts to streamline our flows and work with development partners such as Synopsys-Synplicity, Mentor Graphics, and Cadence to better integrate their tools and IP into our flows so that we can better serve different types of users with the tools, IP, and flows they need to get jobs out the door. One of our employees, Tom Feist, put a name to this directive: “persona-based design.”

In the past, you may have felt that Xilinx was throwing a breadth of tools at you and saying, “Here, you go figure out your flow.” But no longer. Our applications and development teams will – with your guidance – put together recommended methodologies suited for your design needs.

We’ve established methodology groups dedicated to creating recommended flows for four types of Xilinx users:

- The software designer
- The DSP designer

- The hardware designer (with subgroups for power and push-button users)
- The system integrator

I’ve also asked each of these methodology groups to organize their own customer advisory board. Each board will include key customers and partners so that we can understand your concerns and best address your needs and wants.

Of course, I’ve established an overriding mandate that all of these methodologies must be complementary. They must be able to work together – and work together very well. We’re not going to dictate your flow, but we are going to help you automate and converge on a flow that is ideally suited to each of your designer’s needs, and ultimately your group’s needs.

As FPGAs and applications become more complex, communicating with our customers and our partners is imperative. We look forward to continued success and your exciting innovations with Xilinx on board. ●●●

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	Virtex-5 SXT FPGA Platform Optimized for DSP with Low-power Serial Connectivity (1.0 Volt)				Virtex-5 FXT FPGA Platform Optimized for Embedded Processing with High-Speed Serial Connectivity (1.0 Volt)				
	XC5VX35T	XC5VX50T	XC5VX95T	XC5VX240T	XC5VFX30T	XC5VFX70T	XC5VFX100T	XC5VFX130T	XC5VFX200T
Part Number	XC5VX35T	XC5VX50T	XC5VX95T	XC5VX240T	XC5VFX30T	XC5VFX70T	XC5VFX100T	XC5VFX130T	XC5VFX200T
EasyPath™ Cost Reduction Solutions (1)	—	XC5VX50T	XC5VX95T	XC5VX240T	—	XC5VFX70T	XC5VFX100T	XC5VFX130T	XC5VFX200T
Slices (2)	5,440	8,160	14,720	37,440	5,120	11,200	16,000	20,480	30,720
Logic Cells (3)	34,816	52,224	94,208	239,616	32,768	71,680	102,400	131,072	196,608
CLB Flip-Flops	21,760	32,640	58,880	149,760	20,480	44,800	64,000	81,920	122,880
Maximum Distributed RAM (Kbits)	520	780	1,520	4,200	380	820	1,240	1,580	2,280
Block RAM/PO w/ECC (36Kbits each)	84	132	244	516	68	148	228	298	456
Total Block RAM (Kbits)	3,024	4,752	8,784	18,576	2,448	5,328	8,208	10,728	16,416
Digital Clock Managers (DCM)	4	12	12	12	4	12	12	12	12
Phase Locked Loop (PLL)/PMCD	2	6	6	6	2	6	6	6	6
Maximum Single-Ended Pins	360	480	640	960	360	640	680	840	960
Maximum Differential I/O Pairs	180	240	320	480	180	320	340	420	480
I/O Standards	HT, LVDS, LVDSxT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS33, LVCMOS18, LVCMOS15, LVTTL, PCB33, PCI66, PCI-X, GTL, GTL+, HSTL (1.2V), 1.5V (1.8V), HSTL III (1.5V, 1.8V), HSTL IV (1.5V, 1.8V), SSTL2 I, SSTL2 II, SSTL18 I, SSTL18 II								
DSP48E Slices	192	288	640	1,056	64	128	256	320	384
PowerPC® 440 Processor Blocks	—	—	—	—	1	1	2	2	2
PCI Express Endpoint Blocks	1	1	1	1	1	3	3	3	4
10/100/1000 Ethernet, MAC Blocks	4	4	4	4	4	4	4	6	8
RocketIO™ GTX Low-Power Transceivers	8	12	16	24	—	—	—	—	—
RocketIO™ GTX High-Speed Transceivers	—	—	—	—	8	16	16	20	24
Commercial	-1, -2, -3	-1, -2, -3	-1, -2	-1, -2	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2
Industrial	-1, -2	-1, -2	-1, -2	-1	-1, -2	-1, -2	-1, -2	-1, -2	-1
Configuration Memory (Mbits)	13.3	20.0	35.7	79.6	13.5	27.0	39.4	49.2	70.9
Package (6,7)	Area								
FFA Packages (FF): flip-chip fine-pitch BGA (1.0 mm ball spacing)									
FF665	27 x 27mm			360 (8)	360 (8)			360 (8)	
FF1136	35 x 35mm			480 (12)	640 (16)			640 (16)	
FF1738	42.5 x 42.5mm			960 (24)	680 (16)			960 (24)	

Notes: 1. EasyPath™ solutions provide a conversion-free path for volume production.

2. A single Virtex-5 CLB comprises two slices, with each containing four 6-input LUTs and four Flip-Flops (twice the number found in a Virtex-4 slice), for a total of eight 6-LUTs and eight Flip-Flops per CLB.

3. Virtex-5 logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.

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Virtex-4 Family FPGAs



	Virtex-4 LX FPGA Platform Optimized for High-performance Logic (1.2 Volt)						Virtex-4 SX FPGA Platform Optimized for DSP (1.2 Volt)						Virtex-4 FX FPGA Platform Optimized for Embedded Processing & Serial Connectivity (1.2 Volt)					
	XC4VLX15	XC4VLX25	XC4VLX40	XC4VLX60	XC4VLX80	XC4VLX100	XC4VLX160	XC4VLX200	XC4VSX25	XC4VSX35	XC4VSX55	XC4VFX12	XC4VFX20	XC4VFX40	XC4VFX60	XC4VFX100	XC4VFX140	
Part Number	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
EasyPath™ Cost Reduction Solutions ⁽¹⁾	6,144	10,752	18,432	26,624	35,840	49,152	67,584	89,088	10,240	15,360	24,576	5,472	8,544	18,624	25,280	42,176	63,168	
Slices ⁽²⁾	13,824	24,192	41,472	59,904	80,640	110,592	152,064	200,448	23,040	34,560	55,296	12,312	19,224	41,904	56,880	94,896	142,128	
Logic Cells	12,288	21,504	36,864	53,248	71,680	98,304	135,168	178,176	20,480	30,720	49,152	10,944	17,088	37,248	50,560	84,352	126,336	
CLB Flip-Flops	96	168	288	416	560	768	1,056	1,392	160	240	384	86	134	291	395	659	987	
Maximum Distributed RAM (Kbits)	48	72	96	160	200	240	288	336	128	192	320	36	68	144	232	376	552	
Block RAM/FIFO w/ECC (18 Kbits each)	864	1,296	1,728	2,880	3,600	4,320	5,184	6,048	2,304	3,456	5,760	648	1,224	2,592	4,176	6,768	9,936	
Total Block RAM (Kbits)	4	8	8	8	12	12	12	12	4	8	8	4	4	8	12	12	20	
Digital Clock Managers (DCM)	0	4	4	4	8	8	8	8	0	4	4	0	0	4	8	8	8	
Phase-matched Clock Dividers (PMCD)	320	448	640	640	640	960	960	960	320	448	640	320	320	448	576	768	896	
Maximum Single-Ended I/Os	160	224	320	320	384	480	480	480	160	224	320	160	160	224	288	384	448	
Maximum Differential I/O Pairs	LDT-25, LVDS-25, LVDSSE-25, LVDSSE-25, LVPECL-25, LVPECL-25, LVCMOS18, LVCMOS18, LVCMOS15, PCI33, LVTT, LVCMOS33, PCI-X, PCI66, GTL+, HSTL I (1.5V/1.8V), HSTL II (1.5V/1.8V), HSTL III (1.5V/1.8V), HSTL IV (1.5V/1.8V), SSTL18 I, SSTL18 II																	
I/O Standards	32	48	64	64	80	96	96	96	128	192	512	32	32	48	128	160	192	
DS18B8 Slices	—	—	—	—	—	—	—	—	—	—	—	1	1	2	2	2	2	
PowerPC™ Processor Blocks	—	—	—	—	—	—	—	—	—	—	—	2	2	4	4	4	4	
10/100/1000 Ethernet MAC Blocks	—	—	—	—	—	—	—	—	—	—	—	0	0	8	16	20	24	
RocketIO™ Serial Transceivers	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11	
Commercial	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10	
Industrial	4.8	7.8	12.3	17.7	23.3	30.7	40.3	51.4	9.1	13.7	22.7	4.8	7.2	13.6	21.0	33.0	47.9	
Configuration Memory (Mbits)	Available User I/Os																	
Package ^(6,8)	Available User I/Os																	
SFA Packages (SF) flip-chip fine-pitch BGA (0.8 mm ball spacing)	Available User I/Os																	
FFA Packages (FF) flip-chip fine-pitch BGA (1.0 mm ball spacing)	Available User I/Os																	
FF668	Available User I/Os																	
FF1148	Available User I/Os																	
FF1513	Available User I/Os																	
FF672	Available User I/Os																	
FF1152	Available User I/Os																	
FF1517	Available User I/Os																	

Notes: 1. EasyPath™ solutions provide a conversion-free path for volume production.
 2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.
 3. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.
 4. Available I/O for each device-package combination: number of SelectIO pins (number of RocketIO transceivers).
 5. All Virtex-4 LX and Virtex-4 SX devices available in the same package are footprint-compatible.
 6. All products available Pb-free and RoHS-Compliant.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com/virtex4

Virtex-II Family, Virtex-II Pro Family FPGAs

	Virtex-II Family High-performance Logic (1.5 Volt)													Virtex-II Pro Family High-performance Logic with Serial Connectivity (1.5 Volt)												
	XC2V40	XC2V80	XC2V250	XC2V500	XC2V1000	XC2V1500	XC2V2000	XC2V3000	XC2V4000	XC2V6000	XC2V8000	XC2VP22	XC2VP4	XC2VP7	XC2VP20	XC2VP30	XC2VP40	XC2VP50	XC2VP70	XC2VP100						
Logic Resources	EasyPath™ Core Reduction Solutions (1) Slices (2) Logic Cells CLB Flip-Flops Maximum Distributed RAM (Kbits) Maximum Distributed RAM (bits) Block RAM/FIFO w/ECC (18Kbits each) Total Block RAM (Kbits) Digital Clock Managers (DCM) Maximum Single-Ended I/Os Maximum Differential I/O Pairs I/O Standards 18x18 Multipliers RocketIO™ Transceivers PowerPC Processor Blocks Commercial (slowest to fastest) Industrial (slowest to fastest) Configuration Memory (Mbits)																									
Memory Resources	256 512 1,152 3,072 7,680 15,360 240 48 24 432 576 720 864 88 120 200 264 312 328 40 48 56 64 72 84 96 108 144 168 184 219 281																									
Clock Resources	512 1,152 3,072 7,680 15,360 240 48 24 432 576 720 864 88 120 200 264 312 328 40 48 56 64 72 84 96 108 144 168 184 219 281																									
I/O Resources (3)	512 1,152 3,072 7,680 15,360 240 48 24 432 576 720 864 88 120 200 264 312 328 40 48 56 64 72 84 96 108 144 168 184 219 281																									
Embedded Hard IP Resources	512 1,152 3,072 7,680 15,360 240 48 24 432 576 720 864 88 120 200 264 312 328 40 48 56 64 72 84 96 108 144 168 184 219 281																									
Speed Grades	512 1,152 3,072 7,680 15,360 240 48 24 432 576 720 864 88 120 200 264 312 328 40 48 56 64 72 84 96 108 144 168 184 219 281																									
Configuration	512 1,152 3,072 7,680 15,360 240 48 24 432 576 720 864 88 120 200 264 312 328 40 48 56 64 72 84 96 108 144 168 184 219 281																									
Package (4,5)	Available User I/Os																									
Chip Scale Packages (CS): wire-bond chip-scale BGA (0.8 mm ball spacing)	CS144 88 92 92																									
BGA Packages (BG): wire-bond standard BGA (1.27 mm ball spacing)	BG575 31 x 31 mm BG728 35 x 35 mm 328 392 408 516																									
FPGA Packages (FG): wire-bond fine-pitch BGA (1.0 mm ball spacing)	FG256 17 x 17 mm FG456 23 x 23 mm FG676 27 x 27 mm 172 172 200 264 324 392 456 484																									
FPGA Packages (FP): flip-chip fine-pitch BGA (1.0 mm ball spacing)	FP672 27 x 27 mm FP896 31 x 31 mm FP1152 35 x 35 mm FP1148 35 x 35 mm FP1517 40 x 40 mm FP1696 42.5 x 42.5 mm FP1704 42.5 x 42.5 mm 204 (4) 348 (4) 396 (8) 556 (8) 624 720 824 824 824 1,104 1,108 204 (4) 348 (4) 396 (8) 556 (8) 564 (8) 644 (8) 804 (0) 812 (0) 852 (16) 964 (16) 1,164 (0) 1,040 (20)																									
BGA Packages (BP): flip-chip fine-pitch BGA (1.27 mm ball spacing)	BP957 40 x 40 mm 624 684 684																									

Notes: 1. EasyPath™ solutions provide a conversion-free path for volume production: commercial-grade available on slow and mid speed bins (slow bin only on largest device); industrial-grade available on slow speed.
 2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.
 3. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.
 4. Available I/O for each device-package combination: number of SelectIO pins (number of RocketIO transceivers).
 5. All products available Pb-free and RoHS Compliant.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com/virtex2pro

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