

Z8581 Clock Generator and Controller

Zilog

Product Specification

April 1985

FEATURES

- Two independent 20 MHz oscillators generate two 10 MHz clock outputs and one 20 MHz clock output.
- Oscillator input frequency sources can be either crystals or external oscillators.
- Outputs directly drive the Z80, Z8000, 8086, 8088, and 68000 microprocessor clock inputs.
- Can be used as a general-purpose clock generator.
- 18-pin slimline package used; single +5V dc power required.
- Provides ability to stretch High and/or Low phase of clock signal under external control.
 - On-chip 2-bit counter can be used to selectively stretch clock cycles.
- On-chip reset logic
 - Reset output is synchronized with System Clock output.
 - Power-up reset period is maintained for a minimum of 30 ms.
 - External input initiates system reset.

GENERAL DESCRIPTION

The Z8581 Clock Generator and Controller is a versatile addition to Zilog's family of Universal microprocessor components. The selective clock-stretching capabilities and variety of timing outputs produced by this device allow it to easily meet the timing design requirements of systems with microprocessors and LSI peripherals. The clock output drivers of the Z8581 also meet the non-TTL voltage requirements for driving NMOS clock inputs with no

additional external components. The Z8581 provides an elegant, single-chip solution to the design of system clocks for microprocessor-based products.

The Z8581 oscillators are referenced as the system clock oscillator and the general-purpose clock oscillator. Both oscillators are driven by external crystals or other frequency sources.

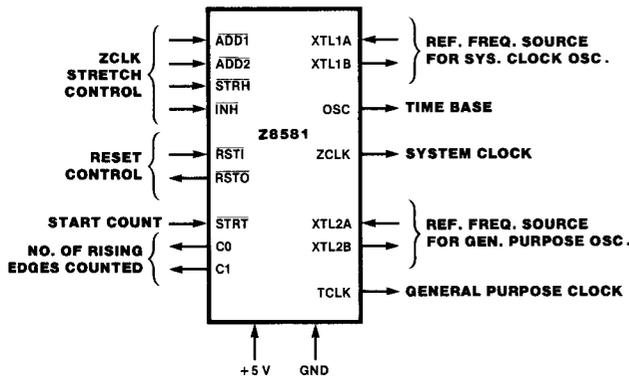


Figure 1. Pin Functions

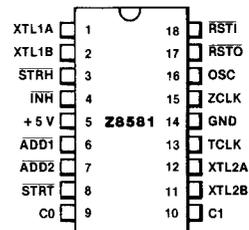


Figure 2. Pin Assignments

PIN DESCRIPTIONS

Figures 1 and 2, respectively, show the pin functions and assignments of the Z8581. Tie unused inputs High through a resistor.

ADD1, ADD2. *Add Delay 1* (input, active Low) and *Add Delay 2* (input, active Low). These signals control the addition of one, two, or three delay periods to a selected half-cycle of the ZCLK output.

C0, C1. *ZCLK Count 0* (output, active High) and *ZCLK Count 1* (output, active High). These signals indicate, in binary, the number or rising edges of ZCLK that have occurred after the assertion of the STRT input.

INH. *Inhibit Delay* (input, active Low). When asserted, this signal inhibits the functions of inputs ADD1 and ADD2.

OSC. *Time Base Clock* (output, active High). This signal provides a TTL-compatible clock output at the same frequency as the system clock frequency source.

RSTI. *Reset In* (input, active Low). When asserted, this signal indicates a reset condition and initiates the assertion of RSTO synchronized with ZCLK.

RSTO. *Reset Out* (output, active Low). When asserted, this signal indicates that a system reset condition is required, either by RSTI going Low or by a system powerup condition.

STRT. *Start Count* (input, negative edge-triggered). When asserted, this signal resets a two-bit binary counter and then enables the counter to count the rising edges of the ZCLK output.

STRH. *Delay ZCLK* (input, active Low). When asserted, this signal causes the current half-cycle of the ZCLK output to be delayed (stretched) for as long as STRH is held Low. This control input overrides the ADD1, ADD2, and INH functions.

TCLK. *General-Purpose Clock* (output, MOS-compatible, active High). This signal is the timing output of the general-purpose oscillator. TCLK's frequency is half that of the external oscillator used to drive the general purpose oscillator.

XTAL1A, XTAL1B. *System Clock Frequency Source A* (input, active High) and *System Clock Frequency Source B* (output, active High). These signals are used by the external oscillator to drive the internal system clock oscillator and the OSC output.

XTAL2A, XTAL2B. *General-Purpose Clock Frequency Source A* (input, active High) and *General-Purpose Clock Frequency Source B* (output, active High). These signals are used by the external oscillator to drive the internal general-purpose clock oscillator.

ZCLK. *System Clock* (output, MOS-compatible, active High). This signal is the timing output of the system clock oscillator. This clock can be modified by the delay (stretch) control inputs. Its frequency, when unmodified, is half that of the external system clock frequency source.

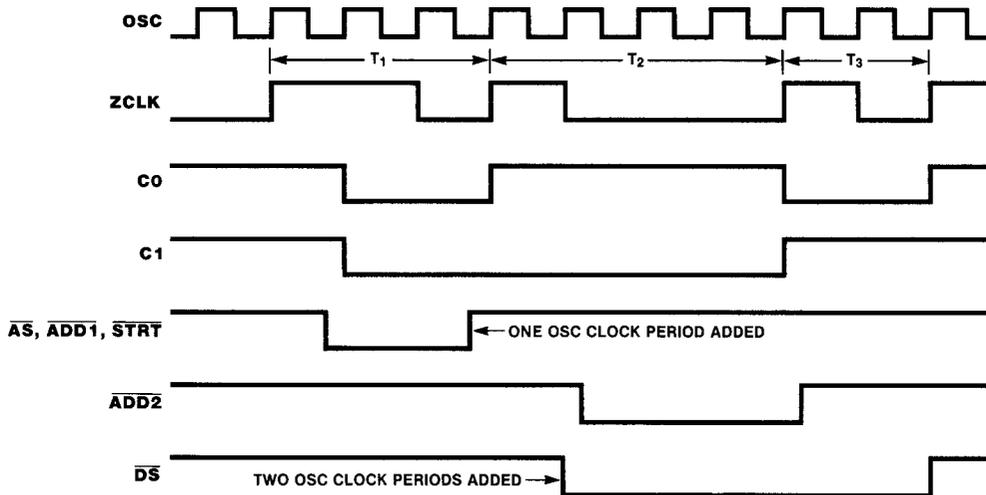


Figure 3. Timing Diagram Stretching Z8000 AS and DS

OSCILLATORS

System Clock Oscillator

The timing outputs provided by this oscillator consist of a Time Base output (OSC), at the frequency of the reference source, and a stretchable System Clock output (ZCLK), at a frequency determined by the stretch control inputs. An on-chip TTL driver at OSC and an NMOS driver at ZCLK eliminate the need for external buffers or drivers. The NMOS drivers can drive 200 pF loads with output rise and fall times of 10 ns maximum.

ZCLK can be stretched under program or hardwired control by selectively adding periods equivalent to a full OSC cycle to either the High or Low portion of a clock cycle. One, two, or three periods can be added to double, triple, or quadruple the duration of the selected ZCLK half-cycle. Adding periods to ZCLK is a function of the ADD1 and ADD2 inputs. These active Low inputs are sampled prior to the rising edge of signal OSC; their sampled status represents the number of periods to be added to ZCLK.

Two additional control inputs, $\overline{\text{INH}}$ and $\overline{\text{STRH}}$, affect the stretch function. Input $\overline{\text{INH}}$, when asserted, inhibits the function of $\overline{\text{ADD1}}$ and $\overline{\text{ADD2}}$. Input $\overline{\text{STRH}}$ stretches the ZCLK output for as long as it is asserted (Low); it overrides all other stretch control inputs.

Table 1 summarizes the functions performed by the stretch control inputs.

The system clock oscillator also contains a 2-bit ZCLK counter. This counter, when initialized by the assertion of $\overline{\text{STRT}}$, counts the next four rising edges of the ZCLK output. The current count is presented on outputs C0 and C1. This counter and its outputs enable the user to determine the occurrence (rising edge) of each of four clocks after a specific event ($\overline{\text{STRT}}$ is asserted). This facility can, for example, be used to determine when a delay is to be inserted into a CPU machine cycle when $\overline{\text{STRT}}$ is triggered by either an $\overline{\text{M1}}$ (Z80) or an $\overline{\text{AS}}$ (Z8000) input signal.

The clock stretch capability allows systems to run at the nominal high speed of ZCLK, except during cycles that

Table 1. Stretch Control Functions

STRH	INH	ADD2	ADD1	Periods Added
0	X	X	X	Unlimited
1	0	X	X	0
1	1	0	0	3
1	1	0	1	2
1	1	1	0	1
1	1	1	1	0

NOTES: X = Don't Care, 1 = High, 0 = Low

require more time than usual to complete a transaction. For example, extended access time may be required in accessing certain areas of memory, in accessing I/O devices, or in other CPU/Peripheral transactions. Figures 3 and 4 illustrate, respectively, the circuit configuration and timing required to stretch the Z8000 Address Strobe ($\overline{\text{AS}}$) and Data Strobe ($\overline{\text{DS}}$) to allow more time for address functions and to enable the CPU to operate with memories that have a relatively long access time.

In addition, the ZCLK stretch control logic can be hardwired to meet various duty cycle requirements. For example, a simple hardwired connection can cause every other ZCLK cycle to be stretched to produce a ZCLK output with a 33% duty cycle.

The system clock oscillator also provides a system reset output ($\overline{\text{RSTO}}$) that is synchronized with ZCLK. This output is controlled by a system reset input ($\overline{\text{RSTI}}$) during normal system reset operations and by delay circuitry in the system clock oscillator during power-up operations. During a normal system reset operation, a Low on $\overline{\text{RSTI}}$ causes $\overline{\text{RSTO}}$ to be asserted (Low) on the next rising edge of ZCLK. Output $\overline{\text{RSTO}}$ is held Low for a period of 16 ZCLK clock cycles (the required reset time for both the Z80 and Z8000 CPU system reset functions). During a power-up operation, $\overline{\text{RSTO}}$ is asserted for a minimum of 30 ms after power is turned on (the time required for both the Z80 and Z8000 power-up functions).

General-Purpose Oscillator

This oscillator provides a fixed frequency General-Purpose Clock output (TCLK) at half its source frequency. This output is useful for system timing functions such as controlling a baud rate generator. Output TCLK can also be used as the frequency reference source for the system clock oscillator.

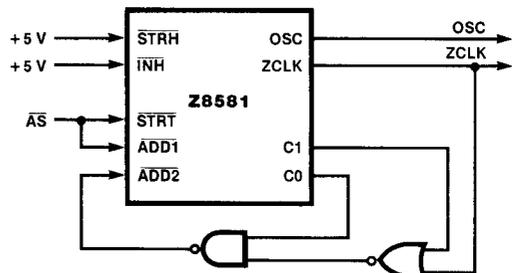


Figure 4. Configuration for Stretching Z8000 Address (AS) and Data (DS) Strobes

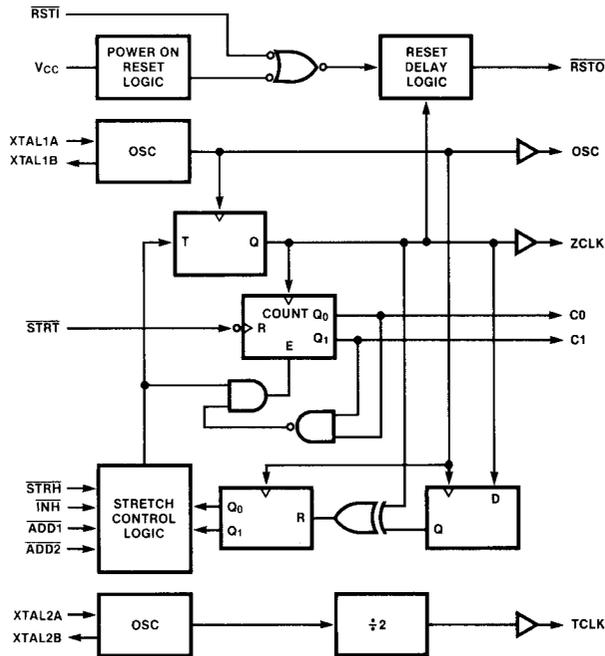
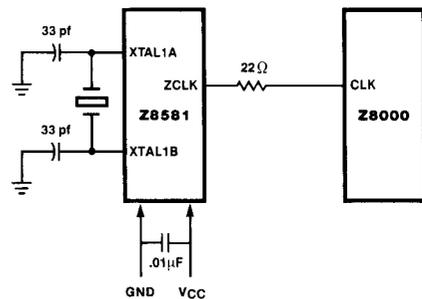


Figure 5. Z8581 Functional Block Diagram

SYSTEM INTERFACE CONSIDERATIONS

Due to the fast rise and fall times produced by the Z8581, transmission line concepts must be applied in order to avoid ringing and reflections on the clock outputs. More specifically, the interconnections between the clock outputs and the loads they are driving must be treated as transmission lines, and it is necessary to match the source impedance of the clock outputs to the characteristic impedances of these transmission lines. In most cases the impedances can be matched by placing termination resistors in series with the clock outputs. These resistors range in value from 22 to 220 ohms, with the value chosen to optimize the clock risetime at the load. (See example below.) It is important to control the impedance seen by the clock output by keeping leads short and avoiding stray inductances wherever possible.

Another important consideration is the bypass capacitor. To avoid distortion of the power supply, the Z8581 requires a high frequency 0.01 μF ceramic capacitor between V_{CC} and ground, and the leads connecting this capacitor to the pins should be kept as short as possible.



NOTE: The Z8581 requires a parallel-resonant fundamental type crystal. The capacitor may be varied to fine tune the frequency.

Figure 6. Z8581/Z8000 Interface

ABSOLUTE MAXIMUM RATINGS

Voltages on all inputs and outputs
 with respect to GND -0.3V to +7.0V
 Operating Ambient
 Temperature. See ordering information
 Storage Temperature -65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only: operation of the device at any

condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The Ordering Information section lists package temperature ranges and product numbers. Refer to the Literature List for additional documentation. Package drawings are in the Package Information section.

STANDARD TEST CONDITIONS

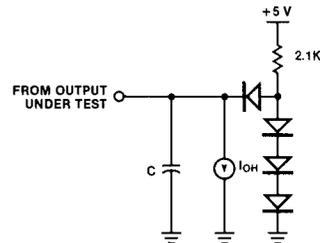
The DC characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Available operating temperature ranges are:

- S = 0°C to +70°C, +4.75V ≤ V_{CC} ≤ +5.25V
- E = -40°C to +85°C, +4.5V ≤ V_{CC} ≤ +5.25V
- M = -55°C to +125°C, +4.5V ≤ V_{CC} ≤ +5.5V

All ac parameters assume a total load capacitance (C), including parasitic capacitances, of 100 pf max, except for parameters 8, 9, 21, and 22 which are 200 pf max. Timing

references between two output signals assume a load difference of 50 pf max.



Z8581 CGC

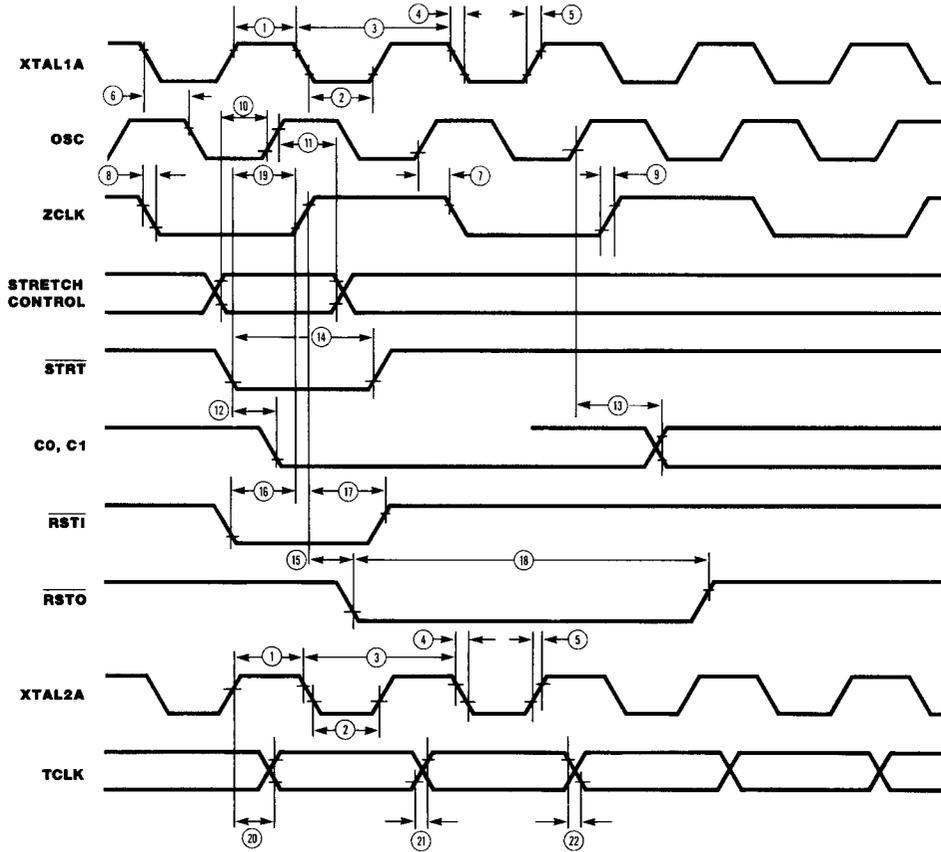
DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Condition
V _{CH}	Clock Input High Voltage	V _{CC} - 0.4	V _{CC} + 0.3	V	Driven by External Clock Generator
V _{CL}	Clock Input Low Voltage	-0.3	0.45	V	Driven by External Clock Generator
V _{IH}	Input High Voltage	2.0	V _{CC} + 0.3	V	
V _{IL}	Input Low Voltage	-0.3	0.8	V	
V _{OH}	Output High Voltage	2.4		V	I _{OH} = -250 μA
V _{OH} (ZCLK, TCLK)	Output High Voltage	V _{CC} - 0.3		V	I _{OH} = -250 μA tested at 5 μs after ZCLK or TCLK rises High
		2.4		V	I _{OH} = -250 μA
V _{OL}	Output Low Voltage		0.4	V	I _{OL} = +2.0 mA
I _{IL}	Input Leakage		± 10	μA	0.4 ≤ V _{IN} ≤ +2.4V
I _{CC}	V _{CC} Supply Current		150	mA	

AC CHARACTERISTICS

Number	Symbol	Parameter	Z8581 6 MHz		Z8581-10 10 MHz		Units	Notes ¹
			Min.	Max.	Min	Max		
1	T _w CH	Clock Input High Width	31		18		ns	2
2	T _w CL	Clock Input Low Width	31		18		ns	2
3	T _p C	Clock Input Cycle Time	82		50		ns	2
4	T _f C	Clock Input Fall Time		10		7	ns	2
5	T _r C	Clock Input Rise Time		10		7	ns	2
6	T _d OSC	Clock Input to OSC Delay		30		20	ns	
7	T _d ZC	OSC to ZCLK Delay		20		15	ns	
8	T _f ZC	ZCLK Fall Time		10		10	ns	
9	T _r ZC	ZCLK Rise Time		10		10	ns	
10	T _s SC	Stretch Controls to OSC ↑ Setup	35		20		ns	
11	T _h SC	Stretch Controls to OSC ↑ Hold	20		10		ns	
12	T _d (ST/CR)	STRT ↓ to 2-bit Counter Reset Delay		35		25	ns	
13	T _d (OSC/CC)	OSC ↑ to 2-bit Counter-Change		20		17	ns	3
14	T _w (STRT)	STRT Low Width	50		30		ns	
15	T _d (RSTO)	ZCLK ↑ to RSTO ↓ Delay		30		20	ns	
16	T _s (RSTI)	RSTI ↓ to ZCLK ↑ Setup	30		20		ns	
17	T _h (RSTI)	RSTI ↓ to ZCLK ↑ Hold	30		20		ns	
18	T _w (RSTO)	RSTO Low Width	16		16		cycles	
19	T _s (ST/ZC)	STRT ↓ to ZCLK ↑ Setup to include ZCLK edge	40		30		ns	
20	T _d TC	Clock Input to TCLK Delay		40		30	ns	
21	T _r TC	TCLK Rise Time		10		10	ns	
22	T _f TC	TCLK Fall Time		10		10	ns	

- NOTES: 1. All timings are preliminary and subject to change.
 2. Clock input other than a crystal oscillator.
 3. Assuming ZCLK rising.



Timing measurements are made at the following voltages:

	High	Low
ZCLK, TCLK	4.0V	0.8V
Output	2.0V	0.8V
Input	2.0V	0.8V

ORDERING INFORMATION

Clock Generator and Controller, 6.0 MHz

18-pin DIP

Z8581 PS
Z8581 CS
Z8581 PE
Z8581 CE
Z8581 CM*
Z8581 CMB*†

Clock Generator and Controller, 10.0 MHz

18-pin DIP

Z8581-10 PS
Z8581-10 CS
Z8581-10 PE
Z8581-10 CE
Z8581-10 CM*
Z8581-10 CMB*†

Codes

First letter is for package; second letter is for temperature.

C = Ceramic DIP
P = Plastic DIP
L = Ceramic LCC
V = Plastic PCC

R = Protopack
T = Low Profile Protopack
DIP = Dual-In-Line Package
LCC = Leadless Chip Carrier
PCC = Plastic Chip Carrier (Leaded)

TEMPERATURE

S = 0°C to +70°C
E = -40°C to +85°C
M* = -55°C to +125°C

FLOW

B = 883 Class B

Example: PS is a plastic DIP, 0°C to +70°C.

†Available soon.

*For Military Orders, contact your local Zilog Sales Office for Military Electrical Specifications.