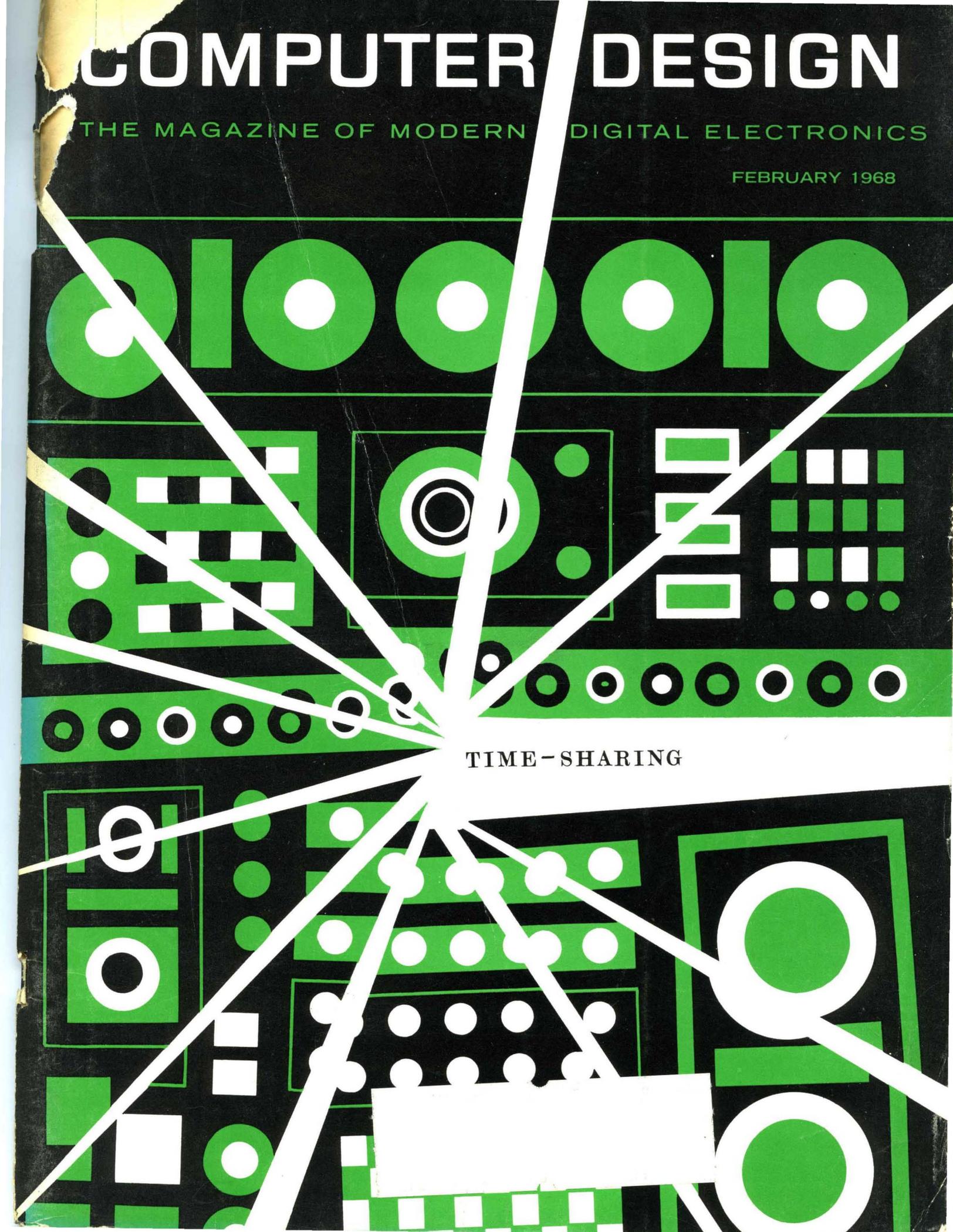


COMPUTER DESIGN

THE MAGAZINE OF MODERN DIGITAL ELECTRONICS

FEBRUARY 1968



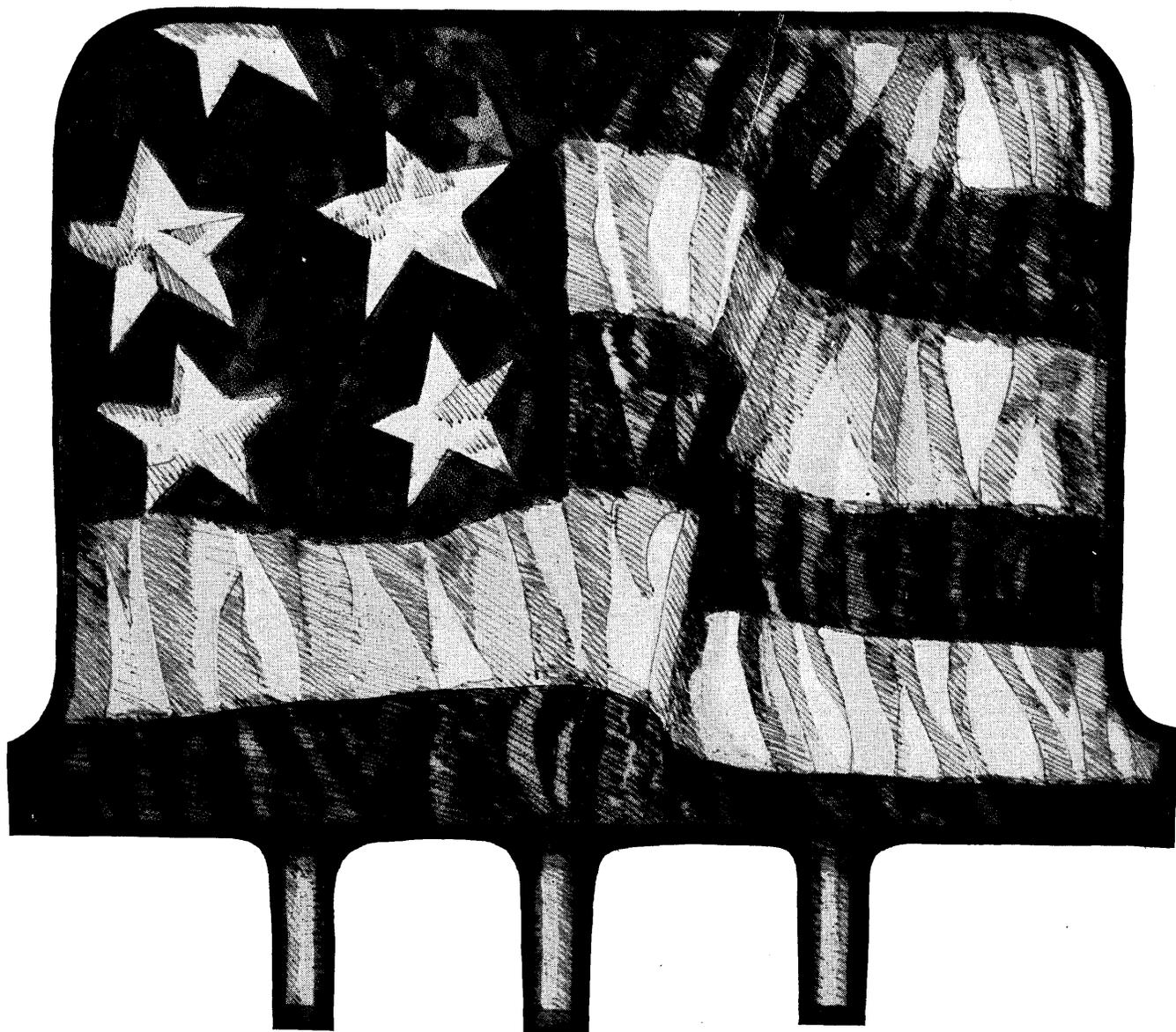
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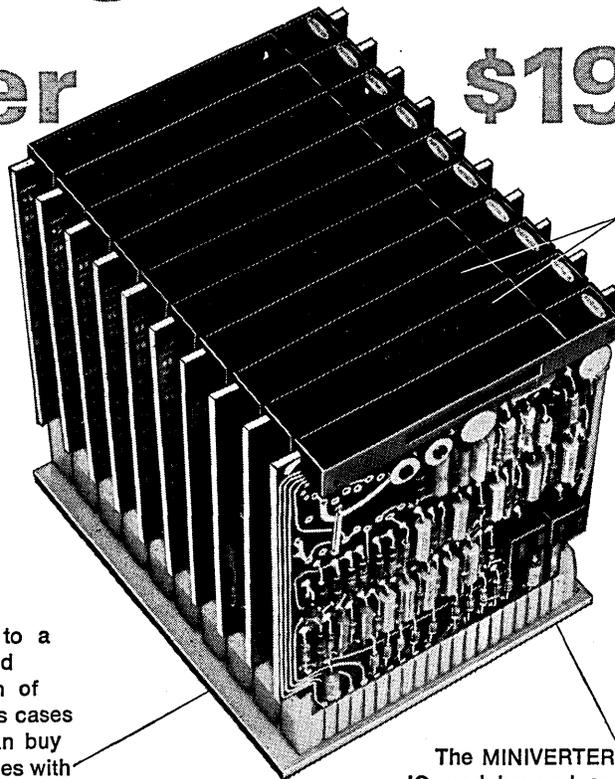
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A 16-channel multiplexer,
sample & hold amplifier
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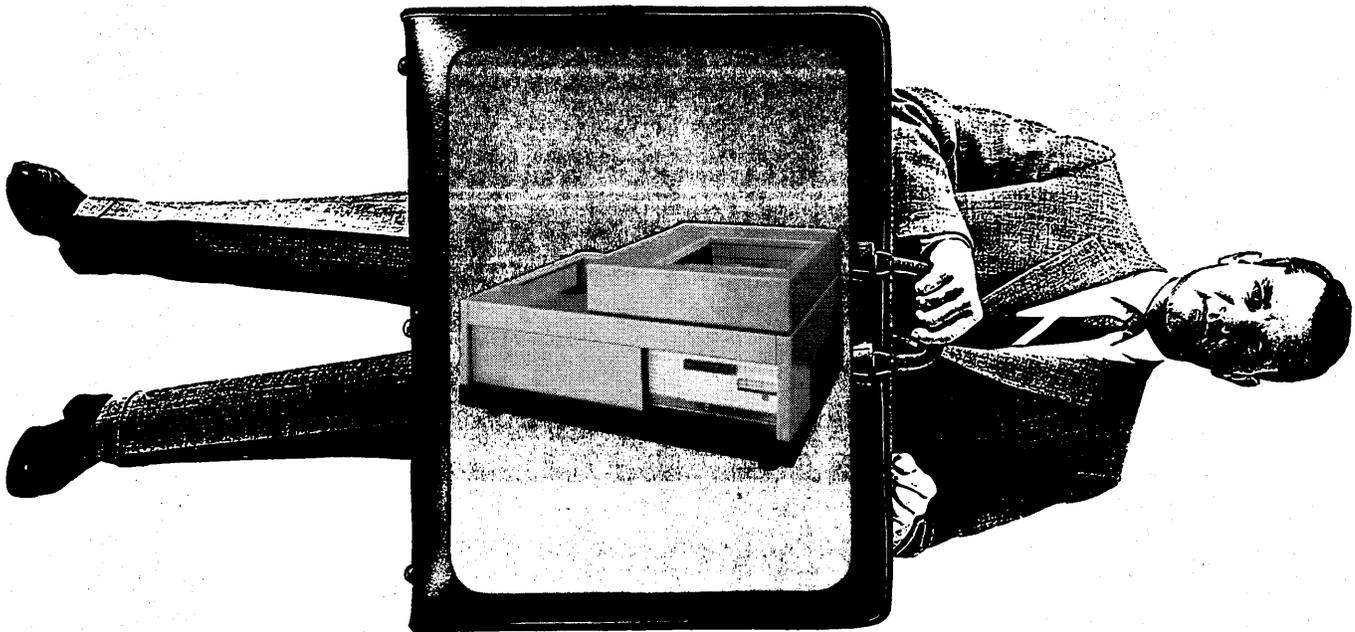
The MINIVERTER includes 9 M-Series IC modules and an analog power supply, all mounted on a compact connector block, pre-wired, tested and ready to use.

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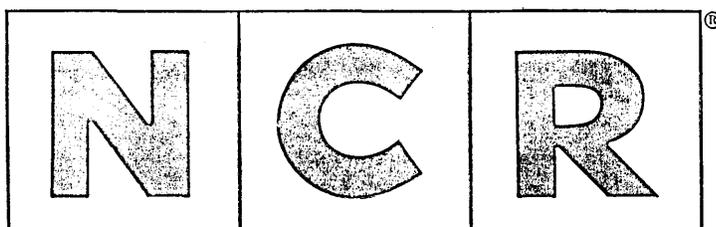
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COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

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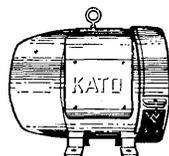
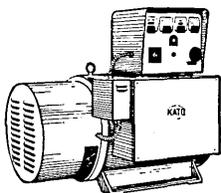
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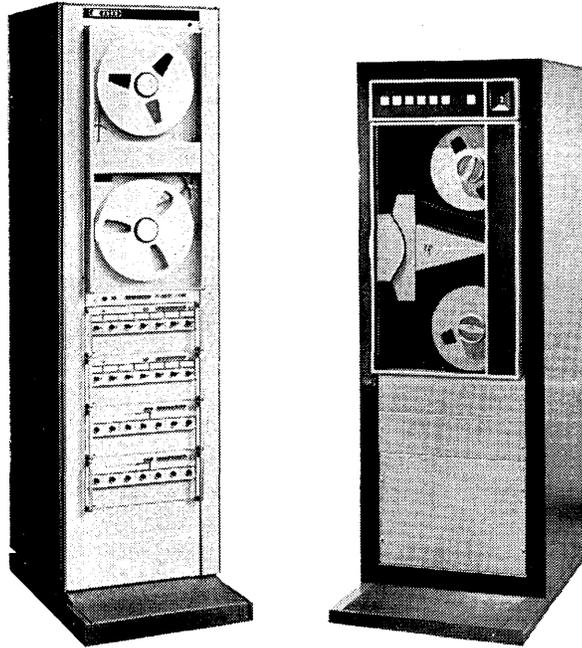
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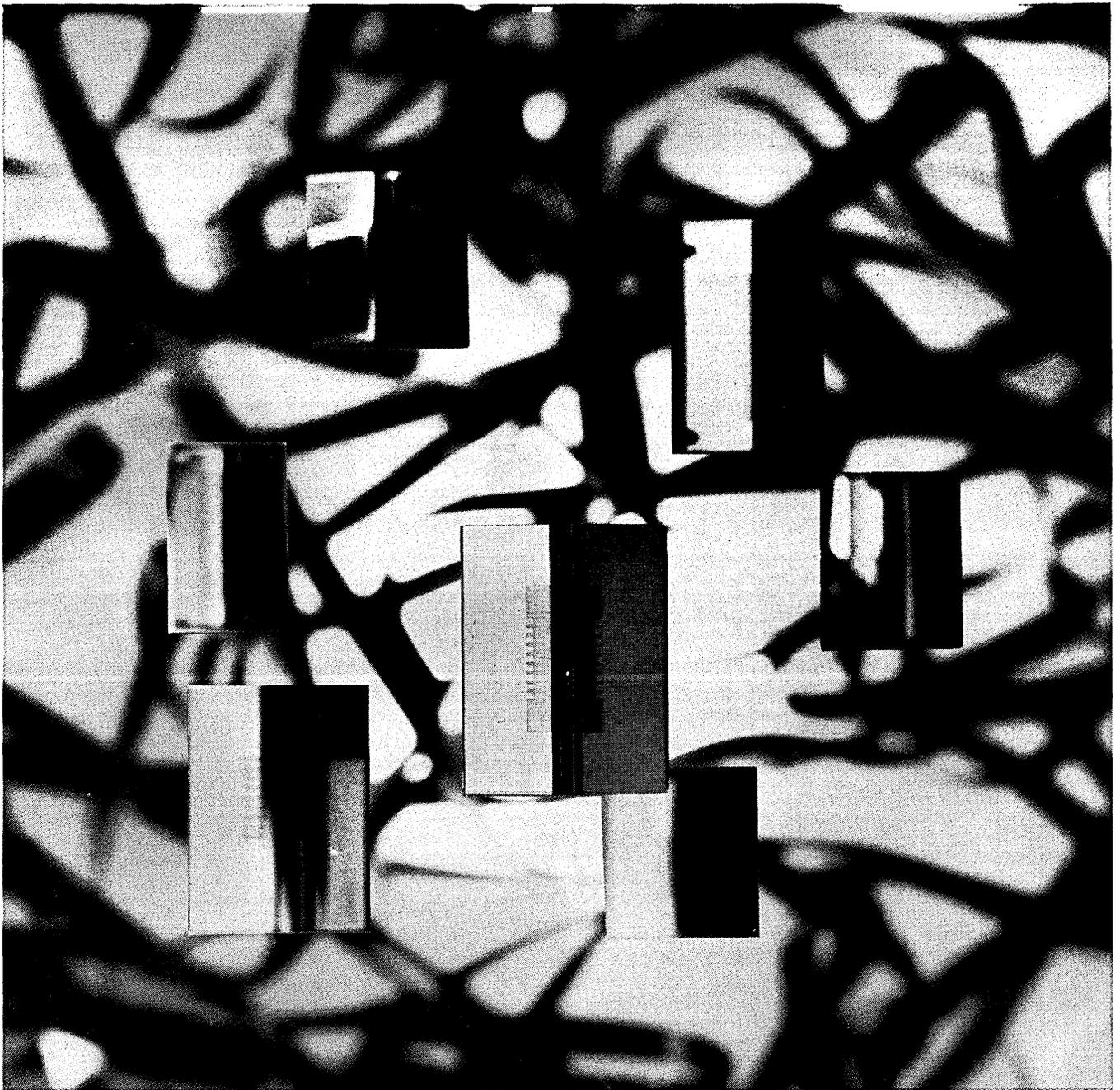
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CIRCLE NO. 7 ON INQUIRY CARD

← CIRCLE NO. 6 ON INQUIRY CARD



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These sparkling new Mark IV D-Subminiatures are *low-cost* connectors with *rear release*, *crimp snap-in* contacts. They're intermateable and intermountable with existing D-Subminiatures. The wine-colored insulators we selected enhance the connector as well as your equipment.

Robust BURGUN-D Mark IV connectors operate in temperatures up to 250°F. They are ideal for plug-in module

applications, cable-to-cable and cable-to-panel installation, computers, business machines and many other commercial applications.

Value analysis will tell you they're low in price because of highly developed pin and socket contacts. The contacts are available in two sizes (which accommodate 18 through 24 AWG stranded wire) and may be ordered separately. Contacts are rear inserted and extracted with a simple expendable plastic tool that's shown above. Closed-entry

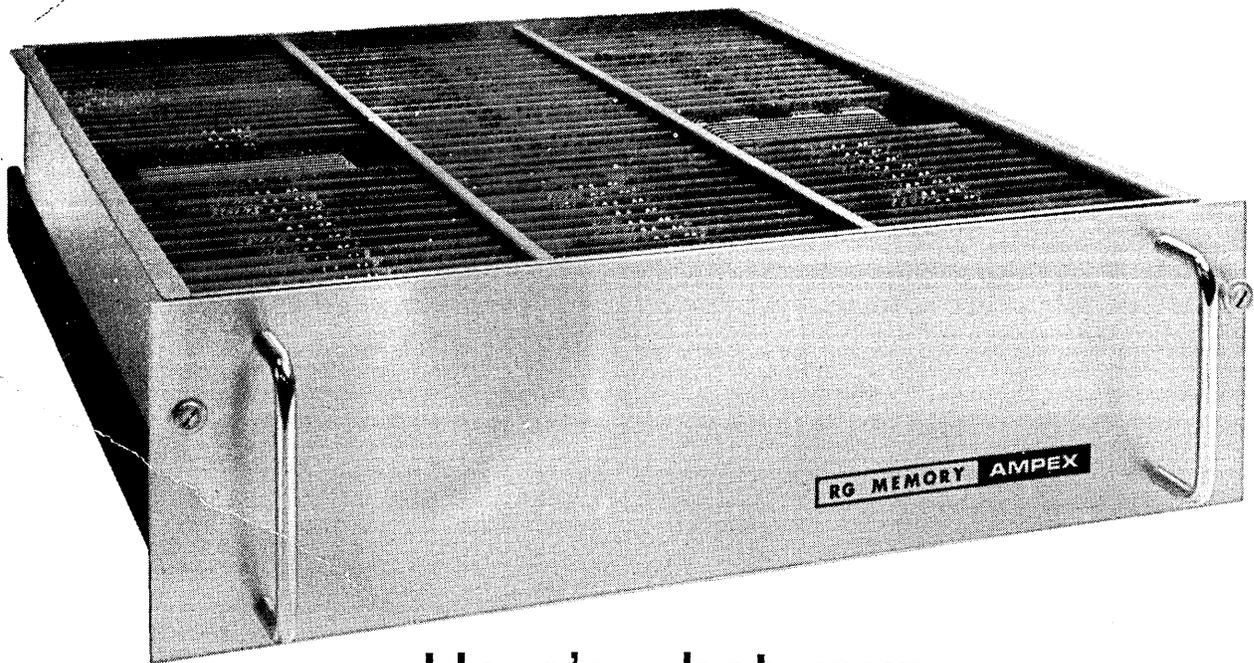
socket insulators correct any misalignment of pins during engagement.

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For our new catalog, write to ITT Cannon Electric, a division of International Telephone and Telegraph Corporation, 3208 Humboldt Street, Los Angeles, California 90031.



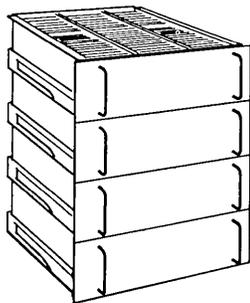
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1. Access data in 350 nanoseconds
2. Expand in modules to 5 million bits
3. Sell for less

When you're outlining the requirements of your new computer or system, pause a moment and consider what our new RG core memory offers: 350 nsec access; 900 nsec full cycle time; integrated circuitry; and expansion from a 4K memory all the way to 64K by addition of modules.



We think you'll want to design these features into your next system. The RG is low in cost, too. You pay less for the RG; your customers pay less for your system.

ALSO NEW FOR 512-TO-4096 WORD TASKS —THE RF-4 CORE MEMORY

This new, high-speed core memory, similar to our RF-1 memory, is built on one large PC board and is capable of word lengths to 20 bits. It uses integrated

circuitry and gives you high speed (1 microsecond cycle time) at low cost.

Check the specs. If they serve your purpose, please drop us a line, or circle the Reader Card number. We would like to send

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IMPORTANT SPECS		
	RG	RF-4
Access time	350 nsec	400 nsec
Full cycle	900 nsec	1000 nsec (half cycle: 650 nsec)
Size (inches)	5¼ x 19 x 21 (per memory module)	5¼ x 19 x 21 (including power supply)
Capacity:	4096; 8192; 12,228; or 16,384 words, expandable in modules to 65,536 words	512 to 4096 words
Word length:	24 to 80 bits	4 to 20 bits

AMPEX

CIRCLE ON. 9 ON INQUIRY CARD

Contemporary Electronics is one of the largest producers of computer pulse transformers in the U.S.

SO?

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Advantages? Here are some.

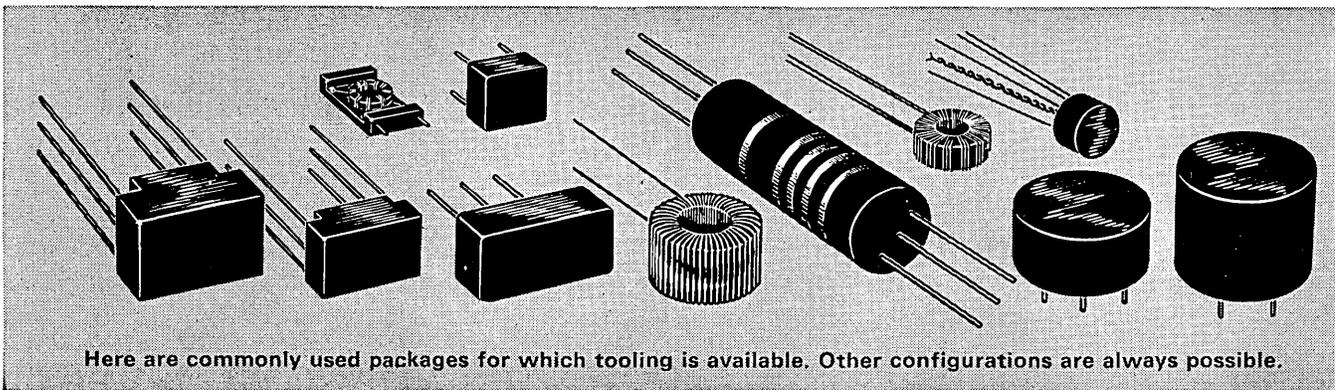
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CIRCLE NO. 10 ON INQUIRY CARD

Cheap mass storage for small computers and how to get the most out of it

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DIGITAL, the leader in small computers, has a low-cost disc and unique magnetic tape unit tailored for the small computer. Now, new software is available to take even better advantage of this low-cost memory.

DECdisc adds 32,768 words of memory for \$6,000. Additional expander discs (up to 3) can be added at \$3,000 each. That means a total of 131,072 words of disc memory for \$15,000.

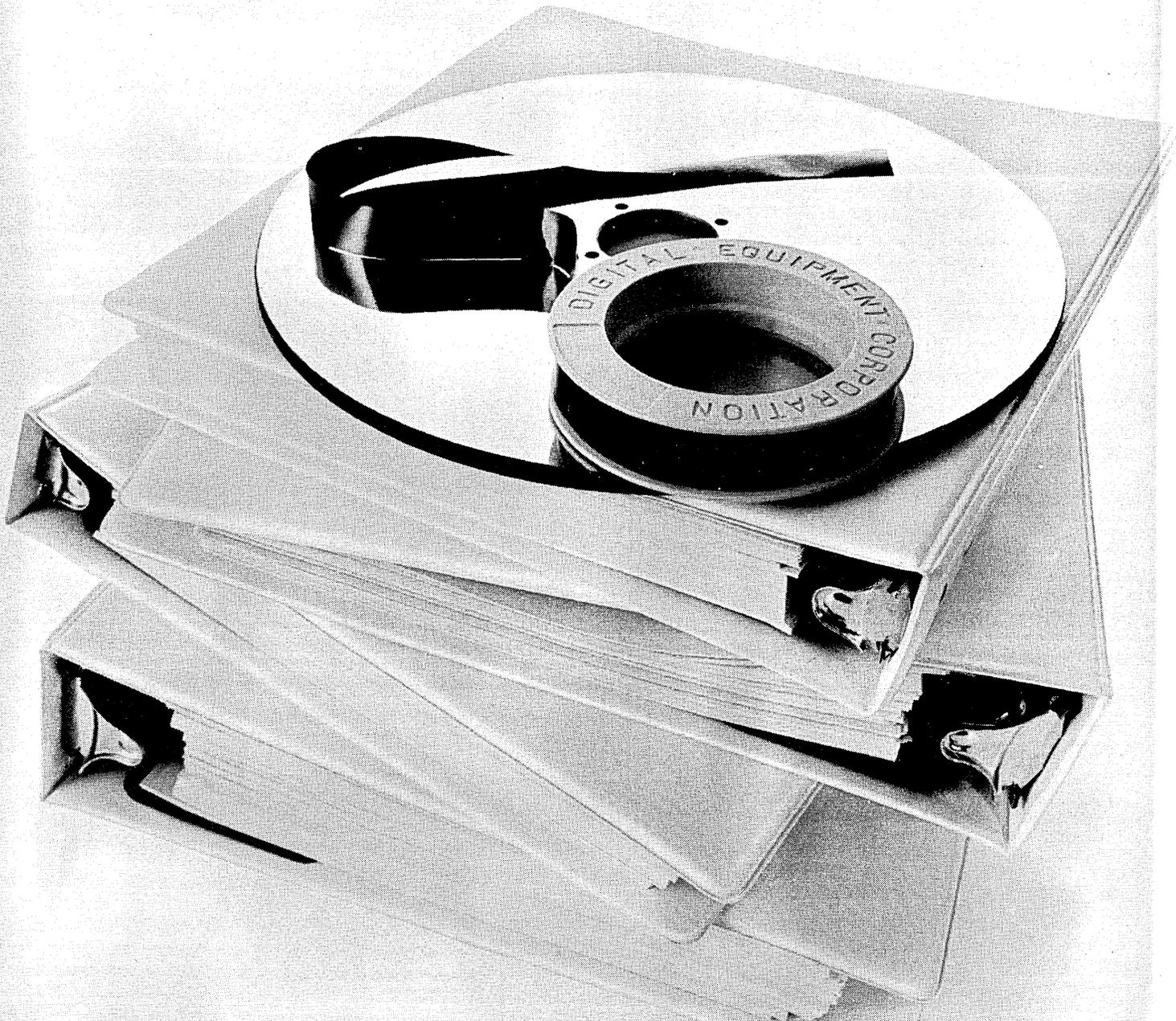
A full scale PDP-8/S computer with 36,864 twelve bit words of memory, for example (4k core plus disc), costs \$18,500.

DECTape, Digital's unique fixed address magnetic tape sys-

tem, provides over 200,000 words of storage on a 3½-inch reel. It's the lowest cost mass storage available anywhere. You can edit and debug programs on line. Then you can put your programs in your pocket and take them away until you want them again.

New keyboard monitor software all but eliminates the laborious use of paper tape and cards. You edit from the keyboard, compile from the keyboard, assemble, load, store, debug all from the keyboard. What might have been hours or days in getting the computer ready for use, is now just minutes.

Available now. PDP-8/S off-the-shelf. PDP-8 in one month. PDP-8/I in the spring. DECdisc and DECTape immediately available. Send for our new Small Computer Handbook. It's free.



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It's a buyer's market. Now you can get exactly the right logic cards to design your logic systems the way you want them . . . without settling for fall-out cards from general purpose computers . . . and without going to all the expense of building specials.

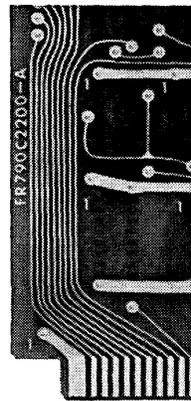
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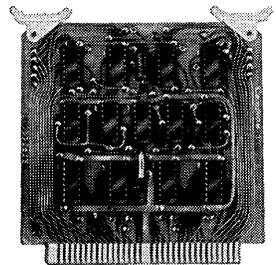
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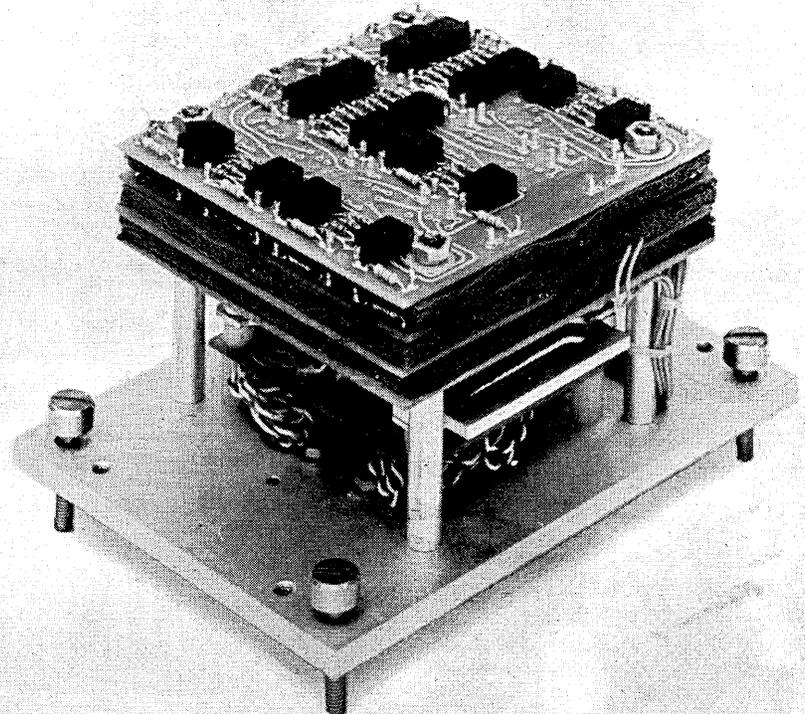
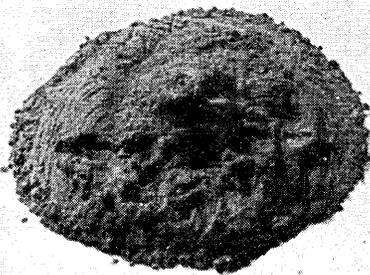
much of this looks like textbook QC procedure. But some of it goes deeper. It's the kind of control you associate with a veteran airline pilot whose experience amounts almost to intuition. As pioneers in ferrites and core memory components, we have people like that in control at every vital stage of manufacture.

This is one reason why Ferroxcube can design and build to exacting requirements (example: military stacks that exceed the en-

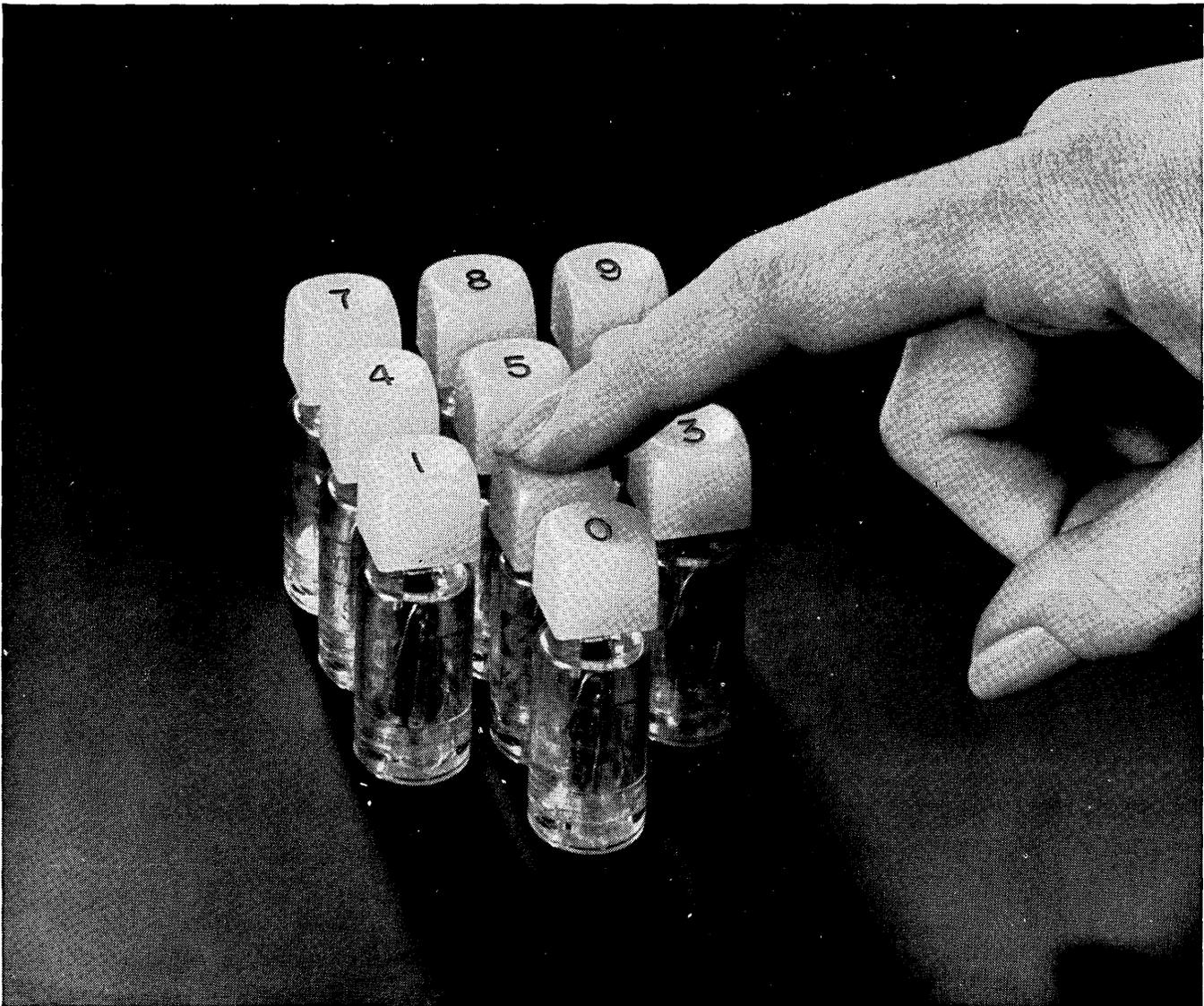
vironmental requirements of MIL-E-16400 and MIL-E-5400). And it's the main reason why every production unit performs like the prototype you approved.

If you specify cores, planes or stacks, talk with the people who pioneered ferrite technology. As a conversation piece, a sheaf of technical literature awaits you. Write for it today.

Ferroxcube 
Saugerties, New York



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These new keyboard switches feature unusually precise action and low-cost mounting. See for yourself—write for samples.

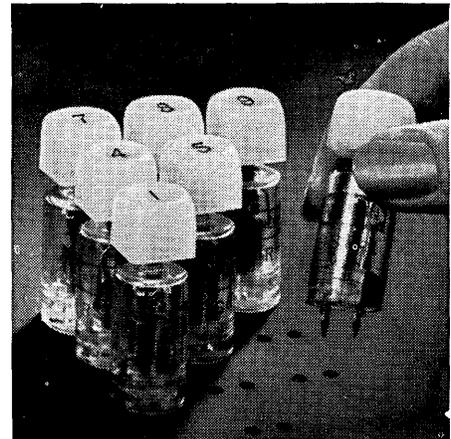
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Designed by Raytheon, they have a featherlight touch that is precise and reliable. Just a 3-oz. touch activates the switch. Because of the unique design, this action can be repeated more than 10 million times. Yet the switches cost as little as 60¢ in production quantities.

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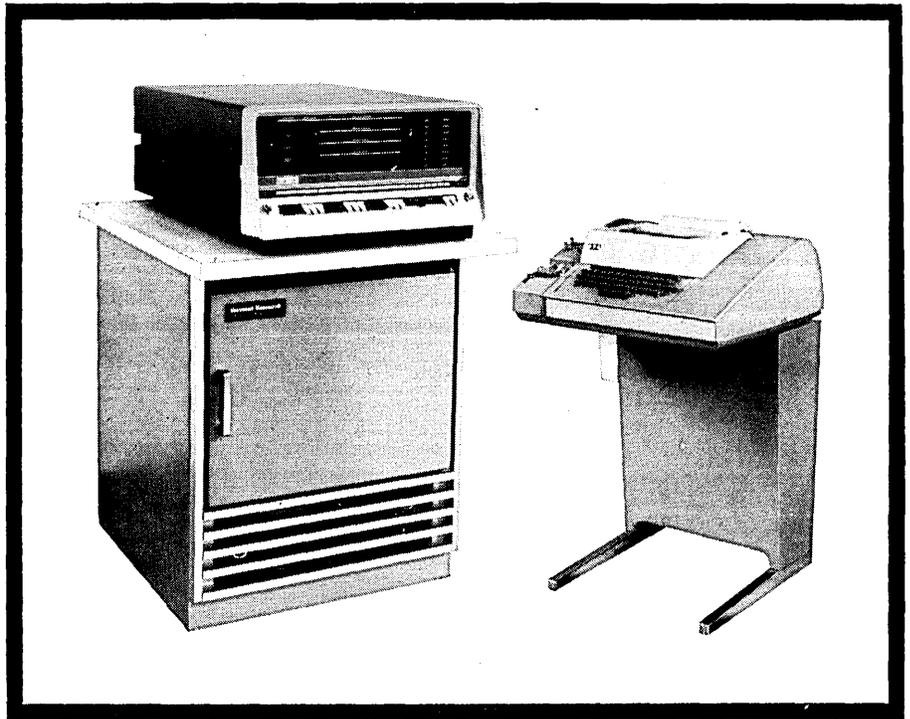
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CIRCLE NO. 15 ON INQUIRY CARD

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2 FOLDED STACK — We've built hundreds of these for SDS computers over the past year. With a 4K x 9 bit capacity, the stack uses our 20 mil cores, and turns out a cycle time of 830 nanoseconds.

3 HIGH/LOW TEMP STACK — This 8K x 18 bit 2½ D, built for RCA, uses our special lithium cores. They have a low temperature coefficient and excellent stability over a 10°C to 55°C range. The beauty of this is that the customer doesn't have to bother with temperature compensation.

4 COMPACT STACK WITH LARGE CAPACITY — For Honeywell, we put together a 32K x 18 bit prototype stack in a space of 600 cubic inches (10" x 20" x 3"). This stack uses our

20 mil cores and has a cycle time of less than 650 nanoseconds.

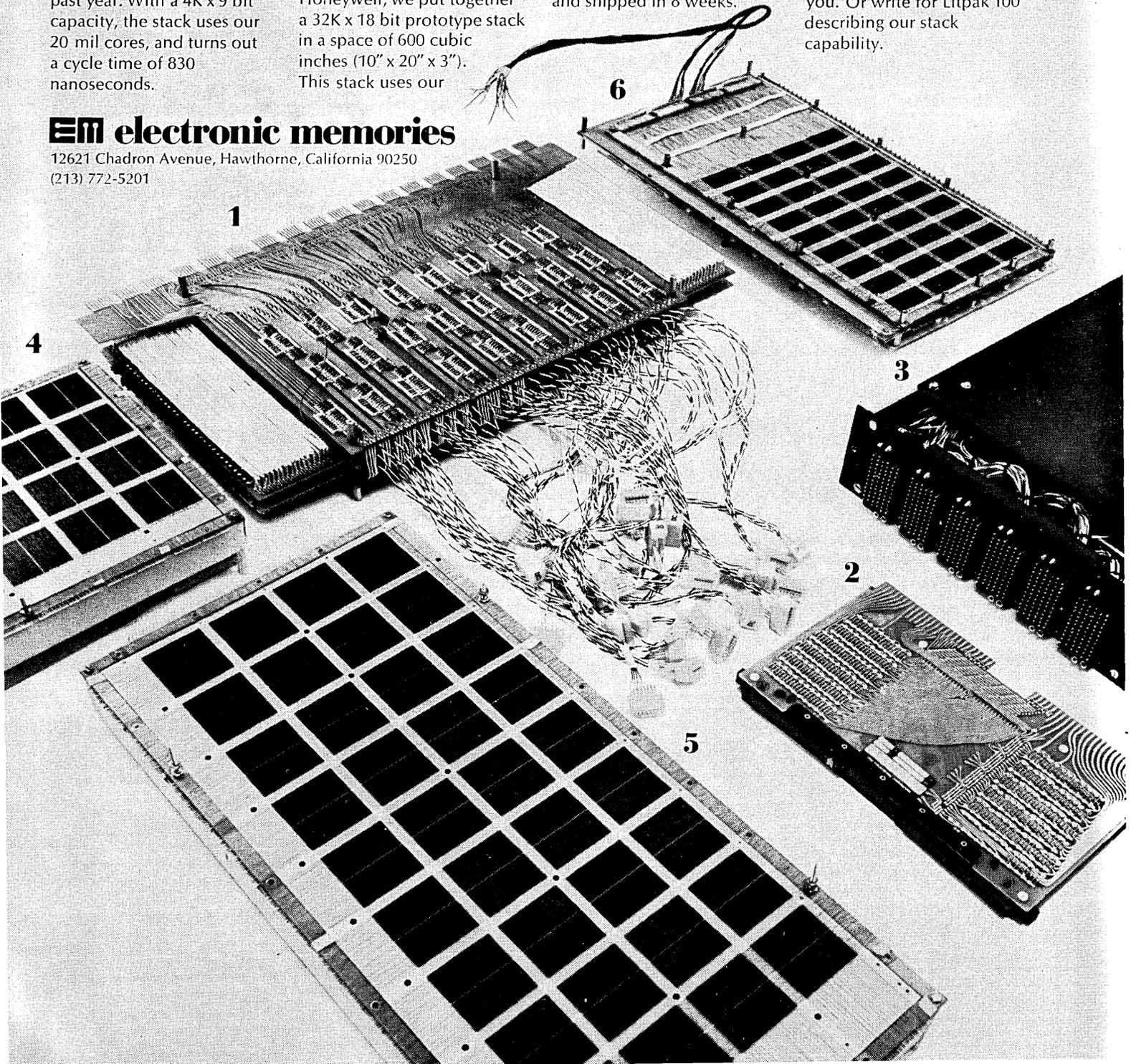
5 SPLIT MODULE STACK — This was a tricky one for Raytheon. It was a special 16K x 18 bit stack, and two sets of diode modules in the word direction had to be placed on each side of the stack. (Usually, they're all on one side.) The whole stack was designed, built, and shipped in 8 weeks.

6 NANOSTACK™ — We use this one in our large capacity NANOMEMORY system, but we've also been making a modified version for over a year and a half for Digital Equipment Corp. The stack has an 8K x 18 bit capacity and measures only 10½" x 20½" x 2".

If your 2½ D requirements are off-beat, call us, and we will see what we can do for you. Or write for Litpak 100 describing our stack capability.

EM electronic memories

12621 Chadron Avenue, Hawthorne, California 90250
(213) 772-5201



no time for errors

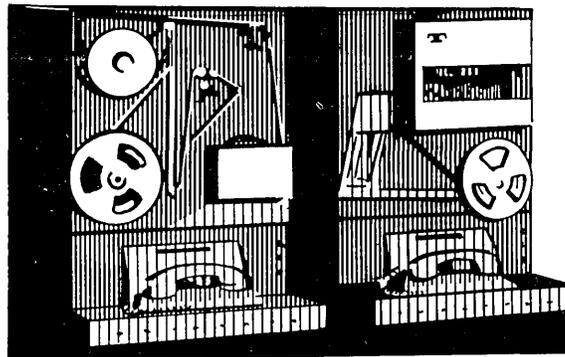
Transmitting data at high speeds through large switching systems is a major factor in the effectiveness of sophisticated data systems. However, without some automatic method for detecting and correcting errors fast, an entire real-time operation could be in jeopardy.

TELESPEED EQUIPMENT IS THE ANSWER

Telespeed 1200 EDC paper tape equipment is designed specifically to automatically detect and correct errors. It operates at 120 characters per second (1200 words per minute), or less when required. It can utilize any 5, 6, 7 or 8-level code including the officially approved United States of America Standard Code for Information Interchange (USASCII).

Operation of the Telespeed 1200 EDC equipment is based on the transmission of redundant information. The sending set transmits data in blocks of 80 characters without the need for special tape format.

Two redundant check characters are generated by a separate tape-reading head on the sending set, and by a photoelectric reader on the receiving set. The two sets of characters are



TELESPEED 1200
EDC EQUIPMENT

compared by the receiving terminal, and transmission continues if the characters agree.

CORRECTING AN ERROR

When the Telespeed 1200 EDC receiving set detects an error, the tape containing the block in which the error occurred is pulled back and retransmitted. The receiving set also

pulls back the erroneous tape block and overpunches all code levels prior to receiving the retransmitted block.

The fact that the two sets of check characters are generated from reading both the original tape and the output tape adds another benefit to the Telespeed 1200 EDC equipment. It not only detects any transmission errors, but also checks the accuracy of the terminal equipment.

For further information on Teletype error detection and correction equipment, send for free literature. Contact: Teletype Corporation, Dept. 71B, 5555 Touhy Avenue, Skokie, Illinois 60076.

machines that make data move



CIRCLE NO. 17 ON INQUIRY CARD

Reader's Choice

IEE introduces 10-gun CRT Display Tube



New readout offers 12 advantages over tubes now in use.

The state of the readout art took on a new dimension recently when IEE, world leader in rear-projection readouts, introduced the 10-gun CRT — an unparalleled method for electronic projection of numbers, letters, messages, etc. Observers report character brightness and clarity, viewed on a fluorescent screen, are optimum under any ambient light condition. Powerless control grid switching... extremely low power consumption... small grid control swing... exceptionally wide view angle... all are features which make the new device ideal for instrument applications. Now available in quantity, all it lacks is a name!

Name IEE's new display tube and win a portable TV set!

On your company letterhead, describe a particular application for the new tube. Then fill in the coupon, attach it to the letter and send them to:



ADVERTISING DEPARTMENT
7720 Lemona Ave.,
Van Nuys, Calif. 91405

Sirs:

My name for the new IEE 10-gun CRT display tube is _____

Name: _____

Firm: _____ Dept.: _____

Address: _____

City: _____ State: _____ Zone: _____

Entries must be in by Feb. 28, 1968. The judges' decision will be final.

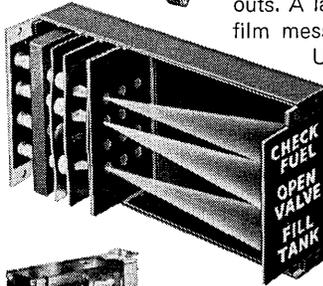
IEE bright, legible, wide-angle readouts:

Any characters desired
Any colors or combinations
Any input, BCD or decimal
Any input signal level
Any mounting, vertical or horizontal

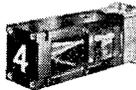
Many sizes
Many configurations
Many lamp lives (to 100,000 hours)
Many brightness choices
Many options and accessories



Standard Readouts: Rear projection principle, like all IEE readouts. A lamp in the rear of the unit illuminates one of the 12 film messages, and projects it to the front viewing screen. Unbeatable readability and versatility.



Large Screen Readouts: For reading distances up to 100 feet. Maximum character size 3 3/8".



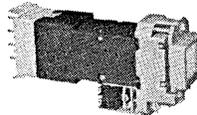
Miniature Readouts: Only 1" wide x 1-5/16" high, yet can be read at 30 feet because of clarity of one-plane projection. Character size: 5/8".



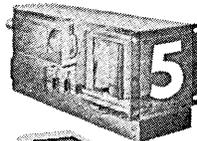
Micro-Miniature Readouts: Only 1/2" wide x 3/4" high, but 20 foot viewing distance and maximum 175° viewing angle because of front-plane display. Character size: 3/8"



Hi-Brite Readouts: Special lens system increases character brightness 50%. Particularly good when high ambient light conditions exist.



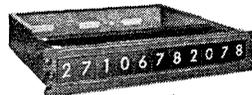
Cue-Switch Readouts: Rear projection readout with push-button viewing screen. Combination switch and display device.



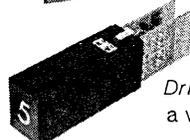
Bina-View Readout: Accepts binary or teletype code, decodes, and displays the proper character.



Status Indicator Readout: Displays up to 12 different messages, individually or in combination. Viewing screen only 3 sq. in.



Indicator Assemblies: Available with up to 11 rear projection readouts, for indicating seconds, minutes, hours, days, etc.



Driver/Decoder Module: Designed to work with IEE Readouts. Accepts a variety of binary codes for decimal conversion.

The new IEE Display Devices catalog gives complete information and specifications on these products, and their accessories. Ask for it.



"I-double-E", the world's largest manufacturer of rear projection readouts.
Industrial Electronic Engineers, Inc. 7720 Lemona Avenue, Van Nuys, California

keeping track of the ins and outs

Teletype data communications equipment serves as the terminals in a variety of computer systems. Many systems designers specify Teletype terminal equipment because they have found the sets to be the most reliable, versatile, and economical available.

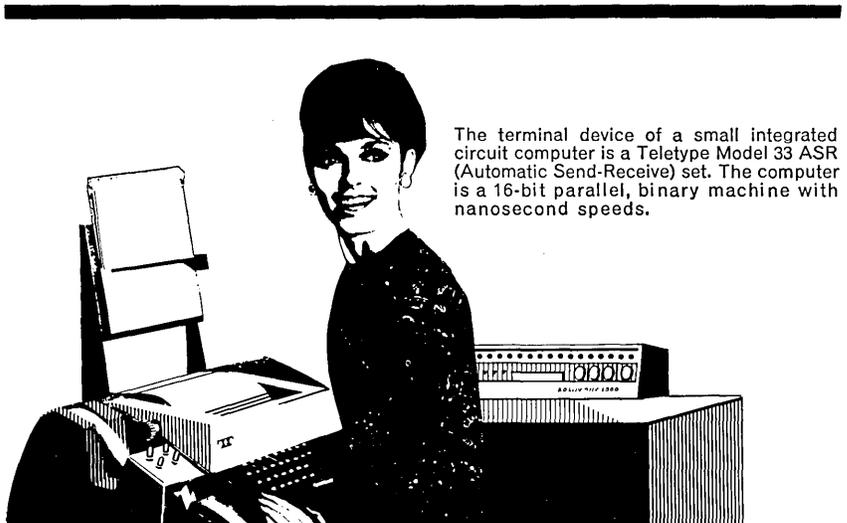
The examples below point up the many capabilities of Teletype equipment as used in a number of different computer systems.

AIDS SCIENTIFIC COMPUTATIONS

Primarily designed for control applications and scientific computations, a computer that uses monolithic integrated circuits can be operated alone, as a multiprocessor system, or as a satellite to a larger computer system. A Teletype Model 35 KSR (keyboard send-receive) set is the system's terminal. It uses an 8-level code compatible with the United States of America Standard Code for Information Interchange (ASCII).

AIDS BILLING AND INVOICING

An electronic billing and invoicing machine uses a Teletype Model 33 ASR (automatic send-receive) set to provide on-line communications involving a variety of accounting data. Continuous pin-feed invoice forms with multiple copies are used in the system. In addition, a punched by-product tape is prepared for further analysis by management.



The terminal device of a small integrated circuit computer is a Teletype Model 33 ASR (Automatic Send-Receive) set. The computer is a 16-bit parallel, binary machine with nanosecond speeds.

Users of a time shared computer system can contact the computer for service and inputs of all instructions, data, and plot programs through standard Teletype equipment. The computer processes the data and transmits via a Model 33 ASR set a complete plot program, including identification codes for that particular plotter and output signals for remote on-line plotting.

A compact 16-bit real-time computer provides high-speed data acquisition and control. The system multiplies and divides faster, has a faster throughput and costs less than many larger systems. It uses a Teletype Model 33 ASR set as its terminal.

AIDS TO YOUR SYSTEMS

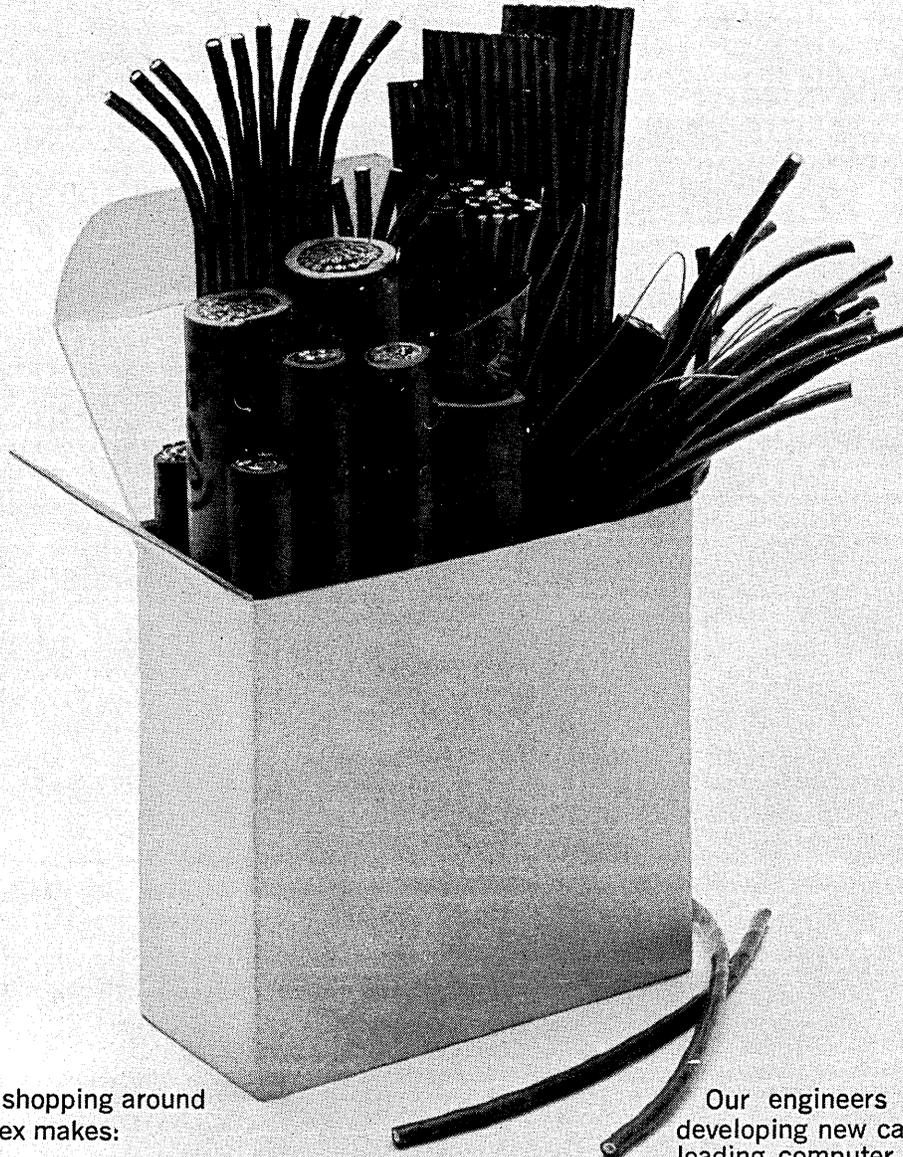
These are only a few of the many Teletype equipment applications in both large and small computer systems. To learn how Teletype equipment can aid the systems you're designing, send for our brochure, "ALL ABOUT TELETYPE EQUIPMENT." Contact: Teletype Corporation, Dept. 71B, 5555 Touhy Avenue, Skokie, Illinois 60076.

machines that make data move



CIRCLE NO. 19 ON INQUIRY CARD

**Yes. You can get every
wire and cable you need
for a computer system in
one neat package...from
Brand-Rex**



You save a lot of shopping around because Brand-Rex makes:

- **Back-Panel Wires**
- **Hook-Up Wires**
- **Miniature, Air-Spaced Coaxial Cable**
- **Power Supply Wires**
- **Patch Cord Wires**
- **Interconnecting cables and Communication Cables.**

You can have just about any configuration... single wire, round cable, ribbon cable, custom profiles... and your choice of insulations including Kynar, Polysulfone, Teflon (FEP and TFE), PVC, semi-rigid PVC, PVC/nylon, polyethylene, foamed polyethylene, FEP/nylon, Rulan and Neoprene. Matched colors if you want.

Our engineers are constantly developing new cable designs for leading computer manufacturers. So if existing Brand-Rex products don't meet your needs, we'll come up with new designs that will.

Hooking-up a computer system? Get all the wire and cable from one good source. Ask Brand-Rex.

AMERICAN  CORPORATION
BRAND-REX DIVISION
WILLIMANTIC, CONNECTICUT 06216
PHONE 203 423-7771



DATA COMMUNICATIONS

equipment for on-line,
real-time processing

...at the press of a button

Time. In today's data communications and processing systems it is measured in microseconds. And Teletype R&D engineers know it. For instance, look at the Push Button Data Generator they have developed to cope with the situation.

The PBDG is an automatic data preparation unit that simplifies and speeds the flow of fixed data. By preprogramming fixed data into the PBDG, you can automatically print up to 24 alphanumeric and other characters by *pressing a single button*.

AIDS COMPUTER OPERATION

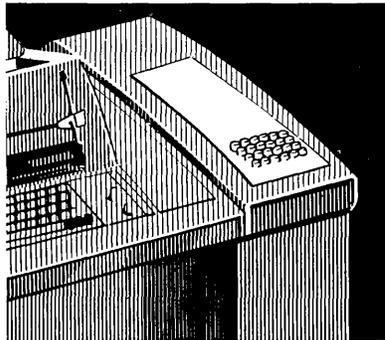
The PBDG can be used wherever there is a need for automatic handling of repetitive data. For instance, in a time sharing system, the intricate instructions needed to activate the computer for a particular user can be programmed into the PBDG, and transmitted automatically to the computer merely by *pressing the appropriate button*.

In addition, the PBDG offers many important advantages to data communications and processing operations. Information is stored and reproduced in the same form every

time at the press of a button. Data is easily programmed or reprogramed for automatic transmission of fixed data. This saves time, saves key strokes, and eliminates errors.

GENERATES 288 CHARACTERS

Operating on either a 5 or 8-level code, the basic Teletype PBDG unit consists of 12 pushbuttons capable



Cabinet at right of this Teletype Model 35 ASR set houses control panel and circuitry of Push Button Data Generator

of generating a total of 288 characters. The PBDG can be used as a self-contained unit or combined with other Teletype equipment to punch paper tape, print page copy, or transmit to a remote unit.

Programming is made and/or changed simply by movement of push-on type terminals. No technical skill is needed to make or change a program. The unit also may be programmed to stop on any predetermined character position. This permits insertion of variable information from a keyboard. After the variable data has been entered, automatic entry of fixed data is continued *at the press of a button*.

AVAILABLE IN SPECIAL CABINET

Where space permits, the PBDG control panel and its associated electronics can be housed in a Teletype printer console. When more than 24 pushbuttons are needed, special cabinets can be provided that contain as many as 96 buttons in units of 12.

For more information about transmitting your data *at the press of a button*, simply request our PBDG data sheet by contacting: Teletype Corporation, Dept. 71B, 5555 Touhy Avenue, Skokie, Illinois 60076.

machines that make data move



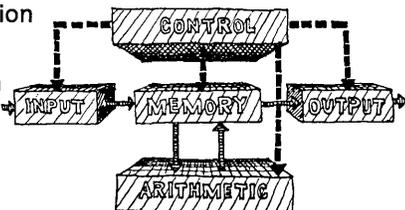
CIRCLE NO. 21 ON INQUIRY CARD

The great LSI race.

While the rest of the semiconductor industry tried to squeeze enough ICs on a chip to get into the MSI/LSI business, Fairchild turned systems inside out. We were looking for an intelligent alternative to component mentality. Our investigation led to a whole new set of design criteria for medium and large scale integration devices.

A computer isn't a computer.

It's a digital logic system. It has the same functional needs as any other digital system: control, memory, input/output and arithmetic. There's no logical reason to custom design a complex circuit for each system. That's why Fairchild MSIs and LSIs are designed to function as fundamental building blocks in any digital logic system. Even if it's a computer.



A little complexity goes a long way.

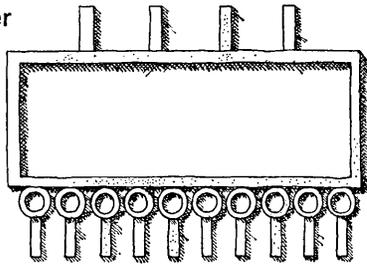
Anybody can package a potpourri of circuitry and call it MSI or LSI. But, that's not the problem. Why multiply components, when you should divide the system? Like we did. We found that sub-systems have a common tendency toward functional overlap. There are too many devices performing similar functions. More stumbling blocks than building blocks. Our remedy is a family of MSIs and LSIs with multiple applications. The Fairchild 9300 universal register, for example, can also function as a modulo counter, shift register, binary to BCD shift converter, up/down counter, serial to parallel (and parallel to serial) converter, and a half-dozen other devices.

Watch out for that first step.

There are all kinds of complex circuits. Some of them have a lot of headache potential. Especially if you want to interface them with next year's MSIs and LSIs. We decided to eliminate the problem before it got into your system. All Fairchild building blocks share the same compatible design characteristics.

We're also making the interface devices that tie them together. For example, our 9301 one-of-ten decoder can be used as an input/output between our universal register, dual full adder and memory cell.

(It could also get a job as an expandable digital demultiplexer, minterm generator or BCD decoder.)



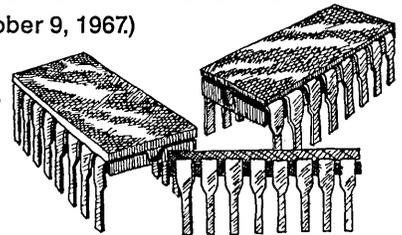
Hurry. Before the price goes down.

Gate for gate, today's complex circuits are about the same price as discrete ICs. But, by the time you're ready to order production quantities, the price should be a lot lower. At least ours will. The reason is simple: Fairchild devices are extremely versatile. There are fewer of them. But, they do more jobs. That means we'll be producing large quantities of each device. That also means low unit cost to you. And you'll have fewer devices to inventory. And fewer to assemble.

If you agree with our approach to medium and large scale integration, we'd like to tell you more about it. There are two ways you can get additional information. One is by mail. Simply write us on your company letterhead. You can also get more data by watching the trade press. Fairchild is introducing a new integrated circuit each week for 52 weeks. (We started on October 9, 1967)

Many of them will be MSI and LSI.

If you'd like to see the last few we've introduced, turn the page.

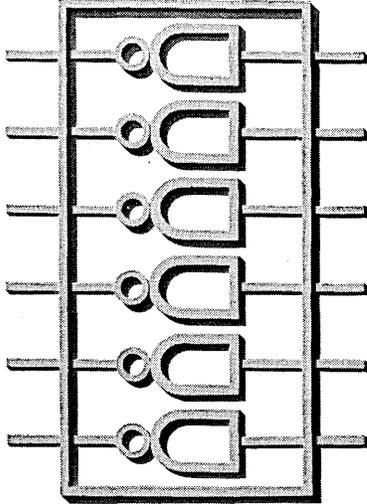


FAIRCHILD SEMICONDUCTOR

A Division of Fairchild Camera and Instrument Corporation
313 Fairchild Drive, Mountain View, California 94040
(415) 962-5011, TWX: 910-379-6435

RECAP:

9112 HIGH LEVEL HEX CONVERTER

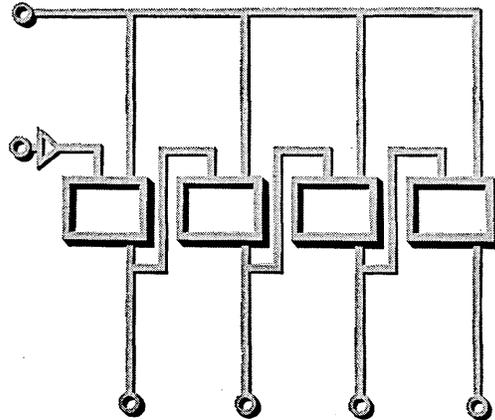


Fairchild Semiconductor / A Division of Fairchild Camera and Instrument Corporation
FAIRCHILD
 SEMICONDUCTOR 3155 Parkside Drive, Mountain View, California 94035, (415) 352-0011 • FAX: (415) 352-0020
 CIRCLE READER SERVICE NUMBER 106

Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number **6.**

The 9112 is part of our new family of high noise immunity integrated circuits. It is designed to convert CMOS input levels to high logic levels. It is ideal for driving MOS devices. The 9112 consists of six high-level DTL gates. Each gate performs a single inversion operation. Worst case noise immunity is 2.5 volts. This high voltage device operates over the entire range of 0 to 200°C. It comes in an hermetic dual in-line package and is available in volume quantities. Fairchild distributors have it in stock now. Write for complete specs and applications information. Ask about our other new products, too.

9989 FOUR-BIT BINARY COUNTER

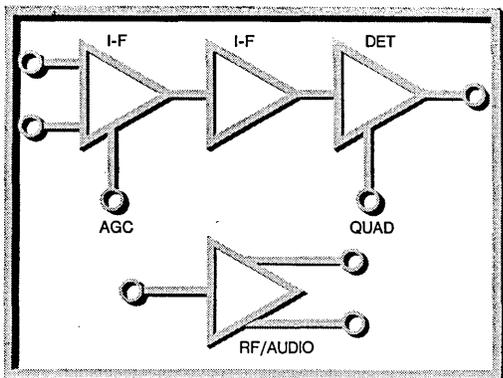


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 CIRCLE READER SERVICE NUMBER 107

Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number **7.**

The 9989 is a low-cost, high-reliability, modulo-16 counter in a single package with present capability. It is compatible with the entire CAI family and can operate directly into RTL, DTL, or TTL circuitry. Typical power dissipation is only 150mW. Its operating frequency is 15MHz. It is designed to operate in the 0°C to +70°C temperature range with minimum power supply voltage of 2.5 to 5.5 volts. The 9989 comes in a 16-pin hermetic DIP. Primary applications include counters, event meters and logic conversion functions. The 9989 is available in volume quantities. Fairchild distributors have it in stock now. Write for complete specs and applications information. Ask about our other new products, too.

JA719 HIGH FREQUENCY COMMUNICATIONS SYSTEM

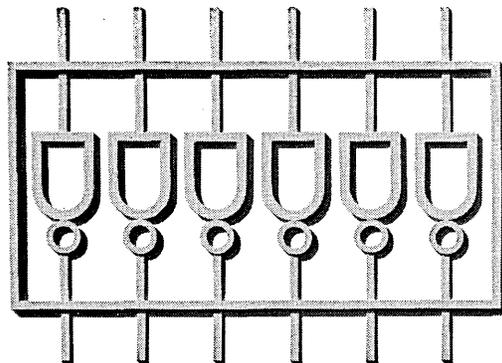


Fairchild Semiconductor / A Division of Fairchild Camera and Instrument Corporation
FAIRCHILD
 SEMICONDUCTOR 3155 Parkside Drive, Mountain View, California 94035, (415) 352-0011 • FAX: (415) 352-0020
 CIRCLE READER SERVICE NUMBER 108

Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number **8.**

The JA719 is a new Dual Integrated Circuit for military and industrial communications systems. It can function as an FM detector, an AM or FM amplifier, a modulator or an audio amplifier. It contains two independent amplifiers designed for IF systems to 50MHz, a frequency-accurate stability (FSS) variable gain AGC capability and extreme flexibility. And, it has three capacitors directly on the chip. The JA719 comes in a hermetic TO-99 package. It's available in quantity in both military and industrial temperature ranges (-55°C to +125°C and 0°C to +70°C). Your Fairchild distributor has it in stock now. Write for complete specs and applications information. Ask about our other new products, too.

9935 EXPANDABLE HEX INVERTER



Fairchild Semiconductor / A Division of Fairchild Camera and Instrument Corporation
FAIRCHILD
 SEMICONDUCTOR 3155 Parkside Drive, Mountain View, California 94035, (415) 352-0011 • FAX: (415) 352-0020
 CIRCLE READER SERVICE NUMBER 109

Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number **9.**

The Fairchild 9935 is a fundamental element in the CMOS family. It can serve as the inverse of virtually any digital logic circuit. It consists of six DTL gates without input diodes. Each gate performs a single inversion operation. The device can be expanded to an unlimited number of inputs and outputs. Each gate can be used in a great variety of functions. For example, it can serve as a buffering circuit, a manual multiplier, or as a full adder. In adders, registers, counters, decoders, etc. It can be "wired or" connected to reduce overall system cost. The 9935 comes in both a 16-pin hermetic DIP and Fairchild's Cerpak™. It's available in both military and industrial temperature ranges (-55°C to +125°C and 0°C to +70°C). Propagation delay is typically 25 nanoseconds. Typical power dissipation is 100mW per gate. The 9935 is available in volume quantities. Fairchild distributors have it in stock now. Write for complete specs and applications information. Ask about our other new products, too.

Fairchild is introducing a new integrated circuit every week. The last two months look like this.

FAIRCHILD
SEMICONDUCTOR

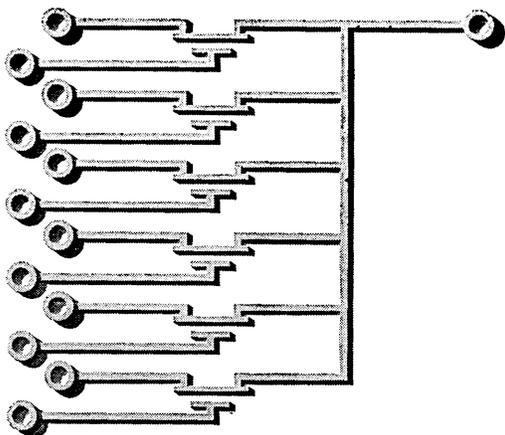
Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number **10.**

3701 SIX-CHANNEL MULTIPLEX SWITCH

The Fairchild 3701 is a P-channel enhancement mode MOS an-channel single output switch. It can be used in virtually any switching application. It's ideal for analog and digital data conversion, logic control in excitation systems, and sense line switching in core memory systems. The 3701 approximates a perfect switch. It has very low "on" resistance (500 Ohms), extremely high "off" resistance (2 x 10¹⁰ Ohms), and zero output leakage. Output leakage current is specified as low as 0.1 nanowatts. Input gate protection minimizes handling problems. It can accept minor static up to 5 volts. Safety and reliability are assured by "Planar II" technology. The 3701 comes in a 16 pin package. It will operate over a temperature range of -55°C to +85°C.

Volume quantities of this device are now available. Your Fairchild distributor has it in stock. Write for complete specs and applications information. Ask about our other new products, too.

*There is a patented routing process.



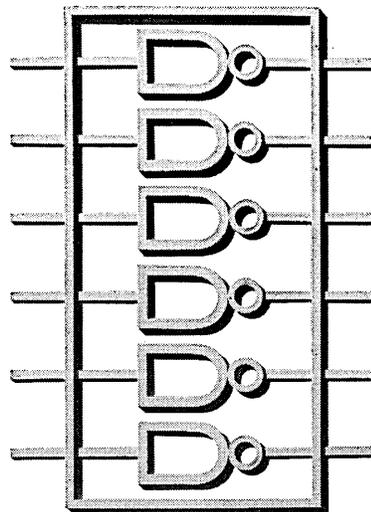
FAIRCHILD SEMICONDUCTOR / A Division of Fairchild Camera and Instrument Corporation FAIRCHILD SEMICONDUCTOR 310 Fairchild Drive, Mountain View, California 94035 (415) 961-8111 TWX: 910-274-0448

CIRCLE READER SERVICE NUMBER 110

Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number **11.**

9016 TTL HEX INVERTER

The 9016 completes our 8000 series TTL family. It is a CMOS device designed primarily for high speed inverter applications. It consists of six inverting gates with input clamping diodes to prevent ringing. Active pull-up is provided in the output for high capacitive drive. It can also be used as a line driver. Propagation delay is 11 nanoseconds maximum. Fan-out of four for general TTL family. Power dissipation per gate is typically 15mW. The 9016 comes in a 14-lead hermetic DIP and in package. It is available in both military and commercial temperature ranges (-55°C to +125°C and 0°C to +70°C). You can now order volume quantities of the 9016. Fairchild distributor has it in stock. Write for complete specs and applications information. Ask about our other new products, too.



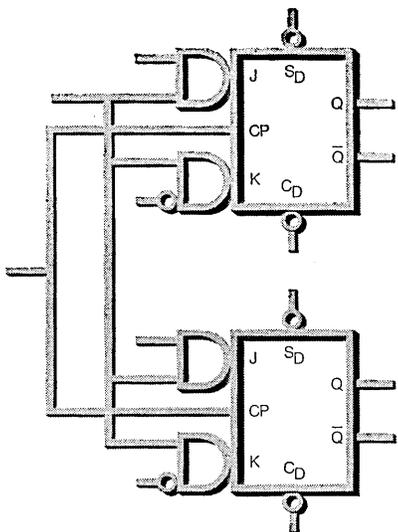
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CIRCLE READER SERVICE NUMBER 111

Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number **12.**

9022 DUAL JK FLIP-FLOP

The 9022 is a CMOS device in a 16-pin hermetic DIP. This TTL circuit consists of two JK flip-flops with a common clock input, common JK input, and separate J and K inputs. The K allows the 9022 to perform as a clock type D flip-flop by tying J and K inputs together. The common clock eliminates the need for gating clock waveforms and can result in simplified logic designs and minimized clock skew problems. The 9022 is fast (20ns) and fan-outable. It is a true DC sensitive master-slave dual flip-flop. As a comparison to our 8000 dual JK flip-flop, it provides additional logical flexibility because it has separate set-direct inputs in addition to clear-direct. Both types of inputs are truly asynchronous and overriding. A simple clock buffer reduces clock bounce and noise. The 9022 comes in both military and industrial temperature ranges (-55°C to +125°C and 0°C to +70°C). It is available in volume quantities. Your Fairchild distributor has it in stock. Write for complete specs and applications information. Ask about our other new products, too.



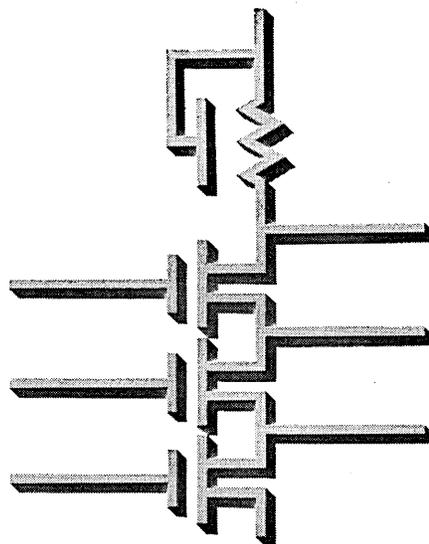
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CIRCLE READER SERVICE NUMBER 112

Starting October 8, 1987, Fairchild promised to introduce a new integrated circuit each week for 52 weeks. This is number **13.**

3102 MOS THREE- INPUT GATE

The 3102 is an extremely versatile three-input breadboard gate which can serve as the fundamental element of a CMOS digital logic system. It can also function as an evaluation tool for determining the performance of Fairchild's line of MOS devices. It is ideal for prototyping, laboratory and MOS integrated circuitry. The 3102 comes in both TO-5 and TO-9 packages. Power dissipation per gate is typically 15mW. The 3102 provides excellent logic handling in logic protection reduces handling problems. Power consumption is typically as low as 10mW. Operating temperature ranges from -55°C to +85°C. Volume quantities of the 3102 are now available. Your Fairchild distributor has it in stock. Write us for complete specs and applications information. Write your e-mail, ask about our other new products, too.



FAIRCHILD SEMICONDUCTOR / A Division of Fairchild Camera and Instrument Corporation FAIRCHILD SEMICONDUCTOR 310 Fairchild Drive, Mountain View, California 94035 (415) 961-8111 TWX: 910-274-0448

CIRCLE READER SERVICE NUMBER 113

Having trouble communicating with the modern generation?

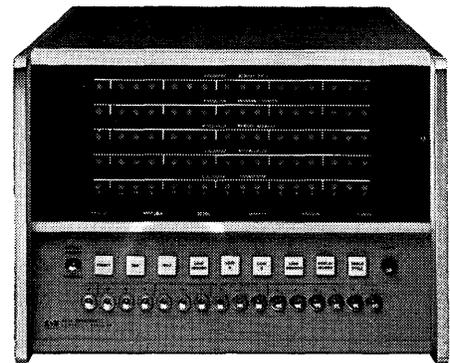
HP software makes it easy.

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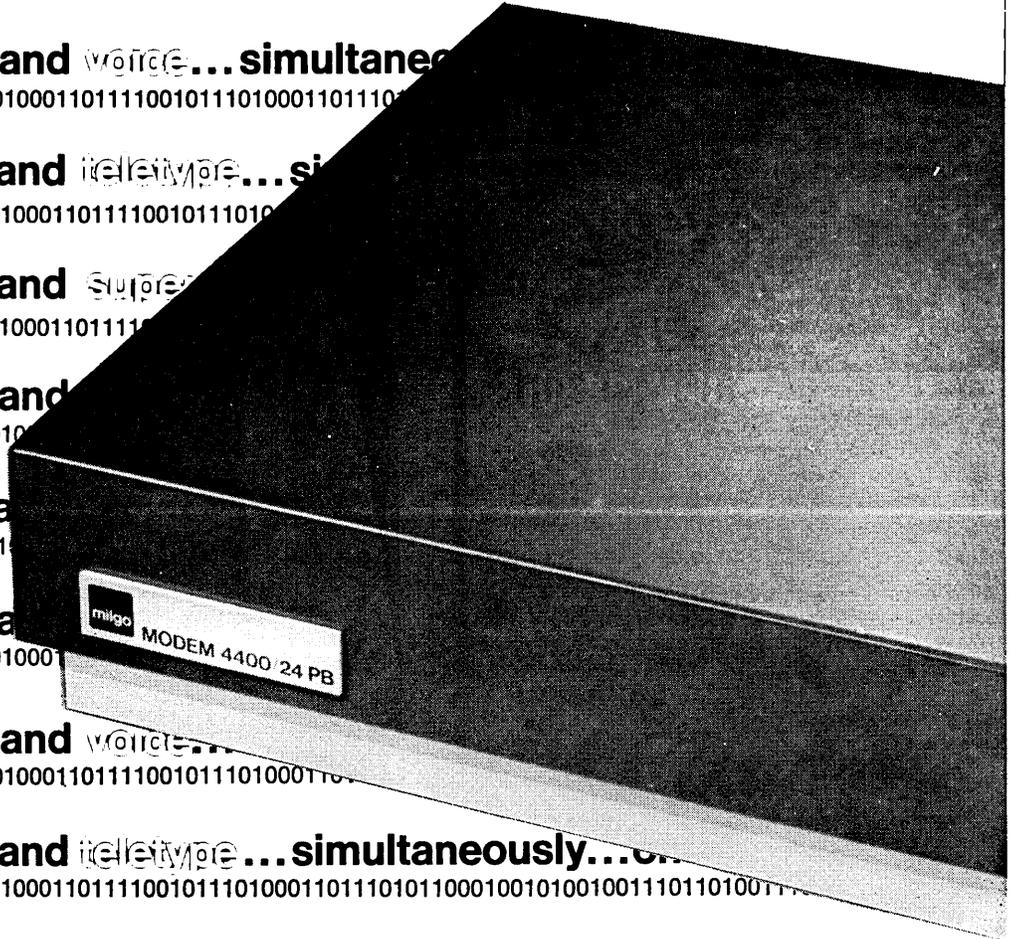
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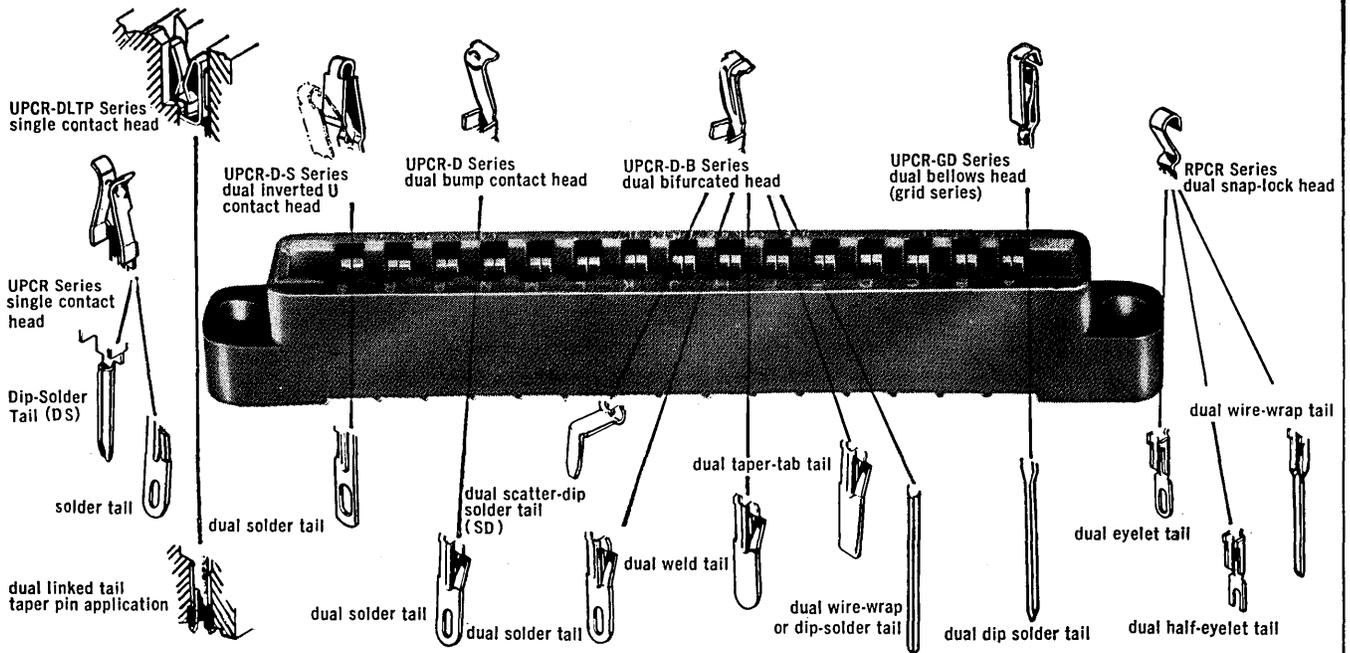
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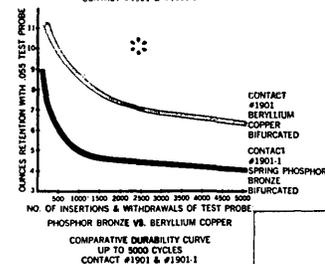
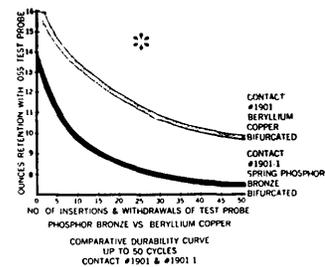
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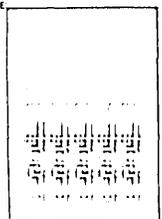
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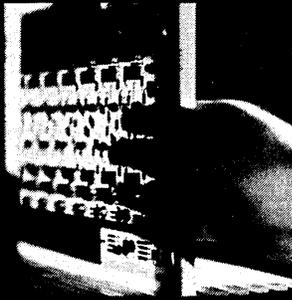
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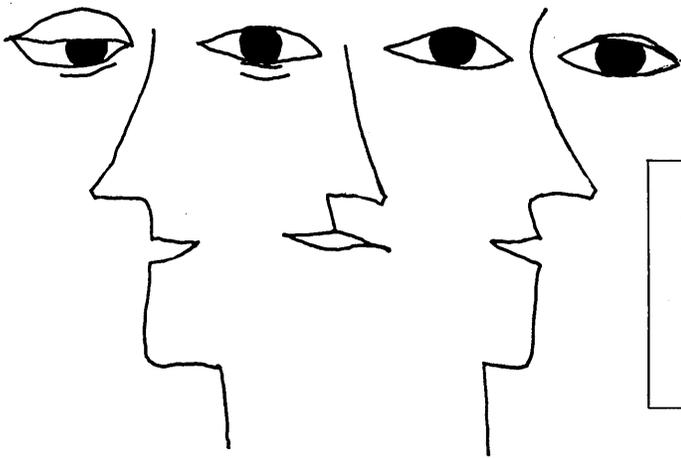
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Senior and junior engineers to perform and recommend circuit design and tests of high performance magnetic recording systems. Previous experience or familiarity with solid state circuits and system test would be helpful.

Logic Design Engineers

Duties involved cut across several technical disciplines and include creation of functional specifications of peripheral equipment controls and central processors; feasibility analysis for proposed systems; determination of the logical sequences of machine operations; determination of circuit and other hardware requirements; improvement of design processing methods and the supervision of prototype test efforts. 1-3 years' of related experience in digital systems planning and specifications.

Mechanical Engineers

To perform in the design, development and testing of small, precision electro-mechanical devices from bread-board model to finished product. If you have a background of 2-4 years' in product-oriented design with experience in one or more of the following areas — high speed mechanisms, linkages, position transducers or computer peripherals, this is an excellent opportunity to perform original and vital development.

Systems Analyst Marketing

This position requires a minimum of 2 years' EDP experience, preferably in computer sales, systems or systems implementation. Experience as a Marketing Analyst or Financial Analyst would be very appropriate.

Software Development

Current expansion plans have created openings at all levels of experience and background. These positions provide excellent personal and professional advancement opportunities within our Programming Systems Division.

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A knowledge of semi-conductor theory as applied to both semi-conductor properties and circuit design theory is necessary, so that devices can be adequately chosen and specified in conjunction with circuit design engineers. Experience in quality and reliability analysis of integrated circuits is desirable. Should be capable of conducting informal circuit design reviews with the responsible circuit design engineers to insure that reliability goals have been met. BS in Physics or EE with some experience in semi-conductor evaluation and applications.

Systems Engineers

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Electrical Engineers or Physicists

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Maintainability Engineer — Electro-Mechanical

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Programming Business Administrator

This position is a natural for an administrator with 1 to 3 years' experience in a design-oriented atmosphere. Ideally the CREATIVE administrator we seek should have a technical background and an MBA or studying toward an MBA. The equivalent in experience would be perfectly acceptable.

IEEE INTERVIEWS

Available with Mr. Curt Collison in New York City. During the show (March 18-21), Mr. Collison can be reached at (212) LT-1-3318. If you desire to set up an appointment at this time for the IEEE Show, please call Mr. Collison (collect) (617) 891-8400.

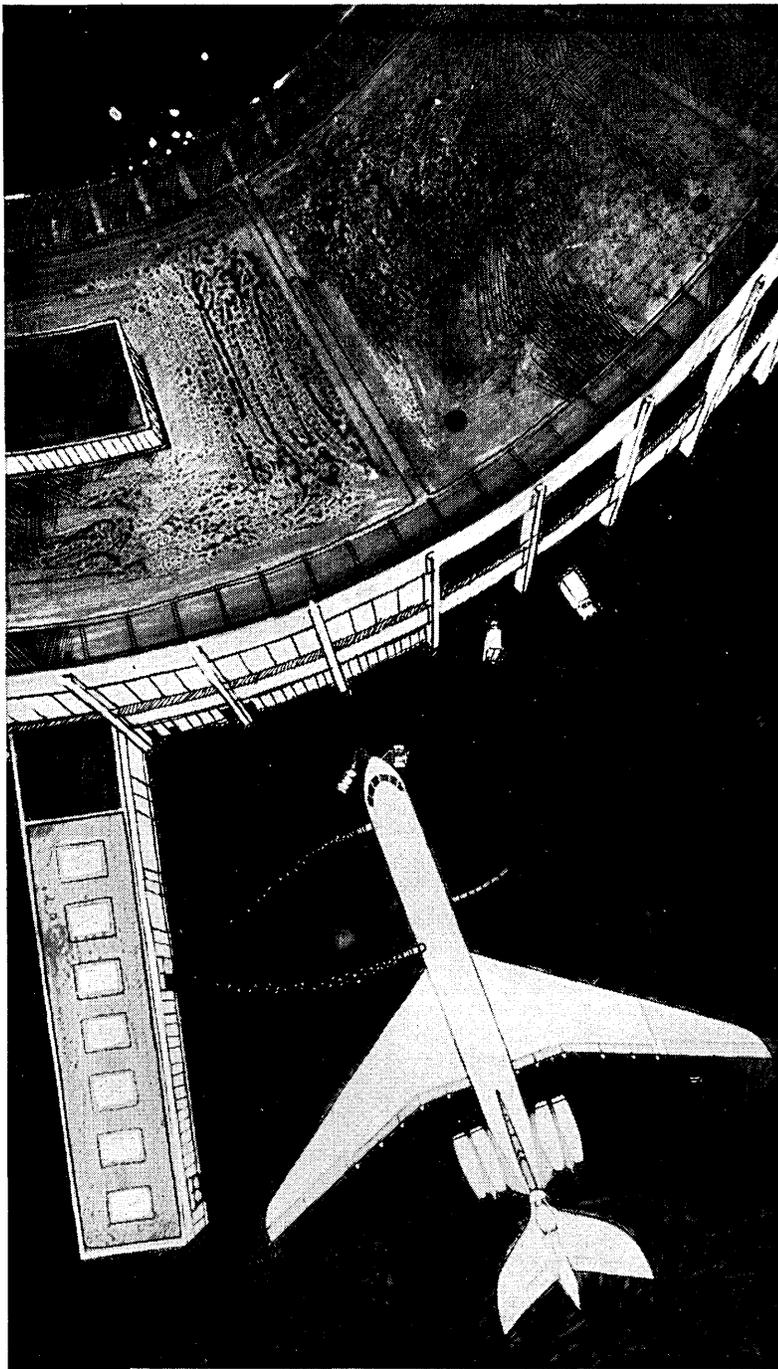
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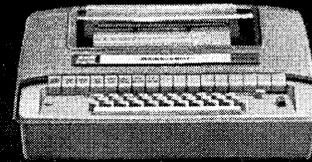
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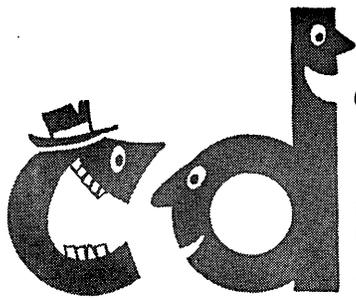
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commentary

Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of T. PAUL BOTHWELL, Contributing Editor.

A Case for Military Application of Commercial, General-Purpose Digital Computers

R. P. BERKOWITZ, Manager, Product Assurance Dept.
H. A. DELLICKER, Manager, Data Control Systems Section
Computer Control Div., Honeywell, Inc.

Military people have generally been excluded from the advantages of commercial, general-purpose digital computers. Commercial computers are low in cost, flexible, available, backed by full system support, and field proven. Military users' problems and applications have much in common with those of commercial users, but the former are restrained because they cannot supply stable, air-conditioned, vibration-free environment for the equipment.

In recognition of the variety and extremes of the military environment, specifications have been developed (MIL specs) to ensure a guaranteed base of performance in military applications. Computers designed to comply fully with these specifications are usually limited in their general capabilities and intended for one function only. And because few are built for any one application, their cost is high.

It is our contention that commercial computers, without any loss of their advantages, can be used in operational military applications through relatively minor mechanical modifications.

Certain Mil Specs Conformed to as a Matter of Course

In good commercial-computer companies, quality control practices conforming to MIL-Q-9858 are usually standard. Close attention is paid to certain military specifications, such as MIL-E-16400, for standard commercial parts procurement and manufacturing processes.

Modified or reconfigured to meet military specifications completely, a high-speed, general-purpose computer will perform the same functions as its commercial counterpart using existing documentation for spare provisioning maintenance, diagnostic routines, and other items of standard documents.

Modification Requirements

The primary purpose in reconfiguring the commercial machine is to have it function in extended operational

environments and to accomplish this with no effect on operational capabilities.

The wiring portion of the computer and the logic cards must remain the same, since they comprise the heart of the machine. Modifications in this area would cause expensive changes in manufacturing processes, software packages, and diagnostic routines.

The reconfigured version has to achieve as near a non-resonant system (below 500 cps) as practical to meet long-term vibration specifications. This has to be achieved while keeping maintenance a simple task, with full access through the front door. Also, each logic card must be removable within two minutes.

Electromagnetic interference suppression must be designed as an integral portion of this modification. Maintainability and full control-panel accessibility have to be possible while meeting the EMI specification MIL-STD-826A.

Typical Modification Techniques

Shown in Figure 1 is a tilt-out drawer in a typical commercial general-purpose computer. The drawer, redesigned to mil-spec shock and vibration requirements, incorporates the standard wired portion of the machine and the standard printed-circuit logic modules. Internal bracing is used to secure the logic cards.

Shown in Figure 2 are four cooling fans which operate in a push-pull fashion with each tilt-out drawer. The fan assemblies, designed to incorporate 50/60 or 400 Hz fans, do not provide any structural support other than to accommodate the fans, whose direction can be reversed to effect various cooling conditions.

The cabinet, a steel enclosure of welded construction providing structural support for the internal parts of the computer, also serves as a shielded enclosure and comes with wire-mesh gaskets (See Figure 2). The cabinet can have casters, leveling feet, lifting eyebolts, and the like, as required.

As a shielded enclosure, the cabinet meets the EMI requirements stated in MIL-STD-826A. A modified

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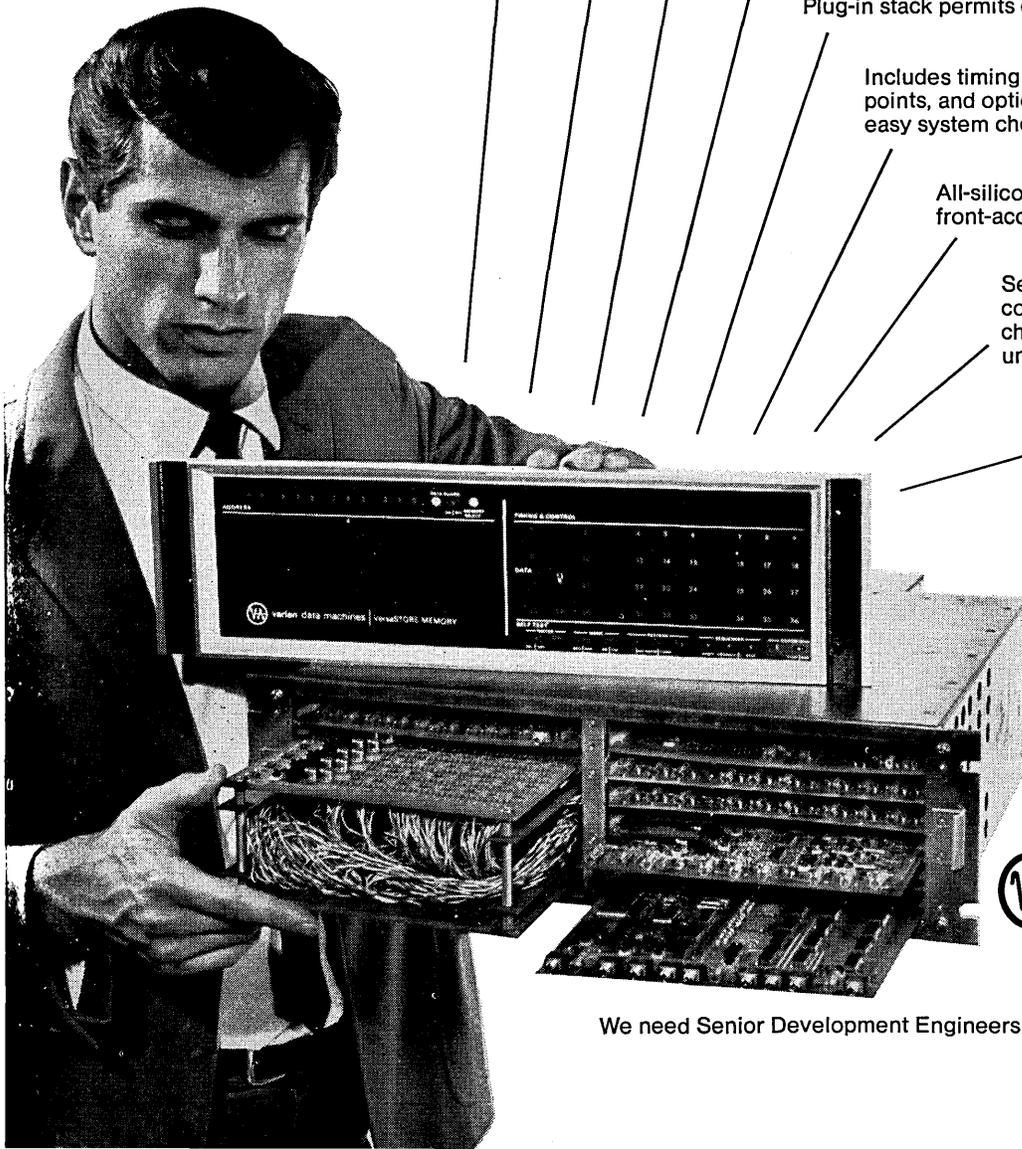
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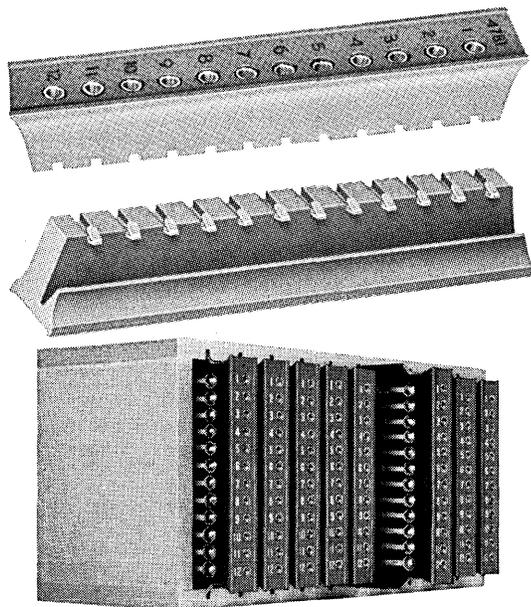
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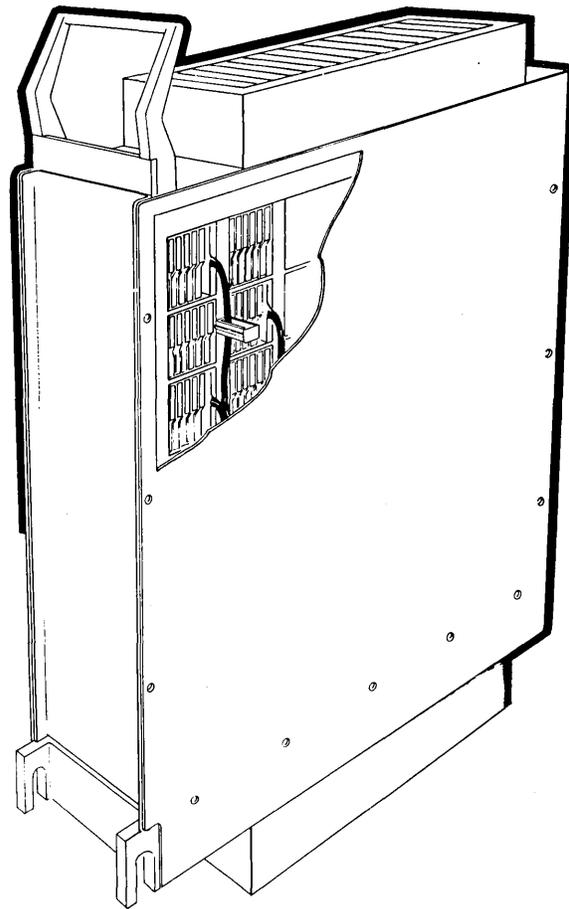


Fig. 1

control panel can be provided that is fully accessible and maintains full EMI suppression during all computer operational modes. Cabinet penetration can be accomplished with EMI connectors located on a connector panel (Figure 2), through which all input/output lines are routed. Power-line filters can be part of the connector-panel assembly or located elsewhere. Air intake and exhaust ports are shielded to allow adequate cooling while maintaining EMI integrity.

A blower system in the cabinet maintains an internal positive pressure. During maintenance, when the tilt-out drawers are extended, sufficient air is forced through the drawer assembly to maintain normal operating temperatures. An alarm circuit indicates the loss of critical cooling air.

Various Modified Computer Configurations and Applications

Commercial computers can be modified in many ways to meet a wide variety of military applications. These are some of them:

1. **Electromagnetic interference suppressed** — This configuration can be used for fixed ground installations where electro-magnetic interference suppression is required, but with a laboratory ambient environment. A standard computer is reconfigured to the extent necessary to achieve EMI suppression to MIL-STD-826A. Internal modifications include the shielded enclosure, control panel, grounding buses, and power-line filters.
2. **Ruggedized** — This configuration can be used for applications in aircraft, shipboard, and van-mounted installations. It includes an internal structure designed

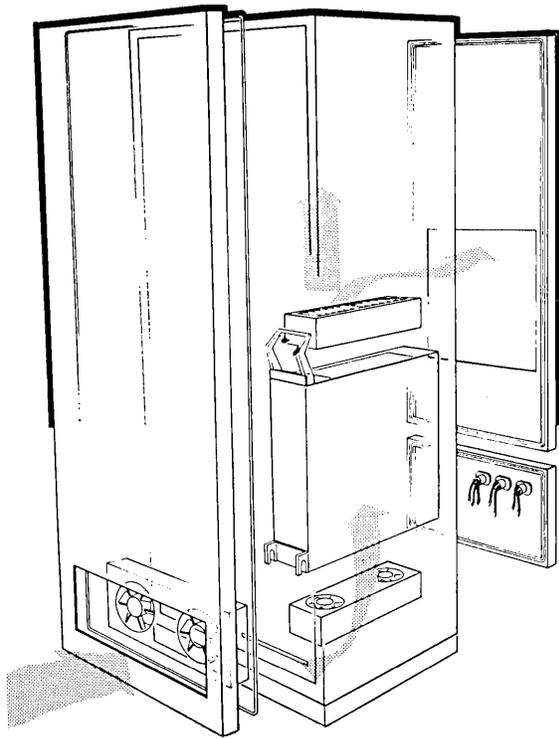


Fig. 2

to meet increased shock and vibration limits. Modifications are limited to the structural design.

3. **Ruggedized and EMI suppressed** — This configuration can be used for applications where shock, vibration, and EMI are part of the operating ambient environment. It encompasses configurations (1) and (2). Computer systems with these modifications can be packaged in either full-rack or half-rack cabinets.

Summary

The flexibility inherent in the real-time, high-speed digital computer allows trade-offs between input/output capability and computational requirements, between programming costs and hardware options. Memory size can be tailored to actual requirements.

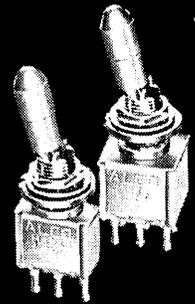
The modified computers retain all the capabilities of the commercial version — software, price, delivery, flexibility, and proven design — while meeting the operational requirements of the military user.

Other advantages are:

1. **Availability of optional features** — Present and future options can be incorporated. New government-sponsored development programs need not be undertaken.
2. **Faster familiarization** — The contracting agency can usually obtain a regular machine in advance of the modified one for systems-integration studies and familiarization.
3. **Service support** — The supplier's existing service organization can usually support the requirements of the user.
4. **Lower price** — The developments costs of the standard commercial computer have been amortized over the total number of computers manufactured for all uses. These savings are passed on to the military contracting agency.
5. **Spare parts** — The modified computers use the standard commercial logic modules and subassemblies.

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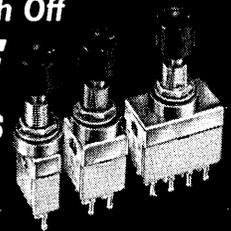
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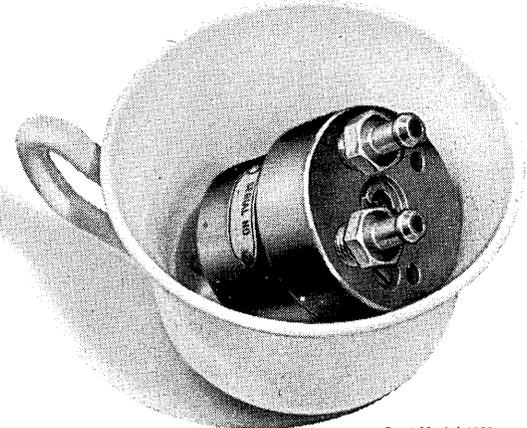


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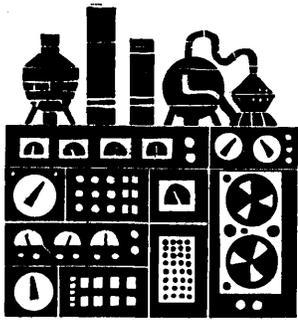
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INDUSTRY NEWS

AUTOMATED CARGO FACILITY — A new \$1.5 million automated cargo distribution center was opened this month in Atlanta by Eastern Airlines. Designed, engineered and installed by American Machine & Foundry Company (AMF), the high speed facility can handle more than 400,000 pounds of cargo a day, with a peak-hour capacity of 150,000 pounds. It can accommodate 20 simultaneous flight arrivals and departures, and automatically separate shipments for 18 primary destinations.

The entire 32,000 square foot cargo handling facility is controlled from a unique console computer/digital dial-a-system unit built by AMF specially for the Eastern facility. The console, manned by two men, controls and monitors all conveyor belts and the sortation system.

From the console position, the supervisor-operator can direct the entire cargo handling operation, including the retrieval of cargo in secondary lanes scheduled for later flights. This cargo can be directed to primary lanes for immediate shipment, to make-up tables for consolidation in pallet shipments, or through the sortation system for rescheduling.

In the second console position, a programmer using keyboard controls can instantaneously reprogram the system to meet increased and varied capacity and distribution needs. From the console's computer readout, he also obtains total shipment weights for transmittal to flight operations.

AUTOMATED STOCK QUOTATIONS — The Board of Governors of the National Association of Securities Dealers recently announced its approval of a com-

prehensive plan to develop an automated quotations system for the vast over-the-counter securities market.

Envisioned in the project is the use of electronic data processing equipment in combination with communications facilities to produce a three-level system responsive to 350,000 inquiries in any given eight-hour trading period and designed to aid both customers and professional traders in the OTC markets.

A Level I service, which is aimed at the requirements of registered representatives and securities customers of retail sales firms, will supply a current representative bid and asked quotation for any security registered in the system. This current representative bid and asked would be supplied initially through the more than 25,000 interrogation display units now in use by broker/dealers throughout the country. Additional display units would be supplied later to meet the growing needs of the industry.

VARIABLE COMMUNICATIONS SYSTEMS — RCA has announced receipt of a \$8 million U. S. Navy contract to develop a computer-controlled system that will enable shipboard communications to be reconfigured in minutes.

Called the Interior Communications System (ICS), the system will allow a ship's internal communications to be completely rearranged by simply changing computer programs instead of rewiring the system as is now necessary. ICS is being developed by RCA's Defense Communications System, Camden, N. J., for the Naval Ship System Command.

Heart of the system will be

RCA's CSP-III communications processor. The computer will be used to perform circuit switching functions now performed by discrete hardware components.

LSI ARRAYS — Several large scale integrated circuits were described to the International Solid State Circuits Conference this month by Dr. Clare G. Thornton, director of research and development for Philco-Ford Corporation's Microelectronics Division in Blue Bell, Pa.

The LSI arrays include a 1024-bit read-only memory (ROM) containing 1,250 transistors on a 70 x 100 mil chip and a 16 x 16 random axis serial memory containing 1,400 transistors on a 100 x 120 mil chip, plus an experimental 2048-bit memory (presently under development) containing 12,000 transistors on a 117 x 117 mil chip designed to operate at speeds in excess of 5 MHz — all in MOS; and a dual-function bipolar complex array containing 400 components on a 110 x 88 mil chip and designed to operate either as a four-stage binary counter (divide by 16) or as a BCD counter (divide by 10) by changing the logic level of a control input.

Dr. Thornton also described methods whereby LSI circuits can be assembled by the silicon wafer-chip technique to produce monolithic subsystems containing as many as 120,000 transistors as a single system. This technique bonds individual LSI chips face down onto a silicon wafer containing a high density of interconnections which are produced by the same basic process as that used on the silicon chips.

In the wafer-chip assembly, Dr. Thornton said, level of complexity and cost per functional element are determined directly by the achievable component density on a given chip. He said key technological determinants for increasing this density include smaller geometry, multi-layer metalization, thin epi layers and shallow diffusions, choice of circuit form, pad locations, and operating voltage.

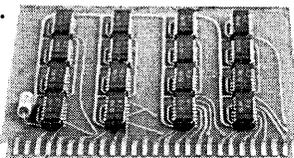


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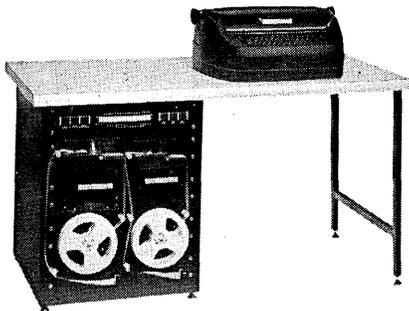
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"In order to determine the expected level of improvement more precisely," Dr. Thornton said, "specific LSI circuits have been subjected to progressive design analysis incorporating what are considered to be a modest level of first, second, and third generation improvements, as related to the indicated determinants.

"Second generation technology, which requires no further technological advances beyond those already demonstrated, permits 1250-2500 bits of serial shift register per ship, or 500-1000 gates per chip (general logic). Third generation technology, represents a reasonable extrapolation into the early 70's and will allow more than 5000 bits and 2000 gates respectively.

"In each case new design rules have evolved incorporating the expected improvements, and a sufficient portion of the circuit and system topology drawn and, where necessary, fabricated, to measure the allowable complexity improvement."

Dr. Thornton reported results of the analysis derived from MOS circuit layouts, both for shift registers (best case) and arithmetic units (worst case).

Using this analysis to predict improvement in component density, he said an increase of X8 for bipolar and X16 for MOS are virtually certain.

SALES OF MEDIUM-SCALE COMPUTERS TO SLACKEN; INCREASED SHIPMENTS OF REMOTE TERMINALS SEEN —

"During the next five years, there will be a significant shift in the distribution of computers by size. Medium-scale machines — those with monthly rentals in the \$5,000 to \$20,000 range — will decrease from the present 51% of the total value of computers installed to just under 28% in 1972. The distribution of large computers, during the same period, will increase from 32% in 1967 to over 48% in 1972." These estimates, which reflect the increasing use of small computers and the growing trend toward terminals on-line with giant computers, were given during a

one-day briefing session for investment analysts conducted by *EDP Industry Report*, the semi-monthly newsletter published by the International Data Corporation for executives concerned with the electronic data processing industry.

Throughout the meeting, a phenomenon termed the "IBM ripple effect" was pointed out by IDC speakers. "What IBM does — or, significantly, what it chooses not to do — is one of the most important criteria upon which other companies base their marketing strategy," notes Patrick J. McGovern, president of IDC. "This is true not only in the case of main-frame manufacturers," McGovern points out, "but also in the case of peripheral equipment manufacturers, software houses, leasing companies, and service bureaus."

The primary reason for this, the investment analysts were told, is the simple fact that IBM computers account for over 73% of the monthly rental value of all installed computers made by American manufacturers. And the situation is not likely to change, since IBM has almost 76% of all computer orders now on manufacturers' books.

Growing Software Market

In an examination of software suppliers, IDC Vice President John P. Breyer pointed out that the market for independent companies has been relatively small, representing only \$180 million of an estimated \$5 billion spent on software during 1967. The market for independent software suppliers, however, is estimated to grow to about \$1 billion out of the \$11 billion that will be spent on software by the year 1972. The independents are expected to be strongest in supplying proprietary packages and specialized applications software.

Breyer noted that most successful software firms fall into two distinct categories: Those with less than 100 employees and those with more than 1000 employees. As companies grow, he explained, there is a loss of management contact with the technical employees, and fragmentation

is likely. This is particularly true because low capital requirements make it relatively easy for personnel to spin off and develop a new software company. Companies which reach a large size usually do so through acquisitions, and are quite widely diversified into such activities as service bureaus and/or education services.

One big trend pointed out in the briefing session is that toward a rapidly expanding market for the independent peripheral manufacturer, especially for on-line terminal equipment. Remote terminals accounted for about 6% of the value of computer equipment shipped in 1967, or approximately \$350 million. By 1972, when computer equipment shipments are expected to increase from 1967's \$5.9 billion to over \$11 billion, the value of remote terminal shipments is expected to increase to 15%, or about \$1.75 billion.

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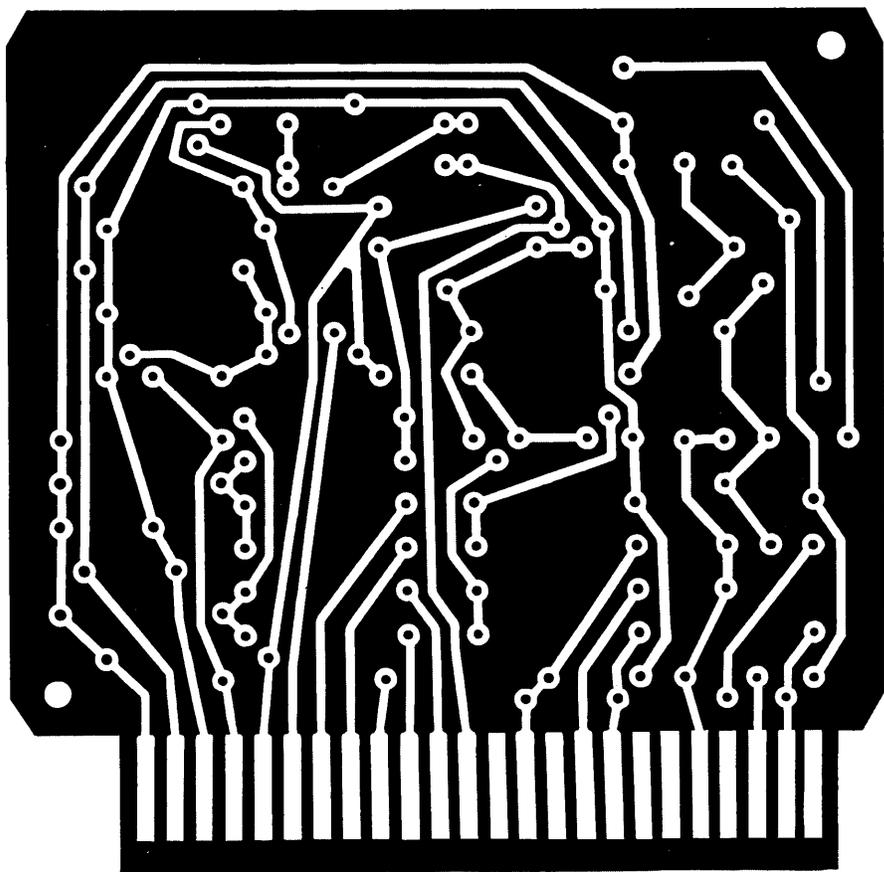
“DID HOMER WRITE BOTH THE ILIAD AND THE ODYSSEY?” — This question long has been a source of debate among classicists and philologists. However, they may be closer to agreement. Tufts University Prof. Frank P. Jones has subjected the masterpieces to the critical scrutiny of an IBM 1130 and concluded that Homer was the single author.

Jones, a professor of classics and a psychological researcher at Tufts, has spent the past two years studying the distribution of metrical patterns (hexameter patterns) in Homer's famous works.

Employing the computer to do the hackwork of counting, arranging, indexing, and composing, he arrived at a conclusion that will endear him to allunitarians, those scholars who attribute both epics to the 850-B.C. poet.

His findings were presented at the recent annual meeting of the American Philological Association in Boston. A session on Computer-Oriented Classicists gave an official blessing to the value of Jones' computer approach.

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Logic modules are built on printed circuit cards. Hole location and front-to-back registration must be very accurate for machine assembly. **Hand assembly is costly.** Plated thru-holes must provide positive continuity. **Rejects are costly.** Circuit boards for logic modules must be easily solderable. **Poor solderability is costly.** Printed circuit cards must be delivered in volume quantity for large-scale logic module production. **Time delays are costly.**

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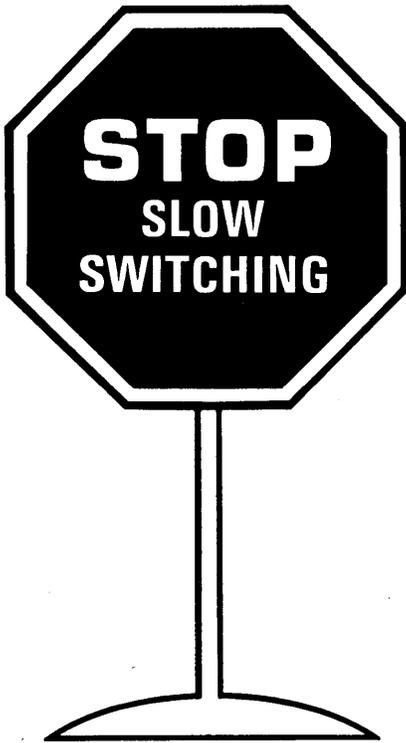
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"The computer," explains Jones, "allowed us to study the poems' whole form, whereas before, by hand, we could take only samples of the form."

Some scholars contend that the *Iliad* and *Odyssey* were written by minstrels over the course of centuries. But now data seems unmistakably to identify Homer's style in all of the 32 metrical patterns of both poems that were studied at Tufts.

It should be added that computers are not new to classic literature. But Jones, in reanalyzing the dactylic hexameter of the Homeric poems, is the first to publish his conclusions.

GOVERNMENT SPECIFICATIONS RETREVAL SYSTEM—Specification Technology, Inc. has developed a unique new computer service which automates the research and processing of government contract specifications.

Central to the system will be a National Cash Register 315 RMC (Rod Memory Computer) scheduled for delivery in March.

The new service, developed after eight years of research and development by STI, represents a breakthrough in the solving of a formidable problem facing both defense contractors and government agencies for several decades.

This is the need for rapid and accurate analysis of a contract's requirements, imposed by the chain of referenced military specifications and standards (normally called a "specification tree").

Now, with the new computer service, specification research which previously took from 3 weeks to 6 months of tedious effort can be accomplished in hours.

The heart of the system is a huge specification library which in turn has been programmed into the NCR computer. The entire library is filed by means of NCR's unique CRAM (Card Random Access Memory) units. Utilizing a sophisticated program, STI's new service has the capability of very rapid retrieval of all specifications forming the contractual

obligation of any contract, bid or proposal.

When the government agency issues an RFQ — Request for Proposal — to a supplier, it submits up to 200 major categories of specifications for the product design. But these key categories are further broken down into "tiers" of requirements, so that perhaps as many as 30,000 demands can be involved. When a main category of specifications is coded into the system, the NCR computer will automatically search out all pertinent sub-tiers and deliver a print-out showing specification numbers, dates of issuance, and 72-character descriptions of what is stipulated by the specification.

Of equal importance, the system provides a service which will show all changes in specifications during the life of the contract. Up to 2,000 changes a month in government specifications will be kept up-to-date in the CRAM magnetic file system. Thus, a company will be able to keep constantly abreast of specification changes and know precisely where it stands as to its contract commitment.

STI says that the significance of this new development to defense contractors is that, for the first time, they will have immediately available a complete specification package for ready analysis. This means prompt response to government bids can be made with assured accuracy and virtual elimination of the risk factor inherent in past methods of operation.

NEW EDP SYSTEM — Announcing the B500 electronic data processing system as another member of Burroughs 500 System family, President Ray W. Macdonald said the new system "will provide a much higher level of data processing capability at lower cost for a very wide segment of the business, governmental and financial communities."

The system is available in several configurations, including orientation to on-line data communications, random access disk file and magnetic tape processing, and multiprocessing. It can

handle on-line communications and off-line production work at the same time.

A special, compact disk file system memory acts as a high speed extension of the B500's main memory, and contains combinations of software elements used by the computer, such as the operating system, the user's program library and the COBOL compiler.

The systems memory has a capacity of 2.4 million characters of data stored in 240-character segments. Any of the 10,000 segments of data can be accessed in an average of 23 milliseconds, and be transferred to and from core memory at a rate of 100,000 characters-per-second.

Thus, software elements are used in the faster main memory only as they are needed, and the 9,600 or 19,200 positions of computer main memory are kept free for processing of data.

Deliveries of the B500 will begin in the fourth quarter of 1968.

DDP-324 COMPUTER — Honeywell's Computer Control Division has introduced a general purpose dual processor computer which it says will perform more than 500,000 operations a second.

The company announced that three of the new integrated circuit computers have been ordered by Conductron-Missouri, a division of Conductron Corp., for use in trainers simulating the Boeing 747 superjet. The St. Charles, Mo., company is building the simulators for Boeing, Pan American World Airways.

Designed for use in simulator, process control and communications systems and for scientific applications where large amounts of on-line reduction are performed, the new DDP-324 computer is said to be priced 16 per cent below comparable machines and its speed is said to be 60 per cent faster. Honeywell estimates the computer segment of the complex simulator systems market, currently valued at \$200 million to be about 10 per cent, the total market is expected to reach \$300 million by 1971 when more than 20,000 new pilots will be needed to meet civilian and military requirements.



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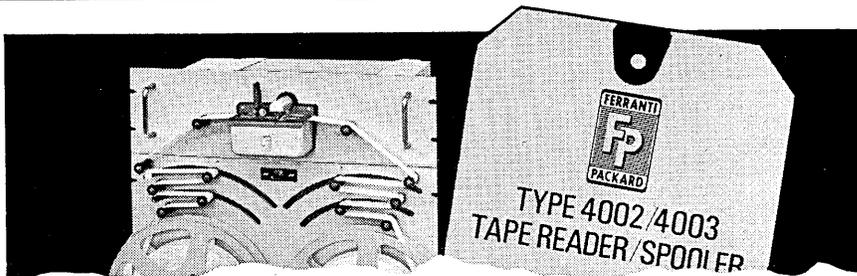
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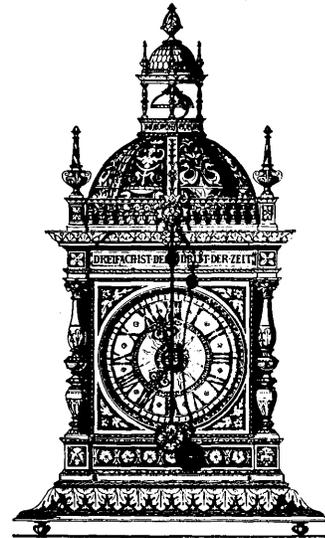
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CIRCLE NO. 38 ON INQUIRY CARD

Fundamentals of Time Shared Computers

by C. Gordon Bell

Associate Professor of Computer Science and
Electrical Engineering, Carnegie Institute of Technology.
Formerly manager of Computer Design, Digital Equipment
Corporation, Maynard, Massachusetts.



“Time-sharing” is discussed generally in this article to cover any application of a computer system that has simultaneous users. The discussion defines general purpose time-sharing so as to include special purpose time-sharing, “real time”, and “on line” systems as a subset. “Graceful Creation”, or the “boot strapping” of a system, is described in which newly created individual user procedures are immediately available to the whole community of users, and the system expands in an open-ended fashion because many users contribute to the formation.

Although the discussion is separated into hardware, operating system software, and user components, a sharp delineation does not exist in reality.

After the basic system is specified, it is the philosophy of the author that the system should be formed in a time-shared environment (including the construction of the operating system software). Few restrictive features or functions should be “built-in”, but instead, be optionally available through the library or common files.

The underlying design criteria should be: flexibility, modularity, simplicity of module intercommunication, and open endedness.

The basic objectives of time-sharing are to increase user and/or overall computer system productivity. Present general computational systems are an extension of special, shared, multiprogrammed systems centered around special applications (e.g., process control, command and control, information inquiry, etc.). As such, time sharing is another technique that makes the computer a more general tool.

All future computers will have at least some basic hardware for a form of time-shared usage. These systems forms will run the gamut from dedicated systems with a permanent user, through general systems with varying number of users, to a network of shared computers.

The article discusses only the basic structure of the system, with emphasis on the hardware, because of space limitations. For example, the issue of scheduling jobs is discussed only superficially by listing the system variables on which scheduling depends, together with a common scheduling algorithm.

TABLE 1. CAPACITY REQUIREMENTS FOR TIME-SHARING SYSTEM APPLICATIONS

Specialized System Service, or Application	Primary Memory for Process (in bits)	Primary Memory for User Data (in bits)	Processing Capacity/ User (in operations*/ interaction†)	File Organization and Size (10 ² -10 ⁹ bits)	Direct Terminals
Desk calculator	very small	very small (<10 ³)	very small (>10 ⁴)	none	typewriter, input keyboard, strip printer, scopes, audio output, or special console.
Stock quotation	small	small (<10 ⁴)	very small (>10 ⁴)	one (small-medium)	see above, stock ticker tape or transactions input, telephone.
Airline reservations	medium	small (>10 ⁴)	small (>10 ⁵)	approx. 6 (medium-large)	special consoles, typewriters, scopes.
On line banking	medium	small (>10 ⁴)	small (>10 ⁵)	approx. 10 (medium-large)	see above, special bank teller consoles.
General conversational computational languages (JOSS, CULLER-FRIED System)	medium	small-very large (10 ³ -10 ⁵)	small-large unbounded (10 ⁴ ->10 ⁵)	multiple files per user, with few file types (medium-large)	typewriter, printer, scope, plotter. (Culler-Fried consists of scope, keyboard, and tablet.)
Specialized computer aided design, engineering, problem solving languages (COGO, etc.)	medium-large	small-very large (10 ³ -10 ⁶)	small-very large (10 ⁴ ->10 ⁶)	see above	see above
Process control	medium-large	medium (>10 ⁵)	small-very large (10 ⁴ ->10 ⁶)	few (small)	physical quantity transducers, general user terminals.
Text editing (Administrative Terminal Service)	medium	small (>10 ⁴)	small (10 ⁴ -10 ⁵)	multiple single purpose files/user. (medium)	typewriter, printer, scope.
On line information retrieval of periodical headings, bibliographies, keywords, abstracts	medium-large	medium (>10 ⁵)	medium (10 ⁵ -10 ⁷)	one (very large)	see above. telephone (dial in, audio out)

*assumes a fairly sophisticated processor and instruction set
 †maximum interaction intervals for user requests are ≈ 10 sec.

File independence, for example, is controlled by associating information with the file concerning the file's users, and uses to which the file may be put. Such file directory data provides system capability to cover a wide range of applications concerning private and public data bases. In fact, systems could be categorized by the organization of their data bases. Table 1 presents some special purpose systems which are ordered approximately in terms of the filing demands. For example, a file containing a teaching program may be universally available, while a program for monitoring the teaching program or for grading the users may not.

Process or program independence (and dependence) is the most expensive hardware aspect of user independence. One program cannot affect nor destroy another; on the other hand, a mechanism for making procedures available to the community's members is necessary.

Instantaneous Criteria

The instantaneous nature of a time-sharing system includes both direct terminals for the users and rapid response to user demands. That is, users are "on line" and served in "real time". An *on line* computer is one which provides terminals which allow users to directly communicate with it by a single, simple action, (e.g., like pressing a typewriter key or looking at a display). The system is never farther away than the nearest terminal. A *conversational program* is an on line program which allows a user to directly communicate or "converse" with it in terms of requests and acknowledgement dialogues at an appropriately rapid rate.

A *real time* system is one which has the ability to execute a required process or program in an "acceptable" period of time as governed by the extra computer process requesting computation power. All systems are real time if they are acceptably fast: e.g., overnight for payroll cal-

ulation might be acceptable!

Normally, we associate "real time" with a mechanical process in which a computer is constrained by a mechanism, e.g., a "real time" computer for air traffic control must be able to process all the inputs from the radar system such that aircraft positional information is not lost.

The *response time* or total time for the system to respond to a demand stimulus is the sum of the *reaction time* (the time until a program is activated from the request time) plus the *processing time* (the time to process the request).

Response times for human users should vary in accordance with their requested demands. The response time for a computational demand, although known and determined by the system, can only be judged for acceptability by its users. In summary, "real time" for a mechanical process means keeping up with the process (not losing information, etc.). "Real time" for a human process is giving an appropriate response in accordance with requests.

Shared Criteria

The sharing of a system by multiple users represents an economic justification by ordering or optimizing random resource requests. The *allocation of resources* is a major system function and includes: processor *scheduling*, or the allocation of processing capacity for process or program execution; *file allocation* provides for the user assigned space from the available file space; *primary or memory allocation* is the allotment of memory space for the execution of processes; and *terminal allocation* or the assignment of terminals to users.

General Purpose Time-Sharing Criteria

All of the above criteria must be met for a time-sharing system. In addition, one other criteria, generality, or open endedness, separates special purpose and general purpose systems. A general purpose time-sharing system must provide for the open-ended creation of new processes or procedures during system operation time, which in themselves may be considered part of the "system." This ability, or *graceful creation* of an improved or ever-expanding system with increasing abilities defines an open-ended general system. In the limit, users concerned with the development of the operating system software may, for example, operate and test a complete, new time-sharing system program to replace the existing system within the framework of the old system. As new processes, languages, procedures, etc., are added to the operating system software or placed in the general user's public domain, the line delineating the operating system process and the user process becomes less sharp.

The method (or language) of procedure creation, testing, and execution is the measure of generality. In summary, a simple test for generality can be made by determining whether a new language can be added to the system from a normal terminal or console. The user should have freedom inherent in the hardware (or at least in the processor), including the ability to write programs in machine language.

SPECIAL PURPOSE AND GENERAL PURPOSE TIME-SHARING

In most new systems, basic time sharing hardware can be easily provided in the design at low cost. The general organization of all computers provides the inherent ability to form a time-sharing system. Indeed, time-sharing systems have been implemented on machines covering a wide range of problem applications. In general, the systems formed, using computers which have little or no supplementary hardware, are restricted to a single application. The ease with which a total system may be implemented on a configuration is determined for the most part by the configuration and the inherent hardware facilities that aid the configuration sharing. The features which assist resource allocation must be included for implementing general purpose systems. The hardware can limit the general purposeness in a fashion similar to the operating system software. The additional hardware to provide some form of resource sharing can be quite small.

Although the ability to implement a general purpose system on a specific hardware configuration may be a desirable design criteria for the hardware, a special purpose or dedicated system may be more desirable. A configuration dedicated to a particular use may be designed to provide a much more efficient utilization of the resources than one which attempts to serve all users solving all problems.

It may be more advantageous to form communities of users who share the same system and are only interested in solving specific classes of problems on single systems. Systems which already are limited by a single resource might stand alone. For example, present hardware file capacity and file access capabilities appear to limit desired library systems. (Thus, a general system cannot supply the necessary resources, nor can the resources be supplied even if a dedicated system were built.) Table 1 gives a list of dedicated computer applications.

A network of dedicated computers

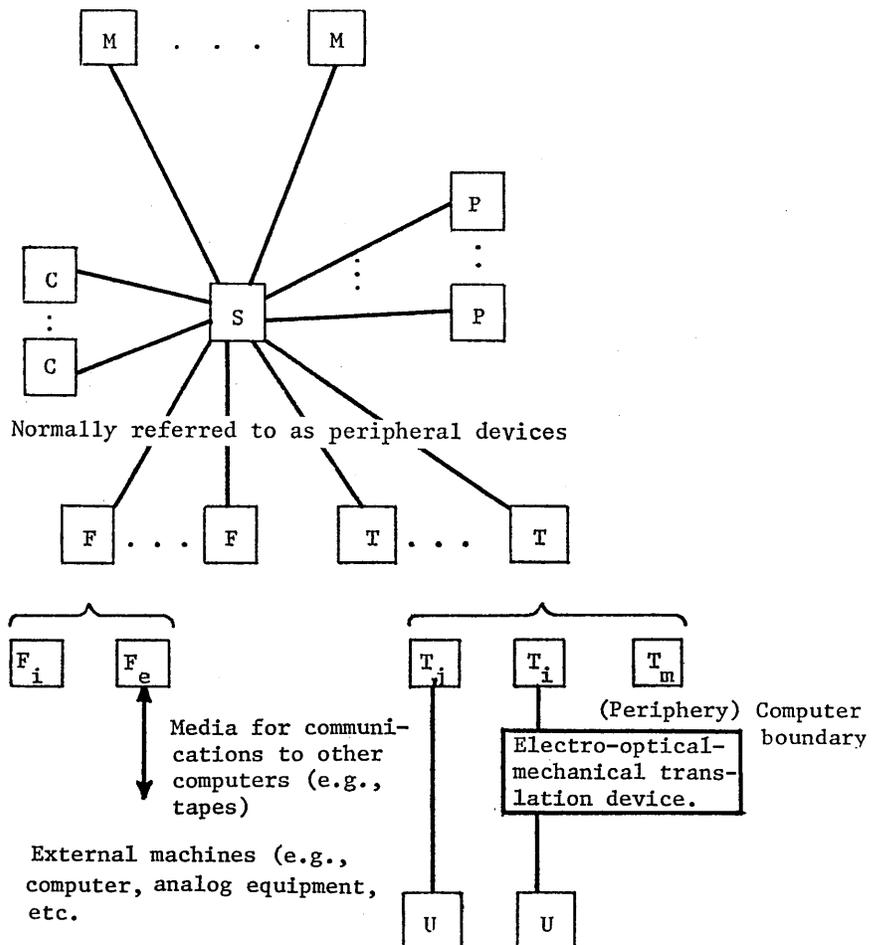
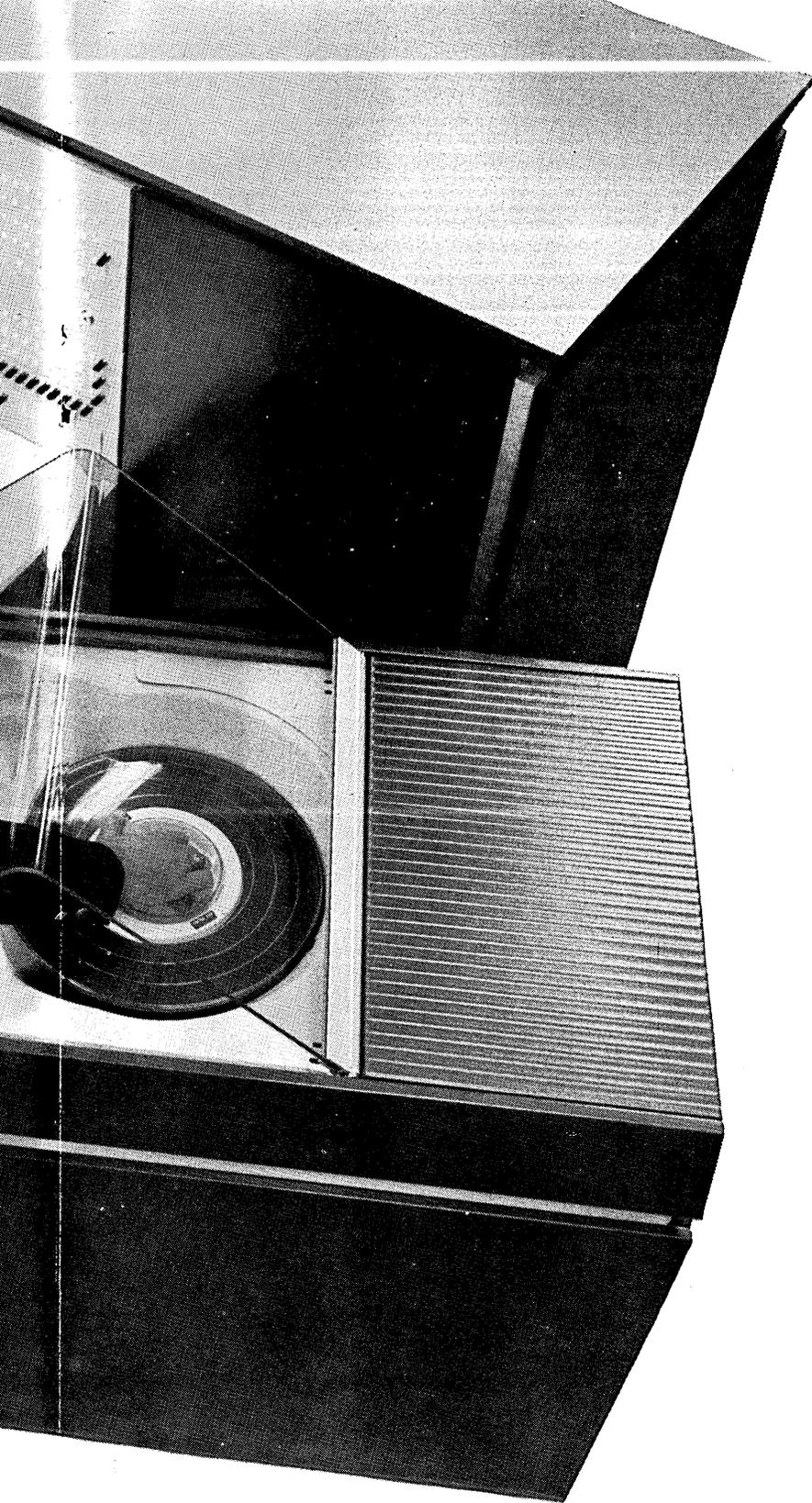


Fig. 3. General structure of present computers in terms of computer components.





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which only solve specific problems, supply special resources, or "understand" specific languages may be a better solution to efficient usage of our machines than the large, general purpose systems which try to provide any or all services.

HARDWARE

COMPUTER STRUCTURE

Although hardware can be considered at various description levels from memories or processors down through "AND" gates, on to circuits, the level of interest for this discussion is the computer and its components. The general structure of the computer is shown in Figure 3. The computer's components are: primary memories, processors, controls, peripherals (terminals and memory files), and switches. The communication between any pair of components is via switches which provide both "data and control" information paths.

A single *computer* has any number of components (memories, processors, controls, peripherals) but every processor in the computer must access some of the common primary memory of the system.

A *multi-processor* computer has more than one processor. Multi-processing is the simultaneous processing of one or more computational programs or processes by multiple processors. Multi-processing methods can vary from non-anonymous job assignment, in which particular processors or types of processors are assigned to specific roles, to anonymous processors being assigned to any job in the system.

It is difficult to have complete anonymity because particular processors in the system can only handle a limited class of jobs (especially Input/Output Processors).

A *parallel processor* computer has multiple, anonymous processors, each of which can be assigned to different, independent, parallel (processed simultaneously) parts of a single task.

All computer structures are special cases of that shown in Figure 3. Most systems have hierarchial or tree-like structures like that of Figure 4. Each switch is, in fact, more closely associated with a particular

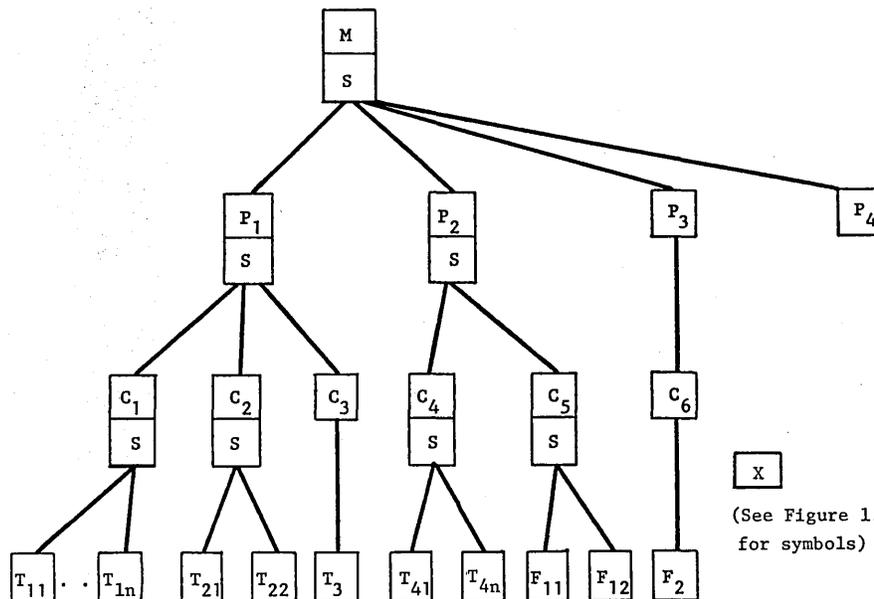


Fig. 4. Structure of a simplex computer system.

component, and takes on the special properties necessary for switching or selection among particular components. Thus, a particular tape control unit may communicate with up to eight tape units and the particular kind of information exchanged between the two units is a function of the kind of units. The tree-like structure exists not only because of the number and type of units and

the way they inter-communicate, but also because the computer is a simplex structure. That is, assuming that it is necessary for communication to be carried out from bottom to top (a terminal or file to primary memory), there is only one path for the communication flow. Figure 5 presents the structural forms the switches take.

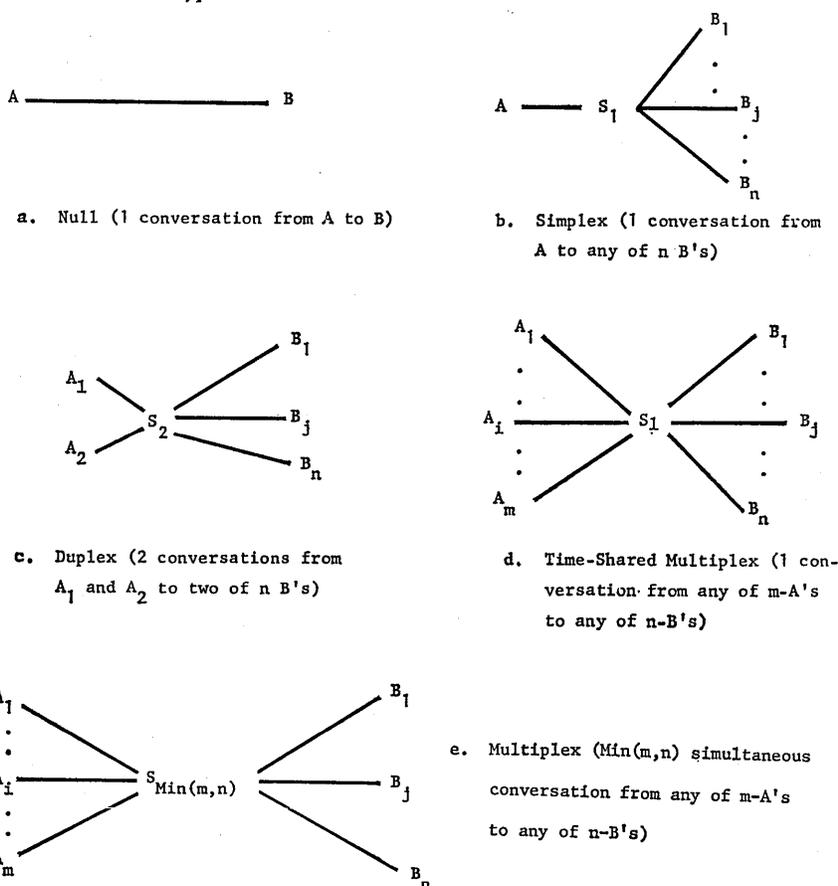


Fig. 5. Computer component switch or selection configurations.

Figure 6 gives a computer with multiple paths between a primary memory module and a given peripheral element. Since there is some redundancy among components, it can be shown that there is a higher probability that the computer will be in an operational state, as measured by some large fraction of memories, processors, terminals, and files being operational. Such an operational state would undoubtedly be at reduced performance. The probability of a system being operational is a function of the computer structure (the number of components and their interconnection) and each component's probability of failure.

For systems requiring a large fraction of availability or a high uptime, it is necessary to at least duplicate each component of the system. Such systems can be designed so that all units are constantly in service (including the duplicates), and when a system failure occurs, the faulty unit is removed or the system re-partitioned for maintenance. Such a design philosophy, called *graceful degradation* or *fail soft*, provides continuous usage even though the capacity may be degraded. Fail soft design imposes the constraint on the hardware that there be a duplicate of each unit and communication path in the system. It is possible to have similar functional duplicates to avoid complete duplication, i.e., a drum can be replaced by a disk. In such cases, the system will continue to function, but at very much reduced capacity. These computers also must have ability to detect first fault occurrence at a computer component so that errors will not propagate through the entire system, making fault location difficult. Once a faulty unit is detected, the system must be able to be dynamically reconfigured.

Multiple units can also provide a means of achieving better overall system performance since the units can be used for operation while they are standing-by.

PRIMARY MEMORY COMPONENT

The *primary memories* (usually core or thin films) retain the active portions of both user and operating system processes. These processes are either being enacted by a processor or are waiting for a processor. The

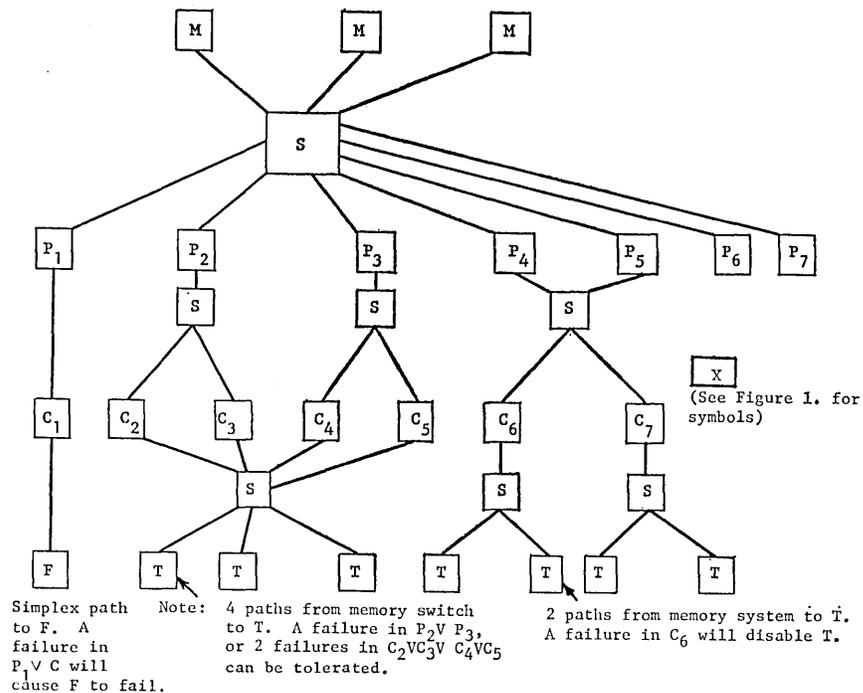


Fig. 6. Hardware structure of multiplexed computer.

primary memory may also contain memory maps and status information regarding the system's users.

The primary memory is the medium of logical intercommunication between the hardware and software components.

The arrangement of the memory subsystem, as shown in Figures 4 and 6, is such that from the processor's viewpoint, a number of *access points*, or *ports*, are provided with which the processors connect. The physical form that a memory subsystem (the memories and the switch to which the processors connect) takes is described by:

1. The number of independent memory modules.
2. The properties of each memory module.
 - The data width (in bits) of information accessed at one time.
 - The quantity of information stored (in bits).
 - The *access time* — the time the module requires to obtain data, given that the module is free, from the time an access request has been made.
 - The *cycle time* — the time the module requires to completely acknowledge a request, and become free for the next request.
 - Memory failure probability (detected failures and undetected failures).
3. The method used to assign physical addresses (which the processor

uses) to physical memory modules and memory words.

4. The switching network which connects with the processors. See Figure 5 for possible switches. These range from 1,2,P (where P is the number of processors), to M (or the number of memory modules) as possible simultaneous conversation among processors and memories.

All primary memories are functionally similar because they store programs while they are being interpreted by a processor; data for programs; and other state information required by the processors. The memories can be separated according to their specific functions on the basis of their cost, size, and speed.

Principal Primary Memory (Core or Thin Film Technology)

This memory is the principal storage for programs while they are run. In most computers, the assumption is made to provide a certain match between processor capacity (in bits/sec.) and the available primary memory cycles (in bits/sec.). In small computers this is the only Primary Memory in the computer.

Bulk Memory or Large Capacity Storage

These memories have the following characteristics relative to primary memory: — cheaper (\$.02-.04/bit versus \$.10-.20/bit); larger

(0.5-1) million words versus 32,000-256,000 words; and slower (8 $\mu\text{sec}/\text{word}$ versus .8 $\mu\text{sec}/\text{word}$).

The assumptions about use are:

1. Problems involving large data structures in which data is randomly accessed.
2. As program base for seldom executed user and system programs.
3. As data base for seldom accessed data. (Whether a program is moved from bulk memory to principal memory is a function of movement overhead, and the expected activity.)

A bulk memory is also often used as a secondary storage device to hold programs and data (types 2 and 3 above) which are transferred to primary memory (higher speed) for execution. Thus, it is treated essentially as a fast, zero access, drum-like device for program swapping.

Scratch-Pad Memories

These memories have the following characteristics relative to primary memory — faster (by a factor of 5); more expensive (by a factor of 10-100); and smaller (20-1000 words). Such memories contain:

1. Short loops for high-speed program execution
2. Control information which may be referenced by I/O processors
3. Either the processor state or copies of the processor state (arithmetic, index registers, status information, etc.).

PROCESSORS

Processors connect with primary memory and enact user computational (arithmetic, symbolic, logical, etc.) processes. Large systems require several types of processors to efficiently handle the different tasks, to provide redundancy, and to match the capacity of the memory system.

Processors can be specified at the computer system level by the following parameters:

1. Instruction set ability
 - Distribution of processing time required for the given algorithm being processed.
 - Distribution of memory space for the algorithm.
2. The number of programs which are recognized as independent processes. (This number is roughly

equivalent to the number of interruptor trap channels.)

3. *Program switching time* or the time to save a process state, and to reset a processor to a new process state.

4. The number of bits (or words) associated with a process which resides in the processor and must be swapped when a new process is selected.

Computation Processors, Central Processing Units, Arithmetic Processors, or General Purpose Processors

These interpret memory-provided processes, and most generally perform arithmetic, symbolic, and logical functions. This conventional processor handles user and operating system processes. In small systems, it is the only processor, and as such interprets input-output commands for peripheral devices.

Special Purpose Processors or Algorithm Processors

These (arithmetic/logical) processors interpret a limited command set for special languages or algorithms and augment a general purpose processor. This type of processor has so far only been used experimentally (e.g., to process IPL V statements or evaluate polynomials). Future possibilities include the use of special processors for cross/auto correlation, fast Fourier series transformation, Matrix Multiplication, etc., algorithms (e.g., IBM 360/2938 Array Processor).

Peripheral Processors, Input-Output Processor, Input-Output Control Units, or Data Channels or Channels

These interpret a limited set of commands or instructions which handle controlling the transmission of data between peripheral control unit peripherals and primary memory.

Peripheral processor programs exist in primary memory, and are usually created by arithmetic processors. Though they do not usually have the arithmetic, logical or symbolic, capability, they do possess enough logic to do algorithm decoding. When necessary, arithmetic processors augment the peripheral processors.

The instructions interpreted by peripheral processors include:

1. Terminal initialization commands.
 - Selection of data transmission path by selecting both the control unit and peripheral device.

- Device function specification commands. These include commands for — reading, writing, unit speed, and directions selection, data transmission formats, etc.

- Location of information within the peripheral. If the device is organized in such a fashion to regard its data as being addressable or accessible by a number, the location must be specified.

2. Peripheral status query commands. At various times, the processor queries the state of the control unit-peripheral device and places the status in primary memory.

3. Peripheral program execution (in addition to initialization and status query commands). These instructions include:

- Branching.
- Setting up of commands for block data transmission.

- Intercommunication with other processors, by issuing commands to the processors. Also, a peripheral processor trapping may transfer job completion information into a queue.

4. Supervision of actual data transmitted between peripheral-control and primary memory.

Block Data Transfer Processors

These processors are a special case of the peripheral processors, and are used to execute the special instruction to transfer an array or block of data in primary memory to another location in primary memory.

Display Processors

These processors are specialized peripheral processors which interpret display procedures. That is, a display processor program in memory, when interpreted by a display processor, yields a picture.

PERIPHERALS

The peripheral devices are at the physical and logical periphery of the computer as can be seen by the tree-like structure of Figure 4. The communication to peripherals is controlled from programs in primary

memory which transfer information with the periphery from memory to processor to control unit to peripheral.

Two types of peripheral devices will be discussed: Terminals and Peripheral or File Memory.

The property which separates a file from a terminal is whether information can be *both* written into and read from the file. That is, the device is capable of both storing and retrieving information. The information stored on the file memory can be utilized in various ways according to other properties of the file.

The terminal serves a different function; that of providing the computer with a path with which to communicate with people, or other machines. A file and terminal may be considered almost identical from a program viewpoint. The terminal is restricted in that information can only be 1) written (reading occurs by some media outside the computer), or 2) read (writing occurs outside the computer), or 3) read or written (e.g., a typewriter can be both read or written by a computer, since the computer cannot read what it has written).

Terminals

Terminals are used to communicate with anything outside the computer and may further be subdivided according to with whom they communicate. The characteristics of the terminals are: information transmission time and form (character or blocks); information format or coding; transmission directions (In, Out, In or Out); and selection or addressing of terminal data, e.g. random, linear or sequential, etc.

Direct Terminals. Direct Terminals provide the human user with a node for direct communication with the computer. These terminals include: typewriters, scopes for display of text or graphical information, audio output devices, telephone input dialing units, and specialized terminals, such as bank teller window consoles, airlines reservations consoles or stock quotation terminals.

Indirect Terminals. Indirect terminals provide a communication path between the human user and the computer, but only via a path which requires off line transformation of information. Information is

available at the indirect terminal in only a machine readable form (e.g., holes in a card or tape, or magnetization of an area of tape). A separate, mechanical translation process is required to convert from machine readable to "people readable" form. Indirect terminals include card or paper tape readers and punches, film or photograph readers, specialized format document readers, (e.g., magnetic ink or typewritten), TV cameras, photographic output devices, magnetic tape units, etc.

Machine Terminals. Machine Terminals are those which link other computers, or electrical form devices (such as temperature or pressure transducers, etc.) to the computer. Such a linkage may include the Dataphone, which is a channel or link for transmitting information outside the computer's periphery via telephone channels. Other forms include: analog-digital conversion, and discrete event, time duration, data encoding methods.

A computer is often used as a terminal to the main computer for the following functions:

1. Concentrating or managing a number of typewriter or other terminals on a text line at a time basis.
2. Pre- and post-processing of information on cards, magnetic tape, printers, and plotters.
3. Processing of high data rate terminals for the main computer, as in the case of CRT displays.
4. Connecting to a process of some other kind, e.g., process control, data logging, information collection, etc.

Peripheral or File Memories

These memories lie at the same structural position as terminals. A file's sole function is the storage of information for use by the process (or programs). The parameters which control how a device is to be used in a system are:

1. Cost.
2. Size of memory.
3. Access time and information quantity characteristics. Information selection or access time may be expressed in terms of the following operators:

- Random — Data selection is a constant and is independent of the address (e.g., core address, drum head selection — generally electronic or optical).
- Linear (uni-directional) — Data

selection time varies proportionately with the address (e.g., tape) required.

- Linear — same as above except that either direction of information address searching and data transmission is permitted (e.g., disk selection or track arm).

- Cyclic Linear (or constant rotational) — Data selection time varies proportionally with the address. Addresses are being changed automatically, and take on cyclic values at some rate (e.g., drum).

4. Addressability of information. Some cases include:

- Files with no explicit hardware addresses.
- Files with addresses specified by embedded data.
- Files with explicit hardware address information associated with access mechanism.

5. Replaceability of information. Information space can be recovered by exactly re-writing over existing information, to replace a single part of a file without the need to re-write the whole file.

6. Removeability or portability of information from the computer, i.e., transferability of information off-line among computers. This property provides for information to be removed from the system and stored off line.

The use to which a particular file is put in the system is a function of the above parameters of all storage devices. The present systems have the requirements for the hierarchy: bits, words, word groups (<100-1000 words), program size word blocks (1000-100,000 words), files, and multiple files. The secondary memory functions in the computer can be broken into the following different tasks for which different kinds of file memory can be used.

Program Swapping Memory. Program swapping memory is used for the retention of programs to be placed in primary memory for direct execution by a processor. "Program swapping memory" and "secondary memory" are considered to be synonymous.

Program Swapping, the underlying principle of many time-sharing systems, is the act of keeping programs in secondary, or file memory, until they are ready to be run (as the scheduler decides), and then exchanging them with programs in primary memory so that they may be

executed by the processor and primary memory. The secondary memory may also be used to provide the user with the appearance of a large, homogeneous, one-level primary memory, if sufficient memory allocation hardware is provided (see memory allocation, below).

The transfer of data between the two levels of memory should be as near the primary memory speed as possible (still allowing some arithmetic processing). The single characteristic of time to exchange users between primary memory and program swapping memory affects the maximum number of users and their response time for swapping systems.

Fixed head drums or discs are most commonly used for swapping, since only a rotational or cyclic linear access is encountered to select data.

A program swapping device may not be necessary unless the system serves a large number of users. It is also possible to use some slower storage components, (e.g., program file memory), as swap data media. The substitution of one file type for another allows a system to be built without complete component redundancies and still satisfy uptime constraints.

Program File Memory. Program file memory is storage used for user data base and user programs which are not usually in a state to be run. The requirements for file memory necessitate the use of large, relatively fast, addressable storage in which data items can be replaced. The units which are used for this purpose include fixed or moving head drums or discs, magnetic card readers, and magnetic tape (whose data can be both addressed and replaced).

Backup File Memory. Backup file memory is storage which can be removed from the computer, and includes magnetic cards and tape, etc. This memory is used to retain a snapshot or state of the system at fixed intervals so that the state of the system can be re-established in the event of a failure. This hardware file does not require explicit addressing, or the ability to replace data.

Archival Memory. Archival memory is used to store user files which are removed from the computer. These files exist principally for cost reasons, and the act of retrieving a file from the archives is one of man-

ual selection from a library for which the computer does not have direct access. Magnetic tapes are used for this purpose, since acceptable retrieval time may range from ¼ hour to one day. The files are roughly equivalent to backup storage files.

CONTROL UNITS

The control units have little logical significance in the computer. The controls exist principally because of the cost ratios of control electronics to peripheral devices, and of control electronics to total system costs. It is desirable that all peripherals include controls so that the simultaneous transmission of data from all peripherals is possible.

The functions which the controls perform are:

1. Electrical logic signal conversion. Lines from peripheral devices, e.g., typewriters must have the same electrical characteristics as the computer logic.
2. Time information transformation (Information coding and decoding). The coding of information is an idiosyncrasy of each device, and as such information must be put in a computer compatible form of information.
3. Buffering or assembly of information. Since each device may inherently transfer bit strings which are a sub-multiple of a computer's word, a complete word may have to be formed prior to memory transmission. Very high speed bit rates for the peripheral data can be reduced to acceptable character or word data rates for transmission to memory by parallel data transmission path and buffering.
4. Selection of a specific peripheral from the set which connects with the control. The control retains the switch position information which selects the peripheral.
5. Selection of information within the peripheral. For devices which have information organized in addressable form, the control contains the value of address for the information to be accessed.
6. Error correction and detection.

SWITCHES

A switch provides a communication path between two different component types. Figure 5 lists the switch

forms. The specific choice of which switch to use is a function of the allowable switch cost, the time allowed to transmit information through the switch, the number of simultaneous conversations, the number of units among which switching is to occur, and the expected reliability of the switch relative to the components from which it is constructed (together with requirements for partitioning parts of the switch which have failed).

The implication of the switch diagrams is that the switch is set to a particular value, and that information then flows along the switching paths, between the components (or rather between registers of the components). A large part of the switch consists of decision hardware for setting the switch positions. In particular, along a path for which information is to be switched, there exists a dialogue between the transmitting unit, the switch, and the receiving unit. The dialogue is: transmitter broadcasts a request for a dialogue to either one or all switch units; the appropriate switch setting or selection or closure is made; the information is sent from transmitter to receiver, i.e., the information dialogue takes place between the two units while the switch is in a given position; and finally, after the dialogue, the switch is opened. In some cases, the dialogue first consists of additional selection information. For example, in a multiple memory module system: a processor first makes a request for a particular memory module; the particular switch is closed which allows the processor-memory module dialogue to take place (the processor transmits a particular memory address to the memory so that a memory word is selected; the data transmission takes place between memory and processor); and, finally, the switch is opened, or the dialogue is terminated.

MULTI-PROGRAMMING AND MEMORY ALLOCATION HARDWARE

Multi-programming is the simultaneous existence of multiple, independent programs within primary memory being processed sequentially or in parallel by one or more processors. *Time-Slicing* describes the division or allocation of a processor's time among multiple programs prior

TABLE 2. MEMORY ALLOCATION METHODS

Hardware Designation	Method of Memory Allocation Among Multiple Users	Limits of Particular Method
Conventional computer — no memory allocation hardware	No special hardware. Completely done by interpretive programming.	Completely interpretive programming required. (Very high cost in time is paid for generality.)
1 + 1 users. Protection for each memory cell	A protection bit is added to each memory cell. The bit specifies whether the cell can be written or accessed.	Only 1 special user + 1 other user is allowed. User programs must be written at special locations or with special conventions, or loaded or assembled into place. The time to change bits if a user job is changed makes the method nearly useless. No memory allocation by hardware.
1 + 1 users. Protection bit for each memory page.	A protection bit is added for each page. (See above scheme.)	No memory allocation by hardware.
Page locked memory	Each block of memory has a user number which must coincide with the currently active user number.	Not general. Expensive. Memory relocation must be done by conventions or by relocation software. A fixed, small number of users are permitted by the hardware. No memory allocation by hardware.
One set of protection and relocation registers (base address and limit registers). Bounds register.	All programs written as though their origin were location 0. The relocation register specifies the actual location of the user, and the protection register specifies the number of words allowed. (See Fig. 7.)	As users enter and leave, primary memory holes form requiring the moving of users. Pure procedures can only be implemented by moving impure part adjacent to pure part.
Two sets of protection and relocation registers, 2 pairs of bounds register.	Similar to above. Two discontinuous physical areas of memory can be mapped into a homogeneous virtual memory.	Similar to above. Simple, pure procedures with one data array area can be implemented.
Memory page mapping*	For each page (2^6 - 2^{12} words) in a user's virtual memory, corresponding information is kept concerning the actual physical location in primary or secondary memory. *If the map is in primary memory, it may be desirable to have "associative registers" at the processor-memory interface to remember previous reference to virtual pages, and their actual locations. Alternatively, a hardware map may be placed between the processor and memory to transform processor virtual addresses into physical addresses. (See Fig. 8.)	Relatively expensive. Not as general as following method for implementing pure procedures.
Memory page/segmentation mapping	Additional address space is provided beyond a virtual memory above by providing a segment number. This segment number addresses or selects the page tables. This allows a user an almost unlimited set of addresses. Both segmentation and page map lookup is provided in hardware. (See Fig. 9.) May be thought of as two dimensional addressing.	Expensive. No experience to judge effectiveness.

to the completion of the programs.

Having multiple programs in primary memory may require special hardware for the protection of programs against each other and memory space allocation. Allocation or relocation provides a user address space which is independent of the computer's actual address space.

In general, the goal is to effectively provide each user or user's program with a large, continuous memory space as though he were the sole user. A further goal is to provide a method such that any two identical blocks in primary memory would not have to be duplicated. This ability has significance in implementing

pure procedures.

A *pure procedure* is the constant or pure or read-only part of a program which has been separated from the variable or data part. Operating systems software (including compilers, assemblers, loaders, editors) is generally written as a set of pure procedures for primary memory conservation.

Unless allocation hardware exists, software may have to carry out this function, in which case, not only is the ability of the system limited, but time is consumed in relocating programs.

Sometimes primary memory is broken into pages of 2^6 to 2^{12} words

for hardware allocation. A number of solutions are possible, and Table 2 gives a list of some current schemes. The methods, boundary registers, memory page mapping, and memory page mapping/segmentation mapping are elaborated in Figures 7, 8, and 9.

The *memory map* is part of the user's status information and is generally held in primary memory. The map contains information to transform user's or virtual addresses into physical addresses in primary memory. It may also contain access control information, including whether a page may be read, read as data, written, or read as program.

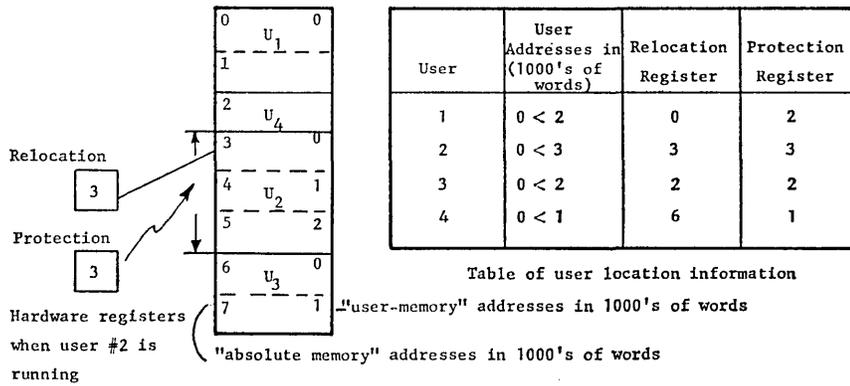


Fig. 7. Memory allocation using boundary or relocation and protection register.

PROGRAM INTERCOMMUNICATION

Although intercommunication among the various hardware elements occurs physically along the lines of the hierarchy, the primary memory provides the main communication path between programs. Communication could be via common files. Normally, two programs only communicate occasionally, and hardware must be used to signal when communication is to occur.

Hardware Interrupts or Traps

Hardware interrupts or traps are intra- and inter-processor state conditions which command the processor to begin the execution of another program or process. The number of conditions which can cause independent program starts is a measure of a processor's capabilities, since state change occurs frequently. *Intra-processor traps* occur for the following reasons:

1. Processor malfunction. The self-checking part of the processor has detected an error. (E.g., a memory access has resulted in an error.)
2. Program or process malfunctions. A program has:
 - Made an arithmetic error (e.g., divide by zero) which, if continued, will yield meaningless results.
 - Made reference to part of a program or data which does not exist or is not available to the program.
3. A timer associated with the processor has signaled that it may be time to do something else.

Intra-Processor Traps for Executive Calls. Hardware instructions are required for efficient intercommunication between the user process and the operating system. The commands for file and terminal activity, and the calling of executive or operating system defined functions is via these special instructions. When they are executed by a user, a trap or interrupt may occur (with a change in status to another mode or process)

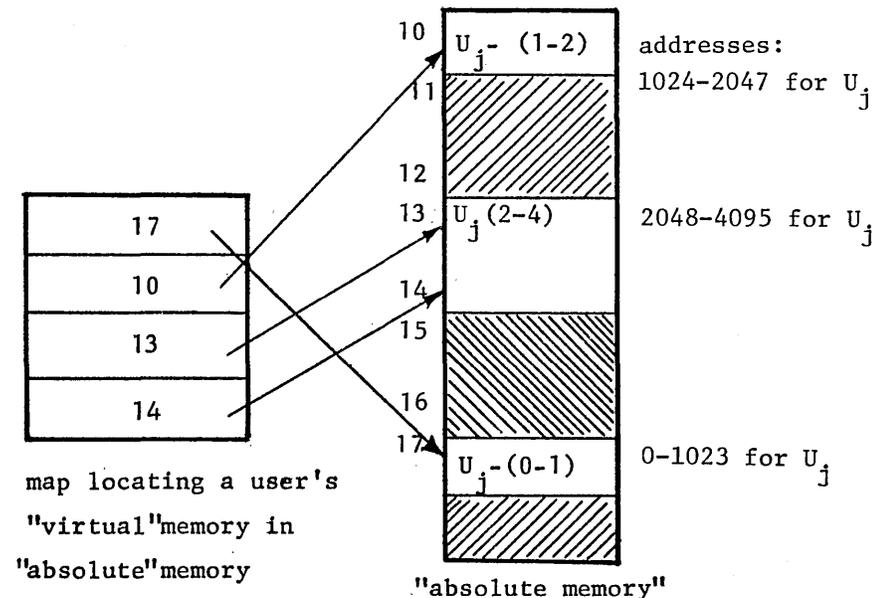


Fig. 8. Memory allocation using page allocation map.

so that the operating system can carry them out. The limits of requirements of these instructions include: decreasing the time between request and action; increasing the number of permissible command types; allowing flexibility in the call type (e.g., subroutine calling with parameters, provisions for data storage on behalf of a user, and the ability of commands to call other commands or nested calls).

Inter-Processor Traps. Inter-processor communication between both arithmetic-arithmetic, and arithmetic-peripheral processors is also accomplished by trapping. Intercommunication among processors is required using interrupts usually when a processor has completed an assigned task or requires another processor's assistance. For example, peripheral processors do not usually have the ability to decide the number of times the reading of faulty records should be attempted before giving up, or what to do after a set of peripheral processes have been carried out.

HARDWARE WHICH FACILITATES GENERAL PURPOSE TIME-SHARING

Special Modes

Privileged instruction set or executive mode denotes a state when the operating system is running and a privileged set of instructions is being executed by the processor for the operating system software. These instructions would not be allowed by a user when running in *user mode* state. The two distinct states, *user mode-executive mode*, represent a minimum requirement to allow allocation and control of resources.

Executive mode allows the operating software system the freedom to activate any terminal, modify any data location, and, in general, do anything which is within the limits of the hardware. User mode implies a restricted set of abilities for the user: no ability to control a peripheral device; access to only a limited data set; etc. This implies that requests for terminal and file activity are via the operating system software. Other modes may be provided which allow the system to reference a user's data, as though the system were a specific user which facilitates data transmission between user and

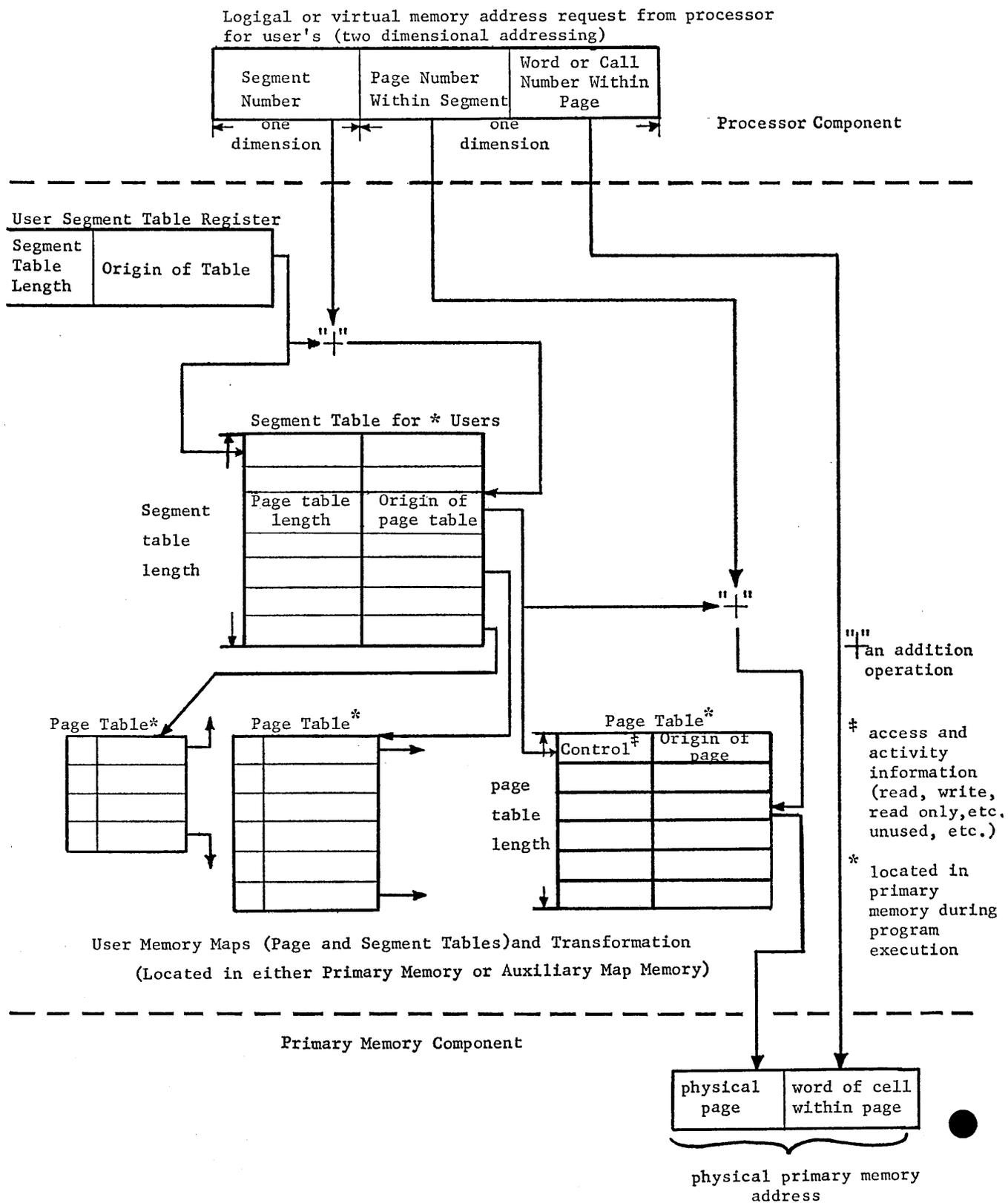


Fig. 9. Memory allocation using pages and segments.

system. For example, users interested in specific terminals might directly control them with no system intervention or overhead. In some cases, a user must directly control a device to effectively utilize it. Additional levels of hardware resource allocation also allow peripherals to be added, and program testing to occur concurrently within normal system use.

Time Measurement Hardware

The switching of processors to processes is done by the scheduling part of the operating system. The software requires a clock or interval timer hardware to measure elapsed time. A processor interrupt accompanies the time interval's termination.

Inter-Processor Interlocks and Communication for Multi-Processing

When multiple arithmetic processors execute the same process or different processes which modifies a common data base (e.g., occurs in scheduling or core allocation procedures), it is necessary to provide hardware interlocks. The interlock prevents the simultaneous multi-processor execution by providing a single processor instruction which simultaneously tests *and* conditionally modifies a primary memory cell by setting into an interlock state. In this way, the first processor enters and locks the process by testing and modifying prior to another processor's use. The second processor must wait for the unlocking to occur before entering.

Inter-processor communication to handle faults and share jobs can take place by normal inter-processor traps or interruptions among processors.

User Status Preservation Hardware

The active user's processor hardware registers and status must be preserved as a processor is switched to a new user on the operating system. Hardware or special instructions which quickly save and restore a user's status and set up another state are desirable to minimize job switching overhead time. They also may simplify the construction of the software and reduce the number of possible errors.

PROPOSED ADVANTAGES FOR TIME-SHARING OF COMPUTERS

In the following discussion, only the positive aspects of Time-Sharing are given. In emerging new systems, there have been just enough positive results to provide us with the ability to imagine how great Time-Sharing can be. Rather than point out how an on line system allows men to be controlled by computer, or how poorly the present machines, which have been adapted for Time-Sharing, perform, I will list the proposed advantages and suggest them as design aspirations.

In general, Time-Sharing replaces an existing form of processing because it offers to provide a better service or cost less, sometimes it offers to do a job that is difficult using another system. It also opens up new avenues of approach which enable a new class of problems to be attacked fruitfully. It is already changing the structure of programs; maybe because of the system structure, but also because of new hardware which might not have been available without Time-Sharing, (i.e., memory segmentation or two dimensional addresses).

ON LINE ADVANTAGES

The direct terminal (by providing a link between computers and man) forms a symbiotic problem solving system. The symbiotic system offers to provide a more complete problem solving system because of the tight coupling between the two components, and power in each processor's domain. For example, in computer aided design the human user synthesizes while the computer analyzes and optimizes. A circuit designer would suggest circuits while the computer would "breadboard" or analyze them. With configuration determined, the computer would optimize the parameter values. Thus, the reactive nature of the on line or direct terminal provides the user with a very responsive tool with which to probe the problem solution space.

A complete tool is available, including all files which hold a user's data base and his procedures are within the system. The problem in transporting physical data is eliminated. Thus, the necessity and in-

convenience of relying on other human systems for the preparation of programs and handling of data is unnecessary. When there is need to create, modify, or destroy a file, the commands are executed quickly.

The total time to make a modification and have another attempt at problem solution, or the problem *turn around time* can be short or appropriate with the task size.

Direct terminal interaction with the system to create and edit files provides a constant monitoring and check on a user's input so that a wide variety of errors can be detected at all levels during the problem solving. That is, data format and validity checking, including the detection of misspelled words occurs at the earliest possible time and lowest level. Clerical functions, including program preparation, drawings, and report generation are part of the system.

Data may be presented in more useful forms to on line users without the need to transfer entire output files to paper. A user may specify only the part of the file or process of interest. More useful forms of data presentation, such as graphs, charts, and diagrams may be presented on displays and plotter.

USER COMMUNITY ADVANTAGES

A general purpose system provides an ever increasing set of procedures for problem solutions, created by its users. Procedures may enter the public domain more rapidly, the author need issue only a notice to the system (which informs other users). Procedures in the public domain become useful more quickly because a large community of users has immediate access to them and incidentally simultaneously checks them. Common or shared data bases (e.g., census data) need only be gathered once and appear in one file.

Routine inter-user administrative tasks such as updating the library, administrative message sending, and availability lists occur at time of origin and are automatically part of the system.

The accounting of resources is by the system with controls imposed by overall human administration. Not only is there better accuracy, but users can be monitored rather than being required to administer their

own time. This, in turn, provides better information about the total utility of the system and its users.

A higher level of standardization is possible and can be achieved among users and hence the ease of using the system should improve. Trivial functions which tend to be rewritten (e.g., error handling of messages, lesser used arithmetic functions, the manipulation of characters to form words, etc.) are more likely to be shared because of the ease of sharing.

The possibility for improving the documentation associated with procedures should improve through the ease of documentation and perhaps pressure of the community to share procedures. The overall documentation (text, diagrams, etc.) which describe a process or problem solution may improve.

FLEXIBLE TERMINAL LOCATION

Most direct terminals may be located where they can most efficiently

serve the users; in fact, they are even portable. No longer will it be necessary for the user to preschedule time, but he can now use the computer as his tool when and where he best is able to work. For some, this may be in an office, for others a laboratory, and still others, their home. Ultimately, consoles will be in all homes. For example, consider the salesman who has a terminal in his home (or a portable one in his car) such that he can help the computer determine a list of the best calls for that day.

ECONOMICAL ADVANTAGES

In general, a community is provided with a much larger system than any single member could afford. For on line or real time systems, the hardware and software overhead associated with this additional ability can be associated with a larger number of users.

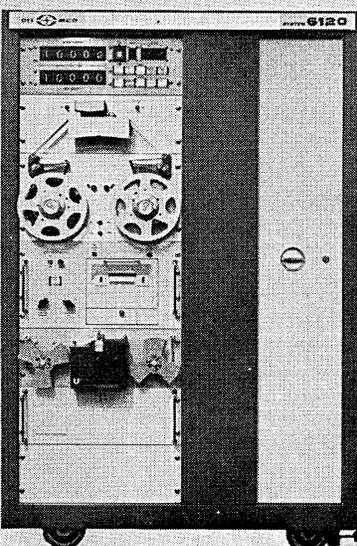
A large number of facilities (coordination of all file activity, transmission of data to terminals, stan-

dard error handling, etc.) which are overhead functions are implemented within a system framework rather than repeatedly by each user as he attempts to form his own system. Parallel requests for resources rather than serial processing provide the system with more information to improve scheduling.

Since the system provides the users with the ability to "watch" the execution of a process, the likelihood of using large amounts of processing capability yielding erroneous results is lessened.

If the community of users is sufficiently large, there should be more than one hardware unit of each type, and in the event of hardware failure, the system can be repartitioned to maintain a working system although of lesser performance.

The second and concluding part of this article, which contains an extensive bibliography on time sharing, will be published in the March issue of Computer Design.



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The Exclusive-Or Element

by IVOR CATT

The Bunker-Ramo Corp.
Teleregister Div.

Failure of the Exclusive-OR Element to take its rightful place as one of the primary logic elements is based on historical reasons which are not valid today. If an I/C family of logic packages exceeds three types, the exclusive OR element should be part of the family.

Historical

It was probably difficult to implement the Exclusive-OR with relays.

When we entered the diode-triode era, diodes in parallel provided the AND or the OR function and a triode provided the INVERT function and also the (very necessary) amplification and restandardization. During the diode-triode era, diodes were expensive and triodes were more so. There was a tendency to try to go through more than one stage of diodes, AND-OR, before reaching the more expensive triode INVERT. This gave the AOI (AND-OR-INVERT) type of gate, which appeared to some designers to minimize the expensive triode, giving a great deal of logical power per triode. However, the majority favored the simple AND-INVERT for reasons of speed and because it was doubtful if all of the logical power of the AOI could be put to good use.

The advent of transistors did not significantly alter the picture. As before, diodes were expensive and transistors (instead of triodes) were very expensive. Some designers used the AND-INVERT, and some argued for the AOI. Some went further, and used, or tried to use, four stages of diodes in series before bringing a transistor to the rescue. The logic function was AOAIOI.

With the development of integrated circuits, tradeoffs that applied to discrete diode transistor logic were transferred directly to integrated circuit design. As far as I can see, no concessions were made when choosing logic functions to the fact that the integrated circuit was a new environment, and new tradeoffs would apply. At least, the resulting products were remarkably similar to the discrete circuits they replaced. As with discrete circuits, the integrated AND-INVERT (called NOR or NAND) took about 80% of the market, and the AOI took about 20%.

Up till now, the idea that AND, OR and INVERT are the basic logic functions has been firmly entrenched. Many techniques have been developed to handle these functions, including Boolean Algebra and minimization with Veich diagrams, minterms and maxterms.

TYPE 1		
A	\bar{A}	
B	1	0
\bar{B}	0	0

TYPE 2		
A	\bar{A}	
B	0	1
\bar{B}	1	0

TYPE 3		
A	\bar{A}	
B	1	1
\bar{B}	1	0

TYPE 4		
A	\bar{A}	
B	0	0
\bar{B}	0	1

TYPE 5		
A	\bar{A}	
B	1	0
\bar{B}	0	1

TYPE 6		
A	\bar{A}	
B	0	1
\bar{B}	1	1

TYPE 7		
A	\bar{A}	
B	1	1
\bar{B}	1	1

TYPE 8		
A	\bar{A}	
B	0	0
\bar{B}	0	0

Fig. 1. Truth tables for the 16 types of logic elements.

Analysis

A logic element with one input, A, can be either a link, with output A, or an inverter, with output \bar{A} . The first type will be dismissed as trivial. The second type, the Inverter, has a truth table as follows:

A	\bar{A}
0	1

A logic element with two inputs, A and B, can be of 16 types. Of these, eight types treat A and B symmetrically. That is, if the inputs are replaced by each other, the output remains the same. The truth tables for these eight types are drawn in Figure 1. We shall dismiss the last two as trivial. This leaves us with types 1 thru 6.

Type 1 is the AND gate. Type 3 is the OR gate. Type 2 is the exclusive OR. The other three types are the image of types 1 thru 3, and we shall neglect them.

We now see that if we limit ourselves to logic elements with two inputs or less, the primary functions appear to be:

1. Inverter
2. AND
3. OR
4. Exclusive OR

For a set of logic elements to be complete, it must include the INVERTER. A complete set of logic elements need contain only the INVERTER and either the AND or the OR. With these two elements, any logic function can be implemented. By studying the truth tables or by using De Morgan's theorem, we see that the AND and the OR function are very similar to each other. In their truth tables, the centre of gravity of the 1's is not at the centre of the table, but falls somewhere on the N.W.-S.E. diagonal. However, the Exclusive-OR appears to

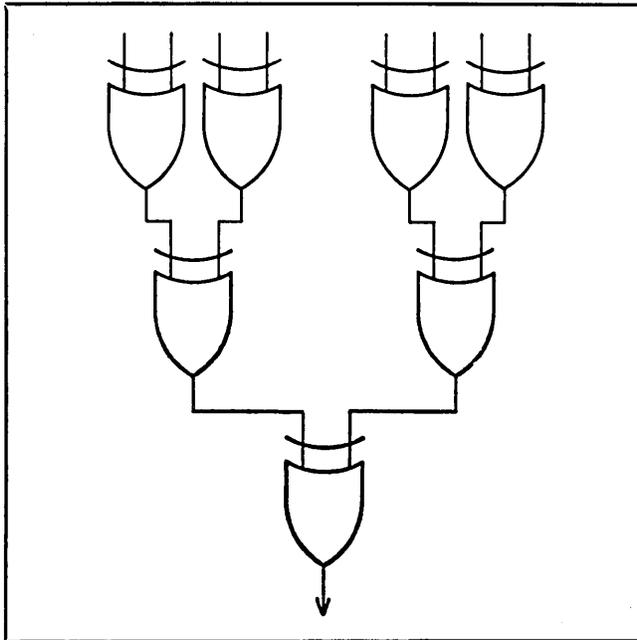


Fig. 2. The exclusion OR used to generate parity.

be a quite different type of function. In its truth table, the centre of gravity of the 1's is at the centre of the table. We can therefore call it a "balanced function," and the output will be true half of the time if we go through all possible combinations of inputs.

If we limit ourselves to functions of two variables or less, we now see that there are three types:

1. INVERTER
2. UNBALANCED FUNCTION (AND or OR).
3. BALANCED FUNCTION (Exclusive OR).

Although one unbalanced function plus the Inverter make up a complete set, a Balanced function (Exclusive OR) plus the Inverter do not. That is, some logic functions cannot be implemented using only Exclusive OR's and Inverters.

So if a family of logic elements is being designed using only one type, then the NOR or the NAND, which embraces both the unbalanced function and the Inverter, is the proper choice to make, and the Balanced function (Exclusive-OR) rightly will not appear in the family.

If a family of logic elements is being designed using more than one type, it looks as though the Balanced function (Exclusive-OR), as one of the three primary logic functions, has a strong claim to be included.

ALTERNATIVE NAMES FOR THE EXCLUSIVE-OR

Probably the greatest disadvantage under which this logic function labours is its name. Other possible names for the Exclusive-OR, which give an indication of its versatility, are as follows:

1. Equivalent (Actually, Non-Equivalent) This is the name it should carry.
2. Parity
3. Comparator
4. Inverter

Figures 2 through 5 illustrate this versatility.

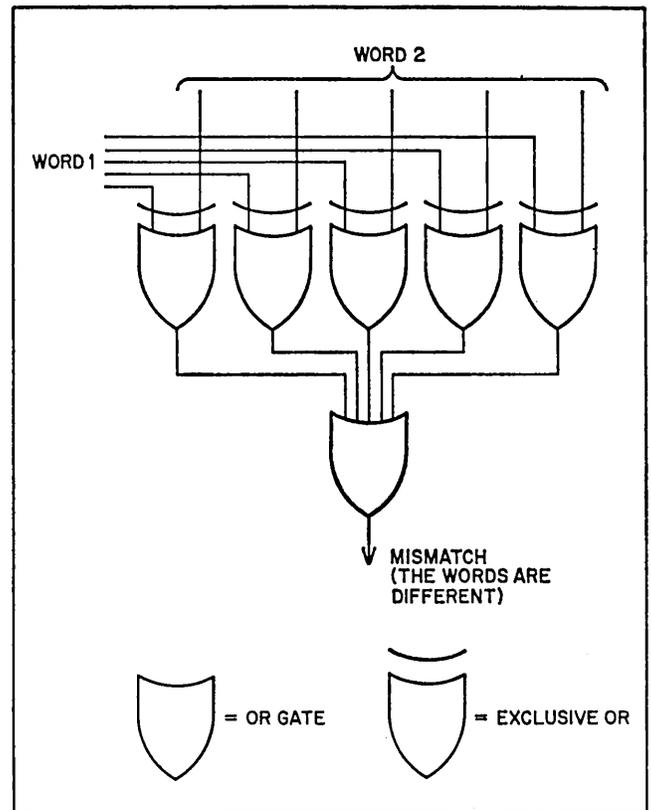


Fig. 3. The exclusive OR used in a comparator.

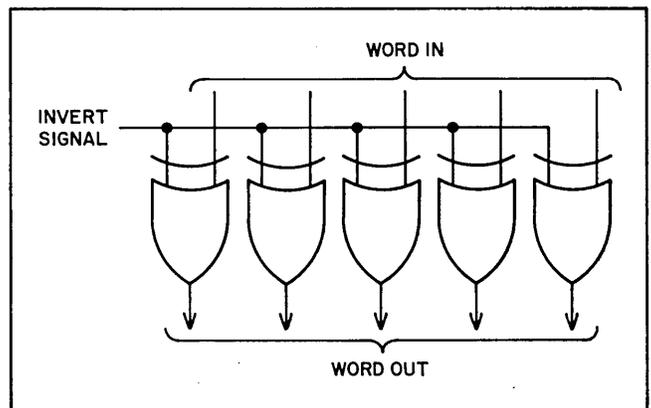


Fig. 4. The exclusive OR used to invert a word (one's complement).

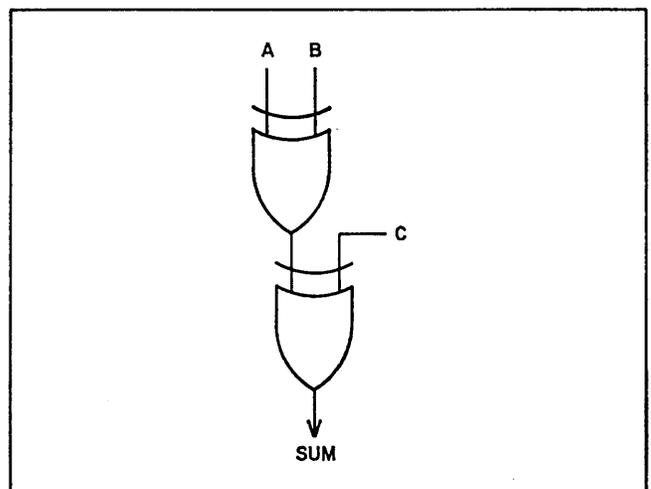


Fig. 5. The exclusive OR used to generate the sum in an adder.

When correctly applied the core buffer equation can reduce the cost of your data acquisition system.

INTERLACED CORE BUFFER APPLICATIONS

BARRETT W. REESE
Senior Systems Engineer
Leach Corporation
Controls Division

Frequently in the design of digital systems, an engineer is required to utilize a core buffer memory. The application usually falls into one of two categories; (a) the core input rate is constant or (b) the core input data rates are variable. When such requirements exist, several approaches to core buffer selection may be used; however, there are approaches which result in the minimum size core buffer required for a particular application.

Three types of core buffer operations are available: random access, sequential access, and sequential-interlace access. In random access, core locations are selected by the direct transfer of random input address to the core address register. For sequential access, the address counter and address register are initially reset. During each subsequent memory cycle the address counter is incremented, and the resulting count transferred into the core address register. Consequently, memory locations are addressed consecutively. The sequential-interlace addressing scheme uses two separate address counters: one for addressing words to be loaded, and one for addressing words to be unloaded. This type of addressing is used most often for buffering data between two points in a system in which input and output rates are not the same; for example, buffering data from an acquisition system to a magnetic tape recorder. To allow the reader greater freedom in core buffer use with digital system applications, a brief derivation of the core buffer interlace equation is presented first.

In digital systems with very low input rates and very high output rates, where sufficient data output can be obtained between input data cycles, core buffering may not be necessary. However, in digital systems requiring core buffer applications it is generally the case that data is being acquired at one rate, say H_{zi} , and must be output at a higher rate, say H_{zo} . Therefore, data must be stored until a pre-determined amount has accumulated and then output at rate H_{zo} . The core buffer performs this storage function economically when properly selected.

Assume that data is being continuously acquired at a rate H_{zi} and that it is to be output in data blocks "a" characters long at a rate of H_{zo} . Since the output rate (H_{zo}) is greater than the input rate (H_{zi}), the output operation must begin after an unknown number of characters have been acquired. This is shown diagrammatically in Figure 1.

H_{zi} = input data rate (data acquisition rate)
 H_{zo} = output data rate
a = length of a data block in characters (bytes)

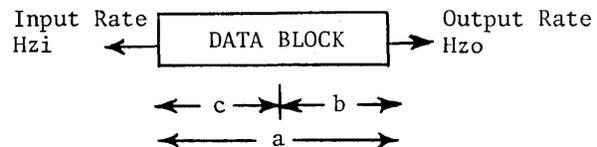


Figure 1

- b = the number of characters acquired by the system and stored in memory while outputting data (interlaced operation)
- c = the number of characters that must be acquired by the system and stored in memory before data output begins
- T_i = the time required to acquire and store "a" characters of data at rate H_{zi}
- T_o = the time required to output "a" characters of data at rate H_{zo}

The time relationships required are such that unload (output) must begin after "c" characters of data are acquired and stored in memory. Therefore, the unknown "c" must be determined. If H_{zo} is greater than H_{zi} , less time is required to output "a" characters than is required to acquire "a" characters; therefore:

$$T_i = T_o + \frac{c}{H_{zi}} \quad (1)$$

This equation states: the time required to acquire "a" characters of data is equal to the time required to output "a" characters, plus the time required to load "c" characters before unload begins.

From the definitions, it can be seen that:

$$T_i = \frac{a}{H_{zi}} \quad \text{and} \quad (2)$$

$$T_o = \frac{a}{H_{zo}} \quad (3)$$

These two equations state that the input and output times are inversely proportioned to the input and output data rates.

Equations 1, 2 and 3 may be used to find the unknown "c":

$$T_i = T_o + \frac{c}{H_{zi}} \quad (1)$$

Substituting 2 and 3

$$\frac{a}{H_{zi}} = \frac{a}{H_{zo}} + \frac{c}{H_{zi}}$$

$$\frac{a}{H_{zi}} - \frac{a}{H_{zo}} = \frac{c}{H_{zi}}$$

$$a - \frac{a H_{zi}}{H_{zo}} = c$$

or
$$a \left(1 - \frac{H_{zi}}{H_{zo}}\right) = c \quad (4)$$

The last equation is the core buffer interlace equation which can be rewritten:

$$c = a \left(\frac{H_{zo} - H_{zi}}{H_{zo}}\right) \quad (4)$$

This equation states that before data output begins, "c" characters must be stored in memory and tells what the minimum core buffer length "c" is for any length of data block for any applicable input and output data rates. This is explained by the two following statements.

If H_{zo} is equal to H_{zi} , then generally, a core buffer is not required and data cannot be output in block form where each block is preceded and followed by a gap in the data.

If H_{zi} is greater than H_{zo} , then a core buffer is not required and data must be output at the acquisition rate.

As $H_{zo} \rightarrow \infty$, the core buffer length approaches the required record length.

As $H_{zi} \rightarrow 0$, the core buffer length approaches the required record length.

Constant Input Data Rate Applications

The following discussions are devoted entirely to applications of the core buffer equation. There are numerous problems which should be considered; a representative few have been selected using a magnetic tape output device.

APPLICATION 1

Assume the following:

Data is being acquired continuously at rate $H_{zi} = 10,000$ bytes/sec.

Data is being output in block form at rate $H_{zo} = 30,000$ bytes/sec.

Data block is to be 5,000 bytes:

$$c = a \left(\frac{H_{zo} - H_{zi}}{H_{zo}}\right) = 5,000 \left(\frac{30,000 - 10,000}{30,000}\right) = 5,000 \left(\frac{2}{3}\right) = 3333.3$$

Therefore, a core buffer 3333.3 bytes long must be used. In practice, this would require a 4096 address core memory.

Before accepting this answer, one other consideration must be investigated. In writing a gapped magnetic tape, time is required to generate a block gap. The block gap time cannot exceed:

$$\text{BGT} \leq \frac{c}{H_{zi}} \quad (5)$$

This equation states that the number of characters that must be acquired by the system and stored in memory, while outputting data, must be equal to or greater than the number of characters which are acquired during the block gap time.

If we assume a fairly standard block gap time of 10 milliseconds to generate a $\frac{3}{4}$ inch block gap (transport start/stop distance may be sufficiently short such that this operation can be performed in less than $\frac{3}{4}$ inch. A write delay may be necessary to inhibit transport writing after tape is up to speed in order to generate a $\frac{3}{4}$ inch gap) then:

$$c \geq H_{zi} \text{ BGT} \quad \text{Restating equation (5)} \\ 3333.3 \geq (10,000) (.01)$$

Since "c" is greater than (H_{zi}) (BGT), then all conditions for operation are satisfied.

APPLICATION 2

Assume the following:

Data is being acquired in block form at an instantaneous rate $H_{zi} = 30,000$ bytes/sec.

Data is being output in block form at $H_{zo} = 20,000$ bytes/sec.

Data block is 10,000 bytes

A data block is acquired once each second.

If this case is studied, it will be seen that although the instantaneous data acquisition rate (30,000 bytes/sec) is higher than the output data rate (20,000 bytes/sec), the average input data rate is 10,000 bytes per second. Therefore, the core buffer equation is still valid:

$$c = a \left(\frac{H_{zo} - H_{zi}}{H_{zo}}\right) \\ = 10,000 \left(\frac{20,000 - 10,000}{20,000}\right) \\ = 5,000 \text{ bytes}$$

For this example, a core buffer of 8,192 bytes is standard.

Again, the block gap time must be considered:

$$c \geq H_{zi} \text{ BGT} \\ c \geq (10,000) (.01) = 100.0 \text{ bytes} \\ \text{and again the example is valid.}$$

APPLICATION 3

Assume the following:

Data is being acquired continuously at a rate $H_{zi} = 28,000$ bytes/sec.

Data is being output in block form at a rate $H_{zo} = 30,000$ bytes/sec.

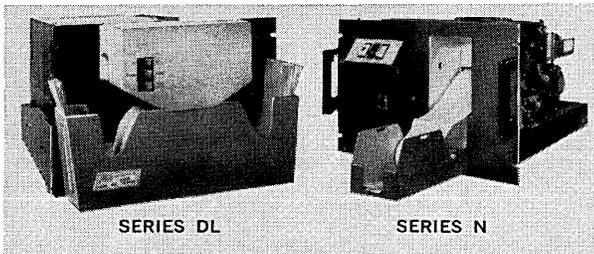
A data block is 500 bytes:

$$c = a \left(\frac{H_{zo} - H_{zi}}{H_{zo}}\right) \\ = 500 \left(\frac{30,000 - 28,000}{30,000}\right) \\ = \frac{500}{15} \\ = 33.3 \text{ bytes}$$

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A core buffer of 33.3 bytes is required for this case. A standard memory would be 128 addresses long.

The block gap time must now be checked to see if the application is valid:

$$c \geq Hzi \text{ BGT} = (28,000) (.01) \\ = 280 \text{ bytes}$$

Therefore "c" is not greater than or equal to (Hzi) (BGT) and the core buffer cannot be interlaced. Now the case of not stopping the tape transport can be investigated. Assume that 7.5 milliseconds are required to generate a block gap if the tape drive is not stopped; then:

$$c \geq (Hzi) (BGT) \geq (28,000) (.0075) = 210 \text{ bytes}$$

This states that for Application 3, the core buffer cannot be interlaced. The engineer then goes to another approach using the core buffer equation as a guide. If the record length is changed, the interlace operation can be made to work.

The problem is to find a record length which will allow 210 bytes to be loaded during the block gap time:

$$a = \frac{Hzo \ c}{Hzo - Hzi} \text{ (core buffer equation solved for a)}$$

$$a = \frac{(30,000) (210)}{30,000 - 28,000} = \frac{6,300,000}{2,000} = 3,150 \text{ bytes long}$$

If nine of the original blocks of data are written as one output block, then interlace is possible and a 512 address core memory would be used.

This can be checked by again applying the core buffer equation:

$$c = a \left(\frac{Hzo - Hzi}{Hzo} \right) = 4,500 \left(\frac{30,000 - 28,000}{30,000} \right) \\ = \frac{4,500}{15} = 300.0$$

This states that 300 bytes (which is greater than the 210 byte record length required) must be loaded before unload begins and start-stop tape drive operation can be used.

APPLICATION 4

Assume the following:

Data is being acquired in block form at $Hzi = 10,000$ bytes/sec.

Data is being output in block form at $Hzo = 10,000$ bytes/sec.

Input data blocks are 500 bytes

Output data blocks are 1500 bytes/sec.

Assume that 100 milliseconds are required for each input data block.

From this assumption, it can be seen that the average input data rate is:

$$Hzi \text{ (avg.)} = \frac{500 \text{ bytes}}{0.1 \text{ sec.}} = 5,000 \text{ bytes/sec.}$$

and is a lower rate than H_{zo} : therefore, the core buffer equation is still valid:

$$c = a \left(\frac{H_{zo} - H_{zi}}{H_{zo}} \right) = 1,500 \left(\frac{10,000 - 5,000}{10,000} \right) = 750 \text{ bytes}$$

This figure would be checked by:

$$c \geq (H_{zi}) (BGT)$$

$$c \geq 5,000 (.01) = 500 \text{ bytes}$$

Therefore, $c \geq (H_{zi}) (BGT)$ and interlace operation is possible with a 1024 addressed core.

Variable Input Data Rate Application

Core buffers are also used in applications where the input data rates are variable. When designing within this parameter, a "ping-pong" data handling technique may be used, as shown in Table 1.

TABLE 1

0 to 65 K Hzi 4022 byte record 62.0 ms		RECORD Y		RECORD Z		
Core Input →	RECORD X	Start Tape	RECORD Y	Start Tape	RECORD Y	Stop Tape
Core Output →		10 ms	96 K Hzo 42.0 ms	10 ms	10 ms	10 ms

The core buffer is first loaded with RECORD "X". Upon completion of this loading, the tape transport is started, requiring 10 ms to come up to speed. When final tape speed is obtained, RECORD "X" is unloaded from core onto tape, followed by 10 ms of tape transport stop time. During the previous cycle, the interlaced operation of loading RECORD "Y" while unloading RECORD "X" had been occurring. Upon completion of RECORD "Y" loading, the tape transport is started and the entire operation is repeated.

Jumping back and forth between two sections of core, each holding one complete record, thus forms the "ping-pong" technique.

In the cited example,

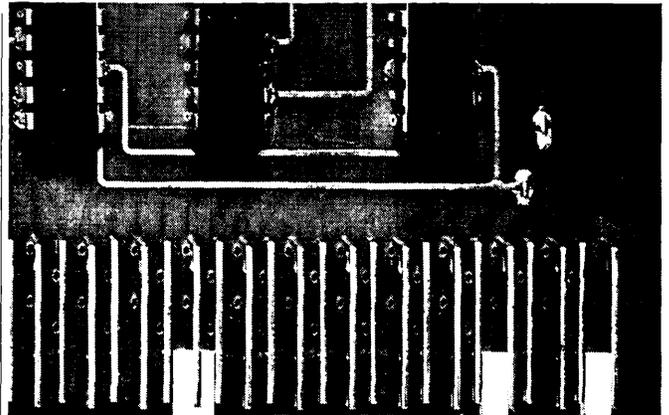
$$\begin{aligned} \text{since } BGT &= 20 \text{ ms (transport start/stop times)} \\ \text{from (5): } c &= (H_{zi}) (BGT) \\ &= (65,000) (.020) \\ &= 1,300 \text{ bytes} \end{aligned}$$

Therefore be substitution in (4):

$$\begin{aligned} 1,300 &= a \left(\frac{96,000 - 65,000}{96,000} \right) \\ a &= 4,022 \text{ bytes} \end{aligned}$$

Since the "ping-pong" operation requires a core size be twice the record length, the core should provide storage for 8,044 bytes. In this case a 8192 addressed core would be used.

When correctly applied, the core buffer equation can reduce the cost of your data acquisition systems. It must be remembered, however, that interlacing operations derived through application of the core buffer equation require rigid timing controls and should be approached with scrutiny.



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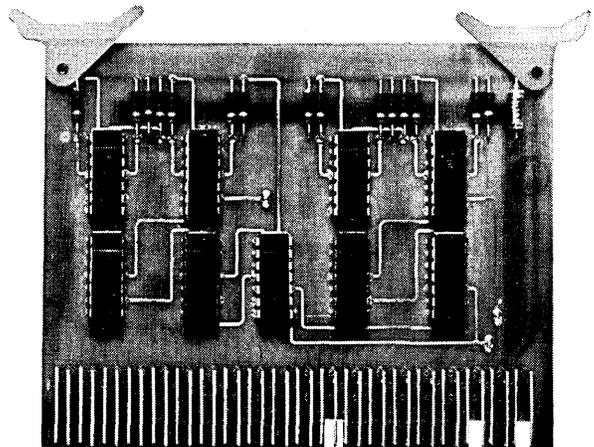
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THE TERNARY NUMBER SYSTEM FOR DIGITAL COMPUTERS

The most efficient radix for a number system is e , the base of the natural logarithm. Since 3 is the nearest integer to e , it is reasonable to investigate the possibility that a ternary computer should be more efficient than a binary computer. For example, a 10-digit decimal number needs 40 bits in binary coded form, 33 digits in straight binary translation, and 21 digits in ternary representation. Provided a ternary-register element costs the same as a binary element, a ternary computer appears to be very attractive. In present computers, the numerical systems are either binary or binary coded because most of the available switching elements are of binary nature. In this paper, a ternary number system is shown to be more efficient than a binary system provided that the ternary-element costs are not more than 1.5 times greater than the cost of a binary element. A ternary algebra is developed, and a ternary switching system is described.

A. Turecki

Palm Beach Operations

Electronic Data Processing, Palm Beach Gardens, Florida

IN DIGITAL COMPUTERS, all the arithmetic operations, fixed or floating point, are carried out on integers. The sign of a quantity and its magnitude in the floating-point system are operated by a sign logic and an exponent logic respectively. Hence, in the number representation for computers there must be methods for indicating sign and exponents of the operand quantities. Most digital computers use positional notation with fixed radices of 2, 8, 10 or 16. At least one mass-produced computer uses a notation with radices of 2 and 5 (the bi-quinary notation which was used the first time in one of the earliest digital computing devices, the Chinese *suan pan*).

The Cost Considerations of Various Radix Systems

Let us assume that to represent each symbol in a given numerical system we need one logic element, and that the maximum numerical quantity to be handled is N . If r is the radix of the system the number of the required elements is $r \log_r N$ for $\log_r N \gg 1$.

For the evaluation of different numerical systems we introduce a function, f_r , the ratio of the required hardware for the r -radix system and for the binary (2-radix) system:

$$f_r = r \log_r N / 2 \log_2 N = r / 2 \log_2 r$$

Setting the derivative of f_r equal to zero,

$$df/dr = (\log_2 r - \log_2 e) / 2(\log_2 r)^2 = 0$$

the minimum occurs at $r = e$. Thus, if the logic and memory elements with r -stable states were only $r/2$ times more complex than the presently used elements with two stable states, the r -radix numerical system would be the most economical.

Let us now consider the case where the numerical systems of the base $r > 2$ are binary coded. For the comparison of the required hardware we should use the function

$$g_r = I_r / \log_2 r$$

where I_r is an integer and is the minimum required number of binary bits for the representation of one digit of the r -base. The magnitude of g_r for some values of r is as follows:

r	2	3	4	5	6
f_r	1.000	0.946	1.000	1.078	1.148
g_r	1.000	1.262	1.000	1.294	1.148
r	7	8	9	10	100
f_r	1.247	1.333	1.420	1.505	7.526
g_r	1.069	1.000	1.262	1.204	1.053

Note that:

- 1) For $r \geq 2$, $g_r \geq 1$;
- 2) for r equal to the positive powers of 2, $g_r = 1$;
- 3) For $r = 5$, g_r reaches the maximum value;
- 4) For $r = 6$, $g_r = f_r$; and
- 5) For $r \gg 1$, $g_r = 1$.

Thus, using two-stable-state logic elements, the most economical numerical systems are of the base of 2, 4, 8, . . . , 2^n ; the decimal system is only 20% more expensive than the binary. If one could develop sufficiently reliable three-stable-state logic elements which would be only 3/2 times more expensive than the corresponding binary element, the saving of 5.4% [$(f_3 - f_2)/f_2 = 0.054$] in the arithmetic unit hardware would be accompanied by an increase in the memory cost by 26% [$(g_3 - g_2)/g_2 = 0.26$] if the memory used were still 2-state. Hence, the ternary system would be justified only if both 3-state logic elements and 3-state memory elements were available.

These comparisons for different numerical systems have not considered the variations in the complexity of required logical schemes since this can be seen only after a scheme is developed. Therefore, the commonly used argument, that present availability of two-state logic elements

Development of a Ternary Switching Algebra

The extension of the Boolean algebra to the ternary switching circuits will be modeled mainly after the many-valued propositional logic introduced by Post.

The three basic Boolean operations are *union*, *intersection*, and *complementation* which are mechanized by *or*, *and*, and *invert* logic elements. These concepts, with certain modifications, will be used in the development of the ternary logic.

A Post algebra P is a class of C of elements p, q, r, \dots with two basic operations; $p \cdot q$ (*product*) and p' (*cycling*). Assuming three truth values (0, 1, and 2) for the elements of C , the above mentioned operators are defined by the following truth tables.

Product				Cycling		
q	p	0	1	2	p'	p'
0	0	0	0	0	0	1
1	0	0	1	1	1	2
2	0	0	1	2	2	0

As defined here, $p \cdot q = \min(p, q)$; that is, the product of p and q equals the smallest truth value, and represents a ternary *and* function.

Many mysteries of multi-valued logics will be cleared up when one realizes that the words *and*, *or*, and *not* have at best only tenuous analogy with their meanings in natural languages. A three-valued logic function means nothing more than the particular matrix pattern of the truth table that is permitted by that relation. If instead of saying *A implies B* in a ternary system, we said *A galumphs B*, considerable clarity might result.

In this article, though it is recognized that there are significant differences in the structure of two-valued and many-valued logics, the analogies between the systems will be stressed and the binary logic will be considered to be a special case of multi-valued logic. For instance, if in the truth table defining the ternary *and* the truth value of 2 is excluded, it becomes the truth table for the familiar binary *and*. The same applies for the *cycling* concept, after eliminating 2, it becomes a binary *not*. In the binary logic, the *double not* of a variable is equal to the variable. It follows then that if a *double not* of a variable yields the variable, then a *triple cycling* in ter-

ternary logic should yield the same result. Hence Post's cycling was defined accordingly.

Fundamental to any logic algebra is the existence of an algebraic form of any function which explicitly gives the value of the function for every combination of variable values; this is the *canonical form* of the function. Closely associated with the canonical form is the *expansion theorem* which expands any function in a series about any of its variables. The canonical form is a result of expanding about all variables of a function. This form is the essence of synthesis; applying the expansion theorem in reverse is the first major step in *minimization*.

A logic switching algebra, to become a useful tool for the analysis and synthesis of switching networks, should operate with connectives which are complete functionally. The *completeness* of a connective or a group of connectives can be described for 3-valued logic as follows:

there are 3^n different functions of n variables, and a given connective is complete if it is possible to express all

the 3^n functions with only that connective or a group of connectives.

There are several ways of proving the completeness of a given connective or a group of connectives; one way is to prove an expansion theorem, while another is to establish an *isomorphism* (one-to-one relationship that preserves the operations of addition, multiplication, and the order relationship) between the algebra to be tested and another algebra which is known to be complete.

By definition a Post function is any element of a finite set P built up from elements of an arbitrary set C by a finite number of combinations of *product* and *cycling* operations. Since the ternary switching functions as defined by tables of logic values are themselves Post functions, there is a canonical expansion of the functions in terms of the product and cycling operation. Hence, the ternary switching logic, as presented here, is complete.

To simplify the analysis and synthesis of the ternary functions, some auxiliary operations will be introduced. These are *sum* ($p + q$) and *negation* (p and J) operations.

$(p + q)$				
q	p	0	1	2
0	0	0	1	2
1	0	1	1	2
2	0	2	2	2

p	\bar{p}	$J_0(p)$	$J_1(p)$	$J_2(p)$
0	2	2	0	0
1	1	0	2	0
2	0	0	0	2

As defined here, $p + q = \max(p, q)$ and $J_k(p) = 2$, if $k = p$; $J_k(p) = 0$ if $k \neq p$.

Note that the J operation, reduced to the binary logic, becomes the binary negation. According to the definition, $J_0(1) = J_1(0) = 0$ and $J_1(1) = J_0(0) = 1$. Therefore, if $J_1(p) = p$, then $J_0(p) = \bar{p}$; the bar signifies binary negation.

In the ternary switching logic, there are $3^3 = 27$ different functions for one variable. The table of all 27 ternary functions can be reduced to the four binary functions for one variable, once again showing that the binary as well as the ternary logics are special cases of the general m -valued logic system developed by Post.

p	0	1	2	Ternary Functions
f_0	0	0	0	$J_0(p) \cdot J_1(p)$
f_5	0	1	2	$J_2(p) + J_1(p) \cdot 1 = p$
f_{21}	2	1	0	$J_0(p) + J_1(p) \cdot 1$
f_{26}	2	2	2	$J_0(p) + J_1(p) + J_2(p)$

p	0	1	Binary Functions
f_0	0	0	$J_0(p) \cdot J_1(p) = p \cdot \bar{p}$
f_5	0	1	p
f_{21}	1	0	$J_0(p) = \bar{p}$
f_{26}	1	1	$J_0(p) + J_1(p) = p + \bar{p}$

In determining logical functions from given truth tables it is necessary to be familiar with some systematic techniques. However, one should not overlook the importance of the truth table inspection before general methods are applied. If a special pattern is noticed, the required function can be written directly from the truth table.

A general method for determining logic equations in terms of J operators, defined by truth tables, is as follows:

- 1) Write down separate J minterms (a minterm of n variables is the Boolean product of these n variables with each variable present in either its true or complemented form) for each non-zero term of the function, making the order of J operators equal to the truth value of the corresponding variables. If this term is 1, multiply the generated minterm by 1.
- 2) To produce the complete equation, realizing the given function, add all the J minterms.
- 3) Simplify the equation.

Example:

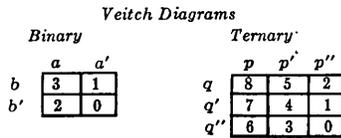
Determine the logic equation for the function f defined by the truth table as shown below.

p	q	f	J minterms
1	1	1	$J_1(p) \cdot J_1(q) \cdot 1$
1	2	1	$J_1(p) \cdot J_2(q) \cdot 1$
2	1	1	$J_2(p) \cdot J_1(q) \cdot 1$
2	2	2	$J_2(p) \cdot J_2(q)$

The portion of the truth table not shown contains all zeros under f .

$$\begin{aligned}
 f &= J_1(p) \cdot J_1(q) \cdot 1 + J_1(p) \cdot J_2(q) \cdot 1 + J_2(p) \cdot J_1(q) \cdot 1 + J_2(p) \cdot J_2(q) \\
 &= J_1(p) \cdot 1 \cdot [J_1(q) + J_2(q)] + J_2(p) \cdot [J_1(q) \cdot 1 + J_2(q)] \\
 &= J_1(p) \cdot 1 \cdot q + J_2(p) \cdot q \\
 &= [J_1(p) \cdot 1 + J_2(p)] \cdot q \\
 &= p \cdot q
 \end{aligned}$$

To simplify the binary logic functions, the Veitch diagram technique is often more convenient and faster than algebraic manipulation. It was found that the Veitch diagrams can be extended, to ternary logic:



The Veitch diagram rules for ternary logic, compared to those for binary logic, are as follows:

- 1) In binary Veitch diagrams, the truth values assumed are $a = 1$ and $\bar{a} = 0$; similarly in the ternary diagrams $p = 2$, $p' = 1$, and $p'' = 0$. The most significant variable in this example is at the top of the diagram for both ternary and binary diagrams.
- 2) Any binary function transferred from the truth table to the Veitch diagram is marked by 1's in the corresponding cells. Since the ternary function is defined in its truth table by either 2's and/or 1's, the corresponding cells are also marked by either 2's or 1's.
- 3) If a cell in the binary Veitch diagram can be either 1 or 0 (i.e., a corresponding minterm is redundant) the cell is marked by X . The cell is redundant in the ternary Veitch diagram only if it can be either 2 or 1 or 0; in this case, similarly, it will be marked by X (i.e., the cell can take any convenient truth value for the function simplification purposes). Any cell of the ternary Veitch diagram can assume only one

truth value or be redundant.

4) For any mechanized binary function, the existence and the non-existence of the output corresponds to the truth values 1 and 0 respectively. In the case of the ternary function, the existence of the output corresponds to either 2 or 1, and the non-existence of the output to 0. A function producing 2 or 1 output will be denoted by f_2 and f_1 respectively. If the truth table defining a function contains 2's and 1's, the total expression for the function will be $f = f_2 + f_1$.

Example:

Use the Veitch diagram for the minimization of the function defined by the truth table in the previous example.

p	q	f
1	1	1
1	2	1
2	1	1
2	2	2

	p	p'	p''
q	2	1	0
q'	1	1	0
q''	0	0	0

Inspecting the Veitch diagram one can see that the pattern is the same as of the matrix defining the ternary intersection. That is, $f = f_1 + f_2 = p \cdot q$.

To become proficient in ternary Veitch diagram techniques, one should first be able to recognize as many different ternary Veitch patterns as possible.

To translate a ternary Veitch diagram into a disjunctive form consisting of J minterms, proceed in the following manner:

- 1) If a pattern can be expressed in terms of *intersection*, *union*, and/or *cycling* connectives such that

$$\begin{aligned}
 f &= f(p, q, \dots, s) \\
 \text{then } f &= J_2[f(p, q, \dots, s)] + J_1[f(p, q, \dots, s)] \cdot 1
 \end{aligned}$$

Example:

	p	p'	p''
q	2	2	2
q'	2	1	1
q''	2	1	0

Since the Veitch diagram is of the function $f = p + q$, $f = J_2(p + q) + J_2(p + q) \cdot 1$

- 2) If the pattern of a function is not readily recognizable, combine 2's and 1's separately into the simplest expressions using the same technique as in the use of the binary Veitch diagrams. If $f_2 = J_2(p, q, \dots, s)$ and $f_1 = J_1(p, q, \dots, s)$ then $f = J_2[f_2(p, q, \dots, s)] + J_1[f_1(p, q, \dots, s)] \cdot 1$

Example:

	p	p'	p''
q	2	1	1
q'	2	0	0
q''	2	0	0

From this pattern, we get $f_2 = p$ and $f_1 = q(p' + p'')$, $f = J_2(p) + J_2[q(p' + p'')]$

$$2 + 1 = 2.$$

- 3) For expressing f_1 , consider any cell with 2 to be a redundant term since $2 + 1 = 2$.

$$\begin{array}{ccc}
 2 & 1 & 1 \\
 2 & 0 & 0 \\
 2 & 0 & 0
 \end{array} = \begin{array}{ccc}
 2 & 0 & 0 \\
 2 & 0 & 0 \\
 2 & 0 & 0
 \end{array} + \begin{array}{ccc}
 1 & 1 & 1 \\
 0 & 0 & 0 \\
 0 & 0 & 0
 \end{array}$$

Using this property for the above example,

$$\begin{aligned}
 f &= J_2(p) + J_2[q(p' + p'')] \cdot 1 \\
 &= J_2(p) + J_2(q) \cdot 1
 \end{aligned}$$

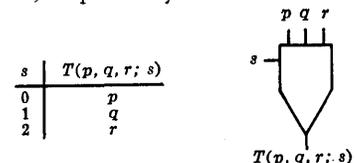
All the described methods of generating logic equations for the functions defined by truth tables can be used for any number of variables. The complexity of handling a higher number of variables does not appear to be greater than the equivalent problem in the binary logic. The fact that the number of different ternary logic functions is much greater than for the same number of binary logic functions does not make the ternary techniques proportionally more complicated.

The Ternary Conditioned-Disjunction

In computer manufacturing, it is more economical and convenient to use only one type of circuit as a basic logic element. For instance, in the present digital computers, to mechanize three basic logic connectives — *and*, *or*, and *not* — we use either *nor* or *nand* logic elements. All the ternary functions can be mechanized by a single logic element.¹ This basic element is a conditioned-disjunction. The notation symbol for the ternary conditioned-disjunction is

$$T(p, q, r; s)$$

and its functional definition can be stated as p, q , or r if $s = 0$, $s = 1$, or $s = 2$, respectively:



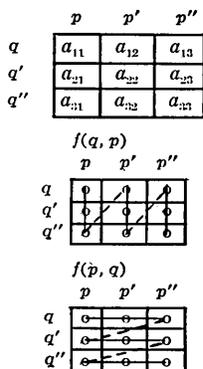
The general expression for the ternary function of n variables in terms of T operators is:

$f(p, q, r, \dots, s) = T[f(0, q, r, \dots, s), f(1, q, r, \dots, s), f(2, q, r, \dots, s); p]$
 where $f(0, q, r, \dots, s), f(1, q, r, \dots, s)$ and $f(2, q, r, \dots, s)$ are the ternary functions of $(n - 1)$ variables. This result follows directly from the Post algebra and the definition of the T operator.

A simple method has been developed for mechanizing ternary functions using T operators. To the author's knowledge, the method appears to be novel since no reference describing it had been found. The procedure is as follows:

- 1) Translate a truth table, defining a ternary function, into its equivalent Veitch diagram;
- 2) Write all the $n!$ possible equations in terms of T operators, where n is the number of variables; and
- 3) Select the equation of the minimal form.

For example, a general Veitch diagram for a ternary function with two variables is shown below:



The two forms of the function can be written: $f(q, p) = T[T(a_{33}, a_{23}, a_{13}; q), T(a_{32}, a_{22}, a_{12}; q), T(a_{31}, a_{21}, a_{11}; q); p]$

$f(p, q) = T[T(a_{33}, a_{32}, a_{31}; p), T(a_{23}, a_{22}, a_{21}; p), T(a_{13}, a_{12}, a_{11}; p); q]$

The above functions, in logic diagram form, are shown in Fig. 1.

As can be seen in the Veitch diagram and the determined equations, writing down the required equations is very simple. Starting from the right bottom corner of the Veitch diagram (i.e., from the minterm designated by the ternary zero) one may proceed either up or to the left producing $f(q, p)$ or $f(p, q)$, re-

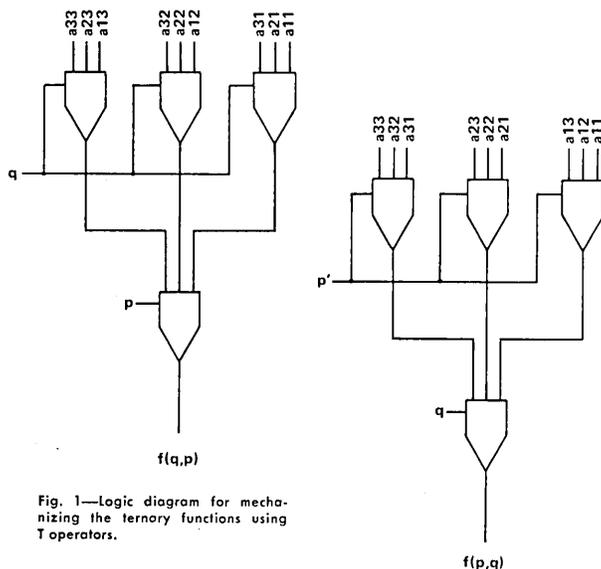


Fig. 1—Logic diagram for mechanizing the ternary functions using T operators.

spectively. Since $f(q, p) = f(p, q)$ the one of the simpler form is selected. With some experience in this technique, it will not be necessary to try all the possible solutions, since some Veitch diagram patterns suggest the factoring ways producing a minimal form.

Conclusions

Essentially, the system of the ternary logic is characterized by a rather close analogy to the systems of Boolean algebra, normally used for the case of the binary logic. One of the more outstanding differences is that in the ternary system the number of the different equations is considerably higher than the number of the binary equations for the same number of variables.

Also, the number of possible ternary operators is higher than the number of binary operators, but in both cases there are single operators which provide complete logic systems. As a whole, the difference between the two logics are predominantly of quantitative nature. After one becomes familiar with some fundamental principles of a multi-valued logic, the ternary logic does not create any conceptual difficulties. However the manipulation of the ternary logic is more complex than that of the binary logic, and probably will remain so regardless of what new switching algebra techniques are developed in the future.

The commonly accepted opinion that the number of components in a ternary computer will be smaller than that used in a binary computer

is based on considerations related to the storage of data by ternary elements. Therefore, the use of the ternary numerical system in digital computers would be justified only if both 3-state switching and memory elements were available. With the recent technological advances in various semiconductor devices, magnetic cores, and cryogenics, there are indications that the circuit design of simple and reliable ternary devices is feasible.

The author has completed the logic design of the following ternary functions: a tri-stable memory element ("tri-flop") for store, trigger, and shift-register applications, timing-pulse generators, comparators, adders, and data transfers between registers. A T operator was used as a basic switching element throughout the exercise for the application of the described ternary logic, and no unusual problems were encountered.

The same T operator can be used as either a 3-state or 2-state switching device, this property being controlled by truth-functional constants associated with T operators. It is an extremely useful property of T operators since some control signals should exhibit two states only.

Although an optimum mechanization of the ternary full-adder has not been achieved, the ternary adder compares very well with the binary adder (ten T -elements versus nine nor -elements). This is significant because the increase in range in changing from binary to ternary notation with the same number of digits, n , is $(3/2)^n$.

In selecting a numerical system, one should also consider the cost and speed of conversion to and from the decimal system. Any binary conversion algorithm can be modified for the ternary conversion and, in most of the cases, the execution of ternary conversion is faster.

There exists a ternary code, referred to as a symmetric code in this paper, which does not require the designations of algebraic signs. The full adder for this code is more expensive than the adder for the straight ternary (14 versus 9 elements). However, the arithmetic can be performed without sign logic or subtractive complementing and sign change correction.

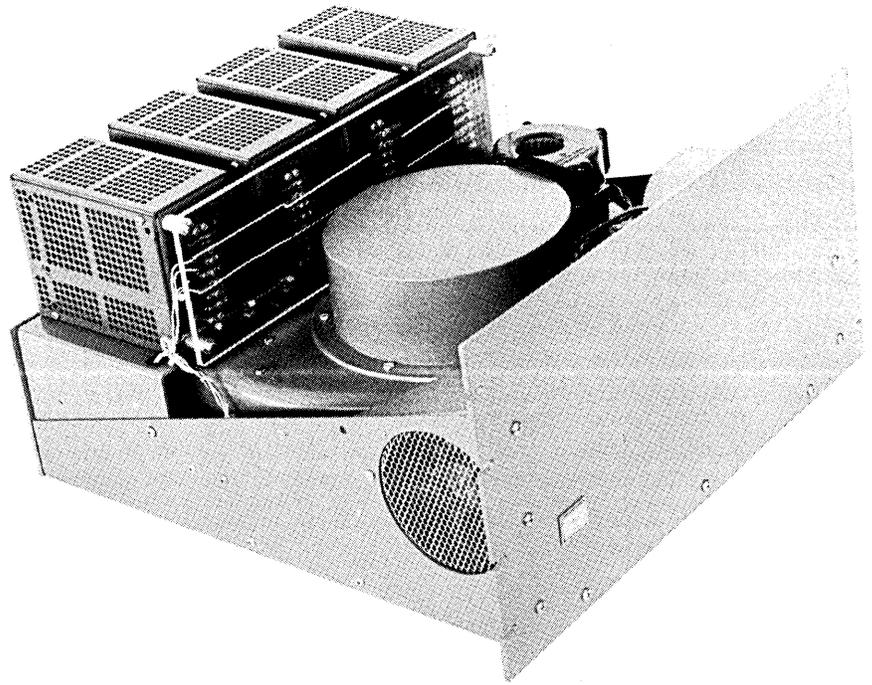
In recent years, many papers have been appearing on ternary logic. The subject is becoming of greater interest to the logicians recognizing many advantages of the system. It is still too early to speculate whether the computer industry will ever switch from binary to ternary logic. An extensive evaluation program is necessary to determine whether the use of the ternary system for digital computers would be justified economically.

Although an engineering team designing their first ternary computer today could have some problems, these would be considerably simpler than the problems encountered by the team designing the first electronic digital computer a mere 20 years ago.

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FLOW CHARTS METHODS

AL MacKINNON, Systems Non Linear

This article describes a method of designing the detailed logic of a digital system.

A flow chart is developed, which in its final form consists of blocks of Boolean Equations interconnected in flow-chart fashion. When completed, the flow chart provides a complete description of the system.

Advantages of this Method

The author has designed several systems using this approach, and would list the advantages as follows:

1. Keeps track of all the different sequences of operation, and ensures no hang-ups.
2. Minimizes redundancy by providing a "visual" representation of the logic.
3. Reduces the mental strain of trying to evaluate the results of undesirable conditions, etc.
4. For checkout. This can be done in an orderly fashion in the following stages:

- (a) each individual box
- (b) small loops
- (c) complete system

Checkout is complete when all the various paths have been successfully followed.

5. As a teaching aid. Since the flow chart is essentially a pictorial illustration of the operation of the system, with all relevant digital operations described in equation form, it provides a very convenient method of explaining the whole system.

Logic diagrams need only be referred to when it becomes necessary to know how a certain function has been mechanized. A logic drawing tends to be of value mainly for its mechanical content, i.e. the physical location of test points, etc., since fault diagnosis is accomplished by using the flow chart.

General Flow Chart Philosophy

The logic is broken down into boxes, such that any input to a box will activate the logic therein and produce a specific output. All operations within the box are described by a set of equations listed in the sequence in which they occur. A very simple example of this would be decoding a pulse count of 9 to set a flip-flop (Fig. 1).

The corresponding flow-chart would be Fig. 2.

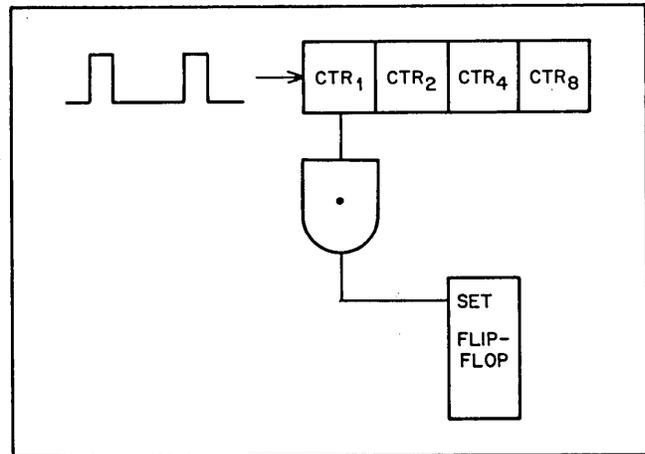


Fig. 1

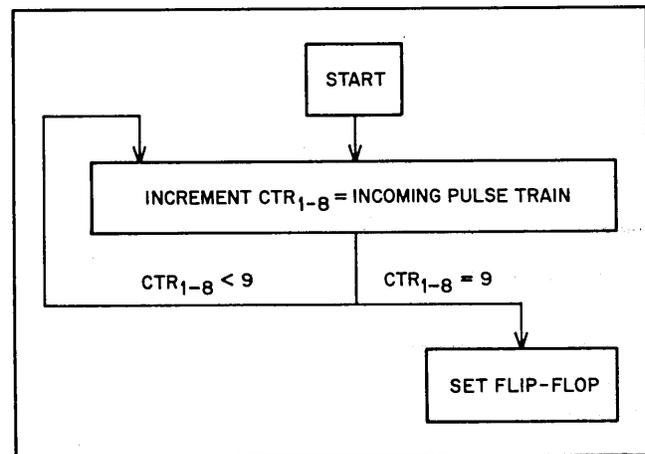


Fig. 2

Which is verbally explained:

Pulses are fed into the box, each pulse incrementing the counter by one count. After each pulse, we leave the box and examine the counter. If it is less than 9, we go into the box again where another pulse will arrive and increment the counter. This process is repeated until upon leaving the box to examine the count, we find the counter has reached 9. At this point, we set the flip-flop.

Mnemonics

In order to successfully transform a sentence or statement into an algebraic equation, some form of mnemonics must be employed. It is best to restrict the number of letters in a mnemonic to 4, and the mne-

OF LOGIC DESIGN

Design Engineer, Systems Inc.

monic should have a fairly close resemblance to the word it describes. Some examples are given below:

POP	Printer operable
CRB	Card reader busy
WEN	Write enable
CDO	Clock dropout
CMA ₀₋₇	Bits 0-7 of the core memory address
(SCT = 2)	The sector counter equals 2

Special Symbols

Additional notation to the Boolean Equations has been developed by the author:

1. δX means "the leading edge of X"
 $\bar{\delta X}$ means "the trailing edge of X"
 i.e. If X is a flip-flop, δX is when the flip-flop sets, and $\bar{\delta X}$ when it clears. If X is a level, δX is when the level goes true, and $\bar{\delta X}$ when it goes false.
2. Δ means "delayed by"
 Hence $\delta FFY \Delta 2 \mu S$ means "the leading edge of flip-flop Y delayed by 2 μS "
 $\bar{\delta FFY} \Delta 3 \mu S = SET FFY$ would read "the trailing edge of flip-flop X delayed by 3 μS sets flip-flop Y", or "flip-flop Y is set 3 μS after flip-flop X clears."

Example

A pulse train consisting of blocks of 14 pulses, each block separated by a gap, is provided. Three control lines, A, B, C are also provided. The states of ABC are independent of each other and the pulse train. Design logic to meet the following requirements:

- (1) If A is set when the 5th pulse arrives, and C is set when the 14th pulse arrives; generate pulse P1.
- (2) If A is not set when the 5th pulse arrives, and B is not set when the 12th pulse arrives, generate pulse P2.
- (3) If A is not set when the 5th pulse arrives, B is set when the 12th pulse arrives, and C is set when the 14th pulse arrives, generate pulse P1.

A dropout detector is available to detect the gap between blocks, and a counter is available to count the pulses.

Statements (1) (2) and (3) above can be put into flow chart form (see Fig. 3). This flow chart was derived in the following fashion:

- (1) The 1st count of significance is 5, so the counter must be allowed to reach this count. (Box 1)

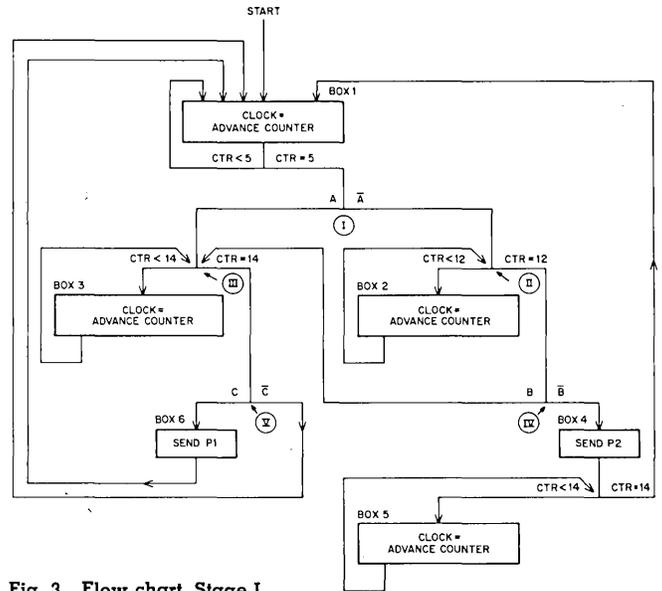


Fig. 3. Flow chart, Stage I.

- (2) The only condition of interest at count 5 is whether A is set or not.
- (3) This brings us to i where a path is provided for A and \bar{A} .
- (4) The next count of significance is 12.
- (5) We are only interested in count 12 if A was not set at count 5.
- (6) This brings us to ii; note that a path has been provided for the counts between 6 and 12. (Box 2.)
- (7) When count 12 arrives, we want to know whether B is set or not iv
- (8) If B is not set, P2 is generated. (Box 4.)
- (9) If B is set, in order to fulfill statement (3), we must go to iii to await count 14.
- (10) P2 was generated on count 12, so two more pulses have to be accounted for. This is done by box 5.
- (11) When count 14 is finally established, iii, we want to know if C is set, so a branch is drawn for C and \bar{C} (point v
- (12) If C is set, P1 is generated. (Box 6.)
- (13) If C is not set, nothing happens, and since this is the last pulse of the block, we go back to box 1 to await the 1st pulse of the next block.

This completes the 1st stage of the flow chart.

The next step is to determine at which points memory elements have to be inserted so that we can tell which particular path has been followed.

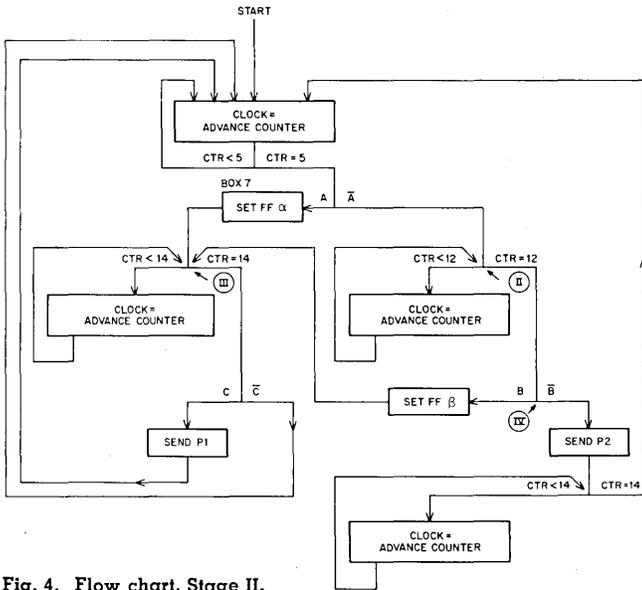


Fig. 4. Flow chart, Stage II.

At *iii*, we must remember whether we have *A* or \bar{A} at count 5. It is a matter of choice whether we set $FF\alpha$ (see Fig. 4) with *A* or \bar{A} at count 5.

We must also remember whether we had *B* or \bar{B} at *iv*, so $FF\beta$ is provided, which will be set by *B* and count 12.

There is no need to provide a flip-flop at *v* since there are no more path options provided after this point.

The addition of $FF\alpha$ and $FF\beta$ complete stage II of the flow chart (Fig. 4).

The next step is to examine these memory elements just added, to see if they can be combined. If their outputs lead us to the same point, they can. This is true in the case of $FF\alpha$ and $FF\beta$, since they both go to *iii*. This makes one of them redundant, so we will remove $FF\beta$ and connect *iv* to the input of box 7. This completes stage III of the flow chart, as shown on Fig. 5.

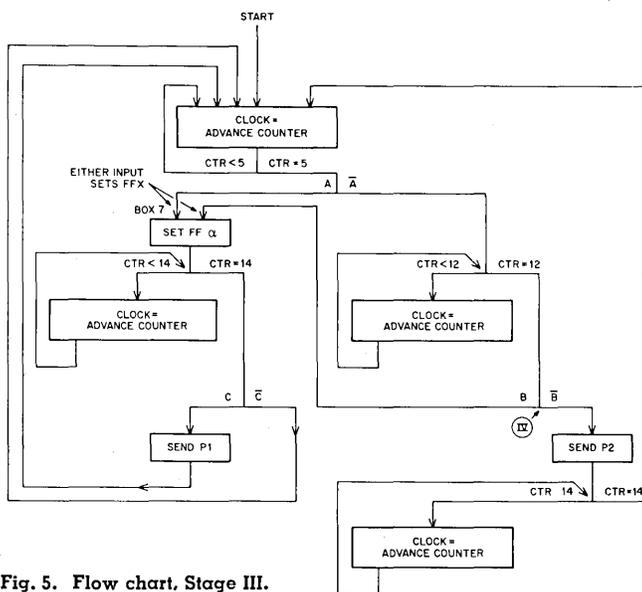


Fig. 5. Flow chart, Stage III.

Note that it is always possible to get back to the beginning from any point in the flow chart. This ensures that no matter what condition occurs, there will be no "hang-ups".

The next step is to replace the words in stage III by equations thus producing stage IV (Fig. 6). Now we are ready to derive equations for

- (a) Advance counter
- (b) Set $FF\alpha$
- (c) Send *P1*
- (d) Send *P2*

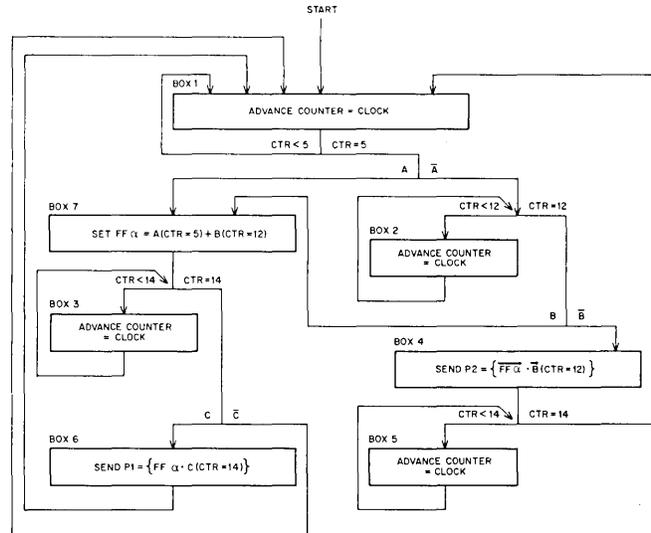


Fig. 6. Flow chart, Stage IV.

- (a) From boxes 1, 2, 3 and 5, we deduce the equation:
Advance counter = clock
- (b) From box 7,
set $FF\alpha = A(CTR = 5) + B(CTR = 12)$
- (c) From box 6,
send $P1 = FF\alpha \cdot C(CTR = 14)$
- (d) From box 4,
send $P2 = FF\alpha \cdot \bar{B}(CTR = 12)$

Now we must ensure that all FFs that get set are subsequently reset. In this example, this would apply to the counter and $FF\alpha$.

Counter

Assuming a 4 stage binary counter, some method must be devised to reset it after 14 counts. Can we use anything occurring in the flow chart? *P1* may not neces-

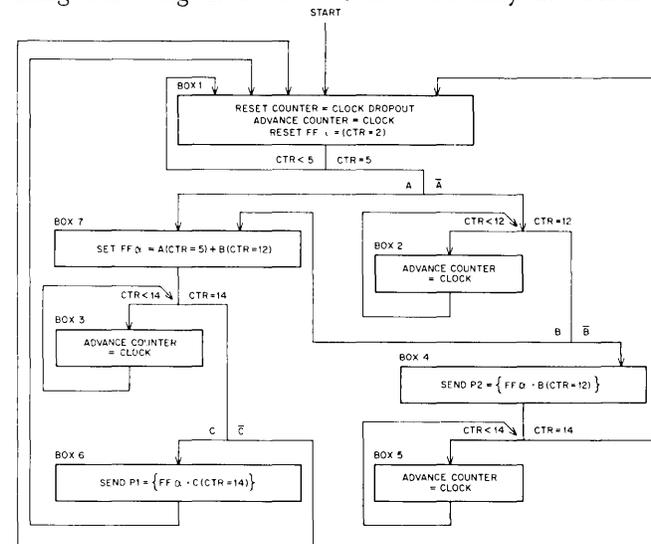


Fig. 7. Flow chart, Stage V.

TIME-SHARING SYSTEM SCORECARD

A SURVEY OF ON-LINE MULTIPLE USER COMPUTER SYSTEMS

This guide is prepared and published periodically by Computer Research Corporation of Newton, Mass. to keep computer users abreast of the rapidly increasing number of time-shared computer systems which, as the publishers say, are bringing man and machine together in close partnership for the pursuit of intellectual and administrative activities. The text and charts are reproduced here with permission of Computer Research Corporation because of the wide interest of Computer Design readers in time shared computer systems.

By glancing at the following charts the reader can judge for himself the progress being made in this new and dynamic field. There are several different definitions of time-sharing. No single definition is adequate for all purposes. The authors have limited this survey to systems that have at least two independent, remote and simultaneously operable consoles (from the user's point of view). If the language capabilities of the system are extensive and general so that a user can create new languages while working on-line, the system has been denoted as a general purpose time-sharing system. Where the language capabilities are more restrictive, permitting the user to work in only one specific problem area, the term special purpose time-sharing system has been used.

The number of commercial and research time-sharing systems has grown so rapidly in the past several months that it is no longer feasible to list each individual system. Therefore, only the first or major occurrences of any time-sharing system that operates on a particular type of computer have been listed.

Information concerning the number of users that can be handled by any particular time-sharing system has been supplied by the organization involved. In some cases the numbers may be unduly optimistic but the data is presented as supplied.

Recent Developments

The continued growth of commercial time-sharing is perhaps the most striking feature in this edition of the scorecard. Almost every major city in the country now has local access to at least one time-sharing service. Most organizations that now offer service are expanding geographically and several new companies are entering the scene. In addition, specialized time-sharing services are beginning to emerge such as the financial analysis service by White, Weld & Co. which will be built upon an SDS 940. Meanwhile, General Electric's MEDINET division has started to offer time-shared service to some hospitals in Massachusetts and New York on an experimental basis.

It is interesting to observe the almost universal slippage in the development of the newer time-sharing systems. Project MAC which expected to be in normal operation with a time-shared GE 645 in June of 67 now estimates that it will be operational in the summer of 68. Performance of the IBM 360/67 has also been disappointing, and some organizations that originally hoped to be operational by this time have declined to make any further predictions as to when their time-sharing capability will be fully realized. The SDS 940 which was reported as a fully operational 32 user system some time ago has also been beset by software problems. SDS now estimates a 32 user capability in March of 1968.

New machines that have been announced with a time-sharing capability include the Digital Equipment Corp. PDP-10, the RCA 70/46 and the Burroughs 5500.

The information reported in this survey is believed to be accurate and was prepared as a public service. Many of the systems described are still being modified and consequently their characteristics may change from time to time. Computer Research Corporation cannot be held responsible for any errors or omissions. Readers desiring more detailed information about a particular system should write directly to the organization listed. This survey may not be reproduced in whole or in part for any purpose without the written consent of Computer Research Corporation.

RESEARCH ORIENTED TIME-SHARING SYSTEMS

Prepared by COMPUTER RESEARCH CORPORATION

ORGANIZATION	STATUS	TYPE	COMPUTER(S)	LANGUAGE(S)	TERMINALS	MAIN STORAGE	SECONDARY STORAGE	NO. OF USERS	REMARKS
Bell Telephone Laboratories ¹ Murray Hill, New Jersey	D (1/68)	G	GE-645 ²	FORTRAN IV, COBOL, PL/1, SNOBOL	TT-37 IBM 1050 CRT (10)	256K	DK (40M Wds.) DR (4M Wds.) Tape Loop (100M Wds.)	100	Highly interactive system for research and production computing.
Bolt Beranek and Newman Inc. ³ Cambridge, Mass.	O (6/64)	G	PDP-1D ⁴	MIDAS, TELCOMP ⁵	TT-33 (90)	24K (4K)	DR (128K Wds.) DR (2 units, 25M Wds. each) MT (2 units)	64	Medical information and communications system for hospitals. Also used for computational and data management facility.
C. S. I. R. O. Canberra City, Australia	O (7/66)	G	CDC 3600	CIDER, INTERP, STATIST, 3600 FORTRAN, COMPASS	CDC 210 (6) CDC 250	32K (2K)	DR (2 units, .5M Wds. each unit) DK (12.5M Wds.) MT (8)	7	General purpose scientific computations.
Dartmouth College ⁶ Kiewit Computation Center Hanover, N. H.	O (9/67)	G	GE-635 DATANET-30 (4)	BASIC, ALGOL-35 (1/68) FORTRAN (1/68)	TT-35 (55)	64K (24K)	DR (768K Wds.) DK (2 units, 4M Wds.) MT (6 units)	200	Datanet-30's have 16K core memory each. Educational and research use.
Edinburgh University Department of Machine Intelligence and Perception Edinburgh, Scotland	O (6/67)	G	Elliot 4120	POP-2	TT (20)	32K (16K)		8	POP-2 language suitable for list processing and numerical computation using FORTRAN type statements.
General Electric Research & Development Center Schenectady, New York	O (7/66)	G	GE-265	BASIC, ALGOL, FORTRAN, LISP and others	TT (45) CRT (3)	16K (6K)	DK (20M Char.) MT (6 units)	21 (TT) 3 (CRT)	Uses include: scientific programming, data acquisition from experiments, system programming development.
Lawrence Radiation Laboratory University of California Livermore, California	Partial O (7/67) Complete D (6/68)	G	PDP-6 (2) CDC 7600 CDC 6600 (3) CDC 3600 IBM-7030 IBM-7094 (2)	FORTRAN, LISP, Assembly Languages	TT (200) PLT (10)	256K ⁶ Words	DK (8 x 10 ⁸ bits) DC (3.2 x 10 ⁹ bits) Photo-Digital Store (1 x 10 ¹² bits)		Use is mostly scientific computation.
Lincoln Laboratory — MIT Lexington, Mass.	O (2/66)	G	TX-2	CORAL, VITAL, MARK 5, LABGOL	TY (5), CRT (4), RAND TABLET, PDP-338 Remote Terminal	105K	DR (20M Wds.)	6	System features fast response time for on-line graphical communication.
Lincoln Laboratory — MIT Lexington, Mass.	O (9/67)	G	IBM 360/67	MACRO Assembler FORTRAN IV	IBM 2741 (30)	128K	DR (1M Wds.) DK (56M Wds.)	20	Establishment of a large computational facility for scientific and engineering research.
Lockheed Georgia Co. Marietta, Georgia	O (7/65)	G	IBM 360/50	FORTRAN IV	IBM 1050 (36) IBM 2200 (6)	64K (20K)	DK (6.45M Char.)	42	System named RAX, developed from earlier 360/40 system, used mostly for engineering.
Lockheed Palo Alto Research Laboratories Palo Alto, California	O (12/66)	S	IBM 360/30	360 Assembly Language (7/68)	IBM 2260 (4) Sanders 720	64K Bytes	DK (2 Units, 2.75 M Bytes each) DC (418M Bytes) MT (1 Dual)	12	System named LACONIQ. Information retrieval and updating, research.
MIT Dept. of Civil Eng. Cambridge, Mass.	D (6/68)	S	IBM 360/40	COGO, STRUDL, ICETRAN	IBM 2741 (5)	128K Bytes	DK (2)	10	System named ICES. Uses include Engineering, Science, Management.
MIT Dept. of Electrical Eng. Cambridge, Mass.	O (5/63)	G	PDP-1.	Macro Assembler	TY (5)	12K (8K)	DR (88K Wds.) ⁷ MT (6 Units) ⁸	5	Experimental time-sharing system for student use in thesis and research projects.
National Bureau of Standards Washington, D.C.	O (4/66)	G	MOBIDIC B ²	DESCAL CL6, CAS, EDIT	TT-33, 35 (4) CRT	16K (6K)	DK (1M Wds.) MT (4 Units)	6	Uses include research in the design of on-line systems and terminals.
Northern Electric Co., Ltd. Research & Development Laboratories Ottawa, Ontario, Canada	O	G	CDC 3300 (2)	FORTRAN, PL/1, COBOL, COMPASS	TT (70) 8130 (4)	82K 65K (4K)	DK (12 Units, 8.2 M Char. each) MT (10 Units)	35	Scientific and Business use.
Ohio State University Columbus, Ohio	D (9/68)	G	IBM 360/50 IBM 360/75	PL/1, FORTRAN IV	IBM 2741 (20) IBM 2260 (8)	512K Bytes 1024K Bytes	DR (1 Unit) DK (1 Unit)	14	
Perkin Elmer Corp. Norwalk, Conn.	O (10/67)	G	SDS-9300 SDS-930	SPEED (Text Editor), FORTRAN IV, META-Symbol, SLIP (12/67)	TT-33, 35 BR IBM 2741 IBM 1050	32K 16K (22K)	DK (67M Char. 1/68) MT (4 Units) DR (4 Units, 8M Char.)	16	Uses include lens design, circuit analysis, scientific engineering and research.
Project MAC — MIT (Phase One) Cambridge, Mass.	O (10/63) ⁹	G	IBM-7094	ALGOL ¹⁰ FORTRAN, MAD, LISP	TT-35 (54) IBM 1050 (56) TLX (1) CRT (2)	64K (32K)	DK (36M Wds.) DR (.5M Wds.) MT (12 Units)	30	Project MAC is an MIT research program sponsored by the Advanced Research Projects Agency (ARPA), D.O.D., under a contract with the Office of Naval Research.

RESEARCH ORIENTED TIME-SHARING SYSTEMS

Prepared by COMPUTER RESEARCH CORPORATION

ORGANIZATION	STATUS	TYPE	COMPUTER(S)	LANGUAGE(S)	TERMINALS	MAIN STORAGE	SECONDARY STORAGE	NO. OF USERS	REMARKS
Project MAC — MIT (Phase Two) Cambridge, Mass.	D (1/68)	G	GE-645 ²	ALGOL, ¹¹ COBOL, FORTRAN IV, PL/I	TT-37 IBM 2741	256K	DK (40M Wds.) DR (4M Wds.) MT (8 Units)	100	Initial limited system operation by early '68. Prototype system by summer of '68 with continual development thereafter.
Purdue University Computer Science Department Lafayette, Indiana	O (9/67)	G	IBM-7094	File Generation, TEXT-90 (12/67), FORTRAN	TT-33 (2) IBM 1052 (2)	32K (16K)	DK (9 Megawords) MT (9 Units)	4	System named PTSS.
RAND Corporation Santa Monica, California	O (11/65)	G	PDP-6	JOSS II	TY (30) ¹²	32K	DK (6M Wds.) DR (1M Wds.)	30	Interpretive system with compact conversational language for small numerical problems.
Stanford University Stanford, California	O (8/64)	G	PDP-1	Assembly Language	PHILCO CRT TT-33, 35	32K (12K)	DR (131K Wds.) DK MT (2 Units)	100	An IBM 360/67 will be operational in 1968.
System Development Corp. Santa Monica, California	O (1/64)	G	AN/FSQ-32 PDP-1	TINT, IPL-TS, JOVIAL, LISP	TT-33, 35 TY, CRT, TLX IBM 1052	65K (47K) 16K Buffer	DR (5 Units, 139K Wds. each) DK (1 Unit, 4M Wds.) ¹³ MT (12 Units)	30	Oriented to command and control experimentation and other general uses.
TRW Systems Group Redondo Beach, California	O (1/65)	S	Bunker-Ramo 340	Culler-Fried System for Mathematical Analysis	4 Consoles ¹⁴ BBN Console	16K	DR (48K Wds.) MT (2 Units)	4	Highly flexible system for on-line manipulation, specification and execution of mathematical and symbolic operations with graphical display of results.
U.C.L.A. Western Data Processing Center Los Angeles, California	O (11/64)	G	IBM-7740 ¹⁵ IBM-7040/ 7094		IBM 1050 (12)	32K	DK DR	12	Jointly financed by UCLA and IBM, system services UCLA and 88 other California schools.
United States Military Academy West Point, New York	O (12/65)	G	GE-225 (3) DATANET 30	CADETRAN ¹⁶	TT (15)	8K 16K (6K)	DK (18M Char.) MT (6 Units)	15	
University of California Irvine, California	O (1/66)	G	IBM 1410 IBM 1440	JOSS ⁵ Coursewriter	IBM 1050 (18)	100K Characters	DK MT (5 Units)		Uses include computer-assisted instruction and the administration of student enrollment.
University of California Irvine, California	D (1/68)	G	IBM 360/50	ISIS CAL	IBM 2741 (28) IBM 2260 (3)	512K Bytes (8K Bytes)	DK (12 Units 7.25 M Bytes each) MT (4 Units)		Instruction, Administration and Research.
University of California Project GENIE Berkeley, California	O (4/65)	G	SDS-930	FORTRAN II, ALGOL, LISP, SNOBOL, CAL, DDT, QED, ARPAS, QSPL	TT-33 (8) TT-35 (8) CRT (2) DATAPHONE (6)	48K (38K)	DR (1.3M Wds.) MT (2 Units) DK (144M Wds.)	16	Features hardware address mapping. The SDS 940 system is based on the results of this ARPA sponsored project.
University of California Santa Barbara, California	D (1/67)	G	IBM 360/50	Culler-Fried System, FORTRAN IV	20 Consoles ¹⁴ RAND TABLET IBM 1050 (3)	64K	4 DK (1.8M Wds.) DR (1M Wds.) Core (.5M Wds.)	16	Extension of the Culler-Fried system now operating on the RW400. The 360/50 system has simultaneous background processing.
University of Illinois Urbana, Illinois	O (1/66)	G	ILLIAC II PDP-7	FORTRAN	TT-33, 35 (8) CRT	8K (6K)	DK (10M Wds.) DR (64K Wds.)	7	Experimental time-sharing system for general university research.
University of Massachusetts Amherst, Mass.	O (9/67)	G	CDC 3600 PDP-8/680	BASIC, SNOBOL, COGO, SMALL, FORTRAN IV	TT-33, 35	32K (8K)	DR (2 Units, 2M Char. each) DK (2 Units, 8M Char each) MT (4 Units)	32 ¹⁷	Uses include education and varied research programs in diverse fields.
University of Pennsylvania Philadelphia, Penn.	O (6/65)	G	IBM-7040 PDP-8	FORTRAN, MULTI-LANG, MAP, ALGOL, LISP, SNOBOL	TT-35 (4) BR (2)	32K (24K)	DK MT (6 Units)	6	Uses include information retrieval, research, and multiprogramming experimentation.
University of Pittsburgh Computer Center Pittsburgh, Penn.	O (3/66)	G	IBM 360/50	ALGOL, PIL, ¹⁸ FORTRAN IV, PL/I (1/68), Assembler	IBM 1050 (3) IBM 2741 (20)	128K Bytes, 1M Bytes LCS (32K Bytes)	DK (2 Units, 7.5M Bytes)	24	General University research and education. Online LINC-8 for medical research available in late 1967.
University of Utah Salt Lake City, Utah	D (12/67)	G	UNIVAC 1108	FORTRAN V, TRAC, COBOL, ALGOL	TT-35 (20)	131K (65K)	DR (6 Units, 1.5M Wds.) MT (8 Units) FASTRAND II	20	Plans include the addition of more displays and bulk core memory.

NOTES

- Development in cooperation with Project MAC, Massachusetts Institute of Technology.
- Multiple processor time-sharing system.
- Developed with the Massachusetts General Hospital under contract from the National Institutes of Health.
- Based upon an earlier S-station PDP-1 System operational 9/62.
- Based on the RAND JOSS language.
- The 256K core storage applies only to the PDP 6's.
- To be replaced by a larger model early in 1968.
- Units have been installed but are not operational.
- Initially time-shared in 1961 at the M.I.T. Computation Center.
- Other languages include FAP, SLIP, COGO, SNOBOL, STRESS, GPSS, COMIT, CPL-1 and QPS-3.
- Most Project MAC Phase I languages will be implemented later.
- Selectric with JOSS keyboard and paging.
- Additional unit available in January of 1968.
- Each console consists of two keyboards and a storage tube display.
- System currently utilizes five computers in addition to central 7740.
- Cadeltran is an extended teaching dialect of FORTRAN.
- 64 with added communications ports.
- Based on the RAND JOSS language.

COMMERCIAL TIME-SHARING SYSTEMS

Users can purchase remote, on-line and interactive computer services from the organizations listed below.

ORGANIZATION	COMPUTER	CONVERSATIONAL LANGUAGES	TERMINALS	NO. OF * USERS	MINIMUM CHARGE PER MONTH	AVG. CHARGE PER TERMINAL HR.	CHARGE PER MIN. OF CPU TIME	DISC § STORAGE/CUSTOMER
Allen-Babcock Computing, Inc. Palo Alto, California	IBM 360/50 ¹	PL/1 (on-line subset)	IBM 2741 TT-33, 35, 37 Friden 7100 IBM 1050	90	\$385.00	None	\$5-\$10 ²	100K+
Applied Logic Corp. Princeton, New Jersey	DEC PDP-6, PDP-10 (12/67) ³	FORTRAN IV DDT, JOSS MACRO-10 Compact COBOL LISP, SNOBOL-6	TT-33, 35 CRT	30 ⁴	None	\$5.00	\$6.00	0+
Bolt Beranek and Newman Inc. ⁵ Cambridge, Mass.	PDP-7/8	TELCOMP	TT-33	⁶	None	\$12.50	None	None
CEIR Inc. Arlington, Virginia	GE-235 DATANET-30	BASIC ALGOL	TT-33, 35	40	\$250.00	\$6.00	None	120K
Computer Sharing Inc. Bala Cynwyd, Pennsylvania	SDS 940	CAL, ARPAS, BASIC, DDT, FORTRAN IV, FORTRAN II	TT-33, 35	32	None	\$30 ⁷	None	60K+
COM-SHARE Inc. Ann Arbor, Michigan	SDS 940	BASIC, CAL, FORTRAN IV, SNOBOL, TAP, DDT, FORTRAN II	TT-33, 35	64	\$100.00	\$10-\$20	\$2.50	0+
DIAL-DATA, Inc. Newton, Mass.	SDS 940	CAL, DDT, QED, FORTRAN II, BASIC, ALGOL, FORTRAN IV, SNOBOL, ARPAS	TT-33, 35	32	\$100.00	\$13.50	\$3.00	60K+
General Electric Co. ⁸ Information Service Dept. Bethesda, Md.	GE-235 DATANET-30	BASIC, ALGOL, FORTRAN	TT-33, 35 PLT	40	\$100.00	\$10.00	\$2.40	0+
International Business Machines ⁹ New York City	IBM 7044	QUIKTRAN	IBM 1050 IBM 2741	80	\$125.00	\$12.50 ¹⁰	None	0+
Intinco Limited London, England	UNIVAC 418 (2)	Stockbrokers Language	TT-33 (60)	60	11	11	11	
KEYDATA Corp. (Adams Assoc.) Cambridge, Mass.	UNIVAC 491	KOP III	TT-28	200	12	12	12	
Pillsbury Occidental Company ¹³ Raleigh, North Carolina	GE-265	ALGOL, BASIC, FORTRAN	TT-33, 35 PLT, CRT	40	\$108.50	\$10.00	\$3.00	0+
REALTIME Systems Inc. New York, New York	B-5500	FORTRAN IV, COBOL, ALGOL	TT, TLX, TWX, CRT	15	\$500.00	\$15.00	\$8.35	0+
TYMSHARE Inc. Los Altos, California	SDS 940	CAL, BASIC, QED, DDT, FORTRAN IV, ARPAS, ALGOL	TT-33, 35 PLT	60	\$80.00 or \$390.00	\$13-\$16	None	60K+
VIP Systems Corp. Washington, D.C.	IBM 1440	IBM Administrative Terminal System	IBM 2741	40	\$375.00	\$7.50	None	100K+

* In all cases the number of simultaneous users can be increased by addition of equipment or by duplicating the computer system.

§ Number denotes amount allocated in characters or bytes, + indicates more available at extra charge.

NOTES

- Special operation codes for efficient conversational interaction added.
- Dependent on amount of core used.
- This new system will be in operation early in 1968.
- Will be increased to 40 in late January.
- Systems located in Cambridge, Massachusetts, East Orange, New Jersey, and London, England.
- Cambridge and East Orange handle 32, London handles 16.
- For first 20 hours, \$25/hour thereafter.

- Service available from offices located in 33 major metropolitan areas.
- Other systems in Chicago, Cleveland, Philadelphia, Los Angeles, and Toronto.
- For first 5 hours, \$11 for hours 6 thru 75. \$9 thereafter.
- A charge of approximately \$5,000 per year plus a usage charge of \$.05 per inquiry.
- For accounting and management uses. Charges on basis of message transmissions, processor time and storage used.
- Trade name Call-A-Computer.

CHARACTERISTICS LISTED IN CHARTS

STATUS

O-operational system, number in parentheses denotes the approximate date that the system went on the air. D-system under development with anticipated date that operations will begin.

TYPE

G-general purpose, S-special purpose.

COMPUTER

manufacturer's name and number of central computers in system.

LANGUAGES

basic languages available on system at present.

TERMINALS

type of terminal equipment available, number of such terminals in parentheses. Code: TT followed by number denotes TELETYPE terminals and model number, TY-typewriter, TLX-Telex console, CRT-cathode ray tube display, BR-Bunker Ramo series 200 display consoles, IBM 1050, 2741-keyboard consoles, IBM 2250, 2260, PHILCO-display consoles, PLT-Plotter.

MAIN STORAGE

first number denotes total core storage in words on system, second number in parentheses, if given, denotes maximum core storage available to an individual user.

SECONDARY STORAGE

DR-magnetic drum, DK-disk file, DC-data cell, MT-magnetic tape, CORE-bulk core, CF-random access card file (K = 1024, M = 1,000,000 wds. per unit).

NO. OF USERS

maximum number of users who can operate simultaneously at any given time.



NEW PRODUCTS

will permit use of relatively inexpensive general-purpose computers at one-tenth the initial cost of the complex central processing equipment now required in high-speed data acquisition systems. Stellarmetrics, Inc., Santa Barbara, Calif.

Circle No. 201 on Inquiry Card

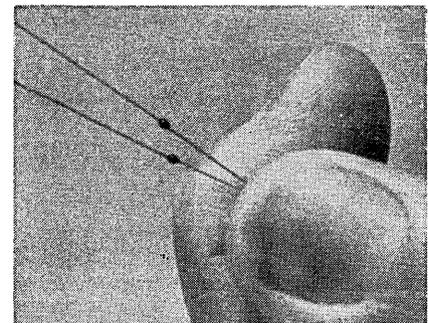
MAGNETIC TAPE

Digital magnetic computer tape, which can be used in extremes of hot or cold temperatures from -55 to $+180^{\circ}\text{F}$, permits extended use of computers in aviation, aerospace, and other applications where it is not feasible to control environmental conditions. Rapid fluctuations between temperature extremes, as might be encountered by a jet interceptor rising quickly to the stratosphere from a jungle airstrip, have no adverse effects on X-N tape performance, according to the manufacturer. It is also not affected by humidity extremes. Wabash Magnetics, Wabash, Indiana.

Circle No. 202 on Inquiry Card

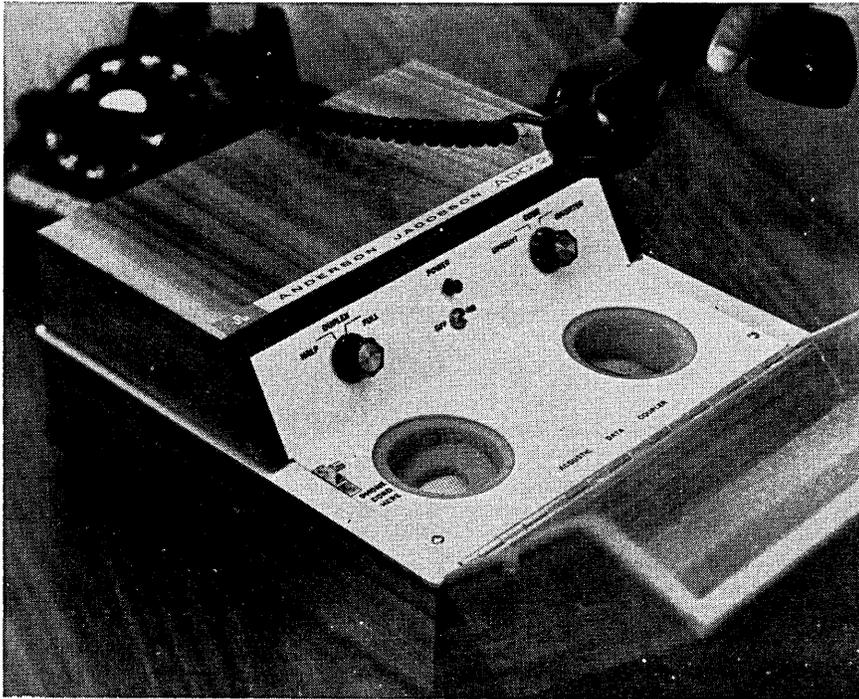
FAST SWITCHING DIODES

As many as six individual, matched silicon junctions are stacked and packaged in a micro epoxy form for switching applications up to 6,000 working volts in the new Micro-Codistor II line of diodes. Switching speeds range as low as 50 nanoseconds for conditions of 10 milliamps,



100 ohms. Applications of these diodes can be extended into the megahertz range. Five separate units measuring only 0.075 " diameter and 0.125 " long, are offered ranging from working inverse voltage (WIV) ratings of 2000 volts to 6000 volts in 1000 volt steps. Peak surge current (8 msec.) varies from 9 amps to 3.5 amps. Computer Diode Corp., Fair Lawn, N.J.

Circle No. 203 on Inquiry Card



PORTABLE DATA COUPLER

A device for sending and receiving data between a remote terminal and a time-shared computer using any ordinary telephone has been developed which can be used typically with a model 33 or 35 Teletype but can be used interchangeably with EIA RS-232 specification interface teleprinters that can operate with a 103A Dataphone. This includes the Friden 7100, Datel Thirty-10, IBM 2741, and various card readers.

The teleprinter-coupler combination provides a remote computer terminal which can be moved from one place to another wherever an ordinary telephone is available. Thus, access to a computer can be from one's own office or home, and there is no need to be constrained to a fixed location. Called the ADC 260, the coupler is designed to handle a bit rate of approximately 300 Baud. It is used at a 110 Baud rate when used with a Model 33 or 35 Teletype. No special interface in the

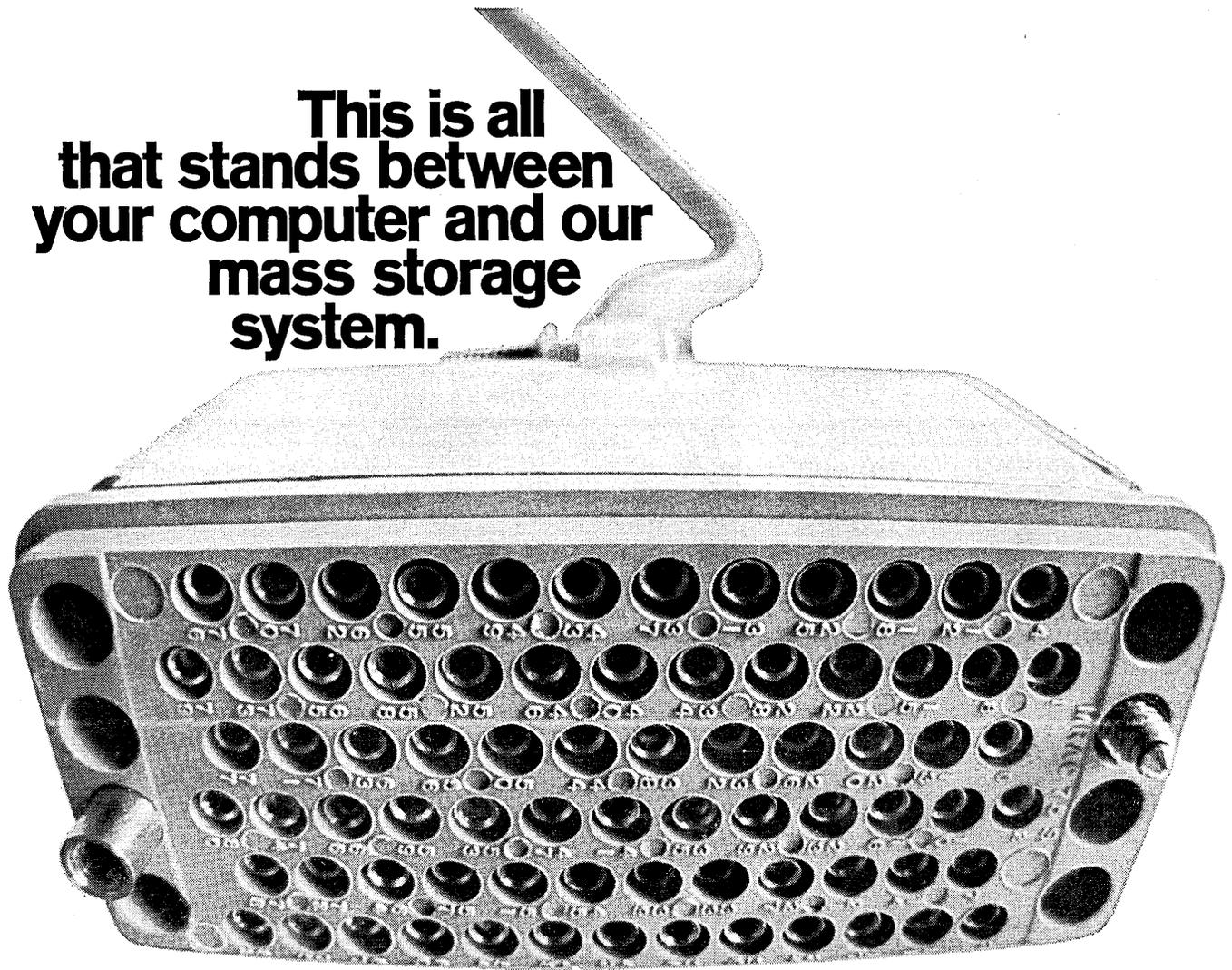
Teletype is required except to install a connection cable which is included. EIA Specification terminals plug in directly. Price is \$570.00. Anderson Jacobson, Inc., Mountain View, California.

Circle No. 200 on Inquiry Card

DATA COMPRESSOR

A data compressor that could cut the computer costs of data acquisition systems by 90 percent has been designed to take the output from high-speed analog-to-digital converters at data rates up to 100 KHZ. The device scans all information channels, but forwards only data that has changed between data samples. Meaningless or redundant data is bypassed, significantly reducing the amount of information fed into the central processor. Read-out is in digital words that can easily be computer-translated into numerical form. Capabilities of the data compressor

**This is all
that stands between
your computer and our
mass storage
system.**

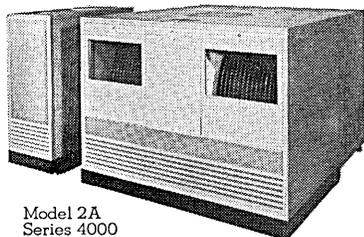


One lowly plug turns the Bryant XLO-1000 Controller into a universal memory system—for any computer, new or already in use. Simple? Even more so, when you add a comprehensive software package that includes handler and maintenance routines.

The auxiliary system is fast and economical too. Designed to operate in several different modes—serial and parallel—it features word transfer rates from 50 microseconds to 900 nanoseconds per word. To and from two computer central processors.

And up to eight data storage devices can be operated from one Controller. You can improve your memory—as your needs grow—from 8 million to 5 billion characters.

Simplicity, economy, speed and flexibility. All funnelled through a plug. It's enough to make a "Bryant Believer" out of anybody. Give us a chance. Write Ex-Cell-O Corp., Bryant Computer Products, 850 Ladd Rd., Walled Lake, Michigan 48088.

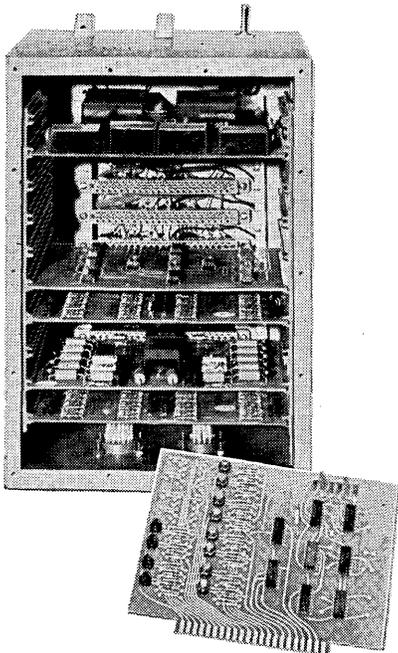


Model 2A
Series 4000
plug-in Disc File System.

**BRYANT
COMPUTER PRODUCTS**

EX-CELL-O CORPORATION

NEW!



VERNITRON Solid-state Digital to Two- Speed Resolver Converter

Already in use on
"HYBRID SERVO SYSTEMS"
to simulate a resolver
transformer

Input of this remarkable unit is 16 bit binary digital data (angle θ) and resolver transmitter data (angle ϕ). This input data is converted to two-speed resolver transformer data; sine ($\phi - \theta$) and sine ($8\phi - 8\theta$).

Input logic levels

Binary "1" = 4 VDC
Binary "0" = 0 VDC
Conversion time, less than 10 microseconds
Accuracy: 1 minute; 30 sec. available
Temperature: 0°C to +70°C. Extended temperature ranges available
DC Power required:
+ 15VDC at 500 ma
- 15VDC at 500 ma

Standard package size

Height: 5.5"; Width: 7.0"; Length: 9.75"

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FULL-SPECIFICATION BULLETIN

THE QUALITY NAME IN
DIGITAL DEVICES

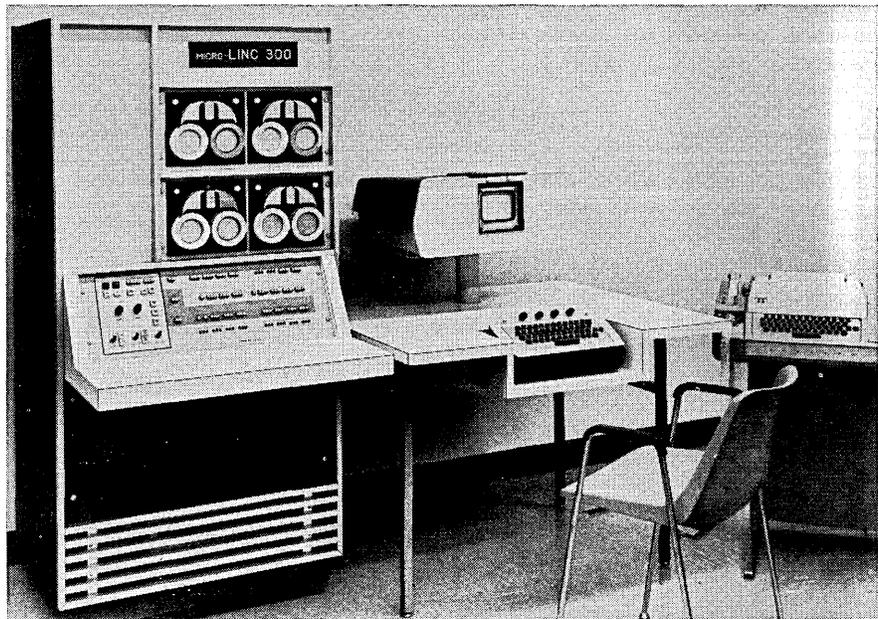


DIGITAL PRODUCTS DIVISION:
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(516) 694-5002 • TWX: 510-224-6890

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ENCODERS, SOLID STATE CONVERTERS,
SYNCHRO-TO-DIGITAL, DIGITAL-TO-SYNCHRO,
AND DIGITAL-TO-RESOLVER CONVERTERS

CIRCLE NO. 45 ON INQUIRY CARD



LABORATORY COMPUTER

The Micro-LINC-300, a sophisticated version of the original LINC computer developed first at M.I.T. and later at Washington University, is said to offer many new features, the most significant being buffered tape, which permits parallel processing while tape instructions are being carried out. A RAM (Rapid Access to Memory) feature has been added which, in conjunction with buffered tape, permits data logging at a 6,000-character-per-second rate. Other characteristics are: 1 microsecond cycle time; 4,096-word core memory

(expandable to 32K); 3 million bits of tape storage, expandable to 12,000,000 bits; alpha-numeric cathode ray tube display; 9-bit A/D converter with conversion rate of 7 microseconds; 16 analog input channels (expandable to 32); and 12 digital sense lines and a 12-bit parallel input to the accumulator. Maximum analog sampling rate of 110,000 samples per second, continuous sampling at a rate of 6,000 samples per second. Price is under \$50,000. Delivery is 90-120 days A.R.O. Spear, Inc., Waltham, Mass.

Circle No. 204 on Inquiry Card

ILLUMINATED SWITCHES

Illuminated dry-reed push-button switches designed for printed circuit boards or panel mounts on any plane have been announced. Reed contact material: Gold alloy and rhodium. Dielectric strength, 500 VAC. Insulation resistance, 100 megohms. Switches are printed with model number, schematic diagram, switch form and contact rating. Pre-travel .062 minimum — total travel 1.75 ± 0.20 . Lamp available from 1.35 to 28.0 volts. Key tops vary in size to specifications. Engraved to specification. Available in black, gray, beige, blue, red and white. Other colors on special order. Series — KBDP and Series KB. George Risk Industries, Columbus, Nebraska.

Circle No. 205 on Inquiry Card

MARK SENSING SYSTEM

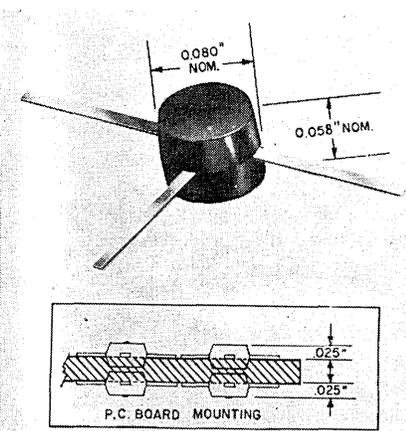
The OpScan 50, a new optical mark sensing system that fills a wide range of data gathering tasks for retailers, manufacturers, transportation companies, insurance firms, banks, etc., operates completely independent of a computer, scanning forms and transferring data in a one-step process to magnetic tape ready for computer processing. The system offers savings in keypunching and key-verifying costs, according to the maker. It does without keypunch operators by having the capability to read either machine-printed or pencil-marked data. Speed is achieved by computer printing of forms, a feature which helps avoid the many clerical errors experienced in the keying steps. The system reads a variety of forms down to as small as one inch by three

inches. It reads data directly from computer-printed, machine-printed, hand-marked, punched, and bar-coded forms. It even reads forms with a combination of machine-printed and hand-marked data. The device works alone, but teams with a computer to speed recordkeeping. It reads data from one inch by three inch forms at a speed of 24,000 per hour, interprets the data, and puts it on magnetic tape. Speed varies according to document size. Once on magnetic tape, the information is ready to be analyzed by computer. Basic price is about \$30,000. Optical Scanning Corp., Philadelphia, Pa.

Circle No. 206 on Inquiry Card

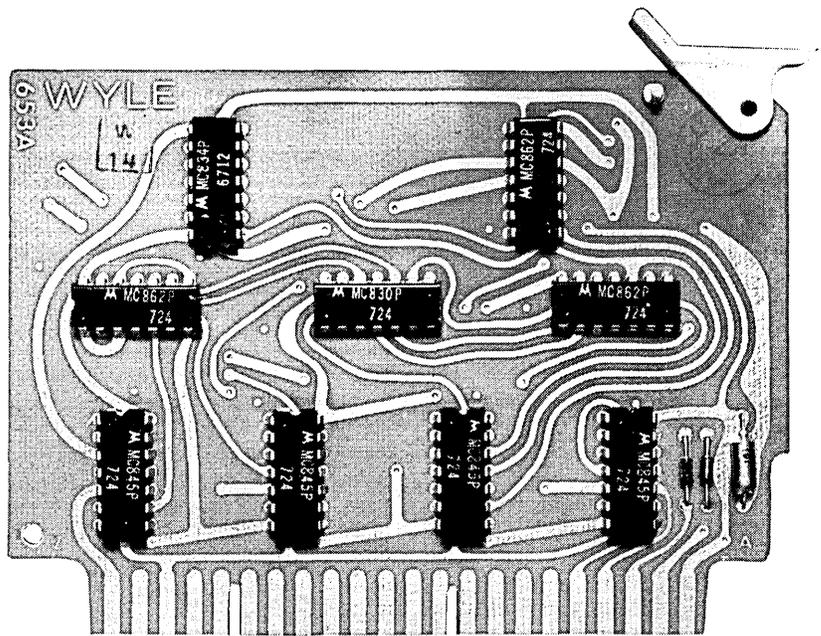
MICRO-MIN TRANSISTOR LINE

A low-level, high-speed switch, MM-T2369, and an RF amplifier, MM-T918, have been added to Motorola's new Micro-T transistor line. Housed in a reliable one-piece, injection molded Unibloc package about one-tenth the size of a TO-18 can, the tiny transistors are intended for high-density or space-limited applications. Ninety-degree spaced leads radiating from the center of the device make it well-suited for miniature PC board use. They can be mounted right side up or upside down, and the position of emitter and collector may be reversed to facilitate layout. This feature is also an advantage in thick-film and small, modular assembly applications. The switch provides a t_{on} of 12 ns max. and t_{off} of 18 ns max. measured at a collector current of 10 mA dc.



Motorola Semiconductor,
Phoenix, Arizona.

Circle No. 258 on Inquiry Card



WYLE LOGIC MODULES

FAST DELIVERY

TECHNICAL ASSISTANCE

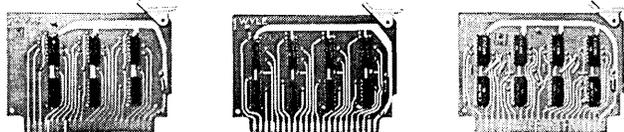
LOW COST

GENERAL PURPOSE DESIGN

BROAD SELECTION

TEN-YEAR WARRANTY

STATE-OF-THE-ART DESIGN



The above are some of the subheads in the Wyle Integrated Circuit Logic Modules short-form catalog. They are seven of the twelve reasons Wyle logic cards may be your best buy. If you want to discuss the other five reasons (or get more detail on the Big Seven), drop us a line on your company letterhead, and we'll send you the catalog. Or better still, call Don Tothe, our product manager, and let him fill you in on what Wyle can contribute specifically to your system. Systems Division, Wyle Laboratories, 128 Maryland Street, El Segundo, California. (213) 678-4251.

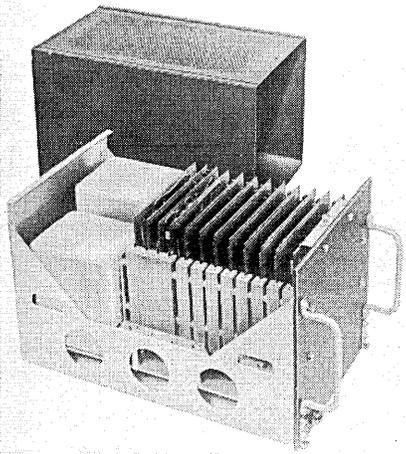
WYLE

CIRCLE NO. 46 ON INQUIRY CARD

MODULAR PACKAGING PANEL

High density packaging panel, with modular design, for 14-lead dual-in-line integrated circuits, permits user to specify any multiple of 30 up to 180 patterns. Each 30 pattern section provides for power and ground plane connections. Extra contacts are available for interconnecting plug applications. Patterns also accommodate adapter plugs for discrete components. Four leaf wiping, beryllium copper gold plated contacts are used for low contact resistance and high reliability. Wire Wrap® or solder pocket termination available. Augat, Inc., Attleboro, Mass.

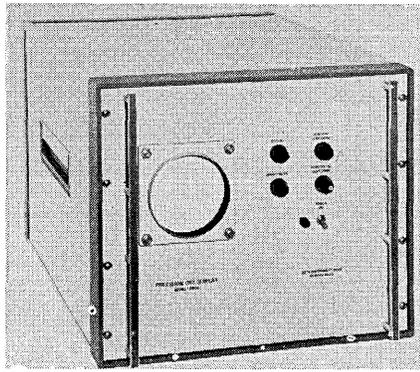
Circle No. 250 on Inquiry Card



8 CHANNEL SYNCHRO/DIGITAL CONVERTER

Use of the dual phase shift technique for converting synchro data to parallel digital data in a new converter provides simple circuitry with few precision components. Variations in the reference frequency are compensated by means of a synchronized oscillator which tracks the reference frequency over the range of 380 to 420 Hz. Multiplexing of 8 synchro channels is by means of a digital time gate so that no error is introduced by multiplexing. Each synchro can be excited by any phase of the three phase generator. A hard wired internal program samples each synchro at the proper timing of the reference waveform. All input synchros are transformer isolated from the converter unit. DC power supplies are self contained. Gap Instrument, Westbury, N. Y.

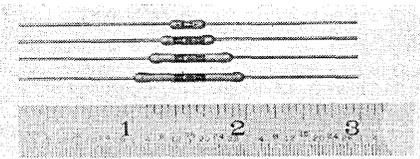
Circle No. 207 on Inquiry Card



X-Y CRT DISPLAY

A high-resolution, 5-inch X-Y CRT display, said to offer maximum performance in terms of resolution and speed at the lowest possible cost, utilizes all solid-state circuitry and is intended for application in film and hard copy recording and film reading. The device resolves more than 1700 elements/diameter. It is capable of random access X-Y deflection from DC to a slewing speed of 7 microseconds for the full diameter. Small-signal bandwidth is greater than 1 megahertz. Other features include high stability, repeatability and linearity. Called the PD900, it utilizes a narrow deflection angle cathode ray tube to minimize deflection defocusing and pin cushion distortion. It is a 5-inch flat-face magnetically-deflected and electrostatically-focused tube. Through the use of highly regulated power supplies, temperature stable components and temperature stabilized circuits, exceptional stability and reliability is achieved. The display includes deflection and blanking circuits, CRT and power supplies. Beta Instrument, Newton Upper Falls, Mass.

Circle No. 208 on Inquiry Card



MINIATURE MEGOHM RESISTORS

A line of miniature megohm resistors, with 80 PPM/°C absolute temperature coefficient, covers the one megohm to 220 megohm range; from 0.5 to 5.0 watts; from 600 to 4000 volts. Units are also available as network sets with matched characteristics with T. C. tracking to 10 PPM/°C on special order. All items

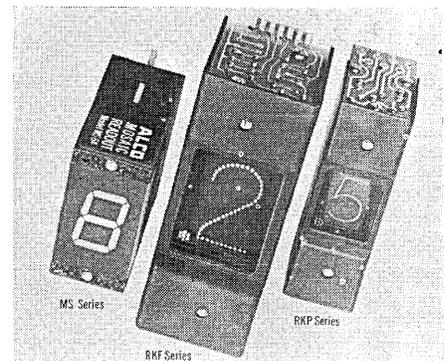
are offered in the standard resistance tolerance of $\pm 1\%$ with tolerances to 0.2% supplied on special order. Maximum operating temperature is 225°C. Caddock Electronics, Riverside, California.

Circle No. 255 on Inquiry Card

ROTARY PULSE GENERATORS

Rotary pulse generators for conversion of rotary motion into digital pulse information have been developed which operate on precision electro-optical principles and use no mechanical contacts or switches. The rotary input to the generators can be taken from a variety of drives such as a footage wheel, shaft coupling, and rack and pinion. Units are available in unidirectional and bidirectional models and can be supplied for use with most electronic counters. Veeder-Root Co., Hartford, Conn.

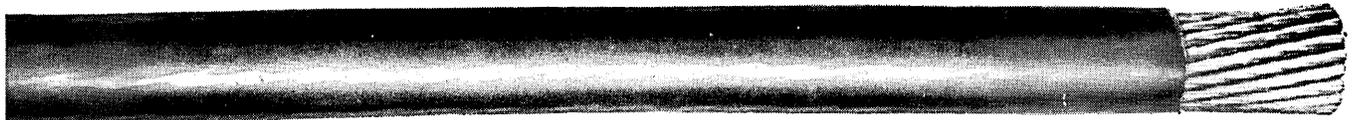
Circle No. 209 on Inquiry Card



BRIGHTER READOUT

An improved series of numeral and symbol readouts is said to make use of a unique "in-line" design to provide crystal-clear displays. The newest addition which is called the RKF Series, and is available for immediate delivery, is larger and brighter, and is designed for users who require higher intensity. The series is available in 6V, 14V or 24V models for both numerals and symbols. Its overall size is 3 1/4" high, by 1 1/4" wide, by 1 5/8" deep, including the printed circuit board. The display area for the figures which are formed by a series of engraved dots, is approximately 1-1/6" high, by 5/8" wide. Prices start at \$18.95 each, with quantity discounts quoted upon request.

Circle No. 254 on Inquiry Card



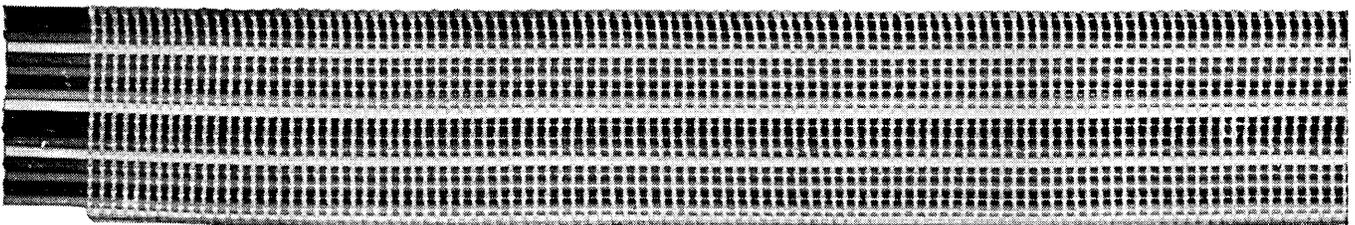
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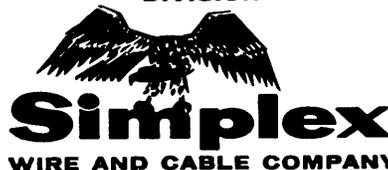


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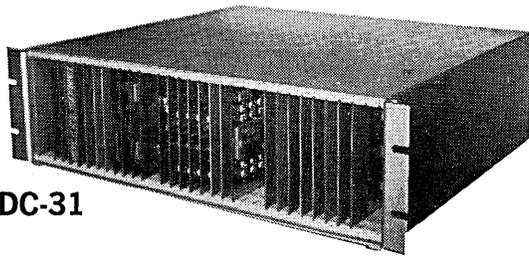
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CIRCLE NO. 47 ON INQUIRY CARD

NEW! MEMORY BUFFER



MODEL DC-31

- FULL CYCLE TIME1 Microsecond
- ACCESS TIME400 Nanosecond
- CAPABILITY128,256 or 512 Words
Up to 8 Bits/Word
- PRICE\$1260 for 128 x 6
In Small Quantities.
- DELIVERY30 Days.

Many options available . . . I C Logic and all silicon semi-conductors . . . All gold connectors . . . Flat mounted components.

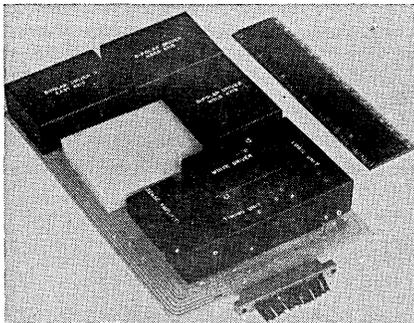


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CIRCLE NO. 48 ON INQUIRY CARD

NON-VOLATILE SHIFT REGISTER

A new thin-film type shift register using a technique described as Domain Tip Propagation Logic (DTPL) provides a non-volatility feature that enables it to retain information if power to the system is lost. Catastrophic failure due to voltage transients is virtually eliminated by nature of the design. Power consumption drops off very rapidly as the bit rate is reduced. In its quiescent state, the register draws 1.2 watts, and can operate in standby



condition with zero current. Functioning over a 0 to 250 KHz bit rate, this serial/serial device has a capacity of 1024 bits. It interfaces with DTL

and TTL logic levels, and maintains its parameters over a 0 to 50°C temperature range. The shift register contains all the necessary electronics to accept or deliver information, write, clear or start a cycle. Measuring 5½ x 8⅝ x 1¼ inches, it weighs only 19 ounces. Priced at \$3,000 in small quantities, available in 60-90 days. LFE Electronics, Boston, Mass.

Circle No. 210 on Inquiry Card

STORAGE BOARD

An integrated circuit storage array, which provides ultra high speed performance for custom system applications, offers a 64-word, 32-bit cycle time of 125 nanoseconds and a capacity (for a single printed circuit array) of 2048 bits. New data can be stored within 125 nanoseconds after a cycle is initiated. Using a bipolar flip-flop microcircuit as the basic method of storage, the storage board operates at very low logic levels and utilizes a unique cell of 16 bits arranged in a 4-word by 4-bit matrix. It is a complete storage subsystem requiring only decoded address inputs, bit driver inputs, timing

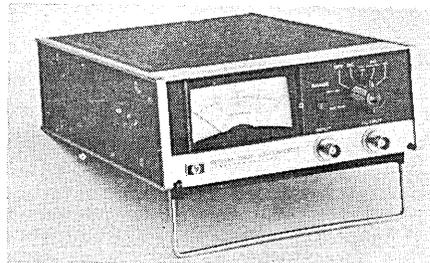
controls and Read and Write controls. Logic functions of the storage board are achieved by two-term address decoders and word drivers to select one of 64 words; by bit/sense lines with amplifiers to provide logic levels; and by buffered outputs to provide standard CT μ L (complementary transistor logic) interface levels. The range of applications includes indexing and scratch pad storage for ultra high speed computing, A-to-D buffer storage of video data as in RADAR data processing, and high speed data format buffering for permanent digital recording on slow speed mediums. The cells are housed in the Dual-In-Line package for standard pin alignment on printed circuit board assemblies. Interconnections are two-dimensional and can be extended to the limits of the word and bit driver. Fairchild Semiconductor, Mountain View, Calif.

Circle No. 211 on Inquiry Card

1.5 INCH VANE AXIAL BLOWERS

A new series of lightweight, high-performance vane axial blowers for spot cooling applications in high density electronic packages recently introduced weighs only 4.2 ounces and is available in 60 and 400 Hz versions with speed ranges from 3,300 to 22,500 RPM. Designated as the V-Line 150, this new series may be obtained in a variety of mounting configurations and terminations. Eastern Air Devices, Dover, New Hampshire.

Circle No. 256 on Inquiry Card

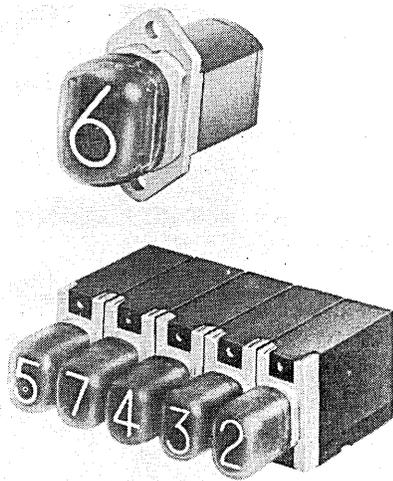


LOGARITHMIC CONVERTER

A logarithmic converter said to have exceptional conversion accuracy over a broad dynamic range, exceptional low-frequency response, and true RMS response has been announced by Hewlett Packard. Conversion accuracy is ¼ dB with dc inputs, ½ dB with ac inputs between 2 Hz and 50 kHz, and 1 dB with ac inputs from 0.5 to 2 Hz and from 50 kHz

to 100 kHz. It functions over an 80-dB input dynamic range — a 10,000-to-1 range of amplitudes. Frequency response in the ac mode extends from 100 kHz down to 0.5 Hz. The new converter will be useful for pulse height analyzer and computer readouts, and for other applications requiring wide dynamic range and/or logarithmic relationships. Adding the outputs of two logarithmic converters, for instance, results in a voltage that is proportional to the log of the product of the two input voltages. Hewlett Packard, Palo Alto, Calif.

Circle No. 259 on Inquiry Card



NIXIE® TUBE DRIVERS WITH ICs

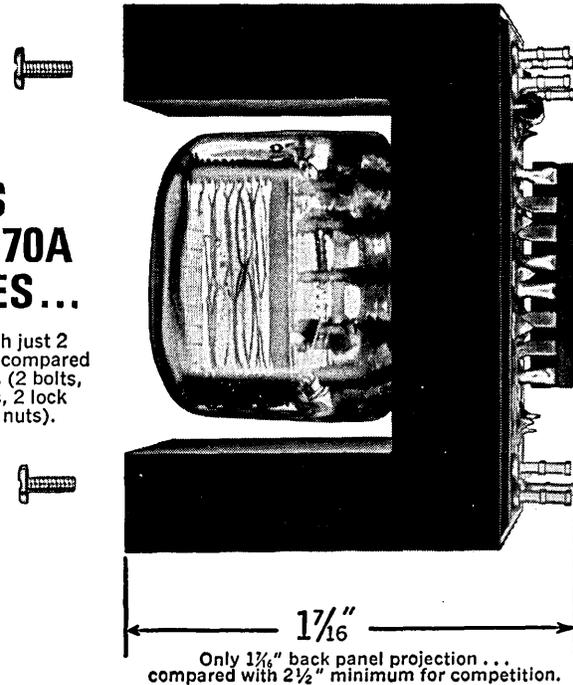
Driver modules for NIXIE® tubes which use integrated circuits have been announced by Burroughs Corp. With prices for decoder/drivers at \$26.00 (100 pieces) including the NIXIE® tube, these modules are said to offer not only the lowest price but the smallest package. Two series, the BIP-8800 and BIP-9800 are available from stock. All modules accept 4 line 8-4-2-1 BCD inputs which are compatible with TTL and DTL and have been designed to exceed applicable sections of MIL-E-5400J and MIL-T-5422E environmental specifications. The BIP-8800 series, designed to drive the standard rectangular NIXIE® tubes (0.5" character height), are available with or without memory (in the same compact package) and can drive either a "0-9" NIXIE® tube or a "0-9 with decimal point" NIXIE® tube. They will be used primarily in industrial test equipment and special-purpose instrumentation. The Burroughs Corp., Plainfield, N.J.

Circle No. 212 on Inquiry Card

NEW LOWER PRICE, SHORTER READOUTS

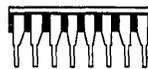
TEC'S TNR-70A SERIES...

Mounts with just 2 screws... compared with others (2 bolts, 2 standoffs, 2 lock washers, 2 nuts).



LOWEST PRICE* OF ANY DIGITAL READOUT WITH I-C DRIVER/DECODER

* \$25.25 each in 100-299 quantities, complete with Burroughs 8422 NIXIE® tube



TEC's TNR-70A Series gives you a complete decoder/driver package. This single monolithic silicon integrated circuit replaces discrete components. Accepts 4-wire 1-2-4-8 BCD inputs and produces 10 mutually exclusive outputs. Signal levels: Logic "1", 0 to +0.4V; Logic "0", +1.5 to +4.0V. TNR-70A Series is not a throw away... it's easily and completely repairable.

Whatever your readout preference: NIXIE tube, segmented or projection, TEC has the practical answer for your system. For complete information, contact your local TEC-Rep, or write direct.

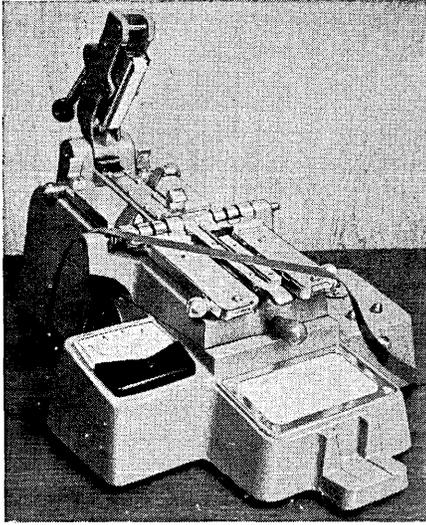


INFORMATION DISPLAY
AND CONTROL DEVICES

TRANSISTOR ELECTRONICS CORPORATION

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CIRCLE NO. 49 ON INQUIRY CARD



TAPE CONSOLIDATOR

Consolidation of magnetic tape by a thermo fusion principle is claimed possible with the model TF4550 consolidator. This innovation is said to permit re-writing and reading over thermo-fused tape areas even with today's advanced 800 bpi, 9-channel systems without any significant signal drop. The producer states that thermo-fused magnetic tape maintains all standard physical characteristics with new tape quality assurance. The real significance of the process, however, is said to lie in the savings in man-hours and dollars that will result from its many applications and features. Prestoseal, Corona, N. Y.

Circle No. 251 on Inquiry Card

DIGITAL TO SYNCHRO CONVERTER

All solid state digital to synchro converter, designed specifically for simulation and industrial control applications, accepts a 10-bit parallel binary input and provides a completely isolated synchro output at 11.8 volts, 400 cps line-to-line, with accuracy of better than 30 minutes of arc from no load to full load without adjustments. Its high power output is capable of driving multiple torque receivers without amplification.

The converter accepts micro-electric logic levels and has a maximum updating speed of 10,000 words per second. Internal storage registers are available as an option. Astro-systems, New Hyde Park, N. Y.

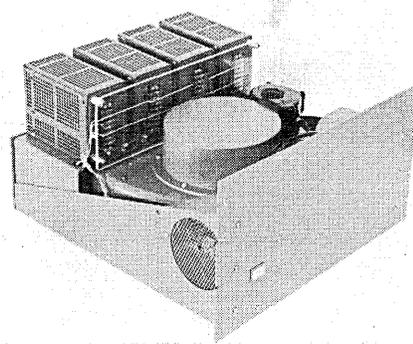
Circle No. 99 on Inquiry Card

TAPE READER

Tape reader priced at approximately one-half the price of competitive

units is claimed to make tape-controlled automation economically feasible for a broad range of industrial applications. The new tape reader uses starwheels to sense the holes in perforated paper tape. Output is presented in the form of contact closures. The unit reads standard 5, 6, 7 or 8 channel tape unidirectionally, at a rate of 30 characters per second. An electromagnet is used to advance the tape. Model 18 Tape Reader is said to provide control equivalent to that of far more costly units without complex circuitry or timing and is as easy to use as a relay. Price: \$180.00 f.o.b. Idea Associates, So. Hackensack, N. J.

Circle No. 213 on Inquiry Card

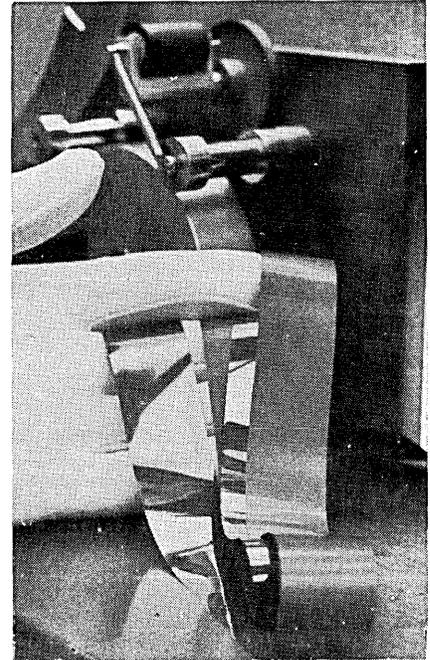


DIGITAL/VIDEO DISC RECORDER

Raster-type TV monitors can now be used for low-cost alphanumeric, graphic, and digital-television-display systems when used in combination with a new digital/video disc memory. Up to 100,000 bits on each track can be accessed at a 3-megabit rate, or up to 7.2-megabit capacity is available at bit rates up to 216 megabits/second with track-combining techniques. Up to 72 completely independent tracks can be provided on a single disc memory. Each track has its own read/write and clock electronics with TTL integrated-circuit interface that permits reading or writing in parallel. Tracks can be written without disturbing data being read from adjacent tracks. The manufacturer claims the use of disc-refreshed TV monitors for display terminals offers exciting opportunities for significant cost reductions in display installations for hospitals and airports, time-shared computer systems, instructional systems, military command centers, etc. Display systems using the disc memory can provide either black-and-white or color

presentations. Each of the display recorders occupies 10½ inches of 19-inch-wide rack space, and is 20 inches deep. Power requirement is 120v AC, 60Hz. Disc speed is 1,800 rpm. The basic 8-track disc memory system sells for \$7,270, with additional 8-track increments available at \$2,400. Data Disc, Inc., Palo Alto, Calif.

Circle No. 214 on Inquiry Card



MAG TAPE UNIT

A self-threading magnetic tape unit, the IBM 2420, is said to operate nearly twice as fast as previously available magnetic tape units using standard half-inch tape. Designed for the IBM System/360 Models 50, 65, 75 and 85, the new unit stores or reads information at a rate of 320,000 bytes a second. The unit, with a new single-capstan drive mechanism, features automatic threading, a tape speed of 200-inches per second, reduced tape wear, and compatibility with existing high-speed IBM tape units. An optional wrap-around cartridge (shown here on both tape reels) can be used with the unit to minimize tape handling. All standard tape reels can be threaded automatically, including 10.5-inch and 8.5-inch reels, as well as 5.25-inch Minireels. The equipment rents for \$1,050 a month and sells for \$54,600. Initial deliveries are scheduled for the fourth quarter of 1968. IBM Corp., White Plains, N. Y.

Circle No. 215 on Inquiry Card

CRADLE® RELAY

TU154 Cradle® relay has received Underwriters' Laboratories recognition for 3 ampere resistive switching at 115 volts AC and is available in 4PDT and 6PDT, with polycarbonate plastic dust cover. The relay is intended particularly for use in industrial controls, computers and other data processing equipment and systems, business machines, and other applications where long life and reliability at maximum economy are desired. Allied Control, New York, N.Y.

Circle No. 248 on inquiry card.

7 MHz SCOPE

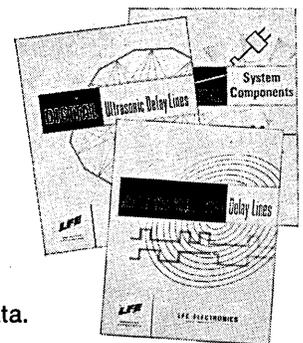
A low-cost, general-purpose oscilloscope with an extended frequency range named Model 555 is designed for both laboratory and field use and contains performance and construction features normally found in larger expensive units. The cathode ray tube is a 5-inch flat-faced Braun tube divided into a viewing area of 8 x 10 centimeters by a removable edge lit graticule. All amplifiers are multistage DC coupled, and solid-state with full compensation for optimum response. The 9-step attenuator has a variable trimmer for each step to provide frequency compensation. An extremely linear time base using a miller circuit provides accurate and precise sweep speeds with variable controls in 19 calibrated ranges. The horizontal amplifier contains a 5X expansion which effectively increases the sensitivity by a factor of 5, and permits positioning of the expanded trace. To standardize time and voltage a 3% calibration is built into the instrument. Specifications of the Model 555 are: Vertical Amplifier Bandwidth: DC to 7MHz within -3db, DC coupled; 2Hz to 7MHz within -3db, AC coupled. Rise Time: 0.05 μ s. Sensitivity: 0.02 v/cm to 10 v/cm in 9 ranges. Input Impedance: 1 Ω parallel capacitance 33PF. Sweep Speeds: 1 μ s/cm to 1 sec/cm in 19 ranges. Accuracy: \pm 5%. Power: 110-122 Volts 60 Hz. Physical: 8" x 10 $\frac{1}{2}$ " x 16". Weight: 22 lbs. A full year warranty for parts and service is provided. Data Instruments, Pennsauken, New Jersey.

Circle No. 252 on inquiry card.

In a word, LFE for glass and magnetostrictive delay lines for digital applications

These are just a sampling of the performance features of LFE's glass and magnetostrictive delay lines. We can supply you with standard delay lines or serial memories with the capacity, bit rate, mode, delay and other parameters you need... or, you can specify custom delay lines, with or without associated electronics, to meet your special design requirements.

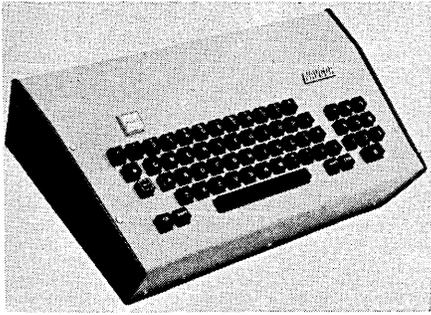
For the complete story write for technical data.



ELECTRONICS DIVISION

Laboratory For Electronics, Inc.
WALTHAM, MASSACHUSETTS 02154
Tel: 617-894-6600 • TWX: 710-324-0681

CIRCLE NO. 50 ON INQUIRY CARD



ELECTRONIC KEYBOARDS

Modular keyboard assemblies, said to offer broad flexibility in meeting today's man/machine interface requirements, are now available in standard configurations, and can be adapted to special applications with a minimum of time and cost. Each key has a life expectancy of over 100 million operations, and repair or modification of a keyboard involves only the removal and replacement of a modular component. A basic keyboard consists of an array of NAVCOR KRM keys mounted directly on an etched-circuit base panel. For coded outputs, a diode matrix is available either on the same etched-circuit board which holds the keys or as a separate board below and parallel to the keyboard. Navigation Computer Corp., Norristown, Pa.

Circle No. 216 on Inquiry Card

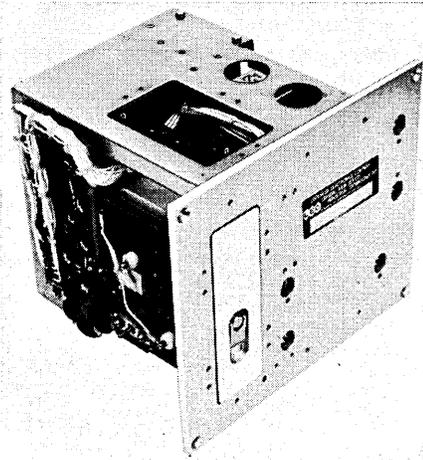


DIGITAL CLOCK

A low cost electro-magnetic digital clock, featuring differential time correction input control and legibility in direct sunlight, uses no mechanical linkages such as gears, ratchets or pawls, and boasts a million-hour lamp life, achieved by using a rugged filament running at about 1/2 of rated voltage. The clock uses a magnetic stepping motor and projects a 300 foot lambert, 1 1/2 inch numeric display. It provides binary coded decimal outputs for use with time recording systems — printers, magnetic tape data acquisition systems, etc. The basis frequency reference for the clock, available in 24 hour and 12 hour models, is the 60 Hz power line. One second timing pulses are derived directly from the 60 Hz

power line through a long life synchronous motor and a photoelectric pickup (no switch contacts or commutators are used). Price is \$740. Numex Corp., Waltham, Mass.

Circle No. 217 on Inquiry Card



MAG TAPE MEMORY READER

Plans for the production and marketing of a small, lightweight, low powered, seven-track memory reader which is capable of storing up to 125,000 characters have been announced by Lockheed Electronics. The digital magnetic tape memory reader, called the Model TR 26S, was originally designed for use on Polaris checkout equipment and is now being placed on the commercial market. The unit is only 6 1/2" x 7" x 6 1/2", weighs less than nine pounds, and has read, rewind, search, and standby modes. The TR 26S is suited for laboratory, field, shipboard and airborne program insertion in computer systems. Price will be below \$4,000, depending upon electronics selection and options. Lockheed Electronics, Plainfield, N. J.

Circle No. 260 on Inquiry Card

PLOTTER

A new high-speed on-line plotter employing a laser optics system as the basic image generation device is completely computer controlled, taking its information from a computer's core memory system. Because of this it is able to plot one line while computing the next line. It plots on roll film up to 100 feet in length and 40 inches in width at a resolution of 200 lines per inch. A five-mil resolution provides continuous tone or line cartographic displays with a minimum loss of continuity.

The plotter's ability to achieve 14 distinct levels of gray between white and black provides effective plotting of variable densities. It is compatible with automatic processing systems and is designed to be used in a computer room alongside other I/O devices. It will plot alphanumeric symbols in any dimension or slant. Dresser Industries, Houston, Texas.

Circle No. 218 on Inquiry Card

INTEGRATED CIRCUITS

A second-generation series of semiconductor integrated circuits, priced as low as 20-cents a gate function, are expected to offer 5 to 10 times greater noise immunity and 5 times greater fan-out than RTL circuits.

Eleven circuits identified as the Utilogic II series, are offered in a dual in-line silicone package which permits the low prices and is said to make them much easier to handle on the user's production line.

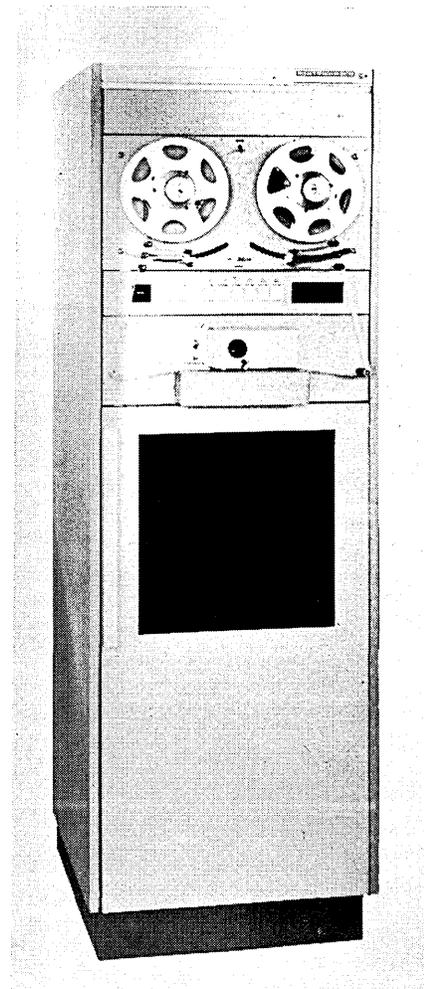
Seven of the circuits are new high-performance multi-functional units including dual J-K binaries and triple and quad gates which make it possible to design systems with much lower can counts. The devices are being offered in two temperature ranges, the LU-series to operate at from 15 degrees to 55 degrees centigrade and the SP-series at 0 degrees to 75 degrees centigrade. Signetics Corp., Sunnyvale, Calif.

Circle No. 219 on Inquiry Card

SOLID STATE RELAY

Solid state relay featuring no moving parts to assure long life, isolated input for reliability, transient protection and positive operation performs the same functions as an electromechanical relay with the added advantages of increased reliability. All solid state engineering eliminates problems caused by bounce . . . mechanical wear and film and grit buildup. Relays can be supplied with internal or external electromechanical output relays when required; are available for over-under voltage, over/under frequency, phase sequence, reverse power or in combinations of these. Features: plug-in mounting; SPST output (solid state); Tele-Craft Electronics, Farmingdale, N. Y.

Circle No. 220 on Inquiry Card



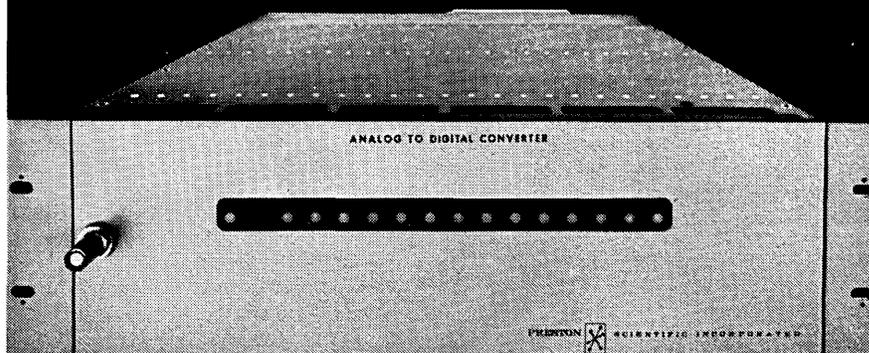
COMMUNICATION TERMINALS

Two new multi-media communication terminals, Model 5072 combined paper tape transmitter/printer receiver terminal and Model 5079 transmit/receive paper tape terminal, use reverse channel techniques and integrated circuits for high efficiency operation. Dial-o-verter Model 5072 requires no on-site programming to transmit punched tape or to receive and print hard copy. The device uses a type 202C data set on the dial telephone network and a type 201B or Rixon Sebit 48 data set on leased lines, handles all EIA standard five-through eight-level punched paper tape codes, at speeds up to 300 characters/second. It receives and prints data at up to 300 lines/minute. The standard printed format is 120 columns wide, 6 lines/inch vertical spacing, and 64-character alphanumeric font. Up to 6 carbon copies may be produced. Digitronics Corp., Alburtown, N. Y.

Circle No. 221 on Inquiry Card

Preston Scientific breaks the price barrier in 14-bit A-D converters!

10,000 samples/sec model 8500 K: \$1995
80,000 samples/sec model 8500 MS: \$3545
196,000 samples/sec model 8500 VHS: \$5485



Never before has so much speed, accuracy and reliability in A-D converters been offered at such low prices!

Behind this achievement is seven years of producing similar units for major aerospace programs. Speed is achieved with specially designed logic circuits, level detectors, and amplifiers. Accuracy is the combined result of extremely stable reference voltage, careful design and parts selection, in-house fabrication of critical parts, and precision assembly. And reliability is achieved through careful design, appropriate component derating, and circuit simplicity.

Each of the 8500 Series A-D converters features accuracy of $\pm 0.01\%$ $\pm 1/2$ LSB and will accommodate input voltages up to ± 10 volts. Input impedance is 10 megohms or greater at DC. Options are available such as faster speeds, sample-and-hold circuitry, Nixie-type readout, and special input voltage ranges. Special models are available by quotation. Write for complete information.

PRESTON



SCIENTIFIC INCORPORATED
 805 East Cerritos Avenue, Anaheim, California 92805

CIRCLE NO. 51 ON INQUIRY CARD

PULSE-RATED FERRITE TOROIDS

Pulse transformer designers in the computer, radar, data acquisition, telemetry and communications fields, will now be able to by-pass trial and error selection of ferrite toroid cores, according to Indiana General Corp. The PR Series, a line of 100-percent tested pulse-rated toroids, will consist of toroids with guaranteed characteristics including pulse inductance, pulse magnetizing current for specified voltage, ET constant, controlled pulse permeability and controlled temperature. Uniformity of the new toroids from sample through production quantities will be assured through A.S.T.M. testing methods which are directly related to end performance. Indiana General Corp., Keasbey, N. J.

Circle No. 257 on Inquiry Card

OILED PERFORATOR TAPE

A unique, relatively low cost, cross-linked cellulose perforating tape with nearly double the strength of conventional paper tapes is said to permit either substantial savings when substituted for more expensive materials in communication, computer, numerical control and data processing applications or a larger factor of safety when used in place of ordinary paper tape. The newly developed product is claimed to be superior in most aspects to vulcanized fibre. One of its major advantages over fibre is that the extra tensile tape is supplied with a carefully controlled oil content for punch and die lubrication. The tape is no thicker than standard perforator tape and is completely compatible with standard-tape equipment. Developed specifically for repeat usage, it comes in 1,000-foot coils, each 8" in diameter with 2" I.D. cores, in 1", 7/8", and 11/16" widths. The color is buff and it is available for immediate delivery. Robins Industries, College Point, N. Y.

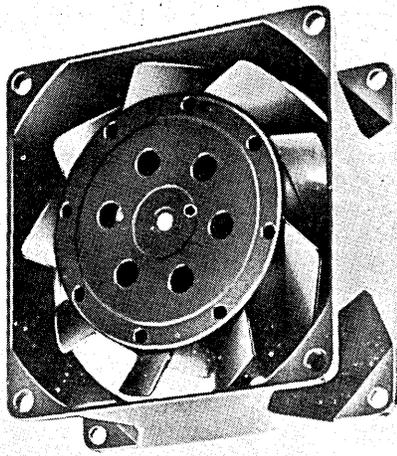
Circle No. 222 on Inquiry Card

EXTENDED STORAGE MODULE

An extended storage digital glass memory module capable of handling 4,096 bits at bit rates of up to 16 megahertz (MHz) has recently been introduced. The manufacturer states that the module represents a new

state of the art for "zero TC" glass delay line storage. Previous capacity for "zero TC" glass delay lines was 2,800 bits at bit rates up to 8 MHz. Applications for the extended storage modules include use as buffers in computer peripheral and data communications equipment as well as a wide variety of digital applications, including signal processing, real-time correlators and spectrum analyzers. As many as eight modules can be run in parallel with common clock and control signals to form a 4,096 by 8-bit "non-rotating drum" memory for use in high-speed buffer applications or as the main memory in small special-purpose computers. Corning Glass, Raleigh, N. C.

Circle No. 223 on Inquiry Card



AXIAL FANS

Compact dimensions for low profile cooling requiring high sustained air delivery have been designed into a new series of miniature axial fans. The series 8500 develops greater pressures from a nine-impeller all-metal fan measuring 3 1/8" square and 1 1/2" deep. Standard mounting centers of 2.812" make it interchangeable with other 3 1/8" fans. Free air delivery rating is 45 cfm and the fan is capable of continuance at back pressures up to 0.175 inches of water. It operates at a noise level of 28.8 dB SIL. The impedance-protected, two-pole, shaded-pole motor has a life-expectancy of 20,000 hours continuous duty without maintenance at an ambient temperature of 55°C and 100,000 hours at room temperature (25°C). Price: \$11.65 each in quantities of 25-49. Pamotor, Inc., San Francisco, Calif.

Circle No. 224 on Inquiry Card

INDICATOR LIGHTS

Indicator lights of this series consist of the housings (type designations LH90/1, LH90/2 and LH90/3) which accommodate the appropriate incandescent or neon cylindrical plug-in lamp cartridges (MS Drawing Numbers 18235, -6, -7, -8). Housing LH90/1 is furnished with collar and accommodates MS18235, -6, -7 plug-in cartridges only. Housings LH90/2 and LH90/3 are furnished without collar. The former housing accommodates MS18235, -6, -7 cartridges only. The latter (LH90/3) houses 48 or 60 volt incandescent cartridges (MS18238) only. These two housings may be used with lens cap types LC30 or LC32, available in a choice of five colors. Hot-stamped or engraved legends may be had. Neon cartridges offer two lens shapes, stove-pipe or long cylindrical for 110-125V AC or 105-125V AC-DC operation. Necessary current-limiting resistors are contained within the lamp cartridges. The AC group use 33K, the AC-DC group use 100K resistors. Dialight Corporation, Brooklyn, New York.

Circle No. 253 on inquiry card.

CARD-EDGE PC CONNECTORS

Four new series of receptacle type connectors for printed circuit applications are now available. Series 600-6 microminiature with .050" center-to-center contact spacing accommodates 1/16" printed circuit board in six sizes: 10, 14, 22, 40, 55 and 64 dual readout contacts, equivalent to 20, 28, 44, 80, 110 and 128 terminations. Series 600-121 for 1/16" printed circuit board and .100" center-to-center contact spacing is available in a single 26 contact size. Unit features bifurcated contact construction and staggered termination design. Series 600-94 for 3/32" printed circuit board and .100" center-to-center contact spacing has two variations of 38 dual contacts and three termination types: solderless-wrap, dip solder or solder lug. Series FT600-13 is a double bellows feed-thru type for 1/16" printed circuit board-to-board interconnection. Center-to-center contact spacing is .156". Continental Connector Corporation, Woodside, N.Y.

Circle No. 326 on inquiry card.

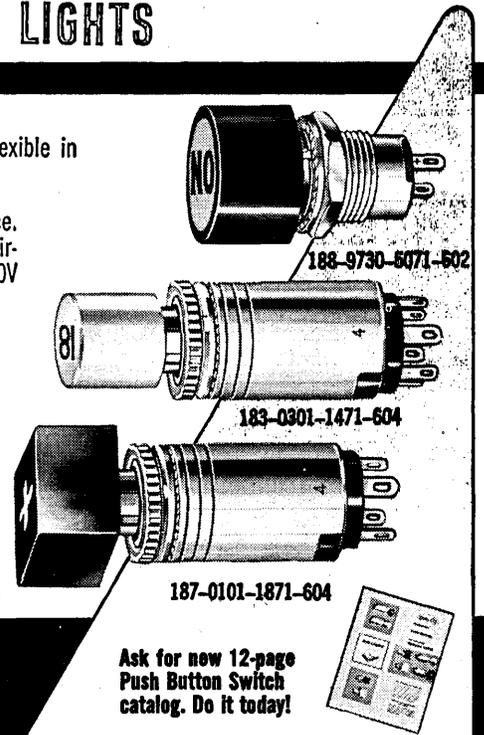
Improve Display Capability with Dialco Sub-Miniature ILLUMINATED PUSH BUTTON SWITCHES and matching INDICATOR LIGHTS

Dialco Switches and Indicator Lights provide almost limitless applications—are flexible in arrangement—economical in price—and feature high reliability.

Switches are the silent, momentary type—requiring 24 oz. (approx.) operating force. Contact arrangements are: S.P.S.T., normally open or normally closed; S.P.D.T. two circuit (one normally open, one normally closed). Ratings: 3 amps, 125V A.C.; 3 amps, 30V D.C. (non-inductive).

The switch is completely enclosed and independent of the lamp circuit. The light source is the T-1-3/4 incandescent lamp, available in voltages from 1.35 to 28V. Switches are made for single hole (keyed) mounting in panels up to 3/16" thick and mount from back of panel in 1/2" clearance hole. Switch forms for dry circuits are also available.

Other features include: 1/2" or 3/4" interchangeable caps, round or square, rotatable or non-rotatable, in a choice of 7 color combinations.



(illus. approx. actual size)



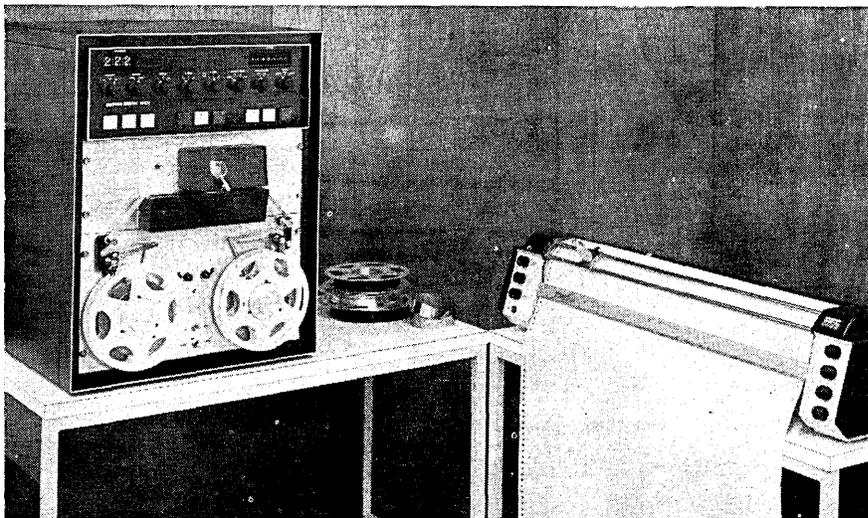
Foremost Manufacturer of Indicator Lights

DIALIGHT CORPORATION

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Ask for new 12-page
Push Button Switch
catalog. Do it today!

CIRCLE NO. 52 ON INQUIRY CARD



3-AXIS N/C TAPE VERIFICATION

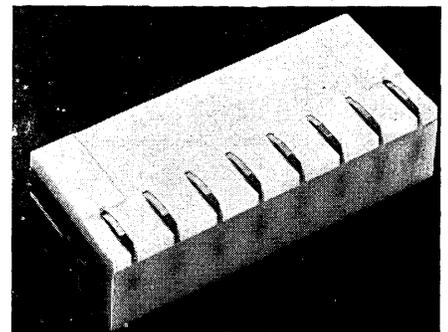
Low-cost system designed specifically for 2- and 3-axis machine tool numerical control (N/C) tape verification, priced at \$16,775 is said to be 3 to 5 times lower in cost than any other equipment available for this purpose. Delivery is quoted at 45 to 60 days. The system visibly plots the programmed cutter path at high speeds from actual machine tool input tapes, eliminating expensive tie-

up of machine tools now doing time-consuming dry-run verification. Two- and 3-axis contouring jobs that require several hours of machine time can be plotted and proofed in minutes with the N/CV system. Parts, 5 feet by 120 feet can be plotted continuously over their entire length when the 1/2 full scale setting is selected. Drawing resolution is optionally either 0.005 or 0.010 inches. Boston Digital, Ashland, Mass.

Circle No. 249 on Inquiry Card

EIGHT-TRACK FLYING HEAD

Eight-track flying magnetic head for disc memories provides reliable performance at packing densities up to 1300 bits per inch. In a multiple interlace configuration 30 tracks-per-inch can be recorded on a disc surface. Track width is 0.020" spaced on 0.132" centers. Inductance is 20 microhenries per winding leg and gap length is 250 microinches. External dimensions are: Length 1.052" x Width .438" x Height .300 max. Prices start at \$160.00 each and vary with quantity. Availability is 6 weeks.



Applied Magnetics Corp., Los Angeles, California.

Circle No. 247 on Inquiry Card



LITERATURE

Self-Contained D-C Voltage Regulators

A 4-page data sheet describing new miniature, self-contained Series 805 D-C voltage regulators provides complete specifications for the fixed-output, +3 to +9 volt hybrid series, presented in an easy-to-read "minimum-typical-maximum" performance chart. Significant construction, performance, and environmental characteristics are also discussed. The data sheet, No. 68485, provides full details on circuit design, and includes a circuit schematic. Additional data on the cermet thick-film regulators is also presented in a series of performance charts, a typical application diagram, and a detailed product outline drawing. Beckman Instruments, Inc., Fullerton, Calif.

Circle No. 322 on Inquiry Card

RFI Filters

Specifications of RFI filters designed to attenuate fluorescent lamp-generated noise in computer centers, instrumented test and research laboratories, clean rooms and other installations are highlighted in a data sheet describing the type F-20064 ballast filter. The new filters weigh only eight ounces and provide noise attenuation that meets or exceeds that of any RFI filter presently available according to the manufacturer. San Fernando Electric, San Fernando, Calif.

Circle No. 320 on Inquiry Card

Mag Tape Recorders

Solid-state logic control and other design features of two new instrumentation magnetic tape recorders/reproducers for portable and airborne applications are described in a brochure by the Data Division of Genisco Technology Corporation. The four-page brochure describes both units as having the same basic specifications, but differing in operational functions, configuration, size,

weight, and operating voltage. Both units comply with MIL-E-5400 and IRIG-106-66. A fast response phase-lock servo, in conjunction with a low inertia capstan motor, provides optimum performance, minimizes mechanical components, and affords seven speeds selectable electrically, without pulley or belt changes, from 1 $\frac{7}{8}$ to 120 ips.

The 10-276 Airborne version is designed for aircraft and high altitude environment applications where extreme shock and vibration are encountered. It operates on 28 volt DC power supply and weighs 65 pounds. Designed for a wide range of mobile, shipboard, laboratory, and field applications, the 10-276 Portable Recorder/Reproducer includes 115 VAC to DC power supply, and weighs 100 pounds in a 14-channel configuration. Genisco Technology Corp., Compton, Calif.

Circle No. 319 on Inquiry Card

Oscilloscope Book

New 128-page book, "Understanding and Using Your Oscilloscope," covers the basic theory of the oscilloscope, its many uses, interpretation of wave forms and operation with associated equipment. A clear writing style is maintained for easy understanding by students and beginners as well as the veteran technician. Chapter headings: History of the Cathode Ray Tube; Basic Oscilloscope Principles; Interesting Oscilloscope Applications; Oscilloscope Controls, and How to Adjust Them; How to Select an Oscilloscope; Auxiliary Equipment; Oscilloscope and Test Equipment Kits. Price is seventy-five cents, postpaid in the U.S.A. Allied Radio Corp., Chicago, Illinois.

Circle No. 318 on Inquiry Card

MCD Scopes, X-Y Monitors

Catalog describes and illustrates storage and general purpose oscillo-

scopes, X-Y monitors, medical monitors and special purpose instruments, and contains a photograph of each unit, 18 instruments in all, plus all pertinent data and specifications. The material presented is arranged to allow ready comparison of various models, either by degree of sophistication or by expected application. Measurement Control, Philadelphia, Pa.

Circle No. 317 on Inquiry Card

Magnetic Tape Systems

Literature describing Honeywell Model 7600 magnetic tape systems is available in a series of three 4-page brochures. The publications are designed to cover the basic capabilities of the analog recording tape system. Medium-band, wide-band and parallel PCM recording capabilities are discussed. Detailed information is presented in each of the illustrated brochures on use of the three types of recording systems, in addition to related operational and design specifications. Honeywell Test Instruments Division, Denver, Colo.

Circle No. 323 on inquiry card.

Station Carrier

A 12-page brochure describing the 83A Single-Channel Station Carrier System, which permits the addition of a private line on an existing cable pair, is available. The 83A, which might be called a "portable spare pair" is suited for transmission of Schedule 4 data services such as Datatel, TWX, and dedicated data circuits. It operates with dial or Touch Calling telephone subsets with no modification required on the subset. The publication includes performance information, equipment description, block diagrams and photographs. Lenkurt Electric, San Carlos, Calif.

Circle No. 324 on inquiry card.

Cooling Systems

24-page catalog R-68 describes 10 series of blowers and systems for cooling electronic cabinets. Designed to fit standard 19" racks per Mil-Std-189, the blowers are available in ranges from 200 to 1200 CFM and are provided with 50 and 60 cycle ball bearing motors. Catalog pages list applicable military and federal specifications; complete construction data; sizes; electrical properties; and RFI shielding applications. Detailed drawings and dimensional callouts are shown, plus air delivery curves and concise ordering information for each series. The catalog features extensive engineering data for practical blower selection, including cooling formulae; air delivery and heat dissipation curves; horsepower requirements; noise criteria. Zero Manufacturing Co., Burbank, Calif.

Circle No. 316 on Inquiry Card

Perforated Tape Components

6-page, two-color short-form catalog describes an entire line of tape punches, readers, and handlers, photoelectric keyboards, I/O typewriters, printers and systems incorporating perforated tape components. Invac Corp., Waltham, Mass.

Circle No. 315 on Inquiry Card

Programmed Image Analysis

6-page color brochure describes a unique general purpose visual image processor which reads from or records on film, differentiating between wanted and unwanted data. Under control of a stored program it can identify and trace only the object of interest, as opposed to "flying spot" techniques, which gather and store all data points on the raster. The brochure describes various subunits of the complete system, including the film handling optical/mechanical unit, signal processing and logic unit, programmable light source (point-plotting CRT), scan control monitor unit and CRT graphic terminal with light pen. A general introduction to the field of automatic image analysis is given, as well as operations involved in a typical application such as the reading of theodolite film. Information International, Los Angeles, Calif.

Circle No. 304 on inquiry card.

GOVERNMENT REPORTS

TERMINATION OF TECHNICAL TRANSLATIONS JOURNAL

The Technical Translations (TT) announcement journal published by the Clearinghouse will be discontinued after December 1967 (Vol. 18, No. 12, Dec. 30, 1967). Beginning in 1968, all U. S. Government-sponsored technical translations will be announced in the Clearinghouse journal, U. S. Government Research and Development Reports (USGRDR). The first issue of USGRDR announcing these translations will be Vol. 68, No. 1, Jan. 10, 1968. USGRDR subscription rates are \$30.00 a year (\$37.50 foreign); single copies cost \$3.00. All reports, including translations, announced in USGRDR will continue to be indexed in the companion journal, U. S. Government Research and Development Reports Index (USGRDR-I), formerly called Government-Wide Index (GWI). USGRDR-I subscription rates are \$22.00 a year (\$27.50 foreign); single copies cost \$3.00.

After December 30, 1967, translations not sponsored by U. S. Government agencies will not be announced by the Clearinghouse. These translations are announced in both the Translations Register-Index published by the Special Libraries Association Translations Center, and in the ETC Quarterly Index published by the European Translations Centre. The Clearinghouse will continue to provide reference information and attempt to answer specific queries on all translations, both Government-sponsored and non-Government-sponsored.

Translations Register-Index is available from the SLA Translations Center, John Crerar Library, 35 West 33rd Street, Chicago, Illinois 60616, at \$30.00 per year.

ETC Quarterly Index is available from the European Translations Centre, 101, Doelenstraat, Delft, The Netherlands, at \$25.00 per year.

Bibliography-Index to US JPRS Research Translations, listing all JPRS issues in subject compilations including their complete table of contents and subject index is available from Research & Microfilm Publications, Inc., Suite 430, 2233 Wisconsin Ave., N. W., Washington, D. C. 20007. Four titles are issued monthly: China & Asia, East Europe, International Developments (Africa, Near East, Latin America) and Soviet Union. Subscription cost: \$30.00 per year for each area. Two semi-annual publications are also issued: Catalog Cards in Book Form for US JPRS Translations, arranged in JPRS publication number sequence with detailed contents for each translation (\$95.00 per year) and Subject-Index to US JPRS Translations (\$20.00 per year). Microfiche copies of individual JPRS translations are available on subscription at \$0.32 per microfiche.

DEVELOPMENT OF AN AUTOMATIC PROCESS START-UP DEMONSTRATOR.

Investigates capabilities of pure fluid elements for application to digital logic such as might be encountered in the sequential "start-up" or "shut-down" of machinery.

Order from Clearinghouse, U. S. Dept. of Commerce, Springfield, Va. 22151. Order No. AD-661 461.



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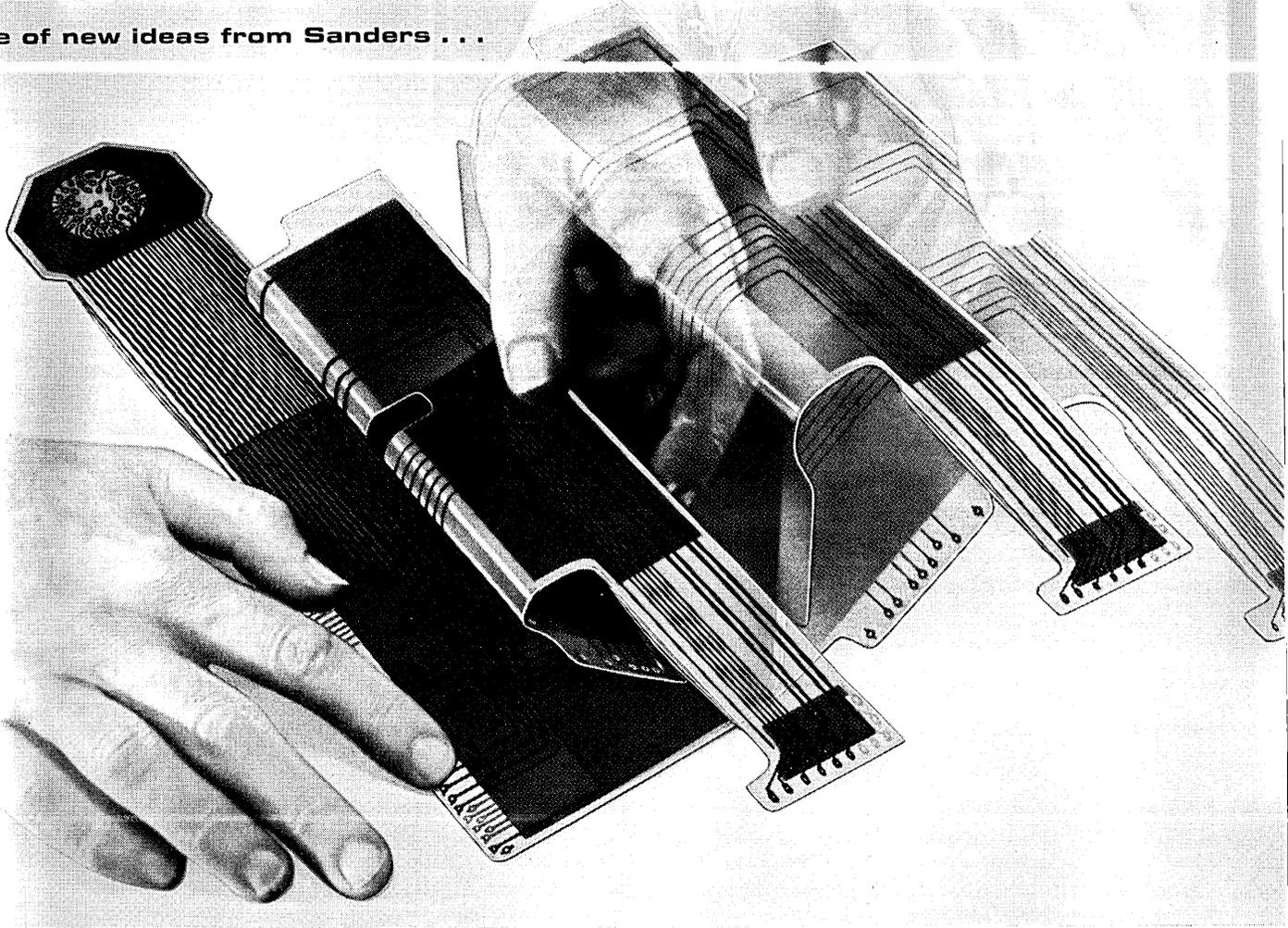


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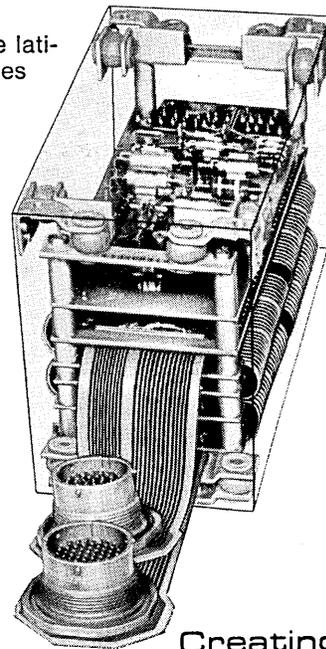
Volume, weight and shape. Reduce these problem areas, and you've got more latitude to meet restrictions imposed by unusual form factors and limited spaces available for interconnections in modern electronic gear.

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