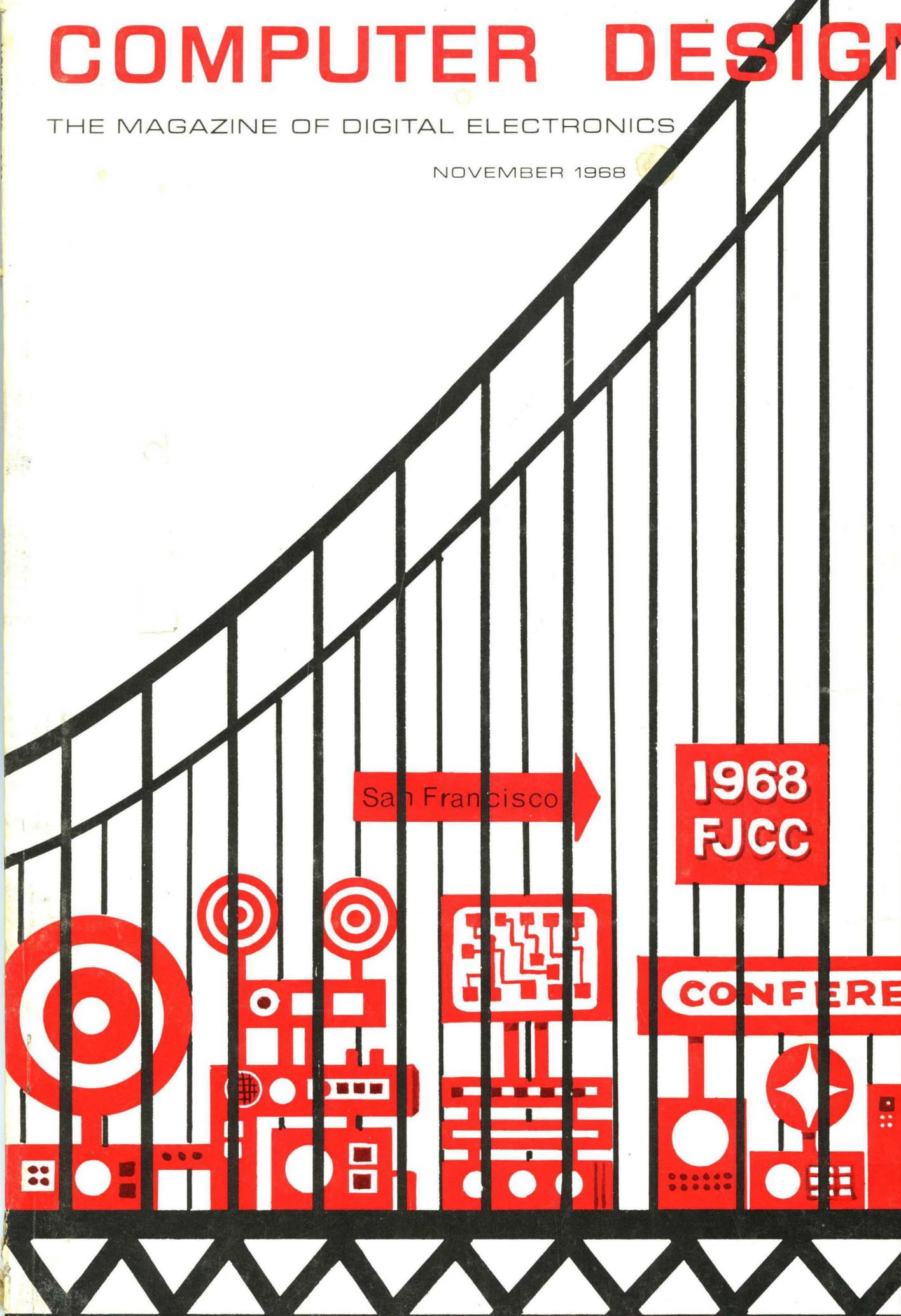


COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

NOVEMBER 1968



San Francisco

1968
FJCC

CONFERENCE

Varian Data Machines' new 520/i dual environment computer gives you 2 computers in 1almost.

We've designed our new 520/i computer with enough hardware power to handle dual, independent tasks that would often require two computers. That's why we've called it a dual-environment computer.

With its two complete, independent sets of hardware registers, including index registers, the 520/i efficiently runs parallel programs or efficiently processes background and foreground information.

Since each program uses its own set of registers, a single 1.5 microsecond instruction transfers control from one environment to the other. This dual-programming capability keeps housekeeping to an absolute minimum. And whatever your data format or word length, the 520/i performs arithmetic in 8-, 16-, 24-, or 32-bit lengths within the same program! And each program can change its own precision at any time.

So if you think you have enough work for two computers—see if the 520/i will do the job. The new Varian Data 520/i with a 4K memory sells for \$7500. If you would like to know more about it, write for a Varian 520/i brochure.



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CIRCLE NO. 1 ON INQUIRY CARD

Logical Logic Engineers Build With Monitor's Monilogic IC Logic Cards

You may select from over 300 different digital and analog IC circuit cards to build your system. The MONILOGIC line consists of A/D's, D/A's, code converters, amplifiers, counters, oscillators, gates, inverters, expanders, delays, matrix gates, numerous interfaces, registers, flip-flops and reference voltages. Also, there are card file drawers and chassis, power suppliers and associated hardware. Request details.



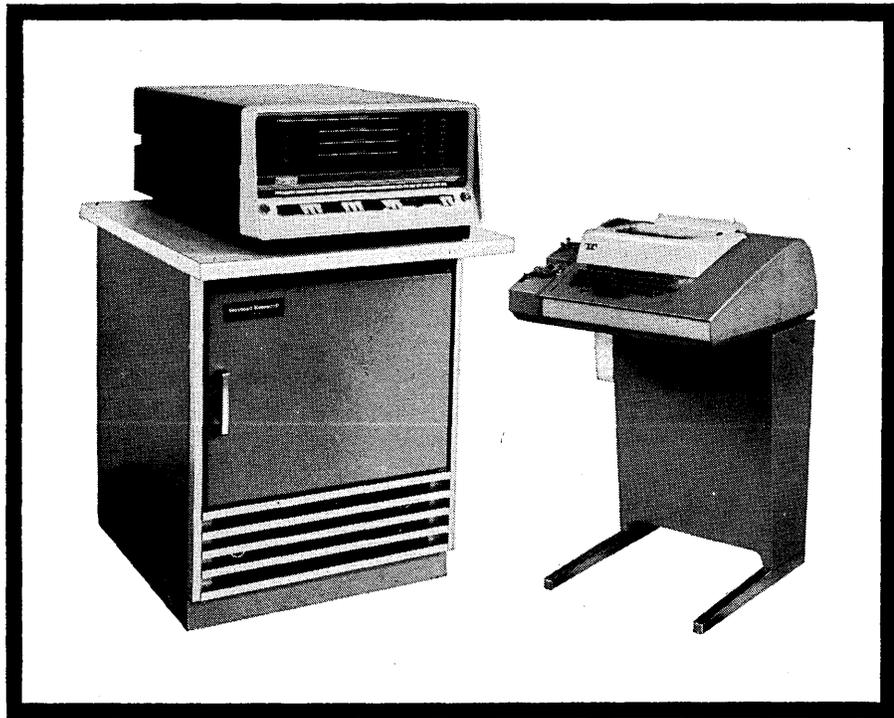
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SYSTEMS

an AYDIN company



CIRCLE NO. 2 ON INQUIRY CARD



Fact:

**In 60 minutes
you can add 131,072 words
to your small computer's memory**

Order a VRC 1104S Drum Memory System *now* for your PDP-8, 8/S or 8/I computer. (Yes, the 1104S is compatible with the new 8/L.) When the system arrives in 90 days, follow the simple installation procedures in the accompanying manual. In one hour you will have connected the 1104S to the computer, run the drum diagnostic tape (included with the manual) to test every bit of the 131,072-word capacity, and have the system on-line.

Interfacing the 1104S is that easy. And it's available in three versions: PCT for program-controlled transfers; DCT for 3-cycle data break; and DMAT for direct mem-

ory access transfers. You get programs for transfer of single pages or entire fields, and non-destructive drum diagnostic routines. Single-word addressing simplifies programming. And don't overlook the benefits of proven VRC reliability: design life, 100,000 hours of operation; MTBF, 15,000 hours; error rate, 1 in 10^{13} bits.

Cost? Modest. A PCT version—with 131,072-word capacity, 8.7msec average access, and three transfer programs plus diagnostic program—is yours for \$9,950. So place your order today . . . and start dreaming up new uses for a small computer that can think big.

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...so is

**Vermont Research
CORPORATION**

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MEMORIES
and
SYSTEMS**

When it comes to engineering opportunities (and the good life, North Country style), the place to come is Vermont Research Corporation. For specific information contact:

RICHARD A. STOVER
Vice President-Engineering

CIRCLE NO. 3 ON INQUIRY CARD

COMPUTER DESIGN/NOVEMBER 1968

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Circulation
over 42,000

COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

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- 52 **DIGITAL INTEGRATED CIRCUIT DESIGN TECHNIQUES**
H. R. CAMENZIND
The design techniques discussed in this article will help the designer to more easily understand and use digital IC's.
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- 77 **ECONOMY OF SCALE AND SPECIALIZATION IN LARGE COMPUTING SYSTEMS** J. R. COX, JR.
There are some economies of scale within the framework of present computation centers. Even more dramatic are the economies of specialization.
- 82 **A METHOD OF DATA TRANSMISSION REQUIRING MINIMUM TURNAROUND TIME** P. E. PAYNE
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Reader Service Card opposite page 132

If you're building any computer except a Computer, you need CT μ L.

CT μ L integrated circuits will give you more speed for less money than any other ICs. They're perfect for process control systems, test instrumentation, central processing units, computer peripheral equipment — just about anything short of an airborne computer.

Keep it in the family.

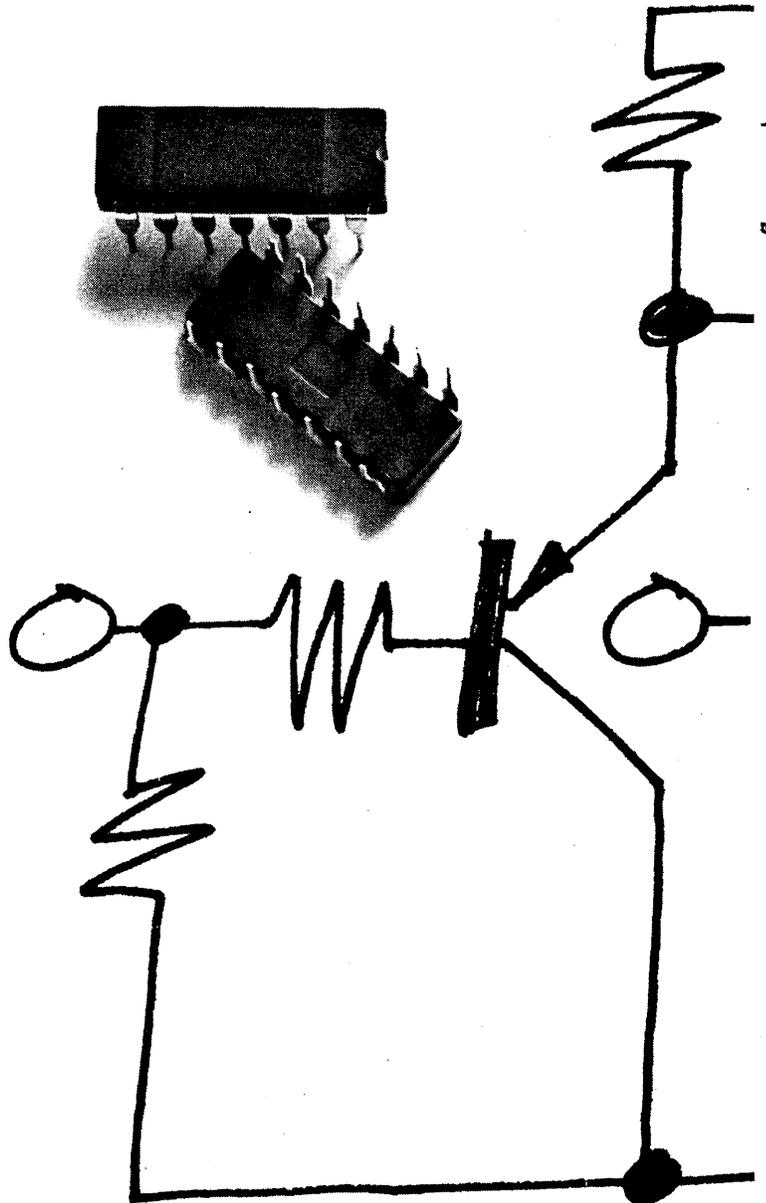
You can build a complete digital logic system with Fairchild's family of CT μ L devices. We have gates, flip-flops, inverters and memory circuits. A dozen different devices that make a computer easy to package. And, you'll need only about 80 percent as many packages as required with TTL.

You get out of it what you put into it.

The key CT μ L characteristic is non-saturating logic. That means you get fast gate propagation delay (typically 3nsec) with slow rise and fall times (typically 6nsec). So, there's no need for transmission lines or complex packaging. You can build an entire computer with normal two-sided circuit boards. Also, CT μ L can handle signal swings as large as 3V. It also provides typical noise immunity of 500mV.

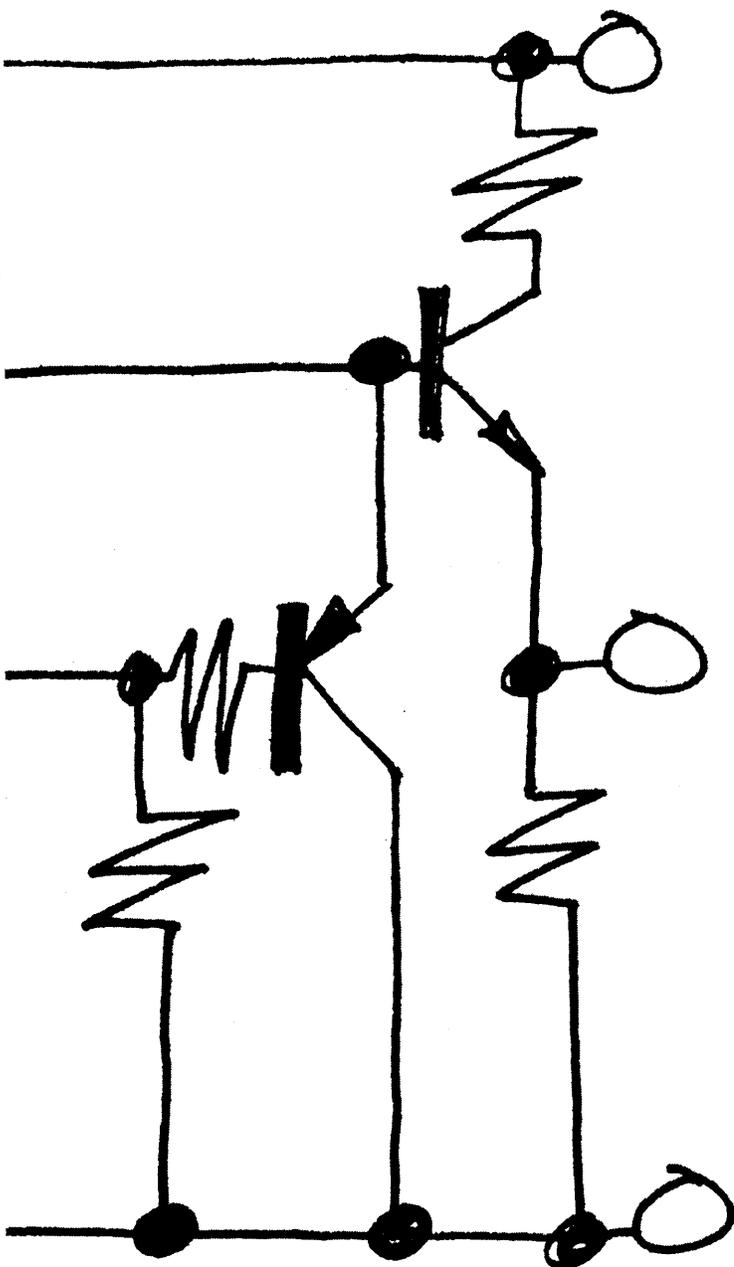
What we'll do for an encore:

MSI CT μ L will be out before the year ends. CT μ L-II will be out even sooner, offering improvements like gate propagation delay of 1.5nsec. (typical, loaded) and a buffer and



The world's largest manufacturer

inverter with propagation delays of 5nsec, compared with 12nsec in standard CT μ L. And, the new MSI and CT μ L-II circuitry will interface beautifully with all these standard CT μ L devices:



Device	Price (100-999)
9952 Dual NOR Gate	\$1.25
9953 Triple AND Gate	1.25
9954 Dual Four-input AND Gate	1.25
9955 Eight-input AND Gate	1.25
9956 Dual Buffer	1.25
9957 Dual-rank Flip-flop	2.00
9964 Dual Three-input and Single-input AND Gates	1.25
9965 Quad Single-input AND Gate	1.25
9966 Quad Two-input AND Gates, one pair with OR-tie	1.25
9967 JK Flip-flop	2.00
9968 Dual Latch	2.00
9971 Quad Two-input AND Gates with OR-tied pairs	1.25
9972 Quad Two-input AND Gates, one pair with OR-tie	1.25

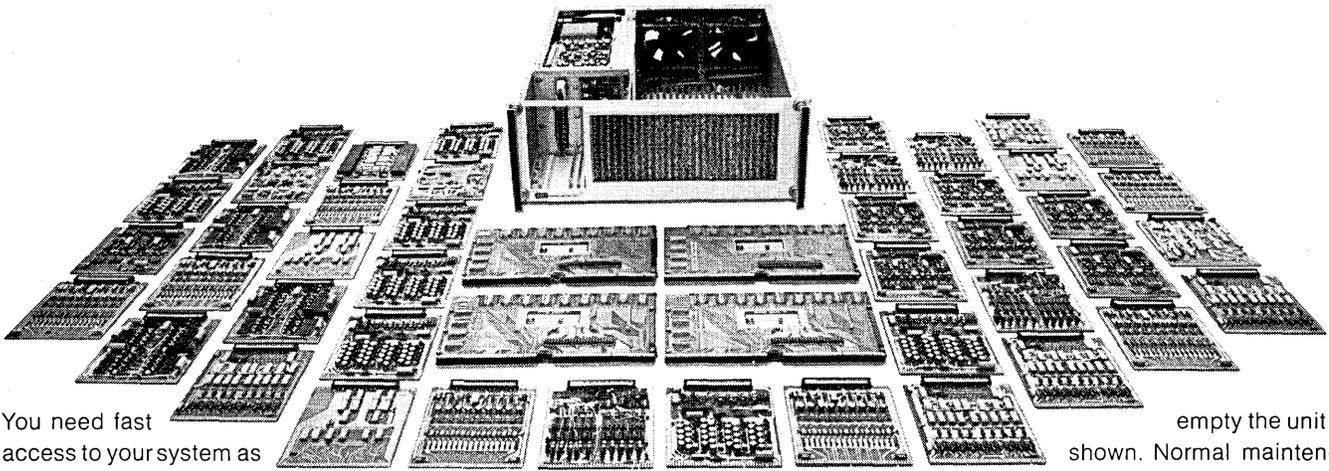
If you want CT μ L-II in sample quantities, call Fairchild. If you want standard CT μ L in production quantities, call a Fairchild distributor. He has everything you need to build any computer. Even a Computer.



Fairchild Semiconductor / A Division of Fairchild Camera and Instrument Corporation / 313 Fairchild Drive, Mountain View, Calif. 94040 (415) 962-5011 / TWX: 910-379-6435

of LSI admits there's another way:

Access time: 6 minutes



You need fast access to your system as well as your information.

Our new medium capacity memory system delivers both. The NANOMEMORY™ 2000 Series has unequaled reliability and operating margin. It packs up to 295,000 bits of information into a single 2½ cubic foot module (7" x 19" x 21.5"). Multiple units can be used for larger capacities. The basic package includes the power supply, 2½D-organized magnetics, IC electronics and an optional self tester. It does everything bulkier systems do—but does it in less space while delivering cycle times as fast as 650 nanoseconds and access times to 350 nanoseconds. □ Should you need it, physical accessibility is just as outstanding. It took six minutes to

empty the unit shown. Normal maintenance is even faster. All

stacks and electronics are mounted on functionally-oriented plug-in cards.

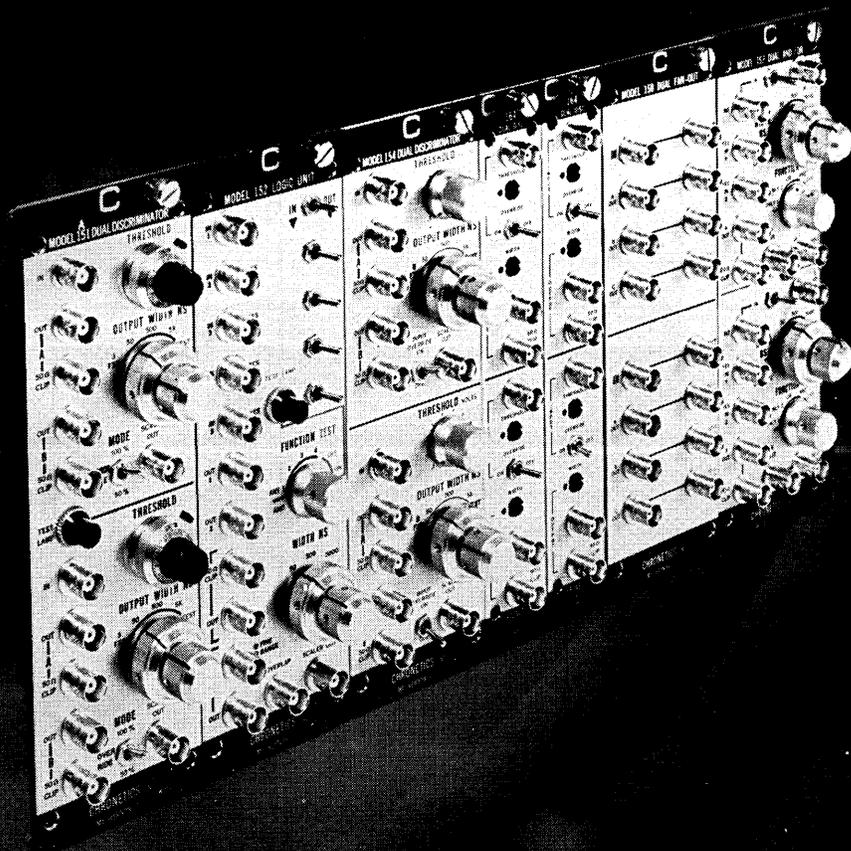
One minute to open the case, then pull a card for easy access to any component. For added convenience, standard parts readily available from your local distributor are used throughout. □ For access to more information on our NANOMEMORY 2650 (650ns cycle time) and NANOMEMORY 2900 (900ns cycle time), please write us.

EM **electronic memories**

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CIRCLE NO. 5 ON INQUIRY CARD

The Brain Picker



Nanologic 150 Can Measure All Of Your Fast Memory's Output Parameters Automatically and Simultaneously At Scan Rates Up To 100 MHz With One Look Per Bit Regardless Of Plane Size.

You can use Nanologic 150 to measure output width, propagation delay, rise time, fall time and amplitude directly on your memory's sense line output. You can measure all these parameters simultaneously and automatically on a Go No Go basis or retain quantitative information. Width, delay, rise and fall times can be measured to within ± 35 psec with 50 psec stability. Peak amplitude and amplitude tolerance can be measured to within 1%.

Nanologic is a real time amplitude and time measurement system capable of operating repetitively at rates in excess of 200 million times per second. Use of strobing modules preceding the measurement modules allows selection of intervals of interest to 3 ns or multiplexing of several sense lines to alternate measurements.

Upwards of seventeen multi-function modules are available "off the shelf". Cost? Well, it depends upon system complexity; it's a modular system. We're sure, though, you'll be pleasantly surprised.

Chronetics' Nanologic is the most widely used and thoroughly proven instrument system of its kind for data acquisition and reduction in nuclear physics research. Eight years of continuous development and use establishes Nanologic as the most stable, most reliable, highest performing, highest quality...

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**I'm Edson deCastro,
President of Data General.**

**Seven months ago we started the richest new
small computer company in history.**

**This month we're announcing our first product:
the best small computer in the world.**

Data General wasn't started on a shoestring.

My associates and I had been with a company where we developed the most successful line of small computers in the business. And we knew the only way to go was big. Right from the beginning.

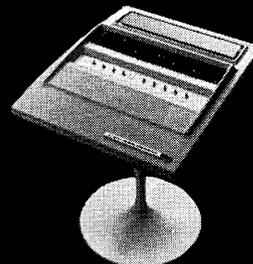
So we got the financing to be big. To build a plant that'll knock out these computers by the hundreds. To develop a large enough technical service organization to really support our customers.

And we designed a revolutionary computer. The NOVA.

Other small general purpose computers are built around an obsolete architecture based on an old technology. NOVA is built around medium scale integration. It's the first with multi-accumulator/index register organization. The first with read-only memory you can program the same way you do core. The first low cost machine that allows you to expand memory or build interfaces within the basic configuration.

One more thing. The price with a 4096 16-bit word memory and Teletype interface is only \$7950. And we're offering the best discounts in the business.

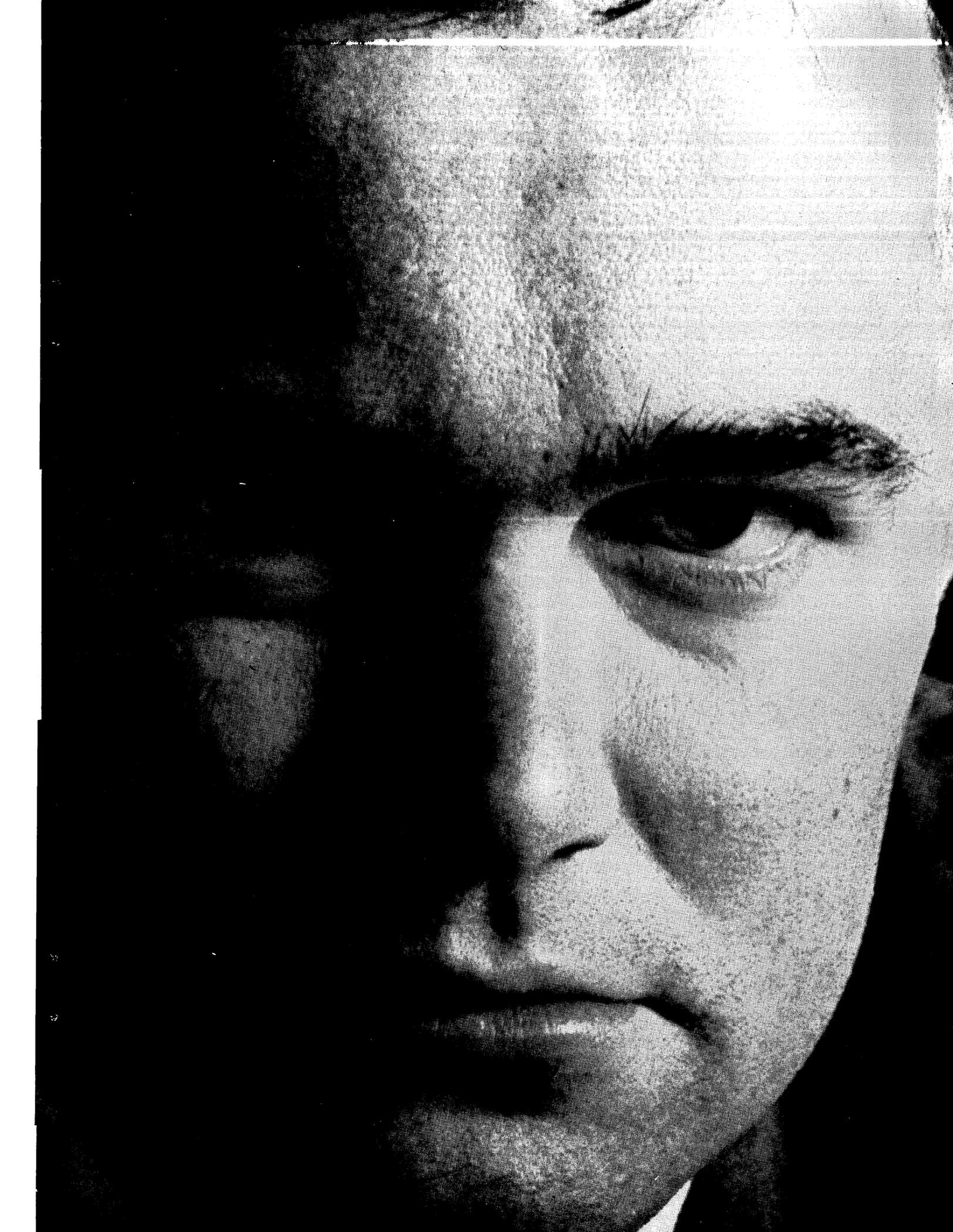
Because if you make a small inexpensive computer, you have to sell a lot to make a lot of money. And we intend to make a lot of money.



**DATA GENERAL
CORPORATION**

275 Cox Street, Hudson, Mass. 01749

Specifications: NOVA is a 16-bit word general purpose computer. It has four accumulators, two of which may be used as index registers. It offers a choice of core or read-only memory of 1K, 2K, 4K, 8K, and up to 32K 16-bit words (or twice that many 8-bit bytes). NOVA comes in the desk top console shown here or a 5 1/4" tall standard rack mount package. Both the desk and rack versions can hold up to 20K 16-bit words of memory or interface for a large number of peripheral devices. NOVA has the most flexible I/O facility ever built into a machine of its class. It will include a high-speed Data Channel and automatic interrupt source identification as standard equipment. Write for more information today. Or see us at the Fall Joint Computer Conference on Wednesday.



TURN AROUND & TUNE IN TO DATA DISC'S New Alphanumeric/Graphic Display

DATA DISC, INC. introduces a low-cost, high-performance, alphanumeric and graphic display system that displays:

- characters in UPPER and lower case
- black on white or **white on black**
- superscript and subscript
- 2560 characters (96 ASCII set)
- 4080 CHARACTERS (64 ASCII set)
- graphics on a 512 x 480 matrix

COST
PER
TERM.

This time-shared display system can generate new displays at the rate of 60 pages per second. The control unit and CRT refresh disc memory can serve up to 128 display terminals, which contain standard TV monitors.

DATA DISC, INC.'s Television Display System (TDS), with only a few terminals, costs less than alphanumeric-only systems. With additional terminals even greater economy can be realized.

NO. OF TERMINALS

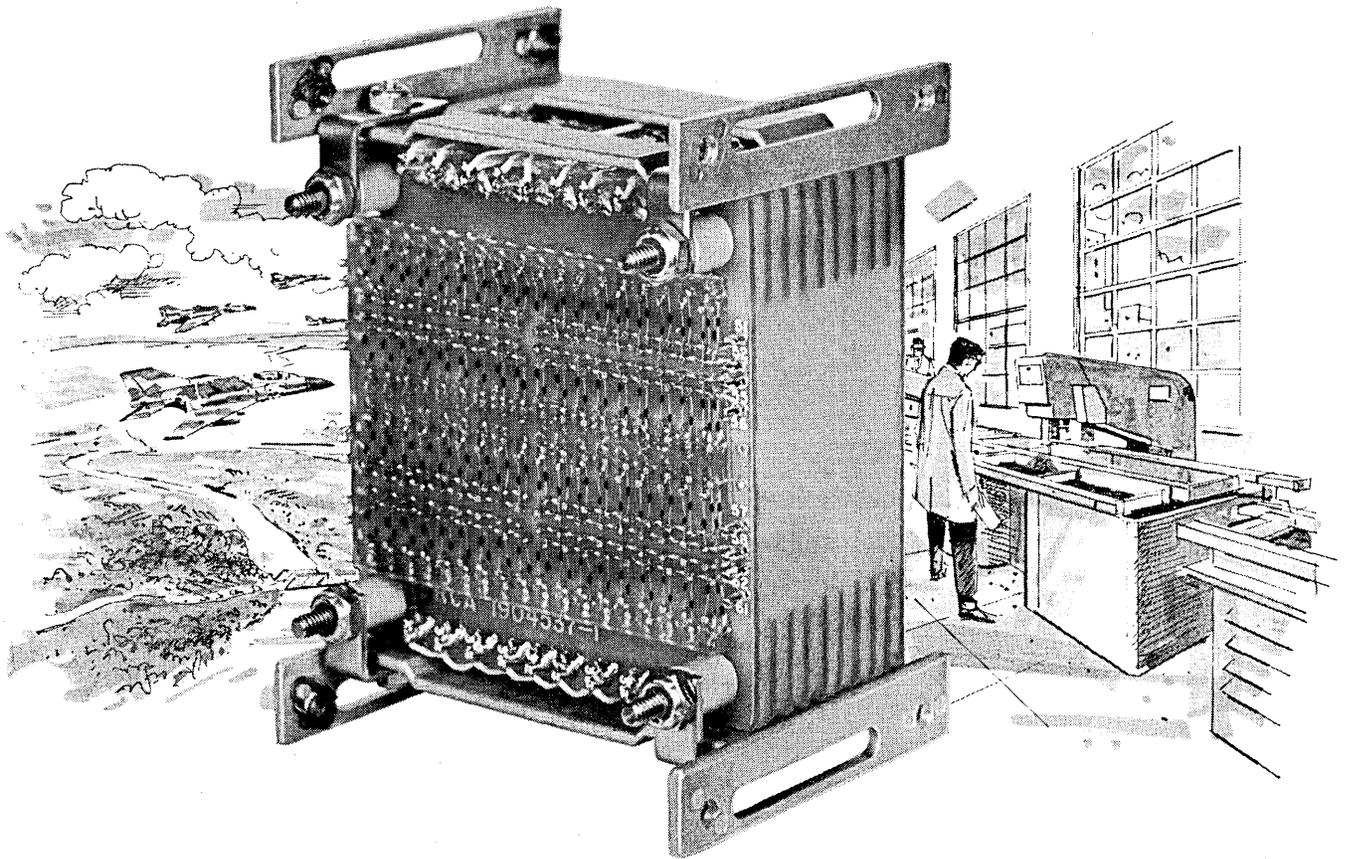
See this equipment at Booth L-3 during the Fall Joint Computer Conference. Or, contact William Stevens, Vice President, DATA DISC INC./Display Division, 1275 California Avenue, Palo Alto, Calif. 94304 (415) 326-7602

You just can't find
a more reliable
high-density
memory stack
than you can
get from RCA

Reliability is important! Availability, too! So we use modular construction for flexibility, improved reliability and faster delivery of storage capacities from 4K x 6 to 4K x 32. And this type of construction offers the highest storage capacity for minimum size.

Improved reliability is inherent in the design, because we use an absolute minimum number of solder joints. Mean-time-between-failure has been calculated as 1.25×10^6 hours.

So *challenge* us on delivery. May we arrange for a demonstration for your specific application? Contact your RCA Field Representative for details. Or call Marketing Department, (617-444-7200, Ext. 242), RCA Memory Products Division, Needham Heights, Mass. 02194. For Technical Bulletin MP317, write RCA Electronic Components, Commercial Engineering Department F-ZB-11, Harrison, N.J. 07029



RCA

CIRCLE NO. 9 ON INQUIRY CARD

The Ferroxcube FI-3

The World's First Plug-Out Memory

The FI-3 comes as a complete memory system ready to plug-in or you can plug-out those capabilities which exist within your system.

The flexibility of the FI-3 is limited only by the versatility of the system with which it will be used.

If your system already has +6 volts or -12 volts or both, we'll sell you the FI-3 without the plug-in power supplies.

If your system requirement is for a self-contained memory, we'll plug-out the 19-inch rack-mounting chassis.

If you don't need 8192 words by 18 bits, we'll plug-out enough mem-

ory to give you only 1024 words by 6 bits or some capacity in between.

In fact, if you have the capability, we'll plug-out everything but the stack and give you the drawings for the rest.

For those busy engineers who want us to do the work, we'll be glad to plug-in all the modules and IC logic cards and supply an FI-3 with:

- 3 μ sec full cycle time
- 2 μ sec half cycle
- multimode timing with full, half or split cycle
- address register/counter
- random or sequential operation

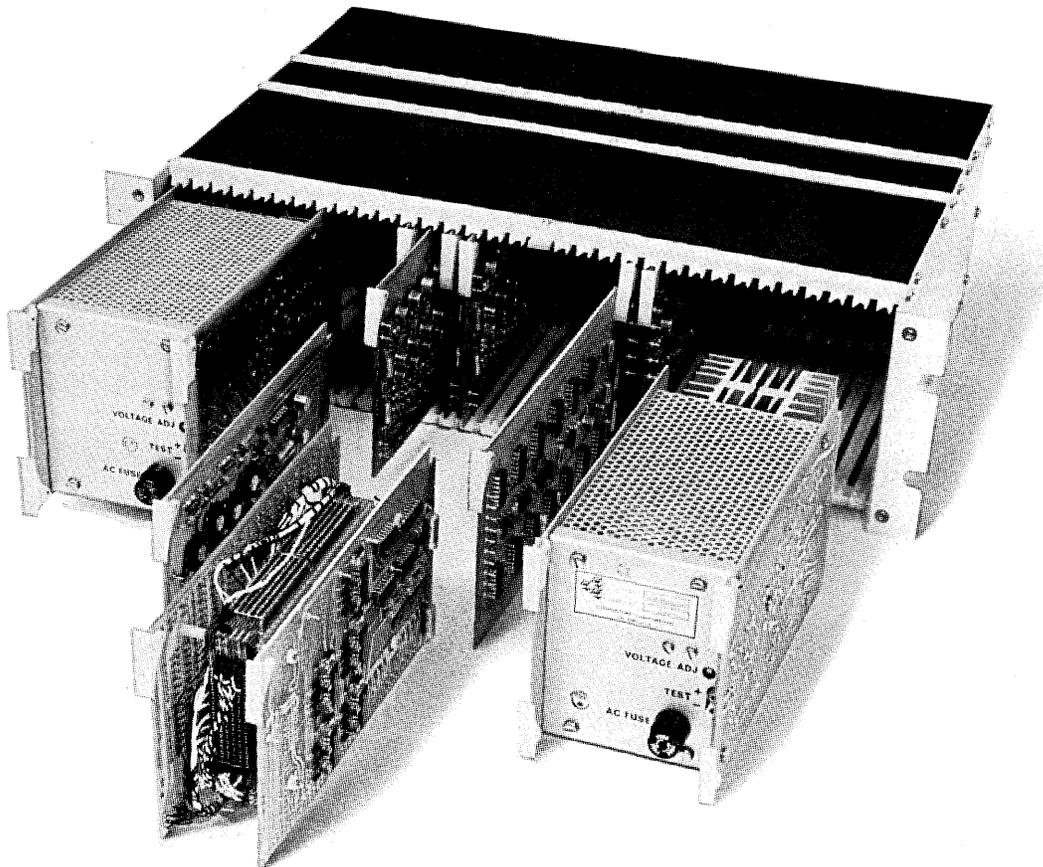
- memory retention
- 3D, 4-wire construction
- 30-mil low temperature coefficient cores

MTRR is enhanced by having only five card types. Field adjustments and temperature compensation are unnecessary. Over 100 catalog-standard FI-3 models to choose from.

And we'll do it in less than 60 days for as little as \$2,000 per unit. The lowest price in the industry.

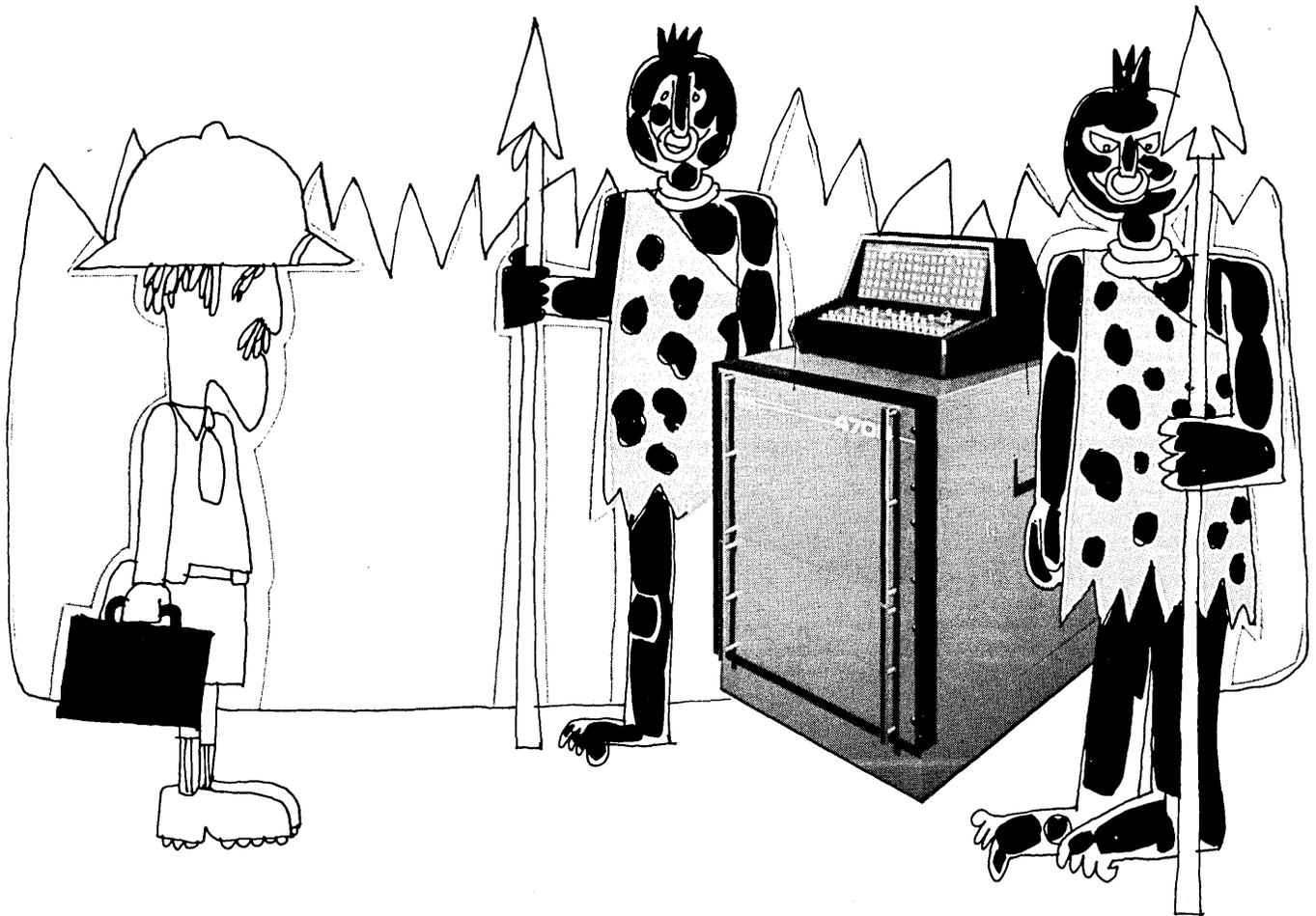
Write to Jack Buckwalter.

Ferroxcube 
Systems Division, Englewood, Colorado



Baltimore—Eastern Components, (301) 322-1412; Burbank, Calif.—(213) 849-6631; Englewood, Col.—(303) 771-2000; Lansing, Mich.—(517) 482-7140; Minneapolis—(612) 820-7955; Northlake, Ill.—(312) 261-7880; Philadelphia—Eastern Components, (215) 927-6262; Phoenix—(602) 264-3120; San Francisco—Wm. J. Purdy Agents, (415) 863-3300; Saugerties, N.Y.—(914) 246-2811; Union, N.J.—(201) 964-1844; Waltham, Mass.—(617) 899-3110; Winston Salem, N.C.—(919) 725-6306; Toronto, Ontario—Philips Electron Devices, Ltd. (416) 425-5161.

CIRCLE NO. 10 ON INQUIRY CARD



Who said you can't buy more 16-Bit computer capability for less than \$30,000?

SCC Says you can — and you don't have to be a Dr. Livingstone to find it.

Our NEW 4700, 16 bit, 920 Nanosecond Digital Computer is the first small machine with a throughput rate fast enough to handle those tough jobs... It costs less than \$15,000 for the basic machine.

The 4700 can free a larger system for more important work. It can be the brains behind a satellite communications network... a message switcher or a data terminal.

The 4700 can control processes while your engineers check out programs simultaneously. It gives you an economical way out of the communications bottleneck... a complete remote capability at a price you can afford.

Compare the 4700 with other computers.

You can spend \$30,000 for a 16-bit model that expands from 4K to 32K. The 4700 expands from 4K to 65K.

You can pay \$30,000 for a 16-bit machine with a 790 nanosecond cycle time. The 4700 does it in 920 nanoseconds, but it only costs half the price.

You can spend \$30,000 for a 16-bit machine and not get hardware double precision and floating point arithmetic. The 4700 offers this option for only \$5,000.

Furthermore, we don't know any 18-bit orange that dares to compare itself with our 16-bit apple.

"SEE US AT BOOTH 201-202-203 DURING FJCC"

Whatever Your Computer Application — Be Sure You Talk With SCC Before You Buy



Scientific Control Corporation

P.O. Box 34529 • Dallas, Texas 75234 • 214 — 241-2111 • TWX 910-860-5509

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El Monte, Calif.

CIRCLE NO. 11 ON INQUIRY CARD

A new Ampex computer tape drive for \$3500.* Wow!

The new Ampex TM-Z is a complete computer-class tape memory system (including read/write electronics) that best fulfills the need for a low-cost, high performance, low speed unit for your computer, data terminal or data acquisition system. Completely computer-compatible, it conforms to all requirements of IBM and ASCII 7- and 9-track formats.

Simplicity of design results in the utmost in reliability and easy maintenance. This completely new, ready-to-plug-in tape memory system features the same precision as the higher speed Ampex TM-7 and TM-16 tape memories.

PERFORMANCE CHARACTERISTICS

Tape Speeds:

Standard speed is 24 inches per second, Read/Write (19.2 kHz transfer rate at 800 cpi). Any single tape speed between 10 and 24 ips can be obtained by utilizing a continuously variable adjustment.

Tape Width and Thickness:

½-inch width, 1.5 mil by 2400 feet (732 meters)

Recording Density:

Standard: 556 and 800 cpi. Optional densities available.

Recording Formats:

Standard: 9-track ASCII 0.6 inch IRIG (IBM 360, 2400 Series compatible).
Optional: 7-track, NRZ 0.75 inch IRIG (IBM 7330, 729 Series compatible).

Start/Stop:

Tolerances permit bilateral interchange of tapes with equipment compatible with IBM and ASCII 9-track standards.

Input Voltage and Frequency:

Voltage: 100-250 volts RMS with transformer taps.
Frequency: 48 to 63 Hz.
Consumption: Average, 400 watts. Peak, 500 watts.

Interface Characteristics, Data and Control Lines:

True: Logic "1" = 0.2 (-0.2 + 0.2 volts)
False: Logic "0" = + 3.3 (- 0.9 + 1.7 volts)
Logic: TTL units employed

Dimensions:

Complete tape memory system, including self-contained data electronics, can be mounted in a standard 19" or 24" rack.
Height: 24"
Width: 19" or 24"
Depth: 17" overall (14½" rack depth)

Weight:

100 lbs. maximum

Functional Modes (selective):

1. Write Forward, Read Forward
2. Read Only Forward
3. Read Only Reverse

Options:

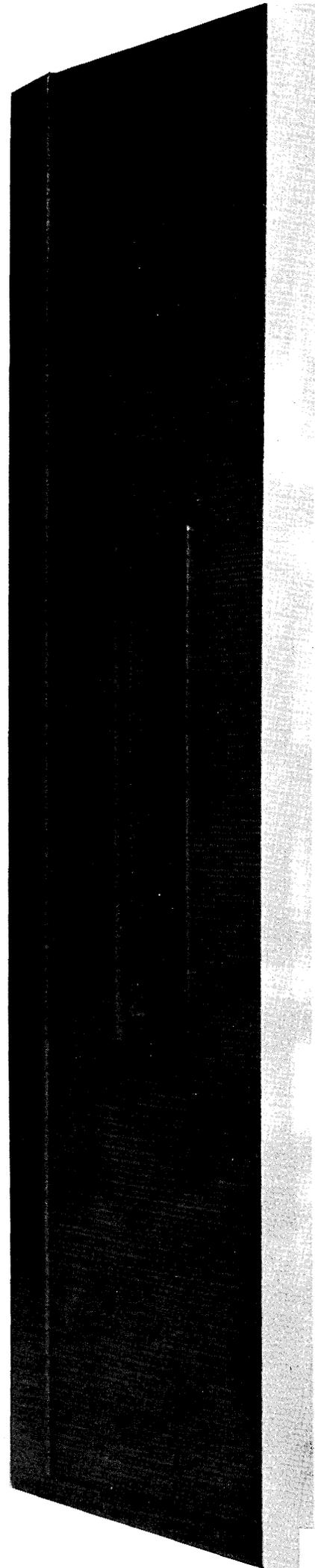
1. Vertical Parity Check
2. Vertical Parity Generate
3. Write Echo Check
4. Longitudinal Parity Check
5. Longitudinal Parity Generate

See our TM-Z at the FJCC in San Francisco.
Or, write for more information:
Ampex Corporation, 401 Broadway,
Redwood City, California 94063.

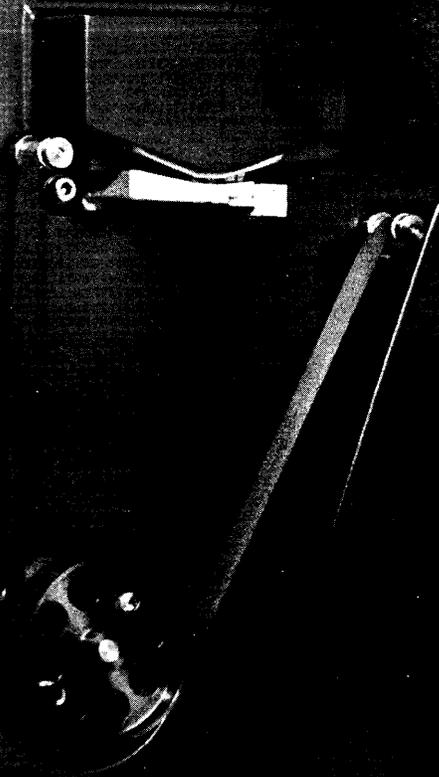
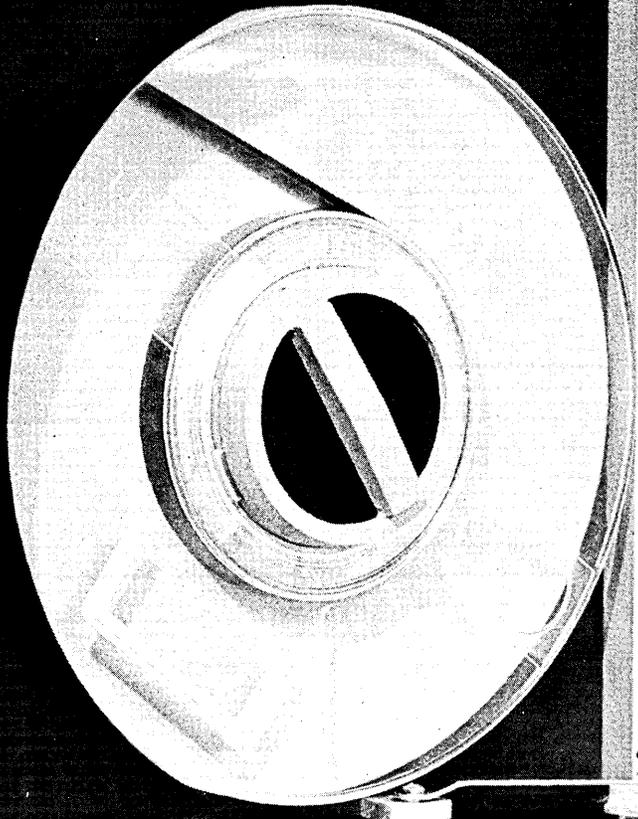
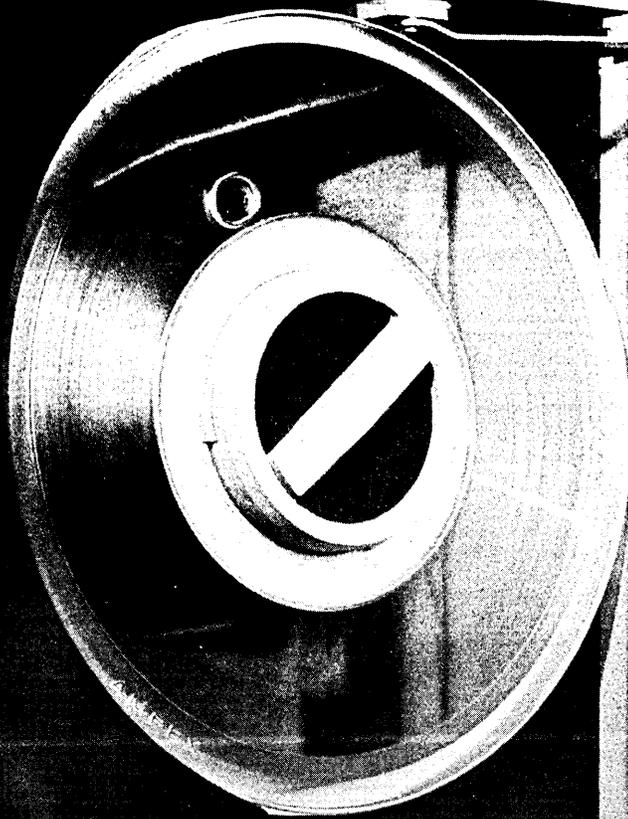
**AMPEX**

CIRCLE NO. 12 ON INQUIRY CARD

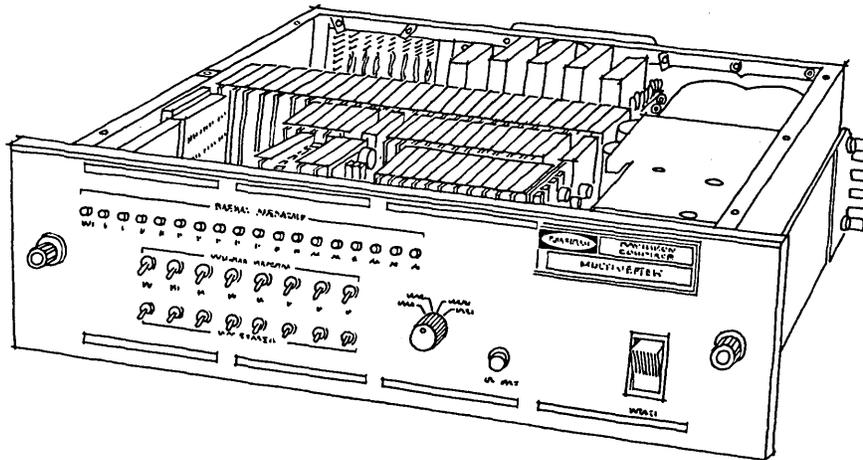
*Price including all read/write and control electronics, in lots of 100 per year.



SEARCH	STOP	REVERSE
PAUSE	FAST FORWARD	FORWARD
PLAY	FILE PROTECT	REMOTE



Raytheon Computer's MULTIVERTER III.® 100 kHz throughput.



Faster throughput is just one of the benefits offered by the MULTIVERTTER III, newest version of our widely-used "analog front end in a box." Multiplexer capacity can be up to 128 channels, the sample-and-hold amplifier has a 2 microsecond settling time and 50 nanosecond aperture, and the converter is our new 15-bit, 0.01% ADC 100.

- Options include**
- IC registers hold up to 512 bits of buffer storage
 - Controls and indicators
 - ADC available as separate unit

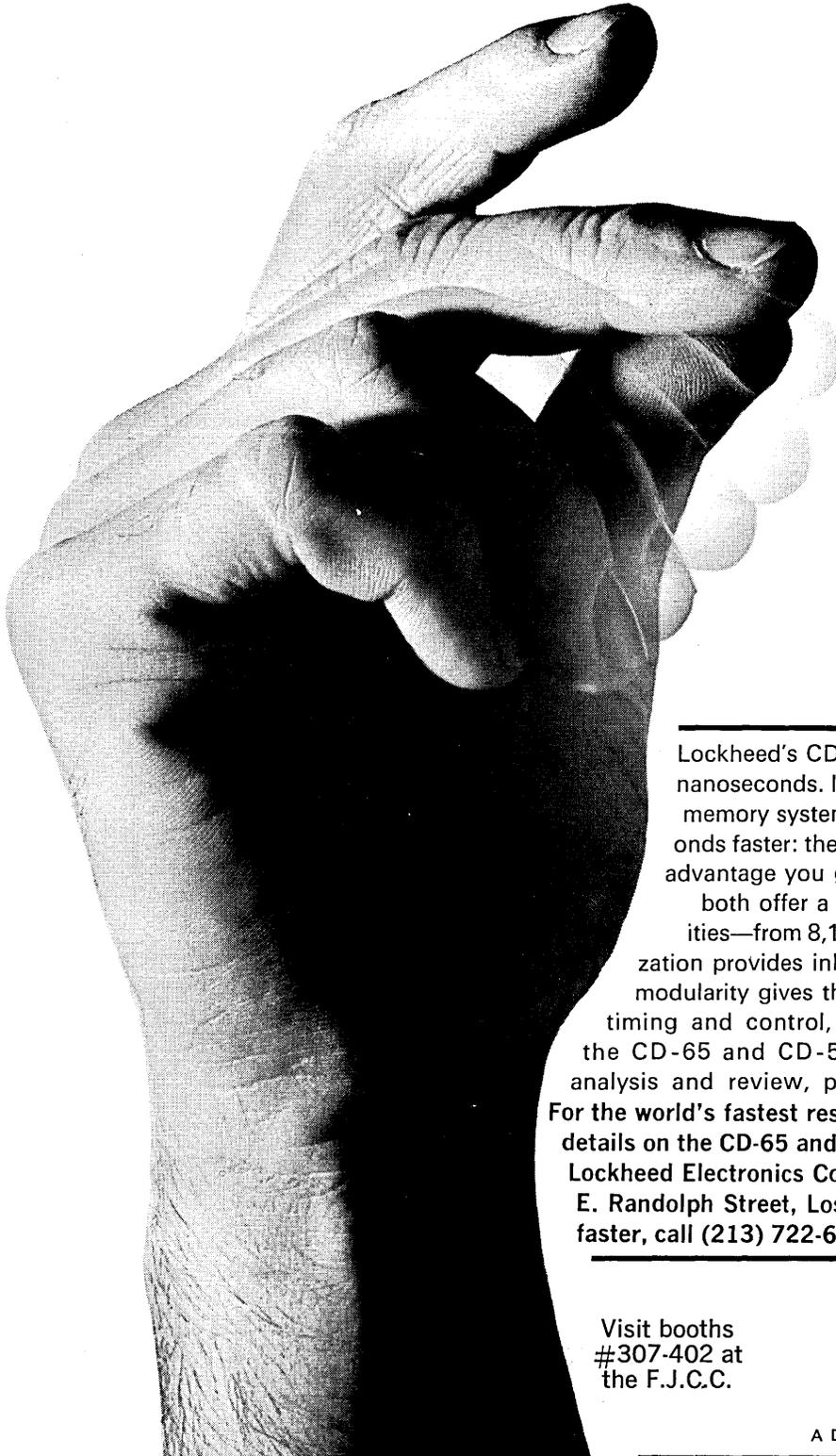
- MUX available as separate unit
- Wiring for additional logic
- 32 channels simultaneous sample-and-hold.

However you want it, the sooner you write or call us, the sooner you'll have it. Raytheon Computer, 2700 S. Fairview St., Santa Ana, California 92704. Phone (714) 546-7160. In Europe and the Mid-East, write Raytheon Overseas, Ltd., Shelley House—Noble Street, London E. C. 2, England, Phone: 01 606 8991, Telex 851-25251. Ask for Data File CB-162.



CIRCLE NO. 13 ON INQUIRY CARD

Lockheed has in production the world's fastest 2½D memory system.



**And one
even
faster.**

Lockheed's CD-65 completes a memory cycle in 650 nanoseconds. It's the world's fastest production 2½ D memory system... except for one that's 150 nanoseconds faster: the Lockheed CD-50. □ Speed is just one advantage you get with the CD-65 and CD-50. They

both offer a wide range of standard storage capacities—from 8,192 to 65,536 words. Their 2½ D organization provides inherently high operating margins. Total modularity gives them highly flexible interface capability, timing and control, and storage capacities. Plus, both the CD-65 and CD-50, subjected to worst-case design analysis and review, perform with exceptional reliability. For the world's fastest response with technical material — full details on the CD-65 and CD-50 — write to: Memory Products, Lockheed Electronics Company, Data Products Division, 6201 E. Randolph Street, Los Angeles, California 90022. Or even faster, call (213) 722-6810.

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At last, fourth-generation computer designs and highly-sophisticated instrumentation designs have become a reality, thanks to the ultra-high speeds that are now possible through the current mode logic of MECL III!

Three different circuits in this new line of emitter-coupled devices are currently available for evaluation. MC1060S and MC1062S, dual 4 and quad 2-input gates, offer propagation delay times that are typically *900 picoseconds* when operated into a 510 ohm load. Reduce the load an order of magnitude and the delay time is only 1.1 nanoseconds; still twice as fast as any comparable form of logic.

In addition, MC1070S, single phase, type "D" Flip-Flop, provides a toggle/shift frequency that is typically *350 MHz*. And, it can be "tweaked" to higher frequencies by application of an external bias.

The standard MECL III package is a stud-mounted, 15-pin ceramic flat pack. The stud, connected to V_{EE} , is designed to improve heat dissipation.

For further information about MECL III or for individual evaluation units, contact us at the address below. Don't wait another day to begin designing the picosecond logic of tomorrow's fourth generation computers.

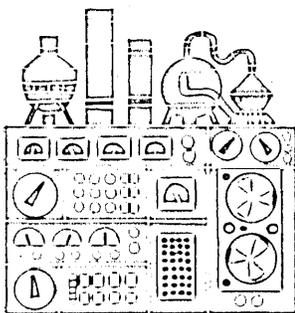


MECL III picosecond logic available in prototype kit

Six MECL III circuits plus a design information brochure are packaged in a useful, compact kit. Devices include two each of the three circuits described here. The advance information brochure contains device specifications plus design rules and applications information. The entire package is available through your Motorola Semiconductor Representative for \$154.00 (any quantity).

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INDUSTRY NEWS

FREQUENCY HOPPING DIGITAL DATA MODEM SUCCESSFULLY DEMONSTRATED

— Experimental tactical communications equipment which permits simultaneous access to satellite relays by many ground, airborne, shipboard, and vehicular terminals, has been successfully demonstrated by Sylvania Electric Products Inc., Buffalo, N.Y.

Known as a digital data modem (modulator-demodulator), the device breaks up the information output of a teletype into a sequence of pulses, according to Leonard E. Gough, Director of Engineering for the Central Division of Sylvania Electronic Systems.

By hopping the pulses over many frequencies, the modem permits simultaneous access to a satellite by several tactical terminals. Because terminals employ various pulse pat-

terns, the hopping technique allows many messages to be transmitted simultaneously over the same band of frequencies.

The modem functions as a small digital processor, converting radio signals to binary information. This information can be added, subtracted, and multiplied in the same manner that a computer arithmetically processes data. Such a digital technique permits design of highly reliable, solid-state components, utilizing integrated circuits for significant over-all weight and volume reduction.

Installed in a mobile ground terminal, the compact unit was tested on a communications link between Sylvania's engineering laboratories in Williamsville, N.Y., and a second satellite communications terminal in Lexington, Mass. Both terminals

were provided by the Lincoln Laboratory of the Massachusetts Institute of Technology, which designed a modem for the Tactical Transmission System (TATS) under an Air Force-sponsored research and development program.

Two-way communication was demonstrated for two and one-half hours between the two points, a distance of approximately 400 miles, via the Lincoln's experimental satellite LES-5.

"Establishment of the link proved the ability of the Sylvania unit not only to function as predicted, but demonstrated its compatibility with Lincoln's experimental TATS modem," Mr. Gough said.

Sylvania developed its modem for the Tactical Satellite Communications Program (TACSATCOM) under a \$3 million Air Force contract.

PLATED WIRE MEMORY ORDERS INCREASE

— Honeywell's Aerospace Division in St. Petersburg, Fla. reports that orders for plated-wire computer memories have given Honeywell "an encouraging lead" in the military and aerospace memory market that it forecasts will exceed \$200 million by 1971.

"Plated wire has moved from the research and development laboratory to the marketplace," said John W. Anderson, vice president and general manager of the division. "So far this year, Honeywell has received orders totaling several million dollars."

"Plated-wire memories are replacing ferrite-core memories in many military and aerospace computer memory applications because of greater speed, non-destructive read-out capability, lower power consumption and higher reliability, Anderson said.

"These inherent advantages will permit increasing use of plated wire in air, sea and ground applications as improved fabrication techniques lead to lower production costs."

Honeywell's new memories first qualified for use on the U. S. Navy's new Poseidon missile. All Poseidon missile-borne guidance computers will be supplied with plated-wire memories, according to Raytheon, prime contractor to the Navy for prototype production units.

Honeywell's first major sale of plated-wire units to be used in spaceborne telemetry systems was made to Space Craft, Inc., Huntsville, Ala. Space Craft said it will use the memories in telemetry systems for major defense programs as well as on projects for NASA.

Thomas S. Crutcher, market manager for computer memories, said the most recent order came from RADC, Griffiss Air Force Base, N.Y. The contract calls for design and de-

velopment of a plated-wire memory for advanced ballistic missile systems

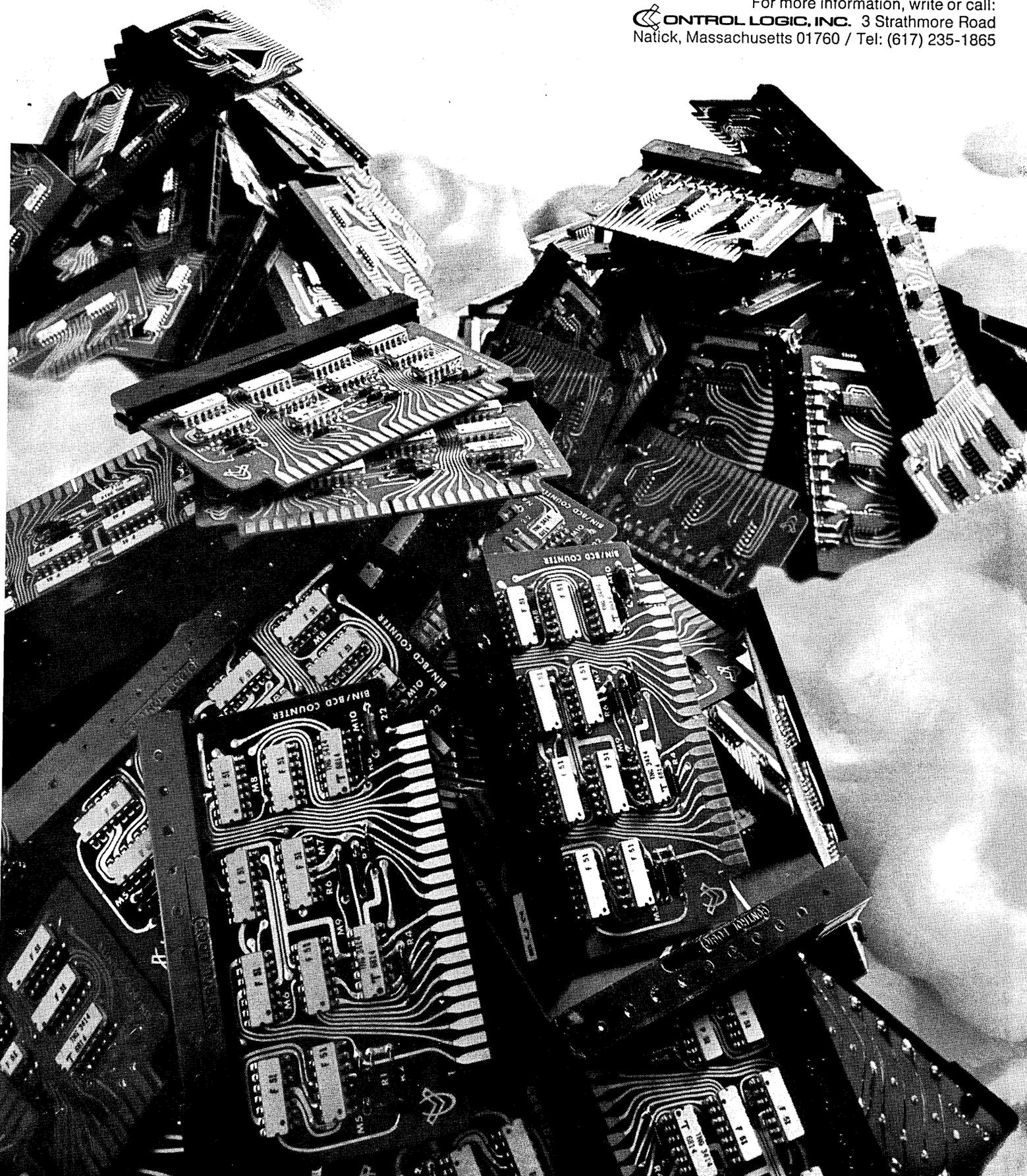
Dr. John N. Dempsey, Honeywell Inc. vice president for research and engineering, said further refinements in plated-wire technology can be expected from work now being conducted at the company's Corporate Research Center in Minneapolis. The research center began plated-wire development work almost five years ago.

"Packaging research already has led to doubling memory capacity in one-half of the volume needed previously," Dempsey said. The four-to-one increase in packaging density has resulted, typically, in 16,000 word-2 bit memories occupying less than 300 cubic inches. Further studies are emphasizing the correlation of magnetic and structural properties of the wire, and changes in these properties during the aging process.

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INDUSTRY NEWS

NAVAL TACTICAL DATA SYSTEM

— Hughes Aircraft Company recent announced it has surpassed the \$125-million mark in the value of computerized shipboard command, control and communication display systems it has built and delivered to the U.S. Navy.

(The seagoing units are designated NTDS, for Naval Tactical Data System.)

Dr. Norman H. Enestein, manager of the company's data processing products division, said the equipment — the first large-scale shipboard application of computer-driven displays — is operating on scores of U.S. and foreign naval warships.

The systems use radars, computers and the "nerve center" data display consoles to provide command personnel with an accurate electronic picture of the immediate tactical situation.

NTDS was originally applied to naval air defense. It has now been given additional roles of air traffic control, tracking of surface and subsurface ships, shore direction bombardment, and rescue coordination.

COMPUTING SYSTEM TO HELP DESIGN AND TEST FLY HELICOPTERS

— Test pilots at Textron's Bell Helicopter Company, Forth Worth, Tex., soon will be able to test fly a newly designed helicopter before it has even been built. The pilots first will fly the "new helicopter" using a mock-up cockpit linked to a specially designed IBM computing system. James F. Atkins, executive vice president, said the computing system will electronically simulate a helicopter in flight, showing pilots and engineers how the aircraft would perform.

The computing system, called a hybrid, combines one digital computer — an IBM System/360 Model 44 — and two analog computers built to IBM specifications by Hybrid Systems Inc. of Houston. George Brooks, supervisor of Bell Helicopter's engineering-computing department, said that the same computing system is helping to develop new helicopter designs and is much faster than conventional computers.

"The new system makes our design work more economical, gives engineers a better insight into their work and greatly reduces the time involved in setting up and solving design problems," he said. "For example, in one recent design study we found the new system provided approximately 100 solutions in the same time that conventional computers would provide a single solution. By making simulated studies on this advanced IBM computing system, we are able to prove the design of a helicopter that will meet a given set of specifications," Mr. Brooks said. "We can even show — before building it — just how it will fly and what it will do."



STANDARD COMPUTER-OPERATING-SYSTEM CONTROL LANGUAGE COMMITTEE FORMED — An ad hoc committee is now being formed under the auspices of the United States of America Standards Institute (USASI) to investigate the need for and feasibility of a standard computer-operating-system control language.

Millard H. Perstein of System Development Corporation (SDC) has been appointed chairman of the committee (USASI X3.4.2F), which becomes a part of the committee structure concerned with data processing, in general, and programming language in particular.

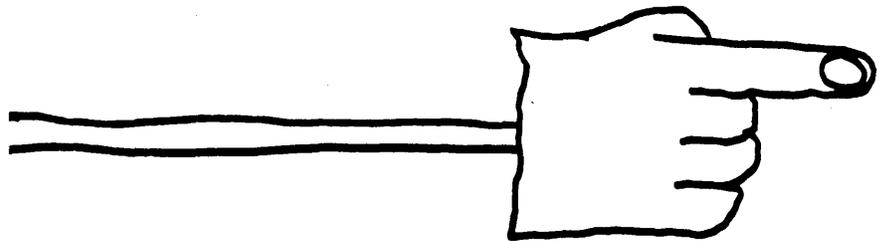
The two-day committee organizational meeting will be held at SDC, Santa Monica, Calif., at 10 a.m. on Tuesday, February 4, 1969. All interested persons are invited to attend the initial meeting.

A wide range of interests will be represented on the committee, including producers and users of computing equipment, terminal equipment, and computing software; trade associations, user organizations and professional societies.

Mr. Perstein said this organizational meeting will be devoted to establishing committee rules, assigning tasks and reviewing work already accomplished in developing a standard.

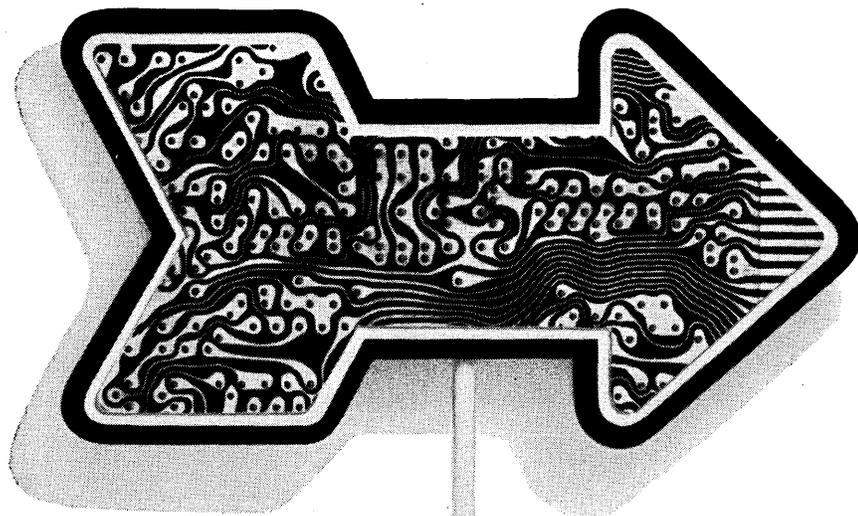
All those who plan to attend are urged to write: Millard H. Perstein, chairman X3.4.2F, System Development Corporation, 2500 Colorado Avenue, Santa Monica, California 90406. Attendees will receive, in advance of the meeting, copies of the committee charter, some of the applicable rules of procedure and working papers concerned with standard computer-operating-system control language.

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Pages 66 and 67

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INDUSTRY NEWS

AFIPS APPOINTS EXECUTIVE DIRECTOR AND PLANS INCREASED SERVICES — Paul Armer, President of AFIPS, has announced the appointment of Dr. Bruce Gilchrist to the newly-established position of AFIPS Executive Director. In this capacity, Dr. Gilchrist will be responsible for developing increased AFIPS services to the AFIPS member societies, governmental bodies and the general public. All AFIPS Headquarters functions will report to Dr. Gilchrist.

Dr. Gilchrist has been a Council Member of the ACM since 1958, serving as Secretary from 1960 to 1962 and Vice President from 1962 to 1964. He was elected Vice President of AFIPS in 1965 and served as President of AFIPS from 1966 to 1968. He currently represents AFIPS on the Division of Engineering of The National Research Council and is the AFIPS liaison representative to the Computer Science and Engineering Board of the National Academy of Sciences.

When making the announcement, Mr. Armer commented that the appointment of a full-time Executive Director marked a key point in AFIPS history, and he looked forward to greatly increased AFIPS activities in many areas. Mr. Armer said that his personal priorities for increased AFIPS activities include providing information services, devoting more effort to educational activities directed at the public, the computer professionals themselves and the government, and, in general, providing a better image for the computer field.

Mr. Armen noted that in its decision to appoint an Executive Director, the Board of Governors of AFIPS recognized that this was just the first step in responsibly meeting a number of long-felt needs. The AFIPS Board has already approved a proposal to start an AFIPS Press to handle the publication of proceedings of AFIPS Conferences and to meet Member Society publishing needs. At its December meeting, the Board will be asked to approve a Public Information program.

Dr. Gilchrist will be responsible for developing plans and programs and assisting in the implementation of approved projects. Mr. Armer emphasized the word "assist," saying that the efforts of volunteers are, and will remain, the mainstay of AFIPS activities.

COMPUTER PROGRAM STORES AND RETRIEVES INFORMATION IN PLAIN ENGLISH— Data Corporation, Dayton, Ohio, has developed an information storage and retrieval system that permits operators to communicate with a computer in plain English instead of in codes or symbols, according to Data board chairman, William F. Gorog.

The system, called Data Central, holds nearly any kind of information in a central data bank. Operators ask questions and can receive answers through a remote console unit or from the computer's high speed printer, as they prefer.

Earlier attempts at similar programs have required complicated codes and symbols or the establishment ahead of time of a filing system that depends on the knowledge of certain key words or symbols to retrieve information, according to Gorog.

Data Central organizes its own internal filing system from information stored in the computer and actually cross files each unit of information by every significant word in it. This means the operator can use any word, except articles like "the" and "a" and other common terms, as a handle to extract information.

The system, originally designed for use with an IBM 360 system, can be adapted to any similar size computer.

COMPUTER LANGUAGE RESEARCH— Computer scientists at the University of Colorado are modifying a number of computer languages to enable a person to conduct a running conversation with the machine while it solves his problem. The project is designed to permit a computer user to interject "what if" and "show me" type questions while a problem is in the computer — and to receive instantaneous replies.

The effort is supported by a \$225,000 grant to CU from the Control Data Corp. (CDC).

Dr. E. Rex Krueger, director of the CU Graduate School Computing Center, where the work is being done, said the project was conceived last spring after the computing center installed a microfilm recorder and a television-like graphic display unit, both of which are tied into a CDC6400 computer. He added that results of the two-year research project "are expected to bring a new dimension to the use of modern computers."

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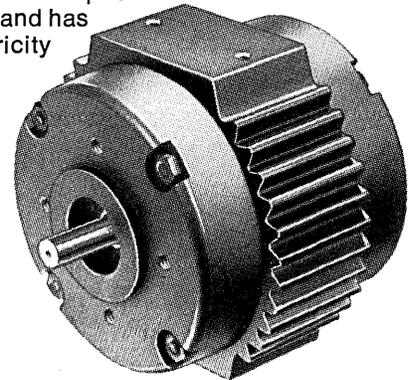
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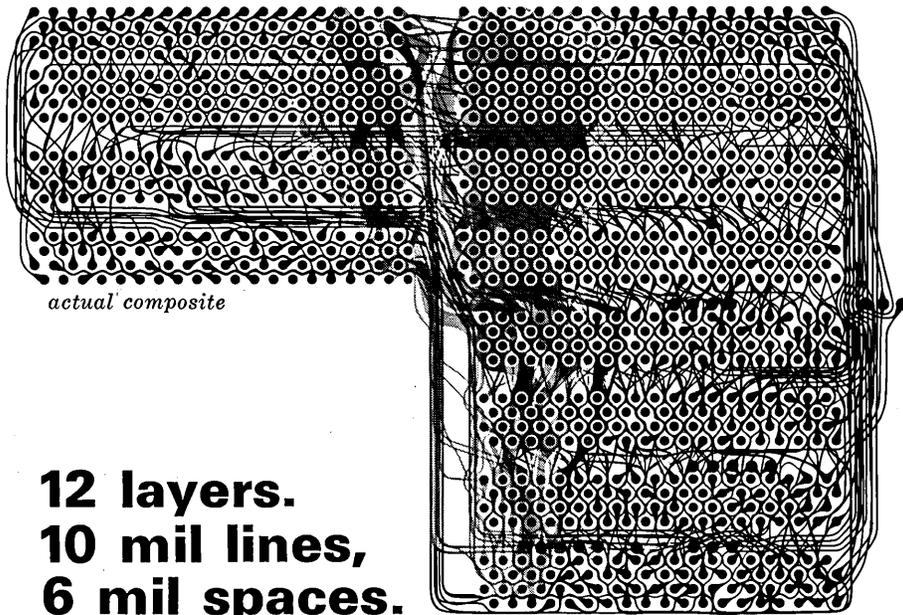
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INDUSTRY NEWS

OLIVETTI UNDERWOOD ENTERS TELECOMMUNICATION EQUIPMENT MARKET—Olivetti Underwood Corporation, New York, N.Y. announced its entry into the telecommunication equipment market in the United States by offering a complete family of teleprinters and on-line real time data terminals.

This new family of equipment includes machines designed for use in conventional telegraphic operations, as well as units specifically designed for connection to computers over telegraph or high speed telephone lines. With over 30 different models available in this new line, Olivetti Underwood is able to provide a machine to fit the many different application requirements encountered in a complete on-line communications system. Its systems specialists are in a position to design a total system satisfying these varying requirements at minimum cost.

In creating the Olivetti Underwood TE 300 Series of heavy duty teleprinters the primary objective was to produce a machine possessing the operating characteristics of an electric typewriter, rather than the somewhat cumbersome characteristics of the conventional teleprinter.

LOCKHEED ELECTRONICS CHANGES DIVISION NAME — Lockheed Electronics Company, Plainfield, N., has announced that its Avionics and Industrial Products Division is renamed the Data Products Division (DPD).

In making the announcement, A. J. Grant, president, stated, "the division's former name no longer describes or reflects its activities, products or services."

Since the Los-Angeles-based division is primarily a manufacturer and developer of computer memory systems, ferrite memory cores, and printed circuit boards, the new name Data Products Division better identifies the division within the electronic data processing marketplace.

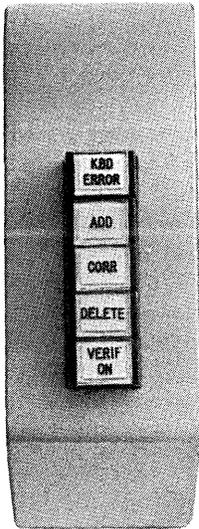
The Data Products Division supplies memory systems and components to most of the major computer companies in the United States and overseas; therefore, it is important that these companies and future customers identify with a manufacturer whose name mirrors its primary products and interest.

DATA COMMUNICATIONS

equipment for on-line,
real-time processing

say bye-bye to boo-boos

The data oriented Teletype Model 35 ACS with verifier helps fill forms fast, without errors



This simple push-button box on the Model 35 ACS (Automated Communications Set) is helping eradicate costly errors in the preparation of forms in hundreds of applications. It's the optional verifier control that literally keeps flying fingers and wandering minds from entering erroneous

characters or omitting vital facts in producing the many and varied forms necessary in keeping a business running smoothly. Forms such as sales and purchase orders; billing records; production; shipping; and distribution schedules.

CORRECTION, PLEASE!

Punched paper tape is really the key to the automated data preparation capability of the 35 ACS. The machine has two tape readers. When verifying, one handles format controls and fixed data—such as company name, address, etc. The other reads variable data—dates, prices, quantities, etc.

The verifier control verifies every character on the variable information tape. Stops operation instantly when the tape is incorrect or the operator leaves out a character, adds too many, or types the wrong one . . . and enables her to take corrective action on the spot. Saves time, too, since the tape verifier concerns itself only with variable information and doesn't go through wasted motions of verifying established fixed data.

FILLS FORM AND VERIFIES AT SAME TIME

Because the fixed data tape also contains the program and format control codes, the form may be entirely filled out while being verified. The two readers alternately interoperate at programmed intervals. Fixed information goes into the proper position on the form automatically. The machine stops, switches over to verification and keyboard operation, so variable data can be added and verified against the prepunched variable data tape.

COMPOSITE TAPE

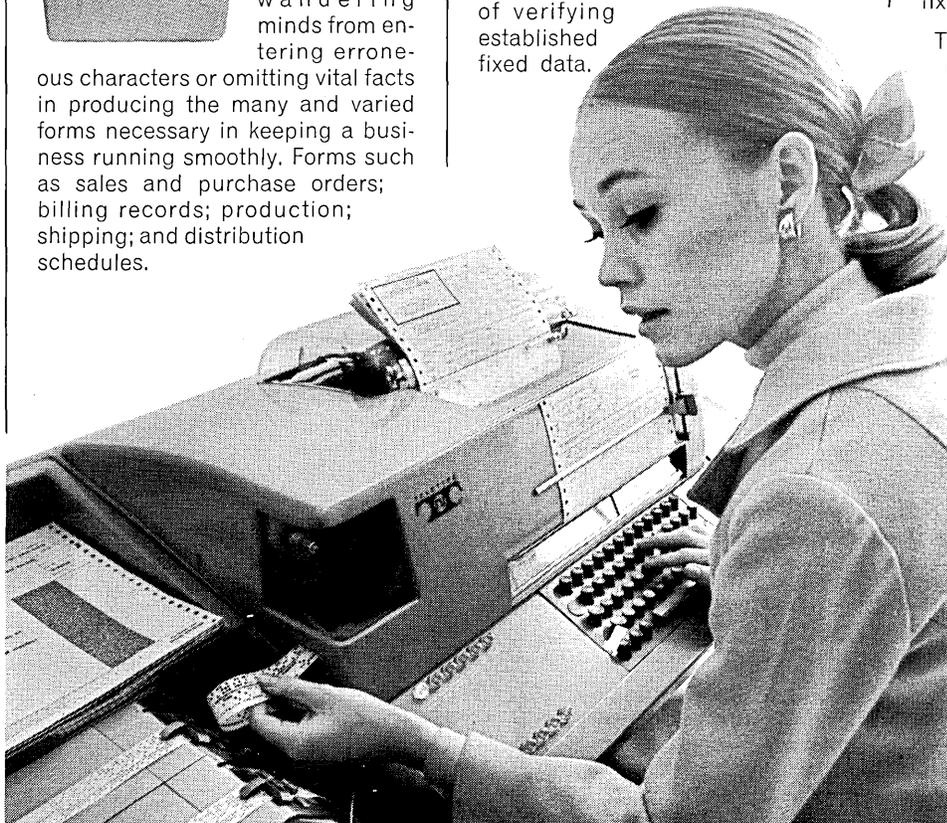
Besides printing the complete business form with carbons, the Model 35 ACS can simultaneously perforate an error-free composite tape containing all or any portion of fixed and variable data desired.

This tape can be used to transmit on-line to remote Teletype equipment; computers; or other business machines. The Model 35 ACS uses the U.S.A. Standard Code for Information Interchange (ASCII).

The Model 35 ACS is available with sprocket feed platen for 8½ inch continuous-fold business forms, or friction feed platen for 8½ inch single or multiple-ply paper.

MORE INFORMATION

If you would like detailed information on this goof-proof form filler, please write Teletype Corporation, Department 71L, 5555 Touhy Ave., Skokie, Ill. 60076.





DEVELOPMENTS

HP Develops BCD and IC-Compatible Low Voltage Numeric Display

Hewlett Packard, Palo Alto, California, has developed a display module which needs only conventional 4-line (8421) BCD and IC-compatible 5 volt power to display any numeral in an array of bright red dots. The flat, sealed module uses gallium arsenide phosphide light-emitting diodes for display, and a monolithic integrated circuit for decoding.

The monochromatic red (6550Å) numerals are produced by selectively energizing a matrix of the light-emitting diodes. The numerals are 0.25" high, but actually appear much larger and are readily legible by people of ordinary vision at distances up to 10 feet, and at angles up to ± 60 vertically and ± 70 horizontally. In addition, the solid-state indicators present no parallax problem since all numerals are produced in the same plane.

Twenty-seven electroluminescent diodes are positioned within a 5 x 7 matrix format and assembled with the IC on a dielectric which supports the electrical interconnections between diodes and the IC. This unit is then assembled in a metal case, and sealed with a glass cover.

The monolithic IC, containing more than 250 active elements, decodes the binary coded decimals and energizes the appropriate diodes to form a visible numeral. Starting with the four conventional BCD signals (8421), the IC logic first generates the complement of each, producing eight inputs to the decoder. These signals then determine a unique drive among ten alternatives, each corresponding to a decimal numeral.

Not all the 35 positions of the 5 x 7 matrix were used to form the numerals (although all 35 would be used to form alphanumeric). Twenty-seven positions will produce all the numerals, and since certain combinations always occur together, the number of necessary diode-driving signals is reduced to 18.

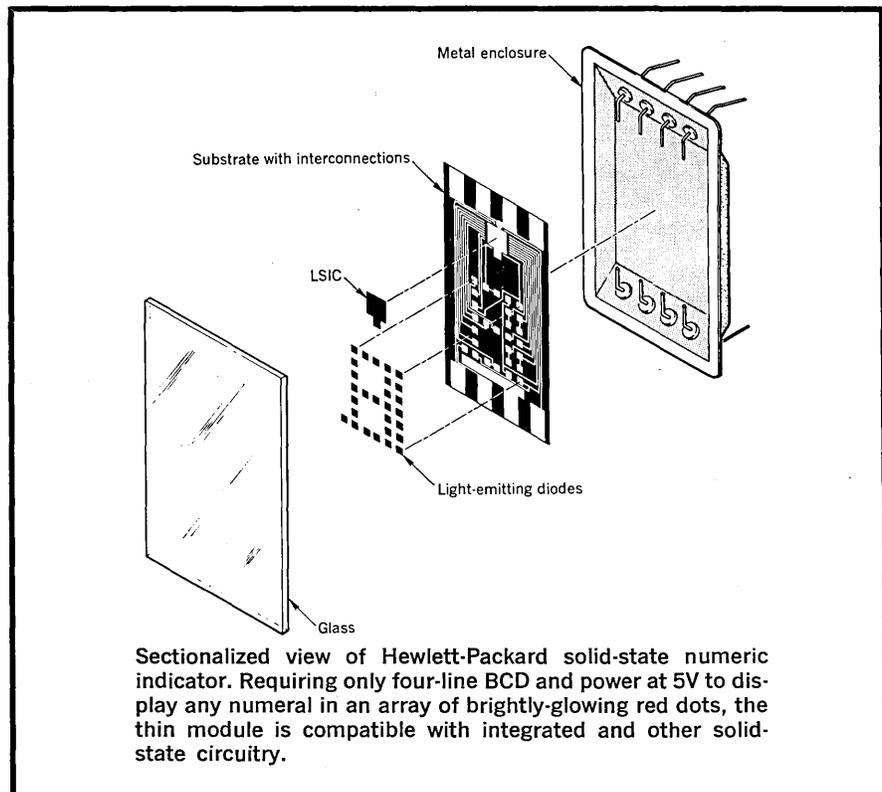
Thus the third IC logic conversion is from ten signals to eighteen. This selection of 18 unique diode combinations preserves immunity from misreading should a single diode or diode set go out; this was considered a necessity, in view of experience with undetected misreadings in classical segmented displays.

Although the theory of light emitting diodes has been understood for some years, the achievement of high luminous efficiency is recent. Attaining it was in part a matter of new technology in growing the materials, and in part determination of optimum trade-offs among the many variables available in devising electroluminescent p-n junctions.

Starting with pure single crystal gallium arsenide, Hewlett Packard grows its own epitaxial layer of gallium arsenide phosphide alloy in production reactors designed and built by the company. Gallium arsenide phosphide wafers up to two inches in diameter can be grown,

while holding the phosphorus-to-arsenic ratio to within 1% throughout the layer, and holding thickness to 1 micron tolerances.

A principal advantage of the low-voltage numeric indicators is their compatibility with integrated and conventional solid-state circuitry; drive and power-supply needs are the same. A further advantage is voltage-variable brightness which achieves optimum readability under widely varying ambient light conditions. Projected reliability is high. This is a result of assembling IC, light-emitting diodes, metallized interconnections, and substrate into a single sealed module. The light-emitting diodes themselves exhibit half-life characteristics; tests have shown that brightness (with constant current) declines to half its original value only after more than 20,000 hours. The compactness of the module makes it suitable for application in instrument panels, status boards, and information displays.



Sectionalized view of Hewlett-Packard solid-state numeric indicator. Requiring only four-line BCD and power at 5V to display any numeral in an array of brightly-glowing red dots, the thin module is compatible with integrated and other solid-state circuitry.

DATA COMMUNICATIONS

equipment for on-line,
real-time processing

sorry, no hieroglyphics, but...

It's the Model 37—a new heavy-duty line of completely data oriented terminals that have incredible communications capabilities

Teletype's new data terminal is one that will have to be seen to be appreciated. Will handle algebraic equations, chemical and engineering formulae, charts, graphs—from the most complex to "everyday" data—at speeds up to 15 characters per second.

FEATURES GALORE

The Model 37 will recognize and react to every code combination in the U.S.A. Standard Code for Information Interchange (ASCII). Print all code graphics, generate all control functions—type in upper and lower case, and even will be able to print in two colors if desired. The computer input/output capability of this machine is complete.

TRAVELING TABS

Model 37's transmission capability is unique. Now, for the first time, it will be possible for an operator to set tabs from the keyboard while the set is either on-line or off. Tabs will be able to be set on-line by a computer—or any remote terminal that uses the ASCII code. There is a tab stop for every *horizontal* and *vertical* space on the page. You can accommodate end-

less tabular variations in copy format. An extremely important feature for those who have a variety of forms to transmit and receive.

Built into Model 37 equipment will be everything needed for easier computer utilization and data transmission. Forward and reverse half-line feed combined with backspace, horizontal and vertical tabulation capabilities—will make the Model 37

the most flexible terminal Teletype has ever offered.

COMPLETE PACKAGE

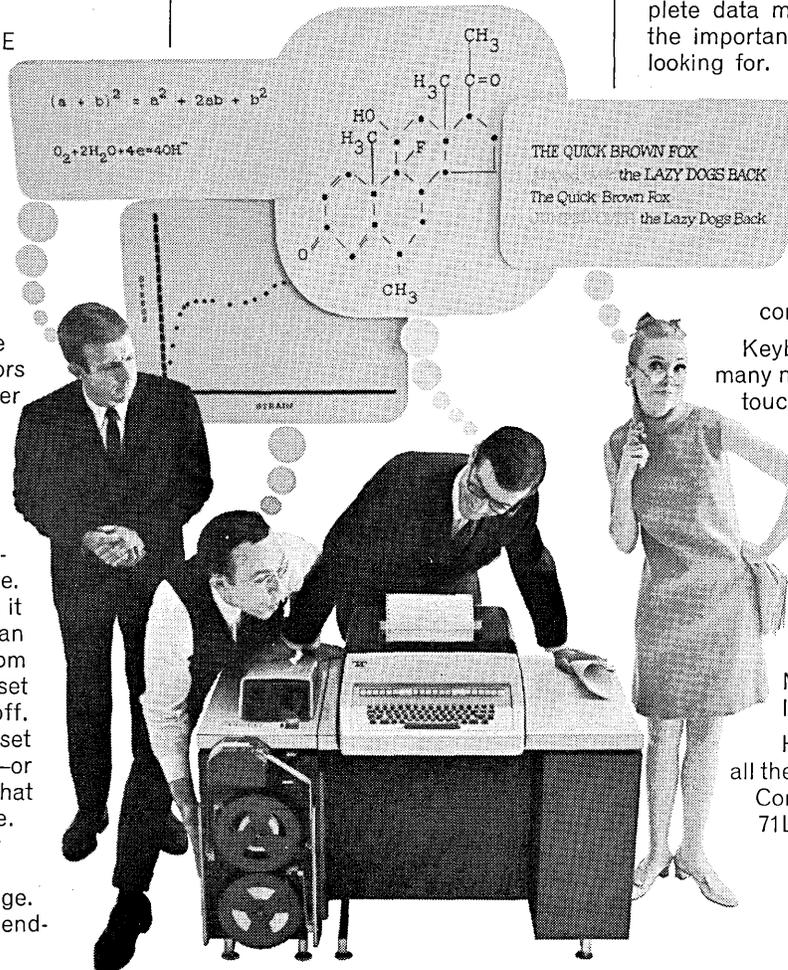
The Model 37 line consists of RO (receive only) and KSR (keyboard send-receive) sets, and the ASR (automatic send-receive) set shown here plus paper tape punches and tape readers housed in modular units compatible with all Model 37 equipment. You will have a complete data moving system with all the important options you've been looking for.

The KSR and ASR sets can be equipped with form feed-out controls that enable an operator to advance multi-copy forms into the printer by remote control. A real timesaver.

Keyboard sets incorporate many new features for easiest touch typing. An "aggregate motion" typebox prints more smoothly with fewer motions at 150 wpm, enabling the machine to operate at maximum speed six months at a stretch with normal servicing.

MORE INFORMATION

Heard enough to want all the facts? Write Teletype Corporation, Department 71L, 5555 Touhy Avenue, Skokie, Illinois 60076.

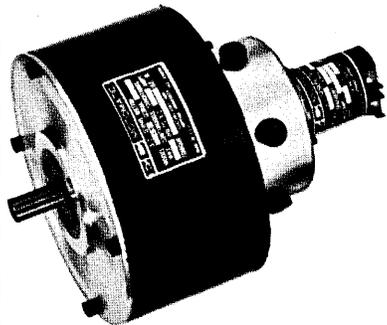


machines that make data move

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DEVELOPMENTS

New MOSFET Offers Potential For Digital Applications

A new type of MOSFET (metal-oxide-silicon field effect transistor) that may have several uses in integrated circuits for digital equipment has been recently developed by G. T. & E.

Devised by Messrs. Paul Richman and Walter Zloczower at General Telephone and Electronics Laboratories, Inc., Bayside, N.Y., the new device is called a P+ π P+ MOSFET. It exhibits all the electrical characteristics of a conventional P-channel MOSFET; however, it is fabricated on a P-type (or π) silicon substrate with high resistance to electrical current instead of the N-type substrate usually used with conventional P-channel devices.

By using this device, Messrs. Richman and Zloczower also devised a complementary MOSFET structure which is unique in that both the N-channel and P-channel devices utilize the same high-resistivity P-type substrate. This achievement greatly simplifies the

fabrication of complementary MOSFET integrated circuits.

"Although we are still testing and evaluating our laboratory models, we foresee several important applications," Mr. Richman said. "These include use in memories for computers and in switching circuits employed in various other types of digital equipment."

Two types of MOSFETS, P-channel and N-channel, are commonly used in integrated circuits today. When both types are incorporated into the same integrated circuit, the configuration is called a complementary MOS circuit. The complementary MOSFETS offer faster operating speeds and negligible power dissipation when in the "stand-by" state.

"Despite the important advantages of complementary MOS circuits, their use has been limited up to now because of difficulties encountered in their fabrication," Mr. Richman added. "The difficulties have arisen because both the N- and P-channel MOSFETS must be put into separate opposite-conductivity type regions within the same silicon base."

Display Panel Does Not Emit Light

A five-inch by five-inch magneto-optic display has been designed by General Electric's Electronics Laboratory in Syracuse, New York, for the U.S. Army Electronics Command, to be used for the display of digital-generated information.

The unique characteristic of this display panel is that it does not emit light. The display image is produced by focusing a light source on the panel at a fixed angle and diffracting this light within the panel itself. The intensity of the display depends directly upon the intensity of the light source.

The display panel consists of a thin magnetic film that exhibits magnetization normal to the plane of the film resulting in the formation of "stripe" domains. The film has a thin layer of Bitter's solution encapsulated on its surface which conglomerates at the domain boundaries to form a diffraction grating, and has a set of orthogonal matrix conductors placed behind it.

In response to generated currents at a selected intersection of the

matrix conductors, the grating re-orient itself 90 degrees from the original direction. By correctly addressing the matrix conductors, the elements are thus turned "on" and left "off" to form an image. The only way to alter information written on the display is to re-orient the grating by introducing a magnetic field of sufficient magnitude. Other features of the display are a long-term, non-volatile memory which is unaffected by power failures and the ability to write on the display electronically or with a magnetic pen.

In addition to this display, the Electronics Laboratory previously built a one-inch square development model of a magneto-optic display for the U.S. Army Electronics Command and a five-inch square, head-up M-O Display on GE funds. Development of magneto-optics displays at the Electronics Laboratory evolved from the Lab's work in magnetic thin films and electro-optical devices. Future emphasis will be given to producing larger display panels and developing techniques to control the inherent color of the panels.

DATA COMMUNICATIONS

equipment for on-line,
real-time processing

whatever happened to red tape?

Nobody can afford it, these data oriented days. Now they use paper tape—to communicate by *Telespeed* terminals.

"Red tape," stalled orders, delayed deliveries, late paychecks, incorrect billings, unanswered letters... These and other evidences of administrative thumb twiddling are fast disappearing from the business scene. Teletype's *Telespeed* equipment is the reason, in many cases.

Telespeed terminals are a complete line of high speed tape-to-tape equipment used by all kinds of modern companies—usually for delivering company data to the processing center the fastest, most practical way. *Telespeed* terminals can transmit a full day's data load over regular telephone lines in a matter of economical minutes.

Information travels from its source to the home office so fast that administrators don't even have time for a good twiddle.

"ROLLS" ITS OWN

Telespeed sending and receiving sets are not only fast, but ultra-economical. Because they "roll" their own tape, they can transmit data unattended, automatically.

Here's how they are used in branch sales offices, for example:

- (1) The day's sales orders, receipts, etc., are entered in paper tape by a girl making off-line use of a regular Teletype ASR (automatic send-receive) set.
- (2) At end of working day, the girl puts the tape in the *Telespeed* sending set and goes home.
- (3) During the late night hours, when line rates are lowest, the home office computer automatically calls the *Telespeed* sender, and gives it a coded signal to transmit.
- (4) The *Telespeed* sending set automatically transmits all recorded data to the computer (or *Telespeed* receiver) at headquarters.



The transmission takes only a few minutes, at most. Some *Telespeed* sets automatically check the transmission for errors, and make corrections, at the same time.

Telespeed equipment means fewer procedural errors, too! Automatic transmission and retransmission of paper tape is many times more accurate than the constant reintroduction of the human element into data preparation.

SPEEDS, MODELS, FEATURES

Telespeed sending and receiving sets operate at 75 characters a second (750 words a minute), 105 cps (1050 wpm), or 120 cps (1200 wpm). None of them require any special code for transmission. The equipment will operate on any 5, 6, 7, or 8-level code including, of course, the U.S.A. Standard Code for Information Interchange (ASCII).

Units are available in completely self-contained floor models, and the popular table top sending set of the "750" line. They will accommodate tape width sizes $\frac{1}{16}$, $\frac{7}{8}$, or 1 inch.

Sending sets consist of a paper tape reader and signal serializer. Receiving sets have a tape punch and signal deserializer. Sending sets have a sensing control to stop operation automatically at the end of the tape.

Optional features include:

Automatic Answer—enables unattended receiver to automatically answer a call from the sending set.

Line Break—when using certain data sets, operator can interrupt transmission to talk.

Discrete Calling—prevents sending set from being turned on by any but its own receiver (or computer).

At computer centers and outlying locations, *Telespeed* sending and receiving sets can be combined into a complete station. This is especially useful for economical computer input-output. Information is sent via *Telespeed* terminals to the processing center where it's fed into the computer. The processed data is then returned by *Telespeed* equipment.

HELPS THREE WAYS

There are three big reasons to investigate *Telespeed* equipment: Faster intelligence, lower costs, and fewer procedural and transmission errors.

With *Telespeed* terminals, you can expect smoother data flow, better customer relations. Reason enough for obtaining complete information on the three full model lines of *Telespeed* equipment, in speeds 750 wpm, 1050 wpm, and 1200 wpm.

Address all inquiries to Teletype Corporation, Dept. 71L, 5555 Touhy Avenue, Skokie, Illinois 60076.





DEVELOPMENTS

Graphic Display Subsystem Uses Digital Deflection Technique

A "second-generation" man-machine communication system, featuring what is reported to be the first announced commercial digital deflection technique in graphic displays, has been developed by the Univac Division of Sperry Rand Corporation, Philadelphia, Pa.

In contrast to the typical analog system displays currently in use, the digital deflective technique produces displays of superior characteristics in terms of speed, resolution and accuracy. This capability is advanced enough to allow design of integrated circuits and detailed drawings of complex mechanical parts.

By using a digital technique, the process of converting digital inputs into analog signals and then amplifying them to high current levels is eliminated. Instead, the Univac digital deflection system permits a digital representation to drive the deflection system directly eliminating the differential amplifiers and feedback loops and their attendant adjustments. The digital technique also provides more stability of image position. Although the theoretical speed of the electron beam is not quite as high as in an electrostatic deflection system, the practical speed is faster because of the precise positioning control that can be achieved.

The graphic display subsystem is designed for direct inter-connection with a large-scale computer system or for remote operation with connections to a central processor via voice grade or wideband communication facilities. It provides instant direct two-way communication through the use of the alphabet, numerals, diagrams, charts and engineering drawings.

The display unit is equipped with a keyboard containing standard alphanumeric and 40 function keys plus a light pen for operator input, and has the capability of plotting

randomly positioned points, vectors, and tabular mode alphanumeric data.

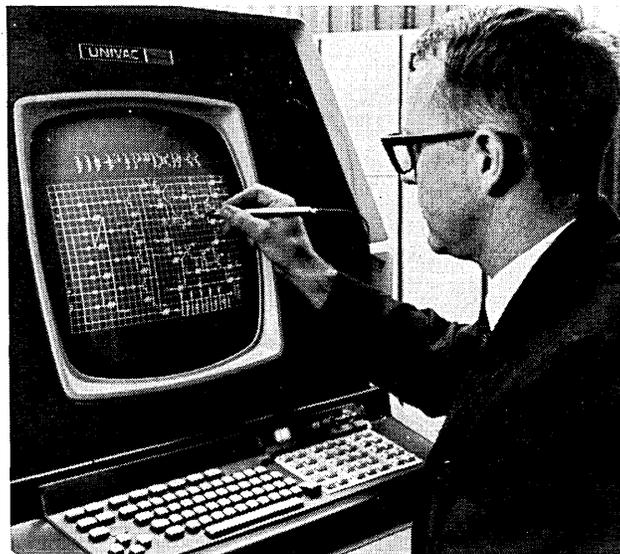
The cathode ray tube in the display unit has a usable viewing area measuring approximately 12 inches by 12 inches with data positioned in a 1024 by 1024 point matrix. Two programmable intensity levels and two programmable character sizes are provided. A 90 degree character rotation is also available under program control. Lines of full screen length may be specified as absolute (with respect to viewing area origin) or relative (with respect to the last position of the beam). Short relative lines may also be specified in a single display command word thus providing fast relative vector capability. A P31 phosphor is used with a beam spot size of 0.020 inches or less.

Character inputs are keyed in a 7-bit ASCII code. The input is decoded and entered into a diode matrix that generates a 3-bit description of the X coordinate, a 3-bit de-

scription of the Y coordinate, and a 2-bit description of the intensity level for each of the strokes used to form a character.

A display controller, which is a part of the subsystem, contains sufficient computing and control capabilities to provide an effective on-line response of the display system without placing an undue burden on the central processor. The controller has a 26 instruction repertoire and an 8,000 (expandable to 16,000) 18-bit, 600-nanosecond memory. Average instructions execution time is approximately 1.2 microseconds. Each controller can handle three consoles working on independent problems simultaneously.

As a result of these techniques, a number of special display devices have been produced. One such device is an ultraprecision display used for multi-layer printed circuit fabrication, which can draw lines and position the beam any place in a 15-inch square area to within plus or minus two-thousandths of an inch.



Using a light pen, an engineer designs an electronic circuit on the screen of a new UNIVAC graphic display subsystem which utilizes a digital deflection technique. From a number of component symbols shown in the upper part of the screen, the engineer can select those components he needs to construct the circuit on the grid provided by the system.

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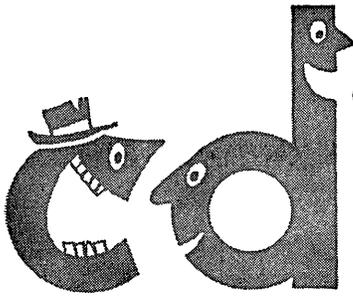
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commentary

Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of T. PAUL BOTHWELL, Contributing Editor.

Reliability Considerations in Designing Industrial Control Computer Systems

H. A. SPIVAK and L. E. HAWKINS, JR.

Industrial control computer systems perform data and control functions which are vital to the safe and efficient operation of industrial processes and plants. Therefore, system reliability is of vital importance, and reliability considerations must be an integral part of the initial circuit, thermal and mechanical design of any industrial control system.

The basic system reliability requirement is the prevention of sudden, gross misadjustment of a control loop. Since control action is applied frequently in a direct digital control (DDC) system to all loops, a hardware failure could conceivably cause such misadjustment in a matter of seconds.

How Reliability is Designed-In

The initial design stage, called the "concept review" is performed before the preliminary layout of the design. During this stage the various methods proposed by the development engineers will be evaluated, and design parameters will be traded off to achieve an optimum design. The reliability goal at this time is to achieve the proper functional operation with a minimum number of components, stressed well below maximum ratings. This technique provides the highest inherent reliability.

After these first considerations have been made, the

designer sketches out a preliminary drawing which details the proposed system. This is brought before a functional circuit review board for the purpose of discussing the design as it affects performance and reliability. With maturing of the initial design, a reasonably accurate estimate of part count by type evolves. By assigning average failure rates to each type and multiplying this rate by its respective quantities, an estimate of the system failure rate can be derived. This simple technique omits distinguishing details, such as operational stresses, thermal conditions, packaging orientation, etc.; therefore, the prediction is subject to inaccuracies. However, this method is used to point out the direction in which reliability design goals can best be achieved. It also is important for highlighting potential problem areas. By the conclusion of this second stage, the original logic diagram emerges complete and substantially verified.

After the detail design has been completed, a unit review is implemented and continued until the design is complete. During this period actual schematics and parts lists are generated. These documents are usually based on prototypes in which most specifications have been incorporated. During this period a thermal analysis is conducted by the packaging engineer. The reliability engineer at this time reviews parts lists to check for component selection and application, and verifies the authenticity of test specifications to be uniform with their intended use. He concludes this final design stage by performing a detailed system reliability estimate providing the design engineer with pertinent data relative to meeting specific reliability and to advise the future customer with average or mean time between anticipated down-times caused by random catastrophic type failures.

(continued on page 39)

The authors of this month's CD Commentary are Herbert A. Spivack, Manager, and Leland E. Hawkins, Jr., Reliability Engineer in the Product Assurance Department at Honeywell, Inc., Computer Control Division. Mr. Spivack has the responsibility of assuring the design adequacy of CCD with regard to reliability. Mr. Hawkins is responsible for reliability analysis of computer systems and electronic components.

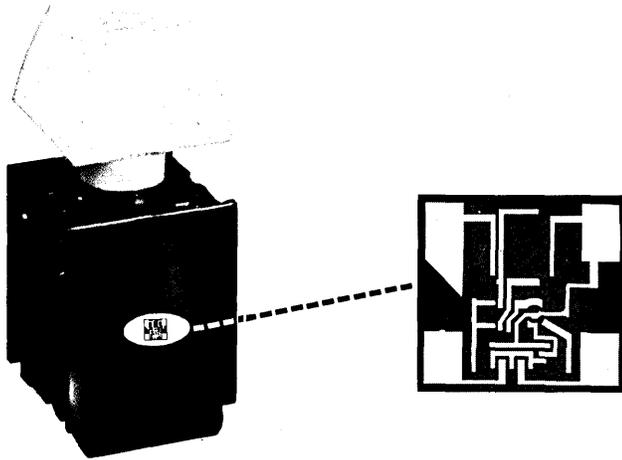
NOTICE TO READER:



**What's happening tomorrow
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What's inside the little black box shown above has advanced keyboards into the next generation, overnight. For more on this major breakthrough, and what it can mean to you, turn the page.

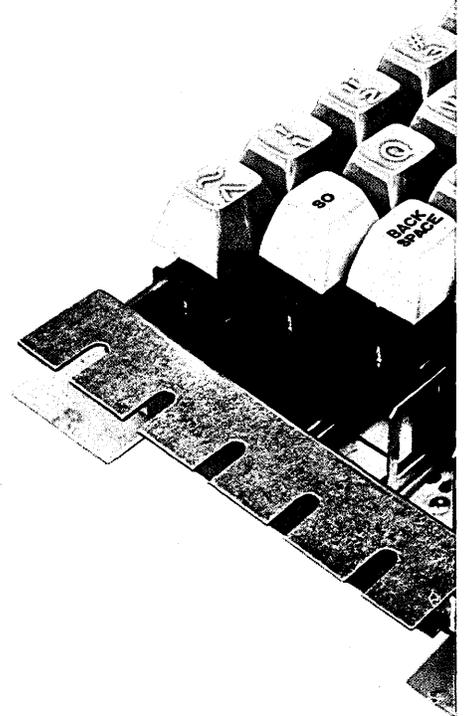
What's inside this little black box?

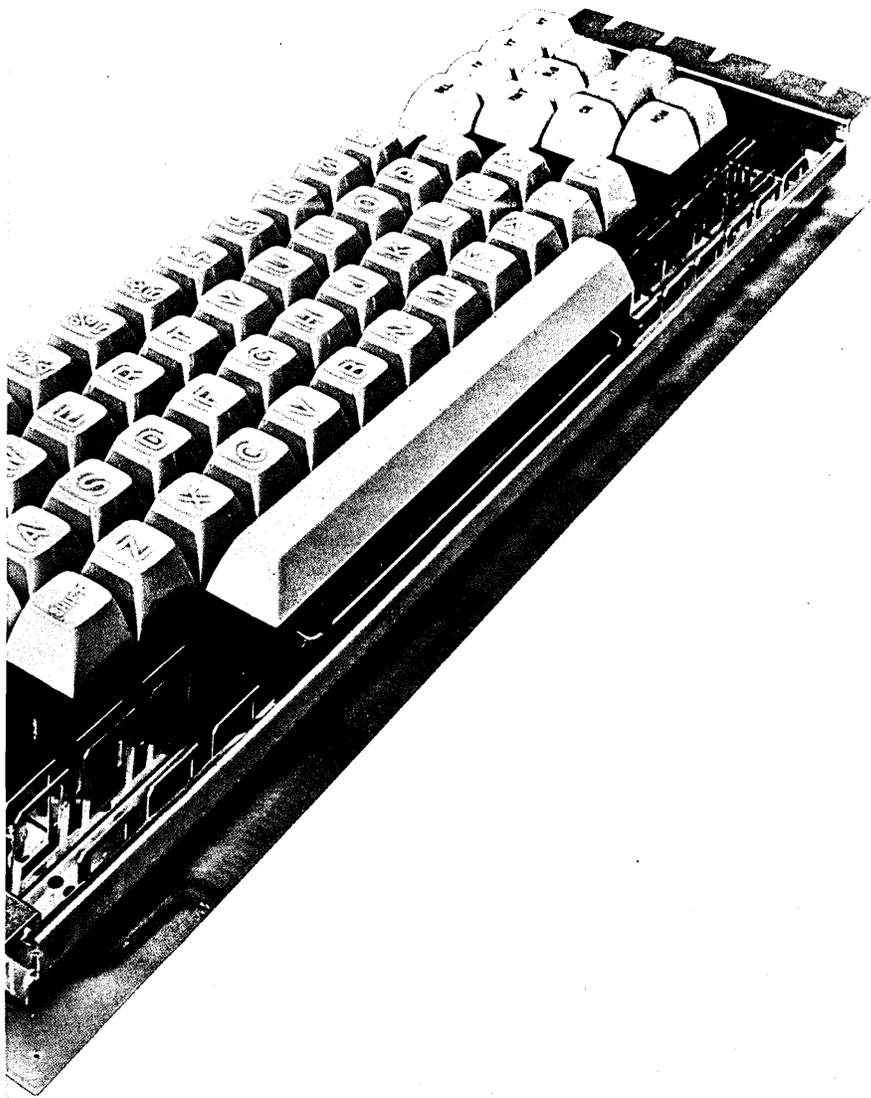


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All in a completely flexible package!

**For more facts on MICRO SWITCH SSK,
turn the page.**

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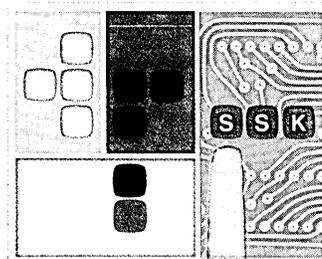
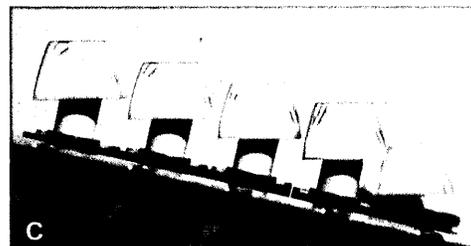
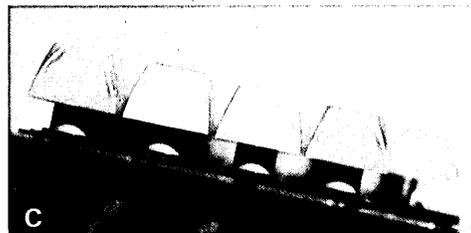
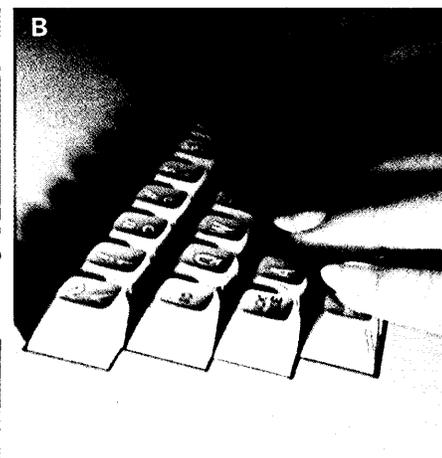
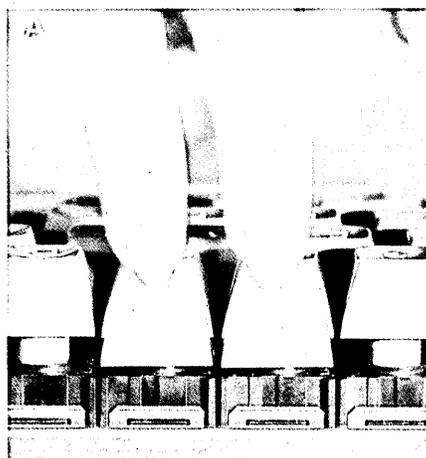
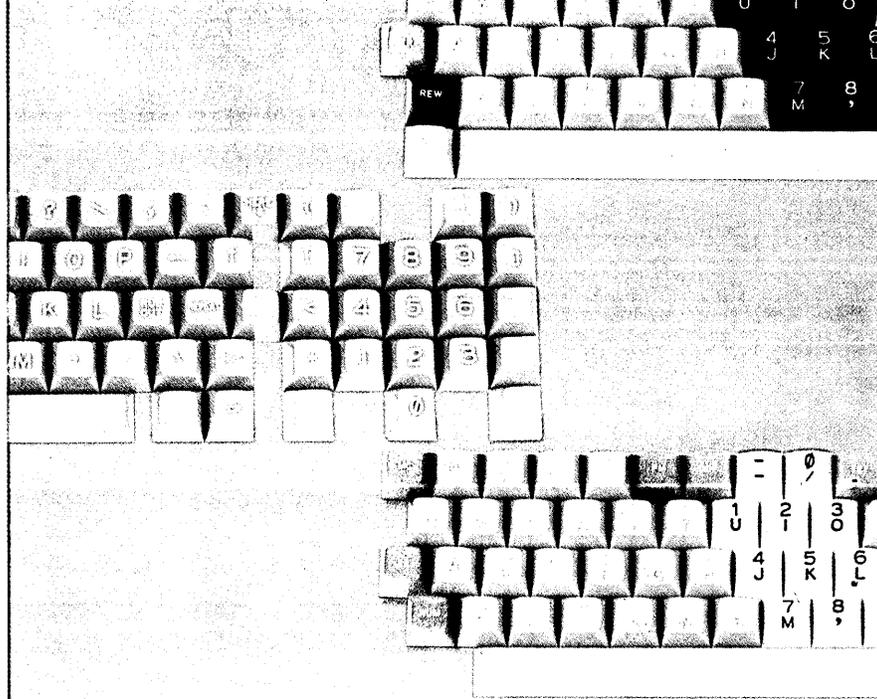
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Circuit failures resulting from either catastrophic component failures or drifting component values can be minimized. The former can be recognized by sudden changes in the operating characteristics of a part of a parameter, resulting in an inoperative condition (e.g., open or short). These failures occur randomly and exhibit a relatively constant failure rate. Causes for the failures are: shock, vibration, humidity; electrical, mechanical, and thermal stress. Today's design methods have reduced the major causes of failure to electrical and thermal stresses. By minimizing these stresses (derating), catastrophic failure incidents are lessened. One way to accomplish this is to design circuits such that nearly all components are stressed less than 50% of their maximum rated value. Electrolytic capacitors are an exception, since their failure rate does not significantly decrease with decreased stress level, and derating results in excessive physical size.

There are two general methods of circuit design used to withstand value variations: (1) worst case analysis and (2) design limit analysis.

In worst case design, component tolerances are selected such that there is only a slight probability that all environmental factors will produce shifts in the same direction as to exceed these maximum tolerances. The circuit is then designed by assuming that all components, independent of one another, have gone to these maximum limits in such combinations as to produce poorest operation. For example, a nominal $\pm 5\%$ resistor may be assumed to have a tolerance of $\pm 20\%$ to allow for resistance variation due to aging, etc. The circuit is then designed by using the worst case value of the component. Some components must drift to their maximum possible value and some to their minimum possible value for worst case operation. This guarantees that the circuit has an even higher probability of operating independently of component shifts since many of the factors which cause one component to increase in value would cause other components to also increase in value.

The disadvantage with worst-case design is conservatism, and may result in an unrealistic view of circuit characteristics or make certain types of circuits very difficult to design with available components. When allowing for extreme component variation and greater reliability, there will be an increase in power consumption and possibly an increase in the number of components. Both factors tend to reduce the overall reliability and may offset the advantages gained by allowing for worst case design.

In some cases, it is advantageous to use a design limit approach, where component tolerances are assumed which are not quite as pessimistic as those set for worst case design. However, the tolerances are broad enough to compensate for the very small percentage of components that would exceed them. The circuit is then designed using these values. The possibility of all components shifting outside these limits is highly improbable. As an example, if the probability that a resistor will deviate past the limit is less than 1 in 100, the probability that two resistors

will deviate past opposite limits simultaneously is less than 1 in 10,000. Considering the number of components in a circuit, it is evident that the failure probability is very small. Use of the design limit value allows more design flexibility and may save power and result in lower cost for given circuit performance.

One disadvantage of design limit analysis is that it may hide potential failure modes if the circuit is unusually dependent on one component. Thus, for a complete design analysis, all components are held at the design limit value, and an analysis is made of the circuit as each component is allowed to deviate to worst case one at a time. The circuit is then specified with all components at the design limit value except one which is at its worst case value. The component chosen for this is the one whose degradation has the most detrimental effect on circuit operation. In some cases, there is no component whose degradation is going to effect a significantly greater variation than all others on circuit performance. However, in most cases, the component to be set to the worst case value is readily apparent upon examination of the circuit. The design then consists of setting all components to design limit conditions except this one, which is at the worst case value.

Circuit design for reliability requires: (1) deratings to minimize part failure and (2) allowance for realistic component part parameter variation to minimize circuit out-of-tolerance failures.

Thermal Design

The removal of heat is of prime concern for product performance and reliability in electronic equipment. By creating an environment in which excessive temperatures are prevented, the components and materials can function without instability and/or failure rates beyond tolerance.

Thermal design, as a solution to the cooling problem, depends on the joint effort of the electronic and mechanical engineers. The task of the electronic engineer is (1) to develop efficient circuitry with a minimum dissipation of wattage, (2) to create circuit configurations which permit segregation of sensitive parts from heat-generating components, and (3) to select temperature-resistant circuit parts with application at conservative wattage stresses. The mechanical engineer's thermal design responsibility rests in the overall development of the packaging configurations and provisions for a cooling system which removes heat and maintains safe temperature gradients from the circuit parts to the ultimate atmospheric sink.

The following system parameters, as a minimum, must be accurately defined before an intelligent decision can be made as to how to best solve the problem:

1. Total heat generated by the system
2. Maximum allowable ambient
3. Ambient pressure
4. Allowable temperature rise throughout the system
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6. Maximum allowable internal "hot spot" and surface temperature which critical electronic devices can withstand over a sustained period without degradation of performance.

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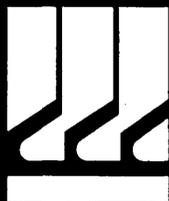
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In order to lead into a quantitative procedure involving a predominantly forced convection cooling design, these other considerations must be made:

- Total system resistance imposed on forced convection (air moving) devices
- Air filter designs and their effects on system thermal impedance as a function of time and the environment
- Location of the air filter with respect to the forced convection device, and its effect on performance
- Ducting requirements for various system functions, packaged in a restricted enclosure
- Minimum air velocities to assume an adequate heat transfer coefficient on the surface of critical electronic devices
- Velocity profiles for each forced convection device
- Location of the forced convection device(s) in the system, and axis orientation
- Environment — business, industrial, or hostile
- Line voltage/frequency variations and effect on forced convection device performance
- Electromagnetic compatibility of thermal design with system performance

Mechanical Design

The mechanical design of industrial control computer systems must be considered equally as important to operational reliability as any other design factor. Especially critical are the techniques used for interconnection wiring, voltage distribution, and ground bussing. The quantity of such interconnections can easily exceed the component count by an order of magnitude and it is imperative that only proven techniques be used. The failure rate for mass interconnection techniques such as solder and wire wrap must be approximately 2×10^{-4} failures per million hours in order that the final system meet the necessary level of reliability.

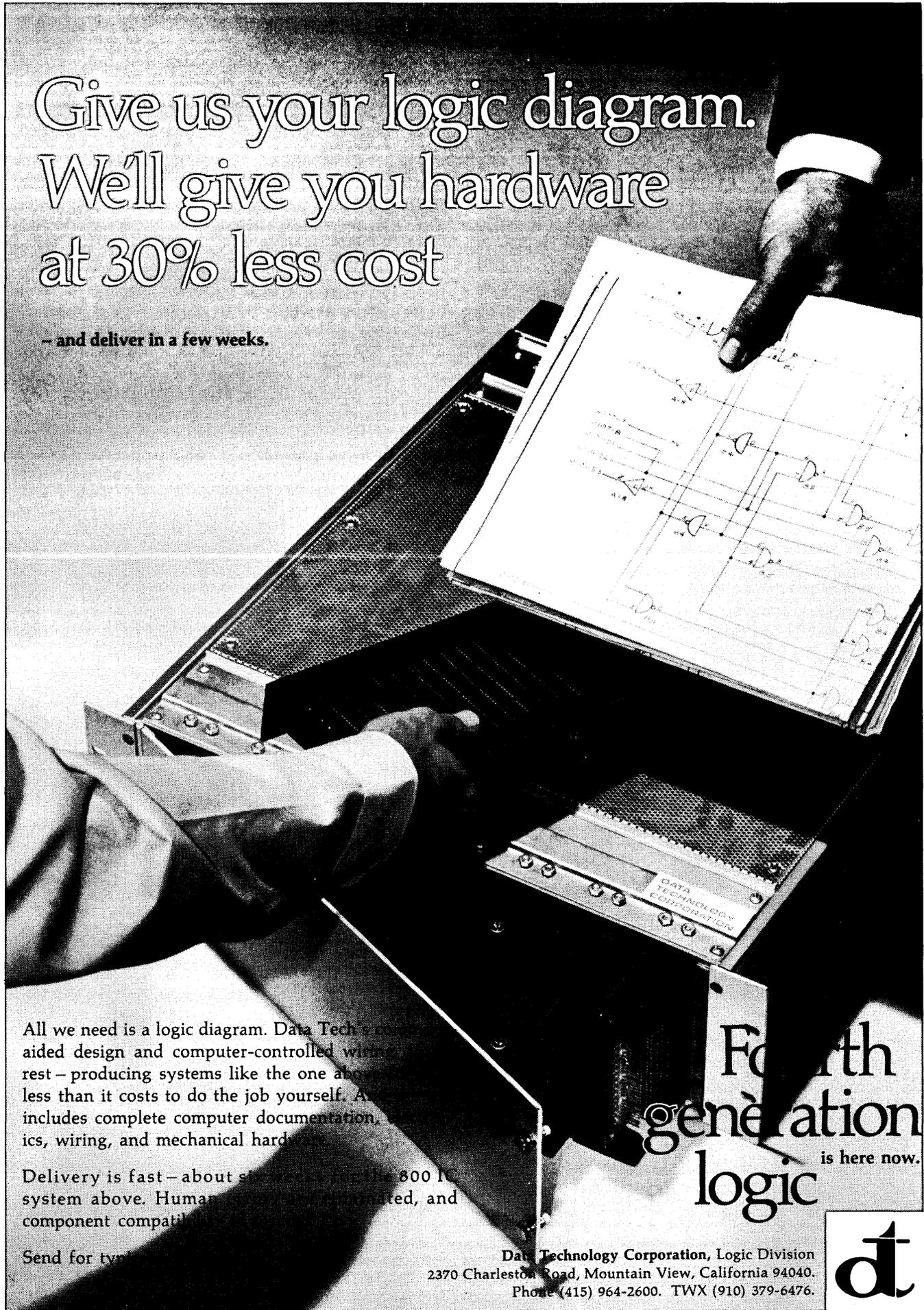
The following standards for mechanical design are necessary for industrial control computer systems. They emphasize the need for rapid maintenance on systems which may be required to operate continuously. Also, the ability to withstand the more severe operating conditions which can be encountered in an industrial environment.

1. The equipment design must be capable of operating reliably in environments where low-level vibrations in the 5-55 CPS range are present. These frequencies can be expected where rotating machinery is present and vibrations are transmitted through building structures. Connectors and switches must have contact pressure to adequately withstand these conditions over the long term. All hardware must utilize lock washers or other proven means to assure continuing tightness.

2. Modular construction utilizing interchangeable printed circuit boards is required.

3. Circuit board connectors and mechanical switches should utilize precious metal contact surfaces to assure long term reliable operation.

4. Metal parts not having natural corrosion protection capabilities must be coated with a suitable protective finish. Contact between the dissimilar materials should be avoided wherever possible and where



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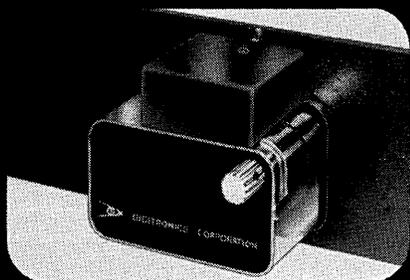
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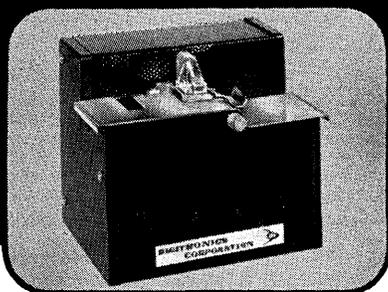
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contact is essential to the design the materials should be coated or otherwise protected against electrolytic corrosion.

5. Materials used in the construction must be resistant to deterioration by climatic and environmental conditions and be moisture- and fungus-resistant.

6. Air filters are required at all air inlets and should be designed for rapid removal for cleaning.

These factors summarize the major mechanical design factors which must be considered for satisfactory reliable operation of an industrial control computer.

Developmental Testing

Unfortunately, the most important factors in preventing failures are not easily specified. One such factor is the extent to which the operation of the system is understood in detail. In the case of hardware, this usually involves detailed bench tests of operation under a variety of conditions of inputs and output and environment. In the case of software or a hardware/software system, this requires extensive exercising. In both cases, it is important that no unexpected occurrences go unexplained. Where the hardware is electromechanical, containing subtle physical processes, as are active in a low-level multiplexer switch, it is important that the nature of the operation be thoroughly understood. As a higher configuration level, there seems to be no substitute for extensive operation by a variety of persons having differing backgrounds and trained in different disciplines. In the case of a DDC system, this implies exhaustive tests of a substantial system configuration with simulation of the process portion of the system.

While such tests will point out the most gross and most serious sources of failures, there is no sure way to subject the system to all conditions which will occur in actual operation. Even with extensive tests it is inevitable that certain portions of the design will contain deficiencies which will in some way degrade system performance. These deficiencies are usually detected and corrected on the first or second system during hardware and software checkout or during acceptance tests. The most important requirement is the existence of procedures for rapidly correcting these deficiencies when they are found.

Summary

The designer has certain tools for reliable design at his disposal:

- Simplify the design to a minimum of parts without degrading performance.
- Perform reliability design reviews by means of reliability analysis.
- Apply component derating techniques to the best possible advantage to reduce failure rates and to increase component life.
- Reduce the operating temperature of components in the equipment by providing heat sinks, appropriate packaging and adequate cooling.
- Eliminate resonant vibrations by proper isolation, and protect equipment against shock, humidity, corrosion, etc.
- Perform rigorous prototype tests and specify thorough production equipment test procedure.

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Techniques of Digital Recording

FRANK LOESCHNER

Cipher Data Products
San Diego, Calif.

Digital magnetic tape recording has grown in acceptance based on the greater use of digital techniques, lower-cost recorders, and a growing variety of recorders. This note will deal with three categories of recording techniques, with specific reference to the below-\$5000.00 price bracket. These are: incremental, continuous, and non-IBM-compatible recorders. An attempt is made to relate the various approaches on a cost basis.

IBM-compatible recorders must produce records on reels which can be accepted by all standard IBM-type computer tape transports. Compatibility requires a number of markings and gaps to be generated as well as vertical and horizontal parity. An important performance parameter is the consistency of character packing density. Byte-to-byte spacing for IBM-compatible tapes is dependent upon three parameters, as follows:

1. Skew (Static and Dynamic)

Static skew is produced by fixed mechanical misalignment of read and write head gaps with a line perpendicular to the direction of tape

travel. Dynamic skew is the result of non-uniformities in the mechanical properties of the tape and the variation of tape tension and stress produced by the tape transport mechanisms.

2. Tape Speed Variations or Incrementing Irregularities

Bit packing density for a continuous running tape machine is determined by the rate at which data is being clocked onto the tape and the speed of the tape. Irregularities in speed produce non-uniform packing density. For the incrementing transport, the tape must be advanced equal increments for uniform packing density. Instantaneous as well as long-term variations must be considered.

3. The Data Present

For the minimum byte-to-byte spacing to be observed, the data present must be of worst-case character. This requires one byte to consist of all zeros except for a one in the latest track followed by a byte with a one in the earliest track. This sequence must occur when the instantaneous speed and skew variations produce minimum spacing.

IBM indicates, for a tape to be readable, that there exist no more than 42 percent byte-to-byte jitter including variations because of tape speed, skew, and bit configurations. This figure is extrapolated from the IBM Systems Reference Library.

File No S-360-19, Form A22-6862-4, as follows:

The minimum time between bytes should not be less than the read character gate time plus 1 usec., which is 14.4 usec., for a tape speed of 37.5 ips and a packing density of 800 bpi. The nominal byte spacing is then:

$$\frac{1 \text{ inch}}{800 \text{ bits}} = 1.25 \times 10^{-3} \text{ inches}$$

The character gate time represents:

$$\frac{37.5 \text{ inches}}{\text{second}} \times 14.4 \times 10^{-6} \text{ seconds} = 5.4 \times 10^{-4} \text{ inches}$$

Bytes spread to this dimension are recovered. The percentage of the nominal spacing is therefore:

$$\frac{5.4 \times 10^{-4}}{1.25 \times 10^{-3}} \times 100\% = 42.2\%$$

A factor which affects the general cost of IBM-compatible recorders is reel size. As the size of the tape reels increases, the cost of the reel drives increases. Currently, a distinct reel drive cost increase occurs when reels reach 8½ inches in diameter. Six- and seven-inch diameter reels can utilize less powerful direct drive motors which sell for approximately \$30.00. The 10½" reels require drives which are at least two times more expensive. All the reel sizes provide complete computer compatibility and can be easily transferred to any standard transport. The smallest reels can store more than 1 million bytes of information, which is more than enough to satisfy most data-taking requirements.

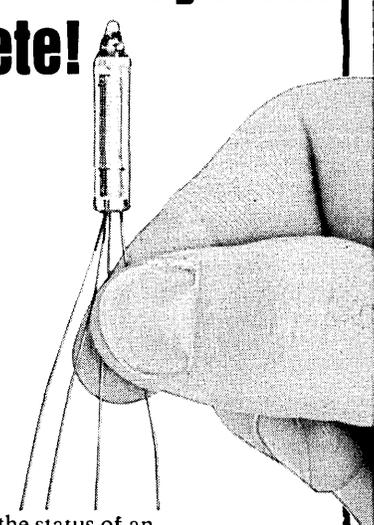
Recorders using reels 8½ inches in diameter and larger often require reel servos to maintain constant tape tension. Reel drives which supply constant torque to the reel produce a tape tension variation proportional to the radius of the tape remaining on the reel. Reel servos employ a sensor connected to the compliance arm which provides a position output. This output is then amplified and used to control the torque of the reel motor, thus providing constant tape tension. Constant tape tension is not mandatory if the machine is designed within the tolerance of the tension variations.

Incrementals

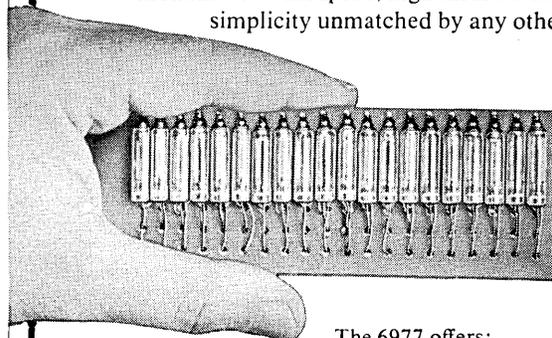
Incremental tape recorders accept asynchronous, or randomly generated, information as it is presented. In generating a 200 bpi IBM compatible tape, the tape is incremented (or stepped) 1/200 of an inch each time a character is recorded. Often data is to be recorded in the field and processed later by a large computer. Many real-time data acquisition applications result in asynchronous data rates which are below 1000 characters/second. In such applications, incremental recorders are particularly suitable.

Incremental tape recorders are also used in conjunction with a memory device or special purpose computer to provide an economical computer input/output tape transport. However, this application is

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diminishing with the advent of lower cost continuous, fast start/stop transports which also provide substantially higher transfer rates.

The heart of the incremental recorder is the capstan drive motor, often referred to as the stepper motor. This motor must increment the tape forward a precise distance each time data is presented. If the tape is not advanced precisely, variation in byte-to-byte spacing (jitter) will result. There are four commonly used stepper capstan drives: 200 steps/revolution stepper motor; 24 steps/revolution stepper motor; harmonic drive-stepper motor; and dc stepper servo (newest entry).

The 200 (or more) steps/revolution motor allows the tape to be driven directly by the proper diameter motor shaft (or capstan). This straight-forward approach provides a minimum of parts and complications and is the most reliable approach available. Motors

of this type, however, exhibit a characteristic ringing, or damped rotational oscillation about the detent position as the motor is stepped, producing byte-to-byte jitter. Further, mechanical resonance usually occurs in the 100 to 150 steps/second region, producing additional jitter at those specific data rates.

Jitter results when data is written before the motor has completely damped from its last step. Mechanical dampers must be used for stepping rates above the resonance rate. Properly designed, they can all but eliminate jitter up to 500 steps/second. Thus, the 200 steps/revolution motors seem ideal where cost and reliability are important.

The 24 steps/revolution motor requires a gear train or belt reducer to couple it to the capstan shaft to reduce each step to increments at the capstan which moves the tape a precise 1/200 or 1/556 of an inch.

Motors of this type are readily available. The reduction technique can be made relatively inexpensive in large quantities, and the approach has more versatility than any other in the low-cost bracket. The technique offers considerably higher asynchronous stepping rates at costs competitive with the smaller increment motors, but with greater complexity. Reliability over a period of time is an important question in this type of motor.

The harmonic drive motor, consisting of a fixed and a flexible spline, produces 400 to 1000 steps/revolution. It offers very high stepping rates while still providing direct drive advantages of simplicity. However, reliability and quality of this approach are still to be proved. Our company is continuing to test it.

The direct drive stepper using a dc motor-tachometer and an optical encoder is the latest innovation in the field. Here the capstan is driven by a dc motor-tachometer servo and is coupled to an optical encoder to provide rotational increment information. The entire capstan system must be low inertia for rapid start and stop characteristics. This stepper drive is necessarily the most expensive. A small amount of data storage may be used with this capstan drive to produce reliable high quality performance at high data rates.

The idea of an optical encoder is perhaps the greatest innovation in the field of incremental recording. An encoder may be applied to any of the earlier mentioned motors to provide exact position information. A stepper, without an encoder, writes the data on the tape while the motor is in a fixed position. When the character is written, the motor is incremented forward one step and waits for the next character. With the optical encoder, the character is held in a register while the motor is incremented forward one step. At a predetermined position in the step, the data is entered "on the fly". The motor goes on to complete the step

(continued on page 51)

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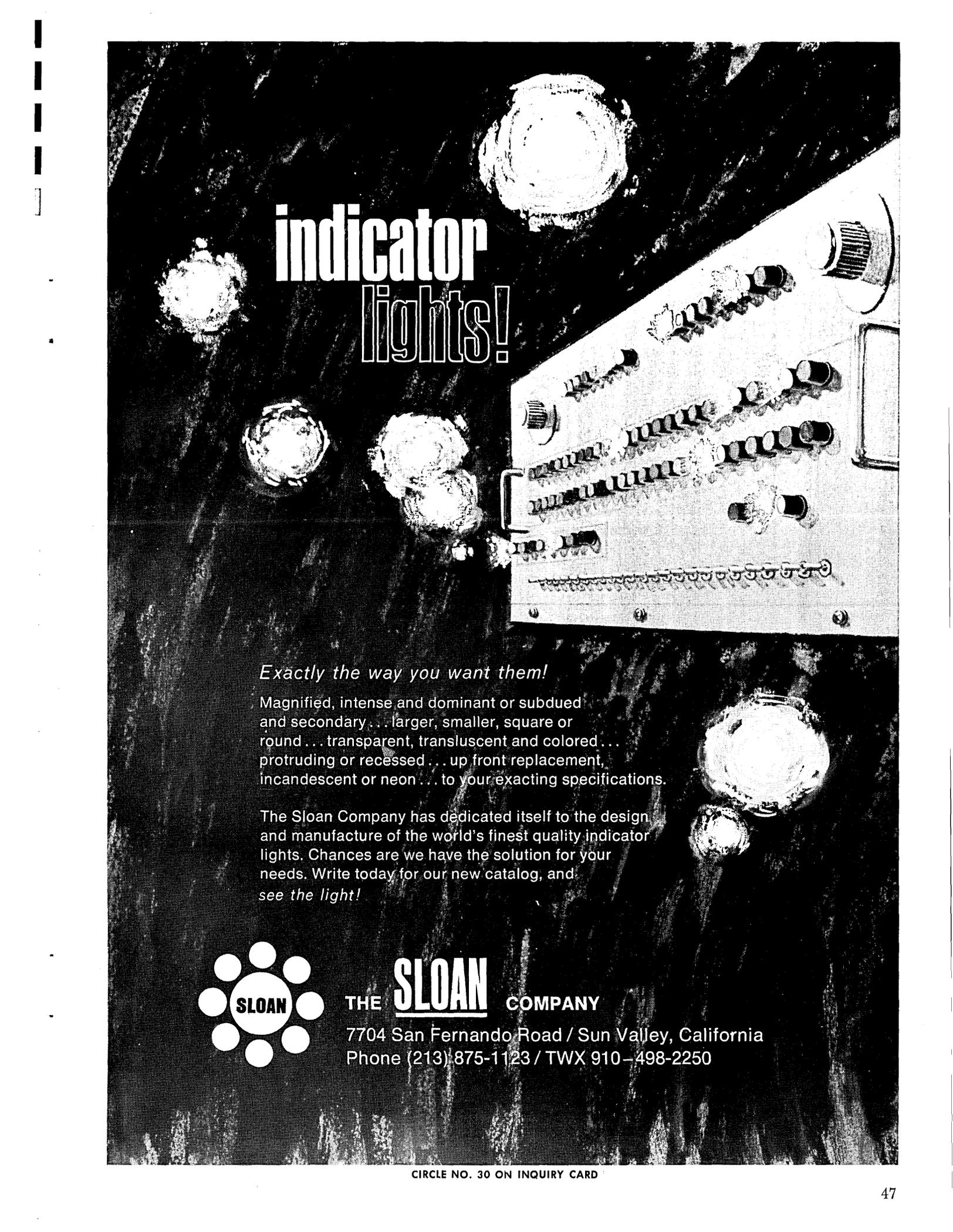
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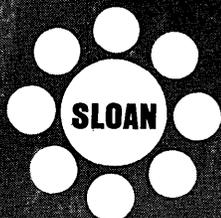


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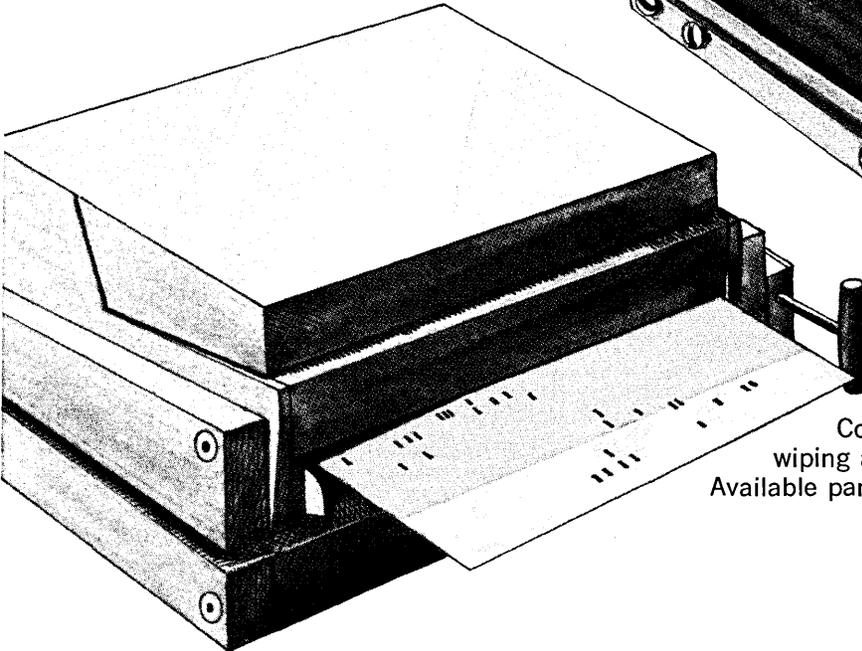
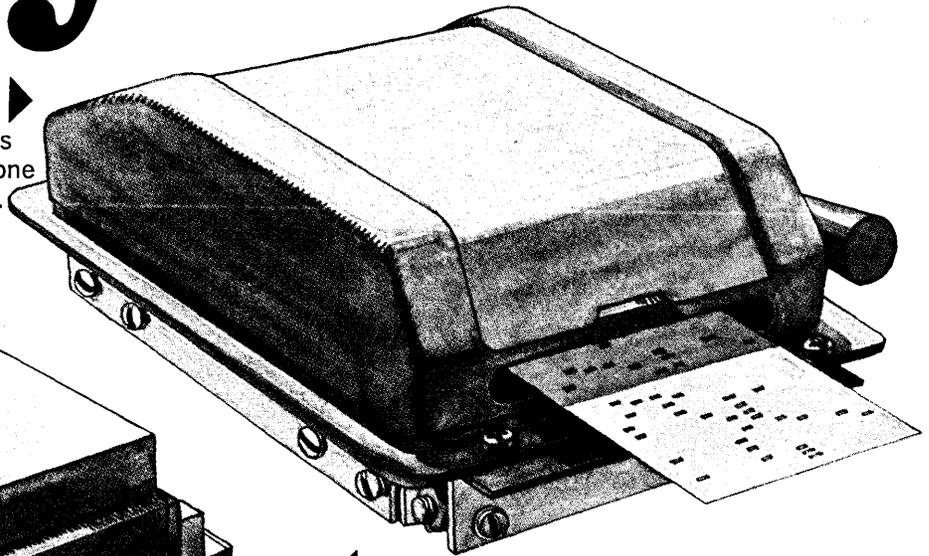


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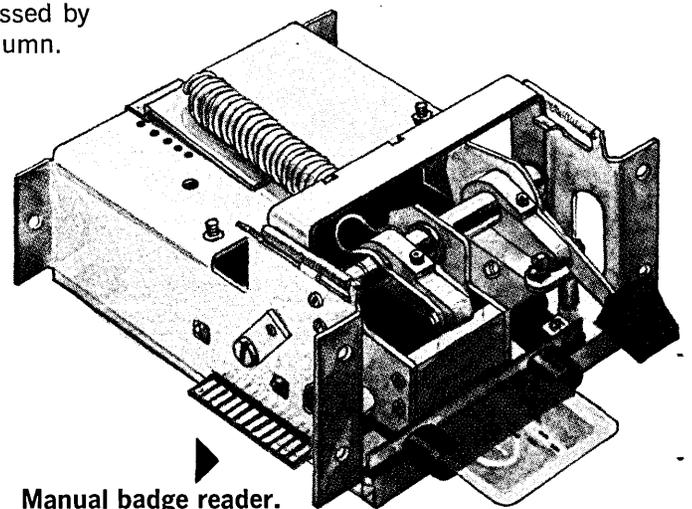
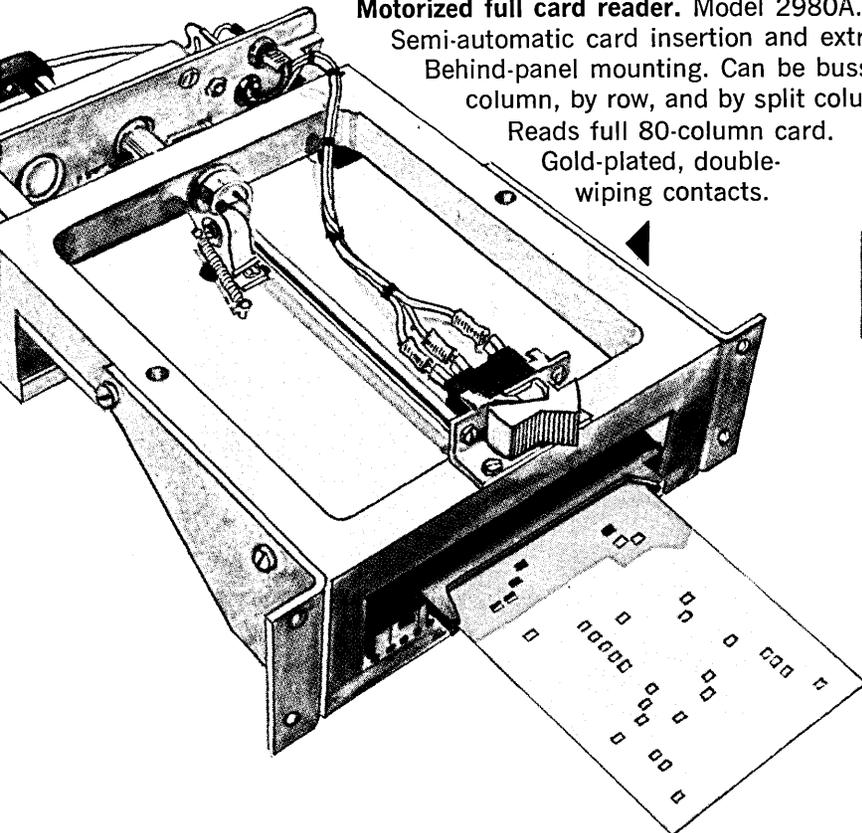
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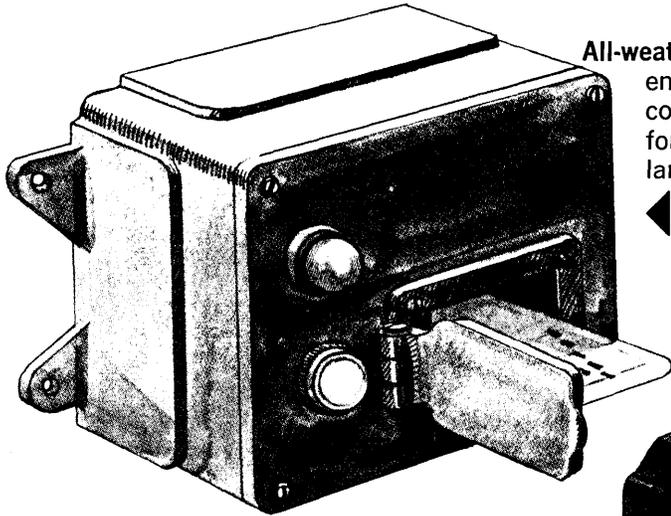
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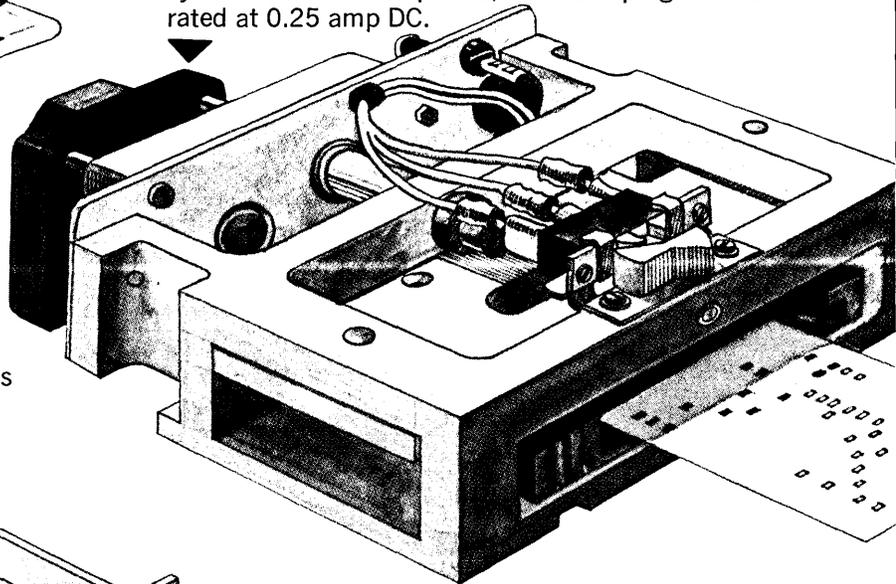
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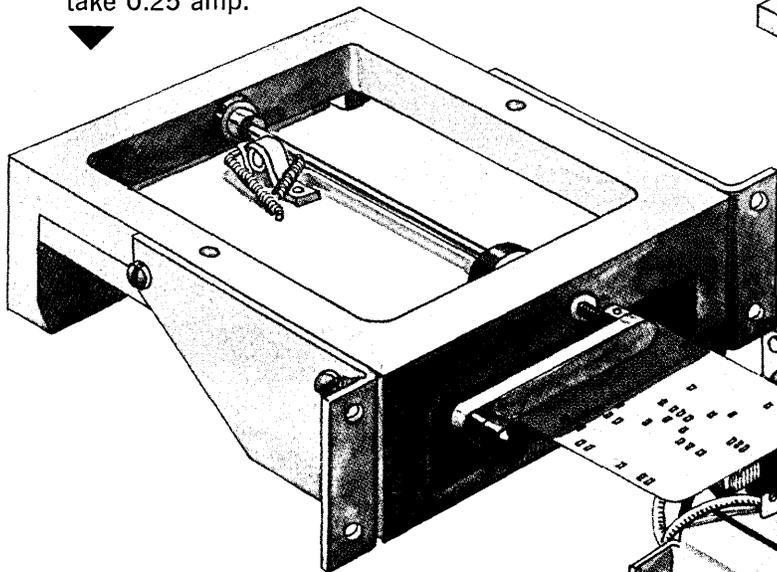


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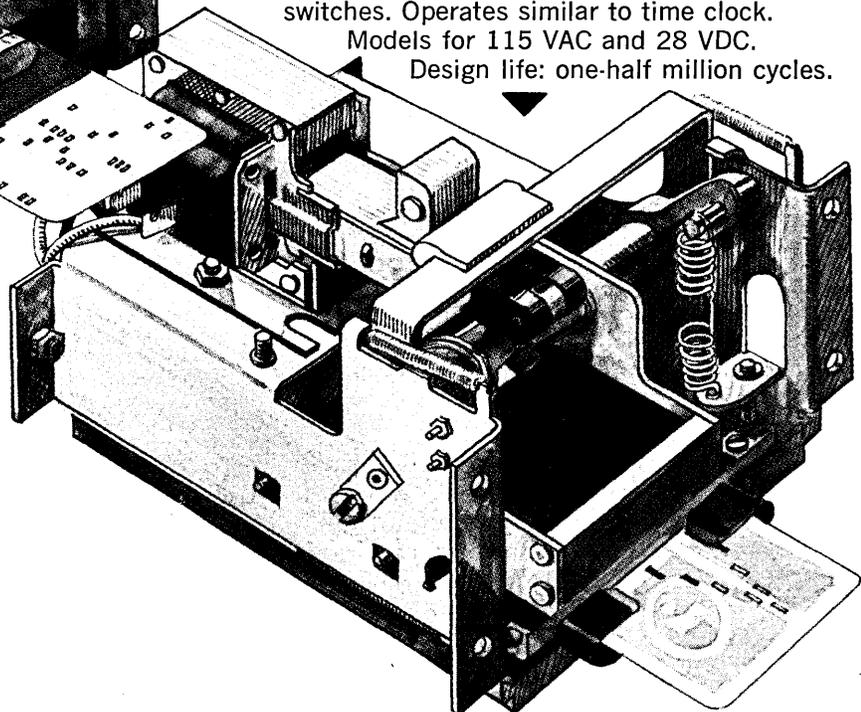
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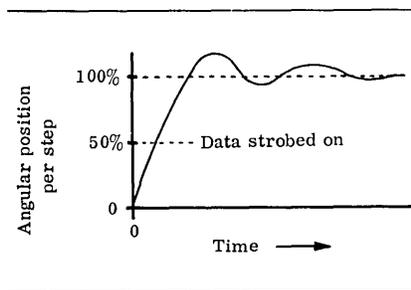
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(continued from page 46)

and waits for the next command. The graph below indicates this operation.



The data is strobed midway between steps, eliminating the variation in motor settling position as a factor in byte-to-byte jitter. However, in many applications as previously mentioned, it is satisfactory and less expensive to omit the use of the encoder at slower data rates and lower packing densities where the stepper has time to settle or where a mechanical damper is provided.

When applied to a dc motor, 200 steps revolution motor, or harmonic drive motor, the optical encoder must be 200 slots/revolution or higher. This type of encoder sells for \$100.00 and up. However, when applied to a 24 steps/revolution motor and reducer system, a \$30.00 encoder may be all that is required.

Continuous

With the advent of lower-cost computers and their current popularity boom, users are requesting low-priced peripheral tape transports. To meet this demand, new generations of continuous 25"/second and slower transports are evolving. One important advantage of continuous recorders is that a dual gap head may be used to read reliably the data on the tape immediately after it is written, thus providing a 100 percent check. A reliable read-after-write technique is not available for incremental recorders as yet. Some of the important features on continuous transports are the command rate, the start and stop char-

acteristics, and interface parameters.

The command rate is the number of stops and starts of the tape in a given period of time, usually per second. As the rate increases beyond one/second, reel servos are required even on smaller reels. As the required rate is further increased, the power supply requirements grow as the square of the command rate. This power increase results since, with limited intermediate tape storage, more power must be supplied to the reel servos to drive them rapidly to a null position before the next command is given. The theoretical limit on the command rate is the number of stops and starts per second that can occur with no data transfer. This rate for the 25"/second is approximately 50 per second. It is very important from a cost standpoint that the user define the minimum command rate, since he may be paying for capability and power supplies which he does not need.

The start and stop characteristics are important. Most computer requirements demand that the recorders start and stop within a record gap. To achieve this characteristic, low-inertia dc motors may be used with optical tachometer feedback. These assemblies cost between \$200.00 and \$500.00 and provide excellent performance. A lower-cost approach uses a stepping motor, taking advantage of the fact that its position can be determined by its incremental nature. This approach is usable only up to about 10"/second but provides simplicity and reliability.

A continuous machine for computer applications is often interfaced at the write register which is connected to the write head drivers and the read register driven from the read head amplifiers. The computer, or recorder interface module, may generate all the various checks, gaps, and tape marks required. These include vertical parity, longitudinal redundancy

check character (LRCC), cyclic redundancy check character (CRCC), record gap, file gap, and file mark block. However, many tape recorders offer these capabilities as options.

There are few reasons why the lower speed continuous tape transport cannot be priced comparably with incrementals. However, at the present time, they are 50 percent more expensive. By using smaller reels and speeds below 10"/second, read/write transports will be available for \$2500.00.

Non-IBM-Compatible

The greatest detriment to the acceptance of non-IBM-compatible recorders is the lack of an industry standard. The two most expensive items of an IBM-compatible recorder—the head and the capstan motor—can be reduced in cost by a factor of 10 if non-IBM-compatibility were accepted. The most logical approach to this type of recorder is to write a Manchester serial code, similar to PCM techniques, on a single serial channel continuously. Input registers store the asynchronous or synchronous data, then dump the data continuously onto tape. The serialized data recorded on tape can easily be checked by using read-after-write techniques, thus assuring proper recording. This type of recorder can provide all the data rate characteristics of incrementals while selling for one-fourth the price. If cassette cartridges were used and an industry standard were set up, users could replace punched paper tape as the low-cost, reliable communication medium. Data rates could be increased over paper tape. A variety of transports could evolve for applications such as data acquisition, computer I/O, telecommunication, and numerical control.

The non-IBM-compatible recorders are not a good recording choice unless standards are set up or unless many data-taking locations are involved with a central processing facility for tape conversion.

The design techniques discussed and analyzed in this article will enable the design engineer to more easily understand and use digital integrated circuits.

DIGITAL INTEGRATED CIRCUIT DESIGN TECHNIQUES

Hans R. Camenzind

Signetics Corporation
Sunnyvale, California

Unquestionably the widest use of integrated circuits has thus far been in the field of digital systems. There are compelling reasons for this fact. First, digital systems generally incorporate large numbers of a few basic circuits, enabling computer manufacturers, for example, to take advantage of the inherent low cost of integrated circuit batch processing. Secondly, and very significant historically, digital circuits are notoriously tolerant of component value variations.

Most circuits in digital systems have only two states — “off” and “on” (or conducting and nonconducting), and an input network or special configuration of active elements that determines under what conditions the circuit provides an output. The most widely used circuits are the AND and OR gates. The AND gate provides an output only when all of its inputs are energized, and the OR gate provides an output when at least one of its inputs is energized. A brief perusal of any logic text will assist the reader in understanding how such logic elements can be combined to perform the various functions required of digital circuits.

The inverting property of the common-emitter connection for transistors has resulted in the widespread application of NAND (negative and) and NOR (negative or) gates in digital applications. These circuits are logically equal to AND and OR gates, except that their outputs are inverted. For example, a NAND gate provides no output only when all its inputs are energized.

Many approaches to digital integrated circuits are possible and have been used in the past. Each has its

advantages and disadvantages. In this article we shall discuss and compare the more prominent representatives of integrated NAND and NOR gates and analyze some special circuits for switching applications.

DIRECT COUPLED TRANSISTOR LOGIC (DCTL)

Direct coupled transistor logic circuits (DCTL) are very simple and require few components. A DCTL NOR gate is shown in Fig. 1. Three transistors share a common load resistor. If base current is supplied to any of the three transistors, its collector will draw current through the load resistor and cause the voltage at point D to drop to the saturation voltage. Thus, a positive voltage applied to any of the inputs A, B, or C results in approximately ground potential at D. In this NOR gate the collectors of all transistors are connected together. For this reason the transistors in DCTL integrated circuits may be placed in a single isolation island, thus conserving chip area.

Fig. 2 shows a DCTL NAND gate. In this circuit three transistors are connected in series. Only when all three transistors are conducting will current be drawn through the load resistor R_L . Since the emitters of the transistors are not at a common potential, the base voltage required to effect conduction is different for each transistor. For input C a voltage correspond-

Editor's Note: This article is based on Chapter 5 of the author's new book, "Circuit Design for Integrated Electronics" published by Addison-Wesley Publishing Co., Inc. We thank the publishers for permission to use this material.

ing to V_{BE} (about 0.7 volt) is required. For input B this voltage is

$$V_B = V_{BE} + V_{CE(sat)},$$

and for input A it is

$$V_A = V_{BE} + 2V_{CE(sat)}.$$

The output voltage when all three inputs are energized is $3V_{CE(sat)}$.

For either configuration the number of transistors is chosen according to the number of inputs required, and V_{CC} is chosen high enough so that the off and on states are clearly distinguishable to subsequent circuits.

The principle used in coupling DCTL logic circuits is shown in Fig. 3. Transistor T_1 represents the output of a logic circuit, and transistor T_2 , the input of the following one. The two logic levels can easily be determined. With transistor T_1 turned on, its collector voltage drops to $V_{CE(sat)}$. In order to turn on transistor T_2 a voltage of V_{BE} is required at its base. Thus, at the coupling point, the voltage fluctuates between $V_{CE(sat)}$ and V_{BE} .

Let us assume that V_{BE} is 0.7 volt and the saturation voltage is 0.2 volt. This leaves a level difference (or noise margin) of 0.5 volt. If we substitute the series gate of Fig. 2 for T_1 , the lower logic level becomes $3 \times V_{CE(sat)}$ or 0.6 volt. In this configuration the noise margin is only 0.1 volt, which is rather small for reliable operation. As we can see, this type of logic depends on a low and predictable saturation voltage.

One of the more serious disadvantages of DCTL logic is an effect called "current hogging." This effect appears when the output of a logic circuit has to be "fanned out," i.e. connected to several inputs of other logic circuits, as shown in Fig. 4. The base currents for all three transistors, T_1 , T_2 , and T_3 , are supplied through R_L . Since the required input voltages of these three transistors are subject to device variations and geometry and their characteristic is nonlinear, the current is not distributed equally among the three transistors (Fig. 5). Therefore the situation might occur where most of the available output current flows into one input and the others are not receiving sufficient current to effect turn-on.

Noise susceptibility is another drawback in DCTL circuits. As we have seen, the logic level swing is determined by $V_{CE(sat)}$ and V_{BE} , a fairly small difference. In addition, the input impedance, being that of a forward-biased diode, is very high at low voltage and thus makes the stage susceptible to noise pickup.

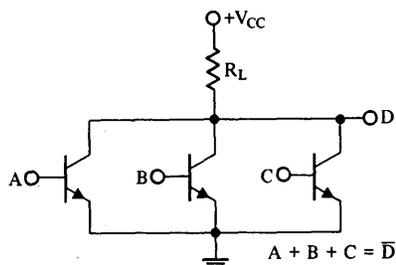


Fig. 1 Direct coupled parallel gate NOR circuit.

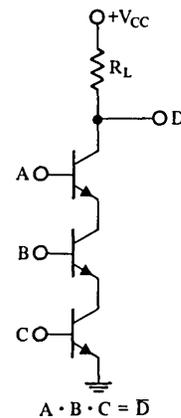


Fig. 2 Direct coupled series gate NAND circuit.

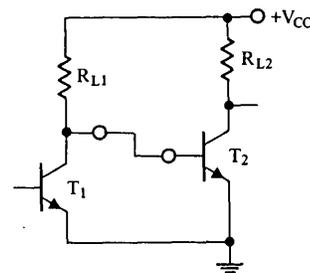


Fig. 3 DCTL stages in cascade.

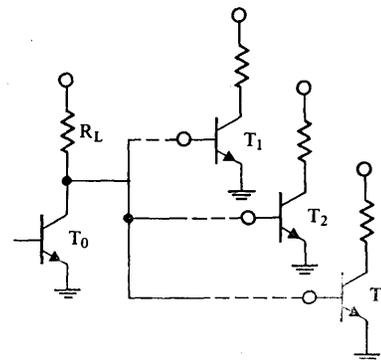


Fig. 4 Output of a logic circuit "fanned out" to three inputs.

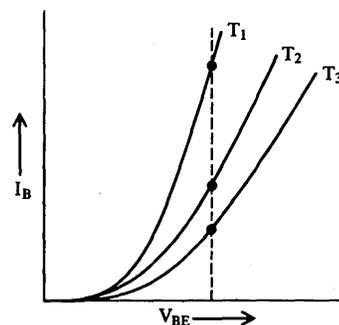


Fig. 5 Differences in the base-emitter characteristics of transistors in DCTL circuits cause an effect called "current hogging."

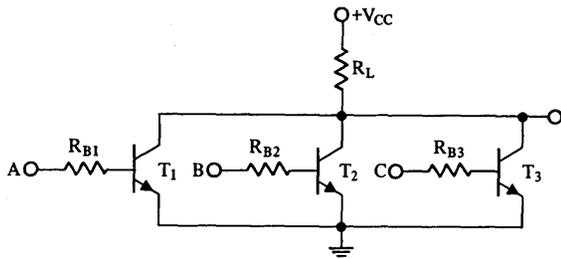


Fig. 6 RTL NOR gate.

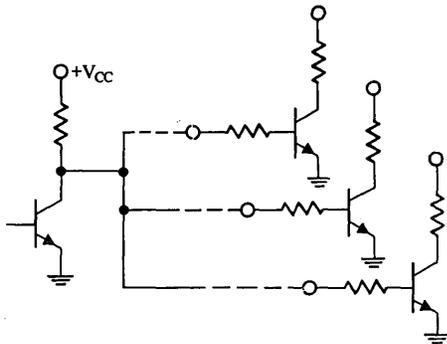


Fig. 7 Output of a logic circuit fanned out to 3 RTL inputs.

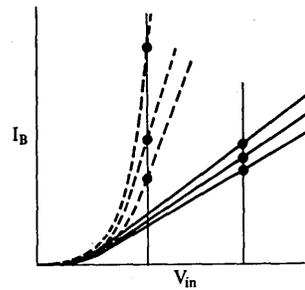


Fig. 8 The addition of a series resistance at the base causes the current from the previous circuit to distribute more evenly.

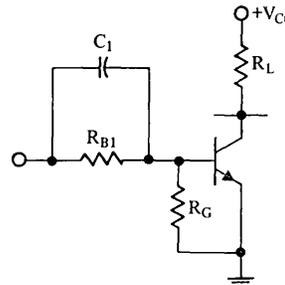


Fig. 9 RCTL stage.

The fact that all transistors are driven into saturation and no negative voltage is available at their bases during the turn-off interval causes the storage time and fall time to be long.

RESISTOR TRANSISTOR LOGIC (RTL AND RCTL)

Some of the shortcomings of DCTL circuits can be remedied with a simple modification. As we have seen, current hogging is a result of unbalanced input characteristics, aggravated by nonlinearity. These problems can be alleviated by connecting a resistor in series with each base, as shown in Figs. 6 and 7. Due to the voltage drop in the resistor, a higher input voltage is required compared to DCTL. But, as Fig. 8 illustrates, the additional resistance tends to equalize the input characteristics.

In the design of resistor-transistor logic (RTL) circuits a number of factors must be taken into account. The value of the load resistance R_L must be low enough so that sufficient current is available for all the inputs connected to it, but it must be high enough to avoid the requirement for high transistor current gain.

The value of the base resistance R_B should be large to avoid current hogging, but it must be small enough to allow a base current sufficient to drive the transistor into saturation.

High current gain is desirable since it allows wider

ranges for both load and base series resistances. On the other hand, excessive transistor gain is expensive and reduces the noise margin.

Compared to DCTL, the RTL circuit is somewhat slower. This is because the base series resistance and the forward-biased base-emitter diode form an RC network, causing additional turn-on and turn-off delay in the transistor.

In a typical RTL integrated circuit with junction isolation, two isolated islands are used, one for the three transistors and one for all four resistors. (In addition to the circuit, a transistor test pattern is diffused into the silicon block to facilitate evaluation.)

A modification of RTL logic is shown in Fig. 9. A capacitor is connected across R_B and an additional resistor leads from the base to the emitter terminal of each transistor. The capacitor with its low impedance at high frequency alleviates the problems of switching speed. The resistor R_G provides a low impedance between base and emitter, thus reducing turn-off time.

The major disadvantages of integrated RCTL logic circuits is the large area required for capacitors; it is for this reason that RCTL circuits are rarely integrated.

DIODE TRANSISTOR LOGIC (DTL AND VTL)

Many of the difficulties inherent in direct-coupled and resistor-coupled logic circuits are avoided by using

diodes as the logic element. A typical DTL circuit is shown in Fig. 10. If one of the three inputs, A, B, or C is at ground potential, diode D_4 is reverse biased. In this state no current flows into the base terminal of the transistor. Its collector voltage — the output D — is therefore at a potential $+V_{CC}$. Only if all three inputs are at a potential high enough so that a current can flow through R_1 and D_4 into the base terminal of the transistor will the output voltage drop to $V_{CE(sat)}$. Note that all logic operations are performed by the diodes. The diode network output is only amplified (and inverted) by the transistor.

Besides avoiding the problem of current hogging, DTL has the advantage of using elements which require only a small amount of chip area in integrated form. Moreover, since all diodes share a common anode they can therefore be placed in a single isolation island. This latter feature conserves area in circuits with a large number of inputs.

The diode D_4 has a rather unusual requirement. Since the transistor saturates when turned on, its turn-off time is considerable. It can be shortened by providing a negative base current during the turn-off interval. If diode D_4 can be made capable of storing a considerable amount of charge, it will conduct this negative base current out of the base of the transistor through one of the input diodes to ground.

The noise margin of this circuit is determined by the saturation voltage of the transistors connected to the input, and the forward voltage of the diode D_4 . A typical noise immunity for such a circuit is in the neighborhood of 400mV. (Note that the input diode

voltages and the V_{BE} of transistor T_1 cancel each other, to a large extent, and track each other with temperature.)

If increased noise immunity is desirable, one or more additional diodes are connected in series D_4 . One of the diodes can be converted into a transistor, as shown in Fig. 11. In this configuration the gain of this transistor is used to reduce the required input power. In order to limit the current in this additional transistor, a resistor must be connected in series with its collector. This can be done by providing a tap within R_1 .

Occasionally it is necessary to feed a large number of logic units from a single circuit or to connect to it a capacitive load such as a transmission line. In the circuits of Figs. 10 and 11 the output impedance is determined in one state by the saturation resistance of the last transistor and in the other state by the load resistor R_L . In the case of capacitive loads, the RC network formed by R_L and the capacitance of the load introduces an exponential rise of the voltage pulse at the output, thus introducing a time delay. While the saturation resistance can be made reasonably small, the value of the load resistance must be chosen as a compromise between output impedance and power-dissipation requirements.

The switching speed of a logic circuit driving a capacitive load can be improved by introducing additional transistors in the output stage, as shown in Fig. 12. In this circuit transistor T_3 is connected as an emitter follower between the load resistor and the load. Its gain is utilized to produce the necessary

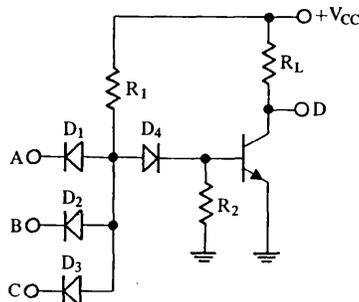


Fig. 10 Diode-transistor logic circuit.

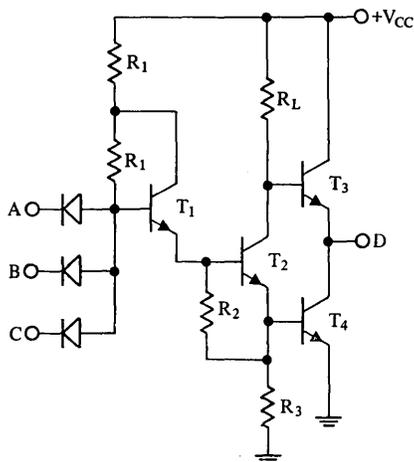


Fig. 11 DTL circuit with higher noise margin and current gain.

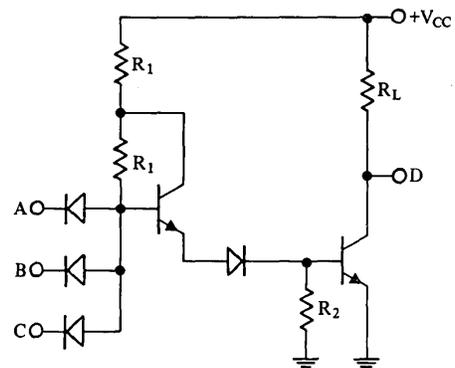


Fig. 12 DTL circuit with output stage.

high current during the switching transient. In addition, it is now possible to increase the value of R_L somewhat and thus reduce the power dissipation of the circuit.

In a configuration such as the one shown in Fig. 12 care must be taken that the two transistors connected in series across the power supply are never turned on simultaneously, since there is no series resistance to limit the current. It is generally difficult to avoid simultaneous conduction during the switching transient, so that small value resistors are sometimes added in series with the output transistors.

In the previous DTL circuits the required voltage at the input — and thus the noise margin — is determined by the number of diodes and transistors connected in series with the diode D_4 . This "threshold" voltage can be adjusted internally by providing an adjustable bias current source as shown in Fig. 13. In this variable threshold logic (VTL) circuit a constant voltage is produced at the base terminal of transistor T_2 by the voltage divider R_4 and R_5 . A constant current determined by R_3 then flows through transistor T_2 which is independent of the level of its collector voltage as long as T_2 is in the active region. With any one of the circuit inputs at ground potential, this current flows through diode D_4 and the base-emitter diode of T_3 is reverse-biased. With all inputs at a positive voltage, however, transistor T_1 is turned on and current flows through T_1 and R_2 . In order to turn on the output transistor T_3 , this latter current must exceed the bias current. Since a voltage drop exists across R_2 the threshold voltage at the input is a function of the amount of bias current used. By increasing V_{BB} in the negative direction, a large bias current results, thus increasing the threshold voltage.

Finally to obtain a large but nonvariable threshold voltage a breakdown or Zener diode can be used in place of diode D_4 . This arrangement (Fig. 14) utilizes the breakdown characteristics of the base-emitter junction to achieve a logic level swing of about 6 volts. This approach is occasionally referred to as diode-Zener-diode-transistor logic or DZTL.

In the circuit of Fig. 14 another method of achieving low output impedance is used. With transistor T_1 turned off, current is allowed to flow through R_L into the base transistor T_2 . A rather large current is therefore available to move the output voltage close to $+V_{CC}$. When transistor T_1 turns on, the load current flows through diode D_5 . In this state the base-emitter junction of transistor T_2 is reverse-biased, cutting it off. As in Fig. 11 the gain of a transistor is utilized to lower the output impedance without increasing current drain. Note, however, that diode D_5 is now connected in series with transistor T_1 and thus a higher voltage drop results.

TRANSISTOR-TRANSISTOR LOGIC CIRCUITS (TTL)

So far we have seen that resistors, capacitors, and diodes can be used as coupling elements in integrated logic circuits. Transistors can also be used as coupling elements to take advantage of certain of their properties.

In Fig. 15 one such circuit is shown. The base-

collector junctions of three transistors are connected between the base of the transistor T_2 and a resistor R_1 . With their emitters unconnected, these three transistors are used merely as diodes, so that current can flow through them into the base of transistor T_2 and turn this latter transistor on.

Let us assume now that the emitter of one of the input transistors, T_A , is connected to ground. Since a base current is available through R_1 , the transistor T_A is saturated forcing its collector voltage to near ground potential. Thus with any of the three inputs connected to ground, transistor T_2 is cut off and the voltage at the output D will move toward the positive supply voltage. In this circuit the collector terminals and base terminals of all input transistors are connected in parallel. In integrated form this feature offers a significant advantage, in that the corresponding collector and base regions of the input transistors need not be isolated from each other. In fact, all input transistors can be reduced to one transistor with many emitters. The identical circuit in integrated form is shown in Fig. 16. In this form only a very small surface area is required for each input.

Besides a saving of area, the TTL circuit has another advantage. As previously mentioned, the turn-off time of a saturated transistor (in our case T_2) is rather long, but can be made significantly shorter by providing a negative base current during the turn-off interval. In a TTL circuit the low collector-emitter impedance of the input transistor in saturation provides an excellent by-pass for the negative base current of T_2 , thus reducing turn-off time.

There are some disadvantages, however. With one or several emitters of the input transistors at ground potential, T_1 is turned on. If at the same time another emitter is held at a positive voltage, this emitter region will act as a collector, drawing current out of the transistor. This effect is due to the fact that even with collector and emitter interchanged (often called the inverted connection), most transistors show a small but significant current gain. Thus, in a TTL circuit the reverse current gain of the input transistor must be made as small as possible by proper choice of carrier concentrations, geometry, and carrier lifetime.

The other disadvantage concerns the noise margin. Transistor T_2 turns on as soon as one of the inputs drops below approximately 0.7 volt. Since the inputs are fed from the output transistor of a similar circuit with its associated saturation voltage, only a small voltage difference exists, resulting in high noise sensitivity. The noise margin can be improved by adding one or several diodes, or base-emitter junctions of transistors, between the collector of T_1 and the base of T_2 thus, increasing the required turn-on voltage. It must be kept in mind, however, that an introduction of a diode in this path cancels the advantage of fast turn-off in a TTL circuit.

A TTL gate which achieves greater noise immunity than that of Fig. 16 without sacrificing the speed advantage is given in Fig. 17. The noise margin is increased by connecting the base-emitter junctions of two transistors, T_2 and T_5 , in series. An emitter follower, T_3 , is used to lower the apparent output impedance and effect fast switching of capacitive loads.

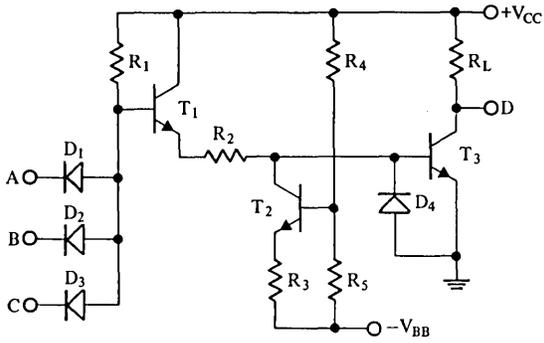


Fig. 13 Variable threshold logic circuit.

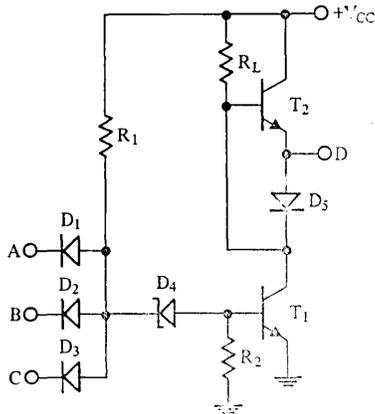


Fig. 14 Diode-Zener-diode-transistor logic circuit.

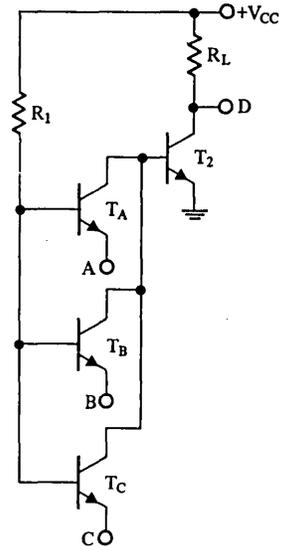


Fig. 15 Discrete form of TTL circuit.

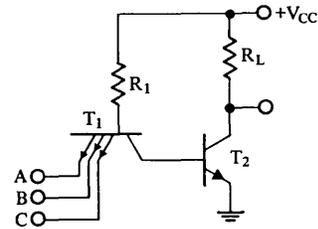


Fig. 16 Integrated form of TTL circuit.

CURRENT MODE LOGIC (CML)

All logic circuits discussed so far have one common disadvantage: the transistors in these circuits are allowed to saturate. As soon as a transistor becomes saturated, a significant amount of charge is stored in the collector and base regions, resulting in a time delay when the transistor is turned off.

In a current mode logic circuit, saturation of the transistors is prevented, to avoid delay due to storage. The major advantage of this group of digital circuits [also called nonsaturating logic, current-steering logic (CSL), or emitter coupled logic (ECL)] is therefore its short propagation delay. In Fig. 18 one of the more simple current mode logic circuits is shown. With all inputs at a low level, only transistor T_4 conducts. The current through T_4 is determined by the difference between V_{BB} and V_{EE} and the emitter resistor R_2 . More accurately the current is given by

$$I = \frac{V_{BB} - V_{BE} - V_{EE}}{R_2}$$

where V_{BE} is the voltage drop of the base emitter diode of T_4 . This configuration is the well-known constant current source. If now one of the inputs A, B, or C

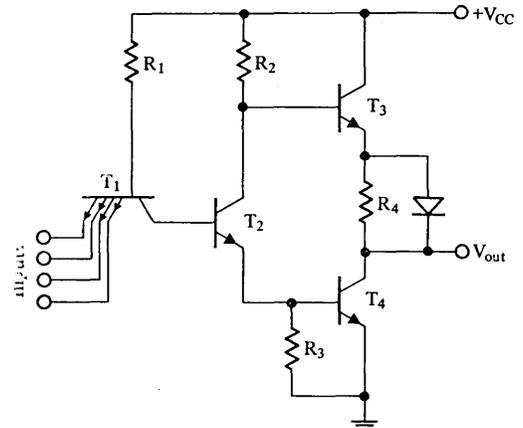


Fig. 17 High level TTL circuit with high current output stage.

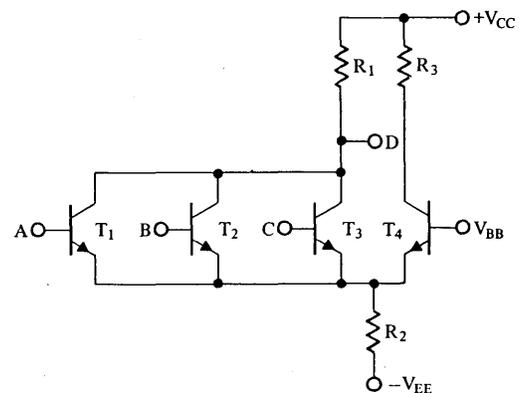


Fig. 18 Current mode logic circuit.

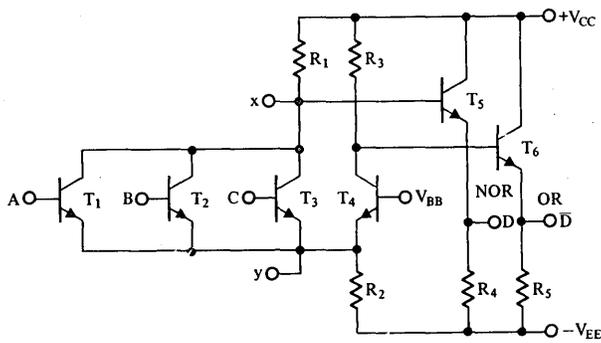


Fig. 19 Current mode logic circuit with level shifting.

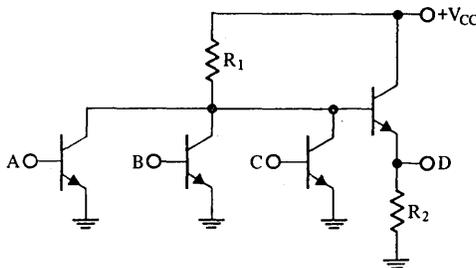


Fig. 20 Complementary transistor logic circuit.

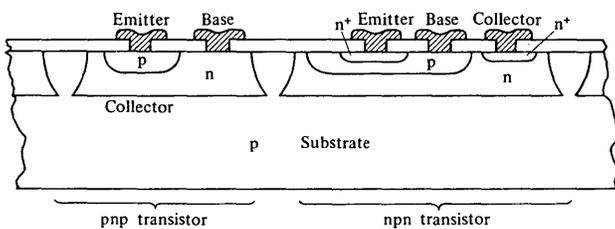


Fig. 21 Cross section of integrated complementary transistors. The collector of the pnp transistor is common with the substrate.

is moved to a voltage level above V_{BB} , the entire current will switch from T_4 to the corresponding input transistors T_1 , T_2 , or T_3 . Thus in this instant the voltage at the collector of T_4 moves toward $+V_{CC}$, while the voltage at the output D moves from $+V_{CC}$ to a level

$$V_D = V_{CC} - R_1 \frac{V_{in} - V_{BE} - V_{EE}}{R_2}$$

With a proper choice of R_1 , the voltage at the output D comes to rest at a potential above the saturation voltage of the conducting transistor.

There are three disadvantages to this circuit, however. First, at least two supply voltages are required. Second, in order to maintain a constant current with temperature and supply voltage variations, these supply voltages must be quite large, resulting in high power dissipation. Third, to keep the transistor out of saturation, the dc voltage level at the output must be higher than that of the inputs.

To make output and input compatible, emitter followers can be connected to one or both outputs,

as shown in Fig. 19. This reduces the output voltage by the V_{BE} of transistors T_5 and T_6 and improves the driving capacities of the outputs.

COMPLEMENTARY TRANSISTOR LOGIC (CTL)

The npn-pnp transistor combinations offer many advantages in digital circuit design. This combination not only increases design versatility and flexibility, but often is the key to high efficiency.

The fabrication of both types of transistors simultaneously in integrated circuits, however, involves either many parameter compromises or many additional processing steps. One method of obtaining pnp transistors, without additional processing steps, shown in Figs. 20 and 21, is by using the base region of the npn transistor as the emitter, its collector region as the base, and the substrate as collector. The resulting structure has low gain due to the great base-width and nonoptimized resistivities. Furthermore, its collector is the substrate and can not therefore be isolated.

In the circuit of Fig. 20, however, the collectors of all pnp transistors are at ground potential and therefore need not be isolated. This AND circuit has the advantage that none of the transistors saturate, which results in a fast switching speed.

In principle this logic gate is very similar to a DTL gate. The input diodes have been replaced by pnp transistors. Although the current gain of this type of transistor is low, it is sufficient to improve the performance of the circuit. Note that in converting the diodes into transistors, no increase in surface area is required.

FIELD EFFECT TRANSISTOR LOGIC CIRCUITS

One of the most significant advantages of field effect transistors is their high input impedance. This property can be used in the design of low-power integrated circuits.

A NOR gate employing four insulated-gate, p-channel, enhancement-mode field effect transistors is shown in Fig. 22. Note that in this circuit no other components are required. The transistors T_1 , T_2 , and T_3 are used as input gates in a manner similar to that in DCTL circuits. Ordinarily one would expect a load resistor between the drain terminals and the supply voltage $-V_{CC}$. To achieve low power dissipation, however, a large value resistor would be required which, in integrated form, would occupy a large area. In this circuit a field effect transistor is used in place of the load resistor. Its gate terminal is connected to the supply voltage, its drain current therefore being dependent on the source voltage — increasing as the source to drain voltage is made larger. This relationship together with the characteristics of the three input field effect transistor is shown in Fig. 23. The apparent resistance of T_4 is a function of the geometry used. For the insulated gate field effect transistor, the drain current is given by

$$I_D = \frac{\mu C_g}{X^2} (V_g - V_T) - \frac{V_D}{2} \quad V_D \text{ for } V_g \leq V_T.$$

To obtain a low drain current (and thus a high resistance), the channel width x of T_4 is made large.

An arrangement of field effect transistors resulting in a NAND gate is shown in Fig. 24. Only if all three inputs are at a negative potential will current be drawn through the fourth field effect transistor causing the output to drop to ground potential.

An integrated MOS logic circuit contains two separate NOR gates with three inputs each. Since no separate isolation is required and all elements occupy only small areas, field effect transistor logic circuits are generally much smaller than equivalent (bipolar) transistor logic circuits. The advantages of small size and low power dissipation, however, are counterbalanced by a significantly lower speed.

Although high speed and low power dissipation tend to be incompatible goals in any circuit, field effect transistors aggravate the problem because of a sizeable input capacitance and the required large voltage swing. In the circuits of Figs. 22 and 24, the gate capacitances of the input transistors of succeeding logic circuits are charged through the high resistance of T_4 . Thus, an RC time constant of appreciable magnitude exists, resulting in a large time delay.

If both n-channel and p-channel field effect transistors are available, a significant improvement in switching speed results. In such complementary circuits (Fig. 25) the load is always driven by the low "on" impedance of a transistor. With the proper choice of threshold voltage only one of the two field effect transistors is turned on at any given time. This results not only in faster switching speed, but also lower power dissipation. In fact, in a properly designed complementary switching circuit measurable power is dissipated only during the switching interval.

Comparison of field effect and (bipolar) transistor logic circuits.

Due to their high impedance and large input capacitance, field effect transistors are considerably slower than their bipolar transistor counterparts. Depending on the application, the speed-power product of bipolar transistor circuits is between 10 and 100 times greater. This difference is, however, bound to decrease as technology improves.

A useful figure of merit for a switching or amplifying stage is the ratio of transconductance to the total capacitance, g_m/c . While this ratio is approaching the theoretical limit for bipolar transistors, a sizeable improvement is still possible in field effect transistors. With continuing improvements in resolution of the photolithographic processes, it is feasible to increase the transconductance while at the same time decreasing the capacitance.

A significant advantage of the field effect transistor is its small size. Compared to bipolar integrated transistor, an insulated gate transistor is smaller by about a factor of five. In some applications field effect transistors are used as high resistances, or other unique properties of the field effect transistor are utilized; this difference is even more dramatic. As opposed to

the speed-power product, the contrast in size is likely to remain fairly constant even as technology improves. Another advantage of field effect transistor integrated circuits is in the processing. The requirement for diffused layers reduces the number of processing steps by approximately 30 percent and thus generally increases the process yield.

COMPATIBILITY OF INTEGRATED LOGIC CIRCUITS

As we have seen, each approach to integrated logic has some advantages and disadvantages. TTL circuits, for example, have short propagation delay but high power dissipation; DTL circuits, on the other hand, are slower in switching speed but at the same time offer reduced power consumption.

In large digital systems it is often advantageous to use a variety of logic circuits simultaneously. In such an application compatibility of the logic circuits is required, since each circuit must be capable of driving one or several other logic circuits.

Thus, compatibility must exist in the logic levels, power supply requirements, and (to a certain degree) speed. Because of incompatibilities in all three categories, field effect transistor logic circuits are generally totally incompatible with bipolar types. This latter group can be separated into three classes: current sinking logic, current sourcing logic, and current mode logic.

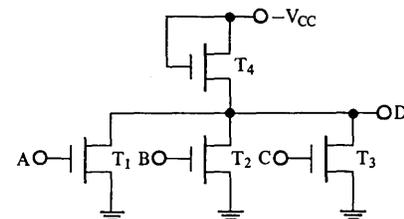


Fig. 22 Field effect transistor NOR gate.

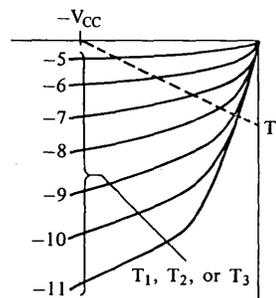


Fig. 23 Characteristics of the field effect transistors in Fig. 22.

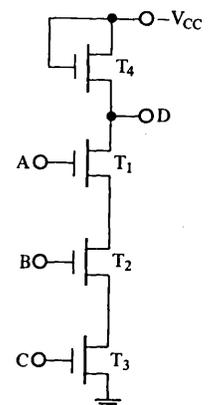


Fig. 24 Field effect transistor NAND gate.

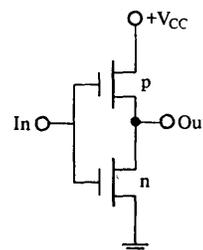


Fig. 25 Switching stage employing complementary field effect transistors.

Current Sinking Logic.

In this class of logic circuits the current is drawn out of the input into the output of the previous logic stage. This driving output therefore acts as a current sink. Examples of current sinking logic are DTL, TTL, and CTL.

Current Sourcing Logic.

In this class of circuits current is fed from the output of the previous stage into the input of the logic circuit. Both DCTL and RTL are representatives of current sourcing logic.

Due to opposite flow of current, current sourcing and current sinking logic circuits are incompatible. Within one class, circuits are compatible only if their logic levels are similar. Some circuits are partially compatible in that one family of circuits is capable of driving another, but not vice versa. An example of partial compatibility are DTL and DZTL circuits.

Current Mode Logic.

Although from the direction of current flow one might classify this group as current sourcing logic, its logic levels, switching speed and power supply requirements are sufficiently different to make it incompatible with either of the two previous classes.

INTEGRATED BISTABLE CIRCUITS

The circuit diagram of a very simple integrated flip-flop or bistable circuit is shown in Fig. 26. The base and collector regions of the two transistors T_1 and T_2 are cross-coupled. If we assume that T_2 is turned on,

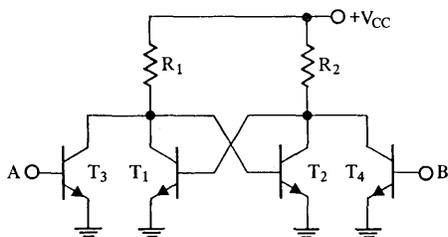


Fig. 26 Direct coupled flip-flop.

then T_2 must be off since its base current is shorted to ground by T_1 . But with T_2 turned off, base current is supplied to T_1 . Therefore, one of the two transistors is always on and one is always off.

The ON state can be switched from one transistor to the other by applying a voltage to one of the two points A or B. If we suppose that the transistor T_2 is in the OFF state, a positive voltage applied to point B causes transistor T_4 to draw current through R_2 . The voltage at the collectors of T_2 and T_4 therefore drops to $V_{CE(sat)}$, and transistor T_1 is deprived of its base current and turns off. Thus the flip-flop has changed states and the voltage at point B can be removed.

This circuit is a derivation of the direct-coupled logic gate. It is readily integrable and has the advantage that only three isolated islands are necessary. On the other hand, the voltage swing at each collector extends only from $V_{CE(sat)}$ to V_{BE} , a rather small margin for most systems. This voltage swing can be improved by adding resistors in series to the base terminals, as is shown in Fig. 27. In this approach, which is an extension of the resistor-transistor logic gate, the upper voltage level at the collectors is determined by the ratio of the collector and base resistors. Although this greatly increases the voltage swing, the loop gain is decreased by a large amount and the switching speed suffers. In conventional discrete component circuits an improvement can be made by shunting the base resistors with capacitors, thus increasing the loop gain during the switching interval. In an integrated circuit these capacitors occupy a very large area, so that it is advantageous to find a solution which requires no capacitors.

In Fig. 28 such a solution is shown. Two additional transistors, T_5 and T_6 , are connected into the loop,

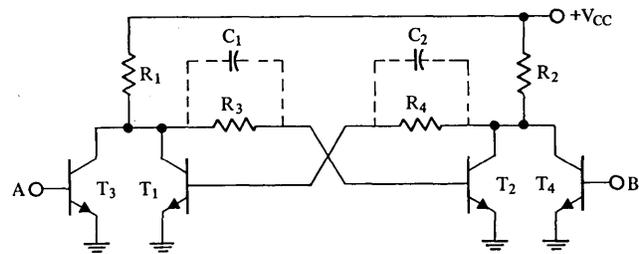


Fig. 27 Resistor coupled flip-flop.

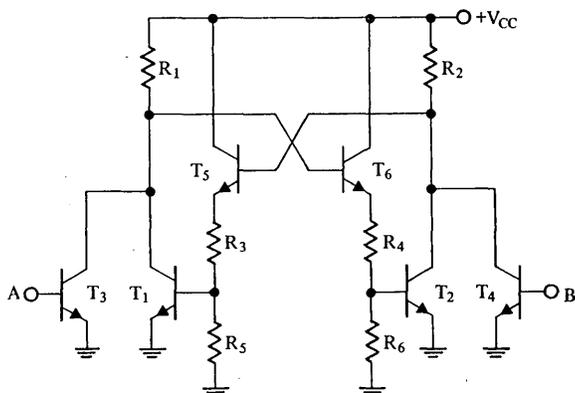


Fig. 28 Resistor coupled flip-flop with increased loop gain.

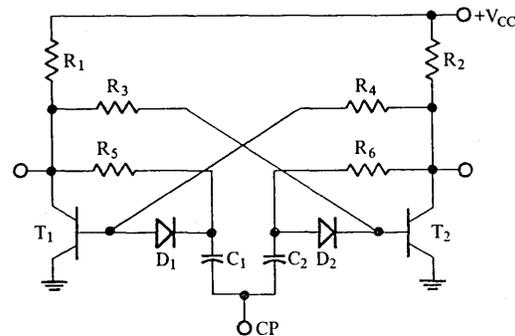


Fig. 29 Conventional center point triggered flip-flop.

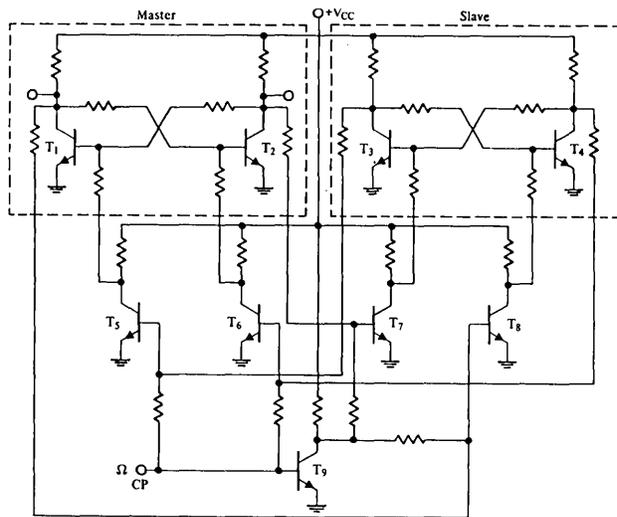


Fig. 30 Center point triggered master-slave flip-flop.

thus increasing the gain. Note that these two transistors are unable to saturate and therefore have no storage time delay.

In many computer applications flip-flop circuits which change states each time a pulse appears at a single input are required. These are often called center-point triggered flip-flops. A discrete-component circuit of this kind is shown in Fig. 29. The transistors T_1 and T_2 and the resistors R_1, R_2, R_3, R_4 form a conventional flip-flop. Let us assume that transistor T_1 is on and T_2 is off. When a negative pulse appears at the center point, the base of transistor T_2 will be unaffected, since the diode D_2 is reverse-biased through R_6 and is thus unable to conduct. At the other side, however, current is drawn out of the base of T_1 , through the diode D_1 . Therefore, T_1 turns off and, by the normal flip-flop action, T_2 is turned on.

For proper operation the trigger pulse must have disappeared by the time the flip-flop changes states. For this reason both the pulse length and the values of the two trigger-capacitors C_1 and C_2 must be within a narrow range.

In an integrated circuit it is always desirable to eliminate the need for capacitors. In this case, where the capacitors also must have a narrow tolerance, such an elimination is doubly important. Many approaches to center-point triggered flip-flops for integrated circuits exist, of which we shall discuss two.

The circuit shown in Fig. 30 employs two independent flip-flops. Either one of them can be used as the "master," while the other one, called the "slave," merely acts as a memory. Let us assume that in the two flip-flops the two transistors T_1 and T_4 are turned on. The voltages at the collectors of T_2 and T_3 are therefore near $+V_{CC}$ and some current is supplied to the bases of T_5 and T_7 . The resistor values in this circuit are chosen so that only if both voltage sources connected to each gate are positive, there is sufficient base current for a transistor to turn on. If now a positive pulse arrives at the center point, T_5 will have sufficient base current to turn on and cause T_1 to turn off. Hence, the master flip-flop changes states. As the pulse at the center point is removed, a positive voltage

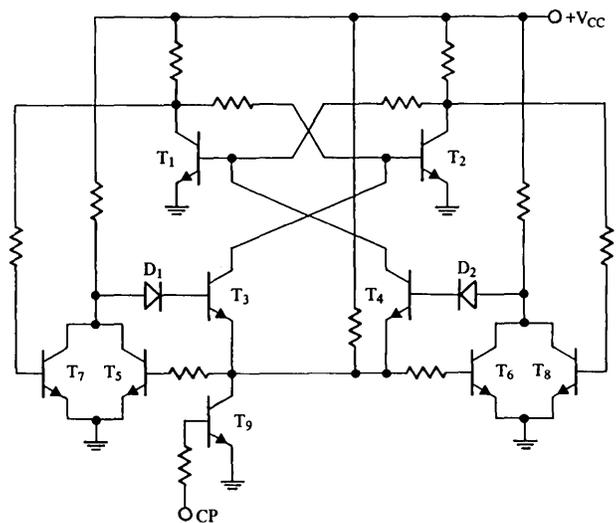


Fig. 31 Center point triggered charge control flip-flop.

becomes available at the collector of T_9 , and T_8 turns on to deprive T_4 of its base current. Thus the slave flip-flop changes states. Since bias is supplied now to the bases of T_6 and T_8 , the next pulse arriving at the center point will cause both master and slave flip-flop to change states again.

In this circuit no capacitors have been used. There is no requirement as to the maximum length of the trigger pulse; in fact, this flip-flop can be triggered with a pulse having an infinitely slow rise time. Due to the large number of resistors and transistors used, however, the maximum trigger rate is somewhat low.

Another approach and one of considerably higher speed is shown in Fig. 31. Here two transistors T_3 and T_4 are used to store a measured amount of charge for a short time. Let us assume T_1 is on and T_2 is off. With positive voltage at the center point, the collector voltage of T_9 is near ground potential. Current thus flows through the diode D_1 and the forward-biased collector-base junction of transistor T_3 to ground. In this state the anode of D_2 is near ground potential, so that no current flows through D_2 and T_4 . As the center point is moved to ground potential, transistor T_3 is suddenly switched into its active region, but its base current is cut off. The charge stored in the forward-biased base-collector diode is released into the base of transistor T_2 . This amount of charge is sufficient to cause the flip-flop to change states. Once T_2 is conducting, D_2 and the collector-base junction of T_4 are forward-biased. Upon the next trigger pulse, a similar amount of charge is delivered to the base of T_1 , causing the flip-flop to change states again.

In this arrangement center-point triggering is again achieved without the help of capacitors. The trigger pulse width can be varied over a wide range without affecting the charge released for triggering.

An integrated center-point triggered flip-flop employing field-effect transistors is shown in Fig. 32. All transistors are of the enhancement mode, insulated gate type.

Transistors T_1 and T_2 form the basic flip-flop. Let us assume that T_1 is on and T_2 is off. With the center point at ground potential, the drain of T_9 is at $-V_{CC}$.

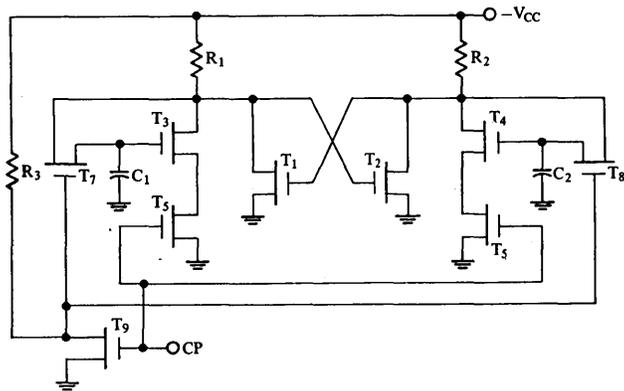


Fig. 32 Center point triggered flip-flop circuit employing field effect transistors.

Thus T_7 and T_8 are conducting and with T_2 off, the capacitor C_2 is charged with a negative voltage, while C_1 remains uncharged.

As a negative pulse arrives at the center point, transistors T_5 and T_6 are turned on and T_7 and T_8 are turned off. The charge stored in C_2 thus causes T_4 to conduct shorting out T_2 , and the flip-flop changes states.

Due to the high input impedance of field effect transistors the two capacitors used in this circuit can be very small—small enough for economic integration. Similar to field effect transistor logic gates, the load resistors can be replaced with source-gate shorted field effect transistor. With this approach the flip-flop of Fig. 32 has the advantage over the previous ones of requiring only a very small area.

LARGE SCALE INTEGRATION

So far we have considered the integration of single digital circuits. In computers it is highly desirable to combine as many circuits as possible in one block. In this way the number of interconnections between the blocks is reduced, enhancing the reliability. In addition, large scale integration offers the possibility of reduced propagation delays since the circuits are in close proximity.

Foremost among the problems encountered in large scale integration is the drastic reduction in yield encountered when the total number of elements is increased beyond the optimum point. However, this optimum point is primarily a function of photolithographic resolution and process control, both of which can be expected to improve with time.

In order to realize some of the potentials of large scale integration "discretionary" wiring is occasionally used. In this approach an oversupply of elements or circuits is provided. These elements or circuits are then tested on the slice and an individual interconnection pattern which avoids faulty units is generated. With this approach the total circuit yield can be greatly enhanced. The cost of this process is considerable; in addition to the individual testing and mask fabrication required, space is wasted in each chip because of the area required for the test-connection pads.

The second problem in large scale integration is that of power dissipation. Even though this power might be small per circuit, the large number of circuits

combined in one chip and the many chips mounted close together to reduce propagation delays create a difficult cooling problem. In order to remove the produced heat, without sacrificing space advantages, coolants must be circulated through the assemblies.

Most significant from the designer's point of view is the problem of partitioning of the entire system. It is in this realm that integrated circuits are having an important influence on systems design.

With single integrated circuits a system such as a computer is designed and partitioned so that a small variety of circuits could be used. Moving toward large scale integration a number of circuits are combined to reduce the number of interconnection pins required. The combination is chosen according to function and is thus different for various parts of the computer. Therefore, a larger variety of packages results. Unchecked, this process could result in so many different packages that the chief economical advantage of integrated circuits (low cost with high production) would be lost.

It is thus desirable to design the system so that it can be partitioned into a number of identical or at least similar subsystems. An example of systems where such an approach is relatively easy to follow are the memory sections of large computers.

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This test technique for digital logic modules and circuit boards simultaneously exercises and compares logic modules of unknown quality against an identical functioning module of the type under test.

A DIGITAL LOGIC MODULE COMPARISON TEST SYSTEM

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The increased use of integrated circuits in instrument and equipment designs has resulted in a dramatic increase in the number and types of test equipment required to perform production testing. The trend to load more and more complex digital logic capability into an increasingly smaller space presents additional production flow problems to the manufacturer's test department. The attendant increase in work load has caused test costs to skyrocket and in some cases has created the need to design and utilize additional test equipment.

This article describes a new digital logic module test system, which we developed to perform fast automatic checkout of various complex modules and printed circuit boards, in different production run quantities. The system was developed for in-house use in order to break an impending production bottleneck. To be effective, the required system for this application had to be fast and relatively easy to use — hence, automatic.

Rather than design a test system with internal capability to generate stimulus and response signals for every possible situation, a more straightforward approach has been taken using a comparison technique.

THE COMPARISON TECHNIQUE

The comparison approach to testing is simple, and the benefits are apparent. The system is easy to



Operator compares unknown module with reference module at console of the digital logic module comparison test system.

operate and economical, and in addition is fast, efficient and flexible. The tester employs a "reference" module of quality known to be good as a basis for comparison against which production modules are tested. Identical test inputs are applied simultaneously to both the reference and production modules in a programmed sequence. Responses at all connector pins are compared simultaneously. The computer which acts as a system controller is programmed to recognize a good module from a bad one and, upon

detection, all module faults are outputted as an error message on the system Teleprinter (Fig. 1).

Since the reference module is, in effect, a dynamic memory of proper test results, large, expensive computer memory is not required. This type of "hardware memory" can also be kept current to production changes right along with the production units being tested.

The heart of the system is the comparison circuits, which are contained on plug-in cards within the computer. A close-up of this part of the test system is shown in Fig. 2. Output signals from the two modules being compared are subtracted by a differential amplifier, routed to a comparator circuit, and tested to see if the subtraction results in an error outside the programmable tolerances of the comparator. One circuit of this type is required for each set of connector pins to be compared.

PROGRAM TIME REDUCED

The comparison technique substantially reduces programming details. Since the reference board does the work of generating the desired outputs, the programmer needs only to specify the input state and the tolerance of the compared result of the two modules. This eliminates programming time; and results in a second benefit. Intimate knowledge of the functions

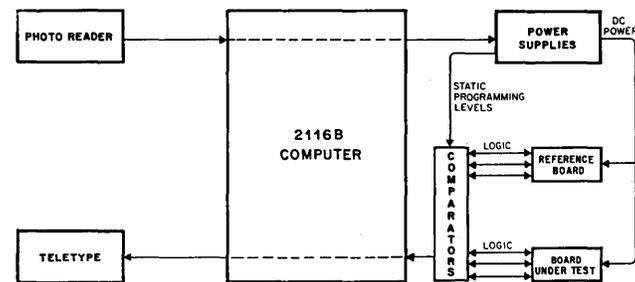


Fig. 1 Block diagram of the digital logic module test system.

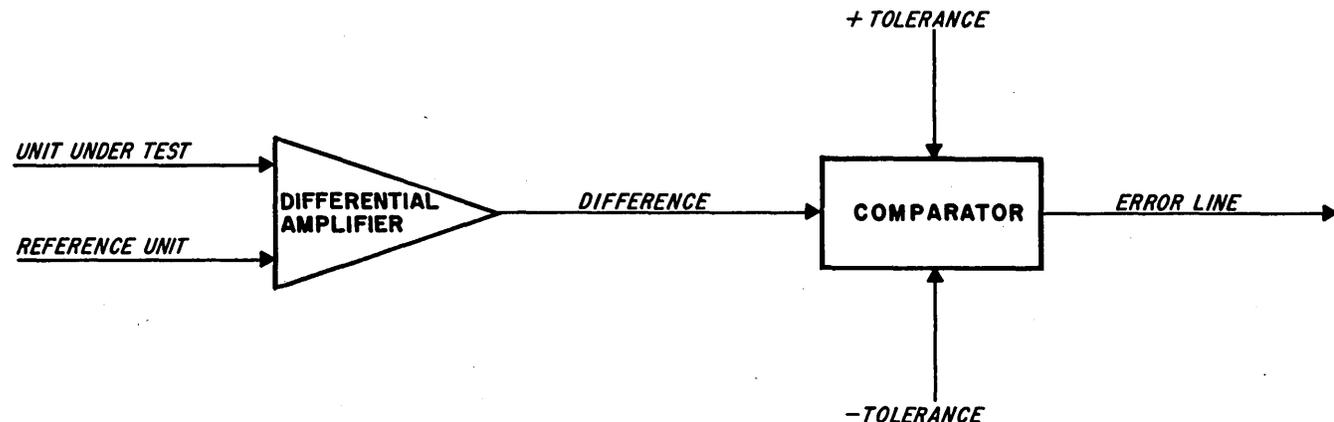


Fig. 2 Comparison circuits of the test system.

of the module for which he is writing a program is not required by the programmer. He needs only to be familiar with digital logic in general.

To maximize the savings in programming time, a special testing language called AuTest has been developed. This language, discussed later in this article, is specifically designed to be quickly learned by digital engineering—type people. One day's study was set as a goal for good comprehension of programming techniques and actual use in simple applications. Programming simplification has not decreased the capability of the language, however. AuTest is able to multiply the programmer's efforts, even to the extent of generating thousands of tests with a single statement command—a powerful marriage of automatic test hardware and software.

The language uses English commands and decimal (not octal) numbers. A test program, therefore, can be used as test documentation, which on complex tests is a substantial savings.

TEST INCREASED, BOTTLENECKS DECREASED

Comparison testing, as employed in this system, is capable of 10,000 tests per second on all pins simultaneously. This speed, combined with the simple ability to program many test results in more complete checkout—of even the most complex circuits. This practical expansion of the scope and range of tests performed results in a more thoroughly tested, more reliable product. The speed with which tests are accomplished naturally decrease production bottlenecks.

Actual module testing adds very little time to the production schedule. Once the test program is resident in core, the system operator merely plugs the reference and unknown modules into their test fixtures, types "RUN" on the Teleprinter, attaches the printout sheet to the tested module and goes on to the next unknown module. Further module troubleshooting may be performed using the same test system, as discussed later in this article.

AUTEST SOFTWARE PACKAGE

AuTest speaks the language of digital design engineers and technicians, and less than one day's instruction is required to master the statements needed to write usable test procedures. The language is so easy to use that the programmer does not even have to know the function of the board for which he is writing a program. He merely has to be familiar with digital logic to effectively program the system.

The actual time spent in programming is a function of the complexity of the module to be tested. Programs for most modules can be written in a couple of days time. As stated earlier, two main reasons why this is possible are: (1) the comparison technique requires that only inputs be specified, and (2) the use of easily understood English and decimal commands of the programming language.

An additional capability of AuTest is its conversational mode, a feature that tells the programmer when he has made a mistake, at the time he makes it. It checks each line of programming immediately after it enters the computer, to see if the pins, voltages and other parameters are valid. If invalid statements are encountered the computer prints out the type of error on the system's Teleprinter, and the error can then be corrected prior to execution time.

The conversational mode provides the users, with the ability to insert or delete statements in the program. To insert a statement, the user need only type the word "INSERT", a label, and the statement to be added. To delete a statement, the user types "DELETE" and the label of the statement to be deleted. This function not only allows the user to easily correct a program when writing it, but also allows easy modification of existing programs should module circuitry be changed.

FAULT ISOLATION

The AuTest software package contains statements that enable the user to isolate faults. With these statements the programmer can tell the computer to print a message on detection of a certain type of error. This enables the system to analyze errors as they occur which greatly reduces the time spent repairing faulty modules. The same statements, used to isolate faults can be used to give instructions to the operator. This is useful when jumpers or other modifications to the module are necessary to complete the testing sequence.

BASIC TEST STATEMENTS

AuTest has two basic types of test statements: individual and multiple. These statements specify the connector pins to be tested, and the voltage levels for the input to both the reference and unknown modules. They then allow the system to compare all of the pins of both modules.

The 'individual' test statement initiates a single comparison test. For example, to perform a test that would input a high level into pins 5, 8, X39, and 212, and a low level into pins 6, AB, and 10, the following command would be written:

```
TEST, HIGH (5, 8, X39, 212) LOW (6, AB, 10)
```

This statement would then compare the outputs of all pins. Errors detected on the specified pins would be conveyed to the output on the system's Teleprinter.

The 'multiple' test statement greatly multiplies the power of the programmer's efforts. This statement inputs and tests all possible combinations of the pins specified. It does this by initiating the test in the LOW state, incrementing in a binary fashion to the HIGH state, and returning the pins to the beginning LOW state. For example, the command to perform multiple tests on pins 8, 22, and 7 would be written:

```
TEST, PERMUTE (8, 22, 7)
```

This statement would initiate the following sequence of tests to the pins specified:

Connector Pin	8	22	7
State	LOW	LOW	LOW
	HIGH	LOW	LOW
	LOW	HIGH	LOW
	HIGH	HIGH	LOW
	LOW	LOW	HIGH
	HIGH	LOW	HIGH
	LOW	HIGH	HIGH
	HIGH	HIGH	HIGH
LOW	LOW	LOW	

When a fault is detected on any test, an error message is conveyed to the output on the system's Teleprinter. This message specifies the number of the test statement, where the error occurred and the pins in error. When a test discloses a fault, the hard copy of the error message can be attached to the module and sent to a repair station. Similarly, good test results can be attached and sent to final assembly.

SUMMARY

The comparison technique combined with the AuTest software package has much to offer the digital equipment manufacturer. It saves testing dollars in all phases of its operation. In a time study analysis of the systems application at our company, testing costs of complex printed circuit boards were reduced by a 10 to 1 factor, including test system programming. In some cases this resulted in a reduction of instrument test costs of 60-70%, while concurrently providing an increase in the number and scope of tests performed.

A substantial test cost saving has been accompanied by additional problem remedies: production test bottlenecks are eliminated and production deadlines met; reliability has increased and warranty repair cost decreased; and above all, the customer is more satisfied.

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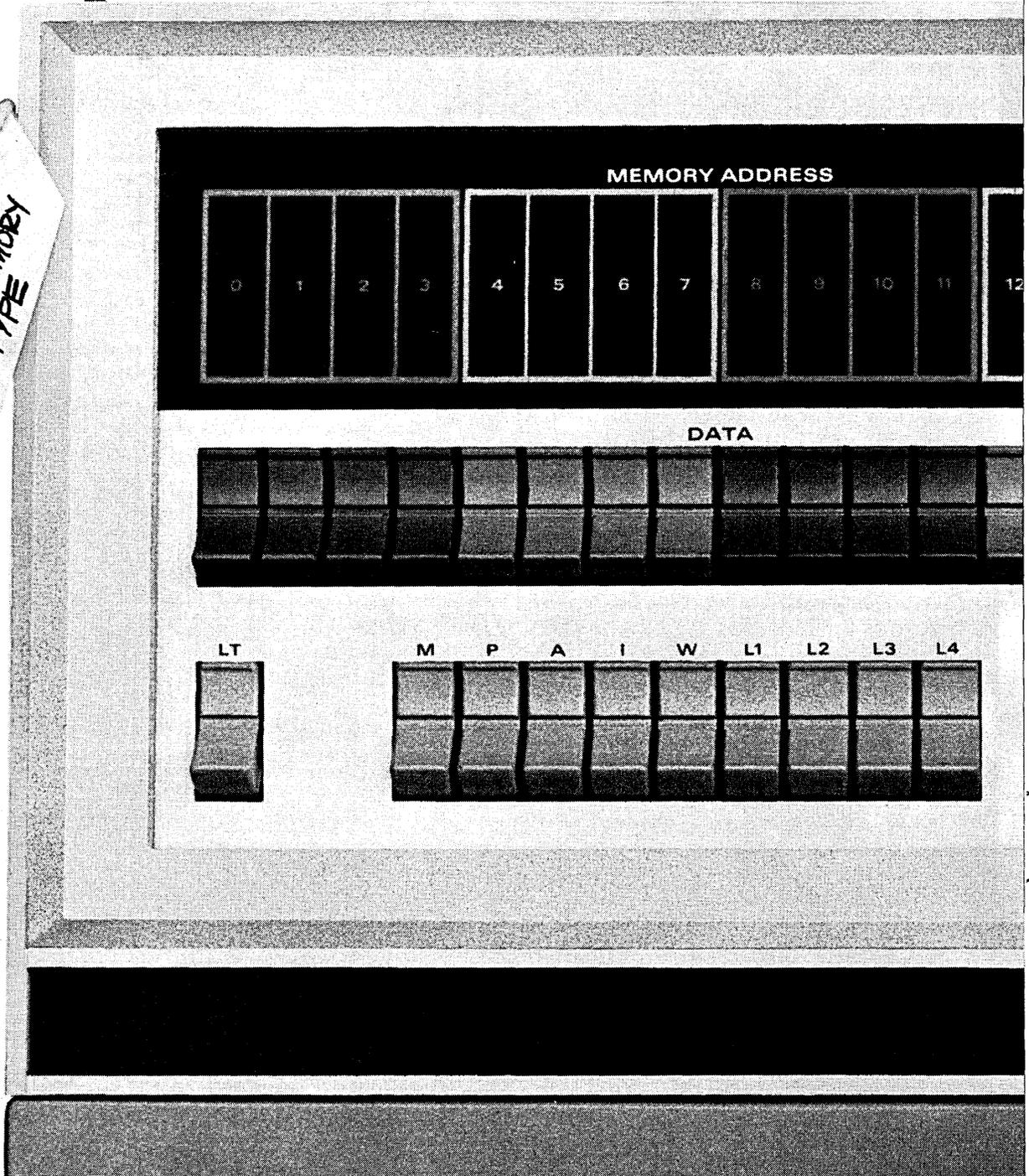
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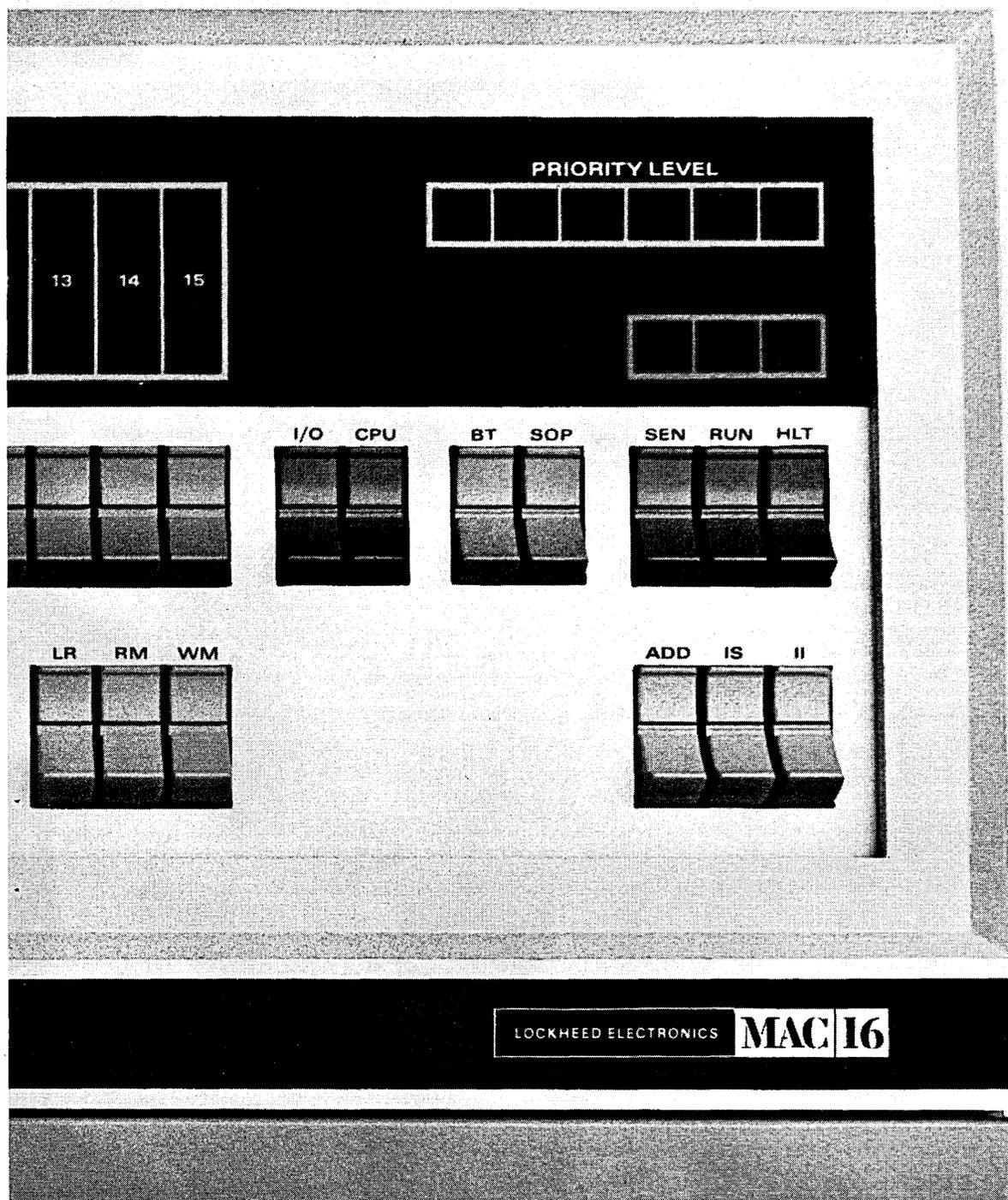
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The first part of this article, system considerations for interfacing tape readers with digital equipment was published in the October issue. This final part presents the logical design of Universal Control Logic.

UNIVERSAL CONTROL LOGIC FOR PHOTOELECTRIC PUNCHED TAPE READERS

Part II – Sequential Logical Design

Gilbert P. Hyatt
Editorial Consultant

Typical signal forms associated with photoelectric punched tape readers for digital system communication are illustrated in Fig. 1. The 8 data bits associated with the tape character are data bit signals B1 through B8, with the tape character skew defined as the lack of coincidence of the data bit signals, shown at the leading and trailing edges of these signals. Superimposed on the center portion of the data bit signals is the "raw" sprocket signal. Leading and trailing edges of tape character signals are relatively square, indicative of an electronic trigger for signal processing. This trigger is not necessarily a requirement if the proper logical mechanization, described in the following text, is implemented. Logical mechanization requires less equipment than the tape character trigger amplifiers. It precludes the requirement for the trigger amplifiers and eliminates many error mechanisms associated with tape reader to digital system communication.

Control logic operation will require two types of inputs from the tape reader. They are the raw sprocket signal (S) and the data bit signals, which are used to form the general bit signal (B). The general bit signal is obtained by the logical OR of all of the eight individual data bit signals in the character. Therefore, the general bit signal (B) will be true from the time that the first data bit on the tape is detected to the time that the last data bit has dropped out (Fig. 1). The B logic signal will, effectively, bracket the tape character; where the B logic signal will be true when any portion of the tape character is read and will be false between the extremities of two adjacent tape characters.

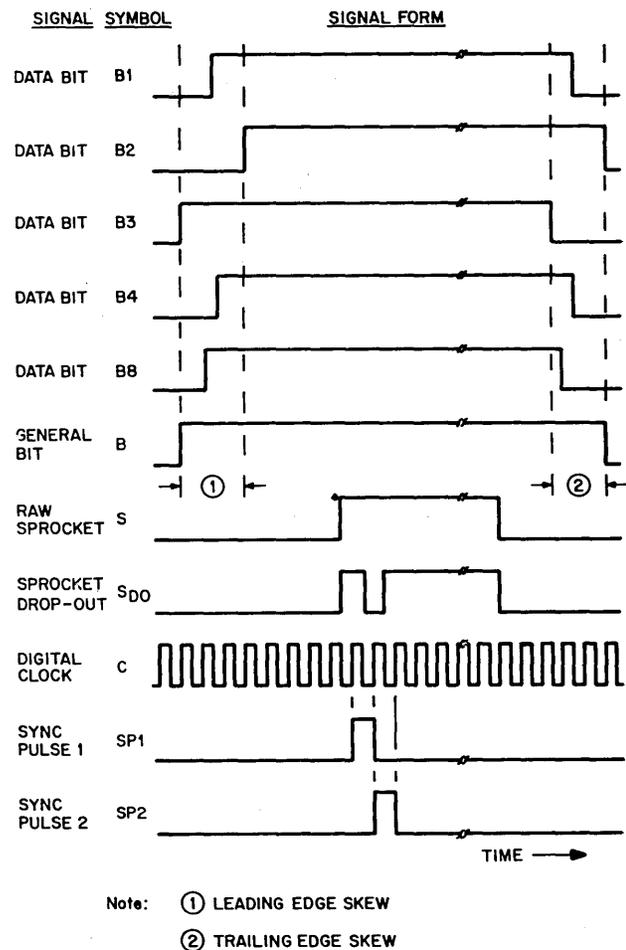


Fig. 1 Typical signal forms.

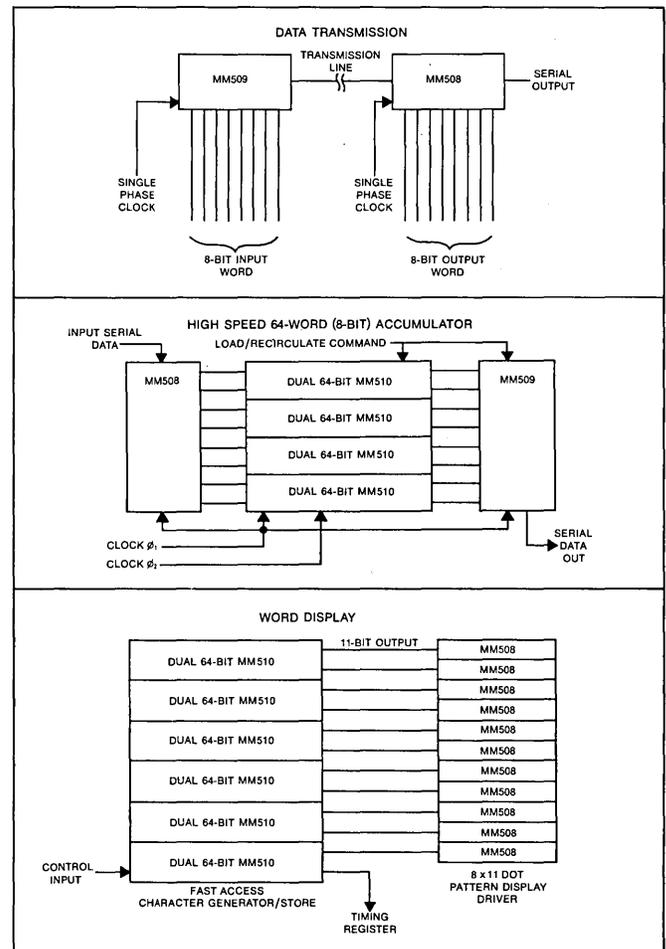
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F2Q F1Q		B S			
		0 0	0 1	1 1	1 0
0	0	P0 ⓪0, 00	P4 ⓪0, 00	P12 01, 00	P8 ⓪0, 00
	1	P1 --, --	P5 --, --	P13 11, 01	P9 11, 01
1	1	P3 --, --	P7 --, --	P15 10, 10	P11 10, 10
	0	P2 00, 00	P6 --, --	P14 ⓪0, 00	P10 ⓪0, 00

WX, YZ
W NEXT STATE OF F2
X NEXT STATE OF F1
Y PRESENT STATE OF SP2
Z PRESENT STATE OF SP1
B, S INPUT STATES
F1, F2 INTERNAL STATES
SP1, SP2 (Y, Z) OUTPUT STATES
WX TRANSITIONARY STATE
WX STABLE STATE
-- "DON'T CARE" STATE

Fig. 2 Karnaugh diagram.

The raw sprocket signal (S) is illustrated in Fig. 1 in conjunction with the digital system clock and data bit signals to show the control logic sequencing and the phase relations of the two signals. Raw sprocket signals will bracket an undefined number of clock pulses due to the sprocket signal pulse width tolerances. They will start on an undefined portion of the clock period, caused by the phase uncertainties due to the asynchronous characteristic of the sprocket signal relative to the clock signals. Sprocket pulse double strobe (drop-out) effect is illustrated in one of its forms, which could result in the same tape character being strobed twice into the digital system if proper precautions are not taken.

The control logic will accept the B and S logic signals and generate a sequence of two synchronization pulses (Fig. 1). These pulses will be used to properly sequence the tape character into the digital system; where the two sync pulses are sequential in nature, precisely one digital system clock period wide, precisely bracketing a clock pulse, and are triggered on by one clock pulse rise time and triggered off by the following one. Once the synchronization pulse sequence is initiated, a sprocket signal dropout will have no effect upon the completion of the sequence. In addition, once the sequence is completed the output is locked-up for the duration of the tape character. In this manner, the raw sprocket signal will initiate the pulse sequence; but, once initiated, the sprocket cannot discontinue the sequence or start a second sequence for that tape character. This sequence will be locked-up for the duration of the tape character and will not function again until the B logic signal has dropped out at the end of the tape character.

LOGICAL DESIGN

Logical design of the Universal Control Logic will be described with respect to synchronous sequential de-

sign techniques. These techniques are illustrated in Fig. 2 using a Karnaugh diagram. Input states are listed across the top as the B and S logical signals. Internal states are listed down the left side as the F2 and F1 flip-flop outputs. Development of the Karnaugh map required four internal states defined by the F2 and F1 flip-flops. The next states of these flip-flops are illustrated in the appropriate box, while the two output states, defined as Sync Pulse 1 and Sync Pulse 2, are to the right of the comma in each Karnaugh map state. Stable states are defined with a circle around the next state term and occur in cases where the next state corresponds to the present state. Transition states are illustrated without circles to indicate that the next clock pulse will cause the control logic to make the transition to the next state shown in the Karnaugh map. Minterm designations of the canonical forms are shown in the upper right hand corner of each Karnaugh map state as the "P" term.

Horizontal transitions in the Karnaugh diagram are results of changes in the B and S input conditions, which are asynchronous functions determined by tape motion. Vertical transitions are accomplished only from transitionary (not circled) states and are synchronous in nature, initiated by the clock pulses. Vertical transitions can not occur for a stable (circled) state until the input state changes to move operation into a transitionary state.

The sequential logical design used in this mechanization follows techniques described in references listed in the bibliography. It should be noted that synchronous logic elements (flip-flops) are used for the secondary state implementation. Therefore, considerations like critical races and various types of hazards do not apply to this logical design.

The Karnaugh map will be developed with respect to the time domain diagram, (Fig. 1) and the truth table and sequencing diagram illustrated in Fig. 3. Operation of the tape reader can begin at any arbitrary point, but will be assumed to start between tape characters, where neither a general bit (B) nor sprocket signal (S) exists. Input signals for this state are logical 0's for the B and S signals and logical 0's for the two internal flip-flops. When the tape starts moving, the first new signal encountered will be the B logic signal when the leading edge of a data bit is detected. This will cause a transition from the P0 to the P8 stable state as illustrated in Figs. 2 and 3. An output sync pulse will not be generated in the P8 state due to the tape character ambiguity caused by the leading edge skew effect. The next condition to occur will be the detection of the sprocket pulse, causing the control logic to make the transition to the P12 state. An output sync pulse is not generated in the P12 state due to the possibility that the clock pulse may have been "shaved", caused by the asynchronous nature of the transition from the P8 to the P12 state.

The first clock to occur in the P12 state will cause the transition to be made to the P13 transitionary state, where the synchronous nature of the logic will preclude errors due to "shaved" clock pulses for the transition through the P12 state. The control logic will remain in the P13 transitionary state for exactly one clock period. This transitionary state will gen-

P Term	Input Conditions		Internal States		Description	Normal Sequence	Double Strobe	Tape Leader	Sync Pulses	
									2	1
	Bit Signal (B)	Sprocket Signal(s)	MSB (F2Q)	LSB (F1Q)						
P0	0	0	0	0	INBETWEEN TAPE CHARACTERS				0	0
P1	0	0	0	1	IMPROPER SEQUENCE		0	0		
P2	0	0	1	0	UNLOCK READ LOGIC		0	0		
P3	0	0	1	1	IMPROPER SEQUENCE		0	0		
P4	0	1	0	0	TAPE LEADER		0	0		
P5	0	1	0	1	IMPROPER SEQUENCE		0	0		
P6	0	1	1	0	IMPROPER SEQUENCE		0	0		
P7	0	1	1	1	IMPROPER SEQUENCE		0	0		
P8	1	0	0	0	BIT LEADING EDGE		0	0		
P9	1	0	0	1	SYNC PULSE 1 (DOUBLE STROBE)		0	1		
P10	1	0	1	0	LOCK-UP READ LOGIC		0	0		
P11	1	0	1	1	SYNC PULSE 2 (DOUBLE STROBE)		1	0		
P12	1	1	0	0	ENABLE SYNC SEQUENCE		0	0		
P13	1	1	0	1	SYNC PULSE 1 (NORMAL)		0	1		
P14	1	1	1	0	LOCK-UP READ LOGIC		0	0		
P15	1	1	1	1	SYNC PULSE 2 (NORMAL)	1	0			

Fig. 3 Truth table and flow diagram.

erate an output defined as Sync Pulse 1, shown as the logical O1 output in the P13 state of the Karnaugh map (Fig. 2). When the next clock pulse sequences the logic, operation will be transferred to the P15 state; defined by the 11 next state term in the P13 box. In the P15 state, sync pulse 2 will be generated for exactly one clock period. At the end of that period, the clock pulse will cause the control logic to make the transition to the P14 stable state, which will result in a "lock-up" of the control logic and disabling of further sync pulse outputs.

As the tape continues past the read head, the sprocket signal will drop out causing the transition to the P10 stable state; which will continue the "locked-up" condition of the control logic. A short time after the sprocket signal (S) has dropped-out, the bit signal (B) will drop-out; thereby causing the control logic to move to the P2 transitional state and, on the next clock pulse, to the P0 stable state pending the arrival of the next tape character. This latter transition will unlock the control logic and permit the generation of a new sync pulse sequence when the next proper tape character is detected.

The states in the Karnaugh map that contain dashes (—,—) are "don't care" functions, where the control logic can never make the transition to these states during normal operation. It is possible that, during the equipment power turn-on sequence or for B signal drop-out, the control logic could enter a "don't care" state. Therefore, it is necessary to ensure that these "don't care" states are transitional states, where the transition will be to a proper and stable state. This will prevent conditions such as the equipment turn-on-operation from causing the control logic to "lock-up" in a stable, but erroneous state that could preclude transitions to states that would permit proper operation.

The double strobe effect, described in Part 1 of this article, is a condition that can be eliminated merely by allowing the double strobe type of transitions to

be properly handled by the control logic. This is accomplished by logically defining the double strobe transitions in Figs. 2 and 3 and ensuring that these are acceptable logical conditions. Internal states of the machine that are characterized by the double strobe contingency are defined as the P9 and P11 states. These states will be entered when a sprocket signal has existed, but has been dropped out during the sequence. It can be seen that the P9 state is similar to the corresponding P13 state and the P11 state is similar to the corresponding P15 state. Therefore, transitions can be made from either pair of these states vertically or within these pairs horizontally in the Karnaugh map without affecting the sequencing or output conditions associated with the control logic. For example: when operating in the P13 state, the transition to the P15 state will be made under normal sequencing or the transition to the P11 state will be made if the sprocket drops out. If the sprocket signal drops-out prior to the clock occurrence when in the P13 state, the transition will be made from the P13 to the P9 state; where the transition can be made back to the P13 state if the sprocket signal picks-up prior to the arrival of the next clock pulse. If the sprocket does not pick-up, the clock pulse will cause the transition to be made from the P9 state to the P11 state; which then can make the transition to the P15 state if the sprocket picks-up before the arrival of the succeeding clock pulse, or to the P10 state if the sprocket remains dropped-out when the next clock pulse arrives. The control logic will remain locked-up in the P10 and P14 states until the complete tape character passes. All of the transitions will be made vertically for output sequencing independent of the sprocket pulse remaining; but the transitions will be made horizontally as the sprocket drops out and pulls in. After once initiating the sequence, it will continue independent of the action of the sprocket; then lock-up in the P14 or P10 states to preclude the possibility of a double strobe error. The double strobe effect will

P	Input States		Internal States		Next State		D Flip-Flop		RS Flip-Flop				T Flip-Flop		Sync Pulse	
	B	S	F2Q	F1Q	F2Q	F1Q	F2D	F1D	F2S	F2R	F1S	F1R	F2T	F1T	SP2	SP1
P0	0	0	0	0	0	0	0	0	0	-	0	-	0	0	0	0
P1	0	0	0	1	-	-	-	-	-	-	-	-	-	-	-	-
P2	0	0	1	0	0	0	0	0	0	1	0	-	1	0	0	0
P3	0	0	1	1	-	-	-	-	-	-	-	-	-	-	-	-
P4	0	1	0	0	0	0	0	0	0	-	0	-	0	0	0	0
P5	0	1	0	1	-	-	-	-	-	-	-	-	-	-	-	-
P6	0	1	1	0	-	-	-	-	-	-	-	-	-	-	-	-
P7	0	1	1	1	-	-	-	-	-	-	-	-	-	-	-	-
P8	1	0	0	0	0	0	0	0	0	-	0	-	0	0	0	0
P9	1	0	0	1	1	1	1	1	1	0	-	0	1	0	0	1
P10	1	0	1	0	1	0	1	0	-	0	0	-	0	0	0	0
P11	1	0	1	1	1	0	1	0	-	0	0	1	0	1	1	0
P12	1	1	0	0	0	1	0	1	0	-	1	0	0	1	0	0
P13	1	1	0	1	1	1	1	1	1	0	-	0	1	0	0	1
P14	1	1	1	0	1	0	1	0	-	0	0	-	0	0	0	0
P15	1	1	1	1	1	0	1	0	-	0	0	1	0	1	1	0

Fig. 5 Sequential design table.

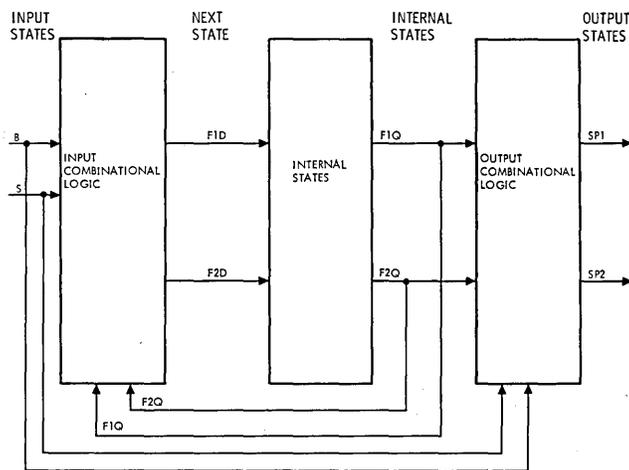


Fig. 4 Control logic functional diagram.

cause transitions illustrated by the horizontal (or diagonal) lines in Fig. 3, where the various transitions can be made between the normal sequence and the double strobe sequence states. The various transitions can be made back and forth between the double strobe states and the normal sequence states without interrupting the proper internal sequence of the control logic or the output sync signals.

A special sequence will be exhibited by a tape leader, where it contains sprocket holes, but not data bit holes. For this condition, the control logic will make the transition from the P0 state to the P4 state, then back to the P0 state for each sprocket signal detected; while not permitting generation of output sync pulses.

A sub-mode of operation could exist where a noise pulse or other error mechanism causes the B logic signal to drop out while in the P8 state, the control logic makes the transition back to the P0 stable state. If the new sprocket signal (S) occurred while the bit signal was dropped out, the control logic would make the transition from the P0 to the P4 stable state. All of these states are stable and would not cause output signals until both the sprocket and bit signals were present simultaneously. This would cause the transi-

tion to be made to the P12 transitional state to initiate a normal sequence of operation.

It is conceivable that the B signal could drop out during the output sequence, thereby transferring operation to the "don't care" states in the Karnaugh diagram (Fig. 2). This condition is defined as a gross error, where the absence of all data bit signals (B1 thru B8) will generate a parity error; thereby discontinuing tape reader operation (see third reference in Bibliography).

SYNCHRONOUS SEQUENTIAL LOGICAL DESIGN

The functional diagram of the control logic is illustrated in Fig. 4, where the input combinational logic operates on the input states from the tape reader in conjunction with the internal states of the control logic to generate the next state conditions for the control logic.

The detailed logical representation of the synchronous sequential logic is illustrated in truth table form (Fig. 5). The canonical minterm designations listed in the P column, correspond to the P states of Figs. 2 and 3. The input states are defined as the bit (B) and sprocket (S) signals. The internal states are defined as the states of flip-flops F2 and F1. The next state logical signals are a function of internal state memory devices used. Therefore, the table will define the input combinational logic required for internal memory devices implemented as D-flip-flops, set-reset-flip-flops, and trigger flip-flops. In addition the output states of the control logic are shown as individual sync pulse lines.

The control logic truth table associated with the two input and two internal states (Fig. 5), completely defines the next state and output state of the device. The next states for the internal flip-flops are defined in the columns corresponding to the type of flip-flop, and were derived from the Karnaugh map (Fig. 2). For example, the P0 state is stable and will, therefore, have the next state equal to the internal state; defined by a circled 00 next state parameter in Fig. 2. The

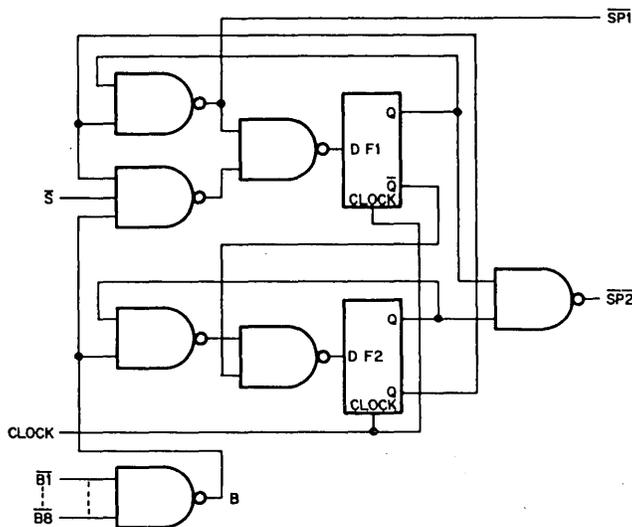
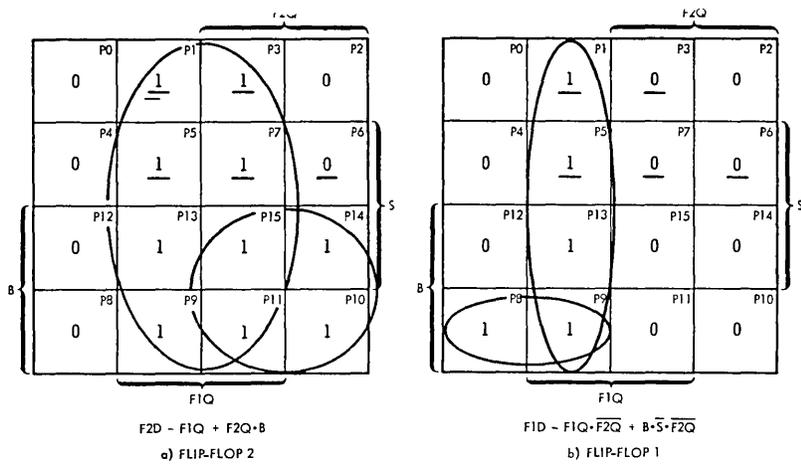


Fig. 7 (a, b & c) D Flip-flop logical mechanization.

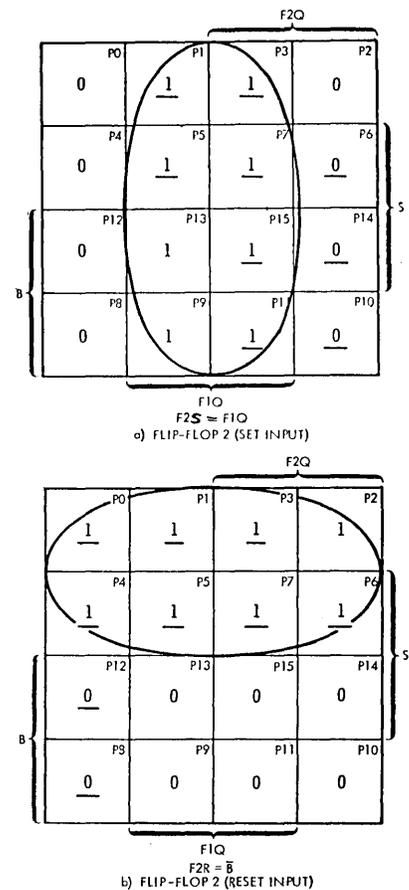


Fig. 8 (a & b) RS Flip-flop logical mechanization.

D FLIP-FLOP		
PRESENT STATE	NEXT STATE	D INPUT
0	0	0
0	1	1
1	1	1
1	0	0

RS FLIP-FLOP			
PRESENT STATE	NEXT STATE	S INPUT	R INPUT
0	0	0	—
0	1	1	0
1	1	—	0
1	0	0	1

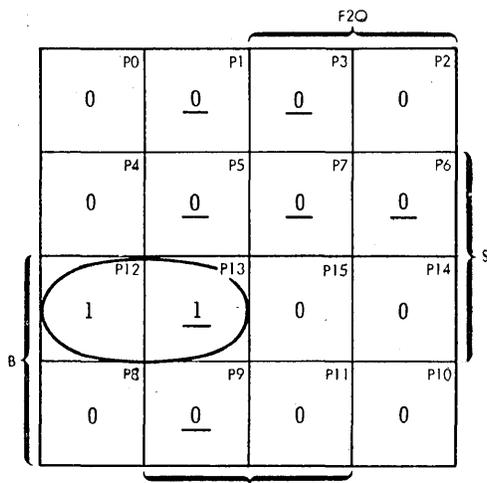
T FLIP-FLOP		
PRESENT STATE	NEXT STATE	T INPUT
0	0	0
0	1	1
1	1	0
1	0	1

Fig. 6 Flip-flop logical definition.

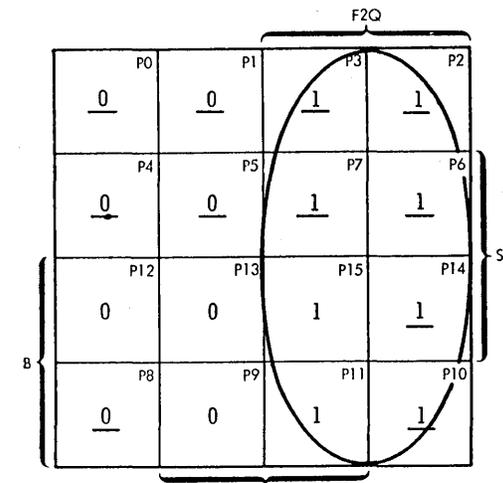
P1 internal state is a "don't care" function, as it cannot be entered under normal operation. Therefore, the next state for P1 is undefined. Similarly, the P2 state will make the transition to the P0 state, defined by the 00 next state parameter in the P2 state box. The balance of the state terms of Fig. 5 can be obtained in a similar manner using the Karnaugh map of Fig. 2. This design technique will be used to generate the logical equations for each of the flip-flop inputs that will implement the transition from the internal state to the next state. These techniques are developed for three types of flip-flops to define the optimum type of circuit and to illustrate the sequential design techniques.

The logical definition of each of the flip-flops is presented in Fig. 6. Applying the internal and next state conditions in Fig. 5 to the flip-flop "transfer functions" presented in Fig. 6 will permit the input logical conditions for each type of flip-flop (D, RS, or T) to be derived as illustrated in the corresponding columns of Fig. 5.

The input logical conditions for the D, RS, and T flip-flops are presented in Veitch diagram form in Figs. 7, 8 and 9 respectively; as derived from the table



$FIS = B \cdot S \cdot \overline{F2Q}$
 c) FLIP-FLOP 1 (SET INPUT)



$FIR = F2Q$
 d) FLIP-FLOP 1 (RESET INPUT)

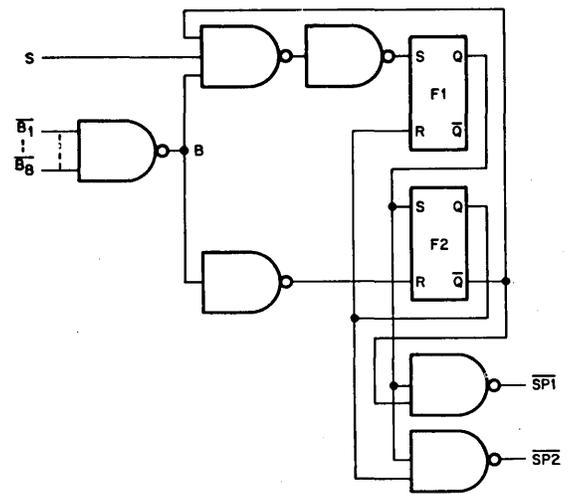
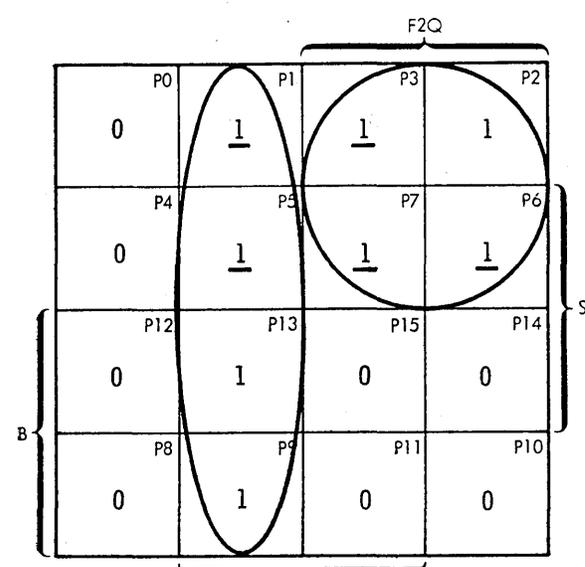
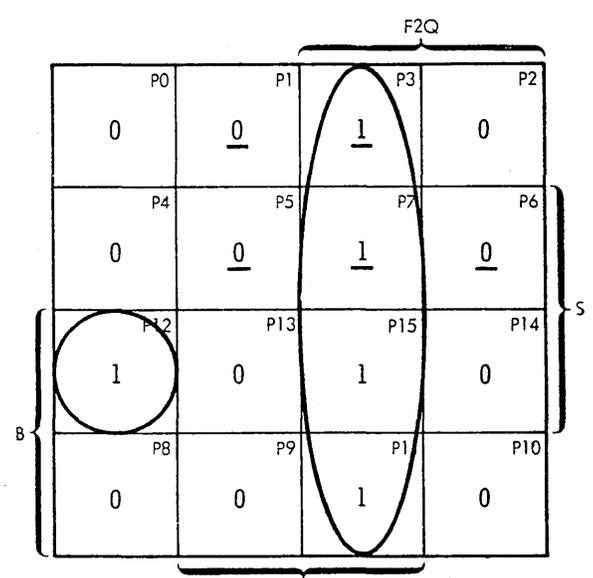


Fig. 8 (c, d & e) RS Flip-flop logical mechanization.



$F2T = FIQ \cdot \overline{F2Q} + \overline{B} \cdot F2Q$
 a) FLIP-FLOP 2



$FIT = FIQ \cdot F2Q + B \cdot S \cdot \overline{FIQ} \cdot \overline{F2Q}$
 b) FLIP-FLOP 1

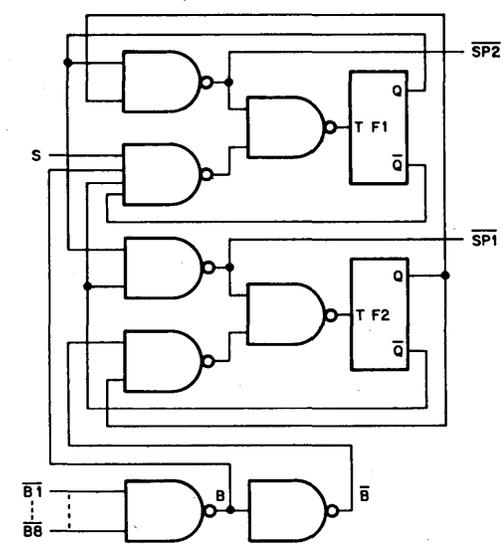


Fig. 9 (a, b & c) T Flip-flop logical mechanization.

in Fig. 5. These diagram representations of the flip-flop input conditions are used to minimize the logical functions, illustrated by the grouping of terms in each diagram. It should be noted that the optimization of the Veitch diagram representation requires the assignment of conditions to the "don't care" terms. These assignments must be checked against the operation defined in Fig. 2 to insure that the control logic will automatically exit from a "don't care" condition if equipment turn-on should force operation into the "don't care" state.

The sync pulse output optimized logical equations are derived in Fig. 10 and applied to the logical diagrams in Figs. 7, 8, and 9.

The output combinational logic requires terms that are sometimes required by the input combinational logic, permitting the two logic blocks to be merged to optimize the design. This is particularly evident in the trigger flip-flop mechanization in Fig. 9, where the logic for the two output sync pulses is identical to the logic for one term of the flip-flop input. Therefore, the output sync pulses can be derived directly from the input combinational logic.

The logical equations corresponding to the Veitch diagram groupings are illustrated with each diagram. The optimized logical diagram, corresponding to the optimized logical equations, for the D, RS, and T flip-flop configurations is shown in Figs. 7, 8, and 9 respectively in conjunction with the associated Veitch diagrams.

SUMMARY

The logical mechanizations; optimized and defined in Figs. 7, 8, and 9, are summarized in Fig. 11. The simplicity of the Universal Control Logic and the multitude of useful operations performed, as described in Part I of this article, yield a basis for the philosophy of performing the maximum amount of signal processing and error compensation in the digital domain. The hardware replaced by this type of control logic and the relaxation of constraints usually imposed on the electro-mechanical, electro-optical, and analog electronic equipment will yield substantial tape reader cost advantages. In addition, digital data communication in complete synchronization with the digital electronic equipment clock and completely independent of the characteristics of the photoelectric punched tape reader presents advantages of inherently compatible

INTEGRATED CIRCUIT CHIP ¹	FLIP-FLOP CONFIGURATION		
	D	RS	T
SINGLE 8-INPUT GATE	1	1	1
DUAL 4-INPUT GATE	0	0	1/2
TRIPLE 3-INPUT GATE	1/3	1/3	0
QUAD 2-INPUT GATE	1 1/4	1	1 1/2
DUAL D FLIP-FLOP	1	0	0
DUAL RS FLIP-FLOP ²	0	1	0
DUAL T FLIP-FLOP ²	0	0	1
TOTAL CIRCUITS	3 7/12	3 1/3	4

¹TEXAS INSTRUMENT 5400/7400 SERIES TOPOLOGY

²DUAL JK FLIP-FLOP EQUIVALENT

Fig. 11 Comparison of alternates.

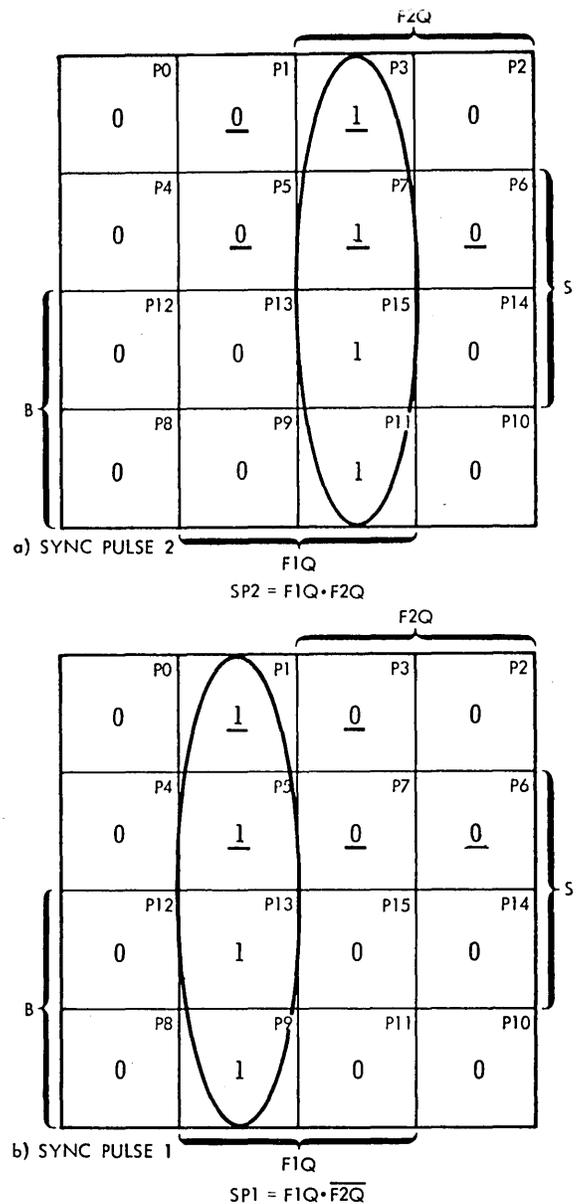


Fig. 10 Sync pulse logical mechanization.

system operation virtually independent of the tape reader and digital electronic equipment characteristics.

The incorporation of Universal Control Logic in photoelectric punched tape readers as a standard item will yield a universal interface with digital equipment and significantly enhance the effectiveness of this type of equipment. It will permit a degree of standardization, compatibility, and problem free operation for punched tape readers that has not been previously available.

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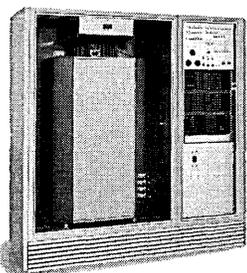
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In the December, 1967 issue of *Computer Design*, G. L. Hollander provided a look at large computer system architecture and how it affects system performance per unit cost. This article is a continuing dialogue of that discussion and points out that if you know what you want to compute, and there is a large amount of it, you can obtain it economically.

ECONOMY OF SCALE AND SPECIALIZATION IN LARGE COMPUTING SYSTEMS*

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Biomedical Computer Laboratory
Washington University School of Medicine
St. Louis Missouri

The development of large computing systems that can be shared among a number of users has been motivated in part by the notion called the "economy of scale." Stated simply this notion asserts that a given computation will be less expensive, the more powerful the system on which the computation is executed. Thus, even though larger systems are more expensive per unit of time, the speed of computation is so great that the cost for a given computation is reduced.

The principle determinant for computer speed is the memory cycle time. No other single factor has had so powerful an influence on performance. Over the past decade memory cycle time has decreased from about 6 μ s to about 2 μ s to about 1 μ s as manufacturers switched from ferrite cores with diameters of 50, 30 then 20 thousandths of an inch in diameter. Meanwhile memory costs have dropped as much as five fold.

Even more dramatic has been the effect of technological development on digital logic. The last decade has seen more than an order of magnitude increase in speed accompanied by a fifty-fold decrease in cost.

COMPUTER ECONOMY EVALUATION

About five years ago somewhat opposing views on the economy of scale were presented by Adams¹ and by Knight.² To aid my own understanding of economies in computing, I decided to review the performance

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of a number of computers presently in production. The selection of eleven machines was made according to my own prejudices, but with memory cycle times all between .75 μ s and 1.00 μ s and with more or less conventional organizations.

If we set out to examine the effect of computer size on the cost of computation, a rather obvious first exercise is the calculation of the cost of a single addition, say at least 32-bits worth. For simplicity we will restrict our attention to central processing equipment. The results are calculated for a minimum configuration of processor, memory and console (each system had 128 K bits of memory which in some cases required a courageous price extrapolation to systems smaller than those available). Fig. 1 shows that the 32-bit addition is at least as costly on the big machines as

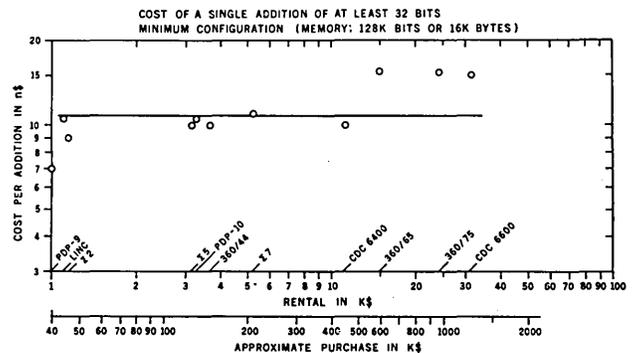


Fig. 1. Estimated cost of a single 32-bit addition in nano-dollars (10^{-9} dollars). The configuration for each machine assumes about 128 kilobits of storage and no peripheral equipment. The equipment cost is shown as either rental or purchase in kilodollars. The cost figure given by the manufacturer was used to estimate the other cost figure using the traditional factor of forty.

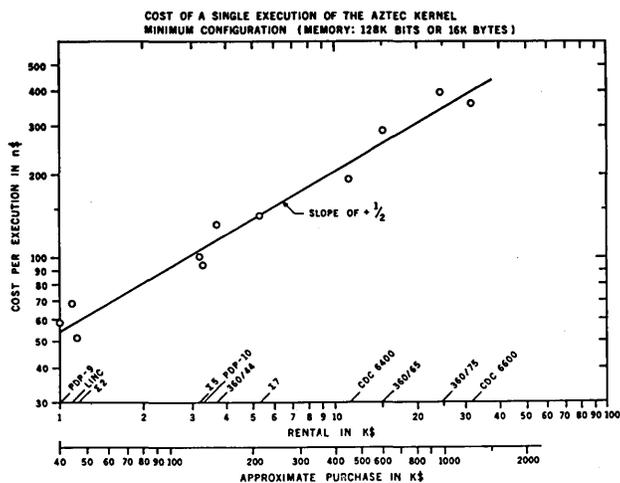


Fig. 2. Estimated cost of a single execution of the AZTEC kernel in nanodollars. The configuration and the abscissa are the same as Fig. 1. Estimates were based on an assembly-language hand-coded kernel.

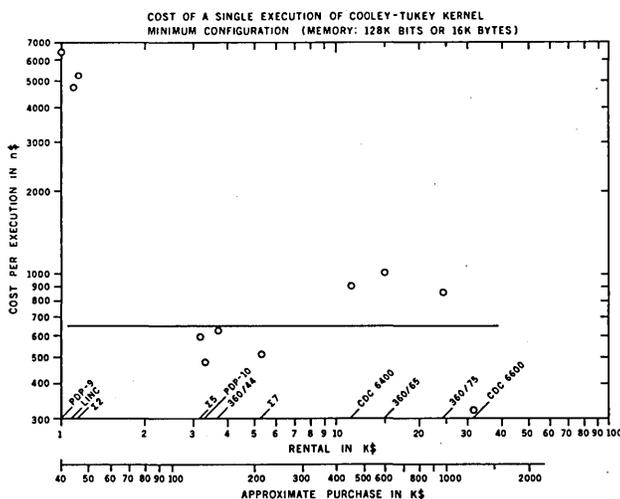


Fig. 3. Estimated cost of a single execution of the Cooley-Tukey kernel in nanodollars. The configuration and the abscissa are the same as Fig. 1. Note the three small machines without floating-point hardware at the upper left and the CDC 6600 with multiple arithmetic units at the lower right.

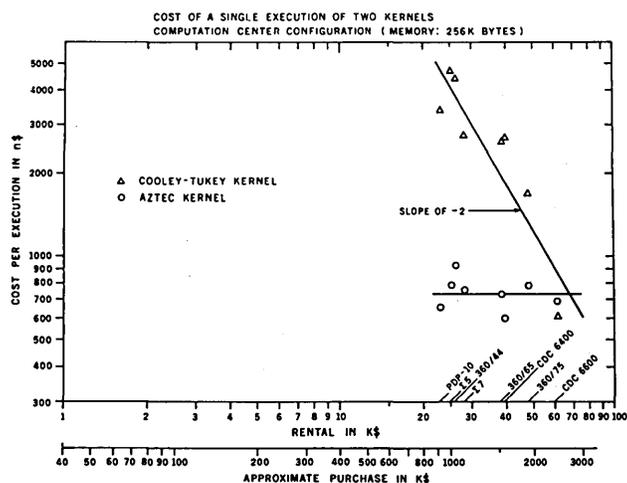


Fig. 4. Estimated cost of a single execution of the AZTEC and the Cooley-Tukey kernels on a typical computation center configuration. This system assumes about 2 million bits of storage, 8 tapes, about 500 million bits of disk storage, a line printer and a card reader. The machine costs indicated along the abscissa reflect the large base cost of this configuration.

on the small ones; obviously not a good demonstration of economy of scale.

Perhaps we should have examined the cost of execution of an entire program, not just a single instruction. I coded an important program segment, or kernel, in assembly language and calculated its execution time for each of the eleven machines. The results for the kernel of a program called AZTEC, developed for pre-processing electrocardiographic data,³ are shown in Fig. 2. Far from demonstrating economies of scale these results seem to indicate that the smallest machines capable of the job would produce the least cost per execution of the AZTEC kernel. This may not be a fair test since the AZTEC algorithm requires much branching and very little computation.

Let's try again with another kernel. This time we will pick a job that requires a large amount of floating-point computation: the Fourier transform of an array of data. The algorithm for this calculation is based on one suggested by Cooley and Tukey⁴, but implemented in the form similar to that described by Molnar.⁵ The results, shown in Fig. 3, are mixed. The small machines with no floating-point hardware (PDP-9, LINC, Σ2) are costly for the execution of this kernel. Those with single floating-point arithmetic units are not too widely spread; the CDC 6600 with a dual multiplication unit and hardware registers for the program loop is comparatively inexpensive.

But all of the foregoing has been somewhat unrealistic, because rather special circumstances would be required to carry out either of the two kernels on a minimum-configuration machine. It would be more appropriate to execute the programs in the setting of a computation center. Fig. 4 shows the calculations repeated for the AZTEC and Cooley-Tukey kernels assuming a rather standard computation center configuration; 2 million bits (256K bytes) of about 1 μs memory, 8 tapes, close to a half-billion bits of disk storage, a line printer and card reader. Only eight machines were considered in this configuration; the three smallest machines could not address 2 million bits of memory. For the remaining eight systems, memory and peripheral devices were adjusted to be as nearly equivalent as possible. First, notice that all machines have shifted their positions to the right along the abscissa. These shifts result from the base cost of memory (averaging about \$10,000 per month) and peripheral devices (also averaging about \$10,000 per month). Clearly the cost of a substantial increment in computational power is small compared to the base cost of memory and peripheral devices. This fact seems to be a crucial one in the analysis of economy of scale.

For the AZTEC kernel no preference for machines large or small is demonstrated here. However, one should not lose sight of the fact that the least costly machine in the computation center configuration is more expensive than any of the machines in the minimum configuration for execution of the AZTEC kernel (Fig. 2)

But now we see clear economies of scale for the Cooley-Tukey kernel. If we accept the line with slope

of -2, we could conclude that doubling the monthly rental would cut the cost per execution by a factor of four. Since the programs more typically executed lie between our highly branching and our highly arithmetic examples, we should expect the performance curve to fall between the two lines in Fig. 4. Thus, if we limit our attention to the computation center environment we do observe some economy of scale.

But the comparisons reviewed so far do not take into account the effect of software on the cost of computation. The economies demonstrated by one computer over another may be nullified by compiler inefficiencies, for example. Thus, these rather specific results should be viewed with caution and only general trends remembered.

SOFTWARE EFFECT

It was convenient to investigate some effects of software on our two kernels within the framework of the amount of specialization appropriate to solve two arbitrarily chosen problems. We have an IBM 360/50 so by necessity it was chosen for several of the following comparisons.

The first of our two problems uses the AZTEC kernel as a model for the kind of computation needed to monitor continuously the electrocardiogram of patients in an acute cardiac unit. We assume 10 beds and a rate of 500 samples per second for a total of 5000 executions of the AZTEC kernel per second, continuously, 24 hours per day. No overhead has been charged for the sharing of a single computer, a rather bold assumption, but one that does not penalize the larger computers.

Fig. 5 shows the cost in dollars per day for the execution of this job in several different ways, first, programmed in G-Level FORTRAN. Here awkward code produced by the compiler more than triples the cost over H-Level optimized FORTRAN or over assembly language. The nearly equal costs of the H-Level compilation and the assembly language is not too surprising when one recognizes that the FORTRAN statements map almost one for one into assembly language.

The abscissa represents a crude specialization coordinate. It indicates, non-metricly, the "down payment" required, before the first execution of the program can be accomplished. Thus, a computer configuration tailored to do the monitoring job and no more is considerably less expensive per execution, but requires a higher down payment. The Programmed Console⁶ is a small specialized computer designed at our laboratory specifically for tasks like AZTEC.

The execution of a three dimensional Fourier transform with a lattice size of 64 x 64 x 64 will require about 2 million executions of the Cooley-Tukey kernel. This is not an unusual requirement in x-ray crystallographic problems and demonstrates the usefulness of fast Fourier transform methods like that of Cooley and Tukey; without it the job might cost 2,000 times as much.

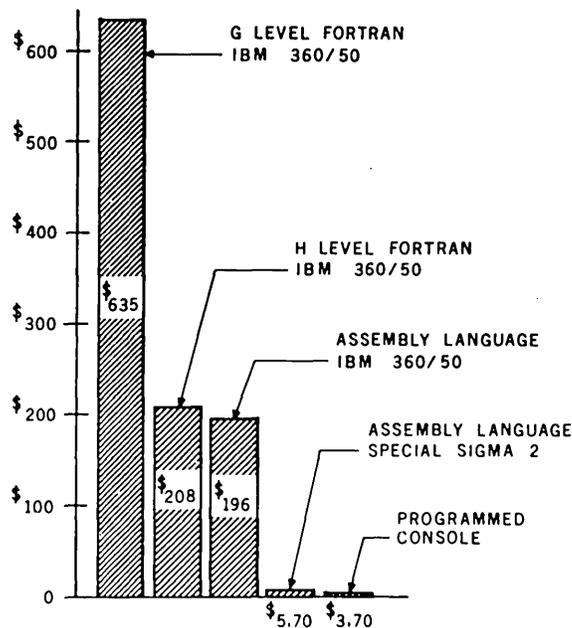


Fig. 5. Estimated cost per day of execution of the AZTEC kernel for each ten beds at 500 samples per second per bed. A time-shared system is assumed with no penalty for system overhead. The abscissa indicates crudely the "down payment" necessary to obtain the first execution.

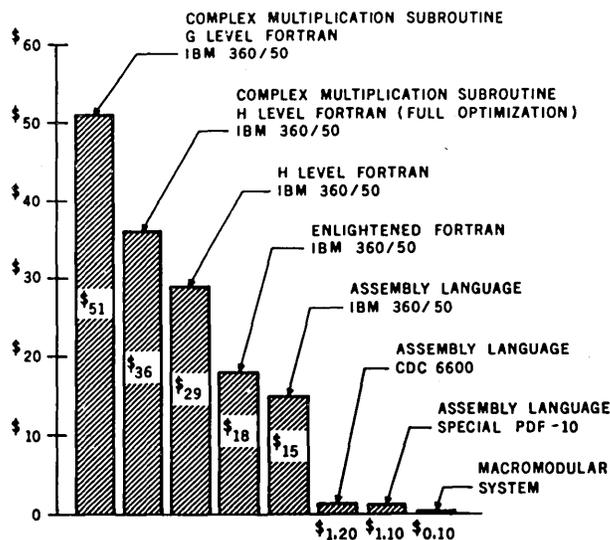


Fig. 6. Estimated cost per execution of a three-dimensional Fourier transform with a lattice size of 64 x 64 x 64. This size problem requires about 2 million executions of the Cooley-Tukey kernel. Again the "down payment" required is suggested by the abscissa.



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Execution of this transform with a minimum down payment would likely use G-Level FORTRAN, variables declared complex and the Cooley-Tukey algorithm. However, as before, optimization of the object program can be achieved by using for compilation the longer running, more space consuming, H-Level FORTRAN. Eliminating calls to the complex multiplication subroutine by declaring all variables real and by explicit complex multiplication in the FORTRAN source program will yield additional economies. Knowledge of the mechanics of the FORTRAN compiler allows the preparation of a FORTRAN source program that is independent of the level of compiler optimization and is almost as fast as the assembly language program.

Each reduction in cost is accomplished by an additional down payment, in several cases solely intellectual. Overall, the cost per execution was cut by more than a factor of three, but the intellectual ante was raised from FORTRAN to assembly language.

A very large cut in cost can be achieved by running the program in assembly language on a CDC 6600. A specially chosen PDP-10 configuration with only the equipment necessary to do the job is also inexpensive. Finally the estimate of the cost of execution of this problem on a macromodular system⁷ specially assembled for the problem (like Molnar's⁵, but with floating point arithmetic and disk storage) shows still another order of magnitude reduction in cost.

CONCLUSION

In summary, we do see some economies of scale within the framework of present computation centers. But even more dramatic are the economies of specialization. We have demonstrated a 500 to 1 reduction in cost as a result of an increase in specialization from straightforward FORTRAN programming to a machine specially assembled for the problem. If we include the economies introduced by the choice of algorithm the ratio is a staggering million to one. If you know what you want to compute and there is a lot of it, you can get it wholesale.

REFERENCES

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CIRCLE NO. 37 ON INQUIRY CARD

A Method of Data Transmission Requiring Minimum Turnaround Time

PAUL E. PAYNE

International Communications Corp.
Subsidiary of Milgo Electronic Corp.
Miami, Florida

A basic requirement placed on present day technology involves the continuous updating and transfer of information between central processing and ancillary equipment. Current demands are for an accelerated rate of information transfer in data communication systems that utilize the public telephone network as the transmission media.

In a data communication system that involves a polling configuration, the reduction of fixed time delays within the system can significantly increase the effective throughput of the system. This application note describes a method of eliminating turnaround time by utilizing the MODEM 4400/48 data set, operating at a fixed transmission rate of 4800 bps. It is applicable to

any central processor and any ancillary devices.

Fig. 1 shows the system layout in its simplest form. The Central Processor will sequentially poll Ancillary Device B followed by Ancillary Device A. Modulators M_1 , M_2 , M_3 , and M_4 are on at all times. Demodulator D_4 is always synchronized to M_1 , and D_1 is always synchronized to M_4 . There is, therefore, no requirement within the system to provide dynamic synchronization times.

The Central Processor polls "B" with instructions to "A" to send after the completion of "B's" message. "A" has been monitoring "B's" message to the Central Processor and detects "B's" end-of-message code. "A" raises Request to Send

which blocks data lead from D_3 to M_2 and which enables data lead from "A" to M_2 . "A" completes its message to the Central Processor. "A" lowers Request to Send to complete the sequence. The Central Processor may poll "A" independently of "B", or "B" independently of "A".

The number of ancillary devices is not limited. The saving in time is achieved by sequentially extracting messages starting with the furthest ancillary and by allowing each polled ancillary to immediately begin its message upon detection of a go-ahead signal which may be a poll directed to the particular ancillary, or an end-of-message from the previous ancillary.

For additional information circle No. 198 on the Inquiry Card.

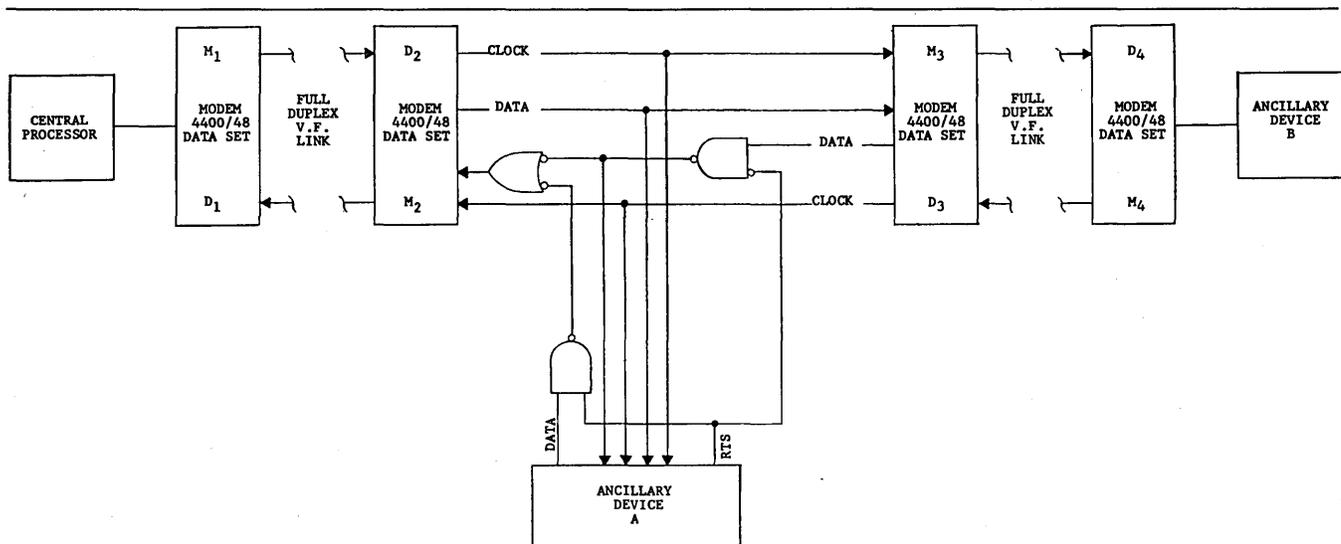


Fig. 1 Polled system layout for reducing data turnaround time.

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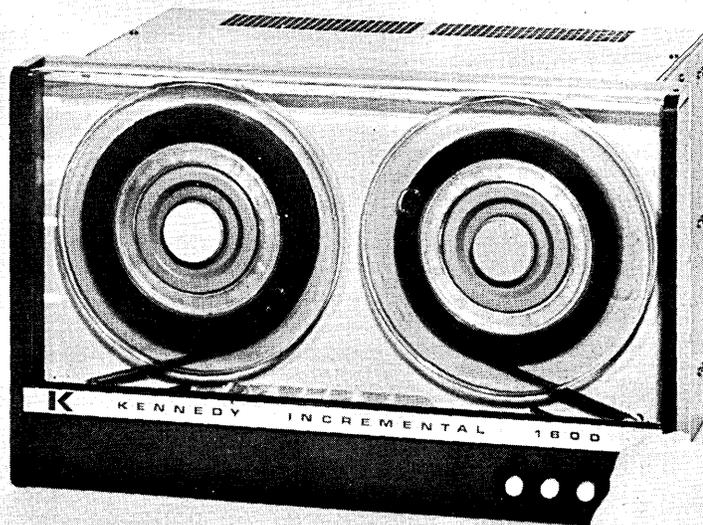
In addition to the write/only version, Model 1600 is available in most of the variations currently offered in other Kennedy models.

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 - Recording format: 7-track IBM compatible
 - Recording speed: 0-300 characters/second
 - Skip rate: 1000 characters/second
 - Density: 200 or 556 BPI
 - Parity generation: Internal, odd or even
 - Gap generation: Internal BOT, EOR, EOF
 - Echo check
 - Input logic levels: IC compatible (DTL) OV ± .5V false 4V (min) true
 - Output levels: IC compatible (DTL) OV ± .5V false + 5V true
 - Size: 19 x 12¼ x 10 deep
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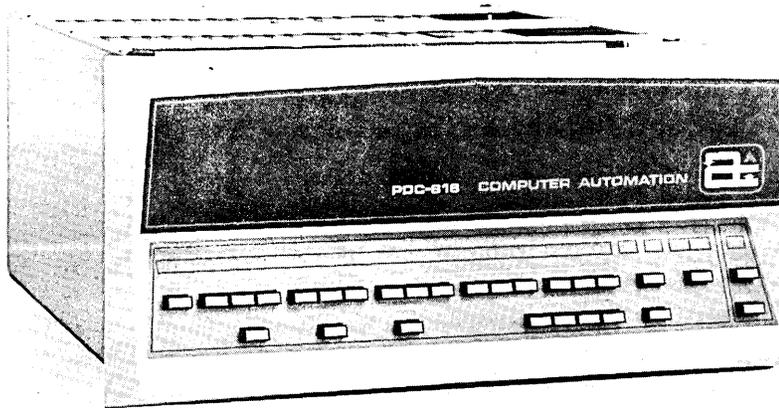
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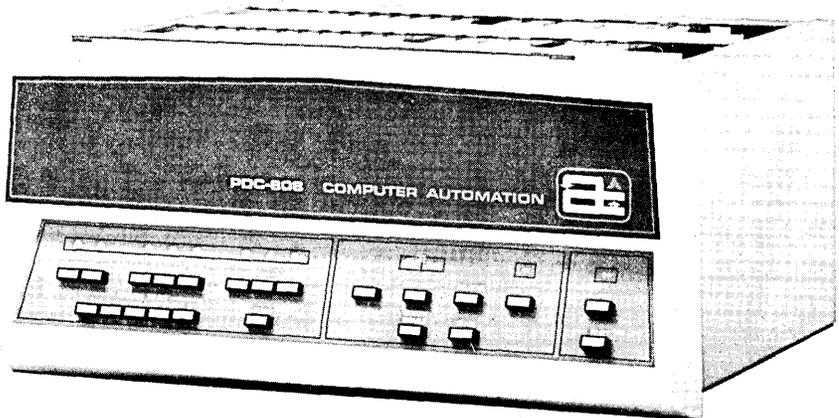
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CIRCLE NO. 40 ON INQUIRY CARD

FALL JOINT COMPUTER CONFERENCE

1968

TECHNICAL PROGRAM EXCERPTS

Brooks Hall : Civic Auditorium

San Francisco

December 9-11

This year's Fall Joint Computer Conference promises to be the most ambitious undertaking in the history of the AFIPS-sponsored conferences. An impressive technical program consisting of forty-seven sessions, with 157 individual presentations and seven panel sessions will offer three full days of heavy involvement for all registrants.

The technical sessions will run from 10:30 A.M. December 9 through most of December 11 and will be held in the Civic Center and at several hotel locations in downtown San Francisco.

Two distinguished educators involved with the impact of computer technology in today's society will be featured speakers. Howard W. Johnson, President of Massachusetts Institute of Technology, will deliver the keynote address for the opening session on December 9. Dr. Garrett Hardin, Professor of Biology at the University of California, Santa Barbara, will address the conference luncheon, December 10.

Pre-registration can be made between 2 and 8 P.M. on Sunday, December 8, at the San Francisco Hilton. An informal cocktail party will be held in the Continental Parlor Six after 4 P.M. for early arrivals. Registration hours at the Civic Auditorium will be 8 A.M. to 5 P.M., December 9 and 10 and 8 A.M. to 12 noon on December 11.

The registration fee for AFIPS members is \$20. Non-member fee is \$30. Those joining one of the member societies at the conference can obtain a \$10 credit toward the registration fee. The fee for full-time students is \$3. This year, there will be a \$5 admission fee for those wishing to visit the exhibits only. There will be no "one day" fee as in previous years. Full registration will include the two-volume proceedings of the technical program.

Due to the magnitude of the technical program, we have selected only the sessions that are of major interest to our readers.

Monday Morning, Dec. 9

Session 1

Time Sharing

Chairman: Kathleen Beisty, Bradford Computer and System, N.Y.
THE PITT TIME-SHARING SYSTEM FOR THE IBM SYSTEM 360., George F. Badger, Jr., University of Pittsburgh.
DEBUGGING IN A TIME-SHARING ENVIRONMENT, William A. Bernstein, IBM Corp.
A TIME-SHARED OPERATING SYSTEM, Alexander S. Lett, IBM Corp.

Session 3

Reliability, Maintenance and Error Recovery In Third Generation Systems

Chairman: Sanford Elkin, Control Data Corp., Palo Alto, Cal.
CONSIDERATIONS FOR SOFTWARE PROTECTION AND RECOVERY FROM HARDWARE FAILURES IN A MULTIPROCESS, MULTIPROGRAMMING, SINGLE PROCESSOR SYSTEM, G. Oppenheimer, RCA Information Systems Div., Camden, N.J.
ERROR RECOVERY THROUGH PROGRAMMING, A. Higgins, IBM Corp., Kingston, N.Y.
OPTS-600, G. W. Nelson, General Electric Co., Phoenix, Ariz.
FAIL-SAFE POWER AND ENVIRONMENTAL FACILITIES FOR A LARGE COMPUTER INSTALLATION, R. C. Cheek, Westinghouse Electric Corp., Pittsburgh, Pa.

Session 4

Numerical Control

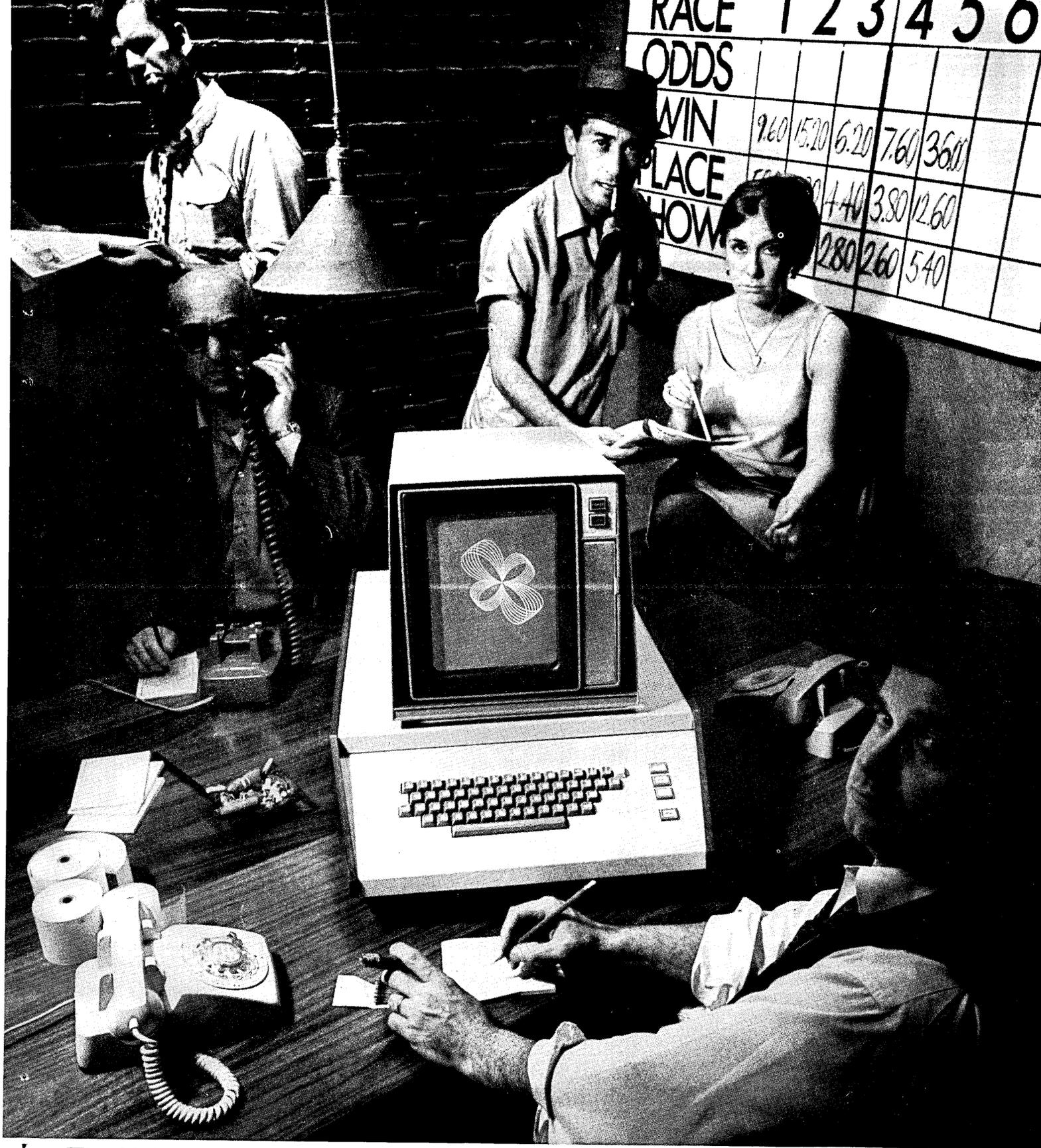
Chairman: Robert Little, IIT Research Institute, Chicago, Ill.
METHODOLOGY FOR COMPUTER SIMULATION, Gastone Chingari, UNIVAC, Philadelphia, Pa.
SUBSETS AND MODULAR FEATURES OF STANDARD APT, Clarence G. Feldmann, MIT, Cambridge, Mass.
A REMOTE BATCH PROCESSING SYSTEM FOR APT, M. E. White, RCA Laboratories, Princeton, N.J.

Session 5

The Computer Field: What Was Promised, What We Have, What We Need (Software Session)

Chairman: Louis Fein, Palo Alto, Cal.
SOFTWARE COMPATIBILITY: WHAT WAS PROMISED, WHAT WE HAVE AND WHAT WE NEED, John A. Gosden, Mitre Corp., Crossroads, Va.
INTERACTIVE SYSTEMS: PROMISES, PRESENT AND FUTURE, Jules I. Schwartz, System Development Corp., Santa Monica, Cal.
MULTIPROGRAMMING: PROMISES, PERFORMANCE AND PROSPECTS, Thomas B. Steel, Jr., System Development Corp.

(continued on page 90)



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Session 6

Applied Mathematics

Chairman: Glen Lewis, University of So. California.

AN ALGORITHM FOR FINDING A SOLUTION OF SIMULTANEOUS NONLINEAR EQUATIONS, R. H. Hardway of Collins Radio Co., Cedar Rapids, Iowa.

AN ECONOMICAL METHOD FOR CALCULATING THE DISCRETE FOURIER TRANSFORM, R. Yawne, Raytheon Co., Bedford, Mass.

NONLINEAR INTERACTIVE STEPWISE REGRESSION ANALYSIS, Leta Edwin, formerly of Comshare, Inc., Ann Arbor, Mich.

RECURSIVE FAST FOURIER TRANSFORMS, George Epstein, ITT Gilfillan, Inc., L.A., Cal.

Monday Afternoon, Dec. 9

Session 7

Panel: The Impact of the FCC Interdependence Inquiry on the Computer Industry

Chairman: Louis Feldner, consultant to Data Communications, Palo Alto, Cal.

Panelists: Manley Irwin and Michael Duggan, Whittemore School of Business and Economics, University of N.H.; Bernard Strassburg of the FCC's Common Carrier Bureau; Paul Rodgers, general counsel, National Association of Regulatory Utility Commissioners, Washington, D.C.; and John Dingell, chairman of the Subcommittee of Regulatory & Enforcement Agencies, U.S. Congress.

Session 9

Terminal Languages

Chairman: Arnold Greenman, Programming Sciences Corp., N.Y. COMPUTER GRAPHIC LANGUAGE, Amalie J. Frank, Bell Telephone Laboratories, Murray Hill, N.J.

TYMSHARE CONVERSATIONAL LANGUAGE, Richard K. Moore, Tymshare, Inc., Palo Alto, Cal.

META PI—AN INTERACTIVE ON-LINE COMPILER-COMPILER, John T. O'Neill, Jr., RCA Laboratories, Princeton, N.J.

Session 10

Frontier Directions in Interactive Graphics

Chairman: Richard Conn, Lawrence Radiation Laboratory.

THE ORGANIZATION AND FORMATTING OF HIERARCHICAL DISPLAYS, G. T. Uber, Lockheed Missiles and Space Co., Sunnyvale, Cal.

PROJECTION OF MULTIDIMENSIONAL DATA FOR USE IN MAN-COMPUTER GRAPHICS, T. W. Calvert, Carnegie-Mellon University, Pittsburgh, Pa.

THE ON-LINE FIRING SQUAD SIMULATOR, R. M. Balzer, Rand Corp., Santa Monica, Cal.

INTERACTIVE TELECOMMUNICATIONS, D. W. Cardwell, Oak Ridge National Laboratory, Tenn.

COMPUTER-DRIVEN DISPLAY FACILITIES FOR AN EXPERIMENTAL COMPUTER-BASED LIBRARY, Donald R. Haring of MIT, Cambridge, Mass.

RESPONSE TIME IN MAN-COMPUTER CONVERSATIONAL TRANSACTIONS, Robert Miller, IBM Corp., Poughkeepsie, N.Y.

Session 12

Digital Simulation of Continuous Dynamic System — Where is it? Where is it going?

Chairman: Jon Strauss, Carnegie-Mellon University.

DIGITAL SIMULATION OF CONTINUOUS DYNAMIC SYSTEMS: AN OVERVIEW, Mr. Strauss.

MATHEMATICS OF CONTINUOUS SYSTEM SIMULATIONS, David H. Brandin, Informatics, Inc., Chicago, Ill.

SALEM—A PROGRAMMING SYSTEM FOR THE SIMULATION OF SYSTEMS DESCRIBED BY PARTIAL DIFFERENTIAL EQUATIONS, S. M. Morris, Lehigh University, N.J.

TAF—A STEADY STATE, FREQUENCY RESPONSE AND TIME RESPONSE SIMULATION PROGRAM, Thomas E. Springer, Los Alamos Scientific Laboratory, N.M.

Discussants: F. J. Sansom, Control Data Corp., and R. D. Brennan, IBM Corp.

Session 16

Plain Talk: Machines That Speak Your Language

Chairman: Gary Martins, RAND Corp., Santa Monica, Cal.

A COMPUTATIONAL MODEL OF VERBAL UNDERSTANDING, R. Simmons, System Development Corp., Austin, Texas.

PROCEDURAL SEMANTICS FOR A QUESTION-ANSWERING MACHINE, W. A. Woods, Harvard University.

A NATURAL LANGUAGE COMPILER FOR ON-LINE DATA MANAGEMENT, Charles H. Kellogg, System Development Corp., Austin, Texas.

Session 17

Pricing Computer Services — What? Why? How?

Chairman: Norman R. Nielsen, Stanford University.

PRICES AND THE ALLOCATION OF COMPUTER TIME, Neil Singer, University of Maryland, College Park, Md.

THE USE OF HARD AND SOFT MONEY BUDGETS AND PRICES, Seymour Smidt, Cornell University, Ithaca, N.Y.

PRIORITY PRICING WITH APPLICATION TO TIME-SHARED COMPUTERS, Maurice Marchand, University of Chicago, Chicago, Ill.

FLEXIBLE PRICING: AN APPROACH TO THE ALLOCATION COMPUTER RESOURCES, Mr. Nielsen.

Session 18

Data Structures for Computer Graphics

Chairman: Andries Van Dam, Brown University.

DATA STRUCTURES AND TECHNIQUES FOR REMOTE COMPUTER GRAPHICS, Ira W. Cotton, UNIVAC, Philadelphia, Pa.

GRAPHICAL SYSTEMS COMMUNICATIONS: AN ASSOCIATIVE MEMORY APPROACH, Edgar H. Sibley, University of Michigan, Ann Arbor, Mich.

DESCRIPTION OF A SET-THEORETIC DATA STRUCTURE, David L. Childs, University of Michigan, Ann Arbor, Mich.

Session 19

Hybrid Systems for Partial Differential Equations

Chairman: J. D. Kennedy, J. D. Kennedy Co., Palo Alto, Cal.

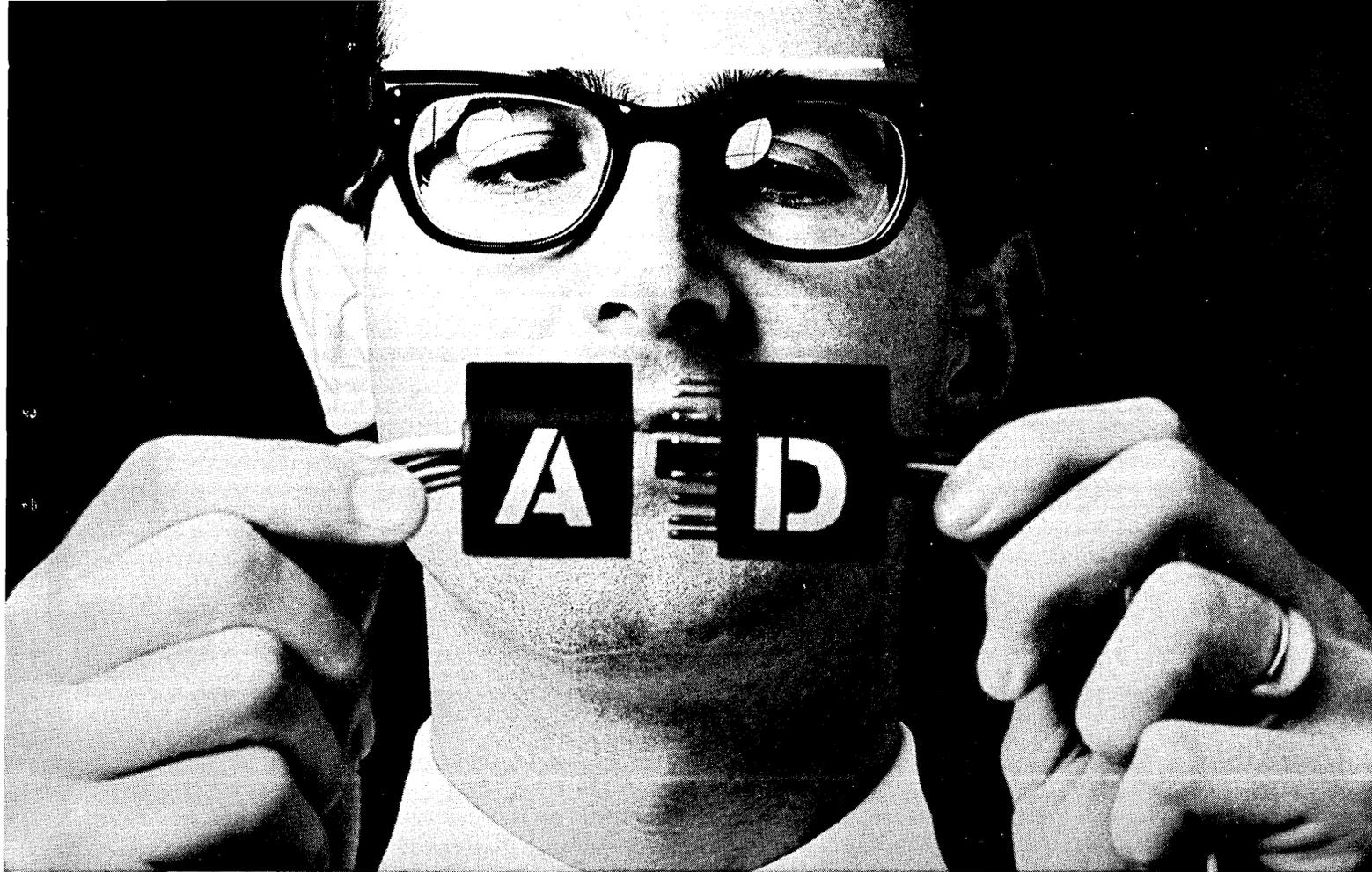
APPLICATIONS OF FUNCTIONAL OPTIMIZATION TECHNIQUES FOR THE SERIAL HYBRID COMPUTER SOLUTION OF PARTIAL DIFFERENTIAL EQUATIONS, Hiroshi H. Hara, Lockheed-California Co., Los Angeles, Cal.

HYBRID ASSUMED MODE SOLUTION OF NON-LINEAR PARTIAL DIFFERENTIAL EQUATIONS, John C. Strauss, Carnegie-Mellon University, Pittsburgh, Pa.

HYBRID COMPUTER INTEGRATION OF PARTIAL DIFFERENTIAL EQUATIONS BY USE OF AN ASSUMED SUM SEPARATION OF VARIABLES, J. Robert Ashley, University of Colorado, Boulder, Colo.

A HYBRID COMPUTATIONAL METHOD FOR PARTIAL DIFFERENTIAL EQUATIONS, G. A. Coulman, Michigan State University, East Lansing, Mich.

PRELIMINARY INVESTIGATION OF A HYBRID METHOD FOR SOLVING PARTIAL DIFFERENTIAL EQUATIONS, R. M. Howe, University of Michigan. (continued on page 92)



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Tuesday Morning, Dec. 10

Session 21

The Mini-Computer

Chairman: Paul R. Low, IBM Corp., Hopewell Junction, N.Y.

THE MINI-COMPUTER: A PROGRAMMING CHALLENGE, R. Hooper of Compta, Inc., Tarzana, Cal.

THE MINI-COMPUTER: A NEW APPROACH TO COMPUTER DESIGN, G. Ottoway, IBM Corp., Triangle Park, N.C.

Session 22

Executive Systems for Hybrid Simulation

Chairman: John E. Sherman, Lockheed Missiles and Space Co., Sunnyvale, Cal.

THE LOCKHEED HYBRID SYSTEM (A GIANT STEP), C. K. Beqient, Lockheed Missiles and Space Co., Sunnyvale, Cal.

A PRIORITY INTERRUPT ORIENTED HYBRID EXECUTIVE, G. N. Soma, Astrodata/Comcor, Inc., Anaheim, Cal.

GROWING PAINS IN THE EVOLUTION OF HYBRID EXECUTIVES, Martin D. Thompson, UNIVAC, St. Paul, Minn.

THE BOEING/VERTOL HYBRID EXECUTIVE SYSTEM, Donald A. Willard, The Boeing Co., Seattle, Wash.

FAMILY I: SOFTWARE FOR NASA AMES SIMULATIONS SYSTEMS, James S. Raby, NASA Ames Research Center.

Discussants: Thomas D. Truitt, Applied Logic Corp., F. John Sansom, Control Data Corp., Robert Egelston, IBM Corp., and Max Gilliland, MacNeal-Schwender Corp.

Session 23

Systems Techniques for Interactive Graphics

Chairman: Irving R. Schwartz, Adage, Inc., Boston, Mass.

STAND-ALONE/REMOTE GRAPHIC SYSTEM, Michael D. Rapkin, IBM Corp., Kingston, N.Y.

AN INTERACTIVE GRAPHICS TERMINAL FOR GENERATION AND DISPLAY OF 2D AND 3D STRUCTURED IMAGES, Thomas G. Hagan, Adage, Inc., Boston, Mass.

A HEAD-MOUNTED THREE-DIMENSIONAL DISPLAY, Ivan E. Sutherland, University of Utah, Salt Lake City, Utah.

A CLIPPING DIVIDER, Prof. Sutherland.

A LOW COST COMPUTER GRAPHIC TERMINAL, Malcolm MacCaulay, University of New South Wales, Australia.

THE RAND VIDEO BASED GRAPHIC COMMUNICATIONS SYSTEM, T. O. Ellis, RAND Corp., Santa Monica, Cal.

Session 26

Process Control Programming Languages

Chairman: Eric A. Weiss, Sun Oil Co., Philadelphia, Pa.

Panelists: Mr. Weiss, John H. Hiestand, Profimatics, Inc., T. J. Williams, Purdue University and F. R. Rield, E. I. du Pont De Nemours and Co.

Session 27

Operating Systems (Part I)

Chairman: Jacques Bouvard, Honeywell, Inc., Wellesley Hills, Mass.

HARDWARE/SOFTWARE INTERACTION ON THE HONEYWELL 8200, T. Hatch, Honeywell EDP, Waltham, Mass.

MEASUREMENT AND ANALYSIS OF LARGE OPERATING SYSTEMS DURING SYSTEM DEVELOPMENT, D. J. Campbell, General Electric Co., Phoenix, Ariz.

THRASHING: ITS CAUSES AND PREVENTION, Peter J. Denning, Princeton University, Princeton, N.J.

Session 28

Large-Scale Integration

Chairman: James B. Angell, Stanford University.

ENGINEERING FOR SYSTEMS USING LARGE-SCALE INTEGRATION (LSI), C. F. O'Donnell, Autometrics, Inc., Anaheim, Cal.

A COMPUTER DESIGNER'S VIEW OF LARGE-SCALE INTEGRATION, Melvin E. Conway, consultant (formerly of Sperry-Rand).

EFFICIENT PARTITIONING FOR THE BATCH-FABRICATED FOURTH-GENERATION COMPUTER, N. Cserhalmi, Raytheon Co., Bedford, Mass.

A HIGH-SPEED MODULAR MULTIPLIER AND DIGITAL FILTER FOR L.S.I. DEVELOPMENT, Donald F. Calhoun, Hughes Aircraft Co., Culver City, Cal.

Tuesday Afternoon, Dec. 10

Session 30

Memory Techniques — Here Today

Chairman: Otto Gutwin, IBM Corp., Essex Junction, Vt.

ASSOCIATIVE PROCESSING FOR GENERAL-PURPOSE COMPUTERS THROUGH THE USE OF MODIFIED MEMORIES, H. Stone, Stanford Research Institute, Palo Alto, Cal.

ADDRESSING PATTERNS AND MEMORY-HANDLING ALGORITHMS, Sherry Sisson, Bell Telephone Laboratories.

DESIGN OF A 100-NANOSECOND READ CYCLE NDRO PLATED WIRE MEMORY, Takashi Ishidate, Nippon Electric Co., Ltd., Kawasaki, Japan.

HIGH SPEED, HIGH CURRENT WORD MATRIX USING CHARGE STORAGE DIODES FOR RAIL SELECTION, S. Waaben, Bell Telephone Laboratories, Murray Hill, N.J.

Session 31

Automated Maintenance and Checkout of Hybrid Simulation Facilities,

Chairman: Maughan S. Mason, IBM Corp., Palo Alto, Cal.

AUTOMATED CHECKOUT OF A LARGE HYBRID COMPUTING SYSTEM, Jesse C. Richards, Lockheed Missiles and Space Co., Sunnyvale, Cal.

HYBRID DIAGNOSTIC TECHNIQUES, Thomas K. Seehaus, The Boeing Co., Seattle, Wash.

Discussants: Gordon R. Bolton, Lockheed Electronics Co., Houston, Texas; Albert S. Jackson, Control Technology, Inc., Long Beach, Cal.; Richard V. Kelley, Electronic Associates, Inc., Mofet Field, Cal.; and A. J. Mauceri, North American Rockwell, Downey, Cal.

Session 32

Dynamic Resource Allocation

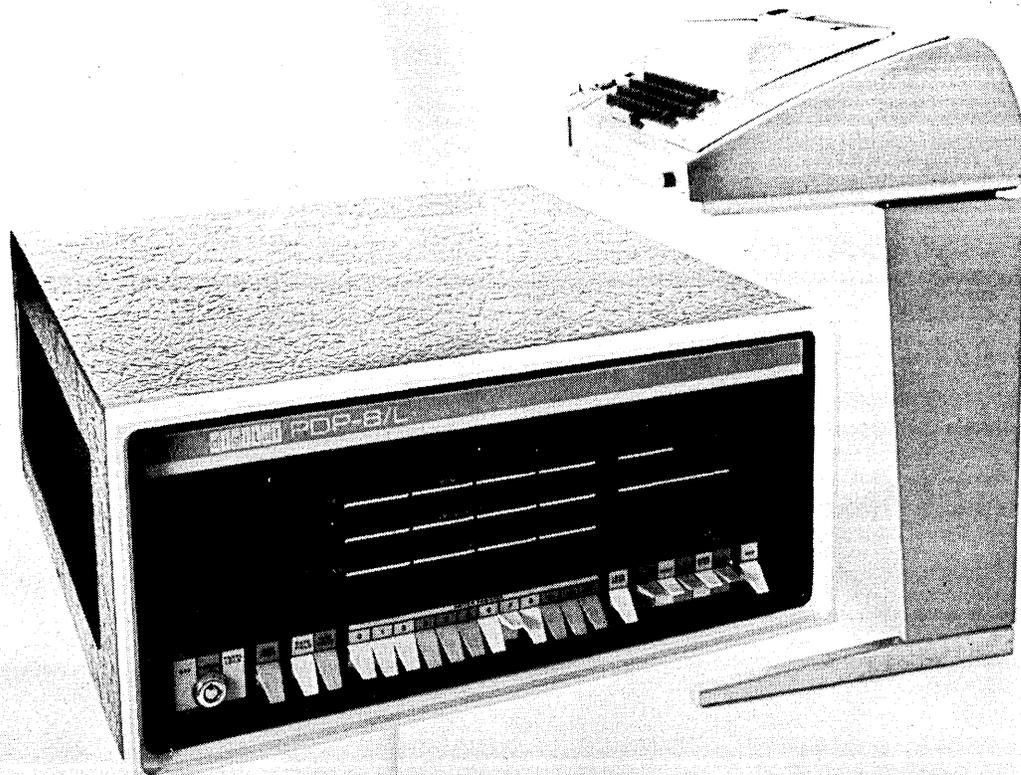
Chairman: Wayne Lichtenberger, University of California, Berkeley, Cal.

DEMAND PAGING IN PERSPECTIVE, C. J. Kuehner, IBM Corp., Yorktown Heights, N.Y.

PROGRAM BEHAVIOR IN A PAGING ENVIRONMENT, B. S. Brawn, IBM Corp., Yorktown Heights, N.Y.

JANUS: A FLEXIBLE APPROACH TO REAL-TIME TIME-SHARING, J. Kopf, Michigan State University, Ann Arbor, Mich.

A PARALLEL PROCESS DEFINITION AND CONTROL SYSTEM, Dan Cohen, Aiken Computation Laboratory, Harvard University. (continued on page 94)



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Session 35

Hand-Printed Character Recognition

Chairman: John H. Munson, Stanford Research Institute.

SOME CONCLUSIONS ON THE USE OF ADAPTIVE LINEAR DECISION FUNCTIONS, E. R. Ide, IBM Corp.

EXPERIMENTS IN THE RECOGNITION OF HAND-PRINTED TEXT: PART 1—CHARACTER RECOGNITION, Dr. Munson.

PART 2—CONTEXT ANALYSIS, Richard O. Duda of SRI, Palo Alto, Cal.

THE DESIGN OF AN OCR SYSTEM FOR READING HAND-WRITTEN NUMERALS, Patrick J. Hurley, IBM Corp, Rochester, Minn.

Session 36

Operating Systems (Part II)

Chairman: Jacques Bouvard, Honeywell, Inc., Wellesley Hills, Mass.

THE DYNAMIC BEHAVIOR OF PROGRAMS, I. F. Freibergs, McGill University, Montreal, Canada.

RESOURCE ALLOCATION WITH INTERLOCK DETECTION IN A MULTI-TASK SYSTEM, James E. Murphy, IBM Corp., Poughkeepsie, N.Y.

A DUAL PROCESSING CHECKOUT SYSTEM, Kenneth C. Smith, Martin-Marietta Corp., Denver, Colo.

AN OPERATING SYSTEM FOR A CENTRAL REAL-TIME DATA PROCESSING COMPUTER, Paul Day, Argonne National Laboratory, Argonne, Ill.

Session 37

New Memory Techniques

Chairman: Arthur V. Pohm, Iowa State University.

HOLOGRAPHIC READ-ONLY MEMORIES ACCESSED BY LIGHT-EMITTING DIODES, D. H. R. Vilkomerson, RCA David Sarnoff Research Center, Princeton, N.J.

SEMICONDUCTOR MEMORY CIRCUITS AND TECHNOLOGY, Wendell B. Sander, Fairchild Semiconductor, Palo Alto, Cal.

2½-D CORE SEARCH MEMORY, Michael W. Rolund, Bell Telephone Laboratories, Murray Hill, N.J.

DESIGN OF A SMALL MULTI-TURN MAGNETIC THIN FILM MEMORY, William D. Simpson, Texas Instruments, Dallas, Texas.

Session 38

Hybrid Simulation Techniques

Chairman: G. W. McClary, Martin-Marietta Corp., Orlando, Fla.
AN ADAPTIVE SAMPLING SYSTEM FOR HYBRID COMPUTATION, George A. Rahe, U. S. Naval Postgraduate School, Monterey, Cal.

A NEW SOLID-STATE ELECTRONIC ITERATIVE DIFFERENTIAL ANALYZER MAKING MAXIMUM USE OF INTEGRATED CIRCUITS, Brian K. Conant, Burr-Brown Research Corp., Tucson, Ariz.

A GENERAL PROGRAMMING TECHNIQUE FOR PATCHABLE SYNCHRONOUS LOGIC ELEMENTS, R. A. Moran, Applied Dynamics, Inc., Ann Arbor, Mich.

Session 40

Progress in Displays

Chairman: Jan M. Engel, IBM Systems Development Division, San Jose, Cal.

EFFECTIVE INFORMATION DISPLAYS, H. R. Luxemberg, Lux Associates.

DISPLAY TECHNOLOGY — LIGHT - VALVING TECHNIQUES, G. J. Chafaris, General Electric Co., Syracuse, N.Y.

DISPLAY TECHNOLOGY — PHOTORECORDING TECHNIQUES, David Wilcox, RADC, Griffith AFB, Rome, N.Y.

DISPLAY TECHNOLOGY — LASER DISPLAYS, Leo Beiser, CBS Laboratories, Stamford, Conn.

SYMBOLS, SENSE AND SIN, Glenn C. Kinney, The Mitre Corp., Bedford, Mass.

DISPLAY PROGRAMMING — 1968, E. M. Thomas, IBM Corp., Kingston, N.Y.

CHALLENGES PRESENTED TO THE COMPUTER FIELD BY DISPLAY TECHNOLOGY, L. C. Hobbs, Hobbs Associates.

Wednesday Morning, Dec. 11

Session 43

Bulk Memory Devices

Chairman: William A. Gross, Ampex Corp., Redwood City, Cal.

NEW HORIZONS FOR MAGNETIC BULK STORAGE DEVICES, F. D. Risko, Bryant Computer Products, Walled Lake, Mich.

LASER RECORDING UNIT FOR HIGH-DENSITY PERMANENT DIGITAL DATA STORAGE, K. McFarland, Precision Instruments Co., Palo Alto, Cal.

A RANDOM ACCESS TERABIT MAGNETIC MEMORY, J. Lucas of the Dept. of Defense, Washington, D.C.

DIAGNOSTICS AND RECOVERY PROGRAMS FOR THE IBM 1360 PHOTO-DIGITAL STORAGE SYSTEM, D. P. Gustlin, IBM Corp., San Jose, Cal.

Session 44

Simulation in the Design and Evaluation of Digital Computer Systems

Chairman: Robert J. Creasy, IBM Corp., Palo Alto, Cal.

SIMULATION DESIGN OF A MULTIPROCESSING SYSTEM, Reino A. Merikallio, IBM Corp., Gaithersburg, Md.

A SIMULATION STUDY OF RESOURCE MANAGEMENT IN A TIME-SHARING SYSTEM, Sandra L. Rehmann, IBM Corp., Gaithersburg, Md.

PERFORMANCE OF A SIMULATED MULTIPROGRAMMING SYSTEM, Meir M. Lehmann, IBM Corp.

Session 45

The Computer Field: What Was Promised, What We Have, What We Need (Hardware Session)

Chairman: Louis Fein, Palo Alto, Cal.

HARDWARE DESIGN REFLECTING SOFTWARE REQUIREMENTS, Saul Rosen, Purdue University, Lafayette, Ind.
WHAT WAS PROMISED, WHAT WE HAVE AND WHAT IS BEING PROMISED IN CHARACTER RECOGNITION, A. W. Holt, Control Data Corp., Rockville, Md.

HIGH SPEED LOGIC AND MEMORY: PAST, PRESENT AND FUTURE, Arthur W. Lo, Princeton University, Princeton, N.J.

Session 47

Panel: Computer Design Automation: What Now and What Next?

Chairman: Jerome M. Kurtzberg, IBM Corp., Yorktown Heights, N.Y.

FUNCTIONAL DESIGN AND EVALUATION, D. R. Gorman, RCA, Cherry Hill, N.J.

INTERFACE BETWEEN LOGIC AND HARDWARE, R. L. Russo, IBM Corp., Yorktown Heights, N.Y.

HARDWARE IMPLEMENTATION, W. E. Donath, IBM Corp., Yorktown Heights, N.Y.

HARDWARE FAULT DETECTION, M. A. Breuer, University of Southern California.



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a total service
from equations to
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*Patent Pending

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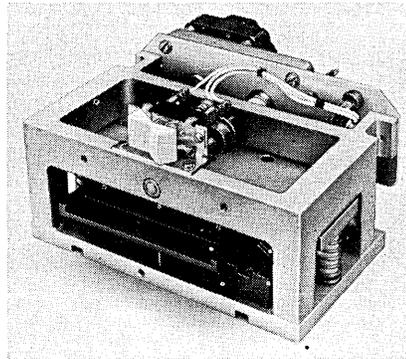
EXHIBIT HOURS

BROOKS HALL — CIVIC CENTER

MON., DEC. 9 — 10 a.m.-6 p.m.

TUES., DEC. 10 — 10 a.m.-9 p.m.

WED., DEC. 11 — 10 a.m.-5 p.m.



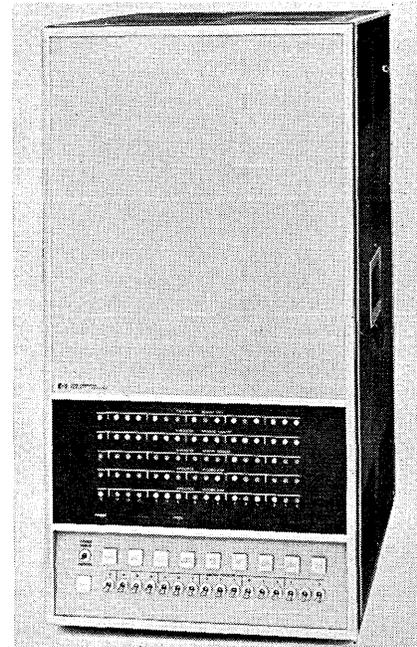
264-BIT CARD READER

For commercial applications requiring up to 264 input data bits, the Model 2900A card reader senses the first 22 columns of a standard 80 column tabulating card. This compact ($6\frac{5}{8}'' \times 6\frac{3}{4}'' \times 3\frac{5}{8}''$) motor-operated reader can be panel-mounted in any plane or used in an optional enclosure for desk top mounting.

A front-panel switch applies power to the motor operating circuit which actuates the 264 normally open sensing contacts. Total opening and closing times average one second. Safety interlocks prevent operation unless the card is properly oriented and inserted. A manually operated version is also available.

The gold-to-gold contacts exhibit less than 50 m Ω resistance and feature a double-wiping action. The contact rating is 250 mA with a dc resistive load. Pin-to-pin capacitance is less than 5 pF and the insulation resistance is greater than 10,000 M Ω . AMP Inc., Harrisburg, Pa. Booth Nos. J4-J5.

Circle No. 231 on Inquiry Card



EXPANDED GP COMPUTER

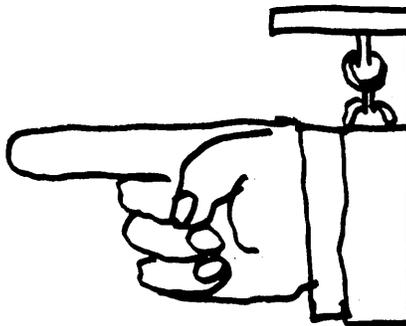
Model 2116B is a 16K, 16-bit word, general-purpose computer which has a cycle time of 1.6 μ s and an add time of 3.2 μ s. Flexibility is provided by 16 pre-wired card slots for interface hardware which permits computer upgrading at any time by insertion of appropriate circuit cards. Interface cards and software exist for CPU options such as direct memory access, hardware multiply-divide, parity check and memory protect. A multi-level priority interrupt system is built-in for the 16 slots. The 2116B has two addressable accumulators, 70 basic instructions, including 39 micro-programmable register reference instructions which can be used to form 1000 different one-word instruction combinations, and 23 assembly-directing pseudo instructions.

It uses an assembler, Fortran and ALGOL compilers, and conversational BASIC.

In its basic configurations, the computer has an 8192-word memory and sells for \$24,000. With a 16K memory it costs \$34,000. Memory may be expanded to 32K with an optional extender. Delivery time is currently 14 weeks. Hewlett Packard Co., Palo Alto, Calif. Booth Nos. 1001-1003, 1010-1012.

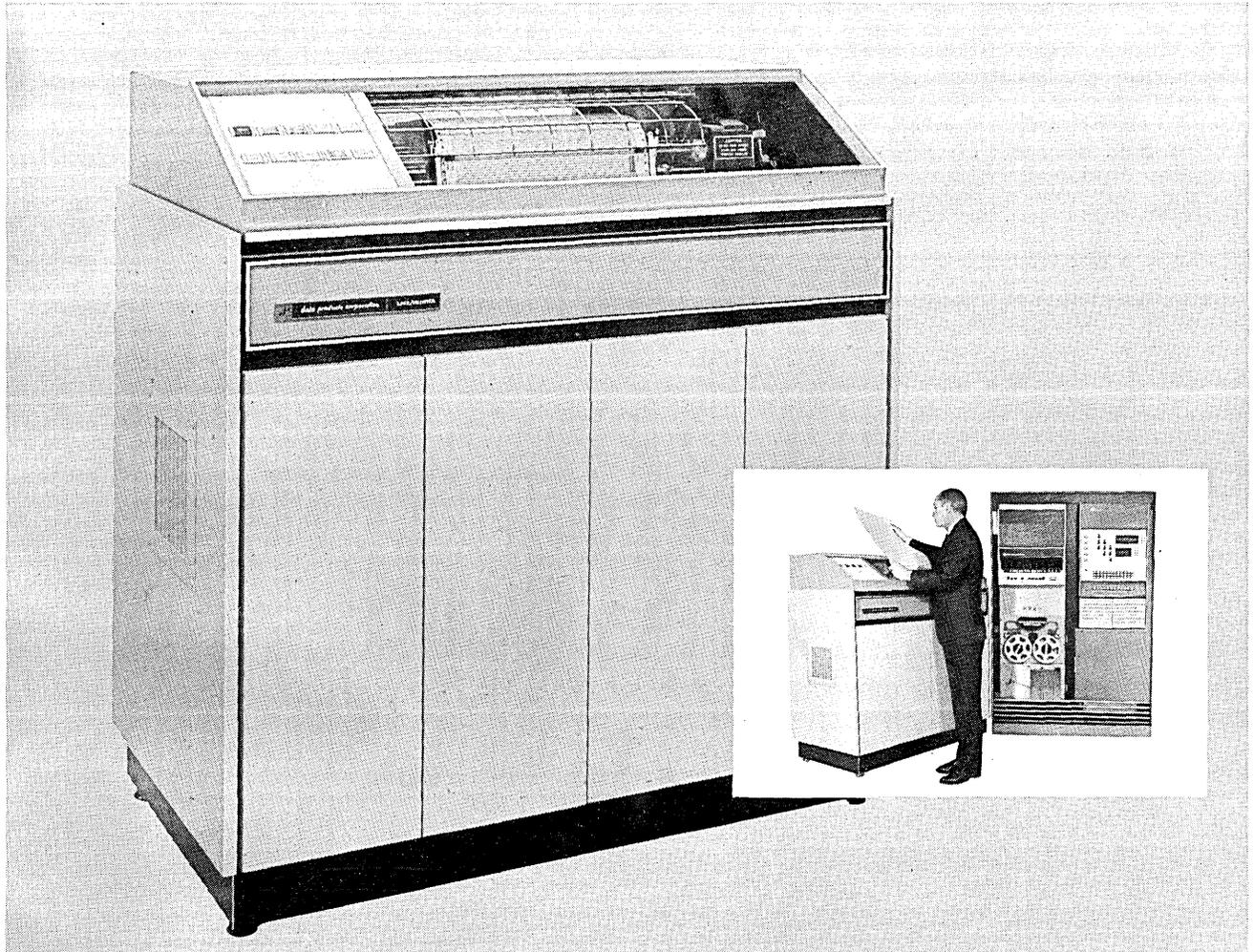
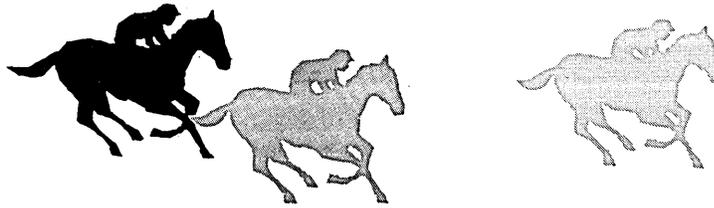
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Back up for
MAC.



Pages 66 and 67

American Totalisator goes to the races ...and the LINE/PRINTER* goes with them!



■ American Totalisator's computerized Multi-Tote System, incorporating the Data Products LINE/PRINTER, was designed expressly for race track use, to provide fast and accurate recording of all ticket sales...with no margin for error. Within seconds after the close of ticket selling, the information is processed and the LINE/PRINTER prints out a complete record of the dollar value and number of tickets sold in each pool, and an audited report on the price calculations. It has to be fast...and it has to be *right*. To make it tougher, Multi-Tote Systems are often transported from one race track to another, and must be operating quickly, without time-consuming set-up and adjustments.

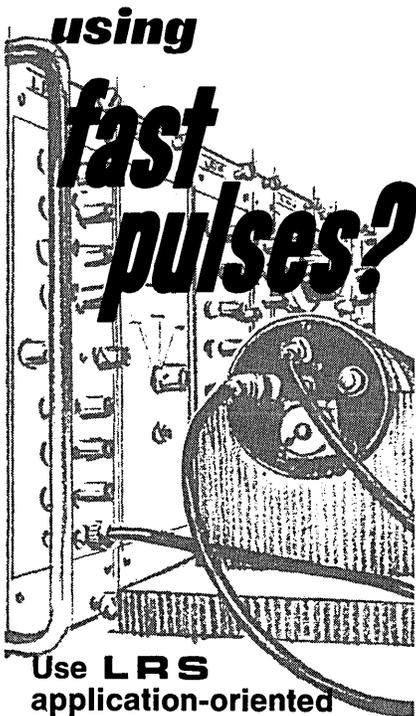
That's why American Totalisator chose the Model 4500 LINE/PRINTER. With a double-numeric drum, it prints at 1200 lines-per-minute with unparalleled reliability. The one-piece hammer, a Data Products exclusive, is virtually friction-free, and requires no periodic adjustments to keep producing sharp, non-smear, multi-copy printout. Maintenance and down-time are minimal.

More and more LINE/PRINTERS are becoming a part of more and more computer systems...and you don't need a racing form to know why. Write Data Products, 8535 Warner Drive, Culver City, Calif. 90230, for our latest LINE/PRINTER literature.

Data Products manufactures LINE/PRINTER™, DISCFILE®, Core Memories, Off-Line Printer Systems, Card Readers & Punches
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* **PHOTON COUNTING** — High-speed data acquisition systems count single or multiple photo events to 100 MHz with direct digital readout onto typewriter, line printer, or on-line computer.

Ask for **DATA FILE PC-9B**.

* **TIME INTERVAL MEASUREMENT** — Timing systems accurately measure time intervals from 50 picoseconds to 50 milliseconds. Analog or digital readout. Input sources typically photomultipliers, solid state detectors, phototransistors, or photodiodes.

Ask for **DATA FILE TM-3**.

* **DIGITAL ANALYSIS OF PEAK SIGNAL AMPLITUDE** — Analog-to-digital converter systems will digitize the amplitude of nanosecond (and longer) waveforms with 0.4% resolution. 6.4 μ s analysis time compatible with standard digital input recording devices. Ask for **DATA FILE 243**.

* **NANOSECOND PULSE INTEGRATION** — Linear and logarithmic ADC's integrate the total charge of negative or positive pulses of 4 to 50 nanoseconds duration. Built-in linear gates and stretchers. No preshaping of input pulse is required. Dynamic ranges from 10^1 to 10^4 .

Ask for **DATA FILE 243**.

* **TRANSIENT WAVEFORM ANALYSIS** — Fast waveform digitizing system will record nanosecond samples of transient signal onto magnetic tape, typewriter, or on-line computer. Full event discrimination on basis of time correlation or amplitude.

Ask for **DATA FILE WDS-1**.

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Ask for **DATA FILE T-208**.

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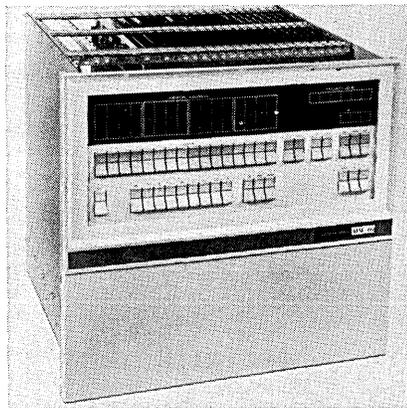
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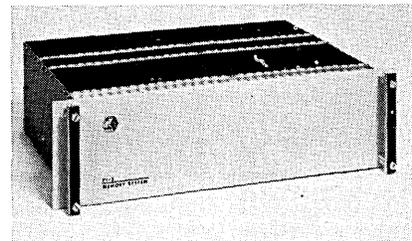
MAC

The first of a new family of computers, MAC 16 is a 16 bit parallel word multi-application computer featuring a 2 μ s add time and a 4096 word core memory, expandable to 65K words. The basic system includes a programmed data channel servicing up to 255 devices with four true nested priority interrupt levels. This priority system automatically stores the machine state upon interrupt and can be expanded to a total of 64 levels. The standard MAC 16 repertoire includes 86 instructions with multiply and divide available as options.

Standard software available includes the LEAP symbolic assembler, program loader, debug and editor programs, math library, I/O driver and hardware diagnostics. LEAP is an advanced assembler with MACRO capabilities. The program loader features relocation, linking and automatic depaging. An ASA standard FORTRAN IV compiler will be available for an 8K word MAC 16 using paper tape or card peripherals. Also provided, are the LEAP assembler and MAC 16 simulator program coded in FORTRAN IV. These programs, LEAP-FORT and MACSIM, will operate on large scale systems such as IBM 360 and 7094. User software development may thus be accelerated and accomplished independent of object machine availability.

The basic rack mounted MAC including 4K words of core memory, power supply, operator control panel and ASR 33 Teletyper is priced at \$11,950 in single unit quantities. The unit with 8K of memory is priced at \$15,900. Lockheed Electronics Company, Data Products Division, Los Angeles, Calif. Booth Nos. 401-404.

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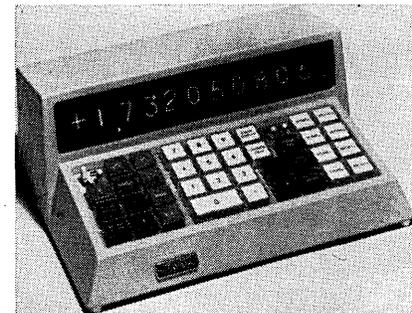


3- μ SEC MEMORY SYSTEMS

The F1-3 types of coincident-current ferrite core memories offer storage capacities from 8K x 6 bits to 8K x 18 bits and feature a 3- μ sec full cycle time (2- μ sec half-cycle time). Access time is 1 μ s maximum. The F1-3 system utilizes integrated DTL circuits and silicon semiconductors mounted on PC cards and are available with address register, sequential counter and memory retention.

Construction of the F1-3 is 3D organization, 4-wire, using 30 mil low temperature coefficient cores. The 8K types of F1-3 memory systems start at \$3,580.00. Ferroxcube Corp., Systems Div., Englewood, Calif. Booth Nos. 1506-1508.

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KEYBOARD CALCULATOR

Model 360SE electronic time-sharing calculator provides four extra random-access storage registers for constants, intermediate answers, or multiple results. It allows the statistician to develop all terms required for calculation of variance and other functions without re-entry of data. Single key-strokes instantly produce square, square root, logarithms (to any base) and exponential operations. Other features include: large, easily read, glare free display; automatic, floating decimal point; and dual, random-recall adders to store intermediate totals and automatically accumulate sums of multipliers and/or entries and sums of products and quotients. Price of the Model 360SE is \$3990; each keyboard costs \$500. Wang Laboratories, Inc., Tewksbury, Mass. Booth Nos. 417-418.

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**Heard the one about
a \$100-\$200 solid state keyboard
promised by a major supplier
for 1970 marketing?**

**It's a good, reliable company and
we have no doubt they'll make it ok.**

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In keyboards, everyone knows the way to go is solid state. And a lot of people are trying. But IKOR has it. Now. And you can get it. Now.

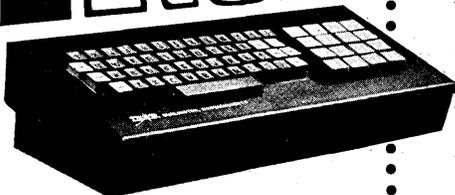
Here's a keyboard with great application versatility available in a wide range of configurations. It interfaces with virtually any data handling device.

Being solid state, its reliability is inherent. The keys are electronically interlocked to prevent errors caused by striking more than one key at a time. Each key generates its own code so it's easy to get exactly the keyboard arrangement you want without wiring changes. Diode matrices, mechanical switching or photo-electric devices are eliminated.

The IKOR board provides serial or parallel inputs to any information system by generating any required code including ASCII, EBCDIC, BAUDOT, Teletype, etc.

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E F C fiberoptics for computer applications

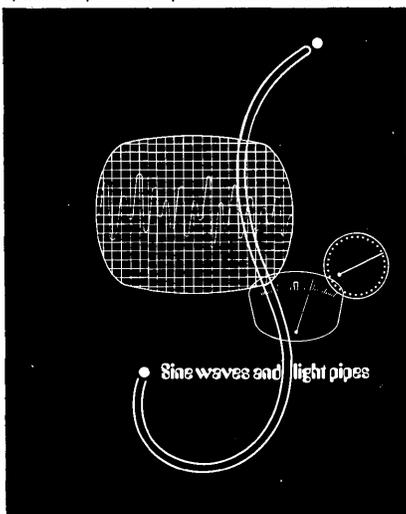
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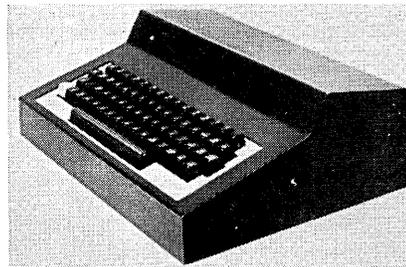
FJCC PRODUCTS



MINI-DRUM MEMORY

The Model 588 low-cost, high performance mini-drum memory system is designed for use in data terminal and test equipment applications. The system has a memory capacity of over 100,000 bits with an average access time of 8.5 ms. Featuring flying heads, nickel cobalt plating and synchronous drive, the drum memory system is priced from \$800 with 45 day delivery. Optional write/read electronics are available. California Peripherals, Northridge, Calif. Booth No. 503.

Circle No. 200 on Inquiry Card



PHOTOELECTRIC KEYBOARD

A data entry device, the Series PK-200 Photoelectric Keyboard, converts key operations into digitally-coded electrical signals, using reliable photoelectric encoding. Keyboard layouts can contain from 10 to 75 keys; the output digital code can be any selected code containing up to 14 bits. Options include: amplifiers which provide transistor or I/C logic level outputs, function key locks, mechanical storage latch, and remote keyboard lock.

The keyboard is 5" high by 11 $\frac{7}{16}$ " deep. Its width and weight depend on the number of keys contained on the unit. Typically, the width of a 48-key unit is 12 $\frac{3}{8}$ ", and the weight is 15 pounds. Digitronics Corp., Albertson, N.Y. Booth Nos. 1602-1603.

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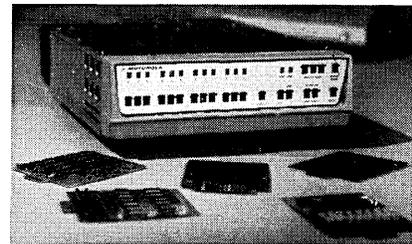
ON-LINE SYSTEM

The cable-connected off-line 7500 system may consist of a magnetic tape handler controller, a card punch, a punched card reader, a line printer, a paper tape punch and a punched paper tape reader. The system allows one device for data input, and one or two for data output. The magnetic tape unit can function as one of the output devices when not used for input purposes.

The card punch operates at a speed of 200 cards per minute and provides echo check for accuracy and offset stacking of cards containing recognized error codes.

The punched card reader operates at 230 cards per minute. With an optional 150 frame per second paper tape punch, 5-, 6- or 8-channel paper tape can be punched (one specified code). Mohawk Data Sciences Corp., Herkimer, N.Y. Booth Nos. 1201-1204.

Circle No. 240 on Inquiry Card



SMALL-SCALE DIGITAL COMPUTER

The MDP-1000 is a logic oriented small-scale, general purpose digital computer designed for use in the communications control field as a message concentrator, a relay center controller, or as a multiplexer for systems having multiple MDR-1000 document reader installations. Capacity of the magnetic core memory is 4,098, 8-bit words expandable to 16,000 words in 4,098 word increments. The random access, single address memory has a 2.16 μ s cycle time and will accept over 400 commands of various types. Address can be direct or indirect, indexed or not indexed.

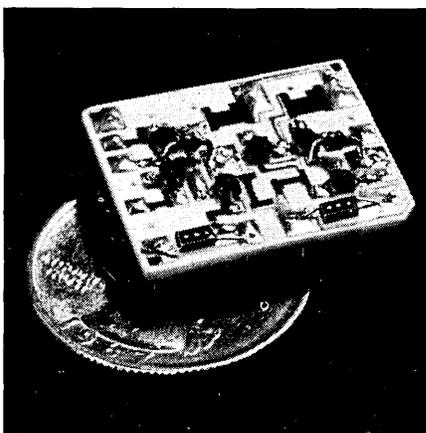
Monolithic integrated circuits contribute to packaging the data processor, power supply, and teletype interface in a 5 x 17 x 21 inch housing. The basic MDP-1000 weighs under 30 pounds and has a power dissipation of 60 watts at 115 volts input. The unit is desk- or rack-mountable and sells for \$8400. Motorola Instrumentation and Control Inc., Phoenix, Arizona. Booth Nos. 1409-1410.

Circle No. 225 on Inquiry Card.

Bypass your problems

or...how Components, Inc. can help clean up digital pulses in a small way

The problem of unpremeditated switching noise is apt to crop up in even the best of IC and hybrid logic arrays, once they are plugged into the system. When it does, the designer has the option of redesigning the circuitry or simply filtering out the spurious noise at appropriate stages. The second approach, although less heroic, is often more practicable if filter components can be found which are sufficiently economical of both space and cost.

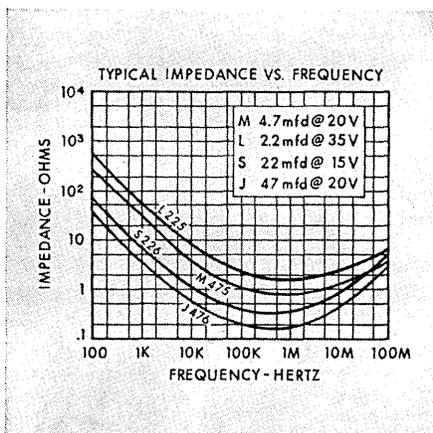


to 125°C, they are available in values from .001 to 220 mfd., with axial or radial leads.

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C.I.'s Non-Polar Minitan capacitors are available for use where ac or occasional voltage reversals are present. Unlike other non-polar solid-tantalums, these little capacitors were designed as non-polars from the ground up. Result: 1) they are available in standard, rather than off-beat capacitance ratings; 2) they are 1/2 to 1/4 the size of other units; 3) they are extremely reliable, even with frequent voltage reversals.

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(others available from .001 MFD @ 50 VDC)

(ACTUAL SIZE)

MINITAN NON-POLAR

(Also available with axial leads)

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NM	
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NS	

.10 MFD @ 35 VNP to 33 MFD @ 4 VNP
(others available from .001 MFD @ 50 VNP)

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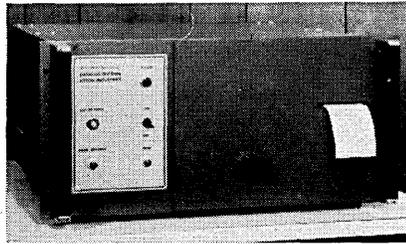
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550 FULTON STREET, TROY, N. Y. 12181

CIRCLE NO. 50 ON INQUIRY CARD

FJCC PRODUCTS



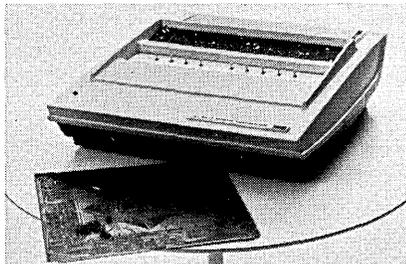
HIGH SPEED DIGITAL PRINTER

Series MC 2400 mechanical printers operate at speeds up to 20 lines per second (Model 2402), 30 lines per second (Model 2408) and 40 lines per second (Model 2404), respectively.

The printer accepts four line coded data input; entry is bit parallel and column parallel. A 8-4-2-1 BCD code is standard; zero suppression is available for any number of columns.

Truly asynchronous printing can begin at any character position on the print drum, thus avoiding the delay of holding data on line until a synchronizing point, located between each character set, is reached. Litton Industries, Litton Datalog Div., San Francisco, Calif. Booth Nos. 2006-2008.

Circle No. 218 on Inquiry Card.



SMALL-SCALE COMPUTER

The NOVA, a small-scale general-purpose computer, features four accumulators, two of which may be used as index registers. These accumulators perform arithmetic and logical operations within the arithmetic unit of the computer without accessing memory. Memory is available in 4096 16-bit word modules up to 32,768 words, as random access core or a unique form of read-only memory which is fully compatible with core memory.

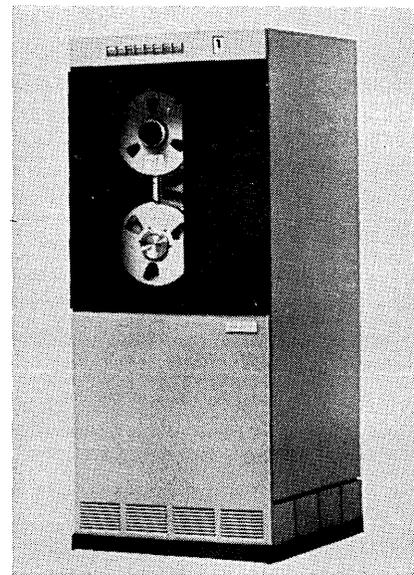
The NOVA is contained in a 5 1/4" tall package which may be mounted in a standard 19" rack. The central processor is contained on two 15" x 15" boards; a 4096 16-bit word memory is contained on one 15" x 15" circuit. Data General Corp., Hudson, Mass. Booth No. 105.

Circle No. 233 on Inquiry Card.

HIGH-SPEED PLOTTER MODULE

A special J1130 plug-in module and cable now permits the IBM 1130 computer to drive CalComp's high-speed 718 flatbed plotter and other 600 and 700 series plotters). The interface module, installed "in the field," is available with IBM-compatible software. The Model 718 Flatbed plotter, measuring 54" x 72", has a maximum operating speed of 900 increments-per-second in the incremental mode and 1687 increments-per-second in ZIP MODE. Prices: Modey 718 flatbed — \$50,000; J1130 module — \$850.00. California Computer Products, Inc., Anaheim, Calif. Booth Nos. 1101-1103, 1110-1112.

Circle No. 208 on Inquiry Card



MAG TAPE SYSTEM AND PAPER TAPE PUNCH

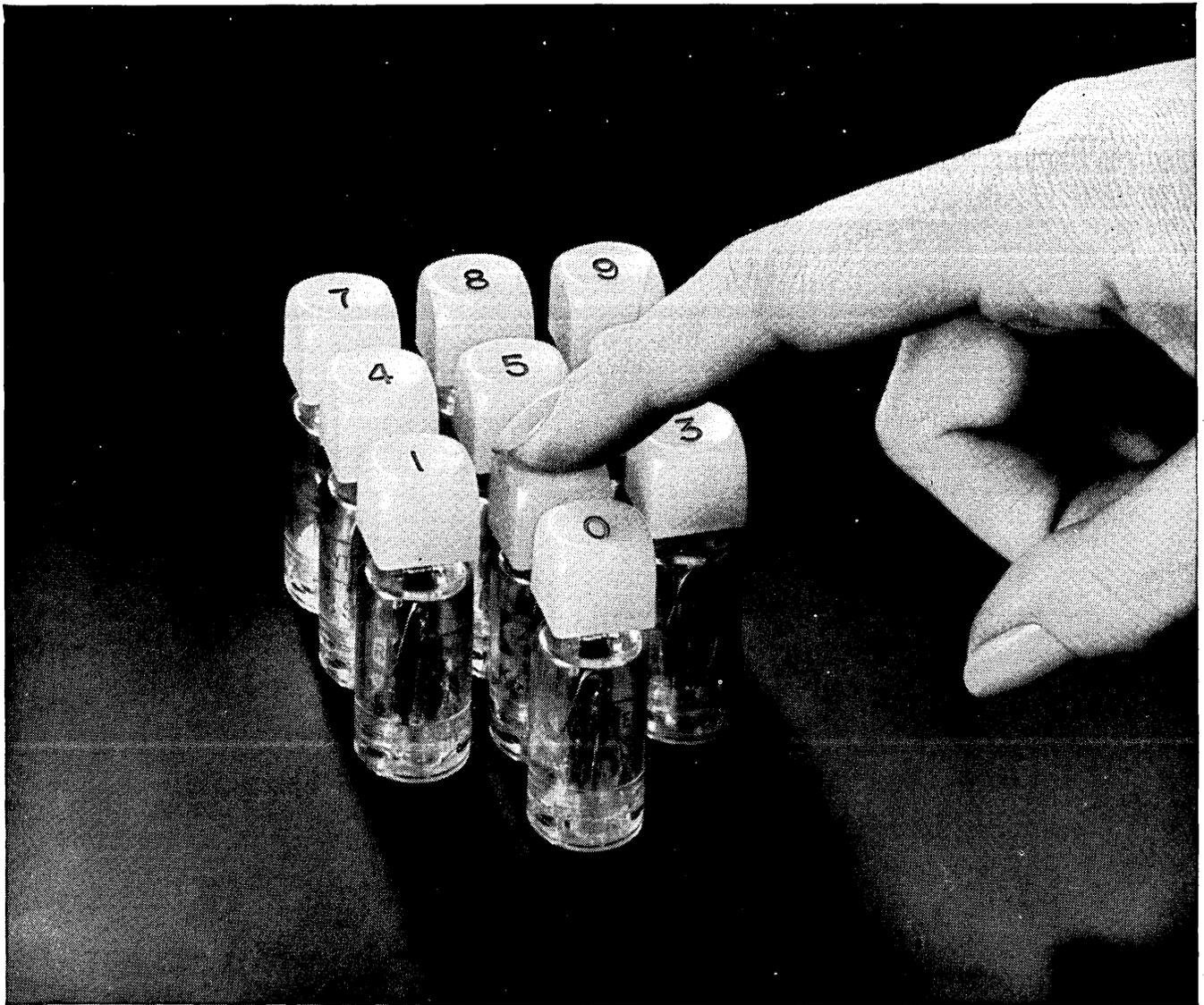
The MTC-114/MTH-117 magnetic tape subsystem handles 7-track tapes with densities of either 200 or 556 bits per inch. Transfer rates are 7.5 and 21KHz, depending on tape density. One subsystem can include up to six tape handlers.

Monthly rental for a 3-tape subsystem is in the \$1,000 range with delivery on a three month schedule.

The PTP-110 paper tape punch uses 8-inch, 1,000-foot reels having a capacity of up to 120,000 characters at 10 characters per inch. Data medium is standard 1-inch, 7 or 8-channel tape or Telex 11/16 inch, 5-channel tape. Software is available.

Delivery of the paper tape punch is six months, with a monthly rental in the \$100 range. General Electric Co., Bridgeport, Conn. Booth P.

Circle No. 210 on Inquiry Card.



These new keyboard switches feature unusually precise action and low-cost mounting. See for yourself—write for samples.

These elegantly styled key switches—designed for handling switching at logic levels—are especially suitable for computers, learning and business machines, and advanced control equipment.

Designed by Raytheon, they have a featherlight touch that is precise and reliable. Just a 3-oz. touch activates the switch. Because of the unique design, this action can be repeated more than 10 million times. Yet the switches cost less than \$1 in production quantities.

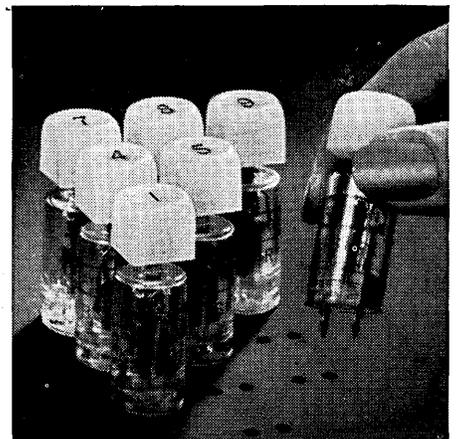
A wide range of standard- and custom-cap shapes, sizes, colors, and alphanumeric characters are available. Char-

acters can be hot stamped, engraved or molded through. Bases can be flat or with 10° slope. Characters can be illuminated by backlighting. All switches are made of high-quality materials: stain-resistant caps; polycarbonate body parts; stainless steel springs; beryllium and stainless steel contacts. They are available in single- and double-level wipe-action types, and in dry-reed, hermetically sealed single- and double-level types.

For free samples, write on your letterhead describing your application to: *Raytheon Company, Industrial Components Operation, Dept. 2351-CD, Quincy, Massachusetts 02169.*



CIRCLE NO. 51 ON INQUIRY CARD



Simple, low-cost mounting. Raytheon switches plug into .125" PC board. Contact pins snap in, firmly lock switch in place for soldering. This permits you to use flow soldering techniques—cut keyboard assembly time and costs.

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That COMPAT can supply large quantities of equipment in relatively short time.

For example; the COMPAT photo typesetting computer was developed in 30 days and in production in 120 days.

Other complete system digital controls have been developed by COMPAT for:

Data communication, Steel mill control system, Stage lighting, Optical page readers, Supervisory control, etc.

"THROW AWAY THE CARDS"! Get the detailed information on COMPAT "HIDICS". Call or write to:

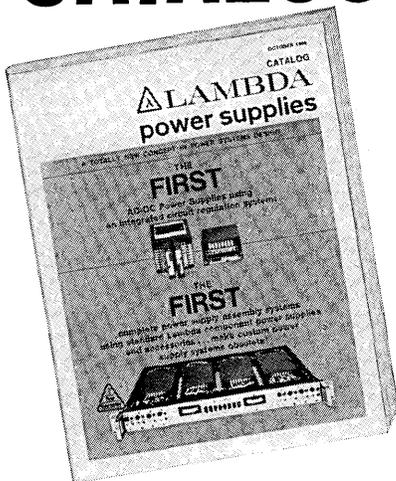
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CIRCLE NO. 54 ON INQUIRY CARD

FJCC PRODUCTS

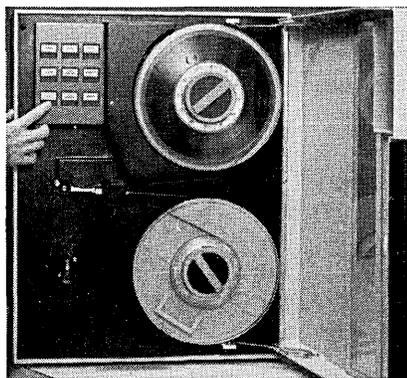
MULTIPLEXER TERMINALS

The TDX is a time division multiplexer which permits the simultaneous transmission of up to 24 independent data channels over a single voice grade telephone channel.

In a typical time sharing application the TDX allows a number of subscribers located in one city access to a central processing unit located in a distant city without the expense of a toll charge each time access is required. The local and remote cities are linked through one full time leased line.

The terminals are available in 8, 12, 16 and 24 channel versions and will interface with input units operating at 110, 134.5 and 150 baud. A built in data set is included for interfacing with the high speed leased line. Rixon Electronics, Inc., Silver Spring, Md. Booth No. 2004.

Circle No. 211 on Inquiry Card

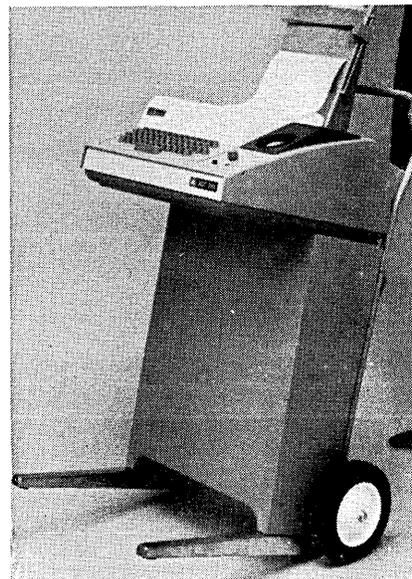


TAPE MEMORY SYSTEM

The TM-Z tape memory operates in both seven and nine track modes and offers tape speeds up to 24 inches per second and packing densities up to 800 bits per inch. Modular design and use of an electronically servo-controlled single capstan tape drive are other features of the system.

Both the transport unit and memory electronics are contained in a single 100-pound package, requiring only 475 square inches of rack space. The TM-Z is comprised of three mechanical and three electronic modules which facilitates repair and decreases down time. The capstan head assembly is pre-aligned and requires no special alignment procedure. Ampex Corp., Redwood City, Calif. Booth Nos. C1-C2, C9-C10.

Circle No. 237 on Inquiry Card.



ACOUSTIC DATA TERMINAL

The Model ADT 233 mobile acoustic data terminal is specially designed for computer time-sharing users. It provides unusually high sensitivity to weak data signals in the presence of noise either on the telephone line or in the room.

The coupler and a Model 33 Teletype have been packaged together to provide a truly self-contained terminal. All the user has to do is dial up a time-sharing computer and place his telephone handset into the acoustic receptacle in the terminal. He can then carry on a two-way data conversation with the computer.

The mobile terminal is compatible and can be used with an ADC 300 at the other end of the telephone line or a Bell 103A2 or 101C Dataphone. It is available either with or without a paper tape punch and reader. Anderson Jacobson, Inc., Mountain View, Calif. Booth No. 501.

Circle No. 216 on Inquiry Card

HIGH SPEED MEMORIES

The 370-core memory offers high speed, with modularly expandable storage capacity. Basic modular size is 4K by 40 bits, with building block capacities of up to 655,360 bits. Full-cycle memory speeds are from 1.5 μ s to 750 ns. The 420 core memory can be used as a full or half-cycle data manipulating system with 4.0 μ s full-cycle speed and an access time of 600 ns. It has a storage capacity of 1,024 words by 8 bits. The compact unit measures 3.35 x 4 x 7.4" and weighs 6 pounds. No special fans or cooling are required. Fabri-tek Inc., Minneapolis, Minn. Booth Nos. 1301-1302, 1309-1310.

Circle No. 220 on Inquiry Card.



MDS/OEM-I/O-FJCC

You guessed it! MDS/OEM Marketing will display Input/Output equipment at the Fall Joint Computer Conference

On your list of things to see at the Fall Joint Computer Conference, jot down "MDS/OEM Marketing Exhibit, don't miss."

We'll have a variety of units representative of the high-performance Input and Output equipment engineered by MDS especially for the original equipment manufacturer.

Included will be Buffered Tape Units; High-Speed and Low-Speed Line Printers; Digital Strip Printers; Card Punches and Readers; Paper Tape Punches and Readers; System 2100 for Low-Cost Control of Piecework and Production Records.

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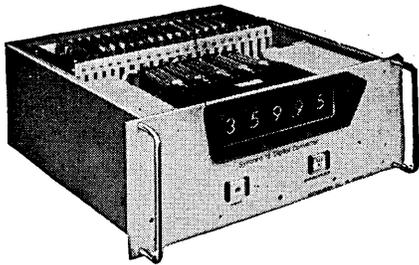
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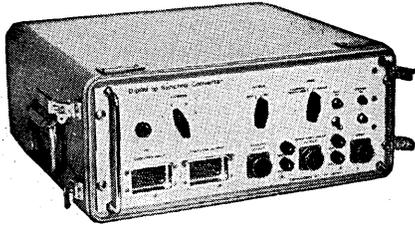
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Advanced Instrumentation



Synchro-to-Digital Converters

A simple, reliable, accurate method of high resolution conversion with resolution and accuracy to 18 bits. Available with straight binary code or BCD code outputs. Ideally suited for use as an interface between analog pickoffs and digital computers or off-line equipment.

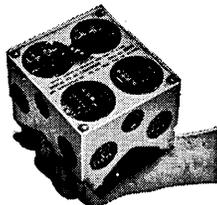


Digital-to-Synchro Converters Digital-to-AC Analog Converters

ASI Converters accept and register digital angles in binary or BCD code and convert these inputs to the equivalent synchro or resolver voltages. Digital-to-Analog AC models convert digital input information to linear AC output signals.

Single-speed resolution and accuracies are available up to 18 bits.

Miniature Solid-State Airborne Units



All solid-state converters featuring high density packaging and ultra-reliability. Available as:

Digital-to-Synchro Converters; Synchro-to-Digital Converters; Digital-to-AC Analog Converters; AC Analog-to-Digital Converters.

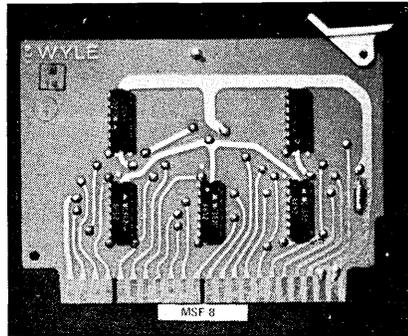
Astrosystems Inc.

Advanced Instrumentation

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New York 11040 • (516) 328-1600

CIRCLE NO. 56 ON INQUIRY CARD

FJCC PRODUCTS



LOGIC CARDS

The need for external gating to allow multi-source flip-flop reset is eliminated by the MSF-8 logic card. To meet common system requirements for reset of storage flip-flops from more than one source, the card eliminates the NAND gate usually required by providing eight RS flip-flops, each with a dual reset input.

Frequency of the unit, is dc to 5 MHz; input loading, one unit load each input; and noise rejection, 750 millivolts typical at logic 0, 1 volt typical at logic 1. A typical flip-flop provided on the logic card is implemented by cross-coupling a two-input NAND gate and a three-input NAND gate. Systems Div., Wyle Laboratories, El Segundo, Calif. Booth No. 112.

Circle No. 214 on Inquiry Card

DATA TRANSACTION SYSTEM

The Modular Data Transaction System is a small, general-purpose computer that acts as a fully functional, free-standing cash register. It is designed to handle every type of point-of-sale transaction — both credit and debit — and produces hard totals, prepares audit tapes, computes change, provides cash sale receipts and processes charge sale slips in multiple copies. It can communicate with a computer — instantly or at periodic intervals — to update credit and inventory records or provide input for accounts receivable, sales audit and reporting and other purposes. Projected price is around \$3000. Singer Co., Friden Div., San Leandro, Calif. Booth Nos. 1707-1708.

Circle No. 202 on Inquiry Card.

SOURCE DATA AUTOMATION

The 100SR is used primarily for transmitting data to a computer center and receiving computer-prepared data employing ordinary telephone company direct-dial circuits.

Compatible with most standard computers, the 100SR system incorporates an IBM Selectric® typewriter used for input and print-out operations. Information, which is stored on magnetic tape, can be retrieved as hard copy print-out at nearly 175 wpm, or transmitted in a direct-dial phone call at 6,000 characters a minute. Among the significant features of the system is the optional PAD (Program And Data) memory unit which stores up to 80,000 characters of pre-verified, frequently-used information and controls formatting for input programs. The PAD Memory is capable of recording only the necessary computer-sensible codes in the magnetic tape cartridge while printing out in hard copy full details of the data input. Communitytype Corp., New York, N.Y. Booth Nos. 1901-1902.

Circle No. 241 on Inquiry Card



COUPLER

The Model 1649 coupler is designed to provide an easy interface between the Digi-Data incremental recorder and digital output devices such as counters and digital voltmeters. This coupler is designed for writing on tape compatible with the IBM 360, 2400 tape drive with 9 track, 800 BPI format. Tapes can be written in binary, EBCDIC or packed decimal. Controls within the coupler allow the user to select the word length and record length. Twelve characters of fixed data can be entered by switches on the front panel.

All of the controls for correct format of the tape for computer compatibility are provided by the combination of the coupler and recorder. Digi Data Corp., Bladensburg, Md. Booth No. 1601.

Circle No. 222 on Inquiry Card.

3 NEW SOFTWARE PACKAGES FOR SALE?

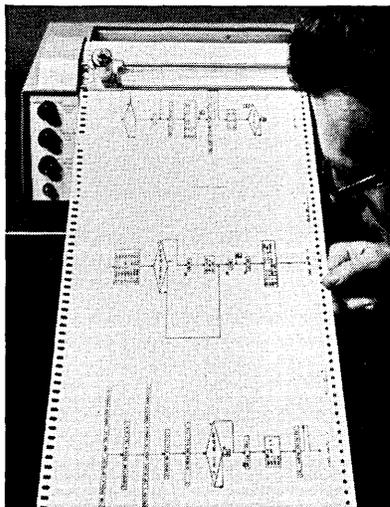


CALCOMP GPCP

(General Purpose Contouring Program)

This program automatically plots functions of two independent variables in the form of contour diagrams or maps. Written in FORTRAN IV, it is easy to use, extremely flexible, accurate, economical. It is about 30 times faster than manual and does jobs impossible to do by hand. Used with any CalComp plotter system, GPCP can be applied to such fields as geophysics, meteorology, engineering, biology and medicine.

Now available for a one-time lease charge of.....\$10,000

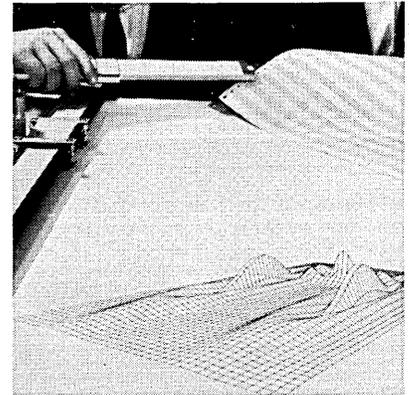


CALCOMP FLOWGEN/F

(Flowchart software package)

This program allows any computer programmer to automatically produce flowcharts of his program on any CalComp plotting system. An extremely useful tool in documentation of checked-out programs, it is even more valuable during the check-out phase of a new program or a new computer. FLOWGEN/F is fast, time-saving, accurate.

Now available for a one-time lease charge of.....\$4,500



CALCOMP THREE-D

(Perspective drawing software package)

This program is a set of FORTRAN subroutines for use with any CalComp digital plotting system to produce perspective drawings of surfaces. It can also generate stereoscopic views of surfaces, and, with CalComp Model 835 microfilm plotter, can produce animated films. Easy to use, flexible and economical, THREE-D can be applied to such fields as marketing, engineering, toolmaking and designing.

Now available for a one-time lease charge of.....\$3,000

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CIRCLE NO. 57 ON INQUIRY CARD

We've submini-priced subminiature switches

and the deal's OFF. . .

Or on. Or off-again-on-again-off-again. Or on-again-on-again-on-again. Now, you can order both subminiature push button switches and subminiature toggle switches at the miniest prices on the market. How mini? Submini! Now how many?

Submini-Price List of Pushbutton and Toggle Switches

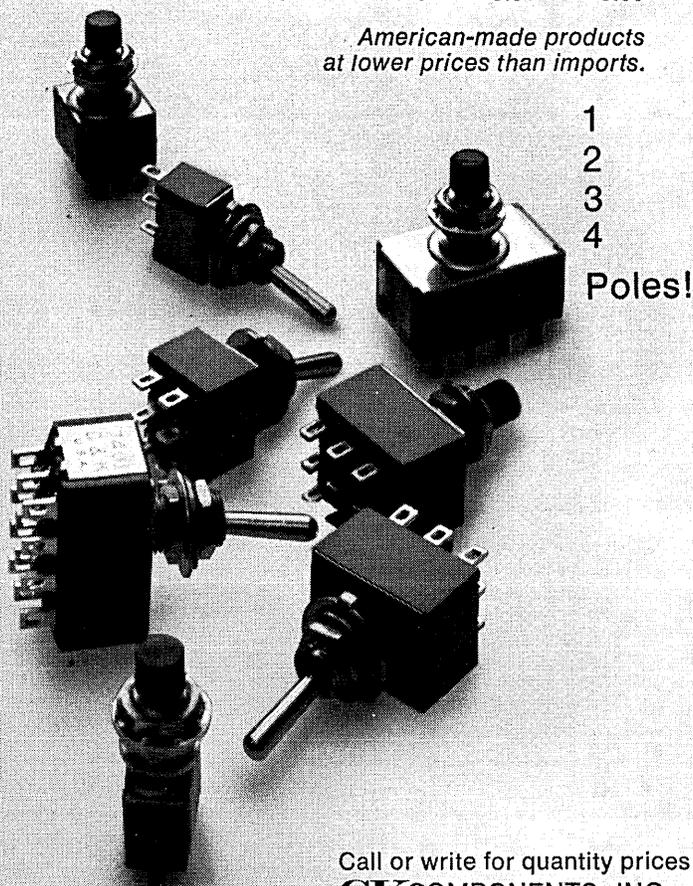
TOGGLE-SWITCH

MODELS	1-24	25-99	100-499	500-999
7101	\$ 1.65	\$ 1.10	\$.96	\$.82
7103, 5, 7, 9	1.95	1.30	1.16	.97
7201	2.15	1.43	1.28	1.07
7203, 5, 7, 9	2.55	1.70	1.52	1.27
7211	2.85	1.90	1.70	1.41
7213	3.15	2.10	1.87	1.55
7215	3.45	2.30	2.06	1.71
7301	3.85	2.57	2.30	1.92
7303, 5, 7, 9	4.80	3.20	2.87	2.38
7401	4.85	3.28	2.90	2.43
7403, 5, 7, 9	6.05	4.10	3.61	3.00
7411, 13, 15	6.90	4.30	4.11	3.41

PUSHBUTTON

SWITCH MODELS	1-24	25-99	100-499	500-999
P8121	\$ 2.55	\$ 1.70	\$ 1.52	\$ 1.27
P8221	3.45	2.30	2.06	1.71
P8321	4.80	3.20	2.87	2.38
P8421	6.05	4.10	3.61	3.00

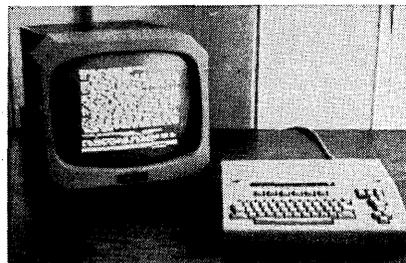
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CIRCLE NO. 58 ON INQUIRY CARD

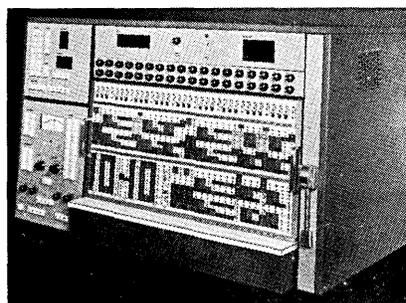
FJCC PRODUCTS



REMOTE DATA TERMINAL

A CRT terminal with a 2000 character display capacity features a 17" CRT with up to 100 characters in a line. Symbol generator is a straight line stroke. A data set interface of up to 2400 bits/sec. or a direct computer interface with up to 500 kHz bit transfer rates is provided. Split screen, pre-programmed forms, format restrictions and tabulation are additional features of the terminal. The font is 64 characters with modular expansion to 96 characters. Upper and lower case alphas are provided. Hendrix Wire & Cable, Hendrix Electronics Div., Milford, New Hampshire. Booth No. 504.

Circle No. 234 on Inquiry Card.



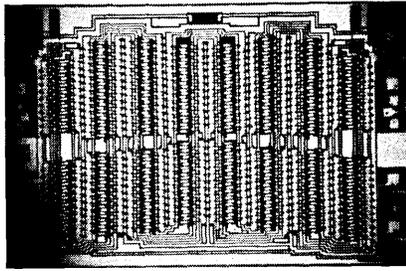
DESK TOP COMPUTER

The 380, a 10-volt desk-top computer, is an analog machine with expandable control logic for hybrid interface. It provides 10 amplifiers which can be easily expanded to 50 using prewired, plug-in techniques; amplifiers operate at full scale over entire 100 KHz bandwidth.

Logic may be added directly on the patch panel for hybrid operation. Basic configuration also provides electronic mode control, two-mode timer, over-range hold/store capabilities, and sophisticated digital function generators. Peripheral display equipment includes multi-channel recorders, X-Y recorders, and Rep-Op display scopes. Electronic Associates, Inc., West Long Branch, N.J. Booth No. N.

Circle No. 207 on Inquiry Card.

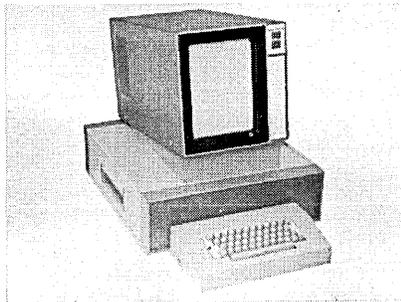
COMPUTER DESIGN/NOVEMBER 1968



STATIC SHIFT REGISTER

The 7C3003, a dual 100-bit static shift register, features a clock repetition rate ranging from dc to 1 MHz, allowing data storage for extended time periods. Unlike dynamic shift registers, this circuit has no minimum clock rate. A total of two hundred bits may be connected into two parallel 100-bit registers or the output of one register may be connected to the input of the other. Longer delays can be accomplished within a single package, thereby minimizing component count. The 7C3003 is offered in the 10-lead TO-5 type configuration at \$30.25 in 100-piece quantities. Texas Instruments, Inc., Dallas, Texas. Booth No. 704.

Circle No. 209 on Inquiry Card.



CRT DISPLAY TERMINALS

The Series 400 family of stand-alone display terminals feature a unique curve generator for graphics, which enables curves to be drawn directly rather than approximately by straight-line segments.

The Model 20 includes a storage-type CRT, an alphanumeric input keyboard, curve and vector generators for graphics, a character generator for alphanumerics, and interfacing for standard data sets (modems).

The display terminal affords significant cost advantages: reduced storage requirements for display files; reduced phone line charges; and reduced time-share rates. Since graphic images can be transmitted faster, the terminal also affords improved response times for interactive computer systems. Computek, Inc., Cambridge, Mass. Booth No. 508.

Circle No. 221 on Inquiry Card

Computer Performance; Calculator Price.



WANG 380

640 Program Steps
24 Storage Registers
 $\text{LOG}_e X$, e^x , X^2 , \sqrt{X} , $\frac{1}{X}$, +, -, X, ÷
Performs Subroutines, Loops,
Branches, Makes Decisions.

\$3795.

No special programming language needed. The Wang 380 learns programs directly from keyboard operations and stores them on plug-in magnetic tape cartridges.

You can tailor system capability to your exact needs with compatible accessories including:

Output Writer, CRT Display, additional Data Storage, Teletype, Trig Pack, and On-line Interface.

There is nothing comparable, anywhere.



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(205) 595-0694	(301) 821-8212	(317) 631-0909	(505) 255-9042	(613) 224-4554	(714) 234-5651
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(212) 682-5921	(304) 344-9431	(404) 457-6441	(513) 531-2729	(615) 588-5731	(717) 397-3212
(213) 278-3232	(305) 564-3785	(405) 842-7882	(514) 482-0737	(617) 851-7311	(805) 962-6112
(214) 361-4351	(305) 841-3691	(412) 366-1906	(518) 463-8877	(702) 322-4692	(901) 272-7488
(215) 642-4321	(312) 889-2254	(415) 454-4140	(602) 265-8747	(703) 877-5535	(916) 489-7326
					(919) 288-1695

CIRCLE NO. 59 ON INQUIRY CARD



Burton Magnekote plating eliminates Litton Systems memory drum rework costs!

When Litton's Guidance and Control Systems Division switched to Burton Magnekote's hard metallic recording surface plating techniques, their memory drum costs were dramatically cut and yield jumped to 98%!

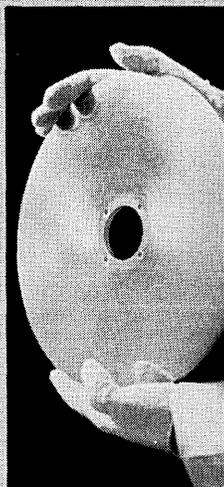
We can do the same for you,

like we've done for many other industry leaders... but here's Litton Systems' story.

Low yields on memory drums substantially exceeded programmed costs. That was in 1967 when they had real memory drum plating problems. Rework expenses tripled drum plating costs. Worst of all, system deliveries were delayed. So they came to Burton Magnekote, specialists in the plating and finishing of hard, metallic recording surfaces for computer drum memories and disc files. Before long, the yield rate of plated drums was 98%.

Magnekote techniques assure uniform magnetic characteristics, maximum bit packing density, controlled coercivity to 650 oersteds and magnetic remanence to 10,000 gauss. Whatever your recording technique, contact or flying head, or packaging requirement, from drums to 18" diameter to discs to 39" diameter, Magnekote can meet it...with the squarest B-H loop in the industry.

So if you have a problem involving plating metallic recording surfaces and want a memory you can forget, follow Litton's lead and call us now!



BURTON MAGNEKOTE
DIVISION OF BURTON SILVERPLATING CO.

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SUBSIDIARY OF ALLOYS UNLIMITED, INC.

MAGNETIC PLATING SPECIALISTS FOR COMPUTER DRUM/DISC MEMORIES

CIRCLE NO. 60 ON INQUIRY CARD

FJCC EXHIBITS

TIME SHARING SYSTEM

Capabilities for time sharing through an entire range of computers will be demonstrated at the FJCC under the general theme REALTIMESHARING. REALTIMESHARING is defined as the dynamic allocation of computer system resources in an interactive environment to meet the simultaneous and varying needs of multiple users.

The multi-language capabilities of TIME SHARE-8, a general purpose, time sharing system built around the 12-bit PDP-8/I computer, will be shown by having terminals operating in FORTRAN, single-user FOCAL®, BASIC and a machine language, either PAL or DDT.

The 18-bit PDP-9 will carry out the REALTIMESHARING theme with a demonstration of concurrent background/foreground operation under the control of a new monitor system, and the 36-bit PDP-10 will demonstrate the simultaneous operation of real-time programs, interactive computation and batch calculation. Digital Equipment Corp., Maynard, Mass. Booth Nos. 907-912.

Circle No. 238 on Inquiry Card.

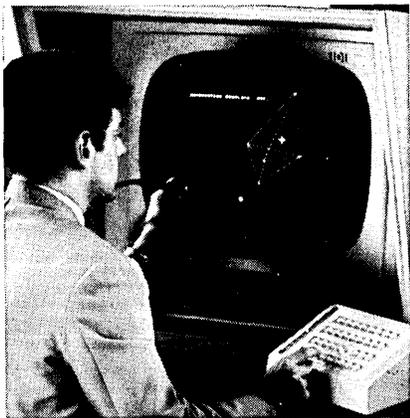
COMPUTER COMMUNICATIONS

A telephone-line link to demonstrate the batch-terminal capabilities of the 620/i and 520/i computers is planned for the FJCC.

The 620/i will serve as a central batch terminal located in a reception center at a Nob Hill hotel. Its function is to receive batches of data from remote data sources, temporarily store the information in a bulk memory device, and feed the data to a large computer in the most efficient format and order. Feeding information to the central terminal will be a 520/i computer located in a booth at the FJCC. The 520/i will act as a remote batch terminal, collecting information from, or transmitting data to such peripheral devices as card readers, line printers, teletype machines, magnetic tape, and high speed paper tape units. The computer funnels the information onto the telephone line that links the remote batch terminal with the central batch terminal.

The system is designed for standard voice-grade duplex telephone links, one per remote batch terminal. The 620/i central batch terminal can handle up to eight remote lines simultaneously. Varian Data Machines, Irvine, Calif. Booth No. G.

Circle No. 235 on Inquiry Card.



GRAPHIC DISPLAY SOFTWARE

A demonstration of several software packages facilitate use of IDIOM, an interactive graphic display system for important areas of application. Also shown will be how the display can be used for such applications as computer-aided design, management information centers and simulation.

The IDIOM display system incorporates unique design concepts which involve the extensive use of hardware display function generation and an advanced display processing unit.

Among the software packages will be an expanded version of GRAF, an electronic drawing board program which enables the user to draw and manipulate any desired figures and/or text. Possible display manipulations include: moving; scaling; copying; and rotating. Another program will be RAID. This is used with IDIOM for debugging programs graphically on the CRT and for rapidly scanning the contents of memory. Information Displays, Inc., Mt. Kisco, New York. Booth Nos. 1509-1510.

Circle No. 227 on Inquiry Card.

COMMUNICATIONS SYSTEMS

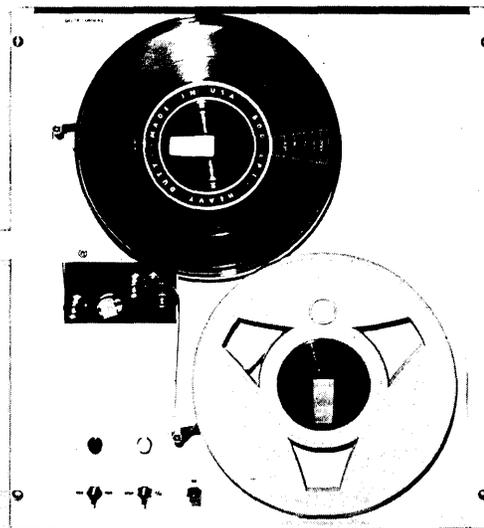
A family of communications systems has been internally configured for the job of data concentration and message processing in addition to general purpose data manipulation.

They feature communications instructions — a number of micro-coded sub-routines which perform communication functions at unusually high speeds — and are based on a 370 ns FIRMware directed processor within the system. Models differ in speed and function: one model is primarily designed for the concentration of communication lines and data sets, while a second model using a higher speed processor provides additional capability for message processing. They range in price from \$15,000 to \$50,000. INTERDATA, Oceanport, N.J. Booth Nos. 1504-1505.

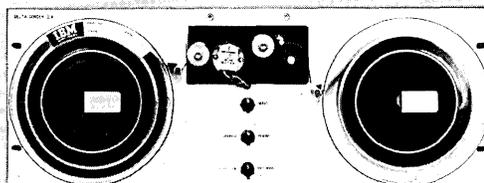
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QUALITY

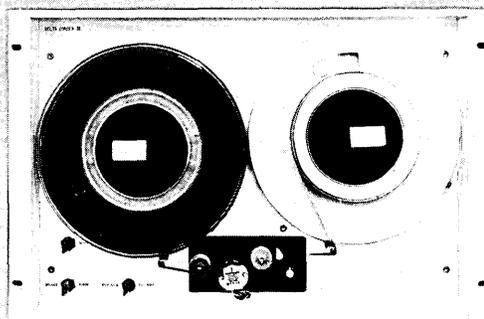
DIGITAL INSTRUMENTAL RECORDING



DELTA-CORDER II
24" Panel
10 1/2" Reel
\$2495



DELTA-CORDER IIA
7" Panel
6" Reel
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DELTA-CORDER III
12" Panel
8 1/2" Reel
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▲ COMPUTER COMPATIBLE
7 AND 9-TRACK FORMAT

▲ CHOICE OF STEPPING
SPEEDS AND DENSITIES

▲ EASE OF STRAIGHT-LINE
TAPE PATH THREADING

▲ PRECISION TAPE HANDLING
FOR NEGLIGIBLE SKEW

▲ AUTOMATIC PARITY AND
GAPPING

▲ NOISE IMMUNE COMPUTER
GRADE CIRCUITS

DELTA-CORDERS, INC.

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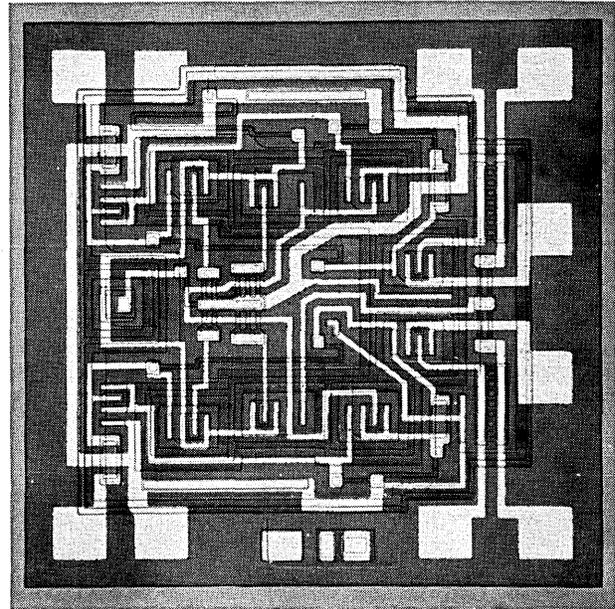
9827 NORTH 32ND STREET ▲ PHOENIX, ARIZONA 85028 ▲ (602) 948-6310

CIRCLE NO. 61 ON INQUIRY CARD

A MONOLITHIC DIFFERENTIAL VIDEO AMPLIFIER

For Memory Applications

FAIRCHILD SEMICONDUCTOR
Mountain View, Calif.



A monolithic video amplifier has been introduced by Fairchild Semiconductor to satisfy design requirements for wide bandwidth, low phase distortion, and exceptional gain stability.

The $\mu A733$ is a two-stage differential input, differential output amplifier employing shunt-series feedback. Emitter follower outputs enable the device to drive capacitive loads and all current source biased stages permit high power supply and common mode rejection. It offers fixed gains of 10, 100 or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. The amplifier also features a typical bandwidth of 120 MHz and an input resistance of 250 K Ω . Operating temperature range is -55°C to $+125^{\circ}\text{C}$. No external frequency compensation components are required. The $\mu A733$ is fabricated with a new second generation low noise, high frequency process resulting in monolithic transistors with f_T 's of 1.2 GHz. To optimize ac and dc circuit characteristics, computer aided design techniques were used which feature a complex

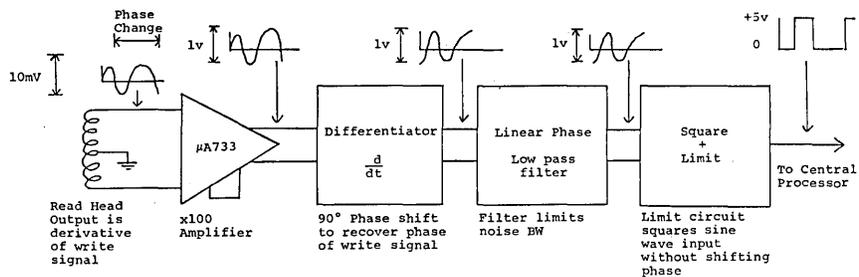


Fig. 1 Typical Phase Encoded Playback System.

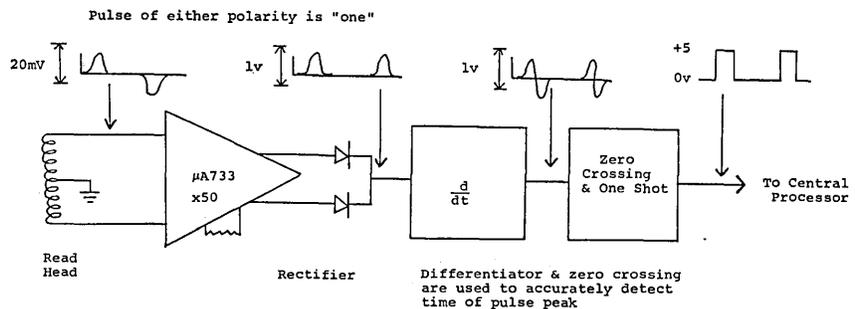


Fig. 2 NRZ Encoded Tape Playback System.

eight parameter transistor model that incorporates monolithic stray capacitances as well as linear and logarithmic options to calculate temperature dependences. The amplifier is expected to find use in many types of computer memories

— magnetic tape, disc, film, and plated wire — as well as in general purpose video applications.

New high speed tape and disc file memories use phase-encoded techniques to attain higher bits per inch

and higher read/write speeds than were previously possible with the more familiar non-return-to-zero system (NRZ). Fig. 1 illustrates a typical phase-encoded playback system. In such a system, the amplifier should have (1) high input impedance and low input capacitance to prevent lowering of the Q of the head, (2) differential inputs and outputs for isolation from system common mode noise, (3) excellent gain stability from unit to unit with temperature and supply variations, and (4) good phase linearity. In this function, the $\mu A733$ features input resistance and capacity of 30 K Ω and 2pF, respectively, a fixed gain of 100 and phase linearity of ± 2 degrees.

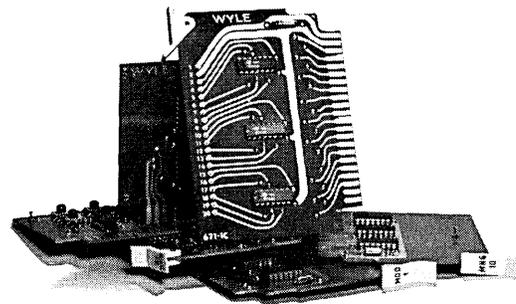
A typical NRZ magnetic tape system is illustrated in Fig. 2. While this application does not require the performance advantages of the $\mu A733$, it is convenient to use it here. Existing designs use a $\mu A702$ which requires three resistors to set the gain and two capacitors and one resistor for frequency compensation. The $\mu A733$ does not need any. Besides, the $\mu A733$ offers 10 times the CMRR at 1 MHz and only $\frac{1}{5}$ as much noise as the $\mu A702$, and it operates from convenient 5- or 6-volt supplies — not +12 and -6 as with the $\mu A702$.

Another application for the $\mu A733$ is in film and plated wire memories which are becoming popular today as ultra-high-speed random access memories. The output signal from the sense line is often only one millivolt in amplitude and exists for only 20 ns; therefore, the amplification and conversion to logic levels of this signal must be extremely fast. In a typical film memory system, the $\mu A733$ will amplify a 1 mV pulse, establishing a 200 V threshold level, and drive a CML gate in 12 ns. The propagation delay is 4.5 ns when driving a CML gate; this is 1.5 times faster than the CML gate itself.

The amplifier with the -55 to +125°C temperature range will sell for \$13.20 in quantities of 100 or more; the 0 to +70°C device, \$6.60 in the same quantities.

For additional information circle No. 199 on the Inquiry Card.

We'll ship a hundred modules in 48 hours.



One takes a little longer.

We stock our standard logic modules in sufficient depth to offer you 48 hour delivery.

But if you want something a little special, like a prototype or a short run for a unique application, we're geared to do that too. In fact, specials are one of our specialties. They just take a little longer.

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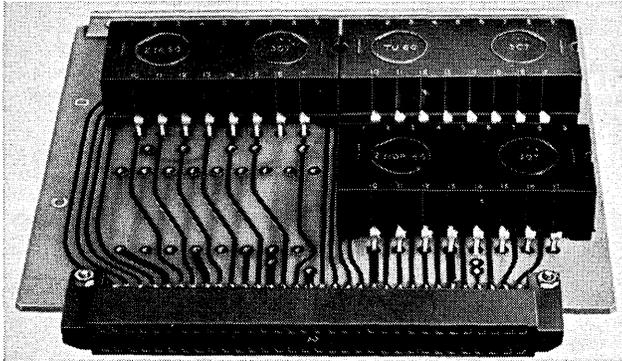
anything from card design to the completed system. Don't let the fact that we're not too big for your little jobs fool you. We're not too little for the big ones either.

Write for our complete IC Logic catalog with application notes. WYLE SYSTEMS, division of Wyle Laboratories
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NEW PRODUCTS



SOLID STATE LOGIC MODULES

A line of solid state logic modules designated '60-Series' Norbits, is designed to operate over a wide range of power and logic level (12-30V), and is well suited for positive sequential logic.

The Norbits are 17-pin, dual in-line packages consisting of silicon devices; transfer-molded encapsulation makes these modules extremely rugged. An important feature of the Norbits is their high immunity to circuit noise; they require only $\pm 25\%$ power regulation when operated at 24 volts. Noise immunity and wide regulation limits make Norbit control systems extremely reliable and reduce the cost of the required power supplies.

All practical 24-volt switching and control functions can be performed with combinations of '60-Series' Norbit NOR gates, inverters, timing modules and low- and high-power amplifiers. The Norbits are designed to interface with the complete Amperex line of decade counters, thumbwheel switches, input devices and accessories. Accessories include printed circuit boards, racks, connectors and power supplies.

Applications include elevator controls, packaging and process controls, machine tools, alarm systems, etc., in which low-speed AC relays have traditionally been used. Amperex Electronic Corporation, Component Division, Hauppauge, New York.

Circle No. 250 on Inquiry Card.

DIGITAL TAPE TRANSPORT

Series 4000 computer compatible magnetic tape transports can be used to write and read $\frac{1}{2}$ inch magnetic tape for both IBM 7 and 9 track formats. The 7 track models are switch selectable between 200/556/800 CPI. The 9 track version is 800 CPI only. Tape speed is 18 inches per second. Because the tape deck is constructed from a rugged temperature stabilized casting, no periodic mechanical adjustments are necessary.

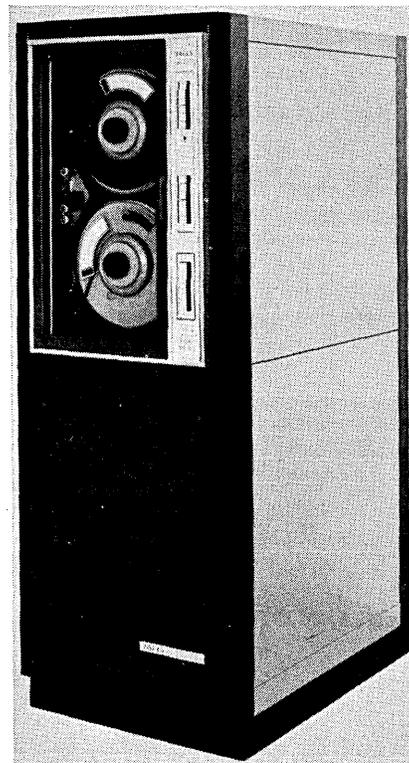
The units are offered in a variety of standard configurations. For instance, the user may choose the transport incorporating only the capstan and drive electronics or purchase units with complete read/write data electronics and complete interface logic.

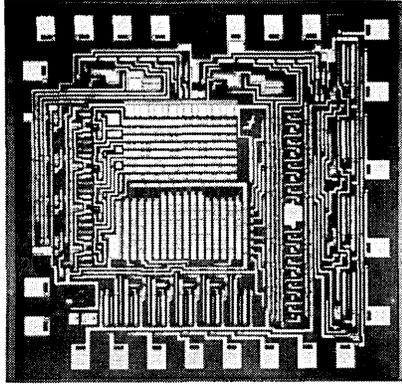
The tape units feature high speed rewind with servo controlled tape tension which takes only $1\frac{1}{2}$ minutes for a full $10\frac{1}{2}$ inch reel.

The Series 4000 handles two full $10\frac{1}{2}$ inch reels of tape even though only $26\frac{1}{2}$ inches of panel space are used in a standard 19 inch rack. For easy access, the transport is hinged on the front panel.

DTL integrated circuit logic and all silicon solid state devices on glass epoxy etched boards with Teflon are used throughout. Low mechanism forces and single capstan drive handle tape gently for long tape life and a built-in tape cleaner assures maximum data reliability. There are no moving parts during standby. Regulated, short circuit proof power supplies are used; operation is unaffected by changes in line frequency. Tally Corporation, Seattle, Washington.

Circle No. 251 on Inquiry Card.





CRT NUMERIC CHARACTER GENERATOR

A seven-segment character generator designed primarily for use with a CRT in the display of numeric information is the 3250, a MOS/LSI circuit with a single-chip complexity of 150 gates.

Offered in a 24-pin dual in-line package, the device accepts a four-bit binary coded word and generates four deflection pulses properly synchronized with a serial train of video pulses that subsequently control the beam on a CRT. The deflection pulses sweep the beam through the seven-segment character in eight clock cycles, while the video pulses blank the appropriate segments needed to form numerals.

The character generator is designed to generate the 10 numerals and a limited number of special symbols or letters. Approximately 550 characters can be displayed at a 60 Hz refresher rate.

Special outputs are available for "I" offset, decimal point and optional control use. Digital-to-analog type outputs are available for x and y current summing amplifiers.

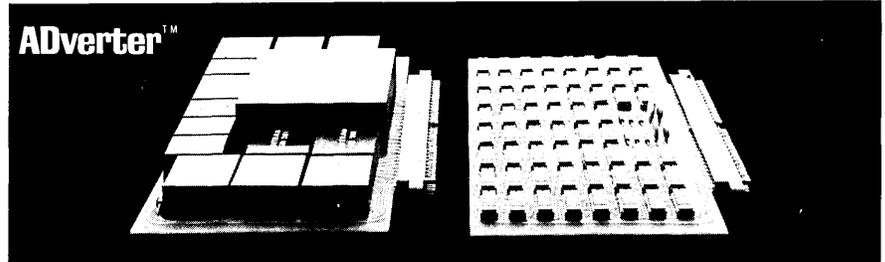
Other features of the 3250 include a 250 kHz segment rate, 160 mW power consumption, and a capability for full and half zeros, which allows a maximum of design flexibility.

The 3250 DIP is now obtainable in an operating temperature range of -55°C to $+85^{\circ}\text{C}$ at prices of \$60 each (quantities of 1-24), \$48 (25-99) and \$40 (100-999). A limited range unit (0°C to $+70^{\circ}\text{C}$) is priced at \$42, \$33.60 and \$28 each respectively. Fairchild Semiconductor, Mountain View, Calif.

Circle No. 254 on Inquiry Card.

NEVER

so many features, so many options in a synchro-to-digital converter for industry



for so little cost!

The ADverter™ Model SD12A1 is a general purpose synchro-to-digital converter, designed especially for the industrial market. It can be used to interface any type of synchro outputs to digital computers, readouts, displays, printers or combinations of the above.

The reliable, all solid state circuitry is composed of integrated circuits and silicone transistors throughout. Packaging features interchangeable, encapsulated sub-modules mounted directly on printed circuit boards. No calibration or adjustment means long, maintenance-free operation.

Ditran also makes digital-to-synchro converters comparable in versatility, features and price to the SD12A1. For further information, call your Local Clifton Sales Office or DITRAN, 25 Adams St., Burlington, Mass. 617-272-6210; TWX 710-332-6668.

\$795⁰⁰ Qty: 1-9

SPECIFICATIONS

INPUT SIGNAL

3-Wire synchro output
11.8Vrms $\pm 15\%$ line to line
400Hz $\pm 25\%$

REFERENCE INPUT

15-40Vrms (from synchro excitation source, one side grounded)

OUTPUT

12-bit parallel binary
MSB = 180°

RESOLUTION

LSB = $5' 16''$

LOGIC LEVELS

+5V $\pm 10\%$ = Logic "1"
0V to +.5V = Logic "0"

ACCURACY

\pm LSB peak error, all sources excluding synchro

TRACKING RATE

35°/Sec for 5' error max.

PACKAGE

2 PC boards, 8.3" x 5.5"
1.1" max. height

POWER REQUIREMENTS

+15V $\pm 5\%$ @ 75ma
-15V $\pm 5\%$ @ 100ma
+5V $\pm 10\%$ @ 400ma

OPERATING TEMPERATURE

0° to $+70^{\circ}\text{C}$

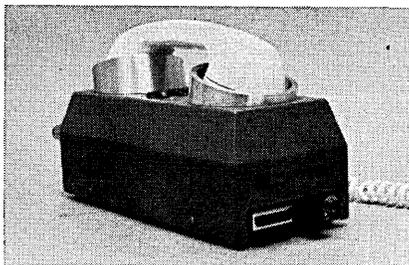
OPTIONS AVAILABLE*

- Multiplexing for multichannel inputs.
 - Coarse-fine mixing of two converters for multispeed synchros (1 and 8 speed, etc.)
 - Operation from resolver sine and cosine outputs.
 - Input levels 2 to 100Vrms; frequency 50Hz to 10KHz.
 - Up to 13 bits resolution.
 - BCD or 2's complement and sign bit outputs.
 - Serial data transfer; internal or external control.
 - Enclosure with prewired connectors.
 - Custom PC card layout and sizes.
 - Operation from 115V, 60Hz.
 - -55° to $+125^{\circ}\text{C}$ operating temperature range.
 - Additional custom features designed upon request.
- * At additional expense

DITRAN 
DIVISION OF CLIFTON
LITTON INDUSTRIES

CIRCLE NO. 63 ON INQUIRY CARD

NEW PRODUCTS



DATA COMMUNICATOR

The NYTRON DC-22 data communicator provides access to time-shared computers from teletypewriters or other similar data terminals via ordinary telephone lines.

The unit will connect to Model 33 and 35 teletypewriters and also to data terminal equipment requiring EIA-RS-232 interface. The DC-22 transmits by acoustical coupling, and receives by either acoustical or magnetic coupling which is switchable to gain maximum data reliability. The communicator will link the computer in either Full- or Half-duplex mode, and will communicate with other DC-22 units in Half-duplex mode.

Specifications include: Size — 11½" long x 4⅛" wide x 4½" high; Power Input—105-125V AC, 60 cps, 15 watts; Transmitted Frequencies — 1070 and 1270 Hz or 2025 and 2225 Hz switchable from the control panel; Received Frequencies — 2025 and 2225 Hz; and Data Rate — To 3000 BAUD. Nytron, Palo Alto, Calif.

Circle No. 255 on Inquiry Card.

FET SWITCH

The 2N5432 n-channel junction FET, designed for analog switches, commutators and choppers, has 5 ohms maximum ON resistance. The 2N5433 and 2N5434 offer 7 and 10 ohms respectively. Coupled with this very low ON resistance is a guaranteed maximum capacitance C_{rss} of only 15 pF.

Drain cutoff current $I_{D(OFF)}$ is less than 200 pA for the series; leakage is 200 pA max. Switching times less than 36 ns are guaranteed for the 2N5432 series.

Packaged in the TO-52, the 2N5432 is priced at \$40.00 in 100 quantities. The 2N5433 and 2N5434 are priced at \$20.00 and \$33.50 respectively. Siliconix, Inc., Sunnyvale, Calif.

Circle No. 267 on Inquiry Card.



TEST CRITERIA: Subject a wide range of cables including flat conductor, standard harness and Cicoil "Super-Flex" cable to a flex test of 420 cycles per minute to destruction.

TEST RESULT: Test stopped at over 70 million flexes with Cicoil "Super-Flex" cable operating perfectly—other cables?—Second best failed at 2 million cycles!

No one yet knows the ultimate life expectancy of Cicoil "Super-Flex" cable assemblies. Many have been in use for over ten years, without failure!

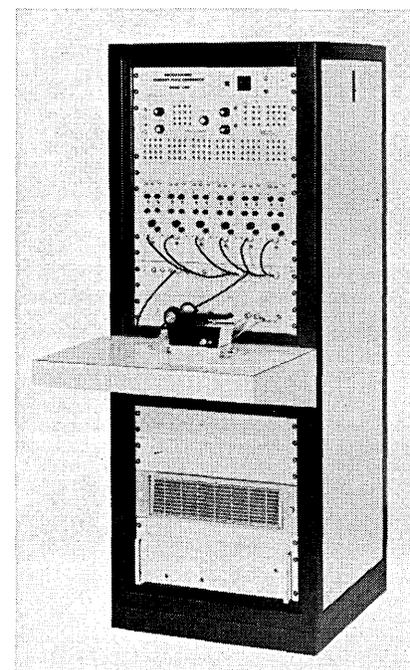
flexibility, highest wiring density or reliable operation in extreme environments, you should be familiar with Cicoil "Super-Flex" cable assemblies. We'll be happy to send

If your cable requirements include maximum literature and samples, plus complete test data.

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CIRCLE NO. 64 ON INQUIRY CARD

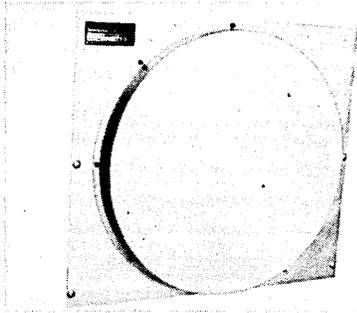


CURRENT PULSE GENERATOR

Model 1780 programmed current pulse generator is a test system for analysis of the parameters of high speed magnetic memory cores.

The program generator provides up to a 16 step pulse program with provisions for repeating single steps, pairs of steps or step quads for either of two available repeat intervals from 2 ms to 200 ns. Program stepping frequency can be varied between 500 Hz to 5 MHz. Drive current pulses can be varied in width from 10 ns to 2 us with rise and fall time continuously adjustable from 15 ns to 500 ns. Current pulse amplitude is variable over the range of from ±50 ma to ±1 ampere. Computer Test Corp., Cherry Hill, N.J.

Circle No. 264 on Inquiry Card.



DISC STORAGE SYSTEM

The 7000 Series disc storage system features a cost of less than 0.3 cents per bit. The line is available in five models ranging in capacity from 0.15 million to 1.2 million bits and has an average access time of 16.5 milliseconds.

Each memory system includes head address, decode and selection systems, bit and sector clocking, and complete "functionally packaged" integrated circuit boards; one for the entire read function, another for the write.

Capable of operation in either a vertical or a horizontal position, the recording media has a maximum track capacity of 37,360 bits. When mounted in a horizontal plane the disc assembly requires only 10½ inches of panel space.

Each weighs 25 pounds and may be mounted on a standard 19-inch relay rack. Information Storage, Inc., Detroit, Mich.

Circle No. 260 on Inquiry Card.

ROM CELL

The 2048 bit read-only memory cell is a four-phase Metal-Thick-Oxide-Silicon array consisting of 11 bits of two dimensional addressing—five and six bits respectively—and eight outputs.

The device permanently stores 2,048 bits of information in a 64 bit x 32 bit matrix positioned into eight segments. Each segment contains an eight bit x 32 bit matrix and an output stage. Access time is 1 µs.

The ROM chip outputs have internal "wire-or" capability, which allows the formation of ROM modules without any other component additions. This organization permits an extremely wide range of operating variations with a modular capability applicable to virtually all ROM systems.

Other features of the 2048 bit ROM are: Outputs can drive TTL, DTL or MOS without interface hardware; the device contains up to 11 bit decoding matrix; and it is expandable to 2048 x 8 ROM modules without additional hardware. Power dissipation is 120 mW @ 1 MHz. General Instrument Corp., Hicksville, N.Y.

Circle No. 273 on Inquiry Card.

PRINTED CIRCUIT CARDS

The "Micropoint" printed circuit card is an ideal replacement for costly multilayer cards. This concept, made possible by the unique Micropoint welder, permits a very high density (15 per cubic inch) of integrated circuits with all necessary wiring on only one layer. Twenty 14-lead flat packages may be mounted on a standard card.

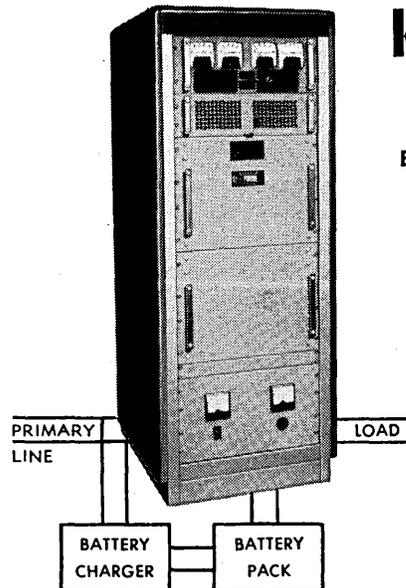
Standard cards include terminals, have edge gold plated pads and 22 test points. The dimensions are 4.55"l by 2.19"w by .062" thick. Microtechnology Div., Sterling Electronics Corp., Canoga Park, California.

Circle No. 270 on Inquiry Code.

MINI PROGRAM BOARDS

A miniature board with a total height of only 7/8" features program holes on 00.100" centers, providing high programming density in a very-small package. Contacts are rugged, durable beryllium copper which are either silver or gold plated. The board accepts program pins with a diameter of 0.040". The unique design of the new series eliminates the extra cover plate by using the top deck, which holds the contacts, as a cover panel. Contacts are recessed; units are supplied with Klip-On solder lugs. Programming Devices Div., Sealectro Corp., Mamaroneck, N.Y.

Circle No. 275 on Inquiry Card.

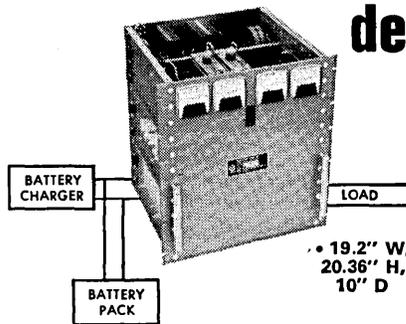


keeps AC profitably on-the-job!

ELECTRO-PAC® "A" Standby Power Supply

- Assures uninterrupted AC power
- Rated for reactive loads
- Regulates AC voltage to the load
- Suppresses line harmonics

The Model 2149 provides consistent power flow to critical processes... orderly start-up or shut-down during emergency power loss situations... dependable power for computer memories, microwave installations, instrumentation operation, and other applications requiring stable, regulated power. Maintenance-free. Available in 8 standard Models: Outputs—0.5 to 7.5 kva at 120 vac, 60 Hz. Inputs—22-29.5 through 105-142.6 vdc, and 100-130 vac, 60 Hz.



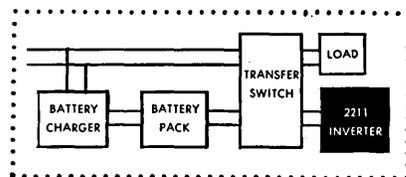
dependable AC power from DC

ELECTRO-PAC® "B" Sine Wave Inverter

- Provides regulated AC from varying DC source
- Rated for reactive loads
- Static circuitry eliminates overload/short circuit damage...no maintenance required

The Model 2211 provides 60 Hz, voltage regulated, harmonic suppressed 120 vac from 24, 48 or 125 vdc power sources. Can be used as a no-break series standby power system with charger large enough to recharge battery and carry the load. It can also be used in parallel systems with electro-mechanical switching.

Circle Reader Service Number, or ask for Bulletins 1351 and 1352...Write Group H11

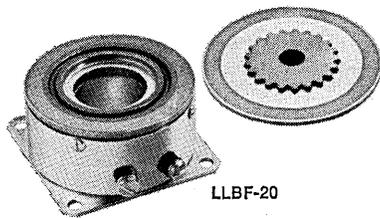


CLARE-ELECTROSEAL CORP.

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946 North Ave., Des Plaines, Ill. 60016

CIRCLE NO. 65 ON INQUIRY CARD

APILON®- FACED COMMERCIAL CLUTCHES/BRAKES



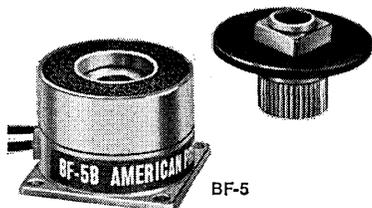
LLBF-20
(½ actual size)

American Precision Industries' Aylon®-faced electro-magnetic clutches and brakes, at rated loadings, have life expectancies of 100 million cycles. The unique Aylon® friction facing outlasts conventional types 10 to 1, virtually eliminating the need to replace facings. An added benefit—no unsightly or contaminated wear products.

Aylon® ceramic friction-faced clutches and brakes are ideally suited for applications where unusually severe loads are placed upon the product for long durations, such as in high-speed printers or in tape tensioning devices where continuous slippage occurs.

Units are available in ratings of 2 lb. in. to 70 lb. in. of torque, in sizes of 1" to 2½" body diameter.

HIGH - TORQUE COMMERCIAL CLUTCHES/BRAKES



BF-5
(actual size)

A low-cost line of commercial clutches and brakes is also available for less demanding applications.

These units can transmit torque without burnishing and are available in the same size and torque ratings as the Aylon® line. Standard coil voltage, 24 VDC. Other voltages available at no additional charge.



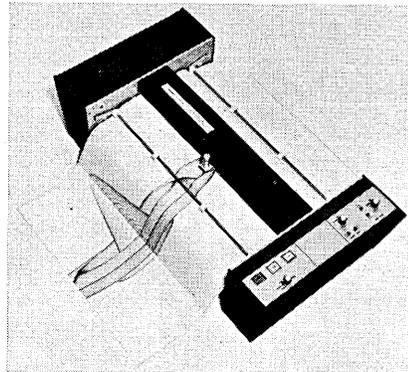
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NEW PRODUCTS



DIGITAL PLOTTER

The DP-3 digital plotter uses the convenient Z-fold chart paper with plotting surface a full 22" wide by 144" in length. This provides standard A, (8½" x 11") B, (11" x 17") C, (17" x 22") and D, (22" x 34") drawing sizes merely by tearing at the appropriate perforations. This logical size does not waste paper as some "odd width" plotters do.

The plotter's drive motors have two mounting positions. This enables the user to rapidly and easily change from .010" step size to .005" step size. Plotting rate is 300 increments per second. It can be used on-line, off-line or at remote time sharing locations.

An introductory price of \$5500 will be in effect until Dec. 31, 1968. On Jan. 1, 1969, the price will be \$6400. Houston Instrument, Div. of Bausch & Lomb Inc., Bellaire, Tex.

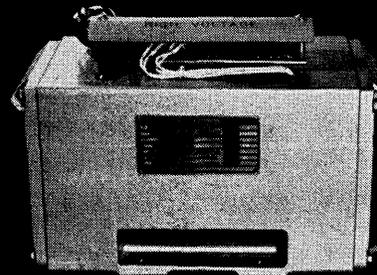
Circle No. 213 on Inquiry Card

MINIATURE PC CONNECTOR

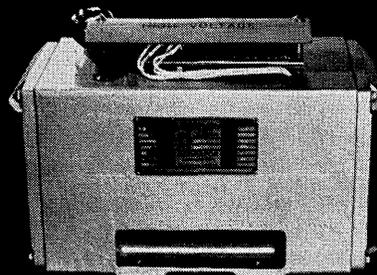
A miniature, two-piece printed circuit board edge connector exceeds the requirements of military specification MIL-C-21097.

The connector consists of male and female halves with 36 contacts in a double row on 0.125-inch centers. The male part is solder-mounted to the pc board providing a more positive contact to the board than is obtained with a slip-on edge connector. The female half mates positively to the male part by means of molded-in pins and bushings. Positive metal-to-metal contact is made between the gold-plated male and female parts, providing further reliability. A variety of termination designs may be used with this connector to permit connection to flexible cable, individual wires, etc. Cinch Manufacturing Co., Elk Grove Village, Ill.

Circle No. 274 on Inquiry Card.



COMPUTER POWER SOURCE



Not just another computer power supply but a complete computer power system. Designed for critical applications in main frame and peripheral equipment which require:

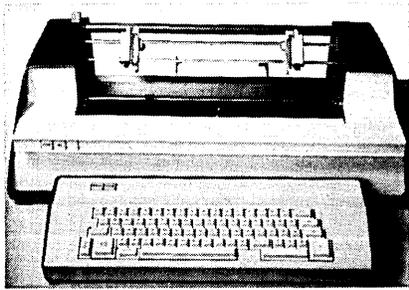
- Maximum Line Isolation
- EMI Reduction
- Positive Protection Against Voltage Overshoot
- Highest Reliability
- Minimum Maintenance
- Short Circuit Protection

All these features are inherent in a NOBRUSH® Power System. Combines the unique qualities of a "Nobrush" Permanent Magnet Generator and solid state rectifiers. Get the complete facts. Write or call:

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315 Tudor Lane, Manassas, Va. 22110
Phone: (703) 368-2101

CIRCLE NO. 67 ON INQUIRY CARD
COMPUTER DESIGN/NOVEMBER 1968



SERIAL IMPACT PRINTER

The Model 630 serial impact printer features a moving printwheel that allows faster, more efficient operation. Electronically controlled stepping motors cut down on moving parts — providing high reliability, low maintenance and longer life. Positive detent assures smudge-free printing. The Model 630 can be ordered with tractor feed or split platen. A companion keyboard is also available.

Other OEM products include reliable 50 cps. paper tape punches and readers in a variety of configurations. Series 500 Tape Punches and Readers incorporate many advanced design features such as small, efficient electromagnets in combination with overcenter springs for trouble-free punching over a long life reluctance type pick up — bi-directional reader — semi-automatic tape feed. Litton Automated Business Systems, Carlstadt, N.J.

Circle No. 239 on Inquiry Card

D/A BINARY LADDERS

A series R-2R, of D/A binary ladder networks with high accuracy and high speed conversion from digital to analog to within $\frac{1}{2}$ the least significant bit over the full military temperature range is available in five stock resistance values.

Operating temperature range of the devices is -55°C to $+125^{\circ}\text{C}$, with ladder resistance values of 1K, 2K, 2.5K, 5K, and 10K. Resistor tolerance is 5% standard, however 1% tolerance is available. Maximum settling time is 50 nanoseconds.

Physical characteristics of the R-2R binary ladders permit close-spaced board sandwiching, compatibility with automatic insertion equipment and ultrasonic board cleaning. The standard DIP mounting pins also provide extra leads for increased vibration and shock resistance. Mepco, Inc., Morristown, N. J.

Circle No. 265 on Inquiry Card.

MICROMINIATURE INDUCTORS

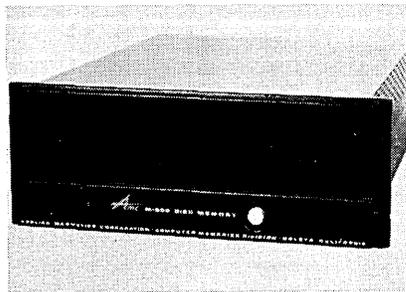
A series of semi-fixed and fixed microminiature inductors, designated 1052 and 1053, provide tiny adjustable or fixed inductors suitable for bonding to thick film substrates.

These low cost inductors offer an inexpensive technique for producing hybrid circuits utilizing chip integrated circuits.

The 1052 microminiature semi-fixed inductor is variable over a range of .06 to 2,000 μH . Prices range from a maximum of \$4.20 each in quantities from 1-9, and are considerably less in production volume.

The 1053 microminiature fixed inductor series is available over a range of .10 to 1,000 μH , with excellent Q readings. Suited for resonant circuits and decoupling applications, it is available at \$3.60 each in quantities of 1-9 and is priced considerably lower in large volume. Cambridge Thermionic Corp., Cambridge, Mass.

Circle No. 269 on Inquiry Card.



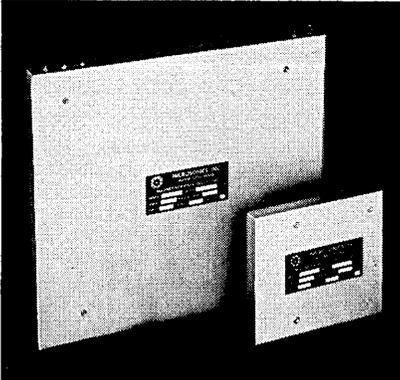
DISC MEMORY

Model M-200 disc memory is a fast access, head-per-track type mass memory specifically designed for small computers. The unit is available in four capacities ranging from 426,000 to 3,408,000 bits and average access time is 8.7 ms. The number of data tracks varies from 16 to 128 with 26,624 bits per track. Three timing tracks are included providing a bit clock, sector and origin pulse.

The memory uses a single 12-inch diameter magnetic disc and features a belt drive, integrated circuit electronics, 8-track flying head bars with precision lapped ceramic bearing surfaces, and compact, lightweight construction. Including electronics the memory weighs 45 pounds and is 7" high for use in a standard RETMA rack. The single quantity price for a 3,408,000 bit capacity unit including read/write electronics and power supply is \$5,600. Availability is three months. Applied Magnetics Corp., Computer Memories Div., Goleta, Calif.

Circle No. 212 on Inquiry Card

Computer Delay Line Storage Systems



Microsonics has proven capabilities and facilities to design and manufacture reliable computer delay line storage systems at high information rates (up to 100mc) which gives long term service in difficult environments of shock, vibration, and temperature. These systems have capability of handling digital signals for computer storage or analog information as in radar signal processing.

Ultrasonics computer storage lines, using fused quartz or zero T.C. glass, represent an ideal medium for high-speed computer storage up to 20mc rates.

Be it Computer Storage Systems; Digital Delay Lines; Magnetostrictive Delay Lines; or Variable and Tapped Delay Lines — Microsonics has the experience and capability to deliver both off-the-shelf and custom-designed systems for any specific operation.

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Improve your system reliability by installing GE photoelectric tape readers



PTR60 (Shown Above) and 70 Series:
—reliable, compact, "through-the-tape" Readers of field-proven design.
—choice of reading speeds up to 500 characters per second.

PTR80 (Shown Below) and 90 Series:
—high performance readers designed for speeds up to 1000 characters per second.
—reflected light reading technique eliminates problems of variation in tape opacity and permits reading of both punched and printed tapes.



Install them and forget them. GE photoelectric tape readers give lasting service with minimum maintenance. Features include:

- no electrical adjustments
- unidirectional or bidirectional operation

- simple, complete controls
- all solid state components
- tape handlers available for entire reader line

Numerous options are offered to meet your special requirements. Mail today for full details.

837-04A

Mail to Mr. R. S. Holmes, Printer-Reader Business Section, General Electric Co., 511 North Broad St., Philadelphia, Pa. 19123

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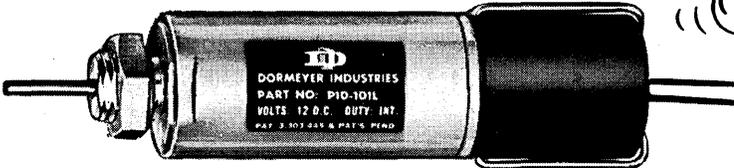
Printer-Reader Business Section

GENERAL ELECTRIC

CIRCLE NO. 69 ON INQUIRY CARD

NOW, THERE'S A

PUSH-TYPE TOO



in the DORMEYER TUBULAR SOLENOID line!

A year ago, Dormeyer introduced its Pull Type Tubular Solenoids. Their compact design, amazing life expectancy and low cost revolutionized design practices! Dormeyer Tubular Solenoids replaced many costly linkages where no solenoid had ever been used before.

Now, there's a Dormeyer Push Type Tubular Solenoid, too, with the same outstanding advantages and the same incredible life expectancy—another demonstration of Dormeyer Dependability!

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FEATURES

- Low cost
- Extremely long life
- 12 VDC—24 VDC (other voltages special)
- Various duty cycles
- Push and pull types
- Simple stud mount (including hardware)



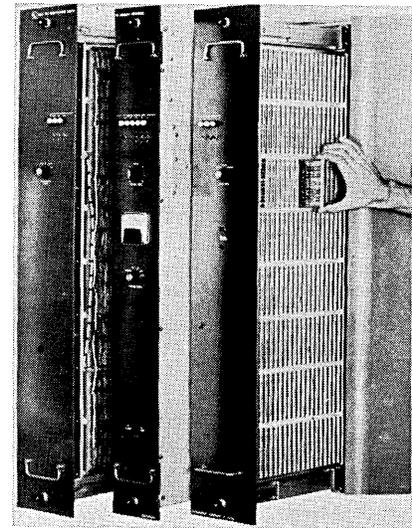
NEW PRODUCTS

ANALOG-TO-DIGITAL CONVERTER

Model ADC U Series is a complete high-speed analog-to-digital converter on a single p.c. board. It accepts input voltages upon command, and converts them to a binary code of up to 12 digits resolution.

This card contains a precision reference supply, logic, weighing network, switching, comparison and internal clock. Pastoriza Electronics, Inc., Newton Upper Falls, Mass.

Circle No. 272 on Inquiry Card.



DIGITAL-TO-ANALOG CONVERTER

The 764 multi-channel D-to-A converter with up to 512 analog output channels provides an economical method of converting digital data to a large number of analog outputs when using a single converter and multiple sample and hold output circuits. Conversion speed is 200,000 per second, for 11 binary bits or 3 BCD plus sign, with an accuracy of 0.01%.

Self check features include manual test/calibrate and the capability to monitor any output channel on a front panel voltmeter by dialing the number of the channel with thumbwheel switches.

A typical application would be in flight simulators where a large number of digital outputs from a digital computer are converted to analog signals for control and the operation of the aircraft cockpit instruments. Electronic Engineering Co. of California, Instruments Div., Santa Ana, Calif.

Circle No. 261 on Inquiry Card.

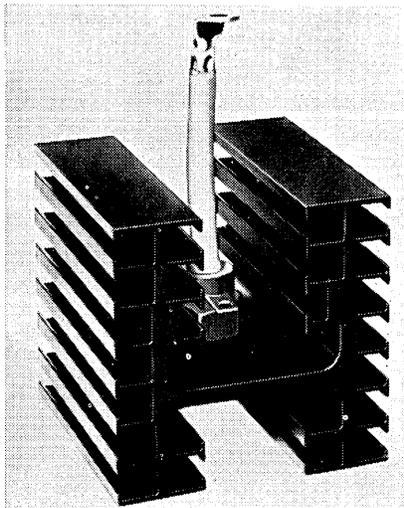
INCREMENTAL RECORDER

Model 70 incremental magnetic tape recorder has the following optional control features: (1) Data Enter — A manual thumb wheel switch and enter button which allows the operator to enter numerical information such as a date or record information; (2) Data Display — Data and parity are sensed at the write head and displayed. These two devices provide a built-in check of the electronic channels.

The recorder also features echo parity check — Parity generated from the sensed data at the record head is compared with the sensed parity. A light indicates an error in the machine electronics.

Basic price of the recorder is \$1,950. The data enter, the data display and the echo parity check are priced at \$200 each. Cipher Data Products, Inc.

Circle No. 256 on Inquiry Card.



HIGH-POWER SCR HEAT SINK

Very low thermal resistance is provided for high-power silicon-rectifier heat-sink mounting by the Model 2507. It provides a thermal resistance of 0.57°C/watt operating at 75 watts without the use of forced air.

Model 2507 is designed for use with components in bridge circuits and pre-packaged systems. The wide mounting shelf provides easy accessibility for mounting, monitoring and replacing the silicon controlled rectifiers or other high-power devices as well as space for necessary circuit connections and terminals.

Three standard modifications of Model 2507 provide for different mounting holes and tapped holes for attaching the units to the system or to each other. In addition, this heat sink is available in lengths other than the standard 4 inches (illustrated). Astrodyne, Inc., Burlington, Mass.

Circle No. 253 on Inquiry Card.

amnesia (am nē'zhə or am nē'zhiə) loss of memory due to a 10% voltage swing. *n.*

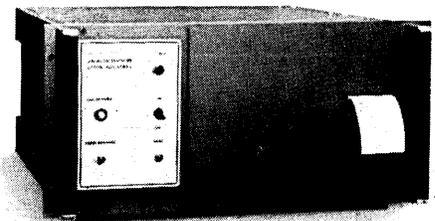
Raytheon Computer's 300 memory keeps right on reading and writing data reliably even when operating voltage and drive currents vary as much as $\pm 10\%$. And over a full temperature range of 0°C to 50°C. The 300 is a 2½D 900 nanosecond core memory for general data systems use. ■ If your definition of memory is: high performance, high reliability, high capacity, and delivery in 60-90 days, see us. Raytheon Computer, 2700 So. Fairview St., Santa Ana, Calif. 92704. (714) 546-7160.

SEE US AT FJCC BOOTH K10

CIRCLE NO. 77 ON INQUIRY CARD



The only impact printer that gives our optical printers a run for the money.



Litton Datalog's MC 2400 — the 40 line a second, state-of-the-art printer.

Here's the first impact printer that approaches our fiber optics printers in speed, reliability and state-of-the-art design. Engineered to be uncomplicated, the solid state MC 2400 offers up to 40 lines per second, 16 column capacity, truly asynchronous operation, single shaft simplicity, and electronically

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The only total portable, laboratory quality oscilloscope.



Model
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And only \$665.

Goes anywhere you need it. And at \$665,* there's no need for scope sharing. Operates from optional internal battery or 110/220 vac 50 to 400 Hz line. Compact 8½" x 9" x 15" size, weighs less than 20 lbs.

Features include: 20 MHz bandwidth; 17 nsec rise time; 18 sweep speeds; internal voltage calibrator; and triggering stability over 30 MHz.

Write for Bulletin TIC 3316 to Motorola Communications & Electronics Inc., 4501 W. Augusta Blvd., Chicago, Ill. 60651.

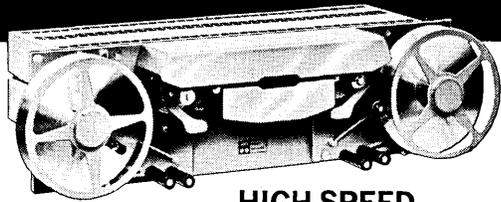
*Exclusive of options.



MOTOROLA
Precision Instrument Products

CIRCLE NO. 72 ON INQUIRY CARD

CHALCO DELIVERS TAPE READERS IN JUST 7 DAYS



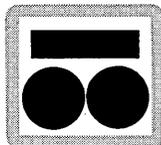
HIGH SPEED PHOTO-ELECTRIC TAPE READERS

Occupies only 3½" of panel space ■ Spoolers for 200 to 1,000 feet of tape ■ Operates asynchronously at any rate between 0 and 150 cps ■ Slews at 600 cps and stops "on character" ■ Lamp is unconditionally guaranteed for 1 year.

\$650⁰⁰
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For catalogue describing the complete line of Chalco tape readers write, call or telegraph:

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TWX 213-327-0167

CIRCLE NO. 73 ON INQUIRY CARD

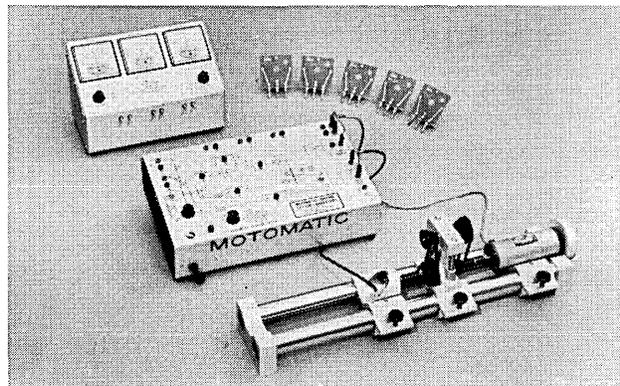
COMMUNICATIONS CONTROLLER

A high-speed serial synchronous communications controller allows users of SDS 9 Series computers to have high speed computer to remote terminal communications. The per data controller is a communications interface for the SDS 9 Series computers that operates and is programmed in much the same way that a standard peripheral is programmed. The controller generates all heading and trailing communications control characters, generates character parity and block parity on transmission. When receiving, it checks incoming character and block parity, and strips off all leading and trailing control characters.

Another feature is that it can be configured in such a way that it operates as an output or input device to the computer (simplex) but full or half duplex to the communications line.

Designed primarily for use with synchronous modems, the controller can be used with virtually any EIA RS 232 B interface modem, or locally over coaxial cable or other hardware. It can be used for computer-to-computer communications, computer-to-remote-batch terminal or other remote terminals such as graphic display terminals. Prices start at \$12,000. Peripheral Data Machines, Inc., N.Y., N.Y.

CIRCLE NO. 280 ON INQUIRY CARD.



CONTROL SYSTEM LABORATORY

Motomatic Control Systems Laboratory (MCSL) is a comprehensive piece of laboratory equipment, including both hardware and software, suitable for detailed university level training in electromechanical control systems principles.

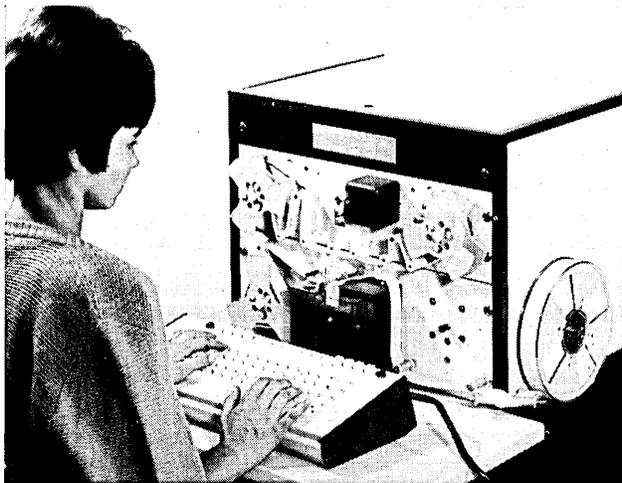
MCSL is completely self-contained and will relieve educators of the difficult job of laboratory development. Industrial applications of the MCSL are: a) design of actual servo systems; b) design of simulated systems; c) general wide-band amplifier.

Unique features of the lab include various changeable compensation networks and adjustable amplifier gain for optimizing system response. Inherent within the system are connections for velocity and/or position control which permit readily obtainable variations in feedback networks. All mechanical components, including the high response patented servomotor-generator, mount on a unique sturdy mechanical chassis.

MCSL can be used to simulate all types of servo systems, permitting the analysis of stability and the evaluation of various parameters and system response.

It is priced under \$1000. Electro-craft Corp. Hopkins, Minn.

CIRCLE NO. 257 ON INQUIRY CARD.

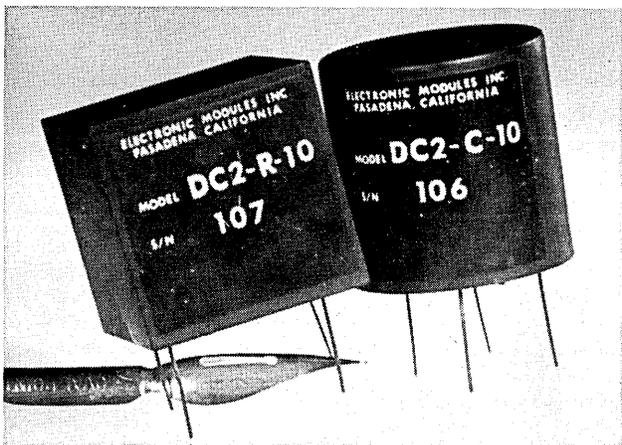


TAPE KEYPUNCH/VERIFIER

The CPV 700 paper tape keypunch/verifier keypunches, verifies and duplicates paper tape. It is available with a 10, 44, or full 67-key, keyboard. The unit can be furnished for any tape code including ASCII and six-channel teletypesetting. Optional extra program loop reader provides automatic code insertion, fixed fields, automatic duplicating at 35 cps. Pulse-type key switches, combined with integrated circuit logic provide free, high-speed operation of the keyboard without double punching, missing codes, etc.

Both punch and reader are bi-directional (may be backed up) for easy error correction. Display lights on the keyboard always show the last code read (or punched). Housed in a 34" high steel cabinet, the unit sells for \$4,500. Computer Products, Inc., Seattle, Wash.

Circle No. 259 on Inquiry Card.



MINIATURE DC TO DC CONVERTER

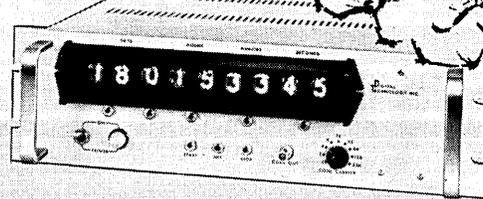
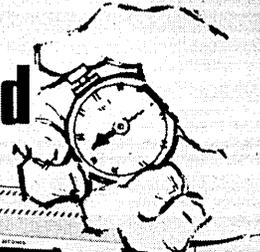
A line of miniature dc to dc converters features high input-to-output isolation, a high degree of line and load regulation and excellent temperature stability over a wide range of load currents. The devices are packaged in one inch cubes or cylinders allowing modular or circuit board application.

Output voltages range from 5 to 100 Vdc and unit loads to 100 milliamperes with an input voltage of 28 Vdc ± 4 Vdc.

The unit is a solid-state device incorporating silicon transistors and diodes with 1% metal film resistors in a cordwood stacked welded package with a weight of 12 grams. Price is \$75 to \$170, in low quantities, depending on type with delivery of 3 to 4 weeks. Electronic Modules, Inc. Pasadena, Calif.

Circle No. 263 on Inquiry Card.

when every Microsecond counts



... you can count on the G-204 Time Code Generator — a real time saver that allows you to index data while recording at high tape speeds — and playback dozens of times more slowly — use your standard tape search to find data to milliseconds — and resolve events to microseconds.

- high speed resolution indexing —
- dub-in real time at faster rates —
- use as normal time-of-year generator —

EQUIPMENT SPECIFICATIONS

SIGNAL OUTPUT: IRIG B Time Code. Frame rates from 1 fps to 256 fps in nine binary steps. Carriers from 1,000 cps to 256kc. Level 3 volts peak-to-peak into 75 ohms.

CONTROLS: Power ON-OFF. Time Preset. Code Rate Selector — 9 position carrier frequency — bit rate and frame rate.

SIZE: Rack mounted 5 1/4" H x 19" W x 13" D



digital technology inc

223 Crescent Street, Waltham, Massachusetts 02154

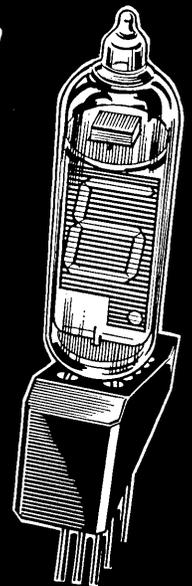
CIRCLE NO. 74 ON INQUIRY CARD

SMALLEST—NEON READOUT INDICATOR

ELFIN™.M.

HAS 8 ADVANTAGES

- 1 SINGLE PLANE** — closely inter-linked segments insure uniform clarity and easy readability.
- 2 BRIGHTER DISPLAY** — brighter neon glow, with no flashover from unlighted stacked filaments.
- 3 WIDER ANGLE VIEWING** — ignited electrodes are all up front to provide widest viewing angle.
- 4 SMALLEST IN SIZE** — 0.41" diameter results in a 4-digit display within a 2" space.
- 5 COMBINATION SPACER & MOUNT** — simplifies P/C wiring; changes leads from round to straight line.
- 6 NUMERIC & OTHER CHARACTERS** — displays 0-9 numerals, + and - symbols, some alpha, and decimal point.
- 7 LONG OPERATION LIFE** — neon displays possess an infinite life span, thereby making them most reliable.
- 8 LOW POWER REQUIREMENT** — exceptional low cathode current of 0.4 ma. per segment makes it ideal for ICs.



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CIRCLE NO. 76 ON INQUIRY CARD

NEW PRODUCTS

NAND/NOR GATES

A series of triple 3-input NAND/NOR gates, the SG-320 series integrated circuits, consist of a three-input AND gate followed by an inverting amplifier with a cascade pull-up output network. Each gate functions as a NAND element in positive logic and as a NOR element in negative logic. The devices in this series operate on a five-volt power supply with a typical propagation delay of six nanoseconds.

The SG-320 gate is available in full military (-55°C to $+125^{\circ}\text{C}$) or industrial/commercial (0°C to $+75^{\circ}\text{C}$) temperature ranges.

The units have a fanout of 11 in the military prime, and fanout of six in the standard version. The industrial prime units have a fanout of nine and five in the standard.

They are available in both fourteen-lead flat-pack or dual in-line plug-in ceramic packages. The devices are wholly compatible with other Sylvania integrated circuits including the company's line of monolithic digital functional arrays. Semiconductor Div., Sylvania Electric Products, Inc., Woburn, Mass.

Circle No. 266 on Inquiry Card.



INCREMENTAL ACQUISITION SYSTEM

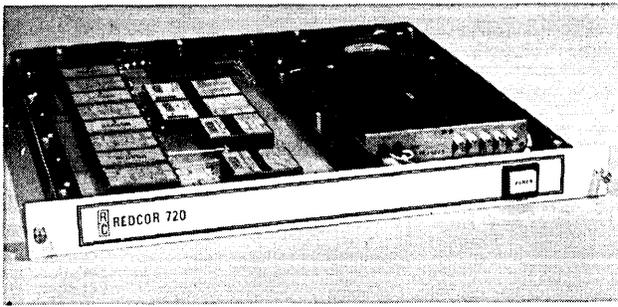
The Ince-Data Mark II data acquisition system utilizes IBM-compatible magnetic tape cartridges to completely eliminate digital playback conversion. It can be cartridge-loaded and programmed in the field. The solid state system has five basic components: programable data formater/controller, analog and digital multiplexer, analog to digital converter, digital clock, magnetic tape recorder. Data format handles up to 144 individual digital characters. Systems control is achieved with a 400-pin patchable connector.

High-speed analog multiplexer sequentially samples 20 differential or 40 single-ended inputs, with single scan, continual scan or start/stop scan rates.

Digital clock correlates all input data; front panel decimal display shows days, hours, minutes and seconds. Clock can be used to drive external controls or remote displays; preset and start/stop controls provide start/stop synchronization with external time standard.

Incremental magnetic tape recorder is 7-track and compatible with IBM NRZI at densities of 200 and 556 BPI, and records at speeds up to 2,000 characters per second synchronous speeds and up to 1,000 characters per second asynchronous. Recorder uses a self-threading single speed cartridge for quick and easy loading or reloading; each cartridge holds 1,000 feet of 1.5 mil mylar tape wound on a removable 6" diameter reel. All recorder controls can be mounted remotely. Ince-Data Corp. Albuquerque, N. M.

Circle No. 258 on Inquiry Card.



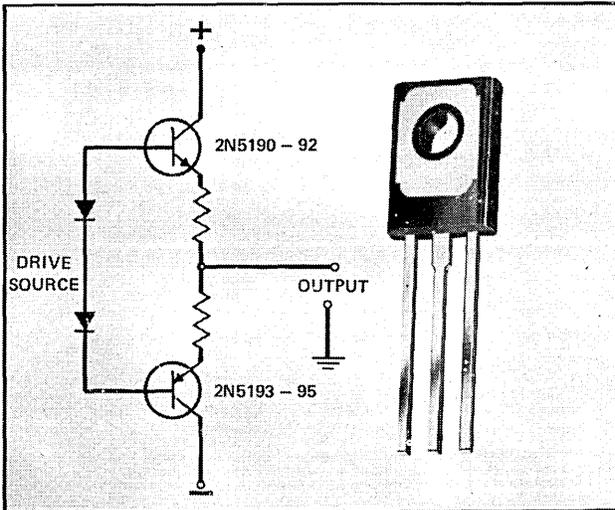
MULTIPLEXER/A-D CONVERTER

The Model 720 multiplexer/A-D converter, consists of a 32 channel multiplexer, sample-and-hold amplifier, 12-bit analog-to-digital converter, reference supply and sequence control unit. The unit may be ordered with 8, 16, 24 or 32 channels. Additional multiplexer units extend the number of channels to 128.

Full-scale input is ± 10 volts and output is 12-bit parallel in any of 3 output codes; offset binary, one's complement, or two's complement. Data and control signals employ DTL logic levels. The sequence control unit permits random or sequential selection of channels as well as short cycle addressing. Throughput rate of the system is 20 KHz.

The unit is packaged in a standard 19" rack-mounting chassis, 1 $\frac{3}{4}$ " high and 18" deep. The basic 32 channel unit sells for under \$3,000. Delivery 60 days ARO. Redcor Corporation, Canoga Park, Calif.

Circle No. 252 on Inquiry Card.



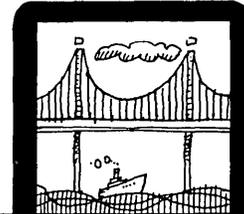
PLASTIC SILICON POWER TRANSISTOR

The NPN/PNP 2N5190-95, 4-amp. Thermopad™ packaged silicon power transistors feature sustained V_{CE0} of 40-80 volts and total device dissipation of 35 watts at 25°C. Dc current gains at 1.5 A range from 20/80 to 25/100 for the units. Other specifications include a collector-to-emitter saturation voltage of 0.6 volts at 1.5 A of collector current, and a minimum current-gain-bandwidth product of 4.0 MHz.

The units can be used as NPN/PNP pairs to gain all the circuit-simplifying advantages of direct-coupled, complementary symmetry plus furnish a higher degree of frequency stability in both ac and dc-driven loads without the addition of expensive, impedance-matching driver transformers. Motorola Semiconductor Products Inc., Phoenix, Ariz.

Circle No. 262 on Inquiry Card.

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High Voltage Bridges

Specifications on miniature transfer-molded, high-voltage single-phase bridges are listed in Data Sheet T-143. Unitrode Corp., Wauertown, Mass.

Circle No. 306 on Inquiry Card

Optical Character Reader

This brochure describes use of the 915 page reader, relating optical character recognition (OCR) technology to the special problems of modern banking. Control Data Corp., Minneapolis, Minn.

Circle No. 311 on Inquiry Card

Aluminum Knobs

A six-page catalog featuring machined aluminum knobs describes in detail six series of knobs including standard, miniature, skirted, deluxe, and various knurled types. Alco Electronic Products, Inc., Lawrence, Mass.

Circle No. 314 on Inquiry Card

Ribbon Connectors

Two popular rack-and-panel connector series, featuring a unique ribbon contact principle for longer life and lower cost, are described in a 16-page catalog. Amphenol Industrial Div., The Bunker-Ramo Corp., Chicago, Ill.

Circle No. 321 on Inquiry Card

Display Storage Tubes

Display storage tubes for applications ranging from airborne search and fire control radar and sonar displays to oscillographic and data storage displays are described and illustrated in a six page quick reference guide. Westinghouse Electronic Tube, Elmira, N.Y.

Circle No. 301 on Inquiry Card

Computer Tape

Bulletin T252, a four-page brochure describes the features, uses and varieties of the 870 Series computer tape. Ampex Corp., Redwood City, Cal.

Circle No. 303 on Inquiry Card

Switches

Practical applications of switches to eight different manufacturing problems are illustrated in a four page booklet "Micro Tips No. 47." Micro Switch, a division of Honeywell, Freeport, Ill.

Circle No. 319 on Inquiry Card

Rack-And-Panel Connectors

A wide range of low-cost rack-and-panel connectors are described in a 28-page guide. Included is an illustrated index, which shows the basic characteristics of each connector. Elco Corp., Willow Grove, Pa.

Circle No. 309 on Inquiry Card

Count/Memory Module

This data sheet completely describes a 15MHz decimal counter and display module which stores the count in a quad latch memory and displays on a cold-cathode readout tube. Integrated Circuit Electronics, Inc., Waltham, Mass.

Circle No. 326 on Inquiry Card

Core Memory Systems

Bulletin TB 402B features Micro Stor, the first in a series of high speed, low cost core memory systems. Complete specifications, input/output interface circuits, timing charts, and connector pin assignments are included. Standard Memories, Inc., Sherman Oaks, Cal.

Circle No. 305 on Inquiry Card

AR Relays

Product Bulletin 154 features assured reliability series relays, including specifications and manufacturing procedures. HiG, Inc., Windsor Locks, Conn.

Circle No. 328 on Inquiry Card

Semiautomatic Wiring System

A four page brochure describes the concept, equipment and operation of the P/2/P semiautomatic wiring system. Marketing Dept., Product Improvement Corp., Santa Ana, Cal.

Circle No. 317 on Inquiry Card

Wire & Cable

In this 48 page business machine wire and cable catalog, illustrated data has been grouped into main categories—single wire, coaxial cable and multi-conductor cable. Brand Rex Div., American Enka Corp., Willimantic, Conn.

Circle No. 300 on Inquiry Card

Dual Scaler Driver

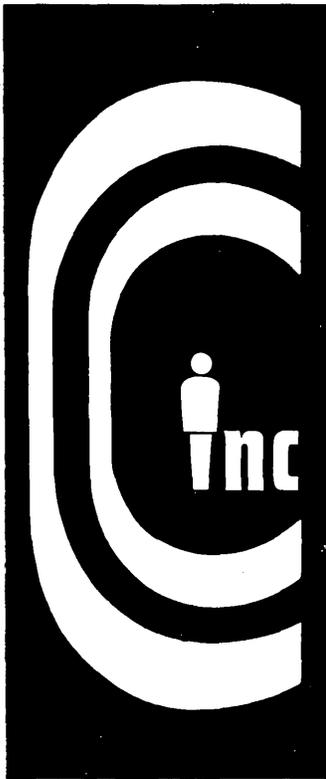
A technical data sheet offers a comprehensive description of the Model 135 dual scaler driver, a compact dual-channel logic amplifier. Included are illustrations and specifications. LeCroy Research Systems Corp., West Nyack, N.Y.

Circle No. 310 on Inquiry Card

Alphanumeric Generator

The Symbolray TM alphanumeric generator for cathode-ray display or hard copy printout is the subject of a 10-page brochure, including specifications, principles of operation and applications. Raytheon Company, Industrial Components Operation, Quincy, Mass.

Circle No. 304 on Inquiry Card



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Intermediate and senior openings exist for engineers to work on advanced development of Mass Storage devices, including magnetic drums, disks and high density magnetic card systems. Two to five years experience in magnetic recording devices or equivalent with BS in EE or Physics.

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Background in both circuit design and logical design and experience with integrated circuits, cellular logic, etc., which constitutes background capability for research work in LSI. BS in EE, MS in EF desired. Two to eight years experience.

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BSME 2-5 years experience Gear trains and mechanisms for audio visual entertainment and education equipment.

CIRCUIT DESIGN ENGINEERS 9-15K

A minimum of two years of circuit design experience. To design control circuitry for computer peripheral devices. Knowledge desirable: digital circuit design using integrated circuits or discrete components, CRT deflection, sync, or video circuit design, data modem circuit design, photocell amplifier design, high current switching circuit design. Openings at all levels.

GUIDANCE/FLIGHT CONTROLS SYSTEMS ANALYSIS 12.5-18.5K

Senior G & C analysts, with experience in conceiving, analyzing evaluating advanced guidance and flight control techniques for tactical missiles. Must be capable of using analog or digital computers in analysis and design of non-linear and couple loop control systems. BS in EE, ME, AE. Physics required, MS preferred.

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Analog circuit design (A/D to D/A particularly desirable), as well as system design and/or logic design. Applicant should have some project responsibilities.

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BEE/ME/equivalent plus two years quality experience in electronics, including preparation of test procedures, design of special test equipment, test data review, material review, etc.

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TEST EQUIPMENT DESIGN 11-18K

BSEE plus five years experience in diversified circuit design, — digital, servos, microwave, audio, and linear micro-circuits. Familiar with digital and simulator techniques.

SENIOR RADAR ENGINEER To 18K

BSEE/MSEE. At least five to eight years' experience in radar systems. Duties include systems engineering in Doppler Radar Equipment.

PROJECT ENGINEERS — Displays Sub-Systems

Minimum BSEE 8-10 years experience.

PROJECT ENGINEERS — Data Processing Sub-System.

Minimum BSEE 8-10 years experience.

SYSTEMS AND PROCEDURES ANALYST

BSBA Minimum plus 3-5 years experience.

MAGNETICS DEVELOPMENT MANAGER To 25K

Requires a BSEE plus 5-7 years in magnetics and materials development. He will supervise the development of new magnetic packaging techniques and processes. His other duties will include the supervision of test and evaluation of electronic and magnetic components. Also included will be the development of new core memory and plated wire design concepts for commercial programs.

MAGNETICS PROGRAM MANAGER To 20K

Requires a BSEE plus five years in the Magnetic Memory field. He must be an outstanding magnetics design engineer. To design a completely new military system incorporating a plated wire memory. To solve engineering and production problems associated with this high speed memory device. Conducting research studies and evaluating their end results. Act as a technical representative with outside organizations and government agencies in negotiations and planning of major contracts and projects.

SENIOR ELECTRICAL ENGINEER — LEAD DESIGN ENGINEER 13-18K

BSEE with a minimum of five years' experience Military Electronics. At least two years' logic design using microcircuits. Navigation experience desirable. Duties to include lead design engineer. Advanced Engineering on navigation and terminal guidance equipment. Will assume project engineer duties.

MARKETING 12-17K

Government Marketing Representatives. BSEE or equivalent plus three years experience in contacting government and prime contractor representatives. Requires knowledge of computer systems.

PACKAGING ENGINEERS 10-15.6K

BME and minimum 2 years experience in design and packaging of airborne electronic equipment. State-of-the-art techniques. Project responsibilities.

DEVELOPMENT ENGINEERS 11-14K

Small Peripherals

Openings exist for intermediate to senior electrical engineers to advance a future development program in small peripherals. The work requires the ability to conceive new and simplified design concepts and carry them through to the design feasibility models. A BSEE degree and a minimum of three years experience is required, preferably in any or all of the following areas: servo systems, position transducers, actuators, logic, solid state and integrated circuits.

MASS MEMORY STORAGE MECHANICAL ENGINEERS 9-18K

Intermediate and senior openings exist for mechanical engineers to work on development of magnetic drums, disks and magnetic card systems. Openings exist in all areas of Mass Storage development, including high-speed small mechanisms design, electro-mechanical servo systems, packaging and test. Requirements are two to five years experience in magnetic recording devices or equivalent with BS in ME, Physics or EE.

PRINCIPAL SYSTEMS ENGINEER To 16K

Applicant should have 3-4 years experience in instrumentation, plant design, distribution, or operation in the power industry, with some experience with on-line Real Time Computer Systems. Previous programming and knowledge of control theory helpful. BS/MS

SENIOR PROGRAMMER To 15K

Applicant should have 3-4 years intensive experience on industrial process control software areas and should have ability to assume lead position on any of the sales order efforts.

DIAGNOSTIC PROGRAMMER To 15K

Applicant should have 2-5 years assembly language programming experience and program system design, preferably in diagnostic or fault analysis programming. 6-9 years computer system design, logic design, or computer test engineering.

ASSISTANT ENGINEERS To 8.4-11K

Applicant should have experience in testing digital circuits and in semi-automatic test equipment. Data processing experience extremely desirable.

ENGINEER — ELECTRONICS To 12-14K (Digital Logic Module Development)

Applicant should have 1-3 years experience in circuit and product design. Ability or experience in communicating with Marketing and Manufacturing personnel as well as with customers very desirable.

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LITERATURE

Gold Plating

Reprints of a technical article on the electroplating of gold on high-reliability electronic devices are offered in quantity. The article discusses development of a plating specification and process for gold plating of components used in semiconductor devices. Technic, Inc., Providence, R. I.

Circle No. 330 on Inquiry Card

Renovated Computers

A two-page illustrated data sheet describes the refurbished Control Data LGP-30, now available at a fraction of the original price, but with a warranty similar to a new machine. Specifications of the computer are presented in detail. Mutual Computer Systems, Culver City, Calif.

Circle No. 323 on Inquiry Card

Teflon Products

A four-page catalog describes a newly-expanded line of Teflon-insulated wire and cable including 50 new miniature Teflon hook-up wires, RG/U transmission line cables and Type E shielded, Teflon-jacketed cables with one to four conductors. Belden Corp., Chicago, Ill.

Circle No. 312 on Inquiry Card

Printed Circuit Boards

A two-page data sheet describes 8 and 10 pin TO-5 and 14 and 16 pin dual-in-line printed circuit boards for design engineers. Specifications listed include power connections, hole diameters and the number of integrated circuits each board will accept. Elgin Electronics Inc., Erie, Pa.

Circle No. 329 on Inquiry Card

Magnetic Tape Recorder

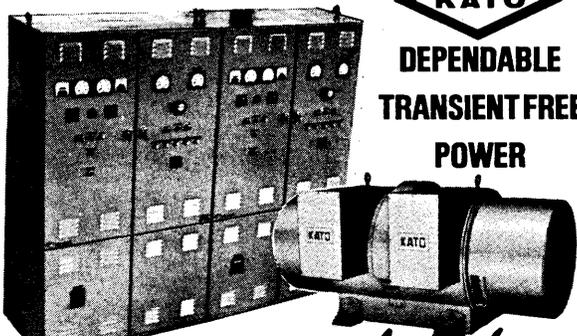
Long record time combined with space-saving, bi-planar reel configuration that provides precise tape guiding are among the major features of the 10-286 instrumentation magnetic tape recorder described in a four page brochure. Data Div., Genisco Technology Corp., Compton, Cal.

Circle No. 302 on Inquiry Card

Vestigial Sideband Data Set

Bulletin ECD-18 on the DigiNet TDM-220 vestigial sideband data set describes equipment for rapid transmission of synchronous or asynchronous serial binary data at speeds up to 2400 bps over 2- or 4-wire dedicated voice lines. General Electric Communication Products Department, Lynchburg, Va.

Circle No. 315 on Inquiry Card



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CIRCLE NO. 96 ON INQUIRY CARD

COMPUTER DESIGN/NOVEMBER 1968

Lens Cap and Base Assemblies

Catalog CR680 provides data, illustrations and military type designations for lens cap assemblies and base assemblies. Dialight Corp., Brooklyn, N.Y.

Circle No. 318 on Inquiry Card

On-Line Disc File Systems

On-line disc file systems are featured in a four page brochure which includes complete specifications and current applications. Bryant Computer Products, Walled Lake, Mich.

Circle No. 320 on Inquiry Card

Programmable Clock

This bulletin describes the Model 1130 Programmable Clock/Calendar which reads the time in hours and hundredths of an hour and the date in month and day into the core storage of the IBM 1130 computer. Chrono-log Corp., Broomall, Pa.

Circle No. 308 on Inquiry Card

Digital Data Monitor

A two-page data sheet contains complete specifications and a systems block diagram on digital data monitors. Lear Siegler, Inc., Cimron Div., San Diego, Cal.

Circle No. 325 on Inquiry Card

Optical Scanner

How an optical scanning system saves time and money for an electric utility is described in a reprinted article on the Digitek 70 optical reader. Optical Scanning Corp., Newtown, Pa.

Circle No. 322 on Inquiry Card

TYO Capacitors

Performance curves that illustrate how TYO capacitors meet or exceed military specification performance requirements (MIL-C-11272) are featured in a four-page data sheet. Electronic Products Division of Corning Glass Works, Corning, N. Y.

Circle No. 324 on Inquiry Card

MOS Devices

A reliability report on a MOS product line describes quality and reliability programs including recent test results. National Semiconductor Corp., Santa Clara, Calif.

Circle No. 316 on Inquiry Card

Repeat Cycle Timers

This four-page bulletin provides complete operating and mounting information on the line of basic repeat cycle timers. The A. W. Haydon Company, Waterbury, Conn.

Circle No. 327 on Inquiry Card

Hard Copy Generator

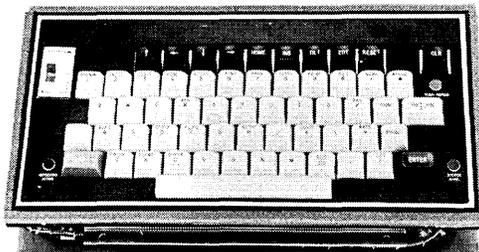
A four-page brochure on the RAP-COR Hard Copy Generator System for computer or video outputs describes the system's capability for recording information displayed on a video monitor or CRT. OPTO-mechanisms, Inc., Plainview, L. I., N. Y.

Circle No. 307 on Inquiry Card



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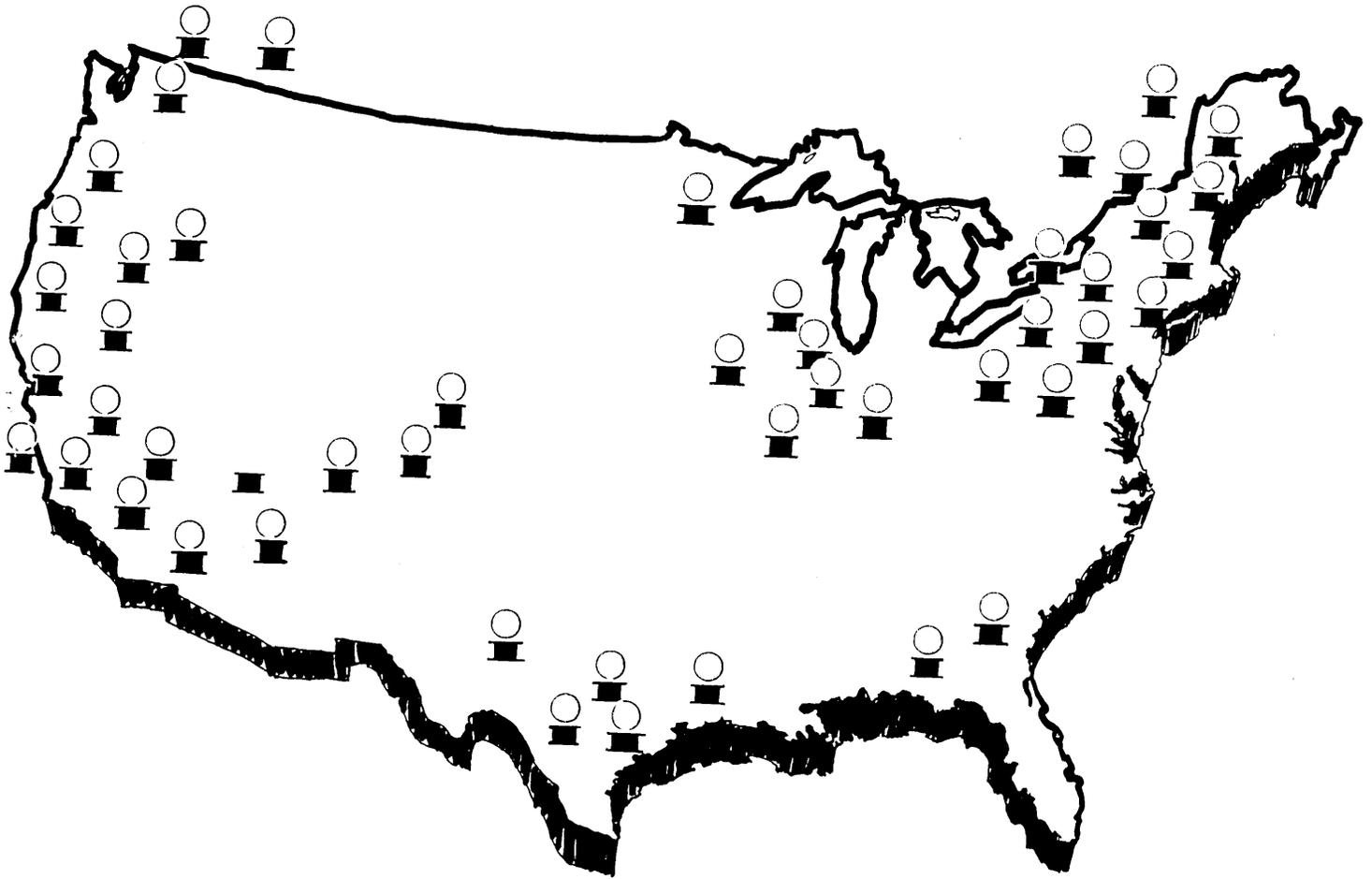
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CIRCLE NO. 98 ON INQUIRY CARD

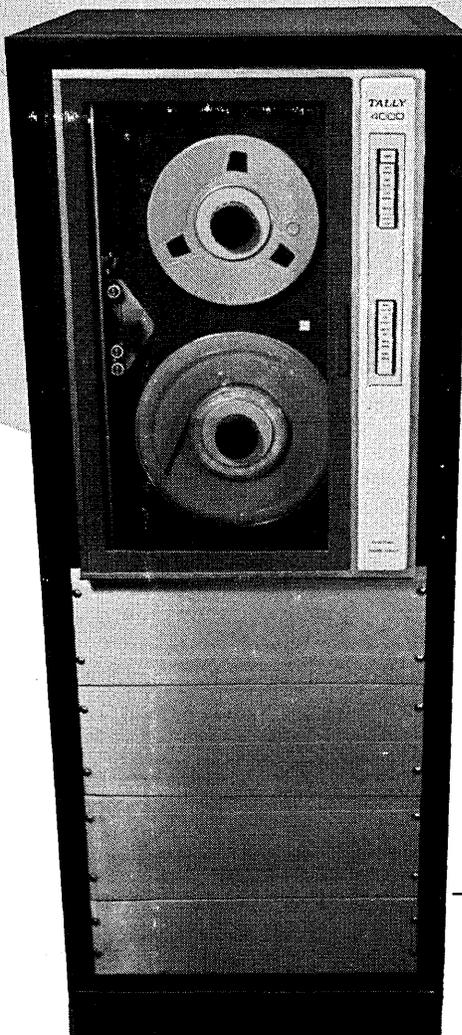
It's one thing to make a low cost digital tape unit, it's something else to make a low cost digital tape unit without compromise. Tally did.

From bare bones to full dress, Tally's new low price Series 4000 computer compatible digital tape units were built from the ground up with no compromises in design.

Series 4000 digital tape units are available and in production now. You can order the transport only with servo and capstan electronics. Or you can order the full dress version with read/write data electronics and complete interface logic.

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- High speed rewind with servo controlled tape tension (another no compromise) takes 1½ minutes for a full 10½ inch reel of tape.
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- DTL logic or 7 and 9 channel formats. Special read only version can handle both formats without head change.
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- Low mechanism forces and single capstan drive handle tape gently for long tape life.

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