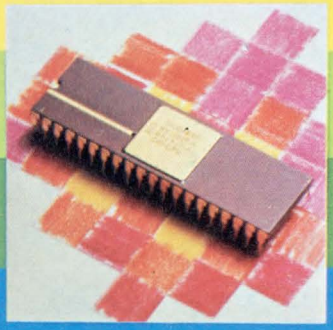
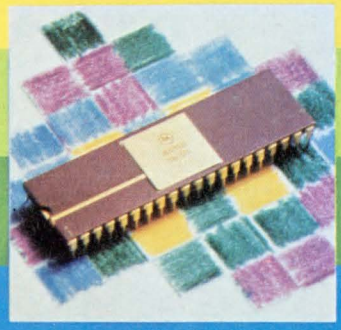
VOLUME 10, NO. 11 NOVEMBER 1980

Digital Design

Computers • Peripherals • Systems





Debugging Multiprocessor Systems

Minicomputers

μP Development Systems

μCs Control Keyboards

New From Kennedy

Model 6450 High Density Cartridge Tape System

Low cost, flexible and reliable backup—that's Kennedy's Model 640 Cartridge Tape Drive and Model 650 Embedded Formatter—combined in one compact package—Model 6450. Model 6450 is loaded with features, such as:

- Low power consumption—the system requires only +5 and +24 volts for a total consumption of under 40 watts.
- Serpentine recording head—eliminates time consuming rewinds between tracks during backup process.
- 6400 BPI recording density—yields up to 17 Mbytes of unformatted data capacity on a 450 ft. cartridge.
- Infrared tape position detection—virtually impervious to ambient light, a major factor in tape position sensing errors.
- Online self test—The 6450 system performs online self test before your backup operation begins.

These are only a fraction of the features that make Model 6450 the most advanced ¼" tape cartridge available. All these features, combined with Kennedy experience and reliability guarantee it.

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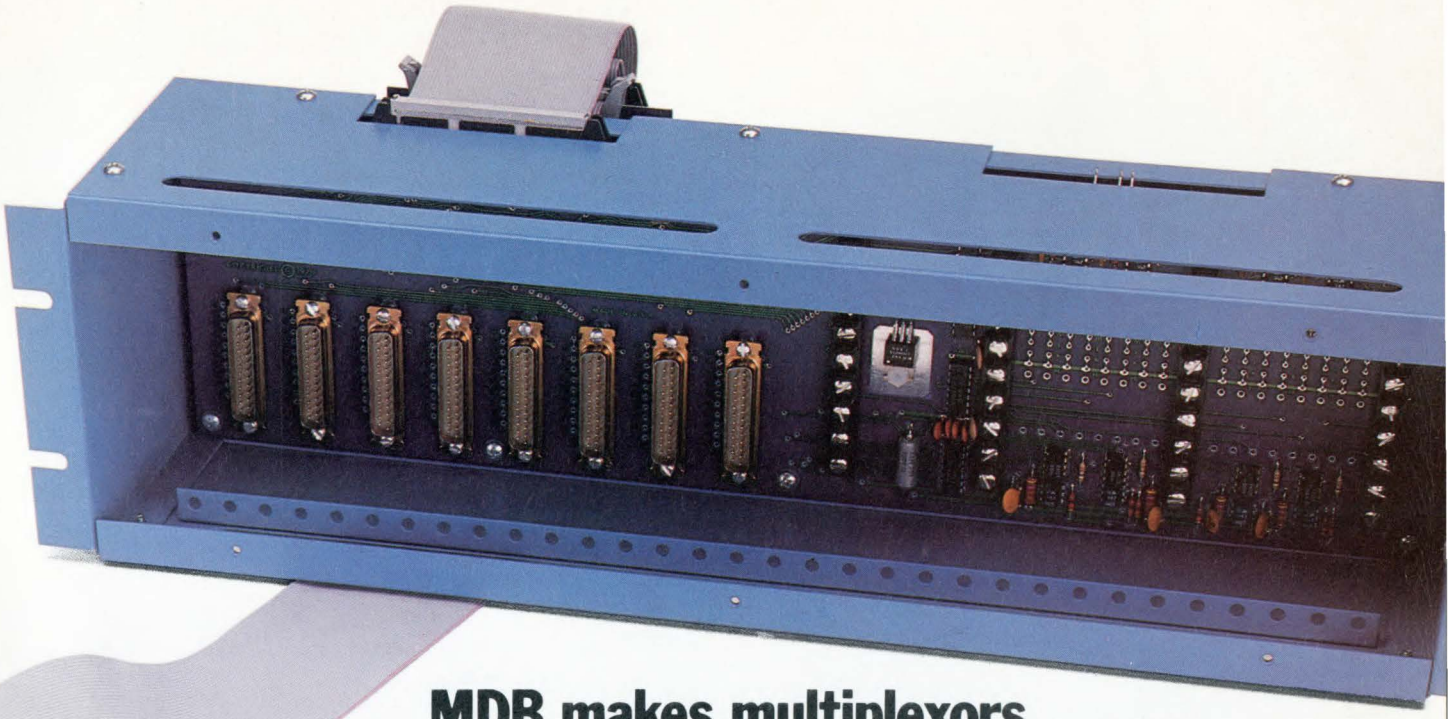
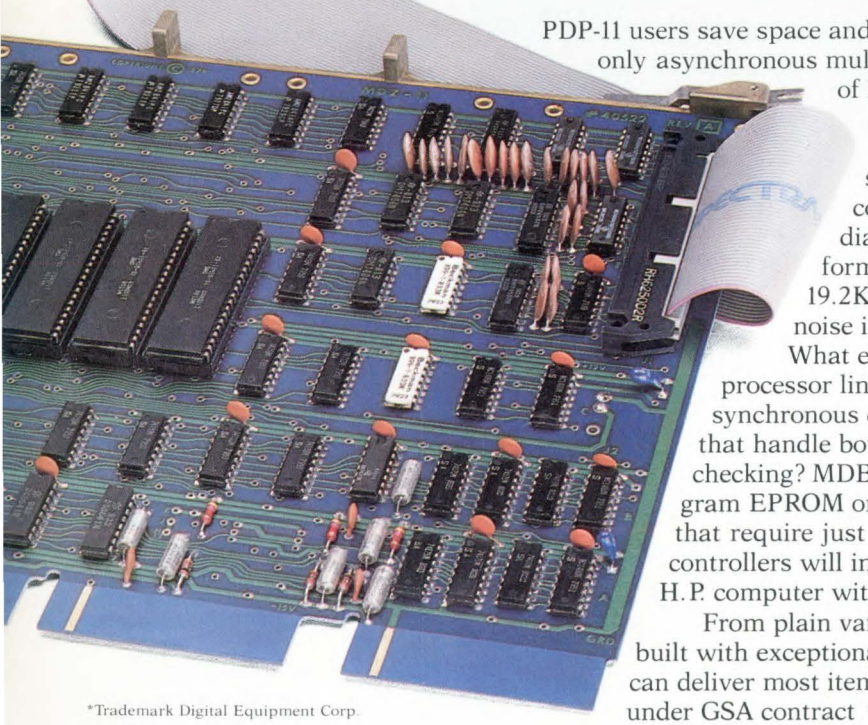


MDB makes multiplexors for the PDP*-11 that let you combine RS232 and current loop on one board.

Imagine what else we can do!



PDP-11 users save space and save money! MDB's DZ11AC is the first and only asynchronous multiplexor that lets you combine up to eight lines of RS232 and current loop in any configuration on a single hex board. No more doubling up on boards, distribution boxes, rack spaces or price. The MDB DZ11AC is fully compatible with DEC DZ-11 operating and diagnostic software and, at the same time, performs at 16 standard data rates from 50 to 19.2K baud with optical isolation for enhanced noise immunity.

What else can MDB do? Have you seen our interprocessor links for LSI*-11 as well as PDP-11? Or MDB's synchronous communications interfaces for Q-Bus* that handle both bit and byte oriented protocols and error checking? MDB makes PROM modules that let you program EPROM on the board and foundation modules that require just one card slot. Our famous line printer controllers will interface your DEC, DG, P-E, IBM Series/1 or H.P. computer with most of the major line printers in the world.

From plain vanilla to state-of-the-art, all MDB products are built with exceptional quality. We warranty them for one year, can deliver most items in 30 days or less and offer them under GSA contract #GS-00C-02423.

Call or write and tell us what we can do for you.

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Orange, California 92665
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Circle 60 for PDP-11, 61 for LSI-11, 62 for DG, 63 for P-E, 64 for IBM.

Complete systems for computer graphics and image processing.

And, we do mean complete! Grinnell systems can include computers, disc drives, terminals and software operating systems. Plus a FORTRAN software and driver package; high resolution TV monitor, camera, and hard copy color printer.

There are also other options to meet any special requirement you might have.

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GMR 260 Series: 1024 x 1024 resolution frame buffers for grey scale, black and white, pseudo color and full color.

GMR 27 Series: High speed, modular graphic and image display systems.

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So, whether you want to analyze images from outer space or monitor a process in a plant, Grinnell has a complete system that can do it. For complete specifications and/or a quotation, call or write today.

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Digital Design

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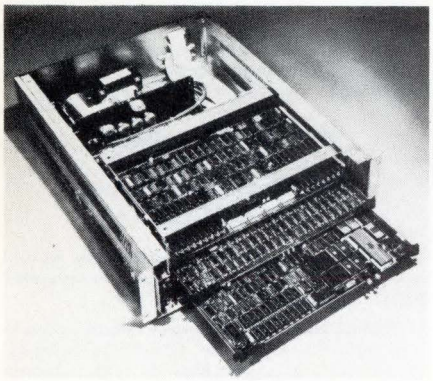
ON OUR COVER

Continued evolution, elimination of earlier trade-offs and extension of capabilities in microprocessor development systems offer designers and integrators improved procedures. (Photo courtesy of Tektronix.)



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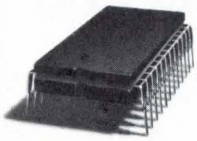

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the semi-custom IC.

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Letters

IBM Invades WP

Dear Editor:

Technology Trends "IBM Invades Word Processing Markets" (August) was an excellent review of the impact of future IBM products upon low-cost (stand-alone) terminals. Could you provide more details on competitive units?

Heinz Gabloffsky
CE & A, Inc.
Tustin, CA

Memory Backup

Dear Editor:

On the design for battery backup of memory systems (June, pg. 94), the series-pass 2N2907 may be replaced by a 2N3765. This will lower the V_{CE} saturation drop. This will guarantee CMOS V_{CE} greater than 4.5 V if V_{CC} equals 5V.

A. Botton
Orsay-Cedex, France

Data Communication Protocols

Dear Editor:

Congratulations on the article Communicating Data With Protocols written by S. E. Traylor in the July issue. In spite of the extensive matter covered, it makes a welcome change from other Electronic and DP magazines as far as impartiality and technical explanations are concerned.

Wolfgate Wittmer
Digital Equipment Corp.

Data Interpretation

Dear Editor:

The article "New Frontiers in 3-D" by M. Prueitt in your June 1980 issue discloses much more than 3-D display techniques, since it states without qualification that "Physicians often prescribe the wrong treatment because they cannot properly interpret the mass of data supplied by modern medical tests." Where is the author's supporting data? We readers want to know quantitatively the effectiveness of modern medicine.

S. Harbaugh
Palm Bay, FL

Designers' Notebook

Dear Editor:

Your "Designers' Notebook" is quite useful to me. I have benefited from the wide variety of problem-solving techniques. Could you expand this section?

Walter Cates
Methods Research
Richards-Gebanr AF Base
Grandview, MO

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IP8500...MORE IMAGERY, MORE FEATURES, LESS COST

DeAnza's new IP8500 image processing and display system introduces a new concept in imagery . . . more for less

It just may be the most powerful system you've seen.

It has 16 memory controllers handling an unprecedented capacity of up to 16 512x512x8 bit image memories. Its array processor easily handles 8 and 16 bit data with 32 bit results including real-time multipliers with 8 bit inputs and 16 bit outputs.

The IP8500 has up to four independent output channels with split screen capability, multiple look-up tables and 8 bit DACs for 256 levels of intensity for each primary color on a RGB color monitor or three separate mono monitors. It also provides high speed warp and rotation with anti-aliasing of a 512x512x8 bit image for warp/-distortion correction or image manipulation.

Features also include independent integer zoom of 2:1, 3:1, 4:1, 5:1, 6:1, 7:1, 8:1; pan feedback intensity translation tables, four independent alphanumeric overlays and dual cursor generators as well as high speed vector and special function generators.

If you're responsible for LANDSAT analysis, NDT, process control synthesis, remote sensing, three-dimensional computer graphics or other image processing and analysis applications which call for single or multi-station high resolution color, multi-image mono or pseudo color displays, find out more about the new DeAnza IP8500.

Call or write today and find out why more is suddenly less.

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Circle 9 on Reader Inquiry Card

Speakout

Paul Snigier, *Editor*

The Other Side

Reformers have been kicking the age discrimination and alien EE football around lately. But it's time to look at the other side.

First, it isn't necessarily age discrimination – that is, fire the older (over 40) engineer and replace him with two new graduates. Too often the fault is with the older EE for allowing himself to grow obsolete. Second, those engineers in backwater-technology industries, such as the appliance industry with its recent mass layoffs, are experts on relays, rotary cam timers, stepper switches, SN7400 logic and less needed skills. It's not age discrimination – just discrimination against older, fading technologies.

With the shortage of qualified EEs, industry is forced to hire more alien EEs, and I notice that more of them are rising into high engineering positions. By 1988, at this rate, one-third of U.S. EEs will be aliens. It's inevitable, so shouldn't American EEs welcome more alien EEs? They will improve American productivity and motivate native-born EEs. Alien EEs are often more knowledgeable and motivated than many U S. counterparts. They have reason to be, as U.S. firms try to hire only the best. Alien EEs or students will do anything to get into the U.S., and you would, too, to escape the incredible poverty, being drafted (sometimes into a shooting war) and other overseas troubles. Many will do anything to get into U.S. universities, which I have learned through conversations with such students, and have been asked to recommend universities.

Can we do anything in the way of reform, as advocated by reformers like Irwin Feerst? Probably not: rapid change and obsolescence are risks of our chosen field. For this reason, I am also opposed to engineering unions or job security for EEs. Sure, doctors, chiropractors, lawyers and dentists all have strong professional groups that limit entry into their fields so they can boost their own salaries. But our country has suffered for this – a situation we don't want in engineering. True, Teamsters have tremendous benefits and job security; but truck driving hasn't changed that much in the past five years, has it? Nor has medicine or lawyering. Nor has plumbing or carpentry. Forming professional unions, banning so-called "age discrimination" and limiting aliens may benefit the job security of American EEs, but the result will be the ultimate strangling of American technology. Industry must have the freedom to prune those who don't keep up.

Perhaps reforms will occur one day, and maybe some of them are good. But, in the meantime, what about your personal survival? You're on your own. What should you do to avoid becoming another victim? Take several precautions.

To avoid obsolescence, EEs are increasingly moving to new firms when they no longer can learn more where they are. In fact, many firms that once wouldn't look at a "job jumper" prefer them today; it's an indication that the man may have broad experience and skills. Other EEs maneuver to get increased experience by expanding their box sideways rather than climb the corporate ladder. They volunteer to assist others in certain jobs to aid their own marketability; they realize there's no incentive for a wise employer to train any EE beyond his present job function (or risk losing him). Both approaches make sense.

But you must do more. First, purchase the best computer books. The price is steep, and the books grow obsolete quickly, but it's worth it. To solve buyer resistance to increasing prices, some book publishers I've talked to say that they will reduce book sizes. A recent Z8000 paperback ($16) contains under 300 pages, yet the firm's earlier Z80 paperback had 35% more pages (yet cost less). So, books have their place, although they cannot keep up with the latest developments and can strain your budget. Here's where the trade press publications such as *Digital Design* and others come in, offering news, cookbook circuits and subroutines, new product information and technical articles that no paperback can offer. Take advantage of this free offer. **If you're a subscriber, you must fill out the requalification card.** If the card is missing, call our Circulation Dept. at 617/232-5470.

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Third, study one hour each day. If you're too tired at the end of the day, then arise one hour earlier.

Fourth, attend seminars. Most are in the $300 to $800 range, so get your firm to foot the bill. Some are excellent, a few are disorganized, and others are "me too" imitations of the more successful ones. Despite what the folders say, try to review the subject before attending for maximum benefit, since seminar material is extensive. Our sister publications *Electronics Test* and *Circuits Manufacturing* sponsor industry-leading seminars, shows and conferences in ATE, testing and PCB fabrication, so you or a colleague may want to call them (617/232-5470) for literature and listings.

Finally, to maximize your marketability, combine two or three fields in a unique and valuable complimentary combination. For example, firms want software/hardware EEs with mechanical packaging skills, advertising personnel with a solid background in publishing and electronics/computers, and EEs skilled in construction and micros with an understanding of energy management. Any such EE is very rare and can name his price. Complaining about aliens or "age discrimination" isn't the answer. Harder work is the solution. If you're willing to pay the price, you can join them.

Technology Trends

VERSAmodule System Expands 68000 family

Some mature micro families are at the end of their life; others, with superior architectures and greater inter-family cohesiveness, are rising stars. The ambitious 68000 will keep designers going well into this decade. A single-board, 68000-based μP, plus chassis, card cage, and realtime multitasking system software package are initial members of the "VERSAmodule" series of board-level products. The 8 MHz VERSAmodule System is related to the VERSAbus which Motorola is supporting as an industry-standard bus for high-performance 16- and 32-bit micros.

The VERSAmodule Monoboard μC (VMM), a complete μC system on a board, is said to be the most powerful 16-bit monoboard μC yet announced. When packaged with the VERSAmodule chassis and the Realtime Multitasking System Software, the VERSAmodule Monoboard Microcomputer provides a total environment for powerful 16-bit applications, thereby freeing the system designer to concentrate on I/O hardware and application software.

VMM is to be the "flagship" of Motorola's VERSAmodule product family. With the combination of its MC68000, a full VERSAbus interface, "System Controller" functionality, substantial ROM and RAM, plus serial I/O, parallel I/O, and timer/counter functions, this product is probably the most powerful 16-bit μC module yet offered. This provides a lower-cost μC system of given functionality and performance. For applications requiring up to 128 kbytes of ROM and RAM, plus two high-speed serial channels (up to 19.2 kbaud) and up to 32 lines of writing, application board products from other 16-bit micro vendors require two to four board for this capability.

Many 16-bit applications, particularly in higher performance control-oriented areas, require a realtime multitasking environment for efficient operation. But, by applying the ready-made VERSAmodule Multitasking System Software package, the user can save many man-months of effort that would otherwise be spent designing, coding and checking out the sophisticated task control algorithms necessary to manage system resources efficiently in real time.

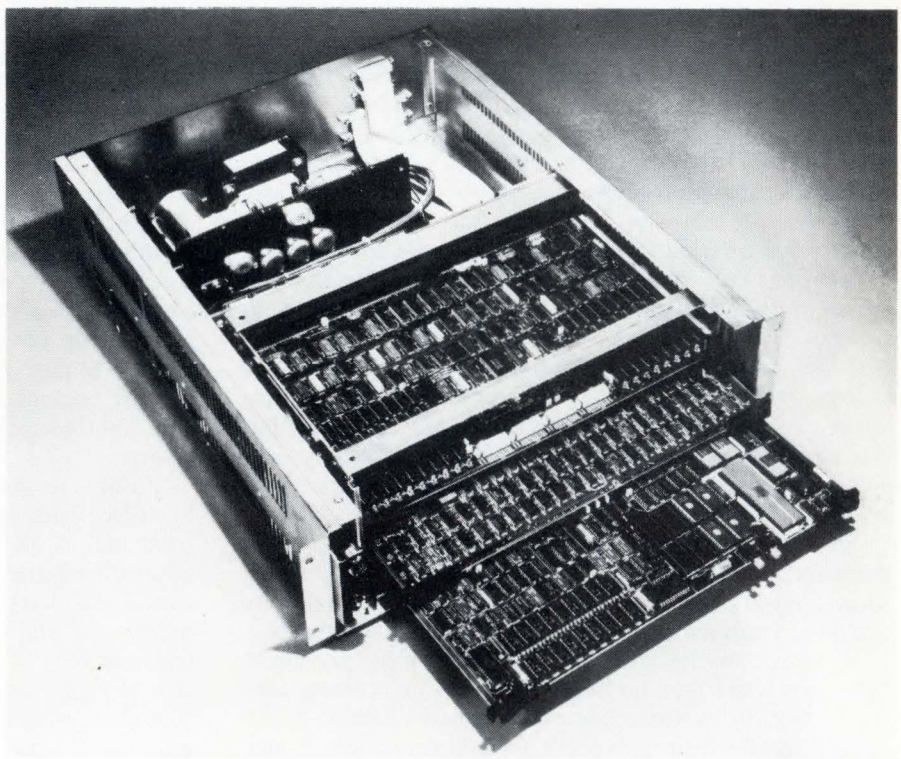
The combination of the VMM and Realtime Multitasking System Software, together provide hardware and software environment for sophisticated realtime applications in industrial automation and laboratory automation.

Multiprocessing and reliability

Often at the front end of a design activity, you must consider growth path if system performance requirements increase over time. The VERSAbus structure offers a graceful method to increase system performance by adding processor boards in a multi-processor configuration. The additional processor modules can be applied to share the processing load as performance requirements expand.

Boards, software and accessories were designed "from ground up" with advanced architectural features to support a high level of system reliability and maintainability.

Reliability-related design features are primarily in the area of "exception processing". "Exceptions" are unexpected events to which the processor must respond in a "graceful" fashion in order to maintain system integrity. Exceptions are recognized by way of processor interrupts. The MC68000 can recognize the following exception conditions individually and switch to a processing routine designed by the user to respond to that specific exception condition: bus error, illegal instruction, divide-by-zero, privilege violation, spurious interrupt and so on.



VERSAmodule 4-slot chassis, with top removed, showing Card Cage and 15-A Power Supply. VERSAmodules shown are (frem bottom slot up) monoboard microcomputer, floppy disk controller and 128-k dynamic RAM.

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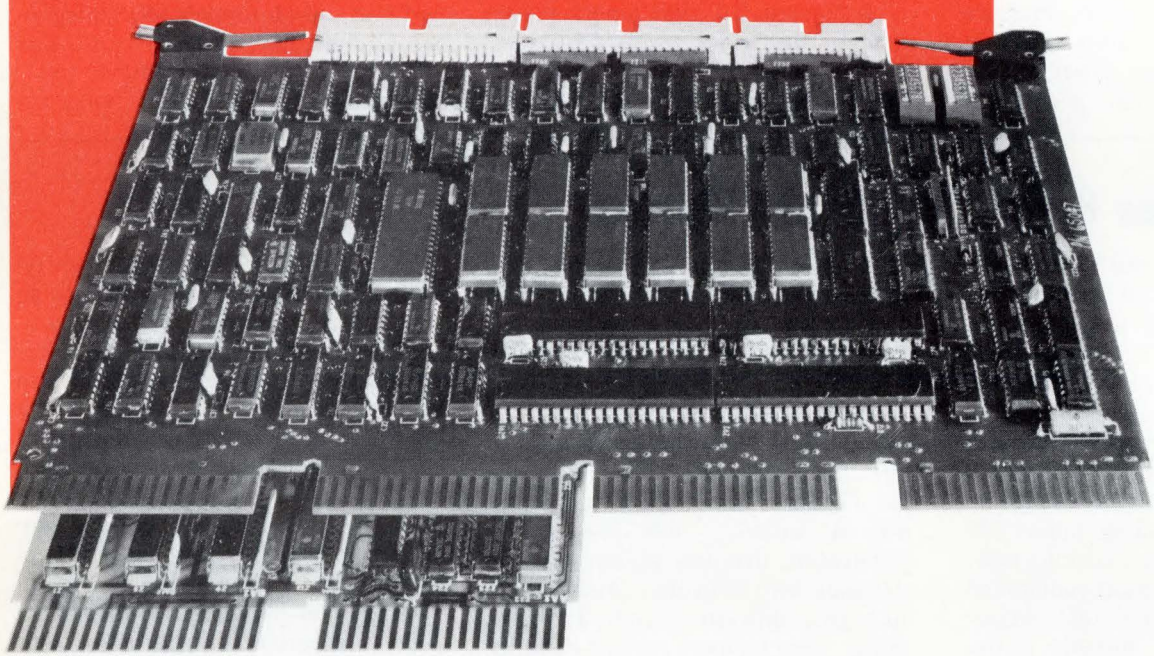

Get more from your LSI-11 and PDP-11 by putting less into it! It's possible, with Dataram's dual-density DEC®-compatible tape controllers that offer an amazingly efficient packaging approach.

For NRZI operation (LSI-11 or PDP-11), a single quad board from Dataram is all that's needed. For phase encoded mode, the simple addition of the dual-size PE board, anywhere in the LSI-11 or PDP-11 backplane, makes it possible. Packaging flexibility that allows you to optimize your DEC configuration.

Dataram's T03/T04/T34 family, summarized in the chart below, offers the widest array of DEC-compatible tape controllers available today.

The T04/T34 controllers, utilizing an integral 16-bit bipolar microprocessor, provide speed capability to handle up to 1600 BPI at 125ips. And they require only +5.0VDC.

Less power. Less space. Less cost. That's a lot of less...and it adds up to more performance for your DEC-based system. From Dataram.

	NRZI		PE
LSI-11	T03	2 DUALS	T04 1 QUAD and 1 DUAL
	T04	1 QUAD	
PDP-11	T34	1 QUAD	T34 1 QUAD and 1 DUAL

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With the ability to differentiate between a wide variety of fault conditions, you can develop a wider variety of appropriate system responses to faults. The system exhibits a wider latitude for "failing softly" while being able to alert maintenance personnel that attention is needed, in many cases even before the critical failure point is reached.

Maintainability

Two lines related to system power failure are included: "AC Fail" and "Power Down". Normally, these lines are driven by AC power failure detection circuitry in the system power supply. Any board which can perform a "power fail" sequence, in order to preserve critical volatile data, monitors the "AC Fail" line in the bus to determine when a possible power failure is detected. Certain critical data can be saved through a period of power outage in non-volatile memory. I/O interfaces and external devices can be "cleaned up" (under application software control) in anticipation of the oncoming "down" condition.

Two system test-related lines exist. The "test" line is normally asserted by the "system controller" when a general system self-test is desired. Any "intelligent" module (board) which can perform a self-test function monitors this line and institutes a self-test procedure when it detects that the line is asserted.

A "System Fail" line reports the results of the self-diagnosis procedure. Any intelligent module which performs a self-test, and in so doing detects an internal failure, asserts the "System Fail" line at the test conclusion, signifying to the system controller module that a failure exists at some location in the system so that maintenance personnel can be alerted or other appropriate action taken. A display light (and supporting internal circuitry) at the top board edge remains illuminated at the conclusion of the self-test sequence if a fault is detected.

Users won't be antagonized since system down-time is minimized, since maintenance personnel manually initiate a self-test on a system where a problem is suspected, and visually detect a failed board through the illuminated "failure" light at the top board edge.

If you want more information, write or call Motorola's MOS Integrated Circuits Div., Microsystems, Box 20912, Phoenix, AZ 85036, (602) 244-5720. **Circle 212**

6805 Invades 8-bit CMOS μP Market

Motorola is about to make big inroads into the 8-bit CMOS μP market with its newly announced and expanding 1-MHz MC14 6805E2 family. The 61 basic instructions are similar to the MC6800, plus a complete set of bit-manipulation instructions to allow any bit in RAM or any I/O pin to be individually set or cleared with a single instruction. Low operating power (20 mW at 3-6 V) and lower standby power (1mW) consumption cut cooling and power supply costs and offer higher noise immunity for portable instruments, telecommunications, POS terminals and appliance controllers.

On-chip functions include an 8-bit timer with software programmable 7-bit prescaler, 112 bytes of RAM and a clock generator. The multiplexed bus has an 8 kbyte addressing range. A 2 kbyte CMOS ROM, the MCM65516, is a companion part (now available). The MOTEL (Motorola/ Intel) circuit detects if a Motorola or Intel μP is connected and properly interprets bus control signals automatically.

The 6805 is housed in 40-pin cerdip or plastic ($45) package. Delivery is off-the-shelf.

Other recent CMOS entries include NEC Microcomputers' single-chip μPD80C48, which draws a scant 10 mA at 6 MHz, unlike Intel's three new HMOS micros, including its 3-MHz 8048L (which draws 40 mA, or four times more current). NEC's Halt instruction can reduce its 10 mA down to 1 mA; or for even lower power consumption, a stop mode exists. For development work, NEC will introduce a ROMless μPD80C35 and EPROM 87C48.

The 6805 promises significant impact on the OEM market/design scene. First, the expanding 6800 family will put heat on Intel, which is saddled with an ancient – but time-tried – architecture that has proven expandable only with difficulty. (And at that, must go in different directions; for example, some industry pundits claim its 8086 bears small resemblance to its predecessor). Second, RCA's long-protected 1802 family comes under further attack with this product entry; overall, the 6805 may be more than an 1802-killer: it may – repeat, may – signal a declining market share for RCA. More designers are likely to commit themselves to a popular family that can expand upward, downward and laterally. OEMs are now tied into tons of support software, costly (and too-often dedicated) systems and proliferating support chips, and second sources. So, to swap horses – or micro families – in the middle of the stream loses momentum for your firm. With the popularity of the loosely-coupled 6800 family behind it, the 6805 promises to become a major force.

Data General Launches Intelligent Workstation Family

The MPT family of microNOVA-based intelligent workstations, MPT/80, 83 and 87, offers a full 16-bit μC, 60 kbytes of local memory and up to 716 kbytes of mini-diskette storage in a compact desktop keyboard/display unit.

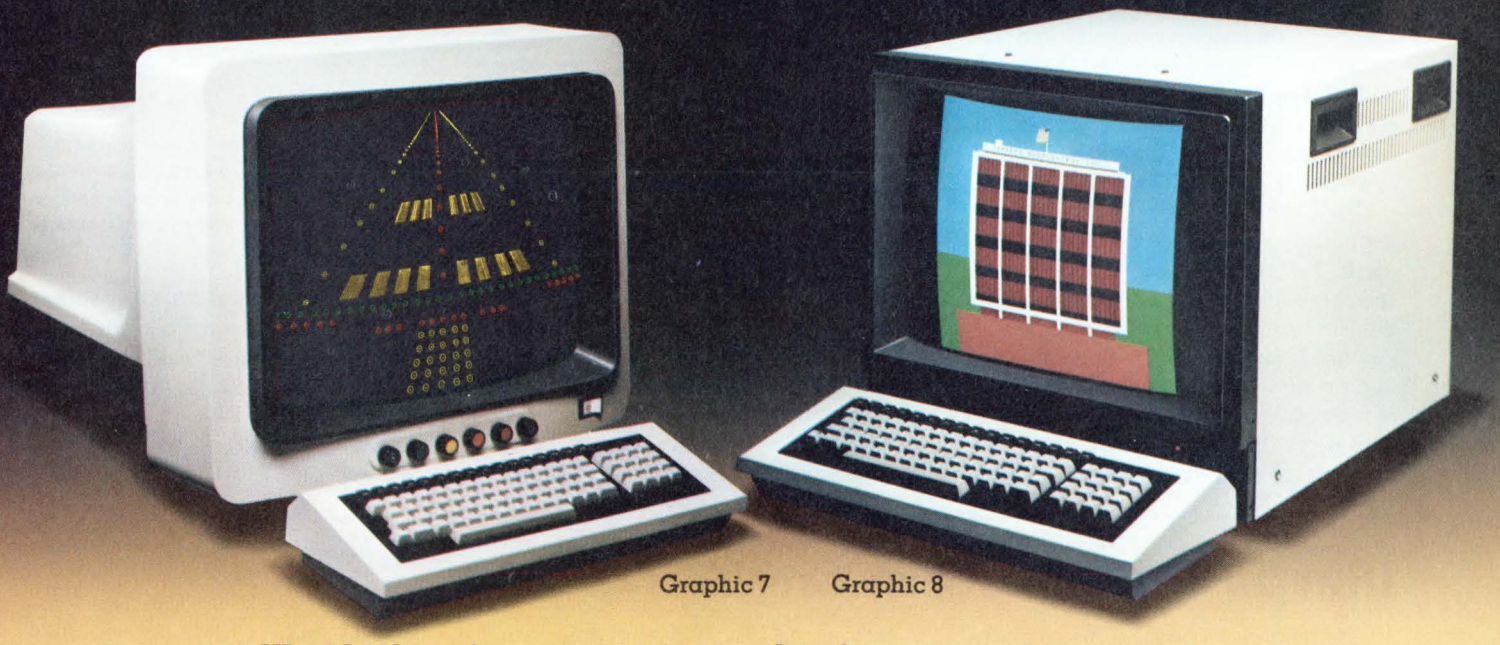
They provide software compatibility with DG processors from the 16-bit microNOVA to the 32-bit MV/8000.

This compatibility gives OEMs a competitive advantage: they are free to develop stand-alone or communications-based applications using any DG CPU. OEMs and end users can write Pascal, Fortran IV or assembly language software for the MPT workstations on DG host systems. Users then customize MPT stations by loading this software for execution; after loading, programs are executed with reduced host overhead.

MPT workstation intelligence and memory allow users to capture and validate data without tapping host system resources. Local files are maintained independently. Local error checking further cuts host overhead and assures "cleaner" data.

Applications for MPT intelligent workstations include OEM-designed distributed processing networks, in-

THE BEST OF BOTH WORLDS: STROKE AND RASTER.



Graphic 7 Graphic 8

Want high performance raster graphics?

Sanders Associates' new Graphic 8 offers you up to 256 simultaneous colors. High resolution. Dynamic operation with double-buffered refresh memory...

Plus upward-instruction compatibility with the Sanders stroke refresh Graphic 7 and its color and 3D options.

But there's more.

Both display systems – Graphic 7 and Graphic 8 – bring you built-in test, FORTRAN support, remote or local operation, interfaces to most computers, and other important user-oriented features.

Sanders' stroke refresh Graphic 7 and new raster Graphic 8 display systems: they put the best of both worlds at your fingertips. For more information, write or phone Sanders Associates, Inc., Information Products Division, Daniel Webster Highway South, Nashua, NH 03061. 603-885-5280.

The Graphics People

SANDERS

Circle 12 on Reader Inquiry Card

dustrial data collection, sensor I/O handling, lab and educational data processing.

The one-piece housing integrates a 12″ video screen, 83-key keyboard, and (when included) 5.25″ floppy diskette storage in one 22″ W by 12″ H by 20″ D 30-lb. cabinet.

For applications requiring no diskette storage, the MPT/80 terminal offers 60 kbytes of dynamic RAM. Where limited on-line storage is cost-acceptable, MPT/83 workstations add one 358-kbyte dual-sided double-density minifloppy drive. Larger storage needs are met by the MPT/87, with 716 kbytes on two integral minifloppy drives, in addition to 60 kbytes of RAM.

A 25-line by 80-character video display features adjustable brightness, blinking, underscore, normal and reverse video, and block-fill fields. In addition to the full 96-character ASCII set, available ROM-based international fonts include British, Swedish, French, German, Spanish and Danish.

Each MPT station includes a built-in keyboard, a 14-key cursor control/numeric keypad, and 10 user-definable special function keys. Solid-state capacitance switches eliminate mechanical key linkages, providing high reliability.

The MPT workstation's single-board construction reduces faults. If repair is necessary, the one-piece top enclosure lifts out of the way on hinge mounts to provide easy access to the keyboard mechanism, CRT and circuitry. The system's self-diagnostic messages will quickly guide repair personnel directly to most faults.

Data General Corporation's MPT family of intelligent workstations can be used in stand-alone or communications-based applications incorporating host central processors ranging from the 16-bit microNOVA™ to the 32-bit ECLIPSE® MV/8000. MPT/80, /83, and /87 workstations include a full 16-bit μC, 60 kbytes of local memory and up to 716 kbytes of mini-diskettes storage – all in one compact keyboard/display unit.

MPT/80, w/o integral mini-diskette storage, $4800; MPT/83, with one integral 358 kbyte mini-diskette, $6000; MPT/87, with two integral 358 kbyte mini-diskettes, for a total of 716 kbytes on mini-diskette, $7100. Delivery 90 days ARO.

Data General, Rte. 9, Westboro, MA 01581. 617/366-8911. **Circle 211**

IBM To Expand In Color Graphics

In the next five years, and particularly 1982-1983, IBM's 3279 Color Display Station will hit hard. The IBM 3270 and 3270-like PCM display markets will grow dramatically. Worldwide shipments of 3270 and 3270-like inquiry/update displays will rise from 739,000 in 1979 to nearly 2.3 million in 1984, an annual growth rate of 25% and dollar volume growth at 30%, compounded annually. This higher revenue growth will be the result of a continual rise in general pricing due to value-added features. Color and graphics will be the most significant variables relative to high value-added pricing.

Worldwide shipments are expected to see a compound annual growth rate exceeding 133%. IBM will dominate the marketplace but competition will be stiff, especially for the U.S. market segment.

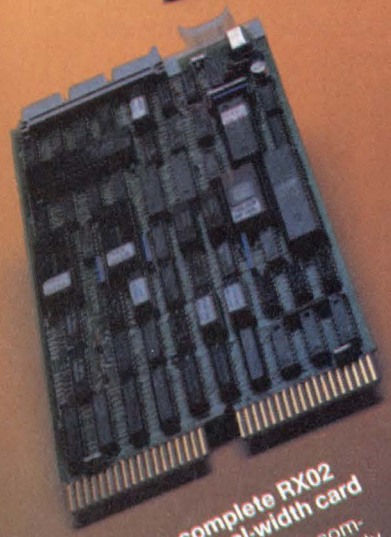
Increased operator/user efficiency

One big fly-in-the-ointment that will affect color graphic sales is the usual factor – cost. Many large end users are already smart enough to recognize that ease and speed of interpreting and understanding complex data (with color graphics) increases operator efficiency and increases data throughput. The result? It's reduction in data entry costs, and it has already led many sophisticated customers to place orders for the 3279.

Within the next two years, CSI (San Jose, CA) predicts IBM will introduce 3279-compatible color-graphics printers; color-graphics plotters and a stand-alone color-graphics workstation cluster. Innovative software enhancers will open up vast new applications areas – IBM database management system and data dictionary support features for color graphics and software items.

Will IBM go unchallenged? Not likely. Major new entrants in the business color-graphics marketplace will include a wide variety of non-traditional PCM vendors such as the scientific color-graphics software and service houses. These firms have a big edge over vendors of monochromatic displays – they have previous experience with sophisticated color-graphics.

DEC COMPATIBILITY

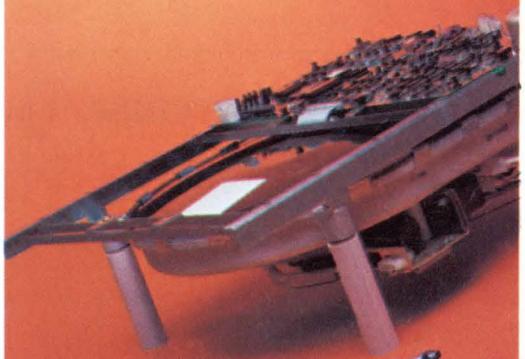


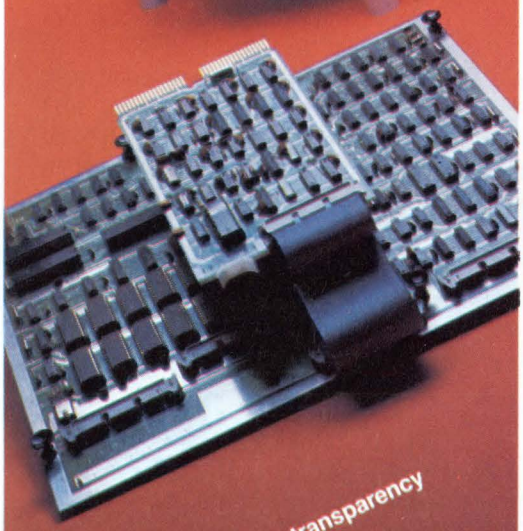
FLEX 02 offers complete RX02 emulation on one dual-width card

Media compatible and software compatible, the FLEX 02 card plugs directly into your LSI-11, 11/2 or 11/23. This low-priced controller has built-in bootstrap; handles single or dual-head floppy disk drives. Order now for 30-day delivery!

Circle 76

DEC COMPATIBILITY





WINC 01 offers RL01 transparency for Winchester-type drives

Software transparent to RL01 driver, WINC 01 maps the data of three RL01 cartridges (15.6 MBs) on one Winchester. Dual-width interface card plugs into LSI-11, 11/2 or 11/23; low-cost controller mounts onto Marksman drive. Call today, they're going fast!

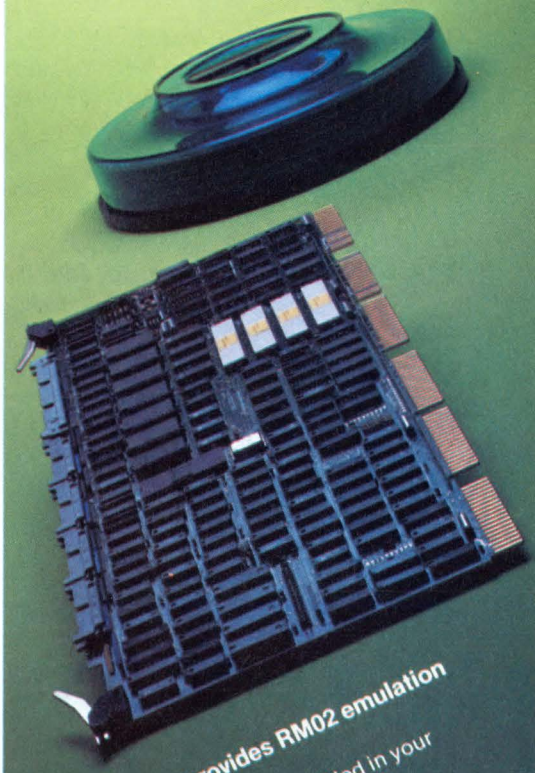
Advanced Electronics Design
440 Potrero Ave., Sunnyvale
CA 94086. 408-733-3555

Boston 617-275-6400
Los Angeles 213-705-0379
U.K. 44 256 61551
France (1)724 19 54
W. Germany 040-310824
Holland (070)46 95 09
Switzerland (022)32 97 20
India 79281
Japan 03-437-5471
Australia (02)438 2444
New Zealand 499 197

FROM AED

Circle 77

DEC COMPATIBILITY



STORM 02 provides RM02 emulation for PDP-11 users

This single hex card, embedded in your PDP-11, runs under standard RM02 drivers. STORM 02 accommodates up to four 80 MB storage module drives and provides disk pack interchangeability with DEC. 30-day delivery and quantity discounts!

Circle 78

Innovative Design

8" Disks "To Go" Overcome The Elements

The problem with Winnies is that they don't travel. Because of their sensitive nature – the slightest surface defect or contaminant can render them useless – they're destined to remain in protective custody, within the drive chamber, for life.

That is, of course, until now. CDI and Memorex have each developed removable 8" rigid disk cartridges: hard disks cleverly packed into cases that keep out the elements, yet expose the disks when they're safely inside the drive.

Eliminating contamination is the main problem in designing these cartridges, according to Drew Berding of Memorex Mini Disc Drive Corp. In developing the Memorex 2001 cartridge, the ounce of prevention tack was taken – engineers knew that keeping the cartridge interior free of contamination would be easier than flushing out contamination already inside.

Two entrances exist in any cartridge through which particles may enter. These are the two areas where drive and cartridge mechanisms interact: the disk hub, which must interconnect with the drive spindle, and the doors that allow the Read/Write heads access to the disk.

At the hub, designers chose a seal which would remain locked despite pressure applied against the hub. When in use, the cartridge case presses against a fixed ring, releasing the hub seal. This, in turn, frees the hub to rotate without drag.

Between the outer, square cartridge case and a round, inner seal protecting the disk lies the cartridge door mechanism. Two .02" thick actuator probes projecting from the disk drive mechanically interact with this mechanism through twin holes in the cartridge outer case (**fig 1**), unlocking and pulling open the sliding doors as the cartridge is inserted into the drive. When the cartridge is pulled out, the mechanism closes and secures the overlapping doors. Once locked, the doors "resist even the most determined effort" to open them, according to Memorex.

(Continued on pg. 19)

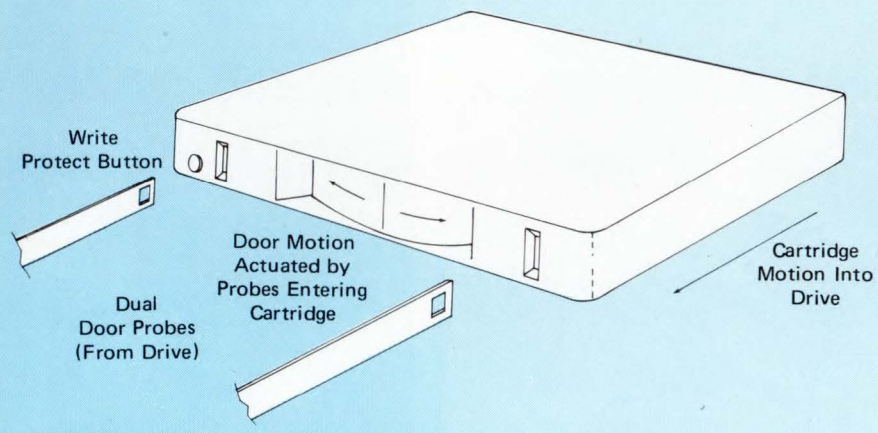


Fig. 1 The cartridge engages the dual door probes as it enters the cartridge receiver. The probes unlock, and slide the doors around the inner seal.

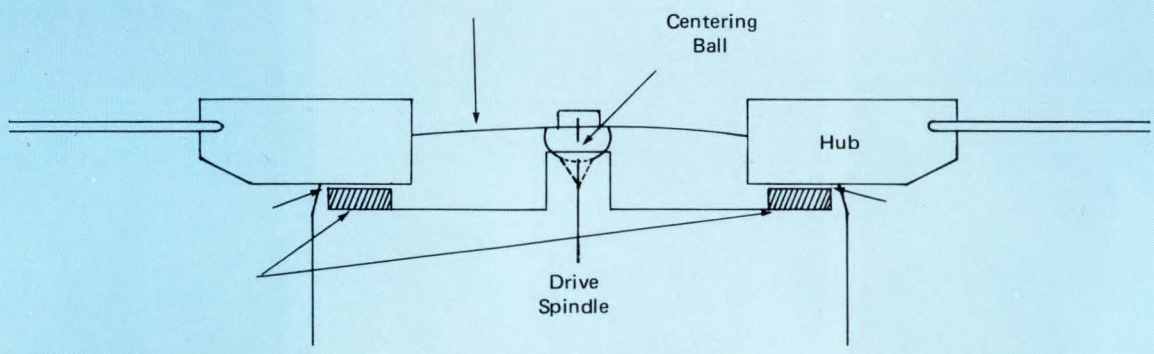


Fig. 2 Cartridge disk centering on drive spindle shows how the centering ball operates independently of the diapghram deflection to register the disk (concentric to the spindle).

MAKE YOUR DUMB TERMINAL SMART.

Teach it to talk back. The SLC-1 Time Machine replies instantly to requests from your computer. It automatically tells it the date and time, enters log-in codes, gives any responses you specify. No changes are required in your operating system. Simply install it in the RS-232 or 20mA current loop serial link that connects your computer and terminal.

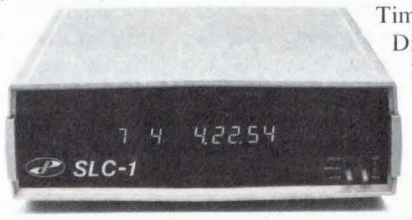
No more operator response errors. No more delays. Now you can automatically re-boot your system after power failure.

Whether you use your computer for business, research, or process control, the Time Machine will save you money. In fact, the first time it prevents a human error, it will more than pay for itself.

The Time Machine doesn't interfere with your computer's operation. It steps in and responds only when it sees the key phrases you have specified. And because it's battery-supported, it never misses a beat or a bit.

The Time Machine comes with a built-in bonus: it is also an independent microprocessor system. Its 1,000 bytes of RAM (expandable to 12K) lets you use it in the off-line mode to free your computer for other tasks. Applications support is available, including a growing 6502 machine language software library.

For more information or literature on the SLC-1 Time Machine, contact Digital Pathways, Inc., 1260 L'Avenida, Mountain View, California 94043, or phone (415) 969-7600.



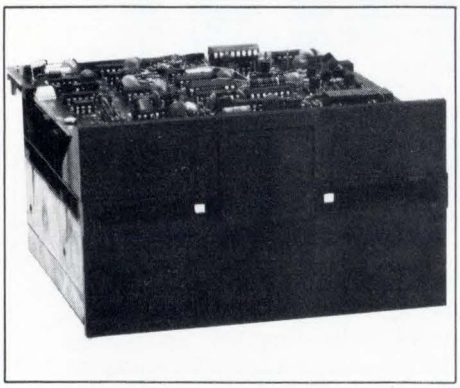
GET INTO THE TIME MACHINE.

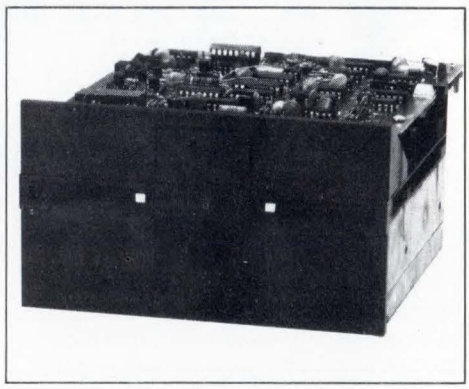
DIGITAL PATHWAYS

Circle 14 on Reader Inquiry Card

GO FIRST CLASS

½ MByte
TM-100-3 (Single-sided)
Capacity (unformatted):
500K bytes
TPI: 96 or 100
Tracks per side:
80 maximum
Recording density:
5535 BPI
Access time:
• Track to track: 3ms
• Average: 90 ms





1 MByte
TM-100-4 (Double-sided)
Capacity (unformatted):
1,000K bytes
TPI: 96 or 100
Tracks per side:
160 maximum
Recording density:
5877 BPI
Access time:
• Track to track: 3 ms
• Average: 90 ms

At an economy Price

It doesn't cost anymore to go first class when it's a Tandon 5¼" flexible disk drive. The reason is simple. We're the recognized leader in mini-floppy read/write head technology. In fact, our patented, double-sided head design is used by all the other major mini-floppy suppliers. And, it makes no difference if you buy one or one-thousand drives, you'll always get the first class price/performance that's made Tandon first choice among OEMs of word processing, small business systems, and personal computers. Tandon is rapidly becoming the first name in mini-floppies because we offer up to *one megabyte* of storage capacity, the fastest access time, a choice of single or double-sided recording, and 96 or 100 tracks per inch. All with proven reliability at an unbeatable price. Because we are the leaders in head technology, Tandon mini-floppies are designed beginning with the head to assure dependability throughout each drive. With Tandon, going first class is both sensible and economical.

Tandon

9333 Oso Ave.
Chatsworth, California 91311
(213) 993-6644

Heads Above The Rest in Disk Technology

Circle 15 on Reader Inquiry Card

Innovative Design

Why would someone be determined to break into your disk cartridge? "It's not that they're malicious," says Berding. "People are just curious. When I hand people cartridges, while they're talking to me they're trying to open the things up. It's like a challenge."

Should some contamination manage to infiltrate the inner casing, Memorex provides a second defense: a flow of clean air from the drive helps keep contamination away from of any perturbations in the surface of the diaphragm on which it is mounted. the disk (this air flow also helps stabilize disk temperature).

The other major difficulty with making disks portable is keeping disks centered each and every time they're plugged into the drive. In the 2001, Memorex built a centering ball into the cartridge disk center **(fig 2)**. When the cartridge is inserted into the drive, this ball slips into a cone-shaped opening in the drive spindle, keeping the disk centered.

Materials choice was another concern, since any substance prone to shedding would pose a serious contamination problem from *inside* the cartridge case. Polycarbonate was chosen for the case; Delrin plastic for the doors.

Several other companies are working on 8″ removable disk cartridge designs. However, for removable disks to garner a significant market share, an industry standard is necessary. In Berding's admittedly biased opinion, the 2001 could well become that standard.

–Bob Hirshon

Ribbon Inker Eliminates Skew Problem

Reinking can cause printer ribbon skew without proper edge alignment and skewing can prevent character imprint at extreme ribbon edges. For example, in a 132-column printer, a skewed ribbon could cause the printer to miss printing characters in column 1 or 132.

A new automatic ribbon reinker **(Fig 1)**, eliminates the problem of ribbon skew. Introduced by Compu-Rite Corp, Tarzana, CA, the reinker uses an optical alignment system to overcome skew.

Besides eliminating ribbon skew, the CR-170's patented variable metering system can ink 3-mil, 4-mil, as well as the more widely-used 5-mil ribbons. Also, since the ink application roller is immersed in the ink reservoir, it eliminates pumps and the possibility of clogging. The unit employs an electronic sensor to insure accurate reversing of the winding mechanism.

The CR-170 printer ribbon reprocessor reinks a ribbon in five minutes at a typical cost of less than one dollar. The manufacturer says that you may reink a ribbon at least three times and still maintain new ribbon quality and specifications. *– Loren Werner*

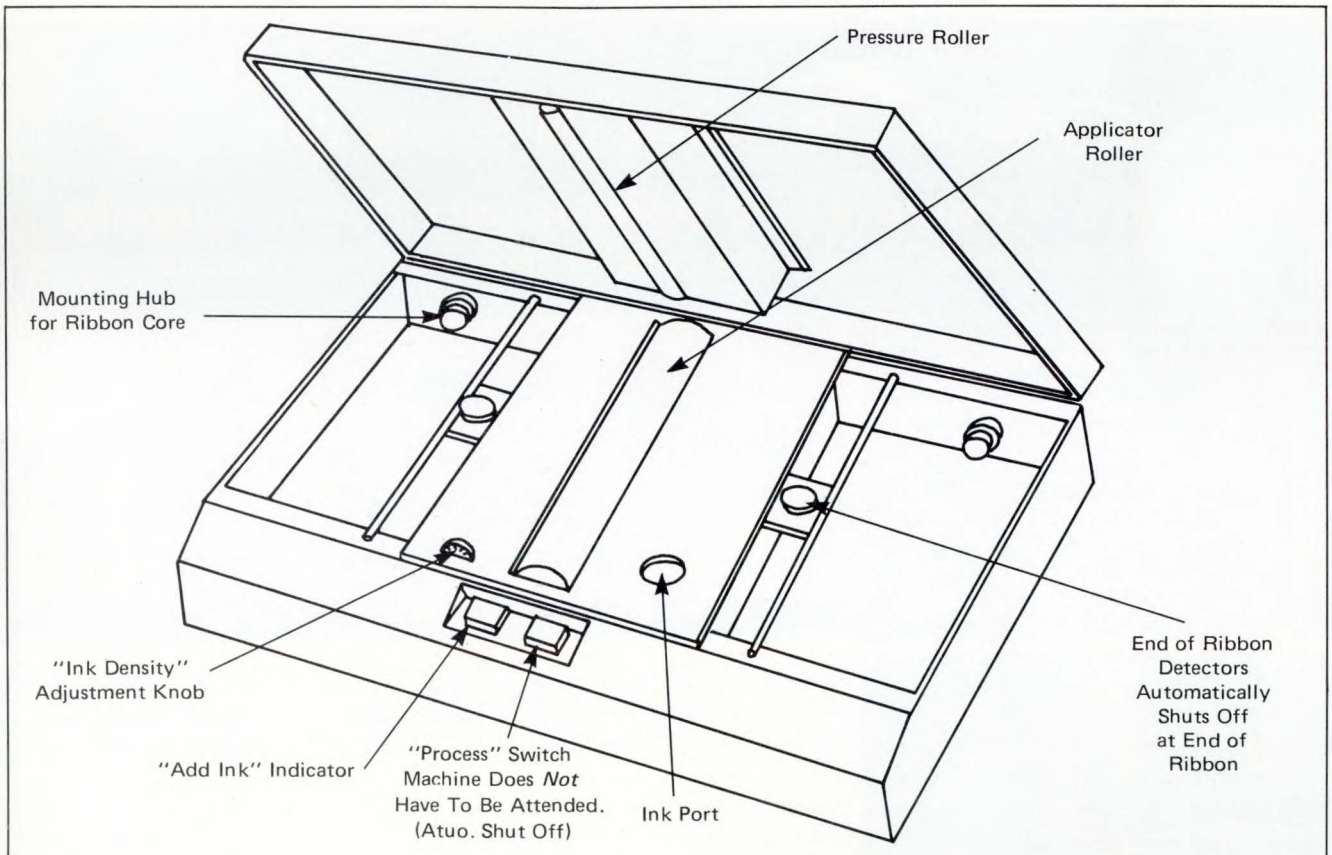


Fig 1 The CR-170 printer ribbon reprocessor operates automatically; the user simply loads the ribbon into the unit, and closes it. Once started, the unit automatically reinks the ribbon, rewinds it and turns itself off.

Innovative Design

Fail-Soft Mini Reconfigures Itself

Model 8000, a 32-bit virtual memory minicomputer, fails softly, automatically regenerates its operating system in less than 8 sec and supports hardware-independent programming. Key to this is its hardware, which its maker – BTI Computer Systems, Inc. – calls Variable Resource Architecture (VRA). BTI describes VRA as a "flexible mix of hardware resources controlled by a single self-regulating operating system." Performance varies over a tenfold range by using up to 8 CPUs. The system can access up to 8 MB of main memory and support up to 200 interactive terminals.

Although VRA is somewhat similar in concept to DEC's Unibus, Unibus operates at a 5 Mbps data transfer rate, whereas BTI's asynchronous bus operates at 60 Mbps, with a 67-ns bus cycle time. BTI claims the bus is fast enough to minimize bus contention and keep 8 CPUs going at or near full capacity. The passive hardwired bus is said to be immune to failure, short of physical damage.

Users configure their systems on the BTI 8000 by adding various hardware modules to its bus. These modules include CPUs, memory, peripheral processing units and a system service unit or SSU (which enhances system automation, reliability and security) to automatically generate the OS program. System start-up initiates automatic hardware module checking. If there has been a change since the previous start-up, the OS automatically reconfigures itself to match the hardware currently in use.

Automatic system generation plays a part in the 8000's fail-soft design. When the 8000 performs diagnostic self-testing during start-up, its control panel display identifies any malfunctioning module. Likewise, a module failing during operation stops the system, and the display indicates the malfunction source. Thus, users can replace the failed module with a spare and restart the system in a matter of minutes, without a service engineer. In multiple module systems, users can remove the failed module and restart the system without it. Automatic generation then adjusts the OS to the new hardware configuration.

VRA also makes the hardware user transparent. All CPU modules look alike to the applications programs. In fact, the OS uses a queue arrangement that swaps applications programs in and out as hardware resources become available. Several CPUs may each partially process a given application program, but only when the CPUs are fully functionally identical. Thus, programmers may develop their code for specific applications without worrying about present or future hardware configurations.

BTI 8000 supports COBOL, BASIC, FORTRAN 77 and PASCAL. Mass production will begin in January 1981.

– Loren Werner

Minicomputer:
System Element or Pile of Bits?

Scott Harris,
Computer Automation, Irvine, CA

"That looks like it was designed by an engineer" – we have all heard the phrase, and it's not a compliment. However, many of the things we praise are also designed by engineers. What's the difference ?

A digital design engineer can be a bit jockey or a system designer. The bit jockey thinks on the smallest level available and tries to squeeze bits out of a chip like a hotrod mechanic squeezing horsepower out of a crankshaft. The system designer implements a concept to produce a needed element. He implements a concept using bits – a concept which is part of a whole system just as an automobile engine is part of a transportation vehicle. Or, put in other terms, the bit jockey might be in the railroad business and conceive of everything in terms of trains, while the system designer recognizes that he is in the transportation business and sees that the solution should be made to fit the problem and not vice versa. When we bend the problem to fit the solution, nuts and bits stick out here and there and someone says, "That looks like it was designed by an engineer."

Solving larger problems

Hardware is unnecessary. Just as pieces of hardware can be created which have nothing to do with any system, so can systems be designed which contain no hardware. However, with the aid of today's technology, we are all attempting to find solutions to larger problems than we've tackled before. These solutions are large and are usually represented by a system using many people, procedures, and capabilities, It is important to recognize (1) that computers are elements or parts of systems which implement certain procedures and provide some capability and (2) that the existence of high-speed digital electronics has for the first time made some procedures feasible.

The point is that complete systems are often designed now before the lines are drawn as to what part is done by people, software, firmware, or hardware. Once a procedure is well understood, it can be automated and provided as a service for the people involved. In fact, the better a procedure is understood, the more it can be moved from the people toward the hardware. An analogy: my '23 model "T" required me to control the choke, spark, and gear from the driver's seat. My 1976 car provides all these as a service. Not only are good systems providing automatically a service which was done manually, they do it so that the user is unaware of it happening and so that it does not interfere with the user concentrating on his real problem – getting from one place to another.

Don't solve wrong problems

Let's use virtual memory as an example of solving the wrong problem. Frequently we are told to limit the scope of a problem to make it more solvable. But if we limit the scope prematurely before we perceive the entire problem, we may be solving the wrong problem. For example, we're all familiar with the idea that virtual memory may make it seem to a user that he has more memory for his own use. But have we considered that if virtual memory were well thought out, it might provide new capabilities to the user, simpler ways of using the system, or greater utilization and increased power for the same resources? Indeed, virtual memory could be only one facet of a storage management scheme which can make the system simpler and more efficient rather than more complex and clumsy.

Let's consider virtual memory itself. Many large computer systems keep only the active portion of a user's program in central memory while it is executing, to allow an increased size program or a larger quantity of programs to run in a fixed amount of central memory. Users may often share programs and files. Some systems also provide intersecting file and program spaces. Until recently, mimicomputers have not offered these advantages because they were considered too complex and expensive.

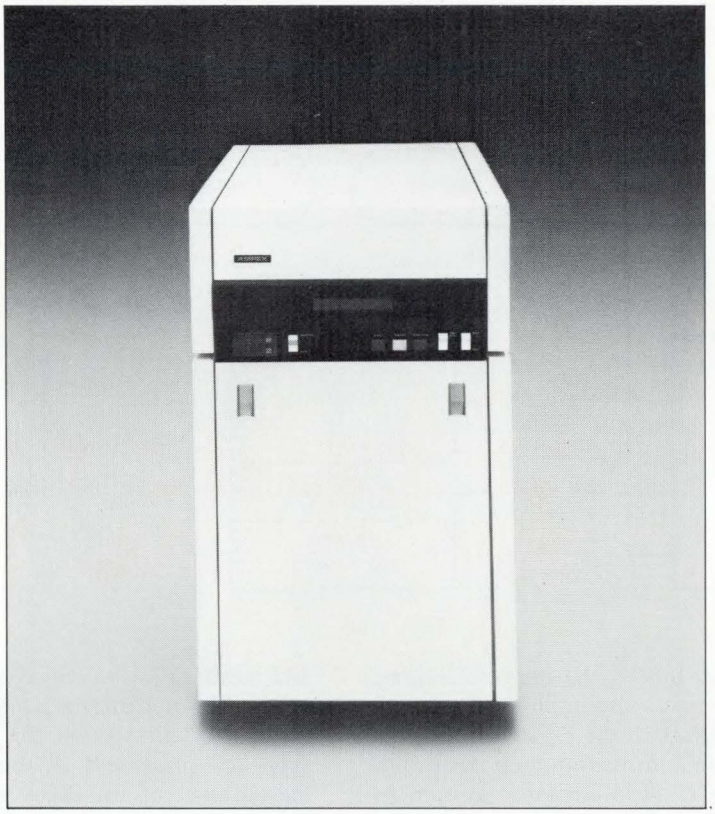
Typcially, two sorts of software are found on minis: (1) minicomputer software which has been enlarged, albeit with chewing gum and baling wire, and (2) mainframe software which has "filtered down" onto minis. The former shows low investment and design generally comes from mainframe software technology of ten or fifteen years ago. But with the advent of more advanced devices, denser circuitry and cheaper memory, the difference between minis and mainframes blurs and mainframe software technology appears on minis. With the implementation of virtual memory operating systems, minicomputers can provide the capabilities of mainframe systems.

Some definitions

"Virtual" is that address which a user program appears to see; "logical," that address which the CPU can see; and "physical," that address which the memories respond to.

Previously, a typical minicomputer had an equivalent logical and physical address space. A virtual memory system, however, decouples the logical and physical address space from each other. A user can now have a logical program addressing ability independent of the physical addresses used

TOTAL CDC COMPATIBILITY AND GREAT DELIVERY, TOO!



The only thing worse than not having enough disk storage, is not being able to get enough disk storage.

Fortunately, the Ampex DM-9300AQ solves both problems. With 300 megabytes of reliable disk pack storage and off-the-shelf delivery.

But the advantages of the DM-9300AQ don't stop with delivery. It's completely compatible with CDC's 300 megabyte drive. So disk packs can be interchanged, written on, or read by either drive. Of course, the industry standard SMD interface, and power sequencing of both units are also compatible.

DM-9300AQ disk pack swapping is as easy as using them. Its large front opening has been designed with the convenience of a top loader, and human engineered for minimal lifting. So even a 20-pound pack is easy to insert and remove. It's such a good idea, we're surprised somebody didn't think of it sooner.

But then, the DM-9300AQ is full of good ideas. Like highly reliable on-track servoing, and a single port daisy-chain interface with ribbon cable that can be converted—in the field—to an internal dual port.

And the same goes for maintenance. Service requires only front, rear, or top access. Side access is eliminated, so you can arrange the units side by side. What's more, the logic chassis in the rear of the unit swings out to provide easy access to all test points and connections. And extensive use of LEDs simplifies trouble-shooting.

The DM-9300AQ has a lot to offer. But what's even better, is that it's all offered right now. With delivery that's ready when you are.

The DM-9300AQ. Just one of a complete line of Ampex plug compatible disk drive memories for nearly any CPU.

For more information, contact Gary Owen at Ampex Memory Products, 200 North Nash Street, El Segundo, California 90245. If you're really in a hurry call him at 213/640-0150. Or contact your local sales office.

Either way, we won't keep you waiting.

AMPEX

MAKES THE DIFFERENCE.

Circle 18 on Reader Inquiry Card

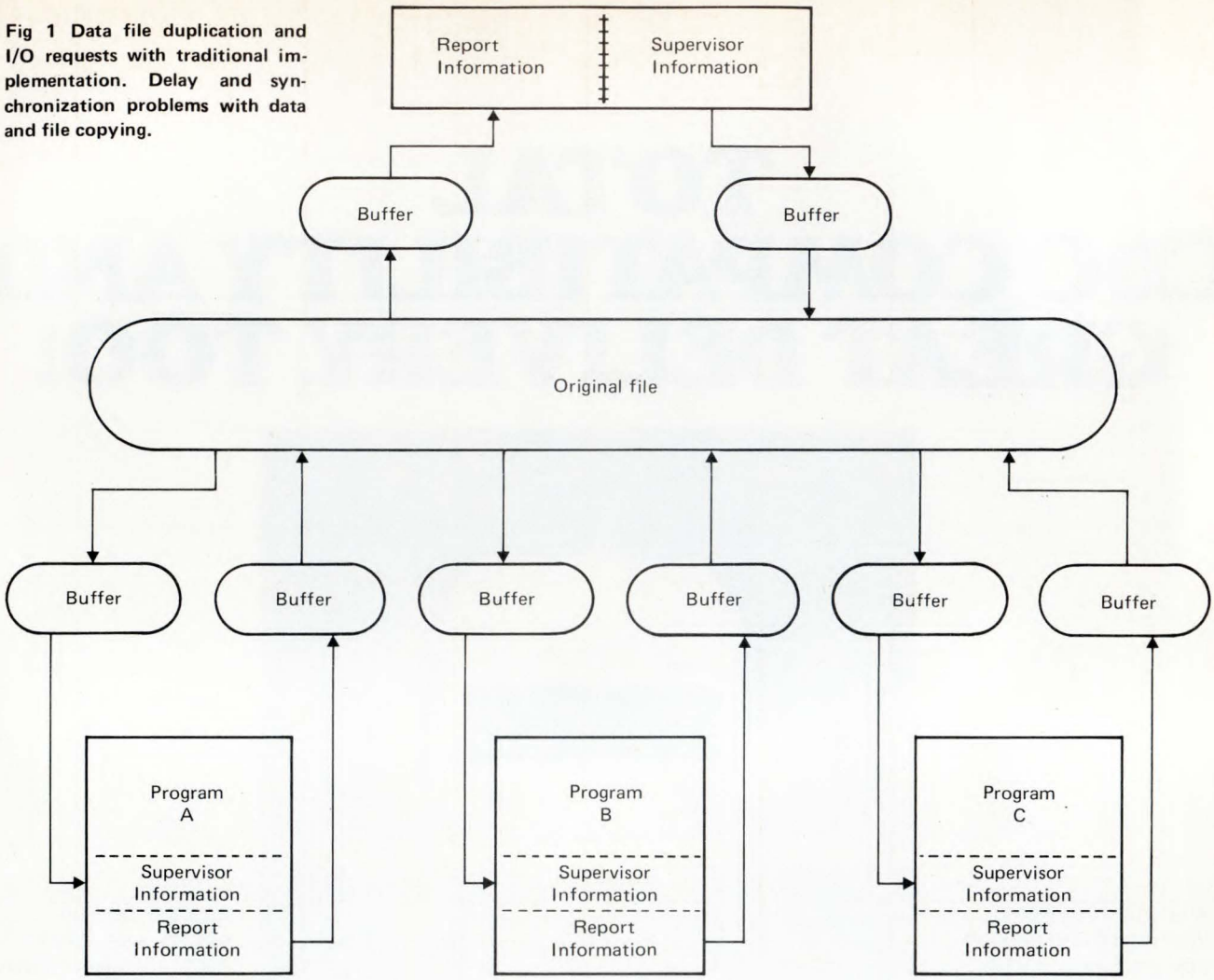


Fig 1 Data file duplication and I/O requests with traditional implementation. Delay and synchronization problems with data and file copying.

by the computer's memory. Indeed the user can address logical memory which does not exist in physical memory and an operating system can catch the event, suspend the user, obtain the appropriate information into some real memory and resume the user, all in a manner so that the memory virtually appears to be there all along. Now the user is not limited by either the logical addressing limit or the machine's physical memory size.

Some bits

A memory management unit (MMU) inserted between logical and physical address space helps support this allocation and deallocation of physical memory for virtual memory needs. The designer of a virtual memory system faces two major decisions about the MMU and the CPU. First, the type and placement of the MMU determine the storage management of the entire system. An MMU of reasonable cost can be implemented whose operation is well defined in software technology using a simple single dimensional technique such as paging. If the map is not placed on the CPU then other devices such as disk controllers may use the MMU and operate in logical address space. In addition, the entire physical memory of the machine can be available as an I/O cache for the disk or other backing store.

The other hardware problem is to insure that the CPU be capable of instruction recoverability. Should an attempt be made to access a virtual address whose contents are not yet in physical memory, the state of the processor must be preserved until the proper resources are available and then the action continued with no information loss. The processor must recover from its inability to complete an instruction in a manner which allows repetition or completion of the instruction later.

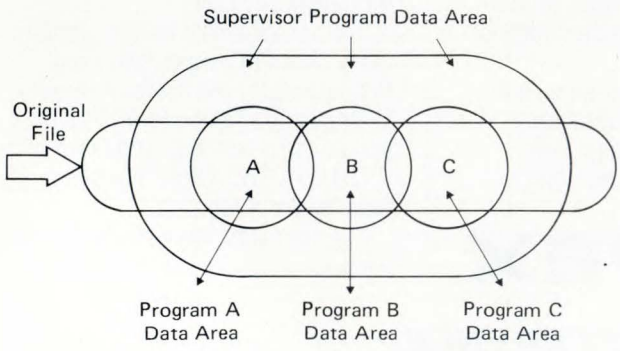
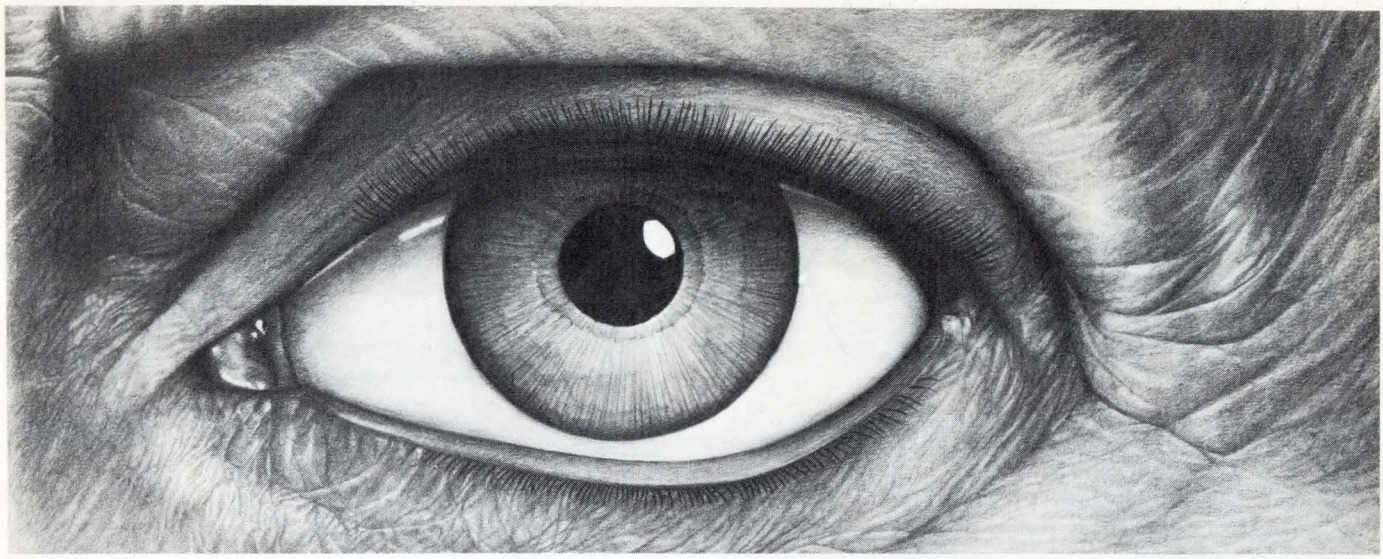


Fig 2 The three independent processes overlap data spaces and share the original data file.

Beyond virtual memory

Virtual memory is just a gimmick – one tree in the forest. If we look more closely, however, we can see that virtual memory is part of the general problem of storage management. And if we are careful while designing the system – operating system, hardware, and software – into CPU,

Foresight, foresight, foresight.



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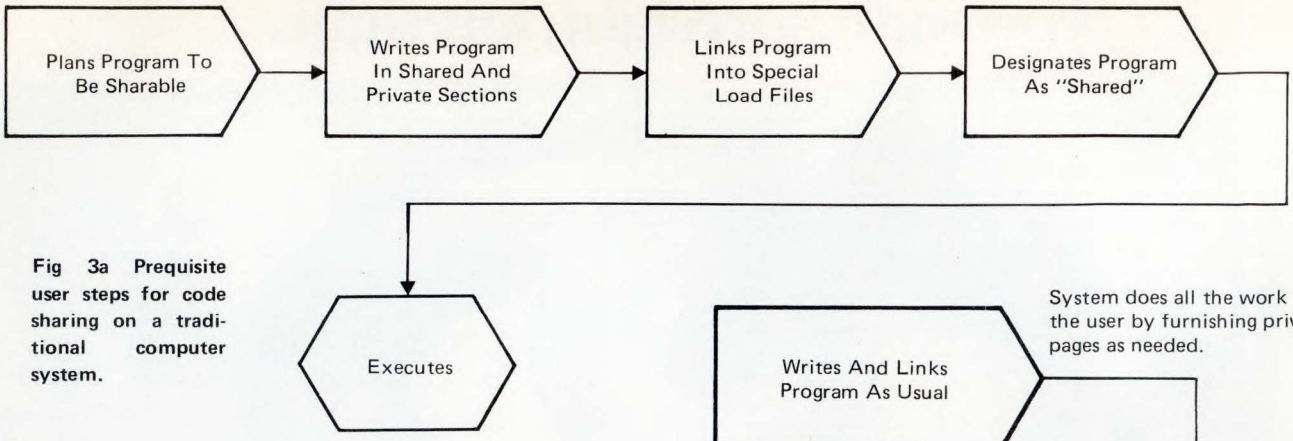


Fig 3a Prequisite user steps for code sharing on a traditional computer system.

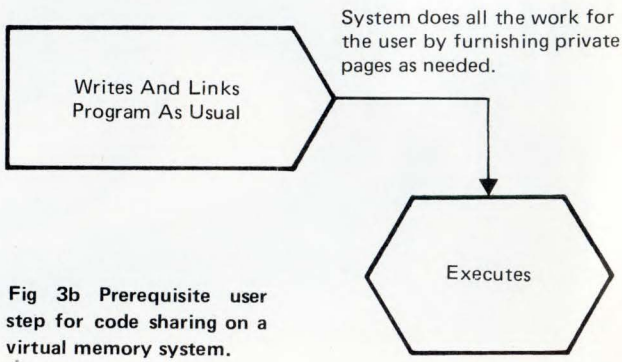


Fig 3b Prerequisite user step for code sharing on a virtual memory system.

MMU, kernels and tasks, we can meet the user needs more exactly. We must remember that the user wants to manipulate collections of information – information which contains procedures or data. Rather than just stuffing some demand paging software into a conventional operating system and making it more complex and unreliable, we have the opportunity to design the system to facilitate all access to data. Indeed the system itself needs the same service. There is also the chance to make the system more efficient if we can eliminate the overhead of storage moving and interfaces between speed bounded devices such as memory and disk.

Taking these considerartions into mind while designing, we can automate the procedure for obtaining information, just as the spark advance was moved under the hood of the car. Let the user simply refer to a space containing his information, and let the hardware and software supervise the location of the data and obtain it when it is referred to. Once the system knows of these data spaces, several benefits accrue. (1) The user doesn't have to supervise them, (2) more than one user can access them, and (3) operations can be performed directly on them (rather than indirectly through traditional file operations.)

Storage management and processor addressability make data and program access transparent to the user. By making all instructions and data items processor addressable, user access to them is implied whenever he addresses the item. The operating system and hardware catch the reference and take explicit action if the item is not already available. One can use the same mechanism to control the accessibility of information so that several users' separate computations can share the same system resources. Sharing should be transparent, general and accomplished without duplication of the shared information.

Example 1 shows intersecting file and program spaces. The greatest advantage in having all operations processor addressable is that information copying between file and buffers is eliminated. Data files do not need partial copying done by a file request through an I/O system, nor is there a need to write back to the files from user buffers after data has been modified. Instead, a program directly addresses the needed data elements in the original file while it appears as data inside the user program.

Duplication is unnecessary. Program complexity is greatly reduced since on-line information and storage can be directly addressed by a one-step operation without the prerequisite of an I/O request. In effect, I/O is done automatically for the user.

Let's look at a hypothetical situation in which data sharing would facilitate the operation of an assembly line. Suppose we have three interdependent processes that require intercommunication of computational results to properly select parameters for the assembly line's speed. We also have a supervisor program that oversees these three processes and uses their data manipulation results to perform its own computations. We have a data file that all three processes and the supervisor program can access. In a traditional minicomputer, a lot of buffer copying and I/O requests would have to be made. Duplicate copies of each processes' data would have to be generated, and these copies written back to the original file, as shown in **Fig 1**.

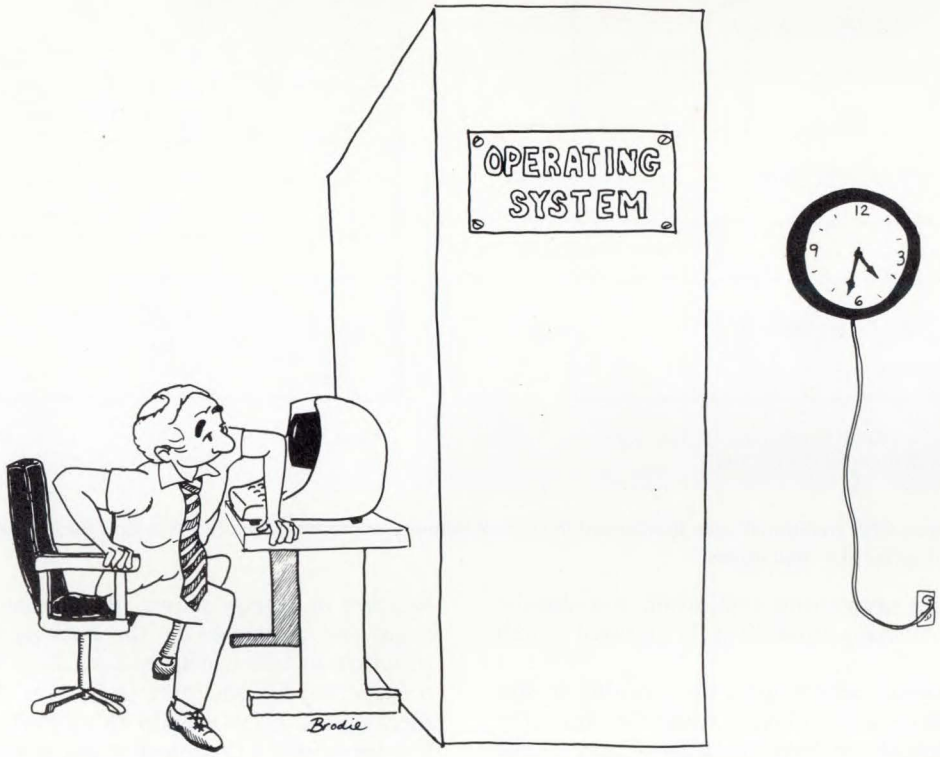
With a virtual memory operating system on a minicomputer, as shown in **Fig 2**, notice that the three interdependent processes have been declared such that they overlap each other's data spaces and also share the original data file. Also, the supervisor program has been declared so that its data space contains all three processes' data areas as well as any portions of the original file it may need for its computations. Task solving is greatly simplified: each interdependent process can use results from each other's computations; each can access and modify the original file directly, and each can be efficiently supervised by a master program that has concurrent access to the original file shared by the other processes. No duplication of information, no intertask communication problems, no time consuming I/O buffering. Instead, all data sharing and modifications are handled implicity.

Example 2

Let's look at a second example: code-sharing on a virtual minicomputer. Normally, sharing of executable code is associated with "boiling cauldrons, eye of newt, and toe of frog." But on a virtual memory operating system, it's really straightforward.

By making all programs sharable and furnishing each user with a private copy of a portion of the program only when necessary, the complex bookkeeping associated with writing, linking and executing sharable programs is eliminated (**Fig 3a** and **3b**). If this is done properly, not only is

Real-time?



Don't let an operating system get in the way.

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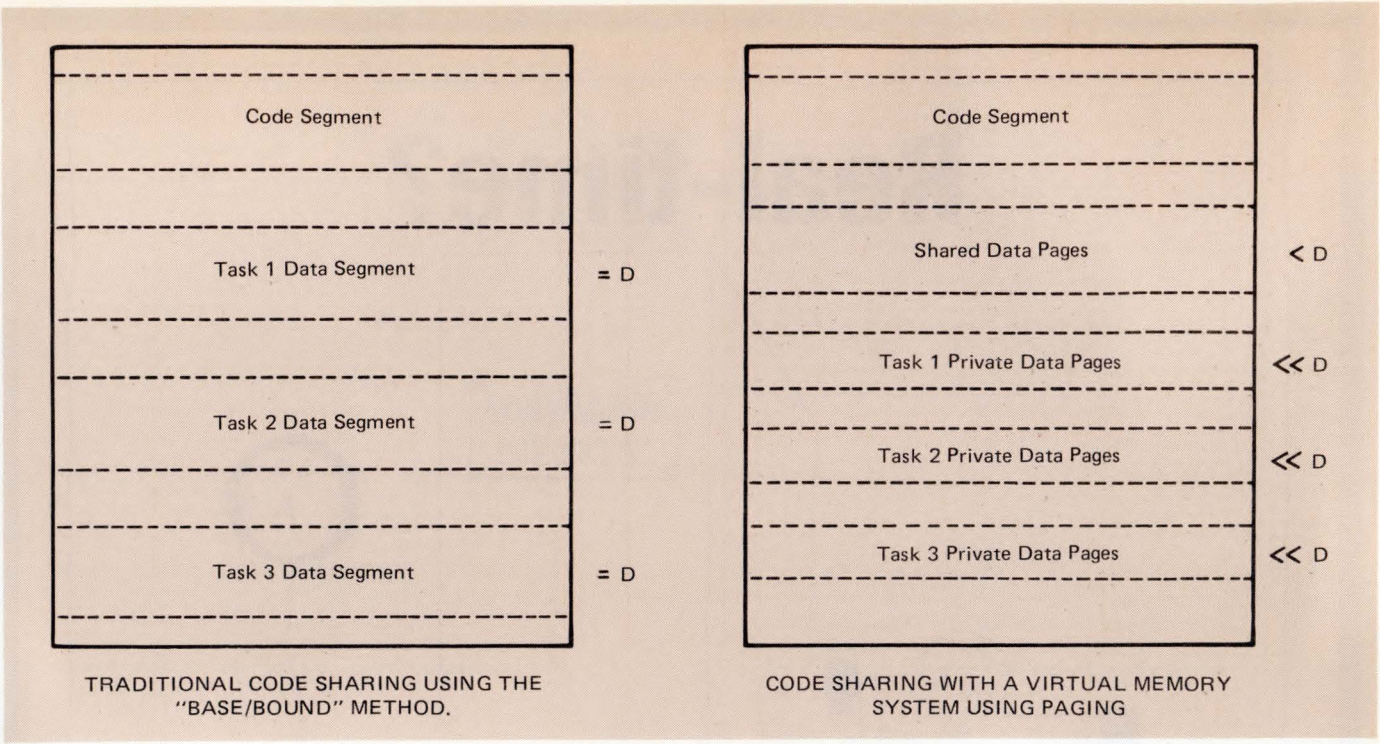


Fig 4 Memory utilization with traditional code sharing and the virtual memory approach. Memory utilization for "N" users portrays code sharing, where "D" is the number of shared pages.

central memory space saved from duplication, but also the actual space on the backing store swap files is saved as well (**Fig 4**).

For example, suppose several users were sharing an editor. When an additional person begins using the editor, the operating system would not have to create a copy of the program for him. Instead, he could execute those portions of the program already in memory. As a user proceeds to execute the program, those pages that were not modified could be dropped or left for other users. Later, when the user continued, those pages would be retrieved directly from the editor file or from pages that other users were already employing. As the user begins altering memory regions that contain a copy of text, that portion of the program would be duplicated into a private copy automatically by the operating system at that time.

Using this approach, all programs can be automatically sharable without the tedious planning and layout that normally accompany sharable code. Each user appears to have a private copy of a program because each modified portion has been duplicated and made unique by the operating system only when needed.

Where are the mirrors?

Now that we've finished talking about what we want from the system, we might ask who has done it or how was it actually done? Honeywell's MULTICS, and Bolt, Baranek and Newmans' TENEX are foremost examples of systems providing these services. Their installation costs, however, are very high. Bell Labs' UNIX hs a mainframe type file system available on a mini, but provides no direct addressing or virtual memory services. If you want to implement such a system yourself, you might consider basing such a system on a small set of mechanisms and then implementing them in software, firmware or hardware.

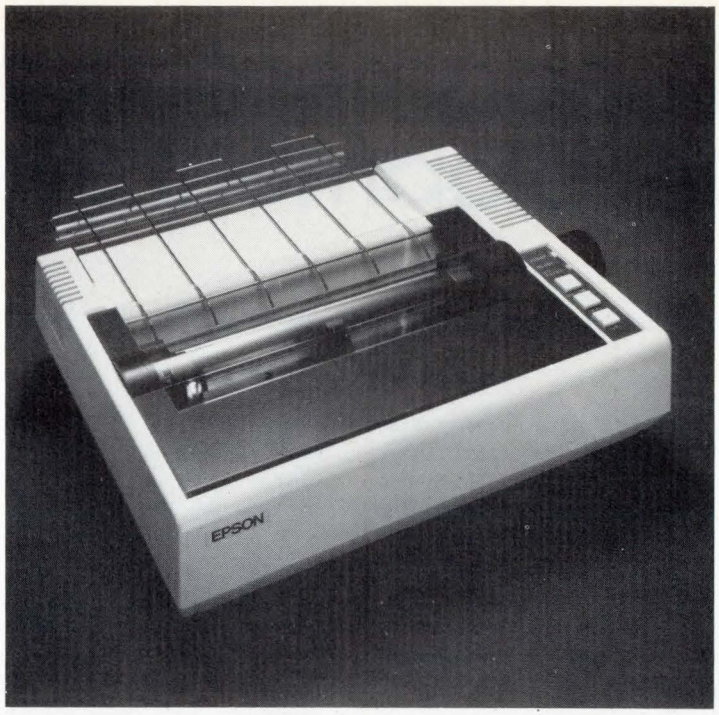
On the Computer Automation PROTOS system, all storage management is based on a set of mapping mechanisms which relate to each other and to storage without elaborate searches or storage moves. By binding all central memory pages and references to the backing store, one of these primitive pseudo machines turns all of central memory into a cache for file and program access. The mainframe type mechanisms which support this activity on a mini fall into five categories: (1) protected and system mode in the CPU, (2) MMU manipulation by CPU and other devices, (3) large amounts of memory and caches, (4) instructions which facilitate operating system performance, and (5) instrutions which facilitate higher level system implementation language performance.

All these mechanisms provide a system with high processing bandwidth, high multiplex rate among users, and minimum I/O and masked interrupt time. Each of them was achieved by looking further down the road while designing and identifying needed functions relative to the goal of the system. Every hardware or software mechanism facilitates storage management so that not only is demand paged virtual memory available, but also intersecting file and program spaces, and shared code for all programs.

Thus, we have a virtual memory operating system on a minicomputer that eliminates duplication of information. Both code and data sharing may be done automatically and in a general manner for all system users. The PROTOS virtual memory operating system will access a file region that the AUTOMAP feature has mapped implicitly, and implicit operation is possible because of immediate, direct processor addressability.

Additionally, programs may be shared, and unnecessary duplication of program areas in main memory is eliminated. These savings, combined with the problem solving convenience of information sharing, give the user new power in a computing system. And virtual memory operating systems like these are now available to minicomputer users.

The MX-80. It not only does everything, it does everything well.



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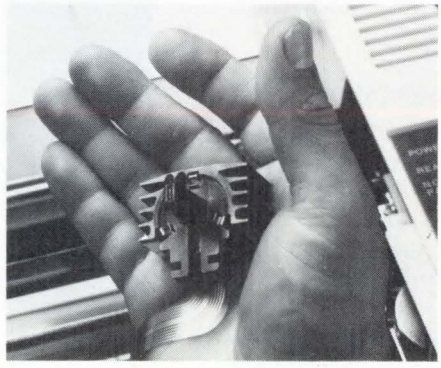
The MX-80 prints bidirectionally at 80 CPS in a user-defined choice of 40, 80, 66 or 132 columns. And if that's not fast enough, its logical seeking function minimizes print head travel time. The MX-80 prints 96 ASCII, 64 graphic and eight international characters with a tack-sharp 9x9 matrix. For a long time. Epson printers are known for reliability and the MX-80 is no exception. But that's not the best reason to buy it either.

The print head has a life expectancy of up to 100×10^6 characters, and when it wears out, just throw it away. A new one costs less than $30 and the only tool you need to change it is attached to the end of your arm. The MX-80 is compact, weighs only 12 lbs., and the whole unit, including the two stepper motors controlling carriage and paper feeding functions, is precisely controlled by an internal microprocessor. But even that isn't why you should specify the MX-80.

The best reason is this: because Epson makes more printers than anyone else in the world, we can afford to sell each one for a little less. So you can get one Epson MX-80 Printer for less than $650. And more than one for even less than that.

That's what we call a small price to pay for a printer that does everything well.



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Fundamentals of μP Development Systems

Paul Wintz
Wintek Corp., Lafayette, IN

Don't shortchange your programmers by cutting corners on development systems. Software is advancing slower than inflation. In any particular application, software costs can range from a small fraction to a large fraction of total system cost. The average for industrial μP applications is 60% to 90% of total project cost. Software costs range from $1,000 to $10,000 for small dedicated control applications, then up to $50,000 or more for sophisticated systems. To gain a better perspective of the total software development picture, re-examine some fundamentals.

Spend the money

Software is the most expensive part of the μP project and the most likely for schedule slips and other problems. It involves designing, coding, debugging and documenting. Coding, although only 10% of the total programming effort, takes an incredible amount of precise and meticulous bookkeeping. A coding error could be a bug that takes hours to find and days to fix. It is not unusual for the fix to create new bugs that appear later in the debugging process.

A program is best constructed by one programmer. Adding a second one increases costs 100% but productivity only 50%; adding a third may increase productivity another 25%. Few people are capable of managing software projects. A group project requires detailed sets of software specifications, and that implies a software design with up to 50% of the program effort. Then it must be rigidly enforced. A solo programmer can change and adapt during the coding process. Try to increase individual programmer productivity – not increase the number of programmers.

Programmer productivity can also be significantly increased by the use of well designed tools. Spend the money; don't hinder programmer efficiency. A good software development system has a computer with appropriate software for helping the programmer to efficiently enter and edit his source code, assemble or compile it, debug it, document it, transfer it to his applications system for final system check out, and, finally, put it into EROM.

Development system-hardware considerations

The minimum hardware requirements for a development system include two disk drives, sufficient memory (ususally 32 k to 56 kbytes), one or more serial I/O ports, and possibly a parallel printer port.

Two disk drives are required so that the user can copy diskettes. Most development systems come with a single system diskette containing the system software. Diskettes have a finite lifetime. Besides, Murphy's Law dictates that before that lifetime is exceeded, the user or a colleague will trash the diskette by physical neglect or by writing over some of the files. So, prepare backup diskettes of the operating system and the software products as they are developed on the system. This copy capability implies two drives, one to read the diskette to be copied and another to write the new one.

Sufficient memory is required to store the operating system (usually about 6 k to 10 kbytes) plus other programs such as editors, assemblers, compilers and user space. As a rule of thumb, an assembly language development system would require 16 k to 32 k of RAM. A small compiler such as small C would require a 48 k system. To support a full compiler, such as PASCAL, C, FORTRAN, PL/W, etc., usually requires a 56 k system.

An RS-232C serial I/O port makes the system plug compatible with any smart or dumb terminal such as a CRT terminal, teletype, TI Silent 700, etc. Multiple serial I/O ports may be required if the system is to support more than one user or if the user wants to add further RS-232C peripherals, such as a serial printer.

A parallel printer port allows a user to connect a parallel line printer capable of supporting speeds much greater than

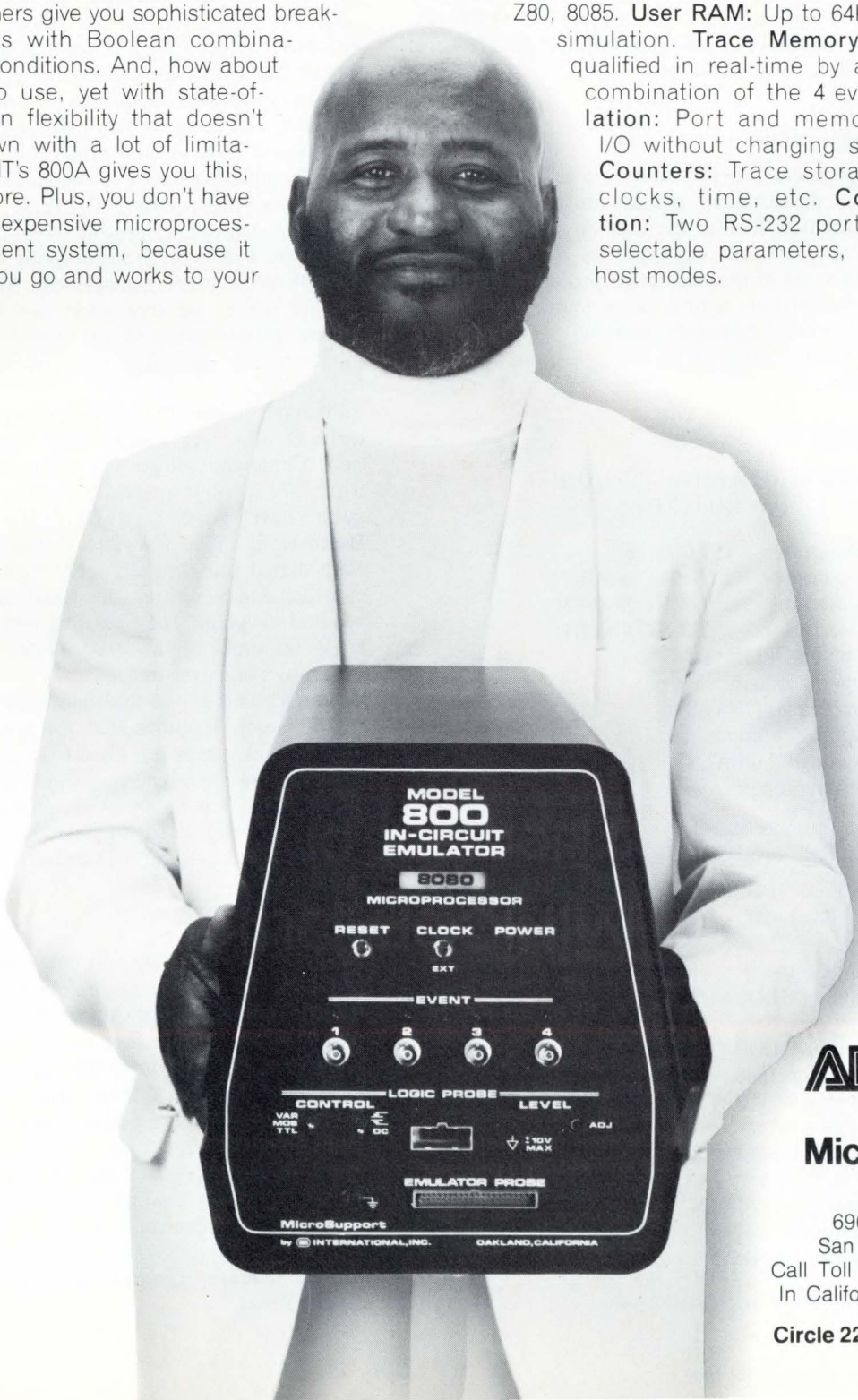
Fig 1 Costs for a good μP development system include a console terminal (Hazeltine 1500, $1200), μC (Wintek Sprint 68, $3995), line printer (Centronics 779, $1350) and applications computer (user supplied).

Comparing Emulators? "This one's beautiful."

It's ADVANT's Model 800A, stand-alone emulator with beauty that's more than skin deep. Just compare it to any others. Ask yourself if they can completely debug, disassemble, and trace in both state and time domains. Will they do all this in real-time, without any wait-states either for you or your results. ADVANT's 800A does, no matter how you use it.

Can the others give you sophisticated breakpoint settings with Boolean combinations of bus conditions. And, how about being easy to use, yet with state-of-the-art design flexibility that doesn't load you down with a lot of limitations. ADVANT's 800A gives you this, and much more. Plus, you don't have to tie up an expensive microprocessor development system, because it goes where you go and works to your schedule. Not others. And that's the real beauty of it.

ADVANT 800A Quick Specs. **Operation:** Stand-alone, real-time, no-wait states, even with mapped memory. **Events:** Four 40-bit bus conditions, including "don't cares," pass counters and delays in real time. **Breakpoints:** Set on any Boolean or sequential combination of the four events. **Emulates:** 8080, Z80, 8085. **User RAM:** Up to 64K, with ROM simulation. **Trace Memory:** 256 deep, qualified in real-time by any Boolean combination of the 4 events. **Simulation:** Port and memory mapped I/O without changing source code. **Counters:** Trace storage, events, clocks, time, etc. **Communication:** Two RS-232 ports, software selectable parameters, with special host modes.



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a serial port. Although several printer interfaces exist, the de facto standard is the Centronics compatible interface. Most printer vendors provide one or more interfaces as options. For example, Centronics offers as an option a Data Products interface; and, similarly, Data Products offers an optional Centronics interface.

Software considerations

Development systems software is (or should be) 98% of the development cost of a development system.

Most development system vendors provide adequate hardware; software is much more varied. Unlike hardware specs – 8″ disk drives, 56-k RAM, RS-232C serial I/O port, Centronics compatible printer port, etc. – software features lack precise meanings. There is no precise definition of a disk operating system (DOS), or even of the features included in an operating system. The same is true of editors, assemblers and compilers. Vendors emphasize plus features but never mention missing features.

The operating system

The operating system provides a convenient interface between user and development system. Most operating systems are file-oriented so that the user can create, modify, copy, delete, assemble, etc. programs by file name. Many operating systems are of the interactive, prompting type and make use of defaults to reduce the amount of time and effort required to enter system commands.

Let's look at an example of an interactive, user-oriented operating system..

```
01 SYO: compilec

                Wintek C Compiler – Ver. 0.61
                  copyright © 1980

  source file descriptor    :STDio.ccc
  object file descriptor    :ND:STDio.MIK
 scratch file descriptor    :ND1:STDio.ASM
  listing file descriptor   :ND2:STDio.LST
          compiling GLOBALS
          compiling isdigit
          compiling GLOBALS
          compiling crcknum
          compiling GLOBALS
          compiling tohex

$0055     digit = (number % 0xFH
*****     line $0055: invalid numeric constant

          compiling GLOBALS
          compiling todec
          compiling GLOBALS
          compiling tooct
          compiling GLOBALS
          compiling strlengt
          compiling GLOBALS
          compiling prtpad
          compiling GLOBALS
          compiling prt1
          compiling GLOBALS
          compiling printf
          compiling GLOBALS
          compiling fprintf
          compiling GLOBALS

$0001     error(s). Compilation Aborted.

Wintek WIZRD DOS
COMMAND – Ver. 1.0a
01 SYO:
```

Only the italicized characters are entered by the user. The session starts with the user calling the C compiler by entering the system command "compilec". The system then prompts the user for the name (file descriptor) of his C language program. The user responds by entering "STDio" which is the file descriptor for his program "standard input/output." He chose to not enter a file name extension and so the operating system uses its default for C language programs "ccc". The system then prompts for a name for the object code file and the user enters ND: (null device) the name of the device on which this file is to reside. The user chose not to enter a file name or extension and so the system supplies the file name "STDio" (same as the source code file name) and the extension "MIK" (its default for MIKBUG object code). After similarly prompting for the scratch and listing file names, the system starts the compilation and prints out a sequence of messages allowing the user to monitor its progress. While compiling the routing "tohex" it uncovers an error and prints out a 2 line error message. After completing pass 1 it aborts because of the error and returns the system prompt 01 SYO:

Additional operating system features to look for include: command indirection, multitasking, multiuser, virtual I/O, and HEAP memory management. Many μC disk operating systems (DOS) are very crude with few bells and whistles. Others include many of the features commonly found in minicomputer operating systems. Here are some features to look for. . . .

Command indirection: Many μCs are used for process control and other applications that require unattended operation. Command indirection allows commands to be read from files without operator intervention. Such programs require a development system with this feature.

Multitasking: This allows partitioning overall system software design into smaller, more manageable modules, each of which can be written, debugged and executed as an independent program. The operating system allocates MPU and RAM resources on an "as-available" basis to the various programs being executed.

Multiuser: This allows multiple users access to the development system. Requires that the multitasking allocate the development system resources to multiple users. In addition, each user's resources are protected from other users.

Virtual I/O: This allows all peripheral devices to be treated in a device-independent manner. Thus it is easy to add device drivers, e.g., for an A/D converter.

The editor

A good text editor lets you enter and edit source code. It should allow you to enter, delete, edit and rearrange blocks of text. Conditional editing commands cause the editor to operate only on the text meeting a specified condition, such as those lines containing a particular character string. Another time-saving feature searches through a large program to quickly find a particular line or section, or a certain set of characters or key words.

Some editor features are invisible to the user, at least superficially. For example, most μC programs contain a considerable number of blank lines and blank spaces within lines. Space compression codes a string of space characters into the number of spaces, thereby using less disk space to store the text.

The assembler

An assembler can increase programmer productivity five fold by handling much of machine language programming tedia. An assembler allows the user to write the program in μP mnemonics, which are more meaningful and easier to remember than machine code. For example, to load accumulator A with the number 5, mnemonic LDA A #5 makes more sense thant the machine code 8605. Labels allow the user to refer to variables by name rather than by memory location where they are stored. For example, it is easier to remember temperature as TEMP rather than the hexadecimal memory address 1A43. Humans evaluate expressions and branch offsets correctly about 85% of the time; assemblers get them right 100% of the time. Finally, assemblers have debug features that find and flag some of the more common programming errors.

Different assemblers sport different bells and whistles. Some features such as conditional assembly, pre- and post-radix notation, programmer flagged errors, macros, free format input, ASCII characters and readily-apparent convenience features reduce the programming effort. Pseudo-ops to reserve memory bytes and form ASCII character strings save programming effort, while TITLE and PAGE make reading documentation easier.

The compiler

Assemblers allow the program to be written in mnemonics rather than hexadecimal machine code but source-code mnemonics are still tied one-to-one to the microprocessor instruction set. Compilers free the programmer from the μP instruction set and allow the program to be written in a language more amenable to the application. Writing a program in a high level language and having the compiler generate the machine code has a number of advantages. Programmer productivity increases tenfold, program reliability improves and maintenance costs drop. Here are compiler advantages.

Coding time and effort: High-level-language source codes allow powerful statements such as IF A EQUALS B AND C IS NOT ZERO THEN DO _____, OTHERWISE DO _____ TEN TIMES. In assembly language it could take a sequence of twenty or more instructions to achieve the sequence of 20-plus instructions to achieve this.

Most programmers turn out the same number of lines of code per day independent of the language they are writing in. Consequently, a program in assembly language might run thousands of lines and take months to write. A high-level language would consume hundreds of lines and take weeks to write.

Debugging time and effort: Debugging programs written in a structured high-level language using good coding practices such as block structure and disciplined flow control is much faster and easier than debugging programs written in assembly language. Furthermore, program changes and fixes are less likely to result in new bugs.

Reliability: A good compiler produces code that is significantly more reliable than the code produced by a good assembly language programmer.

Documentation: It is a very rare program that does not require maintenance. Maintenance includes fixing bugs and adding enhancements after the program is put into use. This is often done by a programmer other than the author. Even the original programmer requires reasonable documentation when reviewing the program months or years later. In either case, before he can maintain the program he must understand how it was supposed to work when written. Programs written in a high level language are shorter and much easier to understand than assembly language programs.

Let's examine the pros and cons of five commonly available compilers.

Basic compilers are easy-to-learn interactive interpreters. Although program loops are translated repeatedly, and execution times suffer, execution is immediate and instructions can be freely added or modified without delay. Advantages: easy to learn and interactive. Disadvantages: archaic flow control, very limited data types, very limited operators, limited number of variables, no structure, no reentrant code and unselfdocumenting.

The C compiler was designed at Bell Labs for writing operating systems. Advantages: structured, compact source code; excellent flow control; rich in data types; rich in operators; generates reentrant code and matches machine structure. Disadvantages: hard to learn and no type checking.

Fortran was designed in 1954 for scientific applications. Advantages: large library of existing programs, commonly understood and still well used. Disadvantages: obsolete, hard to learn, no structure, weak flow control, weak type checking and no reentrant procedures.

Pascal was designed to teach concepts of structured programming. Advantages: structured, easy to learn, good flow control, rich in data types, rich in operators, generates reentrant code, selfdocumenting and excellent type checking. Disadvantages: verbose and token threaded code.

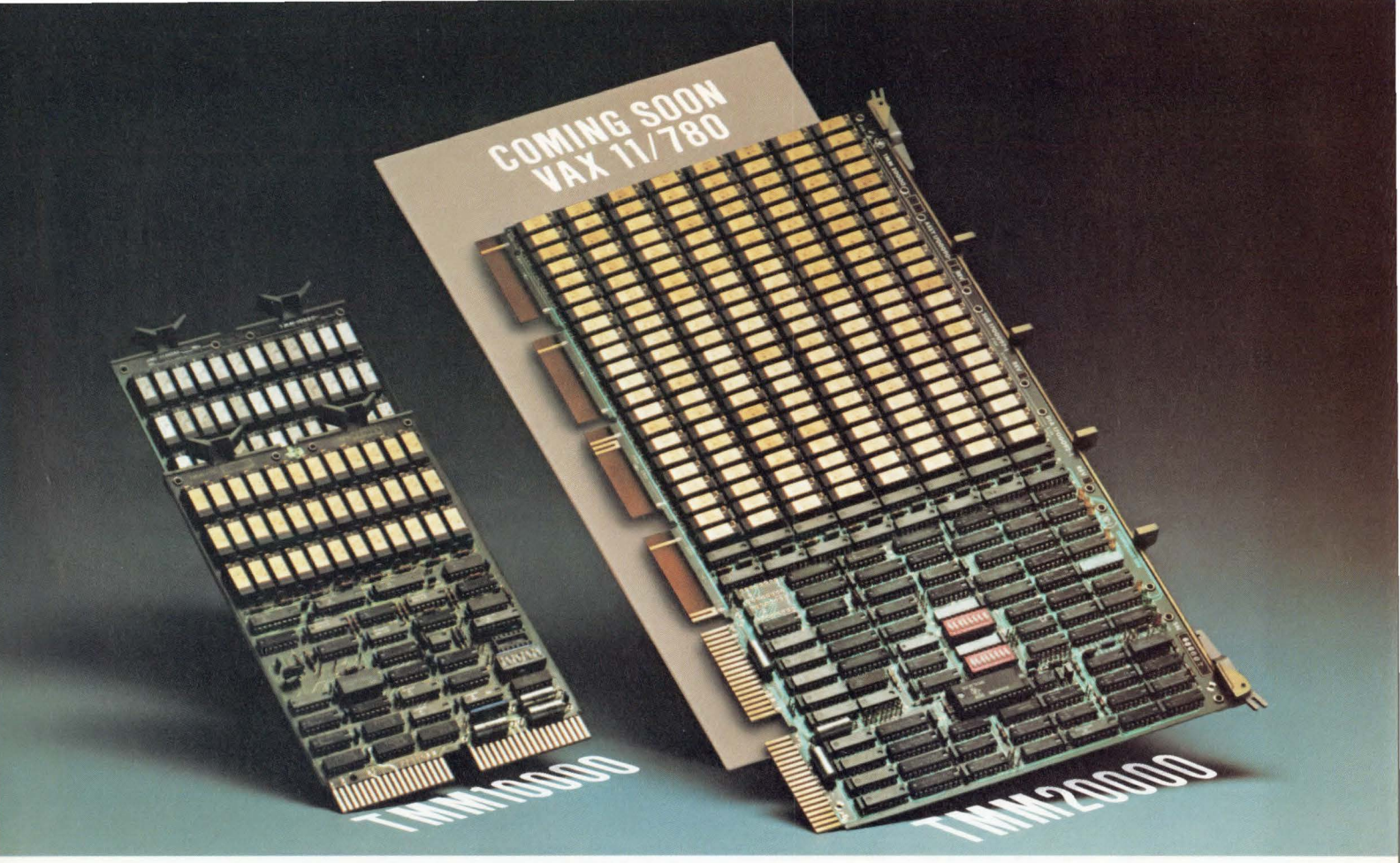
PL/X is a subset of PL/1. Advantages: structured, easy to learn, tailored to specific machines. Disadvantages: weak in flow control data types and operators.

Although compilers are much better than assemblers, they are not the complete answer to every problem. Compilers produce two to four times more machine code than assemblers. Suppose a competent programmer writes a program in assembly language and ends up with 1 kbytes of machine code. If the same programmer (or an equally competent one) wrote the program in a high level language and passed it through the compiler, the end result is usually somewhere between 2 k and 4 kbytes of machine code. In most cases this is of little concern: the extra $30 of ROM to store the extra code is preferable to the extra $2000 of effort it takes to write the program in assembly language. In some cases the extra code may be a serious concern because of execution time; however, in almost all such cases it is only a small part of the program that takes too long to execute, and the solution is to rewrite this part of the program in assembly language.

Finally, we point out that the very reason that makes compilers work – the high level language isolates the programmer from the nitty gritty of the computer hardware – makes most of them (C is an exception) inappropriate for certain tasks requiring bit manipulation; ie, access to particular bits in particular places. For example, subroutines for controlling and reading and writing data to I/O ports leading to peripherals such as terminals, A/D converters, relays and the like typically require only a few lines of assembly language code. It's best to write these I/O drivers in assembly language.

The linker

The most cost effective approach to most μP software projects is to write as much of the program as possible in a high level language. Only I/O drivers and perhaps a few subroutines are written in assembly language. The remaining task is to link these program modules together into the final composite program.



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Some compilers produce assembly language code and the final program is constructed by passing both this code and the code written in assembly language through the assembler.

Some compilers and some assemblers produce *relocatable code*; ie, code which does not have fixed addresses and can be relocated anywhere in memory. A linker is a program that links these *modules of relocatable code* together into a single absolute program.

Additional features

After the programmer enters and edits his program, assembles or compiles it, and then debugs it using the tools mentioned above, his job is not finished. He must do a final debug in the actual applications environment with the A/D converters hooked up to the temperature sensors and the digital outputs driving the pumps. How is he to transfer his program from the development system to the applications computer for final debugging? A *downloader* includes the hardware and software that automatically transfers a file consisting of the applications program residing on diskette in the development system, into the appropriate memory locations in the application system. At this point the user can debug the program in its actual operating physical environment using appropriate monitor debug firmware that will allow him to execute the program, set break points, single step through the program, etc.

Suppose the programmer finds that the program takes too long to execute. Perhaps he has to read a temperature every 1/10th of a second but finds that it takes 0.2 second to execute that part of the program. If the development system contains a *profiler* he can go back to the development system and run a histogram of the time required to execute different parts of the program. A program obeys Pareto's Law and spends 90% of its time executing 10% of the code. After having isolated this 10% part of the program, he can rewrite it to minimize execution time. Then he downloads it into the applications systems and tries again . . . and again.

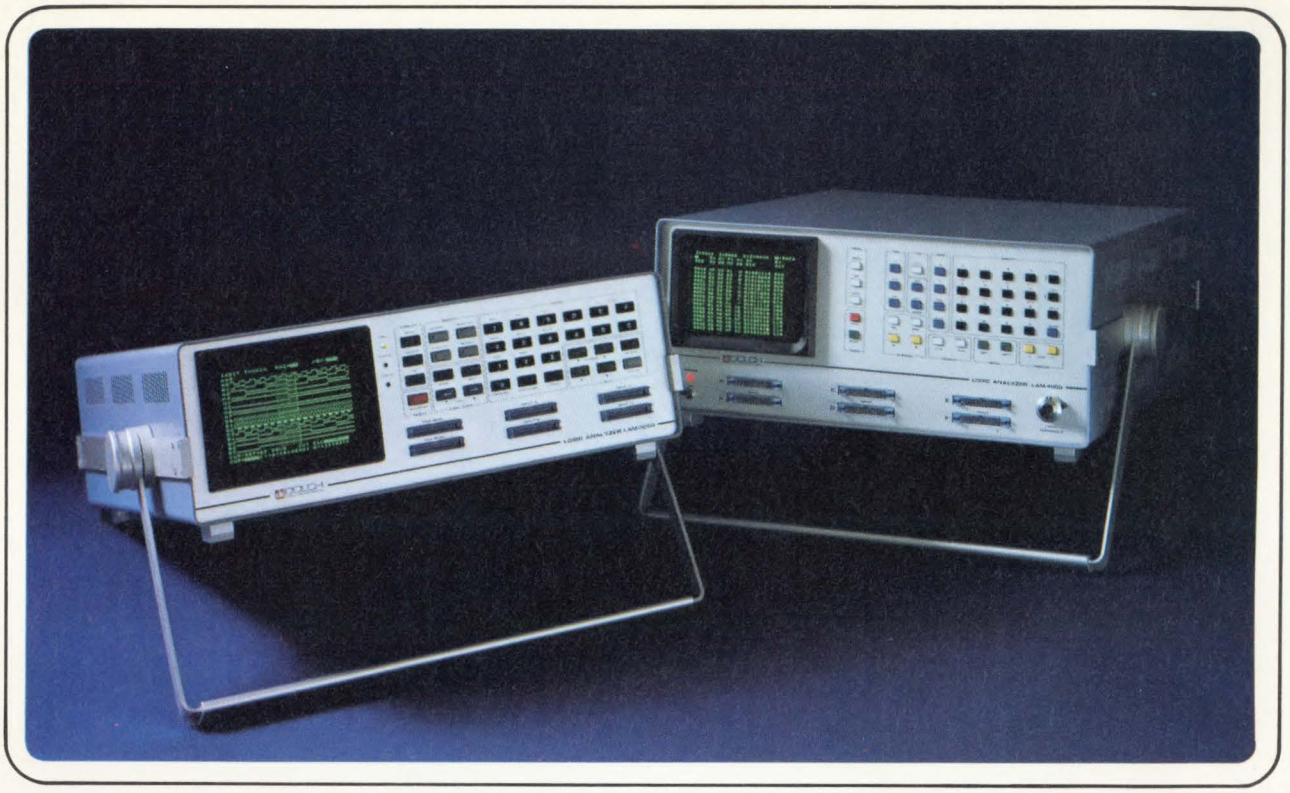
Finally, after he gets this program running as he thinks it should out of RAM in the applications system he must burn it into an EROM with an EROM Programmer. Provided his development system has an *EROM Programmer* option, he merely goes back to his development system, plugs in an EROM and enters a command that transfers his file containing the applications program into the EROM.

An alternative approach to the downloader philosophy is *in-circuit emulation*. The user removes the μP in his applications hardware and plugs in a wiring harness assembly which serves as an umbilical to the development hardware. The user may then set break-points, trace programming operation, etc. Note that the applications hardware must be designed with in-circuit emulation in mind. Otherwise, the user may be in for some unpleasant surprises when the in-circuit emulator does not behave exactly as the μP would in the applications hardware.

Select the best

This concludes the introduction to μP development system basics. Development systems consist of computer hardware and software. The purpose of the hardware is to execute the software. Software makes the system.

Remember, a programmer's productivity depends on his ability and the quality of his development system. Don't be penny wise but pound foolish.



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Logic Analyzer And μP Development System

Aid In Debugging Multiprocessor Networks

Doug Johnson
Tektronix, Inc., Beaverton, OR

When circuits containing multiple processors have to be debugged, the ideal solution is a development system for each μP operating in the circuit. This solution, however, is redundant as well as expensive. A more practical solution would be to use equipment already available in the engineering lab, i.e., one development system and one logic analyzer, to debug your circuit. This article explains how such equipment can debug multiprocessor circuits. We used a μP development system and logic analyzer with external triggering connections that are compatible and readily accessible.

During debugging, you seldom need to actually manipulate code in processors simultaneously. Generally, one processor is programmed and made as operational as possible. Then, the other processors are brought into play one at a time, and the interaction between devices is closely monitored. At this point, it's desirable to monitor both processors for certain improper or erratic operations, providing breakpoints and forced halts to both units if problems occur. In this way, you can thoroughly examine the data occurring in both units leading up to any particular error and find a solution.

Following are examples of typical problems that might occur in a μP circuit, along with several examples of how you can use this combination of development system and logic analyzer to solve problems arising in a multichip environment.

A logic analyzer connected to a development system, has two triggering modes: the logic analyzer can trigger the development system, or vice versa. First, let's see how to trigger the logic analyzer from the development system.

On the 8002A development lab's rear panel, are two outputs for triggering external devices: EVENT 1 and EVENT 2 **(Fig 1a)**. When a corresponding internal-triggering event occurs, a positive TTL-level pulse will be sent to the appropriate EVENT connector. These two outputs can then be tied to either the TRIGGER IN connector or to one or more of the logic analyzer's eight test clips **(Fig 1b)**. The logic analyzer then triggers on any number of event combinations provided by the development system.

To set up the development system for triggering from the logic analyzer, connect the logic analyzer's TRIGGER OUT connector to any of eight test clips provided as development system inputs **(Fig 1c)**. Then set the development system to trigger on one or more trigger pulses coming from the logic analyzer, or use the trigger as an arming device for another internal triggering event.

In addition, you can configure the logic analyzer and development lab to specify complex triggering events that may be needed to solve especially difficult or complex problems. If you set the two devices to trigger each other

Figure 1a

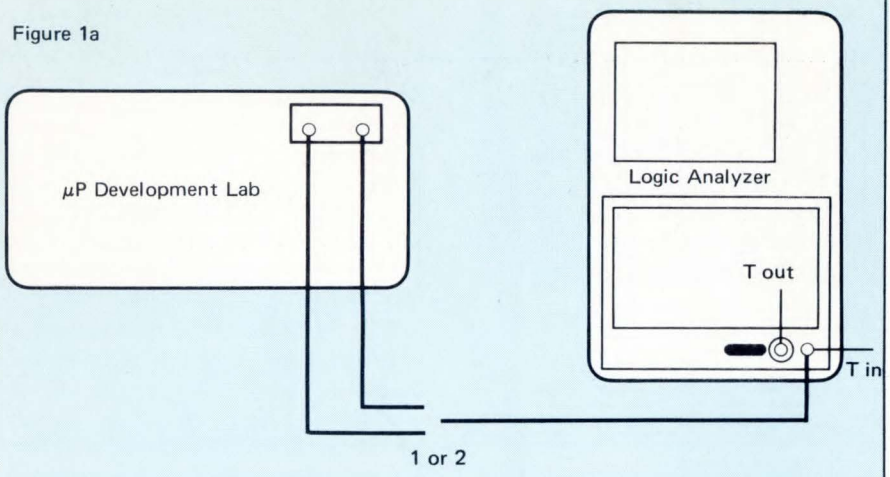


Figure 1b

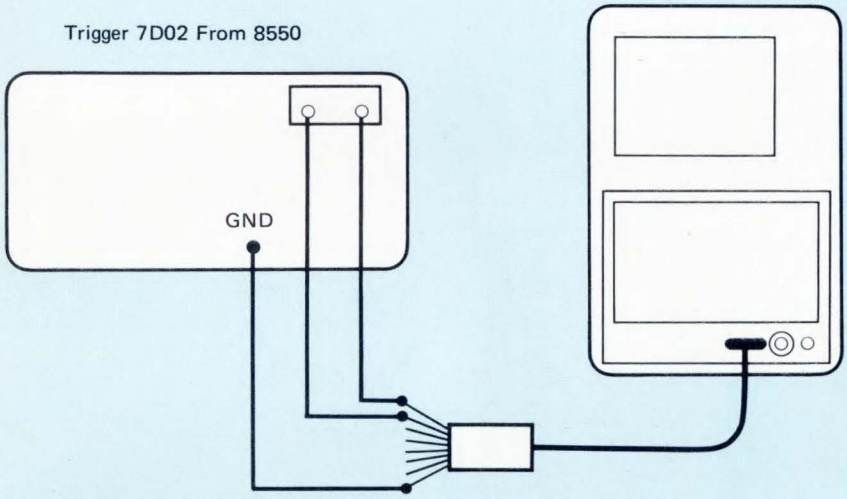
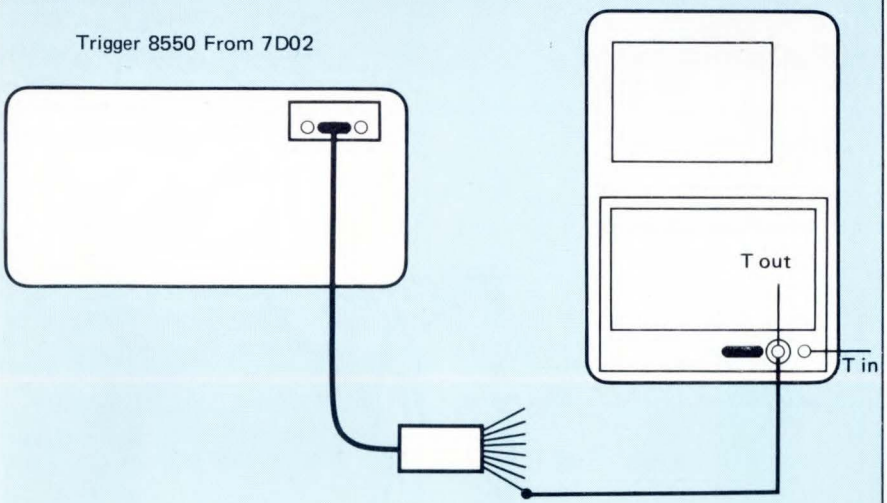


Figure 1c



Development lab (left)/logic analyzer (right)/ connections. (a) The development system's EVENT 1 or 2 output can tie into the logic analyzer's TRIGGER IN (T in) or (b) can be tied to one or more of eight test clips. (c) It works in reverse, with the analyzer triggering the development system.

Designers Prefer Universal Development Systems

(This report is based entirely on material supplied by Millennium Systems, Inc.,)

To develop a successful short term (1979-1983) marketing strategy Millennium has conducted research consisting of: (1) mail survey of engineers chosen at random from a magazine list and our list (2) discussion with two groups of ten working engineers about development systems and related design aids. The research findings show that the recent trend in μP development systems is an economic one which stresses cost justification. Two major approaches to this cost justification are *universality and low cost/add-on alternatives.*

Universal vs. dedicated

Design engineers clearly see universal development aids becoming more usable and useful; the engineers were particularly aware of the fact that a *universal system reduces the learning curve* time for a new μP. They also liked *removing the limitation to one processor* family that a dedicated system imposes (increased capability justifies the price.) When development systems break down a company must often buy more than one system to avoid costly down-time. *Field service support of dedicated systems by IC manufacturers is seen as poor* to non-existent. The entrance of Hewlett-Packard, GenRad and Tektronix into the universal development market is viewed by most engineers as a blessing. They believe that these *instrumentation companies will take better care of them* than the semiconductor companies have done or will do.

Of all development systems sold since 1976 85% to 90% were dedicated systems. As dedicated development systems lose their attractiveness and universal systems gain in popularity, *sales of dedicated systems will grow at an annual rate of about 20% over the next few years while the sales of universal systems will grow at a rate of about 66%.*

Time-related considerations enable dedicated systems to emerge with a clear edge. The dedicated system is built in parallel with the μP's development cycle. Builders of universal systems wait until the processor has been introduced and stabilized in design before producing a supporting development system. The semiconductor manufacturers emphasize this point; however, Millennium's research indicates that point may be overstressed. The interviewed engineers for the most part exhibited *less urgent interest in purchasing state-of-the-art processors and further indicated that second-sourcing is a major requirement.* It follows that they are not entirely committed to a particular manufacturer's development system.

Add-on alternatives

Further research indicated that *only about 25% of all μP development is being done on full-blown development systems.* Another 25% is carried out on single-board computers, homebrew systems and other "custom" devices. Surprisingly, about half of all μP systems development is handled with cross-assemblers and other software running on a general purpose mini- or mainframe computer.

Engineering *management see μP development systems as recognizably expensive.* Not everyone in the lab has access to the MDS when he needs it. Add-on equipment to increase the number of users of a system (dedicated or universal) is attractive.

Semiconductor manufacturers who introduce and sell μPs that are still in the design stage cause problems which are not solved by the presence of full-blown development systems. Engineers say they have a *need for inexpensive tools to help them evaluate* a range of μPs in a specific system environment.

Engineering managers doubt that high-priced, high-end performance systems recently introduced will have a dominant place in today's economy. A medium-sized manufacturing firm may not justify spending $40,000 to $70,000 for a single-user tool when it could invest that much in low-cost design aids for enhancing the capability and performance of existing development systems or host computers. This will be a short term

Continued on page 43

repetitively; the logic analyzer triggers the development lab, which in turn triggers the logic analyzer, and so on.

Circuit

The circuit to be used in the following examples is shown in **Fig 2.** It contains two Z80s, each with its own ROM and RAM for ease of explanation, with identical addresses from 0000 to 3FFF and 4000 to 4FFF, respectively. Also, both processors have access to a common RAM area at address 5000 to 5FFF. Processor 1 is used to handle I/O from a device shown as peripheral 1, and processor 2 handles all computational problems and data storage using peripheral 2. In this circuit, data are therefore passed asynchronously back and forth between the two processors through a common RAM using dynamically allocated message blocks, creating a strong possibility for errors in communication between the two devices.

Examples

Problem 1: During a transfer of input data from processor 1 to processor 2, several bytes of data are lost, causing a malfunction. Processor 1 supposedly transfers 16-128 bytes of data into the common RAM area, then interrupts processor 2 to read out stored data. However, when the data are read out, there are fewer bytes than were stored. Where is the problem? Processor 1? The RAM? Or processor 2?

Solution: To solve this problem you need to know: How many bytes of data were sent? What were the data? How many bytes were received and what were those data? Solving this problem with just one system would be extremely difficult and would require several passes using the development system first to emulate one processor and then the other, with no guarantee that the passes would be identical. One method of acquiring this information using both systems is to set the development system to recognize the routine sending data to RAM and then to store all the data sent. Then trigger the logic analyzer to start recording all data being read in.

Setup: Since the development system will be triggering the logic analyzer in the above example, set up the equipment as shown in **Fig 1b**, with the EVENT 2 lead connected to the external-trigger input of the logic analyzer.

Now set event on the development system to trigger on each write to the global-RAM area. This setup will create a countable unit for the real-time counter.

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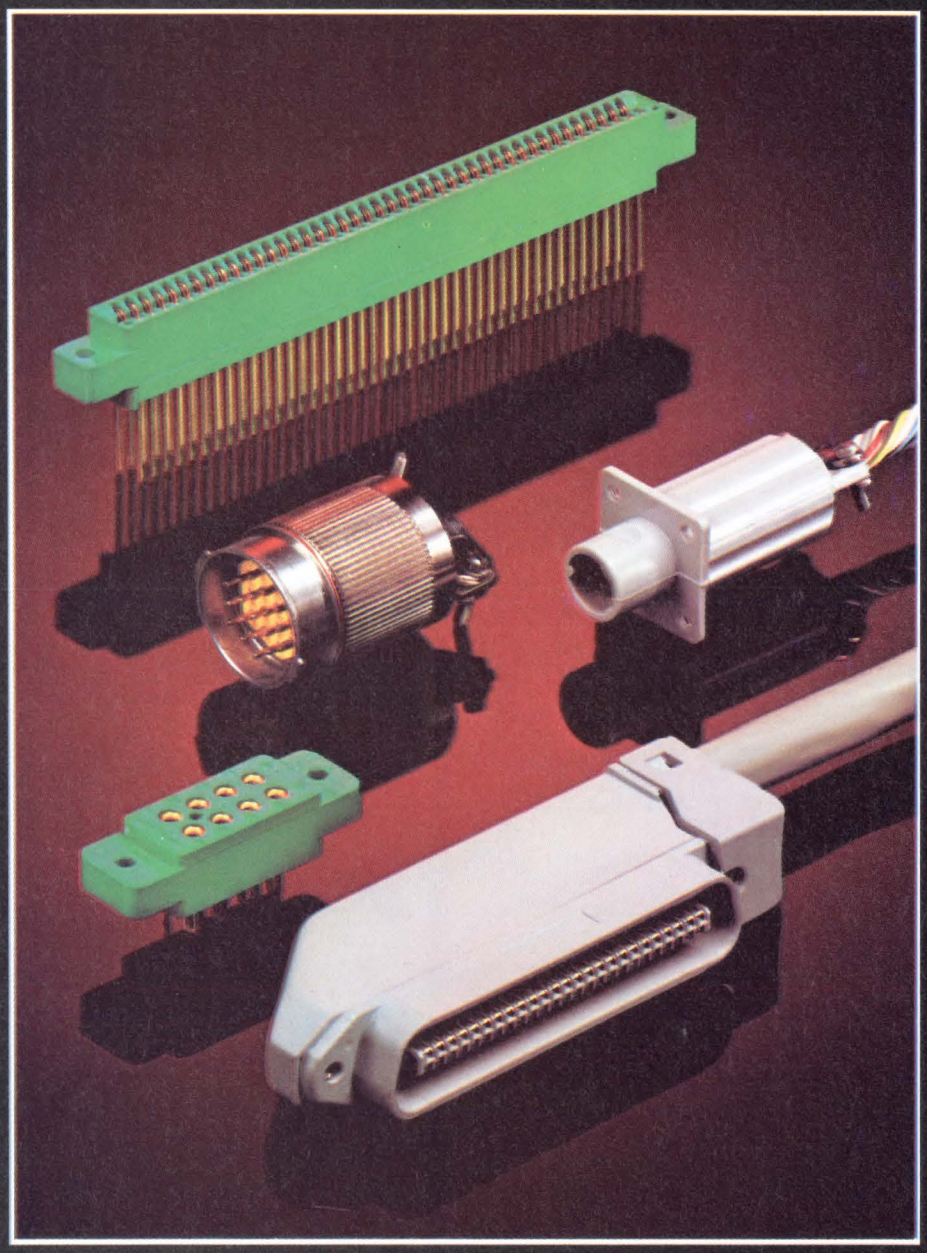

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Π
>EVT 1 CLR A>4FFF B=MW

Then set event 2 to trigger when the data are completely written. For example, if the store routine ends with a return instruction at 234C hex, then EVT2 would be:

> EVT 2 CLR A=234C B=F D=C9

Set the break command to arm mode. Doing so will stop the development system as soon as all the data to be passed have been written to the RAM.

> BIF ARM

Set the counter to count event 1s so a record will be kept of how many bytes were written.

> CNT 1

Finally, set the real-time trace to store only memory writes. This step will save the last 128 bytes of data written to RAM before the break.

> RTT MW

The development system has now been set up to determine how many bytes of data were sent to processor 2 and to save in its real-time buffer all data bytes written. The logic analyzer must now be set up to determine how many bytes of data are read in by processor 2 and to store the data in its trace buffer. After the data have been completely read in, processor 2 will be halted to examine the stored data and the common RAM locations used. First, set the 7DO2 in test 1 to look for a trigger in, which will be EVT 2 coming from the development system. Upon receiving a trigger in, the logic analyzer will branch to test 2.

```
TEST 1
   1TF
1 WORD RECOGNIZER #1
1 DATA=XX
1 ADDRESS=XXXX
1 R/W=X FETCH=X IO/MEM=X
   INT=X
1 /INTAK=X EXT TRIG IN=1
1 TIMING WR=X
1 THEN DO
1 GO TO 2
   END TEST 1
```

Test 2 will look for any read from the global-RAM area and increment counter 1 every time a read occurs. The storage qualifier is also set identically to be read from the global-RAM area, saving all the data read into the 256-word buffer. As part of test 2, word recognizer 3 should be set to trigger on the end of the read from global-RAM routine, whereupon the logic analyzer will halt the process and display the stored data.

```
TEST 2
2IF
2 WORD RECOGNIZER #2
2 DATA = XX
2 ADDRESS = 5XXX
2 R/W = 1 FETCH = X IO/MEM = 0
  INT = X
2 /INTAK = X EXT TRIG IN = X
2 TIMING WR = X
2 THEN DO
2 COUNTER # 1 0-EVENTS
2 0-INCREMENT
2 OR IF
2 WORD RECOGNIZER #3
2 DATA=C9
2 ADDRESS=2A43
2 R/W=X FETCH=1 IO/MEM=X INT=X
2 /INTAK=X EXT TRIG IN=X
2 TIMING WR=X
2 TRIGGER
2 3-ZERO DELAY
2 1-SYSTEM UNDER TEST HALT
2 0-STANDARD CLOCK QUAL.
END TEST 2
QUALIFY
Q STORE ON
Q WORD RECOGNIZER #2
Q DATA = XX
Q ADDRESS = 5XXX
Q R/W = 1 FETCH = X IO/MEM = 0
  INT = X
Q /INTAK=X EXT TRIG IN=X
Q TIMING WR = X
END QUALIFY
```

At this point, processors 1 and 2 are both halted, the development system buffer contains a record of the up to last 128 bytes written to the global RAM, and the system counter contains the number of bytes sent. The logic-analyzer buffer contains a record of all the data read in from the global RAM, and counter 1 contains the number of bytes read in. These data can now be used to determine how many bytes were lost and which bytes they were, providing a much better insight into the malfunction or

continued from page 40

consideration unless recession runs longer or deeper than is currently projected. Instrument makers, also, will have to learn to cope with strong market pressures to end the trend of adding bells and whistles at any price.

Trends

Users generally prefer μP development equipment with multi-processor support capability. With this in mind, manufacturers offer low-cost solutions which provide multi-user capability, which extend existing computer systems capability and which improve price performance ratios. A microsystem emulator would allow a host computer to serve as a μP development system or add another work station to a development system. Such an emulator should support the 6800, 6802, 8080, 8085A, Z80A and 8048 family, including the 8021, 8035, 8039, 8041A, 8049 and 8748. Base price of such a unit would be about $3000 with emulator cards from $1150 to $2000.

Universal systems usually offer one set of commands to control the development/design aid, which means that they are easier to learn and therefore easier to use. Some universal development systems offer less technical features than the dedicated systems by the very nature of their universality. However, our in-circuit emulation is generally considered superior to Intel's ICE in several respects, including the ability to deal with the system under test in real time, at system clock speeds, eliminating the necessity of introducing artificial wait states.

Although most μP manufacturers offer some form of in-circuit emulation, they offer it only as a plug-in add-on to their dedicated micro development systems. Thus, only one designer can use the ICE features at one time – and only on that manufacturer's μP.

Distributed ICE, a concept we pioneered, lets you plug units into a development system (whether it's a manufacturer's MDS or a general-purpose computer), download the program to be tested, and use the Microsystem Emulator as a stand-alone tester.

Universal μP development system manufacturers like Tektronix, Hewlett-Packard, GenRad and Millennium are providing development systems that are superior to dedicated systems. Since they specialize in development systems, and because they have no vested interests in selling chips, the companies can offer systems well-tailored for the system designer.

pointing to a much more specific area to be traced.

Problem 2: Processor 1 receives data from peripheral 1. Based on these data, processor 1 will request one or more tasks of processor 2. During a certain known sequence of two requests, processor 2 fails and returns erroneous data to processor 1, causing processor 1 to crash. These operation requests are specified by sending processor 2 a unique op-request code and any required data needed to perform each task. For the first request in the troublesome sequence, processor 1 passes a 2C hex and several data bytes to processor 2. For the second, processor 1 passes a D1 hex and associated data. However, somewhere into the second task, processor 2 fails, causing it to send a bad packet of data back to processor 1, but only when the other specified task was executed previously. As this sequence of requests happens randomly and is not reproducible at will without significant programming, how can data be acquired on such a randomly occurring event?

Solution: Set the logic analyzer to recognize the sequential execution of these two events using its programmable test capability. If the two requests occur in sequence, then the logic analyzer will record data only for the second task and wait for the faulty packet of data to be written to global RAM before triggering the development system, which will then capture the next packet of incoming data. In this way, the instructions creating the faulty data will be captured in the logic analyzer's memory, and the data will be held in the development system's buffer. This procedure should provide the necessary information to determine where the program is malfunctioning.

Setup: Since the logic analyzer will be used to trigger the development system, connect the two pieces of equipment as shown in **Fig 2**, with the external-trigger-output lead from the logic analyzer connected to the number 1 test-clip input on thedevelopment system. The 7D02 in this example is not equipped with a timing option; therefore, the external trigger will go high whenever a trigger command is executed.

To solve this problem, set the logic analyzer to recognize the sequence of operation requests causing the failure. Since these requests are stored and read in from dynamically allocated blocks of memory in the global RAM, identifying them as they are read in would be nearly impossible. However, the routine that reads in these operation-request blocks writes them into a specific buffer location in internal RAM before they are processed. Therefore, this location can be monitored to identify the desired incoming commands as they are written into this area.

To do this, set test 1 of logic analyzer to look for the first request of the sequence (2C hex), which will be written into the staging buffer at address 4500 hex. When this request is observed, go to test 2 and look for the next request fetched to be the second of the sequence.

```
1 IF TEST 1
1 WORD RECOGNIZER #1
1 DATA = 2C
1 ADDRESS = 4500
1 R/W = 0 FETCH = X IO/MEM =0
  INT = X
1 /INTAK = X EXT TRIG IN = X
1 THEN DO
1 GO TO 2
  END TEST 1
```

Test 2 will look for the next command written into the staging RAM at location 4500 to be a D1 hex. If it is, the system will branch to test 3, where it will start recording data until it reaches the limit or the end of the subroutine. Also, the condition where two consecutive 2C requests occur must be taken into account. If this condition occurs, the system should stay in test 2, not go back to test 1. However, if the next write to address location 4500 is not a D1 or another 2C, then the system will branch back to test 1.

```
TEST2
2IF
2 WORD RECOGNIZER #2
2 DATA = D1
2 ADDRESS = 4500
2 R/W = 0 FETCH = X IO/MEM = 0
  INT = X
2 /INTAK = X EXT TRIG IN = X
2THEN DO
2 GO TO 3
2OR IF
2 WORD RECOGNIZER #1
2 DATA = 2C
2 ADDRESS = 4500
2 R/W = 0 FETCH = X IO/MEM = 0
  INT = X
2 /INTAK = X EXT TRIG IN = X
2THEN DO
2 GO TO 2
2OR IF
2 WORD RECOGNIZER #3
2 DATA = XX
2 ADDRESS = 4500
2 R/W = 0 FETCH = X IO/MEM = 0
  INT = X
2 /INTAK = X EXT TRIG IN = X
2THEN
2 GO TO 1
  END TEST 2
```

In test 3, the logic analyzer is set to record the next 256 events performed by processor 2 or to record until the end of the requested routine specified by word recognizer 3. If the 256-byte

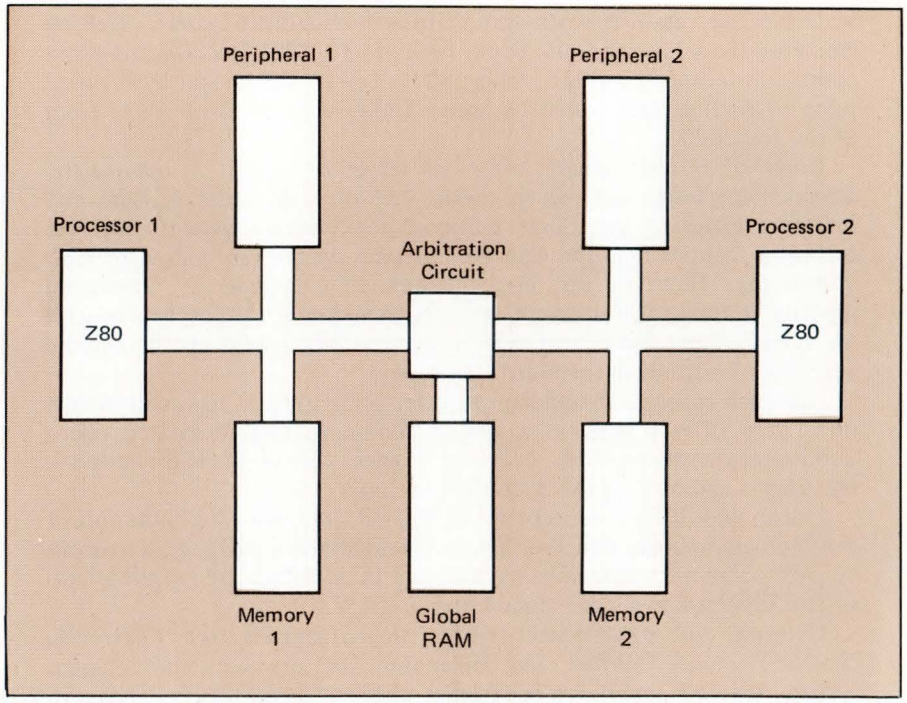

Fig. 2. CPU 1 handles I/O from Peripheral 1; CPU 2 handles computational problems and data storage from Peripheral 2. With data in this hypothetical circuit flowing asynchronously between the two CPU's through a common RAM, errors are possible. Methods described in this article explain how to find such errors when they occur.

limit is reached, the system will branch to test 4, where the program will wait for the end of the requested routine before triggering the development system. However, if the end of the requested routine is reached before the 256-byte limit, test 3 will also generate the trigger for the development system.

```
TEST 3
3IF
3 COUNTER #1 = 256 0-EVENTS
3THEN
3 GO TO 4
3OR IF
3 WORD RECOGNIZER #4
3 DATA = C9
3 ADDRESS = 2E20
3 R/W = X FETCH = 1 IO/MEM = X
  INT = X
3 /INTAK = X EXT TRIG IN = X
3THEN
3 TRIGGER
3         3-ZERO DELAY
3         0-SYSTEM UNDER TEST
          CONT.
3         0-STANDARD CLOCK
          QUAL.
3 ELSE
3
3 COUNTER #1 0-EVENTS
3           0-INCREMENT
3 QUALIFY
3
   END TEST 3
```

In test 4, word recognizer 4 watches for the return instruction at 2E20 hex, signifying the end of the subroutine, before writing to global RAM, which is the last routine executed by the third operation request. When global RAM is written to, the logic analyzer will trigger the development system to start recording the next sequence of data read in from the global RAM.

```
TEST 4
4IF
4 WORD RECOGNIZER #4
4 DATA = C9
4 ADDRESS = 2E20
4 R/W = X FETCH =1 IO/MEM = X
  INT = X
4 /INTAK = X EXT TRIG IN = X
4THEN DO
4 TRIGGER
4         3-ZERO DELAY
4         0-SYSTEM UNDER TEST
          CONT.
4         0-STANDARD CLOCK
          QUAL.
   END TEST 4
```

Now the development system must be set up to receive the incoming trigger from the logic analyzer and to record the desired data sent by processor 2. Set event 1 to trigger on the input supplied by the external-trigger output from the logic analyzer connected to test clip 1.

```
>EVT 1 CLR T = 1XXXXXXXX
```

Event 2 must now be set to halt processor 1 when the reading of data from global RAM is complete. The global-read routine ends with a return instruction at 2EC4 hex, so event 2 will be:

```
> EVT 2 CLR A = 2EC4 D = C9
B = F
```

To halt processor 1 on event 2, use the break if command. Since processor 1 should break on event 2 only if event 1 has occurred first, the ARM condition is required.

```
>BIF ARM
```

Like processor 2, processor 1 writes all the data read in from global RAM into an internal buffer for processing. Therefore, the development-system storage qualifier can be set to store only memory writes, thereby saving the last 128 bytes sent by processor 2.

```
> RTT MW
```

When the whole program is run, upon executing the sequence of operation requests 2C and D1, the logic analyzer will trigger the development system and also save 256 of the last instructions executed during the third request. The development system, in turn, will then save 128 bytes of the data sent by processor 2. By using the development system and logic analyzer in one operation, you can obtain significant data from both processors specifying the events leading up to a system failure. With normal methods of troubleshooting using one device at a time, obtaining these data could take many additional passes, with no guarantee that each pass would cause identical errors.

When used as described, the combination of a development system and logic analyzer that can communicate like the 8002A and 7D02 can provide many sophisticated features for troubleshooting multiprocessor circuits. Other techniques can prove useful, too. You can set up the development system to trigger the logic analyzer so it views hardware timing relationships asynchronously. Or, your can set up the logic analyzer to trigger the development system in a multistep relationship, prividing another rung in the arming ladder that leads up to a specified event. Used together, the development system and logic analyzer can make the rough job of debugging a multiprocessor significanly easier.

Single-Chip Microcomputer Controls Keyboard Scanning

John Wharton.
Intel Corp.

Falling microprocessor prices now make it possible to give a host of previously "passive" consumer products, such as clocks or television sets, enough intelligence to interact with human operators. These products are thus given an edge in a special capability-oriented marketplace. As a result, engineers are designing more products that require an efficient human interface. Although the most pervasive interfaces for this purpose are simple keyboards and displays, engineering decisions now involve more complex considerations.

Three display types

Choosing a display type involves trade-offs on character size, color, font, total power consumption, power supplies needed and cost. Despite advantages, they typical bright red light emitted is (1) considered harsh by some, (2) may present a conflict in applications (such as on automotive information panels) in which red is for warning and emergency. Furthermore, this display may "wash out" in bright sunlight, and since light emitted is monochromatic,

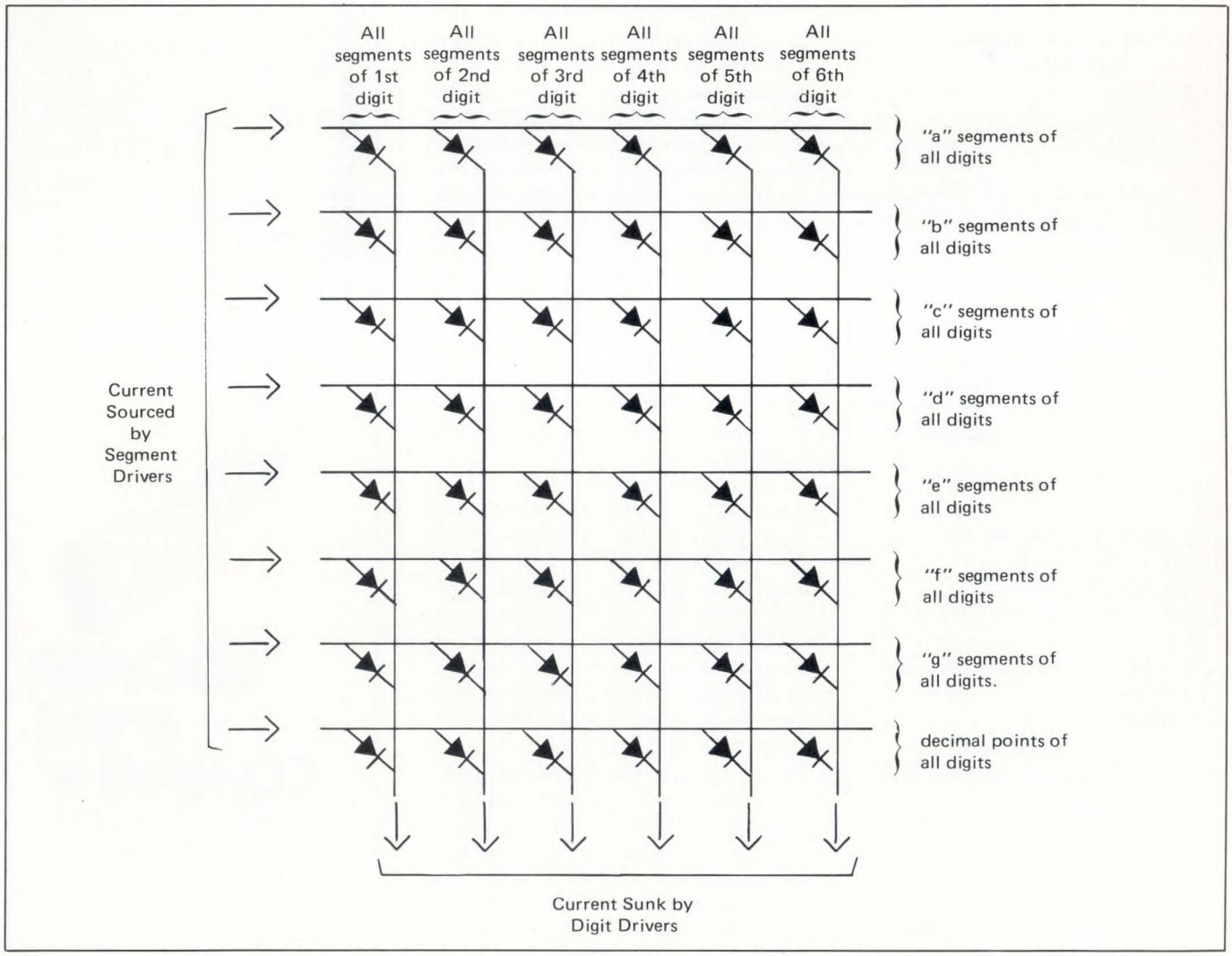

Fig 1. Schematic representation of six-digit, seven-segment common-cathode L.E.D. multiple display.

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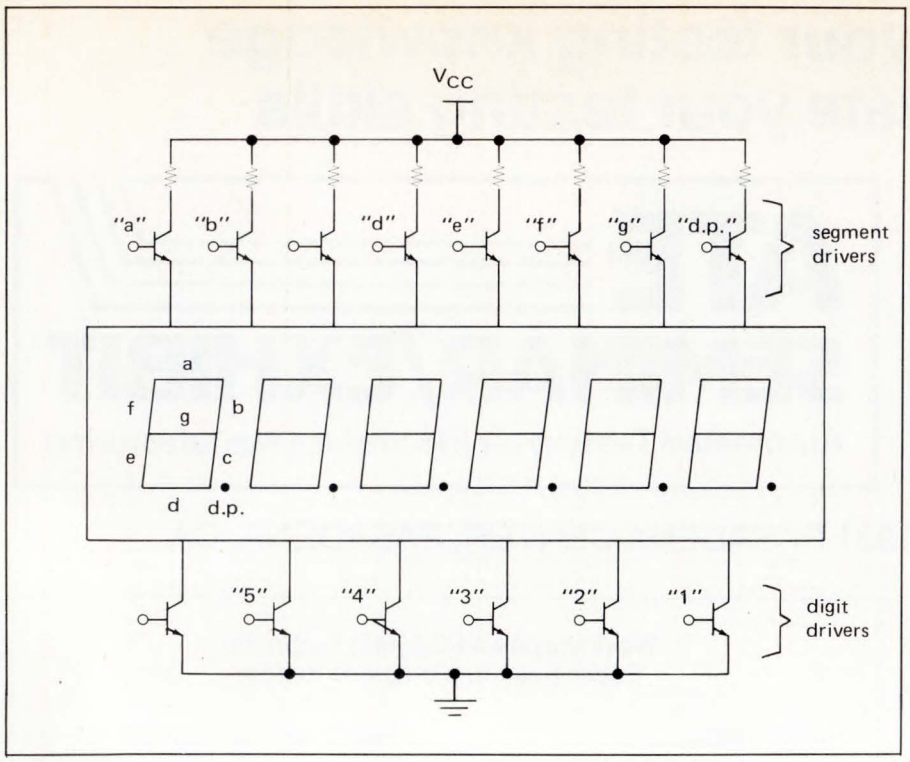

Fig 2. Segment and Digit Drivers used with six-position seven segment L.E.D. display.

optical filters cannot modify the display.

PCG (planar gas discharge) displays operate by placing a high potential (up to 200 V) across electrodes in a glass tube filled with neon gas and are extremely bright and clear. Character shapes are more flexible because the electrode shape determines their structures. PGD displays cost somewhat more than LEDs and require high voltages or AC power for operation.

VFDs (vacuum fluorescent displays) offer a compromise of sorts, and are rapidly becoming "in vogue" in consumer electronics. Since the displays use a filament heated to less incandescence than the cathode, the anode operates with a potential applied to the segments at a considerably lower level (12 to 30 V). This type of display offers the same advantages as PGDs and emits a pleasant blue-green color. Moreover, since the phosphor coatings on the electrodes emit a very wide spectrum of light, inexpensive plastic filters can adjust the display color through a wide range. While vacuum fluorescents do not require very high voltages, the designer usually has to provide low (1-3V) and high (12-30V) voltage supplies for the filament and display characters, in addition to the usual 5Vcc.

Static vs multiplexed displays

All three types of display may be implemented in a static or multiplexed configuration. The multiplexed operation mode offers advantages of less expensive display arrays, less support components, lower fabrication costs and increased system reliability. Moreover, the advent of inexpensive single-chip μCs now removes the drawback of requiring more costly and complicated logic to implement multiplexed displays without appearing to flash or flicker.

Any multiplexed displays, whether implemented in LEDs, PGD tubes or VFDs can be considered character segments all interconnected in a regular 2D array. One terminal of each segment is connected in common with other segments of the same character; the other terminal is connected with corresponding segments of the other characters **(Fig 1)**. (This is the wiring plan with LEDs; PGD tubes use a common cathode for the segments of each character, with current flowing through the neon gas; and VFDs use a flat grid in front of each character, similar to the grid in a vacuum tube triode, to switch characters on and off.)

When the display appears ON, different characters are actually being time-multiplexed: various characters are not ON all at once; rather, only one character at a time is energized. As each character is enabled, some combination of segment drivers is turned ON, with the result that a digit appears on the enabled character. For example, in **Fig 2**, if segment drivers "a", "b", and "c" were ON when the sixth character position was enabled, the digit "7" would appear in the left-most place. Each character is enabled in this way, in sequence, at a rate fast enough to ensure that human eyes perceive display characters to be ON constantly,

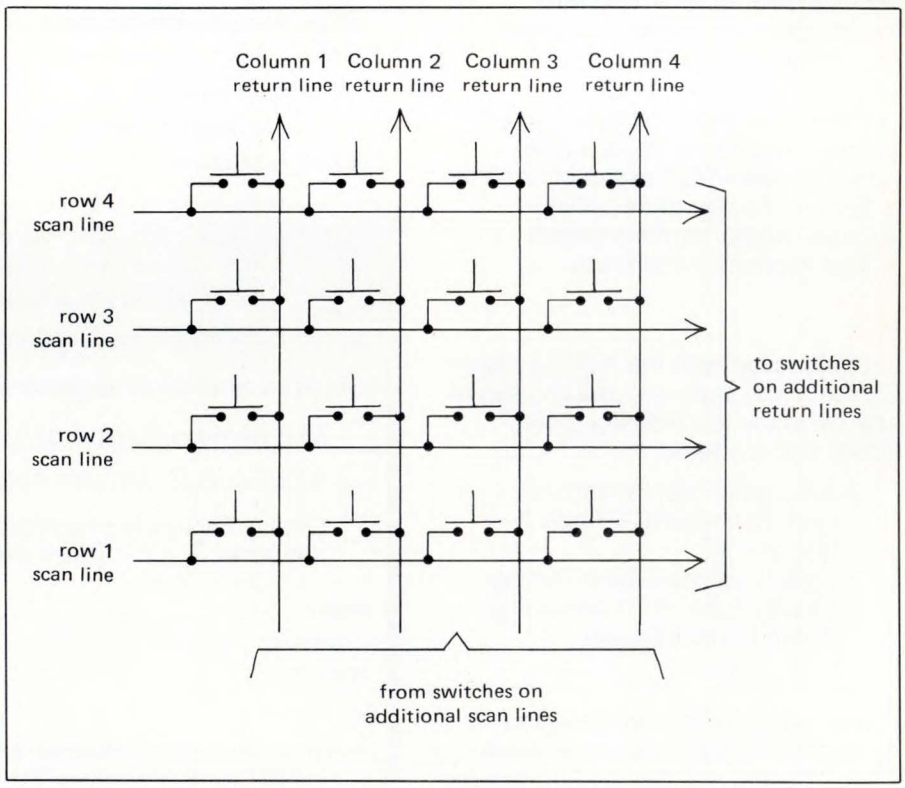

Fig 3. Schematic of X-Y matrix multiplexed keyboard.

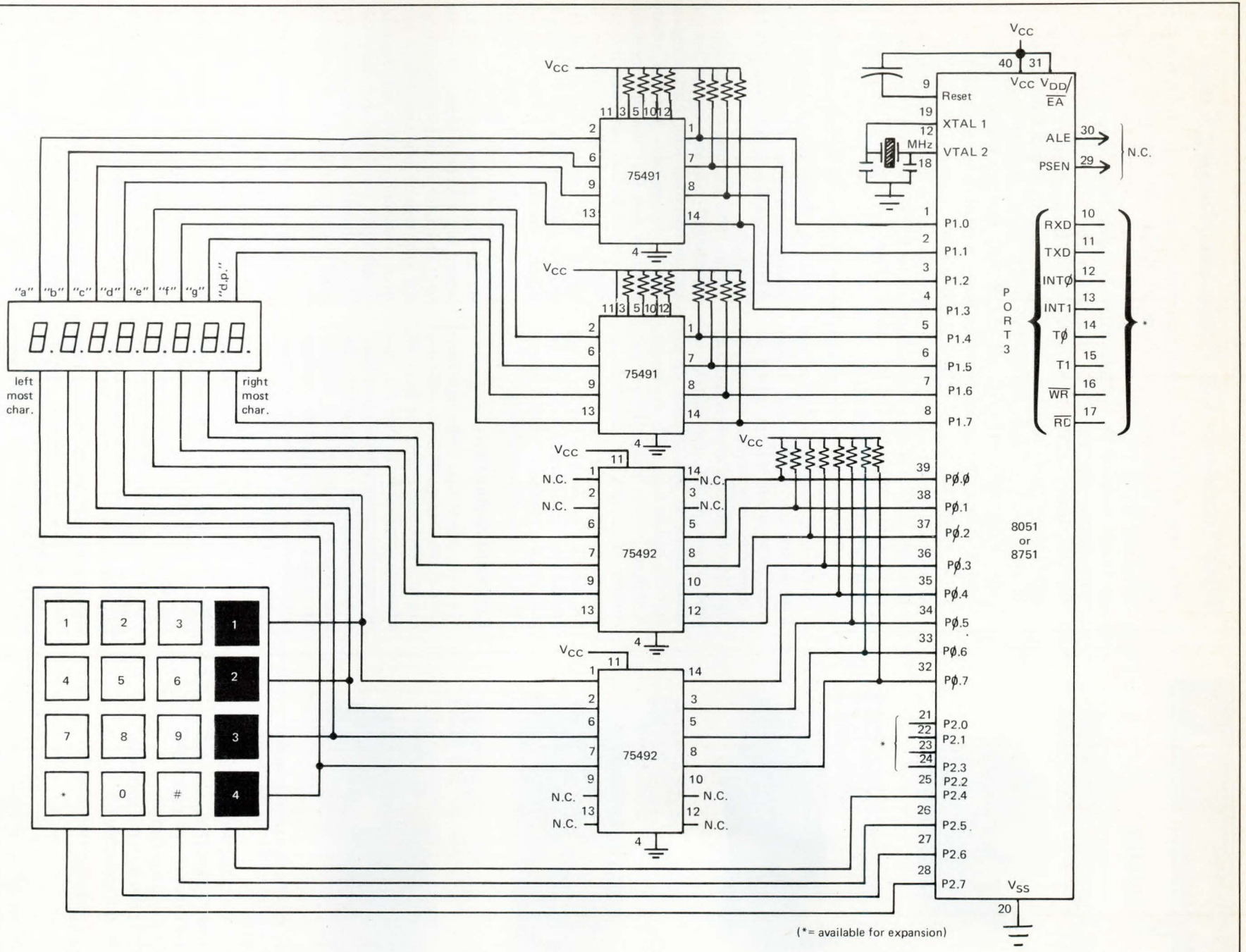

Fig 4. Prototype system schematic.

8048 Successors Cut Production/Stocking Costs

Intel's recent MCS-48 family extension, the 12-KHz 8051, has 4 kbytes of ROM and 128 bytes of RAM and upgrades the 1-kbyte of ROM fourfold. As we go to press, activity in this area is brisk. National's 6-MHz 8050 is operating code and pin-compatible with the 8048. Execution times are typically 2.5 μs for the slower 8050; 1 μs for the 8051. Both chips provide cost advantages over the 8048; since several programs can now reside in these two micros, unlike the 8048, they can serve multiple uses, with the desired routine(s) called up for that specific application. Thus, instead of separate 8048 production runs and multiple stocking for different applications – such as for I/O control, displays or keyboard control – now only one chip is needed, with subsequent reduction in ROM masking fees, and production and inventory costs. Past investments in 8048 software are also protected.

Since each character is ON for only a small fraction of the total display cycle, its segments must be driven by a proportionately higher current, so that their brightness averages out over time. Consequently, the display requires character and segment drivers that can handle high levels of current. A designer can use various driver types, ranging from specially-designed circuits to integrated or discrete transistor arrays. The selection depends on several factors, including type of display, its size, number of characters and polarity of individual segments.

Keyboard application

The same signal that turns each character of the display ON can enable one row of a keyboard matrix. In that row, any keys actuated at the time then pass the signal to one of several return lines, one corresponding to each matrix column **(Fig 3)**. Reading these control-line states and knowing the enabled row makes it possible to compute which (if any) of the keys are depressed.

Note that the keys in **Fig 3** need not be physically arranged in a rectangular array. The words "row" and "column" refer to short and long dimensions of the switch array as they are connected electrically, whether or not this corresponds to physical layout. In fact, keyboard scanning has been used in many applications that do not involve keyboards at all. For example, typical burglar alarm systems use scanning to read a large number of intrusion sensors, and many pin-ball machines scan roll-over switches activated by a steel ball.

In typical μC-based systems, subsystems designed especially for controlling keyboards and displays, handle this rapid character sequencing or multiplexing. These special-purpose integrated subsystems include the Intel 8279 Programmable Keyboard/Display Interface.

The same μC that controls display refreshment can also control normal system operation (and further reduce cost.). At periodic intervals (every msec or so), the computer suspends whatever it is doing as its primary control function and calls a subroutine to refresh the display. This subroutine quickly turns off all display segments, disables the character being displayed, enables the next step, looks up the next character to be displayed, turns on the appropriate segments and processes any keyboard input. After the next character is enabled, the processor may resume whatever task it had been performing before interruption. Today's μCs are so fast that the whole display updating task consumes only a small fraction of the overall processor time.

Moreover, since a computer (rather than a standard decoder circuit) turns the segments OFF and ON, the display repertoire can include patterns for characters other than decimal digits, such as hexidecimal characters, special symbols and many letters of the alphabet. With sufficient imagination, engineers can exploit this capability in a number of applications. (For example, vending machines that interact with users.)

In essence, a μC can handle more functions than the keyboard and display driving logic. Therefore, the added cost of these features in a system is minimal. Total system cost can actually decrease due to the fact that the extremely low price for standard X-Y matrix keyboards and integrated displays can make their use often more

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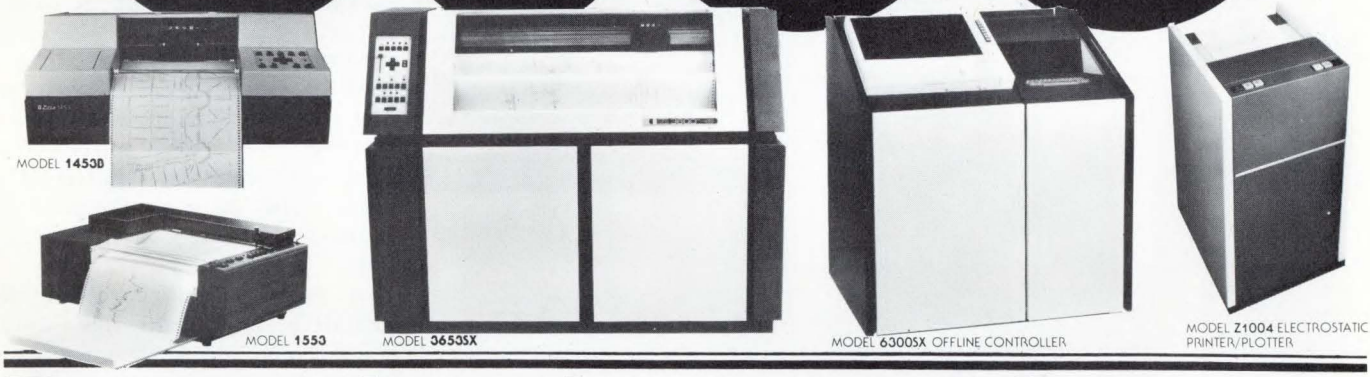

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cost-effective than even a handful of discrete switches and indicators. Thus, a manufacturer can furnish the additional flexibility of keyboard input and display output "free" to such inexpensive consumer products as games, thermostats and tape recorders.

Software

Adding a keyboard input and display output capability to a variety of products that already use μCs requires implementing appropriate software code. In addition to basic software for driving a multiplexed display and/or scanning and debouncing an X-Y matrix of key switches, the system also requires a collection of utility subroutines. These will implement the most commonly-used keyboard and display functions, such as copying simple messages onto the display or determining the encoded value of each position in the switch matrix. Since each potential application contains its own unique combination of keys and display characters, the program requires very little modification to interface a wide variety of hardware configurations. **Table 1** describes a typical collection of keyboard/display utility subroutines and an explanation of parameters that would be passed into and out of each.

Intel has developed a complete software package, including all the utilities listed in **Table 1** for interfacing members of the MCS-51™ family of single-chip μCs with a wide variety of keyboards and displays with a minimum of external components. The core of the MCS-51 family, the 8051, is an expandable single-chip micro that combines an eight-bit CPU with 4K bytes of program ROM, 128 bytes of RAM, 2 timer/counters and 32 programmable I/O lines in a single 40-pin package. Other μCs based on the 8051 include the single-chip micro with EPROM program memory, 8751; and the less expensive 8031, which relies on up to 64 kbytes of external program memory.

The compatiblity of the above listed processors allows the same code with minor modifications to run on any members of the family. The versatile architecture and byte-efficient, applications-oriented instruction set of the MCS-51 family allows the entire package to fit into about 250 bytes of internal ROM and leave 94% of the program memory for a program to cook the perfect piece of toast, analyze a chess or backgammon board, or whatever else is the appliance's or game's primary task. Maintaining the display and scanning the keyboard consume less than 4% of the processor's time.

A single subroutine (called "REFRESH") implements the display multiplexing and keyboard scanning by using the same signal to enable one character of the display and to strobe one row of the X-Y key matrix. The system must call the subroutine often enough to ensure that the display characters do not flicker – at least 50 complete display scans/sec. To allow the designer to make cost tradeoffs on switch selection, he can set the debounce time to be any desired number of complete scans. Thus, the debounce time is a function of the scan rate and the value of the debounce constant.

The assembly language code for the REFRESH routine appears in the printout. In the macro assembler listing, one of the MCS-51 internal timers generates interrupts that serve as time bases for the refresh subroutine. Alternate time bases could be an external oscillator (driving an interrupt pin or polled by an input), a software delay loop in the background program, or

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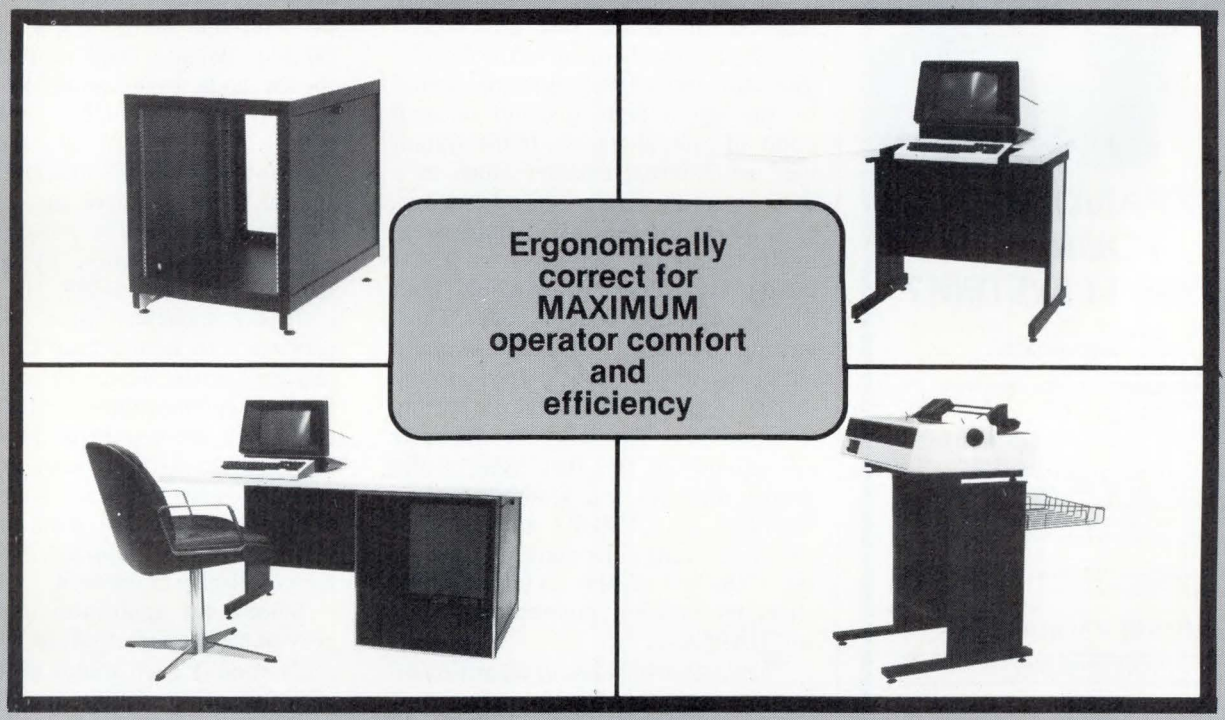

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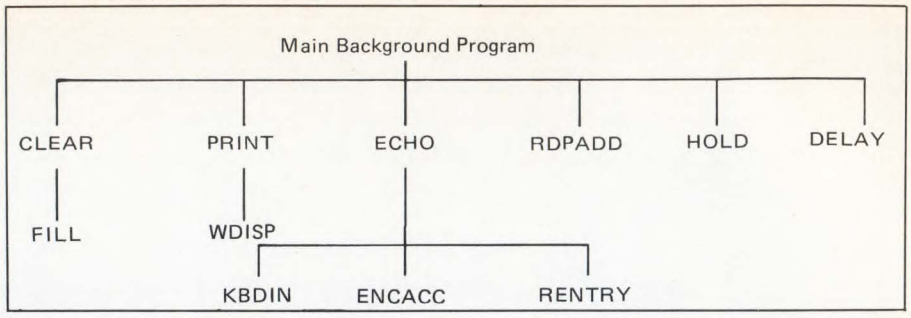

Fig 5. Subroutine interrelationships.

periodic calls to the subroutine from throughout the user's program at appropriate places. The REFRESH routine selects register bank 1 for the needed registers.

The algorithm for driving the display uses a block of internal RAM as display registers, in which one byte corresponds to each character of the display. The eight bits of each byte correspond to the seven segments and decimal point of each character. If the system uses an external encoder (such as a BCD to seven-segment decoder/driver, or a ROM for generating sixteen-segments "starburst" patterns from ASCII input), the table entries would hold the appropriate character codes. Thus, writing characters to the display really entails writing segment patterns to the display register; the actual outputting is automatic. The leftmost character corresponds to the first byte of the display registers, and is accessed when NEXTPL or CURDIG are equal to zero (see listing); the rightmost character is the last display byte, when the character position pointers are equal to CHARNO-1.

The keyboard scanning algorithm requires a depressed key for some number of complete display scans to be acknowledged. Since the system is intended for one-finger operation, the algorithm implements a two-key rollover/n-key lockout. However, you could modify it to allow, for example, one key in the matrix to be used as a shift key or control key to be held down while another key in the matrix is pressed. A note within the body of the listing shows the point where this would be done.

Note that you can depress no more than two keys at a time, unless you place diodes in series with all of the switches – certainly not the case for cheap keyboards – because some combinations of three depressed keys result in the perception of a phantom fourth key. The phantom key would be in the fourth corner when three keys forming a rectangular pattern (in the X-Y key matrix) are down.

When a debounced key is detected, the number of its position in the key matrix (left-to-right, bottom-to-top, starting from 00) is placed into RAM location KBDBUF. An input subroutine in the background program then need only read this location repeatedly to determine when a key has been pressed. When a key is detected, a special code byte should be written back to into KBDBUF to prevent repeated detections of the same key. The routine KBDIN demonstrates a typical input protocol and a method for translating a key position to its associated significance, by accessing table LEGENDS in ROM.

In this implementation of the display scan, we assume that there will be relatively little call for I/O other than for the keyboard/display. If this is the case, then the system needs no additional external logic (such as one-of-eight decoders or seven-segment encoders), though it does need current or voltage drivers to supply power to the type of display being used.

Since each application is unique, provisions are made to allow the user to easily modify such things as the number of characters in the display or the polarity of the drivers used. Throughout the program, symbolic values like CHARNO are used to specify variable values, in this case the number of characters in the display. By specifying that "CHARNO equals 6" at one spot in the beginning of the listing, for example, several other sections of the program in which CHARNO is an operand will be modified automatically to handle a six-digit display. (A more detailed explanation of these variables is included at the beginning of the program listing available on request as noted at the end of this publication.)

Port assignment is also at the discretion of the user. All port references in the listing are "logical" rather than physical port names. The port used to specify which character is to be enabled is referred to as PDIGIT. The output

Continued on page 73

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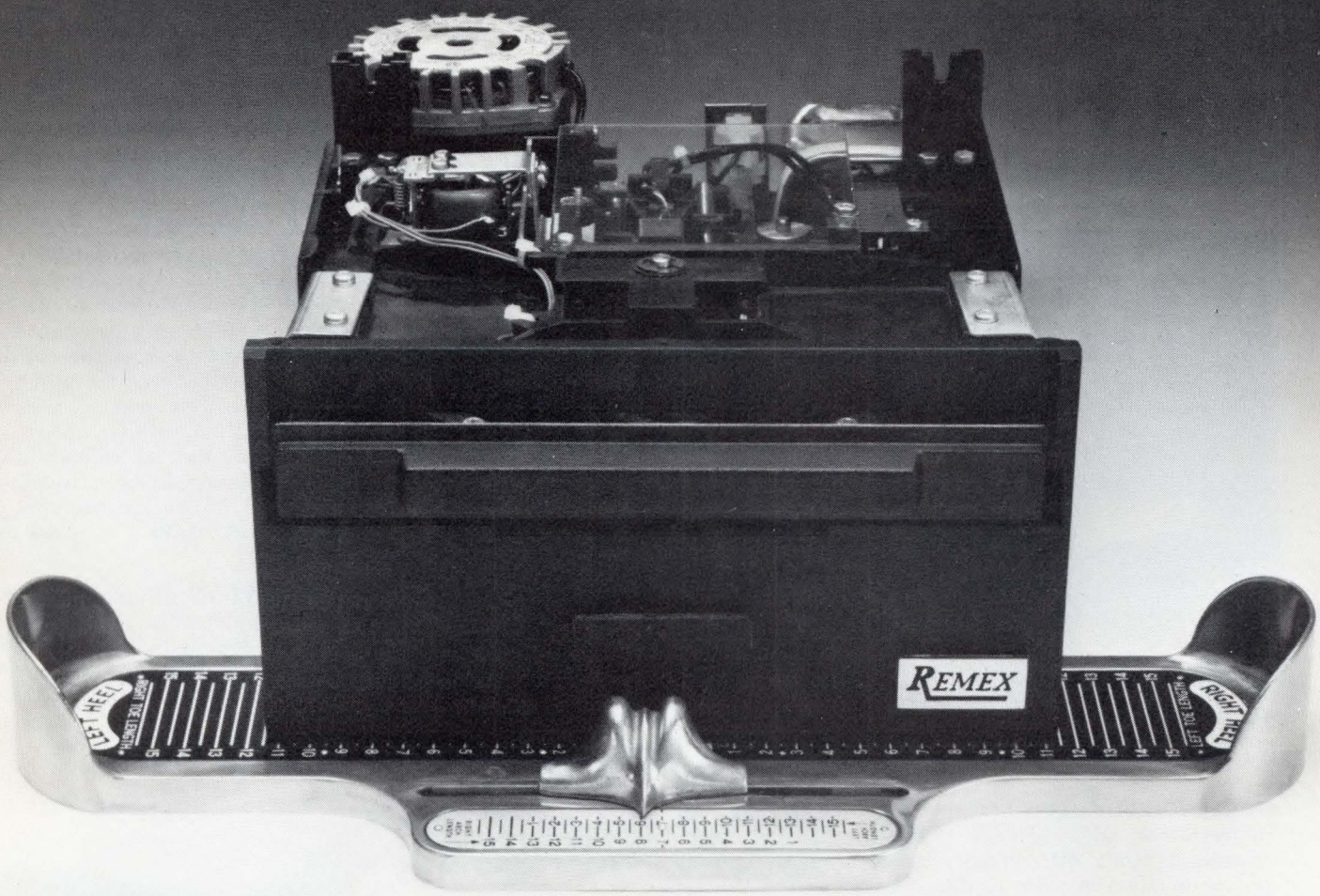

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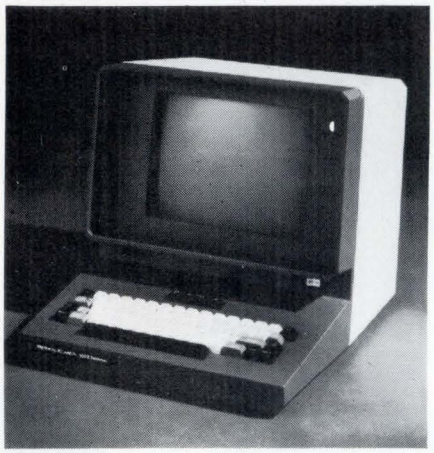

mode; and support for dual character sets. Model 550B is $966. **Perkin-Elmer,** Terminals Div, 360 Rt 206 S., Flanders, NJ 07836 **Circle 134**

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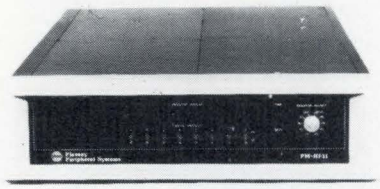

sion kits to provide a maximum 1.5MB of MOS memory. The PM-RF11B supplies 512 kB of MOS memory in a 10.5″ chassis. This chassis allows expansion up to 4MB of dynamic MOS memory by the addition of the PM-RF11B backplane and PM-RF11E expansion kits. The PM-RF11A is $9733, 60 days ARO. **Plessey Peripheral Systems,** 17466 Daimler Ave, Irvine, CA 92714 **Circle 135**

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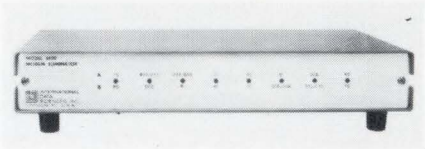


or sync modes, and with terminals configured for half or full-duplex operation. Features provide internal strap selections for primary and secondary RTS/CTS delays, RC controlled by DCD, switched network or private line operation, ring memory functions, and clock source. Data terminal equipment can be located up to 50 feet from the Modem Eliminator. Model 6100 is $360, 60 days ARO. **International Data Sciences, Inc,** 7 Wellington Rd, Lincoln, RI 02865 **Circle 133**

INCREASED CAPACITY TAPE The length on each reel of 701 Black Watch computer tape is 33% greater on the 8 1/2″ reel for a total capacity of 1,600 feet. The 10 1/2″ reel supplies 3,200 feet of tape. The 701 tape has a textured backside coating for protection against physical damage and loss of data. **3M,** Dept DR80-15, Box 33600, St. Paul, MN 55133 **Circle 136**

INDUCTIVE KEYBOARD uses a "pulse transformer" principal which offers a high signal to noise ratio. Closed key coupling produces a peak output which is superior in magnitude to capacitive technology, and minimizes the effects of dust, moisture, etc. The inductive keyboard has solid-state switching. Other features include USASCII encoding, N key rollover, 100 million cycles or more, electronically latched all cap key, and reliability of 45,000 hours MTBF or greater. Optional features include: domestic or international keycap nomenclature; LED indicators for specific key functions; an enclosure; inverted ASCII, or EBCDIC

logic. $100, delivery in Dec. **Tec, Inc.,** 2727 N. Fairview Ave, Tucson, AZ 85705 **Circle 146**

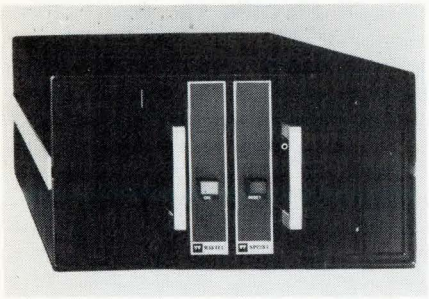
INTERSYSTEM COMMUNICATION PACKAGE This communication software package permits communication between the GenRad/futuredata 2300 series development system and a host (computer or modem) via an RS232 interface. ICOM has 4 basic modes. The command mode allows the user to set baud rate; parity; names of files; and special characters to be deleted or used for control. The interactive mode causes the system to appear as a terminal to the modem or computer. The receive and transmit modes permit the transfer of files between the host system and the development system. ICOM is available without charge to purchasers of the relocatable disk operating system (RDOS). **GenRad/futuredata,** 5730 Buckingham Pkwy, Culver City, CA 90230 **Circle 132**

NEW SPRINT 68 μC functions as a control computer, or as a development system for developing such turnkey systems. New options include a downloader and additional backplane slots.

Other options include a C compiler, and parallel, analog and 488 GP1B interfaces. The basic model includes a 6800 MPU, 48K RAM, RS-232C serial I/O, WIZRD multitasking disk operating system, editor, assembler and 12K BASIC. ($3995). **Wintek Corp,** 1801 South St, Lafayette, IN 47904 **Circle 130**

DATA ACQUISITION AND MEASUREMENT INSTRUMENTATION CATALOG This 6 page illustrated catalog contains United System's line of test and measurement instruments. In addition to digital multimeters, thermometers, calibrators, dataloggers, printers, panel mount instrumentation, counter timers, comparators and load controllers, the catalog details DigiTec's new automatic test system which is a custom combination of their standard product line test and measurement instruments. **United Systems Corp,** 918 Woodley Rd, Dayton, OH 45403 **Circle 131**

SYNCHRONOUS MODEM This new member of the Micro400 Local Dataset family operates at speeds to 19,200 bps over unloaded private line metallic circuits supplied by the telephone company. It is offered either in a tabletop enclosure or in a rack-mount chassis which holds 16 units. The small size and light weight (2 pds) simplifies



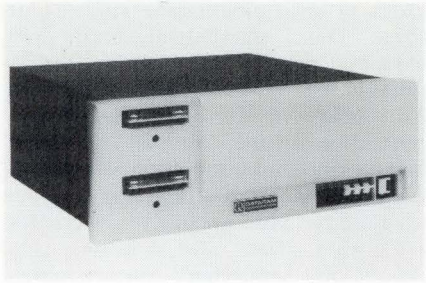
installation and replacement. Built-in loopback tests and data activity displays facilitate troubleshooting. Model 421 is $330 in the standalone version and $260 as a rack-mount card, 60 days ARO. **Micom Systems, Inc,** 9551 Irondale Ave, Chatsworth, CA 91311
Circle 145

PASCAL FOR μC DEVELOPMENT compiles directly into 8080/8085 machine code, resulting in faster and more compact code. The first offering supports the Intel 8080 and 8085 μPs. Source code developed for the 8080 and 8085 will compile to object code for the Intel 8086, Zilog Z8000 and Motorola 68000 as the compilers become available. Extensions for the Pascal 8080/8085 Compiler include an I/O extension allowing an ORIGIN attribute to assign variables to specific memory addresses. It has Interrupt Handling and Linkage to Assembly Language Routines so that the compiler is compatible with the TEKDOS (8002A operating language) linker. Pascal generated code can therefore be linked to assembly code. The Pascal 8080/8085 Compiler is $1950. **Tektronix, Inc,** M/S 76-260, Box 1700, Beaverton, OR 97075 **Circle 137**

DETECTOR/PREAMPLIFIER combines high sensitivity and speed for fiber optic data communications systems. It offers a photo sensitive diode detector and trans-impedance amplifier on the same chip. With responsivity of 30 mV/μW (at V_{CC} of +5V), the MFOD404F will sustain data rates up to 10 Megabaud/sec over medium distances. It is designed for use with the AMP compatible metal fiber-optic connector barrel. The MFOD404F is $37 (1-24), $32 (100-499). **Motorola**, Box 20912, Phoenix, AZ 85036. **Circle 185**

INTERACTIVE PLOTTING PROGRAM accepts English-like, one word commands with up to 4 arguments. It is fully self-documented and can read commands from a computer file. The program's Executive mode defines the area to be used and the range of values to be plotted. The Symbol mode defines a figure, or symbol, which may be displayed later at any point, with any rotation, and scaled to any size. The Plot mode allows selection of a point plot, a solid line plot, a dotted line plot, a dashed line plot, and a bar chart. Axes may be defined, or the program can do the scaling automatically. Executable copies of DL100 are available for DEC PDP-11 computers using he RT-11 or TSX operating systems, with Tektronix-compatible graphics devices. $650 for a single-system license, OEM discounts for multiple copies. **Syscon Design, Inc.,** 815 Manhattan Ave., Suite F, Manhattan Beach, CA 90266.
Circle 191

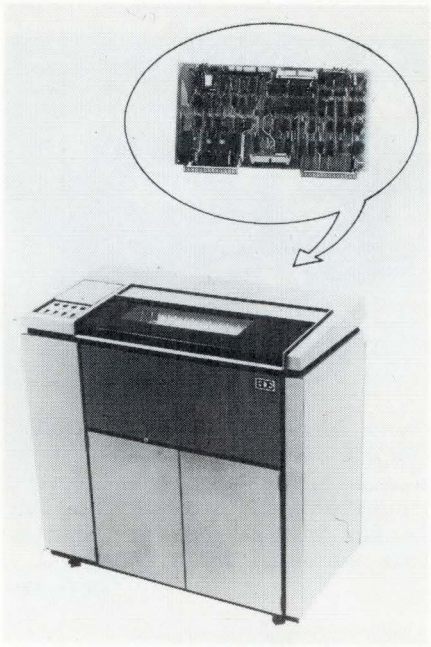
7″ LSI-11 CHASSIS contains 8 quad slots and 2 DEC TU58 cartridge tape drives. The 19″ rack mountable unit provides front loading capability for the TU58 cartridges and LSI-11 system modules. The B04 has 24A of +5VDC and 4A of +12VDC. The operator's console does not occupy a backpanel slot. The chassis is switch-selectable to operate on either 115VAC



or 230VAC. $2900 including chassis, backpanel, power supply, fans, operator's console, chassis slides, two TU58s, and the TU58 controller, 60 days ARO. **Dataram Corp**, Princeton-Hightstown Rd, Cranbury, NJ 08512 **Circle 142**

IC MEMORIES. MOS static and dynamic RAMs, EPROMs and EEPROMs, and Bipolar ECL and TTL compatible RAMs, are described in a new catalog entitled "IC Memories." Individual data sheets provide detailed information on each Hitachi memory; data includes block diagrams, tables, and graphs covering such characteristics as access times, voltage requirements and R/W cycles. **Hitachi America, Ltd,** 1800 Bering Dr, San Jose, CA 95112
Circle 196

μP-BASED PRINTER for the Hewlett-Packard 300/3000 Series 30/33 minicomputers, prints at up to 1800 lpm. The controller includes a Z80 μP, an Intel 8291 talker/listener for interfacing with the GPIB along with associated memory and logic circuits. The HPI-33 program consists of 3 individual modes, the program control mode, the transfer mode, and the test mode. It also responds to self-test



commands which confirm operation of the μP, GPIB interface, printer interface and memory. Seven line printers can also be used with the HPI-33 with speeds of 300 to 1800 lpm. The HPI-33 controller is $2,500, printers from $8200 to $31,500, delivery, 30 days ARO. **BDS Computer Corp**, 1120 Crane St., Menlo Park, CA 94025.
Circle 184

675MB DISK DRIVE. This Winchester technology-based sub-system provides 675MB of random access storage in a fixed, sealed media drive. Features include light load, contact start/stop head design, and μP control of the servo to provide an average seek time of 25 ms. The average latency time is 8.3 ms, yielding a total average access time of 33.3 ms. Model 5660/5661 has a 1209 kB/sec transfer rate and is sold with a Universal Disk Controller. Up to 7 additional Fixed Module Disk Drives can operate from one UDC for a total possible storage capacity of 5.4 billion bytes from a single controller. Deliveries begin in Jan '81. The 675MB FMD with UDC will be $71,260. Additional storage drives are $61,860. **Harris Corp**, 2101 W. Cypress Creek Rd., Ft. Lauderdale, FL 33309.
Circle 176

New Products

PORTABLE DATA TERMINAL communicates with any business or private computer over standard telephone lines via a standard RS232 telecommunications interface. The user can key-in data, review it, transmit it to the computer and also access the computer to receive stored data. It operates at a baud rate of 110 or 300 bps, asynchronous, half or full duplex, and has a 16 character, 16 segment alphanumeric LED display with integrated MOS-LSI display controller. The LK-3000 with communications module (LK-2010) and acoustic coupler is $525. **Nixdorf Computer Personal Systems,** Inc, 168 Middlesex Tpke, Burlington, MA 01803

Circle 129

UNIVERSAL DEVELOPMENT SYSTEM is based on a powerful Z80 CPU with various cross assemblers. The system includes CPU with 64kB RAM, dual 300kB floppy disk drives, full 24 x 80 CRT terminal, 80 cps printer, ROM Emulation and EPROM Programmer Board with 5 kinds of cross assemblers. The UDS-1000 is US$8750 on FOB Taipei basis. **Multitech,** 977 Min Shen E. Rd, Taipei, Taiwan **Circle 195**

ENHANCED DISTRIBUTED PROCESSING SYSTEM. Four new enhancements for the Series 21 include a family of fixed removable disk drives, a remote station printer, COBOL and Extended Data Entry (EDE). The disk drives, ranging from 26-78MB, combine both fixed platters and a removable platter on a single spindle. The System 21/50 will support multiple disks from a single controller and up to 3 drives. The 2175 models range from $14,720-$28,680 with rental and maintenance agreements available. The Model 2141-1 Station Printer can be located up to 2,000 feet from the controller. Four printers, each with its own display station, can be supported by the 21/50. It prints at 45 cps on a 132-character line, with bi-directional printing employing a daisy wheel font. The printer and its CRT may operate independently. The 2141 is $4,960, rental and maintenance available. The COBOL option supports the full range of peripheral devices on Series 21. License fee is $65/month/customer, or at a one-time charge of $2500. EDE provides users with disk storage and its full range of capabilities allows adaption to the users unique requirements. All 4 enhancements are available in early 1981. **MDS,** 7 Century Dr, Parsippany, NJ 07054 **Circle 205**

64K DYNAMIC RAM BOARD requires no wait states with a 4 MHz CPU, supports front-panel operations, and is compatible with most S-100 systems. It supports memory expansion to 512K through its bank-selection system. Berg jumpers allow selection of the board's bank and the bank port's address. Additional jumpers provide flexibility in memory configuration. Any 16K block can be made bank-independent or be disabled, while all 64K can be set to come up bank-enabled on reset and power-on. The 2065, with a one-year guarantee on parts is $700. **California Computer Systems,** 250 Caribbean Dr, Sunnyvale, CA 94086 **Circle 202**

COUNTER/TIMER CARD. This programmable STD BUS card provides three 16-bit counter/timer channels with 6 operating modes each. The card adds a crystal oscillator for accurate programmed timing, a tapped clock divider, an 8-input multiplexer for each channel, and programmable logic states at each clock, gate, and output signal. The 3 channels are configured independently by the program. Each is suitable for event counting from DC to 2.5 MHz, marker and squarewave generation, time interval measurements, one-shot simulation with hardware and software triggering and retriggering, and repetitive interrupt generation. The 7308 operates as a stand-alone peripheral after receiving set-up instructions from the system processor card. From $145 depending on quantity. **Pro-Log Corp,** 2411 Garden Rd., Monterey, CA 93940.

Circle 193

IMAGE ARRAY PROCESSOR Compatible with DEC PDP-11 Systems, up to 16 512X512X8 bit image memories, with 4 memory controllers handling up to 4 memories each, for high resolution color, multi-image monochrome or pseudo color displays. Each controller offers independent pan (scroll) or integer zoom (2:1 - 8:1). A maximum system can store a 1024X1024X32 image with a 512X512X32 bit image window. Other features are real-time histogram calculations and 8 bit multipliers with 16 bit results, fast vector generation, a high speed disk interface, second-order warp hardware, bi-linear or nearest neighbor interpolation, programmable cursor, 64 character font generation, and switchable synchronization. Options available with the new IP 8500 include joysticks, light pens, trackballs and their associated interfaces, monitors, video signal digitizer, alphanumeric overlay generators, and an external synchronization control. **DeAnza Systems,** 118 Charcot Ave, San Jose, CA 95131 **Circle 143**

ENHANCED DISK The 'Native Mode' microcode option for the FAST-3805 semiconductor disk utilizes Fixed Block Architecture to reduce channel commands and decrease the amount of CPU instructions required to set up the I/O. The FAST-3805 is built with high-speed, low power RAMs, for a storage capacity from 12 to 72MB with a constant access time of 400 μs. The standard data transfer rate is 1.5 to 2MB/sec. With up to 4 controllers, the FAST-3805 can achieve an aggregate transfer rate of up to 16MB/sec. It includes Intel's iSBC-86. Initial release of Native Mode is available for IBMs Virtual Memory operating system. Available for purchase or lease. With 1 controller and 12MB of storage, $4870/month (36) or $158,000 on purchase. The FAST-3805 Native Mode option leases for $350/month. **Intel Commercial Systems Div,** 2402 W. Beardsley Rd, Phoenix, AZ 85027

Circle 139

GRAPHICS ADAPTER BOARD interfaces the Printronix line of printer/plotters with the Tektronix 4025 Raster Terminal. The GAB produces high resolution hard copies on plain paper. It allows 2 Raster CRT terminals to be served automatically and provides for the multiplexing of CRT data with no waste of CPU time.

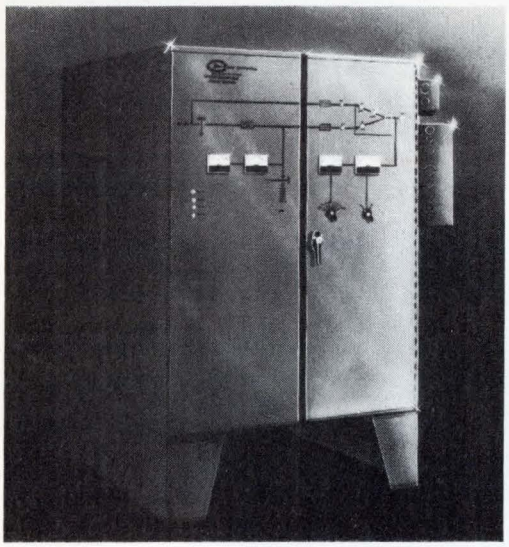
Its Self-Test mode prints 132 columns of 96-character ASCII data, and plots 132 diagonal lines. GAB models are available for storage tube devices, and for interfacing with both raster and storage CRTs. **Trilog, Inc.,** 17391 Murphy Ave., Irvine, CA 92714.

Circle 192

READY-MADE DISK SUBSYSTEMS. These 8″ rigid disk subsystems come in two ready-made "cabinet" series. They are based on the Micropolis Microdisk for S-100 bus microcomputers. Both are available in tabletop and rack-mount cabinets, with space for mini-floppy backup units. The subsystems are also available in one-, two- or three-platter configurations with unformatted storage of up to 8.91, 26.73, and 44.56MB. Power supply options include 50- or 60-HZ AC at 115, 215 or 230 volts. In 100-unit OEM quantities, the 1250 models are priced from $2675. The 1260 models, with an integral EPM controller, are from $2954. **Micropolis Corp**, 7959 Deering Ave, Canoga Park, CA 91304

Circle 167

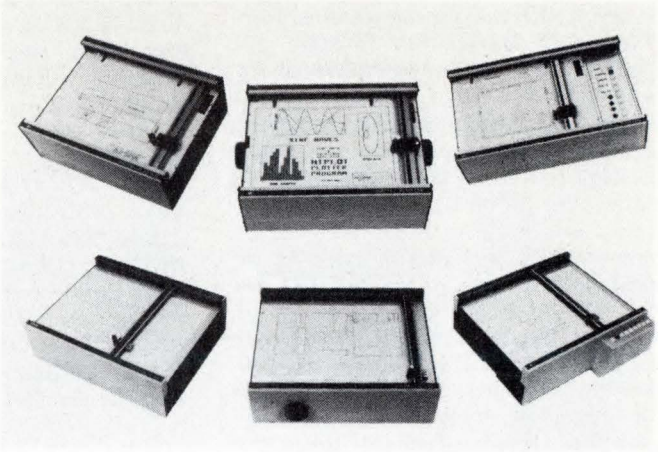
900 LPM BAND PRINTER features several bands, and specialized and foreign character sets. The B-900 print speed is 1,100 lpm at 48 characters, 900 lpm at 64 characters, and 600 lpm at 96 characters. Switch-selectable features include vertical spacing, for 6 or 8 lpi and for multiple form lengths. It also provides up to 5 clear copies. Other features include floor standing quietized cabinet, paper puller, a built-in diagnostic display, large viewing window, paper-out detect sensors and print-to-bottom-of-form capabilities. Both the paper and the cassette ribbons are easily loaded from the front. The B-900 also features a built-in self-test. **Southern Systems, Inc**, 2841 Cypress Creek Rd, Ft. Lauderdale, FL, 33309. **Circle 168**



UNINTERRUPTIBLE POWER SYSTEM This 15KVA UPS provides clean power that eliminates power outages and power disturbances. The unit has low harmonic sine wave distortion (2.5%) and controls output frequency (60 HZ ±.5 HZ) and voltage. The DC bus is floated at 137V DC and uses a battery voltage of 120V DC. The unit includes a Static Bypass Switch (4 msec fault transfer time), 60 HZ 3 phase I/O, and from 750VA to 15KVA. **Clary Corp**, 320 W. Clary Ave, San Gabriel, CA 91776 **Circle 166**

REMOTE CONTROLLED LOGIC ANALYZER This RS232C interface allows its logic analyzer to communicate over telephone lines. Data can be transmitted to and from the field for review, evaluation, repair and testing. Transmitted data can be viewed as a timing diagram on all BPI Logic Analyzers. With a BPI Model 50D Logic Analyzer and the Option 11 Data Formatter, the data can be viewed in binary, hex and octal. The Option 11 Data Formatter also allows status information from the sending Logic Analyzer to be viewed at the receiving location. Model 5020I Interface is $500. **Intech Inc**, BP Instruments Div, 282 Brokaw Rd, Santa Clara, CA 95050 **Circle 180.**

TWO PORT MEMORY BOARDS for the Cromemco SDI Color Graphics Interface give independent high-speed access to the computer memory. They have two sets of address and data lines which lets them process the SDI's memory refresh requests while the CPU independently executes a user program. A direct connection between



the SDI and the two-port memory bypasses the S-100 bus so the CPU accesses the memory as though the SDI were not present. This assures 75% to 100% CPU utilization depending on the software. Model SDI is $595; the 16K two-port memory board, Model 16KTP, is $795 (a 48K version is $1785); a graphics software package on either an 8″ or 5″ floppy diskette is $295. **Cromemco, Inc.**, 280 Bernardo Ave., Mountain View, CA 94043. **Circle 174**

DATA ACQUISITION WITH RAM This monolithic IC data acquisition system contains an 8-bit successive approximation ADC, and 8-channel multiplexer, an 8x8 dual-port RAM with address latches, control logic, comparator, and three-state buffers, all in a 28-pin DIP. The AD7581 connects directly to 8080, 8085, Z80 and 6800. Its on-chip logic provides interleaved DMA. $13.90/100, 90 days ARO for OEM quantities. **Analog Devices**, 804 Woburn St, Wilmington, MA 01887 **Circle 170**

UNIVERSAL INTERFACE PRINTER accepts 20MA Loop, an RS232, an ANS/IEEE 488, and a BCD input. All interface lines are tri-state but may be hard wired active high or low. The 722UA prints solid characters at rates up to 2400 lpm. Maximum line length is 22 characters. Available for rack or table mounting. $2500 – varies with options. **Datadyne Corp.**, Valley Forge Corporate Center, 960 Rittenhouse, Norristown, PA 19403 **Circle 171**

SWITCHING POWER SUPPLIES. A wide range of input-voltage switching power supplies is available to the OEM market. Operation from 90-250 VAC or 10 to 40 VDC or any voltage between these extremes without jumpers, taps or switches is available in 15 through 75 watt switchers. Also offered is a new uninterruptible power supply and battery charger system. A free booklet detailing all the specs is available. **Converter Concepts, Inc.**, 435 Main St., Pardeeville, WI 53954. **Circle 173**

REMOTE PRINTER utilizes dual μP control to print up to 200 cps. Model 2511 is an RO configuration, the 2516 has full keyboard, Send and Receive operation. The 2510 series can sustain a 1200 baud printing rate or will accept data bursts at 19.2K baud with a buffered RS-232 interface. A Lear Siegler 9 pin matrix print head is used for bidirectional printing with full underlining and true descender capability. Digital servo control assures correct character placement. **Digi-Data Corp**, 8580 Dorsey Run Rd., Jessup, MD 20794. **Circle 175**

New Products

NETWORKING SOFTWARE provides network support for the entire family of HP 1000 computers and their real-time executive operating systems. New features of DS/1000-IV include: μP-based, fully buffered interfaces to implement the HDLC link-level protocol; Message Accounting, a transparent, message control protocol; dynamic message re-routing automatically seeks a new path for messages when intended routes are disabled; Remote I/O Mapping enables transparent mapping of local data to any unit-record I/O device in the network; and, access to remote IMAGE/1000 data bases. Original license to use DS/1000-IV is $4000 (additional copies, $1600). No charge for upgrading present DS/1000 subscriptions. **Hewlett-Packard, Co,** 1507 Page Mill Rd, Palo Alto, CA 94304

Circle 138

PL/I COMPILER FOR VAX-11/780 The new language is an extension of the proposed ANSI X3.74 PL/I general purpose subset. VAX-11 PL/I extends the subset to maintain full file organization and access support, and to allow calls to the VAX/VMS operating system for services including SORT, LIBRARIAN, and optional packages. The new compiler can call routines written in all VAX-11 languages, and vice versa, as well as use the common VAX Run-Time Library, including mathematic and trigonometric functions. VAX-11 PL/I is intended for VAX-11/780 configurations containing 512 kB or more of physical memory. The single-use license fee is $12,000, delivery in Dec. **Digital Equipment Corp,** Maynard, MA 01754

Circle 141

DISK STORAGE BOX holds 10 mini-disks, protecting them from dust and debris. The box has no internal parts that might press on the disks to warp them during storage. It provides secure storage to prolong the effective life of stored disks. Available now on special order. **Verbatim Corp,** 323 Soquel Way, Sunnyvale, CA 94086

Circle 144

VECTOR REFRESH WITH COLOR RASTER DISPLAY is now available on a single controller. The Wizzard 7290 is computer-independent and may be interfaced to a variety of computers. It contains its own RAM vector memory and a microcontroller for hardware implementation of graphics features. Data transfers are handled by a 32-bit wide, tri-state graphics bus. A separate 16-bit wide peripheral bus ensures that high speed data transfers are not degraded by peripheral I/O transfers and routine interrupt servicing. The vector memory modules use 16K RAMs for display refresh. Each module contains 16K words of 32-bit RAM and can accept 2K 32-bit words of PROM. Software compatibility is provided by the WAND 7200 package. The vector generator has an average writing time of 160 ns/pixel. The raster system can display the entire 4096x4096 area or zoom in on a smaller viewport. A sample configuration including a single 21″ vector refresh monitor and a single 21″ color raster monitor is $35,000. **Megatek Corp,** 3931 Sorrento Valley Blvd, San Diego, CA 92121

Circle 127

FIBER-OPTIC CABLE This graded-index fiber optic cable has a core diameter of 50 micrometers with a cladding diameter of 125 micrometers. Bandwidth remains 200 MHz-km, and nominal attenuation is 8 dB max. at 850 nm. Numerical aperture is 0.21. Series 2270 is available in configurations of 1, 2, 6, 12, and 18 fibers. Bandwidths up to 1500 MHz-km, and low attenuations approaching 1 dB/km are available on special request. From $1.10-$1.34/ meter in quantities less than 10 km. **Belden Corp,** 2000 S. Batavia Ave, Geneva, IL 60134

Circle 201

Discover what a smart terminal should really be. Meet SOROC's new IQ 135, a terminal ahead of its time. Priced like other not-so-smart terminals, our new IQ 135 offers more features than any other terminal in its price range. So check out the new SOROC IQ 135 and see why we call it the terminal with the incomparable IQ.

Our IQ 135 is an OEM's dream come true, with more functions and features than ever before offered at the price. Based on a Z-80 microprocessor, and fully software programmable, the IQ 135 offers a surprising number of designed-in standard features. Like fourteen user programmable function keys, full text editing, extensive video attributes, and adjustable right-hand margin. All of this, plus lots more, in a smart-looking terminal designed for operator comfort, convenience and efficiency.

When you want to discover what a smart terminal can really offer, look to SOROC—terminals with the incomparable IQ.

SOROC TECHNOLOGY, INC.

165 Freedom Avenue
Anaheim, California 92801
(800) 854-0147
(714) 992-2860

Introducing the Incomparable IQ...

See us at Comdex '80 Booth #1812

Circle 38 on Reader Inquiry Card

SINGLE OUTPUT IC REGULATED OEM SERIES EAPS U

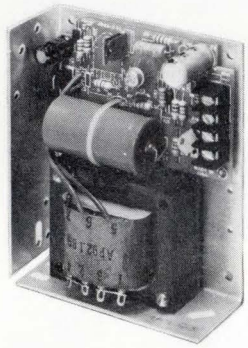
MEETS U L AND C S A REQUIREMENTS

Not available through distributors contact the engineering sales office near you. Minimum sales order 50 units.

FEATURES

- 3 way barrier block output terminals screw, solder connection or fast on tabs
- Higher efficiency cooler operation 45% efficiency at 5VDC, 60% at 15VDC
- Better noise immunity dual input electro-statically shielded transformer
- High reliability over 100,000 hr MTBF (5V 6A per MIL-HDBK-217B at 40°C ambient, full load, nominal line)
- Metal Cased Hermetically Sealed Pass Transistors used on all units over 25 watts
- 85°C 10 yr life computer Grade capacitors
- Meets UL and CSA requirements
- Full 5 yr warranty
- Metal Cased Hermetically Sealed IC regulator
- Fully enclosed, dustproof, insulated Potentiometers
- Wider input line voltage range 103-130V/206-260V 47-63Hz
- Thinner profile 3 plane mounting

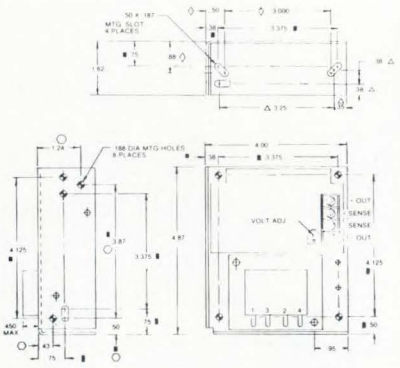
$ 22.25



10-15 Watts

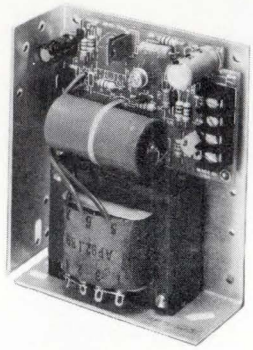
HB Case Series
Meets U.L. and C.S.A. Requirements
5 Vdc @ 1.2 Amps to 24 Vdc @ 0.6 Amps
Optional OVP available for 5V to 24V units

MODEL NUMBER	RATING		REGULATION		RIPPLE
	Vdc	Amps	Line	Load	(Pk/Pk)
EAPS 5-1.2U	5	1.2	±0.05%	±0.10%	3mV
EAPS 12-0.5U	12	0.5	±0.05%	±0.10%	3mV
EAPS 15-0.5U	15	0.5	±0.05%	±0.10%	3mV
EAPS 24-0.6U	24	0.6	±0.05%	±0.10%	5mV



Weight: 2 lbs

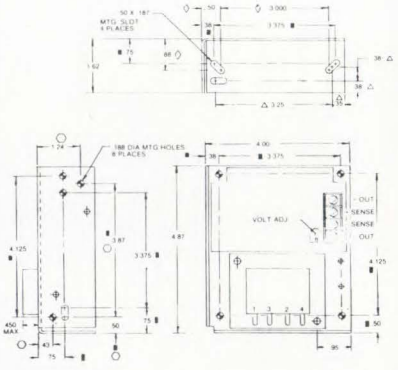
$ 23.25



15-24 Watts

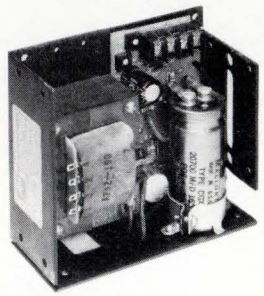
HB Case Series
Meets UL and CSA Requirements
5VDC @ 3 Amps to 24VDC @ 1.0 Amps
Optional OVP available for 5V to 24V units.

MODEL NUMBER	RATING		REGULATION		RIPPLE
	Vdc	Amps	Line	Load	(Pk/Pk)
EAPS 5-3.0U	5	3.0	±0.05%	±0.10%	5mV
EAPS 12-1.6U	12	1.6	±0.05%	±0.10%	5mV
EAPS 15-1.5U	15	1.5	±0.05%	±0.10%	5mV
EAPS 24-1.0U	24	1.0	±0.05%	±0.10%	5mV



Weight: 2 lbs

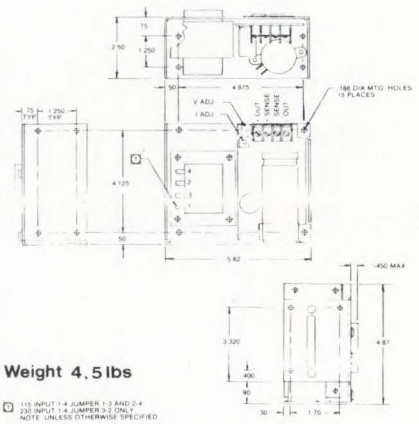
$ 44.95



30-50 Watts

HC Case Series
Meets UL and CSA requirements
5VDC @ 6 Amps to 24VDC @2.4 Amps
Optional OVP Available for 5V to 24V units

MODEL NUMBER	RATING		REGULATION		RIPPLE
	Vdc	Amps	Line	Load	(Pk/Pk)
EAPS 5-6.0U	5	6.0	±0.05%	±0.10%	5mV
EAPS 12-3.4U	12	3.4	±0.05%	±0.10%	5mV
EAPS 15-3.0U	15	3.0	±0.05%	±0.10%	5mV
EAPS 24-2.4U	24	2.4	±0.05%	±0.10%	5mV



Weight 4.5 lbs

NOW! Call Toll Free (800) 854-8288)

See Page 65 for List of Local ADTECH Field Offices . . .

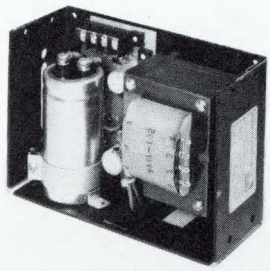
Specifications:

AC Input: 103-130V/206-260V AC 47/63Hz
Derate 10% at 50Hz
DC Output: See tabulation of models
Line Regulation: ±0.05% for ±10% line change
Load Regulation: ±0.1% for ±50% load change
Ripple: Less than 5Mv peak to peak
Transient Response: Less than 50 microseconds
Short Circuit and
Overload Protection: Automatic recovery foldback current limiting
Reverse Polarity Protection: Standard
Remote Sensing: Standard with open sense lead protection
Output Adjustment: ±5% minimum

Operating Temperature Range: 0°C to +50°C at full power rating. Derate linearly to 40% at 70°C or -20°C
Storage Temperature: -30°C to +85°C
Stability: ±0.1% for 24 hours after warm up
Temperature Coefficient: ±0.01% typical ±0.03% maximum
Vibration: Per MIL-STD-810B method 514, procedure 1, curve AB (to 50Hz)
Shock: Per MIL-STD-810B method 516 procedure
Overvoltage Protection: Optional
Efficiency: 5V units 45%; 12V units 55%; 15V units 60%; 24V units 62%
Line Noise Suppression: Electrostatically shielded transformer

ALL MODELS WARRANTED FOR 5 YEARS

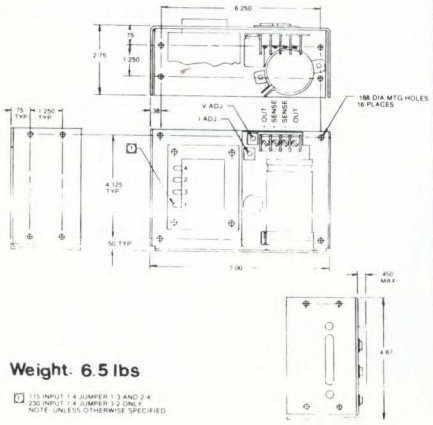
$59.45



50-84 Watts

HN Case Series
Meets UL and CSA Requirements
5 Vdc @ 9 Amps to 24 Vdc @ 3.6 Amps
Optional OVP available for 5V to 24V units

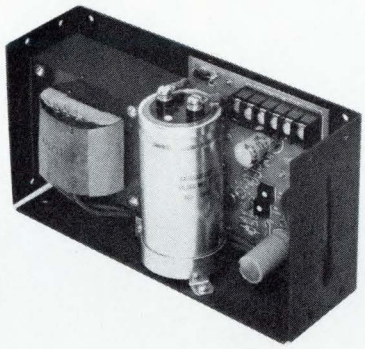
MODEL NUMBER	RATING		REGULATION		RIPPLE
	Vdc	Amps	Line	Load	(Pk/Pk)
EAPS 5-9.0U	5	9.0	±0.05%	±0.10%	5mV
EAPS 12-5.0U	12	5.0	±0.05%	±0.10%	5mV
EAPS 15-4.5U	15	4.5	±0.05%	±0.10%	5mV
EAPS 24-3.6U	24	3.6	±0.05%	±0.10%	5mV



Weight: 6.5 lbs

[1] 115 INPUT 1-4 JUMPER 1-3 AND 2-4
230 INPUT 1-4 JUMPER 3-2 ONLY
NOTE: UNLESS OTHERWISE SPECIFIED

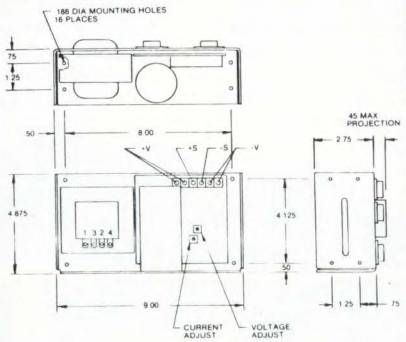
$71.05



60-100 Watts

HD Case Series
Meets UL and CSA Requirements
5 Vdc @ 12 Amps to 24 Vdc @ 4.5 Amps
Optional OVP available for 5V to 24V units

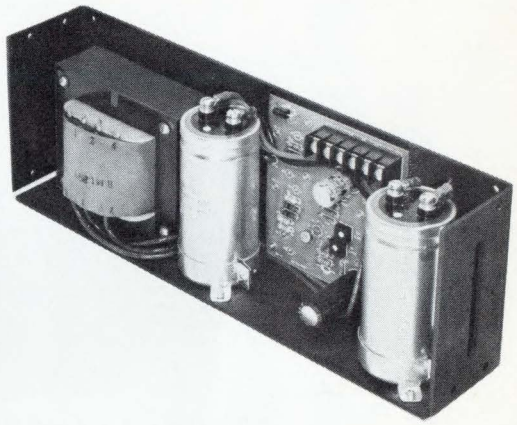
MODEL NUMBER	RATING		REGULATION		RIPPLE
	Vdc	Amps	Line	Load	(Pk/Pk)
EAPS 5-12.0U	5	12.0	±0.05%	±0.10%	5mV
EAPS 12-6.8U	12	6.8	±0.05%	±0.10%	5mV
EAPS 15-6.0U	15	6.0	±0.05%	±0.10%	5mV
EAPS 24-4.5U	24	4.5	±0.05%	±0.10%	5mV



Weight: 7 lbs

115 V INPUT 1-4 JUMPER 1-3 & 2-4
230 V INPUT 1-4 JUMPER 3-2 ONLY

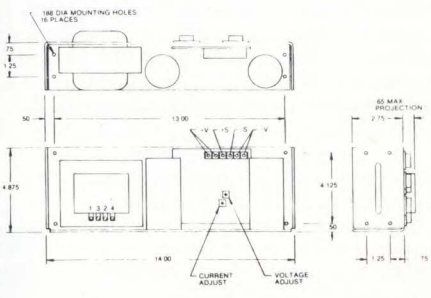
$98.85



90-168 Watts

HE Case Series
Meets UL and CSA Requirements
5 Vdc @ 18 Amps to 24 Vdc @ 7.0 Amps
Optional OVP available for 5V to 24V units

MODEL NUMBER	RATING		REGULATION		RIPPLE
	Vdc	Amps	Line	Load	(Pk/Pk)
EAPS 5-18.0U	5	18.0	±0.05%	±0.10%	5mV
EAPS 12-10.0U	12	10.0	±0.05%	±0.10%	5mV
EAPS 15-9.0U	15	9.0	±0.05%	±0.10%	5mV
EAPS 24-7.0U	24	7.0	±0.05%	±0.10%	5mV



Weight: 9.5 lbs

115 V INPUT 1-4 JUMPER 1-3 & 2-4
230 V INPUT 1-4 JUMPER 3-2 ONLY

ADTECH POWER SUPPLIES

ADTECH POWER

1621 S. Sinclair St., Anaheim, CA 92806 (714) 634-9211 • Telex: 68-1498 • Outside Calif. (800) 854-8288

Circle 39 on Reader Inquiry Card

NEVER BEFORE HAS A BACK-UP SYSTEM BEEN AS INTELLIGENT AS THE SYSTEM IT'S BACKING UP.

This is 3M's HCD-75 High Capacity Data Cartridge Drive. And the reason it's as intelligent as a computer is because it thinks like one.

You see, unlike other back-up systems, the HCD-75 is interfaced directly with the primary system by means of sophisticated, microprocessor electronics. When the host computer has data to feed, the HCD-75 starts automatically. When the host computer stops, it does too. And since the HCD-75 also positions to any location, it not only saves tape cost, but retrieval time as well.

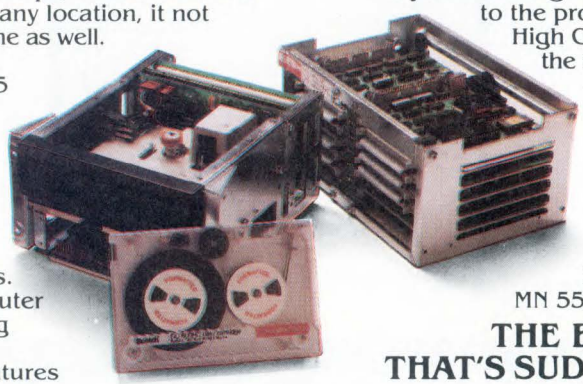
Of course, the use of microprocessors allows the HCD-75 to perform a number of other time-saving functions, too. Like block replacement, so you can easily correct errors or change files which need updating. And fast random access, which makes it useful both as an I-O device or as a storage unit for low-usage files. All of which relieves the host computer from difficult timing and formatting problems.

What's more, the HCD-75 features state-of-the-art error detection and correction capabilities. Even when the system is off-line, self-test diagnostic routines monitor its performance. And, combined with each of its $32.50 high-capacity cartridges, the HCD-75 provides a full 67 megabytes of formatted user information (144 mbytes unformatted). So costly operator interventions are sharply reduced.

If you're looking for a reliable, cost-effective solution to the problem of disk back-up, the HCD-75 High Capacity Data Cartridge Drive is the system you should be thinking about.

Not only has a lot of thinking gone into it. But a lot of thinking comes out of it, too.

For more information, check the listing on the next page for the representative nearest you. Or write: Data Products Division/3M, Bldg. 223-5E/3M Center, St. Paul, MN 55144.

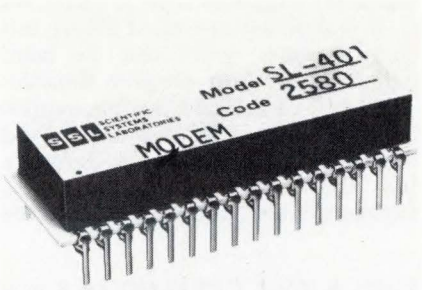


THE BACK-UP SYSTEM THAT'S SUDDENLY WAY OUT FRONT.

Circle 44 on Reader Inquiry Card

New Products

SL-401 DTMF MODEM. This unit combines both transmitter and receiver functions for DTMF signaling systems (PABX's, KTU's, CO's, RCC's, etc.,) Features include: Full binary decoded output, 2X8 encoded input. Crystal controlled. SL-401 is a complete-low



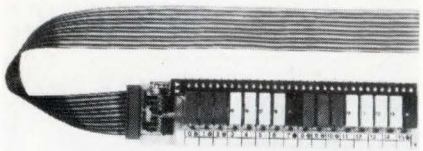
lower DTMF MODEM in a 32-pin Dip hybrid IC package. No external components are required. It provides the complete data communication function. **Scientific Systems Laboratories**, 2031 E. Cerritos, Suite J, Anaheim, CA 92802. **Circle 207**

ENTRY-LEVEL SYSTEM makes removable-disk mass storage available to new computer customers whose needs do not warrant purchase of the larger, more powerful Basic Four Systems. Base configuration of the System 510 consists of a CPU with 64K memory, one disk drive with 20MB capacity, operating system software, a 120 cps printer and one VD terminal. $44,000 delivery 90 days ARO. **Basic Four Corp**, Box C-11921, Santa Ana, CA 92711. **Circle 150**

CMOS SINGLE-CHIP μCs. The single-chip 5840 contains a 2K by 8-bit mask ROM, 128 X 4-bit RAM, programmable timer counter, and 30 I/O lines. Featuring an 8-bit parallel I/O port and 4-bit wide data paths, the 5840 allows connection to an 8-bit system. With ROM bank switching, the 2K by 8 on-board ROM can be externally expanded via a multiplexed bus structure. The other 4 chips in the family give a range of CPUs having 98 to 49 multifunctional instructions, I/O capability from 53 to 21 lines, and memory ranges from 2048 to 768 bytes of internal ROM and from 128 to 32 nibbles of internal RAM. All Series 40 circuits are TTL-compatible at 5V and operate from single supply voltages from 3 to 6 VDC. The 5840 is $6. each/100,000, minimum order is 5,000. Options include 3 program development packages. This MPSP series starts at $1485. **OKI Semiconductor**, 1333 Lawrence Expy, Santa Clara, CA 95051 **Circle 206**

New Products

I/O COMPONENTS This Module Board, using industry standard plug-in I/O modules, can be directly connected to any 5 to 28 MOS, CMOS or TTL circuitry. It negates the need for higher cost buffered modules without giving up the location interchangeability of I/O modules. Features of the MBE-16 I/O Module Board are color coded barrier terminal blocks for



easier wiring and an on-board LED logic voltage indicator to ease trouble-shooting. It also includes a plug-in logic supply and field wiring fuses, positive module hold down, card edge logic connector, and on-board, pull-up resistors. **duTec inc**, 4801 James McDivitt Rd, Jackson, MI 49204

Circle 204

μP SOFTWARE EXECUTIVE. This modular software programming executive for the Intel iAPX 86/88 family establishes a foundation that extends bare hardware architecture. Such an extension provides standardization and facilities for multi-tasking and multi-processing. REX-80/86 promotes modularity and is completely configurable to any hardware environment. It is designed to be compatible with high-level languages such as PL/M and C. It is supplied as a set of library program modules which may be maintained by the host program librarian. The basic REX-80/86 module requires less than 4kB of ROM and 512 bytes of RAM space. **Systems & Software, Inc**, 2801. Finley Rd, Suite 101, Downers Grove, IL 60515 **Circle 194**

TAPE & DISK CATALOG An 8 page short-form catalog describes the Kennedy line of tape transports, disk drives, cartridge transports, asynchronous incremental recorders and control units. Featured is the Model 6809 1/2″ Data Streamer transport and Model 6450 cartridge data system for backing up Winchester disk drives. The brochure also describes the Series 5300 14MB to 70MB 14″ Winchester disk drives. **Kennedy Co**, 1600 S. Shamrock Ave, Monrovia, CA 91016 **Circle 126**

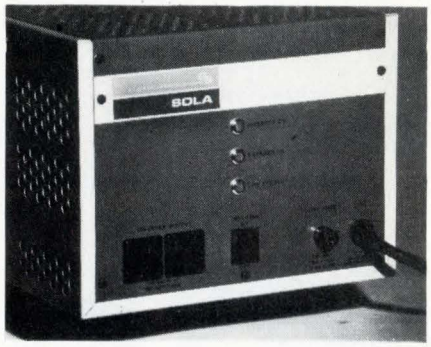
CARTRIDGE TAPE SUBSYSTEM BACKUP. A new 14 MB cartridge tape subsystem provides disk backup and file transport for Perkin-Elmer minis and Tektronix's 4081. The Z-80 based half-card controller is compatible with MUX and SELCH buses. Read while write capability using CRC error checking guarantees data integrity. Comes with software that performs "wild card" file save and restore. Delivery: 30 days. **Scientific Enterprises, Inc.**, 9375 S.W. Commerce Circle, Wilsonville, OR 97070.

Circle 148

TWO NEW SBCs. The MLZ-90 is a complete microcomputer system on a single 6.75 X 12″, 4 layer pc card. It includes a Z-80 type CPU, on-card floppy disk drive controller (up to 16 single or double density drives – direct interface with Shugart Model 801 and 850/851 drives); Am9511 or Am9512 arithmetic processing unit; DMA; one ROM socket; and 8 ROM/RAM sockets. Each of the 9 memory sockets may contain a maximum of 8192 bytes of storage. Compatible memory types are Intel 2716, 2732 and 2764 EPROM and Mostek 4118, 4801, 4816, 4802 and 4864 (or equivalent) byte-wide RAM. The ZRAID-90 software monitor and debugger provides floppy disk and memory mapping routines as well as CP/M DOS bootstrap. The MLZ-90 (2 MHz) is $2285; the MLZ-90A (4 MHz) is $2340; both complete with FDIO, Am9511, and 16 kB of RAM. **Heurikon Corp**, 3001 Latham Dr., Madison, WI 53713.

Circle 177

PORTABLE μPS contains a sealed, lead-acid type battery. In a blackout, the 400 and 750 VA units provide up to 20 minutes of regulated power. The MINI-UPS operates from a single-phase 115 V AC input and provides an output voltage regulated to ±3% of nominal through input fluctuations as great

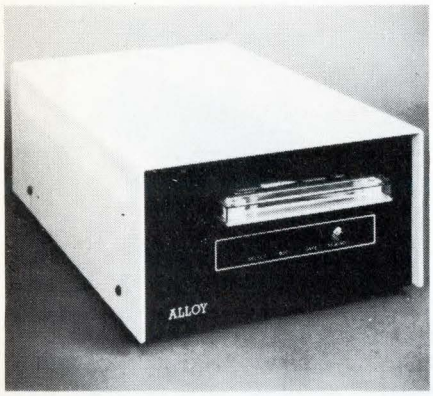


as +10 −20%. Input frequency fluctuations of up to ±10% of nominal (60Hz) are tightly regulated at the output to ±0.5 Hz (one-half cycle). It also attenuates electrical "noise". **Sola Electric**, Div. of General Signal, 1717 Busse Rd, Elk Grove Village, IL 60007

Circle 203

New Products

CARTRIDGE TAPE SUBSYSTEM This S-100 compatible cartridge tape subsystem permits transfer of programs and data files from a Winchester disk to a 13.4 MB 1/4″ tape cartridge. The subsystem features comprehensive menu driven software, with a 2 min./MB backup/restore rate. It has a DS-100 Controller and 6400 bpi cartridge

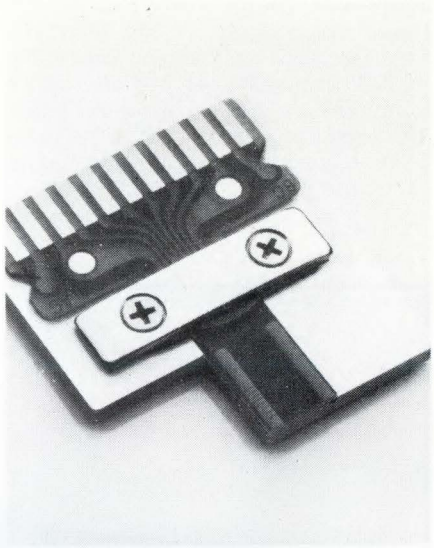


tape drive. Software is distributed on a single sided, single density 8″ floppy disk in CP/M format. TIP is $2100 each rack mount and $2200 each table mount/25. **Alloy Engineering Co, Inc,** 85 Speen St, Framingham, MA 01701 **Circle 160**

V77 DRIVES Model 0876 Magnetic Tape Drive has 9 tracks at 125 ips. At a density of 800 bpi the transfer rate is 100 kB/sec. At 1600 bpi the transfer rate is 200 kB/sec. The controller is mounted with the CPU, and can accommodate up to 4 magnetic tape drives. ($28,215). Model F3359 cartridge disk drive features 15MB of fixed disk storage and an additional 5MB removable disk cartridge. Data transfer rate is 312,500 bytes/sec, with an average access time of 40 ms. Up to 4 F3359 drives, rack mount, can be accommodated by a single controller. ($18,000). **Sperry Univac,** Box 500, Blue Bell, PA 19424 **Circle 163**

PRINTER FOR IBM 3270 produces solid characters by single impressions as opposed to being built up by dots from a matrix. Standard print is executive quality Courier 72 type font. Interchangeable optional printing elements provide a choice of several conventional typefaces as well as OCR and foreign language characters. Model 736 is $5150, 60 to 90 days ARO. **Interface Systems, Inc.,** 462 Jackson Plaza, Ann Arbor, MI 48103 **Circle 159**

THERMAL PRINTHEAD This 1x7-dot thin film thermal printhead, for alphanumeric applications, prints at 10 cps. The design insures flat travel of the head eliminating excessive head wear, providing a minimum scanning length of 75km without failure. Different versions include the head alone, the head mounted on a heat sink alone,



or with cabling to a connector. A 12V supply and 250mA of current are required to produce supply power of 3 W per heating element. Average resistance per element is 45 ohms. KH319 printhead is $15 each/1000. **R.ohm Corp,** Box 19515, Irvine, CA 92713 **Circle 156**

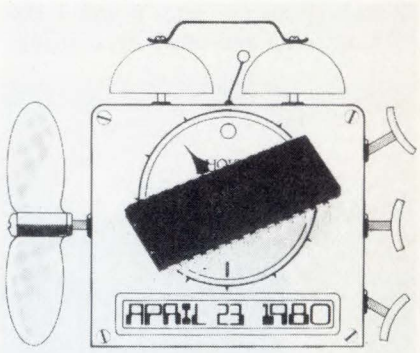
PASCAL COMPILER for the CG series of Z80-based color graphic computers, runs under the CP/M operating system. The CG PASCAL is a two-pass compiler with an interactive symbolic debugger. It compiles large programs directly to Z80 machine language object code at 600 lpm. The programs then can make maximum use of Z80 processing speed while using a minimum amount of memory space. The compiler is $950, CP/M option is $350. **Chromatics, Inc**, 2558 Mountain Industrial Blvd, Tucker, GA 30084

Circle 164

DIGITAL PLOTTERS The DMP family of plotters now comprises 6 models, 2 standard and 4 intelligent, available with plotting sizes of 8 1/2 × 11″ or 11 × 17″. The various configurations can include: built-in RS-232C, parallel interface or μP; remote pen positioning; pen speeds of 2.4 or 3 ips; self-test; plug and software compatibility with other models; and, DM/PL instructions to minimize the need for software. Prices for the DMP series start at $1085. **Houston Instrument**, One Houston Sq, Austin, TX 78753

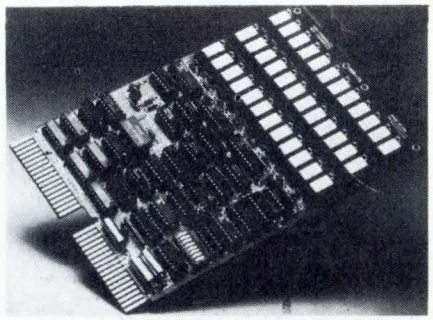
Circle 147

CMOS CLOCK IC interfaces to most μPs. This 8-bit bus compatible micropower CMOS clock uses a battery to keep running when system power is off. It features second count with 12.3 ms resolution, minutes, hours, days, months and years (maximum count of 128 years), an alarm interrupt, leap year compensation, software sync of clock, 3 programmable prescalers to



Hz, stopwatch and elapse timer, on-chip oscillator and 3 divider chain outputs. A readback latch prevents read errors caused by clock running during reading. The HI-8000 CMOS chip is a 28 pin dip at $52/100. **Holt, Inc**, 3303 Harbor Blvd, D-5, Costa Mesa, CA 92626 **Circle 200**

96K-WORD MEMORY MODULE Two new versions of the TMM10000 series add-in modules are compatible with DECs LSI 11/23 computer. Both use 5-volt storage devices allowing increased board densities and lower power dissipation. Two previous versions with 64K words are the TMM



10000-01 and -02. The -01 has 16 bpw plus 2 parity bits ($2400), the -02 has 16 bpw ($2200). The two new 96K modules are the TMM10000-03 with 16 bpw plus 2 parity bits ($3150), and the -04 with 16 bpw ($2900). **Texas Instruments, Inc,** Box 225012, M/S 308, Dallas, TX 74265. **Circle 140**

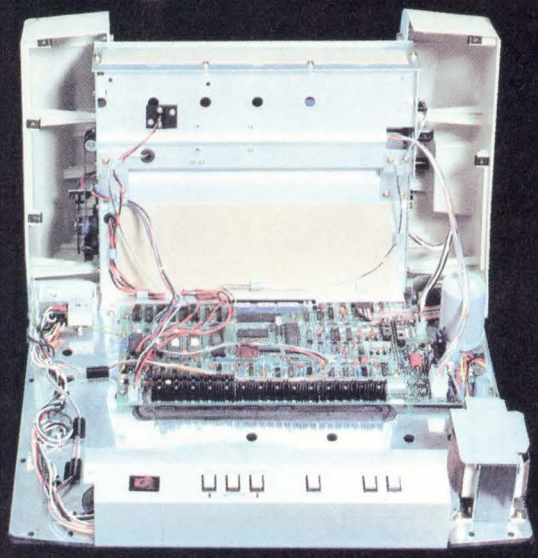
NAME CHANGE To avoid confusion with any Digital Equipment Corp. product, the designation for Sky's Micro Number Kruncher for under $4K has been changed by the manufacturer from MNC-11 to MNK-02. **SKY Computers, Inc.**, Box 1006, N. Chelmsford, MA 08163. **Circle 149**

FAST DELIVERY ON DISK CARTRIDGES. Inmac will ship DEC cartridges within 24 hours ARO. An optional "Ship Sure" service guarantees delivery the following day. Always available in stock is DEC's RKO6K-DC (13.8 MB), RKO7K-DC (28 MB), RLO1K-DC (5.2 MB), and RLO2K-DC (10.4 MB) disk cartridges. They are purchased directly from DEC and guaranteed to meet DEC specifications for 3 years. From $169 each in 6-11 quantities. A free catalog features other DEC-compatible supplies and accessories. **Inmac,** Dept. 1023, 2465 Augustine Dr., Santa Clara, CA 95051.
Circle 189

RACKS & GUIDES FOR PCBs. Design and make your own PCB racks and guides with high dielectric glass epoxy tubes, rods, angles and "U" channels. Rods are 1/4" square, slotted for .062" boards, from pultrusion molded glass fibers and epoxy resin. "Ells" and "U" channels are made of fiberglass laminated epoxy tubing and notched for boards. Thicknesses of .030" or .060" are available with 155°C material. Rods from $1.30/foot, Ells from $1.50/foot. **Stevens Tubing Co,** 128 N. Park St, E. Orange, NJ 07019
Circle 157

RASTER SCAN GRAPHICS SYSTEM A new concept in high performance/low cost modular graphics systems for OEM's is offered with MAGS-10. The system is easily integrated into a user's environment since it is based on two industry standards: hardware is based on Intel's Multibus; software is based on Digital Research's CP /M and MP /M disk operating system. The MAGS-10 series of advanced graphics systems provides the OEM with the power and speed of mini-computer based graphics systems at a fraction of the usual cost. It provides the OEM system designer with the hardware and software flexibility to meet any custom application. In addition, Matrox will custom integrate a specific graphics system according to customer specifications. Prices start at $6,995 for a basic system. OEM discounts available. Delivery, 6-8 weeks. **Matrox Electronic Systems, Ltd.,** 5800 Andover Ave., T. M. R., Quebec H4T 1H4 Canada **Circle 152**

Say Ahh...



Our New grafixPLUS™ 80-column printer opens wide for easy servicing.

Introducing the newest members of our grafixPLUS™ family—the DP-9000 Series 80/132 column printers—built on the same tradition of quality printout, solid design and low cost of ownership established by our 132/220 column DP-9500 Series.

A Case for Serviceability

Not that is comes up often, but want to get inside? Simple. Just remove a few screws and the clam-shell case swings open exposing all major components. This easy access plus built-in self-test and minimum component count yields an MTTR of one-half hour. The 9-wire print head replacement's even simpler . . . two screws and it's out. Without opening the case. And without a service call.

Performance Plus

The DP-9000 Series prints the full ASCII 96 character set, including descenders and underlining, bi-directionally, at up to 200 CPS. Number of columns can go up to 80 or 132, depending on character density—switch or data source selectable from 10 to 16.7 characters per inch. And all characters can be printed double width. The print head produces razor-sharp characters and high-density graphics with dot resolutions of 72X75 dots/inch under direct data source control.

Interface Flexibility

The three ASCII compatible interfaces (parallel, RS-232-C and current loop) are standard, so connecting your computer is usually a matter of plug-it-in and print. Also standard are: a sophisticated communications interface for printer control and full point-to-point communications, DEC PROTOCOL, and a 700 character FIFO buffer. An additional 2K buffer is optional.

When you're ready for a printer (or several thousand), look into the grafixPLUS DP-9000 Series from Anadex—you'll find an open and shut case for quality. Contact us today for details, discounts and demonstrations.

Anadex®
...the plus in printers

Circle 46 on Reader Inquiry Card

...close please.

SALES OFFICES: San Jose, CA (408) 247-3933
Fullerton, CA (714) 871-0501 • Wakefield, MA (617) 245-9160 • Austin, TX (512) 327-5250

ANADEX, INC. • 9825 DeSoto Avenue • Chatsworth, California 91311, U.S.A. • Telephone: (213) 998-8010 • TWX 910-494-2761

ANADEX, LTD. • Dorna House, Guildford Road • West End, Woking, Surrey GU24 9PW, England • Tel: Chobham (09905) 6333 • Telex: 858762 ANADEX G

New Products

MULTI-PROCESSOR MICROSYSTEM supports up to 16 users on an S-100 bus, and is expanded by adding single cards that contain a processor, memory and dual port memory window. Built around a Z-80A, it supports up to 4 Winchester 8″ hard disks with maximum 96 MB storage, with file back-up on cartridge tape drive. The PDOS hard disk operating system offers large scale file management facilities and user/file security. The System 1000-MP is $25,000 with 4 users and 24 MB storage, desk top model or 19″ rack mount. **Computer Service Systems Network,** 120 Boylston St., Boston, MA 02116. **Circle 172**

NEW GPIB TRANSCEIVERS provide a 65% speed-power improvement over the TI SN75160 series. The SN75160A is a data bus transceiver, the SN75161A and SN75162A are management bus transceivers to be used with GPIB controllers to provide a complete μP 16-line interface system conforming to the IEEE 488 standard. They feature built-in terminating resistors on drive outputs; high impedance to bus during power down; an enable control (SN75160A only); 3-state outputs on receivers; hysteresis maximum supply current, and 25 ns maximum propagation delay. ($3-$5/100). **Texas Instruments Inc,** Box 225012, M/S 308, Dallas, TX 75265. **Circle 179**

16 BIT A/D CONVERTER will digitize an analog input signal in 2μs. It can be configured with either single ended or differential inputs with conversion times of 2μs. or 4 μs.

Options include either a 2μs, .006% or a 5μs, .0007% sample and hold in a single ended input configuration. All inputs are DTL, TTL compatible. The ADC-1600 is from $2,050 in 1-9 quantities. **Intech,** 282 Brokaw Rd, Santa Clara, CA 95050 **Circle 169**

ADC/DAC TEST SYSTEM Through a series of software-controlled measurements, the system can accurately measure gain error (%), zero error (% full scale), linearity error (% full scale), differential linearity (% full scale), power supply, rejection ratio, and the accuracy of the internal, voltage reference. It has a multi-processor architecture with a Z-80 μP that controls test calculation, display and keyboard functions. A 6502 μP controls the system's magnetic tape mass storage. Data-handling capabilities of the 1731 ADC/DAC test system include CRT and front-panel pass/fail indicators, manual and automatic binning, parametric measurement test results, and summary screens on the integral CRT. Hard-copy output is available through a choice of IEEE-488 bus, 20-mA current loop, or optional RS-232. I/O data ports allow connection to a computer or calculator, for statistical analysis. It includes 48K RAM-based operating system software, a program library, 5″ CRT, alphanumeric keyboard, and ADC/DAC family board. ($32,500). **GenRad, Inc,** 300 Baker Ave, Concord, MA 01742. **Circle 178**

New Products

Z8000 BIBLE. This 950-pg. "Z8000 Assembly Language Programming" paperback by Lance Leventhal, Adam Osborne and Chuck Collins is the most comprehensive Z8000 tutorial and reference manual published to date. It's also easy to read. Each of its 17 chapters are well-structured in a multiple, inverted-pyramid style. Chapters cover assembler features, instruction set descriptions (378 pgg. alone!), simple programs and loops, character coded data and code conversion, arithmetics, tables/lists, subroutines, I/O, interrupts, use of 8010 MMU with 8001, problem definition/program design, debugging/testing, documentation and even projects. This comprehensive handbook belongs in the library of every Z8000 designer. $19.99 plus shipping. **Osborne/McGraw-Hill,** 630 Bancroft Way, Berkeley, CA 94710. 415/548-2805.

8W POWER SUPPLY, contained on a 4.5″ X 6.5″ card, supplies +5 at 800 mA, +12 at 150 mA, −5 and −12 at 150 mA. This general purpose power supply can also serve as a companion to the M-80 Intelligence Microcomputer. It includes a standard 22 pin edge connector, and 115 VAC and power line switch which can be connected to the board with the supplied connectors. The PS-80 is available in kit form ($35) or assembled and tested ($60). **Miller Technology,** 16930 Sheldon Rd, Los Gatos, CA 95030

Circle 208

CRT WITH DETACHED KEYBOARD offers 11 special function keys – 22 functions with the shift key. These can be programmed to the users requirements via 256 bytes of onboard RAM. The unit also features a 25th status and message line, baud rates between 50 and 19,200, a line drawing character set with 15 special graphic characters and a 128 displayable ASCII character set. A split screen with line lock allows lines of copy to be held on the screen while scrolling other lines for editing. Model 950 is $1195, qty discounts available, delivery in first quarter 1981. **TeleVideo, Inc,** 249 Paragon Dr, San Jose, CA 95131.

Circle 209

X.25 NETWORK PROCESSOR. This packet processor switches packet transmissions between X.25-compatible computers, terminals and other digital devices. Operating as switching nodes in a packet network, each M3216 XPRO can support aggregate data rates to 300Kbits/sec, up to 36,000 call connections/hour, packet rates to 800 packets/sec, up to 1,500 virtual circuits (on 64 channels), async terminal rates to 9600 bits/sec, and sync terminals rates to 64Kbits/sec. Three M3216s can attach to a single Tran M3201 Network Processor, each operating independently, handling both time division switched and packet switched data simultaneously for an aggregate data rate of up to 1.25 million bits/sec. The M3216 XPRO starts at $50,000, 90 days ARO.**Tran Telecommunications Corp,** 2500 Walnut Ave, Marina del Rey, CA 90291 **Circle 215**

DATA CONVERTER allows the attachment of a wide variety of peripheral equipment to an IBM System/34 computer. The unit sends and receives EBCDIC data via IBM binary sync protocol, performs all error-checking functions, translates the data to ASCII, and outputs it in serial async ASCII format to and from user-attached devices. Data may be transmitted at user selectable rates of 75, 110, 150, 300, 600, 1200, 2400, 4800, 9600, or 19,200 Hz. Other async data format options with BAC-34 include parity (even, odd, or none), stop bits (1, 1½, or 2), and data bits (6, 7, or 8). **KMW Systems Corp,** 8307 Highway 71 West, Austin, TX 78735 **Circle 214**

Continued from page 54

MCS-51 Macro Assembler

Keyboard/Display Control with Intel MCS-51 Microcomputers

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ISIS-II MCS-51 MACRO ASSEMBLER V1.0
OBJECT MODULE PLACED IN :F0:KBD51.HEX
ASSEMBLER INVOKED BY:  :F1:ASM51 KBD51.SRC


LOC  OBJ            LINE     SOURCE

                       1     $TITLE('KEYBOARD/DISPLAY CONTROL WITH INTEL MCS-51 MICROCOMPUTERS')
                       2     ;
                       3     ;*************************************************************
                       4     ;
                       5     ;       SYSTEM CONFIGURATION EQUATES:
                       6     ;
  00A0                 7     PINPUT  EQU     P2      ;PORT USED TO SCAN FOR KEY CLOSURES
  0080                 8     PDIGIT  EQU     P0      ;USED TO ENABLE CHARACTERS AND STROBE ROWS OF KEYBOARD
  0090                 9     PSGMNT  EQU     P1      ;USED TO TURN ON SEGMENTS OF CURRENTLY ENABLED DIGIT
  00F0                10     INPMSK  EQU     0F0H    ;DEFINES BITS USED AS INPUT
                      11     ;
  0000                12     POSLOG  EQU     00H
  00FF                13     NEGLOG  EQU     0FFH
                      14     ;
  0000                15     CHRPOL  EQU     POSLOG  ;DEFINES WHETHER OUTPUT LINES ARE ACTIVE HI OR LOW
  0000                16     SEGPOL  EQU     POSLOG  ;\FOR DRIVING CHARACTERS AND SEGMENT PATTERNS
                      17     ;
  0008                18     CHARNO  EQU     8       ;NUMBER OF DIGITS IN DISPLAY
  0004                19     NROWS   EQU     4       ;ROWS OF KEYS (LESS THAN OR EQUAL TO CHARNO)
  0004                20     NCOLS   EQU     4       ;LESSER DIMENSION OF KEYBOARD MATRIX
                      21     ;
  FFFB                22     TICK    EQU     -5      ;INTERRUPT INTERVAL = 5*256 USEC.
  0004                23     DEBNCE  EQU     4       ;NUMBER OF SUCESSIVE SCANS BEFORE KEY CLOSURE ACCEPTED
  0000                24     BLANK   EQU     00H     ;OUTPUT CODE TO BLANK ALL DISPLAY SEGMENTS
                      25                             ;(WOULD BE 20H IF ASCII DECODING ROM USED OR 0FH IF
                      26                             ;7447-TYPE SEVEN-SEGMENT DECODER EXTERNAL TO 8751)
  00FF                27     ESCAPE  EQU     0FFH    ;ESCAPE PATTERN MONITORED BY PRINT ROUTINE
                      28     ;
  000F                29     ENCMSK  EQU     0FH     ;SELECTS WHICH BITS ARE RELEVANT TO ENCACC SUBROUTINE
                      30     ;
                      31     ;*************************************************************
                      32     ;
                      33     ;       BANK 0 REGISTER DECLARATION:
                      34     ;
  REG                 35     NEXTPL  EQU     R7      ;KEEPS TRACK OF NEXT CHARACTER POSITION TO BE WRITTEN
                      36     ;
                      37     ;*************************************************************
                      38     ;
                      39     ;       BANK 1 REGISTER ALLOCATION:
                      40     ;
  REG                 41     ROTPAT  EQU     R4      ;USED TO HOLD INPUT PATTERN BEING ROTATED THROUGH CY
  REG                 42     ROTCNT  EQU     R5      ;COUNTS NUMBER OF BITS ROTATED THROUGH CY
  REG                 43     LASTKY  EQU     R6      ;HOLDS KEY POSITION OF LAST KEY DEPRESSION DETECTED
  REG                 44     CURDIG  EQU     R7      ;HOLDS POSITION OF NEXT CHARACTER TO BE DISPLAYED
  000E                45     ?LASTKY DATA    16Q     ;OCTAL DIRECT BYTE ADDRESS OF LASTKY REGISTER
  000F                46     ?CURDIG DATA    17Q     ;OCTAL DIRECT BYTE ADDRESS OF CURDIG REGISTER
                      47     ;
                      48     ;*************************************************************
                      49     ;
                      50     ;       DATA RAM ALLOCATION
                      51     ;
  ----                52             DSEG            ;FOLLOWING BYTE ALLOCATION REFERS TO ON-CHIP DATA RAM:
  0020                53             ORG     20H     ;RAM ALLOCATION BEGINS AFTER REGISTER BANK 1.
                      54     ;
  0020                55     FLAGS:  DS      1       ;ALLOCATE 8 SOFTWARE FLAGS IN 8051 BIT ADDRESS SPACE
    0000              56     CLOSURE BIT     FLAGS.0 ;DEFINE FLAG TO MONITOR KEY DETECTIONS
  0021                57     NREPTS: DS      1       ;KEEPS TRACK OF SUCCESSIVE READS OF SAME KEYSTROKE
  0022                58     KEYLOC: DS      1       ;INCREMENTED AS SUCCESSIVE KEY LOCATIONS SCANNED
  0023                59     KBDBUF: DS      1       ;CARRIES POSITION OF DEBOUNCED KEY FROM REFRESH ROUTINE
                      60                             ;\ BACK TO BACKGROUND PROGRAM
  0024                61     RDELAY: DS      1       ;NON-ZERO WHEN DELAY IN PROGRESS
  0025                62     SEGMAP: DS      CHARNO  ;BASE OF REGISTER ARRAY FOR DISPLAY PATTERNS
  002D                63     STACK:  DS      10H     ;STACK STORAGE DECLARATION (16-BYTE ALLOCATION)
                      64     ;
                      65     ;*************************************************************
                      66     ;
                      67     ;       NOTE THAT LASTKY, CURDIG, AND CLOSURE RETAIN STATUS INFORMATION FROM
                      68     ;       ONE INTERRUPT TO THE NEXT.  ALL OTHER REGISTERS MAY BE USED IN
                      69     ;       THE USER'S OWN INTERRUPT SERVICING ROUTINE

LOC  OBJ            LINE     SOURCE

                      70     ;
                      71     ;*************************************************************
                      72     ;
                      73     ;       RESET AND INTERRUPT VECTORS:
                      74     ;
  ----                75             CSEG
  0000                76             ORG     0000H
  0000 0200F6         77             JMP     SYS_INIT
                      78     ;
  000B                79             ORG     000BH           ;TIMER 0 OVERFLOWS AUTOMATICALLY CALL LOC 000BH
  000B 758CFB         80             MOV     TH0,#TICK       ;RELOAD TIMER INTERVAL
  000E 120012         81             CALL    REFRESH
  0011 32             82             RETI                    ;RETURN AND RESTORE INTERRUPT LOGIC
                      83     ;
                      84     ;*************************************************************
                      85 +1  $EJECT
                      86     REFRESH:
                      87     ;       SUBROUTINE TO MULTIPLEX SEVEN-SEGMENT DISPLAYS.
                      88     ;       EACH CALL CAUSES THE NEXT CHARACTER TO BE DISPLAYED,
                      89     ;       ACCORDING TO THE CONTENTS OF THE SEGMAP REGISTER ARRAY.
                      90     ;       REFRESH SHOULD BE CALLED AT LEAST EVERY MSEC OR SO.
                      91     ;
  0012 C0E0           92             PUSH    ACC             ;SAVE CPU REGISTERS AFFECTED BY SERVICE ROUTINE
  0014 C0D0           93             PUSH    PSW
  0016 75D008         94             MOV     PSW,#00001000B  ;SELECT REGISTER BANK 1
  0019 759000         95             MOV     PSGMNT,#BLANK   ;TURN OFF ALL SEGMENT DRIVERS
  001C EF             96             MOV     A,CURDIG        ;LOAD POSITION (0,1,2,...) OF DIGIT TO DISPLAY
  001D 2450           97             ADD     A,#CHRSTB-($+3) ;ADD DISPLACEMENT TO STROBE ENCODING TABLE
  001F 83             98             MOVC    A,@A+PC         ;TRANSLATE INTO DIGIT-ENABLE PATTERN
  0020 F580           99             MOV     PDIGIT,A        ;ENERGIZE THE NEXT CHARACTER TO BE DISPLAYED
  0022 7425          100             MOV     A,#SEGMAP       ;LOAD BASE OF REGISTER ARRAY
  0024 2F            101             ADD     A,CURDIG        ;ADD CURDIG DISPLACMENT INTO SEGMAP ARRAY
  0025 F8            102             MOV     R0,A            ;STORE INTO INDEX REGISTER TO ACCESS PATTERN
  0026 8690          103             MOV     PSGMNT,@R0      ;COPY CHARACTER BIT PATTERN TO SEGMENT PORT
                     104     ;
                     105     ;       THE NEXT CHARACTER IS NOW BEING DISPLAYED.
                     106     ;       THE KEYBOARD SCAN ROUTINE IS INTEGRATED INTO THE DISPLAY SCAN.
                     107     ;       WITH THE CURRENT ROW ENERGIZED, CHECK IF THERE ARE ANY INPUTS.
                     108     ;
  0028 7D04          109             MOV     ROTCNT,#NCOLS   ;SET UP FOR <NCOLS> LOOPS THROUGH 'NXTLOC'
  002A E5A0          110             MOV     A,PINPUT        ;LOAD ANY SWITCH CLOSURES
  002C F4            111             CPL     A               ;ANY CLOSURES DETECTED ARE NOW ONE BITS
  002D 54F0          112             ANL     A,#INPMSK       ;MASK-OUT I/O BITS NOT USED FOR RETURN LINES
  002F 7008          113             JNZ     NXTLOC          ;-IF ANY KEYS ARE DEPRESSED IN THE ENABLED ROW
                     114     ;       NO KEY IS NOW DOWN SO THE KEYLOC COUNT MAY BE UPDATED DIRECTLY
  0031 E522          115             MOV     A,KEYLOC
  0033 2404          116             ADD     A,#NCOLS
  0035 F522          117             MOV     KEYLOC,A
  0037 8014          118             SJMP    SCAN6
                     119     ;
                     120     ;       ROTATE BITS THROUGH THE CY WHILE INCREMENTING KEYLOC.
                     121     ;
  0039 33            122     NXTLOC: RLC     A
  003A FC            123             MOV     ROTPAT,A        ;SAVE SHIFTED BIT PATTERN
  003B 500B          124             JNC     SCAN5           ;ZERO BIT IN CY INDICATES KEY NOT DOWN
                     125     ;
                     126     ;       AT THIS POINT A CONTACT CLOSURE HAS BEEN DETECTED AT THE KEY POSITION
                     127     ;       INDICATED BY THE CONTENTS OF KEYLOC.
                     128     ;       THE FOLLOWING CODE DEBOUNCES THE KEY AND
                     129     ;       WRITES ITS POSITION INTO VARIABLE KBDBUF.
                     130     ;       MODIFICATIONS TO THE KEYBOARD SCANNING ALGORITHM (SUCH AS THE INCLUSION
                     131     ;       OF A SHIFT, CONTROL, OR MODE KEY IN THE KEY MATRIX ITSELF)
                     132     ;       SHOULD BE MADE AT THIS POINT, BEFORE THE DEBOUNCE LOGIC BEGINS.
                     133     ;       FOR EXAMPLE, KEYLOC COULD BE COMPARED AGAINST THE POSITION OF ANY MODE
                     134     ;       KEYS, WITH A FLAG BIT SET IF THERE IS A MATCH.
                     135     ;       OR, BY COMPARING KEYLOC AGAINST THE LAST KEY DEBOUNCED,
                     136     ;       TWO-KEY ROLLOVER COULD BE SENSED AND PROCESSED IMMEDIATELY.
                     137     ;
  003D D200          138             SETB    CLOSURE         ;MARK THAT CURRENT SCAN DETECTED A KEY
                     139     ;       SEE IF THE POSITION OF THIS KEY MATCHES THAT OF PREVIOUS KEY SENSED.
                     140     ;
  003F E522          141             MOV     A,KEYLOC        ;CURRENT KEY POSITION
  0041 CE            142             XCH     A,LASTKY        ;SWAP WITH PREVIOUS KEY POSITION
  0042 6E            143             XRL     A,LASTKY
  0043 6003          144             JZ      SCAN5
                     145     ;
                     146     ;       A DIFFERENT KEY WAS READ ON THIS CYCLE THAN ON THE PREVIOUS CYCLE.
                     147     ;       SET NREPTS TO THE DEBOUNCE PARAMETER FOR A NEW COUNTDOWN.
                     148     ;
  0045 752104        149             MOV     NREPTS,#DEBNCE
  0048 0522          150     SCAN5:  INC     KEYLOC
  004A EC            151             MOV     A,ROTPAT
  004B DDEC          152             DJNZ    ROTCNT,NXTLOC
  004D 0F            153     SCAN6:  INC     CURDIG
  004E BF081A        154             CJNE    CURDIG,#CHARNO,SCAN9
  0051 E4            155             CLR     A
  0052 FF            156             MOV     CURDIG,A        ;RESET DISPLAY DIGIT INDEX
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Continued on next page

Continued from previous page

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LOC  OBJ            LINE     SOURCE

0053 F522            157              MOV     KEYLOC,A        ;RESET KEY POSITION COUNT
0055 100004          158              JBC     CLOSURE,SCAN7   ;JUMP IF ANY KEYS WERE DETECTED & CLEAR FLAG
0058 7EFF            159              MOV     LASTKY,#0FFH    ;CHANGE <LASTKY> WHEN NO KEYS ARE DOWN
005A 8009            160              SJMP    SCAN8
                     161      ;
                     162      ;       THE FOLLOWING CODE SEGMENT IS EXECUTED BY THE KEYBOARD SCANNING ROUTINE
                     163      ;       AFTER ALL DISPLAY CHARACTERS HAVE BEEN REFRESHED IF A KEY IS DEPRESSED.
                     164      ;       LOOK AT NREPTS:  IF ALREADY ZERO, DO NOTHING;  ELSE DECREMENT NREPTS.
                     165      ;       IF THIS RESULTS IN ZERO, MOVE LASTKY INTO KBDBUF.
                     166      ;
005C E521            167      SCAN7:  MOV     A,NREPTS
005E 6005            168              JZ      SCAN8           ;IF ALREADY ZERO
0060 D52102          169              DJNZ    NREPTS,SCAN8    ;DECREMENT COUNT & BRANCH IF RESULT IS NOT ZERO
0063 8E23            170              MOV     KBDBUF,LASTKY
                     171      ;
                     172      ;       THE INTERRUPT-DRIVEN PORTION OF THE 'DELAY' UTILITY DECREMENTS RAM
                     173      ;       LOCATION 'RDELAY' ONCE PER DISPLAY SCAN UNLESS VALUE IS ALREADY ZERO.
                     174      ;
0065 E524            175      SCAN8:  MOV     A,RDELAY
0067 6002            176              JZ      SCAN9
0069 1524            177              DEC     RDELAY
006B D0D0            178      SCAN9:  POP     PSW
006D D0E0            179              POP     ACC
006F 22              180              RET
                     181      ;
                     182      CHRSTB:                 ;OUTPUT BIT PATTERN TABLE TO ENABLE ONE-OF-CHARNO CHARACTERS:
0070 80              183              DB      (10000000B XOR CHRPOL)
0071 40              184              DB      (01000000B XOR CHRPOL)
0072 20              185              DB      (00100000B XOR CHRPOL)
0073 10              186              DB      (00010000B XOR CHRPOL)
0074 08              187              DB      (00001000B XOR CHRPOL)
0075 04              188              DB      (00000100B XOR CHRPOL)
0076 02              189              DB      (00000010B XOR CHRPOL)
0077 01              190              DB      (00000001B XOR CHRPOL)
                     191 +1   $EJECT
                     192      ;*********************************************************
                     193      ;
                     194      ;       THE UTILITY SUBROUTINES BELOW IMPLEMENT FUNCTIONS COMMONLY USED IN
                     195      ;       KEYBOARD/DISPLAY APPLICATIONS.  THEIR USE IS DEMONSTRATED IN THE
                     196      ;       "TEST" ROUTINE AT THE END OF THE LISTING.
                     197      ;
                     198      ;*********************************************************
                     199      ;
                     200      CLEAR:
                     201      ;       WRITES 'BLANK' CHARACTERS INTO ALL DISPLAY REGISTERS.
                     202      ;       RETURNS WITH NEXTPL SET TO LEFTMOST CHARACTER POSITION
                     203      ;       ENTRY POINT "FILL" WRITES ACC SEGMENT PATTERN TO ALL DISPLAY POSITIONS
                     204      ;
0078 7400            205              MOV     A,#BLANK
007A 7825            206      FILL:   MOV     R0,#SEGMAP
007C 7F08            207              MOV     NEXTPL,#CHARNO
007E F6              208      CLR1:   MOV     @R0,A           ;STORE THE BLANK CODE
007F 08              209              INC     R0              ;POINT TO NEXT CHARACTER TO THE LEFT
0080 DFFC            210              DJNZ    NEXTPL,CLR1
0082 22              211              RET
                     212      ;
                     213      ;*********************************************************
                     214      ;
                     215      WDISP:
                     216      ;       WRITES BIT PATTERN NOW IN ACC INTO NEXT CHARACTER POSITION
                     217      ;       OF THE DISPLAY (NEXTPL).  ADJUSTS NEXTPL POINTER VALUE.
                     218      ;       RESULTS IN DISPLAY BEING FILLED LEFT TO RIGHT, THEN RESTARTING
                     219      ;
0083 F8              220              MOV     R0,A
0084 EF              221              MOV     A,NEXTPL
0085 2425            222              ADD     A,#SEGMAP
0087 C8              223              XCH     A,R0
0088 F6              224              MOV     @R0,A
0089 0F              225              INC     NEXTPL
008A BF0802          226              CJNE    NEXTPL,#CHARNO,WDISP1
008D 7F00            227              MOV     NEXTPL,#0
008F 22              228      WDISP1: RET
                     229      ;
                     230      ;*********************************************************
                     231      ;
                     232      RENTRY:
                     233      ;       SUBROUTINE TO ENTER ACC CONTENTS INTO THE RIGHTMOST DIGIT
                     234      ;       AND SHIFT EVERYTHING ELSE ONE PLACE TO THE LEFT
                     235      ;
0090 7B2D            236              MOV     R0,#SEGMAP+CHARNO
0092 18              237      RENTR1: DEC     R0              ;POINT TO PREVIOUS CHARACTER
0093 C6              238              XCH     A,@R0
0094 BB25FB          239              CJNE    R0,#SEGMAP,RENTR1
0097 7F00            240              MOV     NEXTPL,#0       ;RESET POSITION POINTER
0099 22              241              RET
                     242      ;
                     243      ;*********************************************************
                     244      ;
                     245      ENCACC:
                     246      ;       TRANSLATE LEAST SIGNIFICANT NIBBLE OF A INTO HEX CHARACTER BIT PATTERN:
                     247      ;
009A 540F            248              ANL     A,#ENCMSK
009C 9000A1          249              MOV     DPTR,#DGPATS
009F 93              250              MOVC    A,@A+DPTR

LOC  OBJ            LINE     SOURCE

                     310      ;       THE INTERRUPT DRIVEN KEYBOARD SCANNER.
                     311      ;       RETURNS ONLY AFTER A NEW KEYSTROKE HAS BEEN DEBOUNCED WITH ITS ENCODED
                     312      ;       VALUE (RATHER THAN ITS POSITION IN SWITCH MATRIX) IN THE ACCUMULATOR.
                     313      ;
00C6 201FFD          314              JB      KBDBUF.7,$      ;WAIT AT THIS INSTRUCTION UNTIL NEW KEY READY.
00C9 7480            315              MOV     A,#80H          ;KBDBUF WILL BE MARKED AS CLEAR
00CB C523            316              XCH     A,KBDBUF        ;LOAD BUFFER VALUE
00CD 9000D2          317              MOV     DPTR,#LEGENDS   ;LOAD DATA POINTER WITH KEY ENCODING TABLE BASE
00D0 93              318              MOVC    A,@A+DPTR       ;OBTAIN BYTE REPRESENTING KEY SIGNIFICANCE
00D1 22              319              RET
                     320      ;
                     321      LEGENDS:
                     322      ;       LOOK-UP TABLE SHOWING KEY MATRIX LEGENDS FOR PROTOTYPE KEYBOARD.
                     323      ;       PHYSICAL KEY LAYOUT IS DRAWN IN THE COMMENT FIELDS.
                     324      ;       BIT6-BIT4 ARE BEING USED TO ENCODE KEY TYPE.  IN THIS CASE:
                     325      ;               BIT4 INDICATES REGULAR DECIMAL DIGITS,
                     326      ;               BIT5 INDICATES RIGHT-COLUMN FUNCTION KEYS,
                     327      ;               BIT6 INDICATES PUNCTUATION MARKS ( * AND # ).
                     328      ;
00D2 4F              329              DB      4FH     ;
00D3 10              330              DB      10H     ;
00D4 4E              331              DB      4EH     ;
00D5 24              332              DB      24H     ;  PDIGIT.4==>  1       2       3       <1>
00D6 17              333              DB      17H     ;
00D7 18              334              DB      18H     ;  PDIGIT.5==>  4       5       6       <2>
00D8 19              335              DB      19H     ;
00D9 23              336              DB      23H     ;  PDIGIT.6==>  7       8       9       <3>
00DA 14              337              DB      14H     ;
00DB 15              338              DB      15H     ;  PDIGIT.7==>  *       0       #       <4>
00DC 16              339              DB      16H     ;
00DD 22              340              DB      22H     ;                 !       !       !       !
00DE 11              341              DB      11H     ;                 !       !       !       !
00DF 12              342              DB      12H     ;                 V       V       V       V
00E0 13              343              DB      13H     ;             PINPUT.7 PINPUT.6 PINPUT.5 PINPUT.4
00E1 21              344              DB      21H     ;
                     345      ;
                     346      ;*********************************************************
                     347      ;
                     348      ECHO:
                     349      ;       READ KEYSTROKE INPUT AND PRINT CORRESPONDING DIGIT TO DISPLAY:
                     350      ;
00E2 11C6            351              CALL    KBDIN
00E4 119A            352              CALL    ENCACC
00E6 1190            353              CALL    RENTRY
00E8 22              354              RET
                     355      ;
                     356      ;*********************************************************
                     357      ;
                     358      HOLD:
                     359      ;       SUBROUTINE CALLED WHEN KEY IS KNOWN TO BE DOWN.
                     360      ;       WILL NOT RETURN UNTIL KEY IS RELEASED.
                     361      ;       (NOTE THAT "LASTKY" IS DIRECTLY ADDRESSED FROM ALTERNATE REGISTER BANK)
                     362      ;
00E9 E50E            363              MOV     A,?LASTKY       ;<LASTKY>=0FFH IFF NO KEYS DOWN
00EB 30E7FB          364              JNB     ACC.7,HOLD
00EE 22              365              RET
                     366      ;
                     367      ;*********************************************************
                     368      ;
                     369      DELAY:
                     370      ;       SUBROUTINE HANGS UP FOR THE NUMBER OF COMPLETE DISPLAY SCANS EQUAL
                     371      ;       TO THE CONTENTS OF THE ACCUMULATOR WHEN CALLED.
                     372      ;
00EF F524            373              MOV     RDELAY,A
00F1 E524            374      DELAY1: MOV     A,RDELAY
00F3 70FC            375              JNZ     DELAY1
00F5 22              376              RET
                     377      ;
                     378      ;*********************************************************
                     379      ;
                     380      SYS_INIT:
                     381      ;       CPU AND PERIPHERAL CONTROL REGISTER INITIALIZATION:
                     382      ;
00F6 75812C          383              MOV     SP,#STACK-1
00F9 750F00          384              MOV     ?CURDIG,#0
00FC 7523FF          385              MOV     KBDBUF,#0FFH
00FF 752200          386              MOV     KEYLOC,#0
0102 1178            387              CALL    CLEAR           ;UTILITY FOR SETTING INITIAL DISPLAY REGISTERS.
0104 C200            388              CLR     CLOSURE
0106 758901          389              MOV     TMOD,#01H       ;CONFIGURE TIMER 0 AS 16-BIT FREE-RUNNING TIMER
0109 758CFB          390              MOV     TH0,#TICK       ;LOAD INTERRUPT RATE VALUE
010C D28C            391              SETB    TR0             ;START TIMER 0 RUNNING
010E 75A882          392              MOV     IE,#10000010B   ;ENABLE TIMER 0 INTERRUPT REQUESTS
                     393      ;
                     394      ;       THE REMAINING CODE SHOWS HOW TO ACCESS THE SUBROUTINES ABOVE.
                     395      ;       IT IS INTENDED FOR DEMONSTRATION PURPOSES ONLY-
                     396      ;       FEW END USERS WANT NAMES POPPING UP ON THEIR CALCULATOR SCREENS.
                     397      ;       THE TEST SEQUENCE IS TO CHECK FOR ANY NEW KEYSTROKES DETECTED,
                     398      ;       TRANSLATE EACH KEYSTROKE INTO A SEGMENT PATTERN,
                     399      ;       AND WRITE IT INTO THE APPROPRIATE DISPLAY REGISTER.
                     400      ;       SPECIAL ROUTINES ARE INVOKED WHEN THE FOUR BUTTONS
                     401      ;       ON THE RIGHT-HAND SIDE OF THE PROTOTYPE KEYBOARD ARE PRESSED:
                     402      ;       TEST1 - FILLS DISPLAY REGISTERS WITH SEQUENTIAL DIGITS FROM '0',
                     403      ;       TEST2 - WRITES WRITES A STRING OF CHARACTERS ONTO THE DISPLAY,
```

```
LOC  OBJ          LINE   SOURCE

00A0 22                          RET
                         ;
                         DGPATS:
                         ;       TABLE OF SEGMENT PATTERNS FOR HEXIDECIMAL DIGITS 0-F.
                         ;       THE TABLE MAY EASILY BE AMENDED OR AUGMENTED TO PROVIDE A DIFFERENT
                         ;       CHARACTER SET OR SPECIAL PURPOSE PATTERNS.
                         ;       FORMAT=>PGFEDCBA IN STANDARD SEVEN-SEGMENT ENCODING (P = DECIMAL POINT)
00A1 3F                          DB      00111111B XOR SEGPOL
00A2 06                          DB      00000110B XOR SEGPOL
00A3 5B                          DB      01011011B XOR SEGPOL
00A4 4F                          DB      01001111B XOR SEGPOL
00A5 66                          DB      01100110B XOR SEGPOL
00A6 6D                          DB      01101101B XOR SEGPOL
00A7 7D                          DB      01111101B XOR SEGPOL
00A8 07                          DB      00000111B XOR SEGPOL
00A9 7F                          DB      01111111B XOR SEGPOL
00AA 67                          DB      01100111B XOR SEGPOL
00AB 77                          DB      01110111B XOR SEGPOL
00AC 7C                          DB      01111100B XOR SEGPOL
00AD 39                          DB      00111001B XOR SEGPOL
00AE 5E                          DB      01011110B XOR SEGPOL
00AF 79                          DB      01111001B XOR SEGPOL
00B0 71                          DB      01110001B XOR SEGPOL
                         ;
                         ;*************************************************************
                         ;
                         PRINT:
                         ;       SUBROUTINE TO COPY A STRING OF BIT PATTERNS TO THE DISPLAY REGISTERS.
                         ;       THE DATA BYTES TO BE PRINTED ARE PASSED AS IN-LINE PARAMETERS DIRECTLY
                         ;       FOLLOWING THE CALL INSTRUCTION, AND ARE ACCESSED VIA THE MCS-51 DPTR.
                         ;       PRINT IN TURN CALLS EITHER SUBROUTINE 'WDISP' OR 'RENTRY'
                         ;       TO ACTUALLY EFFECT WRITING INTO THE DISPLAY REGISTERS.
                         ;       CONTINUES UNTIL AN ESCAPE CODE IS REACHED.
                         ;
00B1 D083                        POP     DPH
00B3 D082                        POP     DPL
00B5 E4                  PRNT_0: CLR     A
00B6 93                          MOVC    A,@A+DPTR          ;LOAD BIT PATTERN INDIRECT
00B7 B4FF03                      CJNE    A,#ESCAPE,PRNT1    ;TEST BY COMPARING WITH ESCAPE PATTERN
00BA 7401                        MOV     A,#1               ;BRANCH BACK OVER ESCAPE CODE
00BC 73                          JMP     @A+DPTR            ;RETURN TO CODE FOLLOWING DATA STRING
                         ;
00BD 1183                PRNT1:  CALL    WDISP              ;OUTPUT TO NEXT CHARACTER POSITION
                         ;##     (CALL    RENTRY             INSTEAD IF MESSAGE IS TO BE RIGHT JUSTIFIED)
00BF A3                          INC     DPTR               ;INDEX POINTER
00C0 80F3                        JMP     PRNT_0
                         ;
                         ;*************************************************************
                         ;
                         RDPADD:
                         ;       TOGGLE DECIMAL POINT IN RIGHT-MOST CHARACTER DISPLAY REGISTER
                         ;
00C2 632C80                      XRL     SEGMAP+CHARNO-1,#80H  ;COMPLEMENT MSB OF LAST DISPLAY REGISTER
00C5 22                          RET
                         ;
                         ;*************************************************************
                         ;
                         KBDIN:
                         ;       KEYBOARD INPUT SUBROUTINE.  INTERFACES THE BACKGROUND PROGRAM WITH
```

```
LOC  OBJ          LINE   SOURCE

                         ;               PAUSES, AND THEN CLEARS THE DISPLAY.
                         ;       TEST3 - FILLS DISPLAY WITH DASHES, THEN JUMPS INTO SUBROUTINE 'CLEAR'
                         ;               WHEN THE KEY IS RELEASED.
                         ;       TEST4 - TOGGLES THE RIGHT-HAND CHARACTER'S DECIMAL POINT.
                         ;
0111 11C6                TEST:   CALL    KBDIN              ;GET NEXT KEYSTROKE
0113 20E506                      JB      ACC.5,TSTKEY       ;JUMP IF KEY IN RIGHTHAND COLUMN
0116 119A                        CALL    ENCACC             ;FORM APPROPRIATE SEGMENT PATTERN
0118 1190                        CALL    RENTRY             ;WRITE PATTERN INTO DISPLAY REGISTERS
011A 80F5                        JMP     TEST               ;LOOP INDEFINITELY
                         ;
011C 540F                TSTKEY: ANL     A,#ENCMSK          ;MASK OFF TYPE-ENCODING BITS
011E 900123                      MOV     DPTR,#TST_TBL
0121 93                          MOVC    A,@A+DPTR          ;LOOK UP OFFSET TO ONE OF THE TEST SEQUENCES
0122 73                          JMP     @A+DPTR            ;INDIRECT BRANCH TO TEST CODE
                         ;
                         TST_TBL:
                         ;       TABLE OF INDIRECT-BRANCH OFFSET VALUES FOR VARIOUS TEST-ROUTINES:
                         ;
0123 00                          DB      0                  ;DUMMY VALUE - THERE IS NO "FUNCTION-0" KEY
0124 05                          DB      TEST1-TST_TBL      ;OFFSET FROM VALUE IN DPTR TO TEST ROUTINE 1
0125 11                          DB      TEST2-TST_TBL
0126 20                          DB      TEST3-TST_TBL
0127 2A                          DB      TEST4-TST_TBL
                         ;
0128 7F00                TEST1:  MOV     NEXTPL,#0
012A EF                  TST11:  MOV     A,NEXTPL
012B 119A                        CALL    ENCACC
012D 1183                        CALL    WDISP
012F BF00F8                      CJNE    NEXTPL,#0,TST11    ;LOOP UNTIL ALL CHARACTERS FILLED
0132 80DD                        JMP     TEST
                         ;
0134 11B1                TEST2:  CALL    PRINT
                         ;       BIT PATTERNS FOR THE LETTERS 'JOHN' ('OHN' IN LOWER CASE LETTERS)
0136 1E                          DB      00011110B XOR SEGPOL
0137 5C                          DB      01011100B XOR SEGPOL
0138 74                          DB      01110100B XOR SEGPOL
0139 54                          DB      01010100B XOR SEGPOL
013A FF                          DB      ESCAPE
                         ;
013B 7464                        MOV     A,#100             ;MAINTAIN DISPLAY FOR 100 COMPLETE SCAN CYCLES
013D 11EF                        CALL    DELAY
013F 1178                        CALL    CLEAR
0141 80CE                        JMP     TEST
                         ;
0143 7440                TEST3:  MOV     A,#01000000B XOR SEGPOL ;PATTERN FOR '-'
0145 117A                        CALL    FILL
0147 11E9                        CALL    HOLD
0149 1178                        CALL    CLEAR
014B 80C4                        JMP     TEST
                         ;
014D 11C2                TEST4:  CALL    RDPADD             ;TOGGLE DECIMAL POINT CHARACTER
014F 80C0                        JMP     TEST
                         ;
                         ;*************************************************************
                         ;
                                 END

ASSEMBLY COMPLETE, NO ERRORS FOUND
```

Continued from page 54

segment pattern is written to PSGMNT, and the keyboard return lines are read by PINPUT. The user may initially assign these logical port names in any manner he pleases.

By way of example **(Fig 4)**, the breadboard used to develop and debug this software used a 4x4 matrix of simple single-pole pushbuttons and an eight character common-cathode LED display with right-hand decimal point. We defined PDIGIT as eight-bit port 0, PSGMNT as port 1, and PINPUT as port 2. We used 75491 and 75492 current buffers as drivers. These buffers are logically non-inverting in that high-level inputs turn a segment or character ON; therefore, the segment and character polarity (SEGPOL and CHRPOL, respectively) were initially set to POSLOG (positive logic).

PDIGIT is the eight bit port used to enable, one at a time, the individual characters of an eight-digit seven-segment display, while also strobing the rows of the keyboard. The highest order bit, BIT7, enables the leftmost character and the bottom row of the keyboard; BIT4 enables the top row of the 4x4 keyboard and the fourth character; BIT0 enables the rightmost character. BIT3-BIT0 could also strobe a 4x8 keyboard. Accessing a look-up table called CHRSTB accommodates the enabling of one bit (active high or low). This technique takes about four bytes more ROM than a technique of rotating a one through a field of zeros in the accumulator an appropriate number of times, but it allows some additional flexibility: if the drivers being used have a combinatorial input (as in the 7545x family of high-current, high-voltage drivers), the CHRSTB table could provide encoded outputs. For example, six bits of buffered output could enable nine digits – 001001, 001010, 001100, 010001, 010010, 010100, 100001, 100010, 100100. If the I/O lines need to be conserved or if many digits must be displayed, you could add an external decoder to the system.

You could realize easily some of the more complex functions listed in **Table 1** by linking together other utilities. **Fig 5** shows how the various subroutines interrelate. Several of the low level utilities are accessed by higher levels, as well as being accessible to the main program itself. The short test program was included in **Table 1** to echo key depressions as they were detected and to invoke four demonstration subroutines.

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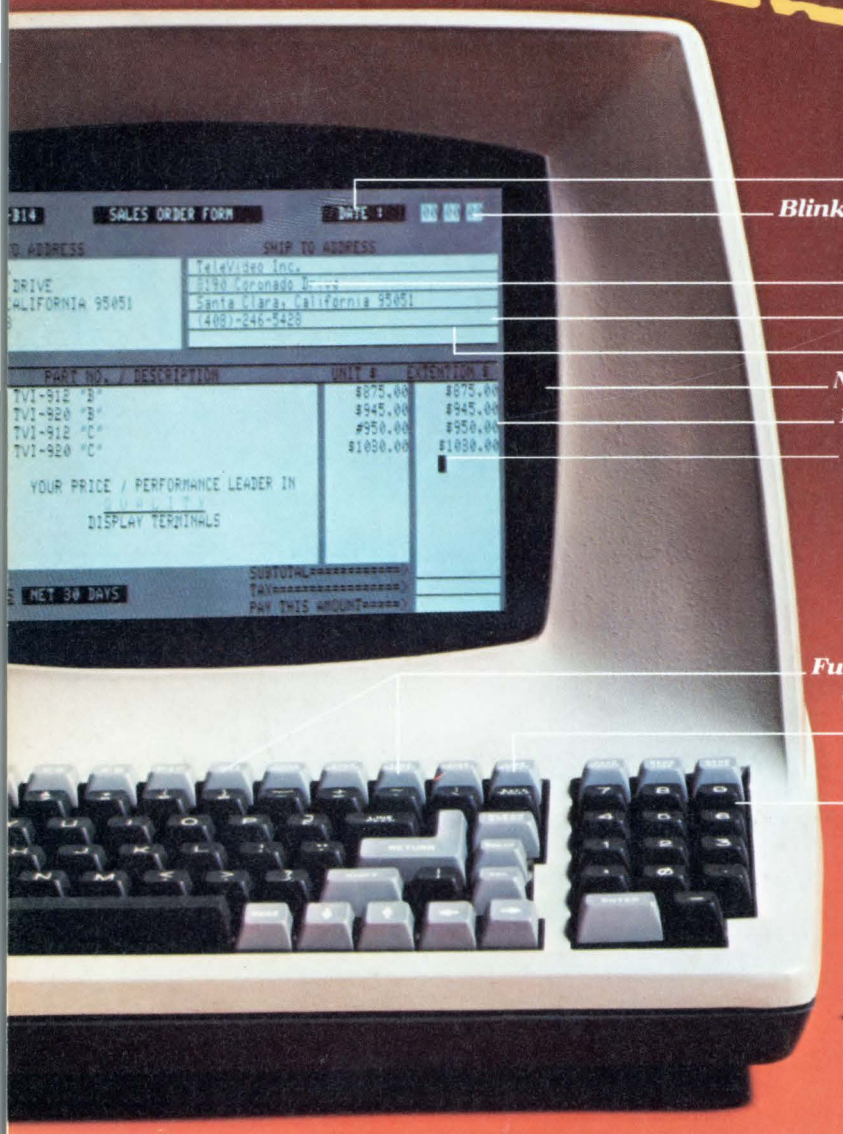

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