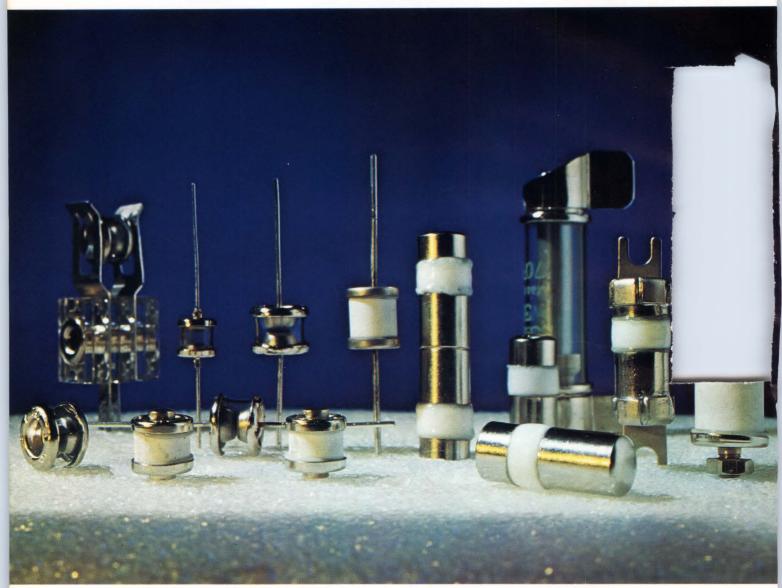
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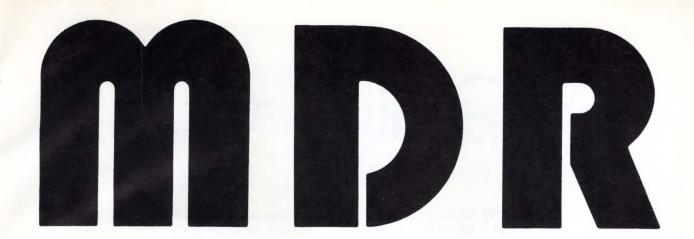
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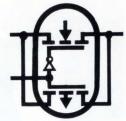
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CMOS FETs



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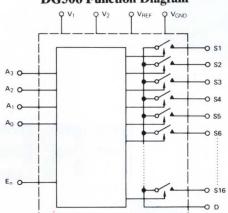
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Here is a single-pole 16-channel multiplexer using paired CMOS FETs, with drivers controlled by a 4-bit binary word input plus an Enable-Inhibit input—all on one chip! Check the functional diagram and then refer to the decode truth table to see what binary word input selects which switch.

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- ON resistance <500 ohms
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- 36 mW standby power

# **DG506 Function Diagram**



## **Decode Truth Table**

<b>A</b> <sub>3</sub>	A <sub>2</sub>	Α1	Α0	En	ON SWITCH
х	Х	х	Х	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0 0 0 0 0 0 0 1 1	0		0	1	2 3 4 5 6 7
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1 1 0	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10 11
1	0		0	1	11
1	0	1 1 0	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

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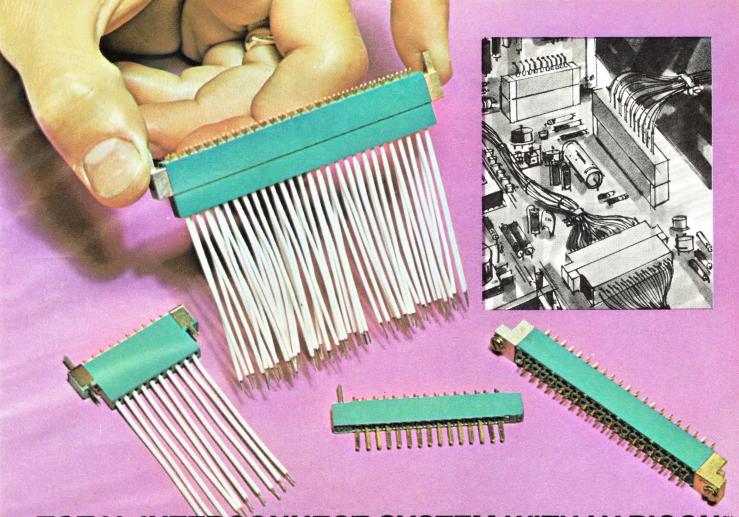
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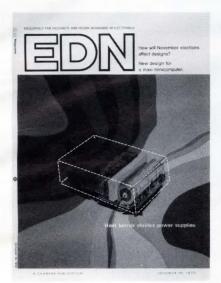
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CORNING



OCTOBER 15, 1972 VOLUME 17, NUMBER 20



## **COVER**

Foam thermal barrier isolates heatsensitive components and allows Acopian to shrink power supply sizes. See story on page 62.

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# **DESIGN FEATURES**

Wider and wiser use of the Nation's engineers is in the offering-if you can believe the

ECL shift registers make versatile pulse delay networks ........ 32 This high-speed shift register can accomplish any desired delay in steps of 10 nsec for timing basic computer decisions or as an adjustable delay line.

Novel computer organization results in design for a maxi-mini ... 39 This mini design is intended for dedicated real-time control systems where minimum program running time and high accuracy are important.

Paying attention to the user's needs can pay off in wide customer acceptance. Here's how a larger and faster terminal was reconfigured to look like the ASR33.

One transistor provides ECL to LED interface . . . Wide-range ramp generator has programmable outputs . . . Rules of thumb avoid production problems . . . Self correction logic for the Johnson counter . . . Another reader responds to odd-modulo divider . . . Vertical sync separator has no integrating network.

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# More of our views on this and that

Here's another collection of opinions, gripes and just plain thoughts we've had lately concerning engineers and the electronics industry:

 We enjoy writing this editorial column. We really do. And we enjoy even more reading the letters and cards we get commenting on the column. Our editorials have been described at one time or another clear across the scale from great to lousy. Recently we even received a card saying that one particular editorial was "pure, unadulterated Cream of Farina," which is a rather nice way of saying something that we believe was not meant to be too flattering. Nevertheless, we appreciate every comment we get, both positive and negative.

· Speaking of cards and letters, we should mention the Signals and Noise section, which appears at the back of each issue. Among other things, this section is, in effect, the reader's editorial column. It provides you the means, via a letter to the editor, to air your opinions, gripes and thoughts concerning engineering and the industry. Take advantage of it. Do, though, try to keep your letters as short as possible. Excessive length

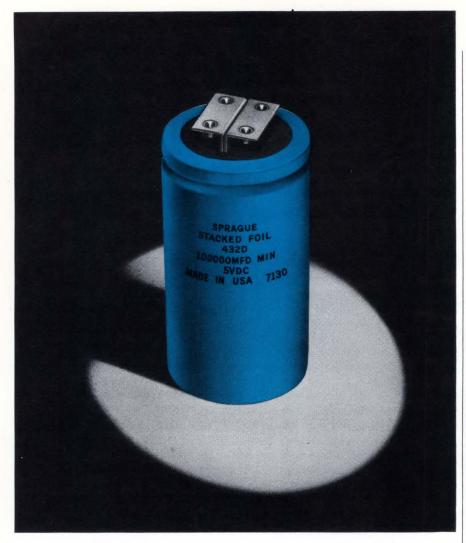
is one of the biggest barriers to our publishing a letter.

 Next year marks the 25th anniversary of the introduction of the transistor by Bell Telephone Labs. Those first point-contact devices may have been unsophisticated and difficult to work with, but they opened the door to the junction transistor, which to a large extent began electronics as we know it today. Everyone now takes the transistor for granted, but can you imagine what the field of electronics would be like

had it never been developed?

 We've always felt that the field of electronics is filled with bright, dynamic aggressive people, which is undoubtedly the fundamental reason for the accomplishments wrought by electronic technology. Some of these bright people, though, get so wrapped up in their own areas of specialty they can't see the woods for the trees. They feel, act and talk as if their particular area of technology is all that really matters, be it semiconductors, instrumentation, electromechanical devices or passive components. To them, anything outside of their specialty is strictly of peripheral interest. Such an outlook is unfortunate, in so much as it diminishes these people somewhat in the eyes of their broad-viewed colleagues, but also because it eventually acts as an impossible barrier to their full development as engineers and people.

Frank Gan Editor



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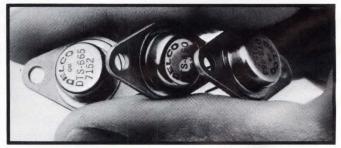
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# Local design center brings custom LSI capability directly to the electronic equipment designer.

With the opening of their first Localogic<sup>TM</sup> design center in Lexington, Mass. last month, Motorala Semiconductor has taken the first step in giving electronic equipment designers the ability to custom design their own LSI chips without traveling to the IC manufacturer's facility and without divulging proprietary information.

A Localogic design center is a stand alone, complete CAD facility, with the same hardware and Motorola developed software presently used in Phoenix.

The center is aimed primarily at companies that have requirements for 10,000 to 30,000 piece part production runs.

Bob Diamond, Motorola manager of remote design centers, estimates the cost of a typical chip design at \$5,-000. He estimates another \$7,000 for fabrication of prototypes from the tapes produced by the center. Actual charges at the design center are \$100 per hour for computer time, \$50 per hour for plotter time and \$25 per hour for consultant time. Consultation is available from the design center resident staff, which includes senior circuit design personnel.

All tapes, plots and programs produced at the center belong to the customer. And after prototypes are built, he also owns the masks. This allows him to get competitive bids for his production run and also sets up a second-source capability.

At the logic center, a customer is first put through a brief training and familiarization program that equips him to work from the system directly on his own chip design, using the Motorola library of completely characterized logic cells.

Each logic cell is a complete function (inverter, quad gate, etc.) used as standard building blocks. These are



X-Y plot shows position of cells and interconnection scheme. In the background is the main computer, a CDC 1700, a disk system with 1.5 million word capacity, and DEC PDP 11/15 used as an I/O processor and plotter control.

handled as units by design automation programs in conjunction with maninteractive machines.

The cell system, trademarked Polycell, presently contains over 100 functions. First is P-channel metal gate MOS. Next is P-channel silicon gate. And finally there are metal gate CMOS devices.

According to Motorola, the cell system provides an order of magnitude improvement over conventional CAD techniques in speed, simplification,

flexibility and economy.

For most design programs, a design center has three outputs:

- a verified data base (mag. tape) for generating production mask artwork.
- a completely graded program (also tape) for computer testing of devices manufactured from the masks.
- •an ink plot for physical checking of the entire design.

For more information check. . . . . 261

# Fiberoptics open new passageways in communication

In the quest for new and improved communication methods, scientists are now considering the use of light waves for data transmission through sheathed glass-fiber conductors as well as through the free atmosphere.

Siemens has recently built two experimental routes with transmission channels made of glass fiber for videotelephone and speech signals. The glass fiber used in the experimental setup at Siemens has a diameter of  $100~\mu m$ . Total reflection occurs along the fiber so that the light ray is always reflected back to the core even when there are bends in the fiber.

With the glass fiber used today, it is theoretically possible to transmit more than 50 megabits/sec, which corresponds approximately to a TV picture channel. A multiple of this will be possible in the future.

The great advantage of thin glass fibers is that they can probably transmit communications far more economically than the heavier copper wires of a telephone subscriber line.

The video and sound signals to be transmitted are converted to amplitude modulated pulses (**Fig. I**) with a repetition frequency of 2 MHz. A gallium arsenide (GaAs) laser diode generates light pulses of a corresponding intensity from these pulses, which enter one end of a glass fiber located close to the laser diode.

At the other end of the transmission section, a photodiode converts the light pulses back to current pulses. The original communication signals are recovered by amplification and demodulation.

However, even the best fibers available have such losses that after a line length of 1 kilometer, only 1% of the original radiation energy is available. It is therefore necessary to amplify after every few kilometers with tiny laser diodes and photodiodes.

Apparently DuPont has partially solved this problem by developing a more efficient fiber as was seen in a

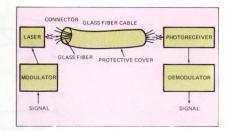


Fig. 1—Siemens' basic scheme for the transmission of video and sound signals through glass fibers.

demonstration at the N.Y. Coliseum during the Electro-Optical Conference last month.

A TV set was operated with both the audio and vido channels reaching it through a single transparent optical fiber (**Fig. 2**). What's more, the reception was free of electronic noise.

Clearly, this exhibition demonstrated jointly by the DuPont Company and Electro Fiberoptics Div. of Valtec Corp. showed how a number of signals may be simultaneously multiplexed through an optical fiber with perfect resolution and no interference.

DuPont developed the "Crofon" fiber-optics material used in the demonstrations, and Electro Fiberoptics developed the technology for using it as a data communications link in electronic equipment.

Because of their ability to perform like a coaxial cable, light guides made of "Crofon" may open an entire new horizon in the electronics industry, the two companies believe.

A large plus in favor of glass fibers for data communication, is its noise immunity. In the demonstration with the TV set, the optical fiber ran alongside a spark tester, yet no noise was visible on the screen.

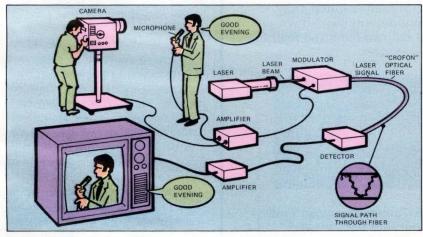


Fig. 2—The successful transmission of TV signals through a single "Crofon" optical fiber was recently accomplished by Du Pont and Electro Fiberoptics.

# Thermal battery weighs 1-1/2 oz; gives 1000V at low current.

A 1-1/2 ounce battery that will yield 1000V at low current for up to 50 seconds has been invented at Sandia Laboratories. It replaces a 500V battery that measures 6.6 cubic inches and weighs a half pound.

Thermal batteries are used in nuclear weapons and in other systems where high voltage would be needed only once, after a period of storage.

They are "one-shot" devices actuated by a small heat-producing (pyrotechnic) charge. After the heat melts the electrolyte in a series of battery cells, the electrolyte becomes conductive and the battery produces electricity via an electrochemical reaction.

The radically new cell stack configuration of the Sandia battery eliminates many of the problems presented by previous designs that included heat generating material as part of each cell or pair of cells.

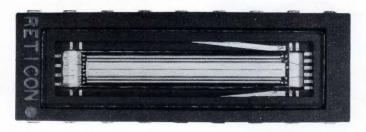
Here, the cells are placed in electrically-insulating, thermally-conducting beryllium oxide tubes. A pyrotechnic material such as iron-potassium perchlorate is located in bulk form outside the tubes. This permits a large increase in the number of cells per



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A Sandia prototype contains 84 cells of this type in a stack, with two pairs of cell stacks connected in series. It is activated by an electrical signal which ignites an electrical "match," a fuse strip, and the pyrotechnic heat generating material.

This design provides two 3-mA, 500V, 50-sec bursts of energy from a package less than a cubic inch and weighing less than 0.9 pound. □

# Superconductivity at 20.3° K cuts cooling costs

For the first time, scientists at RCA Laboratories in Princeton, N. J. have achieved superconductivity in a two-element compound, niobium gallium, at a temperature of 20.3°K (-423. 6°F.) This is only the second time that superconductivity has been observed in any material above 20°K.

Because of its simplicity, the new two-element material is expected to be developed quickly into practical systems.

The eventual result of RCA's achievement could be as much as a 75% reduction in the very-high cooling costs associated with superconductivity. The niobium gallium compound not only is superconducting at a relatively high temperature, but can also be superconducting in far more intense magnetic fields than existing superconductors.

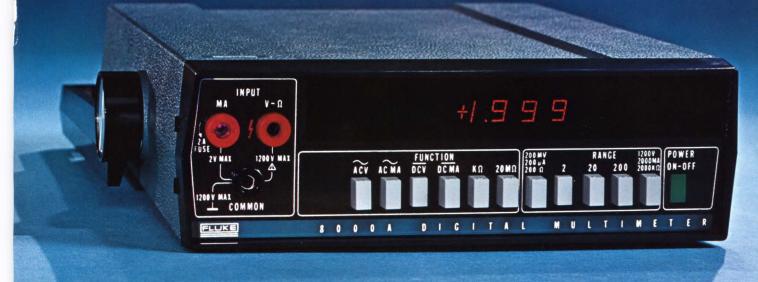
These combined attributes could result in superconducting devices operating at significantly higher temperatures than have been possible up to now. It may even be possible to make practical superconductive systems operate efficiently in magnetic fields larger than 100 kilogauss at 14°K.

The fact that superconductors can carry large amounts of current in large magnetic fields means that generators, motors, transmission lines and magnets employing superconductors can be made much smaller, lighter, and more efficient than conventional equipment.

RCA scientists are presently investigating improved methods of preparing this new niobium gallium which will be suitable for large scale production of superconducting wire or tape.

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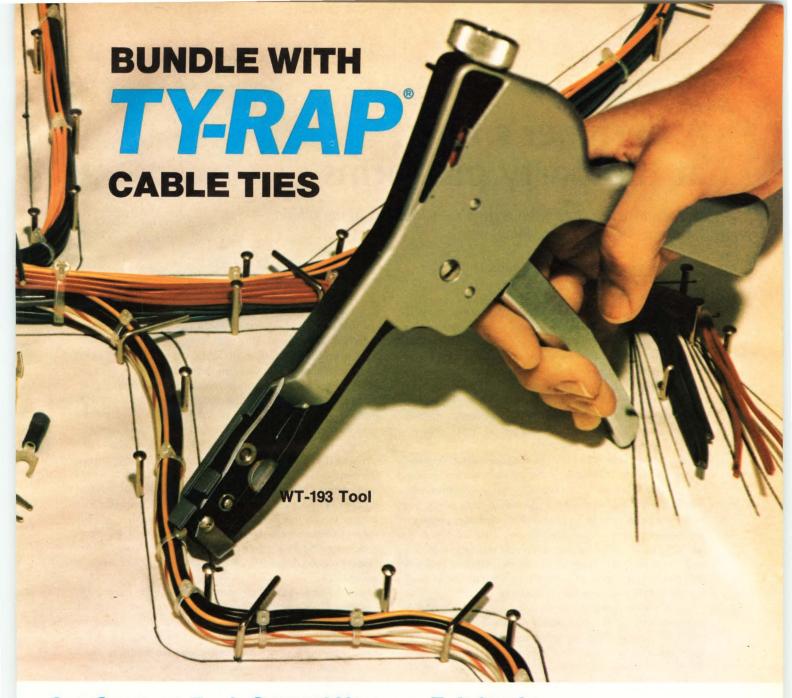
This configuration of the spring-like locking fork terminal itself, is another new idea from T&B. The terminal snaps on like a fork tongue and stays on like a ring tongue. No need to remove screws or nuts to install the terminal.



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# **DESIGN INTERFACE**

# A designer's look at the party platforms

Wider and wiser use of the Nation's engineers is in the offering—if you can believe the politicians

Robert H. Cushman, Special Features Editor

The typical apolitical designer is prone to pass off the platform statements of the political parties as so much "hot air", and that has often been a reasonable course of action. But this year, some rather new and promising prospects for better employment of engineers lie buried in the verbosity of the Democratic and Republican party platforms. Finally, both parties are talking about putting engineers to wider national use than just building bombs. Apparently the success of the moon mission has awakened many people's minds as to what engineers can do.

Both parties state that they see engineers (scientists and technologists, as they say) as the logical problem solvers for our nation's "new" problems, such as environment, housing, mass transportation and energy. Both imply that technology can help solve such interdisciplinary problems as health delivery, crime control and drug addiction. In addition, both parties propose laws and regulations to protect consumers and safeguard workers, which if enacted, will surely force private industry to employ more engineers and buy more electronic products.

If you'll turn to where we've lined up the table of subject headings for the two platforms side by side (pg. 25), you'll see that both touch pretty much on the same subjects, but they arrange these subjects according to quite different priorities. The Democrats put domestic "people problems" first, and foreign policy and military spending last. The Republicans put foreign policy and military spending first and the "people problems" last. Both put "Science and Technology" in the middle.

We've printed excerpts from the portions on military spending and science and technology verbatim (pg. 23 and pg. 24), as these apply directly to engineers. From our study of these sections and our talks with the staffs of the candidates at their Washington headquarters and with other observers on the Washington scene, we've arrived at some tentative conclusions. We don't offer these as aids to voter decision making, as in our narrow concentration on the technical aspects of the platforms we've ignored some of the more important general issues, but we do feel they might help engineers evaluate how current politics might affect their careers.

# How soon? How big?

The most immediate promise of a substantial number of new engineering jobs lies not in these new directions, however. It lies in the Republican party's goal of revitalizing defense R&D. As the excerpt from the Republican platform shows, even this promise is not specifically stated. It

can be assumed, though, that as the Republicans are committed to keeping our weapons more than competitive with our adversaries, who, according to the Republicans, have been outspending us on R&D, we will have to again start spending on new weapon development.

Thus, it can be reasoned that President Nixon, if reelected, would propose that some of the defense funds released by the wind-down of Viet Nam be used for developing new weapons. An engineer in advanced development at the Navy (whose office is within walking distance of the White House, if that means anything) tells us the emphasis is now swinging towards new types of weapon systems, to help us overcome the stagnation of reduced R&D over the past four years. The \$80 billion defense budget which the Republicans wish to sustain is still the biggest sector of the Federal budget of which engineers can with certainty expect a slice. If re-elected, Nixon could propose defense R&D programs that would produce jobs by '74.

But the new-priority programs represent the most exciting long range opportunities for engineering employment. McGovern has repeated and enthusiastically called for numbers of "NASA-like" programs to be directed at pollution, mass transportation, housing, etc. He wants as much money spent on these programs and as many engineers employed as have been "wasted" on military R&D, he says. He is talking of annual budgets in the order of \$3 billion for these programs. He says that unlike defense programs, these new priority efforts will be fundamentally long term, for as soon as any one problem is solved, there will be some more to be tackled.

McGovern's proposals sound like the answer to many an idealistic engineer's dreams. The problem is that nobody can be sure that McGovern could get these programs through Congress. As one R&D engineer familiar with Washington politics tells us, "First he'll have to convince Congress to make his drastic cuts in the defense budget to free the money. There is bound to be resistance to that. Then he'll have to build up the brand new agencies that will contract out these new programs. That will take more time. An engineer would be lucky if he saw any jobs coming out of these new programs before McGovern's four year term was up. He'd probably find that he'd lose his job in the first wave of defense cutbacks and then remain jobless (or on one of McGovern's proposed interim "conversion" programs) some time before he was able to find an opening in one of the new-priority programs."

The Republicans, too, talk of using engineers on these

## **DEMOCRATIC**

Science and Technology

For years, the United States was the world's undisputed leader in science and technology. Now that leadership is being challenged, in part because of the success of efforts in other countries, and in part because of the Nixon Administration's neglect of our basic human and material resources in this field.

As Democrats, we understand the enormous investment made by the nation in educating and training hundreds of thousands of highly skilled Americans in science and technology. Many of these people are now unemployed, as aerospace and defense programs are slowly cut back and as the Administration's economic policies deprive these Americans, as well as others, of their livelihood.

So far, however, the Nixon Administration has paid scant attention to these problems. By contrast, the Democratic Party seeks both to increase efforts by the federal government and to stimulate research in private industry.

In addition, the Democratic Party is committed to increasing the overall level of scientific research in the United States, which has been allowed to fall under the Nixon Administration. And we are eager to take management methods and techniques devised for the space and defense programs, as well as our technical resources and apply them to the city, the environment, education, energy, transportation, health care and other urgent domestic needs. We promise also to work out a more effective relationship between government and industry in this area, to stimulate the latter to a greater research and development effort, thus helping buoy up the economy and create more jobs.

Finally, we will promote the search for new approaches in science and technology, so that the benefits of progress may be had without further endangering the environment indeed, so that the environment may be better preserved. We must create a systematic way to decide which new technologies will contribute to the nation's development, and which will cause more problems than they solve. We are committed to a role for government in helping to bring the growth of technology into a harmonious relationship with our lives.

# Political Party Statements on Science and Technology

(exerpted from platforms)

### REPUBLICAN

Science and Technology

Basic and applied scientific research and development are indispensable to our national security, our international competitive position, and virtually every aspect of the domestic economy. We have initiated a new research and development strategy which emphasizes a public-private partnership in searching out new ideas and technologies to create new jobs, new internationally competitive industries and new solutions for complex domestic problems.

In support of this strategy we have increased Federal effort in civilian research and development by 65 percent—from \$3.3 billion to \$5.4 billion—and expanded research in drug abuse, law enforcement, health care, home building, motor vehicle safety, energy and child development as well as other fields.

We will place special emphasis on these areas in which break-throughs are urgently needed:

- -Abundant, clean-energy sources;
- -Safe, fast and pollution-free transportation:
- -Improved emergency health care;
- Reduction of loss of life, health and property in natural disasters:
- Rehabilitation of alcoholics and addicts to dangerous drugs.

Additionally, we urge the fair and energetic enforcement of all fire prevention laws and applaud the work of the National Commission of Fire Prevention and Control. We encourage accelerated research on methods of fire prevention and suppression, including studies on flammable fabrics, hazardous materials, fire equipment and training procedures.

The space program is yielding impressive dividends in earth oriented applications of space technology—advances in medicine, industrial techniques and consumer products that would still be un-

known had we not developed the technology to reach the moon. We will press ahead with the space shuttle program to replace today's expendable launch vehicles and provide low-cost access to space for a wide variety of missions, including those related to earth resources. We pledge to continue to extend our knowledge of the most distant frontiers in space.

We will also extend our exploration of the seabed and the sea. We will seek food for the hungry, power for future technologies, new medicines for the sick and new treatments of water for arid regions of the world.

The quantities of metals and minerals needed to maintain our economic health and living standards are so huge as to require the re-use of all recoverable commodities from solid waste materials. We pledge a vigorous program of research and development in order to seek out more economical methods to recover and recycle such commodities, including the processing of municipal solid wastes.

We pledge to extend the communications frontier, and to foster the development of orbiting satellite systems that will make possible wholly new, world-wide educational and entertainment programs.

We recognize that the productivity of our Nation's research and development efforts can be enhanced through cooperative international projects. The signing of the Moscow agreements for cooperation in space, environment, health, and science and technology has opened a new era in international relations. A similar agreement between the United States and Polish Governments will permit expansion of programs such as the jointly funded Copernicus Astronomical Center and the Krakow Children's Hospital.

Finally, we pledge expanded efforts to aid unemployed scientists and engineers. We are determined to see that such on-going efforts as the Technology Mobilization and Reemployment Program are effective.

# Political Party Statements on Defense Weaponry

(exerpted from platforms)

### DEMOCRATIC

Military Policy

We propose a program of national defense which is both prudent and responsible, which will retain the confidence of our allies and which will be a deterrent to potential aggression.

Military strength remains an essential element of a responsible international policy. America must have the strength required for effective deterrence.

But military defense cannot be treated in isolation from other vital national concerns. Spending for military purposes is greater by far than federal spending for education, housing, environmental protection, unemployment insurance or welfare. Unneeded dollars for the military at once add to the tax burden and pre-empt funds from programs of direct and immediate benefit to our people. Moreover, too much that is now spent on defense not only adds nothing to our strength but makes us less secure by stimulating other countries to respond.

Under the Nixon stewardship of our defense policy, lack of sound management controls over defense projects threatens to price us out of an adequate defense. The reaction of the Defense Department to exposure of cost overruns has been to strike back at the critics instead of acting to stop the waste.

Needless projects continue and grow, despite evidence of waste, military ineffectiveness and even affirmative danger to real security. The "development" budget starts pressures for larger procurement budgets in a few years. Morale and military effectiveness deteriorate as drugs, desertion and racial hatreds plague the armed forces, especially in Vietnam.

The Democratic Party pledges itself to maintain adequate military forces for deterrence and effective support of our international position. But we will also insist on the firm control of specific costs and projects that are essential to ensure that each defense dollar makes a real contribution to national security. Specifically, a Democratic Administration should:

Plan military budgets on the basis of our present needs and commitments, not past practices or

force levels;

Stress simplicity and effectiveness in new weapons and stop goldplating and duplication which threatens to spawn a new succession of costly military white elephants; avoid commitment to new weapons unless and until it becomes clear that they are needed;

Reject calls to use the SALT agreement as an excuse for wasteful and dangerous acceleration of our military spending;

Reduce overseas bases and forces: and

Rebuild the morale and military tradition of our armed forces through creative programs to combat drug abuse, racial tensions and eroded pride in service. We will support reforms of the conditions of military life to restore military service as an attractive career for men and women from all segments of our society.

By these reforms and this new approach to budgeting, coupled with a prompt end to U.S. involvement in the war in Indo-China, the military budget can be reduced substantially with no weakening of our national security. Indeed a leaner, better-run system will mean added strength, efficiency and morale of our military forces.

Workers and industries now dependent on defense spending should not be made to pay the price of altering our priorities. Therefore, we pledge reconversion policies and government resources to assure jobs and new industrial opportunities for all those adversely affected by curtailed defense spending.

### REPUBLICAN

# A Modern, Well Equipped Force

We believe that the first prerequisite of national security is a modern, well equipped armed

From 1965 to 1969 the Vietnam war so absorbed the resources of the Defense Department that maintenance, modernization, and research and development fell into neglect. In the late 1960's the Soviet Union outspent the United States by billions of dollars for force modernization, facing the United States with the dangerous prospect that its forces would soon be qualitatively inferior. Our Reserve Forces and National Guard had become a dumping ground for cast-off arms and equipment. The military posture of our country became seriously undermined.

To assure our strength and counter the mounting Soviet threat. President Nixon directed:

the most significant ship construction and modernization program since World War II;

the development of new types of tactical aircraft such as the F-15, a lightweight fighter, and a fighter plane for close support of ground troops;

improvements in our strategic bomber force and development of the new B-1 strategic bomber;

development of a new TRI-DENT submarine and undersea missile system;

greatly increasing the capability of existing strategic mis-siles through multiple warheads:

- strengthening of strategic defenses, including initial deployment of an anti-ballistic missile system;

the largest research and development budget in history to insure continued technological superiority;

 equipping of the National Guard and Reserves with the most modern and sophisticated weapons;

-improved command and control communications systems.

We draw a sharp distinction between prudent reductions in defense spending and the meat-ax slashes with which some Americans are now beguiled by the political opposition. Specifically, we oppose plans to stop the Minuteman III and Poseidon programs, reduce the strategic bomber force by some 60 percent, cancel the B-1 bomber, reduce aircraft carriers from 16 to 6, reduce tactical air wings by a third, and unilaterally reduce U.S. forces in Europe by half.

### Democratic Theme: "For the people" U.S. Party Platforms '72 I. New directions II. Jobs, prices and taxes (in terms of section headlines Jobs, income and dignity full texts of each run over **Economic management** Toward economic justice 100 typed pages) Tax reform Labor management relations Labor standards Occupational health and safety Farm labor III. Rights, power and social justice Republican Free expression and privacy Theme: "A Better Future for All" Right to be different Rights for children, women, youth, poor people, American Indians, physically disabled, mental-I. PREAMBLE ly retarded, elderly, veterans, servicemen and service women, and consumers. II. TOWARD A FULL GENERATION OF PEACE **Foreign Policy** Quality and quantity of social service New Era of Diplomacy Health care The Nixon Doctrine Family planning Peace in the 1970's Puerto Rico The Middle East Virgin Islands, etc. The Atlantic Community IV. Cities, communities, counties and the environment Japan Partnership among governments The Soviet Union Urban growth policy China The cities Latin America Housing and community development Africa New towns Defense Transportation A Modern, Well Equipped Force Environment, technology and resources A New Partnership Choosing the right methods of An All-Volunteer Armed Force environmental protection Improvements in Service Life lobs and the environment Better Defense Management Science and technology **Arms Limitation Energy resources** For the Future The oceans III. A NEW PROSPERITY Public lands Jobs, Inflation and the Economy V. Education Strategies and Achievements School finance The Road Ahead Early childhood education **Taxes and Government Spending** Equal access to quality education International Economic Policy Bilingual education Small Business Career education (technicians) IV. IMPROVING THE QUALITY OF LIFE Higher education Health Care Arts and humanities Education VI. Crime, law and justice Welfare Reform Preventing crime Law Enforcement Narcotic drugs The Fight Against Organized Crime Organized and professional crime Rehabilitation of Offenders Rehabilitation of offenders Drug Abuse The quality of justice Agriculture and Rural Life Farming and the rural life Community Development Exporting our abundance Housing Strengthening the family farm Transportation Guaranteeing farm people a voice Environment Revitalizing rural America Natural Resources and Energy **Foreign policy** Vietnam Science and Technology Military policy The Individual and Government Volunteerism Disarmament and arms control Arts and Humanities A BETTER FUTURE FOR ALL US and the world community International economic policy Children **Developing nations** Youth The methods and structures of **Equal Rights for Women** US foreign and military policy Older Americans IX. The people and the government Working Men and Women Senority **Ending Discrimination** Secrecy Spanish-speaking Americans Administrative agencies Indians, Alaska Natives & Hawaiians Conflict of interest Consumers Campaign finance Veterans Regulation of lobbyists CONCLUSION Taking part in the political process

new-priority problems, but because they are not planning to cut back on the defense budget to make large funds available, their new-priority programs must necessarily be much smaller.

There is another problem with these new-priority programs so far as engineers are concerned, we feel. They will be less clean cut than NASA. NASA's concern was a pure, extra-terrestrial one, and therefore, one that could be tackled objectively by engineers on their own. These new-priority programs are for messy earth-bound projects and it is likely they will be riddled with politics and confusion. Engineers will probably not be running these shows. They'll find they'll be working for sociologists and naturalists. It will be something like the experiences engineers have faced in medical electronics where they have to work under doctors and hospital administrators. But this is no reason for shying away from the problems.

## Engineering societies' view

How does the NSPE (National Society of Professional Engineers) which now also represents the IEEE as a lobbying front view the platforms? Paul Robbins, executive director of NSPE, told us that in conjunction with the IEEE (and a few other societies) the NSPE put the following suggestions for "planks" before the platform committees of both parties:

- 1—"To utilize fully the technological capacity of engineers and scientists in the development of economic progress and the solution of social problems in the Nation."
- 2—"To revise private pension plan laws to protect employees who are forced to change jobs frequently because of changing technological priorities."

Robbins feels that both suggestions were adopted to some degree by both parties. In the case of engineers being used on non-defense problems he said the Democratic platform expressed understanding of "the enormous investment made by the Nation in educating and training hundreds of thousands of highly skilled Americans in science and technology" and acknowledges that, "Many of these people are now unemployed as aerospace and defense programs are slowly cut back . . ." He said he liked the way the Democrats then pledged to increase the overall level of research in private industry, and to apply space and defense techniques to domestic problems while at the same time creating more jobs and buoying the economy.

The Republican platform pledges ". . . expanded efforts to aid unemployed scientists and engineers" and ". . . to

see that such on-going efforts as the Technology Mobilization and Reemployment Program are effective." The Republicans also support basic and applied R&D and point to initiation of a new R&D strategy, emphasizing a public-private partnership in searching out new ideas and technologies in order to create new jobs, new industries, and new solutions to complex domestic problems.

On the question of pensions, Robbins says he finds the Democratic platform reading, "to protect individual's pension rights by pension reinsurance and early vesting," encouraging. In the Republican platform, he likes the way they cite their activities in trying to get measures to "strengthen private pension plans through tax deductions that encourage their expansion, improved vesting, and protection of the investments in these funds."

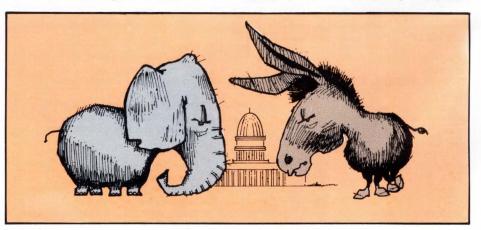
# Summing up the engineering viewpoints

From our talks with engineers in general we guess that they will be torn between their natural conservatism (in the sense they like to see in-depth analysis behind any proposed action) and their long-standing desire to see their problem-solving talents being more widely used by their country. Nixon will appeal to their minds and McGovern will appeal to their hearts.

A factor in some engineers' decision making may be their resentment over the aloof treatment they have received from the Nixon administration. As another official of the NSPE privately told us, "I'm afraid the Nixon administration has only given token aid to engineers displaced by defense cutbacks and foreign competition."

Yet this same man was also concerned about whether McGovern, if elected, could really convince Congress in these tight-money times to start spending tens of billions of dollars on NASA-like programs to combat pollution, etc. He is not sure that the U.S. voters are afraid enough yet of these new threats to encourage Congress to increase our national deficit. It might be that with McGovern the engineers would be more certain of loosing more additional defense jobs than they would be of gaining new non-defense jobs.

Our own view is that the very fact that both platforms now talk of technology as a basic problem-solving tool is in itself extremely encouraging. EE's eventually ought to benefit, for while there is a mounting concern about the harmful effects of other technologies (chemical, power and automotive) there is no sign in either platform (other than some brief references to wire tapping) that either party feels electronics is anything but a problem solver.



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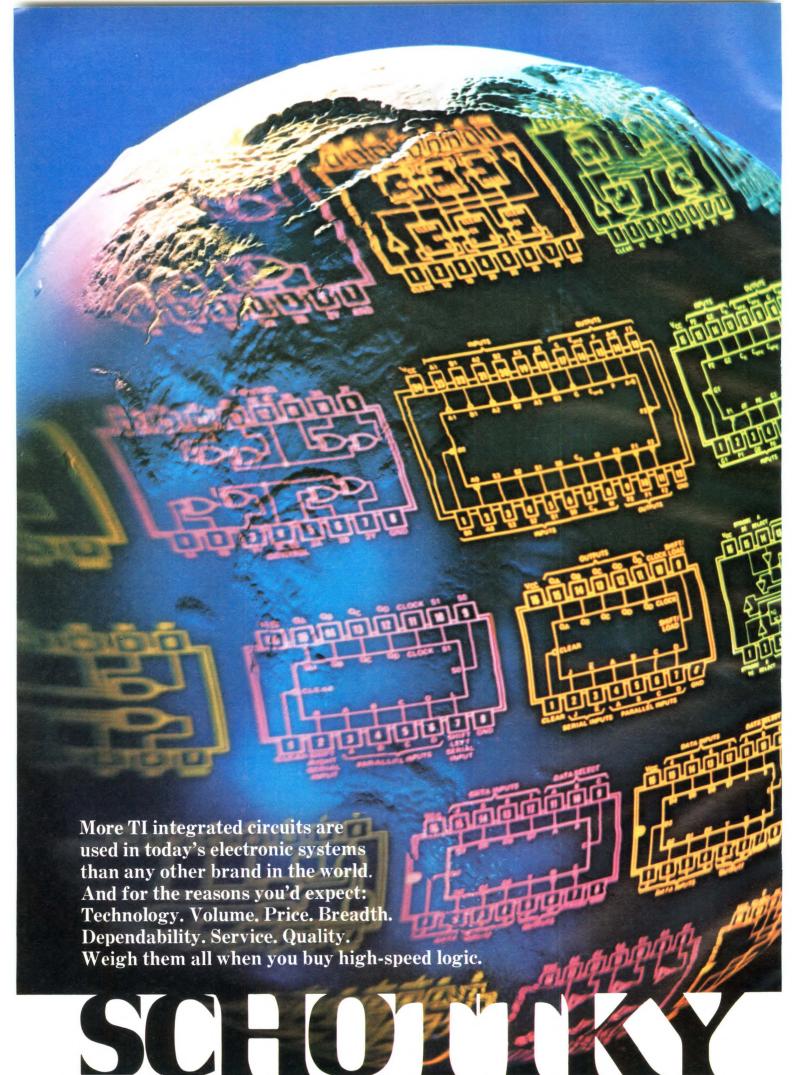
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SN54S/74S175	Quad D-type flip-flop, complementary outputs/clear
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SN54S/74S195	4-bit parallel-access shift register

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SN54S/74S86 SN54S/74S135	Quadruple Exclusive – OR Quadruple Exclusive – OR/NOR
SN54S/74S181	4-bit arithmetic logic unit and function generator
SN54S/74S182	Carry look-ahead generator for SN54S/74S181

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SN54S/74S251	8 to 1-line with tri-state outputs
SN54S/74S157	Quad 2 to 1-line, true output
SN54S/74S257	Quad 2 to 1-line with tri-state true outputs
SN54S/74S158	Quad 2 to 1-line, inverting output
SN54S/74S258	Quad 2 to 1-line with tri-state inverting outputs
SN54S/74S153	Dual 4 to 1-line

### Decoders/Demultiplexers

SN54S/74S138	3 to 8-line
SN54S/74S139	Dual independent 2 to 4-line

### Series 54S/74S Schottky SSI circuits

SN54S/74S00 SN54S/74S03 SN54S/74S04 SN54S/74S05 SN54S/74S10 SN54S/74S11	Quadruple 2-input positive-NAND gate Quadruple 2-input positive-NAND gate, o.c. output Hex inverter Hex inverter, o.c. output Triple 3-input positive NAND gate Triple 3-input positive AND gate
SN54S/74S15	Triple 3-input positive AND gate, o.c. output
SN54S/74S20	Dual 4-input positive NAND gate
SN54S/74S22	Dual 4-input positive NAND gate, o.c. output
SN54S/74S40	Dual 4-input positive NAND buffer
SN54S/74S64	4-2-3-2-input AND-OR-INVERT gate
SN54S/74S65	4-2-3-2-input AND-OR-INVERT gate, o.c. output
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SN54S/74S112	Dual J-K negative-edge-triggered flip-flop (125 MHz) with preset and clear
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SN54S/74S114	Dual J-K negative-edge-triggered flip-flop (125 MHz), common clock and clear
SN54S/74S133	13-input NAND gate
SN54S/74S134	12-input NAND gate with tri-state output
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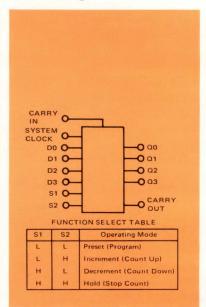
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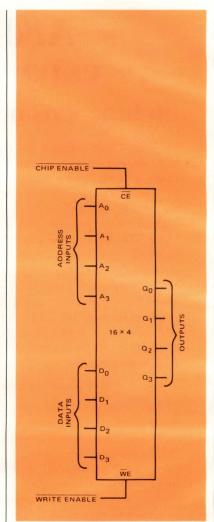
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Just to make it interesting, we have included a "Design Idea" sheet in the file so you can explore ways of using the new devices. Just jot down your circuit diagram showing possible applications using any one or more of the following:



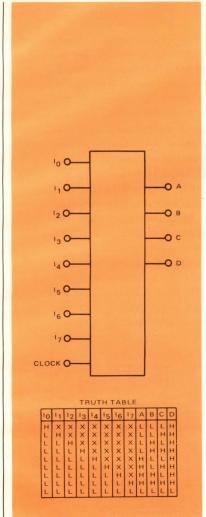
MC10136 Universal Hexadecimal Counter, MC10137 Universal Decade Counter. The MC10136 and MC10137 are both fully synchronous counters, MC10136 is a hexadecimal (0 thru 15 binary) counter, and MC10137 is a BCD decade counter. Logic configurations are similar for both counters.

The flexibility of these devices allows the designer to use one basic counter design for all applications. When used with appropriate MECL III prescalers, frequencies can be extended to over 500 MHz.



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CHECK NO. 16

# ECL shift registers make versatile pulse delay networks

This high-speed shift register can accomplish any desired delay in steps of 10 nsec for timing basic computer decisions or as an adjustable delay line.

Jon M. DeLaune, Motorola, Inc.

Flip-flops that will shift at rates in excess of 100 MHz open many exciting possibilities for new design techniques. For example, these ECL "10,000 Series" devices allow shift register designs that can be employed in many applications as variable digital delay lines.

The flip-flop used in the circuit described here is the MC10135, a dual master-slave dc coupled  $\bar{J}$ - $\bar{K}$  flip-flop with separate asynchronous set and reset inputs and a common clock input. Both flip-flops in the package have complimentary Q and  $\bar{Q}$  outputs provided. Flip-flop specifications include a typical toggle frequency of 140 MHz and typical propagation delay time of 3 nsec. Operating voltage is -5.2V with negligible degradations in operation for  $\pm 10\%$  variations in supply voltage.

**Fig. 1** illustrates a flip-flop logic block connected as a 2-stage shift register. The  $\bar{J}$ - $\bar{K}$  and R-S truth tables for the individual flip-flop are also shown. For shift register operation, the J and K inputs must be complements.

Fig. 2 is the logic diagram for an n-bit shift register

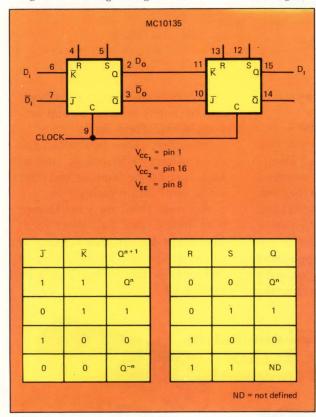
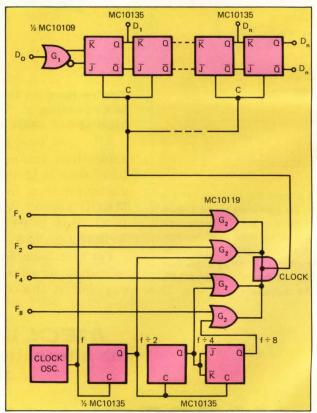


Fig. 1–2-stage ECL shift registers are very simple and can provide pulse delays of any desired length, in increments of 10 nsec. Both  $\bar{J}$ - $\bar{K}$  and RS truth tables are shown.

which includes the necessary logic for controlling the delay of the register by powers of two. The incoming data to be delayed is considered to be asynchronous with the internal clock oscillator, and random in nature. Normal data, once started, may have a random pattern, but the intervals will normally be regular unless used in crypto work or there is noise. The input data ( $D_0$ ) might appear as shown in **Fig. 3** which also illustrates typical waveforms that would result from  $D_0$  and a 50 MHz clock.  $G_1$  is used to split the input into DATA ( $D_0$ ) and NOT DATA ( $D_0$ ) because the  $J-\bar{K}$  flip-flop requires complementary data (dual rail logic). The OR and NOR outputs of each gate have essentially the same propagation delay, so output skew will not present a problem.

The input levels of  $f_1$ - $f_8$  shown in the lower portion of **Fig. 2** allow the selection of the clock frequency  $(f_m/2^m)$  where "m" is the number of flip-flops used to divide the basic frequency of the clock oscillator. Input  $f_1$ - $f_8$  are negative logic inputs, i.e., only one input should be low at a



**Fig. 2—Delay register and variable-rate clock** provide a highly versatile design technique. For large shift registers the clock load of the register may dictate the use of a driver.

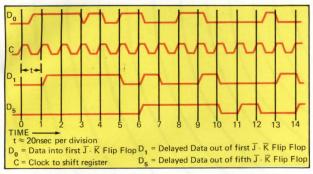


Fig. 3—Typical delay register waveforms for a 50 MHz clock frequency show the relationship of the data input and the first and fifth flip-flop outputs. Note that the pulse on  $D_0$  at t=3 is missed due to its brevity. To insure data capture, the min input pulse must exceed one clockperiod.

time. The low input will enable the desired clock frequency. If all inputs go HIGH, the register will store the data that was being shifted in the register.

## Timing is straightforward

Several of the possible timing conditions that may occur between  $D_0$  and the input clock are illustrated in **Fig. 3**. For example,  $D_0$  is low between time marks 3 and 4. This LOW data input is not picked up by the first flip-flop because no positive clocking edge is present.

For timing purposes, the worst-case parameters for the MC10135 are:  $t_{pd\ max}$  clock to output = 4.5 nsec; setup time = 2.5 nsec; and hold time = 1.5 nsec. **Fig. 4** should help clarify the definition of these parameters. Setup time is defined as the minimum time, prior to the positive going clock, that data to the  $\bar{J}$ - $\bar{K}$  inputs must be settled. The hold time is the minimum time, after the positive going clock, for which the data must be held steady.

The data delay though the first flip-flop is a minimum of the setup time plus the delay time of the flip-flop, or a maximum of the clock period ( $\tau$ ) plus the delay time and the setup time of the flip-flop. With a worst-case delay time for the MC10135 of 4.5 nsec and a setup time of 2.5 nsec, operating at a clock frequency of 50 MHz yields a minimum delay of 7 nsec or a maximum of 27 nsec.

The gate for  $G_1$  is the MC10109 and  $G_2$  is the MC10119; both are high-speed gates. These devices exhibit typical progagation delays of 2 and 3 nsec respectively. Five dual flip-flops may be driven with a typical rise time of 2 nsec and fall time of 3 nsec. If you keep lead lengths short and use low inductance printed circuit wiring, the register shown in **Fig. 2** will shift reliably at clock rates in excess of 100 MHz. The incremental delay from flip-flop 1 to flip-flop 2 is  $\tau$  and this relationship holds throughout the length of the delay register.

### Improvements are available

Two other SSI dual flip-flops may be used to improve the delay register performance. Both the MC10131 and MC10231 devices are type "D" master-slave flip-flops. The type "D" is a single rail device, as opposed to the J-K which, as mentioned, is dual rail. This eliminates the need for  $G_1$  which will allow a higher clock frequency to be used. The MC10131 will operate at 150 MHz typically allowing values of  $\tau$  to be set as small as 6.7 nsec. The MC10231 is an even higher-speed ECL "10,000" device

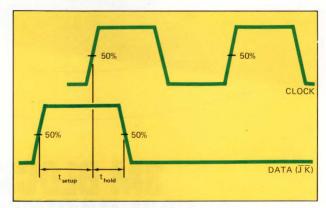
which permits values of  $\tau$  as small as 5 nsec.

Two other MSI devices will provide 4-bits of delay per package at high speed. These are the MC10141 and the MC1694 4-bit shift registers. The MC10141 is typically capable of shift rates in excess of 100 MHz and the MC1694 device will shift up to 300 MHz. Both of these devices are fully compatible with "10,000" Series ECL.

With any flip-flop that has an asynchronous data input, there is a small, but still finite, probability that a data change and a clock change will occur within the "aperture time" of the flip-flop. The "aperture time" of a flip-flop may be defined as the very short period when the decision is made to go to either a ONE or a ZERO. If both data and clock change within this period, the flip-flop delay time will be greater than normally expected. "10,000" ECL is noted for its extremely short aperture time, so these problems are minimized.

The pulse-width degradation and delay-error uncertainties of the output are a maximum of one clock period for asynchronous inputs. This would amount to 10 nsec for a 100 MHz shift register, and can be reduced by using a faster clock.

As you can see, "10,000" Series SSI and MSI functions can be used to form state-of-the-art high-speed delay shift registers. Incremental delays as small as 10 nsec are easily obtained with "10,000" Series ECL and as small as 7 nsec using a higher power series, like ECL III. By using a variable clock generator such as the MC1658 Voltage Controlled Multivibrator, you can obtain a continuous variable delay.

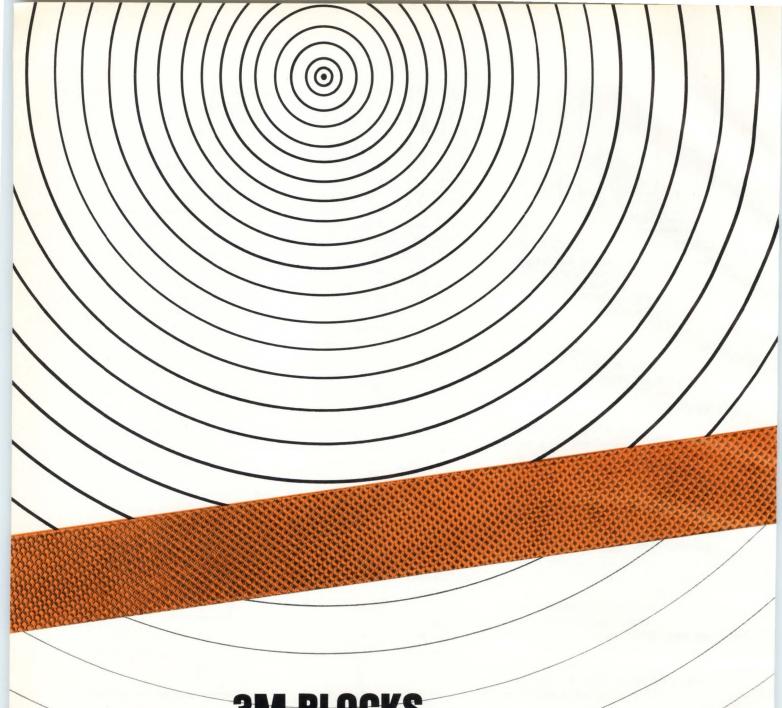


**Fig. 4—Setup and hold time** requirements are defined as shown here. Data must be steady for the indicated time prior to and following the positive-going clock pulse.

# Author's biography

Jon DeLaune is Section Manager of Emitter Coupled Logic and Central Processor Computer Applications at Motorola Inc., Semiconductor Products Div. in Phoenix. He has written numerous high-speed logic articles and has been awarded one patent on digital phase locked loops. He holds a BSEE and a MSEE from Texas A & M University.





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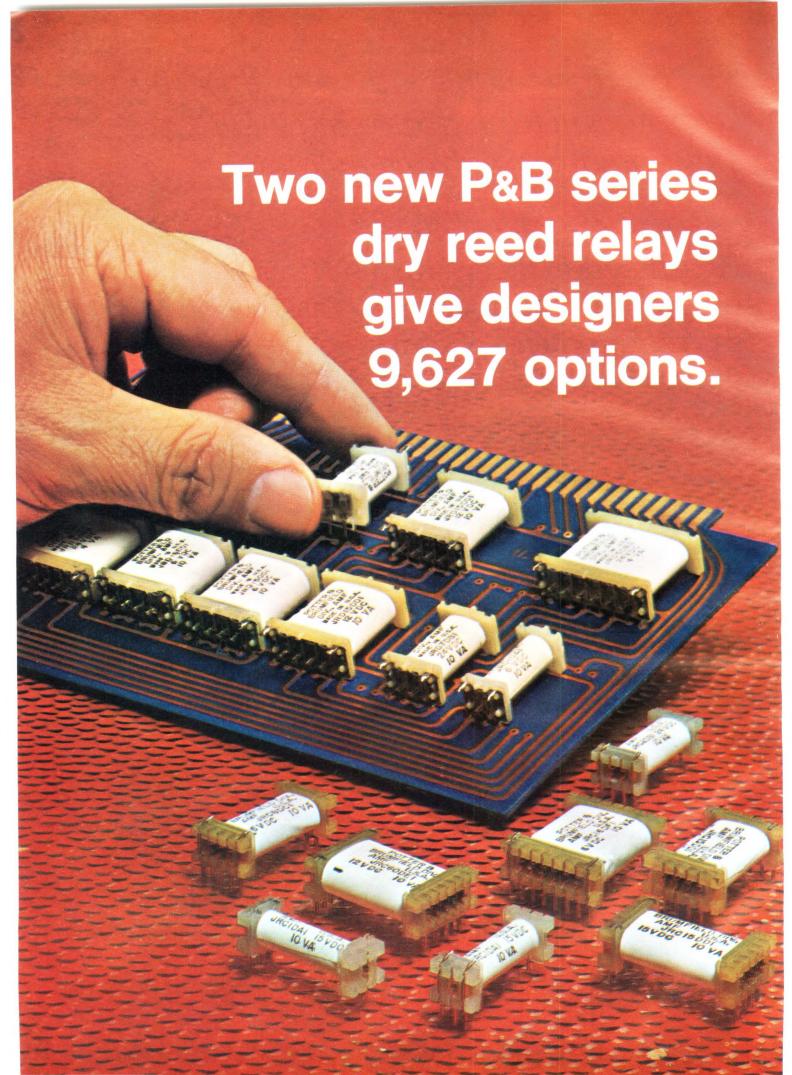
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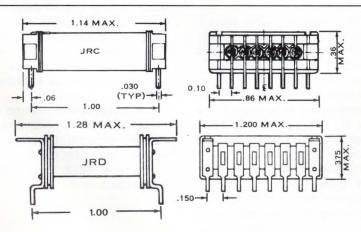
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The key to the 1310A's outstanding performance is its unique, advanced cathode ray tube which uses electrostatic deflection to control its electron beam.

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Yet, despite all these advantages,

the 1310A costs only \$3000 - far less than competitive displays (covers and stand, \$100 extra). Or, for \$2875, you can get all the features of the 1310A, in the new 14-inchdiagonal 1311A. OEM price schedules are available on both the 1310A and 1311A.

For further information on both of these new displays, contact your local HP field engineer. Or write Hewlett-Packard, Palo Alto, California, 94304. In Europe: 1217 Meyrin-Geneva, Switzerland.



OSCILLOSCOPE SYSTEMS

#### **COMPUTER HARDWARE**

## Novel computer organization results in design for a maxi-mini

This mini design offers improved performance and is intended for dedicated real-time control systems where minimum program running time and high accuracy have top priority.

#### Robert C. Sanford

Minicomputers have been sprouting up like weeds, and each newly announced marvel claims to be "new," "improved" and best for all users. Why then, with such a surfeit of goodies do we need another design for a mini?

Simply because, in spite of all the claims for new organizations, new bus structures, modularity, and so on, computers today are really no different from Von Neumann's concept of 25 years ago. Faster? Smaller? Cheaper? Certainly! But they still use the same organizational concept. Von Neumann set forth five separate, autonomous units: input, output, memory, arithmetic, and control. Take a look at the block diagram of any mini and all five are still there (**Fig. 1**).

It's true that a lot of registers and counters appear that don't fit these designations. But each one can be considered as part of arithmetic or control, and may be lumped into these units. Often, both arithmetic and control are further lumped together as the "processor", but they're still there. Input and output may be treated separately or together in an I/O section, but they're also there. And that, of course, leaves memory. This is always an autonomous unit, and most mini-computer specs are concerned primarily with memory characteristics, often the only claim to fame.

#### How is this design different?

This design breaks with tradition by considering the arithmetic logic unit (ALU) and control as the only truly autonomous units. All other elements are treated simply as registers subservient to the ALU. With very few exceptions, all operations are transfers between registers through the ALU so that arithmetic or logic can be performed during each transfer. The only concession to memory here is that transfer takes a little longer.

The design also breaks with several minicomputer conventions. Most minis are designed with low cost as the

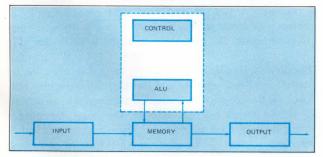


Fig. 1 – Von Neumann organization on which all minis are based. Dotted area is sometimes called the processor. Note that memory is the central function through which all paths flow.

chief objective, with performance secondary.

This design is aimed at performance, with cost secondary. It is intended for dedicated real-time systems where program time is a limiting factor. Many systems simply don't have sufficient program time for software executives or real-time operating systems. They need a mini that can do a maxi job.

Speed in itself is not enough. This design uses a 1  $\mu$ sec memory—faster than some but slower than others. The secret to high performance is fewer instructions per program, less core needed per program, true direct addressing of all memory, diversified self-explanatory instructions, partial overlapping of instructions, simplified software and integral hardware arithmetic, DMA and DMC.

The first break with convention is the word length — 24 bits instead of 16. This length was selected to provide reasonable accuracy of single-precision arithmetic to seven decimal digits, which cannot be done with only 16 bits. Next, 24 bits is also a multiple of eight, so it holds three ASCII characters instead of two, and it is multiple of six for non-ASCII characters. Each word can handle two 12-bit A/Ds or D/As at once, and this takes care of most system needs. If the encoder uses 15 bits, as some do, it requires one word, but the other bits are available for discrete operations in the same word. Shaft encoders of 19-21 bits can be handled by a single word.

#### What addressing means will be used?

Conventional minis use addressing tricks—they're called addressing modes—to make up for the lack of addressing bits in a 16-bit word. Paging, indexing, and indirect, relative, and immediate (literal) addressing are techniques to move about in memory beyond the limits of the addressing field, which rarely exceeds nine bits or 512 words. A word of 24 bits provides 15 bits to directly address 32k words, with 9 bits still left over for the instruction, instead of the usual 4-6. This makes programming easier, saves instructions, saves memory, saves machine

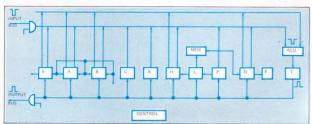
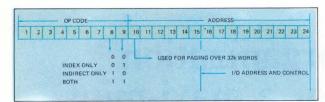


Fig. 2—Proposed organization make the ALU central to all operations, with all other functions treated as registers. Memory is subservient.



**Fig. 3—Word structure used in the new design.** Number of bits for I/O address is up to the designer.

time, and simplifies assembler and compiler by eliminating paging or its equivalents.

Paging (sectoring) uses one bit to locate the address field in a base page or the current page. Its chief use is in assembler software. Since it is not needed with 24 bits, it is not included here. However, the technique could be used if memory is required greater than 32k words.

Indexing, in addition to permitting movement in memory, is a powerful programming tool and is available in this design for every address, whether direct or indirect. Also included is multi-level indirect addressing, even though it requires an extra memory cycle for each level. Each level requires an extra word of memory and an extra instruction to fill that word, but it is so valuable a programming tool in providing pointers, that it is desirable.

Relative addressing is usually a software function to permit easier programming. An instruction can be moved forward or backward from the current instruction address within the limits of a small address field. Some minis have included relative addressing as a hardware function, but it gives little advantage and is not specifically included here, even though the capability is inherent in the design.

Immediate or literal addressing has been ballyhooed quite a bit. It is chiefly used in minis with short word lengths. Each instruction uses two words—some call them bytes to makes it sound better, but they're words just the same—the second word being the address. Twice as many words of memory are required but this only helps to sell more memory to make the system useful. Therefore, immediate addressing is not included in the proposed design.

#### Memory is subservient in the new architecture

**Fig. 2** is a block diagram of the proposed design. Now look at the diagram of the mini of your choice. In the conventional mini, the ALU is the heart of operations. It is fed on one side by memory and on the other side by various registers. I/O may or may not feed through the ALU. The ALU output always feeds an accumulator and usually one

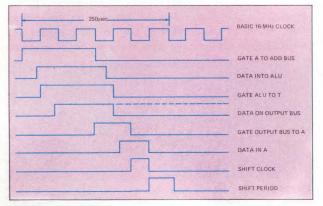


Fig. 4—Timing cycle for add and shift in multiply instruction.

or more other registers. I/O almost invariably inputs to a register, sometimes through the ALU, and output to the I/O is from a register, often without any gating.

In **Fig. 2**, the ALU is also the heart of operations since only here can any "computing" be done. Now, however, the ALU doesn't have a "memory" side and a "register" side as inputs; all registers can feed either side of the ALU. Thus, arithmetic or logic can occur on every transfer through it. Since memory and I/O are treated as registers, the statement applies to them also. Output from the ALU is buffered in temporary register T and then fed to all registers. Register T holds each result long enough for output to I/O, which looks just like any other register.

Function register F is an exception to the rule because it merely holds the instruction during execution and is not a part of computation. A few other registers feed only one side of the ALU, but this is not a limitation of the concept. It is simply the result of the author's choice of certain functions as being unnecessary.

#### TABLE I

#### **REGISTER DESIGNATIONS**

- A SINGLE-PRECISION ACCUMULATOR
- B FREE REGISTER OR SECOND HALF OF DOUBLE-PRECISION ACCUMULATOR
- C SHIFT COUNTER (DOWN)
- D REGISTERS A AND B TOGETHER
- E SINGLE OVERFLOW BIT
- F FUNCTION OR INSTRUCTION REGISTER
- H 16-WORD MSI MEMORY
- L LOCATION OR MEMORY ADDRESS
- M IN-OUT REGISTER FOR CORE MEMORY
- P PROGRAM COUNTER (UP-DOWN)
- T TEMPORARY STORAGE FOR ANSWER
- X INDEX COUNTER (UP)

#### How do the registers function?

Now for the registers. Since there is no standard whatever for designating computer registers, we can call them what we wish. Designations are selected to indicate the register's purpose, yet not confuse the instruction scheme. **Table I** lists the registers and their functions. Jam-transfer is preferable to reset-set operation and is included in all but the MSI counters, since it eliminates the reset clock time. The counters do require resetting, but since they count to zero in most operations, this requirement is not serious. Jam-transfer can be implemented if the counters are constructed of flip-flops and gates instead of MSI logic.

Registers A, B, C, P, and X are not the usual simple registers. Conventionally, a counter is simply a register that is incremented by passing its contents through the ALU while adding one. Registers (counters) C, P, and X are really counters, available in MSI from several sources. Registers A and B are separate and can be used separately but, because they provide an extended accumulator are actually right-left shift registers as well. The particular register capabilities desired are not normally available in MSI shift registers, so they can be made of dual flip-flops and gates. Conventional shifting schemes require almost as many gates, so there is little difference in cost. Shifting speed is limited only by the hardware, and not by the organization.

	TABLE II	
FIRST LETTER	MIDDLE LETTER	LAST LETTER
A	T (Transferred to)	Α
В	I (Inverted to)	В
С	S (Swapped or interchanged)	С
D	P (Plus)	D
E	`L (Less)	E
H (Needs address)	T (C) (Two's complement)	H (Needs address)
I (Input)	A (And)	M (Needs address)
J (Jump)	O (Or)	O (Output)
L (Left shift)	X (Exclusive OR)	P
M (Needs address)	A (Arithmetic shift)	S (Sign)
P	L (Logical shift)	U (Unity or one)
R (Right shift)	R (Rotational shift)	Z (Zero)
S (Sign)	A	M (Minus)
T (Test)	В	N (Not set)
T(C) (Two's complement)	L (A LSB)	S (Set)
U (Unity or one)	M (A MSB)	
Z (Zero)	N (None)	
	W (When any)	

Each of the three counters is different in that C counts down, X counts up, and program-counter P counts up or down. Counter C stores the number of shifts in shift instructions. With an up-counter, the number has to be inverted before entry into the counter. Although the inversion could be done in the "load C" instruction, it is easier for the programmer not to have to invert, but simply load the number directly. Counter X is a conventional index register except that it counts up directly instead of adding one to its contents. This permits conventional programming use of the index register in the assembler. The program normally counts up, but the down-count capability is used in double-precision instructions. Assembler pseudoinstructions – or regular instructions, for that matter – can be made to pulse the counter for relative addressing over a few addresses, either forward or backward.

Register E is a single flip-flop to handle overflow. It is bused to both sides of bit 1 of the ALU for addition to registers. When machine status is stored during interrupts, the bit is stored along with register C as a word in temporary memory.

Finally, we have register H. This is actually more than a register, for it is a 16-bit MSI memory. Some of the locations are dedicated for storage during interrupts and DMA, so not all 16 bits are available for scratch-pad storage. However, the 8 or 9 words that are left should be adequate for the types of scratch-pad use to be expected in a mini. Register H is not intended as a semiconductor memory, but as a simple scratch pad.

#### Memory requirements are flexible

Read-only memory (ROM) is not included because this would normally be an option dependent on the system requirements. ROM can certainly be included—treated as another register—if it is desired. An example might be permanent storage of a sine-cosine table, useful in control systems. Remember that regular memory addresses must be reduced by the amount of ROM. Perhaps the best ar-

rangement would be 16k of regular memory and up to 16k of ROM; the choice of memory would be selected by the bit not used for 32k words.

Most MSI is rated in the 15 MHz range or higher, but, in practice, cannot be used at such rates in a complete system because of the delays through several devices. The proposed clock rate is 16 MHz, but only to permit staggered clock pulses at a machine rate of 4 MHz. Thus, any machine operation not involving memory or I/O occurs within 250 nsec. It is possible to perform shift instructions at twice this rate (8 MHz), because registers A and B can be shifted directly without requiring any transfers.

Using conventional circuitry and techniques, generic instructions can be performed within one memory cycle (fetch-fetch). Since this design permits any normal operation in 250 nsec, a core or other memory with that cycletime could be used. The immediate feeling is that a SC memory is just what the doctor ordered to gain speed. However, dedicated systems often require that the program be instantly available at all times and there is no time to read in a program each time the computer is used.

The author visualizes a core memory with a cycle time of one  $\mu$ sec. Once core is selected as the medium, it is ridiculous to pay the cost penalty for a few extra nsec. Any number of memories are available off-the-shelf that meet the requirement. An additional reason for the choice of 1 MHz is that the clock can be easily counted to provide milliseconds or other decimal time values for a real-time clock and for synch in the external system.

#### Simple programming is the key to speed

A 1 MHz memory-cycle rate offers little or no speed advantage over most minis in normal operations. However, complex instructions such as double add or subtract do provide speed advantages because they can be performed in the same time as their single-precision counterparts, and without setting the machine into a "double-precision" mode.

			TABL	E III		
BASIC ME	MORY FUNCTIONS		TRANSFER F	UNCTIONS		I/O FUNCTIONS
LOAD	STORE	ATB	BTA	CTA	HTA	ITA 1-3
MTA	ATM	ATC	BTC	СТВ	HTB	ITB 1-3
MTB	BTM	ATH	BTH	CTH	HTC	ITM
MTC	CTM	ATP	BTP	ETS	HTP	ATO 1-3
MTD	DTM	ATX	BTX	EIS	HTX	BTO 1-3
MTH	HTM	AIA	BIA	MIM	HIA	MTO
MTP	PTM	AIB	BIB	STE	HIB	
MTX	UTM	AIC	BIC	SIE	HIC	
MIA	XTM	AIH	BIH	SIS		
MIB	AIM	ASB	BSM			
MIC	BIM	ASM				
MID	HIM					
MIĦ						
SET-RESET FUNCTIONS		LOGIC FUNCTIONS			SHIFT FUNCTIONS	
UTA	ZTA		AAB	BA	Н	NMZ (Normalize)
UTB	ZTB		AAH	BA	AM	LLS
UTC	ZTC		AAM	BC	H	LLD
UTD	ZTD		AOB	BC	M	RLS
UTE	ZTE		AOH	B>	(H	RLD
UTH	ZTH		AOM	В	(M	LRS
UTP	ZTP		AXB	HA	AM	LRD
UTS	ZTS		AXH	H	MC	RRS
UTX	ZTX		AXM	H	KM	RRD
						LAS
						LAD
						RAS
						RAD

The real speed advantage is gained in programming. The instruction list provides so many functions that any program requires fewer instructions to do the job. Compare a short program from your favorite mini with this instruction list and see.

With few exceptions, the instructions specify a source, operation, and sink for the data. Letters selected for instructions are a compromise to avoid having a letter mean two different things, insofar as possible. The first and last letter of an instruction represent a register by its abbreviation or a quantity. Zero is the letter Z and decimal one is expressed as unity U to avoid using the letter O, which stands for output. The middle letter designates the operation to be performed during the instruction's execution. Table II lists the letters for each position in an instruction and Table III lists the instructions selected by the author. These are by no means the only possibilities, but are the ones deemed worth implementing.

Let's take some examples. A conventional mini might use LDA for "load A from memory" since memory is the usual source and is understood. Our instruction is MTA, which means, memory (source) transferred (T) to A (sink). It could just as easily have been MIA or memory inverted to A, which normally requires two instructions.

When arithmetic or logic is to be performed, two sources are required. In this type of instruction, the first letter is both a source and the sink. Thus, APM says that A is a source and will receive the answer, and that the operation is A plus M, which is equivalent to a conventional

ADD instruction. The symbols + and - could be used but they require shifting on an ASR, so P and L were selected; the L for less instead of M for minus to avoid confusion. The instruction could as easily have been MPA, where A is added to memory and restored to the same memory location. This also normally requires two or more instructions.

Since no register is designated D, this letter can be used in any position to indicate a double word (A and B registers). The only exception is the DIV (divide) instruction, which is self-explanatory. In the shift instructions, D means double word, or what is commonly called a "long" shift.

Special rules apply to shift and control instructions because they can be easily recognized. All shifts start with L (left) or R (right) as the first letter, which distinguishes them as shift instructions. The second letter is always L (logical), R (rotate), or A (arithmetic) to describe the shift, and the last letter is S (single) or D (double) to describe register size.

Multiply (MPY) and divide (DIV) don't fit the system, but are so obvious and so commonly used that they are retained here. To stay with the system, they could be written A\*M or A/M, but again, shifting is required on an ASR, and the author prefers to stick with letters.

Control instructions also present problems. Standard formats such as HLT (halt), NOP (no operation), INH (inhibit interrupt), ENB (enable interrupt), and CMP (compare) have been retained because they are both common and self-explanatory. The CMP instruction and I/O instructions need special mention. They are followed by a 1, 2, or 3, or by an understood 0. These numbers represent sin-

APB	BPA	HPA	MPA	DPM	TCA (Two's Complement
APE*	BPH	HPB	MPB	DLM	TCB
APH	BPM	HPM	MPD	MPY (Multiply)	TCD
APM	BPU*	HPU*	MPH	DIV (Divide)	TCM
APU*	BLA	HLA	MPU*		
ALB	BLH	HLB	MLA	XPU*	
ALE*	BLM	HLM	MLB	XLU*	
ALH	BLU*	HLU*	MLD		
ALM			MLH		
ALU*			MLU*		

gle types of comparisons where a complete comparison is not desired and time must be saved. The comparisons are: greater than, equal to, and less than, and it is understood that these are (A) compared to memory. If no digit follows CMP, the usual type of instruction is implemented and all three comparisons are made, with variable skips.

Much thought was given to whether skips or jumps should be implemented. A conditional jump saves an instruction over a conditional skip, but permits no other action except a jump. A skip permits any type of instruction to be inserted, but, except perhaps for halt, what other instruction is ever encountered in a normal program? So, conditional instructions are jumps, all starting with the letter J to distinguish them. The remaining letters are somewhat ambiguous in that they represent different meanings from normal instructions, but are acceptable because the letter J is so distinctive that no confusion should arise.

Input-output instructions are listed separately but are really only register transfers, the same as other instructions. Basic I/O instructions are followed by 1, 2, or 3 if partial words are to be handled, or by an understood zero if a complete 24-bit word is to be handled. This permits byte commands to or from the A or B register, which is particularly useful in writing assembler software. A separate external assembly register can be added to collect and distribute 24-bit words as an I/O controller function if desired, in which case the byte function could be eliminated or used to control the external register instead of A or B.

Only two classes of instructions begin with the letter T; the T register is not externally available and signifies test, or when followed by C signifies two's complement. Set-up for I/O instructions is by IOP (input-output pulse). Here again the meaning is obvious and the usage is common.

To implement these or other instructions the designer might prefer, nine bits of the 24-bit word are used as the instruction field. This provides 512 possible combinations, but all are not used. Two bits are used to indicate indexing and indirect addressing as is common. These are only required for memory-reference instructions and are therefore available for use in the CMP and I/O instructions to determine the 0, 1, 2, or 3. For simplicity, they are the last two instruction bits, 8 and 9, and numerical representations of an instruction are read from the earlier bits (**Fig. 3**).

A memory-reference instruction might be, for example, 000,111,100 (octal 074). Indexing, indirect, or both, would be indicated by simply adding 1, 2, or 3 octal to the number. An octal number would thus be as easy to read and understand as the binary version. A special case

is CMP, which is a memory-reference instruction. Here the 1, 2, or 3 would be interpreted as the type of comparison, and no indexing or indirect would be allowed. A particular designer might prefer to eliminate this condition in favor of comparison through an indirect or indexed word.

No attempt whatever is made to correlate instruction letters with octal digits, tempting though it might be. There simply are not enough possible combinations. Memory-reference instructions are limited to a maximum of 64, each with four possible combinations of indexing, and/or indirect addressing. This uses eight of the nine available instruction bits, and totals 256 combinations. The remaining bit (bit 1) provides an additional 256 non-memory instructions, which includes those presented plus room for many more, as desired. The restriction on ROM addresses previously mentioned might be alleviated by using some of the spare combinations to handle them. Thus, a code and address for memory could be duplicated for ROM if the extra bit is added. Register H is another case of a "non-memory" code that requires an address.

Bootstrap loading could be handled by a ROM using one of the spare codes. However, since loading is an extraneous function and is not part of computation or logic, it might more reasonably be handled by a ROM under control of a panel button instead of a code.

#### Only a few interrupts are really needed

And now we come to interrupts. Many minis brag about having the capability of many—even hundreds—of levels of priority interrupt, some through hardware and others through software. The question boils down to how many interrupts can a dedicated mini anticipate in a typical system? Very few, since nearly everything is under program control—or ought to be. An eight-level MSI priority network is available, capable of expansion, and this is recommended. Eight levels should be more than enough, even if one or two are dedicated to direct memory service.

Each interrupt creates an indirect jump through its dedicated memory address to a user supplied subroutine. Part of the function of register H is to provide high speed automatic storage of computer status and data during an interrupt. After recognition and before control is turned over to the dedicated location, a wired-in routine will successively store registers A, B, C (includes bit E), L, M, P, and X, in register H in dedicated locations. Because of the speed with this scheme, this should take under 2  $\mu$ sec. When the interrupt is concluded, the registers are reloaded automatically and the regular program goes merrily on.

	CONTROL FUNCTIONS	
CMP 1-3 (Compare)	JMP (Unconditional)	J1N (Switch 1 not set)
ENB (Enable Interrupt)	JSR (Jump-store or Subroutine)	J1S (Switch 1 set)
HLT (Halt)	JAM (A minus)	J2N (Same for all switches  —number up to designer
INH (Inhibit Interrupt)	JAN (A negative)	J2S
IOP (I/O set pulse)	JAZ (A zero)	J3N
NOP (No operation)	JBM (B minus)	J3S
TPI (Test Interrupt)	JBN (B negative)	JNS (No switches set)
TRL (Test ready line)	JBZ (B zero)	JWS (When any switch set
	JLN (A least significant not zero)	
	JLZ (A least significant zero)	
	JMN (A most significant not zero)	
	JMZ (A most significant zero)	

#### DMA and DMC are inherent

Since every register has a dedicated location in H, other possibilities present themselves. Conventional DMC is in some ways like an interrupt in that it waits until the current instruction is finished, and uses regular I/O lines and the regular memory data and address registers. Since it uses no other registers, no storage is needed, but address lines into the memory address register and additional gates are used. The DMC then contains the starting address and address counter, plus multiplexing facilities.

DMC in the proposed system requires no gates into the memory data register since direct I/O to memory transfer is a normal function, and no time is lost. Thus, conventional DMC could be included. But, suppose a DMC call caused registers P and C to be stored and the first two input words were an address and a count. These would be fed to P and C respectively, which would then take over the functions of the usual extra DMC hardware, and no changes would be made to the computer. The DMC would still control multiplexing, plus supplying counting pulses to the two counters.

Suppose that a DMA call causes registers C, L, M, and P to be stored, which takes only one  $\mu$ sec. Two additional locations in H contain a starting address and count, and these are fed to P and C as in DMC. DMA would then operate exactly the same as DMC with no changes being required, but now an instruction would be interrupted during transfer as in any DMA.

Dedicated systems sometimes require high-speed storage of one or two data words at random times, to be operated on in bulk later in the program. Normal DMA does not permit this because a dedicated counter will not release DMA until the count is complete. For such service, counter C could be left unstored and a separate counter in DMA would control the action.

Programmed transfer of bulk data could operate just like DMC except that the starting address and count would be stored in two memory words and called by the instruction in a form of immediate addressing. Another variation would be to leave the words in H as in DMA, and initiate operation with an instruction.

#### Timing cycle reduces execution time

Hardware multiply-divide is either included already or is purchased for nearly all dedicated minis, except for simple control systems. Hardware multiply-divide is inherent in the proposed design because all but a small amount of control logic is already there. Timing was selected specifically to permit an addition or subtraction, plus a shift, in a 250 nsec machine cycle, or  $4/\mu$ sec. Thus, simple forms of multiplication and addition take only 6  $\mu$ sec plus fetch time. A small amount of control hardware will permit shifting across zeros and ones, and even operation on two bits at a time to reduce the time needed per instruction. Further time gain can be achieved by shifting at 8 MHz.

Instructions such as normalize (NRM) and pseudo-instructions in the assembler can make good use of the spare storage in register H to provide further gains in speed. A little practice on the part of the programmer can do the same, using H for scratchpad storage of intermediate results in complex equations. It is quite possible that the wide variety of capabilities in the proposed design will permit easy hardware implementation of compiler functions such as queues, stacks, and field limits.  $\Box$ 

#### Author's biography

Robert C. Sanford has been a man of many talents during his 18 years of engineering for several leading electronics firms. He has had 14 years experience with digital systems, logic, analog equipment and circuit design plus 4 years of technical editing. Mr. Sanford has had numerous articles



published, has 3 patents and is a senior member of IEEE. He received his BSEE from the University of Missouri.

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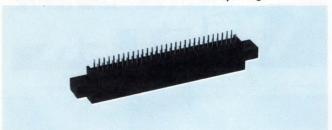
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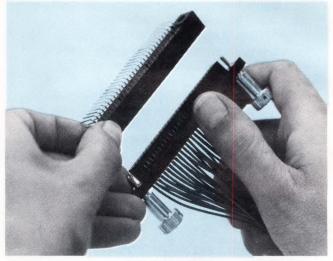


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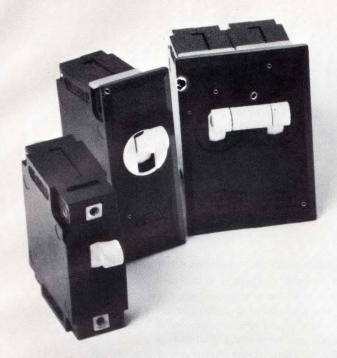
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## Marketing strategy shrinks a terminal in half

Paying attention to the users' needs can pay off in wide customer acceptance. Here's how a larger and faster terminal was reconfigured to look like the popular ASR33.

A. A. Kirscht, Western Union Data Services Co.

When the product planners of Western Union Data Services Co. determined that the company should market the GE TermiNet 300 Series, they imposed one essential condition for this marketing decision: the GE Automatic Send and Receive Model had to be reconfigured to reduce its size in half.

Not being a manufacturer, Data Services Co. (DSC) has followed a marketing strategy of "piggyback design" which involves choosing the best data communications product of a class and reconfiguring it to make it even more acceptable to end-users. For example, under an OEM agreement, GE has repackaged its ASR model to DSC's requirements and DSC is marketing this reconfigured model under its own label.

Why did DSC insist on reducing the ASR model to half its size? Primarily because of its experience in marketing Teletype Model 33s and 35s.

The Teletypes have long been one of the dominant computer terminals in use. However, terminal users have demonstrated a bias against the more reliable but larger Model 35. Even for applications for which the Model 35 was more suitable, users preferred the Model 33 (**Fig. 1**) for its compactness and portability, in addition to its price.

This obvious preference for a compact terminal on the part of users made us realize that if we wanted to be successful in marketing a terminal to those who would be upgrading from a 10 to 15 cps Model 33 to 30 cps terminal, we had to offer a terminal that looked very much like the Model 33 and sold for less than the GE model. After all, the Model 33 is the terminal to which users have been accustomed for some eight years or more.

Users of Model 33s had become accustomed to the compactness of the unit—it could even be found in the large crowded bullpen-type office. With the advent of the acoustic coupler which could be added to the unit, mobility was possible, thus making any telephone a pipeline to a computer. Users had added various forms of wheels and handcarts to the Model 33, so that the terminal could easily be moved from place to place. Terminal mobility permitted a pool of people to use fewer terminals.

It made good marketing sense to offer a terminal whose size conformed as close as possible to that of the Model 33. The problem was that the product deemed the best 30 cps terminal on the market came in a desk model that was twice the size of the Model 33. **Fig. 2** shows the original GE ASR desk model and the reconfigured DSC version.

To achieve the Model 33's compactness meant that the

TermiNet punch and reader unit had to be reconfigured since its original location in the desk drawer would be eliminated in the process of transforming the TermiNet's standard desk housing into a Model 33-like configuration—basically a terminal composed of a printing unit and a punch and reader unit mounted on a pedestal. It also meant that considerable equipment such as the logic, control and power for the paper-tape reader and punch had to be fitted into the limited space of a Model 33's pedestal, part of which was already occupied by the data set.

An additional demand for space in the terminal's pedes-

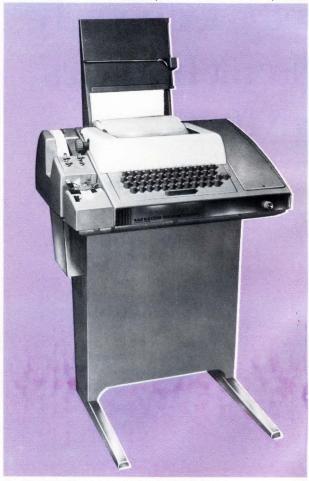


Fig. 1 – Data communications users have long been accustomed to the compactness of the Teletype Model 33 teletypewriter. It made good marketing sense to offer a terminal that looked very much like the Model 33.

tal grew out of an analysis of the paper handling capabilities of the keyboard send-and-receive unit in the TermiNet series. Part of the problem of handling six-part paper fanfold was that the electronic "bustle" for this basic unit protruded from the box through the printing mechanism and back to a form accumulating shelf.

It was decided that the paper-handling mechanism should be redesigned and that the bustle with its 20 circuit boards should also be incorporated into the pedestal so as to reduce the distance between the platen and the rear of the terminal. Compactness was obviously a marketing plus, but it also held out the opportunity for improved terminal operation. **Fig. 3** shows the paper-handling mechanism of the reconfigured DSC model with the supply loaded. The original desk-model bustle is also shown.

Of course, packing the electronics in the confined pedestal ran the risk of incurring heat reliability problems. Other factors that had to be considered were the sensitivity of components to electronic interference, and accessibility to the components for maintenance.

The first question to be decided was the location of the bustle with its 20 circuit boards. The most logical place for these sensitive circuit boards would have been the bottom of the pedestal. In this position, they would have been protected from the heat generated by the power supply.

However, the low-level signals in the cable between the housing for the circuit boards and the printer demanded minimum distance between these two elements. This requirement mandated that the housing for the circuit boards be located in the upper portion of the pedestal closest to the printer (**Fig. 4**). Of course, this left the heat problem to be resolved, since the power supply would be in the lower portion of the pedestal.

Space limitations in the pedestal required that the hous-

ing for the circuit boards be as small as possible. For this reason, the housing was designed as a basic skeleton in the form of a card cage. This design allowed space on either side of the circuit boards for positioning of the necessary connectors. The circuit card cage contained three connectors which had to be easily accessed for plugging in the line interface and punch and reader cables.

Of course, the entire circuit card cage had to be removable for maintenance purposes. This was achieved without modification of the cage itself or the printed circuit mother board into which the circuit cards were connected.

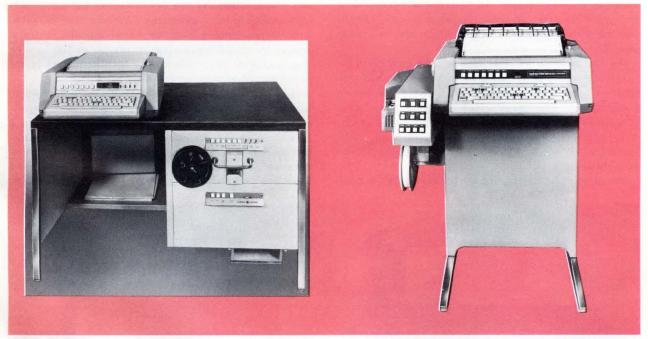
The circuit boards themselves had to be positioned in the card cage for easy accessibility and removal for maintenance purposes. This was accomplished by vertically positioning the boards.

Vertical positioning of the circuit boards was an important requirement for another reason—it minimized the effects of the heat generated by the power supply in the lower portion of the pedestal.

The next factor of major importance was the location of the power supply and the necessity of combatting its heat generation. Now since the transformer is the major heat generating element, it was mounted in the lowest practical position away from the circuit card cage to lessen the impact of its heat generation. Only a slight modification of the power supply unit was required.

The impact of the power supply's heat generation was further mitigated by installing a fan below the punch unit.

With the card cage and power supply appropriately located, the additional elements of punch board, reader board, modem control board and modem had to be mounted in the remaining space in the pedestal. To achieve easy accessibility to all components, the modém was attached to the support bracket of the circuit card by means of a clip. When servicing the equipment, a mainte-



**Fig. 2**—**The General Electric TermiNet 300** Automatic Send and Receive on the market today (left) is housed in a desk configuration with the punch located in the lower drawer, the reader in the upper drawer. It was from this configuration that Western Union Data Services Co.'s EDT 300 ASR evolved. The Western Union Data Dervices Co.'s EDT 300 ASR teleprinter (right) is half the size

of the GE desk model. This compactness was achieved by mounting the printing unit on a pedestal and storing the logic, control and power for the paper-tape reader and punch with the data set in the pedestal, and mounting the punch and reader modules on the left side of the pedestal. Note the striking similarities in appearances between the EDT 300 and Model 33 in Fig. 1.

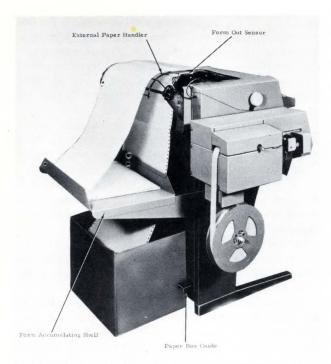


Fig. 3 — Part of the problem of handling six-part paper fanfold was that the electronic "bustle" of the original GE desk unit protruded from the back and blocked the normal path of the paper from the box through the printing mechanism, and back to a form accumulating shelf. Incorporating the bustle in the pedestal eliminated this problem.

nance man merely slips out the clip and the modem is easily removed to gain access to the three circuit boards behind it—the punch board, the reader board and the modem control board.

In a standard terminal configuration, ac power is required for three of the basic elements; namely, the printer, power supply, and modem. To have just one power cord emanating from the set, an ac power strip was mounted onto the power supply bracket into which each ac cord is plugged.

The next question to be decided was the location of the punch and reader unit. Operators of Model 33s had long been accustomed to having the punch and reader unit on the left side of the terminal, which was good reason alone to position the unit in that fashion. Furthermore, trial runs had shown that operators encountered a threading problem when the punch and reader unit was positioned on the right side.

More important, redesigning the positioning of the origi-

nal desk model's punch and reader units created the opportunity to further improve terminal operation. In the desk model, the punch was located in the lower drawer, the reader in the upper drawer. Positioning these units in closer proximity was important for two reasons:

First, this is the way these units are positioned on the Model 33, and operators were accustomed to this design.

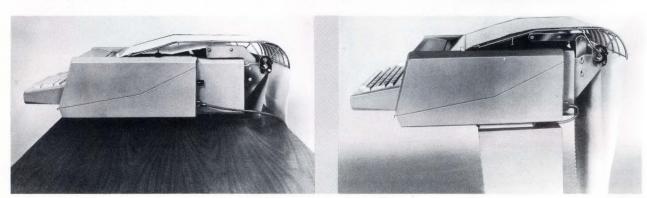
Second, in certain applications users benefit from the close proximity of these two units. Having the punch and reader in the same line permits the operator to more conveniently punch up tape at the same time the computer is polling her terminal and pulling off the data from the terminal's reader.

Also, some applications call for the use of a master tape for purposes of format control for filling in data as a form is created. The master tape is run through the reader to create a new tape on the punch as the operator inserts the data. Having the punch and reader in the same line permits the operator to handle this operation more easily.

It was one problem to orient the punch and reader module for operator convenience, but still another to make the electrical connection between this module and the remaining components in the set base. The wiring had to be run unobtrusively to the base of the pedestal where the connections are made. To achieve this, a cut-out was made on the side of the pedestal behind the punch and reader module. A plate was designed to provide a cylindrical surface to resist wire insulation abrasion. This plate could be reversed to plug up the access hole on the side of the pedestal and permit the use of the same pedestal for a KSR or ASR version.

One of the major shortcomings and complaints in using the Model 33 in a crowded office space for prolonged periods was the high level of noise. When we moved the punch and reader out of the desk and on to the side of the unit it was found that the noise level of the punch was high enough to be objectionable. We overcame this problem by providing 1/2 in. of sound-insulating material around the punch mechanism, as shown in **Fig. 5.** With this insulation, the ambient noise level produced by the punch was considered acceptable.

However, the effect of this sound insulation material was poor heat dissipation from the punch. Consequently, an exhaust fan (seen in Fig. 5) was added below the punch to accomplish two design objectives: first, to insure satisfactory punch operation over the specified temperature range and second, to create an air path within the pedestal to reduce heat build-up among electronic components.



**Fig. 4**—A **side view of the GE desk model** (left) is shown with its "bustle", the storage area for 20 circuit boards. A side view of the Western Union Data Services model is shown (right) with the bustle removed and stored in the pedestal.

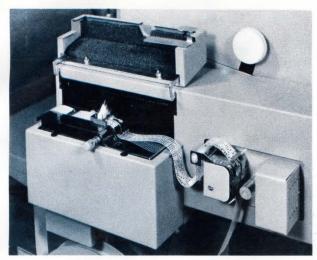


Fig. 5 — When the punch and reader were moved out of the desk drawers, the noise level of the punch was objectionable. This problem was overcome by providing 1/2 in. of sound-insulating material around the entire punch mechanism. The insulation in the upper part of the punch is visible in the photo.

This proved to be the effective solution for combatting the heat generated by the power supply.

The punch and reader housing was so designed that the exhaust fan used for cooling the punch mechanism created an air flow from the room ambient air into the base of the pedestal through the access hole between the pedestal and punch and reader into and out of the punch itself. Air circulation was further enhanced by liberally perforating the rear pedestal cover with louvers at the lower and uppermost areas to permit natural circulation in the pedestal.

An important redesign consideration involved operator controls on the control panel. The Model 33 controls for

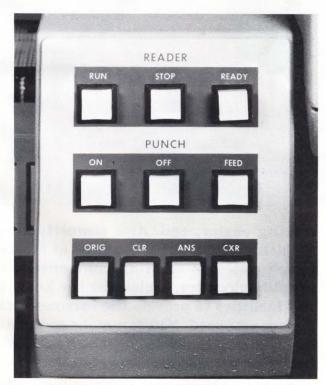


Fig. 6 – The control panel was simplified to three pushbuttons for the reader and three for the punch, versus the 14 on the original desk model.

the punch and reader mechanism are very straight forward, and even the uninitiated could quickly master the operation of the terminal for time-share purposes. The punch and reader controls on the desk-type automatic send/receive unit shown in Fig. 2 were numerous and located inconveniently for the operator. Again, marketing strategy dictated a design similar to the Model 33.

The controls were simplified (**Fig. 6**) to three pushbuttons for the reader and three for the punch, versus the 14 on the original model. The nomenclature was even changed to more meaningful terms which a Model 33 operator could understand. An additional row of pushbuttons are provided only for those applications which require the control of the data set in originating a call to the computer. Tests conducted using various people, secretaries, engineers, etc. have confirmed the ease of operation permitted by the redesign of these controls.

The control panel of the punch-reader module had to be easily removable so that it could be exchanged for other panels specifically tailored to customer requirements. A panel was designed to snap in place and the switch wiring terminated at a connector. An additional cable with connectors at both ends was arranged to be plugged into the connector control panel at one end and the associated electronics in the base of the pedestal at the other end. In this fashion, the exchange of a control panel could be easily accomplished.

Terminal mobility was emphasized earlier as being an important user requirement for a terminal that would appeal to the Model 33 market. Not only does mobility enable larger numbers of office personnel to share fewer terminals, but mobility also eases the installation of the equipment, making it possible for one man to handle the terminal. The printer of the redesigned TermiNet terminal was so oriented so that it could easily be attached to a handcart to achieve mobility.

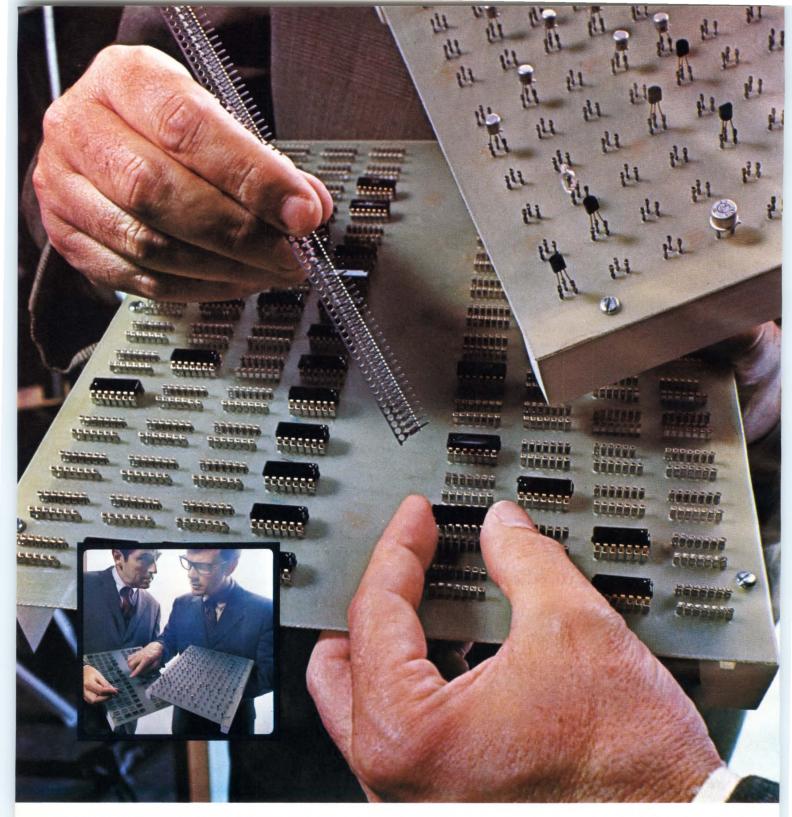
One final redesign touch involved the proper placement of the paper supply box which is used for fanfold paper. While basically a small detail, DSC's experience in working with Model 33 operators had indicated a need for a better means of lining up the paper supply box than the human eye. A paper box guide as seen in Fig. 3 at the base of the pedestal was a simple enough solution to eliminate the guesswork.

#### Author's biography

Arthur A. Kirscht has been Vice-President and Manager of engineering for Western Union Data Services Co. since April, 1971. In this position, he is responsible for all engineering functions in the company, including both applications engineering and new product development engineering. He



previously was Assistant Vice-President of engineering for Western Union Telegraph Co. Prior to joining Western Union, he held several management engineering positions with the General Electric Co. Art received his BSME in 1950 from Oregon State University.



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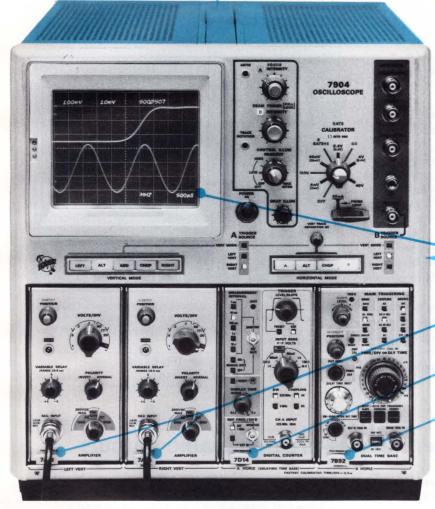
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### EDN DESIGN AWARDS

#### One transistor provides ECL to LED interface

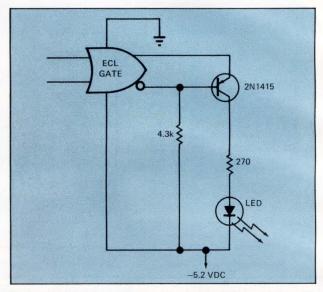
George A. Altemose, General Instrument Corp., Hicksville, N.Y.

This circuit utilizes a germanium PNP transitor to drive an LED. Only the normal ECL-5.2V dc power supply is required.

Operation of the circuit is as follows: when A' is high, A' = 0.7V and A = -1.5V. The transistor base is reverse biased, and the LED is off. When A is high, A = -0.7V, and the base is forward biased. The base current is limited by the 4.3k resistor to about 1 mA. The transitor saturates and the LED turns on. The transistor is germanium in order to insure saturation. Some types of ECL, such as Motorola's MECL II, have internal output pulldown resistors; in these cases, the 4.3k resistor is not required.

This circuit is particularly advantageous in systems consisting exclusively of ECL logic, where the addition of an ECL to saturated logic level translator would require the addition of a +5V dc power supply.

In addition to single LED's, seven-segment or other arrays can also be driven. These arrays must have the common-cathode configuration such as the Fairchild FND10, or the Monsanto MAN3. Another application is optoelectronic coupling, using a device such as Motorola's new MOC 1000 module.

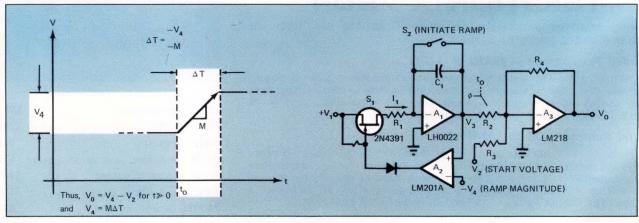


**Germanium PNP transistor** provides direct interface of LEDs and ECL logic systems without a second power supply. This system can be expanded to drive common-cathode LED arrays such as the MAN3 or FND10.

To Vote For This Circuit Check 150

#### Wide-range ramp generator has programmable outputs

Charles F. Wojslaw and Warren A. Buschmann, National Semiconductor, Santa Clara, Calif. This generator, although implemented with only three op amps, offers the flexibility of programmable start and stop voltages and slope, with a wide range for each control.



Voltages V<sub>2</sub> and V<sub>4</sub> control the outputs of this wide-range ramp generator.

In the circuit, op amp  $A_3$  functions as a summing amplifier,  $A_1$  as an integrator and  $A_2$  as a stop-limit comparator for the JFET switch  $S_1$ . Amplifier  $A_2$ , through switch  $S_1$ , regulates the generator output at the stop voltage set by  $V_4$ .

The generator output voltage,  $V_o$ , is the sum of the integrator output voltage,  $V_a$ , and the initial or start voltage,  $V_o$ 

$$V_{o} = -\left[\frac{R_{4}}{R_{2}}V_{3} + \frac{R_{4}}{R_{3}}V_{2}\right],$$

where 
$$\begin{array}{ll} V_3=\frac{I_1}{C_1}\,\Delta T=-\frac{V_1}{R_1C_1}\,\Delta T=-M\Delta T\,. \\ If & R_2=R_3=R_4 \end{array}$$

then  $V_0 = M\Delta T - V_2$ .

The ramp period,  $\triangle T$ , is a function of the ramp magnitude,

V<sub>4</sub> and the ramp's slope, M.

For a high-voltage ramp generator, only  $A_3$  is required to be a high-voltage amplifier. Resistors  $R_2$ ,  $R_3$  and  $R_4$  can be used to scale the lower voltages of  $V_2$  and  $V_3$ . The only limitation for the start and stop voltages is the max. voltage limitation of  $A_3$ . With the proper selection of  $V_1$ ,  $R_1$  and  $C_1$ , the range of slope value can be set from  $10^{-3}$  to  $10^6 V$  per second. Polarity may be controlled through the signs of  $V_1$ ,  $V_2$ ,  $V_4$  and the inputs of  $A_2$ . Controls  $V_1$ ,  $V_2$ , and  $S_2$  may be externally or computer controlled.

Applications for the generator include timing and sweep circuits as well as use as a function generator.

To Vote For This Circuit Check 151

#### "Rules of thumb" avoid production problems

**Stuart J. Lipoff,** Ft. Lauderdale, Fla.

The most commonly used circuit in any radio-frequency design is the L-C resonant circuit. In spite of this, many engineers often neglect some basic considerations during the design of such circuits. This can lead to problems on the production line. As an aid to preventing such problems two easily remembered "rule of thumb equations" will be presented. By their simple application in your next design, you can insure that your L-C circuit will tune the complete range of interest.

The two considerations necessary to insure that an L-C circuit will tune over a specified frequency range are the effects of both inductor and capacitor tolerance, and the tuning ratio (maximum to minimum) of the variable coil or capacitor.

First, the effect of the component tolerance will be considered. Let T be the specified tolerance on the inductor or the capacitor. Then, Equation (1) through (4) follow direct-

(1)  $\omega = \frac{1}{\sqrt{LC}}$ (2)  $\Delta \omega = \frac{1}{\sqrt{LC}} - \frac{1}{\sqrt{LC(1+T)}}$ (3)  $\frac{\Delta \omega}{\Delta} = 1 - \frac{1}{\sqrt{1+T}} = 1 = -\sqrt{1-T+T^2-T^3+\cdots}$ (4)  $\frac{\Delta \omega}{\omega} = 1 - \sqrt{1-T}$  for T < < 1(5)  $(a + b)^{\alpha} = a^{\alpha} + a^{\alpha-1}b + 1/2 \alpha(\alpha - 1) a^{\alpha-2}b^2 + \cdots$ (6)  $\frac{\Delta \omega}{\omega} \approx 1/2 \text{ T for } T < < 1$ where:  $\omega = \text{resonant frequency}$ T = component tolerance

Box 1. Equations for effect of component tolerance

ly. Equation (5) is the statement of the binomial theorem in non-integer form. Neglecting the higher-order terms in both Equations (3) and (5) and substituting Equation (5) into Equation (4), Equation (6) results.

Equation (6) states that the tolerance on the resonant frequency due to the part tolerance, T, will be  $1/2 \times T$ , for the usual case of T much less than one.

Example:

Given: A simple L-C resonant circuit with the capacitor having nominal value of 15 pF and tolerance of 10%. If the nominal resonant frequency is to be 150 MHz, over what range will the actual resonant frequency vary?

Answer: The frequency will vary 5% of 150 MHz, or about 143 to 158 MHz. Therefore, the circuit must be able to either tune this range or be broadband enough to insure resonance on the production line.

The agreement of this simple formula, for the above example, was checked against the calculated exact variation in resonant frequency by solving Equation (2). The exact variation due to a 10% tolerance on the capacitor is a frequency of 4.65% low and 5.41% high about 150

(7) 
$$\omega_1 = \frac{1}{\sqrt{L_1 C_1}}$$

(8)  $\omega_2 = \frac{1}{\sqrt{L_2 C_2}}$ 

(9)  $L_1 = \frac{1}{\omega_1^2 C}$  or  $C_1 = \frac{1}{\omega_1^2 L}$ 

(10)  $L_2 = \frac{1}{\omega_2^2 C}$  or  $C_2 = \frac{1}{\omega_2^2 L}$ 

(11)  $\frac{C_1}{C_2} = \frac{L_1}{L_2} = \left(\frac{\omega_2}{\omega_1}\right)^2 = \frac{f_2^2}{f_1}$ 

where:  $L_1, C_1 = \text{maximum component values}$ 
 $L_2, C_2 = \text{minimum component values}$ 
 $\omega_1 = \text{low end of tuning range}$ 
 $\omega_2 = \text{high end of tuning range}$ 

Box 2. Equations for tuning ratio

MHz. This shows agreement to the approximation of 5%.

The next consideration for circuits that must tune over a specified range is the required maximum to minimum tuning ratio of the variable component. Let  $\omega_1$  and  $\omega_2$  be the low and high side, respectively, of the tuning range. Note that the choice for  $\omega_1$  and  $\omega_2$  should be the necessary tuning range extended by  $1/2 \times$  the sum of the capacitor and inductor tolerances. Therefore, in Equation (7),  $L_1$  or  $C_1$  represent the maximum value of the part, and  $L_2$  or  $C_2$  represent the minimum value in Equation (8).

Solving for the values of the component extremes, Equations (9) and (10) result. Finally dividing Equation (9) by Equation (10), Equation (11) results. The simple result is that the tuning ratio of either the variable L or C must be the square of the necessary frequency ratio.

#### Example:

Given a simple L-C resonant circuit with the capacitor fixed and equal to 15 pF with 5% tolerance. It is desired to tune over the range 150 MHz to 175 MHz by

using a variable inductor with a 5% tolerance. What tuning range is necessary for this coil to insure resonance?

Answer: Since there is a 5% tolerance on both the coil and the capacitor, the necessary tuning range must be extended by  $1/2 \times (T_L + T_C)$ , or 5%. Therefore, it is necessary to tune from 142.5 to 183.75 MHz using nominal parts, to insure resonance with parts at the worst-case tolerance extremes. The tuning range necessary on the coil is therefore the square of the frequency ratio (183.75/142.5), or 1.66. So the coil must have a ratio of minimum to maximum of 1.66. Calculating L<sub>1</sub> from Equation (9) the result is an L<sub>1</sub> of 0.075  $\mu$ H. Thus, L<sub>2</sub> must be 0.075/1.66, or 0.045  $\mu$ H.

To Vote For This Circuit Check 152

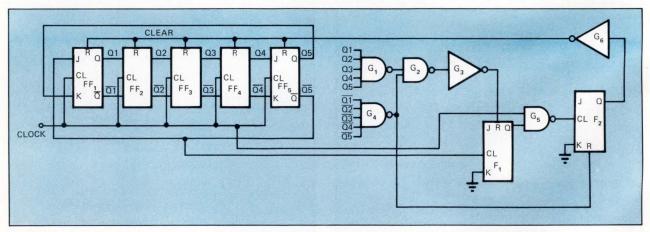
The reverse-ring counter version of the Johnson counter is very useful because of its simplicity and ease in decoding output counts. For a ten-count configuration the decoded outputs are determined by the state/decode scheme shown in **Table 1.** 

Difficulty arises when a bit drops out or is added or noise disturbs the counter contents leaving the counter unable to correct itself. Self correction can be performed by the logic circuitry shown in the schematic.

Assume that at power turn-on, the Johnson counter flip-flops come on scrambled or while circulating, its counting sequence is disturbed. Gates  $G_1$  thru  $G_3$  and flip-flop  $FF_1$  check for proper conditions of the flip-flops of the counter at count 5 or when Q5 goes low. All flip-flops should be at logic ONE. If the counter is not all Ones by the time Q5 changes from Logic 1 to Logic 0 and the counter clock goes high again, flip-flop  $F_2$  is set by Gate  $G_5$  and Gate

Count	Q5	Q4	Q3	Q2	Q1	Output Decode
0	0	0	0	0	0	<u>Q1</u> <u>Q5</u>
1	0	0	0	0	1	$Q1 \overline{Q2}$
2	0	0	0	1	1	Q2 Q3
3	0	0	1	1	1	Q3 Q4
4	0	1	1	1	1	Q4 Q5
5	1	1	1	1	1	Q1 Q5
6	1	1	1	1	0	Q1 Q2
7	1	1	1	0	0	Q2 Q3
8	1	1	0	0	0	Q3 Q4
9	1	0	0	0	0	Q4 Q5

 $G_6$  in turn clears the counter. Gate  $G_4$  detects the reset counter condition for all Zeroes and clears  $F_1$  and  $F_2$  and the counter continues to count as required.  $\square$ 



**Bit loss or noise** in this Johnson counter is automatically corrected once each cycle with the additional logic shown in the lower half of the schematic.

To Vote For This Circuit Check 153

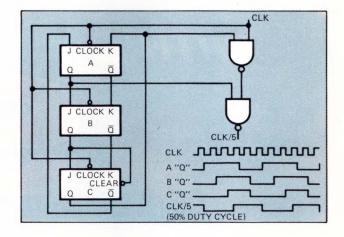
#### Another reader responds to odd modulo divider.

Christopher L. Maginniss RCA, Camden, N. J.

Dear Sir:

After glancing at the logic involved in the ÷ 5 network with 50/50 duty cycle in the Circuit Design Awards section of the July 1, 1972 issue of EDN, I felt certain that a simpler design could be found. Within two minutes, I convinced myself with the enclosed solution.

To Vote For This Circuit Check 154



#### Vertical sync separator has no integrating network

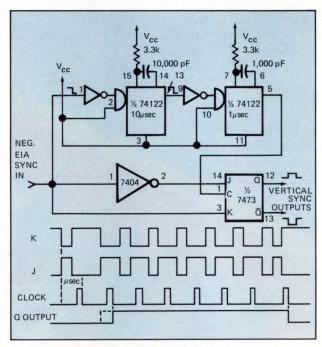
Walter G. Jung, Forest Hill, Md.

Standard approaches to separating the vertical synchronizing pulse interval in an EIA TV composite sync waveform involve an integrating network to remove the rapid horizontal rate changes and a level detector to sense the longer duration vertical rate pulses. This scheme by its very nature must contribute a delay due to the integration.

An interesting method to sense the vertical rate information digitally is shown in the figure. This system uses the controlled clocking sequence of a J-K flip-flop to detect the presence of the vertical sync interval.

Referring to the timing diagram, the flip-flop is fed complementary TV sync signals at its J and K inputs (waveforms J and K). It is clocked by a pulse delayed slightly longer than the horizontal sync interval (10  $\mu$ sec) and with a narrow width (1  $\mu$ sec). During the normal scan time, the clocking sequence of the J-K flip-flop reads the time interval of 11  $\mu$ sec after the leading edge as a LOW; thus, the first clock pulse after this change clocks the flip-flop Q output to a ONE. It remains at this level for six clock periods and reverts to the ZERO state again after the vertical sync interval has passed.

The system offers a much shorter delay time, as the leading edge error will only be slightly greater than the time required to "bracket" the horizontal pulse width.



The clocking sequence of the J-K flip-flop determines the presence of the vertical sync interval.

To Vote For This Circuit Check 155

#### **Rules & Announcements**

Your vote determines this issue's winner. All circuits published win a \$20 cash award. In addition, all issue winners receive a \$50 U.S. Savings Bond and become eligible for the annual \$1000 U.S. Savings Bond Grand Prize.

**Vote now**, by checking the appropriate number on the Information Retrieval card.

**Submit your own circuit, too.** Mail entries to Circuit Design Program Editor, EDN, 221 Columbus Ave., Boston, MA 02116.

#### Readers have voted:

Mark Trueblood winner of the July 15th Savings Bond Award. His winning circuit is "3 components make stable crystal oscillator". Mr. Trueblood is a graduate student at Wesleyan University in Middletown, Conn.

W.B. Crittenden and E.J. Owings Jr. winners of the August 1st Savings Bond Award. Their winning entry is "Zener-diode controls Wein-bridge oscillator." Mr. Crittenden and Mr. Owings are with Westinghouse Electric Corp., Baltimore, Md.



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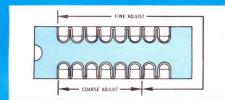






Figure 1

Figure 2

Figure 3

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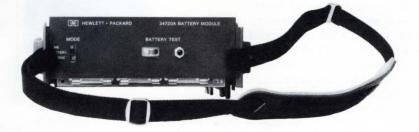
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DIGITAL VOLTMETERS

## Miniature power supplies offer higher reliability, increased output

PROGRESS IN MODULES

New miniaturized power supplies from Acopian Corp., Easton, Pa., operate with less stress on critical components while simultaneously providing greater output power. This has been accomplished by abandoning the customary approach of encapsulating all components into a thermally uniform block. Instead a thermal barrier is utilized to isolate the most sensitive portion of the regulator circuitry from the components which generate the heat.

Outputs up to 10.5W are provided by the  $3.5 \times 2.5 \times 1.25$  in. modules, which are designed for mounting directly on pc boards. Compared to previous models, they offer a 200% increase in output power from a 37% increase in volume. No derating is required through an ambient temperature range of -20 to  $+71^{\circ}$ C.

The component dissipating the most wattage—the series pass transistor—has been located at one end of the module. Next to it, in the central portion, is the other major source of heat, the stepdown transformer. The pc board occupies the other end. However, between it and the transformer is a plastic foam thermal barrier which blocks nearly all of the heat. "Touch testing" by EDN's editors proved, to our satisfaction, that the temperature gradient across the barrier is both sharp and significant.

The reduction in heat seen by the board improves circuit parameters such as temperature coefficient and eliminates the need for derating at high ambient temperatures. But more important is the improvement in reliability this portends. One only has to look at the life-vs.-temperture curves for filter capacitors (invariably the weakest link of a power supply) to see the significance of temperature reduction. They show that useful life is increased by a factor of ten to twenty

Modular power supply is intended for pc-board mounting. If the designer intends to use it at full rating he ought to be sure to mount the hot end away from any critical components on the board. See the cover of this issue for an idea of how the components are mounted inside the module.

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when operating temperature is decreased from +85°C to +25°C. Acopian doesn't claim that operating temperature is reduced to this degree, but does state that the capacitors in the new supplies are stressed significantly less than those in comparable competitive modules.

The capacitors are located as far away as practical from the heat shield. Reference diodes and all transistors except the output stages are mounted in an orderly row on the edge of the regulator pc board that butts up against the cool end of the case.

Acopian will employ this new design in all of its pc-mountable modules, single and dual output, which have an output of 5W or over. The initial offerings to utilize the new configuration are the Model 5E150, hav-

ing a 5V, 1.5A output (\$98), and the Model D15-35, with tracking  $\pm$ 15V outputs rated at 350 mA (\$105). Both operate on inputs of 105-125V ac, 47-420 Hz. Additional models are to be announced before year end.

Acopian plans to maintain its tradition of "all orders shipped within three days after receipt" with new modules. EDN was impressed, on a recent visit to the Acopian plant, to see how their orderly manufacturing techniques enable them to make each supply to order (none are stocked) and still ship in three days. The spokesman told EDN that "For over ten years now, we haven't failed to keep our promise." Comments from EDN readers also bear this out. Acopian Corp., P.O. Box 585, Easton, Pa., 18042. Phone (215)258-5441.

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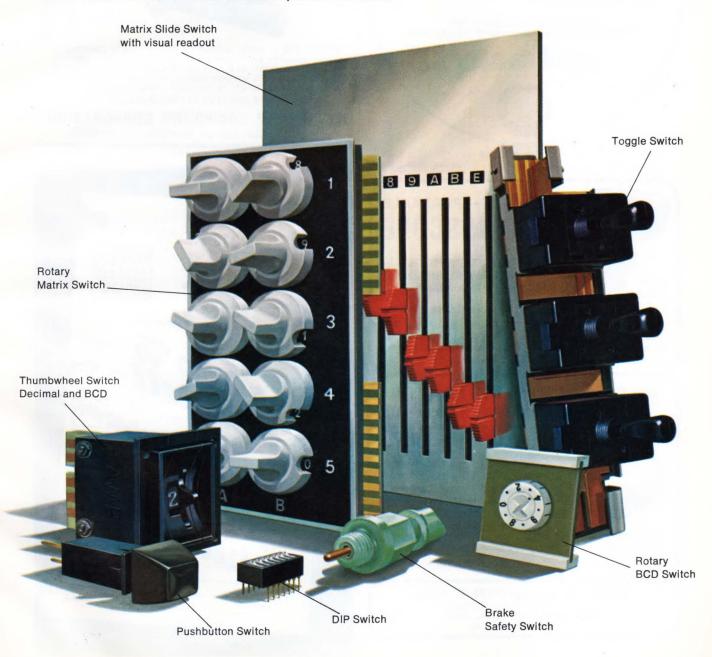
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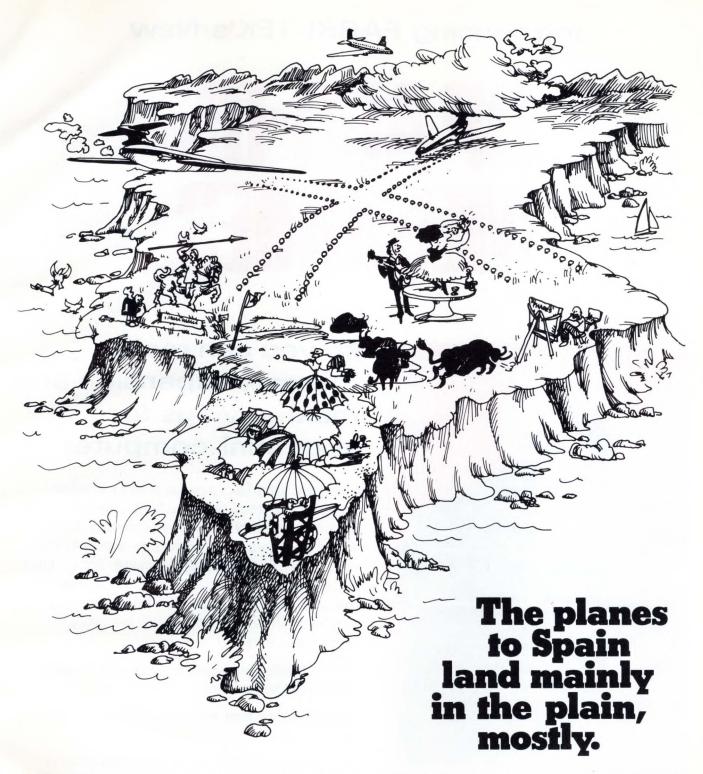
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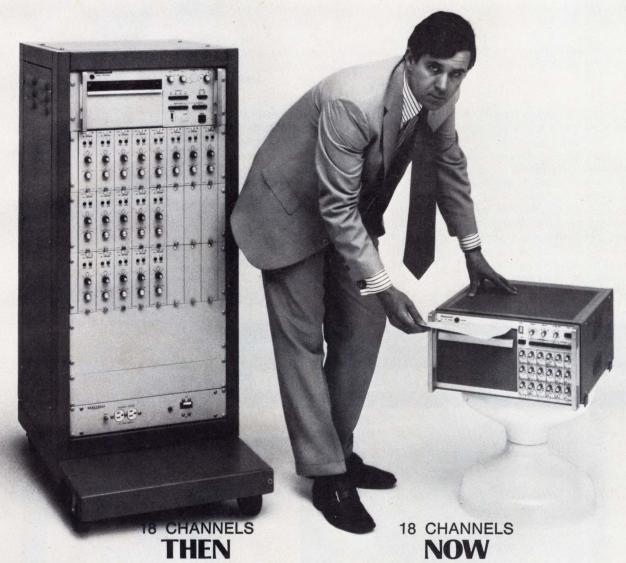
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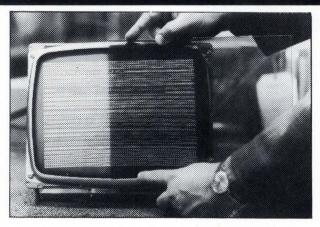
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from 110 Bands to 1200 Bands (120 cps) in
either half or full-duplex mode are available. \$2875. Omega Data Processing,
180 Valley Rd., Wayne, N J 07470. Phone
(201) 694-2329.

**BREADBOARD SIMPLIFIES INTERFACES FOR DEC COMPUTERS.** The Model 10-DE-77 board has double sided 36 contact connector fingers and accepts 18 fourteen-or sixteen-pin DIPs. It is etched in 2 oz-copper on flame retardant glass epoxy. Finish is 0.00002-in gold. All holes are plated-thru #62 drill (0.038). \$9. Douglas Electronics, 718 Marina Blvd., San Leandro, CA 94577. Phone (415) 326-2000. **186** 

TAPE TRANSPORT TAGS ONE PRICE FOR ALL SPEEDS. The D-600 tape transport is available with standard speeds of 25, 37.5, 45, and 75 ips, and packing densities of 556/800 bpi, 7 or 9-track, read-after-write configurations. \$3995. Capability for 7/9 track read-only operation may also be specified. An option at \$900 is 1600 cpi packing density. Per Data, 102 New South Rd., Hicksville, NY 11801. Phone(516)938-2851.

DIGITAL PRINTERS AVAILABLE AS SEP-ARATE COMPONENTS. DM-550 series medium speed 3 lps printers can print up to 21 columns. The print drum has 16 positions per column, and can print 50 different characters and numbers. All electronics on one pc board, power supply and the print mechanism can be supplied as separate components. It can also be supplied without the print mechanism to interface to a Seiko print unit. \$480. Keltron Corp., 225 Crescent St., Waltham, MA 02154. Phone (617) 894-0525.

**LQW POWER INCREMENTAL RECORDER FOR REMOTE DATA LOGGING.** Using a stepping motor drive, Model 201 cassette recording system provides true incremental recording at a density of 615 bpi, yielding 2.214 million bits of storage on one Phillips 300-ft cassette. The 201 uses CMOS logic for low power and high noise immunity. During recording it draws only 54 mA from the 12V supply. \$425. Memodyne Corp., 369 Elliot St., Newton Upper Falls, MA 02164. Phone (617) 527-6600. **189** 

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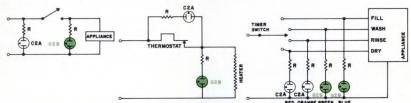


Finally, a broad spectrum bright green glow lamp from General Electric, that gives you greater design flexibility than ever before. It emits green and blue light with suitable color filters. It is called G2B.

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CHECK NO. 39

#### COMPUTER PRODUCTS



SINGLE MOTOR TAPE DRIVE ELIMINATES DISTORTION of data bits caused by unequal tension from spring loaded tensioning arms in reel-to-reel systems. Model 2021 cartridge tape drive uses the 3M DC300A data cartridge and features a fixed-position dual-gap read-while-write head, 800 to 1600 bpi recording on one, two, or four channels, and 30 ips read/write speed. Pricing ranges from \$200 for the mechanism to \$500 for the complete unit with electronics. Mohawk Data Sciences Corp., 781 Third Ave., King of Prussia, PA 19406. Phone (215) 337-1910. **190** 



DIGITAL PRINTER IS DESIGNED TO INTERFACE WITH MINIS. Model 722MMA is available in a numeric as well as a standard ASCII alphanumeric version. Throughput is 600 lpm with a line length of 22 characters or a throughput of 220 cps. Basic unit price is less than \$2000. Datadyne Corp., Bldg. 37A, Valley Forge Ctr., King of Prussia, PA 19406. Phone (215) 265-1793.

CALLED NUMBER RECORDER FEATURES AUTOMATIC SIGNAL PRINTOUT. The Model 250 universal telephone decoder with automatic printout of both Touch-Tone and rotary dial signals records date of call, off-hook time, on-hook time, and responds to \* and # keyboard symbols whenever these special functions are utilized. Printed indication of the presence of 2600 Hz tones is available optionally. \$1995. Voiceprint Laboratories Corp., P.O. Box 835, Somerville, N J 08876. Phone (201) 722-7391.

CRT DISPLAY CONTROLLER FOR PDP-11 USES ITS OWN MOS RAM. The Model 5300 CRT display controller displays up to

3200 upper case ASCII A/N symbols on any standard NTSC-compatible video monitor. Standard format is 40 lines of 80 characters each. Characters are formed as a 7 x 5 dot matrix in a 10 x 6 dot field. The 5300 features an internal 2k word x 16-bit MOS RAM which is accessible by both the PDP-11 UNIBUS and the display refresh logic. Technical Associates, 4521 W. Napoleon Ave., Metairie, LA 70001. Phone (504) 888-4884.

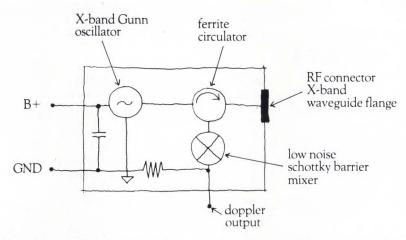


INFORMER UNIT DISPLAYS 32 CHARACTER MESSAGES. The 9700 Series of alphanumeric displays offers simple, reliable, instantaneous display capability for use in both data processing and process control applications. The display units have 16- or 32-character display capability, and can display the complete 64 standard ASCII character set. The 9700 system provides visual display of computer generated messages and is fully self-refreshing. \$684. Texas Digital Systems, Inc., P.O. Box 3701, Bryan, TX 77801. Phone (713) 822-5446.

MODEM/CHANNEL SIMULATOR CHECKS ERROR RECOVERY PERFORMANCE. The Validata 9150 is designed to inject random errors into both the transmitted and/or the received data in any synchronous data communication system. It injects a precise amount of random data errors into each data stream, thus simulating noisy data channels, allowing the error recovery performance of the system to be tested. \$1440. International Data Sciences, Inc., 100 Nashua St., Providence, RI 02904. Phone (401) 274-5100.

LARGE SCREEN COLOR DATA DISPLAY. Both alphanumeric and graphic data may be displayed on the TCR-25. RGB input circuitry makes for relatively simple interface with data systems. Users may choose between Hi-Lite matrix or controlled phosphor CRTs, depending on application and ambient light conditions. Other color monitor sizes include the TCR-14 14-inch, and TCR-19, 19-inch models. Miratel Div., Ball Brothers Research Corp., 1633 Terrace Dr., St. Paul, MN 55113. Phone (612) 926-2721.

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#### **CIRCUITS**

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220

BACKWARD-WAVE OSCILLATOR COVERS ENTIRE "B" BAND. The RWO 50 has an electronic tuning range of 33 to 50 GHz at a minimum power output of 10 mW. It is particularly suitable for millimeter-wave measurements, waveguide transmission systems, short-range millimeter radar systems, microwave spectroscopy and plasma research. The construction of the tube features an additional electrode gun. The RWO 50 is priced in the \$5000 range. Siemens Corp., 186 Wood Ave. So, Iselin, N J 08830. Phone (201) 494-1000.

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The low-cost SHA-5 features low tracking error of 0.1%, low drift of 20 uV/°C and low droop rate of 5 uV/ms. It is priced at \$32 in 100-unit quantities. The SHA-6 is designed for 16-bit A/D converters. It features a gain range of 1 to 1000 and stability versus time and temperature of  $\pm 0.0002\%$  (/month and /°C). The SHA-6 is priced at \$375, 1-9 units. Analog Devices, Rte. 1 Industrial Park, P.O. Box 280, Norwood, MA 02062. Phone (617) 329-4700.

50 TO 500W SERVO AMPLIFIER USES NEW CURRENT-LIMITING TECHNIQUE. The A5281 servo amplifier is used for machine-tool control, peripherals, and general industrial control. The low output impedance of  $0.01\Omega$  can easily be converted to thousands of  $\Omega$  with current feedback by a jumper connection. The compensation circuit makes stabilizing the servo loop a simple routine, while positive current limit protects alnico magnet motors. This 12A, 50V amplifier costs \$465. Westamp, 1542 15th St., Santa Monica, CA 90404. Phone (213) 393-0401.

**D/A CONVERTER FEATURES FAST OUT- PUT SETTLING TIME.** The 10-bit DAC-GI series has output settling time of 25 nsec

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224



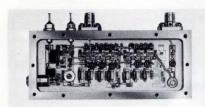
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225

HYBRID DECODER/DRIVER MINIMIZES DISPLAY COSTS. The 5V Series 20457 decoder/driver is designed to decode 8421 BCD data to 12 outputs, or, if only 10 decoded outputs are required, the two remaining may be converted to lamp buffers. Packaged in a 24-pin DIP, prices start at \$14.45 for the non-memory version (20488) and \$16.65 for the 20456 with memory. Industrial Electronic Engineers, Inc., 7720-40 Lemona Ave., Van Nuys, CA 91405. Phone (213) 787-0311.

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160-MHz HYBRID IC LOG AMPLIFIER FEATURES A 50-MHz BANDWIDTH. The thin-film "ICLT" Series offers a high IF frequency coupled with a wide bandwidth. The small size and low power drain makes them ideal for use in modern wideband manpack and airborne radars, ECM receivers and missile-guidance systems. Other features include 80-dB dynamic range and direct coupled video. Power requirements are 70 mA at 12V dc. RHG Electronics Laboratory, Inc., 94 Milbar Blvd., Farmingdale, NY 11735. Phone (516) 694-3100.

228

NUMA-LOGIC CONTROLS SIMPLIFY TROUBLESHOOTING. The Numa-Logic 300 Series solid-state controls use a simple English logic format and are available with a full range of input, output and logic function cards plus a variety of power supplies and rack configurations. A translucent plastic lens etched with pictorial symbols fits over LED indicators and allows monitoring of control signals coming into and leaving the panel. Westinghouse Electric Corp., Westinghouse Bldg., Pittsburgh, PA 15222. Phone (412) 391-2800.

HIGH-GAIN LOOP ANTENNA COLLAPSES FOR PORTABILITY. Loop antenna for magnetic field measurements in the range of 150 kHz to 32 MHz consisting of a coaxial cable supported on a mast can be quickly dismantled for storage or transportation. It offers up to 16 dB greater sensitivity than smaller antennas. Overall loop dimensions are  $52 \times 46 \times 5$  in. It may be used with any  $50\Omega$  input rfi meter or calibrated receiver. Singer Instrumentation, Los Angeles Operation, 3211 S. La Cienega Blvd., Los Angeles, CA 90016. Phone (213) 870-2761.

MULTIPLE-OUTPUT DC POWER SUPPLIES FOR COMPUTERS AND PERIPHERALS. The sixteen models housed in four basic case sizes are offered in dual or triple-output are available with voltage outputs of 5V, 6V, ±15V, 18V, 20V and 24V. Models 2K and 2L are dual output units with currents of 2.5A and 5A. Triple-output models 2R and 2S have currents to 5A and 8A. 100-piece prices are: 2K, \$37; 2L, \$65; 2R, \$69; and 2S/ \$119. Powertec, Inc., 9168 DeSoto Ave., Chatsworth, CA 91311. Phone (213) 882-0004.

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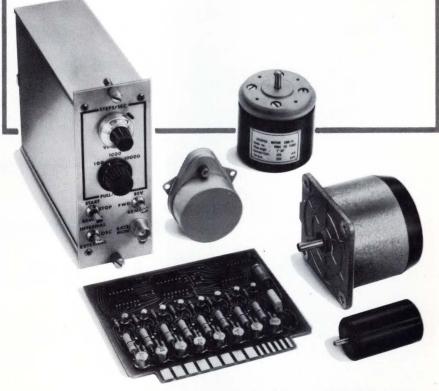
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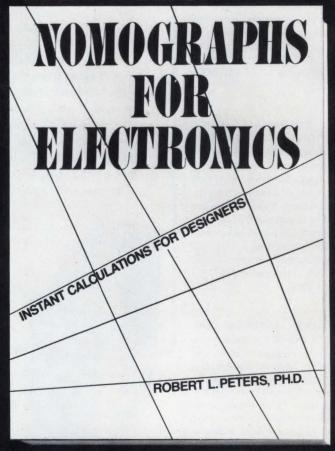
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DIGITAL MULTIMETERS



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#### **EQUIPMENT**

DIGITAL ACCURACY COMES TO OS-CILLOSCOPES. The new 7000-Series plugin offers both time delays and the ability to delay by a number of events. Following a trigger and after a preselected time, this unit will give a delayed trigger output. The delay time is indicated on the scope CRT readout and is displayed along with the measured signal. Accuracy is 0.5 ppm ±2 nsec and jitter is less than 2.2 nsec. Delay time is 100 nsec to 1 sec. \$1475. Tektronix, Inc., P.O. Box 500, Beaverton, OR 97005. Phone (503) 644-0161.

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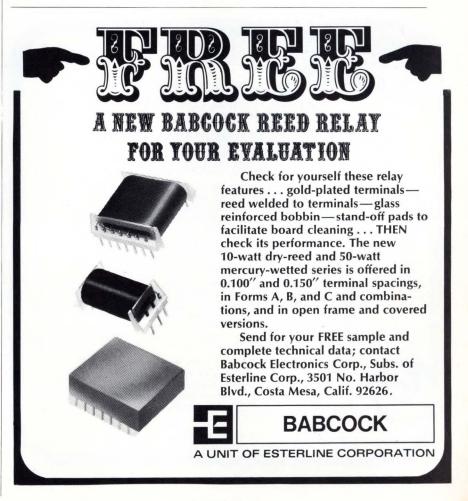
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RAM/ROM TESTER CHECKS BOTH MOS AND BIPOLAR MEMORIES. The Model 150 bench-top tester offers automatic and manual testing of up to 4096 × 8-bit RAMs and ROMs. The operator has manual control of read/write timing while the basic timing rate is up to 8 MHz. A built-in confidence check verifies all internal circuitry prior to RAM/ROM testing. Up to eight RAMs may be tested in parallel while four ROMs may be exercised. Spectrum Dynamics, Inc., 2300 E. Oakland Park Blvd., Ft. Lauderdale, FL 33306. Phone (305) 556-4467.





#### COMPONENTS/MATERIALS

CIRCUIT-DECK SWITCHES HAVE RESIS-TOR NETWORK BUILT IN. Two circuitdeck switches, the Model 1391-41 Decade Attenuator and 42 Ratio Attenuator, combine switching function with resistive components, conductors, interface connections, and switch pads into a single monolithic structure. The Model 41 Decade Attenuator with op amp gain resistors provides precision ratio division of four decades ranging from 1 to 0.0001. The 42 Ratio Attenuator is a combination of a simple resistive string divider and a ladder network. Helipot Div., Beckman Instruments, Inc., P.O. Box 11866, Santa Ana, CA 92711. Phone (714) 871-4848

HYBRID CAPACITOR DESIGN KIT COVERS COMPLETE CAPACITANCE RANGE used in hybrid circuits. Each kit contains a total assortment of 280 KEMET tantalum and ceramic chip capacitors and supporting technical literature. The total range of KEMET chip capacitors is 1 pF through 100 μF. Union Carbide Corp., Components Dept., P.O. Box 5928, Greenville, SC 29608. Phone (803) 963-7421.

THUMBWHEEL SWITCHES COMBINE LOW COST AND SMALL SIZE. SM Series Subminiature Switches are housed in a 0.312 in. wide package and feature a unique "Snap-N-Lock" front clip mounting design. This eliminates the need for close tolerance panel cutout. Standard versions include 10 Position Decimal, BCD, Complementary BCD, and BCD plus Complement. Price is \$2 each in small quantities. Syscon, Inc. P.O. Box 265, Freehold, N J 07728. Phone (201) 462-1534. 234

#### CAPACITOR LINE USES CERAMIC MA-TERIAL WITH DIELECTRIC CONSTANT

of 50,000. This titanate ceramic material represents a significant reduction in size for ceramic capacitors used for coupling and decoupling in AF circuits. Radial leaded, flat capacitors having capacitance values up to 220 nF. The voltage rating is 40V dc in comparison with 16 or 30V dc in comparable ceramic capacitors. Operating temperature is -25°C to 85°C. Samples are available from stock. Siemens Corp., Components Div., 186 Wood Ave. S., Iselin, N J 08830. Phone (201) 494-1000.



GREEN NEON LAMPS WIDEN INDICATOR COLOR CHOICE. The lamp, the first long-life green neon glow lamp, actually adds two colors, green and blue (with filter), to the red, yellow and orange of present glow lamps. Called the G2B, the new lamp is directly interchangeable electrically and physically with GE's C2A glow lamp. Average useful life of the G2B is 10,000 hours. General Electric Co., Nela Park, Cleveland, OH 44112. Phone (216) 266-2258.

GaAsP LAMPS OFFER HIGH LUMINANCE AT LOW CURRENT, long life, and low cost. Available in models 521-9185, red non-diffused, and 521-9186 red diffused lenses, they provide a high luminous intensity —750 foot L at 20 mA. Price of these units is \$.38 in quantities of 1000. Dialight Corp., 60 Stewart Ave., Brooklyn, NY 11237. Phone (212) 497-7600. 237

SILICON BLUE PHOTO-CELL HAS PEAK RESPONSE IN VISIBLE REGION. A photovoltaic silicon blue cell offering a spectral response that peaks at 700 nm, the SBC-2020, features minimized dark current, a high linearity of output photocurrent, and rapid response time. Shigoto Industries, Ltd., Empire State Bldg., New York City, NY 10001. Phone (212) 695-0200. 238



INSULATED HEAT PIPE WITHSTANDS HIGH VOLTAGES. This heat pipe withstands voltages of 44 kV between heat source and heat sinks. It incorporates a fused ceramic adiabatic section between the copper evaporator and copper condenser section. Units are available to cover a wide range of sizes and temperature ranges. Isothermics, Inc., 291 River Rd., Clifton, N J 07014. Phone (201) 473-3555.

ing technical literature. The total range of KEMET chip capacitors is 1 pF through 100 peratu availal Dept., P.O. Box 5928, Greenville, SC 29608. Phone (803) 963-7421. 233



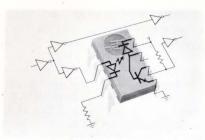
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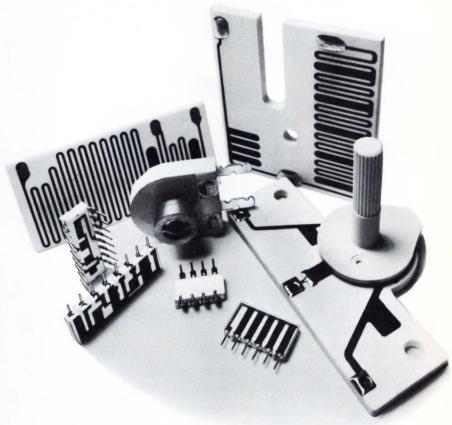
VERY HIGH-SPEED OPTICAL ISOLATORS HAVE 5 MHz BANDWIDTHS. These Model 5082-4350 Series isolators have a propagation time of only 226 nsec max. Gainbandwidth product is achieved by coupling the LED to a monolithic IC chip consisting of a photodiode detector driving a transistor amplifier. Prices are \$2 to \$5 each in 1000-piece orders. Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, CA 94304. Phone (415) 493-1501.

RUGGEDIZED EDGE-READING METER IS ILLUMINATED. Designated "parkermeter" Series EMI-30, this instrument is 1/2 in. thick, 2.9 in. wide. The meter weighs less than six oz. Illumination is provided by two or more subminiature lamps. Any number of EMI meters may be grouped on 1/2 in. centers for high-density display; 38 can be accommodated in the width of a 19 in. rack. Price: \$66.50 in quantities of 100 pieces. Airpax Electronics, Controls Div., 6801 W. Sunrise Blvd., Ft. Lauderdale, FL 33313. Phone (305) 587-1100.



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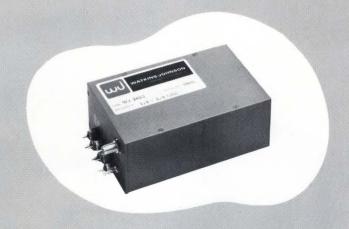
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#### COMPONENTS/MATERIALS

SLOTTED OPTICAL LIMIT SWITCH INCORPORATES AN LED EMITTER and a photo-darlington optical sensor. The new unit is available in two models, the MCA8 and MCA81, the principal difference being the transfer ratio of LED current to collector current. The new units permit direct interfacing with TTL. Price is \$2.85 to \$3.70 in 100 quantities. Monsanto, 10131 Bubb Rd., Cupertino, CA 95104. Phone (408) 257-2140.



FREE SAMPLES OF HIGH BRIGHTNESS NEON LAMPS. High Bright neon lamps give almost 50% more light (at the same current) than standard neons. They operate at 0.1-1.0 mA without flickering with adequate illumination for indicator use. The family of T-2 lamps available in any length from 1/2 in. to 1 in. Glowlite Corp., Subsidiary of El-Tronics, Inc., Pauls Valley, OK 73075. Phone (405) 238-5541.



CERAMIC HEAT TRANSFER WASHERS EXHIBIT LOW THERMAL IMPEDANCE. Breakdown voltage is 1000V, min. The low thermal resistance (0.15°C per W) ensures that the full power capability of the semiconductor could be utilized while insulating the device with 100% confidence. Thermal performance is 5 times better than mica. The price for 1-49 is 58¢ each. Jermyn, 712 Montgomery St., San Francisco, CA 94111. Phone (415) 362-7431.

**OPTICAL COUPLERS PROVIDE 4000V ISOLATION.** The H15A1 and H15A2 modules have a typical 3  $\mu$ sec. rise/fall time. They have 0.100 in.-pin spacing and will fit into DIP sockets. All models are IC compatible. Suggested resale prices range as low as \$.38 in 1000 lot quantities. General Electric, Electronics Park, Bldg. #7, Mail Drop 49, Syracuse, NY 11320. Phone (315)

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Spurious	-80 dB	-70 to
Phase Noise	-63 dB	-
A-M, FM Capability	standard	
Search-Sweep	standard	
		-

Runner-up A	Runner-up B
1 MHz to 160 MHz	10 kHz to 110 MHz
1 ms	5 to 100 ms
+ 13 dBm	+ 13 dBm
-70 to -100 dB	-80 dB
-60 dB	-50 dB
no	optional
no	optional
	1 MHz to 160 MHz 1 ms +13 dBm -70 to -100 dB -60 dB no

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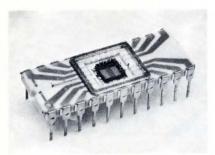
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ASCII CHARACTER GENERATOR PROVIDES 64 CHARACTERS of 63-bits each, arranged in a 9 × 7 format. The circuit is fabricated using P-channel silicon gate technology and offers access and cycle times of 350 nsec. The MF7107 is directly DTL and TTL compatible. It is available in a 22 lead cermaic DIP package at \$18.20 in 100-999 quantities. Microsystems International Ltd., Box 3529, Station C, Ottawa, Canada K1Y4J1. Phone (613) 828-9191.

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TTL MULTIPLEXER WITH STORAGE REPLACES TWO MSI CIRCUITS. The SN54/74298 quad 2-input multiplexer consists basically of the SN74157 multiplexer with a quad D-type flip-flop added to store information selected by the quad multiplexer. The circuit selects one of two 4-bit data sources and stores data synchronously with the system clock. Texas Instruments Inc., 13500 N. Central Expressway, Dallas, TX 75222. Phone (214) 238-2011.

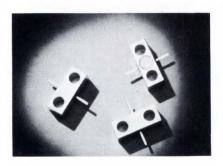
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HIGH SPEED OP AMPS EXHIBIT 500 V/μSEC UNITY GAIN SLEW RATES, 70 MHz small signal bandwidth, and 15 MHz full power bandwidth. The LH0032/LH0032C utilizes a J-FET input stage to achieve bias currents in the 10 pA range, while the LH0024/LH0024C employs a conventional bipolar input stage. 100-piece prices are: LH0024, \$40; LH0024C, \$15; LH0032, \$40; LH0032C, \$18. National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051. Phone (408) 732-5000.

COMPLEMENTARY NPN/PNP PLASTIC POWER TRANSISTORS ARE RATED AT 5A. The NPN silicon power units are indentified as the SDT 5101-03 and the PNP as the SDT 5111-13 Series. Specifications include typical gain of 100 each at 1.0A and typical  $V_{CE}$ (sat) each at 2.0A of less than 0.5V. They are priced at 70c per pair in 100 pair quantities. Solitron Devices, Inc., Semi-Conductor Div., 1177 Blue Heron Blvd., Riviera Beach, FL 33404. Phone (305) 848-4311.

MOS INTERFACE CIRCUIT is designed to interface or convert data from serial communications links to data processing equipment. The TMS6010 combines full transmit, receive, and format functions on a single MOS/LSI chip. The TMS6010 is immediately available in a 40-pin plastic DIP. It is priced at \$15 in 250-piece quantities. Texas Instruments Inc., 13500 N. Central Expressway, Dallas, TX 75222. Phone (214) 238-2011.

N-CHANNEL SI-GATE RAM IS BIPOLAR COMPATIBLE. The EA 1502 is a 1024 by 1 random access memory with input level shifters and an output sense amp on the chip for direct TTL compatibility at the address and data inputs, and the data output. The EA 1502 operates on ±12V power supplies. The RAM also features an "automatic refresh" mode. Price is \$27.50 in 100-piece quantities. Electronic Arrays, Inc., 501 Ellis St., Mt. View, CA 94040. Phone (415) 964-4321.



STRIPLINE PIN DIODES OPERATE FROM 100 MHz to 12 GHz. Designed to withstand adverse environment, these new diode switches/attenuators pass MIL specs for a variety of environmental tests. The new package is a direct mechanical replacement for the present metal-plastic package. In quantities of 10 through 99, unit price is \$21.50. Hewlett-Packard Co., 1501 Page Mill Rd., Palo Alto, CA 94304. Phone (415) 493-1501.

SCHOTTKY TTL/MSI MULTIPLEXERS ANNOUNCED SN54S/74S151, an 8-line-to-1-line multiplexer, SN54S/74S157, a quad 2-line-to-1-line multiplexer with noninverting data lines, and SN54S/74S158, a quad 2-line-to-1-line multiplexer with inverting data lines are now available for use in high performance TTL systems. 74S devices are available from stock in plastic DIPs for \$4.50 to \$7.20 each in 100-piece quantities. Texas Instruments Inc., 13500 N. Central Expressway., Dallas, TX 75222. Phone (214) 238-2011.



LOW COST MINIATURE PACKAGE INTRODUCED FOR LICs. Called the "Pico Pak", it has a silicone plastic body that measures 0.21 by 0.14 by 0.06 in., while a comparable 8-pin dual-inline package is 0.73 by 0.27 by 0.18, and a flatpack measures 0.25 by 0.25 by 0.07. Intersil is offering three circiuts in the Pico Pak, the 8007 FET-input op amp, the 8021 micropower op amp, and the 8001 precision low power comparator. Intersil, 10900 N. Tantau Ave., Cupertino, CA 95041. Phone (408) 257-5450.

TTL IC ENCODERS REPLACE 7 SSI PACK-AGES. Designated the SN54/74147 and the SN54/74148, the MSI circuits encode 10-line-to-4-line and 8-line-to-3-line data, respectively. The 147 encodes full 10-line decimal to its corresponding 8-4-2-1 binary code with full on-chip input priority. Prices range form \$2.27 to \$14.31 depending on package and temperature range. Texas Instruments Inc., 13500 N. Central Expressway, Dallas, TX 75222. Phone (214) 238-2011.

**TRACKING REGULATORS PROVIDE**  $\pm 15V$  **POWER FOR OP AMPS.** The MC1568 may be programmed to outputs of  $\pm 14.5$  through  $\pm 20V$  by adding two suitable external resistors. At  $\pm 15V$  the absolute value of output voltages agrees within a max. of 1%. The MC1468 sells for less than \$3 in 100-up quantities. Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036. Phone (602) 273-6900.

TTL/MSI LED/LAMP DRIVERS REPLACE SEVERAL PACKAGES. Two TTL/MSI each contain a four-bit synchronous counter, a four-bit latch, and a seven-segment decoder/LED or lamp driver. Designated the SN54/74134 and 144, these circuits each contain the equivalent of 86 gates. The 143 features constant current outputs. Prices range from \$3.60 to \$21.60 Texas Instruments, Inc., 13500 N. Central Expressway, Dallas, TX 75222. Phone (214) 238-2011.

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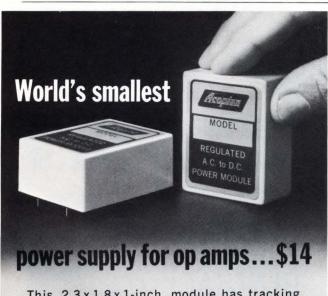
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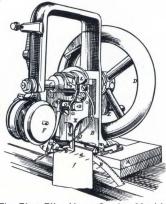


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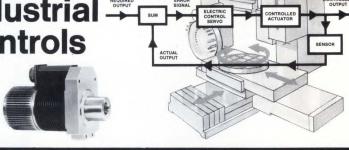


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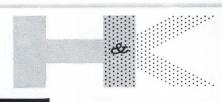


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#### LITERATURE



MODEMS - A 6-page brochure describes Models 2020 and 2021, a pair of Bell 202C compatible modems capable of asynchronous operation up to 1200 baud over dialup telephone lines. An outline drawing of the printed-circuit card is included, as well as a Model 2020/2021 block diagram, a data mode timing diagram, an illustration showing typical carrier detect circuit operation and a block diagram of both calling and answering station call procedure sequences. Intertel, 6 Vine Brook Pk., Burling-208 ton, MA 01803.



POWER-SUPPLY SELECTION GUIDE. A new 6-page selection guide provides a convenient method of selecting standard Cirkitblock<sup>TM</sup> modules allowing the user to build his own custom power supply. Simple tables give information for forming complete power-supply systems by connecting one or more output modules to an input power module. The guide also shows photographs of typical applications. Powercube Corp., 214 Calvary St., Waltham, MA 02154. 212



ULTRAMINIATURE DC POWER SUPPLIES are described in a 2-page brochure. It gives specifications and features on a complete line of pc-board mounting dc power supplies for both digital and linear integrated circuits as well as a/d and d/a converters. Included is a selection guide which categorizes dc power supplies according to output (voltage and current), regulation data, price information, and complete mechanical specifications. Datel Systems, Inc., 1020 Turnpike St., Canton, MA 02021

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PORTABLE INSTRUMENTATION RF-CORDERS. A 36-page brochure describes the Philips ANA-LOG 7 and ANA-LOG 14 portable cartridge instrumentation recorders. The brochure contains detailed technical descriptions of the features and functions of the recorders and their accessories and provides information on various applications and related instrumentation requirements. Test & Measuring Instruments Inc., 224 Duffy Ave., Hicksville, NY 11802.

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RATIO STANDARDS. A bulletin describes precision voltage dividers for instrument standards in calibration laboratories. They feature 1-ppm terminal linearity and ratio resolution to seven places. All units have transient suppression and are available with either high or low-frequency capability. Certification is provided with these ratio standards showing traceability to NBS. Singer Instrumentation, 3211 S. LaCienega Blvd., Los Angeles, CA 90016. 213 SPECTRUM ANALYZER CATALOG. Nelson-Ross spectrum analyzers, available for measurements from 0.5 Hz up to 6.5 GHz, are shown in a new catalog which provides specifications for 15 complete spectrum analyzers and 30 low cost plug-in analyzers for Tektronix and Hewlett-Packard oscilloscopes. Also included are several new analyzers and accessories not previously described. Nelson-Ross Electronics Div., 5 Delaware Dr., Lake Success, NY 11040. 217

ACCUMULATING DIGITAL PRINTER. The technical data sheet describes the Series 7726 accumulating digital printer which is used to produce printed records for inventory control and cut-to-length applications. Standard features are automatic and remote paper advance, BCD or BCD input, leading zero suppression, decimal point, busy signal, and totalize/non-totalize, with add/ subtract functions in the totalize mode. Veeder-Root, 70 Sargeant St., Hartford, CT 210

**AUTOMATIC CALLING UNITS.** Bulletin #7002 describes the various models and versions of the 907801 series of equipment. Five different models, each in either pulse or tone outdialing, is covered. Features of each, EIA interface specifications and other important information is included. Ordering information including appropriate part numbers for each model is contained in the bulletin. G. V. Controls, Div. of Sola Basic Ind., 101 Okneb Pkwy., Livingston, N I 07039.

PROXIMITY FOCUSED IMAGE INTENSI-

FIER. An 11-pg. booklet entitled "The Proximity-Focused Image Intensifier" explains the basic operation of the proximity focused image intensifier and compares it to other types of image intensifiers. It also contains a section on the Channeltron electron multiplier array and how it is used in conjunction. with proximity focused image intensifiers. The Bendix Corp.'s Electro-Optics Div., Galileo Park, Strubridge, MA 01581. 218

PHOTOELECTRIC CONTROLS PROVIDE VERSATILITY AT LOW COST. The well illustrated 8-pg. brochure describes various applications of standard plug-in logic cards in self contained, remote or multiple controls. The inherent versatility is shown in all detail and summarized by a log output/signal duration comparison chart. Other information includes specific data on various housings, dimensions and wiring diagram. Micro Switch - Farmer Electric, Tech Circle, Natick, MA 01760. 211

HOW TO CUT COMMUNICATIONS COSTS. The 8-page, brochure presents a full discussion on how multiplexing - especially time division multiplexing-can be employed by large communications users to economically cut phone-line transmission costs. The brochure also describes how to get all incoming traffic into your computer more efficiently. Request "Safe and Simple" brochure by sending a written request on company stationery to: Infotron Systems Corp., 7300 N. Crescent Blvd., Pennsauken, 215 NJ08110.

CRT CONSOLE. An actual size poster of the FOX 1 CRT console-communications center of the FOX 1 process management and control systems - features the CRT display and keyboard portions of the console. It is printed on a 35-x-35-in. heavy stock suitable for wall-mounting. Available with the poster is a brochure describing the console's display capabilities depicting the console's applicability to various industries and to various plant control needs. The Foxboro Co., Foxboro, MA 02035.

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by Dennis L. Lock

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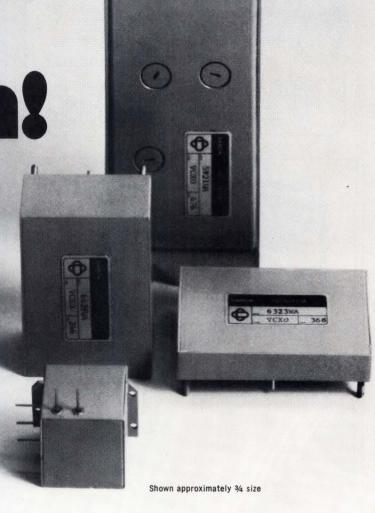
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#### **SPECIFICATION GUIDE\***

OI EDITION GOIDE				
Parameter	Basic and Multiplier VCXOs	Mixer and Mixer- Multiplier VCX0s		
Center Frequency	1 KHz to 300 MHz	100 Hz to 300 MHz		
Frequency Deviation	±0.01% to ±0.25% of C.F.	±10 Hz to ±1 MHz		
Frequency Stability 24 hr. @ 25°C	±1 to ±10 ppm	±0.5% of peak deviation		
0 to 65°C (no oven)	±10 to ±50 ppm	±2% of peak deviation		
Linearity	to within 1% of best straight line	to within 1% of best straight line		
Minimum Deviation Rate	0 (dc)	0 (dc)		
Maximum Deviation Rate	0.2% of C.F. (100 KHz max.)	10 KHz to 100 KHz		
Mod. Voltage (Typical)	±5 V peak	±5 V peak		
Mod. Input Impedance	>50 K ohms	>50 K ohms		
<b>Output Power Available</b>	0.5 mw to 20 mw	0.5 mw to 20 mw		
Load Impedance	50 ohms to 10 K ohms	50 ohms to 10 K ohms		
Power Requirements (Typical)	$-25~\mathrm{V} \pm 1~\mathrm{V}$ @ 30 ma	$-25~{ m V} \pm 1~{ m V}$ @ 40-50 ma		
C.F. Manual Adjustment Range	±0.01%	±5% of peak deviation		

<sup>\*</sup> Obviously, the limits are not absolute. The interrelationship of parameters for VCXOs are of such a nature as to permit optimization of any one or more characteristics to satisfy customer requirements.





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#### Core-memory maker responds

Dear Sir:

After reviewing the answers and predictions regarding the memory market of the mid-70's as presented in the "Speak Out" article by Fillingham and Chong of Nemonic Data Systems (EDN/EEE March 1, 1972), we're torn between sputtering with rage and holding our sides from laughing. The arguments in favor of plated wire are based on faulty marketing combined with foolhardy optimism. We would like an opportunity to set the record straight, point by point.

Messrs. Fillingham and Chong predict a \$625 million high speed random-access non-IBM memory market in 1973. However, market surveys by the Arthur D. Little Co. and by Quantum Sciences show that the available market is less than 20 billion bits. At the present trends, the average price of core memories will be below 1 cent a bit; this would yield a market value of only \$200 million, or less than 30% of the value asserted by the article.

Once more in reference to the most recent established market surveys, the plated wire share in 1971, 1972 and 1973 is less than 1%. For the plated wire industry to achieve a 10% market share in 1972, they would have to increase their penetration 10 fold in one year. Nonsense!

Extrapolation of the 1971 market predicts plated wire to have less than a \$5 million potential in 1973. This is hardly a base for the capital equipment already invested by most companies, let alone a market for new developments.

I am assuming that the plated-wire memory prices at half million bit capacities being delivered are a shade over 1 cent per bit, not 0.1 cent per bit as written. However, this price is far from competitive. Today core memories are shipping in volume in capacities of 150,000 bits at less than 1 cent per bit. Published price lists from most core manufacturers are available to prove the 1 cent/bit fig-

ure. Five-million-bit core memories are shipping at 0.6 cents/bit today. Core memories were delivered in 1971 at prices close to 0.7 cent/bit. The present reduction trends in core memories indicate that further price reductions of at least 10% may be expected in 1973.

On the subject of "old-thinking" technologies, once more the plated wire people have underestimated the advanced technologies of present day production core memories. Present day core memories are not an oldthinking technology; they are made with modern day automated techniques packaged in streamlined highbit-density packages operating at speeds of between 500 nanoseconds and 650 nanoseconds in the major production units. On a feature-byfeature basis, core memories win out but sell at lower prices; this is why the "old thinkers" buy core memories. Sincerely,

Philip A. Harding Director of Marketing Commerical Products Electronic Memories

#### So you want to get ahead, do you?

One of our readers has come up with some extremely helpful hints. Follow them religously and you are sure to get somewhere!!!

#### Position improvement

Every red blooded American, and others, wants to succeed. There are certain well-proven techniques that can be applied towards this goal.

- a. Arrive and leave your office before and after your boss, respectively.
- b. If you can't buy 30,000 shares of your company's stock, call up 3000 friends and ask them to buy 10 shares each and give you their proxies.
- Dress well, play bridge, tell jokes and be intelligent, but don't do any of these things better than the boss.
- d. Oh yes! It also helps a little to do a good job.

#### Self-improvement

If you don't keep up with the fast pace of technical advancement, you may have to open a delicatessen and hang your diplomas over the steam table. Come to think of it, that doesn't sound too bad.

#### Go back to school

Take the latest courses of your per-

suasion, although you may find that you're the most backward in your class. Bright, hungry, aspiring, young students will look at you admiringly, but pitifully. You can always audit the course and no one will know; however, no company refund. If you take the course for credit, ask your instructor if he consults. As a last resort, do the homework.

#### Go to lectures

Bring yourself abreast of the field. Listen to a paper that took two years to culminate and then put it under your belt in 15 minutes. Out of town lectures are usually more meaningful than those close to home. After all, the company pays for this trip, so the least you can do is to make an attempt to get something out of it.

#### Go to conventions

See what your competitors have accomplished and learn how you should have done it yourself. Walk from booth to booth for miles and miles. Collect a ton of literature (which will be discarded in 2 weeks anyway). You may accomplish very little that day, but you'll feel so tired it will seem that you must have accomplished a great deal. A. W. Zinn

#### Drat that tail light -

My friend, P. H. Dee, is still mulling over a puzzling problem with his car. His right rear stop light refuses to work, even though he has checked the bulb and found both tail and stop filaments OK, and his VOM shows he has 12V between the stoplight wire and ground when the brakes are applied. Even more mystifying is that both tail lights work under normal circumstances. But, when he applies the brakes, the right tail light goes out. The left light works normally, both tail and stop filaments lighting at their appropriate times. Maybe you can help P. H.?

Very truly yours,

F. R. Collins, Alcoa Conductor Products Co.



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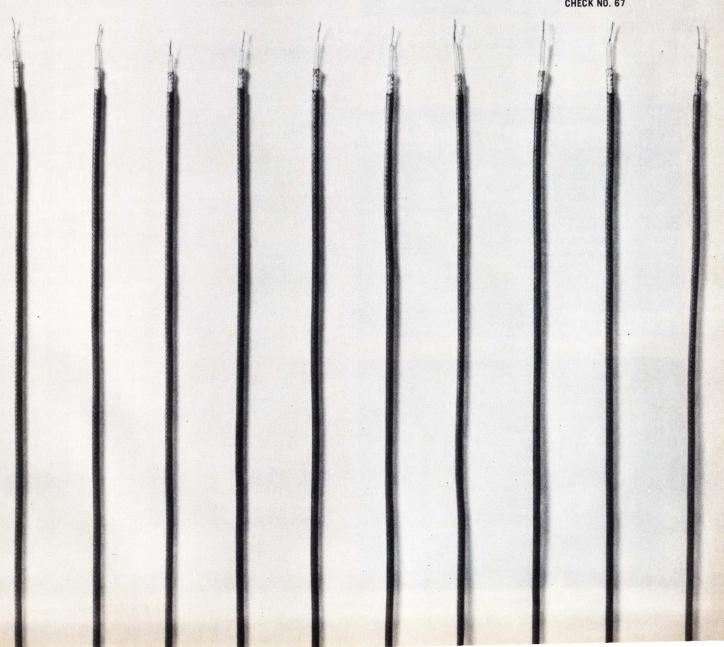
It's the third from the left. Times' new high-strength miniature cable, designed and constructed to eliminate the conductor breakage problems commonly experienced by users of RG-178B/U, RG-179B/U and RG-180B/U.

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#### **Application Notes**

BETA VARIATION METHOD FOR COM-PUTER SIMULATED CIRCUITS. The relation between the gain of a transistor and its collector current may be simulated following the method described in a 27-pg. AED-CAP application note. The method is presented as an augmentation of the Ebers and Moll transistor model commonly used in computer simulation of electronic circuits. It may be used in SofTech's simulation system—AEDCAP—or in other simulation systems. SofTech, 391 Totten Pond Rd., Waltham, MA 02154. selection and evaluation guide on synchro and resolver data conversion is now available. Covering the many sophisticated approaches available, the booklet describes some of the most advanced state-of-the-art conversion devices applicable to industrial, commercial, avionics and military ground-support systems. Accompanying the guide are application notes comparing tracking, multiplexed, synchro-to-linear and synchroto-nonvariant sine/cosine converters. Data Device Corp., 100 Tec St., Hicksville, NY

MINIATURE ACTIVE FILTER. A hybrid, two-pole, audio-frequency filter that can be used as a basic building block to generate virtually any complex filter function is featured in a new publication. The 8-page catalog sheet fully describes the features of the Model 881 universal active filter, a hybrid IC using multiloop negative feedback to achieve exceptional stability. Helipot Div., Beckman Instruments, Inc., 2500 Harbor Blvd., Fullerton, CA 92634.

BIOGRAPHY OF A MINI. The four-color 16-pg. document describes the development, featuers and applications of the 16-bit NAKED MINI 16 and ALPHA 16 minicomputers and the philosoophy that lead to their creation as true OEM system components. In addition to minicomputer performance and specifications, the brochure details the exhaustive quality assurance procedures that contribute to the products' realiability. Computer Automation Inc., 18651 Von Karman, Irvine, CA 92664.

C-V MEASUREMENTS MADE WITH LOCK-IN AMPLIFIER. An illustrated 16-page application note describes in detail the use and advantages of a lock-in amplifier and current-sensitive preamplifier for accurate measurement of semiconductor admittance. In addition, an in-depth discussion of the measurement theory, including the required mathematics, calibration procedures and measurement methods are provided. Princeton Applied Research Corp., PO Box 2565, Princeton, N J 08540.

STORED PROGRAM MAGNETIC TEST SYSTEM. A 36 page brochure on the Delta 400 includes sections on cost and operation—as well as comprehensive application notes. Delta 400 is comprised of a series of test/measurement and data acquisition systems which provide stored-program, digital control and programmable instrumentation for evaluating magnetic memory elements and arrays. Computest Corp., Three Computer Dr., Cherry Hill, N J 08002.

REAL-TIME NOISE ANALYSIS. Several common applications for real-time analysis are discussed showing how real-time analysis can be used to measure and analyze noise to help the engineer involved in the control and reduction of noise. Features, peripheral equipment and custom systems are discussed to show the broad capabilities of a GR real-time analysis system. General Radio, 300 Baker Ave., Concord, MA 01742.

CIRCUIT DIAGNOSIS VIA A LOGIC PROBE. Application note describes the use of two inexpensive digital test instruments. The logic pen measures logic levels and the presence or absence of pulses and pulse trains. The Chronos DTM measures period, pulse width, and delay of pulses and pulse trains in digital logic circuitry. Advanced Digital Research Corp., 1901 Old Middlefield Way, Mt. View, CA 94040.

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