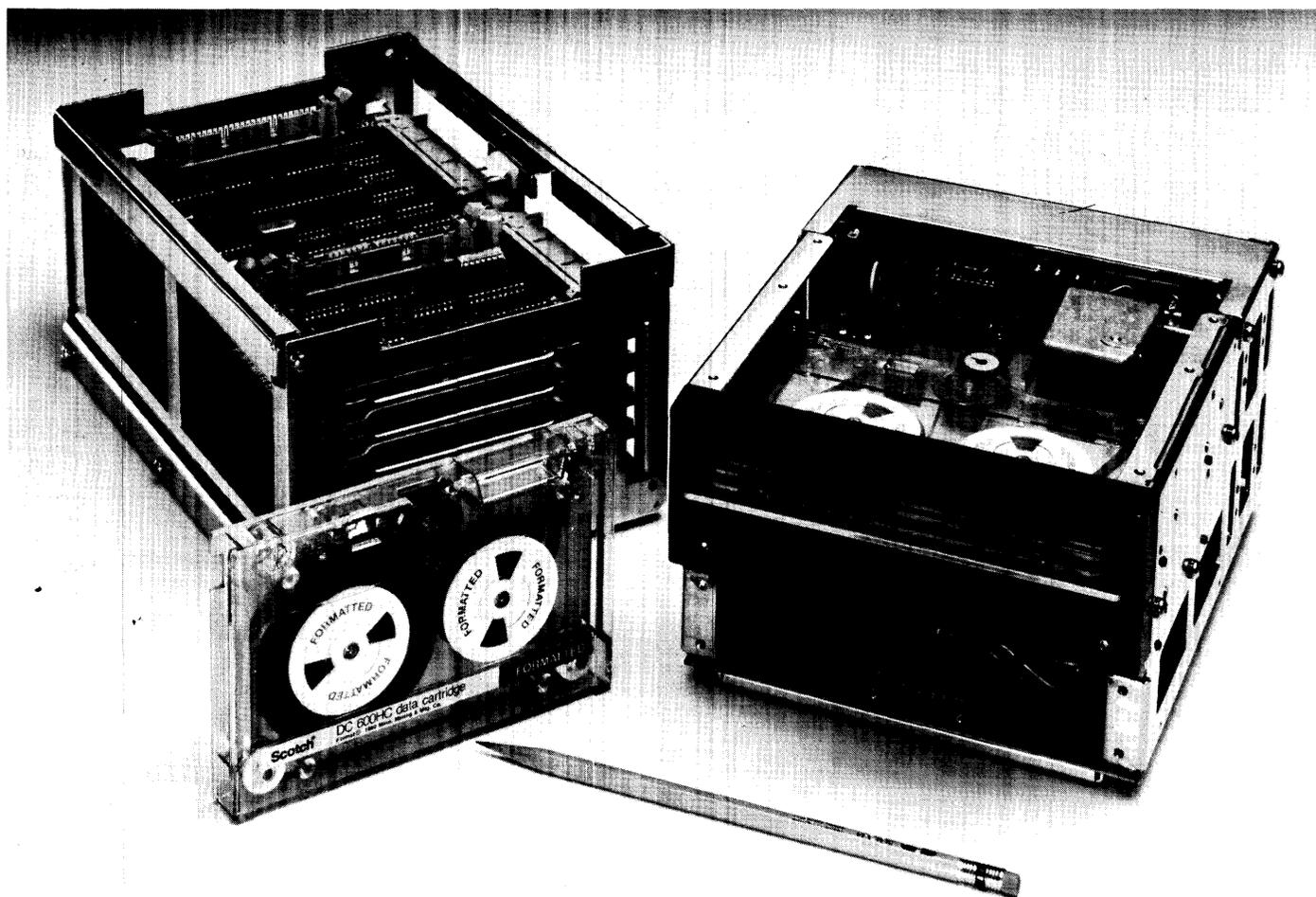


# 3M Brand HCD-75 High Capacity Data Cartridge Drive System

## User Manual

February 1983



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# OVERVIEW

The 3M HCD-75 High Capacity Data Cartridge Drive System is a 1/4" tape cartridge system that can be used to record up to 67.1 megabytes of user data on the 3M Brand DC600HC Data Cartridge. The HCD-75 system consists of three basic components—drive module, controller module, and data cartridge—that offer the flexibility to fulfill the user's specific requirements. The compact design of the system itself and the high density storage capability of the magnetic tape help to save the user both space and expense as compared with the one-half-inch tape systems.

The system command structure for the HCD-75 is simple and straightforward. The HCD-75 features parallel data input/output of 16-bit words (or optional 8-bit bytes). The system's dual, 1024-byte I/O buffers allow asynchronous transfer at an average rate of approximately 35 KBYTES/SEC at 60 IPS or 17.5 KBYTES/SEC at 30 IPS.

Local control of all tape drive functions frees the host from:

- Controlling the tape direction and speed.
- Locating the desired block.
- Encoding and decoding data.
- Fault detection.
- Error detection and correction.
- Skipping defects in the tape.

One HCD-75 controller can run up to four drives, without special modifications and without giving up any of the system's high reliability. The HCD-75 drive module and controller run their own self-testing routines that can quickly pinpoint any faults and pass information about them on to the operator by means of precise error messages.

An important HCD-75 feature, tape segmenting, can be called into play when relatively fast access times are required. Tape segmenting is a means of dramatically reducing access times by artificially shortening the length of tape over which operations take place.

Inherent to all magnetic recording media are imperfections which will cause loss of recorded data. To overcome these imperfections the DC600HC cartridge can be completely certified by performing a write operation on the entire cartridge while keeping track of all unlocatable keys. After the write is complete a skip table is generated with the unlocatable keys and an off line Verify operation is initiated. On completion of the Verify a bad block table will have been built within the controller listing all unrecoverable data blocks by key address. This table along with the unlocatable keys can be merged together to form a skip table that can be recorded on that cartridge.

## DOCUMENTATION

This document, the HCD-75 User Manual, is intended to provide the user with more detailed information than may be found in introductory marketing material. Although this manual does include some introductory information about the HCD-75 system, the information is presented as a part of the more detailed information that is needed to operate HCD-75 system components.

The HCD-75 User Manual is structured in sections, each of which covers system components in detail and describes step-by-step procedures for operating an HCD-75 system. Installation information and specifications are presented in such a way as to allow the user to install and operate a system without having to refer to other sources of information.

The sections of this manual and their central topics are:

1. Overview—This section provides an introduction to the HCD-75 system and its operation.
2. General Description—The second section of the manual describes each of the principal HCD-75 system components and its place in the system:
  - Drive module.
  - Controller module.
  - Parallel and serial interfaces.
  - Data cartridge.

In addition, operating characteristics and parameters of the system are detailed.

3. Parallel Interface—This section provides specific information concerning the parallel interface control and data lines. Full description is given concerning parallel interface commands and data transfers.
4. Data Controls—Provides information concerning how to set up for DC615HC cartridges. Describes the function of a skip table and how to generate the skip table. Information is also given on shortening access time, addressing modes and serpentine recording.
5. Drive Module—Describes how to change the drive address and the meaning of the two LEDs on the front of the drive.
6. Serial Interface—This section provides full description for RS232 Diagnostic Serial interface commands.

7. **Memory location of Interest**—This section is a collection of memory locations that may be of interest to the user.
8. **User Options**—This section contains information on special features of interest to the user.
9. **The Installation section** provides the information that is required in order to install and HCD-75 system. Not only are procedures outlined, but packaging is described and installation mounting and dimensions are illustrated. Specific instructions for assembling cabling for the system are also included.
10. **System Specifications**—In this section are the measurement boundaries within which the HCD-75 system will operate and which must be controlled at the location where the system will be operated.

# GENERAL DESCRIPTION

## DC600HC DATA CARTRIDGE

The 3M Brand DC600HC Data Cartridge is a self-contained, magnetic tape storage medium designed for use with the 3M HCD-75 High Capacity Data Cartridge Drive System. Each DC600HC data cartridge contains 600 feet of 1/4" magnetic tape with a capacity of up to 67.1 megabytes of user data. A 3M Brand DC615HC Data Cartridge with 150 feet of tape is also available.

The pre-formatting of each tape by 3M eliminates any need for conventional inter-record gaps. Instead, permanent forward/reverse-reading keys establish block locations on the tape, saving the user time by internally handling error detection and correction without requiring any further formatting by the user. During read operations, error detection and correction routines ensure typical error rates of less than one unrecoverable error in  $10^{10}$  bits. Each data block can contain 1024 bytes of user data, as well as synchronization, header, and error-correction information. Beginning-of-tape (BOT) and end-of-tape (EOT) locations are already in place on the tape and each is uniquely identified.

The DC600HC Data Cartridge format records data using inverted modified frequency modulation (IMFM) recording on 16 tracks with a density of 10,000 bits per inch and provides unlimited record replacement.

## HCD-75 DRIVE MODULE

The HCD-75 Drive Module directs and supports the operation of the tape activity. The principal components of the drive module are:

- Mechanical assembly.
- Motherboard.
- 2 pc card assemblies.

The design of the drive allows its assemblies and parts to be completely interchangeable between drives without further alignment or adjustment.

The HCD-75 Drive Module has three major functions:

- A stable baseplate allows repeated, accurate positioning of the cartridge and tape.
- Cartridge control of sensing and tape motion.
- A serial read and write data channel.

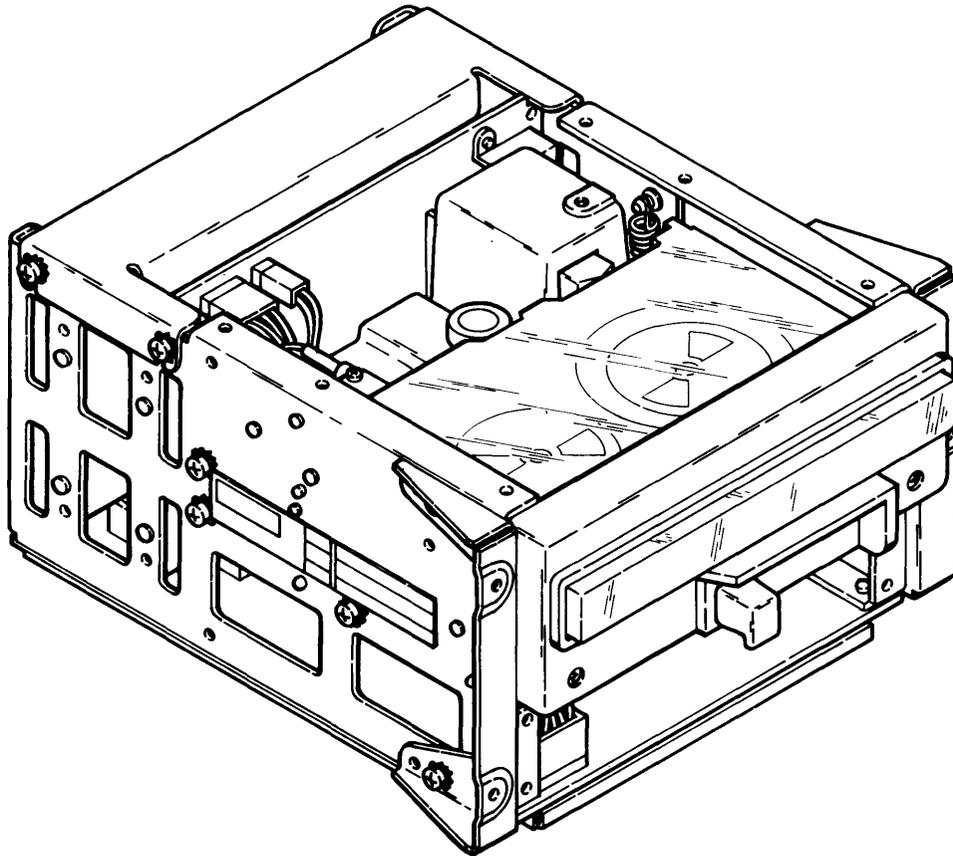
A significant number of other sophisticated features have been incorporated into the design of the drive module:

- Cartridge positioning.
- Tape speed control.
- Tape-to-head contact.
- Tape head positioning.
- Read/write electronics.

**Cartridge positioning:** The data cartridge is accurately positioned and held stable during operation by means of a 3-point positioning scheme. The 3-point scheme eliminates the uncertainty of positioning that often occurs in systems with four or more points. In addition, a mechanical interlock between the cartridge eject lever and the head positioner prevents the removal of a cartridge while it is being used by the system.

**Tape speed control:** Tape speed is digitally controlled by the drive microprocessor, information is sent to the microprocessor by an electromagnetic pickup near the gear mounted on the drive motor shaft. This digital servo mechanism, controlled by the microprocessor, eliminates all potentiometer adjustment points, reduces total power consumption and significantly improves speed control.

**Tape-to-head contact:** Using a single-gap, read/write tape head, the HCD-75 applies maximum pressure at the critical point where information passes between the tape and head. This pressure feature sharply reduces the chances that debris can come between the tape and head and cause the accidental loss of information (a separation loss or dropout).



**FIG. 1 HCD-75 Drive Module**

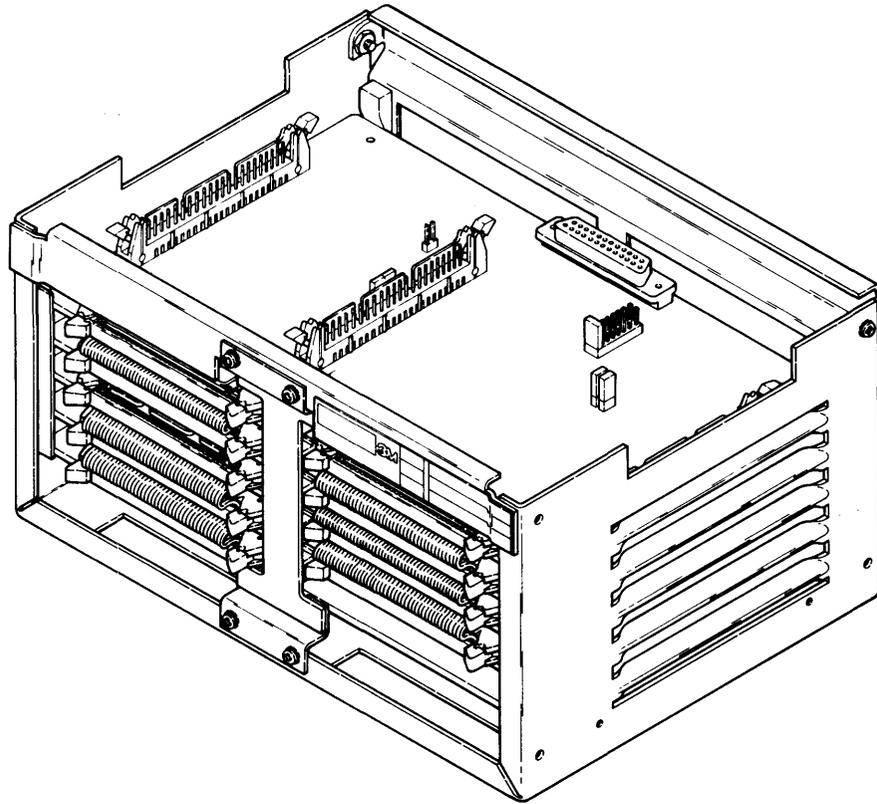
**Tape head positioning:** In the HCD-75 drive module, a stepper motor accurately aligns the gap of the tape head with the track location on the tape. Each step of the motor causes only 0.78 milli-inch (.00078 inch) of head travel, which allows highly accurate alignment of the head and tape track. The stepping head design of the HCD-75 completely eliminates all maintenance adjustments for head position.

**Read/write electronics:** The HCD-75 microprocessor automatically sets amplifier gain when a data cartridge is inserted into the drive.

#### **HCD-75 CONTROLLER MODULE**

Mechanically, the controller module of the HCD-75 is a 5-card pc assembly that acts as the digital data channel and control center for the entire HCD-75 system. Control of the system is exercised through a microprocessor, which has been programmed to execute the following basic control functions:

1. Issue appropriate motion commands to the drive module,
2. Coordinate all timing considerations within the data channel electronics,
3. Interlock motion commands with activity in the data channel, and
4. Perform all error detection and correction functions during read and write operations, without involving the host computer.



**FIG. 2 HCD-75 Controller Module**

**Controller Description:** The major tasks performed by the controller can be organized into three categories that relate directly to magnetic tape operation: write operations, read operations, and system operations. Specific tasks in each category are described below.

### **Write Operations**

During write operations, the controller performs the following tasks:

1. It controls the placement of input data into the dual 1024-byte I/O buffers.
2. It starts tape motion and monitors the block keys to locate the block to be used (as commanded by the host) and then commands the drive module to position the tape head on the track requested.
3. It either immediately writes 1024 bytes of data onto tape (if the buffer section is full when the block is located) or halts tape motion at the appropriate block (if the buffer is not full). It then restarts tape motion when a full buffer of data is present.
4. It converts the parallel data of the buffer into a serial stream.
5. It calculates Cyclic Redundancy Check Characters (CRCs) for each 256-byte frame of user data and inserts these CRCs into the bit stream.
6. It generates error correction frames 5 and 6 (along with the CRCs) and appends them onto the bit stream.
7. It encodes the data from NRZ (non-return-to-zero) format to IMFM format.
8. It precompensates the write data bit stream for peak-shift phenomena.
9. When delivering the precompensated write data, the controller:
  - a. starts tape motion,
  - b. reads the block key, and
  - c. uses the position of this key to accurately locate the position of the first data bit.

It then clocks the data stream rate in order to create a 10,000-bpi packing density within the data frames.

## Read Operations

During read operations, the controller performs the following tasks:

1. It controls operation of the drive module while searching for the desired block and track.
2. It directs the head to the appropriate track and block location to be read.
3. Accepts the serial data from the tape and reassembles the data into parallel data.
4. Performs error correction when the CRC indicates correction of the data is required.
5. Converts the IMFM data to NRZ format.
6. Controls the drive motion to read data until:
  - End of file mark is encountered
  - Both buffers are full, awaiting user to accept data.

## SYSTEM FUNCTIONS

The functions described in the following paragraphs are provided by the HCD-75 controller and may be unrelated to specific system operations of reading and writing.

### Self-Test

Upon power up, all system memory—including that in the drive module—is self-tested by running check sums. If a problem is detected during the memory test sequence, the controller sets its ATTENTION output and provides status information to the system computer. Also, the LED on the Memory board is turned on if the memory tests fail. The auto-load sequence also acts as a system self-test. After a cartridge is inserted into the drive, the controller monitors performance during the auto-load sequence that follows. If a problem is detected the controller sets the ATTENTION output and unloads the cartridge.

### Data Verification

The controller can verify—as an off-line function—the readability of information previously written. In this function, the controller reads each block of information between a specified starting address and a specified ending address to make certain that every block in that area can be reproduced accurately, either directly or by using the system error-correction method.

If the data cannot be read properly after three read retries of a block, the block number is entered into a specified area of controller memory (bad block table) and the system moves on to verify the next block.

When the controller reaches the specified ending block in the verification process, the controller attention flag is set. At this time, the host computer can interrogate the controller memory to determine how many unreadable blocks were found and what their addresses are by track and key number.

### Skip Table

If specific locations on a tape are known to be bad, the host computer may enter the addresses of those locations into an area of controller memory called a SKIP TABLE. After the locations have been entered into the table, the HCD-75 will automatically skip over the locations in subsequent operations.

### Tape Segmenting

In some applications, typical on-line storage capacity requirements might be low, but relatively fast access times are required. Tape segmenting is a means of dramatically reducing average access times by shortening the length of tape over which operations take place. In tape segmenting, the HCD-75 is programmed with a block address at which a segment begins and a stopping block address. The HCD-75 then performs desired operations on tracks 0 through 15, but only between these starting and stopping points.

## USER INTERFACE

The usual method of data transfer for the HCD-75 system is by means of a parallel interface. Serial data transfer is available, but is used almost exclusively for testing the system, not for normal operations.

### Parallel Interface

The HCD-75 system includes a fully buffered, asynchronous interface that provides maximum flexibility in connecting the system to different host interface structures. The parallel interface is a general-purpose interface that consists of:

- 16 data input lines
- 16 data output lines
- 4 control lines
- 2 data handshake lines
- 1 initialize (reset) line

The four control lines are used to set the direction of communication across the interface, to announce whether data on the 16 input lines is a command to be executed or information to be written, to initiate a transfer of data, and to interrupt operation in the event of a fault condition in the drive.

The data line options, which are implemented by means of various cabling connections, allow four possible configurations:

1. 16-bit unidirectional
2. 16-bit bidirectional
3. 8-bit unidirectional
4. 8-bit bidirectional

### Serial Interface

As a standard feature, the HCD-75 provides a serial interface port that conforms to RS232 protocol. This serial interface can be used for:

- checkout and troubleshooting
- initial product evaluation (by user)
- special prompts are available to use this port for system data transfers

### AUTO-LOAD SEQUENCE

The auto-load sequence is a series of steps that are automatically performed before a read or write operation can begin on a newly inserted data cartridge. The sequence serves the following purposes:

- Establishes proper tape tension and tape pack position within the cartridge, by automatically rewinding the tape from end to end before any read or write operation
- Assures that the head is properly positioned with respect to the tape and that the tape tension is set for accurate contact with the head
- Checks for foreign cartridge
- Sets amplifier gain by using the prerecorded keys on the tape
- Determine precisely where the physical edge of the tape is located and, using its location as a reference point, accurately locate the tape track positions.

The auto-load sequence normally begins at EOT (end of tape) but can be executed from any tape position.

### CAUTION

“File Protect” must *not* be on safe if a write operation is to be executed after an auto-load sequence is completed.

In order to set up the HCD-75 system and execute the auto-load sequence with a data cartridge, the following steps are carried out in the order listed below:

1. To begin the auto-load sequence, turn on the two power sources as follows:
  - a. Power on the +5VDC source first and allow it to stabilize (for a minimum of 100 milliseconds).
  - b. Then turn on the +12VDC power.
2. The two LEDs on the drive’s mother PC board will light. (The LED on the right is the Drive Fault light and the LED on the left is the Cartridge Fault light. Refer to Fig. 3.)

The tape head steps down until an audible chatter indicates that it is at its lowest position. The two LEDs should then go out.
3. Insert a DC600HC Data Cartridge.
4. The drive shifts the head up to the center of the tape and, at a low speed, sets the amplifier gain.
5. The drive checks, at a low speed, for a foreign cartridge.
6. The drive motor speed is checked.
7. The tape is wound to EOT (if not already there) at high speed.

8. The drive uses the edge seek routine to determine precisely the location of the tape edge and then centers the head on track 0.
9. The tape is rewound to BOT at high speed.
10. The drive resets the gain, at a low forward speed.
11. The drive locates the edge of the tape and centers the head on track 0.
12. While tape motion has stopped, the head moves to track 15.
13. The drive locates the edge of the tape and centers the head on track 0.
14. The drive checks the repeatability of the head stepper assembly. (If stepper counts are incorrect, steps 13 through 15 will be repeated.) The stepper motor is accurate to within one stepper position and there are 19 positions from the center of one track to the center of the next track.

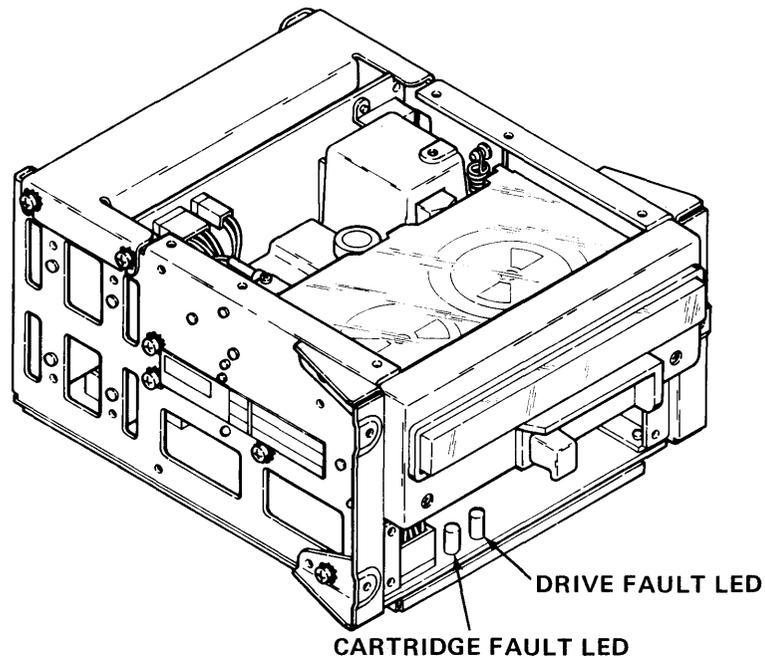
15. The drive locates the head on track 0.
16. The tape is rewound to BOT at high speed.
17. At BOT, on track 0, the system is ready for operation.

Execution time for the auto-load sequence is:

	<b>60 IPS</b>	<b>30 IPS</b>
DC600HC	1 min. 45 sec.	DC600HC 2 min. 33 sec.
DC615HC	45 sec.	DC615HC 1 min. 0 sec.

**NOTE**

Assumes starting from EOT.



**FIG. 3 Drive Module**

# DC600HC AND DC615HC HIGH CAPACITY DATA CARTRIDGE PRERECORDED FORMAT

## GENERAL INFORMATION

The DC600HC and DC615HC are 1/4" tape data cartridges used for high capacity digital data storage. The DC600HC cartridge contains 600 feet of tape for user data, the DC615HC cartridge has 150 feet of tape for user data. High capacity is achieved by:

- Using an improved magnetic coating to optimize recording properties for high flux densities.
- Using thin tape to increase the length possible in the cartridge.
- Using a prerecorded format so as to reduce the gap size needed between records.
- Using a stepping head to give 16 tracks of data on the cartridge.

The physical form of the DC600HC and DC615HC are similar to the DC300 data cartridge described in ISO 4057, ECMA 46 and ANSI X3.55 which are referred to as STANDARDS in this cartridge description.

## PRERECORDED FORMAT

The cartridge is prerecorded in production with a full width recording head which writes completely across the full one-quarter inch width of tape. The tape length is divided into three areas. These are an EOT area, a recording area, and a BOT area. The recording area of the DC600HC is divided into 4114 blocks (DC615HC is divided into 1042 blocks) which are separated by prerecorded keys. See figure 4 below.

## CARTRIDGE "SIZING"

For system implementation of cartridge sizing and more detail concerning tape segmenting, see the Data Control section.

**PHYSICAL END AREA**—The physical end of tape areas are erased and thus contain no recorded signals.

**BOT AREA**—The BOT area contains the recorded BOT pattern consisting of recorded areas of 5,000 frpi (197 frpmm) signal alternating with erased areas.

**EOT AREA**—The EOT area contains the recorded EOT pattern which is a continuous 5,000 frpi (197 frpmm) recorded signal.

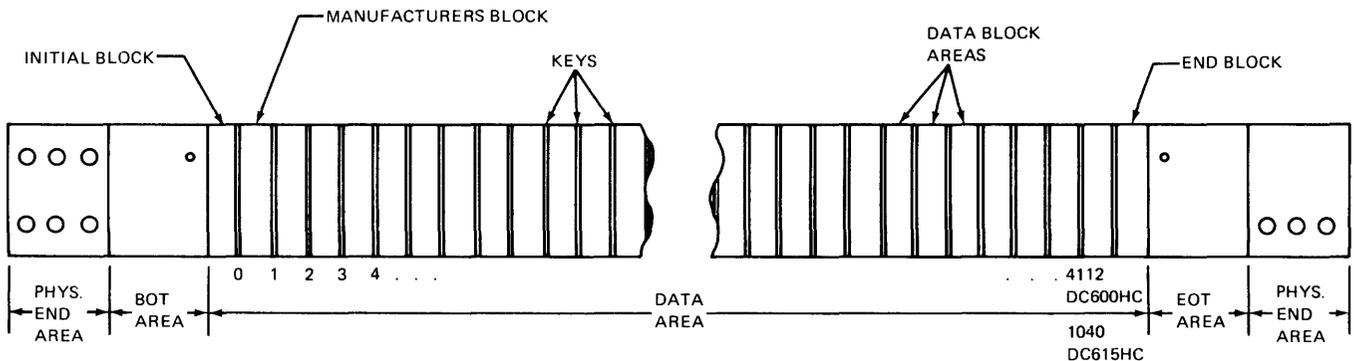
**DATA AREA**—The data area is located between the BOT area and the EOT area, consisting of data block areas each separated by keys.

**INITIAL BLOCK**—The initial block is an erased length of tape nominally 1.764 inches (44.81 mm), which separates the BOT pattern from the first key.

**END BLOCK**—The end block is an erased length of tape nominally 1.764 inches (44.81 mm), which separates the EOT pattern from the last key.

## NOTE

DC300A or DC300XL Cartridges will not operate in the HCD-75 System.



**FIG. 4 Prerecorded Format**

**MANUFACTURERS BLOCK**—Absolute block 0000. The data is recorded in ASCII (the parity bit is set to zero). Line 1 is the cartridge type. Line 2 is the number of user data blocks per track. Line 3 is a copywrite notice. And line 4 is the cartridge identification code.

Example. <CR><LF>  
 DC600HC <CR><LF>  
 4096 <CR><LF>  
 FORMAT <C> 1980, MINN. MINING and MFG.  
 CO. <CR><LF>  
 XXXXXXXXXXXXXXXX <CR><LF>  
 <ESC>

**NOTE**

The Manufacturers block must not be overwritten.

**KEY**—A recorded signal containing a unique number to identify a location along the length of the tape.

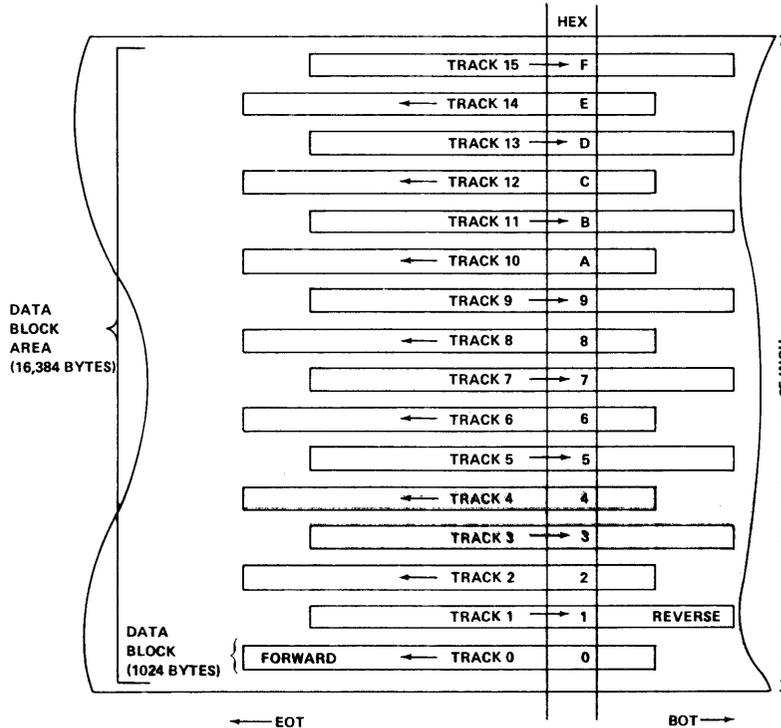
**DATA BLOCK AREA**—A space between keys reserved for recorded data blocks. The data block area is identified by the key which precedes it.

**DATA BLOCK**—User recorded data within a data block area.

**FORWARD KEY**—A key which is readable, least significant bit first, when moving in the forward direction of tape travel.

**REVERSE KEY**—A key which is readable, least significant bit first, when moving in the reverse direction of tape travel.

**IMFM**—The method of recording used to encode the key numbers. It is an abbreviation meaning Inverted Modified Frequency Modulation.



Media is .25 inch wide. Note the difference between data block and data block area. Above format is identical on both DC600HC and DC615HC data cartridges.

**FIG. 5 Track Format**

## RECORDED FORMAT

The Recorded Format defines how data is recorded on a DC600HC or DC615HC data cartridge under control of the HCD-75 system. Two methods of addressing data are available in the HCD-75, Absolute and User block addressing. Refer to the paragraph Absolute Addressing in the Data Controls Section.

**TRACK FORMAT**—In order to reduce access time and make the tape appear to be 16 times longer, serpentine recording is used. In this mode all even numbered tracks are read in the forward direction, and the odd numbered tracks are read in the reverse direction. The most significant Hex digit of the HCD-75 address method defines the track starting with track 0 near the bottom edge of tape. Figure 5 details how a data block area between keys is divided up into 16 tracks.

**ABSOLUTE KEYS**—The absolute keys are the numbers recorded on tape at the time of manufacture. The hex key numbers run from 0000 at BOT to 1010 at EOT (0000 to 0410 on a DC615). Refer to Figure 6 for details of data block area uses. Refer to the section on Absolute Addressing in the Data Controls section for details on absolute addressing of keys versus user addressing.

**DIAGNOSTIC BLOCKS**—Data block areas 1 through 5 are reserved for system diagnostic activity and manufacturing check-out. These blocks are not specifically defined and should not be used.

**SYSTEM BLOCKS**—The system blocks at the BOT end of the cartridge may be used to store permanent data relevant to the particular data cartridge. Such information as a bad location (Skip Table), error rate performance, file locations and so on may be stored in these data block areas. There are no accepted standards for use of these areas. However, many users have chosen the absolute data block area between key numbers 8 and 9 as the location of the skip table. The table may be written more than once to insure recovery. Absolute address 8 on all forward tracks and address 9 on reverse tracks could be used.

The system blocks at the end of tape are not accessible by the HCD-75 system.

## WARNING

Do not overwrite Absolute block 0000; this is the Manufacturers block and must be left intact.

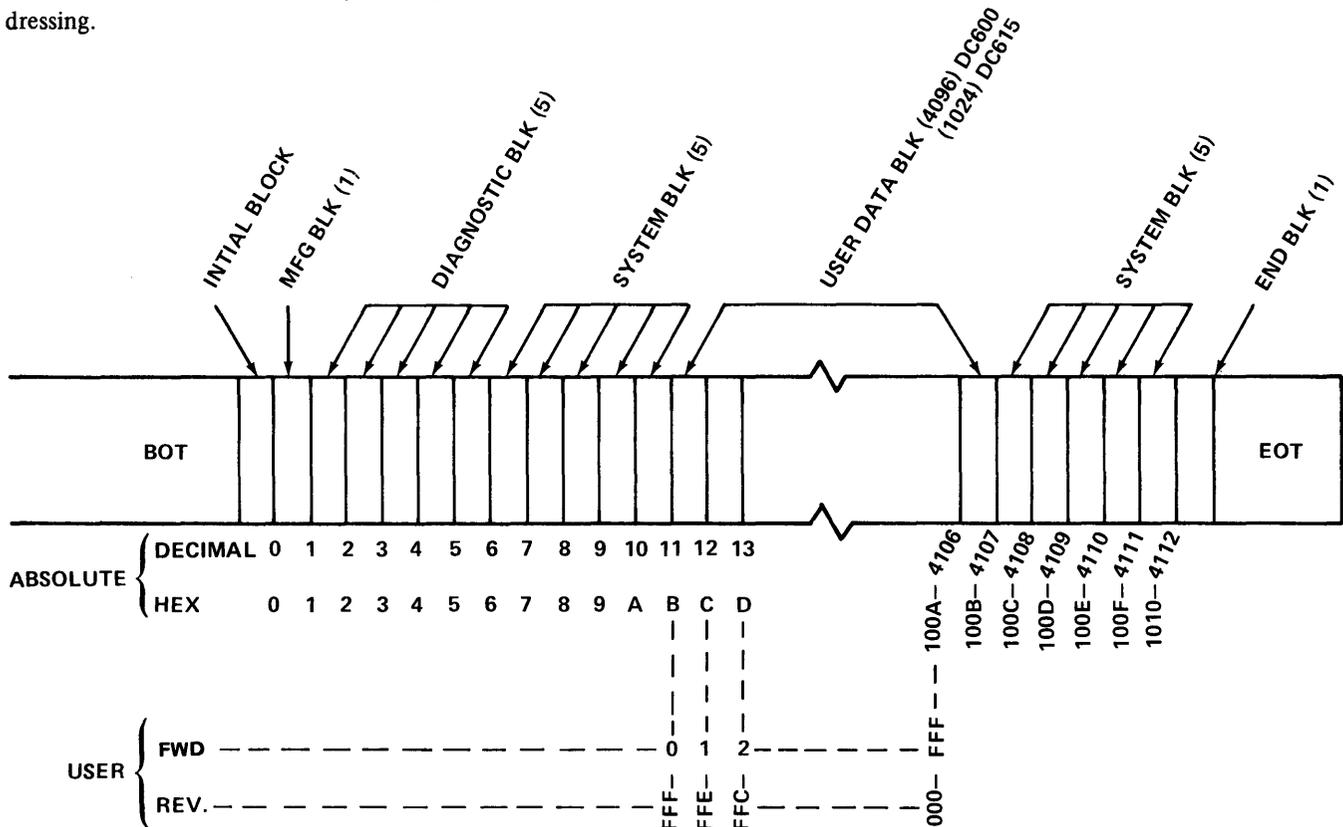


FIG. 6 DC600HC Data Blocks

**USER DATA BLOCKS**—There are 4096 user data block areas in a DC600HC and 1024 areas in a DC615HC. Dividing the areas up by 16 tracks gives 65,536 or 16,384 data blocks respectively. The normal user block address mode is used to access these blocks. The HCD-75 system interprets and translates user key numbers into the absolute key numbers on tape. User block addresses start at 000 and proceed up to FFF on each track. Forward tracks start with X000 at absolute block 00B and end with XFFF at absolute block 100A. Reverse tracks start with X000 at absolute block 100A and end with XFFF at absolute block 00B. The track is selected by the fourth digit of the address. Example OFFF selects the last user block of track 0, 1000 selects the first user block on track 1. This gives a continuous addressing from 0000 to FFFF and allows for serpentine recording.

**DATA BLOCK FORMAT**—Each data block consists of six frames: four with 256 bytes of actual data in and two with error correction data. The format of each frame is the same. See Figure 7.

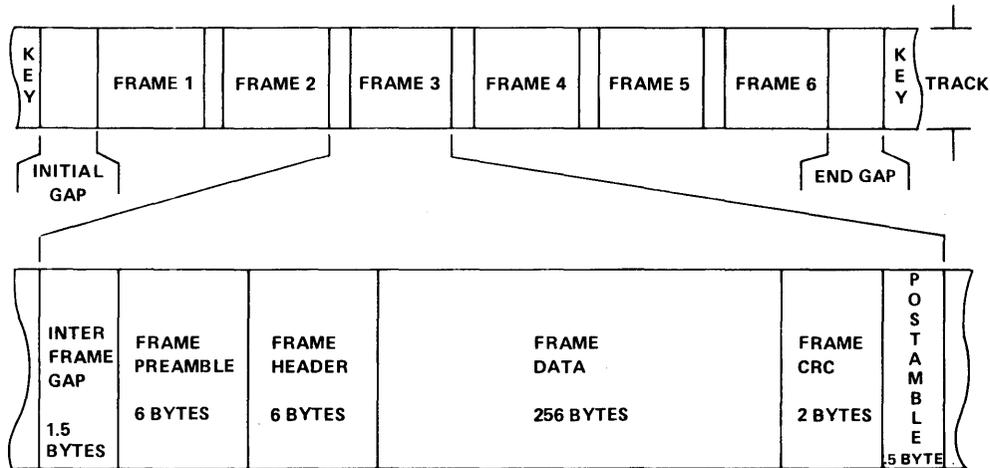


FIG. 7 DC600HC Data Block Format

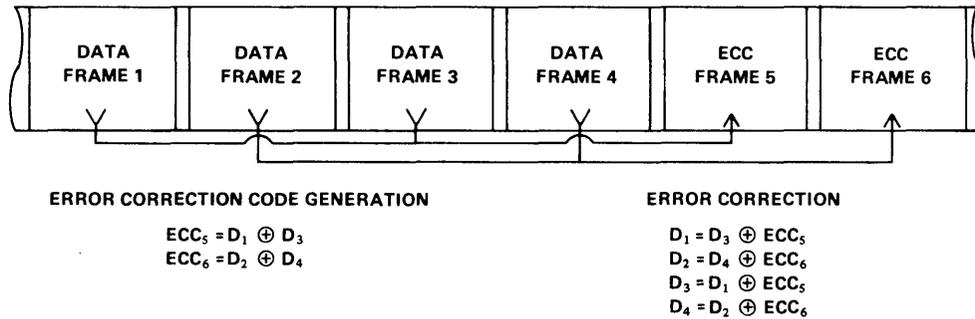
## ERROR CORRECTION

The data portion of a frame consists of 256 bytes of either actual data or error correcting data depending on the frame number.

Frame numbers 1 through 4 contain actual data. Frames five and six contain error correction data. Byte one of user data in frame one is combined with byte one of user data in frame

three to produce byte one of error correction frame five. In similar fashion bytes 2 through bytes 256 of frames 1 and 3 are combined to fill out frame 5. Frame 6 is produced by combining frames 2 and 4.

The combination process is an exclusive-or of bit b1 in each byte of user data to produce bit b1 of the corresponding error correction byte, bits b2 through b8 are combined in similar fashion. See figure 8.



**FIG. 8 Error Correction**



# PARALLEL INTERFACE OPERATION

## GENERAL

The HCD-75 controller module is connected to the host via 50 pin cables. The interface is easily adapted to any host computer.

## INTERFACE LOGIC

All Interface lines to the HCD-75 are TTL compatible with 0 to +0.8 VDC = low and +2.5 to +5.0 VDC = high. Inputs are terminated with a 220/330 ohm resistor and go to 74LS14 TTL line receivers. Outputs are 7438 TTL open collector buffers.

## INTERFACE SIGNALS

The HCD-75 interface signals and their functions are described below. Specific details about the use of the signals are presented in the sections of this document that deal with specific operations.

**DATA INPUT BUS**--Sixteen lines ( $2^0 - 2^{15}$ ) that are used to transfer commands or data to be written from the user's equipment to the HCD-75.

**DATA OUTPUT BUS**--Sixteen lines ( $2^0 - 2^{15}$ ) that are used to transfer read data or status information from the HCD-75 to the user's equipment.

**COMMAND/DATA**--An input to the HCD-75 that is used to indicate whether information on the input bus is a command to be executed or data to be written. It is set high to indicate a command input, and set low to indicate a data transfer. This line must be set before the READY signal (described below) goes low and must not be changed until READY returns to high.

**INPUT/OUTPUT**--An input to the HCD-75 that is used to control the direction of transfers between the user's equipment and the HCD-75. This line is set high to send commands or data to the HCD-75, and is set low to send data or status in the opposite direction, from the HCD-75 to the user's equipment. This line must be set before the READY signal goes low and must not be changed until READY returns to high. When the command mode has been established by the COMMAND/DATA line, the INPUT mode must be selected by this line.

**READY**--An input to the HCD-75 that is set low when the user's system is initiating a data transfer. To end the transfer, READY is returned to high. READY must also be held high during power-up, reset, or initialization. The COMMAND/DATA and INPUT/OUTPUT lines must have been appropriately set at least 100 nanoseconds before setting READY low. The Controller will not interpret a command until READY is returned high.

**INITIALIZE**--An input to the HCD-75 that, when pulsed low, resets all controller interface logic, terminates any operation, and puts the HCD-75 into the ready state. The INITIALIZE pulse must be at least ten microseconds in duration if power is on. During power up the HCD-75 system is automatically initialized. The power up initialization takes approximately 400 milliseconds, do not take the INITIALIZE line low during this time.

**ATTENTION**—An output from the HCD-75 that is set low to indicate a fault condition, or, during read operations, to indicate an end-of-file mark. When the ATTENTION output goes from high to low, the user's equipment should immediately halt the transfer of data by setting the READY line high. The user's equipment should then respond to the ATTENTION output by issuing a REPORT STATUS command to the HCD-75. The ATTENTION line will then return to high.

**TRANSFER REQUEST**—An output from the HCD-75 that is set low when the HCD-75 is ready to accept a word of data during write operations or when a valid word of data is present on the DATA OUTPUT BUS (described below) during a read operation. This line is set high after the TRANSFER ACKNOWLEDGE input goes high. This line stays high for approximately 500 nanoseconds and then returns low, waiting for the user to process the next word of data.

**TRANSFER ACKNOWLEDGE**—An input to the HCD-75 that must go high when a valid word of data has been placed on the DATA INPUT BUS (described below) during write operations, or when the user's equipment has captured the word of data on the DATA OUTPUT BUS (described below). The TRANSFER ACKNOWLEDGE line is set low after TRANSFER REQUEST goes high. During write operations, the line should go high no sooner than 100 nanoseconds after the word to be written has been placed on the DATA INPUT BUS. This line is to be low when READY is taken from high to low.

**BYTE 1**—An input to the HCD-75 that is used only in the 8 bit configurations. This line is used to clock the lower byte of a two byte word for commands words or data across the interface.

**BYTE 2**—An input to the HCD-75 that is used only in 8 bit configurations. This line is used to clock the upper byte of a two byte word for commands words or data across the interface.

## RESET

RESET occurs on power-up and performs the following functions:

- Checks memory (PROMs and RAMs).
- Clears all RAMs (buffers A and B).
- Clears skip table and bad-block table.
- Clears frame error accumulations.

It then sets 232D and 232F to three read retries and three key retries, and sets the cartridge limits to 0000 starting data and 0FFF ending data block at locations 2323 and 2324. (Addresses are HEX.)

The user may change the starting and ending blocks (Segmenting) and if desired can change the retry counts.

A reset by means of J5 jumper (that is, by momentary removal of this jumper), which is located on the controller interface (top PC board), will regain control of the system without powering-down the controller. This type of reset will not execute an auto-load of the drive and cartridge, but will require the reestablishment of memory locations.

## DATA TRANSFERS

The transfer of information between the HCD-75 and the user's equipment is carried out in units of 16-bit words (2 parallel bytes) by way of dual, 1024-byte buffer memories in the controller module. The use of two buffers permits asynchronous operation, which occurs in the following way:

- During write operations, the user communicates with the first half of the buffer (buffer A) until that buffer is full.
- The controller then switches the user's input to the second half of the buffer (buffer B) and, at the same time, empties buffer A to tape.
- When buffer B is full, the user's input is switched back to buffer A, and so forth, until the entire file has been transferred and written on tape.

Read operations proceed in a similar way.

The optimum data transfer rate is achieved by maintaining continuous tape motion, and is determined by the rate at which the drive module is able to empty or fill the buffer sections of the controller. An average data transfer rate of approximately 35 kilobytes/second (17.5 kilowords/second) between the user's equipment and the HCD-75 will create continuous tape motion on 60 IPS units. For 30 IPS units an average data rate of 17.5 kilobytes/second gives continuous tape motion. The maximum transfer rate between the HCD-75 and the user's equipment is 2.67 megabytes/second and occurs in bursts to/from buffers A and B.

Transfers between the user's equipment and the HCD-75 occur in four different operating modes:

1. the transfer of functional commands to the HCD-75,
2. the transfer of write data to the HCD-75,
3. the transfer of read data from the HCD-75, and
4. the transfer of status information from the HCD-75.

These operating modes are described in detail in the following sections.

**CONNECTOR PIN ASSIGNMENTS  
CONNECTOR P7**

PIN	FUNCTION
1	TRANSFER REQUEST
3	TRANSFER ACKNOWLEDGE
13*	BYTE 1
15	DATA OUTPUT,BIT 2 <sup>0</sup>
17	DATA OUTPUT,BIT 2 <sup>1</sup>
19	DATA OUTPUT,BIT 2 <sup>2</sup>
21	DATA OUTPUT,BIT 2 <sup>3</sup>
23	DATA OUTPUT,BIT 2 <sup>4</sup>
25	DATA OUTPUT,BIT 2 <sup>5</sup>
27	DATA OUTPUT,BIT 2 <sup>6</sup>
29	DATA OUTPUT,BIT 2 <sup>7</sup>
31*	BYTE 2
33	DATA OUTPUT,BIT 2 <sup>8</sup>
35	DATA OUTPUT,BIT 2 <sup>9</sup>
37	DATA OUTPUT,BIT 2 <sup>10</sup>
39	DATA OUTPUT,BIT 2 <sup>11</sup>
41	DATA OUTPUT,BIT 2 <sup>12</sup>
43	DATA OUTPUT,BIT 2 <sup>13</sup>
45	DATA OUTPUT,BIT 2 <sup>14</sup>
47	DATA OUTPUT,BIT 2 <sup>15</sup>
49	ATTENTION
50	INITIALIZE
ALL EVEN PINS No's. 2 through 42	COMMON

\*8-bit configurations only

**CONNECTOR PIN ASSIGNMENTS  
CONNECTOR P8**

PIN	FUNCTION
5	INPUT/OUTPUT
7	COMMAND/DATA
9	READY
15	DATA INPUT,BIT 2 <sup>0</sup>
17	DATA INPUT,BIT 2 <sup>1</sup>
19	DATA INPUT,BIT 2 <sup>2</sup>
21	DATA INPUT,BIT 2 <sup>3</sup>
23	DATA INPUT,BIT 2 <sup>4</sup>
25	DATA INPUT,BIT 2 <sup>5</sup>
27	DATA INPUT,BIT 2 <sup>6</sup>
29	DATA INPUT,BIT 2 <sup>7</sup>
33	DATA INPUT,BIT 2 <sup>8</sup>
35	DATA INPUT,BIT 2 <sup>9</sup>
37	DATA INPUT,BIT 2 <sup>10</sup>
39	DATA INPUT,BIT 2 <sup>11</sup>
41	DATA INPUT,BIT 2 <sup>12</sup>
43	DATA INPUT,BIT 2 <sup>13</sup>
45	DATA INPUT,BIT 2 <sup>14</sup>
47	DATA INPUT,BIT 2 <sup>15</sup>
ALL EVEN PINS No's. 2 through 42	COMMON

NOTE: All unassigned pins must float.

## DATA LINE OPTIONS FOR VARIOUS CABLING CONNECTIONS

### 16-Bit Unidirectional

The standard configuration, 16-bit unidirectional, operates as two separate 16-bit data buses for communication of data, commands, and status information over two 50 conductor cables. This configuration is illustrated by the drawing and the circuit requirements (Fig. 9 and 10).

As the illustration shows, the bus for transfers into the HCD-75 is in the Data In interface cable (connector P8 on the interface p.c. board). The bus for transfers out of the HCD-75 is in the Data Out interface cable (connector P7 on the interface p.c. board).

At the host side of the interface, all data lines driven by the HCD-75 system must be terminated with 220-ohm resistors to +5V and with 330-ohm resistors to ground. In addition, all lines to the HCD-75 system must be driven by devices capable of sinking 24 milliamps to ground. The HCD-75 drives all lines with 7438 TTL-type open collector drivers. See figure 10 16-Bit Unidirectional circuit.

Shorting jumper plugs must be placed between pins 2 and 3, 4 and 5 of J2.

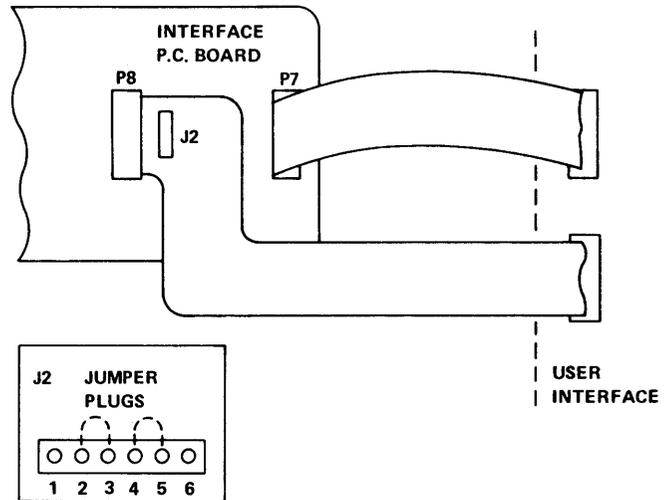


FIG. 9 16-Bit Unidirectional

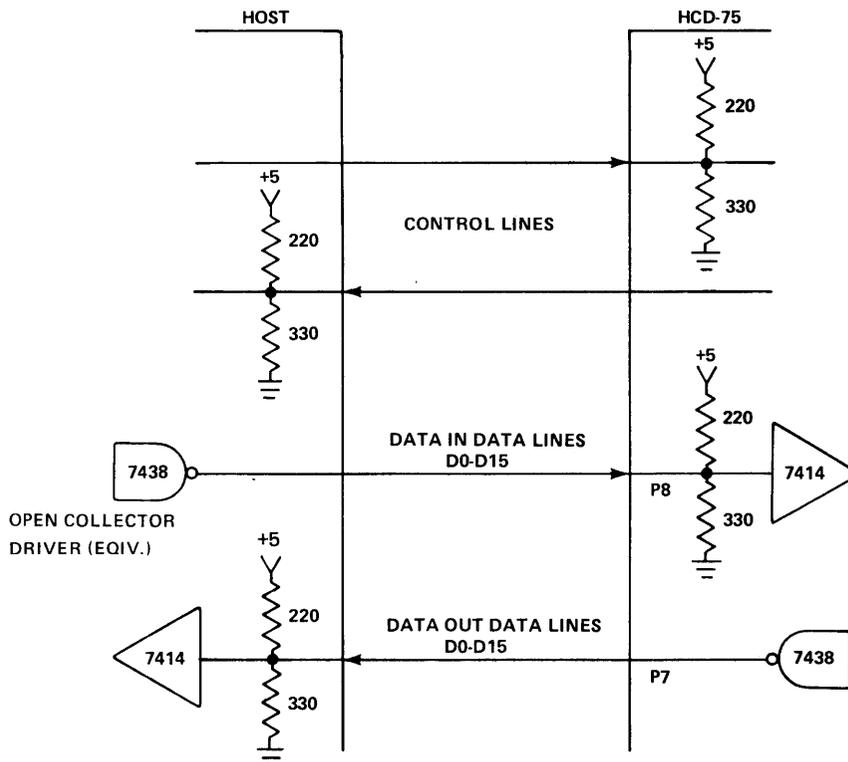


FIG. 10 16-Bit Unidirectional Circuit

## 16-Bit Bidirectional

The 16-bit bidirectional configuration provides for communication of data, commands, and status information over one 16-bit bidirectional data bus. This configuration operates in the same way as the standard 16-bit unidirectional configuration, differing only in the type of cable hook-up required. As shown below, in this mode only one 50 conductor cable is used, daisy-chaining connectors P7 and P8 (Fig. 11).

This cabling configuration connects the 16 open collector output drivers of the output cable (connector P7) to the 16 input receivers of the input cable (connector P8) on the

system, in this way forming a 16-bit bidirectional bus. See figure 12 16-Bit Bidirectional Circuit.

Due to the double 220/330 ohm termination resistors a line drive such as a 7438 capable 48 milliamps of current must be used.

Shorting jumper plugs must be placed between pins 2 and 3, 4 and 5 of J2.

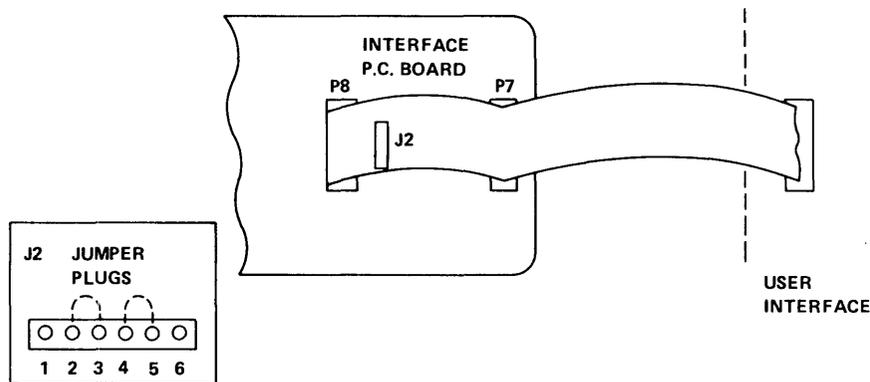


FIG. 11 16-Bit Bidirectional

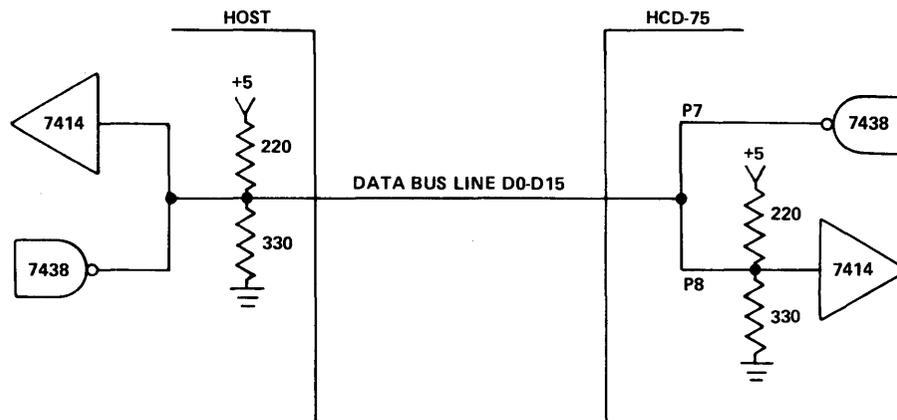


FIG. 12 16-Bit Bidirectional Circuit

## 8-Bit Unidirectional

For the 8-bit unidirectional bus mode, two separate 50 conductor cables are required, one connected to each of the interface connectors P7 and P8. To select this mode, shorting plugs should be placed between pins 1 and 2, and between pins 5 and 6, of J2 on the Controller Interface P.C. Board; as illustrated in Fig. 13.

The user 8-Bit Input Bus connects to P8 of the Interface P.C. Board where it is converted to a 16-Bit Bus by use of the Byte 1 and Byte 2 Control Lines, the 16-Bit Output Data is converted by Byte 1 and Byte 2 Control to 8-Bit Data from P7.

In this mode, each line receiver should have a termination resistor network of 220-ohm resistor to +5V and 330-ohm resistor to ground. In addition, each data line from the host should be driven by a 7438 TTL driver or by an equivalent that can sink 48 milliamps to ground. See figure 14 8-Bit Unidirectional Circuit.

To transmit data in this 8-bit mode:

- |       |   |
|-------|---|
| Read  | <ol style="list-style-type: none"><li>1. Wait for TRANSFER REQ line to go low</li><li>2. Set BYTE CONTROL 1 line high</li><li>3. Accept byte 1</li><li>4. Set BYTE 1 CONTROL line low</li><li>5. Set BYTE 2 CONTROL line high</li><li>6. Accept byte 2</li><li>7. Set BYTE 2 CONTROL line low</li><li>8. Set TRANSFER ACKN line high</li></ol>  |
| Write | <ol style="list-style-type: none"><li>1. Wait for TRANSFER REQ line to go low</li><li>2. Place byte 1 on data lines</li><li>3. Set BYTE 1 CONTROL high</li><li>4. Set BYTE 1 CONTROL low</li><li>5. Place byte 2 on data lines</li><li>6. Set BYTE 2 CONTROL high</li><li>7. Set BYTE 2 CONTROL low</li><li>8. Set TRANSFER ACKN high</li></ol> |

### NOTE

Data transfers in the 8 bit mode must always be in an even number of bytes.

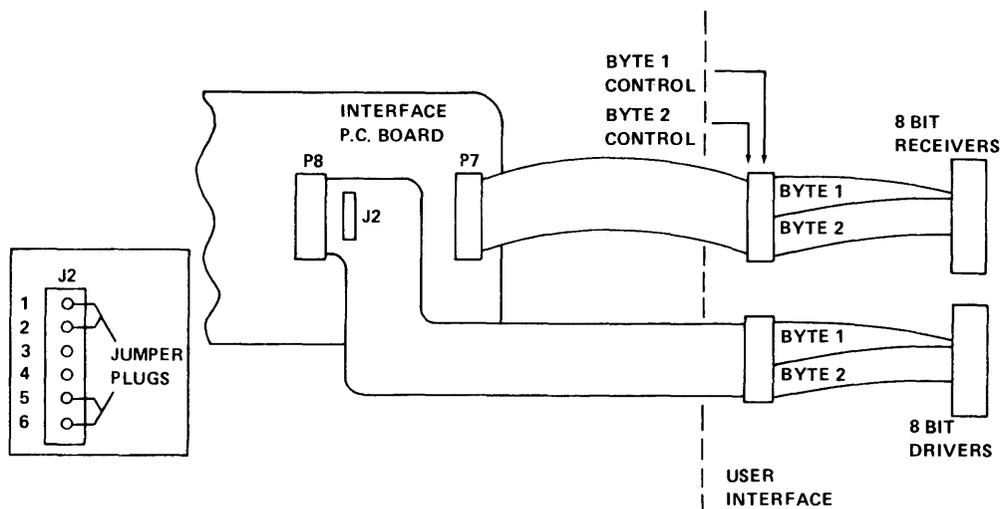


FIG. 13 8-Bit Unidirectional

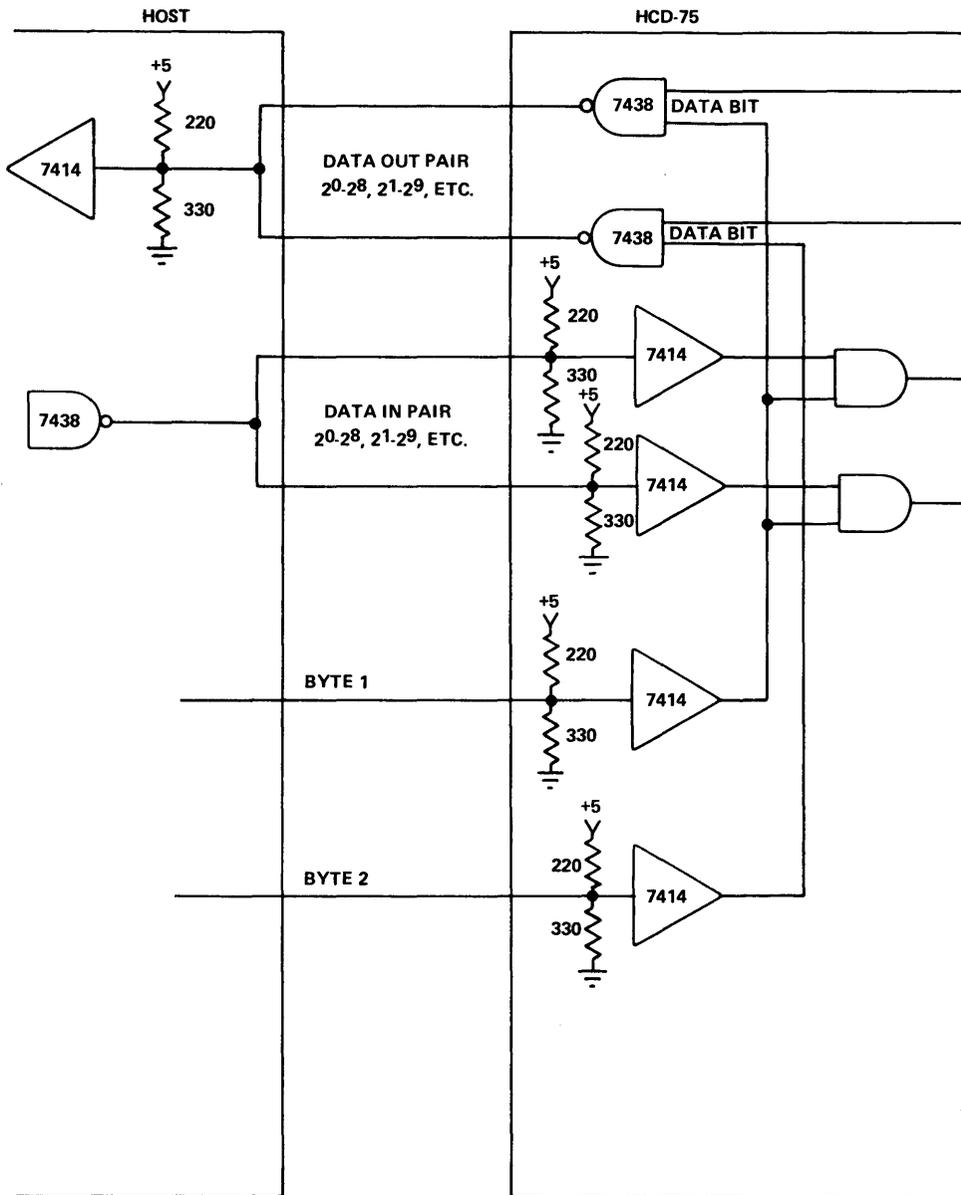


FIG. 14 8-Bit Unidirectional Circuit

## 8-Bit Bidirectional

For the 8-bit bidirectional configuration, a single 50 conductor cable is used to daisy-chain the two HCD-75 parallel interface connectors, P7 and P8, together. To select this mode, the controller interface p.c. board J2 shorting plugs should be placed between pins 1 and 2, and between pins 5 and 6, as illustrated in Fig. 15.

The 16-bit Data In bus and Data Out bus are made bidirectional by daisy-chaining connectors P7 and P8 together. The host converts the 16-bit bidirectional bus to an 8-bit bidirectional bus by using the byte 1 and byte 2 control lines to gate either byte 1 or byte 2 into or out of the host buffer elements. See 8-bit unidirectional.

In this mode, each line receiver should terminate with 220-ohms to +5V and 330-ohms to ground. In addition, the lines should be driven by 7438 TTL-type drivers or by an equivalent that can sink 48 milliamps to ground. Refer to Fig. 16.

To transmit data in this 8-bit mode:

- |       |   |
|-------|---|
| Read  | 1. Wait for TRANSFER REQ line to go low |
|       | 2. Set BYTE CONTROL 1 line high         |
|       | 3. Accept byte 1                        |
|       | 4. Set BYTE 1 CONTROL line low          |
|       | 5. Set BYTE 2 CONTROL line high         |
|       | 6. Accept byte 2                        |
|       | 7. Set BYTE 2 CONTROL line low          |
|       | 8. Set TRANSFER ACKN line high          |
| Write | 1. Wait for TRANSFER REQ line to go low |
|       | 2. Place byte 1 on data lines           |
|       | 3. Set BYTE 1 CONTROL high              |
|       | 4. Set BYTE 1 CONTROL low               |
|       | 5. Place byte 2 on data lines           |
|       | 6. Set BYTE 2 CONTROL high              |
|       | 7. Set BYTE 2 CONTROL low               |
|       | 8. Set TRANSFER ACKN high               |

### NOTE

Data transfers in the 8 bit mode must be in an even number of bytes.

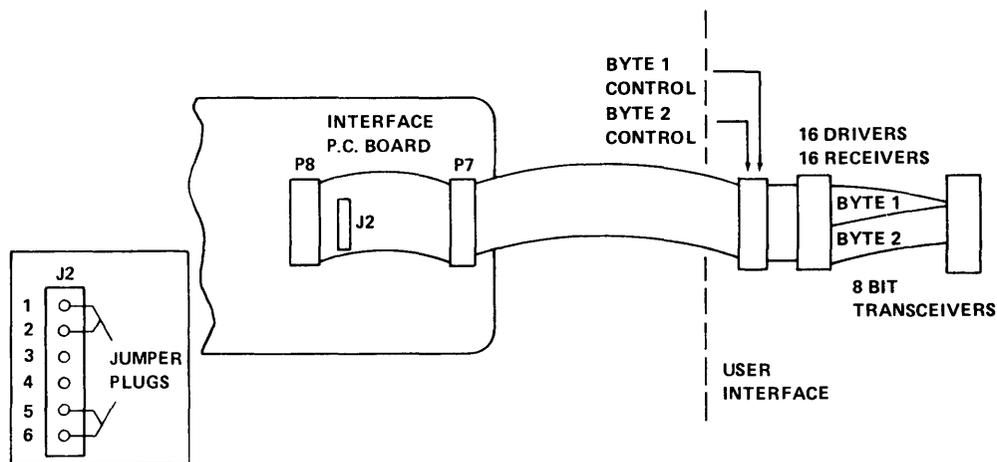
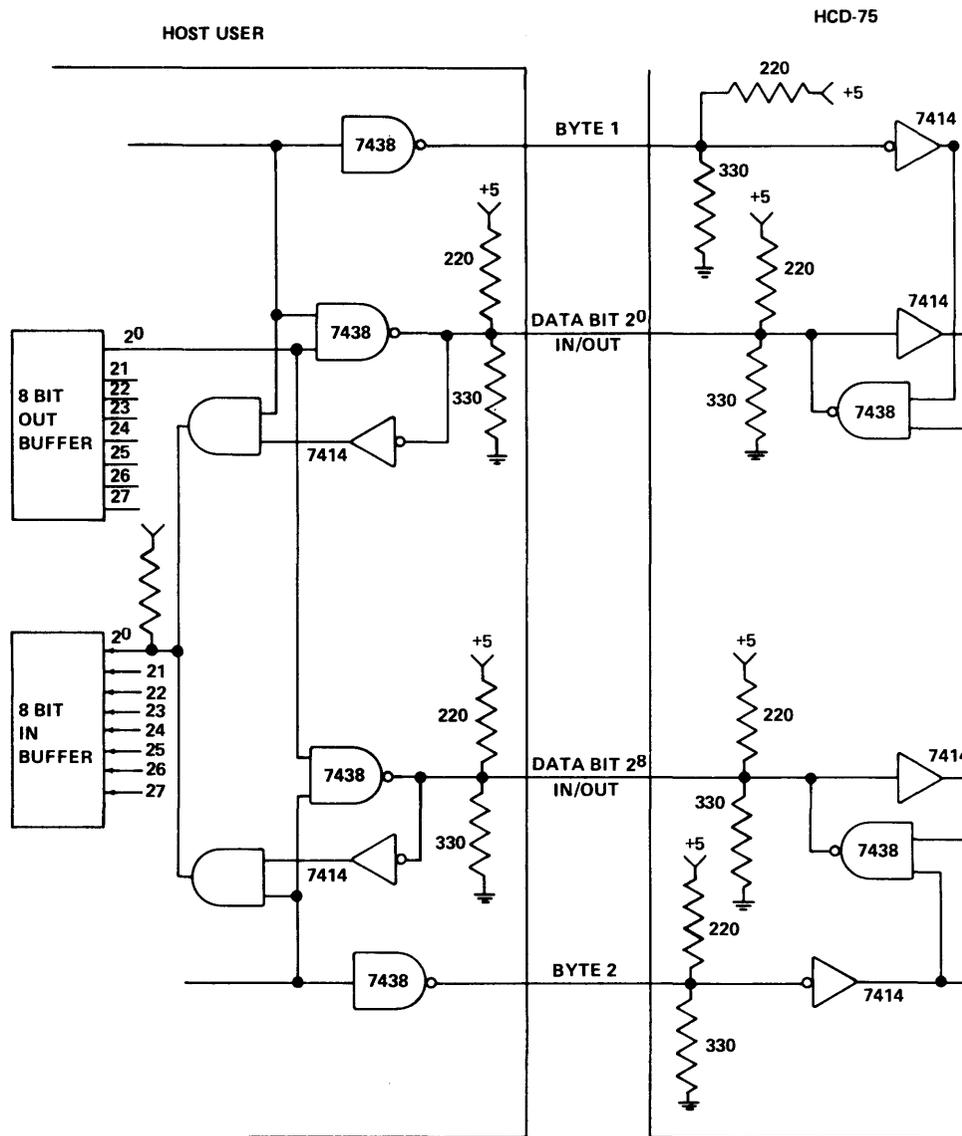


FIG. 15 8-Bit Bidirectional



**FIG. 16 8-Bit Bidirectional Circuit**

## COMMAND TRANSFER

Commands consist of from one to three 16-bit words that are transferred to the HCD-75 over the DATA INPUT BUS.

The first word contains information specifying which of the four possible drives is to be used and the function to be performed. The second and third words (when they are required)

are beginning and ending block locations, respectively, for the command functions. The following table—Command Word Structure—illustrates the organization of the command words. The various commands are defined in a later section in this document.

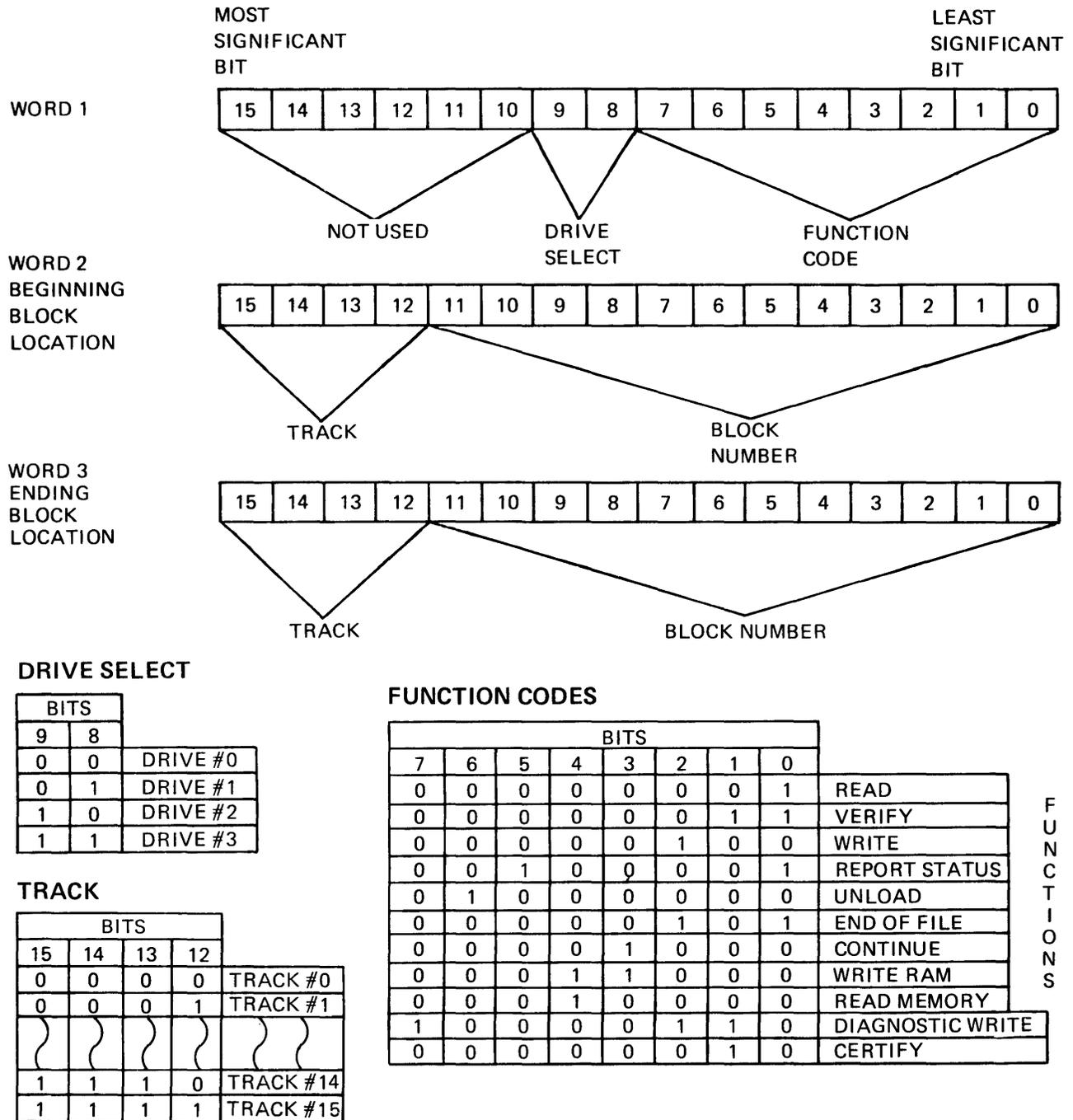


FIG. 17 Command Word Structure

To enter a command, carry out the following steps:

1. Set the INPUT/OUTPUT line high.
2. Set the COMMAND/DATA line high.
3. Set READY low after a minimum delay of 100 nanoseconds from the time when steps 1 and 2 have been completed.
4. Monitor the TRANSFER REQUEST output: when it goes low, place the first command word onto the DATA INPUT BUS.
5. Set the Transfer Acknowledge line high. This level will open the input latches and return the Transfer Request output to high, indicating that the cycle is complete. After Transfer Request goes high, return Transfer Acknowledge to low and remove the data. The maximum time that Transfer Acknowledge can remain high after Transfer Request goes high is 100 microseconds.
6. Where the commanded function requires more than one word, repeat steps 4 and 5 for the additional words.
7. When all required command words have been entered, set READY high to end the command sequence.
8. The HCD-75 assumes that all command transfers consist of three words. If a command consists of only one or two words, the HCD-75 will continue its cycle by sending a transfer request for the next word if READY has not been reset high. Setting READY high will terminate the command transfer and force TRANSFER REQUEST high.

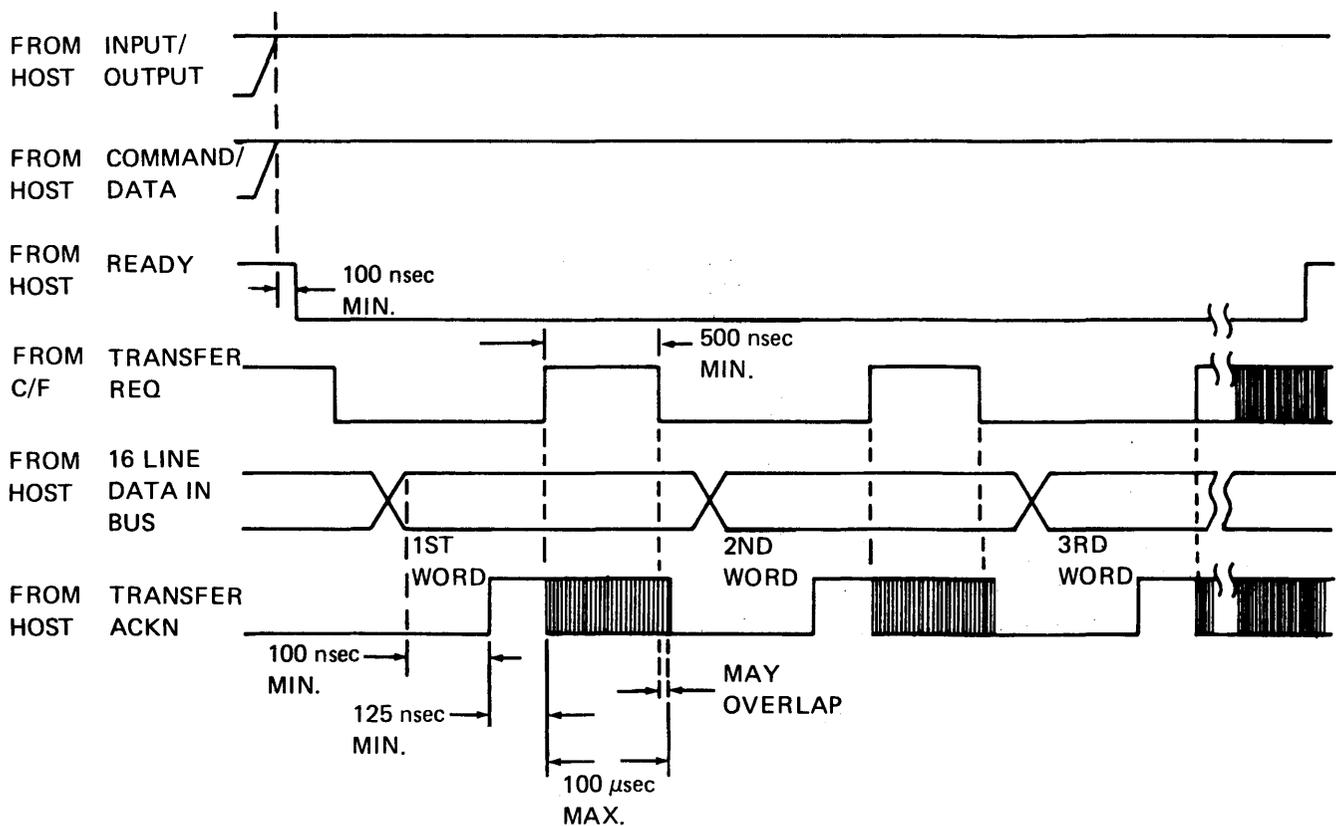


FIG. 18 Command Transfer

## BLOCK TIMING

During the transfer of a block of data Transfer Request normally is high for approximately 500 nanoseconds. At certain points during the block transfer, this time is lengthened.

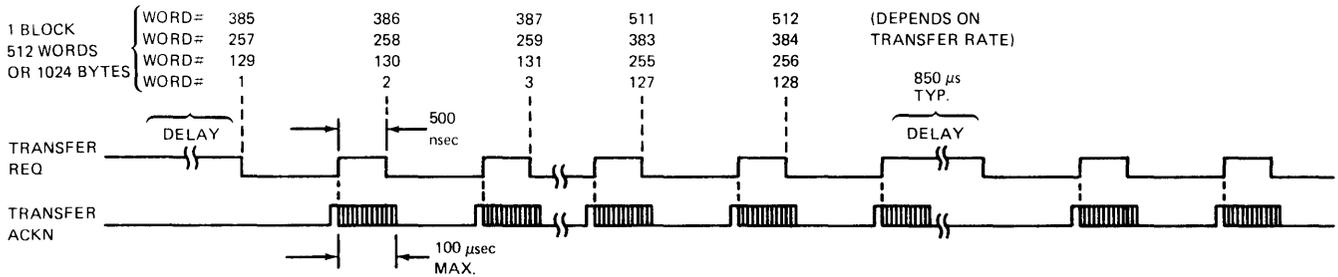


FIG. 18A Block Timing

Transfer Acknowledge being high may overlap Transfer Request going low, but Transfer Acknowledge must go low within 100 microseconds after Transfer Request goes high.

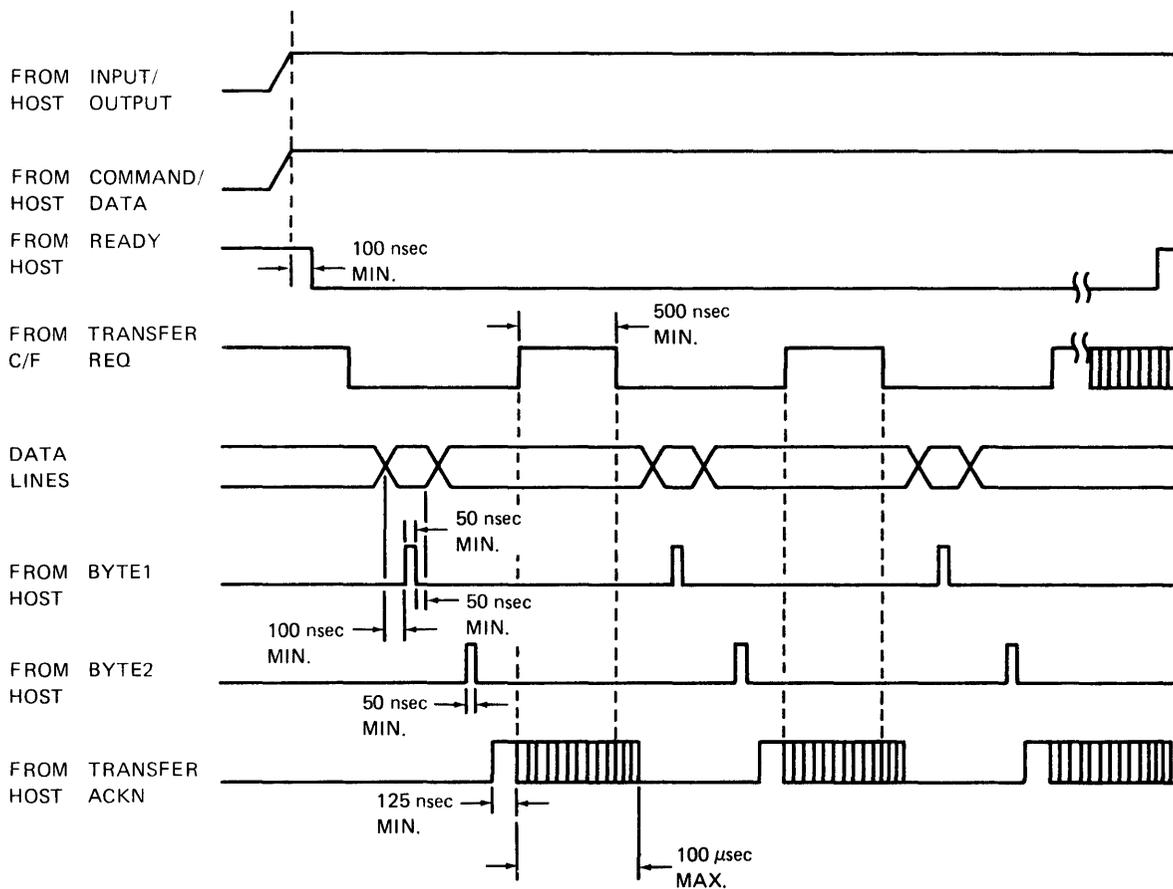
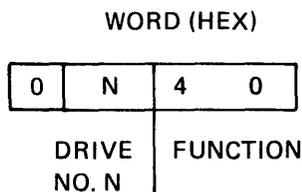


FIG. 18B 8-Bit Transfer

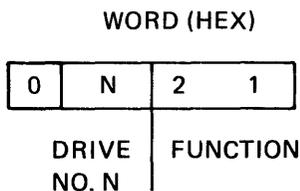
## COMMANDS

**UNLOAD**—The UNLOAD command causes the cartridge to be wound to END OF TAPE and then stopped. It also unlocks the cartridge eject lever so that the cartridge can be removed.

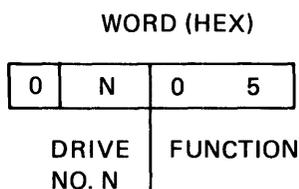


**REPORT STATUS**—The REPORT STATUS command causes the HCD-75 to report its current status as described in the section on status transfers. This command may also be used to close a write operation by completely emptying a partially filled buffer onto tape. The status is then reported as usual.

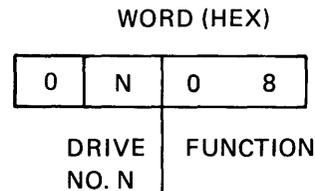
When the host has transferred the last word during a write operation, the use of a REPORT STATUS command will record the remainder of the data in the next record, complete with the character count present. Status word 3 will report the location of this last record.



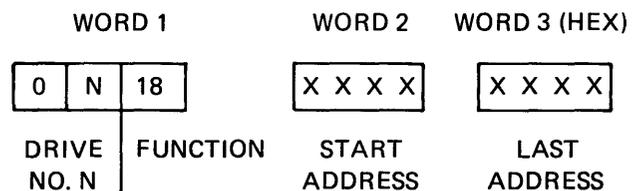
**END OF FILE**—This one-word command should be issued on completion of a write operation to completely empty a partially filled buffer onto the tape, and embed in the data header of the next block an END OF FILE mark. Each time this command is issued, a DATA BLOCK LOCATION without data will be written with the END OF FILE mark embedded in the header.



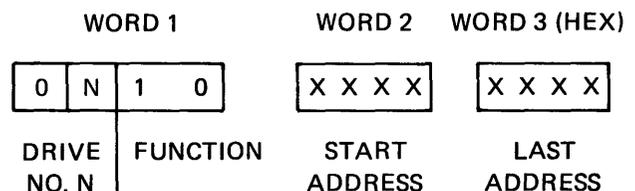
**CONTINUE**—The CONTINUE command, when issued, will cause the WRITE operation to continue in the next DATA BLOCK LOCATION after an unreadable key was detected. The CONTINUE command will cause READ to resume after it was halted due to detection of an EOF mark.



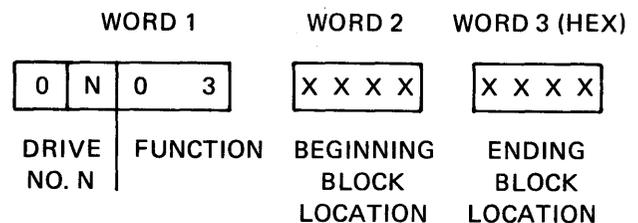
**WRITE RAM**—The WRITE RAM command is used to test the controller interface when used with the READ MEMORY command, and also to store the block location table in RAM. This three-word command will set the controller up to store information in specified RAM locations between addresses 2000 and 27FF (HEX). The information is transferred over the DATA 0-15 IN bus in the same way as a DATA TRANSFER.



**READ MEMORY**—This three word command causes the controller to transfer the contents of the specified memory locations over the DATA 0-15 OUT bus in the same way as the READ DATA TRANSFER. The limits are 2000 to 27FF (HEX).



**VERIFY**—This three-word command reads all blocks designated and checks data content against the CRC. After the function has been completed, the interface ATTN line will be set low and a REPORT STATUS Command should be issued.



**VERIFY BAD BLOCK TABLE**—After the ATTENTION output is set low followed by a REPORT STATUS command, the status word will indicate whether or not an unrecoverable error has occurred. If an error occurs the READ MEMORY command (previously described) may then be used to read the bad block location(s). Address 237F (HEX) specifies the number of bad location(s). These locations are stored in a table beginning at address 2380 (HEX). The table provides for 128 locations and can be used to build a skip table.

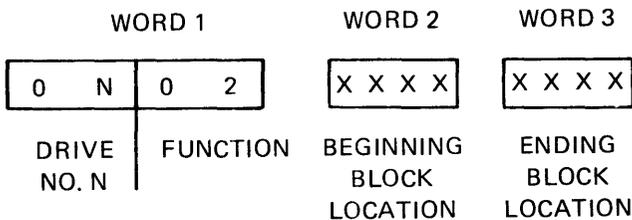
**CERTIFY COMMAND** The HCD-75 system Certify Command is a part of the standard 30 and 60 IPS controller firmware package starting with Revision 5 (30 IPS) or Revision 3 (60 IPS). The Certify Command may be used in place of the normal Verify Command to generate a table of all permanent error locations on a given cartridge. Whereas, the Verify bad block table indicates only unrecoverable data error locations, the Certify bad block table will indicate all permanent error locations, even if the error is a single frame format recoverable type error.

The bad block table for the Certify Command starts at 237F and is identical in form to the Verify bad block table. The total error table of both transient and permanent errors is located in memory starting at address 2400.

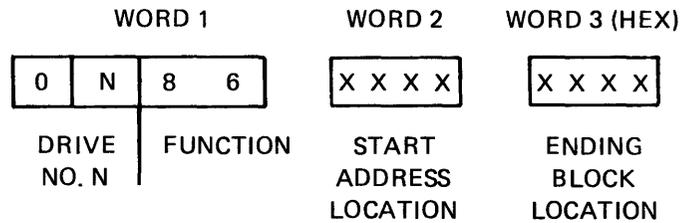
The significant difference between the Verify and Certify command is that the HCD-75 drive module read amplifier gain is lowered by 14% to test tapes to a higher performance specification.

The Certify command has three possible modes of operation. Certify data only, keys only, or both keys and data. To select the option set memory location 231E to:

- 0000—Certify Data only (Default)
- 0001—Certify Keys and Data
- 0080—Certify Keys only



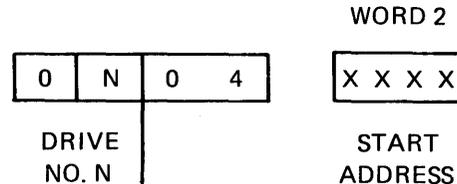
**DIAGNOSTIC WRITE**—This command writes the contents of BUFFER A in each block from the Starting Address to the Ending Address. The host sets up BUFFER A (see Memory Locations of Interest) before starting this command. Once this command is started no data transfers are needed from the host. This command is similar to the RS232 Diagnostic Write command except that the pattern written must be stored by the host in BUFFER A using a Write RAM Command.



### WRITE DATA TRANSFERS

Write data is transferred from the user's equipment to the drive in 16-bit words over the DATA INPUT BUS. Tape motion is under control of the controller module.

A write function requires a two-word command input. The first word contains the number of the drive module to be used and the write function code. The second word contains the beginning block and track number.



To write data, the following procedure is used:

1. Enter the two required command words as described.
2. After the READY input has been set high to end the command sequence, set the INPUT/OUTPUT line high.
3. Set the COMMAND/DATA line low.

4. After a minimum delay of 1 microsecond following completion of steps 2 and 3, set READY low.
5. Monitor the TRANSFER REQUEST output. When it goes low, place the first word of write data on the DATA INPUT BUS.
6. After a minimum delay of 100 nanoseconds following completion of step 5, set the TRANSFER ACKNOWLEDGE line high. After TRANSFER REQUEST goes high, return TRANSFER ACKNOWLEDGE low, and remove the data.
7. Repeat steps 5 and 6 until all write data has been transferred to the HCD-75.
8. After transferring the last word of write data, set READY high and issue either a REPORT STATUS or END OF FILE command to close the WRITE TRANSFER. This operation will cause the last data to be written on tape. The END OF FILE command is used to identify the last DATA TRANSFER as an END OF FILE.
9. To interrupt the write data transfer at any time, set READY high after TRANSFER ACKNOWLEDGE goes low.
10. The Logical End of Tape will stop the drive and set the Attention. A report status command should be issued.

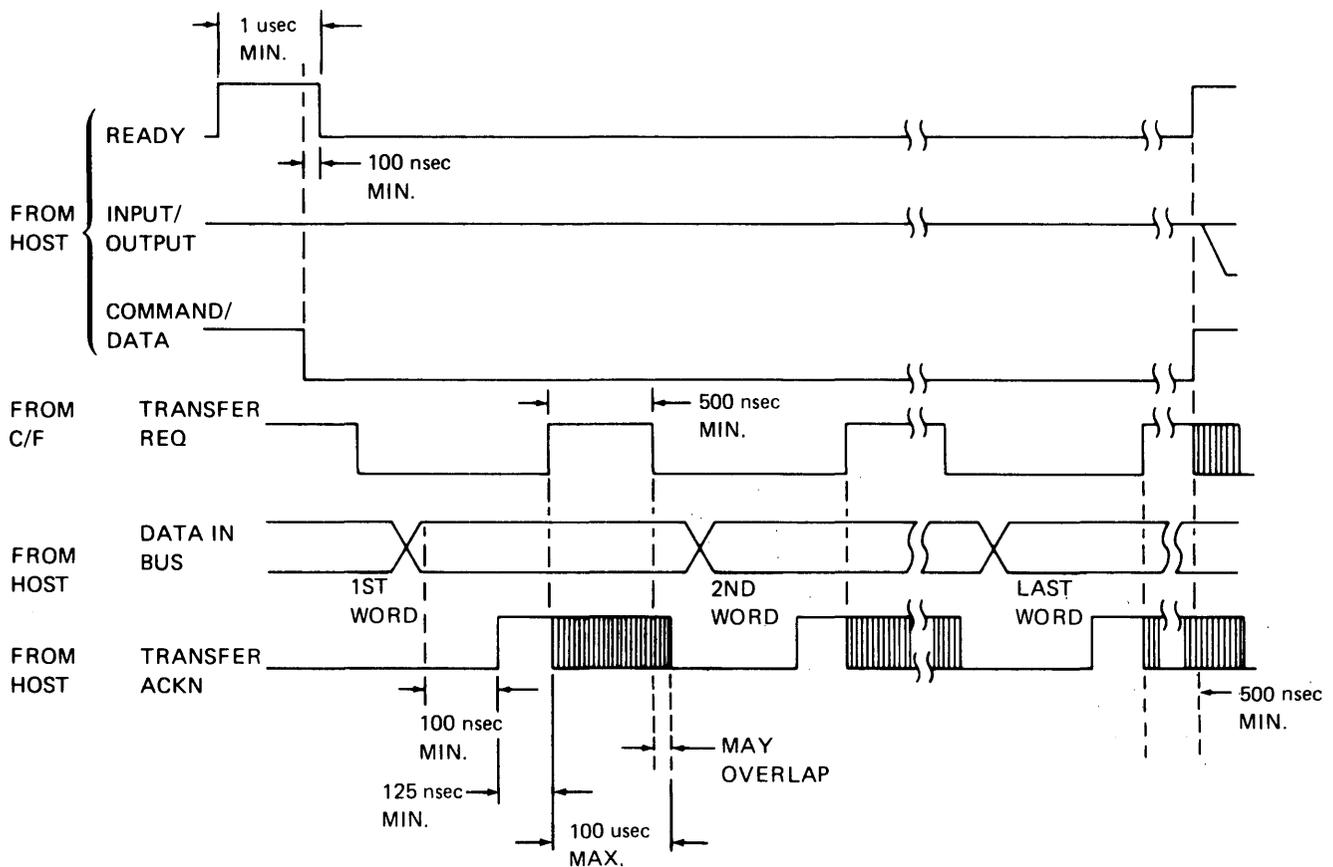
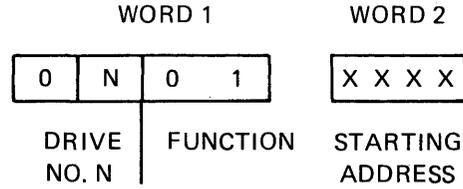


FIG. 19 Write Data Transfer

## READ DATA TRANSFERS

Read data is transferred from the HCD-75 to the user's equipment in 16-bit words over the DATA OUTPUT BUS. The operation is asynchronous and timing is controlled by the TRANSFER REQUEST and TRANSFER ACKNOWLEDGE lines. If the user's equipment is unable to respond to a TRANSFER REQUEST, the HCD-75 will stand by until the user's equipment is able to respond. If data is accepted by the user at a rate that empties one output buffer before the other has been filled, the HCD-75 will not issue the next TRANSFER REQUEST until the buffer has been completely loaded. In either event, the tape motion is automatically started and stopped, as required, under control of the HCD-75 electronics.

A read function requires a two-word command input. The first word contains the number of the drive module to be used, and the read function code. The second word contains the track and block number at which the read function is to commence.



To read data, the following procedure is used:

1. Enter the two required command words as described earlier.
2. After READY is set high to end the command sequence, set the INPUT/OUTPUT line low.
3. Set the COMMAND/DATA line low.
4. After a minimum delay of 1 microsecond following completion of steps 2 and 3 above, set READY low.

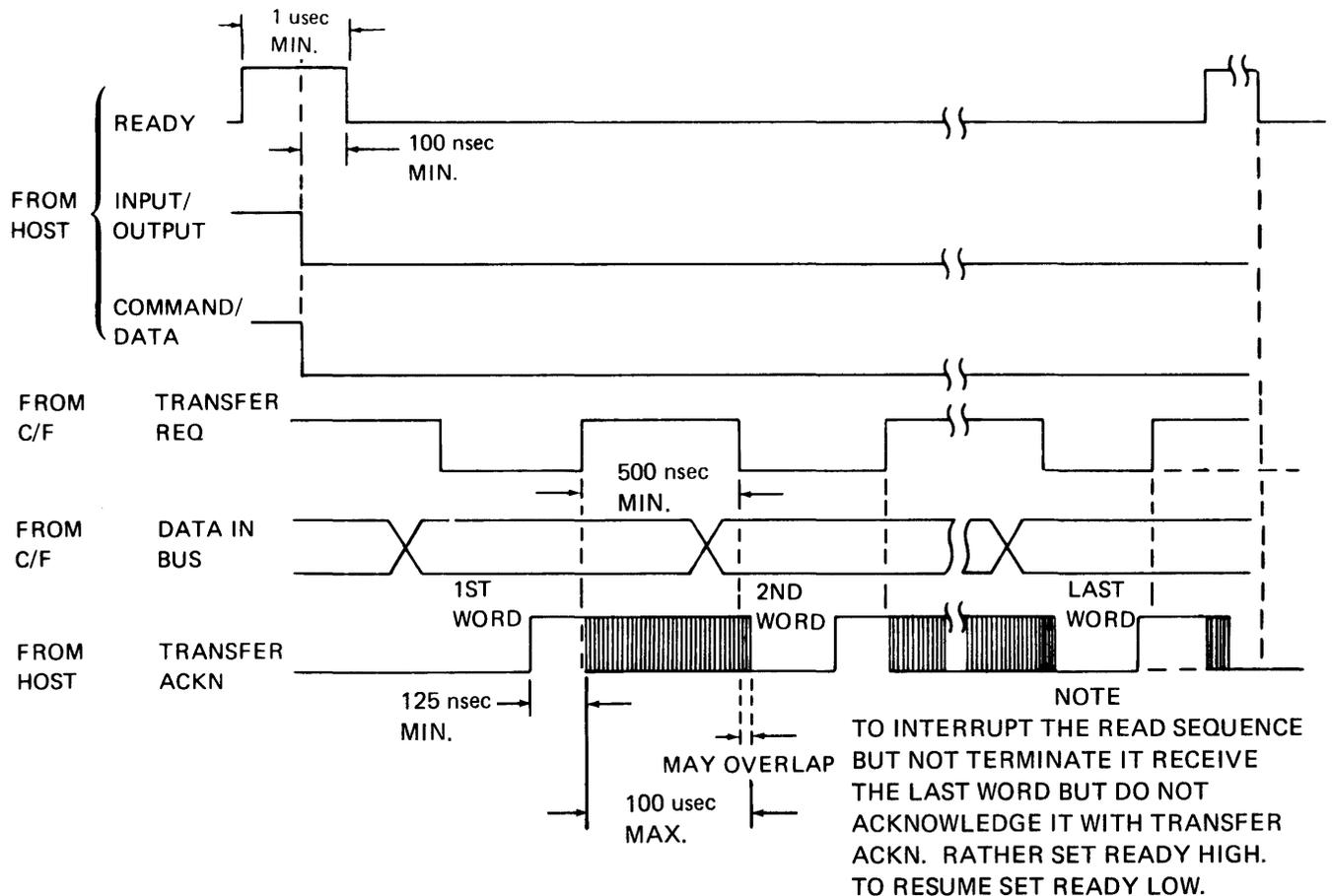


FIG. 20 Read Data Transfer

5. Monitor the TRANSFER REQUEST output. When it goes low, the first word of valid data is present on the DATA OUTPUT BUS.
6. When the user's equipment has acquired this word of data, set the TRANSFER ACKNOWLEDGE line high. The TRANSFER REQUEST line will then go high after which the TRANSFER ACKNOWLEDGE should be set low.
7. Repeat steps 5 and 6 until the required data has been read.
8. To exit from the read sequence, set the READY input high and issue a REPORT STATUS command. This command is required to properly synchronize tape position with current buffer status for subsequent operations.
9. If an END OF FILE or Logical End of Tape is detected, the read function will be halted and the ATTENTION output will be set. The user's equipment should then immediately issue a REPORT STATUS command. If the read function is to be resumed at the very next block, a CONTINUE command should be issued by the user's equipment.

#### NOTE

To interrupt data flow at any time while reading, do not send a TRANSFER ACKNOWLEDGE (i.e., do not set TRANSFER ACKNOWLEDGE high) to indicate that the last word prior to interrupt has been received. Instead, set READY high in place of the TRANSFER ACKNOWLEDGE. To resume, set READY low and wait for the next TRANSFER REQUEST and the next word.

## STATUS TRANSFERS

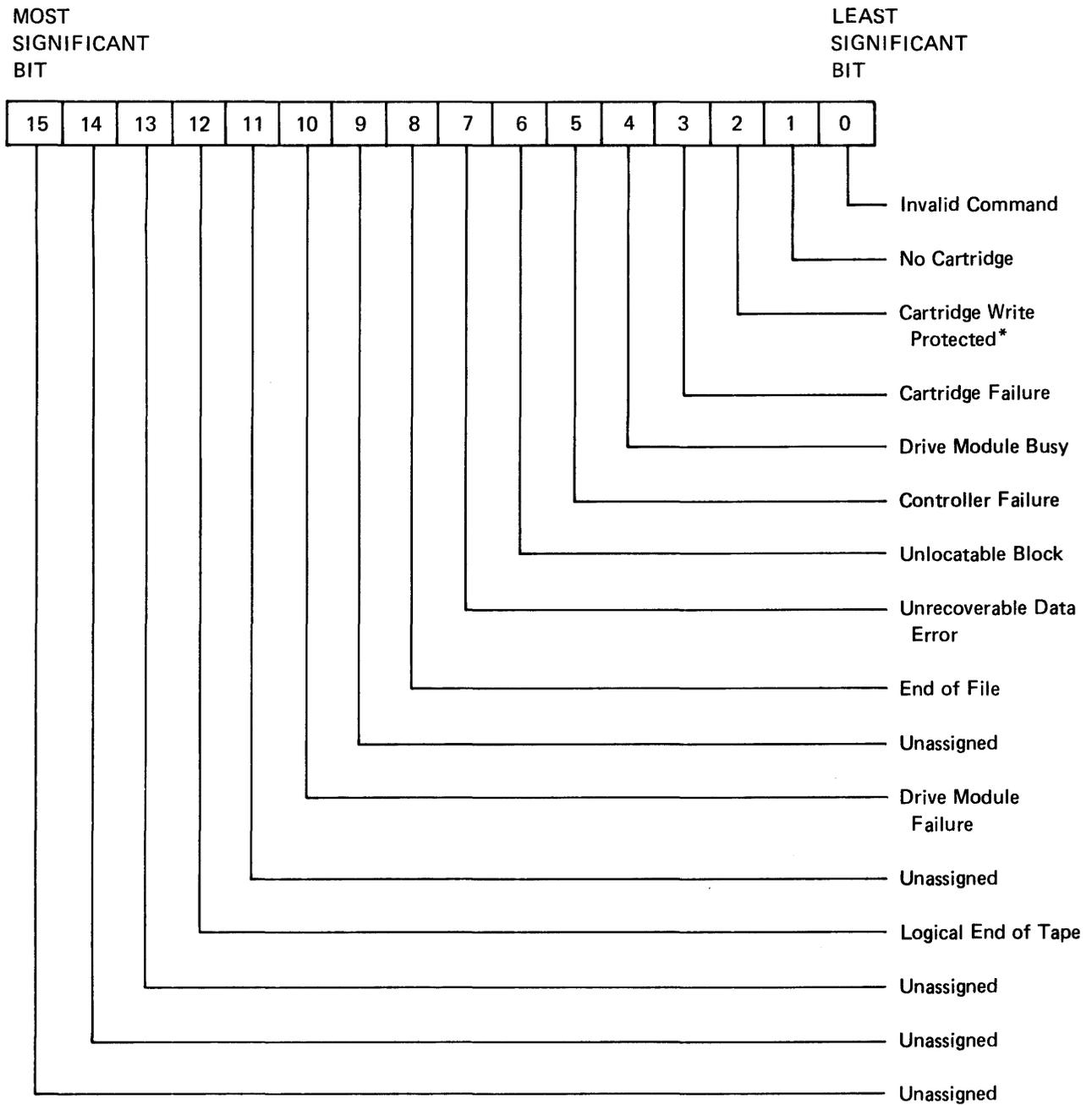
HCD-75 STATUS is transferred to the user's equipment in 16-bit words over the DATA OUTPUT BUS. If the drive detects an abnormal internal condition or if a change in status occurs (detecting END OF FILE), the ATTENTION output is set low. The user's equipment should then issue a REPORT STATUS command.

Status information is presented in the form of three 16-bit words. The first word has bits assigned to specific fault conditions: a bit will be set low to indicate a specific fault, and several bits may be set low simultaneously. The second word specifies the number of the selected drive module and drive status. The third word specifies the current block and track position. See the following illustration for details about the status words.

The following procedure is used to obtain status information from the HCD-75:

1. Enter a REPORT STATUS command as described.
2. After READY is set high to end the command sequence, set the INPUT/OUTPUT line low.
3. Set the COMMAND/DATA input low.
4. After a minimum delay of 1 microsecond following the completion of sets 2 and 3, set READY low.
5. Monitor the TRANSFER REQUEST output. When it goes low, the first status word is present on the DATA OUTPUT BUS.
6. When the user's equipment has acquired this status word, set the TRANSFER ACKNOWLEDGE input high. After the TRANSFER REQUEST goes high, set the TRANSFER ACKNOWLEDGE low.
7. Repeat steps 5 and 6 to acquire the second and third status words.
8. Set READY high to end the STATUS transfer.

### I. System Status Word (First Word)



\*Cartridge Write Protected status sets ATTN low if the issued command was a write command.

*INVALID COMMAND 0001:* The controller issues this status when any of the following events occurs.

1. If the controller has received an illegal function code that is not in the controller function code repertoire.
2. If the host does not set the INPUT/OUTPUT line high when it tries to send a command to the controller.
3. If the start address (WORD 2) or end address (WORD 3) of the COMMAND is not in the segment range specified by the stored limits 2323 and 2324 (Hex).

*NO CARTRIDGE 0002:* No cartridge in the drive.

*CARTRIDGE WRITE PROTECTED 0004:* This status is issued if the cartridge switch is on SAFE. The ATTN line will be set low if the host tries to execute a WRITE command. In the event of a READ or VERIFY command, this status code does not stop its execution.

*CARTRIDGE FAILURE 0008:* This status is issued if the drive detects either: 1) an off-tape condition while the drive is running, or 2) an abnormal motor load while the controller is in idle mode waiting for a command from the host.

*DRIVE BUSY 0010:* This status is issued if the drive is in the auto-load sequence or the controller has received a command from the host.

*CONTROLLER FAILURE 0020:* This status is issued if the controller detects any hardware failure in the system (e.g., malfunctioning timers, malfunctioning or abnormal DMAs). In most cases, re-executing the command will clear the problem; if it does not, the controller should be replaced.

*UNLOCATABLE BLOCK 0040:* If this status is issued without the UNRECOVERABLE DATA ERROR status, it indicates that the controller has encountered an unlocatable key when it writes to tape.

## NOTE

In write mode, if this status is issued together with the UNRECOVERABLE DATA ERROR, it indicates that the beginning block number specified in the write command is in the skip location table at (277F-27FF) that is built by the host. In verify mode, if this status is issued together with the UNRECOVERABLE DATA ERROR status, it indicates that there are blocks with unrecoverable data errors for that verify command. Users should examine the bad block location table built by the verify command at memory locations (237F-23FF).

*UNRECOVERABLE DATA ERROR 0080:* When this status is issued without the UNLOCATABLE block status, it indicates that the controller encounters a bad block (unrecoverable data block) in a read command. See previous NOTE under UNLOCATABLE BLOCK for details about this status being issued together with the UNLOCATABLE BLOCK status.

*END OF FILE 0100:* This status is issued after the read command if the controller encounters the END-OF-FILE block that was written earlier with the end-of-file command.

*DRIVE FAILURE 0400:* This status is issued if the controller detects an abnormal condition in the drive while it is reading or writing (e.g., off-tape, gain error, head stop error, tach error). If the problem persists after another attempt, either the cartridge or drive should be replaced.

*LOGICAL END OF TAPE 1000:* This status is issued while the controller is reading or writing, and indicates that the controller has already encountered the last block of the last track of the current selected segment.

## NOTE

System status words are additive; for example, a 0040 (UNLOCATABLE BLOCK) and a 0080 (UNRECOVERABLE DATA ERROR) will be reported as 00C0.

## II. Drive Status Word (Second Word)

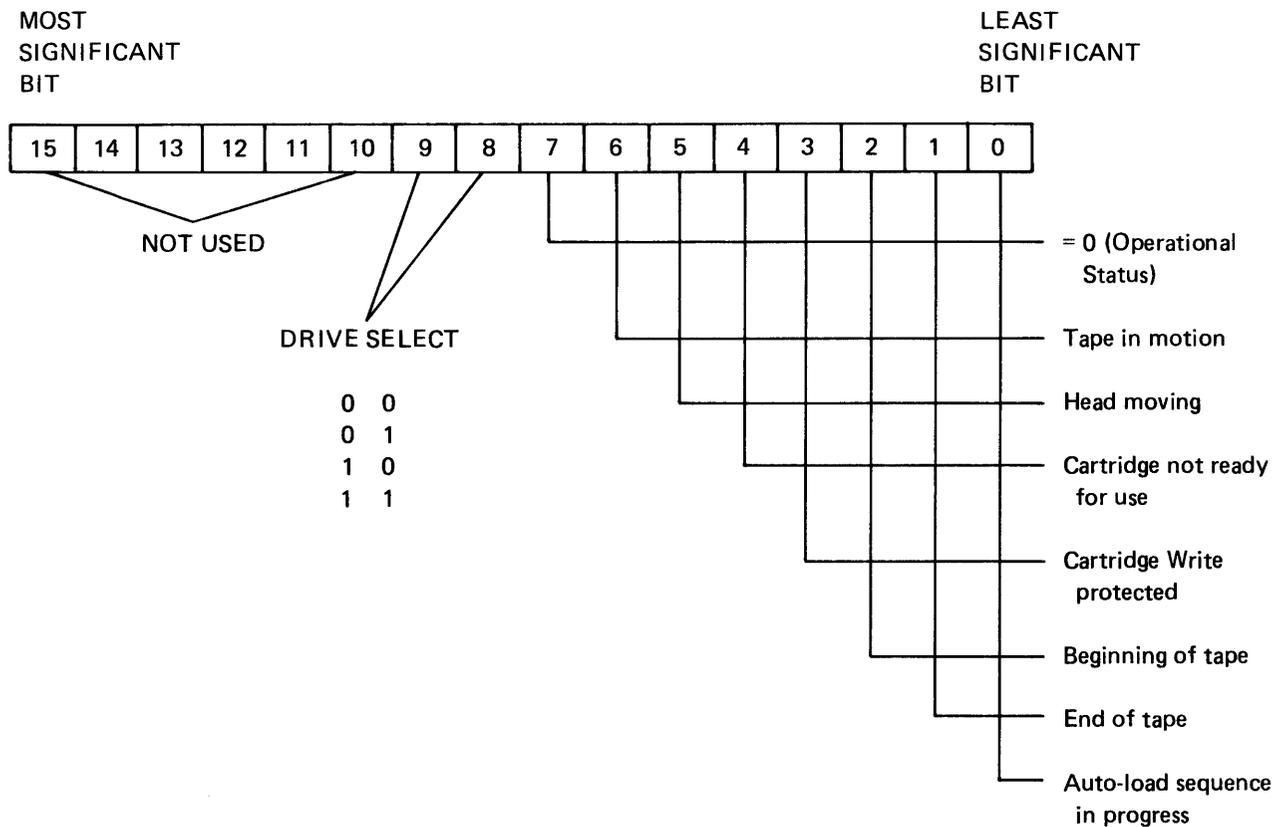
The second status word describes the active drive status at the time when the three status words are reported out. This word also specifies which drive is selected. When most read or write commands are completed, the tape is still moving; therefore, a drive status of 0X40 is normal.

The HCD-75 presents two different groups of status codes: OPERATIONAL and FAILURE. OPERATIONAL status is presented in real time, as the drive is executing commands or is idle. OPERATIONAL status indicates normal

drive operating conditions and is always available on the status lines, except for the times indicated below. Failure status indicates drive failure.

The status bit 7 should be tested to determine which status (OPERATIONAL or FAILURE) is being presented. OPERATIONAL status is low (0 bit); FAILURE status is high (1 bit).

### Operational Status



### NOTE

If a nonexistent drive address is selected, status word two comes back 0XFF, where X is the nonexistent drive number.

Because more than one status is possible at the time status is reported, OPERATIONAL status words are additive.

Bit 7. *OPERATIONAL STATUS* **0 N 00** :  
Drive Status  
No. N

This bit is low and indicates all conditions are normal. Under normal condition all other bits can be low.

Bit 6. *TAPE IN MOTION* **0 N 40** : On ramp-up from a stopped state, this line goes high only after tape has reached the requested operating speed. It remains high while tape is in motion. When stop is commanded, this line remains high until all mechanical motion has ceased. When a change of direction is commanded, this line will go low shortly after the change command has been received. It will then return to the high state after tape has reached the operating speed in the new direction.

Bit 5. *HEAD MOVING* **0 N 20** : This line is high only when the head is being stepped.

Bit 4. *CARTRIDGE NOT READY FOR USE* **0 N 10** : This line is high on power-up, reset, or after a drive failure has been acknowledged. Its function is to alert the user that a cartridge auto-load sequence is required before normal write-read operation can be done. The line remains high throughout the auto-load sequence, and then goes low after the drive has stopped at BOT.

Bit 3. *CARTRIDGE WRITE PROTECTED* **0 N 08** : This status line is used during the auto-load sequence. It is high if the cartridge is write-inhibited.

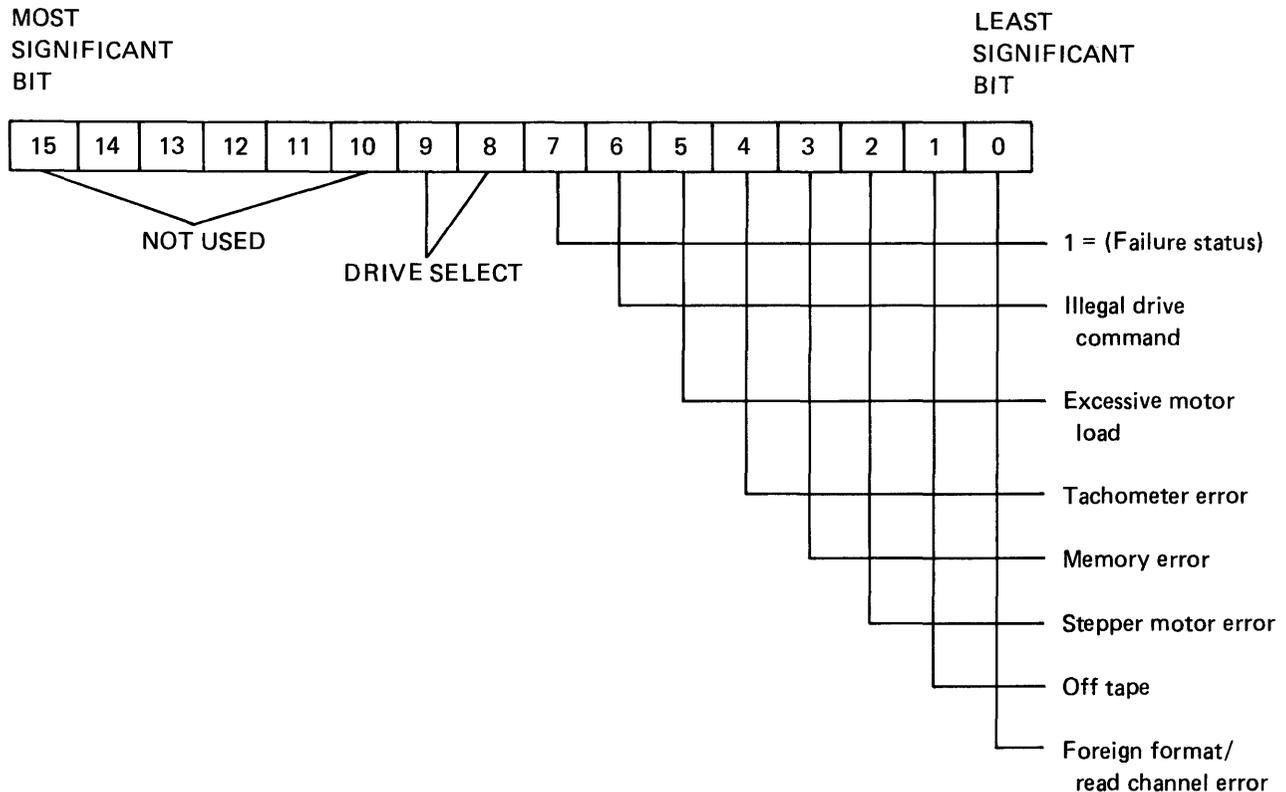
Bit 2. *BEGINNING OF TAPE* **0 N 04** : This status line goes high as the tape BOT pattern passes the head in the reverse direction. It remains high until the drive receives the next forward motion command or until the drive is reset.

Bit 1. *END OF TAPE* **0 N 02** : This status line goes high as the tape EOT pattern passes the head in the forward direction. It remains high until the drive receives the next reverse motion command or until the drive is reset.

Bit 0. *AUTO LOAD SEQUENCE IN PROGRESS* **0 N 01** : This status line is high throughout the cartridge auto-load sequence cycle. This cycle is activated under these conditions:

- a. After power-up reset, when the cartridge is inserted into the drive.
- b. After a drive failure, or unlock or unload command, where the cartridge has been removed, then reinserted.

## Failure Status (Second Word)



Bit 7. *FAILURE STATUS*

0	N	XX
Drive No.		Status
N		

: Line 7 only

goes high whenever any of the other lines indicate a failure has occurred. Therefore the status reported will be a combination of Bit 7 and one or more other bits.

Bit 6. *ILLEGAL DRIVE COMMAND*

0	N	C0
---	---	----

: This status line goes high under the conditions listed below and remains high until it has been acknowledged:

- a. Forward motion was commanded while at EOT.
- b. Reverse motion was commanded while at BOT.
- c. The command that was received is not in the drive command repertoire.
- d. Write to protected RAM memory (00BA-00FF) was attempted.
- e. The RW enable line was in write polarity at command transfer time.
- f. The RW enable line was in read polarity during write data transfer.

Bit 5. *EXCESSIVE MOTOR LOAD*

0	N	A0
---	---	----

: This line goes high if the drive is ever out of speed control for from two to four inches of tape travel. This status is not set until after the drive has stopped tape motion on its own and then remains high until after it has been acknowledged.

Bit 4. *TACHOMETER ERROR*

0	N	90
---	---	----

: This status line indicates that the drive has sensed the loss of the tachometer feedback signal while the tape was in motion. After the drive stops motion, the status is set high until it has been acknowledged.

Bit 3. *MEMORY ERROR*

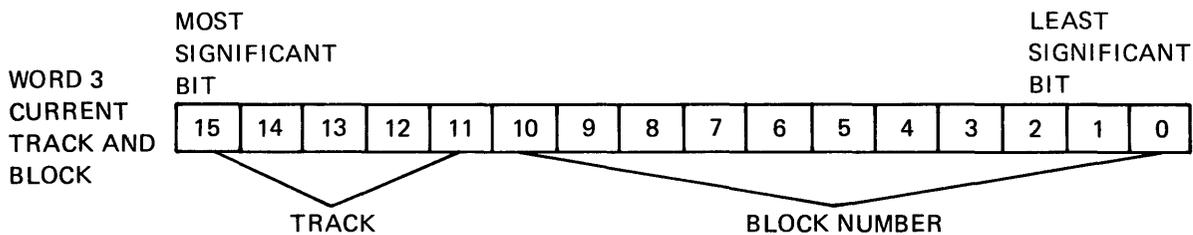
0	N	88
---	---	----

: On power-up reset, the drive tests prom and ram memory for reliability. If these tests indicate failure, the status is set and remains high until it has been acknowledged. The drive considers any of these conditions to be the same as power-up reset:

- a. reset during application of +5VDC.
- b. reset while the head is stepping.
- c. reset during the auto-load sequence.
- d. reset or cartridge out-in after a drive failure.

- Bit 2. **STEPPER MOTOR ERROR** 0 N 84: This type of error can occur only during the cartridge auto-load sequence and indicates a mismatch of counts for two tape edge seeks. The error status must be acknowledged before the status is cleared.
  
- Bit 1. **OFF TAPE** 0 N 82: During the auto-load sequence, this error can occur if the head steps too far below the expected range during a tape edge seek. It can also occur at any time that 3.5 inches of tape has passed the head without the presence of data. Drive motion will automatically be stopped for this error; then, status is presented to the user and remains until it has been acknowledged.
  
- Bit 0. **FOREIGN FORMAT/READ CHANNEL ERROR** 0 N 81: This status can only occur during the auto-load sequence. It indicates that either a cartridge with a foreign format has been inserted or that the read amplifier gain was set too low for reliable use. After motion has stopped, the status is set and remains until it has been acknowledged.

### III. Current Track and Block Word (Third Word)



The third word of the controller status is the current track and block of the tape relative to the controller, not to the host. The following information explains the form that the third word will take for each of the possible modes.

**IN WRITE MODE:** If a status response is issued after the controller executes a write command, this third word indicates the next block on tape that the controller will write when a buffer is filled with host data. However, when the status report command was issued because of an ATTN condition (i.e., the ATTN line set low), this third word will specify the block number where the controller detected the ATTENTIONable status.

**IN READ MODE:** If a status response is issued after a read command, this third word indicates the next block that the controller will read from tape as soon as one of the two buffers is empty (i.e., the host has taken data out of the buffer). This implies that there may be 2 buffers (equivalent to 2 data blocks) waiting to be taken by the host. It does not specify the block location where the computer is, relative to the controller.

However, when a status command is issued because of an ATTENTION condition, this third word specifies the block location where the controller detected the ATTENTIONable status.

**IN CONTINUE MODE:** See the write mode or read mode for explanation.

**IN OTHER MODES:** The third word indicates the last block the controller completed.



# DATA CONTROLS

## Data Verification and Bad Block Table

The controller can verify—as an off-line function—the readability of information previously written. In this function, the controller reads each block of information between a specified starting address and a specified ending address to make certain that every block in that area can be reproduced accurately, either directly or by using the system error-correction method.

If the data cannot be read properly after three read retries of a block, the block number is entered into a specified area of controller memory (bad block table) and the system moves on to verify the next block.

When the controller reaches the specified ending block in the verification process, the controller attention flag is set. At this time, the host computer can, if there are errors, interrogate the controller memory to determine how many unreadable blocks were found and what their addresses are by track and key number.

The bad block table begins at address 237F (HEX), which contains a hex number representing the number of data blocks in the table. The block locations (track and block number) are stored beginning at address 2380 (HEX). The table may contain up to 128 locations. This table is used to form the skip table.

## Skip Table

If specific locations on a tape are known to be bad, the host computer may enter the addresses of those locations into an area of controller memory called a SKIP TABLE. After the locations have been entered into the table, the HCD-75 will automatically skip over the locations in subsequent operations.

In actual practice, many HCD-75 users are generating a skip table made up of locations of blocks with unreadable keys (found during the writing of data) and blocks in which written data cannot be recovered (found during verify operations). The table is then recorded on the tape at a user-specified location.

The skip table can either be stored in a user data block or in absolute block 0008 (see Addressing in this section).

When the cartridge is used again, the system is programmed to immediately read the block that contains the bad location addresses and enters this data into the skip table memory locations of the HCD-75. The use of the Bad Block and Skip Table features of this system significantly enhances its error performance characteristics.

The skip table begins at address 277F (HEX), which contains a hex number representing the number of data blocks in the table. The block locations (track and block number) are stored beginning at address 2780 (HEX). The table may contain up to 128 locations. The location must be sorted in ascending order and maintained by the host. The HCD-75 will skip these data block locations in all read or write and verify operations. See FLOW CHARTS in Fig. 22A and 22B for details.

**MANUFACTURERS BLOCK**—Absolute block 0000. The data is recorded in ASCII (the parity bit is set to zero). Line 1 is the cartridge type. Line 2 is the number of user data blocks per track. Line 3 is a copywrite notice. And line 4 is the cartridge identification code.

Example. <CR><LF>  
DC600HC <CR><LF>  
4096 <CR><LF>  
FORMAT (C) 1980, MINN. MINING and MFG.  
CO. <CR><LF>  
XXXXXXXXXXXXXXXXXX <CR><LF>  
<ESC>

#### NOTE

The Manufacturers block must not be overwritten.

**CARTRIDGE “SIZING”**—The length of the DC615HC is 0000-3FFF Hex user block addresses. The DC600HC is 0000-0FFF user block addresses. After power up the controller by default is set for the use of a DC600HC cartridge and the controller memory location 2324 Hex is set to 0FFF. For proper operation with a DC615HC cartridge this location **MUST** be set to 03FF. If tape segmenting is employed location 2324 may be set to less than 03FF.

Tape cartridge size information is contained in the Manufacturers Block at the beginning of the tape (Absolute Loc. 0000).

The following flow chart in Fig. 21 is one method for cartridge sizing.

Alternates include:

- Reading the Manufacturers Block into the host and checking there.
- Asking the operator what type of cartridge was inserted.

#### WARNING

In any case the system must be left in user mode (Loc. 2328 set to 0000) when finished or the system will not operate as expected.

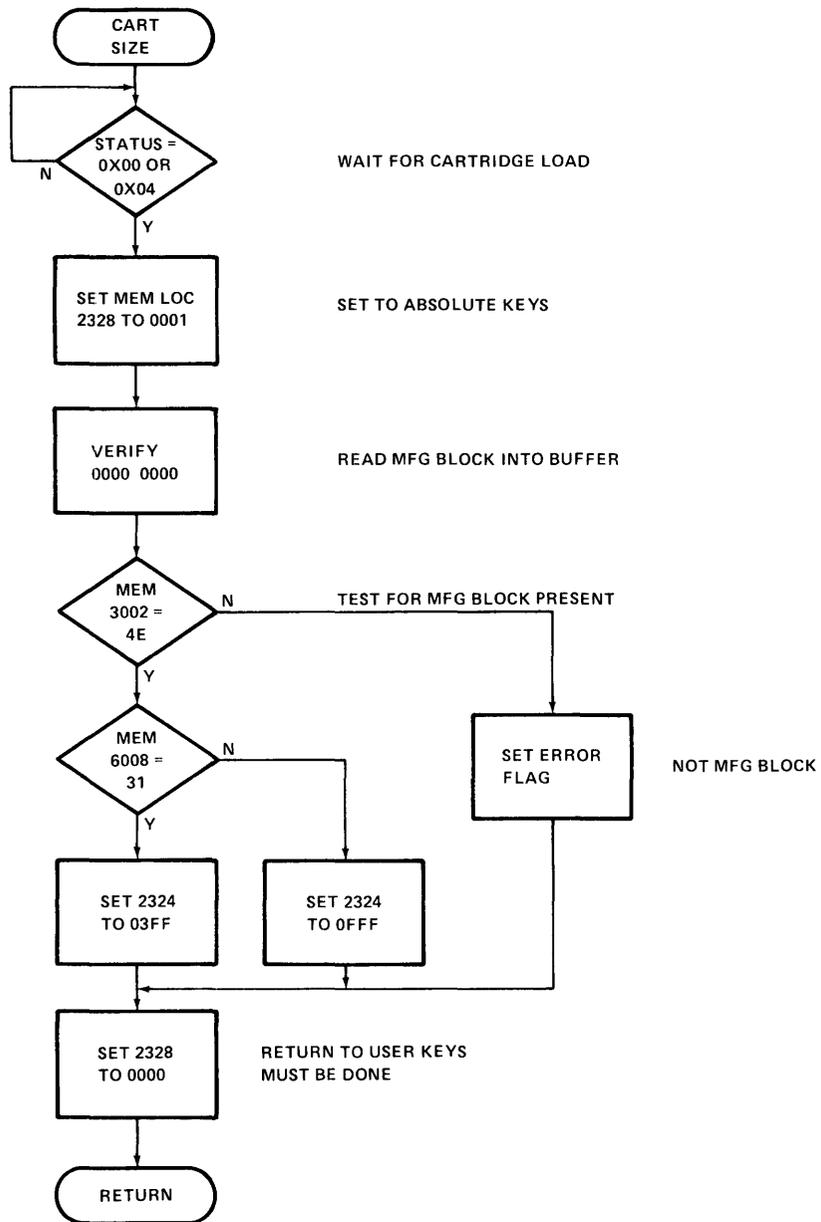


FIG. 21 Cartridge Sizing

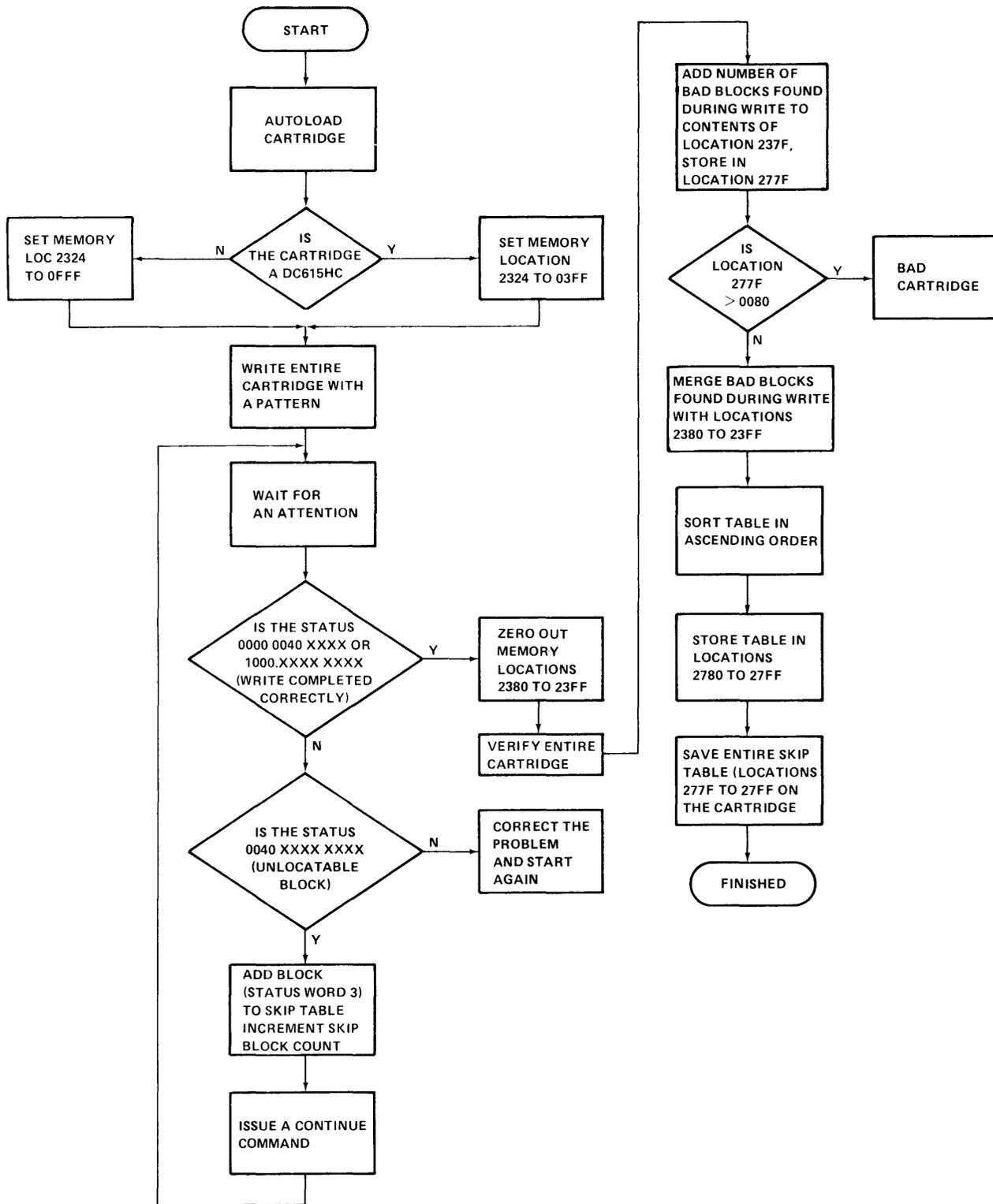


FIG. 22A To Create a Skip Table

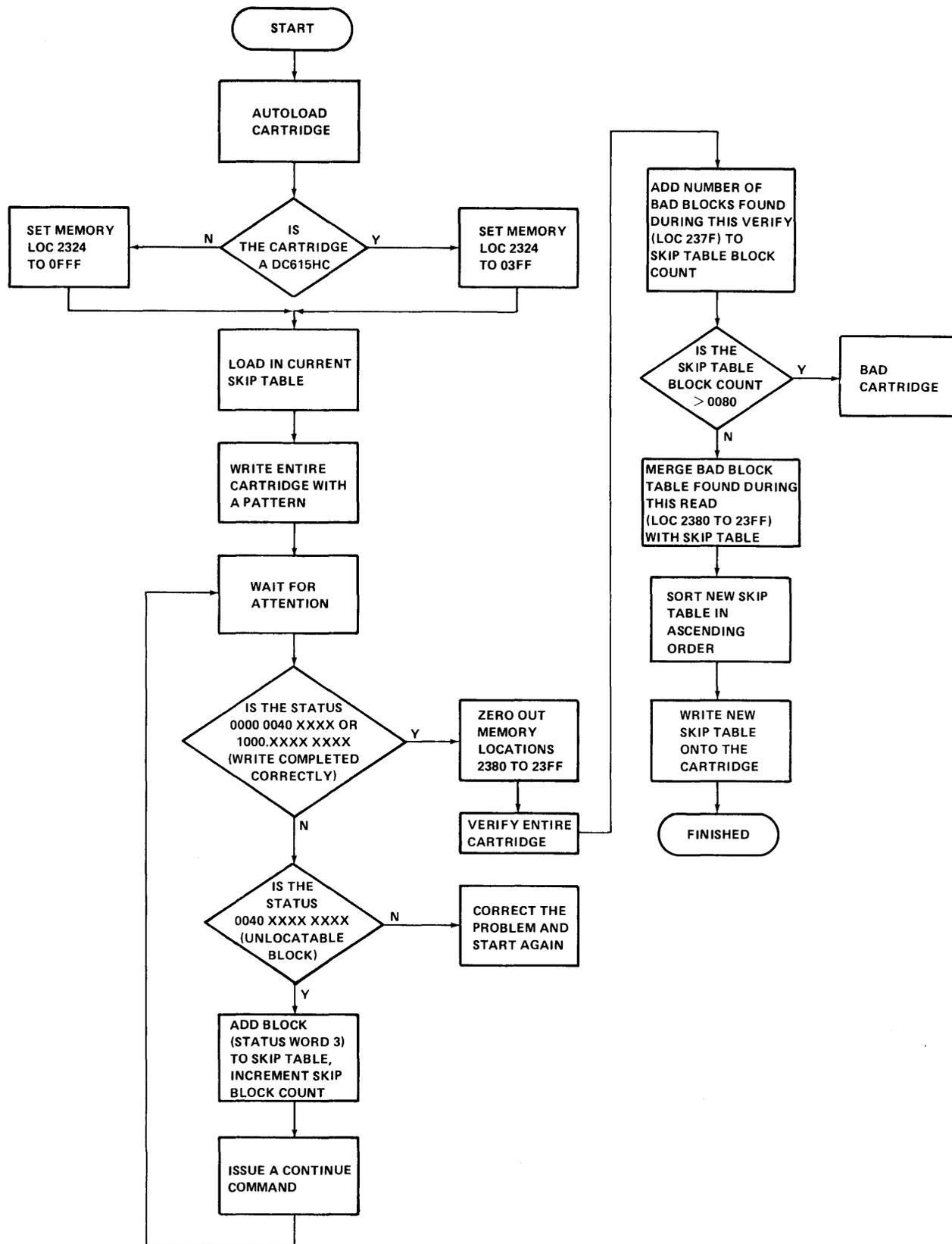


FIG. 22B Update Skip Table

**Tape Segmenting**

Tape segmenting is an important HCD-75 feature that provides the necessary operating functions when the system is used in special applications.

In this type of application, typical on-line storage capacity requirements might be low, but relatively fast access times are required. Tape segmenting is a means of dramatically reducing average access times by shortening the length of tape over which operations take place. In tape segmenting, the HCD-75 is programmed with a block address at which a segment begins and a stopping block address. The HCD-75 then performs desired operations on tracks 0 through 15, only between these starting and stopping points.

The table below, "Segmented DC600HC Average Access and Back-Up Time," gives average access times for various block segments specified. To compare two typical instances, note that a 4.2-megabyte record (that is, a full track) would have a 43.2 second average access time if recorded across the entire 600-foot length of the cartridge. Tape segmenting using 0.25 megabytes per track will reduce this time to 2.77 seconds. While average access time is significantly reduced through tape segmenting, back-up time is not affected. For 30 IPS the full tape average access time is 83.7 and the segmented average access time is 3.59.

**Segmented DC600HC  
Average Access and Back-Up Time  
60 IPS**

<b>SEGMENT SIZE MEGABYTES</b>	<b>AVE ACCESS (SEC) 60 IPS</b>	<b>DATA BLOCKS/ TRACK</b>	<b>BACK-UP TIME (MINUTES)</b>
.13	1.15	8	.16
.26	1.21	16	.22
.50	1.31	32	.35
1.0	1.52	64	.60
2.1	1.93	128	1.1
4.2	2.77	256	2.1
8.4	4.43	512	4.1
16.8	7.78	1024	8.1
33.6	14.45	2048	16.1
67.1	27.80	4096	32.1

**Segmented DC600HC  
Average Access and Back-Up Time  
30 IPS**

<b>SEGMENT SIZE MEGABYTES</b>	<b>AVE ACCESS (SEC) 30 IPS</b>	<b>DATA BLOCKS/ TRACK</b>	<b>BACK-UP TIME (MINUTES)</b>
.13	1.15	8	0.2
.26	1.24	16	0.3
.50	1.39	32	0.6
1.0	2.78	64	1.1
2.1	2.33	128	2.1
4.2	3.59	256	4.1
8.4	6.08	512	8.2
16.8	11.09	1024	16.4
33.6	21.08	2048	32.6
67.1	41.09	4096	65.6

To segment a tape:

1. Set memory location 2323 to the desired beginning block of the track (the first character must be 0).
2. Set memory location 2324 to the desired ending block of the track (the first character must be 0). For a DC600HC cartridge the maximum ending block is 0FFF, but for the DC615HC cartridge it is 03FF.

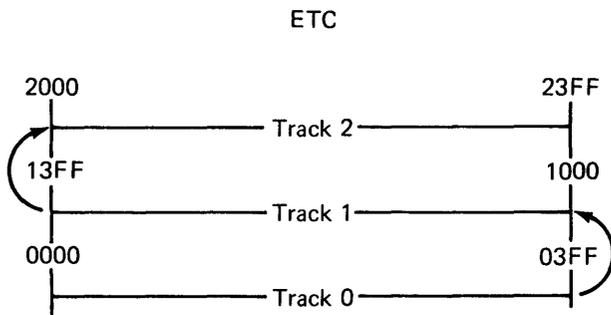
The most significant digit of the block address is the track number. For track 0, the block set in location 2323 is now seen by the host system as block 0000. The track length is the difference between the starting and ending blocks. Track 1 starts at 1000, this continues through F000 for track 15.

## Addressing

The HCD-75 system provides two methods of addressing cartridge block locations, the absolute mode and the user address mode. The absolute mode uses the actual prerecorded cartridge keys to address data blocks on the cartridge. The user mode simplifies the addressing of data blocks by interpreting and translating a consecutive addressing scheme into the absolute cartridge block keys. By default, the user mode of addressing is selected on power up. To select the absolute mode, memory buffer location 2328 must be changed from 0000 to 0001 by use of a Write Ram command. To return to the user key mode, memory location 2328 must be reset to 0000.

To access the manufacturers block, the diagnostics or system blocks, the system must be set to the absolute mode.

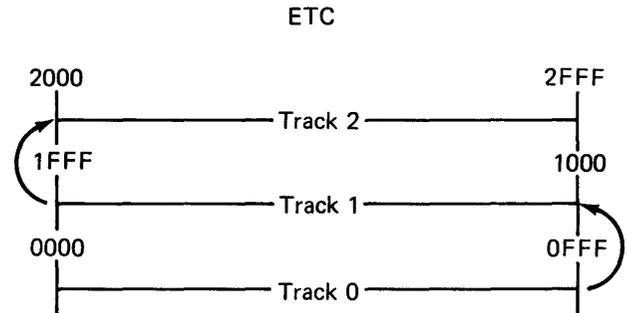
When using a DC615HC, the user addresses do not run consecutively but the order is the same.



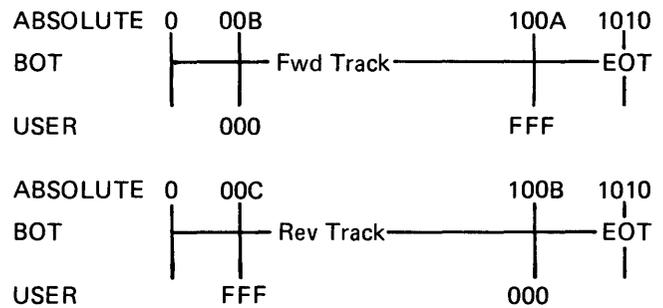
Whenever a DC615HC cartridge is used the following default parameters must be changed using a Write Ram command.

Loc.	(Default) DC600 HC	DC615
2323	0000	0000
2324	0FFF	03FF

The user mode provides a simple consecutive address scheme for the DC600HC starting with 0000 (track 0 block 0) and proceeding up to FFFF (track F block FFF) in a track by track serpentine method.



The user mode addresses are related to the absolute keys that are recorded on tape as follows:



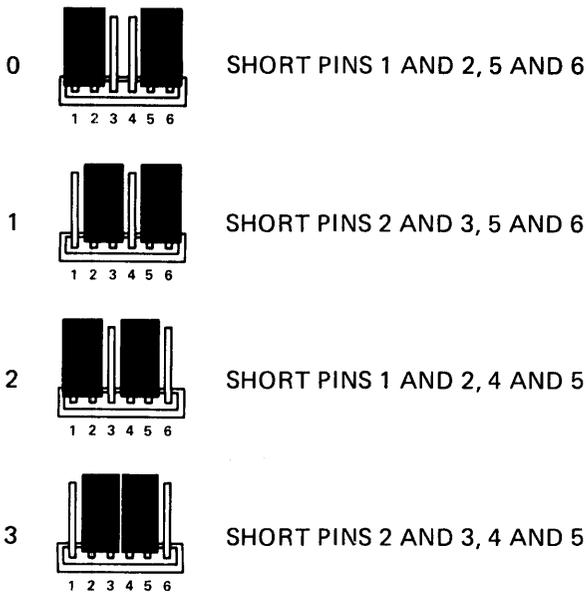


# DRIVE MODULE

## SELECTING DRIVE ADDRESSES

On one controller as many as four drive modules can be used. The drive addresses are 0, 1, 2, and 3. The drive is set to address 0 at the factory. To change the drive address:

- Loosen the four screws holding the P.C. Board shield and remove from drive.
- Locate the microprocessor assembly which is the double board assembly at the back. Reach down and pull it out by pulling on the ends of the large chips (damage may occur if the paper connector is pulled on to remove assembly).
- Lay the microprocessor assembly down with the PROM board side facing up.
- Locate J1 (Drive Select) at the bottom of the PROM board.
- The addresses are:



### NOTE

Some of the addressing information given in the past was for addresses 1 to 4, since the drive must be addressed as 0 to 3 this information is being given in the form of addresses 0 to 3.

Replace the microprocessor assembly and securely fasten the P.C. Board hold down shield over it.

## DRIVE INDICATORS

The drive alerts the user to problems by the status command and the 2 LEDs on the front of the drive. The drive fault conditions are:

Memory error—both ROM and RAM memory are tested following reset. Memory error status is set if either fails.

Motherboard L.E.D. indicators—two indicators on the front of the drive motherboard can be used to isolate possible trouble sources. One indicator is for possible drive problems and the other for possible cartridge problems. These patterns apply:

CONDITION	DRIVE L.E.D.	CARTRIDGE L.E.D.
Reset	ON	ON
Start of auto load sequence	OFF	OFF
Abnormal drive motor load	OFF	ON
Abnormal tach feedback	ON	OFF
Memory error	ON	OFF
Stepper motor error	ON	ON
Off tape	ON	ON
Read ampl. or A.G.C. error in drive	ON	OFF
Read ampl. error due to foreign cartridge	OFF	ON



# SERIAL INTERFACE

As a standard feature, the HCD-75 provides a serial interface port that conforms to RS232 protocol. This serial interface can be used for:

- checkout and troubleshooting
- initial product evaluation (by user)

All HCD-75 functions that can be performed using the parallel interface can also be performed using the serial interface. However, the serial interface can execute data transfer instructions on a block-per-command basis only. For example, in a read operation, a separate command must be entered for each block to be read.

## INTERFACE CONNECTIONS

An EIA standard 25 pin female connector located on the "Interface" PC board is used for the RS232 compatible signals.

## INTERFACE SIGNALS

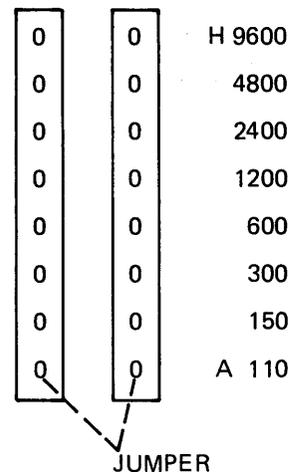
The following table identifies the RS-232C signals, their mnemonics and their characteristics:

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1	PROTECTIVE GROUND	POWER GROUND—This line provides a safety ground connection to the RS232C compatible terminal.
2	TRANSMIT DATA	TRANSMIT DATA—This line transfers data to the controller.
3	RECEIVE DATA	RECEIVE DATA—This line transfers data from the controller.
4	REQUEST TO SEND	REQUEST TO SEND—This signal prepares the modem for data transfer. When high, this signal places the modem in the transmit mode and, when low, in the receive mode.
5	CLEAR TO SEND	CLEAR TO SEND—This signal, when high, indicates the modem is ready to transmit data.
6	DATA SET READY	DATA SET READY—This signal is a high level.
7	SIGNAL GROUND	SIGNAL GROUND—This line provides a common signal connection to the RS-232C communications device.
8-25		Not Used

## DATA TERMINAL INTERFACE SPECIFICATIONS

CHARACTERISTICS	SPECIFICATIONS
Selectable baud rate	110, 150, 300, 600, 1200, 2400, 4800, 9600
Parity	No Parity
Number of bits transferred	8 Data bits
Stop bit select	1 Stop bit
Transmission Mode	Full duplex

\*Baud rate selector is located on the "INTERFACE" P.C. Board, and is identified as J1. A jumper plug selects the rate.



## OPERATING INSTRUCTIONS

### General

In the idle mode, the HCD-75 controller is looking for a command from either the host or an input on the serial port. When the controller receives an input from the serial port, it will block further inputs from the host until the user finishes the diagnostic mode by entering an S command. After the first character input from the serial port, the message: @ RS232 MONITOR X.X followed by 3 words of status are displayed.

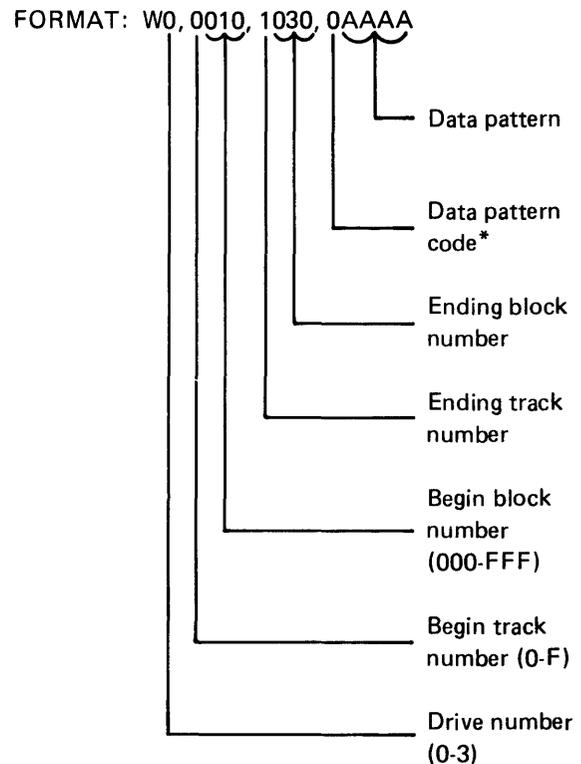
### Commands

The controller outputs an @ to the terminal as a prompt whenever it is waiting for a command. Each command string is terminated with a carriage return. The first character determines the type of desired operation, the next characters provide the additional parameters for the command. If an error is made when typing in the command, depress the ESC key to abort the current command line input. All command parameters are entered in HEX format. All command inputs are to be entered in upper case letters. There is a repeat command mode where the system will execute the command repeatedly if you enter an @ character before entering the carriage return. To stop this mode, depress the ESC key to abort the repeat mode. The prompt character @ will come back to indicate that the system is ready for new command input.

The depression of a key on the keyboard will halt the system while it is outputting characters, depress another key to continue the display. Depress an ESC key to abort the current operation.

The depression of a @ character and "carriage return" after the prompt character @ will put the system into the repeat command mode, performing the previous command repeatedly.

### 1. Write Diagnostic Command: W



\*Data pattern code:

- 0: fixed pattern
- 1: sequential pattern
- 2: random pattern, require to input an initial random number not 0000.
- 3: ASCII data, require an ASCII input string after carriage return (CR); an ESC key will terminate the input mode.
- 4: write data from the current WRITE BUFFER.

This command will write a number of block locations with data on the selected drive, using a fixed data pattern, a random pattern with an input starting random number, a sequential pattern starting with an input initial number, an ASCII data string, or the contents of the current write buffer (Buffer A).

The Controller RAM memory addresses 277F-27FF contain the user skip location table. The HCD-75 will skip these data block locations in all read, write and verify operations. The format for the skip table is similar to the table of bad block locations built by the VERIFY command in RAM memory addresses 237F-23FF. There are two WRITE BUFFERS A & B. However, WRITE BUFFER A is the only one used by the serial interface. Each buffer has 4 data frames and 2 error correction frames.

## WRITE BUFFER A\*

### FRAME 1

2000	Block #
2001	Record type (high byte), track and frame # (low byte)
2002	Character count for the whole block, data only (byte count)
2003	Data
	⋮
2082	Data
2083	Unused

### FRAME 2

2084	Block #
2085	Record type, track and frame #
2086	Character count
2087	Data
	⋮
2106	Data
2107	Unused

### FRAME 3

2108	Block #
2109	Record type, track and frame #
210A	Character count
210B	Data
	⋮
218A	Data
218B	Unused

### FRAME 4

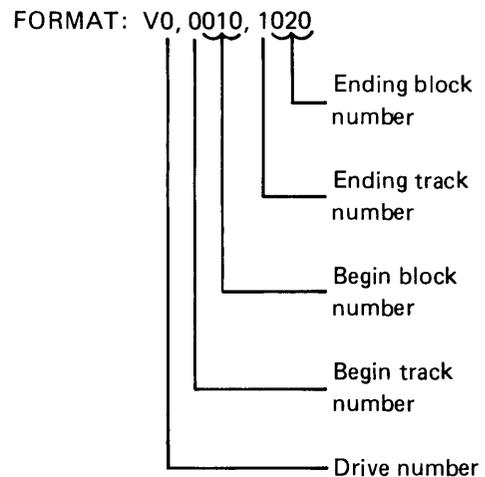
218C	Block #
218D	Record type, track and frame #
218E	Character count
218F	Data
	⋮
220E	Data
220F	Unused

\*After the write operation, all block #, record and track and frame # in the WRITE BUFFER are changed because they were used to construct the frames 5 and 6 during the write operation.

## NOTE

The block # observed in the buffers is the absolute key number prerecorded in the data block key.

## 2. Standard Verify: V



This command will perform a verify function for a number of tracks with starting block and ending block.

### Key Verification Option:

The Verify Command has three possible modes of operation. Verify data only, keys only, or both keys and data. To select the option set memory location 231E to:

0000—Verify Data only (Default)  
0001—Verify Keys and Data  
0080—Verify Keys only

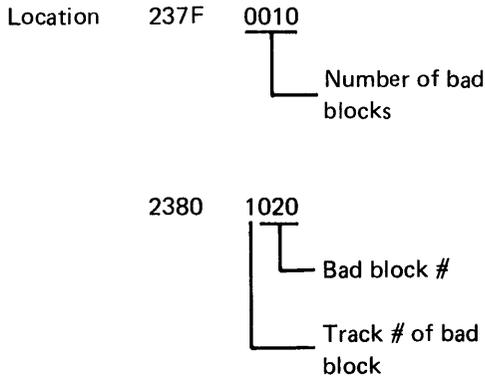
The difference between the Verify Command and the Certify Command is that the Certify Command reduces the price gain setting.

**ERROR STATISTICS**

**PART A: BAD BLOCK LOCATION TABLE**

On return from the command execution, the user can examine memory location 237F for the number of bad blocks (blocks containing unrecoverable errors) and memory locations 2380-23FF for bad block locations (128 decimal locations).

EXAMPLE:



**PART B: GENERAL ERROR INFORMATION**

Users can also examine the following locations for error statistics:

- 232B Total number of frame errors\*
- 232C Total number of retries on data blocks
- 232D Maximum number of retries allowed for a single data block (programmable).
- 232E Total number of retries on key
- 232F Maximum number of retries allowed on a key (programmable)

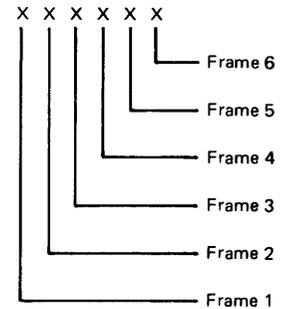
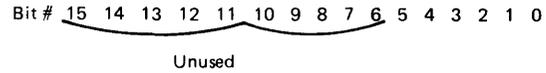
**PART C: BLOCK ERROR TABLE**

- 2400 Number of entries in table\*\*
- 2401 Block number
- 2402 Bit map for frames with errors in the above block\*\*\* (in hex format).
- 2403 Block number
- 2404 Bit map for frames with errors in above block
- ...
- 26FF Block number
- 2700 Bit map for frames with errors in above block

\*FRAME ERROR: Can be due to a CRC error, an improper frame header or a format timing error detected by the controller formatter.

\*\*Each entry occupies 2 locations

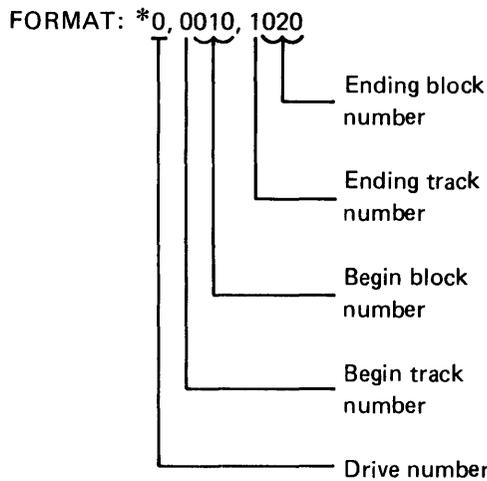
\*\*\*Bit map structure:



X = 0 good frame  
X = 1 bad frame

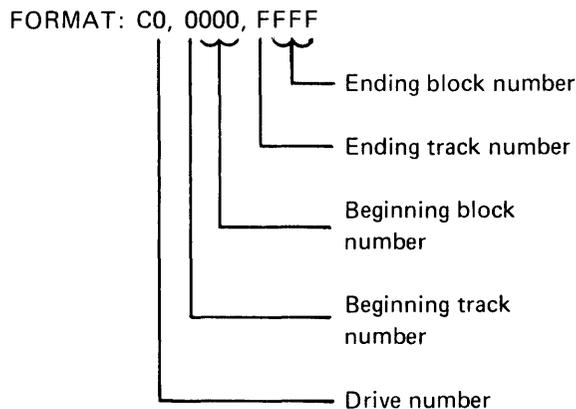
If the table is overflowed in the middle of the verify command then it will start over to record at the beginning of table (location 2401), the location 2400 will not be reset to zero. At the beginning of the next verify command the following locations are cleared to accumulate statistics: 232B, 232C, 2400, 237F.

**3. Special Verify (Stop on Error): \***



This command will perform a verify function for a number of tracks with starting block and ending block. This special command will stop on the first block containing a frame error. No error correction is made and users can examine the error in read buffer A. The error statistics in the standard verify command also apply to this command.

**4. Certify Command: C**



The HCD-75 system Certify Command is a part of the standard 30 and 60 IPS controller firmware package starting with Revision 5 (30 IPS) or Revision 3 (60 IPS). The Certify Command may be used in place of the normal Verify Command to generate a table of all permanent error locations on a given cartridge. Whereas, the Verify bad block table indicates only unrecoverable data error locations, the Certify bad block table will indicate all permanent error locations, even if the error is a single frame format recoverable type error.

The bad block table for the Certify Command starts at 237F and is identical in form to the Verify bad block table. The total error table of both transient and permanent errors is located in memory starting at address 2400.

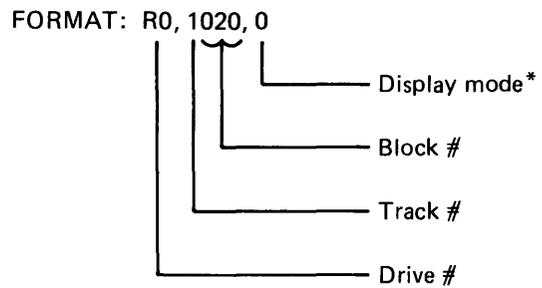
The significant difference between the Verify and Certify command is that the HCD-75 drive module read amplifier gain is lowered by 14% to test tapes to a higher performance specification.

**Key Certification Option:**

The Certify Command has three possible modes of operation. Certify data only, keys only, or both keys and data. To select the option set memory location 231E to:

- 0000—Certify Data only (Default)
- 0001—Certify Keys and Data
- 0080—Certify Keys only

**5. Read: R**



**\*Display mode:**

- 0: no display after read
- 1: display the block of ASCII data just read (BUFFER A only)
- 2: display the block of HEX data just read (BUFFER A only)

This command will read 1 block of data from tape and receive it in controller buffer memory (READ BUFFER A). The block comes back from the drive in 6 frames. Each frame is 128 words of data. The first 4 frames are data, the last 2 frames are error correction. The addresses of 4 data frames are as follows:

READ BUFFER A

FRAME 1

2000	Block #
2001	Record type, track and frame #
2002	Character count (for the whole block, data only)
2003	Data
	{
2082	Data
2083	CRC

FRAME 2

2084	Block #
2085	Record type, track and frame #
2086	Character count
2087	Data
	{
2106	Data
2107	CRC

FRAME 3

2108	Block #
2109	Record type, track and frame #
210A	Character count
210B	Data
	{
218B	CRC

FRAME 4

218C	Block #
218D	Record type, track and frame #
218E	Character count
218F	Data
	{
220F	CRC

FRAME 5 (ECC frame for frames 1 and 3)

2210	Block #
2211	Record type, track and frame #
2212	Character count
2213	Data
	{
2292	Data
2293	CRC

FRAME 6 (ECC frame for frames 2 and 4)

2294	Block #
2295	Record type, track and frame #
2296	Character count
2297	Data
	{
2316	Data
2317	CRC

**NOTE**

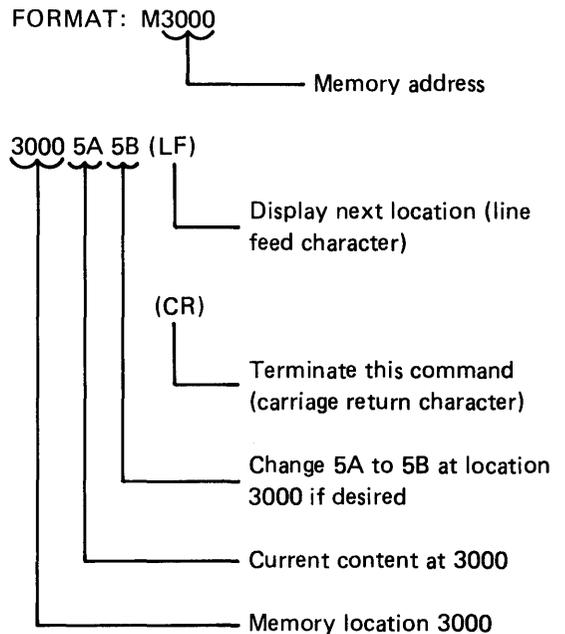
If frame 5 or 6 is used to correct one or more of the data frames the frame # for the data frame will be a 5 or 6 and no ECC data will be read into the buffer.

Error Statistics: The read command will generate the 'general error information' as in Part B of the VERIFY command.

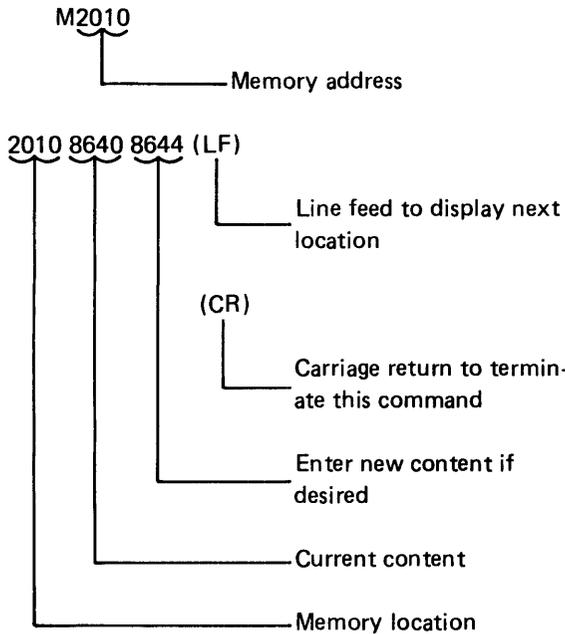
READ BUFFER B

This buffer is not used in Reads or Writes from the RS232 Serial Port.

6. Memory: M

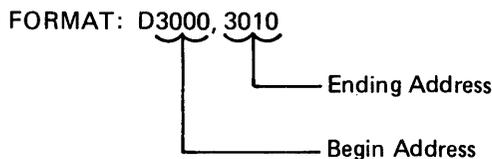


Displays a certain memory location in the controller. If a memory location between 2000-27FF is wanted, this command will display a word of data, not a byte since location 2000 is a combination of location 6000 and 3000. (The upper byte of 2000 is the data at 6000 and the lower byte of 2000 is the data at 3000). After memory content is displayed, enter the new content if desired.



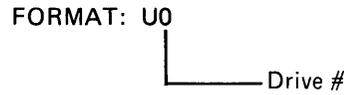
This command may be used to determine the level of controller software by display memory location F001.

**7. Display Memory: D**



Display memory content from address 3000 to 3010. Each line of display has 8 bytes (or words) of data depending on the requested address (2000-27FF: word location, anything else: byte location). This command can be used to examine the controller firmware addresses (E000-FFFF). To halt the display, depress a key, to continue display depress another key. To abort the command, halt the system first by depressing a key then type an ESC key.

**8. Unload Cartridge: U**



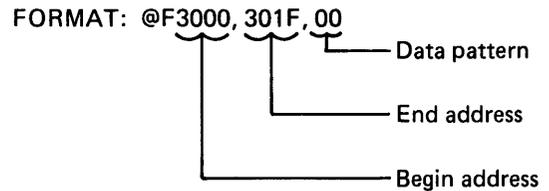
This command causes the cartridge to be wound to END OF TAPE and stopped. It also unlocks the cartridge eject lever so that the cartridge can be removed.

**9. Status Request: T**



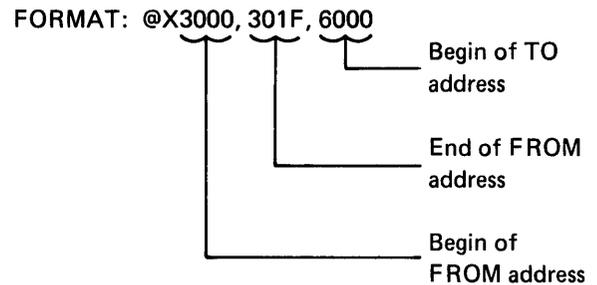
This command will return the drive and controller status (3 words).

**10. Fill Memory: F**



This command will fill up memory location from 3000 to 301F with the data pattern 00 (if the address is 2XXX the data byte will be written into 6XXX and 3XXX).

**11. Transfer Memory: X**



This command will transfer the content of memory location from 3000 to 301F to memory locations starting at 6000. (Do not use this command to move memory address 2XXX).

12. End: S

FORMAT: @S

Release HCD-75 controller from diagnostic mode and allow the controller to look for commands from the HOST interface.

Controller Status:

When you first request control of the HCD-75 on the serial interface, the status currently stored in memory is reported out. An updated status is outputted when an operation is completed or aborted because of an error condition. The status request also outputs the stored status information. All status is reported as three 4 digit HEX words.

CONTROLLER STATUS (WORD 1)

<u>HEX</u>	<u>CONDITION</u>
0000	NORMAL STATUS—COMMAND COMPLETE
0001	INVALID COMMAND
0002	NO CARTRIDGE
0004	CARTRIDGE WRITE PROTECTED
0008	CARTRIDGE FAILURE
0010	DRIVE MODULE BUSY
0020	CONTROLLER FAILURE
0040	UNLOCATABLE BLOCK
0080	UNRECOVERABLE DATA ERROR
00C0	VERIFY ERROR DETECTED
0100	END OF FILE
0400	DRIVE MODULE FAILURE
1000	LOGICAL END OF TAPE

DRIVE STATUS (WORD 2)

<u>HEX</u>	<u>CONDITION</u>
0X00	NORMAL STATUS
0X01	LOAD SEQUENCE IN PROGRESS
0X02	EOT
0X04	BOT
0X10	CARTRIDGE NOT READY FOR USE
0X20	HEAD MOVING
0X40	TAPE IN MOTION
0X81	READ AMP GAIN ERROR
0X82	BAD FORMAT—OFF TAPE
0X84	HEAD STEP ERROR
0X88	MEMORY ERROR
0X90	TACH ERROR
0XA0	EXCESSIVE MOTOR LOAD
0XC0	ILLEGAL DRIVE COMMAND
0XFF	NO SUCH DRIVE

(X IS DRIVE NUMBER)

NOTE

If a nonexistent drive is selected the second status word comes back 0XFF.

CURRENT BLOCK LOCATION (WORD 3)

The current HCD-75 status can be examined any time once the HCD-75 is in the RS232 MONITOR X.X. mode. The memory locations for the 3 status words are:

- Word 1: 2325
- Word 2: 2326
- Word 3: 2327

## MEMORY LOCATIONS OF INTEREST

The memory locations mentioned here are the only ones available for user access. All memory locations not mentioned here are reserved to the manufacturer. The memory locations and contents are in hex. Most locations are also listed in the text, see RS232 Serial, Parallel Interface, and Data Control sections.

231E	Controls Certify and Verify commands
0000	Data only (default)
0001	Data and Keys
0080	Keys only
231F	Controls Block size
0100	256 bytes/block
0200	512 bytes/block
0300	768 bytes/block
0400	1024 bytes/block (default)
2320	First word of a normal command
2321	Second word of a normal command
2322	Third word of a normal command
2323	Beginning user block address for a track
2324	Ending user block address for a track
2325	First word of status message—controller
2326	Second word of status message—drive
2327	Third word of status message—current block loc.
2328	Set user or absolute key mode
	User = 0000, Absolute = 0001
232B	Total number of frame errors*
232C	Total number of retries on data blocks
232D	Maximum number of retries allowed for a single data block (programmable)
232E	Total number of retries on keys
232F	Maximum number of retries allowed on a key (programmable)
237F	Number of entries in the Bad Block Table
2380	Beginning of Bad Block Table
	{
23FF	Ending of Bad Block Table
277F	Number of entries in the Skip Table
2780	Beginning of Skip Table
	{
27FF	Ending of Skip Table
F001	Revision level of controller PROMs

### BUFFER A

#### FRAME 1

2000	Block #
2001	Record type, track and frame #
2002	Character count (for the whole block, data only)
2003	Data
	{
2082	Data
2083	Write-not used
	Read-CRC

#### FRAME 2

2084	Block #
2085	Record type, track and frame #
2086	Character count
2087	Data
	{
2106	Data
2107	Write-not used
	Read-CRC

#### FRAME 3

2108	Block #
2109	Record type, track and frame #
210A	Character count
210B	Data
	{
218A	Data
218B	Write-not used
	Read-CRC

#### FRAME 4

218C	Block #
218D	Record type, track and frame #
218E	Character count
218F	Data
	{
220E	Data
220F	Write-not used
	Read-CRC

FRAME 5 (ECC frame for frames 1 and 3)

2210	Block #
2211	Record type, track and frame #
2212	Character count
2213	Data
	{
2292	Data
2293	Write-not used
	Read-CRC

FRAME 6 (ECC frame for frames 2 and 4)

2294	Block #
2295	Record type, track and frame #
2296	Character count
2297	Data
	{
2316	Data
2317	Write-not used
	Read-CRC

BUFFER B--PARALLEL READ/WRITE

FRAME 1

2400	Block #
2401	Record type, track and frame #
2402	Character count
2403	Data
	{
2482	Data
2483	Write-not used
	Read-CRC

FRAME 2

2484	Block #
2485	Record type, track and frame #
2486	Character count
2487	Data
	{
2506	Data
2507	Write-not used
	Read-CRC

FRAME 3

2508	Block #
2509	Record type, track and frame #
250A	Character count
250B	Data
	{
258A	Data
258B	Write-not used
	Read-CRC

FRAME 4

258C	Block #
258D	Record type, track and frame #
258E	Character count
258F	Data
	{
260E	Data
260F	Write-not used
	Read-CRC

FRAME 5 (ECC frame for frames 1 and 3) Write-not used

2610	Block #
2611	Record type, track and frame #
2612	Character count
2613	Data
	{
2692	Data
2693	Read-CRC

FRAME 6 (ECC frame for frames 2 and 4) Write-not used

2694	Block #
2695	Record type, track and frame #
2696	Character count
2697	Data
	{
2716	Data
2717	Read-CRC

**BUFFER B: DURING VERIFY OR CERTIFY COMMANDS**

2400	Number of entries in table**
2401	Block number
2402	Bit map for frames with errors in the above block***(in hex format).
2403	Block number
2404	Bit map for frames with errors in above block
⋮	⋮
26FF	Block number
2700	Bit map for frames with errors in above block

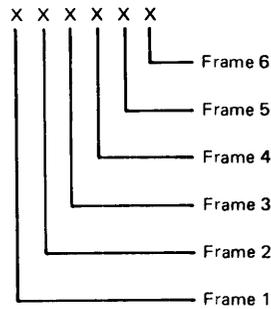
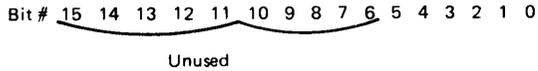
X = 0 good frame  
 X = 1 bad frame

If the table is overflowed in the middle of the verify command then it will start over to record at the beginning of table (location 2401), the location 2400 will not be reset to zero. At the beginning of the next verify command the following locations are cleared to accumulate statistics: 232B, 232C, 2400, 237F.

\*FRAME ERROR: Can be due to a CRC error, an improper frame header or a format timing error detected by the controller formatter.

\*\*Each entry occupies 2 locations

\*\*\*Bit map structure:





## USER OPTIONS

### VARIABLE BLOCK SIZE

Due to the unique data addressing requirements of certain host operating software systems, it may be convenient to change the HCD-75 data block size. An option has been provided to reduce the block size from the standard 1024 bytes to 256 bytes, 512 bytes or 768 bytes. Thus, data can be addressed in any of the above block sizes. Data cartridge capacity is reduced proportionately because the same prerecorded key-to-key spacing, which identifies a block of data, is maintained. Less than the maximum 1024 bytes of user data will be recorded in each block. The block as written on tape will be filled with blank characters for the unused portions. On read back, only the bytes of user data are transferred out.

This variable block size has been incorporated into the standard HCD-75 controller software on 30 IPS systems with Revision 5 or later software and Revision 3 or later software on 60 IPS systems.

To activate this option, either through the parallel interface or the interactive R.S.232 data port, the controller memory location 231F must be reprogrammed. The default setting of 231F is a hex 0400 for 1024 bytes per block. The following hex codes will change the block size as indicated.

0100 for 256 bytes/block and 16.7 megabytes total  
0200 for 512 bytes/block and 33.5 megabytes total  
0300 for 768 bytes/block and 50.3 megabytes total

The above totals refer to total data storage capacity of a DC600HC. If a DC615HC is used, each total must be divided by 4. All addressing is the same as a full 1024 byte block basis.



# INSTALLATION AND CHECKOUT

## PACKAGING

HCD-75 System components are packaged by 3M in a way designed to protect them from vibration damage and from the effects of static electricity. Each component is placed first into a 3M Velostat anti-static bag made of electrically conductive plastic. Then, the component is placed into a shipping carton with protective foam inserts.

When unpacking components, care should be taken to ground both personnel handling the equipment and the work area where the equipment is to be used. Specially designed 3M Static Control Mats for floors and work tables are available for anti-static protection.

All of the packaging material—Velostat bag, foam inserts, and shipping carton—should be saved for use in the event that the equipment has to be shipped to another location or to 3M.

## Requirements

Equipment and materials required (in addition to HCD-75 System standard components):

- 1 data terminal (optional)
- 1 power supply (fully described below)
- 1 DC600HC Formatted Data Cartridge
- cables: power and interconnect

## CAUTION

Position the drive module at least 24 inches from Cathode Ray Tube (CRTs). If this is not possible, shield the drive module.

## CHECKOUT

Remove the HCD-75 system from its packing. Set it up on a nonconductive surface, obeying all normal static precautions. Connect the drive interface cable and the power

supply cables. The power supply must be known to have +5 volts and +12 volts in the proper ranges.

- Apply power to the HCD-75 system.
- Check the Memory LED on the controller. It should come on and then go off.
- Look for the two drive LEDs to come on.
- Listen for the audible chatter.
- After the chatter ends check the drive LEDs to see that both are off.

## WARNING

If any of these steps do not occur turn off power. Check all cabling and voltages (+5V must be +4.9 volts to 5.25 volts as measured on the Controller Interface Board).

- Insert a known good cartridge (either a DC615HC or a DC600HC).
- After a moment the tape will start moving slowly.
- The tape then comes up to speed and the head moves down, up and back down.
- The tape is run at high speed to BOT.
- The head moves down, up and back down again.
- The autoloader finishes by rewinding again to BOT.

The HCD-75 system diagnostic checkout is complete. If a RS232 device is available continue, otherwise bypass the next steps.

- Connect the RS232 device.
- Use the M Command to set Loc. 2324 to 007F.
- Enter W0 0000 F07F 05555. This writes on all 16 tracks for a length of 128 blocks.
- Enter V0 0000 F07F. This checks the data just written.
- Enter M237F. If this location is approaching 0080 try a different cartridge. If the new cartridge shows a low count in 237F use this cartridge to complete checkout. If the second cartridge also has a very high count reexamine the power and refer to the Power Requirements section.

This completes the checkout of the HCD-75 system. The system is ready to be installed in the user's system.

## POWER REQUIREMENTS

A HCD-75 system consisting of one drive module with controller requires the following power:

- +5 VDC + 5% - 2% @ 6.0 amps
- +12 VDC + 10% - 5% @ 1.75 amps

During motor acceleration/deceleration, a surge to 3.5 amps (50 millisecond duration) will occur on the +12 volt input.

### NOTE

- more than 5.25 VDC can cause chip damage
- less than 4.9 VDC can result in excessive data errors (because of the effect of the low voltage on the operations of the controller).

### CAUTION

Linear power supplies are recommended for the HCD-75. If a switching power supply is used in the system, the tape drive chassis must be isolated from the switching power supply chassis.

### NOTE

The auxiliary circuit (+12 VDC) should not be on unless the control circuit (+5 VDC) is on.

When turning power off, turn off the +12 VDC power first and then turn off the +5 VDC power.

Twist power cable to help reduce noise pickup.

### CAUTION

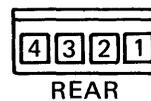
Gold contacts mixed with tin contacts can cause voltage drop due to oxidation.

The high current required by these units may cause excessive voltage drop in the power cables. Voltage must meet specified values on the HCD-75 Interface Board.

## Power Cables

One power cable is required for the HCD-75 Controller Module and one power cable for each data Drive. The following materials are required to make cables for one Controller and one Drive:

- 8 contacts, Crimp Gold Molex KK 08-56-0106
- 2 Housing, 4 CKT Molex KK 09-50-3041
- 2 Key, Polarizing Molex KK 15-04-0219



In addition, cut three lengths of #16 GA stranded insulated wire for each cable required. Cut to the desired length, but no more than 4 feet to a Drive and no more than 12 inches to the Controller.

Crimp a contact to one end of each of the three wires. Insert the crimped contacts into pin locations 1, 2, and 4. Insert key into location 3. Twist the three wires into a cable and connect the cable leads to the appropriate power supply. (See the pin list below and the Power Connector Illustration that follows it.)

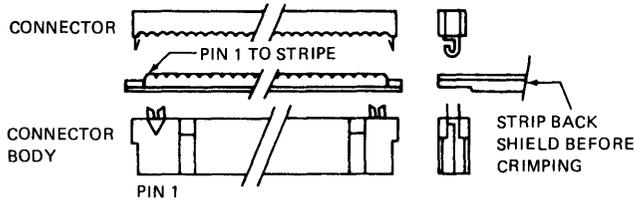
- Pin 1 = +12 VDC
- Pin 2 = GND
- Pin 3 = Key
- Pin 4 = +5 VDC

## Interconnect Cables

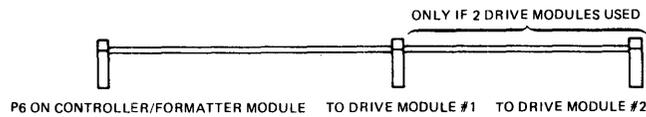
Materials required to construct cables to connect one HCD-75 Drive Module to a Controller and from a Controller to the user's system are:

- six 50 CKT socket connectors 3M 3425-6000
- adequate length of 50 conductor shielded cable 3M 3469/50

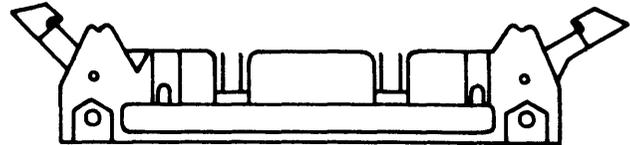
Make one cable to connect the drive to the controller, no more than four inches long if mounted back to back, and a maximum length of 15 feet if the drive is separated from the controller. Strip back the shield one-half inch from the end to which the connector is to be installed. Install the connector on the striped cable to #1 pin side (50 Conductor Cable Connector illustration below).



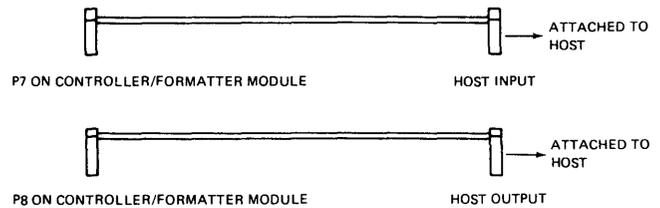
If two or more drives are used with a controller, configure the connecting cable as shown in the illustration below.



Make two cables to interface between the input bus and output bus of the HCD-75 Controller and the user's system. Assemble the connector and cable in the same way interconnect cables are hooked up in the description above. If the same type of connector is to be used at the user interface, two headers (illustrated below) are required to interface with the cable connector used. Use 50 CKT right-angle connectors—3M 3433-1200—or straight connector on the user interface.



HEADER

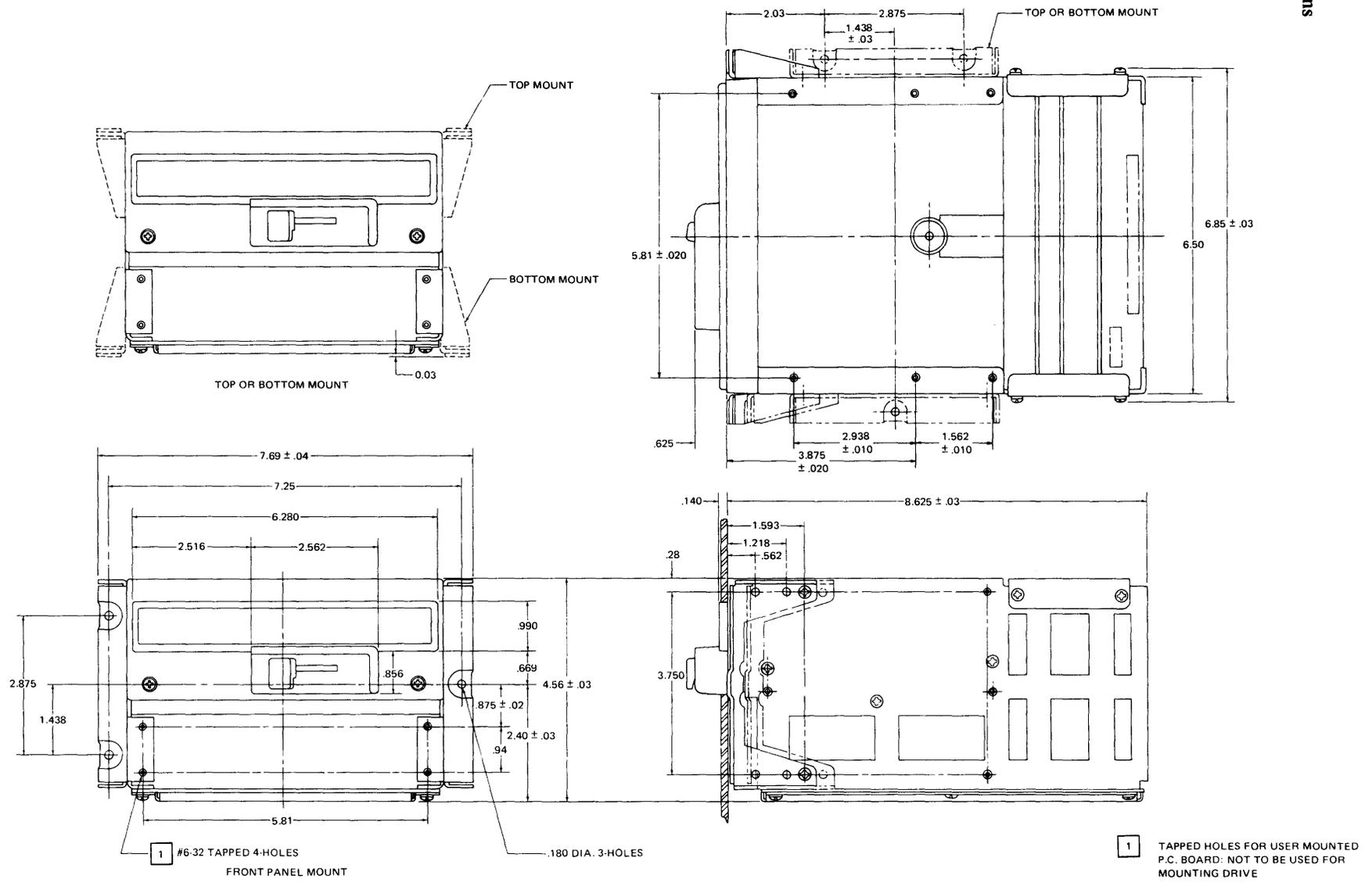


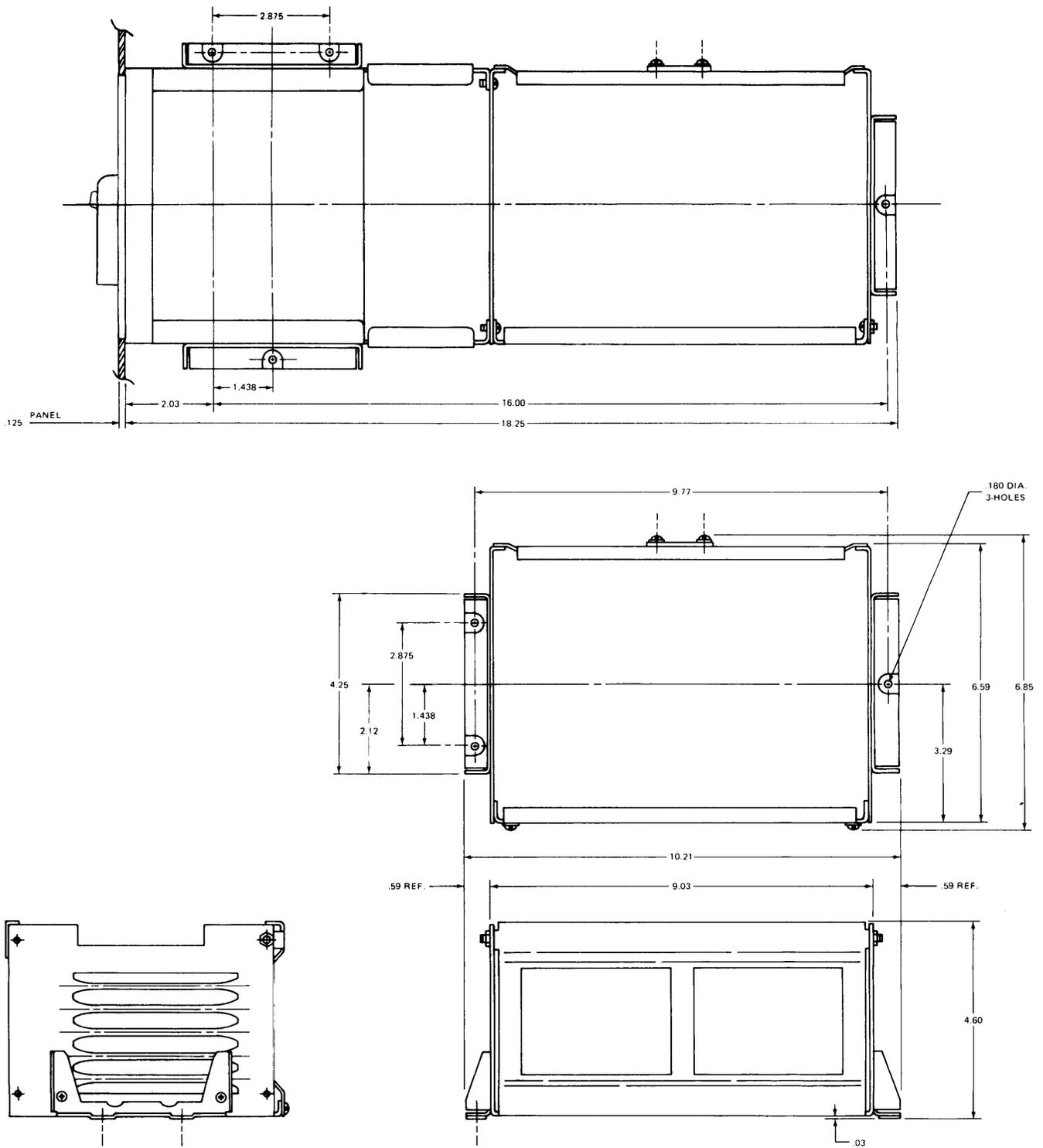
### CABLE KIT

The HCD-75 Kit, Cable and Connector provides enough connectors and cable to interface one HCD-75 Controller Module and two HCD-75 Drive Modules to the user's system. The kit part number is 80-9700-0207-9. Included with this kit are the following:

ITEM	DESCRIPTION	MFG. PART NO.	QUANTITY
1	Contact, Crimp Gold	Molex KK 08-56-0106	12
2	Housing, 4 CKT.	Molex KK 09-50-3041	3
3	Key Polarizing	Molex KK 15-04-0219	3
4	Conn, 50 CKT Socket	3M 3425-6000	7
5	Cable 50 Cond. Shielded	3M 3469/50	25 Ft.
6	Header, 50 CKT RT. Ang.	3M 3433-1202	2

FIG. 23 HCD-75 Mounting Dimensions





**FIG. 24 Controller Mounting Dimensions**

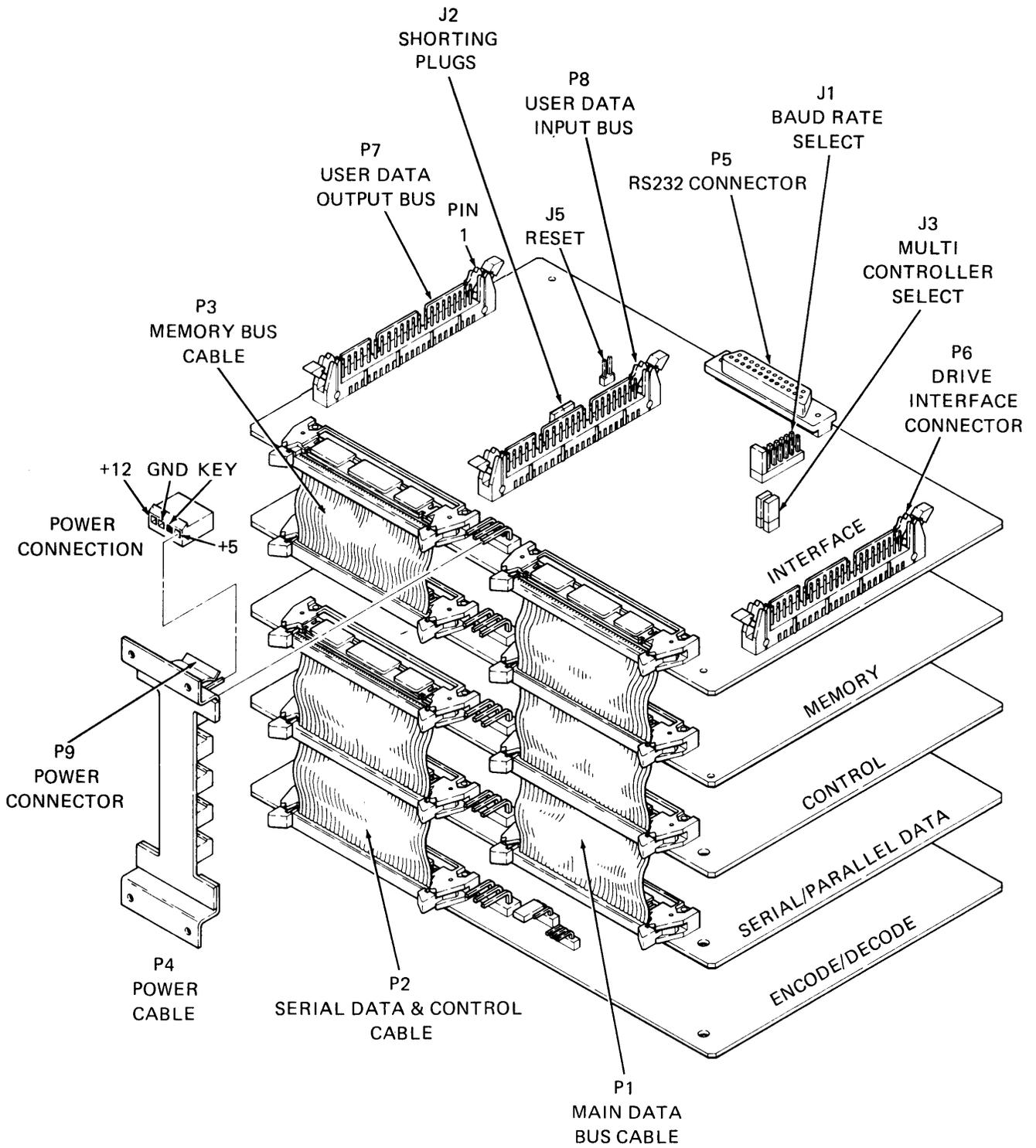


FIG. 25. Controller PCB Cable and Plug Locations

# SYSTEM SPECIFICATIONS

## Mechanical Specification

### Drive Module

- Width 6.85 inches (174 mm)
- Height 4.60 inches (117 mm)
- Depth 8.625 inches (219 mm)  
(Front face of bezel)
- Weight 6 pounds (2.72 kg)
- Mounting Via mounting brackets  
(Mounting horizontal or vertical, but not upside down.)

### Controller Module

- Width 6.85 inches (174 mm)
- Height 4.60 inches (117 mm)
- Depth 9.25 inches (235 mm)
- Weight 5.2 pounds (2.4 kg)
- Mounting Via mounting brackets  
Controller may be attached to drive module or mounted up to 15 feet away, using mounting brackets.
- P.C. Board Orientation:  
Vertical (no forced air flow)  
Horizontal (with forced air flow)

## Temperature and Humidity

### Drive Module

- Temperature  
Storage -40°F to 149°F  
(-40°C to 65°C)  
Operating 41°F to 113°F\*  
(5°C to 45°C)\*  
Operating without Cartridge 32°F to 120°F  
(0°C to 50°C)
- Humidity  
Storage 10% to 95% R.H.  
Operating 20% to 80% R.H.  
noncondensing\*  
Maximum Wet Bulb 79°F (26°C)

\*Cartridge Limiting

### Controller

- Temperature  
Storage -40°F to 149°F  
(-40°C to 65°C)  
Operating 32°F to 120°F  
(0°C to 50°C)  
\*P.C. boards in the Horizontal plane must be forced air cooled to remove heat build-up between boards.)
- Humidity  
Storage 10% to 95% R.H.  
Operating 10% to 95% R.H.

## Power Requirements

### Drive Module

- Voltage +5 VDC (+5%, -2%)  
+12 VDC (+10%, -5%)  
1%  
● Ripple +5 VDC—typ. 1.5 amp,  
max. 1.6 amp  
+12 VDC—idle .13 amp,  
max. 0.15 amp  
+12 VDC—run 1.0 amp,  
max. 1.1 amp  
(3.5-amp, 50-millisecond motor surge)
- Current
- Power +5 VDC—typ. 5.75W,  
max. 8.4W  
+12 VDC—typ. 12W,  
max. 14.5W
- Total power Running typ. 17.75W,  
max. 22.9 W  
Idle typ. 8W, max. 10W

### Controller Module

- Voltage +5 VDC (+5%, -2%)  
+12 VDC (+5%, -2%)  
1%
- Ripple +5 VDC—typ. 4.1 amp,  
max. 4.4 amp  
+12 VDC—typ. .6 amp,  
max. .65 amp
- Current
- Power +5 VDC—typ. 20.5W,  
max. 23.1W  
+12 VDC—typ. 7.5W,  
max. 8.9W
- Total power typ. 28.0W, max. 32.0W

## Reliability

### Drive and Controller

- MTBF 10,000 hours (with regular maintenance)
- MTTR 30 minutes

### Maintenance Replacement Schedule

- Servo motor 15,000 600-foot cartridge cycles
- Head 50,000 600-foot cartridge cycles
- Stepper motor 15,000,000 steps

### Performance

- Speed Read/Write 60 IPS 30 IPS  
Search 90 IPS 60 IPS
- Data Throughput 35K bytes/second (average) at 60 IPS  
17.5K bytes/second (average) at 30 IPS  
2.67 megabyte/second (burst)
- Capacity (DC600HC) 144 megabytes unformatted  
67.1 megabytes formatted
- Tracks 16
- Block size 1024 bytes
- Blocks/track (DC600HC) 4096
- Recording Density 10,000 BPI
- Recording Method IMFM
- Error Detection CRC
- Error Correction HCD-75 ECC Format
- Error Recovery 3 retries with ECC
- Error Rate Less than 1 error in  $10^{10}$  bits
- Track-to-Track seek 195 milliseconds
- Ramp Times

IPS	(MILLISECONDS)	
	UP	DOWN
30	75	65
60	92	85
90	115	120

This equipment is a UL recognized component per file E76824.

# HCD ENVIRONMENTAL TEST RESULTS

## Shock and Vibration

## NOTE

### Drive Module

- Vibration (operating) Tested to 1G, 5 to 2000 Hz, 3 axis
- Shock (non-operating) Tested to 50G, 11 milliseconds, half sinewave

### Controller Module

- Vibration (operating) Tested to 2G, 5 to 2000 Hz, 3 axis
- Shock (non-operating) Tested to 50G, 11 milliseconds, half sinewave

The information provided above are results of tests performed by an independent laboratory on two randomly selected production units. This data is intended as a general design guideline when considering system packaging requirements for anticipated shock, vibration, EMI, and pressurization levels. Performance to the above levels is neither warranted nor guaranteed by 3M and these test results shall not be considered a part of 3M's published specification for the HCD-75 High Capacity Cartridge Drive system.

## Altitude

### Operating

- Drive and Controller Tested to 10,000 ft.

### Non-operating

- Drive and Controller 50,000 ft.

## Electromagnetic Interference\*

\*Run to basic limits of MIL-STD-461 and 462

### Drive Module

- Radiated 60 db (avg.) 15 KHz to 1 GHz
- Flat Cable Conducted 60 db (avg.) 15 KHz to 50 MHz
- Susceptibility above 2V/meter 15 KHz to 250 MHz

### Controller Module

- Radiated 60 db (avg.) 15 KHz to 1 GHz
- Susceptibility above 2V/meter 15 KHz to 250 MHz

## ROUTINE MAINTENANCE

### Drive Module

In order to ensure that the drive module will continue to operate at optimal levels, the cleaning of the tape head and the drive puck should be included in the operator's routine maintenance schedule. This should be done after 80 hours of usage or as required.

The procedure for cleaning the head and puck is a relatively simple one and requires only a cotton swab moistened with ethyl alcohol. To clean the drive module components:

1. Press the Cartridge In (CIN) switch—
  - the tape head will come up, and
  - the drive puck will begin to rotate.
2. Clean the head and puck carefully with the moistened swab.
3. Press the CIN switch again.

The drive module components will now be ready for operation.

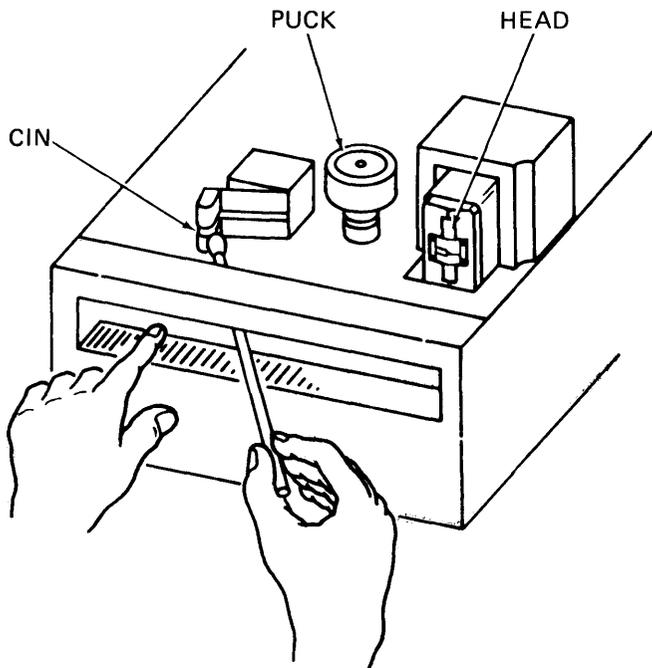
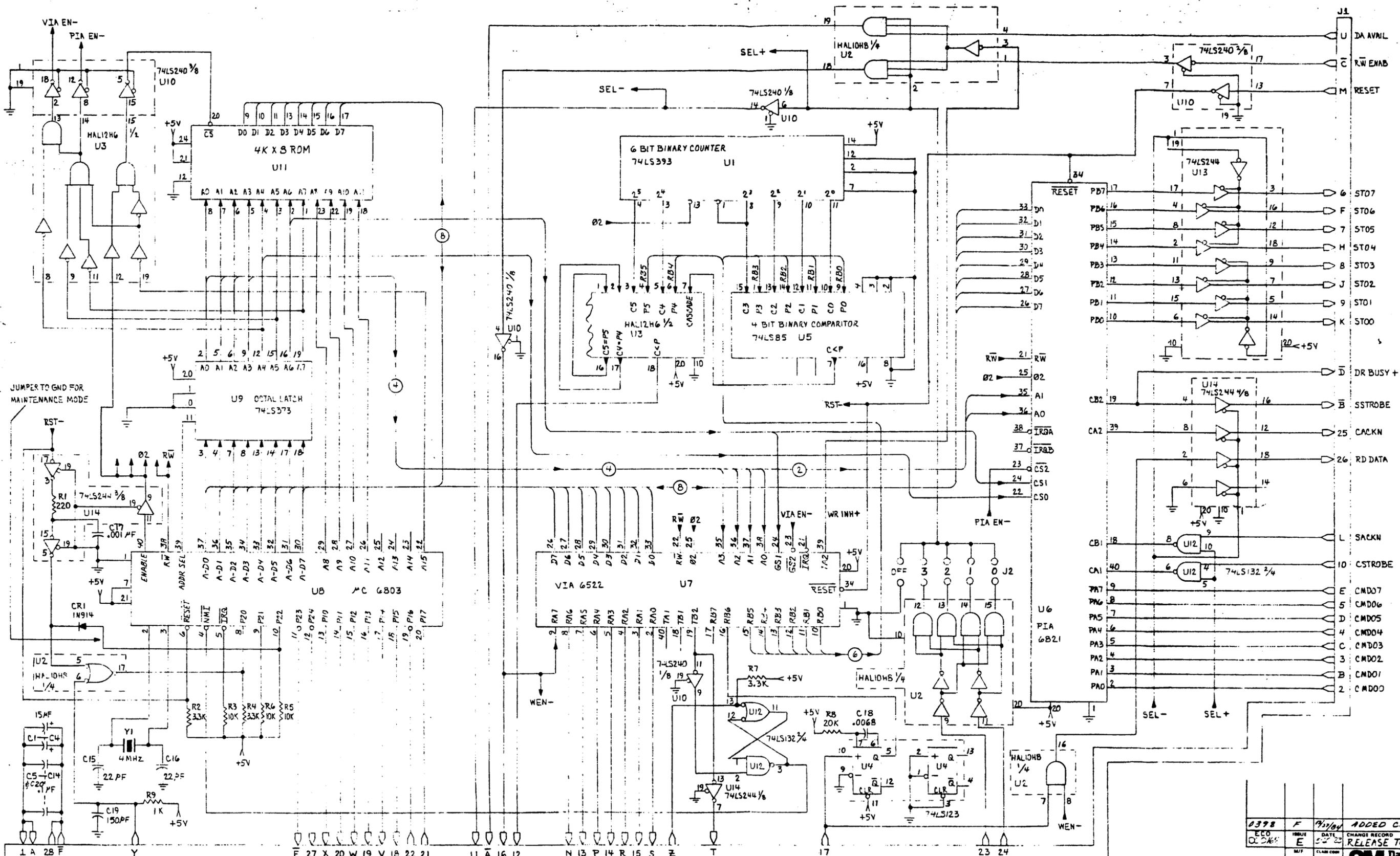


FIG. 26 Head Clearing



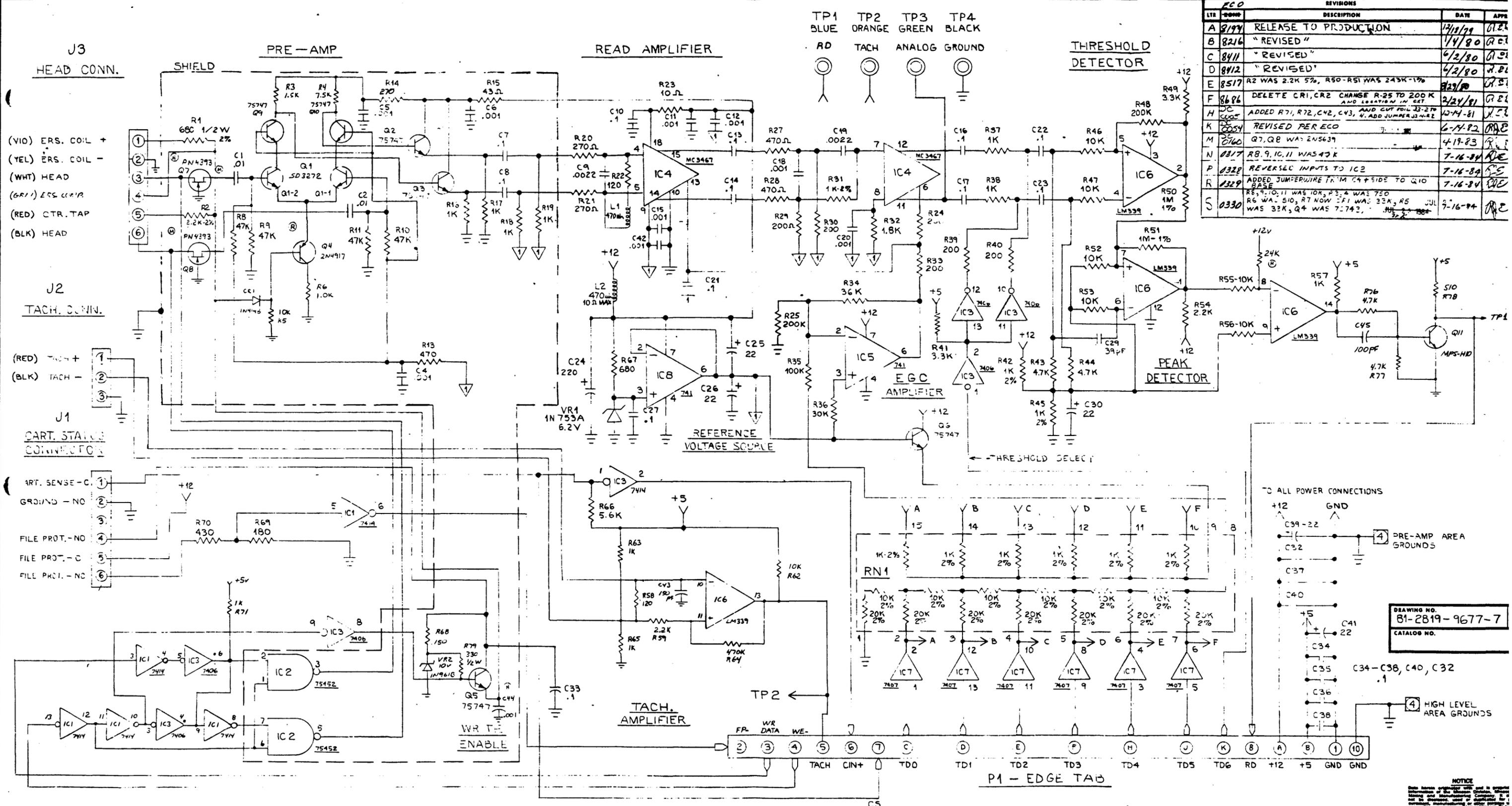
NOTES: UNLESS SPECIFIED  
 1. RESISTORS IN Ω, 1/4 W 5%  
 2. CAPACITORS IN MFD.

0398	F	9/17/84	ADDED C80	NG
ECO	E	DATE	CHANGE RECORD	BY
0398	E	5-22-82	RELEASE TO PRODUCTION	AJ
M/J	CLAM	COM		

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 MINNESOTA MINING & MANUFACTURING CO.  
 © 2011 COPYRIGHT 1984

USED ON	MATERIAL	SCALE	TITLE
TOLERANCES - UNLESS NOTED	INCHES	MM	PCB ASSEMBLY
DRW: 5-27-82 M.A.F.	CHKD BY: 8-17-82 M.A.F.	APPROVED BY: 8-17-82 M.A.F.	HCD-75 DRIVE CONTROL
DO NOT SCALE DRAWING	APPROVED BY: 8-17-82 M.A.F.	D	PART NO: 78-8044-4918-5

DES

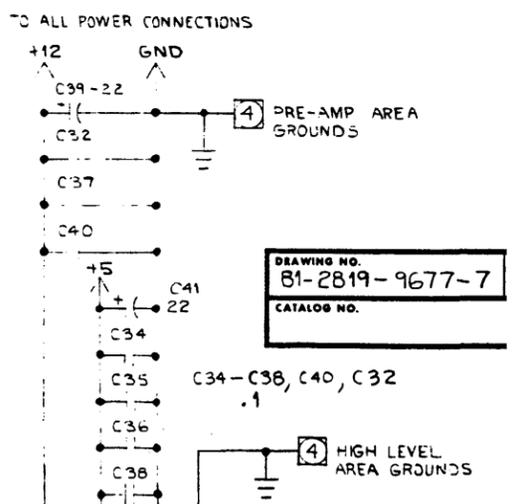


REV. NO.		REVISIONS	
LT#	DATE	DESCRIPTION	DATE
A	8/1/77	RELEASE TO PRODUCTION	11/11/77
B	8/21/78	"REVISED"	1/4/80
C	8/11/78	"REVISED"	6/2/80
D	8/11/78	"REVISED"	6/2/80
E	8/5/77	R2 WAS 2.2K 5%, R50-R51 WAS 245K-1%	8/23/80
F	8/6/76	DELETE C1, C2 CHANGE R-25 TO 200K AND LOCATION IN CAT.	2/24/81
H	8/10/77	ADDED R71, R72, C42, C43, AND CUT FOLIO 23-27	12/14/81
K	8/26/76	REVISED PER ECO	6-14-82
M	8/26/76	Q7, Q8 WAS 2N5637	4-19-83
N	8/31/77	R8, 9, 10, 11 WAS 47K	7-16-84
P	8/32/77	REVERSED INPUTS TO IC2	7-16-84
R	8/32/77	ADDED JUMPERWIRE FROM C4 SIDE TO Q10 BASE	7-16-84
S	8/33/77	R8, 9, 10, 11 WAS 10K, R3, 4 WAS 750 R6 WAS 510, R7 NOW 251 WAS 33K, R5 WAS 33K, Q4 WAS 75742, Q5 WAS 75747	7-16-84

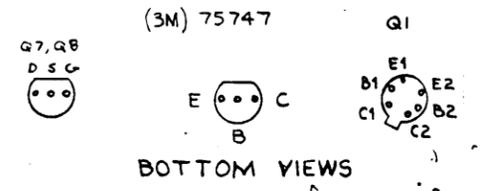
J3 HEAD CONN.  
 (VID) ERS. COIL +  
 (YEL) ERS. COIL -  
 (WHT) HEAD  
 (GRN) ERS. COIL P  
 (RED) CTR. TAP  
 (BLK) HEAD

J2 TACH. CONN.  
 (RED) TACH +  
 (BLK) TACH -

J1 CART. STALL CONNECTOR  
 (ART. SENSE - C) 1  
 (GROUND - NO) 2  
 (FILE PROT. - NO) 4  
 (FILE PROT. - C) 5  
 (FILE PROT. - NO) 6



- 4. PINS 1 AND 10 ON P1 ARE BOTH GROUND, BUT ARE NOT CONNECTED ON PC BOARD.
- 3. CAPACITORS - MICROFARADS
- 2. RESISTORS - OHMS, 1/4W, 5%
- ▽ DESIGNATES REFERENCE OF AMPLIFIER (IC 4) AT 6.0 VOLTS ABOVE GROUND.

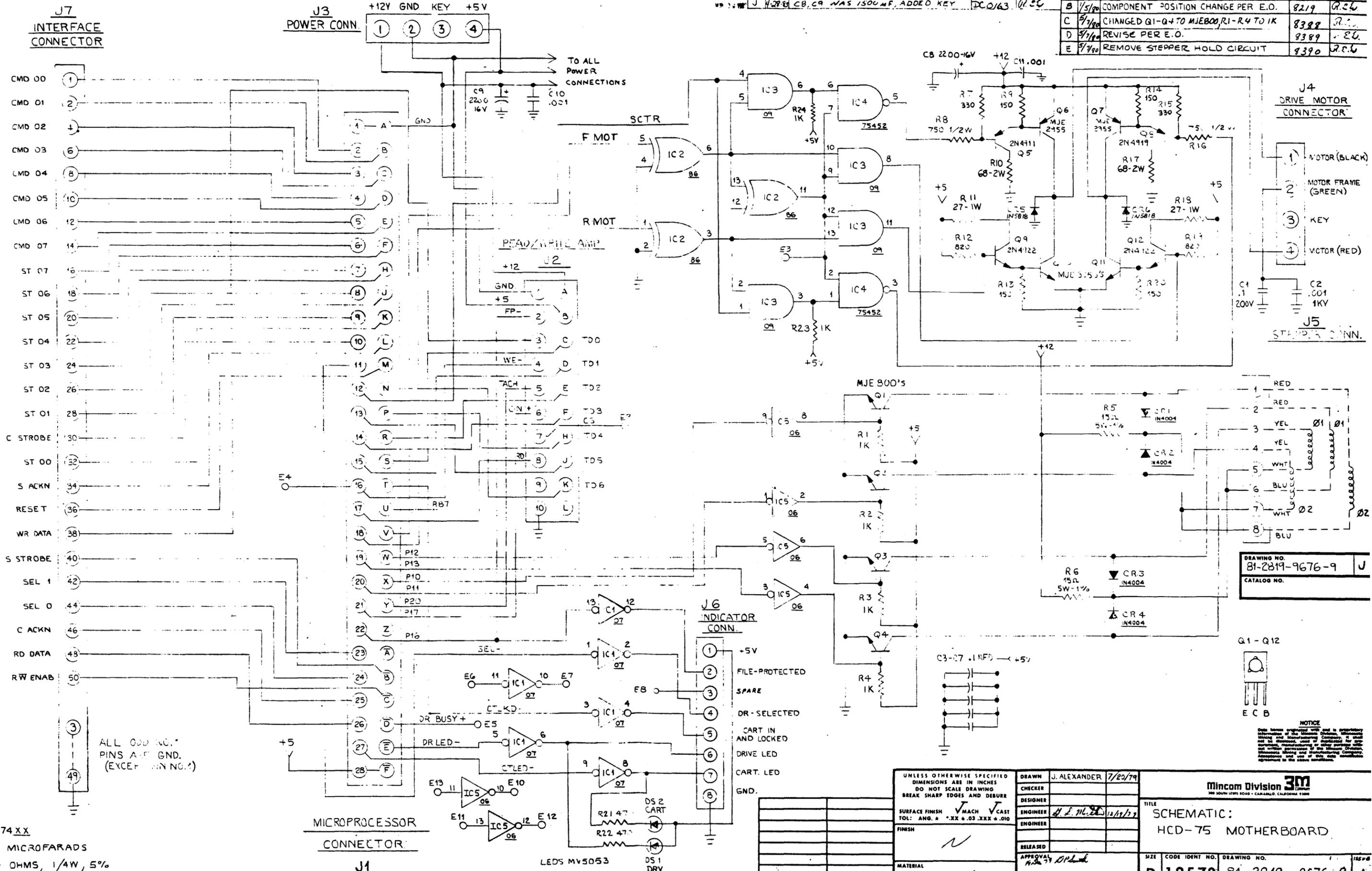


NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWING BREAK SHARP EDGES AND DEBURR		DRAWN J.ALEXANDER 12-15-79		Minicom Division 3M	
SURFACE FINISH √ MACH √ CAST TOL: ANG. & .XX & .03 .XXX & .010		CHECKER		TITLE SCHEMATIC: HCD-75 READ/WRITE AMPLIFIER	
FINISH		DESIGNED BY J.D. M... 12-18-79		SIZE CODE IDENT NO. DRAWING NO.	
MATERIAL		RELEASED		D 12578 81-2819-9677-7	
NEXT ASSY		APPROVAL 1/28/81 J.D. M...		SCALE WEIGHT SHEET 1 of 1	
APPLICATION		APPROVAL			

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REV	DATE	DESCRIPTION	BY	APPROVE
F	7/21/79	R11,R18 WAS 47-1/2W R10,R17 WAS 150-1W	GR20	
G	7/22/79	REMOVED F1 FUSE, ADD CONN. KEY	GR23	
H	8/1/79	CR5, CR6 WAS IN 4004	GR20	
J	7/27/79	CB, C9 WAS 150UF, ADDED KEY	DC063	
A	7/1/79	RELEASE FOR PRODUCTION	8195	GR26
B	7/5/79	COMPONENT POSITION CHANGE PER E.O.	8219	GR26
C	7/7/79	CHANGED Q1-Q4 TO MJE800, R1-R4 TO 1K	8388	GR26
D	7/7/79	REVISE PER E.O.	8389	GR26
E	7/7/79	REMOVE STEPPER HOLD CIRCUIT	9390	GR26



- 3. ALL IC'S ARE 74XX
- 2. CAPACITORS - MICROFARADS
- 1. RESISTORS - OHMS, 1/4W, 5%

NOTES: UNLESS OTHERWISE SPECIFIED

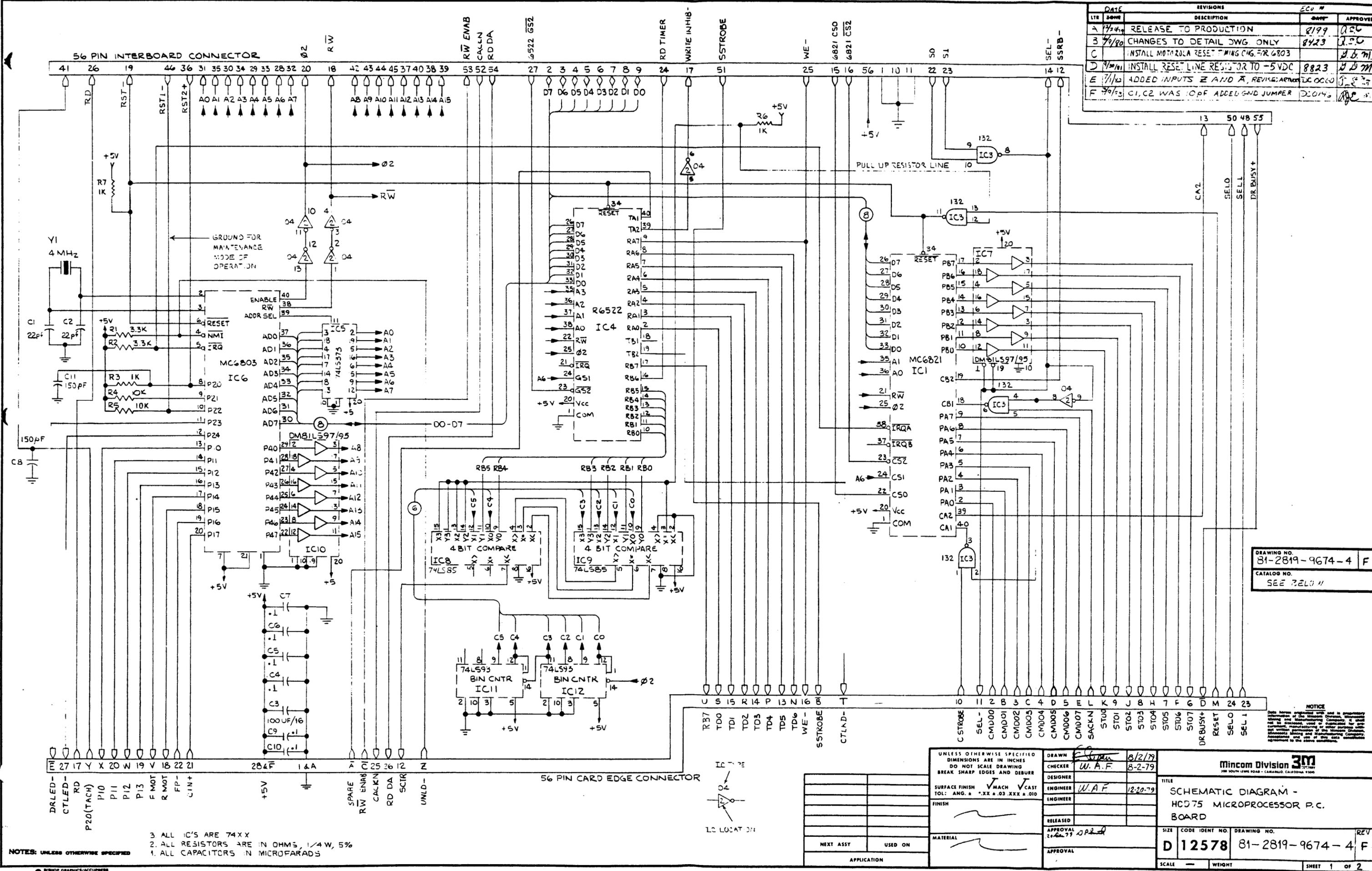
DRAWING NO. 81-2819-9676-9 J  
 CATALOG NO.

Q1 - Q12  
 E C B

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CHECKER		DESIGNER		TITLE	SCHEMATIC: HCD-75 MOTHERBOARD
ENGINEER		ENGINEER		SIZE	D 12578
RELEASED		APPROVAL		CODE IDENT NO.	81-2819-9676-9
APPROVAL		APPROVAL		DRAWING NO.	
APPROVAL		APPROVAL		ISSUE	
APPLICATION		MATERIAL		SCALE	
NEXT ASSY		USED ON		WEIGHT	
				SHEET	2

DATE		REVISIONS		ECO #	
LTR	DATE	DESCRIPTION	DATE	APPROVED	
A	7/24/79	RELEASE TO PRODUCTION	8199	RSC	
B	7/29/80	CHANGES TO DETAIL DWG ONLY	8423	RSC	
C		INSTALL MOTOROLA RESET TIMING CHG FOR 6803			
D	7/30/81	INSTALL RESET LINE RESISTOR TO -5VDC	8823	J.D.M.	
E	7/1/82	ADDED INPUTS Z AND A, REVISED	DC 0000	J.D.M.	
F	7/9/83	C1, C2 WAS COP ADDED GND JUMPER	DC 0143	J.D.M.	



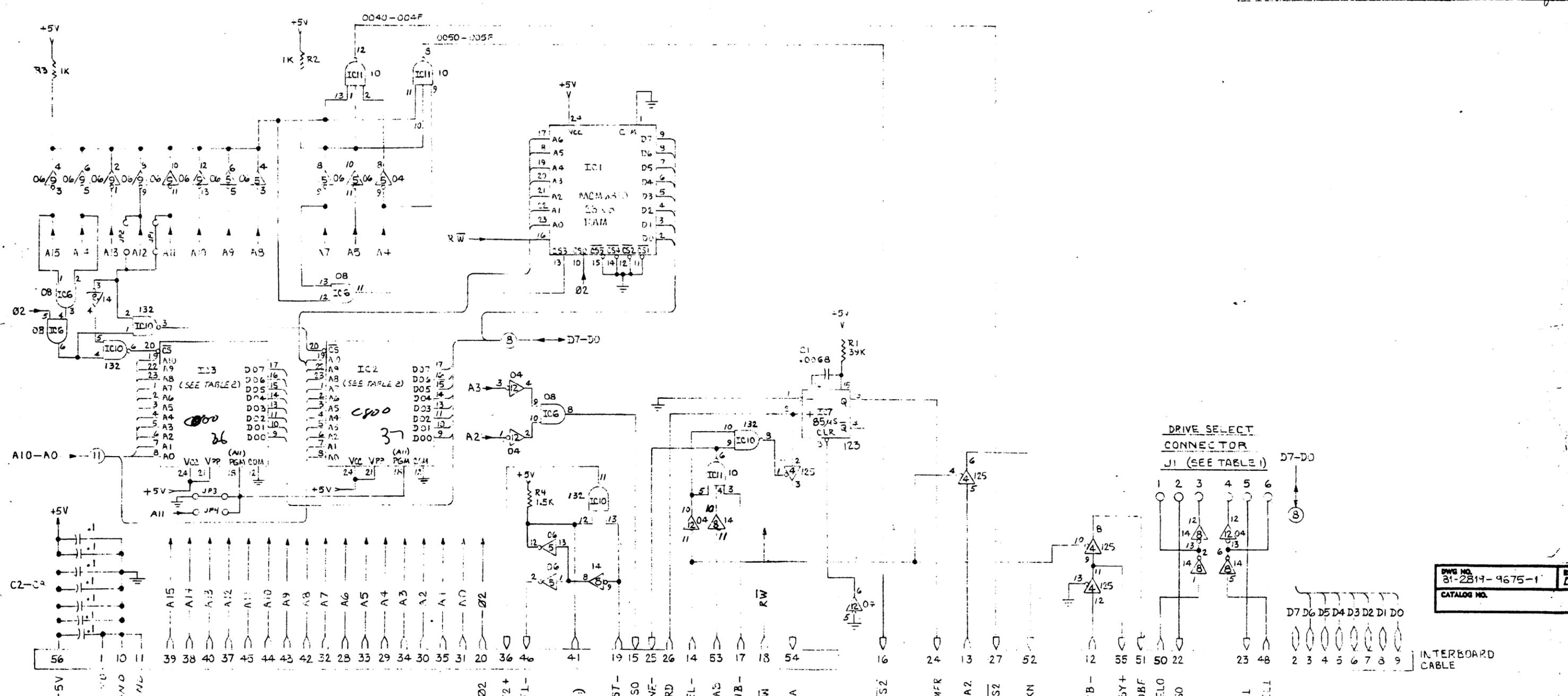
DRAWING NO. 81-2819-9674-4 F  
 CATALOG NO. SEE REL 11

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWING BREAK SHARP EDGES AND DEBURR		DRAWN: <i>[Signature]</i> 8/2/79 CHECKER: W.A.F. 8-2-79 DESIGNER: W.A.F. ENGINEER: W.A.F. 12-20-79 RELEASED: <i>[Signature]</i> APPROVAL: <i>[Signature]</i>	<b>Minicom Division 3M</b> 390 SOUTH LEWIS ROAD - CARROLL, CALIFORNIA 95006 TITLE: SCHEMATIC DIAGRAM - HCD75 MICROPROCESSOR P.C. BOARD
SURFACE FINISH: $\sqrt{\text{MACH}}$ $\sqrt{\text{CAST}}$ TOL: ANG. ± .XX ± .03 .XXX ± .010 FINISH: <i>[Signature]</i> MATERIAL: <i>[Signature]</i>		RELEASED: <i>[Signature]</i> APPROVAL: <i>[Signature]</i>	SIZE: D 12578 CODE IDENT NO.: 81-2819-9674-4 F DRAWING NO.: 81-2819-9674-4 F REV: F SCALE: — WEIGHT: — SHEET 1 OF 2

NOTES: UNLESS OTHERWISE SPECIFIED  
 3. ALL IC'S ARE 74XX  
 2. ALL RESISTORS ARE IN OHMS, 1/4W, 5%  
 1. ALL CAPACITORS IN MICROFARADS

DATE		REVISIONS	DATE	APPROVED
SYM	ZONE	DESCRIPTION		
A	1/24/79	RELEASE TO PRODUCTION	8201	W.A.F.
B	7/16/79	REVISE DRAWING	8413	W.A.F.
C	9/20/79	INSTALL MOTOROLA RESETTIMING CHG. FOR 6903	8827	W.A.F.
D	11/1/79	ADDED JPI-4, TABLE 2	10114	W.A.F.



**TABLE 1**  
DRIVE SELECT

DRIVE NO.	JUMPER
1	1-2, 5-6
2	1-2, 4-5
3	2-3, 5-6
4	2-3, 4-5

**TABLE 2**  
PROM ADDRESSING

JUMPER	TYPE	LOC.	ADDR.
JPI.3	2716	IC2	C800-CFFF
		IC3	C000-C7FF
JP2.4	2532	IC2	F000-FFFF
		IC3	E000-EFFF

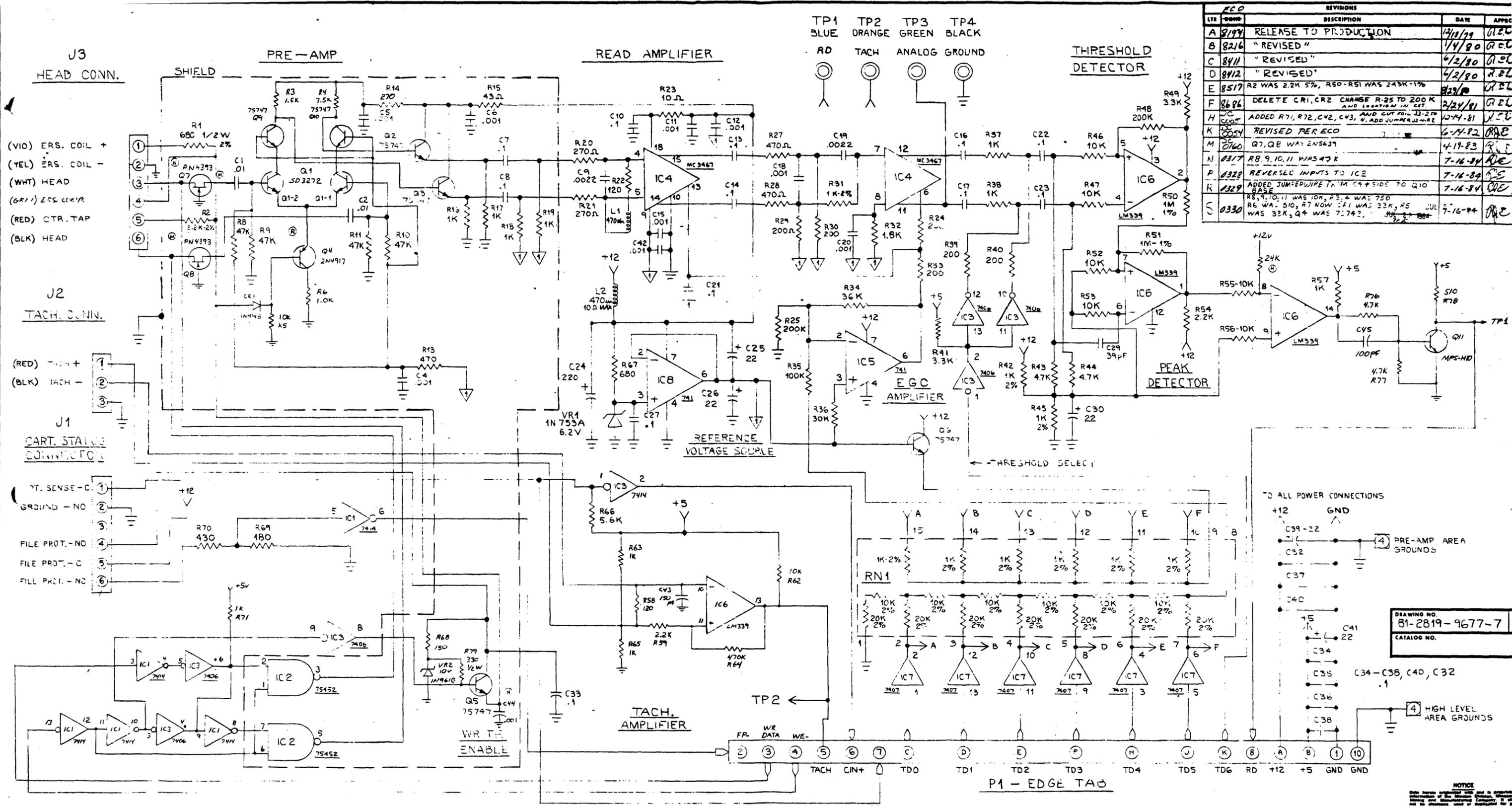
3- ALL IC'S 74XX  
 2- ALL RESISTORS OHMS 1/4W 5%  
 1- ALL CAPACITORS ARE IN UF  
 NOTES: UNLESS OTHERWISE SPECIFIED

DWG NO. 81-2819-9675-1  
 CATALOG NO.   
 INTERBOARD CABLE

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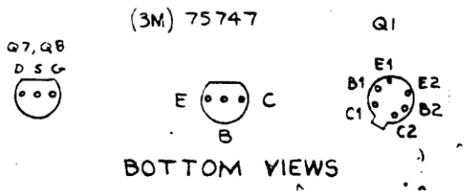
UNLESS OTHERWISE SPECIFIED		DRAWN	W.A.F.	12-5-79
ALL DIMENSIONS IN INCHES		CHECK	W.A.F.	12-5-79
ALL THREADS PER MIL-S-7742		DES APPR		
SURFACE FINISH PER MIL-STD-18		ENG APPR	W.A.F.	12-20-79
TOLERANCES		INS APPR		
ANG ± 5° JOK ± .01 JOK ± .010		RELEASED		
BREAK SHARP EDGES & DEBURR		APPROVAL		
DO NOT SCALE DRAWING		APPROVAL		
FINISH				
MATERIAL				
SCALE				
WEIGHT				

**3M Minicom Division**  
 TITLE: SCHEMATIC DIAGRAM  
 HCD75 PROM MEMORY P.C. BOARD  
 CODE IDENT NO. 12578  
 SIZE D  
 DRAWING NO. 81-2819-9675-1



REV	DATE	DESCRIPTION	BY	CHKD
A	9/17/79	RELEASE TO PRODUCTION	J.A.	DRS
B	8/21/80	"REVISED"	J.A.	REL
C	8/11/80	"REVISED"	J.A.	REL
D	8/12/80	"REVISED"	J.A.	REL
E	8/17/80	R2 WAS 2.2K 5%, R50-R51 WAS 243K-1%	J.A.	REL
F	8/29/81	DELETE CRI, CR2 CHANGE R-25 TO 200K AND LOCATION IN SET.	J.A.	REL
H	10/14/81	ADDED R71, R72, C42, C43, 4. ADD JUMPER J3-R2 BASE	J.A.	REL
K	6/14/82	REVISED PER ECO	J.A.	REL
M	4-17-83	Q7, Q8 WAS 2N5637	J.A.	REL
N	7-16-84	REVERSED INPUTS TO IC2	J.A.	REL
P	7-16-84	ADDED JUMPER WIRE FROM C4 SIDE TO Q10	J.A.	REL
S	7-16-84	R8, R9, R10, R11 WAS 10K, R2, R4 WAS 750, R6 WAS 510, R7 NOW R1 WAS 33K, R5 WAS 33K, Q4 WAS 7-742.	J.A.	REL

- 4. PINS 1 AND 10 ON P1 ARE BOTH GROUND, BUT ARE NOT CONNECTED ON PC BOARD.
- 3. CAPACITORS - MICROFARADS
- 2. RESISTORS - OHMS, 1/4W, 5%
- ▽ DESIGNATES REFERENCE OF AMPLIFIER (IC4) AT 6.0 VOLTS ABOVE GROUND.



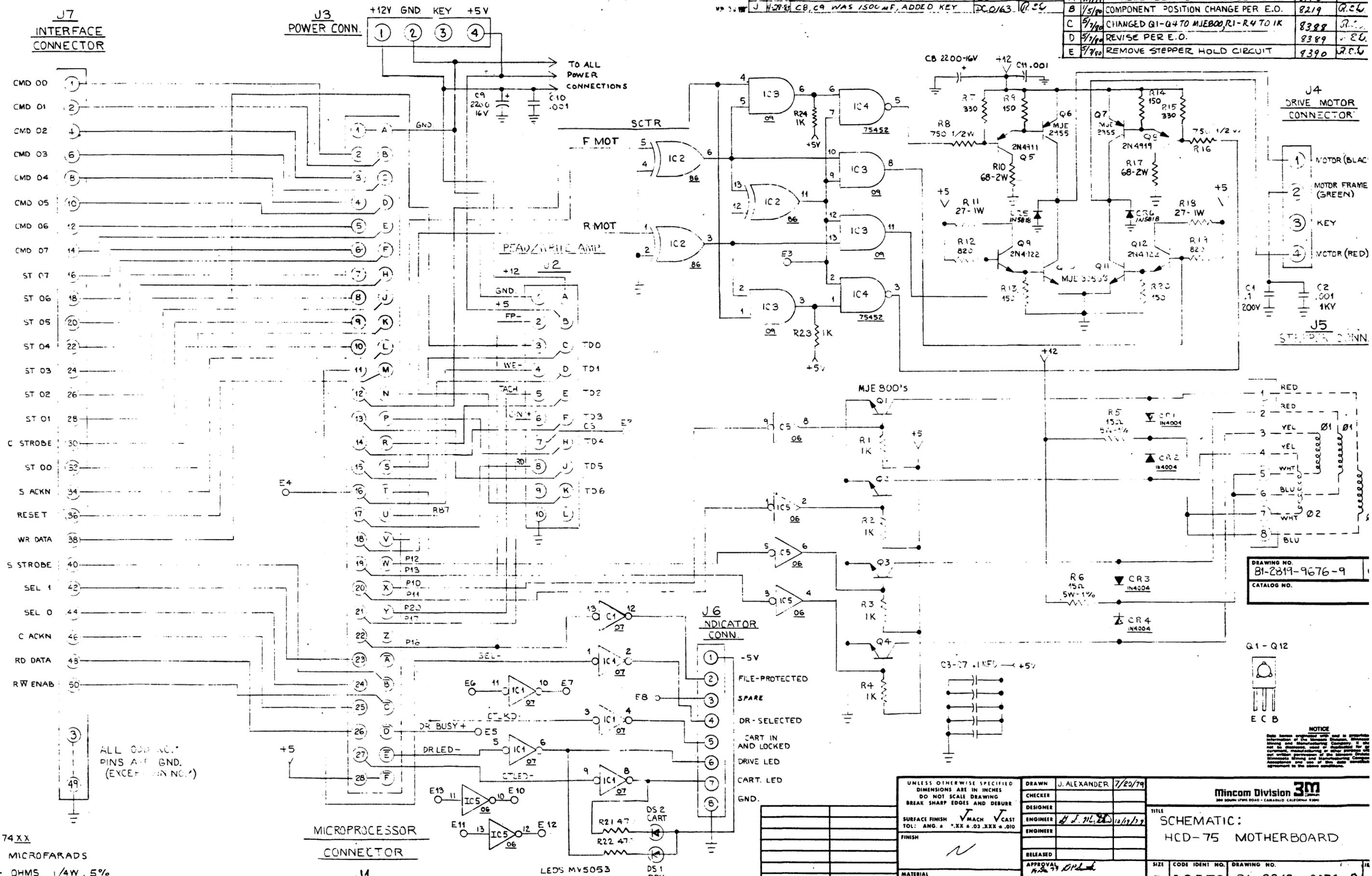
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWING BREAK SHARP EDGES AND DEBUR		DRAWN	J.ALEXANDER	12-15-79
SURFACE FINISH √ MACH √ CAST TOL: ANG. ± .XX ± .01 .XXX ± .00		CHECKER		
FINISH		DESIGNER	H.J. MSLC	12-18-79
MATERIAL		ENGINEER		
NEXT ASSY		RELEASED		
USED ON		APPROVAL	J.A.	
APPLICATION		APPROVAL		

DRAWING NO. 81-2819-9677-7		CATALOG NO.	
TITLE SCHEMATIC: HCD-75 READ/WRITE AMPLIFIER		SIZE	CODE IDENT NO.
D 12578		81-2819-9677-7	
SCALE	VERSION	SHEET	OF 2

REV. NO.		DATE	DESCRIPTION	BY	APPROV.
F	7/21/79		R11, R18 WAS 47-1/2W R10, R17 WAS 150-1W	8493	J.A.
G	7/22/79		REMOVED F1 FUSE, ADD CONN. KEY	8723	J.A.
H	8/11/79		CR5, CR6 WAS IN4004	8800	J.A.
J	11/29/79		CB, C9 WAS 150UF, ADDED KEY	DC0163	J.A.

REV.	DATE	DESCRIPTION	BY	APPROV.
A	11/11/79	RELEASE FOR PRODUCTION	8195	J.A.
B	1/5/80	COMPONENT POSITION CHANGE PER E.O.	8219	J.A.
C	5/7/80	CHANGED Q1-Q4 TO MJE800, R1-R4 TO 1K	8388	J.A.
D	5/7/80	REVISE PER E.O.	8389	J.A.
E	5/7/80	REMOVE STEPPER HOLD CIRCUIT	8390	J.A.



1. RESISTORS - OHMS, 1/4W, 5%
2. CAPACITORS - MICROFARADS
3. ALL IC'S ARE 74XX

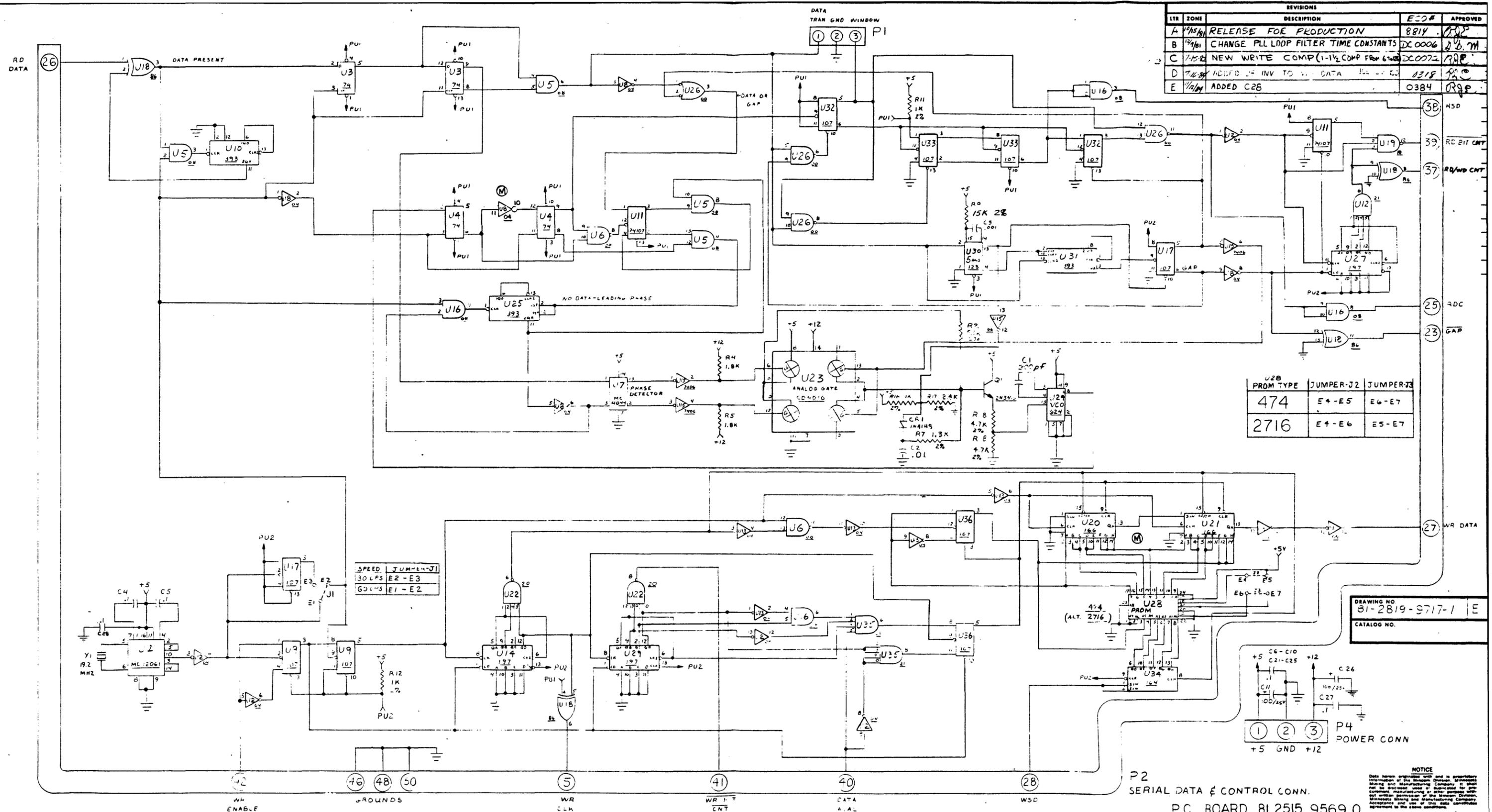
NOTES: UNLESS OTHERWISE SPECIFIED

DRAWING NO. 81-2819-9676-9  
 CATALOG NO.

NOTICE  
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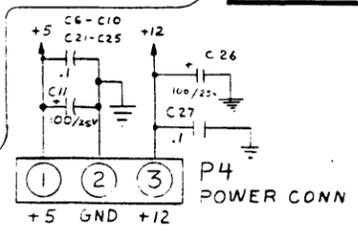
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWING BREAK SHARP EDGES AND DEBURR		DRAWN J. ALEXANDER 7/20/79		Mincom Division 3M	
CHECKER		DESIGNER		TITLE SCHEMATIC: HCD-75 MOTHERBOARD	
ENGINEER		ENGINEER		SIZE	CODE IDENT NO. DRAWING NO.
FINISH		RELEASED		D	12578 81-2819-9676-9
MATERIAL		APPROVAL		SCALE	WEIGHT
NEXT ASSY	USED ON	APPROVAL		SHEET	OF
APPLICATION					

REV	ZONE	DESCRIPTION	ECO#	APPROVED
A	1/15/81	RELEASE FOR PRODUCTION	8814	[Signature]
B	1/19/81	CHANGE PLL LOOP FILTER TIME CONSTANTS	DC0006	[Signature]
C	1-15-81	NEW WRITE COMP (1-1/2 COMP FROM 6-1/2)	DC0072	[Signature]
D	1-16-81	ADDED 2F INV TO DATA	1218	[Signature]
E	1/16/81	ADDED C28	0384	[Signature]



PROM TYPE	JUMPER-J2	JUMPER-J3
474	E4-E5	E6-E7
2716	E4-E6	E5-E7

DRAWING NO  
81-2819-9717-1 E  
CATALOG NO.



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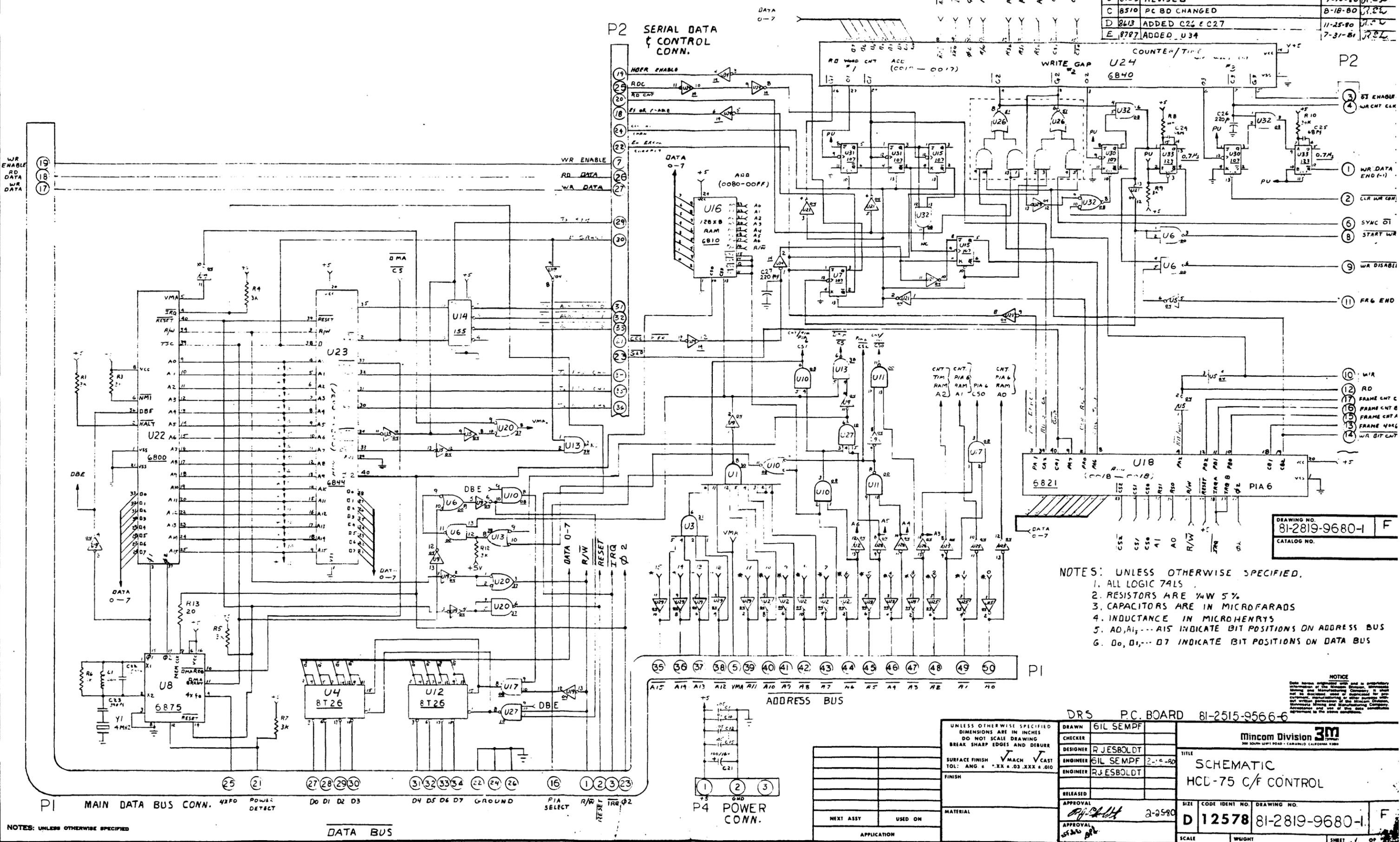
- 6. PUI PULL UP SOURCE R11
- 5. PU2 PULL UP SOURCE R12
- 4. PC BOARD 81-2515-9569-0
- 3. IC'S 74LS SERIES
- 2. CAPACITORS MICROFARADS
- 1. RESISTORS OHMS 1/4W 5%

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWING BREAK SHARP EDGES AND DEBURR		DRAWN: GLICHAUER 10-12-81		Minicom Division 3M	
SURFACE FINISH: V MACH V CAST TOL: ANG & *XX & .03 .XXX & .010		CHECKER: [Signature] 11-12-81		TITLE: SCHEMATIC	
FINISH		DESIGNER: [Signature]		HCD-75 C/F ENCODE/DECODE	
MATERIAL		ENGINEER: [Signature]		60 IPS	
NEXT ASSY		RELEASED		SIZE: D 12578	
USED ON		APPROVAL		CODE IDENT NO: 81-2819-9717-1	
APPLICATION		APPROVAL		DRAWING NO: E	
				SCALE: ~ WEIGHT: SHEET 1 OF 2	

F 0319 REVISED CRC FF CIRCUIT, REMOVED RESET FROM U16, MOVE DMA FROM IRQ AT U15. 7-16-80 JLE

REVISIONS				
REV	ZONE	DESCRIPTION	DATE	APPROVE
A	0277	RELEASE FOR PRODUCTION	2-25-80	RJS
B	8453	REVISED	7-10-80	JLE
C	8510	PC BOARD CHANGED	8-18-80	JLE
D	8613	ADDED C26 & C27	11-25-80	JLE
E	8787	ADDED U34	7-31-81	JLE



- NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL LOGIC 74LS
  2. RESISTORS ARE 1/4W 5%
  3. CAPACITORS ARE IN MICROFARADS
  4. INDUCTANCE IN MICROHENRYS
  5. A0, A1, ... A15 INDICATE BIT POSITIONS ON ADDRESS BUS
  6. D0, D1, ... D7 INDICATE BIT POSITIONS ON DATA BUS

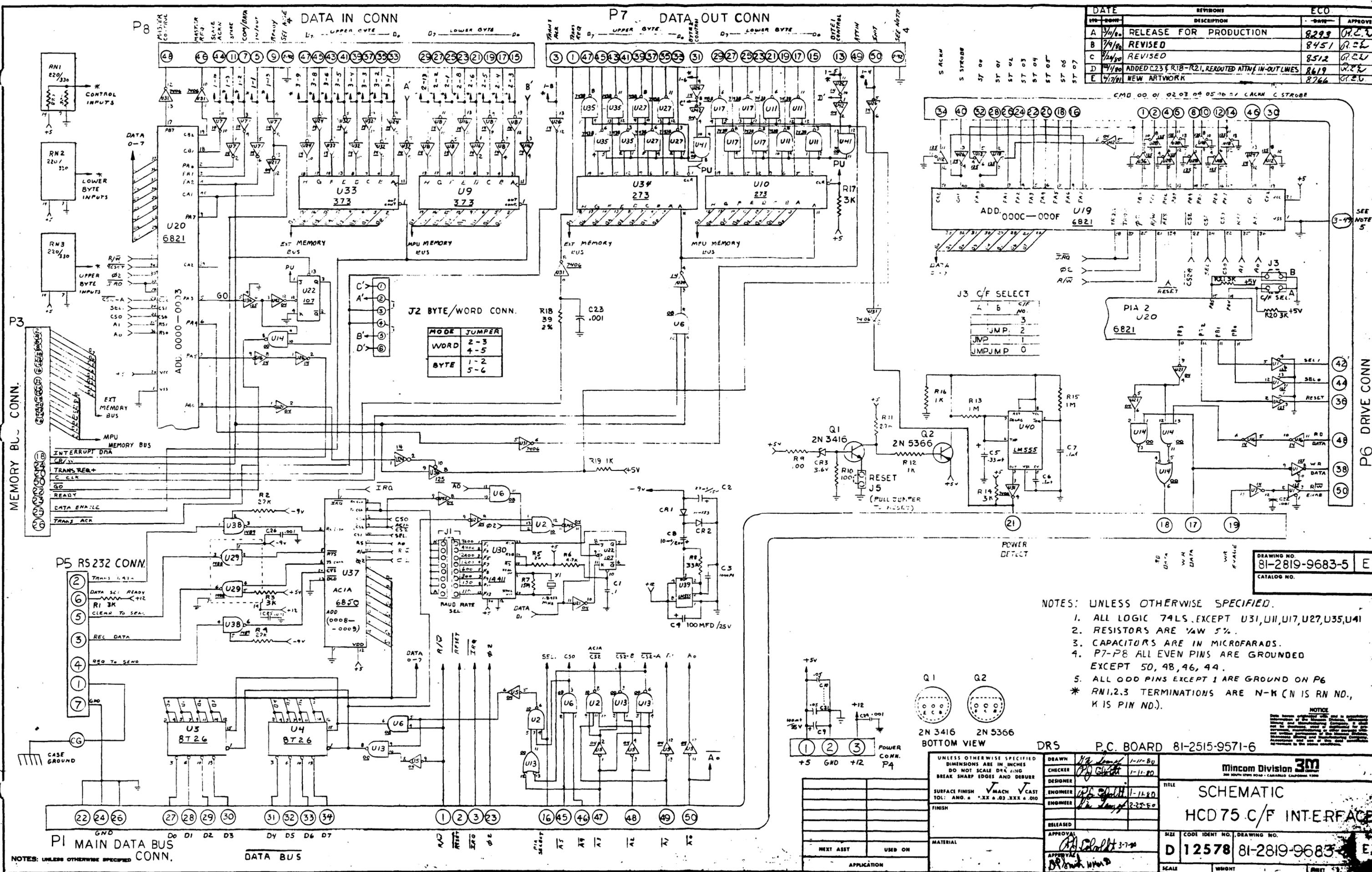
DRAWING NO. 81-2819-9680-1 F  
CATALOG NO.

DRS PC BOARD 81-2515-9566-6

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWING BREAK SHARP EDGES AND DEBURR		Minicom Division 3M	
DRAWN	GIL SEMPFF	TITLE	SCHMATIC
CHECKER		SIZE	D 12578
DESIGNER	R JESBOLDT	CODE IDENT NO.	81-2819-9680-1
ENGINEER	GIL SEMPFF	DRAWING NO.	F
ENGINEER	R JESBOLDT	SCALE	
RELEASED		WEIGHT	
APPROVAL		SHEET	1 / 1
APPROVAL		OP	

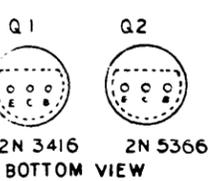
NOTES: UNLESS OTHERWISE SPECIFIED





DATE	REVISIONS	ECO
A 3/10/80	RELEASE FOR PRODUCTION	8299 J.C.L.
B 7/9/80	REVISED	8451 J.C.L.
C 1/14/80	REVISED	8512 J.C.L.
D 4/1/80	ADDED C23, R18-R21, REROUTED ATTN. IN-OUT LINES	8619 J.C.L.
E 7/7/81	NEW ARTWORK	8766 J.C.L.

- NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL LOGIC 74LS EXCEPT U31, U11, U17, U27, U35, U41
  2. RESISTORS ARE 1/4W 5%.
  3. CAPACITORS ARE IN MICROFARADS.
  4. P7-P8 ALL EVEN PINS ARE GROUND EXCEPT 50, 48, 46, 44.
  5. ALL ODD PINS EXCEPT 1 ARE GROUND ON P6
- \* RN1,2,3 TERMINATIONS ARE N-K (N IS RN NO., K IS PIN NO.).

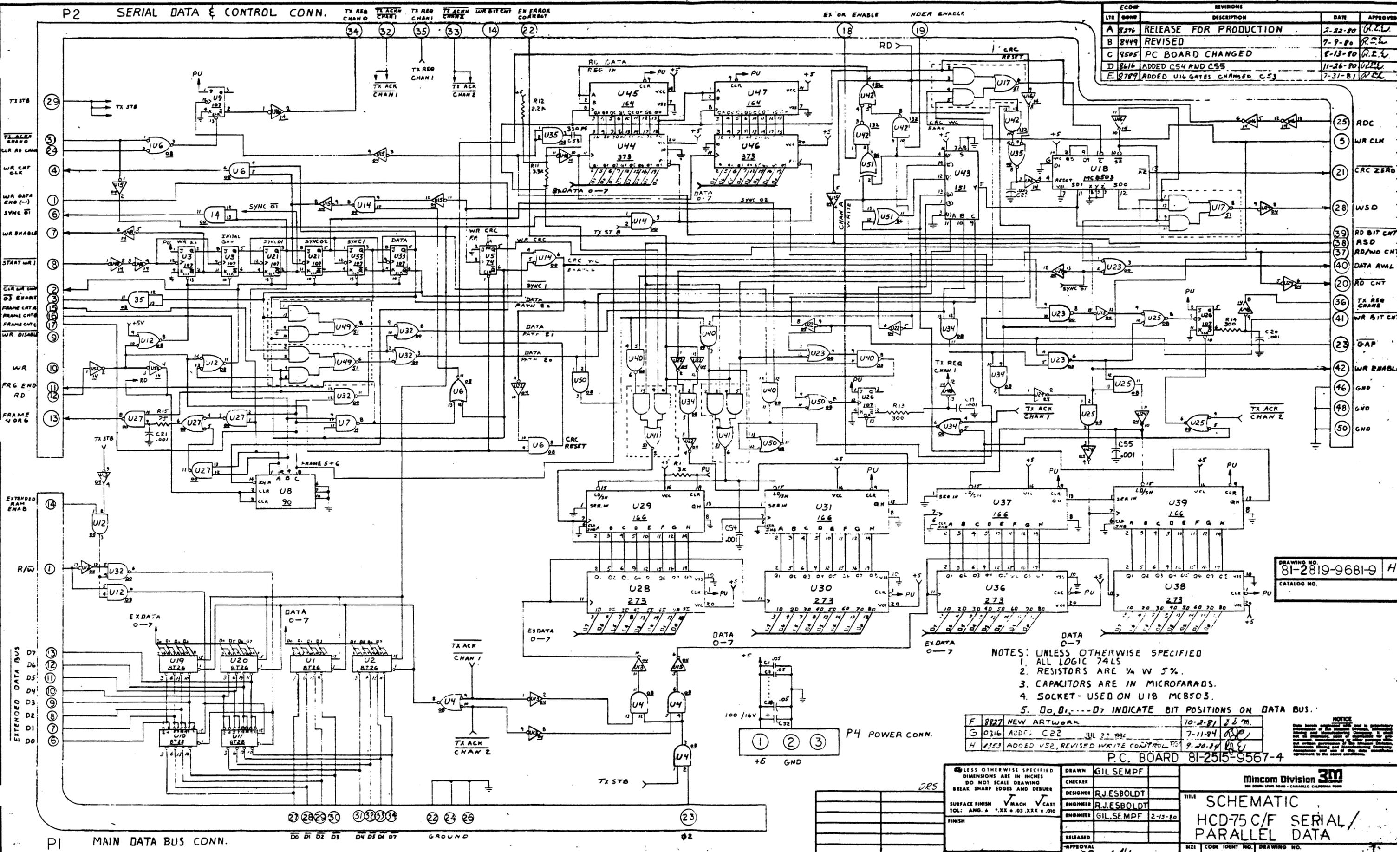


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWING BREAK SHARP EDGES AND DEBURR		DRAWN	1-11-80	Minicom Division 3M 200 SOUTH STURGE ROAD - CARROLLVILLE, CALIFORNIA 95959
SURFACE FINISH ✓ MACH ✓ CAST TOL: ANG. & .XX & .03 .XXX & .010		CHECKER	1-11-80	
FINISH		DESIGNER	1-11-80	TITLE <b>SCHMATIC</b> <b>HCD75 C/F INTERFACE</b>
		ENGINEER	2-25-80	
RELEASED		ENGINEER		SIZE CODE IDENT NO. DRAWING NO. <b>D 12578 81-2819-9683</b>
APPROVAL		RELEASED		SCALE
NEXT ASST	USED ON	APPROVAL		WHIGHT
APPLICATION				

NOTES: UNLESS OTHERWISE SPECIFIED

DRAWING NO. 81-2819-9683-5 E  
CATALOG NO.

P2 SERIAL DATA & CONTROL CONN.



ECOM	REVISIONS	DATE	APPROVED
A 8276	RELEASE FOR PRODUCTION	2-22-80	R.E.L.
B 8449	REVISED	7-9-80	R.E.L.
C 9505	PC BOARD CHANGED	8-13-80	R.E.L.
D 8616	ADDED CS4 AND CS5	11-26-80	R.E.L.
E 8789	ADDED U16 GATES CHANGED CS3	7-31-81	R.E.L.

DRAWING NO. 81-2819-9681-9 H  
 CATALOG NO.

- NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL LOGIC 74LS
  2. RESISTORS ARE 1/4 W 5%.
  3. CAPACITORS ARE IN MICROFARADS.
  4. SOCKET-USED ON U18 MC8503.
  5. D0, D1, ... D7 INDICATE BIT POSITIONS ON DATA BUS.

F 8827	NEW ARTWORK	10-2-81	J.E.M.
G 0316	ADDED C22	7-11-84	R.E.L.
H 1553	ADDED U52, REVISED WRITE CONTROL	9-20-84	R.E.L.

P.C. BOARD 81-2515-9567-4

SURFACE FINISH TOL: ANG. & .XX & .03 .XXX & .010 FINISH	DRAWN	GIL SEMPF	TITLE SCHEMATIC HCD-75 C/F SERIAL/ PARALLEL DATA
	CHECKER		
	DESIGNER	R.JESBOLDT	
	ENGINEER	R.JESBOLDT	
RELEASED		2-13-80	SIZE CODE IDENT NO. DRAWING NO. D 12578 81-2819-9681-9 H
APPROVAL	APPROVAL 2-22-80		SCALE WEIGHT

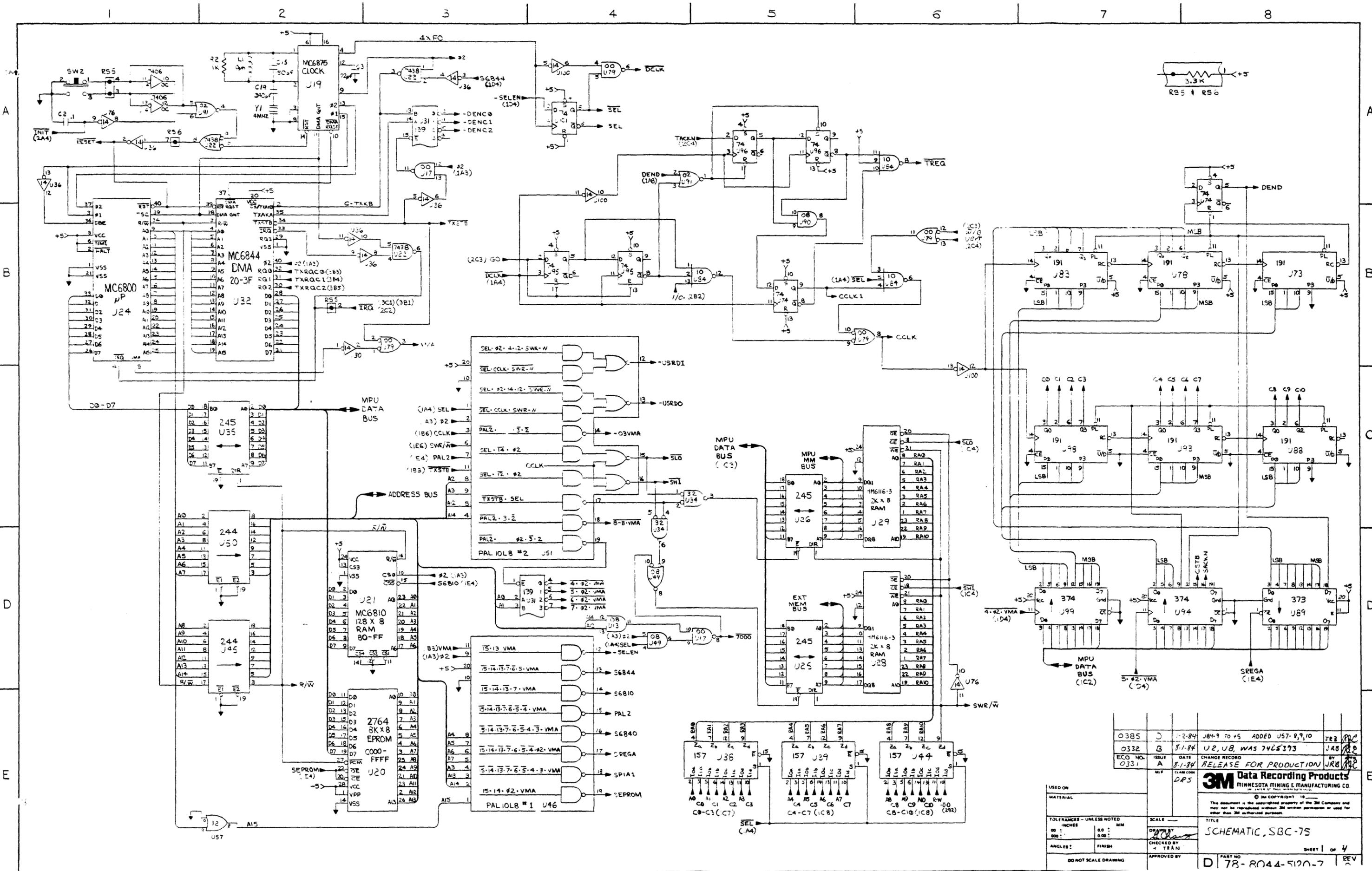
NOTES: UNLESS OTHERWISE SPECIFIED

DATA BUS

P1 MAIN DATA BUS CONN.

P4 POWER CONN.

Minicom Division 3M



0385	D	1-2-84	J849 TO +5	ADDED U57, 9, 10	JR2	JRC
0332	B	5-1-84	U2, U8, WAS 74LS393		JAR	JRC
ECO NO.	A	DATE	CHANGE RECORD	RELEASE FOR PRODUCTION	JRB	JRC
0331	A	8-1-84			JRB	JRC

**3M Data Recording Products**  
MINNESOTA MINING & MANUFACTURING CO.

USED ON: MATERIAL: \_\_\_\_\_

TOLERANCES - UNLESS NOTED: 0.0 INCHES / 0.0 MM, 0.00 INCHES / 0.00 MM, ANGLES: FINISH

SCALE: \_\_\_\_\_

TITLE: SCHEMATIC, SBC-75

DRAWN BY: \_\_\_\_\_

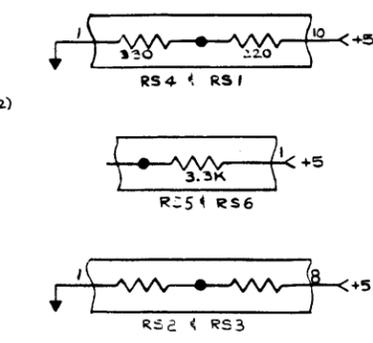
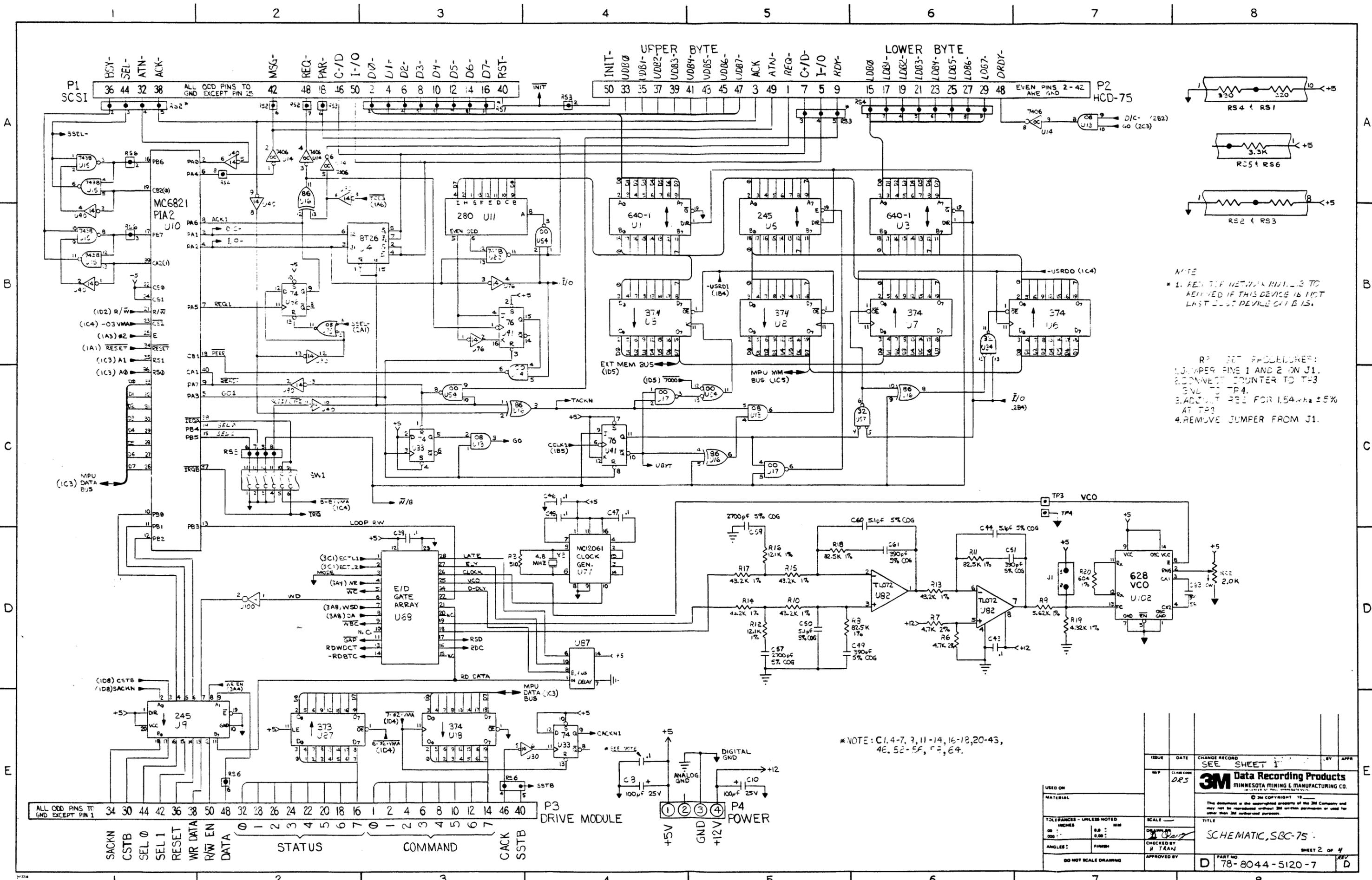
CHECKED BY: \_\_\_\_\_

APPROVED BY: \_\_\_\_\_

PART NO: D 78-8044-510-7

SHEET 1 of 4

REV: \_\_\_\_\_

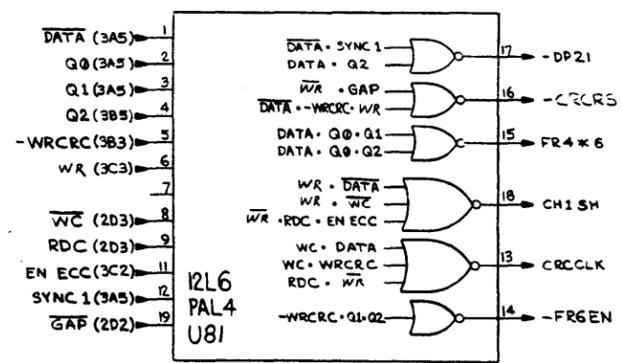
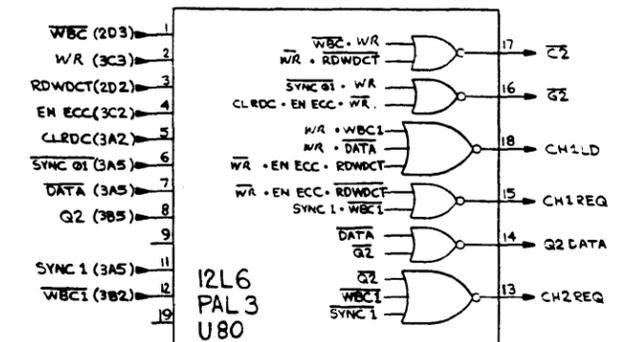
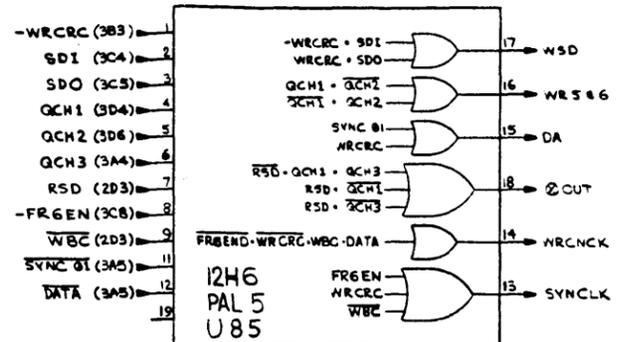
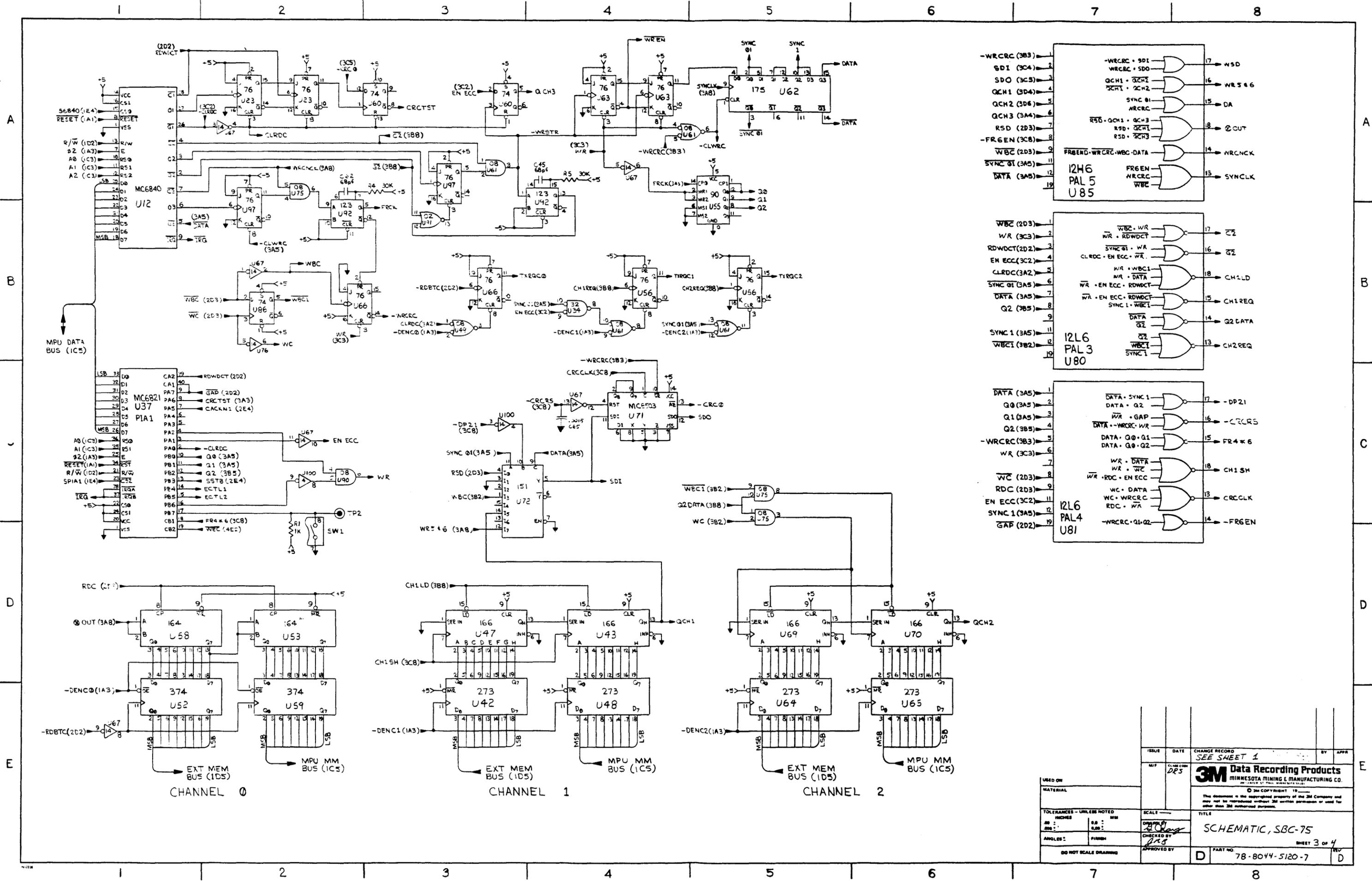


NOTE  
 \* 1. REMOVE NETWORK R11, L2 TO  
 REMOVED IF THIS DEVICE IS NOT  
 LAST TEST DEVICE ON B15.

RA SET PROCEDURES:  
 1. JUMPER PINS 1 AND 2 ON J1.  
 2. CONNECT COUNTER TO TP3  
 3. ENL TO TP4.  
 4. ADJUST R22 FOR 1.54 MHz ± 5%  
 AT TP3  
 5. REMOVE JUMPER FROM J1.

\* NOTE: C1, 4-7, 7, 11-14, 16-18, 20-43,  
 4E, 5E-5F, F, E4.

ISSUE	DATE	CHANGE RECORD	SHEET 1	BY	APPR
M/P	CLS CODE	DRS	3M Data Recording Products		
MINNESOTA MINING & MANUFACTURING CO.					
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TOLERANCES - UNLESS NOTED		SCALE		TITLE	
INCHES	0.005	AS SHOWN		SCHEMATIC, SBC-75	
ANGLES	FINISH	DRAWN BY		CHECKED BY	
		H. T. AM		H. T. AM	
DO NOT SCALE DRAWING		APPROVED BY		PART NO	
		D		78-8044-5120-7	
				SHEET 2 OF 4	
				REV D	



ISSUE	DATE	CHANGE RECORD	BY	APPR
		SEE SHEET 1		
M/F	CLM CON	3M Data Recording Products		
MINNESOTA MINING & MANUFACTURING CO.				
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TOLERANCES - UNLESS NOTED	SCALE	TITLE		
INCHES	AS SHOWN	SCHEMATIC, SBC-75		
ANGLES	FINISH	SHEET 3 OF 4		
DO NOT SCALE DRAWING		APPROVED BY	PART NO.	REV
			78-8044-5120-7	D



**Important Notice:**

*3M warrants the equipment covered hereby to be free from defects in material and workmanship for twelve (12) months from date of original shipment to purchaser. During this warranty period 3M will repair or replace defective equipment FOB its place of business without charge to purchaser.*

*This warranty applies to defects arising out of normal use and service of the equipment as specified by 3M. This warranty does not cover abnormal operation of the equipment, accident, alteration, negligence, misuse and repairs or servicing performed by other than 3M authorized representatives. Purchaser shall upon request by 3M, furnish reasonable evidence that the defect arose from causes placing a liability on 3M. If the defect did not arise from causes placing a liability on 3M, purchaser shall reimburse 3M for expenses incurred in inspecting the equipment at the request of purchaser.*

*The obligation of 3M under this warranty is limited to repair or replacement of the defective equipment and is the only warranty applicable to the equipment. 3M shall not be liable for any injury, loss or damage direct or consequential arising out of the use of or inability to use the product. No changes in the warranty shall be effective without the prior approval in writing of both parties. This warranty and obligations and liabilities thereunder shall replace all warranties or guarantees express or implied arising by law or otherwise, including the implied warranty of merchantability.*

**Data Recording Products Division/3M**

223-5N 3M Center  
St. Paul, Minnesota 55144

