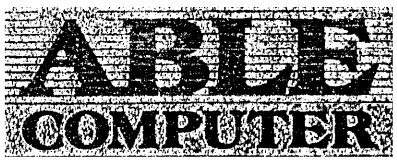
# QNIVERTER
## User's Guide

10067X07

APRIL 1981



# QNIVERTER
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# SECTION 1
# HOW TO USE THIS MANUAL

Congratulations on your purchase of a QNIVERTER from ABLE COMPUTER. We are sure that it will provide you with years of satisfactory service. We have prepared this manual to help you maximize the effectiveness of the QNIVERTER in your system.

This manual is provided to assist you with the installation, use, and care of QNIVERTER; it does not provide repair information. If you have problems with your QNIVERTER, we prefer that you let us repair it in our factory.

This manual assumes that you are familiar with the PDP-11 Unibus and LSI-11 Q Bus architecture. For information about these architectures, refer to the following DEC documents:

- *PDP-11 Processor Handbook*
- *PDP-11 Peripherals Handbook*
- *PDP-11 Terminals and Communications Handbook*
- *Microcomputer Handbook*

This manual is organized into the following sections:

- Section 2 describes the QNIVERTER including its features and specifications.
- Section 3 explains how to install QNIVERTER.
- Section 4 provides troubleshooting tips and tells who to call for service.
- Section 5 provides application information.
- Section 6 contains programming information.
- Section 7 describes how QNIVERTER works.
- Appendix A provides Q Bus connector assignments.
- Appendix B lists Unibus connector assignments.
- Appendix C provides a list of spare parts.
- Appendix D contains the QNIVERTER list of materials.

# SECTION 2
# WHAT IS QNIVERTER ?

## 2.1 GENERAL DESCRIPTION

The QNIVERTER is a quad-width board (see Figure 2-1) that performs one of two functions:

- Permits an LSI-11/2, LSI-11/23, or PDP-11/03 computer system to access Unibus compatible controllers and memories. The LSI-11 remains as bus arbitrator and all latency specifications are bound by the LSI-11.

- Permits a PDP-11 Unibus system to access LSI-11 compatible controllers and memories. The bus arbitration is performed by the Unibus CPU.

With QNIVERTER, memories and controllers may reside on both the Unibus and Q Bus. NPR data transfers are supported across the QNIVERTER in either direction.

The QNIVERTER installs into a quad slot of an LSI-11 backplane. A pair of Unibus connectors on the board provide connection to a Unibus cable (not supplied). The QNIVERTER's dual functions are easily user selected.

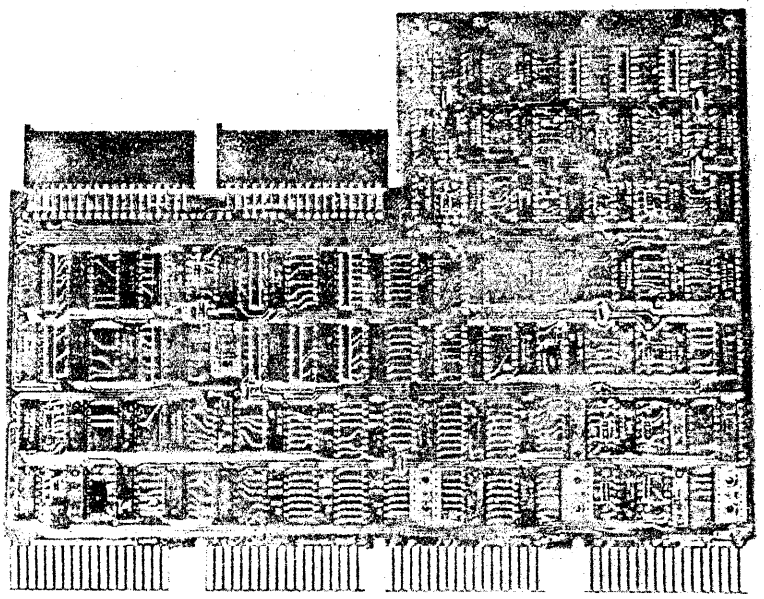

Figure 2-1: QNIVERTER, Model 10067

## 2.2 FEATURES

QNIVERTER provides the user with a choice of applications which allow:

- Readily available Unibus devices to be used on an LSI-11 computer system, or
- Less expensive and more compact LSI-11 devices to be used on a Unibus computer system.

QNIVERTER supports the features of the LSI-11/23 including:

- Four-level interrupt structure
- Memory parity
- Full 256K byte addressing.

QNIVERTER is software transparent to the host computer.

As an added bonus, QNIVERTER provides extended bus load capabilities:

- Q Bus drive capability equivalent to an LSI-11 computer can be added to a Unibus computer system, or
- 19 Unibus loads can be added to an LSI-11 computer system.

## 2.3 SPECIFICATIONS

### 2.3.1 ELECTRICAL SPECIFICATIONS

Bus loading: -1 Unibus load
-1 LSI bus load

Drive Capability: -19 Unibus loads to include 50 feet of cable or less
-LSI drive capability equivalent to an LSI-11 computer

Power Required: -In a Unibus computer system--3.2 amps @ +5 volts (which includes the Q bus terminator), ±12 volts is not required.
-In an LSI-11 computer system--2.5 amps @ +5 volts.

### 2.3.2 PHYSICAL SPECIFICATIONS

Size: Standard quad-width module measuring 10.45 x 8.40 inches (excluding handles).

External Connection: Two connectors compatible with a standard Unibus extender cable.

# SECTION 3
# HOW TO INSTALL QNIVERTER

## 3.1 UNPACKING QNIVERTER

QNIVERTER is shipped in a special container to prevent any damage during shipment. Unpack it carefully and verify that no damage has occurred. If there is damage, notify the carrier immediately. Save the shipping carton to show proof of damage or in case the product requires shipment.

## 3.2 VERIFY THAT YOU RECEIVED WHAT YOU ORDERED

Be sure that you have received the correct order by checking the product number on the component side of the board near the handles. The QNIVERTER product number is 10067. (See photo on page 2-1.)

If you have not received the correct equipment, notify our factory immediately.

## 3.3 USING QNIVERTER WITH A PDP-11 SYSTEM

The QNIVERTER is shipped ready for installation in conjunction with a PDP-11 computer system. For use with an LSI-11 computer system, refer to paragraph 3.4. To be sure that QNIVERTER is ready to attach LSI-11 compatible devices to a PDP-11 Unibus, verify the following on the QNIVERTER printed circuit board:

A. E6 is jumpered to E4. (See Figure 3-1 for location of "E" points.)

B. Resistor termination modules are installed in the following locations: (See Figure 3-1 for location of resistor modules.)
   - RM11 - Q Bus Termination- 330 ohm pull-up, 680 ohm pull-down
   - RM12 - Q Bus Termination- 330 ohm pull-up, 680 ohm pull-down
   - RM13 - Q Bus Termination- 330 ohm pull-up, 680 ohm pull-down
   - RM5 - Unibus Termination- 390 ohm

### 3.3.1 PDP-11 SYSTEM INSTALLATION EQUIPMENT REQUIRED

To use QNIVERTER with a Unibus computer system, the following user-supplied equipment is required:

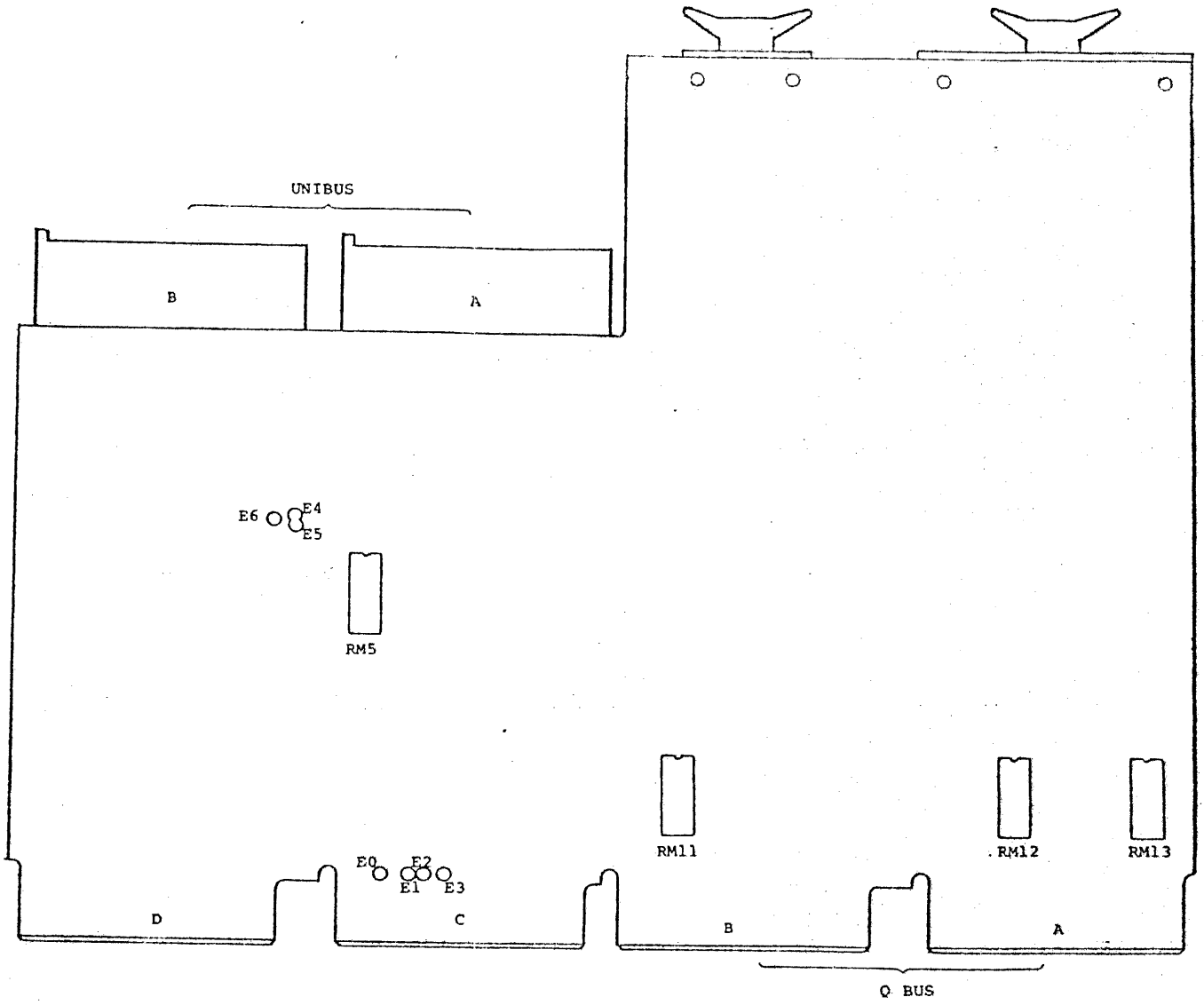


Figure 3-1: QNIVERTER Board Layout

- Unibus cable
- Quad LSI-11 backplane for installation of QNIVERTER and LSI-11 devices
- Appropriate power sources for LSI-11 devices

### 3.3.2 PDP-11 SYSTEM CONFIGURATION

Figure 3-2 is a block diagram illustrating QNIVERTER used with a PDP-11 system. The QNIVERTER installs into the quad LSI-11 backplane slot normally occupied by the LSI-11 CPU. Guide the QNIVERTER carefully into the card guides of the selected slot. When the QNIVERTER begins to make contact with the backplane connectors, add a small amount of force to insure that the QNIVERTER is well seated in the backplane. Connection to the Unibus is accomplished by installation of one end of a Unibus cable into the connectors provided on the QNIVERTER. The other end of the Unibus cable must be installed where the Unibus terminator is installed in the present system. This places the QNIVERTER as the last device on the Unibus with the Unibus termination supplied by QNIVERTER.

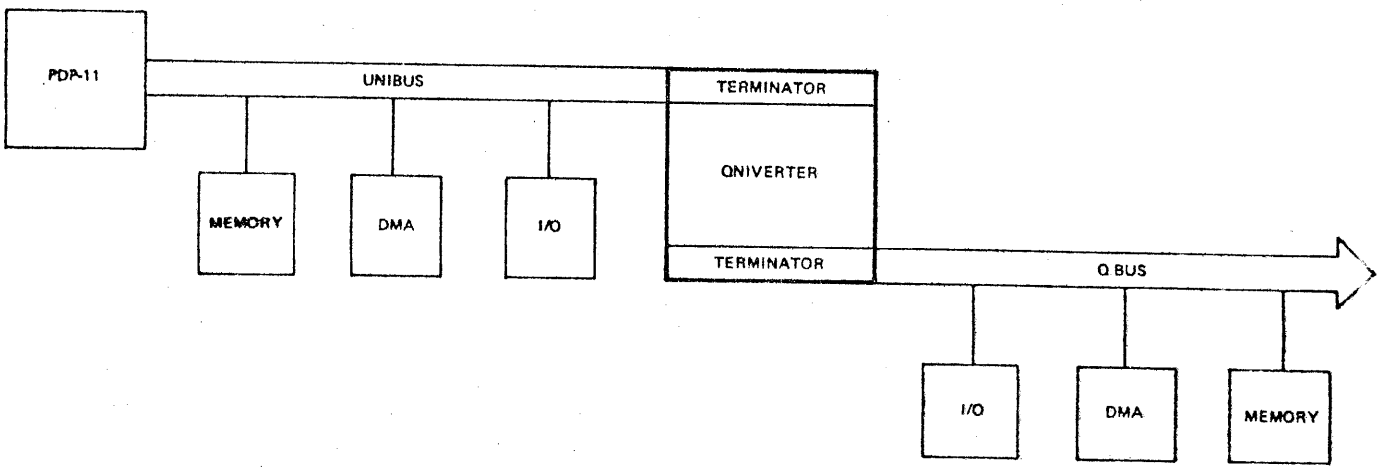


Figure 3-2: Simplified Block Diagram - PDP-11 System

## 3.4 INSTALLING QNIVERTER IN AN LSI-11 SYSTEM

The QNIVERTER is shipped configured for a Unibus arbitrator. To configure it for an LSI-11 bus arbitrator, perform the following:

- Remove jumper between E6 and E4 and install a jumper between E6 and E5.
- Remove the resistor termination modules listed below from their IC sockets (store them in a safe place for possible future use):
  - RM11
  - RM12
  - RM13
  - RM5

### 3.4.1 LSI-11 SYSTEM INSTALLATION EQUIPMENT REQUIRED

To install QNIVERTER in an LSI-11 computer system, the following user-supplied equipment is required:

- Unibus cable
- M930 Unibus terminator or equivalent
- Unibus backplane for installation of memories and controllers
- Appropriate power sources for the Unibus memories and controllers

### 3.4.2 LSI-11 SYSTEM CONFIGURATION

Figure 3-3 is a block diagram illustrating QNIVERTER installed in an LSI-11 system. The QNIVERTER is a quad-width module and requires one quad LSI-11 backplane slot for installation. Prior to installing the QNIVERTER, the LSI-11 system should be checked for proper system configuration to insure that modules are placed in the proper backplane slot. This can be used to insure that high priority devices are physically located ahead of lower priority devices. The QNIVERTER should be included in the system configuration considerations. Priority level 4 devices should be located behind the QNIVERTER; priority level 5,6, and 7 devices should be placed ahead of the QNIVERTER.

The QNIVERTER is now ready to be installed. Guide the QNIVERTER carefully into the card guides of the selected slot. When the QNIVERTER begins to make contact with the backplane connectors, add a small amount of force to insure that the QNIVERTER is well seated in the backplane.

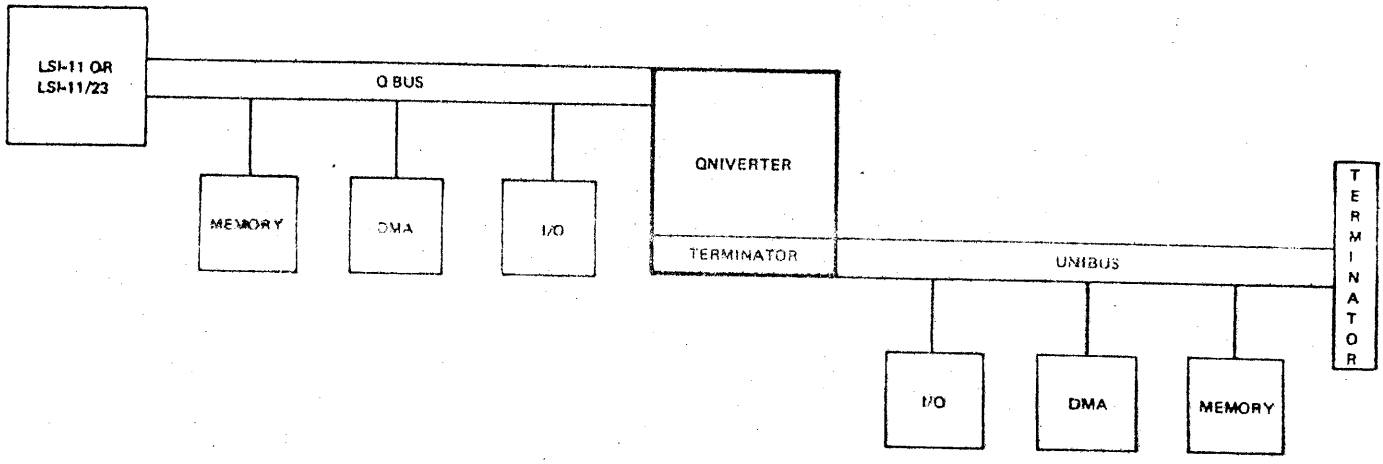


Figure 3-3: Simplified Block Diagram - LSI-11 System

Once QNIVERTER is installed into the desired backplane slot, install a Unibus cable into the top connectors provided on QNIVERTER. The opposite end of the Unibus cable must be installed into the Unibus-In slot of a DD11 type backplane (connectors A and B) or into a Unibus-In slot of an externally mounted controller. The QNIVERTER provides Unibus termination for the beginning of the Unibus. The far end of the Unibus will require a separate terminator. Note: The Unibus controller and terminator require the appropriate power to allow system operation.

## 3.5 INSTALLATION VERIFICATION

The QNIVERTER is totally software transparent to the arbitrating CPU system. Therefore, any diagnostic appropriate for the device attached through QNIVERTER to the arbitrating system bus may be used to verify proper installation. (Note that certain device/memory diagnostics may not be completely computer independent. Consult the diagnostic listing for the applicable devices and computer(s).)

With the QNIVERTER installed, the computer system is provided with a second bus structure: Unibus or Q bus. The arbitration of the two buses is performed by the processor in the system: either the PDP-11 or the LSI-11. The QNIVERTER is software transparent. It is important to insure that address assignments of devices on the Unibus and LSI-11 bus do not conflict. This can be accomplished by verifying that there are no duplicate address assignments.

NOTE: When installing QNIVERTER in a DEC BA11-N backplane, the jumpers between E0 and E1, and between E2 and E3 must be removed.

# SECTION 4

# WHAT TO DO IF QNIVERTER DOES NOT WORK

## 4.1 HOW TO CARE FOR QNIVERTER

ABLE products are designed to provide years of service with a minimum of care. Here are a few tips to help you avoid problems.

- If a printed circuit board is frequently inserted and removed, it tends to build up a gum-like residue on the contacts. Clean this residue off using alcohol or freon or by gently rubbing with a pencil eraser. (Rubbing vigorously can remove some of the gold on the contacts, so go easy.)

- Every six months remove each printed circuit board and clean off any accumulated dust. Dust can impede air flow. While the board is out, inspect it for any visual evidence of a potential problem such as damaged components, loose connections, etc.

- Schematics for your QNIVERTER can be ordered from the ABLE factory. Order document number 10067003.

- If you wish to maintain a spare parts inventory, refer to the recommended list in Appendix C.

- If a problem arises with the operation of your QNIVERTER, follow the steps outlined in the following sections.

## 4.2 TROUBLESHOOTING TIPS

If QNIVERTER does not function properly, verify proper installation of the board as follows:

1. Using Sections 3.3 and 3.4 verify that the jumper selection and resistor module installation are correct.

2. Verify that QNIVERTER is properly installed into an LSI backplane. Refer to appropriate DEC literature for backplane information.

3. Verify that the Unibus cable is installed correctly with notches aligned and is firmly seated in the QNIVERTER Unibus connectors.

4. Check the +5 volts power on the LSI backplane and Unibus backplane. Use a voltmeter and measure from ground to +5 volts on pin CA2, DA2, AA2, or BA2 on the backplane. Power should be +5.0 volts ±5%. If the power is not within this range, adjust the power supply.

5. Check that there are no vacant slots (missing bus grants) between QNIVERTER and other modules in the [illegible] plane.

If QNIVERTER still does not function properly, call ABLE as described in the following sections.

## 4.3 WHEN TO CALL FOR SERVICE WITHIN THE UNITED STATES

ABLE's goal is to provide each customer with a product that works well in his system. We design and build our products to provide high reliability and to minimize problems. When a problem does arise, it is our intent to do everything in our power to quickly and efficiently solve it.

If your QNIVERTER does not function properly and you are within the United States, call our Product Support Center before sending it for repair:

ABLE COMPUTER
17251 Langley Avenue
Irvine, California 92714

(714) 979-7033
TWX 910-595-1728

If your product requires repair, we prefer that you return it to the factory in the original container from your QNIVERTER or a corregated cardboard carton with at least one inch of cushioning material on all sides. Ship it to the above address. Include a description of the problem and a hard copy of the failure mode or diagnostic printout when available. Be sure to include your name, address, and telephone number.

Refer to the warranty and service document shipped with QNIVERTER or call our Product Support Center for further information.

## 4.4 WHEN TO CALL FOR SERVICE OUTSIDE THE UNITED STATES

ABLE's goal is to provide each customer with a product that works well in his system. We design and build our products to provide high reliability and to minimize problems. When a problem does arise, it is our intent to do everything in our power to quickly and efficiently solve it.

If your QNIVERTER does not function properly, contact your local distributor for the name and address of your local distributor:

TWX 910-595-1728

# SECTION 5
# HOW TO USE QNIVERTER

## 5.1 TYPICAL PDP-11 UNIBUS SYSTEM APPLICATION

This application allows the user of PDP-11 Unibus systems to take advantage of the often lower-cost peripherals (and memories) available for the LSI-11 computer. Figure 3-1 is a block diagram of a typical application. The QNIVERTER and LSI-11 peripheral devices or memories are installed in an LSI-11 quad backplane and supplied with +5 volt power. The QNIVERTER is installed in the backplane slot normally occupied by the LSI-11 processor. The QNIVERTER, other devices, and memories in the LSI-11 backplane are connected to a PDP-11 Unibus computer system by a standard Unibus extender cable connected between the top side of the QNIVERTER and the last Unibus slot (A & B) in the PDP-11 backplane. Appendix B contains a Unibus connector list. The QNIVERTER is electrically the last device on the Unibus and provides the far-end Unibus termination.

QNIVERTER provides the system with a second bus structure, the LSI-11 Q bus. The arbitration of the two buses is performed by the PDP-11 processor located on the Unibus.

## 5.2 TYPICAL LSI-11 Q BUS APPLICATION

This application allows the wider range of PDP-11 Unibus peripherals and memories to be used with the LSI-11 computer. Figure 3-2 is a block diagram of a typical application. The QNIVERTER can be installed in any quad slot of the LSI-11, LSI-11/2, LSI-11/23, or PDP-11/03 systems. Other LSI-11 interfaces and memories can be located either ahead or behind the QNIVERTER. Devices located behind the QNIVERTER have a lower priority (both interrupt and NPR/DMA) than the Unibus devices attached to the QNIVERTER.

The Unibus peripherals and memories are installed in a Unibus backplane which must be supplied with the appropriate power. An M930 terminator (or equivalent) must be the last device installed in the Unibus backplane. The Unibus backplane is connected to the QNIVERTER with a standard Unibus extender cable connected between the first Unibus connectors in the Unibus backplane and the connectors on the top end of the QNIVERTER. Appendix A contains a Q bus connector list; Appendix B contains a PDP-11 Unibus connector list.

The QNIVERTER provides the LSI-11 system with a second bus structure, Unibus. The LSI-11 processor controls the arbitration of both buses.

# SECTION 6
# HOW TO PROGRAM QNIVERTER

QNIVERTER provides the system of which it is a part with a second bus structure: Unibus or Q bus. The QNIVERTER is completely software transparent to the host (arbitrating) computer. Note that QNIVERTER is designed to operate with a single computer performing bus arbitration; it is not intended to be used as an interprocessor coupler.

Since QNIVERTER is software transparent to the host computer, any diagnostic appropriate for the device(s) being connected through QNIVERTER to the system may be used to verify system operation. Note that certain device/memory diagnostics may not be completely computer independent. Consult the diagnostic listing for the applicable devices and computer(s).

NOTE: THE MOST IMPORTANT CONSIDERATION IS TO INSURE THAT ADDRESS ASSIGNMENTS OF DEVICES ON THE UNIBUS AND Q BUS DO NOT CONFLICT.

# SECTION 7
# How QNIVERTER Works

This section describes how QNIVERTER works. The first subsection describes the major functional elements of QNIVERTER. The second subsection lists and describes the Unibus I/O signals. The third subsection lists and describes the Q bus I/O signals. The first subsection descriptions are referenced to a block diagram, Figure 7-1, that illustrates the relationship among the functional units of QNIVERTER, and timing diagrams supplemented by descriptive tables that illustrate the relationship among the signals of the buses.

## 7.1 FUNCTIONAL DESCRIPTION OF QNIVERTER

The QNIVERTER matches the characteristics of the Unibus and Q bus. It does this "characteristic matching" bidirectionally; Q bus compatible devices can be connected into a PDP-11 (Unibus) computer system, and Unibus compatible devices can be connected into an LSI-11 (Q Bus) computer system. Note that the QNIVERTER cannot be used as an inter-computer coupler. Only one processor is the system arbitrator. The user positions a jumper in QNIVERTER to select either the Unibus or the Q bus as the source of the system arbitration.

Figure 7-1 is a block diagram of the QNIVERTER. The blocks can be grouped into four major categories. The blocks within a category perform related functions.

The major categories are as follows:

- Bidirectional information transfer
- Bidirectional bus request and interrupt priority transfer
- Bidirectional information transfer control and direct-to-memory transfer control
- QNIVERTER timing and control

Table 7-1 lists the logic blocks in each category and relates the Unibus/Q bus signals to the logic blocks (when applicable).

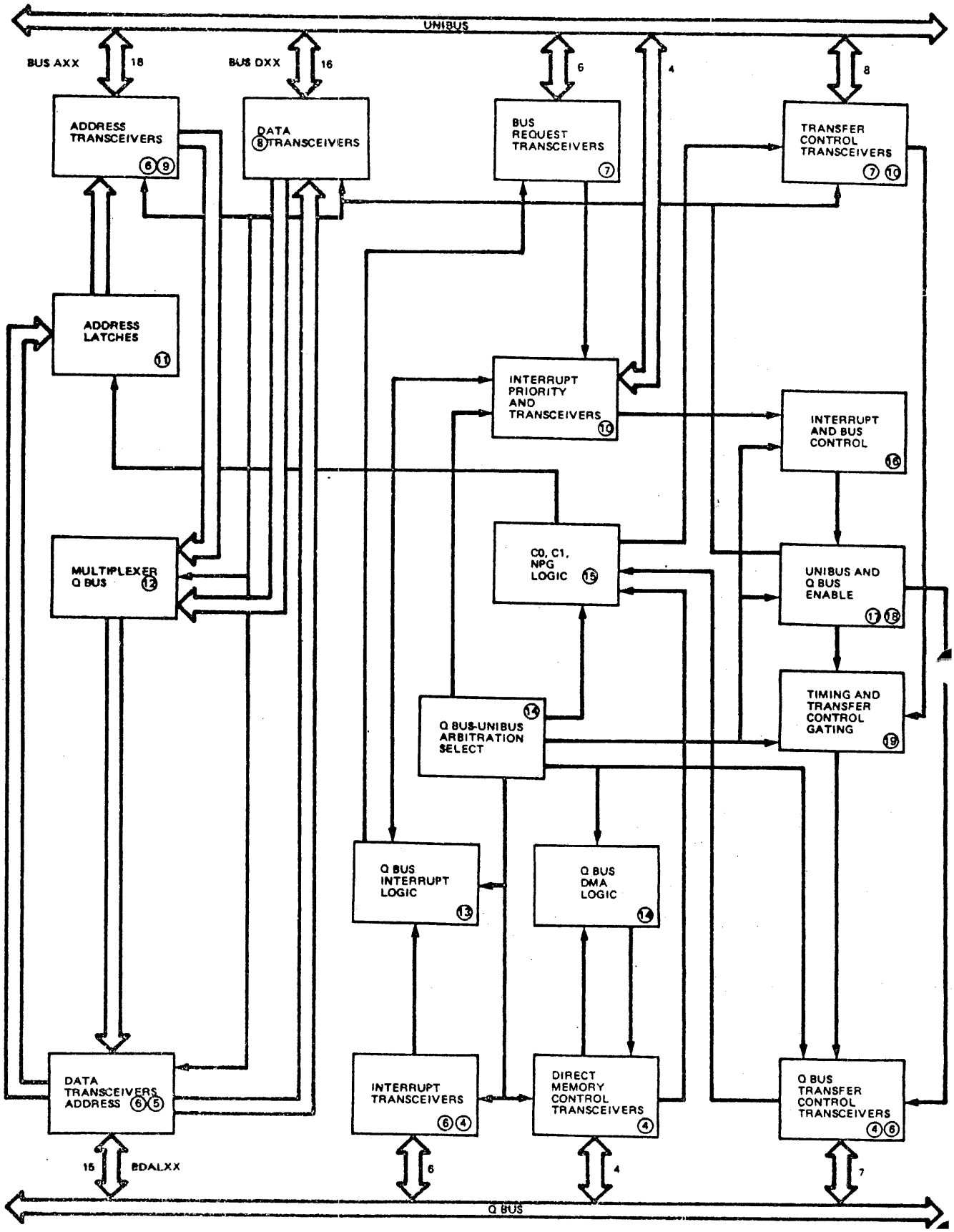


Figure 7-1: Block Diagram QNIVERTER

| CATEGORY | LOGIC BLOCKS | Q BUS/UNIBUS SIGNALS |
|---|---|---|
| A. Information Transfer | 1. Unibus Address Transceivers | BUS-A00 to BUS-A17 |
| | 2. Unibus Data Transceivers | BUS-D00 to BUS-D15 |
| | 3. Q Bus Multiplexer | BUS-A00 to BUS-A17 and BUS-D00 to BUS-D15 |
| | 4. Q Bus Data/Address Transceivers | BDAL00 to DBAL17 |
| | 5. Q Bus Address Latches | Q Bus Address Lines |
| B. Bus Request and Interrupt Priority | 1. Bus Request Transceivers | BUS-BR4 to BUS-BR7, BUS-INTR, BUS-SACK |
| | 2. Interrupt Priority and Bus Grant Transceivers | BUS-BG4 to BUS-BG7 |
| | 3. Q Bus Interrupt Logic | |
| | 4. Q Bus Interrupt Transceivers | BIRQ4 to BIRQ7, BIAKI, BIAKO |
| C. Information Transfer Control and Direct-to-Memory control | 1. Transfer Control Transceivers | BUS-MSYN, BUS-SSYN BUS-C0, BUS-C1, BUS-BBSY, BUS-INIT, BUS-PB, BUS-NPR, BUS-NPG |
| | 2. C0, C1, and NPG Logic | |
| | 3. Q Bus DMA Logic | |
| | 4. Direct Memory Control Transceivers | BDMR, BSACK, BDMGI, BDMG0 |
| | 5. Q Bus Transfer Control Transceivers | BSYNC, BDIN, BDOUT, BINIT, BWTBT, BRPLY, BBS7 |
| D. QNIVERTER Timing and Control | 1. Q Bus-Unibus Arbitration Select | |
| | 2. Unibus and Q Bus Enable | |
| | 3. Interrupt and Bus Control | |
| | 4. Timing and Transfer Control Gating | |

Table 7-1: Logic Blocks to Bus Signals Reference

Since the PDP-11 Unibus and the LSI-11 Q bus were developed by the same manufacturer, signal transfer concepts, data word widths, and address word widths are similar. The differences between the two bus structures occurred because the LSI-11 processor is microprocessor-chip based. Pinout restrictions on the microprocessor chip dictated that the number of bus lines be reduced from the 56 lines available on the Unibus to some number within the physical capability of a standard 40-pin integrated circuit package. The number of control and information lines on the Q bus is 35. The largest reduction of lines was realized by time sharing the 16 data lines with the 18 address lines on the Q bus, a reduction of 16 lines over the Unibus (the Unibus has separate data and address lines). Other reductions were made by changing slightly the concept of granting "bus mastership" on different priority levels.

In the Unibus system the arbitration section of the processor received requests for the use of the Unibus over four priority-structured bus request lines. The arbitrator responded to bus requests over four bus grant lines. The LSI-11 and LSI-11/2 implemented only one bus request and one bus grant, permitting only one level of interrupt priority. The LSI-11/23 permits 4 level interrupt priority as well as allowing addressing up to 128K words.

In addition to the preceding bus-concept differences, there are timing differences between the two buses. The LSI-11, Q Bus, processor is microprocessor-chip based and is therefore slower than the MSI/SSI based processor on the Unibus.

Therefore, the primary tasks required of the QNIVERTER are:

- Multiplex addresses and data from the Unibus onto the single 18-bit address/data lines of the Q bus and demultiplex the Q bus address/data lines onto the separate address and data lines of the Unibus.
- Bidirectionally match the grant/request signals with the Q bus interrupt signals
- Bidirectionally match the NPR and DMA requests
- Bidirectionally match the timing among the signals of the two buses.

As mentioned previously only one processor can be in the system of which the QNIVERTER is a part. A jumper in the QNIVERTER Q Bus-Unibus Arbitration Select logic is positioned so that the logic of the QNIVERTER responds properly to the controlling computer. This jumper establishes either the Unibus as arbitrator or the Q bus as arbitrator. The controlling computer is attached to the arbitrating bus.

Throughout the following discussion, the function of the individual logic elements is only briefly described; in most cases the name of the logic block describes the function of the block, i.e., transceiver (buffers and conducts signals in both directions), latch (storage element), etc.. This material is more concerned with the relationship among the logic elements while transferring information or control between the two buses. Thus, the descriptive material is referenced to timing diagrams that show the relationship among the bus signals when either the Unibus or the Q bus is arbitrator.

### 7.1.1 QNIVERTER TIMING AND CONTROL

As listed in Table 7-1 the logic blocks that make up the QNIVERTER timing and control section are as follows:

- Q Bus-Unibus Arbitration Select
- Unibus and Q Bus Enable
- Interrupt and Bus Control

- Timing and Transfer Control Gating

When the QNIVERTER is installed in a system, the user positions a jumper in the Q Bus-Unibus Arbitration Select logic to match the characteristics of the QNIVERTER with the controlling processor, which will be positioned either on the Unibus or the Q bus. The two signals generated by this logic (UARBT and QARBT) effect every element of QNIVERTER and set the rest of the control logic into the proper mode of operation.

The Unibus and Q Bus Enable logic comprises a group of gates, a flip-flop, and a multiplexer controlled by the Q Bus-Unibus Arbitration Select logic. The gates develop outputs for the multiplexer based upon the arbitrator and the requested type of transfer (Unibus to Q bus, Q bus to Unibus). The multiplexer gates enable signals to the information transfer section of the QNIVERTER. This logic "steers" data between the two buses properly regardless of the arbitrator. It:

A. Controls the Q bus multiplexer

B. Clocks the address latches

C. Enables the Q bus data drivers

D. Enables the Unibus data and address drivers.

The Interrupt and Bus Control logic is the interface between the bus requests from the Unibus and the interrupt circuit of the Q bus when the Q bus is arbitrator. Note that bus requests from Unibus devices are translated by the QNIVERTER into interrupt requests to the LSI-11 when the Q bus is arbitrator.

The Timing and Transfer Control Logic match the characteristics of the following signals:

| UNIBUS | Q BUS |
|---|---|
| MSYN | SYNC |
| SSYN | BDOUT, BDIN |
| | BRPLY |

This logic also contains the Q bus parity error detect gates.

### 7.1.2 INFORMATION TRANSFER

This section of logic transfers addresses and data between the Unibus and the Q bus. Either write or read data transfers can be initiated by either the Unibus or the Q bus, regardless of which bus is the arbitrator. Figure 7-2 and Table 7-2 illustrate the relationship among the Unibus and Q bus data transfer signals, addresses, and data lines during a Unibus-initiated write sequence. Figures and Tables 7-3, 7-4, and 7-5 illustrate the following transfer sequences:

7-3 Unibus-initiated read
7-4 Q bus-initiated write
7-5 Q bus-initiated read

During the transfer sequences the Q bus multiplexer, address latches, and driver sections of the bus transceivers are controlled by signals from the Unibus and Q bus Enable logic. The transfer control signals from the two buses are conditioned by the Timing and Transfer Control Gating logic. The signal source for controlling the Q bus multiplexer and address latches is the conditioned Q bus SYNC signal.

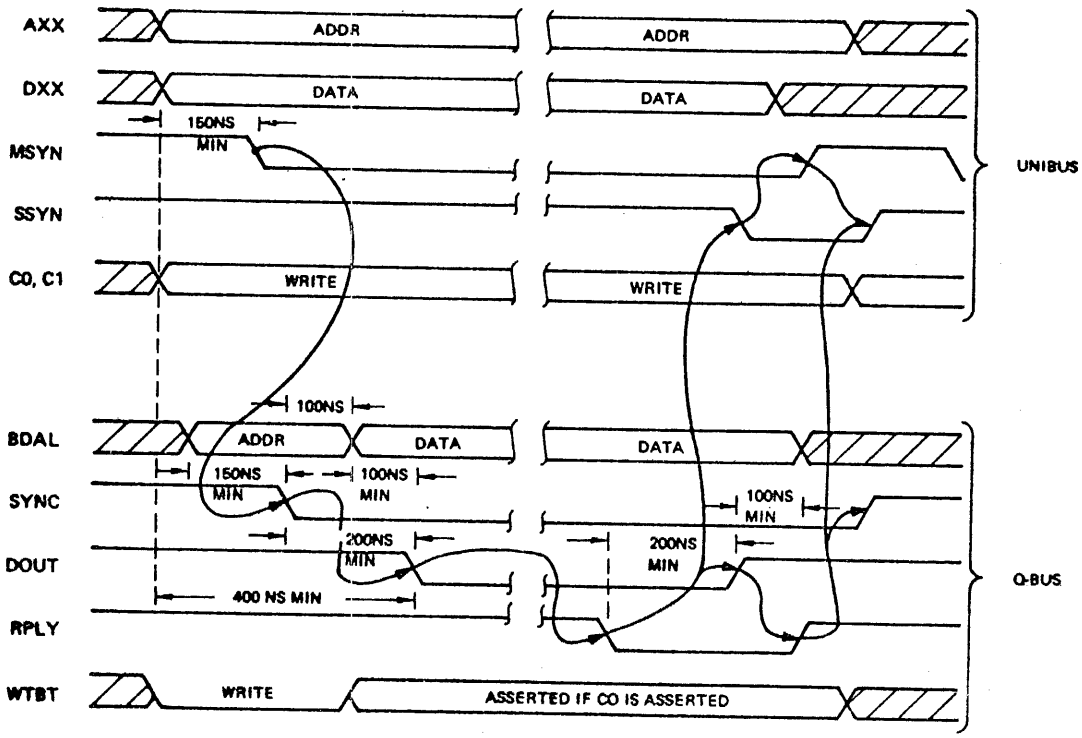


Figure 7-2: Unibus Initiated Write

| STEP | UNIBUS | QNIVERTER | Q BUS |
|---|---|---|---|
| 1. | a. Device address on bus.<br>b. Data on bus.<br>c. C1 asserted. C0 asserted if byte transfer, negated if word transfer.<br>d. MSYNC asserted. | | |
| 2. | | a. Gate address to BDAL lines.<br>b. Assert WTBT. If C0 asserted WTBT remains asserted through cycle. If C0 negated, negate WTBT within 100 ns after SYNC asserted.<br>c. Assert SYNC. | |
| 3. | | a. 100 ns after SYNC asserted replace address with data on BDAL lines.<br>b. 200 ns after SYNC asserted, assert DOUT. | |
| 4. | | | When data received by addressed device assert RPLY. |
| 5. | | a. After 200 ns generate SSYN.<br>b. Negate DOUT.<br>c. After 100 ns remove data from BDAL. | |
| 6. | Negate MSYN. | | |
| 7. | | a. Negate SSYN.<br>b. Negate WTBT if C0 has been asserted. | Negate RPLY |
| 8. | TRANSFER SEQUENCE COMPLETED | | |

Table 7-2: Unibus Initiated Write Data Transfer

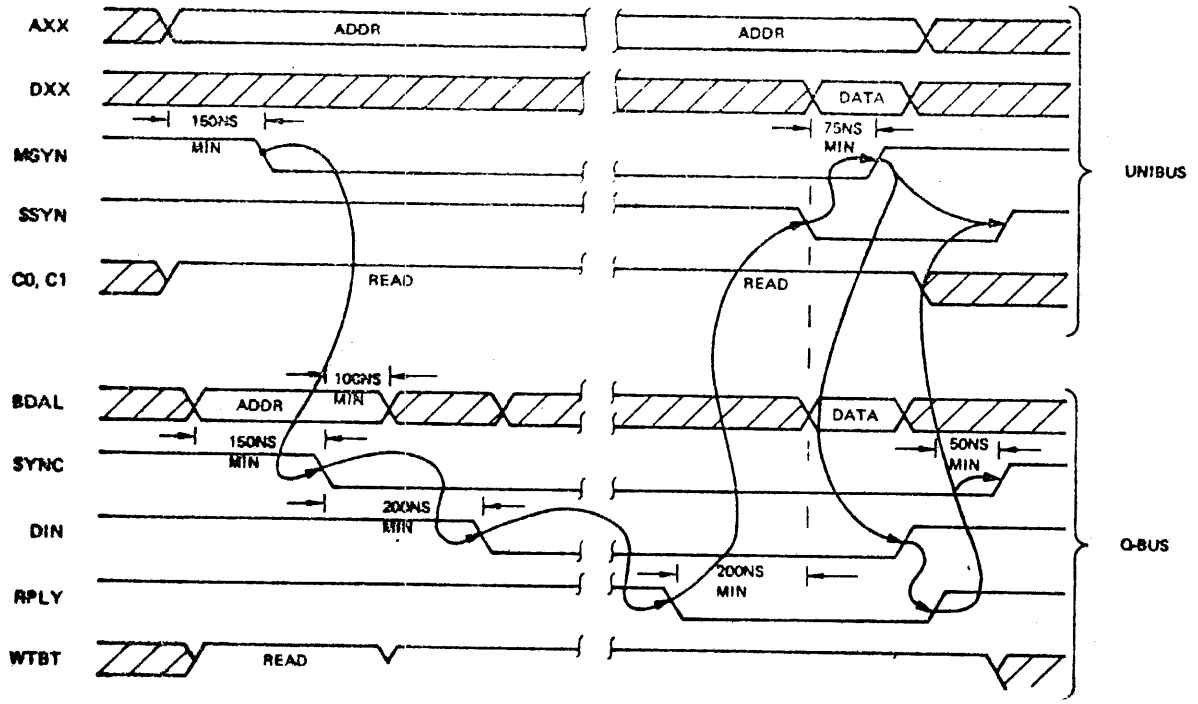


Figure 7-3: Unibus Initiated Read

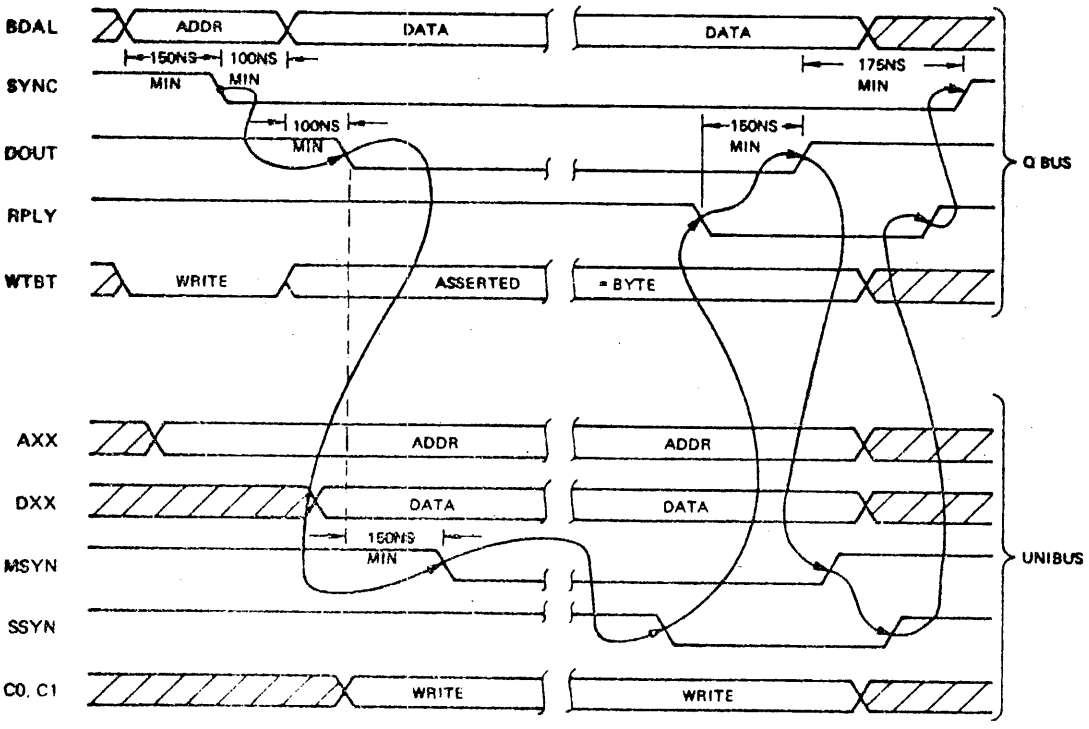


Figure 7-4: Q Bus Initiated Write

| STEP | UNIBUS | QNIVERTER | Q BUS |
|---|---|---|---|
| 1. | a. Device address on bus.<br>b. C0, C1 negated.<br>c. MSYNC asserted. | | |
| 2. | | a. Gate address to BDAL lines.<br>b. Assert SYNC.<br>c. Delay 200 ns, assert DIN. | |
| 3. | | | Addressed device. Assert RPLY and place data on BDAL lines. |
| 4. | | a. Gate data from BDAL to Unibus data lines.<br>b. Assert SSYN. | |
| 5. | a. Input data and negate MSYNC. | | |
| 6. | | Negate DIN | |
| 7. | | | Negate RPLY and remove data on BDAL lines |
| 8. | | Negate SSYN | |
| 9. | TRANSFER SEQUENCE COMPLETED | | |

Table 7-3: Unibus Initiated Read Data Transfer

| STEP | Q BUS | QNIVERTER | UNIBUS |
|---|---|---|---|
| 1. | a. Address on BDAL lines.<br>b. Assert WTBT.<br>c. 150 ns later assert WTBT. | | |
| 2. | | a. Gate Address from BDAL to Unibus AXX lines.<br>b. Assert C1. Assert C0 if byte transfer. | |
| 3. | a. Negate WTBT if word transfer.<br>b. Replace address with data on BDAL lines.<br>c. Assert DOUT. | | |
| 4. | | a. Gate data from BDAL to Unibus DXX Lines.<br>b. Assert MSYN. | |
| 5. | | | When addressed device accepts data, assert SSYN. |
| 6. | | Assert RPLY. | |
| 7. | Negate DOUT and remove data on BDAL lines. | | |
| 8. | | Negate MSYN | |
| 9. | | | Negate SSYN |
| 10. | | Negate RPLY. | |
| 11. | Negate SYNC | | |
| | TRANSFER SEQUENCE COMPLETE | | |

Table 7-4: Q BUS Initiated Write Data Transfer

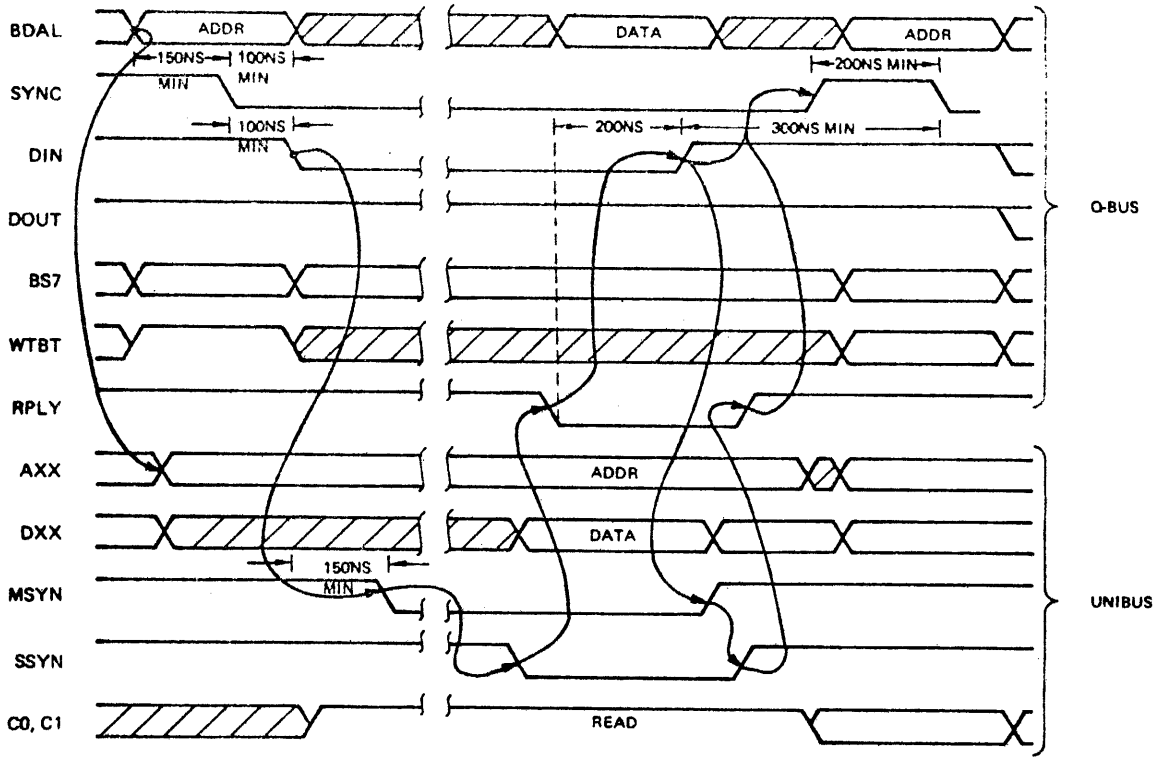


Figure 7-5: Q-Bus Initiated Read

As listed in Table 7-1 the logic blocks that make up the QNIVERTER information transfer section are as follows:

- Unibus Address Transceivers
- Unibus Data Transceivers
- Q Bus Multiplexer
- Q Bus Data/Address Transceivers
- Q Bus Address Latches

An important feature of the QNIVERTER is the bus termination characteristics when used with either a Unibus-arbitrated system or a Q bus-arbitrated system. Terminating resistor modules are permanently installed on all Unibus input/output lines. Removable terminating resistor modules are installed on the Q bus input/output lines when the QNIVERTER is used in a Unibus-arbitrated system. These resistor modules are removed, however, when QNIVERTER is used in a Q bus-arbitrated system because line termination is provided by the LSI-11 computer.

| STEP | Q BUS | QNIVERTER | UNIBUS |
|---|---|---|---|
| 1. | a. Address on BDAL lines.<br>b. 150 ns later assert SYNC. | | |
| 2. | | a. Gate address from BDAL to AXX lines.<br>b. Negate C0 and C1. | |
| 3. | Assert DIN. | | |
| 4. | | Assert MSYN | |
| 5. | | | a. Addressed device asserts SSYN.<br>b. Addressed device places data on DXX lines. |
| 6. | | a. Assert RPLY<br>b. Gate data from DXX to BDAL lines. | |
| 7. | Input data on BDAL lines and negate DIN. | | |
| 8. | | a. Negate MSYN<br>b. Negate RPLY | |
| 9. | Negate SYNC | | |
| 10. | | | Negate SSYN and remove data on DXX lines. |
| | TRANSFER SEQUENCE COMPLETED | | |

Table 7-5: Q BUS Initiated Read Data Transfer

### 7.1.3 BUS REQUEST AND INTERRUPT PRIORITY

As listed in Table 7-1 the logic blocks that make up the QNIVERTER bus request and interrupt priority section are as follows:

- Bus Request Transceivers
- Interrupt Priority and Bus Grant Transceivers
- Q Bus Interrupt Logic
- Q Bus Interrupt Transceivers

The state of this logic, the order in which signals are transferred, depends upon which bus is the arbitrator. The order of signal flow is established by the Q bus-Unibus arbitration select logic.

Figure and Table 7-6 illustrate the signal sequence for an interrupt request when the Unibus is arbitrator. When the Unibus is arbitrator, the bus request and interrupt driver sections of the Unibus transceivers are enabled and the interrupt drivers in the Q bus transceivers are disabled. Note that the receiver sections of all transceivers are always enabled.

As mentioned in paragraph 7.1, one of the major differences between the Unibus and the Q bus is in the interrupt logic of the buses. Interrupts on the Unibus must first request use of the bus, receive a bus grant (on one of four levels), then generate an interrupt accompanied by the device address (vector). On the Q bus the use of the bus is assumed and interrupts are requested on one of four levels, which establishes priority among the devices on the Q bus.

Note from Figure 7-6 that a Q bus IRQ on one of four levels is gated onto one of the four BR lines of the Unibus. The BG signal from the Unibus is compared with the Q bus IRQ signals in the Q bus interrupt logic to generate the DIN signal and establish IAKI and RPLY conditions to the interrupting device on the Q bus. This device then places its address on the BDAL lines and the conditioning circuits in the QNIVERTER generate Unibus signal SACK, BBSY, INTR, place the Q bus data (vector) on the Unibus data drivers, and waits for the processor to accept the vector by generating a SSYN.

Figure and Table 7-7 illustrate the signal sequence for an interrupt request when the Q bus is arbitrator. Bus requests (BRX) are connected to IRQ lines by the driver section of the interrupt transceivers. The IAKI signal from the Q bus enables a group of gates in the interrupt priority and transceivers logic that connect the outputs of a priority register to the Unibus BG line associated with the requesting device. The requesting device then generates the SACK, BBSY, and INTR signals (most of which are ignored by the Q bus), and places its vector address on the Q bus via the Q bus multiplexer and Q bus address/data drivers.

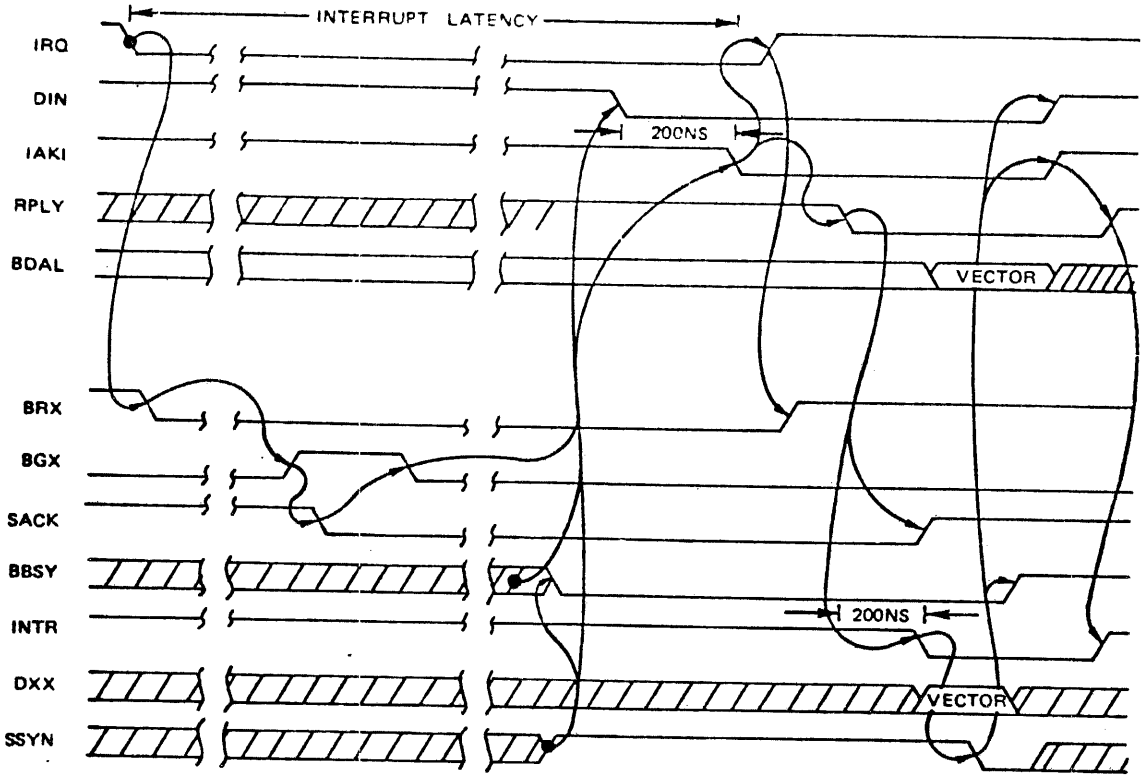


Figure 7-6: Interrupt Sequence - Unibus Arbitrator

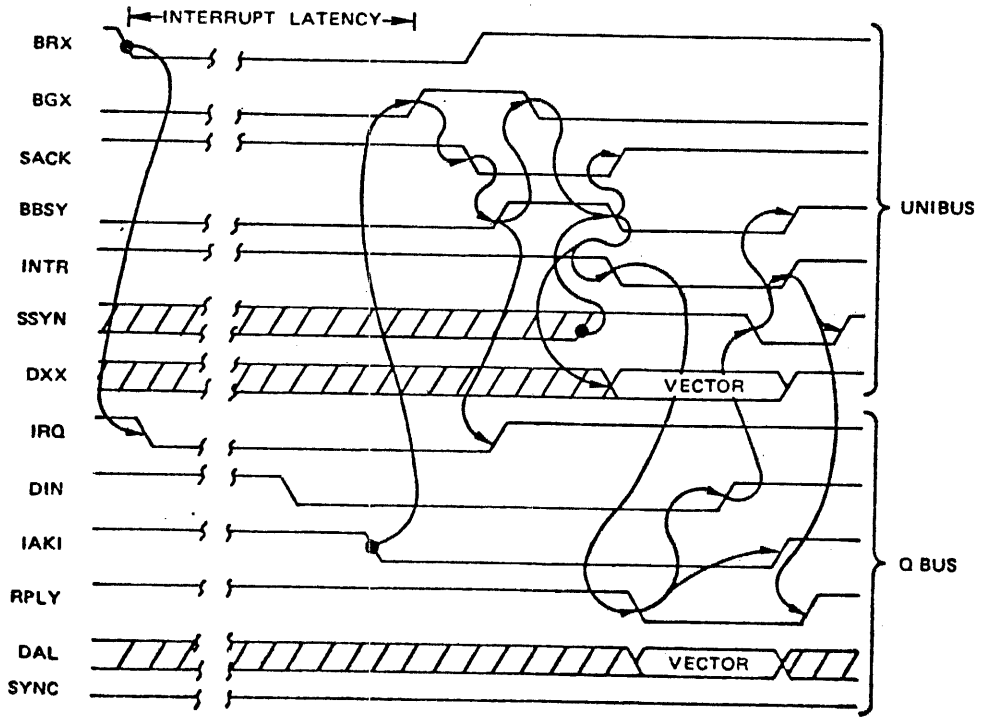


Figure 7-7: Interrupt Sequence - Q Bus Arbitrator

| STEP | Q BUS | QNIVERTER | UNIBUS |
|---|---|---|---|
| 1. | IRQ asserted | | |
| 2. | | BRX asserted | |
| 3. | | | BGX asserted. |
| 4. | | Unibus SACK asserted | |
| 5. | | | Remove BGX |
| 6. | | | Remove BBSY |
| 7. | | a. Assert DIN<br>b. 150 ns later assert IAK1 | |
| 8. | Negate IRQ | | |
| 9. | | Remove BRX | |
| 10. | Interrupt device places vector on BDAL lines and asserts RPLY | | |
| 11. | | Gate Interrupt Vector from BDAL lines to DXX lines. | |
| 12. | | a. Assert INTR<br>b. 1 | |
| 13. | | a. Negate DIN<br>b. Negate IAK1 | |
| 14. | Negate RPLY | | |
| 15. | | a. Negate BBSY<br>b. Remove vector from DXX lines.<br>c. Negate INTR | |
| 16. | | | Negate SSYN |
| | SEQUENCE COMPLETED | | |

Table 7-6: Q BUS Interrupt Sequence-Unibus Arbitrator

| STEP | UNIBUS | QNIVERTER | Q BUS |
|---|---|---|---|
| 1. | Assert BRX | | |
| 2. | | Assert IRQX | |
| 3. | | | a. Assert BDIN<br>b. Assert IAKI |
| 4. | | Assert BGX | |
| 5. | a. Assert SACK<br>b. Negate BRX | | |
| 6. | | a. Negate BBSY<br>b. Negate IRQX | |
| 7. | | Negate BGX | |
| 8. | a. Assert BBSY<br>b. Negate SACK<br>c. Assert INTR<br>d. Place vector on DXX lines | | |
| 9. | | Gate Interrupt vector from DXX to BDAL lines | |
| 10. | | Assert BRPLY | |
| 11. | | | a. Input vector on BDAL lines and negate BDIN<br>b. Remove IAKI |
| 12. | | Assert SSYN | |
| 13. | a. Negate INTR<br>b. Negate BBSY | | |
| 14. | | a. Negate BRPLY<br>b. Remove Interrupt vector from BDAL lines.<br>c. Remove SSYN | |
| | SEQUENCE COMPLETED | | |

Table 7-7: UNIBUS Interrupt Sequence-Q BUS Arbitrator

Although most of the device response signals are ignored by the Q bus arbitrator, the signals are used by the QNIVERTER to properly time acknowledge (IAKI) and reply (RPLY) signals so that the requesting device can remove its signals in the proper sequence to insure a valid transfer.

### 7.1.4 INFORMATION TRANSFER AND DIRECT TO MEMORY CONTROL

As listed in Table 7-1 the logic blocks that make up the QNIVERTER information transfer and direct to memory (DMA) control are as follows:

- Transfer Control Transceivers
- C0, C1, and NPG Logic
- Bus DMA Logic
- Direct Memory Control Transceivers
- Q Bus Transfer Control Transceivers

Three of the logic elements are primarily concerned with buffering the write/read transfer control (handshaking) signals between the two buses and buffering the four DMA control signals to the Q bus. The remaining two logic elements primarily match the characteristics of the Q bus DMA timing signal sequence with the Unibus NPR timing signal sequence. In Unibus terminology direct to memory requests are referred to as non-processor requests (NPR). Regardless of the terminology (NPR,DMA) the effect is the same in both systems; requests are made for data transfers directly to memory without processor intervention.

Figure and Table 7-8 illustrate the signal sequence for a DMA request when the Unibus is arbitrator. Figure and Table 7-9 illustrate the signal sequence for a DMA request when the Q bus is arbitrator. Note the similarity in the signal names and signal responses between the two buses. The major difference between the two buses is that transferring addresses and data to the Unibus is a one-step process and transferring addresses and data to the Q bus is a two-step process (address and data lines are time shared on the Q bus).

Mode control lines on the two buses have different terminology. In the Unibus system the device must decode the condition of control lines C0 and C1 to determine if the required transfer sequence is a data in (DATI), a data in pause (DATIP), a data out (DATO), or a data out byte (DATOB). In Q bus devices detecting the required type of transfer is simpler. Q bus signal BDOUT specifies an output transfer, BDIN specifies either an input transfer or that an interrupt operation is occurring, and BWTBT specifies read/write operation and if the output transfer is on a byte basis. The C0, C1 portion of the C0, C1, and NPG logic decodes and codes the mode control signals between the two buses.

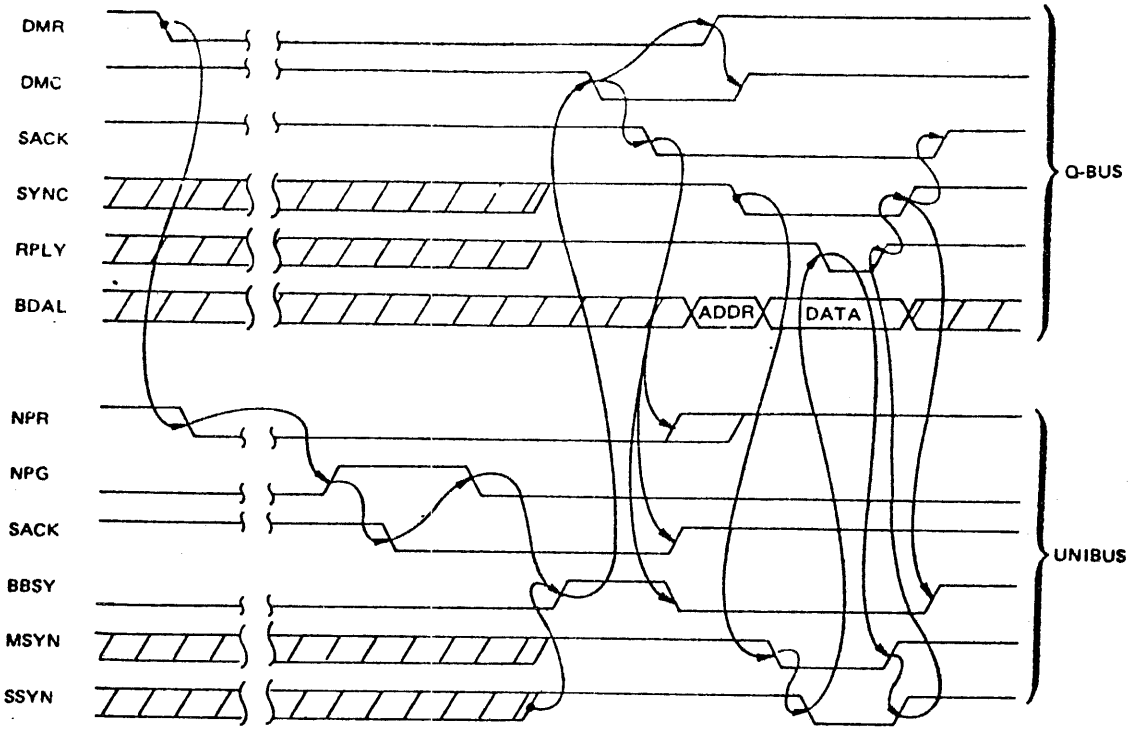


Figure 7-8: DMA Request - Unibus Arbitrator

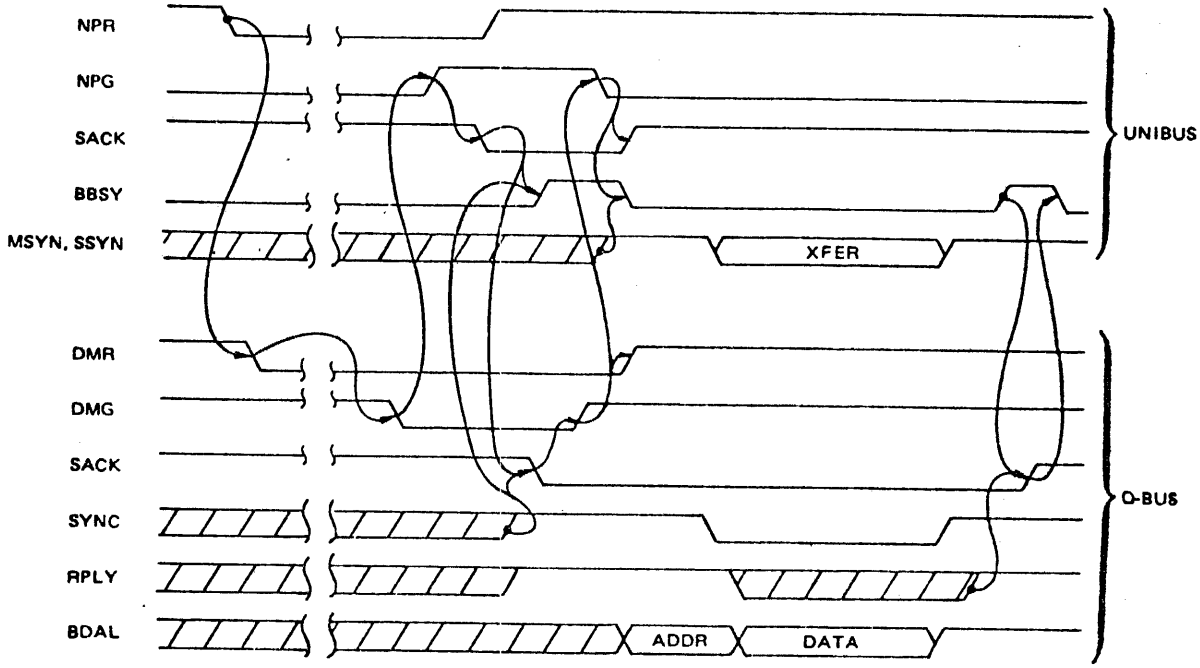


Figure 7-9: DMA Request - Q Bus Arbitrator

| STEP | Q BUS | QNIVERTER | UNIBUS |
|---|---|---|---|
| 1. | DMR Asserted | | |
| 2. | | NPR Asserted | |
| 3. | | | NPG Asserted |
| 4. | | SACK Asserted | |
| 5. | | | NPG Negated |
| 6. | | | BBSY Negated |
| 7. | | DMG Asserted | |
| 8. | SACK Asserted | a. SACK negated | |
| | | b. BBSY asserted | |
| 9. | DMR Negated | | |
| 10. | | DMG Negated | |
| 11. | Place address on BDAL lines | | |
| 12. | | NPR Negated | |
| 13. | a. Assert SYNC<br>b. Assert DOUT or DIN | | |
| 14. | | a. Place address on AXX lines<br>b. Assert MSYN | |
| 15. | | | Assert SSYN |
| 16. | Remove DOUT/DIN | | |
| 17. | | Negate MSYN | |
| 18. | | | Remove SSYN |
| 19. | Remove SYNC | | |
| 20. | Remove SACK | | |
| 21. | | Remove BBSY | |
| 22. | | | Assert BBSY |
| | TRANSFER SEQUENCE COMPLETE | | |

Table 7-8: Q Bus DMA Request - Unibus Arbitrator

| STEP | UNIBUS | QNIVERTER | Q BUS |
|---|---|---|---|
| 1. | Assert NPR | | |
| 2. | | Assert DMR | |
| 3. | | | Assert DMG |
| 4. | | Assert NPG | |
| 5. | Assert SACK (Unibus) | | |
| 6. | Negate NPR | | |
| 7. | | | Negate SYNC (End of previous bus cycle) |
| 8. | | Assert SACK (Q Bus) | |
| 9. | | Negate BBSY | |
| 10. | | | Negate DMG |
| 11. | | Negate NPG | |
| 12. | a. Negate SACK (Unibus)<br>b. Negate DMR<br>c. Assert BBSY<br>d. Place address on AXX lines<br>e. Place data on DXX if write operation | a. Place address onto BDAL lines<br>b. Assert SYNC | |
| 13. | Assert MSYN | | |
| 14. | | a. Switch Data to BDAL lines from DXX lines<br>b. Assert DIN or DOUT | |
| 15. | | | Assert RPLY |
| 16. | | Assert SSYN | |
| 17. | Negate MSYN | | |
| 18. | | Negate DIN or DOUT | |
| 19. | | Remove RPLY | |
| 20. | | Remove SSYN | |
| 21. | | Remove SYNC | |
| 22. | Remove BBSY | | |
| 23. | | Remove SACK | |
| | TRANSFER SEQUENCE COMPLETED | | |

Table 7-9: Unibus DMA Request - Q Bus Arbitrator

## 7.2 UNIBUS I/O SIGNALS

| Signal Name | Description |
|---|---|
| A17 - A00 | Address bits. These bits select the slave device and/or memory address. |
| D15 - D00 | Data bits. These bits contain the information to be transferred. |
| C0, C1 | Control lines. These lines specify the type of data transfer: DATI, DATIP, DATO, or DATOB. |
| MSYN | Master sync. This signal is generated by the bus master to request a data transfer. |
| SSYN | Slave sync. This signal is generated by the slave device in response to MSYN to indicate that the device is ready with data for the bus or has read data from the bus. It is also generated by the processor during an interrupt to indicate that it has accepted the interrupt vector. |
| INTR | Interrupt. This signal is generated by QNIVERTER along with the interrupt vector during an Interrupt sequence. |
| BR4 - BR 7 | Bus request. One of these signals is used to request use of the bus for an interrupt at the level specified. |
| BG4 - BG7 | Bus grant. This signal is generated by the processor to grant use of the bus for an interrupt at the specified level. |
| NPR | Non-processor request. This signal is generated by a DMA device to request use of the bus for a data transfer. |
| BBSY | Bus busy. This signal indicates that the Unibus is in use. |
| SACK | Selection acknowledge. This signal is generated in response to Bus Grant to inhibit further bus grants and to indicate that a device is selected to use the bus upon completion of the sequence currently in progress. |

## 7.3 Q BUS I/O SIGNALS

| Signal Name | Description |
|---|---|
| BAD16, BAD17 | Extended address bits. |
| BBS7 | Bank 7 select. The bus master asserts BBS7 when an address in the upper 4K bank (I/O address) is placed on the bus. |
| BDAL0 - BDAL15 | 16-line data/address bus over which address and data information are communicated. Address information is first placed on the bus by the bus master. The same device then either receives input data or supplies output data to the addressed slave device or memory over the same lines. |
| BDCOK | DC power OK. |
| BDIN | Data input: specifies either an input operation or an interrupt operation. |
| BDOUT | Data output: specifies an output operation with respect to the bus master is taking place and data is stable on the data/address lines. |
| BDMG1, BDMG0 | DMA grant input and DMA grant output. Processor generated daisy-chained bus mastership grant signal to the highest priority DMA requesting device on the bus. |
| BEVNT | External Event interrupt request. |
| BDMRL | Direct memory access (DMA) request: requested by devices to gain bus mastership. |
| BIAKI, BIAKO | Interrupt Acknowledge input and interrupt acknowledge output. A daisy-chained signal generated by the processor in response to an interrupt request. |
| BIRQ | Interrupt request. asserted by a device to request service by the processor. |
| BSACK | Select acknowledge: asserted by a DMA in response to the BDMG0 signal from the processor, indicating that the DMA device is bus master. |
| BRPLY | Reply: asserted in response to BDIN or BDOUT and during IAK transactions by a slave device. Indicat either that the slave has placed data on the bus or has received data from the bus. |

| Signal Name | Description |
|---|---|
| BSYNC | Synchronize: asserted by the bus master to indicate that it has placed an address on BDAL0-BDAL15 and BAD16, BAD17. The transfer is in process until BSYNC is negated. |
| BWTBT | Write/byte: used in two ways during a bus cycle:<br>1. Indicates that an output sequence is to follow rather than an input sequence.<br>2. Asserted during DBOUT in a DATOB bus cycle for byte addressing. |

# Appendix A
# Q Bus Connectors

This appendix contains connector information for the LSI-11 Q bus.

| CONNECTOR D | | |
|---|---|---|
| SIDE 1 | PIN | SIDE 2 |
| | A | +5V |
| | B | -12V |
| | C | GND |
| | D | +12V |
| | E | |
| | F | |
| | H | |
| GND | J | |
| | K | |
| | L | |
| GND | M | |
| | N | |
| | P | |
| | R | |
| | S | |
| GND | T | |
| | U | |
| +5V | V | |

| CONNECTOR C | | |
|---|---|---|
| SIDE 1 | PIN | SIDE 2 |
| | A | +5V |
| | B | -12V |
| | C | GND |
| | D | +12V |
| | E | |
| | F | |
| | H | |
| GND | J | |
| | K | |
| | L | |
| GND | M | BIAKI-L |
| | N | BIAKO-L |
| | P | |
| | R | BDMGI-L |
| +12B | S | BDMGO-L |
| GND | T | |
| | U | |
| | V | |

| CONNECTOR B | | |
|---|---|---|
| SIDE 1 | PIN | SIDE 2 |
| BDCOK-H | A | +5V |
| BPOK-H | B | -12V |
| | C | GND |
| | D | +12V |
| | E | BDAL02-L |
| | F | BDAL03-L |
| | H | BDAL04-L |
| GND | J | BDAL05-L |
| MSPARE-B | K | BDAL06-L |
| MSPARE-B | L | BDAL07-L |
| GND | M | BDAL08-L |
| BSACK-L | N | BDAL09-L |
| BIRQ-7 | P | BDAL10-L |
| BEVNT-L | R | BDAL11-L |
| PSPARE-4 | S | BDAL12-L |
| GND | T | BDAL13-L |
| PSPARE-2 | U | BDAL14-L |
| +5V | V | BDAL15-L |

| CONNECTOR A | | |
|---|---|---|
| SIDE 1 | PIN | SIDE 2 |
| BIRQ5-L | A | +5V |
| BIRQ6-L | B | -12V |
| BDAL16-L | C | GND |
| BDAL17-L | D | +12V |
| | E | BDOUT-L |
| | F | BRPLY-L |
| | H | BDIN-L |
| GND | J | BSYNC-L |
| MSPARE-A | K | BWTBT-L |
| MSPARE-B | L | BIRQ-4 |
| GND | M | BIAKI-L |
| BDMR-L | N | BIAKO-L |
| BHALT-L | P | BBS7-L |
| BREF-L | R | BDMGI-L |
| +12B | S | BDMGO-L |
| GND | T | BINIT-L |
| PSPARE-1 | U | BDAL00-L |
| +5B | V | BDAL01-L |

# Appendix B
# Unibus Connectors

This appendix contains connector information for the Unibus.

| CONNECTOR B | | |
|---|---|---|
| SIDE 1 | PIN | SIDE 2 |
| BUS-BG6-H | A | +5V |
| BUS-BG5-H | B | GND |
| BUS-BR5-L | C | GND |
| GND | D | BUS-BR4-L |
| GND | E | BUS-BG4-H |
| BUS-ACLO-L | F | BUS-DCLO-L |
| BUS-A01-L | H | BUS-A00-L |
| BUS-A03-L | J | BUS-A02-L |
| BUS-A05-L | K | BUS-A04-L |
| BUS-A07-L | L | BUS-A06-L |
| BUS-A09-L | M | BUS-A08-L |
| BUS-A11-L | N | BUS-A10-L |
| BUS-A13-L | P | BUS-A12-L |
| BUS-A15-L | R | BUS-A14-L |
| BUS-A17-L | S | BUS-A16-L |
| GND | T | BUS-C1-L |
| BUS-SSYN-L | U | BUS-C0-L |
| BUS-MSYN-L | V | GND |

| CONNECTOR A | | |
|---|---|---|
| SIDE 1 | PIN | SIDE 2 |
| BUS-INIT-L | A | +5V |
| BUS-INTR-L | B | GND |
| BUS-D00-1 | C | GND |
| BUS-D02-L | D | BUS-D01-L |
| BUS-D04-L | E | BUS-D03-L |
| BUS-D06-L | F | BUS-D05-L |
| BUS-D08-L | H | BUS-D07-L |
| BUS-D10-L | J | BUS-D09-L |
| BUS-D12-L | K | BUS-D11-L |
| BUS-D14-L | L | BUS-D13-L |
| BUS-PA-L | M | BUS-D15-L |
| GND | N | BUS-PB-L |
| GND | P | BUS-BBSY-L |
| GND | R | BUS-SACK-L |
| GND | S | BUS-NPR-L |
| GND | T | BUS-BR7-L |
| BUS-NPG-H | U | BUS-BR6-L |
| BUS-BG7-H | V | GND |

# Appendix C
# Spare Parts List

This appendix provides a recommended spare parts list for those wishing to maintain a parts inventory.

| Part | ACT Part Number | Vendor Part No. | Vendor* | Reference Designation |
|---|---|---|---|---|
| I.C. Quad 2-In NAND | 349-074-000 | 7400 | T.I. | U3,15,41,42,49, 62,64,76 |
| I.C. Hex Inverter | 349-074-004 | 7404 | T.I. | U4,12,23,34,35, 52,58,63 |
| I.C. Quad 2-In AND | 349-074-008 | 7408 | T.I. | U40,57,69,71 |
| I.C. Triple 3-In Pos NAND | 349-074-010 | 7410 | T.I. | U47,50,54,78 |
| I.C. Triple 3-In AND | 349-074-011 | 7411 | T.I. | U8,33,48,55,67 |
| I.C. Dual 4-In Pos NAND | 349-074-020 | 7420 | T.I. | U16 |
| I.C. Quad 2-In Pos NAND | 349-074-038 | 7438 | T.I. | U13,66,73 |
| I.C. Dual D F-F | 349-074-074 | 7474 | T.I. | U7,51,56,70,77, 79 |
| I.C. 4-2-3-2 In-AND-OR-Inu | 349-174-064 | 74S64 | T.I. | U20 |
| I.C. Quad 2-Line to 1 Mux | 349-174-158 | 74S158 | T.I. | U75 |
| I.C. 4-Bit Register | 349-074-278 | 74278 | T.I. | U19 |
| I.C. Quad 2-Line to 1 Mux | 349-274-157 | 74LS157 | T.I. | U29,36,37,43, 44 |
| I.C. Quad Bistable Latch | 349-074-075 | DM7475 | Nat'l | U24,27,28,31, 32 |
| I.C. Quad Bus Rec. | 345-008-640 | DS8640 | Nat'l | U11,65,72 |
| I.C. Quad Bus-Transceiver | 345-008-641 | DS8641 | Nat'l | U1,2,5,6,9,10, 14,17,21,22,25, 26,30,38,45,46, 53,59,74,80 |

*Vendor: T.I. = Texas Instruments, Nat'l = National

# Appendix D
# List of Materials

This appendix contains the QNIVERTER list of materials including vendors and part numbers.

| Description | Vendor Part No. | ACT Part No. | Qty. | Reference Designation | Vendor* |
|---|---|---|---|---|---|
| PWB - Qniverter | | 10067001 | 1 | | |
| ART - Qniverter | | 10067002 | | | |
| Schem. - Qniverter | | 10067003 | | | |
| I.C. Quad 2-In NAND | 7400 | 349-074-000 | 8 | U3,15,41,42, 49,62,64,76 | T.I. |
| I.C. Hex Inverter | 7404 | 349-074-004 | 8 | U4,12,23,34, 35,52,58,63 | T.I. |
| I.C. Quad 2-In AND | 7408 | 349-074-008 | 4 | U40,57,69,71 | T.I. |
| I.C. Triple 3-In Pos NAND | 7410 | 349-074-010 | 4 | U47,50,54,78 | T.I. |
| I.C. Triple 3-In AND | 7411 | 349-074-011 | 5 | U8,33,48,55,67 | T.I. |
| I.C. Dual 4-In Pos NAND | 7420 | 349-074-020 | 1 | U16 | T.I. |
| I.C. Quad 2-In Pos NAND | 7438 | 349-074-038 | 3 | U13,66,73 | T.I. |
| I.C. Dual D F-F | 7474 | 349-074-074 | 6 | U7,51,56,70, 77,79 | T.I. |
| I.C. 4-2-3-2 In-AND-OR-Inu | 74S64 | 349-174-064 | 1 | U20 | T.I. |
| I.C. Quad 2-Line to 1 Mux | 74S158 | 349-174-158 | 1 | U75 | T.I. |
| I.C. 4-Bit Register | 74278 | 349-074-278 | 1 | U19 | T.I. |
| I.C. Quad 2-Line to 1 Mux | 74LS157 | 349-274-157 | 5 | U29,36,37,43, 44 | T.I. |
| I.C. Quad Bistable Latch | DM7475 | 349-074-075 | 5 | U24,27,28,31, 32 | Nat'l. |
| I.C. Quad Bus Rec. | DS8640 | 345-008-640 | 3 | U11,65,72 | Nat'l. |
| I.C. Quad Bus-Transceiver | DS8641 | 345-008-641 | 20 | U1,2,5,6,9,10, 14,17,21,22,25, 26,30,38,45,46, 53,59,74,80 | Nat'l. |
| Cap.,4.7µf Tant.Tubular,20% 20V | CCM020-475-20 | 322-244-475 | 4 | C3,5,14,19 | |
| Cap.,.01µf,Cer.Disc,5%,HV | TBP103M10DZ5U | 321-129-103 | 7 | C4,6,7,12,15,16, 18 | |
| Cap.,1000Pf,Silver Mica, Dip 5% HV | CD15FD102J03 | 320-029-102 | 1 | C10 | |
| Cap.,680Pf,Sil.Mica Dip,5% HV | CD15FD681J03 | 320-029-681 | 2 | C1,9 | |
| Cap.,470 Pf.Sil.Mica,Dip,5% HV | CD15FD471J03 | 320-029-471 | 2 | C8,11 | |

* T.I. = Texas Instruments, Nat'l = National

| Description | Vendor Part No. | ACT Part No. | Qty. | Reference Designation | Vendor |
|---|---|---|---|---|---|
| Res. Mod 180/390 SIP 8 Pin | 764-5R180/390 | 312-582-001 | 8 | RM1,2,3,4,6,8, 9,10 | Beckman |
| Res. Mod 390 DIP 14 Pin | 899-3-R-390 | 311-681-391 | 1 | RM5 | Beckman |
| Res. Mod 180 SIP 8 Pin | 764-1-R180 | 311-582-181 | 1 | RM7 | Beckman |
| Cap., 330Pf, S.L.Mica, DIP 5% HV | CD15FD331J03 | 320-029-331 | 3 | C2,13,17 | |
| Res., 330, ¼W, 5% | RC07GF331J | 310-012-331 | 3 | R10,12,16 | |
| Res., 220 ¼W, 5% | RC07GF221J | 310-012-221 | 7 | R2,3,6,8,9,11, 14 | |
| Res., 680, ¼W, 5% | RC07GF681J | 310-012-681 | 2 | R13,17 | |
| Res., 1K, ¼W, 5% | RC07GF102J | 310-012-102 | 5 | R1,4,5,7,15 | |
| Res. Mod 330/680 DIP 14 Pin | 314E331681 | 312-681-002 | 3 | RM11,12,13 | Allen Brad |
| Eyelet, Brass | | 617-333-001 | 4 | | S. Phillips |
| Diode, Switching | FDH600 | 341-200-600 | 1 | CR1 | |
| W/W Post | PO25-443-1 | 560-400-101 | 7 | E0-E6 | |
| Connector, 36 Pin, Mod | | 90000045 | 2 | A,B | Cal-Data |
| Card Extractor | CP2 | 630-000-001 | 1 | | S. Phillips |
| Card Extractor | | 90000031 | 1 | | S. Phillips |
| Socket I.C. 14 Pin | 514-AG-11D | 575-401-401 | 4 | RM5,11,12,13 | Augat |

# Glossary

The -H or -L after a signal name indicates:

-L = low true
-H = high true

| TERM | DEFINITION |
|---|---|
| A00 through A17 | Address bits 00 through 17 |
| AL00 through AL17 | Address latch bits; output of Q bus multiplexer |
| BBS7 | Q bus bank 7 select |
| BDAL00 through BDAL17 | Q bus data and address bits 00 - 17 |
| BDIN | Q bus data in |
| BDIRQ04 through BDIRQ07 | Q bus 4-levels of interrupt request |
| BDMR | Q bus direct memory request |
| BDNGI | Q bus direct memory grant in |
| BDNGO | Q bus direct memory grant out |
| BDOUT | Q bus data out |
| BG-IN | Unibus grant in |
| BG-OUT | Unibus grant out |
| BG-SEL | Unibus grant select |
| BIAKI | Q bus interrupt acknowledge in |
| BIAKO | Q bus interrupt acknowledge out |
| BINIT | Q bus initialize |
| BRPLY | Q bus reply |
| BRRQ | Composite bus request signal |
| BSACK | Q bus select acknowledge |
| BSYNC | Q bus synchronize |
| BUS-A00 through BUS-A17 | Unibus address bits 00-17 |
| BUS-BBSY | Unibus busy |
| BUS-BG4 through BUS-BG7 | Unibus grant levels 4 through 7 |
| BUS-BR4 through BUS-BR7 | Unibus request levels 4 through 7 |
| BUS-C0, BUS-C1 | Unibus control lines C0 and C1 |
| BUS-D00 through BUS-D15 | Unibus data bits 00 through 15 |
| BUS-INIT | Unibus initialize |
| BUS-INTR | Unibus interrupt |
| BUS-MSYN | Unibus master sync |
| BUS-NPG | Unibus non-processor grant |
| BUS-NPR | Unibus non-processor request |
| BUS-PB | Unibus parity bit |
| BUS-SACK | Unibus selection acknowledge |
| BUS-SSYN | Unibus slave sync |
| C0, C1 | Internal control lines |

| TERM | DEFINITION |
|---|---|
| D00 through D15 | Internal data lines from Unibus |
| DAL00 through DAL17 | Internal 18 data/address lines from Q bus |
| DHOLD | Data hold |
| DIN | Internal data in from Q bus |
| DMGEN | Direct memory generate |
| DMGI | Internal direct memory grant in |
| DMGO | Internal direct memory grant out |
| DMR | Internal direct memory request |
| DOUT | Internal data out from Q bus |
| DSTRB | Internal data strobe |
| IAKI, IAKO | Internal interrupt acknowledge in and out |
| IDIN | Internal interrupt data in |
| INIT | Internal initialize |
| INTR | Internal interrupt request |
| IRQ4 through IRQ7 | Internal 4-level interrupt request |
| ISACK | Internal select acknowledge |
| ISYN | Internal interrupt synchronize |
| I567 | Interrupt from Q bus levels 5,6,or 7 |
| LNPG | Last non-processor grant |
| MSYN | Internal master sync |
| MX00 through MX17 | Q bus multiplexer outputs |
| NPG | Internal non-processor grant |
| NPR | Internal non-processor requests |
| PUP1, PUP2 | Pull ups 1 and 2 |
| QARBT | Q bus arbitrator |
| QBAD | Q bus address |
| QBCLR | Q bus clear |
| QBEN | Q bus enable |
| QBENQ | Q bus enable, Q bus arbitrator |
| QBENU | Q bus enable, Unibus arbitrator |
| QDBSY | Q bus data busy |
| QDMGO | Q bus direct to memory go |
| QIAKO | Q bus interrupt acknowledge out |
| QIBSY | Q bus interrupt busy |
| QINIT | Q bus interrupt |
| QPER | Q bus parity error |
| QSACK | Q bus select acknowledge |
| QXFER | Q bus transfer |
| RPLY | Internal reply |
| SHOLD | Synchronize hold |
| SSYN | Internal slave synchronize |
| SYNC | Internal synchronize |
| UARBT | Unibus arbitration |
| UBBSY | Unibus busy |
| UDEN | Unibus data enable |
| UDENQ | Unibus data enable, Q bus arbitrator |
| UDENU | Unibus data enable, Unibus arbitrator |

| TERM | DEFINITION |
|---|---|
| UINT | Unibus interrupt |
| URPLY | Unibus reply |
| UXFER | Unibus transfer |
| WTBT | Internal write byte from Q bus |
| XBBSY | Transfer bus busy |
| XBR4 | Transfer interrupts 4, or 5, or 6, or 7 |
| XCo, XCl | Transfer control bits 0 and 1 |
| XDDR | Transfer direct data request |
| XIAKI | Transfer interrupt acknowledge |
| XMSYN | Transfer master synchronize |
| XNPG | Transfer non-processor grant |
| XRPLY | Transfer reply |
| XSACK | Transfer select acknowledge |
| XSSYN | Transfer slave synchronize |
| XSYN | Transfer synchronize |
| XUSAK | Transfer Unibus select acknowledge |

# INDEX

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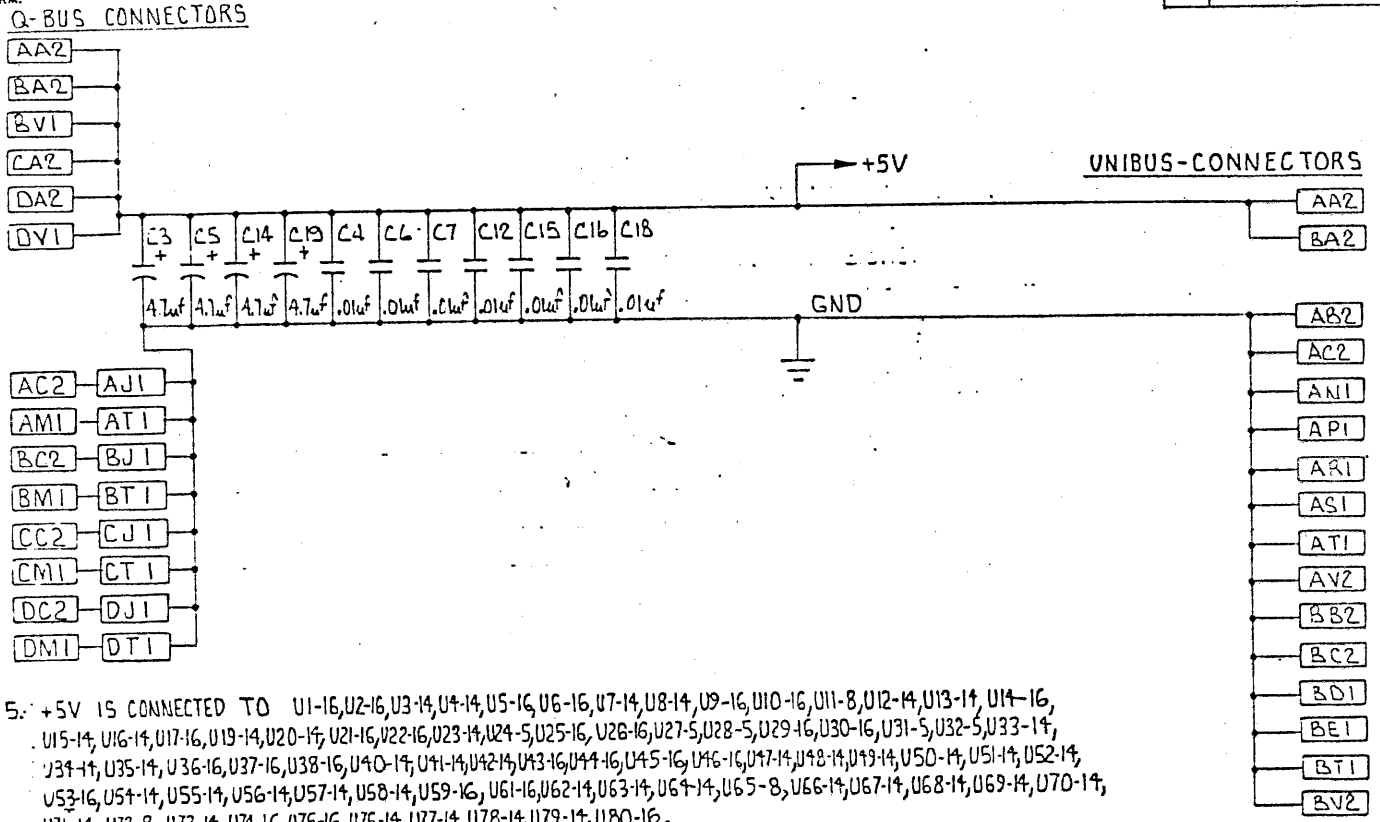
| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPROVED |
| B | PRODUCTION REL. PER E.O.00135 | 10-25-79 | |
| E | INC. PER E.O. 00147 | 1-17-80 | |
| K | INC. PER. E.O. 00517 | 15MAR82 | |
| N | INC. PER. E.O. 01305 | 1/21/83 | |




REF. ONLY

5. +5V IS CONNECTED TO U1-16,U2-16,U3-14,U4-14,U5-16,U6-16,U7-14,U8-14,U9-16,U10-16,U11-8,U12-14,U13-14,U14-16, U15-14,U16-14,U17-16,U19-14,U20-14,U21-16,U22-16,U23-14,U24-5,U25-16,U26-16,U27-5,U28-5,U29-16,U30-16,U31-5,U32-5,U33-14, U34-14,U35-14,U36-16,U37-16,U38-16,U40-14,U41-14,U42-14,U43-16,U44-16,U45-16,U46-16,U47-14,U48-14,U49-14,U50-14,U51-14,U52-14, U53-16,U54-14,U55-14,U56-14,U57-14,U58-14,U59-16,U61-16,U62-14,U63-14,U64-14,U65-8,U66-14,U67-14,U68-14,U69-14,U70-14, U71-14,U72-8,U73-14,U74-16,U75-16,U76-14,U77-14,U78-14,U79-14,U80-16.

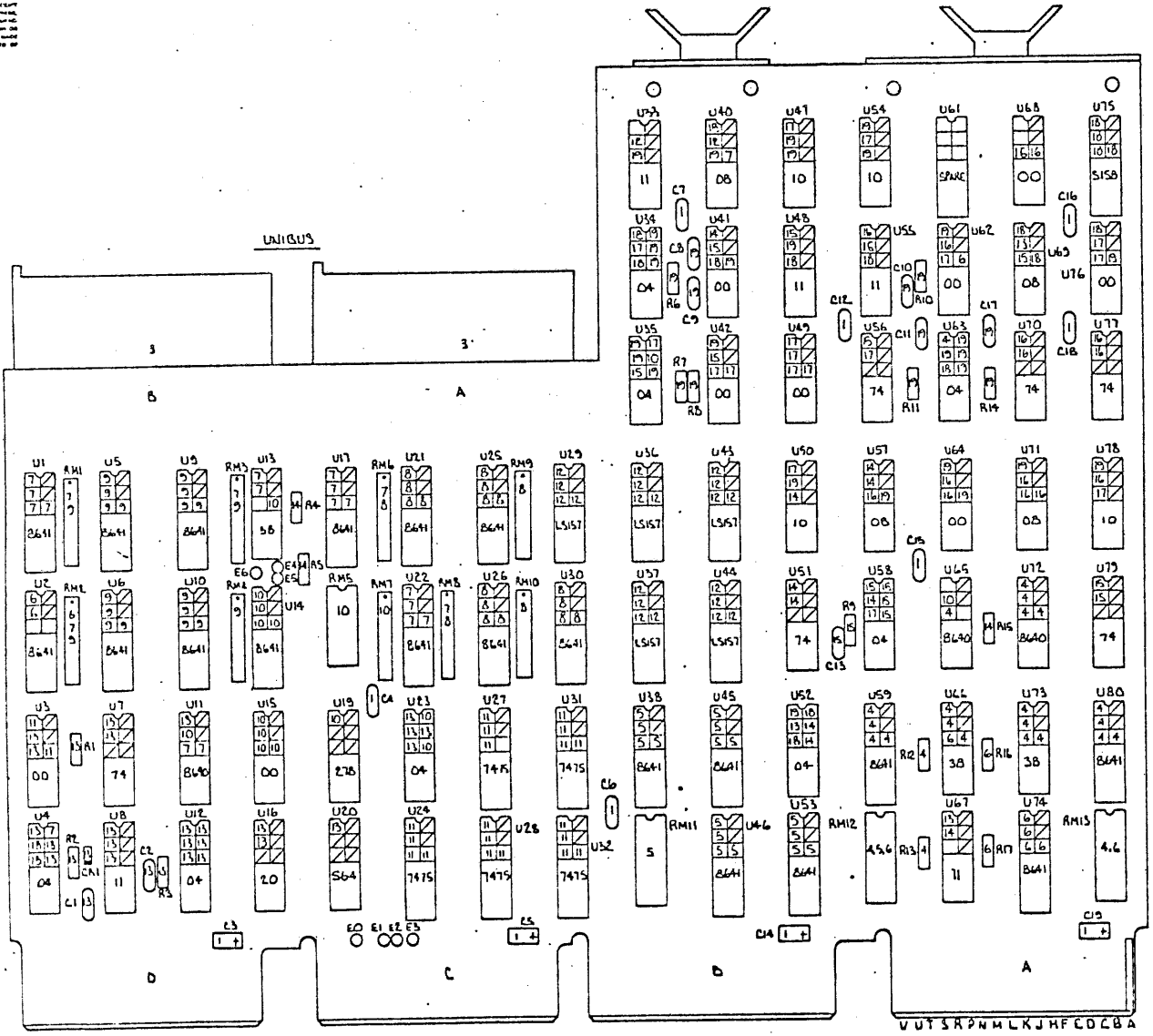
4. GND IS CONNECTED TO U1-8,U2-8,U3-7,U4-7,U5-8,U6-8,U7-7,U8-7,U9-8,U10-8,U11-1,U12-7,U13-7, U14-8,U15-7,U16-7,U17-8,U19-7,U20-7,U21-8,U22-8,U23-7,U24-12,U25-8,U26-8,U27-12,U28-12,U29-8,U30-8,U31-12,U32-12, U33-7,U34-7,U35-7,U36-8,U37-8,U38-8,U40-7,U41-7,U42-7,U43-8,U44-8,U45-8,U46-8,U47-7,U48-7,U49-7,U50-7,U51-7,U52-7,U53-8, U54-7,U55-7,U56-7,U57-7,U58-7,U59-8,U61-8,U62-7,U63-7,U64-7,U65-1,U66-7,U67-7,U68-7,U69-7,U70-7,U71-7,U72-1,U73-7,U74-8, U75-8,U76-7,U77-7,U78-7,U79-7,U80-8.

3. ALL CAPACITORS ARE IN PF.

2. RMS.11,12 & 13 ARE SOCKET MOUNTED & REMOVEABLE.

| | | |
|---|---|---|
| TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ∠ | ACT ABLE COMPUTER TECHNOLOGY | |
| APPROVALS | DATE | SCHEMATIC- QNIVERTER |
| DRAWN JRT | 7/19/79 | |
| CHECKED [illegible] | 1-20-83 | SCALE / SIZE B DRAWING NO. 1006700 3 |

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPROVED |
| N | SEE SHT 1. | | |




| REFERENCE DESIGNATION CHART | | |
|---|---|---|
| COMP. TYPE | LAST NO. USED | UNUSED |
| I.C. | U80 | U12, 39, 60 |
| | | (61, 81 |
| CAPACITOR | C19 | |
| RESISTOR | R17 | |
| RES. MOD | RM13 | |
| DIODE | CR1 | |

SCHEMATIC, QNIVERTER

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| SHT | 1 | B | 2 | SHT |
|---|---|---|---|---|
| 10 | BUS-BG6-H | A | +5V | 1 |
| 10 | BUS-BG5-H | B | GND | 1 |
| 7 | BUS-BR5-L | C | GND | 1 |
| 1 | GND | D | BUS-BR4-L | 7 |
| 1 | GND | E | BG4-H | 10 |
| 6 | BUS-ACLO-L | F | DCLO-L | 6 |
| 9 | AD1-L | H | AD0-L | 9 |
| 9 | AD3-L | J | AD2-L | 9 |
| 9 | AD5-L | K | AD4-L | 9 |
| 9 | AD7-L | L | AD6-L | 9 |
| 9 | AD9-L | M | AD8-L | 9 |
| 9 | AD11-L | N | AD10-L | 9 |
| 9 | AD13-L | P | AD12-L | 9 |
| 9 | AD15-L | R | AD14-L | 9 |
| 6 | BUS-AD17-L | S | AD16-L | 6 |
| 1 | GND | T | C1-L | 7 |
| 7 | BUS-SSYN-L | U | BUS-C0-L | 7 |
| 7 | BUS-MSYN-L | V | GND | 1 |

| SHT | 1 | A | 2 | SHT |
|---|---|---|---|---|
| 7 | BUS-INIT-L | A | +5V | 1 |
| 7 | INTR-L | B | GND | 1 |
| 8 | DO0-L | C | GND | 1 |
| 8 | DO2-L | D | BUS-DO1-L | 8 |
| 8 | DO4-L | E | DO3-L | 8 |
| 8 | DO6-L | F | DO5-L | 8 |
| 8 | DO8-L | H | DO7-L | 8 |
| 8 | DIO-L | J | DO9-L | 8 |
| 8 | DI2-L | K | DI1-L | 8 |
| 8 | BUS-DI4-L | L | DI3-L | 8 |
| | | M | DI5-L | 8 |
| 1 | GND | N | PB-L | 7 |
| 1 | GND | P | BBSY-L | 7 |
| 1 | GND | R | SACK-L | 7 |
| 1 | GND | S | NPR-L | 7 |
| 1 | GND | T | BR7-L | 7 |
| 10 | BUS-NPG-H | U | BUS-BR6-L | 7 |
| 10 | BUS-BG7-H | V | GND | 1 |

## UNIBUS

| SHT | 1 | D | 2 | SHT |
|---|---|---|---|---|
| | | A | +5V | 1 |
| | | B | | |
| | | C | GND | 1 |
| | | D | | |
| | | E | | |
| | | F | | |
| | | H | | |
| 1 | GND | J | | |
| | | K | | |
| | | L | | |
| 1 | GND | M | | |
| | | N | | |
| | | P | | |
| | | R | | |
| | | S | | |
| 1 | GND | T | | |
| | | U | | |
| 1 | +5V | V | | |

| SHT | 1 | C | 2 | SHT |
|---|---|---|---|---|
| | | A | +5V | 1 |
| | | B | | |
| | | C | GND | 1 |
| | | D | | |
| | | E | | |
| | | F | | |
| | | H | | |
| 1 | GND | J | | |
| | | K | | |
| | | L | | |
| 1 | GND | M | BIAKI-L | 6 |
| | | N | BIAKO-L | 6 |
| | | P | | |
| | | R | BDMGI-L | 6 |
| | | S | BDMGO-L | 6 |
| 1 | GND | T | | |
| | | U | | |
| | | V | | |

| SHT | 1 | B | 2 | SHT |
|---|---|---|---|---|
| 6 | BDCOK-H | A | +5V | 1 |
| 6 | BPOK-H | B | | |
| | | C | GND | 1 |
| | | D | | |
| | | E | BDALO2-L | 5 |
| | | F | BDALO3-L | 5 |
| | | H | BDALO4-L | 5 |
| 1 | GND | J | BDALO5-L | 5 |
| | | K | BDALO6-L | 5 |
| | | L | BDALO7-L | 5 |
| 1 | GND | M | BDALO8-L | 5 |
| 4 | BSACK-L | N | BDALO9-L | 5 |
| 4 | BIRQ7-L | P | BDALIO-L | 5 |
| 6 | BEVNT-L | R | BDALI1-L | 5 |
| | | S | BDALI2-L | 5 |
| 1 | GND | T | BDALI3-L | 5 |
| | | U | BDALI4-L | 5 |
| 1 | +5V | V | BDALI5-L | 5 |

| SHT | 1 | A | 2 | SHT |
|---|---|---|---|---|
| 4 | BIRQ5-L | A | +5V | 1 |
| 4 | BIRQ6-L | B | | |
| 6 | BDALI6-L | C | GND | 1 |
| 6 | BDALI7-L | D | | |
| | | E | BDOUT-L | 4 |
| | | F | BRPLY-L | 6 |
| | | H | BDIN-L | 4 |
| 1 | GND | J | BSYNC-L | 4 |
| | | K | BWTBT-L | 4 |
| | | L | BIRQ4-L | 4 |
| 1 | GND | M | BIAKI-L | 4 |
| 4 | BDMR-L | N | BIAKO-L | 6 |
| 6 | BHALT-L | P | BBS7-L | 6 |
| 6 | BREF-L | R | BDMGI-L | 4 |
| | | S | BDMGO-L | 4 |
| 1 | GND | T | BINIT-L | 4 |
| | | U | BDALOO-L | 5 |
| | | V | BDALOI-L | 5 |

## Q-BUS

| SCALE | SIZE | DRAWING NO. |
|---|---|---|
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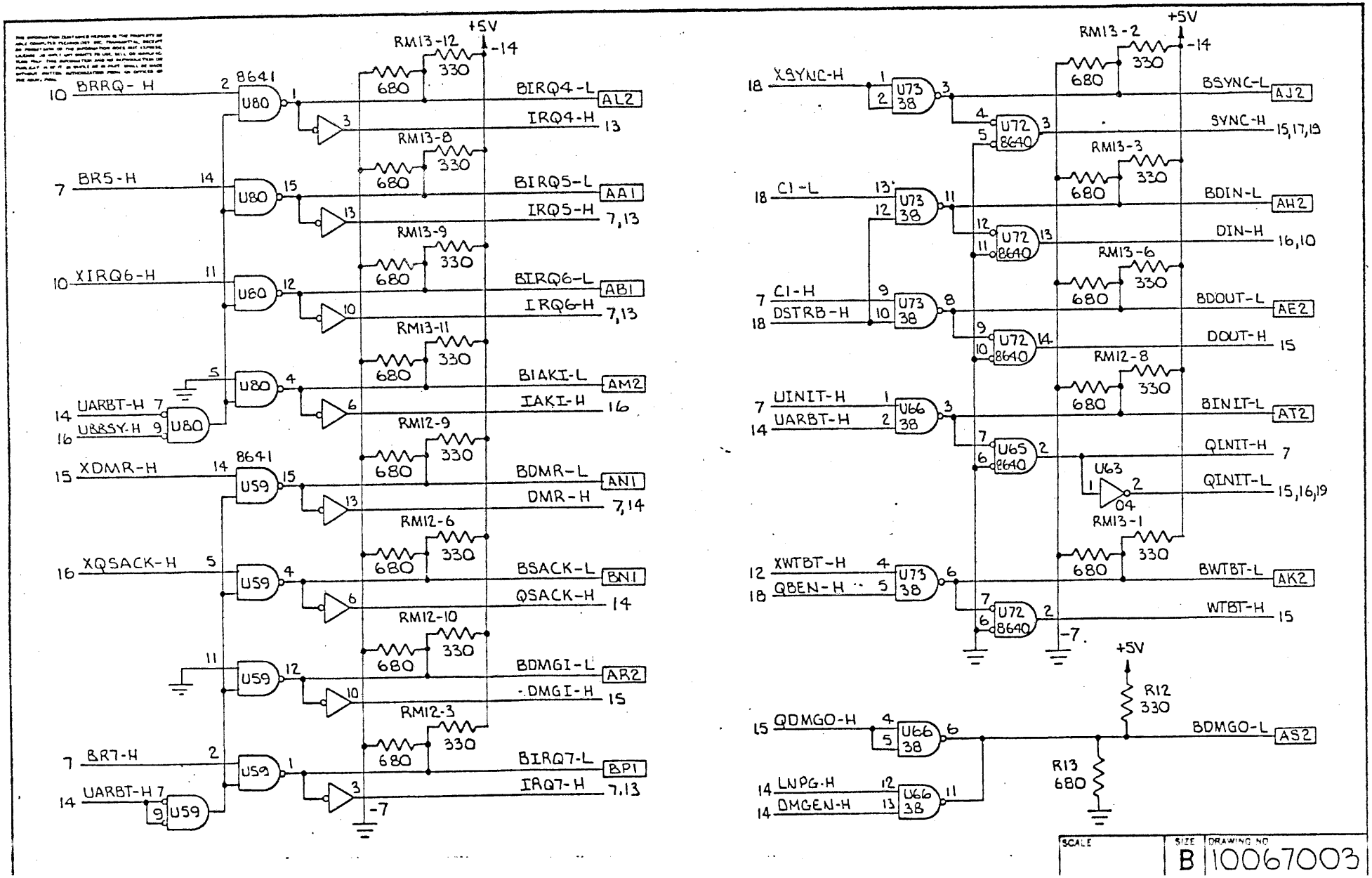


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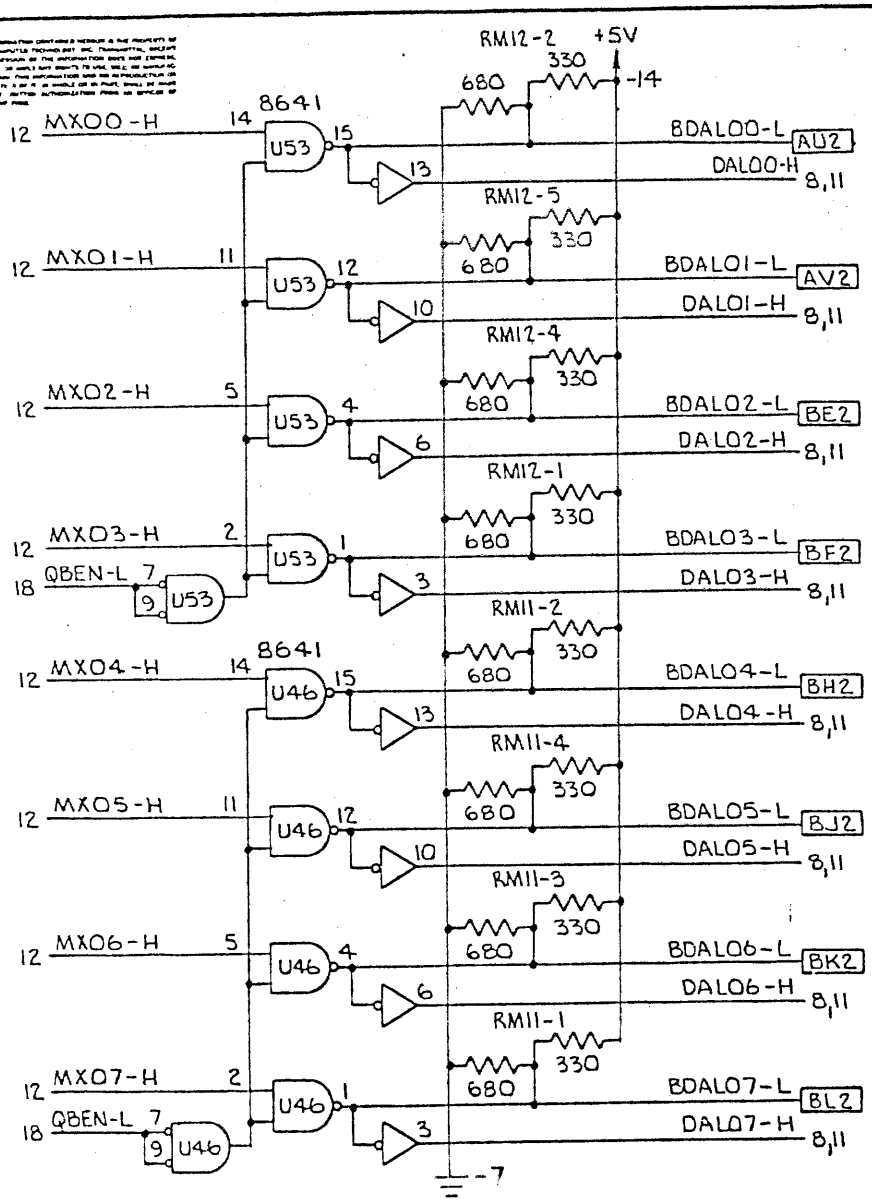


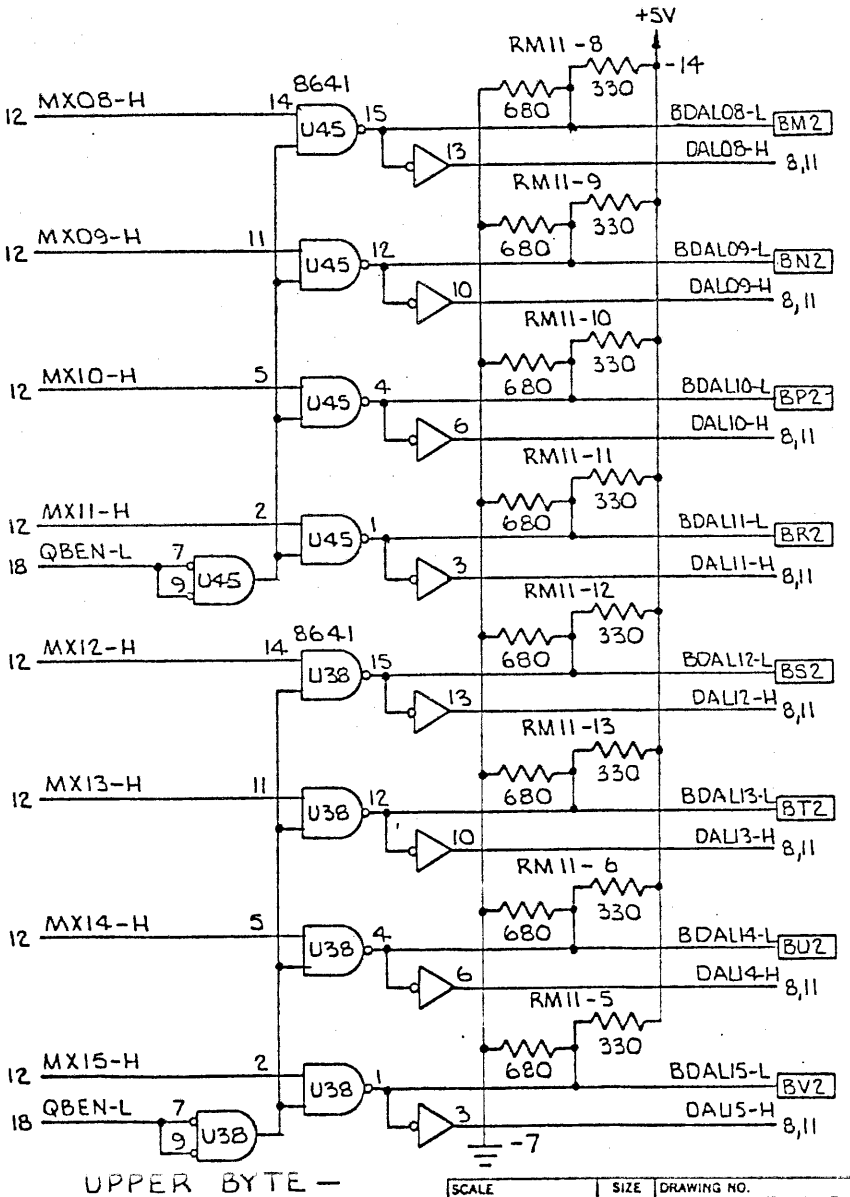


UPPER BYTE —

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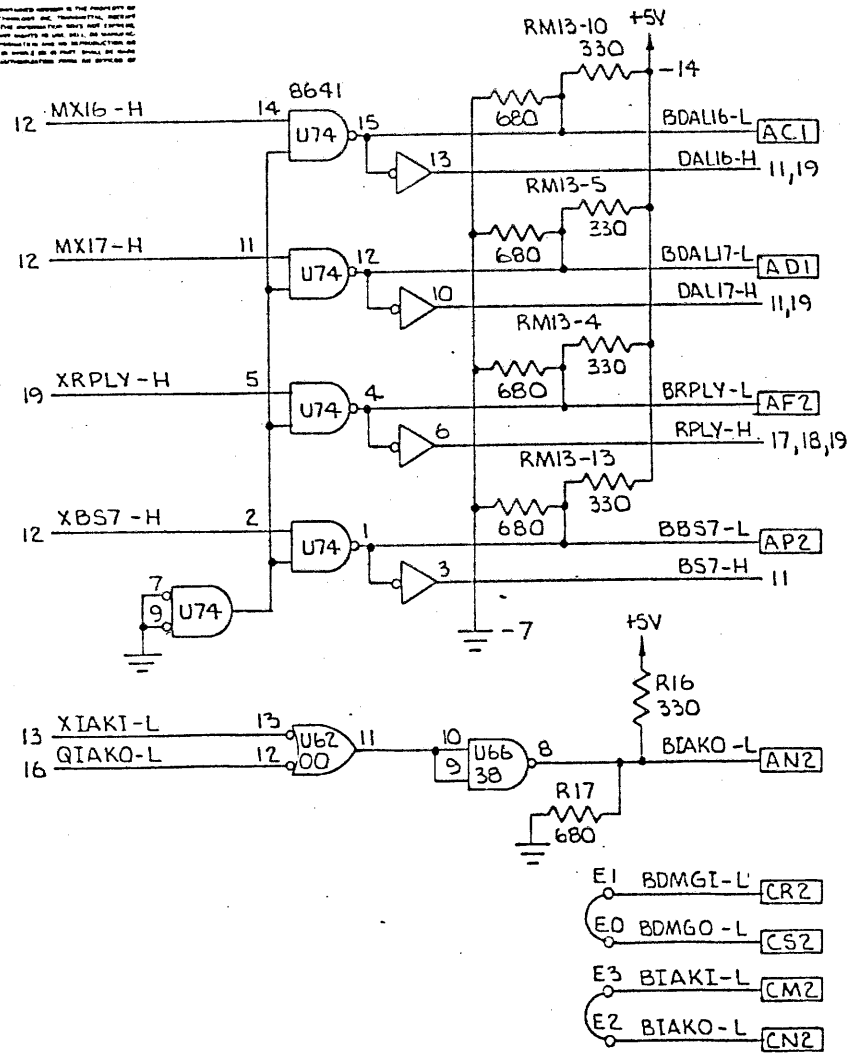
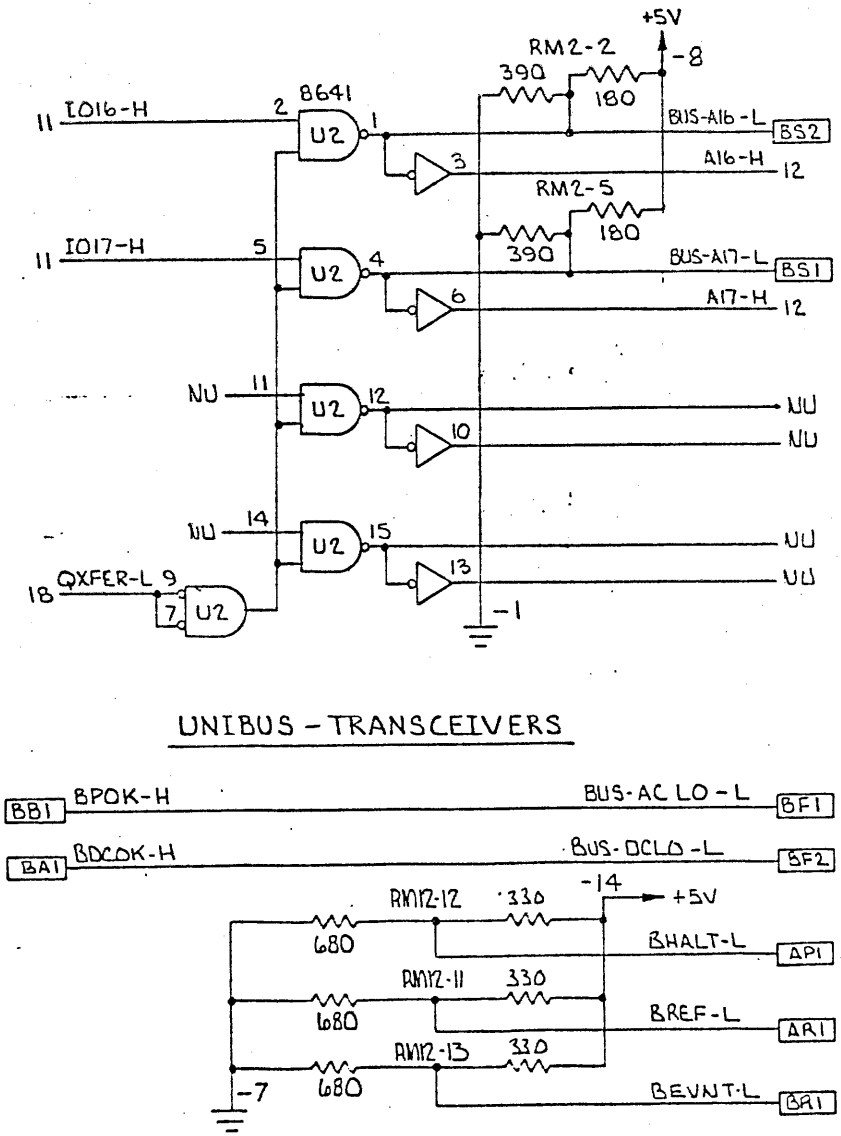



Q-BUS TRANSCEIVERS

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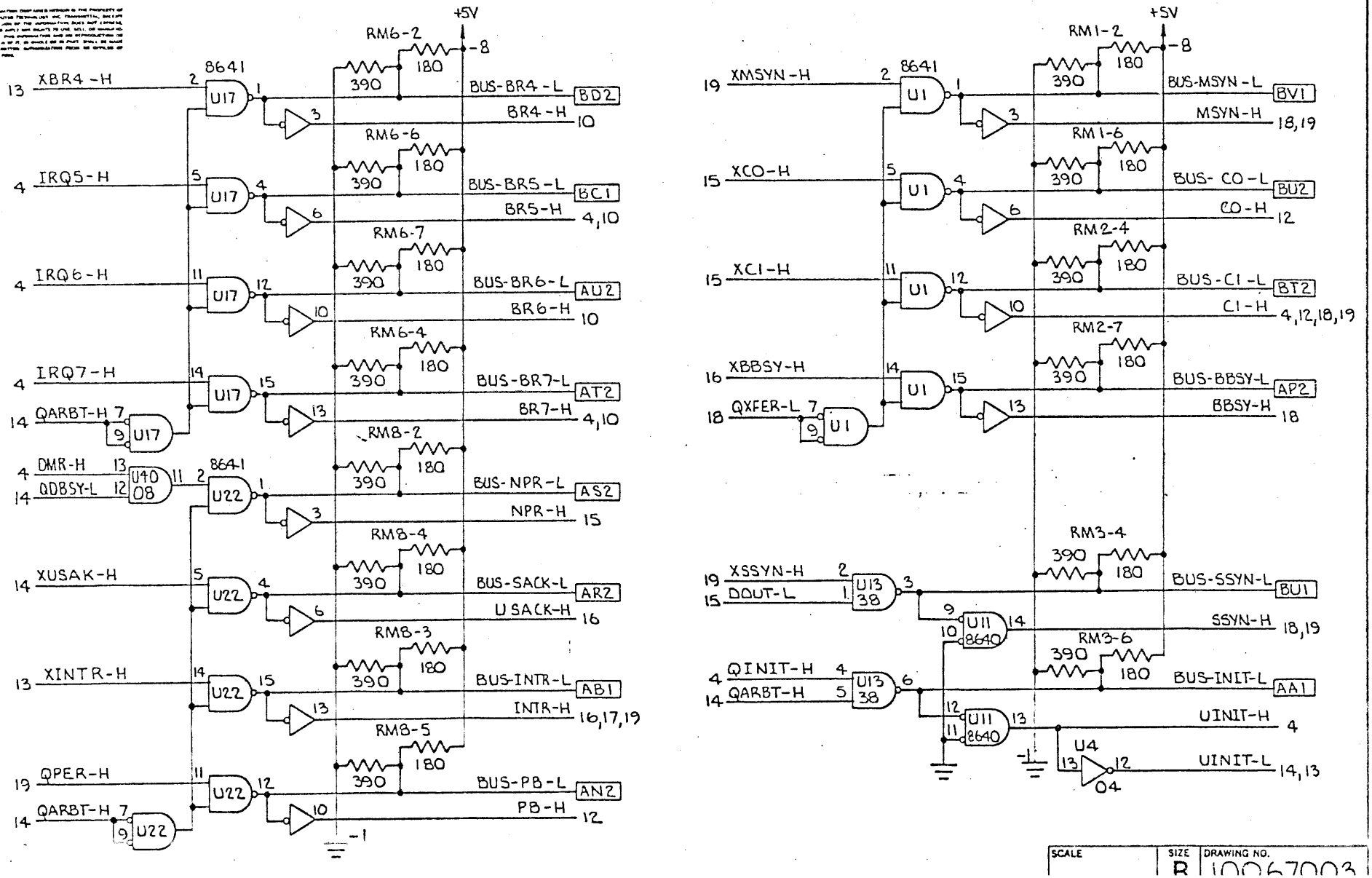


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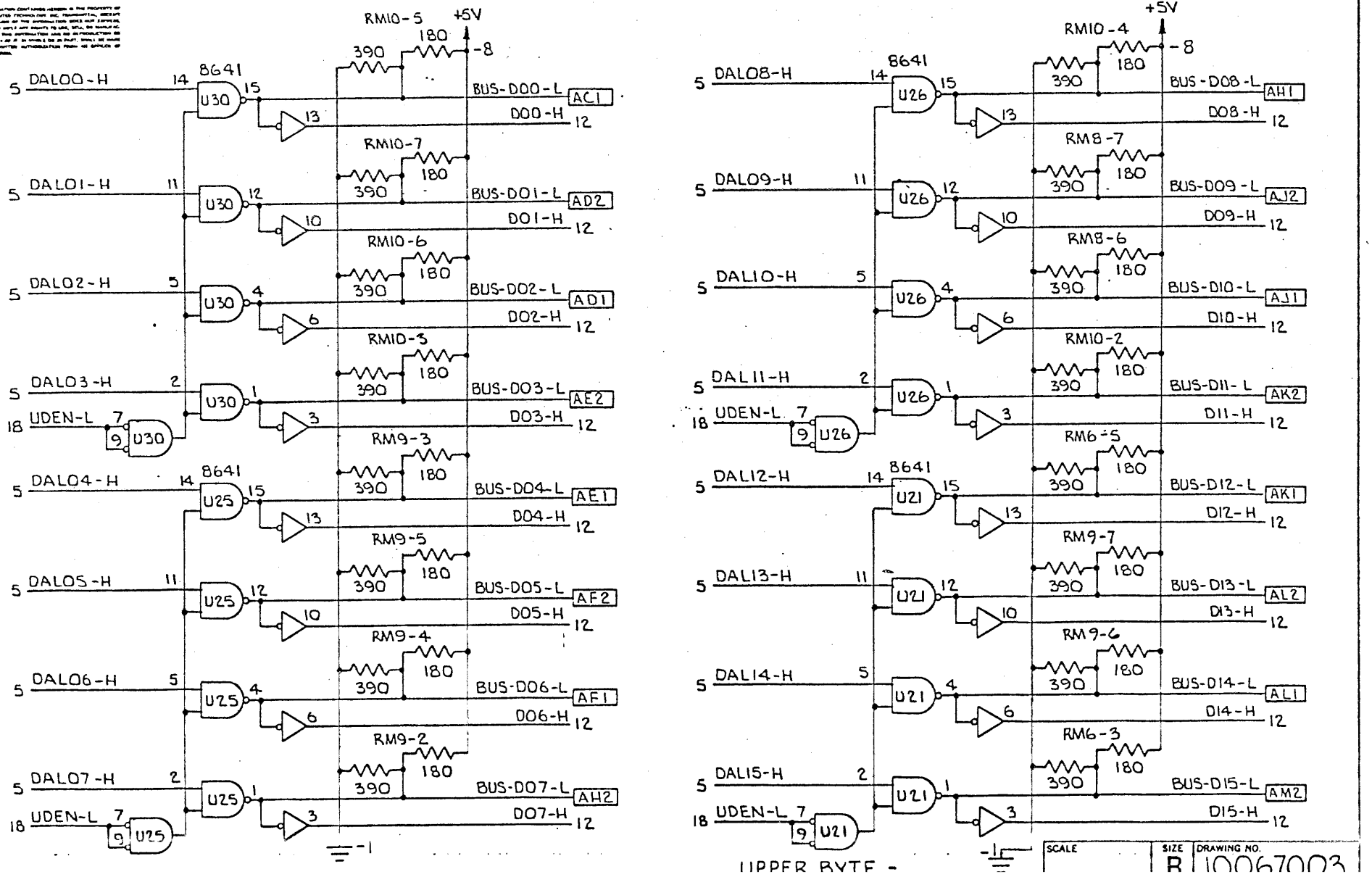
RM10-5
+5V
180
390
-8
5 DALOO-H
14
8641
U30
15
BUS-DOO-L
AC1
13
DOO-H
12
RM10-7
180
390
5 DALO1-H
11
U30
12
BUS-DO1-L
AD2
10
DO1-H
12
RM10-6
180
390
5 DALO2-H
5
U30
4
BUS-DO2-L
AD1
6
DO2-H
12
RM10-3
180
390
5 DALO3-H
2
U30
1
BUS-DO3-L
AE2
18 UDEN-L
7
9
U30
3
DO3-H
12
RM9-3
180
390
5 DALO4-H
14
8641
U25
15
BUS-DO4-L
AE1
13
DO4-H
12
RM9-5
180
390
5 DALO5-H
11
U25
12
BUS-DO5-L
AF2
10
DO5-H
12
RM9-4
180
390
5 DALO6-H
5
U25
4
BUS-DO6-L
AF1
6
DO6-H
12
RM9-2
180
390
5 DALO7-H
2
U25
1
BUS-DO7-L
AH2
18 UDEN-L
7
9
U25
3
DO7-H
12
-1
+5V
RM10-4
180
390
-8
5 DALO8-H
14
8641
U26
15
BUS-DO8-L
AH1
13
DO8-H
12
RM8-7
180
390
5 DALO9-H
11
U26
12
BUS-DO9-L
AJ2
10
DO9-H
12
RM8-6
180
390
5 DALIO-H
5
U26
4
BUS-DIO-L
AJ1
6
DIO-H
12
RM10-2
180
390
5 DALII-H
2
U26
1
BUS-DII-L
AK2
18 UDEN-L
7
9
U26
3
DII-H
12
RM6-5
180
390
5 DALI2-H
14
8641
U21
15
BUS-DI2-L
AK1
13
DI2-H
12
RM9-7
180
390
5 DALI3-H
11
U21
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BUS-DI3-L
AL2
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DI3-H
12
RM9-6
180
390
5 DALI4-H
5
U21
4
BUS-DI4-L
AL1
6
DI4-H
12
RM6-3
180
390
5 DALI5-H
2
U21
1
BUS-DI5-L
AM2
18 UDEN-L
7
9
U21
3
DI5-H
12
-1
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SCALE
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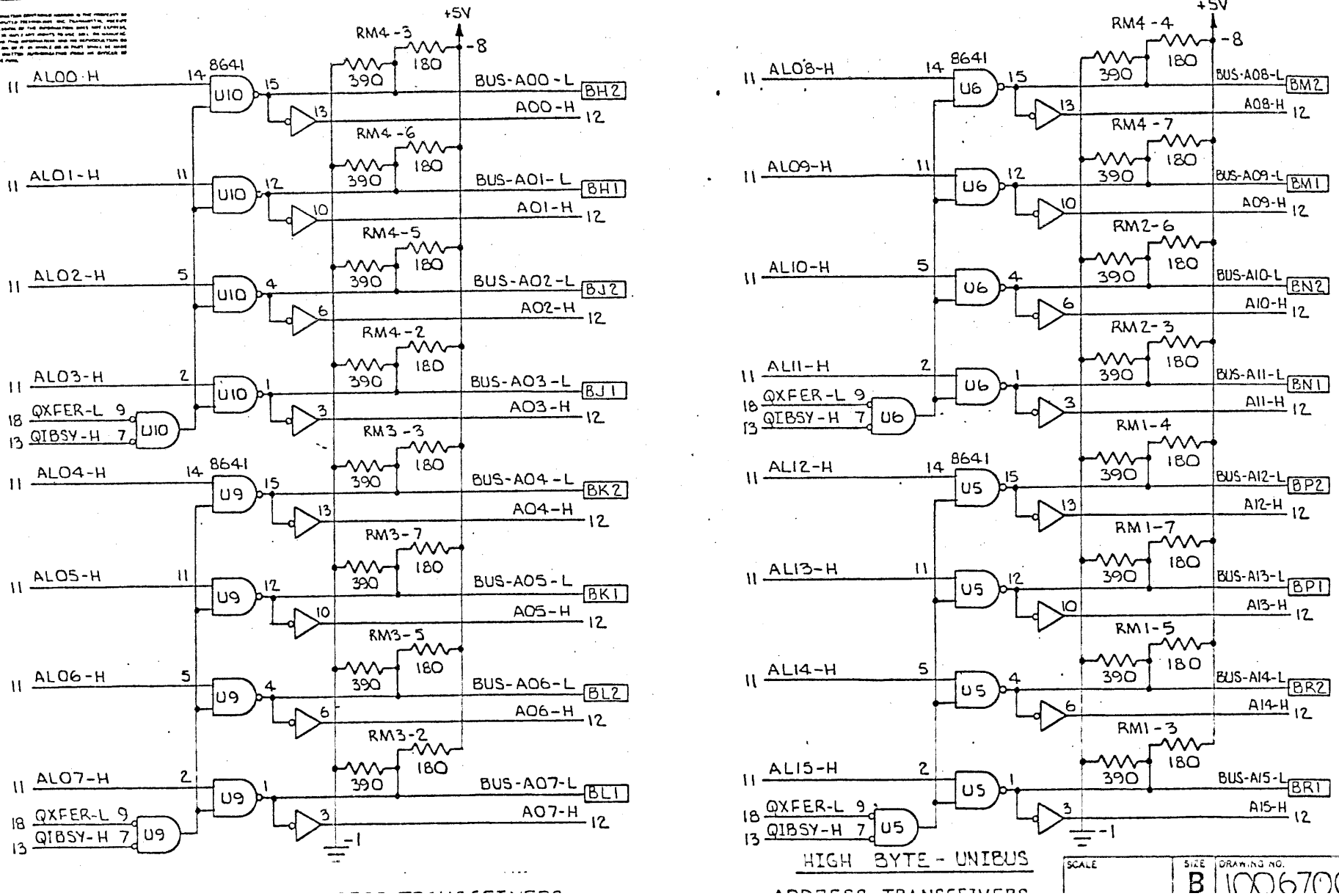
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8641
U10
U9
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ALO1-H
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ALO4-H
ALO5-H
ALO6-H
ALO7-H
QXFER-L 9
QIBSY-H 7
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BUS-A01-L
BUS-A02-L
BUS-A03-L
BUS-A04-L
BUS-A05-L
BUS-A06-L
BUS-A07-L
BH2
BH1
BJ2
BJ1
BK2
BK1
BL2
BL1
A00-H
A01-H
A02-H
A03-H
A04-H
A05-H
A06-H
A07-H
12
+5V
RM4-4
RM4-7
RM2-6
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RM1-7
RM1-5
RM1-3
390
180
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U6
U5
ALO8-H
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ALI0-H
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ALI3-H
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ALI5-H
QXFER-L 9
QIBSY-H 7
BUS-A08-L
BUS-A09-L
BUS-A10-L
BUS-A11-L
BUS-A12-L
BUS-A13-L
BUS-A14-L
BUS-A15-L
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BM1
BN2
BN1
BP2
BP1
BR2
BR1
A08-H
A09-H
A10-H
A11-H
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A15-H
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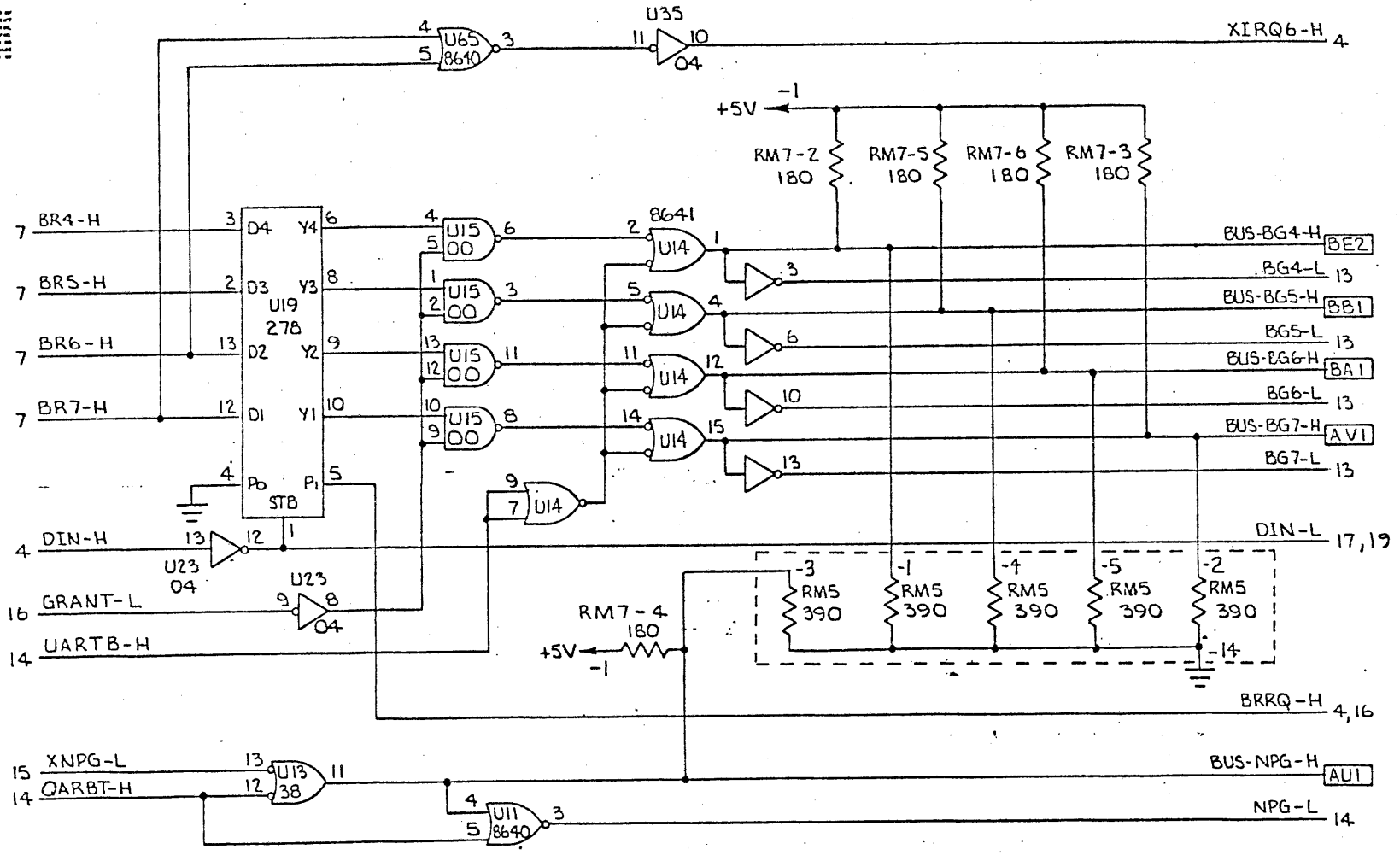


UNIBUS INTERRUPT PRIORITY - Q-BUS ARBITRATOR

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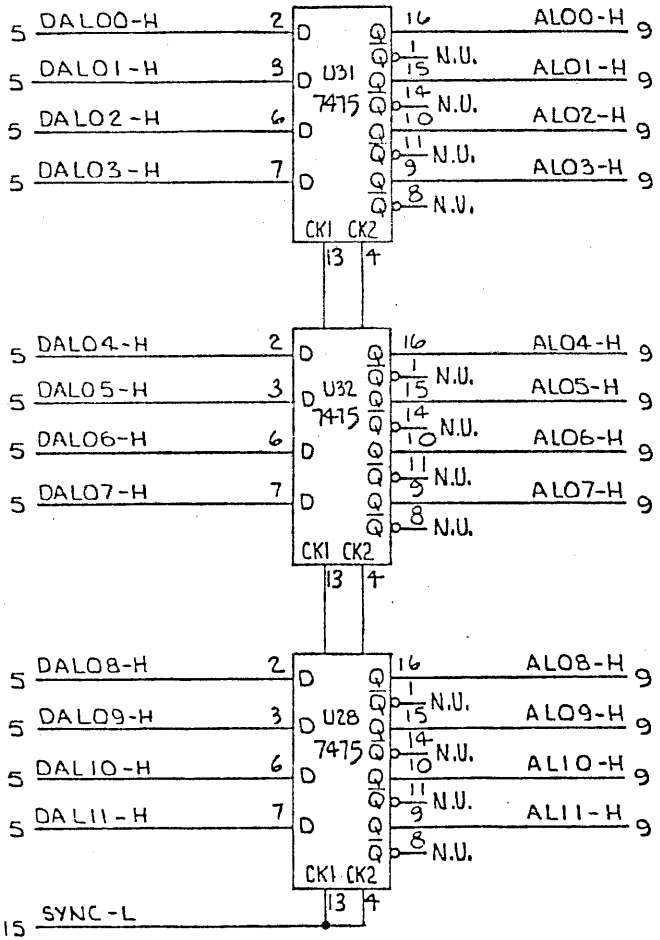
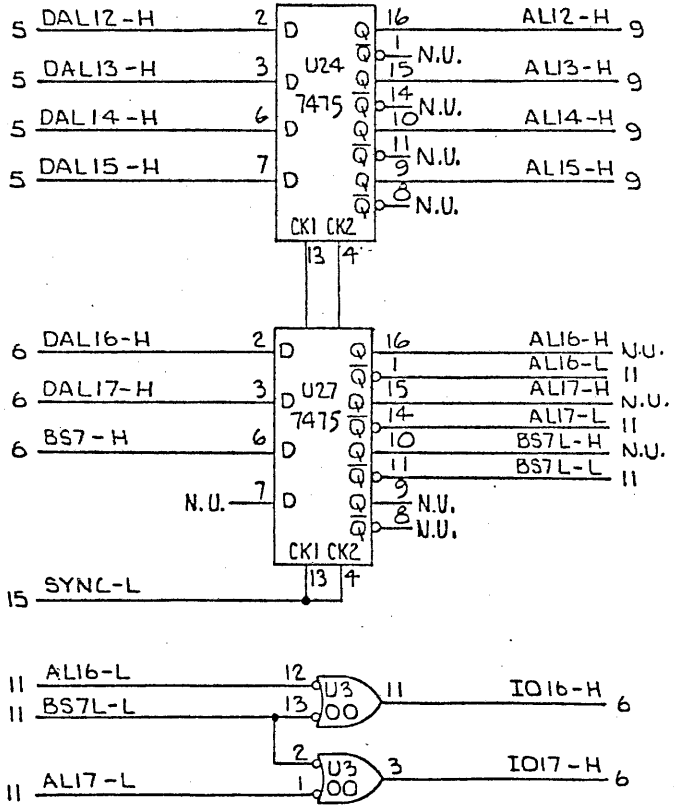
10




LOWER ADDRESS LATCH




UPPER ADDRESS LATCH

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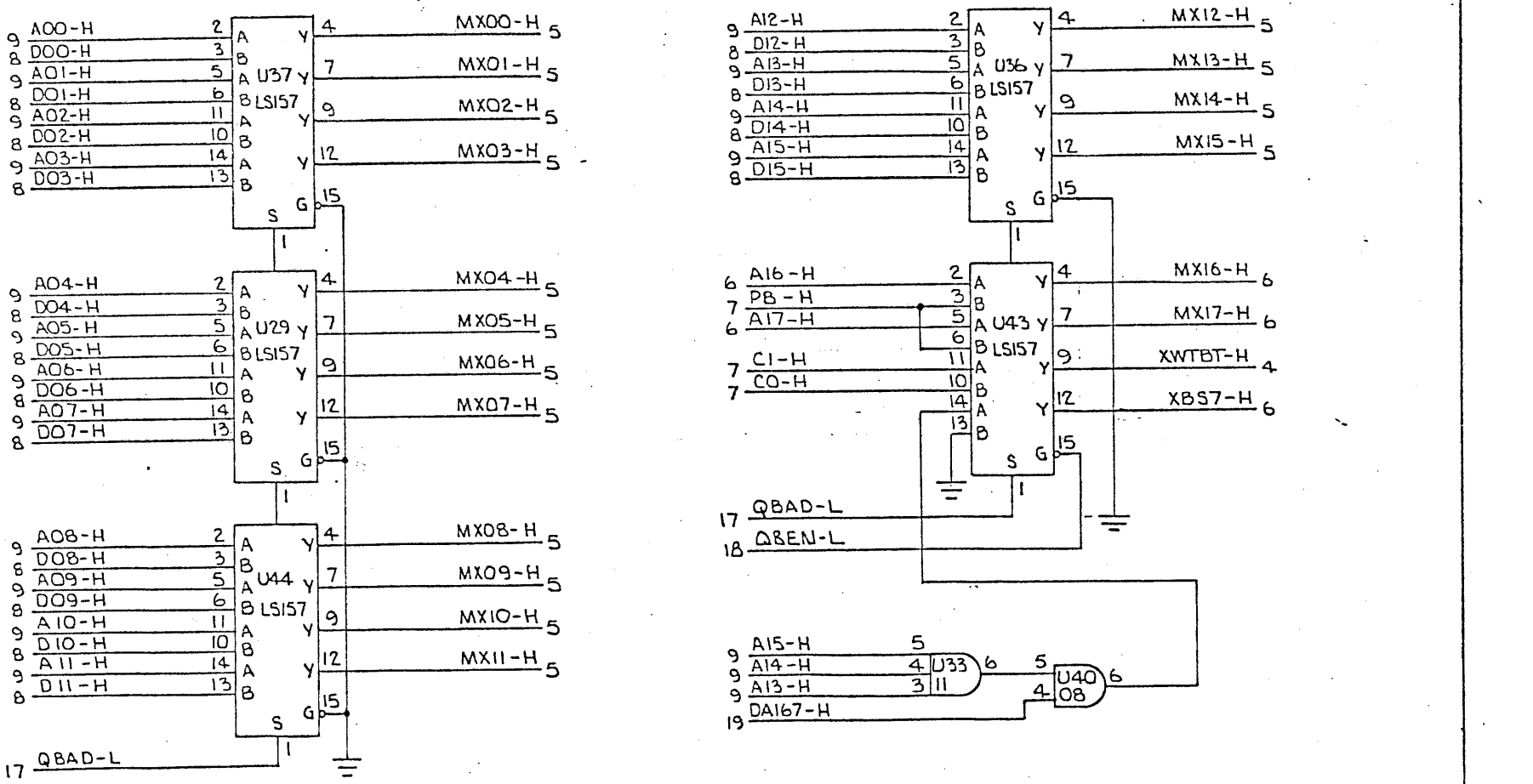


Q-BUS MUX

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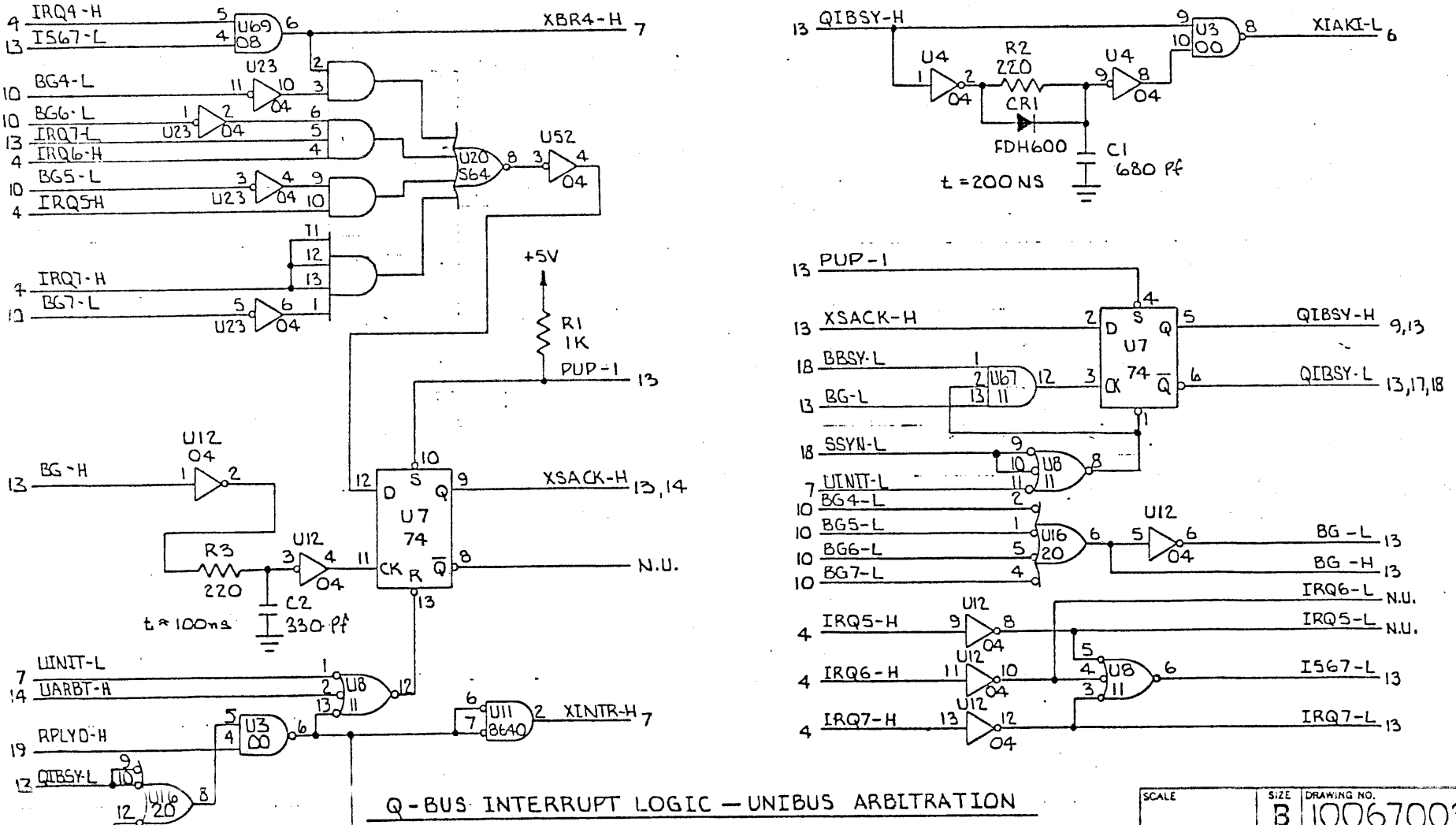


# Q-BUS INTERRUPT LOGIC — UNIBUS ARBITRATION

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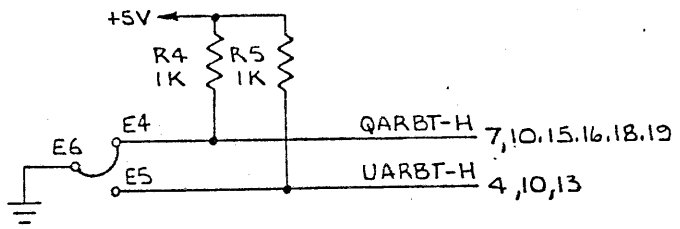
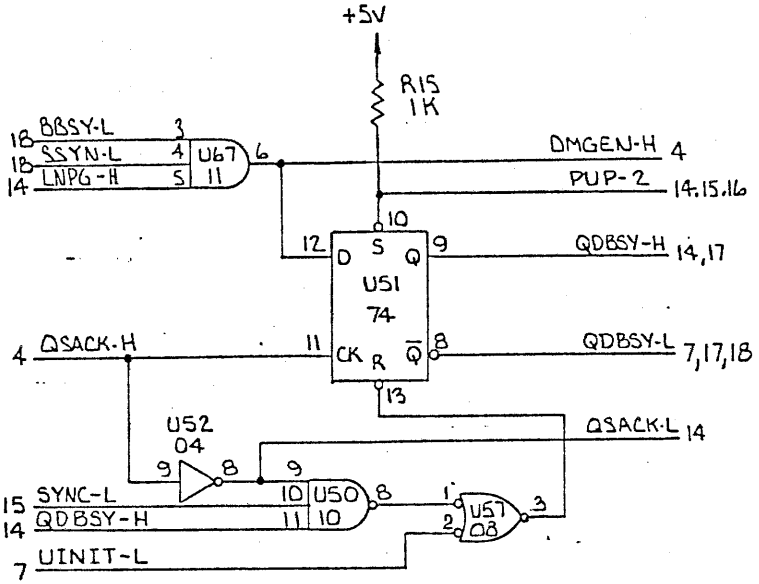
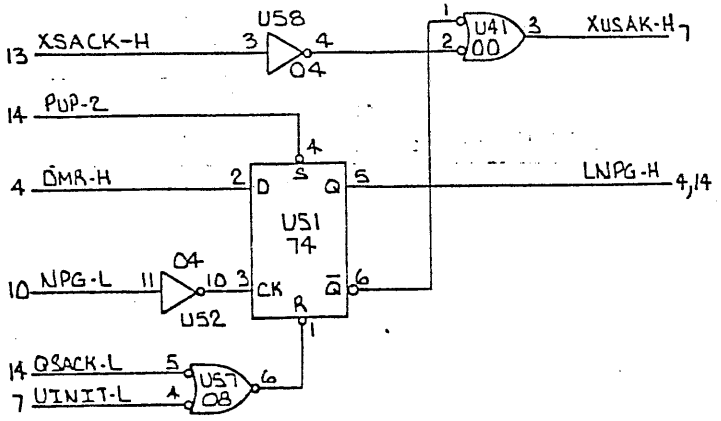



ARBITRATION SELECTION




Q-BUS DMA-UNIBUS ARBITRATOR

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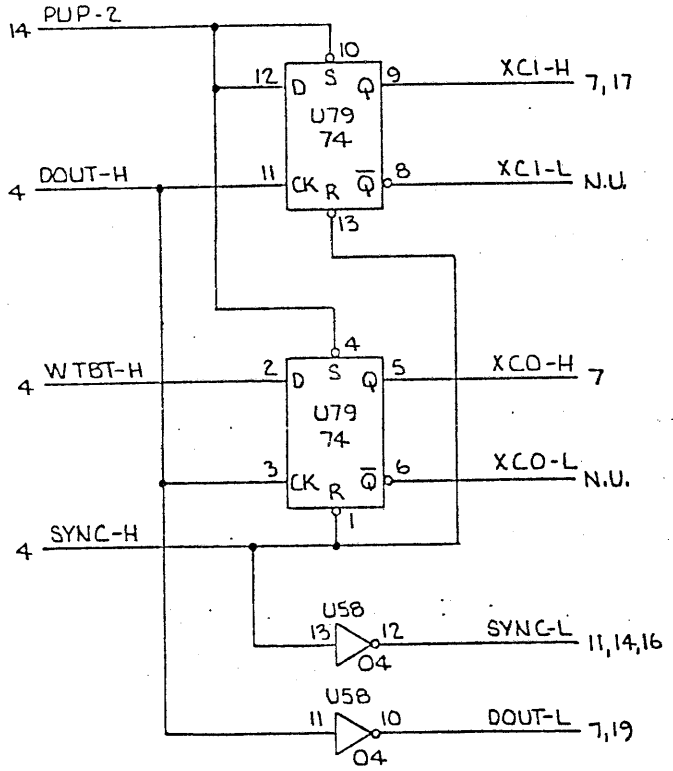
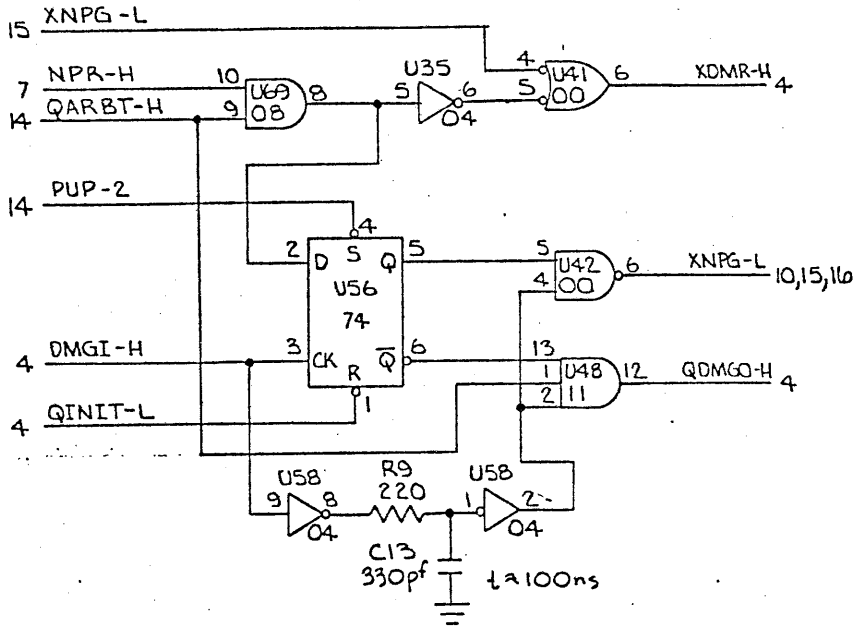
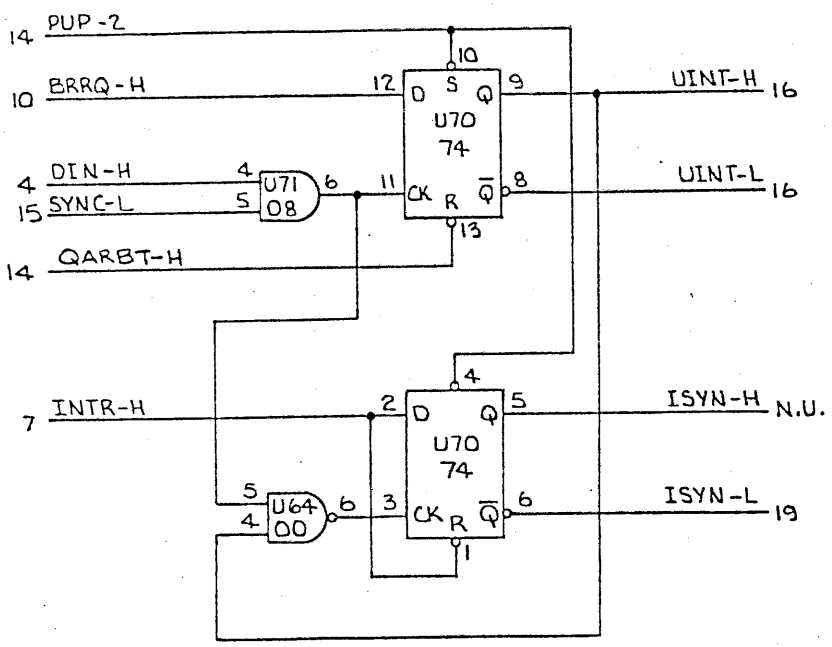
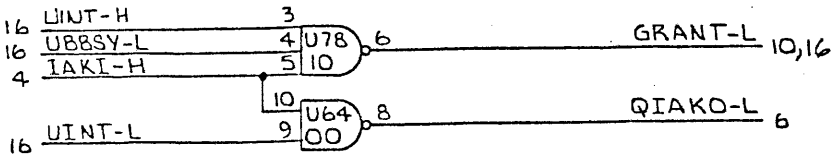



UNIBUS CO AND CI – Q-BUS ARBITRATOR

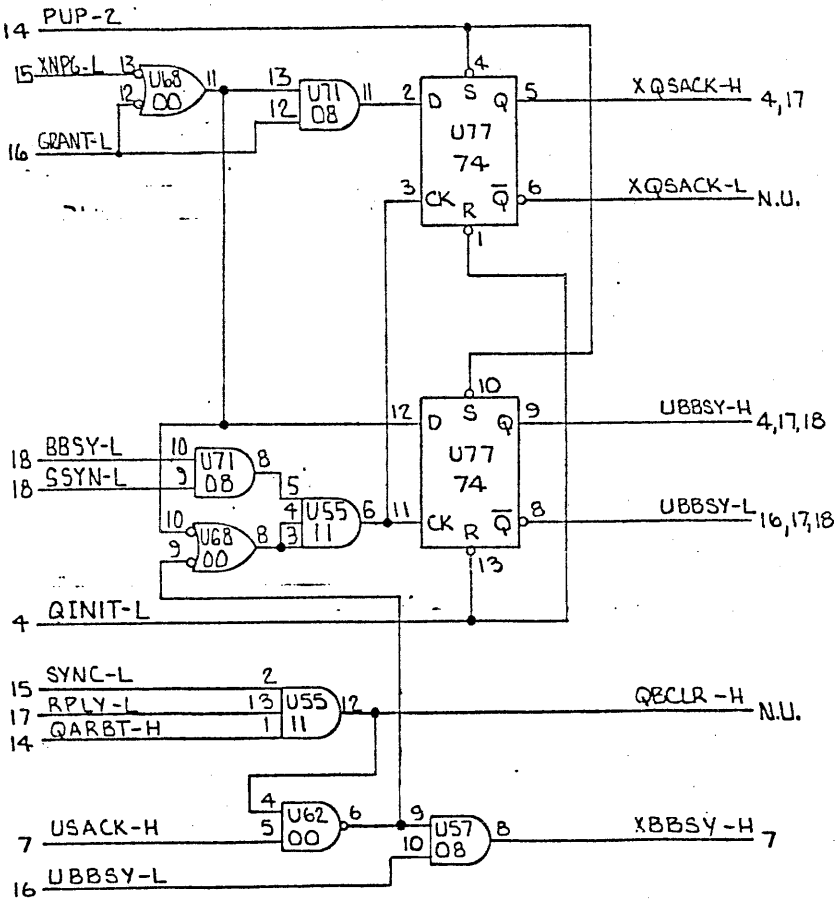



NPG - Q BUS ARBITRATOR




INTERRUPT CONTROL - Q BUS ARBITRATOR




BUS CONTROL - Q BUS ARBITRATOR

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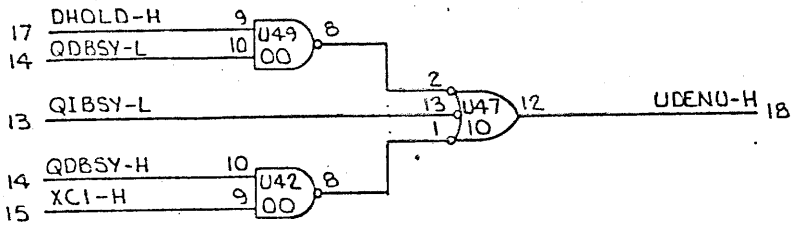
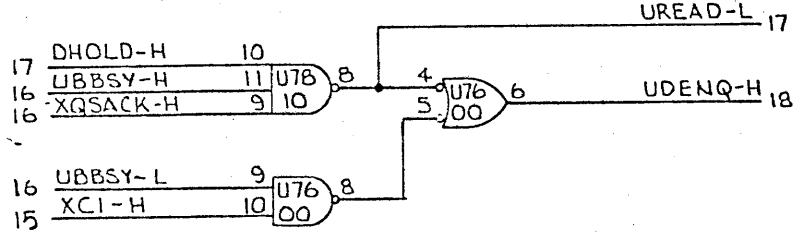
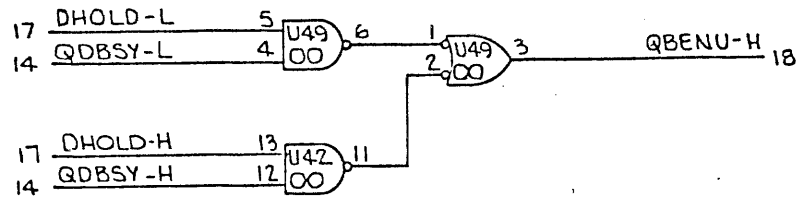


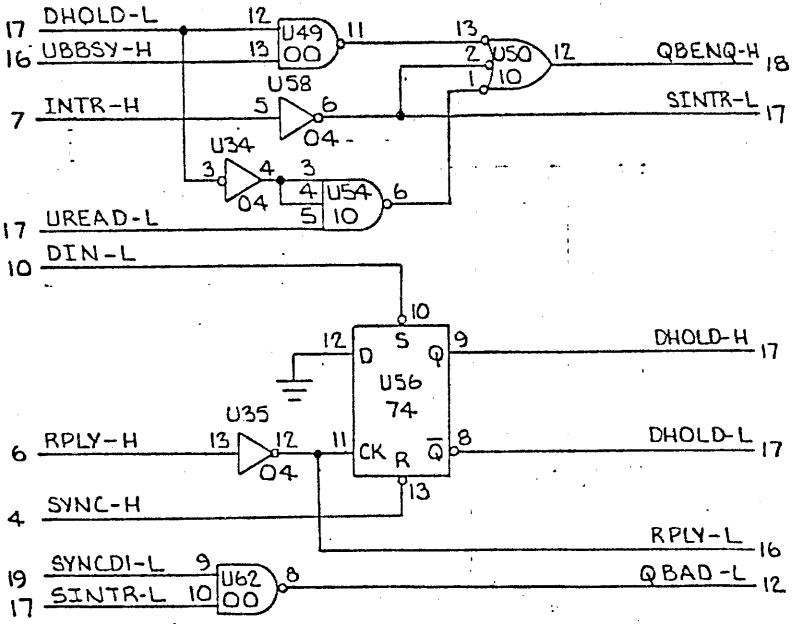

UNIBUS DATA ENABLE- UNIBUS ARBITRATION




UNIBUS DATA ENABLE – Q-BUS ARBITRATION




Q-BUS ENABLE - UNIBUS ARBITRATION




Q BUS ENABLE - Q BUS ARBITRATION

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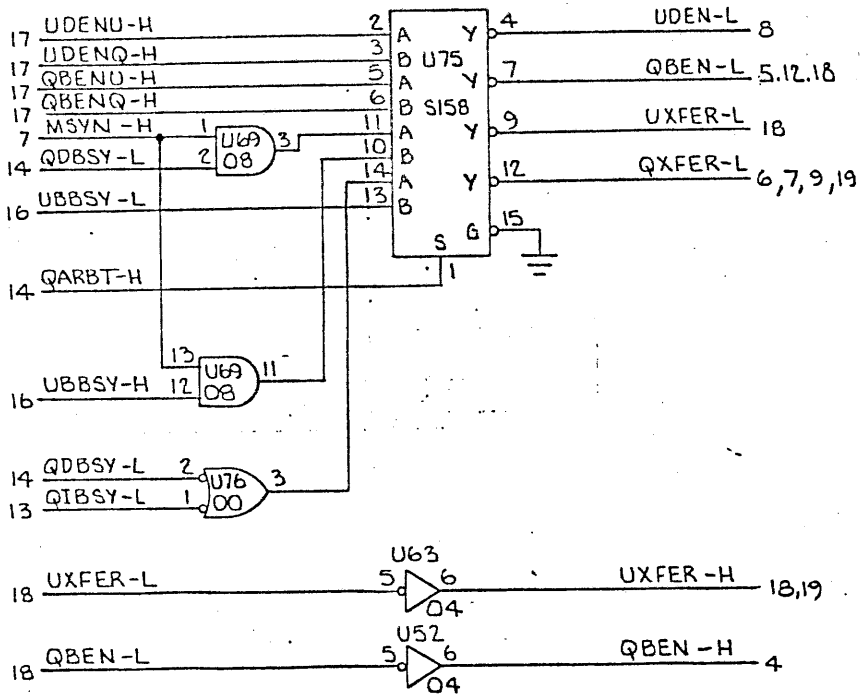
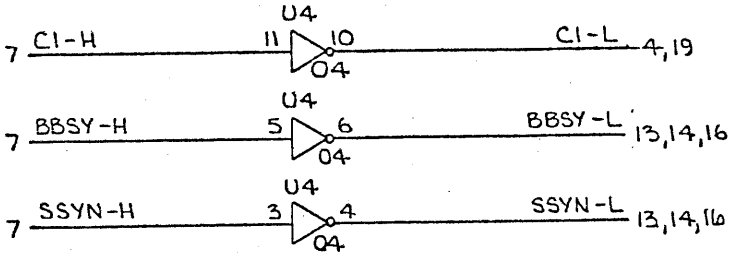
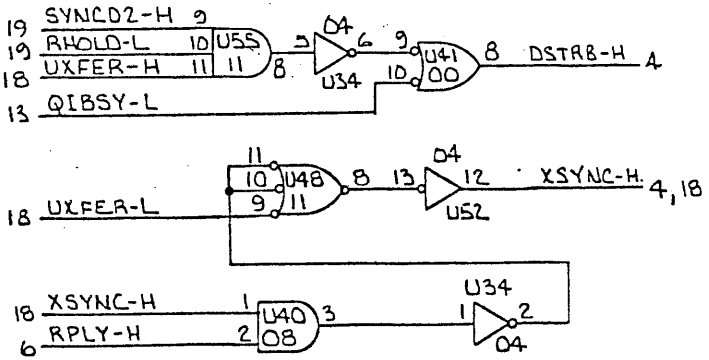









## UNIBUS ADDRESS ENABLE

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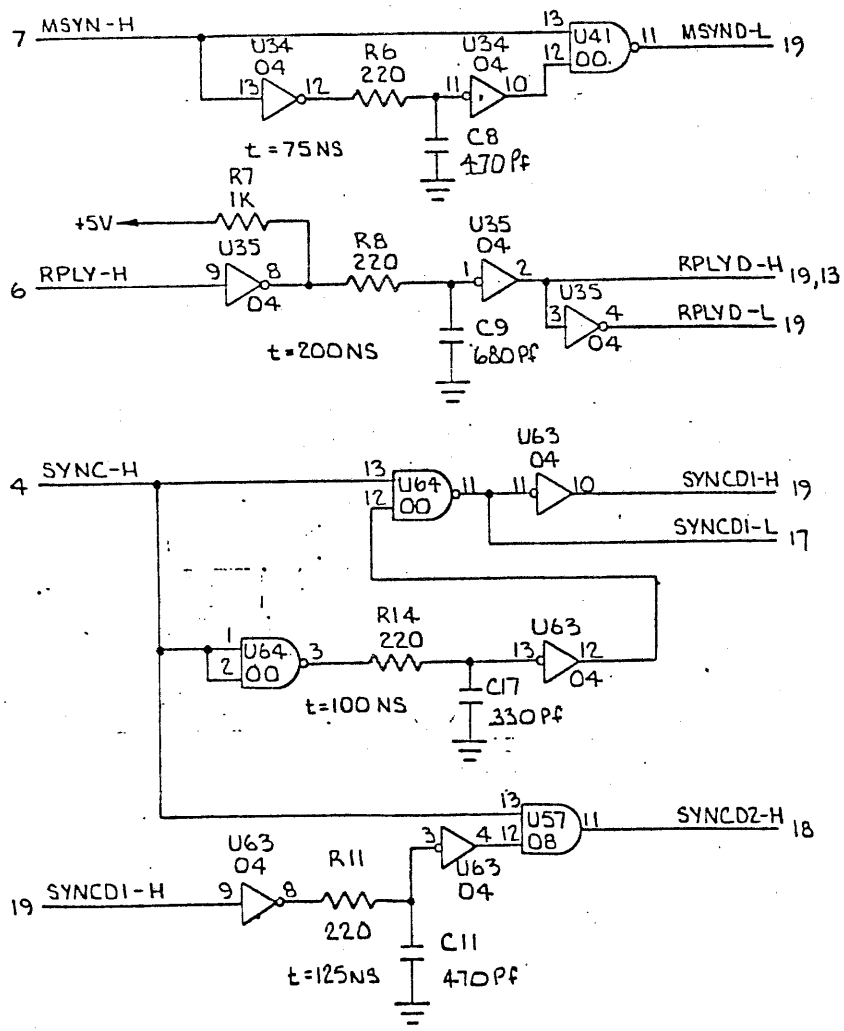
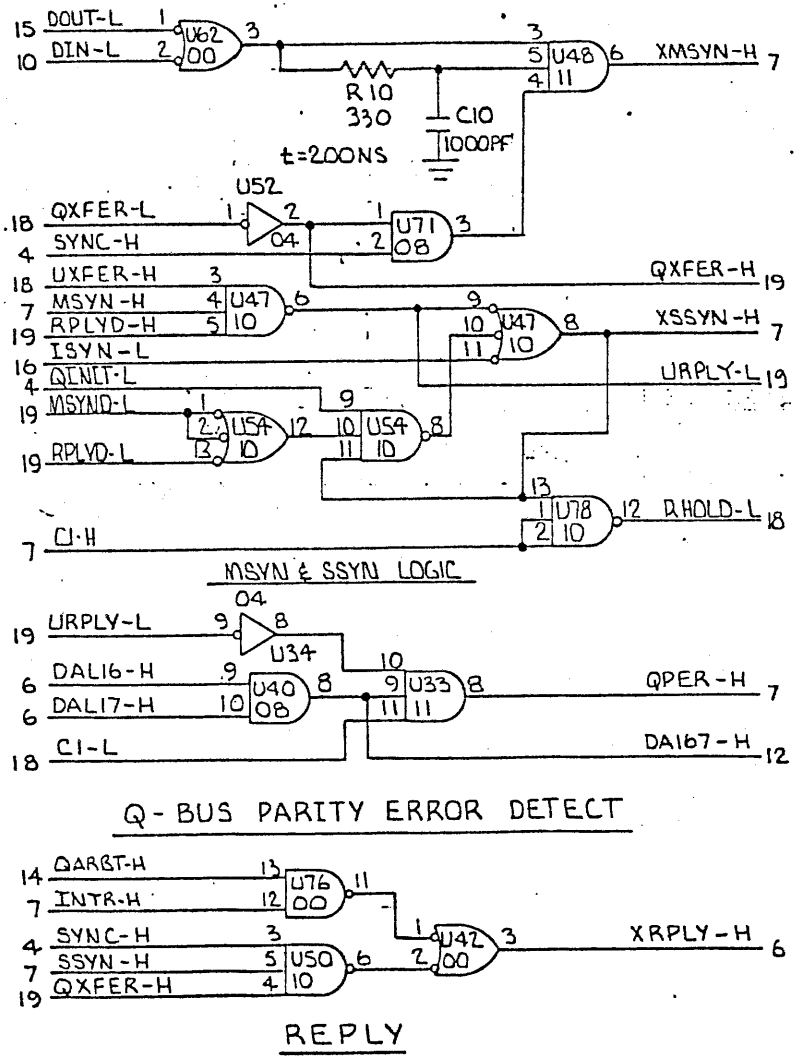



MISC. TIMING CKTS.

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