

A.C.T.

UNIVERTER

USER'S GUIDE

First Edition

June 1976

MOV /8

DAGE OPTIONS DISABLES

18 BIT ADDRESSING

Copyright by ABLE COMPUTER TECHNOLOGY

#### ERRATA

There is an Errata Sheet attached to the back cover of this manual. It is important to note the changes indicated.

# TABLE OF CONTENTS

### 1.1 Purpose and Scope 1.2 Product Definition SECTION II: DESCRIPTION 2.1 General 2.2 Physical Description Functional Description 2.3 SECTION III: INSTALLATION 3.1 General 3.2 UNIVERTER Position 3.3 Strapping Options SECTION IV: PROGRAMMING 4.1 General 4.2 UNIVERTER Registers 4.2.1 Pseudo Status Register 4.2.2 Map Registers 4.2.3 Map-Control Register

Programming Limitations

INTRODUCTION

SECTION I:

4.3

÷10			to prove the planting the story of the engineering story in the story of the story	
		•		
				Ç
				-
				i
				-7
				•
			·	
				~.
				÷

#### 1.1 PURPOSE AND SCOPE

This publication is intended for the user of the Able Computer Technology UNIVERTER Model 10001 in conjunction with a Digital Equipment Corporation LSI-11 system. It thus assumes an audience with a working knowledge of the LSI and PDP computer systems.

#### 1.2 PRODUCT DEFINITION

The UNIVERTER (Figure 1) is an easily installed low-maintenance PC board that provides full compatibility between the LSI-11 computer and the PDP-11 Unibus. Because ABLE COMPUTER TECHNOLOGY developed the UNIVERTER for full bidirectional compatibility with all current Unibus controllers, the concern about the source or destination of controller signals has been eliminated. Thus, the UNIVERTER supplies a complete communications link between the Unibus and LSI controllers and memories so they can be combined into a total system that is entirely transparent to PDP software.

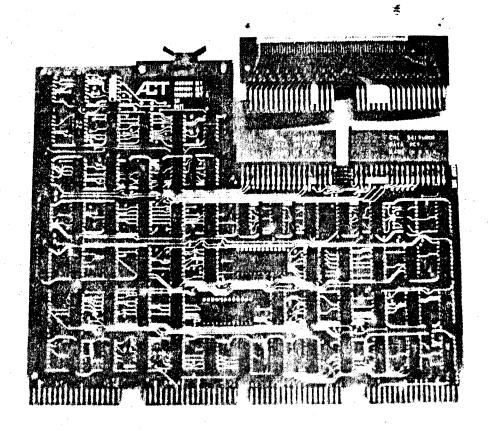


Figure 1. UNIVERTER - Model 10001

#### 2.1 GENERAL

The Model 10001 UNIVERTER, an option for the LSI-11, converts the LSI bus structure to a Unibus one and vice versa, with the LSI as bus arbitrator. In addition to providing the essential communications link between the two intrinsically incompatible bus structures, the UNIVERTER offers as standard features two important items that enhance its range of applications within the system:

- a.) A Pseudo Status Register that permits user-specified priority control over the four Unibus interrupt levels (BR4 through BR7).
- b.) An Extended Memory Map (including Map and Map-Control Registers) that permits a virtual addressing scheme with address extended up to 512K.

Inasmuch as the UNIVERTER is an internal option for the LSI-11 that plugs directly into the computer backplane, the external electrical and environmental requirements conform to those of the LSI-11 system.

#### 2.2 PHYSICAL DESCRIPTION

The UNIVERTER is a standard quad-width PC board that can be directly installed in either an LSI-ll card cage or in the PDP-11/03. It is fitted with two standard connectors on top for attachment of the Unibus cable.

Figure 2 is a simplified block diagram of a typical system containing a UNIVERTER. The figure shows clearly the essential accomplishment of the UNIVERTER: to make LSI-bus features and Unibus features appear mutually transparent and thus all accessible from both the Unibus controllers and LSI controllers, as well as from the LSI-ll processor.

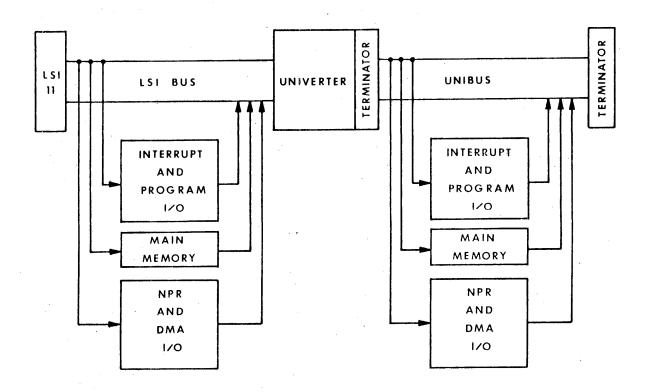


Figure 2. System Block Diagram

#### 2.3 FUNCTIONAL DESCRIPTION

Figure 3 is a simplified block diagram of the UNIVERTER itself. In this figure, the LSI bus is on the left and the Unibus on the right. former has one interrupt level, and the latter has four (BR4-7 and BG4-7). This incompatibility is bridged in part by the Pseudo Status Register, which permits user control of the four Unibus interrupts. When these are not required, the Pseudo Status Register autoinitializes to a transparent state that causes an LSI interrupt if any Unibus interrupt level requests an interrupt. the LSI acknowledges the interrupt, the UNIVERTER automatically places the acknowledgement on the highest requesting Unibus level.

The LSI bus shares the address/data (BDAL) lines in time-multiplex mode to perform the following sequence:

- 1. Display address
- 2. Issue SYNC
- 3. Remove address
- 4. Display data
- 5. Issue DATA IN or DATA OUT

The UNIVERTER operates under the LSI-11 interrupt and DMA priority structure. The entire Unibus side of the UNIVERTER (including all of the controllers linked to it) appear to the LSI bus as one physical device. Thus, the relative priorities of the Unibus subsystem and other LSI devices are determined by the physical location of the UNIVERTER

with respect to the LSI processor board, i.e., devices closer to the processor than the UNIVERTER have higher DMA and interrupt priority than Unibus devices.

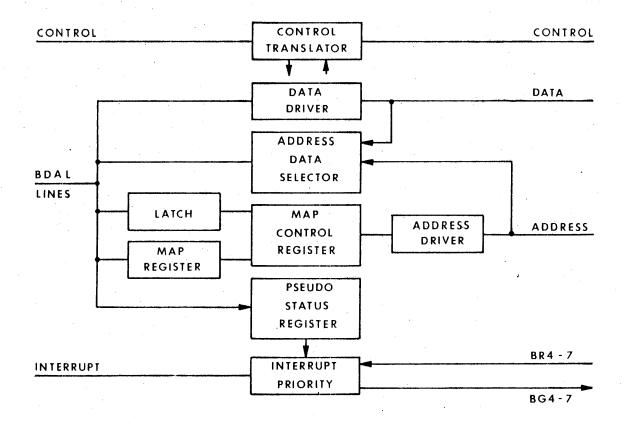


Figure 3. Block Diagram - UNIVERTER

Interrupts to the LSI-11 from given Unibus levels can be suppressed by use of the UNIVERTER Pseudo Status register. If an interrupt request is allowed by the UNIVERTER, acknowledgement lines are prevented from propagating to LSI devices farther from the processor than the UNIVERTER. Programming the Pseudo Status Register is covered in Section 4.2.

#### 3.1 GENERAL

The LSI connector module compises four slots of four columns each. The UNIVERTER and main LSI boards are four connectors wide, but most LSI I/O controllers are only two connectors wide. These latter can be installed two abreast in a slot since the LSI bus is duplicated for each pair of connectors.

The Unibus exhibits some of the best electrical characteristics in the industry because it terminates in the characteristic impedance of the cable ( $\sim 120\Omega$ ). The Unibus in a UNIVERTER installation has a terminator at <u>each</u> end (Figure 2).

#### 3.2 UNIVERTER POSITION

The UNIVERTER can go in any vacant full slot after the LSI board so long as no empty slot or half-slot occurs between the UNIVERTER and the LSI boards (Figure 4).

The distance between the UNIVERTER and the LSI boards determines the priority of the Unibus I/O devices. Devices on the LSI bus ahead of the UNIVERTER have higher priorities than the Unibus I/O devices, while LSI devices behind the UNIVERTER have lower priorities.

The flat Unibus cable plugs into the two connectors on the top of the UNIVERTER (Figure 1).

CAUTION: Install the UNIVERTER with component side facing the LSI. Power must be removed before insertion or removal of the UNIVERTER.

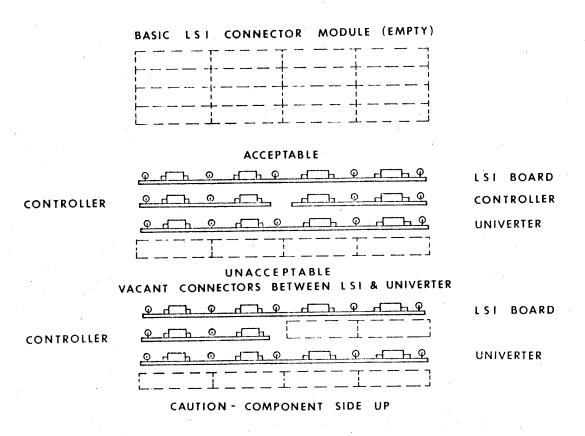


Figure 4. Connector Utilization Chart

#### 3.3 STRAPPING OPTIONS

UNIVERTER wire-wrap posts (Figure 5, El through E9) permit several strapping options.

To convert the Pseudo Status Register from the standard  $777600_8$  to  $777700_8$ , cut the etch between E9 and E10, and jumper E9 to E8.

To disable all UNIVERTER control enhancement (Pseudo Status and Map Registers), cut the etch between El and E2, and jumper E1 to E7.

To obtain access to 512K of memory from the Unibus (which has only 18 normal address bits), the PA and PB lines (PDP parity) are used as the two additional address lines. To strap this configuration, jumper E3 to E4 and E5 to E6.

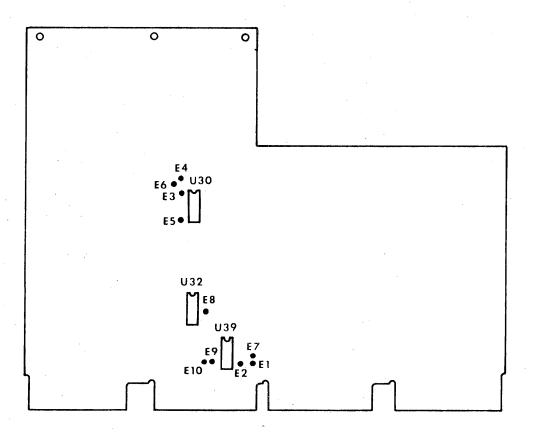


Figure 5. Option Strapping

#### 4.1 GENERAL

While it is true that the basic UNIVERTER is transparent in all respects to existing LSI/PDP software, incompatibilities exist due to design differences built into the two computers. These points require special consideration and are fully discussed in Section 4.3

WARNING: Disregard of the limitations will lead to random program errors.

#### 4.2 UNIVERTER REGISTERS

The UNIVERTER contains three types of registers: the Pseudo Status Register, the Map Registers, and the Map-Control Register.

#### 4.2.1 Pseudo Status Register (7776008)

The format of the Pseudo Status Register is

15	·	7 6	5		0
	1	PRIOR:	ITY	*	
	ļ				

where the interrupt priority bits (7-5) function like a PDP-11 status register. The Pseudo Status Register is reset to ZERO by RESET.

<u>CAUTION</u>: The Pseudo Status Register must be loaded under software control and is not automatically updated by the processor.

To change the address of the Pseudo Status Register to 7777008, cut the etch at E9-E10 and jumper E9 to E8.

## 4.2.2 Map Registers (7776028 through 7776348)

The format of the Map Register is

15	7	6.	.5	. 4	. 3	2	1	0
	A19	A18	A17	Al6	A15	A14	A13	A12

where the contents of these registers replace the high-order bits of the virtual address on the bus. Each register controls a 2K-block of virtual addresses (Figure 6). Two areas are reserved and nonrelocatable: 0-2K (vector space) and 30-32K (I/O space).

As shown in the figure, register assignments and block assignments are contiguous. Thus, 7776028 controls 2-4K virtual, 7776048 controls 4-6K virtual, etc.

Since Map Registers are volatile, after Power Up they must be initialized by software. To prevent a specific block from being relocated, software makes the register data equal to the virtual address.

THE UNIVERTER virtual memory scheme applies only to memory on the Unibus. Therefore, if memory is on the LSI side of the UNIVERTER, the Map Registers <u>must</u> be equal to the virtual addresses

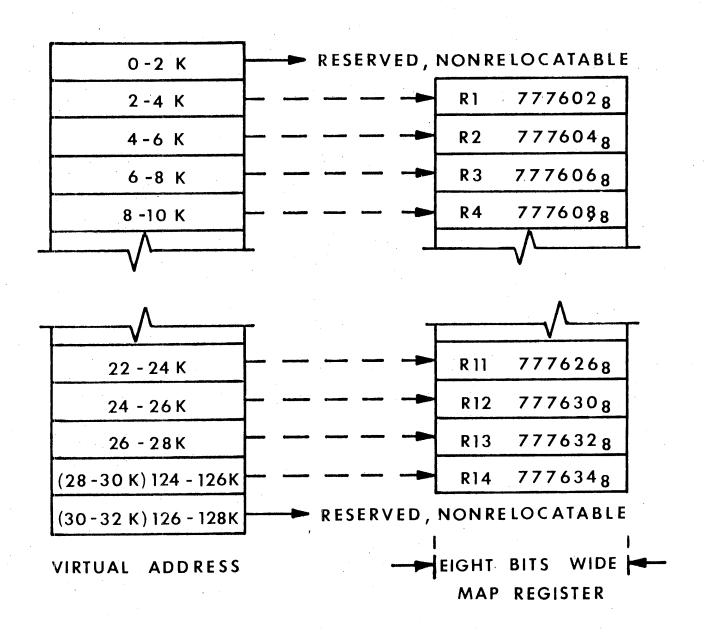


Figure 6. Map Register Control Assignments

applicable to the amount of LSI memory. For example, if 0-8K is on the LSI bus, Map Registers R1-R3 must have data values of  $001_8$ ,  $002_8$ , and  $003_8$ .

<u>CAUTION</u>: This memory block cannot be mapped.

Thus, addresses capable of being generated by the software  $(0-32\text{K or }000000_8\text{ to }177777_8)$  are considered virtual addresses. UNIVERTER monitoring of the 2K blocks of these addresses is such that the four most significant bits of the sixteen-bit address effect operation of the Map Registers. For example, set the address 0-32K as  $vv0000_8$  to  $vv7777_8$ .

The Map Registers permit memory access from 0 to 512K as physical addresses to the Unibus. These physical addresses ppp00000 $_8$  to ppp7777 $_8$  provide an octal address range of 0000000 $_8$  to 3777777 $_8$ . Thus there are 256 (000 $_8$  to 377 $_8$ ) 2K blocks of addresses in the 512K range of physical addresses, and sixteen (00 $_8$  to 17 $_8$ ) 2K blocks in the 32K range of virtual addresses.

If instead of using the four most-significant virtual-address bits vv as the most-significant physical address, we use the eight Map-Register bits ppp, we have a virtual memory scheme where vv becomes the address of one of sixteen Map Registers. Relocations are made in 2K groups.

The physical address transferred to the Unibus is thus a combination of the lower twelve

virtual-address bits (11-0) and the contents of the addressed Map Register (A17-A12). The latter can use the former Unibus parity lines (PA and PB) to provide bits A19 and A18 when the UNIVERTER is strapped for 512K. Figure 7 shows this development of the physical address.

The PDP-11 converts virtual addresses of 28-32K to 124-128K. Since I/O addresses are not usually assigned to addresses below 126K, the UNIVERTER allows that space to be assigned as memory space.

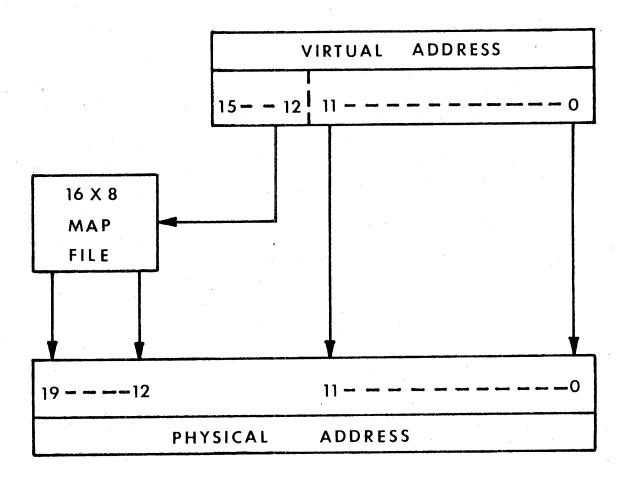


Figure 7. Physical Address Generation

# 4.2.3 Map-Control Register (777636<sub>8</sub>)

Bit 0 of the Map-Control Register determines the addressing scheme. When bit 0 is ZERO, the virtual address is equal to the physical address. When bit 0 is ONE, the Map Registers relocate the virtual address to the new physical address according to the system explained in Section 4.2.2.

System reset resets the Map-Control Register.

#### 4.3 PROGRAMMING LIMITATIONS

The user must be constantly aware that LSI-11 software is not fully compatible with the rest of the PDP-11 computer family. Since the UNIVERTER successfully bridges the <u>bus</u> incompatibility, it is easy to assume that <u>all</u> incompatibilities are corrected. This is not true.

There are three cases where software incompatibilities cannot be overcome by UNIVERTER hardware.

The most important of these is the operation of the program status register. The LSI status register cannot be accessed as a memory address. This means that much current PDP software will not work on the LSI, where the status register can be accessed only by special MOVE instructions. To be transparent across the LSI/PDP line, the PDP software must be modified to use an indirect method of addressing the status register. Such methods include operations using a trap vector or an artifical value on the stack to initialize the status register with the proper configuration.

There is also a conflict between the standard UNIVERTER option addresses and those of the Memory Management Unit (MMU). However, the basic UNIVERTER addresses of  $777600_8$  to  $777636_8$  can be strapped to  $777700_8$  to  $777736_8$ .

Another strapping option permits disabling of all UNIVERTER options (Section 3.3).

Finally, it must be noted that information read from the UNIVERTER registers is <u>image data only</u>. Thus, the contents of the Pseudo Status Register and of the Map-Control Register cannot be read directly onto the bus. When data are written into these registers, a copy of the data is stored in a RAM. If the system is initialized, the data read from these registers are not valid until the registers have been written into at least once since initialization.

In all other cases, the UNIVERTER is transparent to existing software. However, note that use of UNIVERTER special features requires software modification.

The following corrections must be made as noted:

#### 3.3 STRAPPING OPTIONS

Third paragraph to read the following:

To disable all UNIVERTER control enhancement

(Pseudo Status and Map Registers), cut the etch

between El and E2, and jumper El to E7.

4.2.3 Heading should read the following:

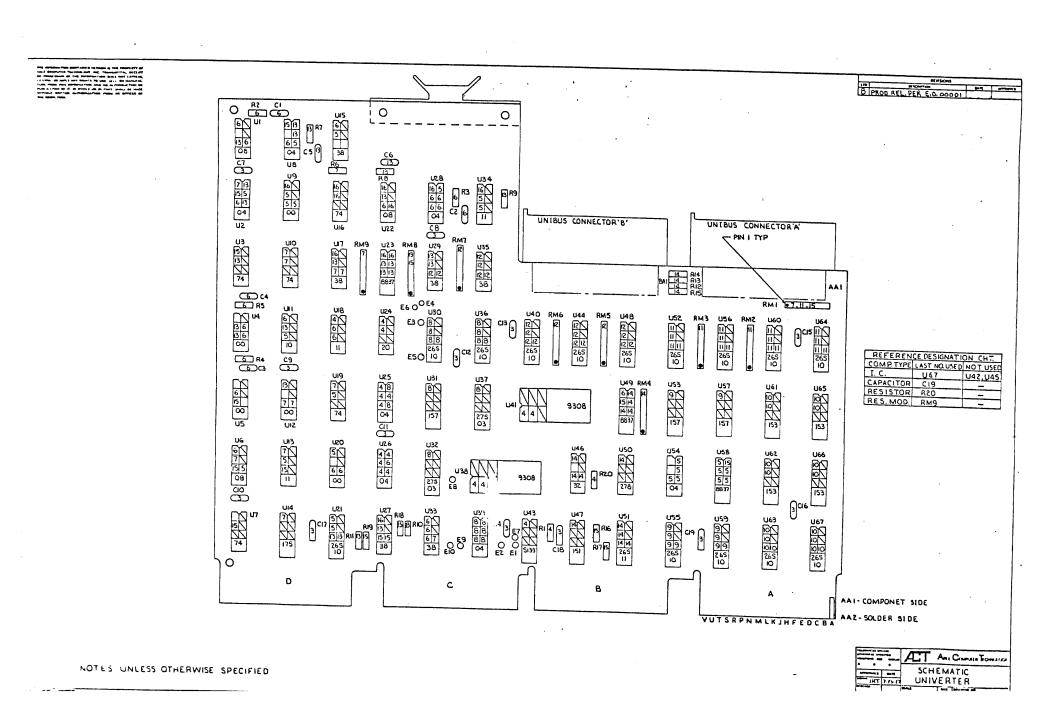
Map-Control Register (7776368)

THE INFORMATION CONTAINED HEREON IS THE PROPERTY OF ABLE COMPUTER TECHNOLOGY, INC. TRANSMITTAL, RECEIPT ON POSSESSION OF THE INFORMATION DOES NOT EXPRESS, LICLINSE, OR IMPLY ANY RIGHTS TO USE, SELL, OR MANUFACTURE FROM THIS INFORMATION AND NO REPRODUCTION OR PUBLICATION OF IT, IN WHOLE OR IN PART, SHALL BE MADE WITHOUT WRITTEN AUTHORIZATION FROM AN OFFICER OF THE ABOVE FIRM.

# REF. ONLY

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES		AIT	ABLE	COMPUTER TECHNOLOGY
400000000		50	`HF	MATIC
APPROVALS	DATE			
JRT	7/8/77		ΗV	ERTER
CHECKED	5-2-72	SCALE	SIZE	DRAWING NO.
/	6.2.75		В	10001003
11	1.2.78	DO NOT SCA	LE DRA	WING SHEET LOGIA

2. ALL CAPACITORS ARE IN MICROFARADS 1. ALL RESISTORS ARE 1/4 WATT, 5% NOTES: UNLESS OTHERWISE SPECIFIED



THE INFORMATION CONTAINED HEREON IS THE PROPERTY OF ABLE COMPUTER TECLINOLOGY, INC. TRANSMITTAL, RECEIPT ON POSSESSION OF THE INFORMATION DOES NOT EXPRESS, EXCENSE, OR IMPLY ANY RIGHTS TO USE, SELL, OR MANUFACTURE FROM THIS INFORMATION AND NO REPRODUCTION OF PUBLICATION OF IT, IN WHOLE OR IN PART, SHALL BE MADE WITHOUT WRITTEN AUTHORIZATION FROM AN OFFICER OF THE ABOVE FIRM.

THRU

C16

.01UF ---- GND

- GND

 $-C17 \perp C18 \perp C19$ 

T 47UF T 4.7UF T 4.7UF

LSI CONNECTOR D

HT	1	D	2	SHT
15 15	BDCOK-H <b>BPoK-</b> H	Α	+5	
15	BPOK-H	ВС		
			GND	
		D		
		E		
		E		
		H		
	GND	J		
		K		
		<u> </u>		
	GND	М		<u> </u>
16	BSACK-L	N		
		P		
		R		
		S		<u> </u>
	GND	IT		
		U		
		LV		
		ΝE	CTOR C	
C 1 17		-		

		V		!!
	LSI CON	ΝE	CTOR C	
SHT	ı	C	2	SHT
		Α	+5V	
		В		
		C	GND	
		D		
		E	BDOUT-L	6
		E	BRPLY-L BDIN-L	5
		Н		6
	GND	J	BSYNC-L	6
		K	BWTBT-L	5,6
		ل ا	BIRQ-L	15
	GND	M	BIAKI-L	15
13	BDMR-L	N	BIAKO-L	15
		P	BBS7-L	
		R	BDMG1-L	13
		S	BDMGQ-L	13
	GND	T		
		U		
		V		

	UNIBUS C	201	INECTOR'E	<u>3'</u>
SHT	l	В	2	SHT
14	BG6-H	Α		
14	BG5-H	В	GND	
14	BR5-L	C	GND	
	GND	D	BR4-L	14
	GND	E	BG4-H	14
15	AC-LO-L	F	DC-LO-L	15
12	AQI-L	Н	A00-L	12
12	A03-L	J	1-20A	12
_12_	A05-L	K	A04-L	12
12	A07-L	L	A06-L	12
12	A09-L	M	A08-L	12
12	AII-L	N	AIO-L	12
8,12	AI3-L	P	A12-L	8,12
8,12	A15-L	R	A14-L	8,12
8,12	A17-L	S	A16-L	8,12
		II	CI-L	7,6
13	SSYN-L	U	CO-L	7
13	MSYN-L	V	GND	

SHT		Α	2	SHT
7	INIT-L	Α	+57	
15	INTR-L	В	GND	
	D00-L	C	GND	
	D02-L	D	DOI-L	. 11
	DO4-L	E	DO3-L	. 11
	D06-L	F	DO5-L	- 11
	D08-L	H	DO7-L	11
	D10-L	J	D09-L	11
	D12-L	K	DII-L	11
11	D14-L	L	DI 3-L	11
8	A18-L	M	DI5-L	11
	GND	7	A19-L	8
	GND	P	BB5Y-L	16
	GND	R	SACK-L	16
	GND	S	NPR-L	13
	GND	T	BR7-L	14
13	NPG-H	U	BR6-L	14
14	BG7-H	V	GND .	

UNIBUS CONNECTOR'A'

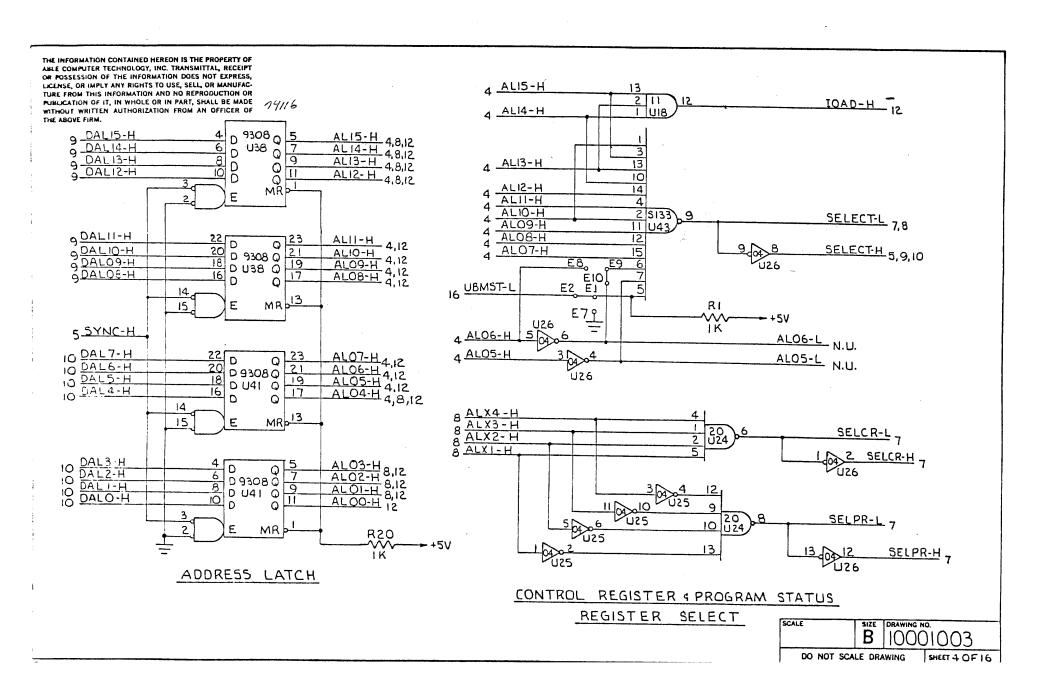
	LSI	CON	1/1/	ECTOR
SHT	1		В	2 +5V
			Α	+5V
			В	
			C	GND
			D	
			E	BDAL 3
			F	BDAL:
			H	BDAL S BDAL S
	GND	)	J	BDALS
			K	BDAL
			L	DUAL
	GND		М	BDAL 8
			N	BDALS
			P	BDAL II
			R	BOALI
			S	BDALL
	GND		T	BDALI
			U	BDALI
			V	BDALIS

SHT	1	Α	2	SHT
		Α	+5V	
		В		
		C	GND	
		D		
		E	BDOUT-L	5
		F		
		H	BDIN-L	5
	GND	J	BSYNC-L	5 5 5
		K	BWTBT-L	5
		L		
	GND	M	BIAKI-L	15
		N	BIAKO-L	15
		P		
		R		
		S		
	GND	T	BINIT-L	5
		U	BDALQ-L	10
		V	BDALI-L	10

LSI CONNECTOR A

UNIBUS CONNECTORS 'A' AND 'B' HAVE THE TERM 'BUS'

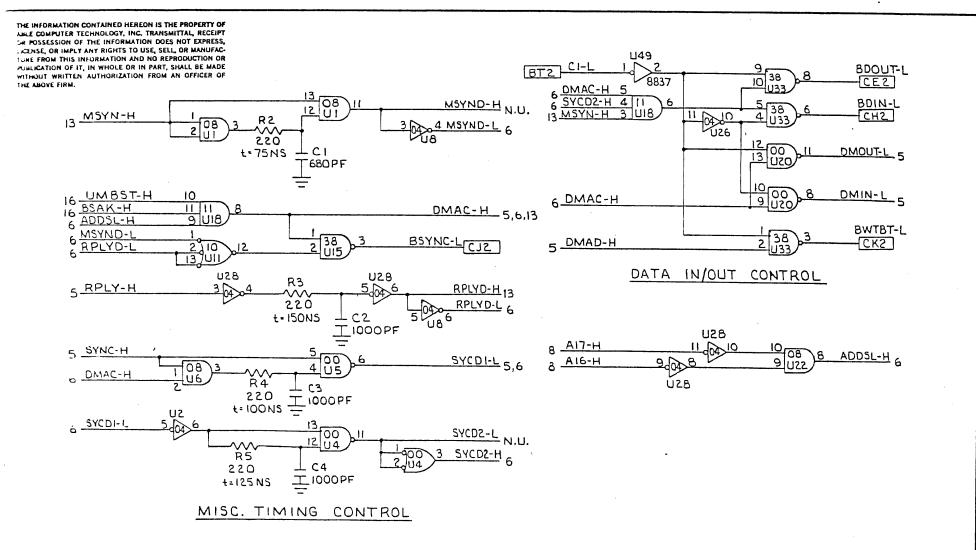
SCALE	B	10001003
-------	---	----------



THE INFORMATION CONTAINED HEREON IS THE PROPERTY OF ABLE COMPUTER TECHNOLOGY, INC. TRANSMITTAL, RECEIPT OR POSSESSION OF THE INFORMATION DOES NOT EXPRESS, LICENSE, OR IMPLY ANY RIGHTS TO USE, SELL, OR MANUFAC-TURE FROM THIS INFORMATION AND NO REPRODUCTION OR PUBLICATION OF IT, IN WHOLE OR IN PART, SHALL BE MADE BUS-CO-L WITHOUT WRITTEN AUTHORIZATION FROM AN OFFICER OF BU-2 BWTBT-LCK-2 THE ABOVE FIRM. 5 DOUT-H WRITE-L & - AM26S10 4 SELECT-H 6 DMAC-H WRITE-H 7 U58 6 RESET-H 7 5 ENDA-L U54 RESET- L 7,13,15,16 DAEN-L 9,10 DMAD-I 6 DMOUT-U58 AJZ BSYNC-L -5.6,7,13,14 6 SYCDI-L 8837 DMAD-H 6,9,10 6 DMAC-H U58 DOUT-H 5,7 AEZ BOOUT-L DMAD-L 5 DOUT-L 7-WRTE-H U58 16 UBMST-1 N.U. AHZ BDIN-DIN-H U54 1000 6 DBEN-L II 5,13,14 U58 6 DMIN-L WTBT-H 7 5 DIN-L LSI RECEIVERS 13 DENB-H 74 5 SYNC-H 85U UI9 13 SSYN-H  $\bar{Q}$ 10 11 9 U34 ENDA-L 5 15 SINTR-5 SYNC-H AM26510 15 SINTR-L REPLY CONTROL RPLY-L 16 B 10001003 SCALE

DO NOT SCALE DRAWING

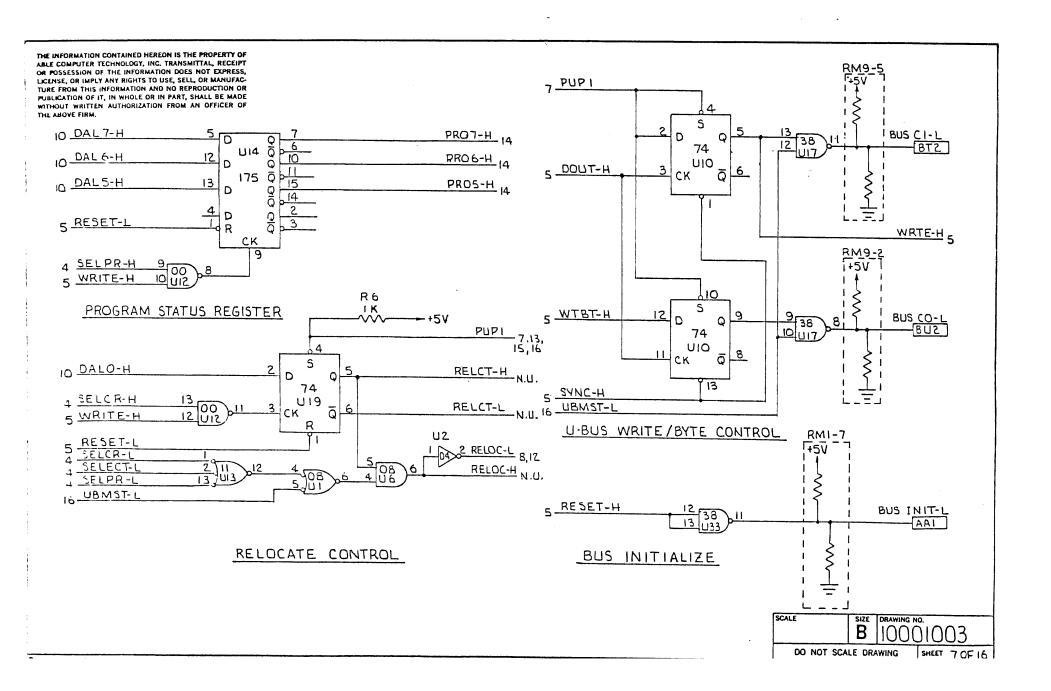
SHEET 5 OF IS



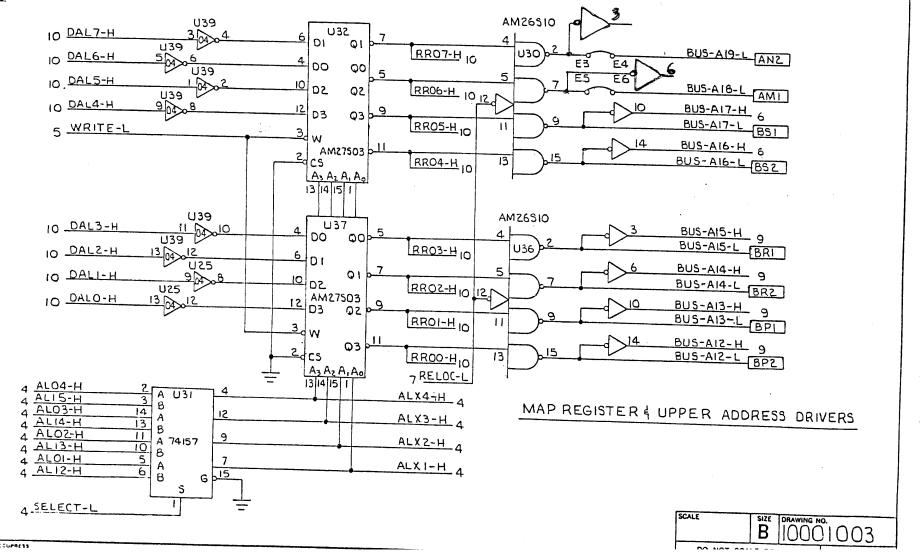
SCALE SIZE DRAWING NO.

B 10001003

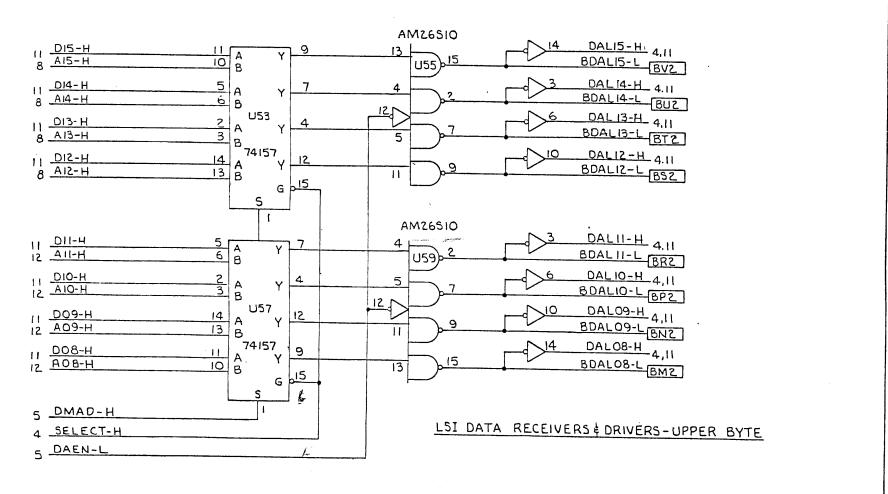
DO NOT SCALE DRAWING SHEET 6 GF 16



THE INFORMATION CONTAINED HEREON IS THE PROPERTY OF ABLE COMPUTER TECHNOLOGY, INC. TRANSMITTAL, RECEIPT OR POSSESSION OF THE INFORMATION DOES NOT EXPRESS, LICENSE, OR IMPLY ANY RIGHTS TO USE, SELL, OR MANUFACTURE FROM THIS INFORMATION AND NO REPRODUCTION OR PUBLICATION OF IT, IN WHOLE OR IN PART, SHALL BE MADE WITHOUT WRITTEN AUTHORIZATION FROM AN OFFICER OF THE ABOVE FIRM.



THE INFORMATION CONTAINED HEREON IS THE PROPERTY OF ABLE COMPUTER TECHNOLOGY, INC. TRANSMITTAL, RECEIPT OR POSSESSION OF THE INFORMATION DOES NOT EXPRESS, LICENSE, OR IMPLY ANY RIGHTS TO USE, SELL, OR MANUFAC-TURE FROM THIS INFORMATION AND NO REPRODUCTION OR PUBLICATION OF IT, IN WHOLE OR IN PART, SHALL BE MADE WITHOUT WRITTEN AUTHORIZATION FROM AN OFFICER OF THE ABOVE FIRM.

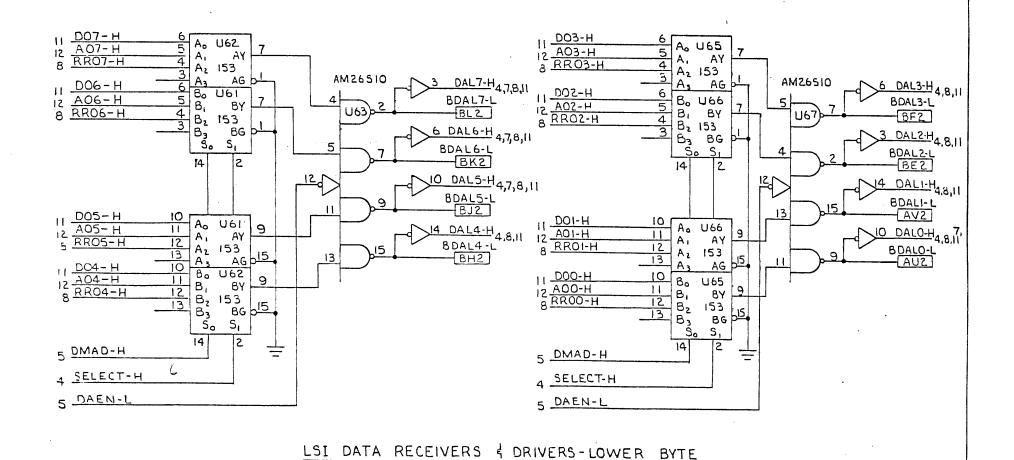


SCALE SIZE DRAWING NO. B

DO NOT SCALE DRAWING

SHEET O OF IS

THE INFORMATION CONTAINED HEREON IS THE PROPERTY OF ABLE COMPUTER TECHNOLOGY, INC. TRANSMITTAL, RECEIPT ON POSSESSION OF THE INFORMATION DOES NOT EXPRESS, LICENSE, OR IMPLY ANY RIGHTS TO USE, SELL, OR MANUFACTURE FROM THIS INFORMATION AND NO REPRODUCTION OR PUBLICATION OF IT, IN WHOLE OR IN PART, SHALL BE MADE WITHOUT WRITTEN AUTHORIZATION FROM AN OFFICER OF THE ABOVE FIRM.

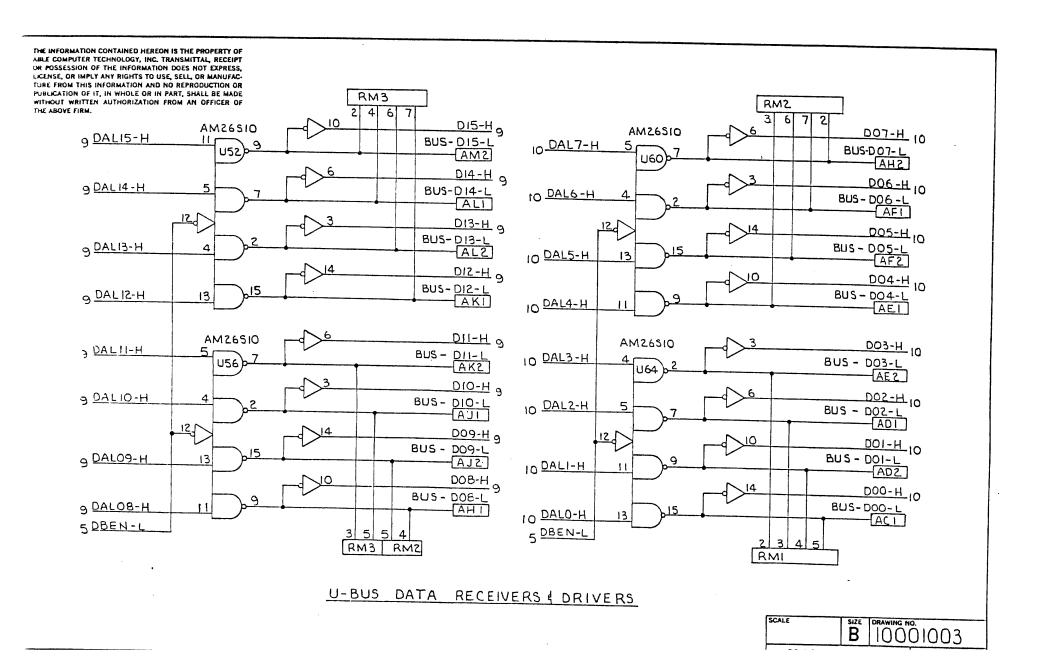


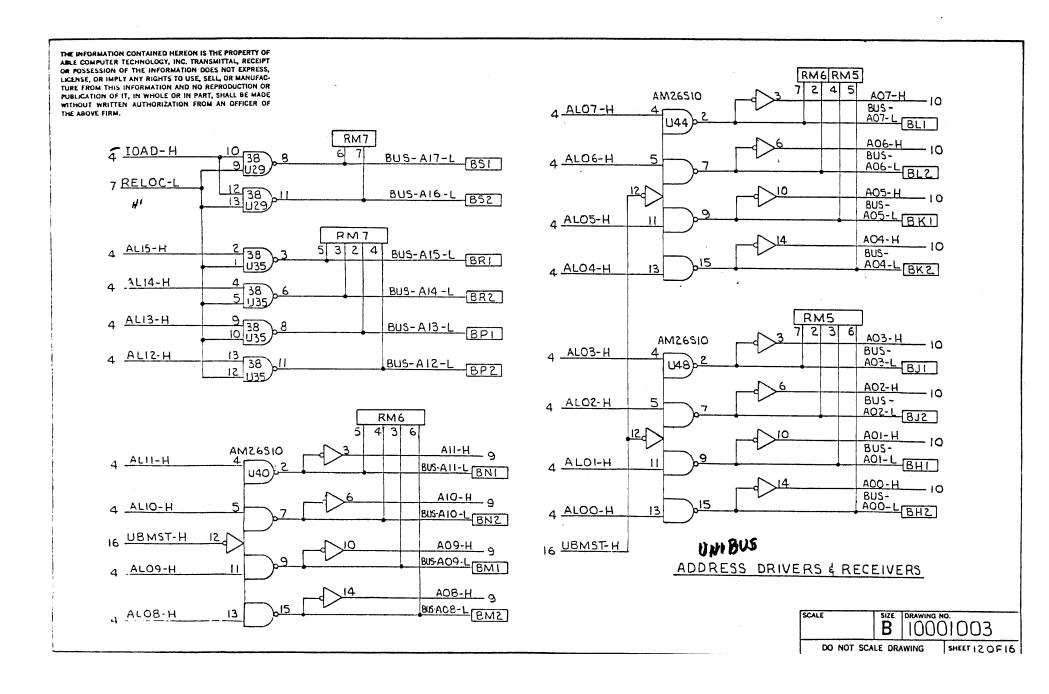
SCALE

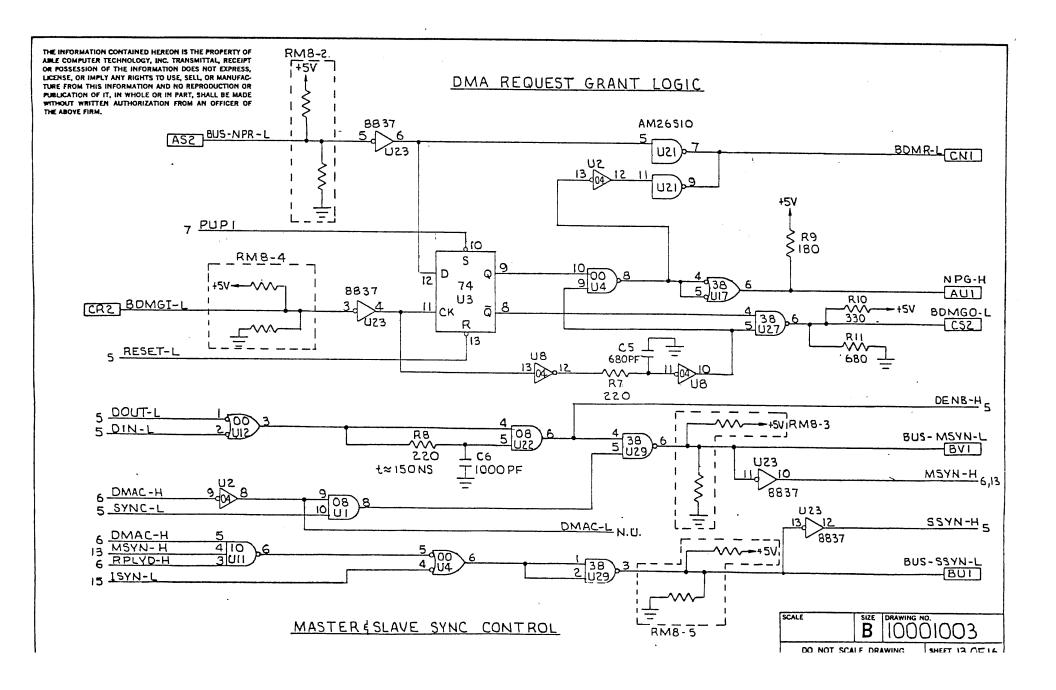
10001003

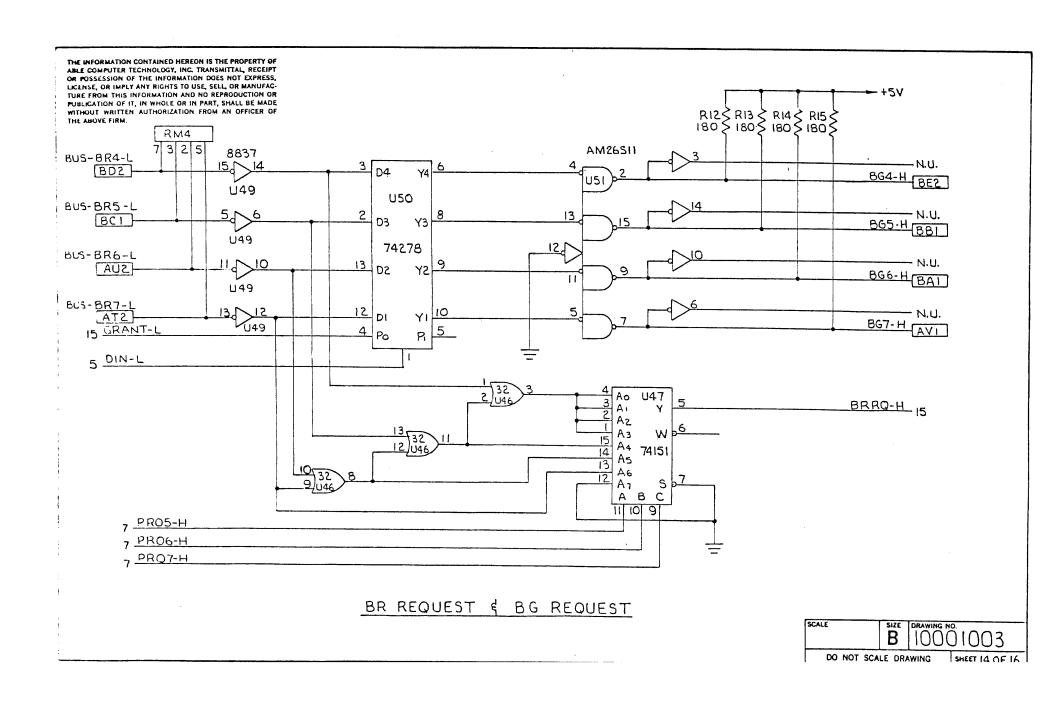
SHEET 10 OF 16

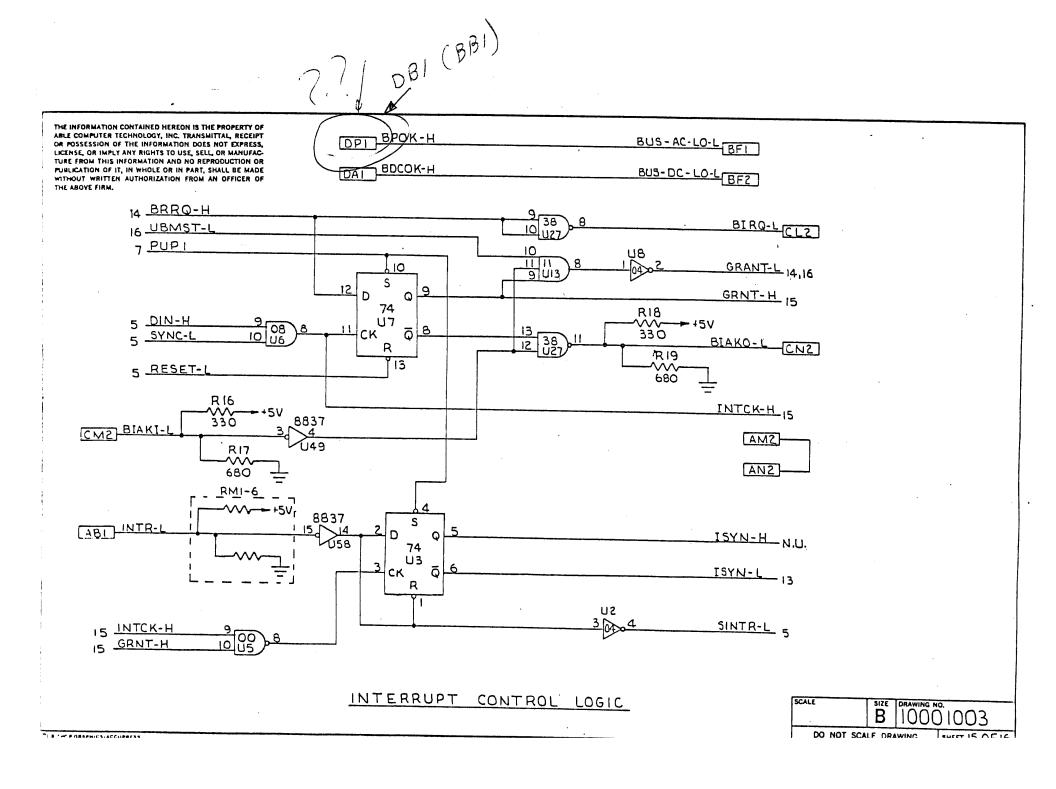
B 10











THE INFORMATION CONTAINED HEREON IS THE PROPERTY OF ABLE COMPUTER TECHNOLOGY, INC. TRANSMITTAL, RECEIPT OR POSSESSION OF THE INFORMATION DOES NOT EXPRESS, LICENSE, OR IMPLY ANY RIGHTS TO USE, SELL, OR MANUFACTURE FROM THIS INFORMATION AND NO REPRODUCTION OR PUBLICATION OF IT, IN WHOLE OR IN PART, SHALL BE MADE WITHOUT WRITTEN AUTHORIZATION FROM AN OFFICER OF THE ABOVE FIRM. SACK-H 16 8837 BUS-SACK-L AR2 BSAK-H 6 15 GRANT-L BSACK-L DNI 74 16 BBSY-H U16 BSAK-L N.U. 5 RESET-L 7 PUPI 10 UBMST-H 6,12 74 RM8-7 U16 BUS - BBSY-L 8837 , 13 5 RESET-L 16 SACK-H UBMST-L 4 5,7,15 BSACK & BBSY CONTROL LOGIC SCALE B 0001003

DO NOT SCALE DRAWING

SHEET 16 OF 16