

Play the blue-chip cards from ABLE.

Your UNIBUS system will perform better and last longer.

COMMUNICATIONS PRODUCTS

ABLE DH/DM™ (16-LINE COMBINATION DH11 & DM11 REPLACEMENT)

INSTALLS IN: UNIBUS systems...1 hex SPC slot. **DATA RATES:** 14 standard rates plus 19.2K baud and a user programmable rate. **PROCESSING ADVANTAGES:** Word transfer (in lieu of byte DMA) cuts bus time in half. **OPERATING MODES:** Full duplex with modem control. **IMPLEMENTATION ADVANTAGES:** On-board self-test/display. One bus load.

QUADRASYNC/B™ (4-LINE DL11 REPLACEMENT/EIA)

INSTALLS IN: All PDP-11's; 4-lines per SPC slot at one unit load to Unibus. **DATA RATES:** 7 independently selectable baud rates for each of 4 channels (150-9600). **ELECTRICAL:** EIA standard RS232C (Modem control not supported). **VECTOR/ADDRESS SELECTION:** Vector and address values to be set on boundaries of 008 or 408. 16 continuous word address for Vector or Address.

QUADRASYNC/C™ (4-LINE DL11 REPLACEMENT/CL)

INSTALLS IN: All PDP-11's; 4-lines per SPC slot at one unit load to Unibus. **DATA RATES:** 7 independently selectable baud rates for each of 4 channels (150-9600). **ELECTRICAL:** 20MA current loop (Send : Receive). **VECTOR/ADDRESS SELECTION:** Vector and address values to be set on boundaries of 008 or 408. 16 continuous word address for Vector or Address.

QUADRASYNC/E™ (4-LINE DL11-E REPLACEMENT)

INSTALLS IN: All PDP-11's; 4-lines per SPC slot at one unit load to Unibus. **DATA RATES:** 7 independently selectable baud rates for each of 4 channels (150-9600). **ELECTRICAL:** EIA standard RS232C — with modem control. **VECTOR/ADDRESS SELECTION:** 16 continuous word address for Vector or Address — starting values selected on any boundary.

QUADRACALL™ (4-LINE DN11 REPLACEMENT)

INSTALLS IN: All PDP-11's; 4-lines per SPC slot at one unit load to Unibus. **PERFORMANCE:** Interfaces up to 4 Bell 801 ACU's with Unibus enabling any PDP-11 to dial any DDD network number to establish data link. **INPUT/OUTPUT:** 5-input signals from ACU are handled by EIA RS232 receivers. 6-output signals are transmitted using EIA RS232 drivers. **VECTOR/ADDRESS SELECTION:** Allows selection of device address and vector by use of pencil switches.

ABLE DV/16 (16-LINE DV11 REPLACEMENT)

INSTALLS IN: All PDP-11's; in less than one half the space of DV11. **DATA RATES:** 16-line throughput of up to 30,000 char/sec (19.2K baud full duplex for each line) total. **PROCESSING ADVANTAGE:** Word transfers (in lieu of byte DMA) permit user to operate within one half the DV11 bandwidth for data transfers. **OPERATING ADVANTAGE:** User may mix sync and async lines in combinations of 4 or 8 lines with modem control and full system software compatibility with all DV11 performance features.

ABLE DZ/16 (16-LINE DZ11-E REPLACEMENT)

INSTALLS IN: All PDP-11's in any standard hex-width SPC slot; takes half the space at half the bus loading imposed by the DZ11-E. **DATA RATES:** All 15 standard DZ11 baud rates (50-9600). **IMPLEMENTATION ADVANTAGES:** On-board pencil switches allow address and vector selection flexibility without the need for jumpers. Data format is program-selectable for each channel.

MEMORY PRODUCTS

SCAT/45™ (ADD-IN FASTBUS MEMORY)

INSTALLS IN: PDP-11/45, -11/50 and -11/55. **EXPANDS IN:** 32K word increments/board. One-half of the available Fastbus space will accept full 124K word complement. **ADDRESSES ON:** Any 4096 word boundary across entire 124K word range. User has full memory complement at 330 nsec cycle-time memory instead of 32K word limitation imposed by the computer manufacturer.

CACHE/45™ (CACHE BUFFER MEMORY)

INSTALLS IN: PDP-11/45, -11/50 and -11/55. **CAPACITY:** 2048 byte (1K word). **ENHANCEMENT FACTOR:** Run time reductions to 50% (100% speed improvement) are achievable. **CACHE PARITY:** Automatically goes off-line in event of any data error. **RANGE SELECTION:** User may optimize hit ratio by upper/lower limit switch settings. **SPECIAL FEATURE:** Cache/45 can be enabled via software or console switches.

CACHE/434™ (4K WORD CACHE MEMORY)

INSTALLS IN: PDP-11/34 and -11/34A without using any additional backplane space! **CAPACITY:** 8192 byte (4K word). **ENHANCEMENT FACTOR:** Run time reductions to 40% (70% speed improvement) are achievable. **CACHE PARITY:** Automatically goes off-line in event of any data or address error. **RANGE SELECTION:** User may optimize hit ratio by upper/lower limit switch settings. Cache action monitor indicates hit rate.

CACHE/440™ (4K WORD CACHE MEMORY)

INSTALLS IN: PDP-11/35 and -11/40 without using any additional backplane space! **CAPACITY:** 8192 byte (4K word). **ENHANCEMENT FACTOR:** Run time reductions to 40% (70% speed improvement) are achievable. **CACHE PARITY:** Automatically goes off-line in event of any data or address error. **RANGE SELECTION:** User may optimize hit ratio by upper/lower limit switch settings. Cache action monitor indicates hit rate.

EMULOADER™ (ODT/BOOTSTRAP LOADER REPLACEMENT)

INSTALLS IN: PDP-11/05, -11/10, -11/35, -11/40, -11/45, -11/50 and -11/55. **MECHANICAL:** Dual width card replaces standard Unibus termination; requires no additional backplane space. **OPERATING ADVANTAGE:** Provides fixed console emulator (ODT) and bootstrap loaders for DL11, PC11, RF11, RK06, RK11, RP04/05/06, RP11, RS03/04, RX11, TC-11, TM11 and TU16. **SPECIAL FEATURE:** Performs memory diagnostic each time a boot operation is done from ODT.

GENERAL PURPOSE PRODUCTS

QNIVERTER™ (Q-BUS TO UNIBUS CONVERTER OR UNIBUS TO Q-BUS CONVERTER)

INSTALLS IN: LSI-11, LSI-11/23, PDP-11/03 and PDP-11/23 via quad-width card. **APPLICATIONS:** Allows Unibus-compatible controllers and memories to be used with LSI computer systems, or LSI-based peripherals to be used with PDP-11 computer systems. **FEATURES:** Supports features of LSI-11/23 including the full 128K address capability.

REBUS™ (BUS REPEATER — DB11 REPLACEMENT)

INSTALLS IN: All PDP-11's; without using any additional backplane space. **MECHANICAL:** One dual-width card plugs into the same pair of connectors as the Unibus extension cable which is then plugged into the REBUS connectors. **COMPATIBILITY:** Allows for 18 additional bus loads and 50 foot bus extension. Requires no software changes. Bus cycle time unaffected for devices on CPU side of REBUS — increased by 250 nsec max. for devices on outboard side.

DUAL I/O™ (GENERAL INTERFACE-DR11-C REPLACEMENT)

INSTALLS IN: All PDP-11's; in any SPC slot via quad-width card. **APPLICATION:** Dual I/O is equivalent to two (2) DR11-C's and provides the logic for program-controlled parallel transfer of 16-bit data between two (2) external user devices and a Unibus system. **OPERATING ADVANTAGE:** Provides user the hardware/software equal to a dual DR11-C in one-half the space and one-half the bus loading of DR11-C's.

INTERLINK/UNI (DR11-B AND 1/2 DA11-B REPLACEMENT)

INSTALLS IN: All PDP-11's in any SPC slot via hex-width card. **APPLICATIONS:** Provides full DR11-B (DMA INTERFACE) and one side of DA11-B (UNIBUS LINK) capability on a single card. **OPERATING ADVANTAGES:** Requires only one hex-width card in each computer to effect link vs. full four-slot system unit per computer. Exhibits one bus load. Directly software transparent as a DR11-B replacement or when expanded to DA11-B equivalency.

BUSLINK/UNI, LSI OR U TO Q (CPU TO CPU LINK; UNIBUS TO UNIBUS, UNIBUS TO Q-BUS OR Q-BUS TO Q-BUS)

INSTALLS IN: All PDP-11's and/or LSI-11's via pairs of hex-width, hex/quad-width, or quad-width cards and supplied cables. **APPLICATION:** Provides full DA11-B (Unibus or Q-bus link) compatibility on single cards. BUSLINK operates at DA11-B transfer rates over distances of up to 50 feet. **OPERATING ADVANTAGE:** Requires only one card per CPU to effect link at minimal bus loading vs. full system unit per computer.

ABLE cards give you the best way to make your present PDP-11 run better than ever and avoid up-grading to a more expensive model. We give you time to plan ahead and to control your cash flow with the most sophisticated line on the market today. Our cards are priced competitively. They install in minutes. They provide immediate results. And they always out-perform the competition. They should. We are the only computer people in the computer-system-enhancement business. Write for details.

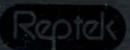


the computer experts

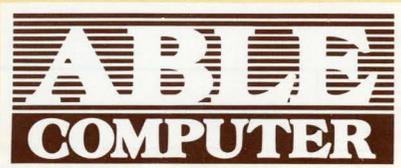
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(714) 979-7030. TWX 910-595-1729, ACT IRIN

ABLE COMPUTER-EUROPE, 74/76 Northbrook Street, Newbury
England RG9 1AE. (0635) 32125. TELEX 848507 HJULPHG.

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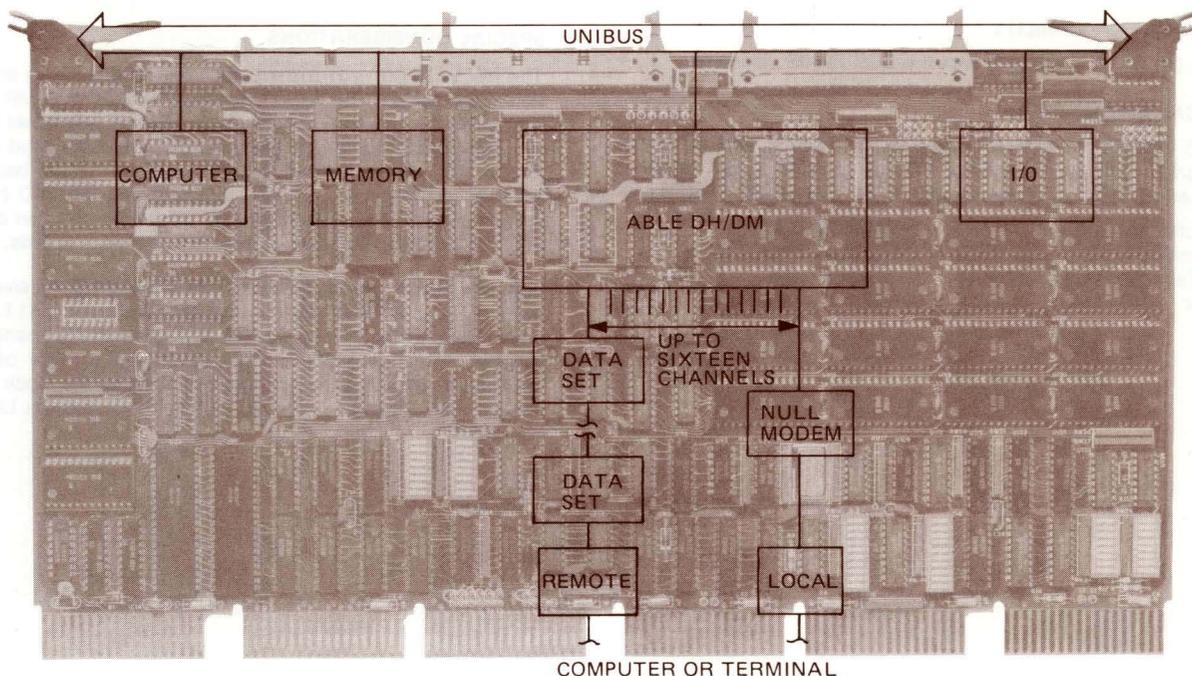
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San Jose, CA 95128
(408) 947-0622



#3750⁰⁰

ABLE DH/DM (DH11/DM11 Replacement)

The single board ABLE DH/DM is a sixteen-line DMA multiplexer with modem control for the Unibus* family.



FEATURES

- Software compatible with the DEC* DH11 and DM11-BB
- Requires only one hex SPC slot
- Presents one-third the bus loading at less than half the power
- Word rather than byte output transfers double data transfer rate capability or cut Unibus time in half
- Modem control standard on all lines — for use when needed
- On-board switches for address and vector selection add flexibility and eliminate jumpers
- Unwanted characters are not printed out in maintenance mode ... saves paper and runs quietly
- Diagnostic loopback connectors are built in — guess where the other kind are when you need them
- Comprehensive self-test diagnostic with LED display
- Larger silo size (four times standard depth) and improved input handling reduce system loading

GENERAL DESCRIPTION

The ABLE DH/DM is a microprogrammed controller with modem control. It connects any standard Unibus to 16 asynchronous communications lines and provides DMA output capabilities. It is software compatible with the DEC DH11 and DEC DM11-BB.

Physically, the ABLE DH/DM is comprised of a single hex-width board, a distribution panel, and interconnecting cables. ABLE DH/DM can be installed in any hex-width SPC slot of a standard DEC DD11 system unit.

PROGRAMMABLE LINE PARAMETERS

Character Length	5, 6, 7, or 8 bits
Number of Stop Bits	1 or 2 for 6-, 7-, or 8-bit characters 1 or 1.5 for 5-bit characters
Parity Generation/Detection	Odd, even, or none
Operating Mode	Full duplex
Xmtr/Rcvr Speed (Baud)	0, 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, plus 19.2K (Replaces External A), and External B.

ADDRESS SELECTION

Independent address selection for the DH and DM functions of the ABLE DH/DM are set via on-board pencil switches. Address range for the DH is 760000 through 763776 and requires eight consecutive word locations in the floating address space. Address range for the DM is 770400 through 770776 and requires four consecutive word locations in the DM11-BB fixed address space.

VECTOR SELECTION

Independent vector selection for the DH and DM functions are set via on-board pencil switches over the full vector range (000 - 774). The DH requires two consecutive interrupt vectors; XX0 for the receiver and XX4 for the transmitter. The DM requires one interrupt vector.

PRIORITY SELECTION

The ABLE DH/DM priority level is set to BR5 for the DH and BR4 for the DM. These may be user modified.

DIAGNOSTIC COMPATIBILITY

The ABLE DH/DM is compatible with the DEC ZDHM diagnostic.

ELECTRICAL INTERFACE

The ABLE DH/DM provides a voltage level interface and connector whose signal levels and connector pinning conform to EIA Standard RS232-C and CCITT Recommendations V.24. Leads supported are:

Protective Ground	Signal Ground
Transmitted Data	Received Data
Data Terminal Ready	Ring Indicator
Carrier	

ORDERING INFORMATION

Model (DEC #)	ABLE Order Number	Description
DH/DM (DH11-AD or DH11-AE)	10100-1	Hex-width board with EIA panel.

NOTE: Use DEC BC03M-XX series or equivalent cables for local connection of EIA/CCITT terminals. Use DEC BC05D-XX or equivalent for modem connection. Not supplied by ABLE.

SPECIFICATIONS

Bus Loading: The ABLE DH/DM presents only one unit load to the Unibus.

Power Requirements: 4.4 amps @ +5V
0.2 amps @ +15V
0.2 amps @ -15V

SPECIAL CONSIDERATIONS

The ABLE DH/DM provides substantial savings in space and cost due to its unique design. The design incorporates USART's with internal baud rate selection and an on-board clock. With the clock set to 200 baud, the ABLE DH/DM provides the user with the same baud rate selection as the DEC DH11 and additionally provides 19.2K baud without an external clock board. For users not requiring the 200 baud rate, the on-board clock offers the advantage of a wide selection of frequencies (150 to 9600 baud) without adding separate clock boards.

Special applications that require different speeds for receive and transmit (split baud rates) are handled differently from the DH11. The internal baud rate selector of each USART is used to set the speed of either the receiver or the transmitter in the usual manner. The other speed is obtained by selecting the appropriate speed for the clock and programming External B (1111) or 200 baud (0110) into the Line Parameter Register.

ABLE has created a veritable store of DEC computer enhancements. ABLE's unique products help you get more out of your Unibus system. Look at our current product listing . . . you will find solutions of genuine value.

SPECIAL MEMORY PRODUCTS

SCAT/45 (330 nsec Fastbus Memory)
CACHE/434 (8KB Unibus Cache)
UNIMAP (4MB PDP-11/23 Upgrade)

GENERAL PURPOSE PRODUCTS

QNVERTER (Dual-Purpose Converter)
REBUS (DB11-A Replacement)
DUAL I/O (Dual DR11-C)
INTERLINK (DR11-B Replacement)
BUSLINK (DA11-B — Unibus/Q Bus)

COMMUNICATIONS PRODUCTS

QUADRASYNC/B,C (4-line DL11-B, DL11-C)
QUADRASYNC/E (4-line DL11-E)
QUADRACALL (4-line DN11)
ABLE DV/16 (DV11 Replacement)
ABLE DZ/16 (DZ11-E Replacement)
ABLE DH/DM (DH11 and DM11 Replacement)
ABLE VxDZ (VAX Controller)
ABLE Q/DH (QBus DH/DM)

SYSTEMS PRODUCTS

ENABLE/34 (RSTS/E System Expander, Add-In)
MEGABOX (RSTS/E System Expander, Add-On)
44 MAGNUM (Economic PDP-11/44 Alternative)

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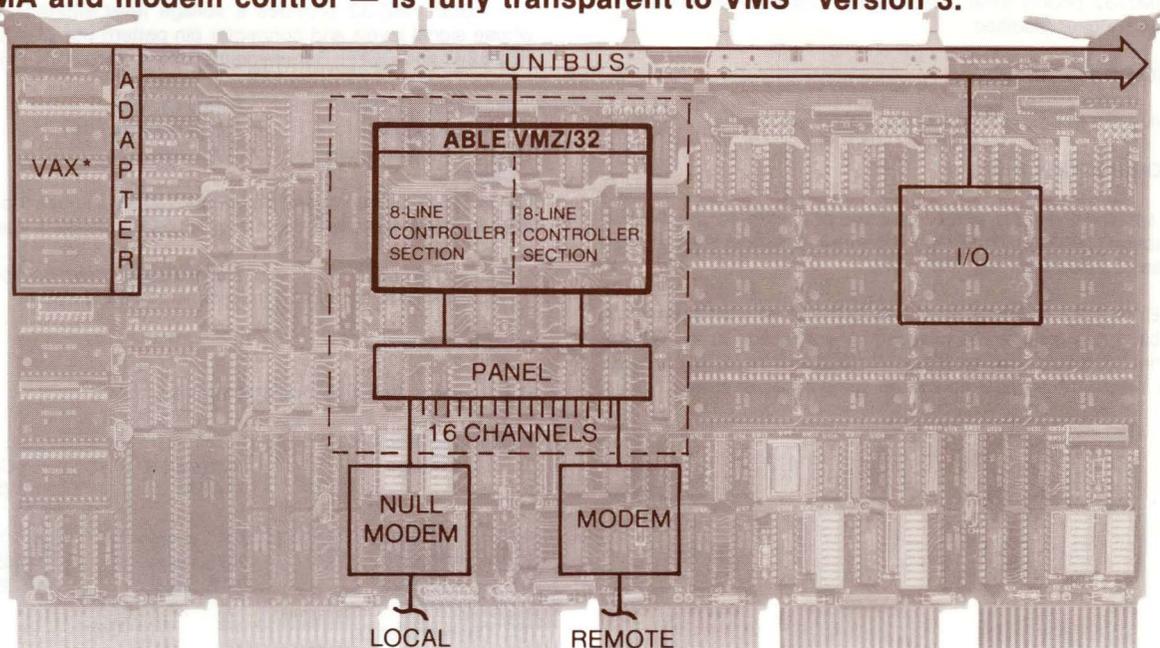
1732 Reynolds Avenue
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\$4250⁰⁰

ABLE VMZ/32™ (Equivalent to 16 DMF/32 Asynchronous Lines)

The ABLE VMZ/32 — a single-board microcontroller for 16 asynchronous lines with *programmable DMA* and modem control — is fully transparent to VMS* version 3.



FEATURES

- ABLE VMZ/32 will:
 - + Outperform existing DZ and DH products,
 - + Operate on standard VMS version 3 driver, and
 - + Allow user-elected product migration without board replacement.
- Substantial performance improvement in all VAX computer systems is gained by:
 - + An integral buffered output silo (like the ABLE VX/DZ) with improved performance under VMS *without* software modification . . . *no* third party software,
 - + The ability to select DMA mode for long output transfers . . . improved throughput,
 - + An "output throttle" which allows an external device to control and optimize its own data rate . . . a software transparent "natural" enabling small printers, graphics terminals, etc. to eliminate X-ON/X-OFF overhead, and
 - + Modem control which is interrupt driven . . . eliminates software overhead for program scan required by DZ's.
- The ABLE VMZ/32 has modem control and split baud capabilities on all lines.
- ABLE's standard on-board diagnostic performs comprehensive self-test with LED display.

GENERAL DESCRIPTION

The ABLE VMZ/32 is a microcontroller. Each can connect a VAX system to 16 asynchronous communication lines. The ABLE VMZ/32 provides a tailored design to optimize VAX system performance. It emulates the asynchronous line functions of two DMF/32's with an efficiency rivaling or exceeding DH performance. DZ-class modem control is provided on all lines for user-implementation as needed.

Physically, the ABLE VMZ/32 consists of a single hex-width board, distribution panel, and interconnecting cables. It installs into any hex-width SPC slot of a standard DEC DD11 backplane or equivalent in half the space and half the bus loading of either the DEC DZ11-E or two DMF/32's. The ABLE VMZ/32 is compatible with the standard DEC VMS driver under version 3.

An optional 16-line EIA/CL line adapter provides user selection of EIA or current loop operation on a line-by-line basis.

PROGRAMMABLE LINE PARAMETERS

Character Length:	5, 6, 7, or 8 bits
Number of Stop Bits:	1 or 2
Parity Generation/Detection:	Odd, even, or no parity
Operating Mode:	Full duplex
Transmitter/Receiver Speed:	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19.2K

Breaks may be generated and detected on each line.

ADDRESSABLE REGISTERS

The ABLE VMZ/32 has sixteen addressable registers for each eight-line group. Software uses five registers for asynchronous operations. The remaining eleven registers are associated with other DMF/32 functions and exist for DMF/32 compatibility only.

ADDRESS SELECTION

Address selection is via on-board pencil switches. Addresses are in the range 760000 through 763776. The ABLE VMZ/32 requires 32 contiguous word addresses beginning on an even boundary (76XX00).

VECTOR SELECTION

The vector is software programmable.

PRIORITY SELECTION

The ABLE VMZ/32 priority level is factory set to a BG5 level interrupt. This level may be user modified.

DIAGNOSTIC COMPATIBILITY

The ABLE VMZ/32 is compatible with the UETP exercisers.

SPECIAL CONSIDERATIONS

- Address selection on the ABLE VMZ/32 is limited to the floating address space (76XX00-763776), and addresses must start on even boundaries of 100 octal. (eg. 760400).
- The ABLE VMZ/32 has split baud capability on all sixteen lines. A separate baud rate generator is provided for connection to any receive channel that has been selected to operate with split baud. All channels operating in split mode must select the same receiver speed.

ORDERING INFORMATION

Model	ABLE Order Number	Description
ABLE VMZ/32 (With EIA)	10185-0	Hex-width board, EIA distribution panel, and interconnecting cables.
ABLE VMZ/32 (With EIA/CL)	10185-1	Hex-width board, dual purpose (EIA and/or 20ma current loop) line adapter/panel and interconnecting cables.

ELECTRICAL INTERFACE

The ABLE VMZ/32 provides a voltage level interface and connector whose signal levels and connector pin pattern conform to EIA Standard RS232-C and CCITT Recommendations V.24. Leads supported are:

Protective Ground	Signal Ground
Transmitted Data	Received Data
Data Terminal Ready	Ring Indicator
Carrier	

Current loop (20ma) operation (model 10185-1) uses the following pins. Each is opto-isolated and can be configured for active or passive operation.

Transmitted Data	Transmitter Current Source
Received Data	Receiver Current Source

SPECIFICATIONS

Bus Loading: Presents one unit load

Power Requirements:

Voltage	Current (EIA)	Current (20ma)
+5 volts	6.9 amps	7.7 amps
+15 volts	0.35 amps	0.35 amps
-15 volts	0.15 amps	0.80 amps

Silo Characteristics:

Input Silo	Two silos, one for each 8 lines, 48 characters per silo.
Output Silo	Sixteen silos, one for each line, 32 characters per silo.

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SYSTEMS PRODUCTS

ENABLE/34 (RSTE/E System Expander, Add-in)
 MEGABOX (RSTS/E System Expander, Add-On)
 44 MGNUM (Economic PDP-11/44 Alternative)
 MAGNUM+ (1 MB PDP-11/44 Alternative, with imbedded 80 MB Disk)

SPECIAL MEMORY PRODUCTS

SCAT/45 (330 nsec Fastbus Memory)
 CACHE/434 (8KB Unibus Cache)
 UNIMAP (4MB PDP-11/23 Upgrade)

GENERAL PURPOSE PRODUCTS

QNIVERTER (Dual-Purpose Converter)
 REBUS (DB11-A Replacement)
 DUAL I/O (Dual DR11-C)
 INTERLINK (DR11-B Replacement)
 BUSLINK (DA11-B—Unibus/Q Bus)

COMMUNICATIONS PRODUCTS

QUADRASYNC/B.C (4-line DL11-B, DL11-C)
 QUADRASYNC/E (4-line DL11-E)
 QUADRACALL (4-line DN11)
 ABLE DV/16 (DV11 Replacement)
 ABLE DZ/16 (DZ11-E Replacement)
 ABLE DH/DM (DH11 and DM11 Replacement)
 ABLE VX/DZ (VAX Controller)
 ABLE Q/DH (QBus DH/DM)
 ABLE VMZ/32 (16 asynchronous line DMF/32 equivalent)

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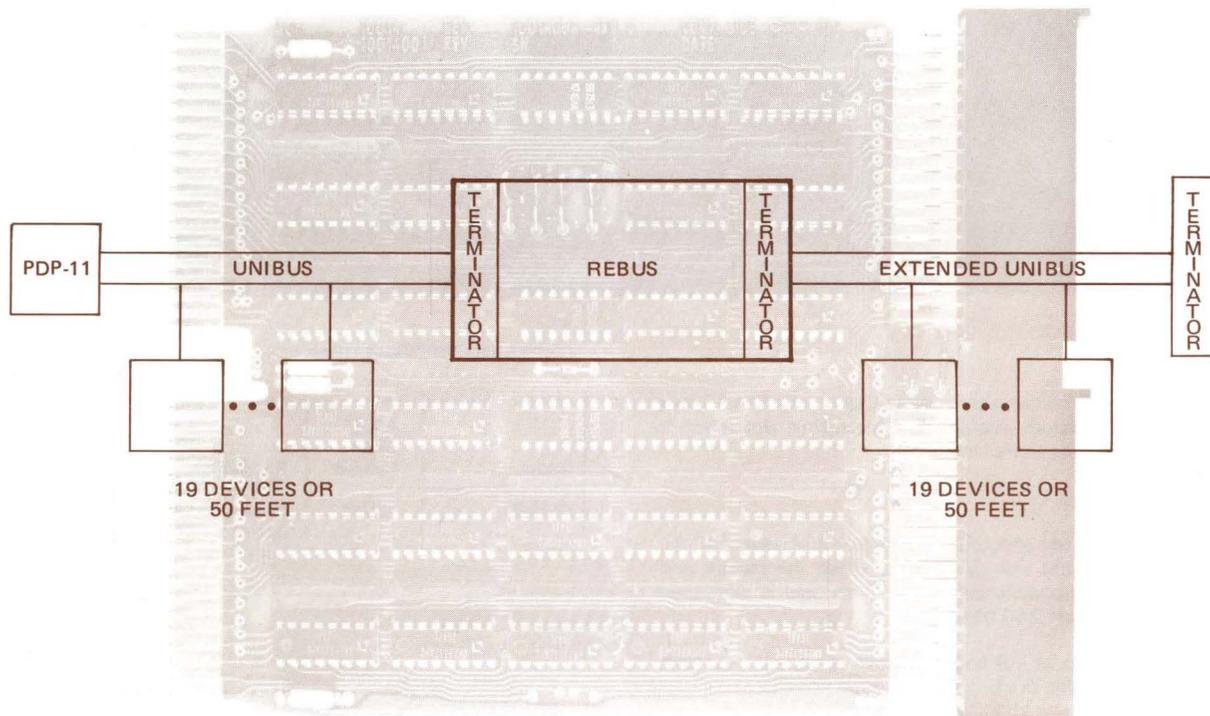


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REBUS™ (DB11-A Replacement)

REBUS is a Unibus* repeater for the PDP-11* that takes no extra space in your computer.



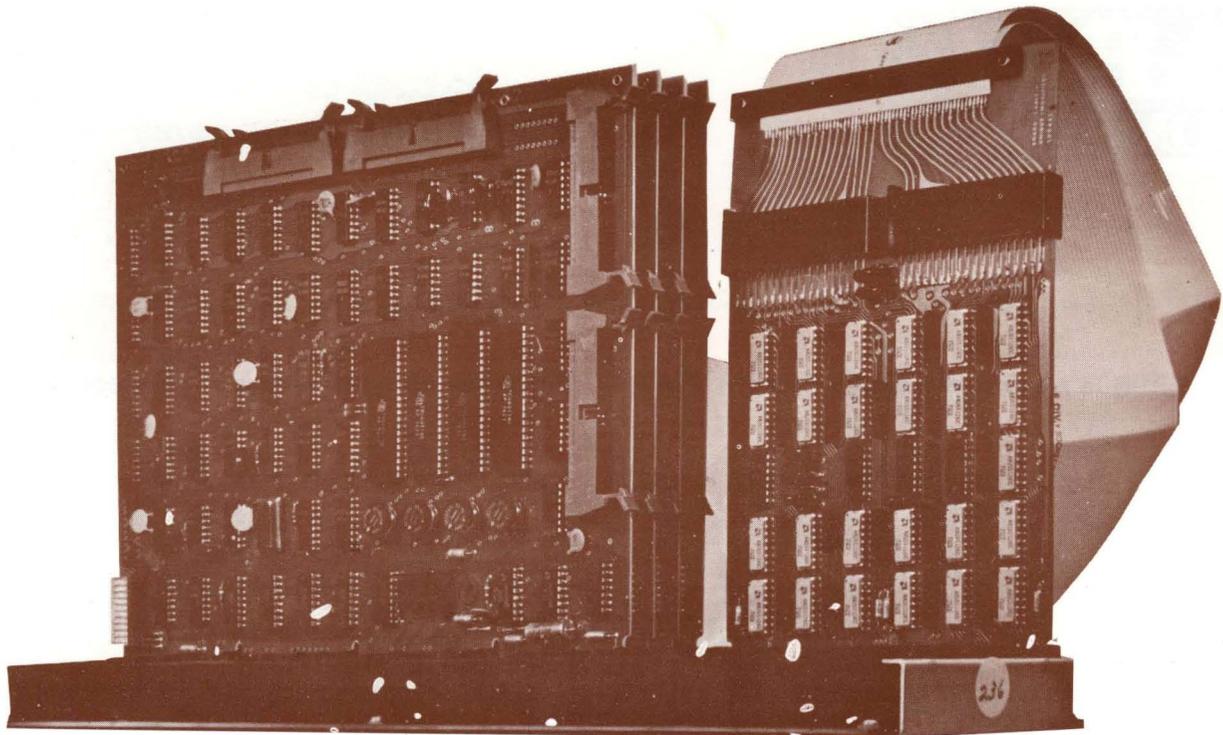
FEATURES

- REBUS doubles the Unibus load capacity by providing a physical and electrical extension of the Unibus
- REBUS is easy to implement — it installs in the last backplane slot normally occupied by a Unibus cable or interconnect module
- REBUS saves space by eliminating the need for an additional dedicated 4-slot mounting module
- Cycle time across REBUS is less than that of the DEC* DB11-A
- Software compatible — no software changes are required to use the REBUS.

GENERAL DESCRIPTION

REBUS allows physical and electrical extension of the Unibus. It will drive 19 extra bus loads and permits a 50-foot extension in bus length. Bus cycle time is unaffected for devices on the same side of the REBUS and increased by a maximum of 250 nsec. for devices communicating through the REBUS.

The REBUS is a dual-width board installed in the pair of connectors normally used for the Unibus cable or interconnect module. The extended Unibus is made available via on-board Unibus connectors permitting easy connection to a Unibus cable.



INSTALLATION

Installation of the REBUS is shown above. Note that no additional space is required. The REBUS installs into the last backplane slot which is normally occupied by an interconnect module.

SPECIFICATIONS

Bus Timing: Cycle time is not affected if the master and slave devices are on the same side of REBUS. When the master and slave are on opposite sides, the cycle time is increased by no more than 250 nsec.

Power Required: 4.5 amps at +5 volts (includes termination for both sides of the bus)

Unibus Loading: 1 bus load each side

Unibus Drive Capability: 19 additional loads and up to 50 feet of cable

ORDERING INFORMATION

Model	ABLE Order Number	Description
REBUS	10014	Dual-width module; Unibus cable not included.

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SPECIAL MEMORY PRODUCTS

SCAT/45 (330 nsec Fastbus Memory)
 CACHE/45 (2KB Fastbus Cache)
 CACHE/434 (8KB Unibus Cache)
 CACHE/440 (8KB Unibus Cache)
 EMULoader (ODT/Boot Loader)

GENERAL PURPOSE PRODUCTS

QNIVERTER (Dual-Purpose Converter)
 UNIVERTER (Converter with Map)
 REBUS (DB11-A Replacement)
 DUAL I/O (Dual DR11-C)
 INTERLINK (DR11-B Replacement)
 BUSLINK (DA11-B--Unibus/Q Bus)

COMMUNICATIONS PRODUCTS

QUADRASYNC (4-line DL11)
 QUADRASYNC/E (4-line DL11-E)
 QUADRACALL (4-line DN11)
 DMAX/16 (DH11 Replacement)
 DV/16 (DV11 Replacement)
 DZ/16 (DZ11-E Replacement)

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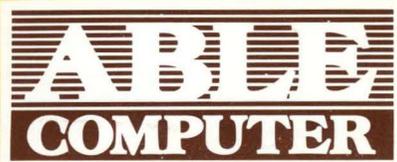


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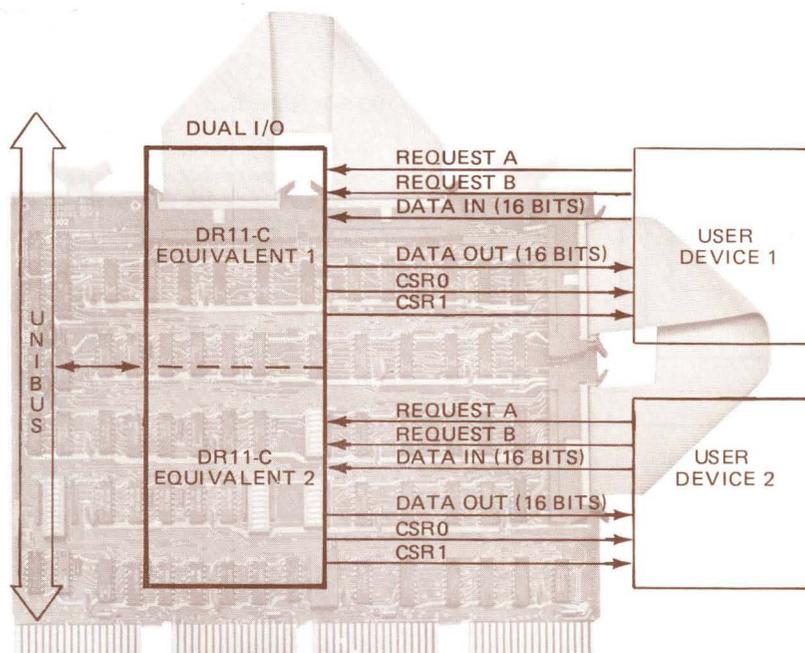


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DUAL I/O™ (Dual DR11-C Replacement)

The Dual I/O is a space-saving general purpose interface between one or two user selected peripherals and the PDP-11* Unibus*.



FEATURES

- Saves space and power — the DUAL I/O provides all of the features of two DEC* DR11-C units on one quad module
- Unburdens the Unibus — presents half the bus loading of two DR11-C interfaces
- On-board switches for address and vector selection add flexibility without the need for jumpers
- The use of hysteresis receivers between the DUAL I/O and an external device improves noise immunity
- The DUAL I/O is fully compatible with your PDP-11 operating system software and diagnostics
- DUAL I/O's can be used as interprocessor programmed links to allow multiple processors to transfer data from one to the other.

GENERAL DESCRIPTION

The DUAL I/O is a general purpose interface between the PDP-11 Unibus and two user peripherals. The interface provides the necessary logic for program-controlled parallel transfer of 16-bit data between two external user devices and the Unibus. The DUAL I/O is software and connector compatible with two DR11-C interfaces.

The DUAL I/O can also be used as part of an interprocessor programmed link allowing multiple processors to transfer data from one to the other. Two DUAL I/O modules can be cross connected to allow two-way data transfer between two Unibus systems. Three DUAL I/O modules can be interconnected to provide three-way data transfer. See the diagram on the reverse side.

The DUAL I/O is contained on a single quad module that can be plugged into any SPC slot. The interface has four 40-pin Berg connectors (two for each user device) for all user input and output signals. Each set of connectors is pin compatible with the DR11-C connectors.

ADDRESS SELECTION

The DUAL I/O contains two independent address selection circuits for independent addressing of each section of the DUAL I/O. The address range is from 760000 through 777776 and is selected via pencil switches.

VECTOR SELECTION

The DUAL I/O contains two independent vector selection circuits. The vector range is from 000 through 774 and is selected via pencil switches.

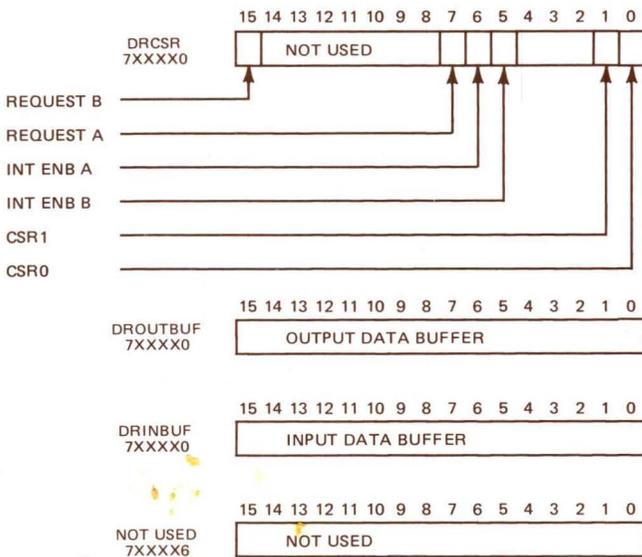
PRIORITY SELECTION

DUAL I/O priority selection is normally set for a BR5 level interrupt. The level can be easily changed.

DIAGNOSTIC COMPATIBILITY

ZDRC DR11-C Device Register Test

REGISTERS



ORDERING INFORMATION

Model	ABLE Order Number	Description
DUAL I/O	10039	Quad-width board with two maintenance cables.

SPECIFICATIONS

Bus Loading: The DUAL I/O presents only one unit load to the Unibus.

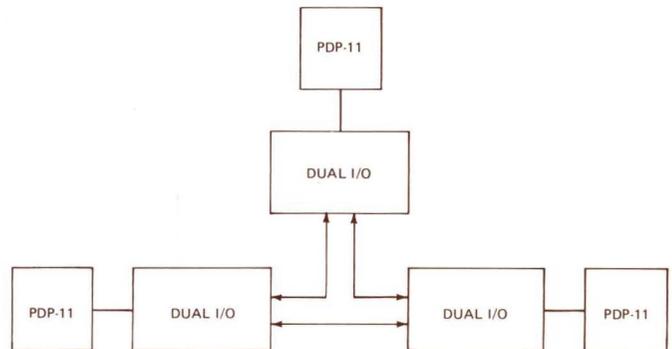
Power Required: 1.7 amps at +5 volts (± 15 volts not required)

Input: One standard TTL unit load with diode protection clamps to +5 volts and ground. Logic 1 = +3 volts; logic 0 = 0 volts.

Output: TTL levels capable of driving:
 Data - 8 unit loads (74175)
 Other - 30 unit loads (7437).

MAINTENANCE

Two 40-pin flat ribbon cables (supplied) can be used to connect input to output to allow host computer maintenance diagnostic check out. These cables should be left connected on unused ports of the DUAL I/O or spurious interrupts may occur.



DUAL I/O As Three-Processor Programmed Link

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SCAT/45 (330 nsec Fastbus Memory)
 CACHE/45 (2KB Fastbus Cache)
 CACHE/434 (8KB Unibus Cache)
 CACHE/440 (8KB Unibus Cache)
 EMULOADER (ODT/Boot Loader)

GENERAL PURPOSE PRODUCTS

QNVERTER (Dual-Purpose Converter)
 UNIVERTER (Converter with Map)
 REBUS (DB11-A Replacement)
 DUAL I/O (Dual DR11-C)
 INTERLINK (DR11-B Replacement)
 BUSLINK (DA11-B--Unibus/Q Bus)

COMMUNICATIONS PRODUCTS

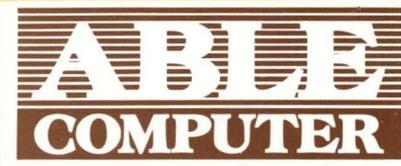
QUADRASYNC (4-line DL11)
 QUADRASYNC/E (4-line DL11-E)
 QUADRACALL (4-line DN11)
 DMAX/16 (DH11 Replacement)
 DV/16 (DV11 Replacement)
 DZ/16 (DZ11-E Replacement)

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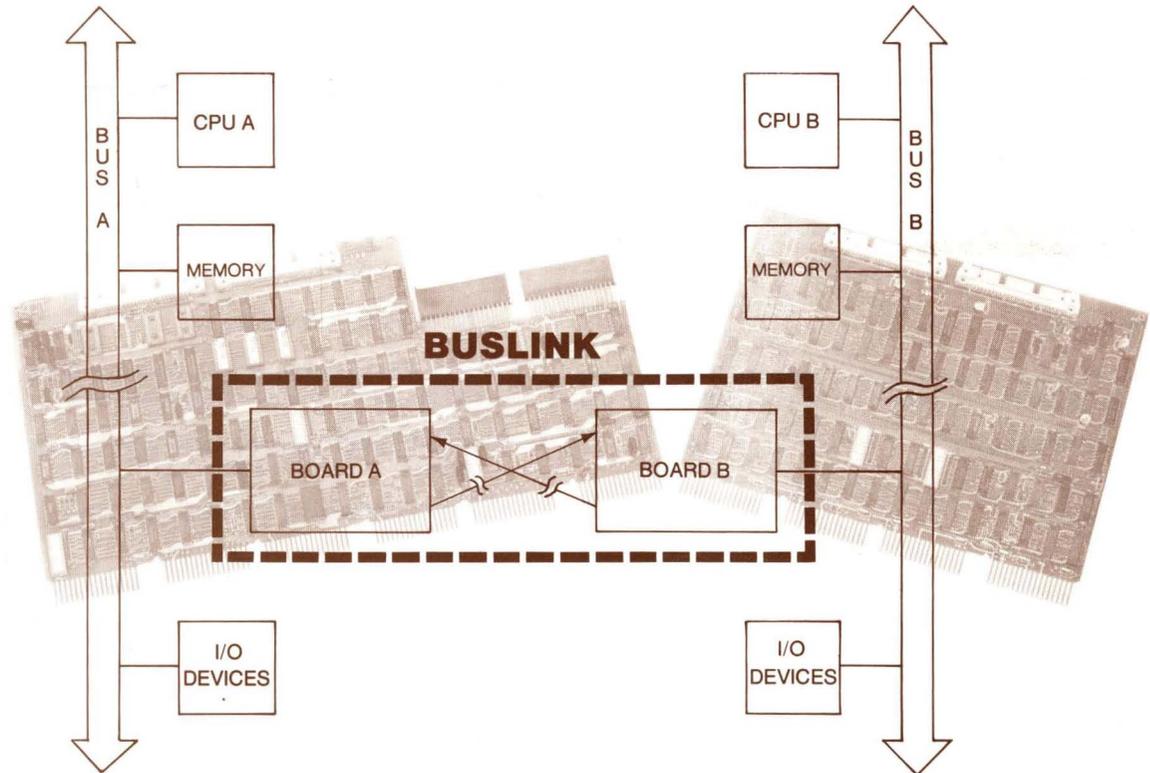
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BUSLINK™ (Interprocessor Link)

The BUSLINK is a high speed, parallel, half duplex, DMA channel between two DEC* computer systems.



FEATURES

- The BUSLINK is composed of two ABLE INTERLINK interface boards and interconnecting cables which allow complete computer link operation between two PDP-11* systems, two LSI-11* systems, or a PDP-11 and an LSI-11 system.
- Three basic BUSLINK models suit a variety of applications:
 - BUSLINK/UNI for the PDP-11 requires one fourth the space and one fourth the power of its DEC equivalent, the DA11-B.
 - BUSLINK/LSI for the LSI-11 offers DA11-B features for the LSI-11
 - BUSLINK/U-Q provides a PDP-11 to LSI-11 system link.
- On-board switches for address and vector selection add flexibility to each BUSLINK without requiring jumpers
- The use of hysteresis receivers offers improved noise immunity between systems.

GENERAL DESCRIPTION

BUSLINK allows computer link operation between two computer systems. Using the DMA facilities of the two computers, BUSLINK transfers 16-bit parallel data at rates up to 250 or 500 thousand words per second depending upon the computer systems linked.

BUSLINK/UNI provides a data transfer channel between any two PDP-11 Unibus* systems. It is software and diagnostic compatible with the DEC DA11-B. BUSLINK/UNI consists of two INTERLINK/UNI modified hex-width boards and interconnecting cables. Each INTERLINK board plugs into an SPC slot of one of the PDP-11 systems. No backplane modification is required for installation if the boards are installed into the first or last slot of an SPC backplane.

BUSLINK/LSI provides a data transfer channel between any two LSI-11 computer systems. It consists of two INTERLINK/LSI quad-width boards and interconnecting cables. The INTERLINK/LSI requires a quad-width backplane slot in each computer system for installation.

BUSLINK/U-Q provides a data transfer channel between any PDP-11 Unibus system and any LSI-11 system. It consists of an INTERLINK-UNI which installs in the PDP-11 system, an INTERLINK/LSI which installs in the LSI-11 system, and cables to connect the two systems.

* Trademark of Digital Equipment Corporation.

BUSLINK and INTERLINK are trademarks of ABLE COMPUTER TECHNOLOGY

ADDRESSABLE REGISTERS

Addressable registers on each INTERLINK are:

Register	Mnemonic	Operation	Bus Address
Word Count	DRWC	Read/Write	7XXXX0
Bus Address	DRBA	Read/Write	7XXXX2
Control and Status	DRST	Read/Write	7XXXX4
Data Buffer	DRDB	Read/Write	7XXXX6

ADDRESS/VECTOR SELECTION

Address selection for each INTERLINK is via on-board pencil switches. Addresses range from 760000 through 777776 and are normally set to 77241X.

Vector selection is also via pencil switches and has a range of 000 through 774. The vector is normally set to 140.

PRIORITY SELECTION

For use with a PDP-11, each INTERLINK/UNI is shipped with a BR5 level interrupt priority. The priority level can be easily changed.

INTERLINK/LSI is fixed to a level four interrupt.

SOFTWARE SUPPORT

All BUSLINK models are software supported by RSX-11M, RSX-11S, DECNET-M, DECNET-S, and a handler is available from DEC for RSX-11D.

DIAGNOSTIC COMPATIBILITY

ZDRB, DEC's NPR Interface Test, is compatible with BUSLINK. (See Special Considerations.)

SPECIFICATIONS

Power Requirements:

BUSLINK/UNI	2.0 amps @ +5 volts per system
BUSLINK/LSI	1.5 amps @ +5 volts per system
BUSLINK/U-Q	1.5 amps @ +5 volts, LSI-11 system 2.0 amps @ +5 volts, PDP-11 system (No other voltages are required)

Bus Loading: 1 unit load per system

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QUADRASYNC/E (4-line DL11-E)
QUADRACALL (4-line DN11)
DMAX/16 (DH11 Replacement)
DV/16 (DV11 Replacement)
DZ/16 (DZ11-E Replacement)

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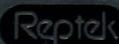
ORDERING INFORMATION

Model	ABLE Model Number	Description
BUSLINK/LSI	10062-0	Two quad-width boards, maintenance cable, and set of two 25-foot shielded interconnect cables.
	10062-1	As above with 50-foot cable set in lieu of 25-foot cable set.
BUSLINK/U-Q	10063-0	Quad-width LSI-11 board, modified hex-width Unibus board, maintenance cable, and set of two 25-foot shielded interconnect cables.
	10063-1	As above with 50-foot cable set in lieu of 25-foot cable set.
BUSLINK/UNI	10064-0	Two modified hex-width boards, maintenance cable, and set of two 25-foot shielded interconnect cables.
	10064-1	As above with 50-foot cable set in lieu of 25-foot cable set.

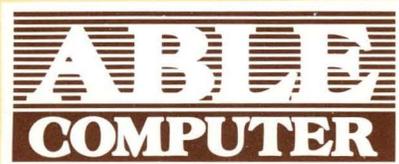
SPECIAL CONSIDERATIONS

- Some PDP-11 system software and diagnostics may not be compatible with the LSI-11 without software modification.
- The INTERLINK boards are available for DMA interface operation on a single PDP-11 or LSI-11 computer.
 - The INTERLINK/UNI is a single modified hex-width board that operates with any PDP-11.
 - The INTERLINK/LSI is a single quad-width board that operates with any LSI-11
- Both the INTERLINK/UNI and INTERLINK/LSI are system software compatible with the DEC DR11-B. They contain the DA11-B type logic on-board for ready conversion to use as BUSLINKS. For further information, contact ABLE.
- For use with INTERLINK/LSI, the quad-width LSI-11 backplane must provide Q Bus on the A and B connectors but may provide Q Bus on the C and D connectors as well.

Represented by:

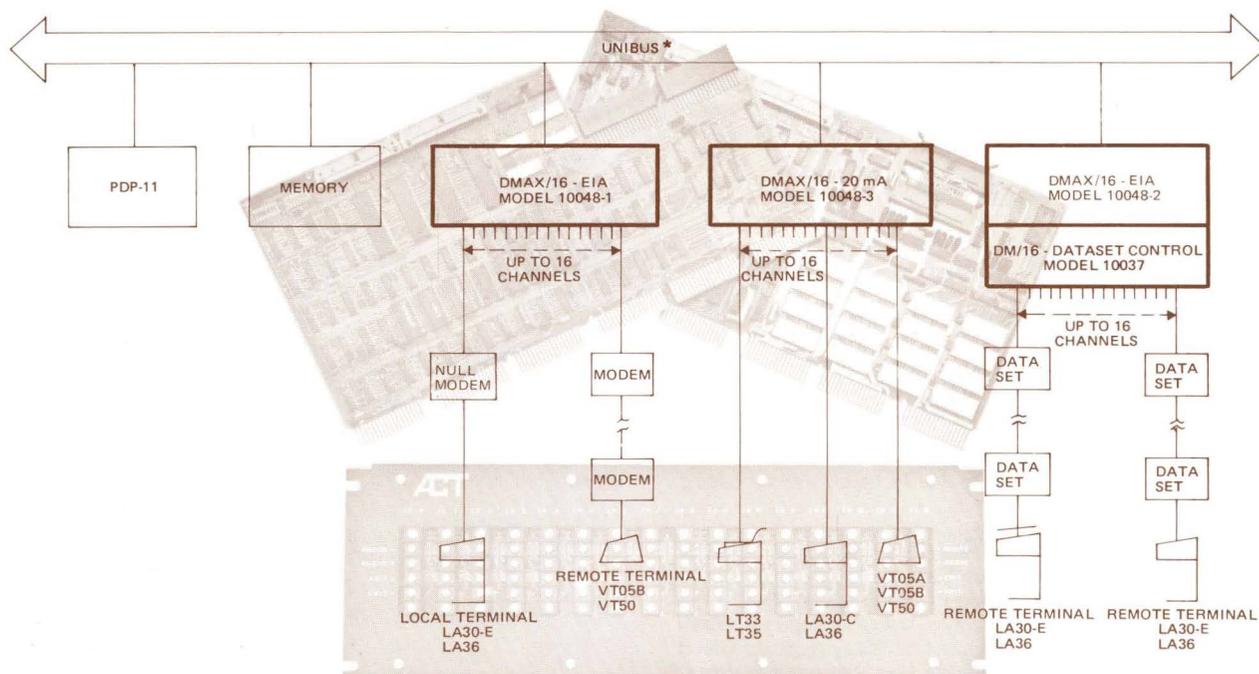


2444 Moorpark Ave
San Jose, CA 95128
(408) 947-0622



DMAX/16™ (DH11 Replacement)

The DMAX/16 is a fully buffered, programmable DMA multiplexer that doubles the data transfer rate capability of a PDP-11* based data communication system by using word rather than byte transfers.



FEATURES

- Like the DEC* DH11, DMAX/16 provides DMA output capabilities thus freeing the processor from interrupt handling
- DMAX/16 uses word rather than byte data transfers which doubles data transfer rate capability over the DH11 or cuts Unibus time in half
- Requires only two hex slots rather than a dedicated nine slot backplane
- A built-in external clock allows on-board baud rate selection — no clock cards required
- No output to terminals in loopback maintenance mode prevents unwanted data from being printed on the terminal
- Supports 19.2K baud rate
- The DMAX/16 can be easily installed in an SPC backplane — no backplane modification needed.

GENERAL DESCRIPTION

The DMAX/16 is a microprocessor based controller which connects a PDP-11 to 16 asynchronous communications lines and provides DMA (direct memory access) output capabilities. It is system software compatible with the DEC DH11.

Physically, the DMAX/16 is comprised of a modified hex-width control board, a hex-width data board, a distribution panel, and interconnecting cables. One model also includes a dataset (modem) control board. DMAX/16 can be installed in any standard DEC DD11 peripheral mounting panel.

PROGRAMMABLE LINE PARAMETERS

Character Length	5, 6, 7, or 8 bits
Number of Stop Bits	1 or 2 for 6-, 7-, or 8-bit characters 1 or 1.5 for 5-bit characters
Parity Generation/Detection	Odd, even, or none
Operating Mode	Half or full duplex
Transmitter/Receiver Speed (Baud)	0, 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, 19.2K (was Ext. A), External B

Breaks may be detected and generated on each line.

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10048X08-0281

We reserve the right to improve our products at any time.

DIAGNOSTIC COMPATIBILITY

The DMAX/16 is compatible with the following diagnostics provided by DEC.

- ZDHA DH11 Static Logic Test
- ZDHB DH11 Memory Test
- ZDHC DH11 Receiver and Transmitter Logic Test
- ZDHD DH11 Speed Selection Test*
- ZDHE DH11 Character Length & Basic Data Test
- ZDHF DH11 Single Line Data Test
- ZDHG DH11 Multi-line Data Test
- ZDHH DH11 Auto-Echo Test
- ZDHI DH11 Break and Half Duplex Test
- ZDHJ DH11 Echo Test
- ZDHK Modem Control Multiplexer Diagnostic
- ZDHN DH11 Data Reliability Test/Single Line Echo & Patterns/Cable Test
- ZDHM DH11 Diagnostic*

*Note: The external clock frequency must be set at 200 baud.

SPECIAL CONSIDERATIONS

The DMAX/16 provides substantial savings in space and cost due to its unique design. The design incorporates USART's with internal baud rate selection and an on-board external clock frequency. With the external clock set to 200 baud (factory setting) the DMAX/16 provides the user with the same baud rate selection as the DEC DH11 and additionally provides 19.2K baud without an external clock board. For users not requiring the 200 baud rate, the external clock frequency offers the advantage of a wide selection of frequencies (0 to 18.0K baud) without adding separate clock boards.

Special applications that require different speeds for receive and transmit (split baud rates) are handled differently from the DH11. The internal baud rate selector of each USART is used to set the speed of either the receiver or the transmitter in the usual manner. The other speed is obtained by adjusting the external clock frequency to the appropriate speed and programming External B (1111) into the Line Parameter Register. (Note that all channels which use External B share the same external clock frequency.) This method of split baud rate selection is suitable for most applications; check with the factory if in doubt about implementing split baud rates for your application.

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 DZ/16 (DZ11-E Replacement)

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ORDERING INFORMATION

Model (DEC #)	ABLE Order Number	Description
Basic Board Set (Not offered by DEC)	10048-0	Modified hex-width control board, hex-width data board, interconnecting cables, test cables. Two Berg connectors on the data board provide for connection to a distribution system.
EIA Version Without Dataset Control (DH11-AE)	10048-1	Basic Board Set plus EIA distribution panel and interconnecting cable. Does not include cables for local connection of EIA/CCITT terminals; use BC03M-XX series cables.
EIA Version With Dataset Control (DH11-AD)	10048-2	Basic Board Set plus EIA distribution panel and interconnecting cable. Includes hex-width dataset control board and interconnecting cable. Does not include dataset cable; use BC05D-25. Use BC03M-XX series cables for local connection of EIA/CCITT terminals.
Current Loop Version (DH11-AA, DH11-AC plus 4 DM11-DA Line Adapters)	10048-3	Basic Board Set plus 20 mA current loop distribution panel and interconnecting cable. Does not include cables for terminal connection.

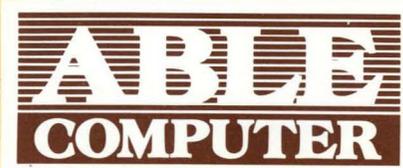
SPECIFICATIONS

Bus Loading: The DMAX/16 presents less than two unit loads to the Unibus: one receiver and two drivers. The dataset control presents one unit load.

Power Requirements:

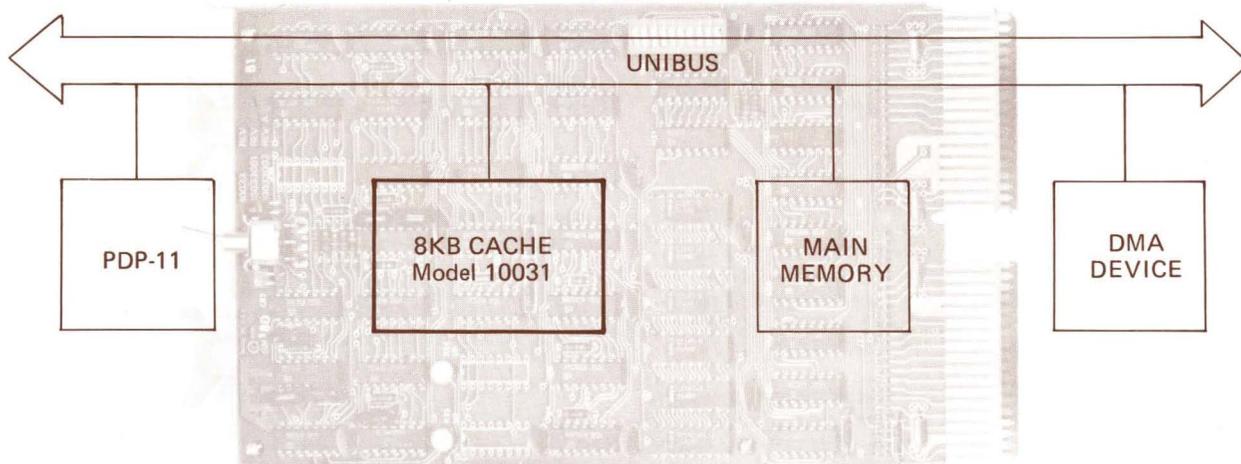
Model	Voltage	Current
10048-0	+5 volts ±15 volts	8.0 amps 0.25 amps
10048-1	+5 volts ±15 volts	8.0 amps 0.25 amps
10048-2	+5 volts ±15 volts	10.3 amps 0.75 amps
10048-3	+5 volts ±15 volts	8.0 amps 0.75 amps





CACHE/434™ CACHE/440™ (8K BYTE UNIBUS* CACHE)

The CACHE/434 and CACHE/440 are the industry's first 8K byte cache memories for the PDP*-11/34, -11/34A and PDP-11/35, -11/40 computers respectively.



FEATURES

- ABLE's versatile 8K byte cache memory (THE CACHE) can significantly increase throughput on PDP-11/34, 11/34A, 11/35, or 11/40 systems
- THE CACHE requires no additional backplane space — it mounts in the space normally required for a Unibus interconnect module
- THE CACHE is easy to install — no backplane modification or system generation is required
- THE CACHE is fully compatible with your operating system and requires no hardware or software changes
- THE CACHE utilizes data parity checking to insure the integrity of data presented to the Unibus
- Address parity protection insures proper CACHE performance over the specified address range
- Activity indicators let you know that THE CACHE is functioning and provide an indication of the approximate hit ratio
- An automatic CACHE disable feature prevents system down time in the event of CACHE failure
- THE CACHE offers address limiting which allows the user to optimize system performance.

GENERAL DESCRIPTION

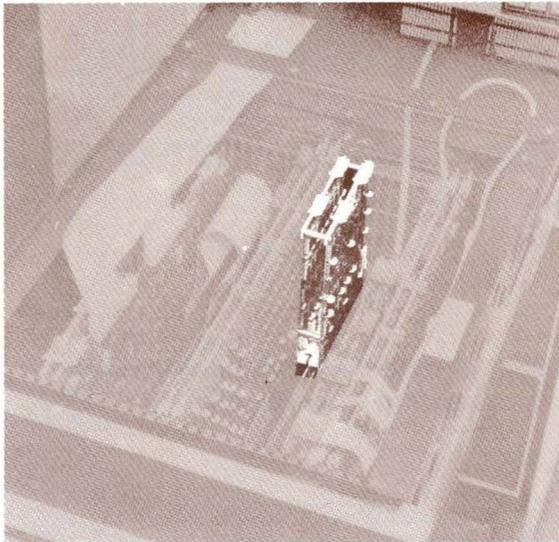
THE CACHE contains 8192 bytes of high-speed memory. It is implemented on a pair of dual-width modules. In the PDP-11/34 and -11/34A, it replaces the M9202 interconnect module; in the PDP-11/35 and -11/40 systems, it replaces the M981 interconnect module.

DATA AND ADDRESS PARITY — THE CACHE monitors both address and data parity. If a parity error occurs, data is not permitted to pass onto the Unibus. A switch on the module allows the user to choose between two modes of operation: in one mode THE CACHE takes itself off-line when an error occurs, in the other mode THE CACHE continues to run and continues to pass only good data onto the Unibus.

ACTIVITY INDICATORS — Two activity indicators give visual display of CACHE operation. A green LED indicates hit rate — the more reads from CACHE, the brighter the light. A red LED indicates CACHE error.

ON-LINE/OFF-LINE SWITCH — This conveniently located toggle switch is especially useful for running benchmarks and allows THE CACHE to be disabled for maintenance checks.

ADDRESS LIMIT SWITCHES — Upper and lower address limit switches are provided for users who want to optimize THE CACHE performance by specifying the exact operating range of THE CACHE in 8K word increments. This allows the user to tailor THE CACHE to his system for maximum system performance.



CACHE/434 installs in place of M9202 in PDP-11/34 and -11/34A (shown above). CACHE/440 installs in place of M981 in PDP-11/35 and -11/40.

FUNCTIONAL DESCRIPTION

THE CACHE utilizes a "write through" algorithm. Data read from Unibus main memory is mapped into THE CACHE as it is accessed by the processor. On succeeding read operations this mapped data is read directly from THE CACHE. DMA reads are not mapped into THE CACHE if the DMA device is physically located behind THE CACHE.

During memory write operations from either the processor or a DMA device, data already in THE CACHE is updated so that it is always identical to the data in main memory. If the data to be written is not currently mapped in THE CACHE, THE CACHE remains unchanged.

DIAGNOSTIC COMPATIBILITY

Diagnostics may be run with CACHE except the following:

1. Certain diagnostics based on time-dependent software may not operate properly with CACHE due to significant speed enhancement.
2. Parity memory diagnostics that write wrong parity on a location already mapped into CACHE will not give the expected parity error, causing a diagnostic error printout where there is no actual hardware malfunction.

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SPECIAL MEMORY PRODUCTS

- SCAT/45 (330 nsec Fastbus Memory)
- CACHE/434 (8KB Unibus Cache)
- UNIMAP (4MB PDP-11/23 Upgrade)
- ENABLE/34 (RSTS/E System Expander)

GENERAL PURPOSE PRODUCTS

- QNIVERTER (Dual-Purpose Converter)
- REBUS (DB11-A Replacement)
- DUAL I/O (Dual DR11-C)
- INTERLINK (DR11-B Replacement)
- BUSLINK (DA11-B — Unibus/Q Bus)

COMMUNICATIONS PRODUCTS

- QUADRASYNC/B, C (4-line DL11-B, DL11-C)
- QUADRASYNC/E (4-line DL11-E)
- QUADRACALL (4-line DN11)
- ABLE DV/16 (DV11 Replacement)
- ABLE DZ/16 (DZ11-E Replacement)
- ABLE DH/DM (DH11 and DM11 Replacement)
- ABLE VaxDZ (VAX Controller)

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ORDERING INFORMATION

Model	ABLE Order Number*	Description
CACHE/434	10031 for PDP-11/34 and 34A	Dual-width module with set of resistor packs for converting to CACHE/440.
CACHE/440	10031 for PDP-11/35 and 40	Dual-width module with installed resistor packs.
*Be sure to specify the computer model number.		

SPECIFICATIONS

- Size: 8192 bytes
- Word Length: 24 bits (16 data + 2 parity; 5 address + 1 parity)
- Storage Media: 4096 x 1 RAM's
- Typical Access Time: 35 nsec
- Cycle Time: Limited only by CPU cycle time
- Bus Loading: 1 unit load
- Power: CACHE/434 5 amps at 5 volts
- CACHE/440 6.2 amps at 5 volts (includes Unibus terminator)

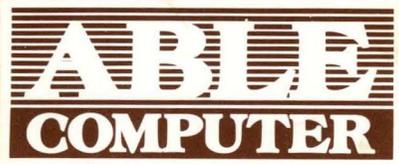
SPECIAL CONSIDERATIONS

Memory installed within the DD11-P processor backplane cannot be included in CACHE operation. If it is not possible to physically place this memory behind THE CACHE, it can be excluded using the upper and/or lower address limit switches.

Represented by:



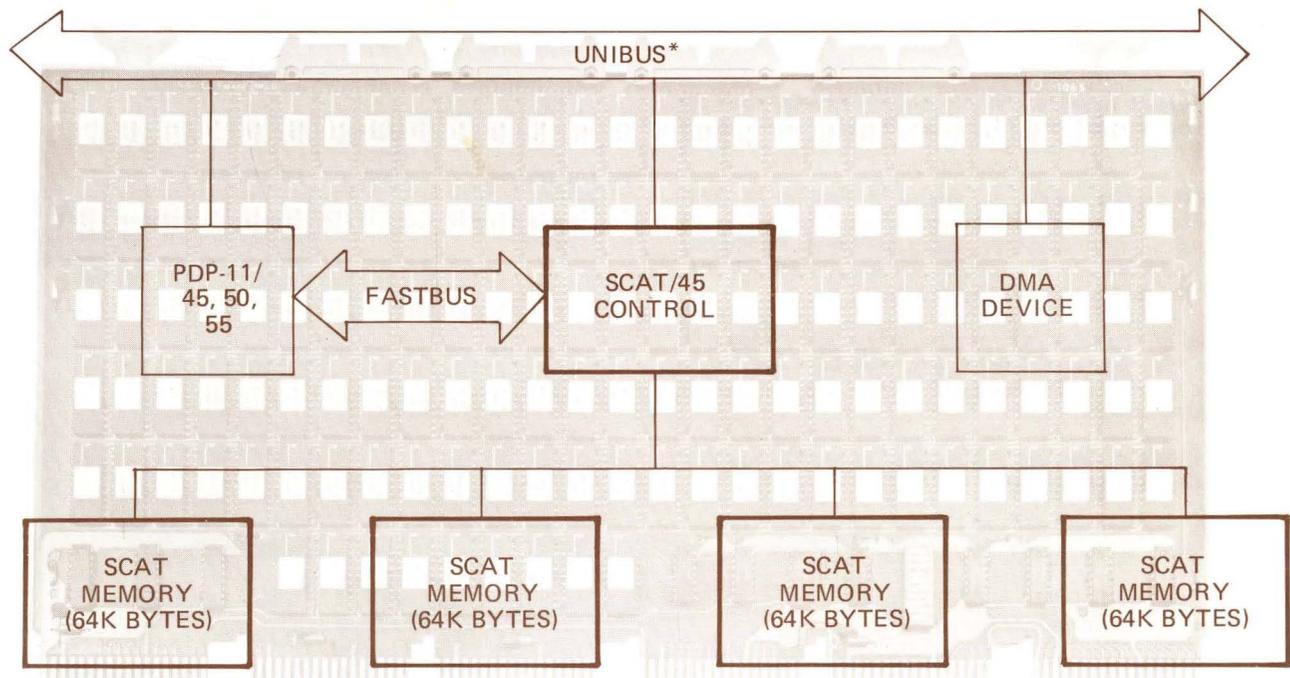
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San Jose, CA 95128
(408) 947-0622



SCAT/45™

(Add-In Fastbus* Memory)

Your PDP*-11/45, 11/50, or 11/55 processor can function up to three times faster with ABLE's SCAT/45 Fastbus memory.



FEATURES

- With SCAT/45 maximum utilization of the Fastbus can be realized — all 256K bytes of memory can reside on the Fastbus
- Processor instruction cycle time is reduced to 330 nsec with SCAT/45 compared to the 970 nsec time required when using 32K bytes of DEC* Unibus memory
- SCAT/45 offers substantial cost savings — 256K bytes of memory from ABLE costs about as much as 64K bytes from DEC
- SCAT minimizes Unibus loading
- Easy to install — only one +5 volt power regulator needed
- Simplifies system configuration and can eliminate the need for expansion boxes and bus repeaters
- SCAT/45 is system software compatible with the PDP-11/45, 11/50, and 11/55
- The high density design of SCAT/45 allows 64K bytes of Fastbus memory on each hex module.

GENERAL DESCRIPTION

The Fastbus was designed to decrease memory access time by providing a separate memory bus. Until now only 32K of memory could be placed on the Fastbus. With SCAT/45 all 256K bytes of memory can be accessed by the Fastbus (4K words are reserved for I/O space).

SCAT/45 is add-in parity memory for PDP-11/45, 11/50, and 11/55 computers. It is a dual port memory that conforms to both Unibus and Fastbus disciplines. It can be used with DEC bipolar or MOS memory already on the Fastbus if there is a control slot available (slot 16 or 21).

SCAT/45 is comprised of a hex-width control board, one to four hex-width memory boards, and an optional +5 volt power supply regulator. The control board can control from one to four memory modules. Each memory module contains 32K x 18 bits of static high speed MOS memory. A switch on each board specifies which memory it is in the series.

INSTALLATION

- SCAT/45 control modules(s) install in Fastbus slots 16 or 21
- SCAT/45 memory modules install in Fastbus slots 18 to 20 or 22 to 25
- Optional H744 power supply installs per DEC guidelines

DIAGNOSTIC COMPATIBILITY

- ZQMC 0-124K Memory Exerciser, 16K Version (DEC provided Mod for Fastbus Memory)
- ZQMB 0-124K Memory Exerciser
- ZQMA Memory I/O Exerciser
- CMFA Combined MOS/Core Parity Memory Test

SPECIAL CONSIDERATIONS

1. Certain diagnostics based on time-dependent software may not operate properly with SCAT/45 due to significant speed enhancement.
2. Each SCAT/45 control module is capable of handling all 256K bytes of memory. If further run time reductions are desired, two control units allow the processor to access memory via the Fastbus at the same time a DMA device is accessing memory via the Unibus. (See block diagram of a typical configuration.)
3. Devices used on the SCAT/45 reflect a failure rate of less than 0.012% per 1000 hours. ECC which is normally considered to be requisite for dynamic MOS devices is neither required by nor applicable to the SCAT/45.
4. An H744 +5 volt power supply is required to provide power to SCAT/45 (purchased separately).

SPECIFICATIONS

Fastbus Cycle Time* 330 nsec
Unibus Loading 1 unit load per control board

*Fastbus architecture eliminates deskew times inherent to the Unibus. This allows processor instruction times to be significantly improved using Fastbus memory. Processor instruction times should not be compared with Fastbus or Unibus memory cycle times which are different measurements. PDP-11/45 class processors with SCAT/45 will always outperform any current Unibus memory complement.

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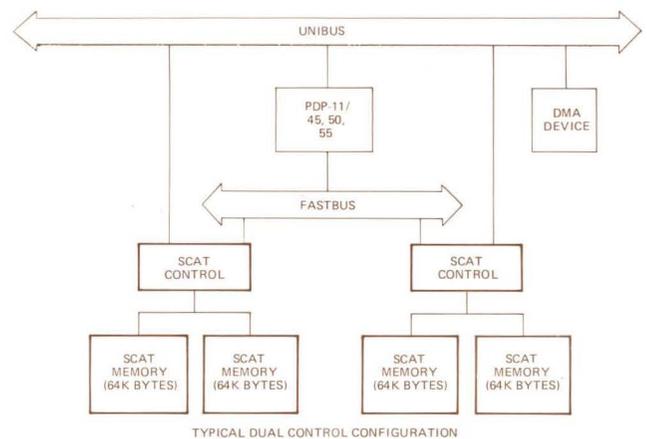


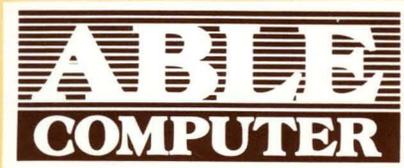
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ORDERING INFORMATION

Model	ABLE Order Number	Description
32K Fastbus Memory System	10019-0	Consists of one hex-width memory and a hex width control board
64K Fastbus Memory System	10019-1	Consists of two hex-width memory boards and a hex-width control board
96K Fastbus Memory System	10019-2	Consists of three hex-width memory boards and a hex-width control board
128K Fastbus Memory System	10019-3	Consists of four hex-width memory boards and a hex-width control board
Control Unit	10017	Consists of one hex-width control board
Memory Unit	10025	Consists of one hex-width memory board

Accessory	ABLE Order Number	Description
+5 Volt Power Supply	H744	The +5 volt power supply can supply power for up to four memory boards plus two control boards. Available from ABLE or DEC.

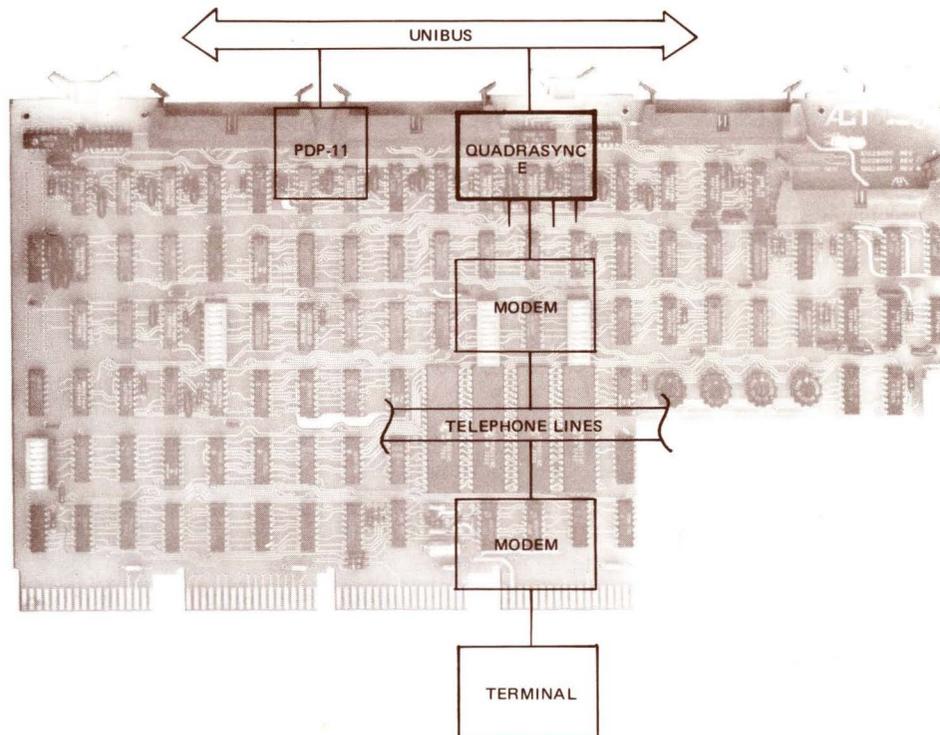




QUADRASYNC/E™

(Four Line DL11-E Equivalent)

The space-saving QUADRASYNC/E provides an interface between the PDP-11* Unibus* and four asynchronous communication channels with full dataset control.



FEATURES

- QUADRASYNC/E offers the features of four DEC* DL11-E's on one extended quad-width module
- The compact unit saves you space and power
- Presents only one unit load for four lines while DEC's DL11-E presents one for each line
- On-board switches for address and vector selection add flexibility without the need for jumpers
- Rotary switches allow easy selection of baud rates
- Eight baud rates are independently selectable for each channel
- Data format is jumper selectable for 5, 6, 7, or 8 data bits and 1, 1.5, or 2 stop bits
- QUADRASYNC/E is compatible with DEC operating system software
- QUADRASYNC/E supports full dataset control operation.

GENERAL DESCRIPTION

QUADRASYNC/E provides full duplex or half duplex communication between a PDP-11 and four asynchronous communication channels. It receives serial data from peripheral devices, converts it to parallel words and presents it to the Unibus. It accepts parallel data from the bus and converts it to serial data for transmission to peripheral devices.

QUADRASYNC/E provides complete dataset control for remote connection to EIA/CCITT terminals or to another PDP-11 computer. The user may select baud rate, address and vector locations, character format, and parity.

QUADRASYNC/E is contained on an extended quad-width module with four, 40-pin DEC compatible Berg connectors. Leads supported include: Receive, Transmit, Carrier, Ring, Request to Send, Clear to Send, Data Terminal Ready, Secondary Transmit Data, and Secondary Receive Data. EIA cables are ordered separately.

DATA FORMAT

Data format is serial with a choice of 1, 1.5, or 2 stop bits and 5, 6, 7, or 8 data bits. Parity is selectable as odd, even, or no parity.

DATA RATES

QUADRASYNC/E offers eight selectable baud rates. Transmitter and receiver operate at the same baud rate. The user may choose from the following rates:

9600	2400	600	150
4800	1200	300	75

ADDRESS SELECTION

Address selection is via on-board pencil switches. Addresses are in the range 774000 through 777776. Each QUADRASYNC/E requires 16 contiguous word locations.

VECTOR SELECTION

Vector selection is via on-board pencil switches. Vectors are in the range 000 through 774. Each QUADRASYNC/E requires 16 contiguous vector locations.

REGISTERS

QUADRASYNC/E has four addressable registers as follows:

Receiver Status Register (RCSR)	7XXXX0
Receiver Buffer Register (RBUF)	7XXXX2
Transmitter Status Register (XCSR)	7XXXX4
Transmitter Buffer Register (XBUF)	7XXXX6

SPECIAL CONSIDERATIONS

Address and vector locations are not independently selectable for the four channels but require 16 contiguous locations that are specified by one set of switches.

SPECIFICATIONS

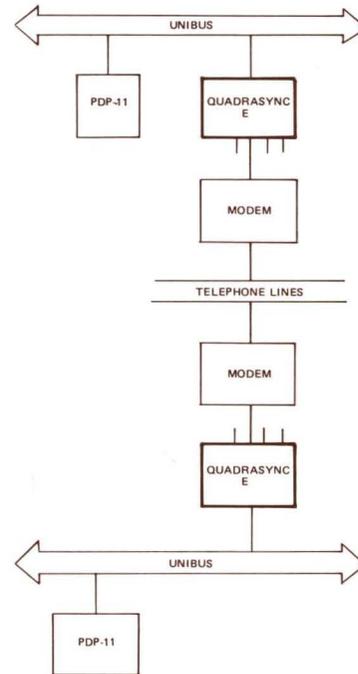
Bus Loading: 1 unit load

Power Required:	Voltage	Current
	+5 volts	2.30 amps
	+15 volts	0.10 amps
	-15 volts	0.20 amps

ORDERING INFORMATION

Model	ABLE Order Number	Description
QUADRASYNC/E	10028	Extended quad-width module for connection to four remote EIA/CCITT terminals. Does not include modem cable; use cable number 90000013.

Accessory	ABLE Order Number	Description
Modem Cable	90000013	25 foot cable equivalent to the DEC BC05-C-25 cable. One required per channel.



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SPECIAL MEMORY PRODUCTS

SCAT/45 (330 nsec Fastbus Memory)
 CACHE/45 (2KB Fastbus Cache)
 CACHE/434 (8KB Unibus Cache)
 CACHE/440 (8KB Unibus Cache)

GENERAL PURPOSE PRODUCTS

QINVERTER (Dual-Purpose Converter)
 REBUS (DB11-A Replacement)
 DUAL I/O (Dual DR11-C)
 INTERLINK (DR11-B Replacement)
 BUSLINK (DA11-B — Unibus/Q Bus)

COMMUNICATIONS PRODUCTS

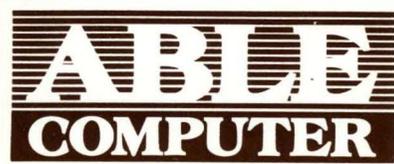
QUADRASYNC (4-line DL11)
 QUADRASYNC/E (4-line DL11-E)
 QUADRACALL (4-line DN11)
 ABLE DV/16 (DV11 Replacement)
 ABLE DZ/16 (DZ11-E Replacement)
 ABLE DH/DM (DH11 and DM11 Replacement)

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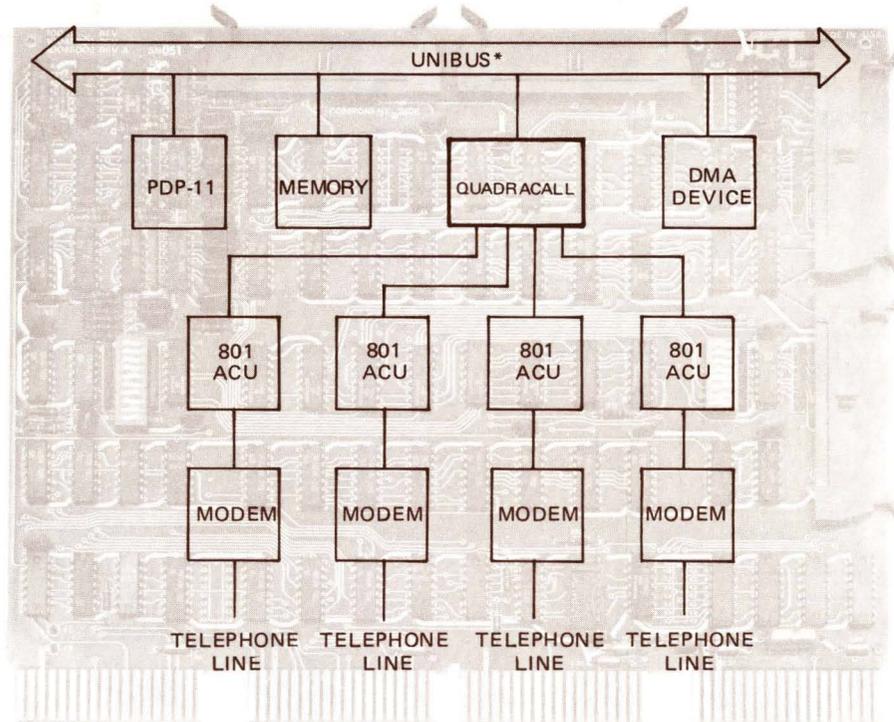




QUADRACALL™

(Four Line DN11 Replacement)

QUADRACALL is a single quad-width module that connects up to four Automatic Calling Units (ACU) to a PDP-11*.



FEATURES

- QUADRACALL is software compatible with four DEC* DN11 units and provides connection to four Bell 801 ACU lines
- Saves space even for the one line user — requires one quarter the space of the DEC DN11
- Unburdens the Unibus — presents only one unit load to the Unibus while the DN11 presents four unit loads for four-line operation
- On-board switches for address and vector selection add flexibility without the need for jumpers
- The QUADRACALL single quad module is easy to install compared with DEC's four slot dedicated backplane
- Cost effective — QUADRACALL provides four channels for about as much as a one channel DEC DN11.

GENERAL DESCRIPTION

QUADRACALL provides an interface between a PDP-11 computer and up to four Bell 801 Automatic Calling Units (ACU). With QUADRACALL and an ACU a PDP-11 can dial any telephone number to establish a data link without the need for user intervention.

The user has access to all lines of the ACU through the QUADRACALL. Input leads to the QUADRACALL are: Power Indicator, Data Line Occupied, Abandon Call and Retry, Data Set Status, and Present Next Digit. Output leads from QUADRACALL include: Digit Present, Call Request, and four digit leads to each ACU.

QUADRACALL is contained on a single quad-width board and can be plugged into any SPC slot. Connection between the ACU and QUADRACALL is accomplished via four 40-pin Berg connectors mounted on the module and a modem cable terminated with a standard 25-pin EIA connector (ordered separately).

ADDRESS SELECTION

Address selection is accomplished via on-board pencil switches. The address range is 760000 through 777776 and is normally set to 775200. QUADRACALL requires four contiguous addresses beginning on a boundary of zero.

VECTOR SELECTION

Vector selection is via on-board pencil switches. The vector range is from 000 through 774, and is normally set to 300.

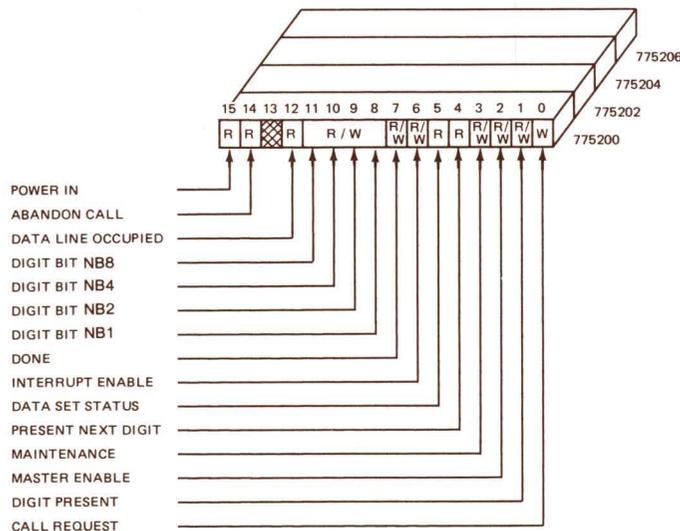
PRIORITY LEVEL

QUADRACALL is shipped at a BR4 interrupt level. The priority level can be easily changed.

DIAGNOSTIC COMPATIBILITY

ZDNA DN11 Digital Dialer

PROGRAMMING INFORMATION



ORDERING INFORMATION

Model	ABLE Order Number	Description
QUADRACALL	10045	One quad-width module equivalent to four DN11's

Accessory	ABLE Order Number	Description
Modem Cable	90000013	25 foot cable with 25-pin EIA connector. Equivalent to the DEC BC05C-25 cable. One required per channel.

SPECIFICATIONS

Bus Loading: The QUADRACALL presents one unit load to the Unibus

Power Required: 1.9 amps at +5 volts
0.2 amps at -15 volts
0.2 amps at +15 volts (or +8 vrms)

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SPECIAL MEMORY PRODUCTS

SCAT/45 (330 nsec Fastbus Memory)
CACHE/45 (2KB Fastbus Cache)
CACHE/434 (8KB Unibus Cache)
CACHE/440 (8KB Unibus Cache)

GENERAL PURPOSE PRODUCTS

QNIVERTER (Dual-Purpose Converter)
REBUS (DB11-A Replacement)
DUAL I/O (Dual DR11-C)
INTERLINK (DR11-B Replacement)
BUSLINK (DA11-B — Unibus/Q Bus)

COMMUNICATIONS PRODUCTS

QUADRASYNC (4-line DL11)
QUADRASYNC/E (4-line DL11-E)
QUADRACALL (4-line DN11)
ABLE DV/16 (DV11 Replacement)
ABLE DZ/16 (DZ11-E Replacement)
ABLE DH/DM (DH11 and DM11 Replacement)

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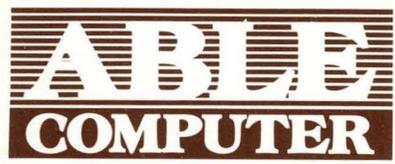


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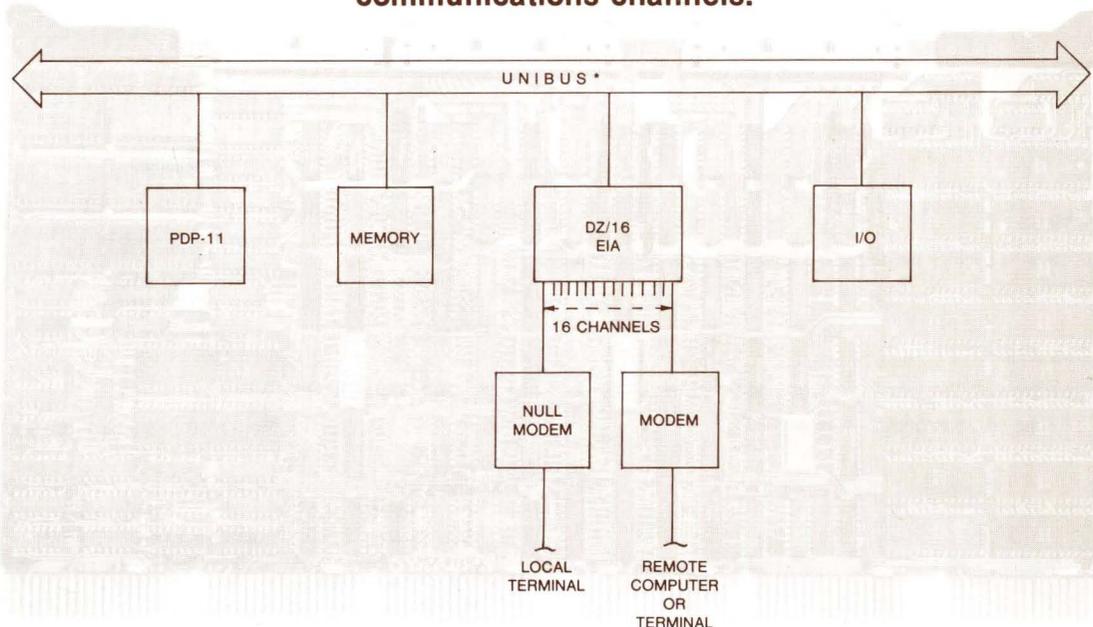
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San Jose, CA 95128
(408) 947-0622



DZ/16

(DZ11-E Replacement)

The DZ/16 is a space-saving multiplexer that connects a PDP-11* to sixteen asynchronous communications channels.



FEATURES

- Like the DEC* DZ11, the DZ/16 is a low cost method of connecting multiple terminals at moderate throughput
- Uses half the space of the DZ11-E by providing 16-line operation on only one hex-width board
- Unique on-board self-test with LED display
- Presents half the Unibus loading of the DZ11-E
- On-board switches for address and vector selection add flexibility without the need for jumpers
- Supports all DZ11 baud rates
- Data format is program selectable for each individual channel
- The DZ/16 is compatible with DEC diagnostic and operating system software

GENERAL DESCRIPTION

The DZ/16 is a microprocessor based controller which connects a PDP-11 to 16 asynchronous communication lines by emulating the functions of two DZ11 controllers.

Physically, the DZ/16 consists of a hex-width board, EIA distribution panel, and interconnecting cables. It installs into any hex-width SPC slot of a standard DEC DD11 backplane.

PROGRAMMABLE LINE PARAMETERS

Character Length	5, 6, 7, or 8 bits
Number of Stop Bits	1 or 2 for 6, 7, or 8-bit characters 1 or 1.5 for 5-bit characters
Parity Generation/Detection	Odd, even, or no parity
Operating Mode	Full duplex
Transmitter/Receiver Speed (Baud)	50, 75, 110, 134.5, 150, 300, 600 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600

Breaks may be generated and detected on each line.

ADDRESSABLE REGISTERS

The DZ/16 has six addressable registers that require only four words per eight-line group.

Register	Mnemonic	Operation	Bus Address
Control and Status	CSR	Read/Write	76XXX0
Line Parameter	LPR	Write Only	76XXX2
Receiver Buffer	RBUF	Read Only	76XXX2
Transmitter Control	TCR	Read/Write	76XXX4
Transmit Data	TDR	Write Only	76XXX6
Modem Status	MSR	Read Only	76XXX6

ADDRESS SELECTION

Address selection is via on-board pencil switches. Addresses are in the range 760000 through 763776. The DZ/16 requires eight contiguous word addresses beginning on a boundary of 76XXX0.

VECTOR SELECTION

Vector selection is via on-board pencil switches. The vector range is from 000 through 774. The DZ/16 requires four contiguous addresses beginning on a boundary of XX0.

PRIORITY SELECTION

The DZ/16 priority level is factory set to a BG5 level interrupt. This level may be user modified.

DIAGNOSTIC COMPATIBILITY

The DZ/16 is compatible with the following diagnostic provided by DEC:
ZDZA DZ11 8-Line Asynchronous Multiplexer Test

ORDERING INFORMATION

Model (DEC #)	ABLE Order Number	Description
DZ/16 (DZ11-E)	10090-1	Hex-width board, EIA distribution panel, and interconnecting cable.

ELECTRICAL INTERFACE

The DZ/16 provides a voltage level interface and connector whose signal levels and connector pinning conform to EIA Standard RS232-C and CCITT Recommendations V.24. Leads supported are:

Protective Ground	Signal Ground
Transmitted Data	Received Data
Data Terminal Ready	Ring Indicator
Carrier	

SPECIFICATIONS

Bus Loading: Presents one unit load.

Power Requirements:

Voltage	Current
+5 volts	4.2 amps
+15 volts	0.35 amps
-15 volts	0.15 amps

SPECIAL CONSIDERATIONS

- Address selection on the DZ/16 is limited to the floating address space (76XXX0 - 763776).
- The DZ/16 emulates two DEC DZ11's, providing sixteen communication channels. For those cases when the user may require only eight lines on the DZ/16, an optional switch is provided to disable the upper eight lines (8-15) from responding. Because this option disables the second set of lines, only the first four contiguous addresses and the first two vector locations are accessible.

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SPECIAL MEMORY PRODUCTS

SCAT/45 (330 nsec Fastbus Memory)
CACHE/45 (2KB Fastbus Cache)
CACHE/434 (8KB Unibus Cache)
CACHE/440 (8KB Unibus Cache)
EMULOADER (ODT/Boot Loader)

GENERAL PURPOSE PRODUCTS

QNIVERTER (Dual-Purpose Converter)
UNIVERTER (Converter with Map)
REBUS (DB11-A Replacement)
DUAL I/O (Dual DR11-C)
INTERLINK (DR11-B Replacement)
BUSLINK (DA11-B--Unibus/Q Bus)

COMMUNICATIONS PRODUCTS

QUADRASYNC (4-line DL11)
QUADRASYNC/E (4-line DL11-E)
QUADRACALL (4-line DN11)
DMAX/16 (DH11 Replacement)
DV/16 (DV11 Replacement)
DZ/16 (DZ11-E Replacement)

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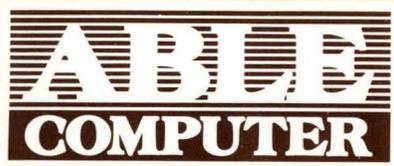


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Represented by:

Reptek

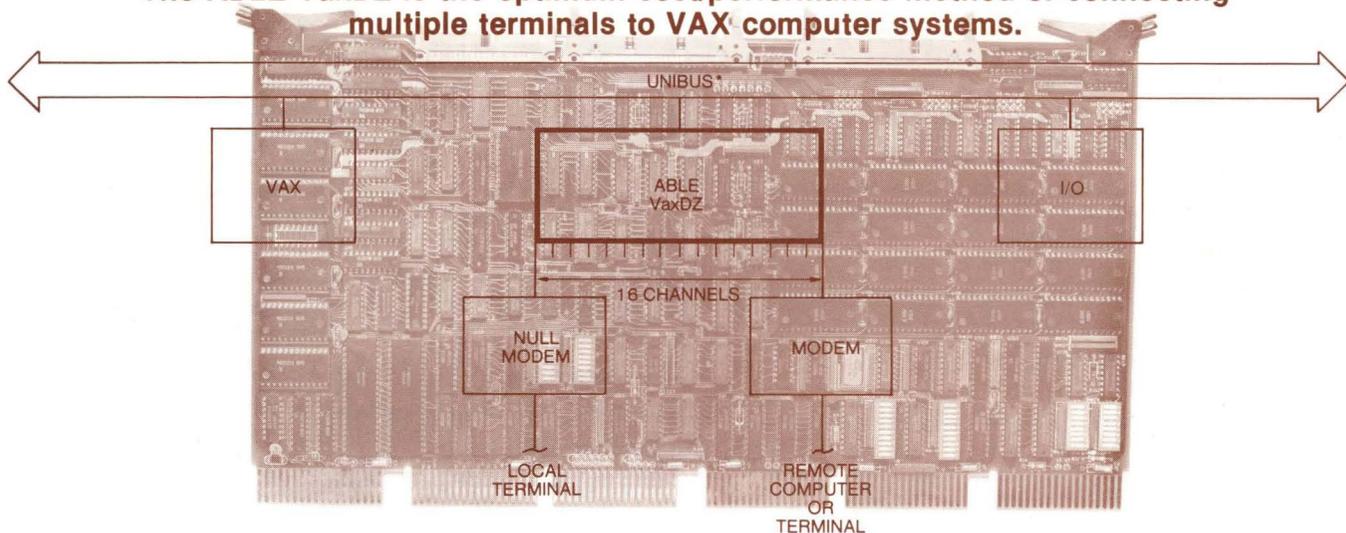
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San Jose, CA 95128
(408) 947-0622



ABLE VaxDZ

(Optimized Communications Controller for VAX*)

The ABLE VaxDZ is the optimum cost/performance method of connecting multiple terminals to VAX computer systems.



FEATURES

- ABLE VaxDZ is an extension of ABLE's established line of micro-programmed communications controllers which:
 - + Outperform existing DZ and DH products,
 - + Operate compatibly with standard diagnostics/operating systems, and
 - + Are designed to allow user-elected product migration without board replacement.
- Substantial performance improvement in all VAX computer systems is gained by an integral:
 - + OUTPUT buffer which lets you select any silo depth from 0 to 16 characters per line. You literally can set the optimum performance level for your system.
 - + INPUT buffer twice the DZ11 standard size (an intelligent silo alarm control), which supports dramatic improvement in input character handling at every possible line configuration.
 - + "Output throttle" which allows any external device to control the clear to send (CTS) line and optimize its own data rate. This is a software transparent "natural" for small printers, graphics terminals, etc., to eliminate serial X-ON/X-OFF problems.
- Supports all DZ baud rates plus split and non-standard baud rates when specified.
- Unique on-board diagnostic performs comprehensive self-test with LED display.

GENERAL DESCRIPTION

The ABLE VaxDZ is a microprocessor-based controller. It connects a VAX to 16 asynchronous communication lines. The ABLE VaxDZ provides a tailored design to optimize VAX system performance. It emulates the functions of two DZ controllers with an efficiency rivaling or exceeding DH performance.

Physically, the ABLE VaxDZ consists of a single hex-width board, distribution panel, and interconnecting cables. It installs into any hex-width SPC slot of a standard DEC DD11 backplane or equivalent in half the space and half the bus loading of the DEC DZ.

An optional 16-line EIA/current loop line adapter provides user selection of EIA or current loop operation on a line-by-line basis.

PROGRAMMABLE LINE PARAMETERS

Character Length	5, 6, 7, or 8 bits
Number of Stop Bits	1 or 2 for 6, 7, or 8-bit characters 1 or 1.5 for 5-bit characters.
Parity Generation/Detection	Odd, even, or no parity
Operating Mode	Full duplex
Transmitter/Receiver Speed	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600

Breaks may be generated and detected on each line.

ADDRESSABLE REGISTERS

The ABLE VaxDZ has six addressable registers that require only four words per eight-line group.

Register	Mnemonic	Operation	Bus Address
Control and Status	CSR	Read/Write	76XXX0
Line Parameter	LPR	Write Only	76XXX2
Receiver Buffer	RBUF	Read Only	76XXX2
Transmitter Control	TCR	Read/Write	76XXX4
Transmit Data	TDR	Write Only	76XXX6
Modem Status	MSR	Read Only	76XXX6

ADDRESS SELECTION

Address selection is via on-board pencil switches. Addresses are in the range 760000 through 763776. The ABLE VaxDZ requires eight contiguous word addresses beginning on an even boundary (76XX00, 76XX20, 76XX40, 76XX60).

VECTOR SELECTION

Vector selection is via on-board pencil switches. The vector range is from 000 through 774. The ABLE VaxDZ requires four contiguous addresses beginning on a boundary of XX0.

PRIORITY SELECTION

The ABLE VaxDZ priority level is factory set to a BG5 level interrupt. This level may be user modified.

DIAGNOSTIC COMPATIBILITY

The ABLE VaxDZ is compatible with user on-line diagnostics and standard DEC diagnostics.

SPECIAL CONSIDERATIONS

- Address selection on the ABLE VaxDZ is limited to the floating address space (76XXX0-763776), and addresses cannot start on odd boundaries such as 76XX10.
- Consult the ABLE factory for details of split baud rate and non-standard baud rate operation.
- To benefit from the full range of ABLE VaxDZ features, an ABLE-supplied software autopatch is required for version 2X of VMS. Users are required to execute an ABLE VaxDZ software license and to specify media as either floppy disc or TU58 cassette.

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SPECIAL MEMORY PRODUCTS

SCAT/45 (330 nsec Fastbus Memory)
 CACHE/45 (2KB Fastbus Cache)
 CACHE/434 (8KB Unibus Cache)
 CACHE/440 (8KB Unibus Cache)

GENERAL PURPOSE PRODUCTS

QNIVERTER (Dual-Purpose Converter)
 REBUS (DB11-A Replacement)
 DUAL I/O (Dual DR11-C)
 INTERLINK (DR11-B Replacement)
 BUSLINK (DA11-B — Unibus/Q Bus)

COMMUNICATIONS PRODUCTS

QUADRASYNC (4-line DL11)
 QUADRSYNC/E (4-line DL11-E)
 QUADRACALL (4-line DN11)
 ABLE DV/16 (DV11 Replacement)
 ABLE DZ/16 (DZ11-E Replacement)
 ABLE DH/DM (DH11 and DM11 Replacement)

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ORDERING INFORMATION

Model	ABLE Order Number	Description
ABLE VaxDZ with EIA	10140-0	Hex-width board, EIA distribution panel, and interconnecting cables.
ABLE VaxDZ with Line Adapter/Panel	10140-1	Hex-width board, dual purpose (EIA and/or 20ma current loop) line adapter/panel and interconnecting cables.

ELECTRICAL INTERFACE

The ABLE VaxDZ provides a voltage level interface and connector whose signal levels and connector pin pattern conform to EIA Standard RS232-C and CCITT Recommendations V.24. Leads supported are:

Protective Ground	Signal Ground
Transmitted Data	Received Data
Data Terminal Ready	Ring Indicator
Carrier	

Current loop operation (model 10140-1) uses the following pins:

Transmitted Data	Transmitter Current Source
Received Data	Receiver Current Source

SPECIFICATIONS

Bus Loading: Presents one unit load

Power Requirements:

Voltage	Current (EIA)	Current (20ma)
+ 5 volts	4.2 amps	5.0 amps
+ 15 volts	0.35 amps	0.35 amps
- 15 volts	0.15 amps	0.90 amps

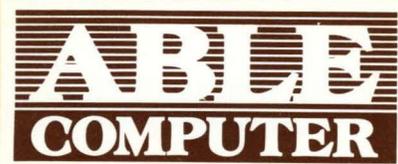
Silo Characteristics:

Input Silo	Two silos, one for each 8 lines 128 characters per silo.
Output Silo	Sixteen silos, one for each line 1 to 16 characters per silo

Represented by:

Reptek

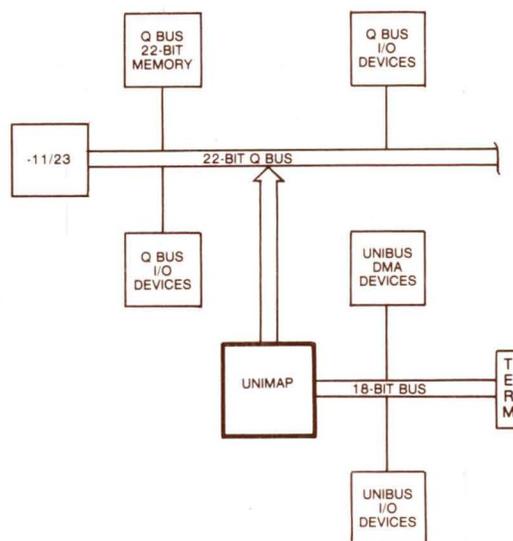
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UNIMAP™

(Allows 4M Byte Upgrade
For PDP-11/23* Systems)

UNIMAP takes - 11/23 systems through the 256K byte addressing barrier into the 4 megabyte world.



FEATURES

- Finally, with UNIMAP, your -11/23 systems have the I/O mapping strength of -11/70's, -11/44's or PAX-enhanced -11/24's with up to 4 million bytes of main memory fully available for optimization of CPU, Q Bus* and/or Unibus* operations.
- With UNIMAP, an -11/23 based system can now literally match strides with the larger and more expensive systems.
- UNIMAP conveniently provides LTC (Line Time Clock) function to maintain software compatibility with major existing operating systems.
- UNIMAP adds IOM (I/O map) function providing software compatible 4M byte addressing for 18-bit DMA devices.
- UNIMAP breaks the 256K byte addressing barrier:
 - + Adds Unibus DMA advantage;
 - + Supports much greater added-value potential for OEM's;
 - + Provides dramatic system performance improvements.
- UNIMAP supports the addition of up to 19 bus loads to any existing -11/23 system.
- Special memory implementations, like Unibus bus window and Unibus dual port operations, are user selectable.
- Installation is simple and direct.
- UNIMAP is software compatible with RSTS/E*, RSX-11* and UNIX.

GENERAL DESCRIPTION

UNIMAP is implemented on a modified quad-width board and is designed to allow 18-bit Unibus DMA devices to address 4 megabytes of Q Bus memory. This is accomplished through the implementation of a bus converter, an arithmetic unit I/O map (IOM) and Line Time Clock (LTC) circuitry to ensure operating system compatibility with standard operating systems.

UNIMAP installs into a quad slot of an LSI-11* backplane and interfaces to the Q Bus via the A and B connectors. A pair of Unibus connectors on the board provide connection to a Unibus cable. The physical arrangement is specifically designed to allow users easy connection of a Unibus cable for external Unibus devices. UNIMAP also provides one end of Unibus termination.

UNIMAP is designed to meet or exceed the needs of the following types of PDP-11/23 systems:

- Timesharing systems with more than eight users;
- Systems dependent on large applications programs;
- Systems which manipulate large data arrays.

INSTALLATION

UNIMAP can be installed into any quad slot of an LSI-11/23 or PDP-11/23 system. LSI-11 interrupt devices and memories can be located ahead of or behind the UNIMAP. All Q Bus devices located behind the UNIMAP will have a lower interrupt priority level than the Unibus devices.

SYSTEM CONFIGURATION

To include UNIMAP in an LSI-11/23 or PDP-11/23 system, the following user-supplied equipment is needed:

- Unibus cable
- M930 Unibus terminator or equivalent
- Unibus backplane for installation of controllers
- Appropriate power source

PRIORITY LEVEL

The LTC has a fixed interrupt level of 6.

VECTOR SETTING

The LTC has a fixed vector setting of 100 (octal).

REGISTERS

UNIMAP contains two sets of registers, the Unibus Map Registers (UMR) and the Line Time Clock Register (LTC).

The UMR's are 32 pairs of 22-bit address relocation registers (17770200 - 17770376) enabling Unibus DMA devices to operate with 22-bit Q Bus memory:

The LTC register (17770546) provides a standard clock used by the operating software to perform such functions as scheduling and recording time of system use. Bit 07, the Monitor bit, is Read/Write 0 Only and is set by the clock and cleared by the program. Interrupt Enable (Bit 06) is Read/Write bit. When set, the clock generates an interrupt.

SOFTWARE

The UNIMAP is software compatible with RSTS/E, RSX-11, and UNIX operating systems.

ORDERING INFORMATION

Model	ABLE Order Number	Description
UNIMAP	10143	Quad-width board; Unibus cable not included.

SPECIFICATIONS

Power Required	5.1 amps @ +5V ±12V not required
Drive Capability	19 Unibus loads
Q Bus Loading	1 DC load 2 AC loads

SPECIAL CONSIDERATIONS

1. UNIMAP is designed to operate with a single computer performing bus arbitrations; it is not intended to be used as an interprocessor function.
2. Certain LSI-11/23 applications mounted in dual-width backplanes will not physically accommodate a quad-width board, like UNIMAP.
3. Older backplanes may not have the signals bussed which are required for 22-bit addressing and therefore, may require modification. The required signals are BDAL 18 through BDAL 21, with pin assignments BC1, BD1, BE1, and BF1.
4. LSI-11/23 CPUs with an etch revision A level are not upgradable to 22-bit addressing and will not operate with a UNIMAP.
5. All Q Bus memory must support 22-bit addressing.
6. To provide control of the UNIMAP by the LSI-11/23, a control signal (BUBMAP-L) must be wired on the backplane to connect the two boards.
7. In order to utilize the I/O map functions with currently available 22-bit software, 18-bit Q Bus DMA devices cannot be supported: equivalent Unibus devices are supported.

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SPECIAL MEMORY PRODUCTS

SCAT/45 (330 nsec Fastbus Memory)
CACHE/434 (8KB Unibus Cache)
UNIMAP (4MB PDP-11/23 Upgrade)
ENABLE/34 (RSTS/E System Expander)

GENERAL PURPOSE PRODUCTS

QNIVERTER (Dual-Purpose Converter)
REBUS (DB11-A Replacement)
DUAL I/O (Dual DR11-C)
INTERLINK (DR11-B Replacement)
BUSLINK (DA11-B — Unibus/Q Bus)

COMMUNICATIONS PRODUCTS

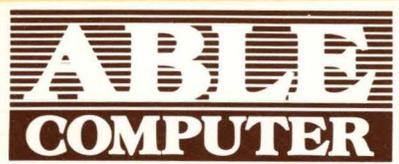
QUADRASYNC/B, C (4-line DL11-B, DL11-C)
QUADRASYNC/E (4-line DL11-E)
QUADRACALL (4-line DN11)
ABLE DV/16 (DV11 Replacement)
ABLE DZ/16 (DZ11-E Replacement)
ABLE DH/DM (DH11 and DM11 Replacement)
ABLE VaxDZ (VAX Controller)

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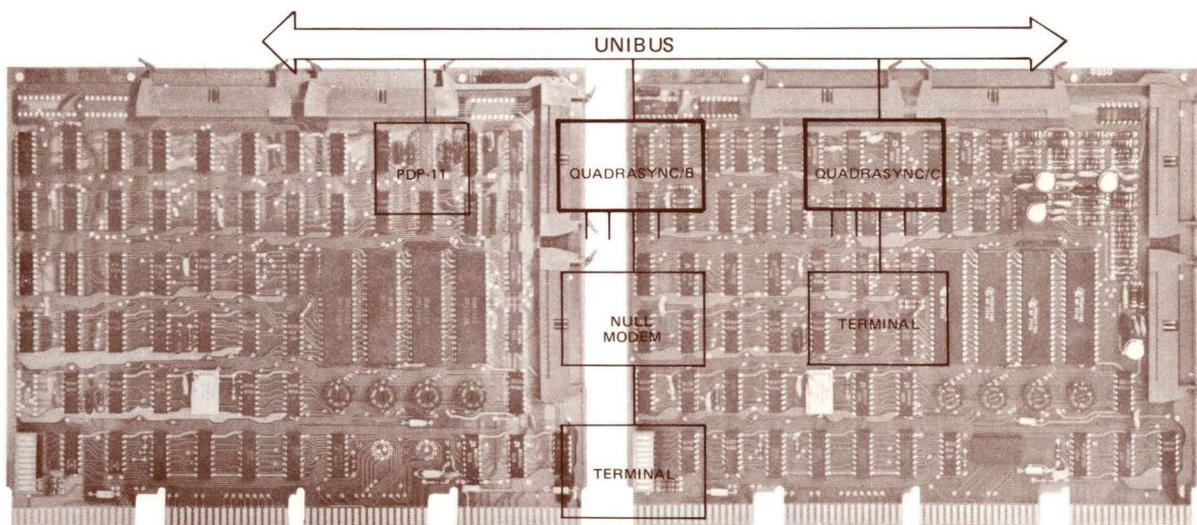




QUADRASYNC/B™ QUADRASYNC/C™

(Four Line DL11-B and
DL11-C Equivalents)

The space saving QUADRASYNC/B and QUADRASYNC/C provide an interface between the PDP-11* Unibus* and four asynchronous communication channels.



FEATURES

- QUADRASYNC/B and /C offer the features of four DEC* DL11's on one quad-width module
- Each compact unit saves you space and power
- Presents only one unit load for four lines while DEC's DL11 presents one for each line
- On-board switches for address and vector selection add flexibility without the need for jumpers
- Data format is jumper selectable for 5, 6, 7, or 8 data bits and 1, 1.5, or 2 stop bits
- Rotary switches allow easy selection of baud rates
- Seven baud rates are independently selectable for each channel
- QUADRASYNC/B and /C are compatible with DEC operating system software.

GENERAL DESCRIPTION

QUADRASYNC/B and /C provide full duplex or half duplex communication between a PDP-11 and four asynchronous communication channels. They receive serial data from peripheral devices, convert it to parallel words and present it to the Unibus. They accept parallel data from the bus and convert it to serial data for transmission to peripheral devices.

QUADRASYNC/B provides connection to EIA/CCITT terminals; it supplies a voltage level interface and connector whose signals conform to EIA standard RS232C and CCITT Recommendation V.24. Leads supported include: Transmit, Receive, Request to Send, and Data Terminal Ready. QUADRASYNC/C provides an interface to 20ma current loop terminals.

QUADRASYNC/B and /C are quad-width modules with four, 40-pin DEC compatible Berg connectors. EIA and current loop cables are ordered separately.

DATA FORMAT

Data format for QUADRASYNC/B and /C is serial with a choice of 1, 1.5, or 2 stop bits and 5, 6, 7, or 8 data bits. Data and stop bits are jumper selectable. Parity is neither generated nor checked.

DATA RATES

QUADRASYNC/B and /C offer seven selectable baud rates. Transmitter and receiver operate at the same baud rate. The user may choose from the following rates:

9600	2400	600	150
4800	1200	300	

ADDRESS SELECTION

Address selection is via on-board pencil switches. Addresses are in the range 774000 through 777776. Each QUADRASYNC/B and /C requires 16 contiguous word locations for addresses starting on boundaries of 00 or 40.

VECTOR SELECTION

Vector selection is via on-board pencil switches. Vectors are in the range 000 through 774. Each QUADRASYNC/B and QUADRASYNC/C requires 16 contiguous locations for vectors starting on boundaries of 00 or 40.

REGISTERS

QUADRASYNC/B and /C have four addressable registers as follows:

Receiver Status Register (RCSR)	7XXXX0
Receiver Buffer Register (RBUF)	7XXXX2
Transmitter Status Register (XCSR)	7XXXX4
Transmitter Buffer Register (XBUF)	7XXXX6

SPECIAL CONSIDERATIONS

1. Address and vector locations are not independently selectable for the four channels but require 16 contiguous locations that are specified by one set of switches.
2. Address and vector locations must begin on boundaries of 00 or 40.
3. The QUADRASYNC/C is active receive and transmit.

ORDERING INFORMATION

Model	ABLE Order Number	Description
QUADRASYNC/B EIA Version	10015	Quad-width module for connection to four EIA/CCITT terminals. Does not include cable; use cable number 90000008.
QUADRASYNC/C Current Loop Version	10022	Quad-width module for connection to four current loop devices. Does not include cable; use cable number 90000011.

Accessory	ABLE Order Number	Description
Cable for QUADRASYNC/B	90000008	25 foot cable equivalent to the DEC BC03L cable.
Cable for QUADRASYNC/C	90000011	25 foot cable equivalent to the DEC KL8/E cable.

SPECIFICATIONS

Bus Loading: 1 unit load

Power Required:	Voltage	Current
QUADRASYNC/B	+5 volts	1.95 amps
	+15 volts	0.10 amps
	-15 volts	0.20 amps
QUADRASYNC/C	+5 volts	2.15 amps
	+15 volts	0 amps
	-15 volts	0.20 amps

ABLE has created a veritable store of DEC computer enhancements. ABLE's unique products help you get more out of your Unibus system. Look at our current product listing . . . you will find solutions of genuine value.

SPECIAL MEMORY PRODUCTS

SCAT/45 (330 nsec Fastbus Memory)
CACHE/434 (8KB Unibus Cache)
UNIMAP (4MB PDP-11/23 Upgrade)
ENABLE/34 (RSTS/E System Expander)

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