acm

# SIGDA NEWSLETTER

SPECIAL INTEREST GROUP ON DESIGN AUTOMATION

VOLUME 4 NUMBER 2 JUNE 1974

## Contents:

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MEMBERSHIP

SIGDA dues are $3.00 for ACM members and $5.00 for non-ACM members. Checks should be made payable to the ACM and may be mailed to the SIGDA Secretary/ Treasurer listed above, or to SIGDA, ACM Headquarters, 1133 Avenue of Americas, New York, N. Y. 10036. Please enclose your preferred mailing address and ACM Number (if ACM member).

SIG/SIC FUNCTIONS

Information processing comprises many fields, and continually evolves new subsectors. Within ACM these receive appropriate attention through Special Interest Groups (SIGs) and Special Interest Committees (SICs) that function as centralizing bodies for those of like technical interests ... arranging meetings, issuing bulletins, and acting as both repositories and clearing houses. The SIGs and SICs operate cohesively for the development and advancement of the group purposes, and optimal coordination with other activities. ACM members may, of course, join more than one special interest body. The existence of SIGs and SICs offers the individual member all the advantages of a homogeneous narrower-purpose group within a large cross-field society.

ACTIVITIES

1) Informal technical meetings at SJSS and FJCC.
2) Formal meeting during National ACM meeting + DA Workshop.
3) Joint sponsorship of annual Design Automation Workshop.
4) Quarterly newsletter.
5) Panel and/or technical sessions at other National meetings.

FIELD OF INTEREST OF SIGDA MEMBERS

Theoretic, analytic, and heuristic methods for:
1) performing design tasks,
2) assisting in design tasks,
3) optimizing designs through

the use of computer techniques, algorithms and programs to:
1) facilitate communications between designers and design tasks,
2) provide design documentation,
3) evaluate design through simulation,
4) control manufacturing processes.

EDITORS MESSAGE

It is with great pleasure that I welcome Bob Smith from SMU as co-editor of the SIGDA Newsletter. It is our intent to increase the technical content of the Newsletter. With Bob's excellent contacts in academia we hope to increase the number of items available for publication.

This issue has another fine bibliography as well as an article from last years ACM conference that didn't get published there.

Future plans include publication of more bibliographies covering all aspects of design automation. Bill Van Cleemputt from the University of Waterloo has sent me an extremely comprehensive (1500 item) bibliography. We hope to publish sections of it in the near future.

This years Design Automation Workshop has a fantastic technical program. There are over 50 papers being presented including 4 tutorials. The concept of an entry level tutorial preceeding the technical presentation in major areas should be a great help to people wanting to hear papers out of their specialty. I hope to see you all in Denver on June 17th.

Steve

Steve Krosner

# CHAIRMAN'S MESSAGE

As I peer northward out my window and watch the traffic move across the Mid-Hudson Bridge, I see a full range of products of man's creation and design.

The suspension bridge which gracefully spans the Hudson River is unique and when designed probably used established technology and structural design techniques. One builds such a bridge "right" the first time. There is no early build and test.

Then there is the automobile, designed out of some standard and some specially designed parts, designed for appearance, comfort, and performance. The individual components are tested to assure that they meet specifications and then the assembly is built, tested, and as required changed to meet certain economic, market, and technical objectives.

On the other hand, the fence outside was designed to the extent that its intended placement was roughly staked out, visualized in the contractor's mind, the cost was quickly estimated, then it was built out of readily available parts.

One can easily visualize the use of computer resources to specify the fencing objectives against a plot plan and even to provide a 3-dimensional view on a graphic display so that the esthetics can be judged. An accurate cost estimate and a complete bill of material can then be outputted. To stake the fence out and erect it would still be left to the contractor.

However, to some it may be a little more difficult to visualize providing vehicle designs directly through the use of computer resources and against supplied technical and economic objectives, as it may also be to visualize the complete design of a suspension bridge which must be correct the first time.

But what was not visualized yesterday is often reality today. May I suggest that you attend the DA Workshop in Denver, June 17-18-19 to be brought up to date.

I'll see you there.

The success of the 1972 and 1973 conferences on computer-aided design has shown the need for a meeting that will bring together industrial users and research workers in all branches of c.a.d. CAD 74 will meet this need.

The dominant theme will be engineering users of c.a.d. - mechanical, civil, architectural, structural, chemical, electrical and control. Recent advances in computer-aided techniques and design methods, either already proven or under development, will be emphasized. Examples can be found in drawing offices, in stress analysis, in project management and in manufacture.

Special c.a.d . topics will be grouped into separate sessions. Examples are optimization, surface and shape description, and graphics. These special-topic sessions will concern themselves with developments in c.a.d. which will affect engineering in 2 - 5 years' time.

Apart from cost and time savings, computer methods have a considerable effect on organizations and people. The conference will, therefore, include sessions on the social implications of c.a.d., the teaching of c.a.d., and the design process itself.

Each session will comprise an invited survey of the state of application or research, followed by submitted papers on particular systems. Sessions are being planned so as to accommodate 100 papers.

CALL FOR PAPERS

Authors are invited to submit synopses of papers. Final date fo synopses is 31st May 1974 but early submissions will be given priority in arranging the conference sessions.

Papers should be sent to the Conference Organizers.



Conference Organisers
M. I. Dawes and G. W. Jones

Exhibition Manager
T. McGowran

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Company Registered in England Registered number 385206

## Needed - ADDITIONAL BOOK REVIEWERS

We have received a copy of COMPUTER-AIDED DESIGN for review. We are looking for two additional reviewers. Please contact Dave Hightower (address inside front cover) directly.

The book is the Proceedings of the IFIP Working Conference in Principles of Computer Aided Design, Findhoven, October 16-18, 1972, and edited by J. Vlietstra and R. F. Wielinga.

The Papers included in the Proceedings are:

1. The Scope of Computer-Aided Design.
2. Foundations of the many manifestations of computer augmented design.
3. Total technology - Integrating design with production.
4. New Concepts in interactive Computing and their relationship to Computer-Aided Design.
5. The engineer's creative activity in a CAD environment.
6. Computer aids in system building.
7. Computer - aided design - an extension of man.
8. Methodical design, the basis of computer-aided design.
9. Software methods in developing CAD programs.
10. Program and information structures in computer-aided design.
11. Lifetime and evolutionary properties of applications software.
12. Computer generation of symbolic network functions - an overview.
13. Computer-aided system reliability analysis and optimization.
14. A system for computer-aided design in architecture.
15. Non-numerical problem solving methods in computer-aided design.

16. Computer-aided design in aircraft industry.

17. Computer-aided design using SYSFAP.

18. A plant and buildings draughting and scheduling system.

19. The application of computer aids to hospital building.

Reduced rates for SIGDA members: The publishers are offering the book at a discount to SIGDA individual members for their personal use. The book is offered at US $19 if prepaid (list around $23.20). Send orders to North-Holland Publishing Co., P.O. Box 211, Amsterdam or American Elseiver Publishing Co. 52 Vanderbilt Ave., New York, N.Y. 10017.

## BOOK AND JOURNAL REVIEWS

The SIGDA Technical Committee intends to review selected books and journal articles and publish the reviews within the SIGDA Newsletters; however, we are in need of additional reviewers. Send your name, address and area of interest to Dave Hightower (address inside front cover). More literature on Design Automation is being published and we feel this is one service we can provide for the DA profession.

# JOURNAL - COMPUTER-AIDED DESIGN

A journal which we will start reviewing on a trial basis is "Computer-Aided Design" published by IPC Science and Technology Press Ltd. (IPC House, 32 High St., Guildford, Surrey, England). The journal is published four times a year and is devoted exclusively to the design-aided application areas.

Again we request those interested in reviewing articles to contact Dave Hightower.

The tables of contents for the last two issues are:

Vol 5, No. 4 October 1973

Computer-aided design in electron optics, P. W. Hawkes.

Computer aids in experimental nuclear plant design, R. K. Hilton.

The application of a computer to hopper design, N. Bundalli.

The balanced approach to process design by computers, H. P. Hutchinson and M. E. Leesley.

An analogue approach to surface definition, J. P. Bloomer, M. M. Sadeghi and G. N. Fedbring.

From words to wires by computer-aided design, A. H. Evans and P. Edmonds.

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Cubic Spline fitting with controlled end conditions, J. D. Adans.

Graphics facilities for computer-aided architectural design, H. Sussock.

The BERSAFE finite element system, T. K. Hellen and S. J. Protheroe.

An integrated c.a.d. system for an architects department, J. W. Paterson.

The inefficiency of the adjoint network approach to the calculation of first order sensitivity coefficients, T.B. M. Neill

Computer simulation of a submersible vehicle, C. Wo and J. O. Geremia.

ELEVENTH ANNUAL DESIGN AUTOMATION WORKSHOP
DENVER HOLIDAY INN, JUNE 17-19, 1974
H.M. WALL, GENERAL CHAIRMAN

## *MONDAY, JUNE 17*

8:00 AM PARTITIONING TUTORIAL — **M. HANAN**, IBM CORPORATION, YORKTOWN HEIGHTS, N. Y.

9:00 AM WELCOME TO DENVER — **P. O. PISTILLI**, ARRANGEMENTS CHAIRMAN

9:05 AM INTRODUCTION — **H. M. WALL**, GENERAL CHAIRMAN

9:20 AM KEYNOTE SPEECH — **STEPHEN J. LUKASIK**, DIRECTOR OF ADVANCED RESEARCH PROJECTS AGENCY, DEPT. OF DEFENSE

10:20 AM ANNOUNCEMENTS

11:00 AM
**"DATA BASE DESIGN FOR DESIGN AUTOMATION – A TUTORIAL"**
E. HASSLER, *TEXAS INSTRUMENTS, DALLAS, TEXAS*

## SESSION 1: LSI

CHAIRMAN: W. CREWS, *MOTOROLA, MESA, ARIZ.*

1:30 PM
**"CRITIC: AN INTEGRATED CIRCUIT DESIGN RULE CHECKING PROGRAM"**
L. M. ROSENBERG AND C. BENBASSAT, *RCA CORP., SOMERVILLE, N. J.*
A production proven IC design rule checking program, CRITIC, which can perform prescribed or user specified physical description checks is described.

2:00 PM
**"MASTER SLICE LSI COMPUTER AIDED DESIGN SYSTEM"**
Y. OZAWA, M. MURAKAMI AND K. SUZUKI, *OKI ELECTRIC INDUSTRY CO. LTD., TOKYO, JAPAN*
This paper presents an LSI-CAD system which is intended for practical use in master-slice LSI design and testing including five sub-systems, a comimon data file, and an on-line graphic display.

2:30 PM
**"ADVANCED LILAC – AN AUTOMATED LAYOUT GENERATION SYSTEM FOR MOS/LSI"**
T. KOZAWA, H. HORINO, T. ISHIGA AND J. SAKEMI, *TOKYO, JAPAN*
An advanced automated layout design system with Cell, ROM-SR, and PLA models for MOS/LSI. The program can generate composite patterns for single chip micro computer MOS/LSI arrays from logic descriptions.

## SESSION 2: GRAPHICS I

CHAIRMAN: J. LOURIE, *IBM CORP. NEW YORK, N. Y.*

1:30 PM
**"COMPUTER AIDED PROCESS DESIGN AND SIMULATION FOR FORGING OF TURBINE BLADES"**
N. AKGERMAN AND D. J. KASIK, *BATTELLE COLUMBUS LABORATORIES, COLUMBUS, OHIO*
A system of computer programs, which utilizes interactive graphics and computer animation, for the design of the forging process for turbine blades, is the subject of this paper.

2:00 PM
**"METASYSTEM: A HIERARCHICALLY STRUCTURED GRAPHIC TOOL"**
N. P. DOONER, J. R. LOURIE, P. VELDERMAN, A. C. GUBIOTTI, AND A. KAUFMAN, *IBM CORP., YORKTOWN HEIGHTS, N. Y.*
This paper explores an interactive graphic system built from a set of hierarchically structured functions. The cohesiveness of each module and minimal interface of modules is presented.

2:30 PM
**"AN INTEGER ARITHMETIC PATH EXPANSION ALGORITHM"**
T. A. WEBER AND D. G. SCHWEIKERT *BELL LABS, MURRAY HILL, N. J.*
Several algorithms essential to the plotting of an expanded slant-line path, for low resolution graphical displays, such as CRT's, have been combined and implemented.

## SESSION 3: PARTITIONING

CHAIRMAN: M. HANAN, *IBM CORP., YORKTOWN HEIGHTS, N. Y.*

3:30 PM
**"AN INTERACTIVE MAN MACHINE APPROACH TO THE COMPUTER LOGIC PARTITIONING PROBLEM"**
M. HANAN, A. MENNONE AND P. K. WOLFF, *IBM CORP., YORKTOWN HEIGHTS, N. Y.*
An interactive approach to the problem of partitioning computer logic which combines aspects of manual and automated approaches and creates results which are better than those obtainable by either approach independently is described.

4:00 PM
**"THE USE OF TOPOLOGICAL MODELS FOR THE CIRCUIT LAYOUT PROBLEM"**
W. M. VANCLEEMPUT, *UNIVERSITY OF WATERLOO, ONTARIO, CANADA*
A state-of-the-art survey of topological methods for solving the circuit layout problem, including one model, which allows pin and gate assignment as a function of layout, is presented.

4:30 PM
**"A PARTITIONING TECHNIQUE FOR LSI CHIPS INCLUDING A BUNCHING ALGORITHM"**
P. T. WANG, *IBM CORP., MANASSAS, VA.*
This paper discusses a partitioning technique which initially orders circuits according to a scoring mechanism, and thus uses a two-stage interchange technique to arrive at a final partition.

## SESSION 4: GRAPHICS II

CHAIRMAN: N. P. DOONER, *IBM CORP., YORKTOWN HEIGHTS, N. Y.*

3:30 PM
**"A SIMPLE COMPUTER-AIDED ARTWORK SYSTEM THAT WORKS"**
D. G. RESSLER, *RCA CORP., SOMERVILLE, N. J.*
A complete computerized artwork processing system for integrated circuits and printed circuit boards is described. The system includes digitizers, plotters, a design rule checker, and a pattern generator command program.

4:00 PM
**"AUTOMATED INSPECTION OF ELECTRONIC ASSEMBLIES"**
C. A. HARLOW, S. E. HENDERSON, D. A. RAYFIELD, AND S. J. DWYER, III, *UNIVERSITY OF MISSOURI, COLUMBIA, MISSOURI*
Automatic Visual Inspection Systems for electronic assemblies have been investigated. Three major phases have been researched: scanning devices, software algorithms, and possible computer systems.

4:30 PM
**"MAP: A USER CONTROLLED AUTOMATED MASK ANALYSIS PROGRAM"**
C. L. MITCHELL, *M&S COMPUTING, INC,* AND J. M. GOULD, *NASA, HUNTSVILLE, ALA.*
A general program for mask analysis is presented. The command language including operational, list processing and dimensional processing commands is described.

6:00 PM COMMON INTEREST GROUP MEETINGS
PARTITIONING
DATA BASE DESIGN
ACM SIGDA
IEEE DA TECH COMM

## *TUESDAY, JUNE 18*

8:00 AM
SIMULATION AND TEST GENERATION TUTORIAL
S. A. SZYGENDA, *UNIVERSITY OF TEXAS, AUSTIN, TEXAS*

## SESSION 5: DOCUMENTATION SYSTEMS

CHAIRMAN: C. E. RADKE, *IBM CORP., POUGHKEEPSIE, N. Y.*

9:00 AM
**"AUTOMATED DESIGN AND MANUFACTURE OF PRINTED CIRCUIT BOARDS"**
D. L. PETERSON, *LEAR SIEGLER, INC., GRAND RAPIDS, MICH.*
The reasons behind one company automating the design of printed circuit boards are exposed. The resultant accomplishments, the economic benefits and the reduction in calendar days for development as a result of automation are detailed.

## SESSION 5: DOCUMENTATION SYSTEMS

9:30 AM

**"A SIMPLE, EFFICIENT DESIGN AUTOMATION PROCESSOR"**

L. E. DRUFFEL, D. C. SCHMIDT AND R. A. WAGNER, *VANDERBILT UNIVERSITY, NASHVILLE, TENN.*

A base system which processes, provides simulation, allows physical description of small logical switching systems (e. g., controllers, mini-computers) is described. The system was developed as a design, education, and research tool.

10:00 AM

**"MICROPROGRAMMING DESIGN SUPPORT SYSTEM"**

A. YAMADA, *NIPPON ELECTRIC CO., LTD., TOKYO, JAPAN*

A microprogramming design support system addressing requirements for central processors, peripheral controls and terminals is described. The total system is described from the design language to the post-processing of bit patterns.

11:00 AM

**"COMPUTER AIDED SCHEMATICS"**

G. G. HAYS, *WESTINGHOUSE ELECTRIC CORP., BALTIMORE, MARYLAND*

A program is described which aids in the generation of support publications for digital hardware. Besides an indicated 33% cost savings, shorter publication time and earlier start of the publication effort is achieved.

11:30 AM PANEL DISCUSSION – DOCUMENTATION SYSTEMS

## SESSION 6: TEST DATA GENERATION

CHAIRMAN: **S. A. SZYGENDA**, *UNIVERSITY OF TEXAS, AUSTIN, TEXAS*

9:00 AM

**"AUTOMATIC TEST GENERATION AND TEST VERIFICATION OF DIGITAL SYSTEMS"**

J. P. VERMA, B. M. SELOVE AND J. N. TESSIER, *BURROUGHS CORP., CITY OF INDUSTRY, CALIF.*

A series of programs were developed over the years to completely automate the test cycle – using DA files as input. The output is a test deck in the language of card test equipment and a list of detected or undetected failures.

9:30 AM

**"MSI/LSI IMPACT ON DIGITAL SYSTEM TESTING"**

H. H. HUANG, *NCR CORP., SAN DIEGO, CALIF.*

10:00 AM

**"A SYSTEM OF COMPUTER PROGRAMS FOR EFFICIENT TEST GENERATION FOR COMBINATIONAL SWITCHING CIRCUITS"**

E. KJELKERUD, *THE ROYAL INSTITUTE OF TECHNOLOGY, STOCKHOLM, SWEDEN*

Programs for test generation, fault simulation and test minimization for combinational switching circuits form a special strategy directing the choice of a test set. The object is to minimize the number of tests required for the detection of logical faults.

11:00 AM

**"A HEURISTIC TEST GENERATION ALGORITHM FOR SEQUENTIAL CIRCUITS"**

T. ARIMA, J. OKUDA, G. AMAMIYA AND M. TSUEOYA, *NIPPON ELECTRIC CO., LTD., TOKYO, JAPAN*

A new algorithm for test generation for a sequential circuit with at least one thousand logic blocks is discussed. It is based on special values expressed in boolean vectors, their logical operations, and three basic theorems.

11:30 AM PANEL DISCUSSION – TEST GENERATION

## SESSION 7: FUNCTION DESIGN TECHNIQUES

CHAIRMAN: **D. J. HUMCKE**, *BELL LABS, HOLMDEL, N. J.*

9:00 AM

**"A PROGRAMMABLE CONFIGURATOR"**

T. W. SIDLE, F. BEUGER, L. W. LEYKING AND A. G. LIVITSANOS, *BURROUGHS CORP., CITY OF INDUSTRY, CALIF.*

A program definition language is used to specify rules for translating a purchase order into the required set of hardware and software components.

9:30 AM

**"SPECULATIONS ON THE FUTURE OF DESIGN AUTOMATION"**

S. Y. H. SU, *CITY UNIVERSITY OF NEW YORK, NEW YORK, N. Y.*

The future direction of the use of design automation for designing and developing digital data processing systems and hardware is highlighted. Some of the unresolved problems are indicated and some thoughts toward resolving them are suggested.

10:00AM

**"AN EXPERIMENTAL COMPARISON OF FORCE DIRECTED PLACEMENT TECHNIQUES"**

D. C. WILSON AND R. J. SMITH, II, *SOUTHERN METHODIST UNIVERSITY, DALLAS, TEXAS*

Significant differences are noted in the computational efficiency of the algorithms compared and in the relationship of the placement solution to the routability of a board.

## SESSION 7: FUNCTION DESIGN TECHNIQUES

11:00 AM

**"A TOOL FOR COMPUTER DESIGN"**

H. WEBER, *IBM, BOBLINGEN, GERMANY*

This paper critically analyzes the development process. It covers methods which keep the function of the system being developed invariant.

11:30 AM

**"TRANSMISSION LINE MODELS FOR TRANSIENT ANALYSIS"**

S. J. GARRETT, *UNIVERSITY OF SOUTH FLORIDA, TAMPA, FLORIDA*

A method of incorporating a model of any two conductor transmission line in terms of a SCEPTRE transient analysis problem is described. Several examples are used, and their computer response is compared with actual results.

## SESSION 8: ARCHITECTURE

CHAIRMAN: **E. E. DUDNIK**, *UNIVERSITY OF ILLINOIS, CHICAGO, ILL.*

**1:30 PM**

**"PROGRAM PLANNING FOR NEW TOWN DESIGN PROBLEMS"**

M. LOS, *UNIVERSITY OF PENNSYLVANIA, PHILADELPHIA, PA.*

This paper formalizes the new town design problem as a problem in combinatorial programming, describes computer algorithms designed to solve it and reports computational experience.

**2:00 PM**

**"OPTIMAL POLYOMINO MAPS"**

H. B. SHAPIRA, AND R. S. FREW, *YALE UNIVERSITY, NEW HAVEN, CONN.*

The procedure for generating an optimal polyomino from a given set of preferences and the creation of a variably proportioned rectilinear map from that n-celled animal is described.

**3:00 PM**

**"A COMPUTER AIDED LAND USE STUDY TECHNIQUE"**

E. E. DUDNIK AND W. SCHACHTEL, *UNIVERSITY OF ILLINOIS, CHICAGO, ILL.*

This paper describes a computer-aided decision-making technique by which site evaluation with respect to land use can be made.

**3:30 PM**

**"INTERACTION, INTERFACES, AND DESIGN"**

J. S. GERO, *UNIVERSITY OF CALIFORNIA, BERKELEY, CALIF.*

Many design processes are iterative in nature and require extensive designer/computer interaction. As an experiment in interactive architectural design, four basic interactive functions were implemented in APL. These functions are described and their conversational use illustrated.

## SESSION 9: SIMULATION

CHAIRMAN: **S. Y. H. SU**, *CITY UNIVERSITY OF NEW YORK, NEW YORK, N. Y.*

**1:30 PM**

**"A MINICOMPUTER-BASED LOGIC-FAULT SIMULATOR"**

M. FLOMENHOFT AND B. M. CSENCSITS, *BELL LABS, ALLENTOWN, PENNSYLVANIA*

A unit-gate-delay three-valued-logic parallel fault simulator handles up to 1500 gates on a minicomputer with 16K core. Capabilities, programming novelties, and performance statistics will be presented.

**2:00 PM**

**"FUNCTIONAL TESTING OF LSI GATE ARRAYS"**

G. VAUGHN, *MOTOROLA INC., MESA, ARIZ.*

This report is a description of the problems encountered while functionally testing LSI gate arrays in a production environment and some solutions we are implementing for these problems.

**3:00 PM**

**"TIMING ANALYSIS FOR DIGITAL FAULT SIMULATION USING ASSIGNABLE DELAYS"**

E. W. THOMPSON, S. A. SZYGENDA, N. BILLAWALA, AND R. PIERCE, *UNIVERSITY OF TEXAS, AUSTIN, TEXAS*

This paper presents implemented techniques for timing analysis, and termination of fault induced activity, within an assignable delay digital fault simulation environment.

**3:30 PM** PANEL DISCUSSION – SIMULATION

## SESSION 10: GENERAL APPLICATIONS

CHAIRMAN: **J.G.BRINSFIELD**, *BELL LABS, WHIPPANY, N. J.*

**1:30 PM**

**"A COMPUTER AIDED SYSTEM FOR THE DESIGN, MANUFACTURE AND TEST OF DIGITAL PRINTED CIRCUIT BOARDS"**

R. J. SUMMERS, *WESTINGHOUSE ELECTRIC CORP., BALTIMORE, MD.*

A Computer Aided System (CAS) for the design, manufacture, and test of printed boards containing digital circuits is described. Along with a walk through of the system, the cost savings and production increases obtained are indicated.

## SESSION 10: GENERAL APPLICATIONS

**2:00 PM**

**"COMPUTER AIDED SHIP DESIGN AT THE MARITIME ADMINISTRATION"**

A. H. WOODYARD, *U. S. DEPT. OF COMMERCE, WASHINGTON, D. C.*

Organization of the computer aided ship design process is detailed, illustrating input and output with a sample design. Design verification of certain phases of the design process is treated using graphical aids.

**3:00 PM**

**"RTL – THE FIRMWARE DESIGN AUTOMATION SYSTEM"**

R. L. HASTERLIK, *HONEYWELL INFORMATION SYSTEMS INC., BELLERICA, MASS.*

A system to control design and development of a microprogrammed device is summarized. Documentation of the design, simulation of the firmware, and assembly of the firmware are system facilities.

**3:30 PM**

**"AUTOMATED SIGN DESIGN AND STENCIL CUTTING SYSTEM"**

W. M. BARNES, *COMPUTER TALK, INC., IDLEDALE, COLO.*

A real-time minicomputer system for sign design, stencil making, payroll and time keeping, file management, font design, maintenance and hardware diagnostics is presented.

**5:00 PM** COMMON INTEREST GROUP MEETINGS
INTERCONNECTION
SOFTWARE DA
SIMULATION AND TEST GENERATION
ARCHITECTURE

## *WEDNESDAY, JUNE 19*

8:00 AM

**INTERCONNECTION TUTORIAL**

D. W. HIGHTOWER, *BELL LABS, HOLMDEL, N. J.*

## SESSION 11: INTERCONNECTION

CHAIRMAN: D. W. HIGHTOWER, *BELL LABS, HOLMDEL, N. J.*

9:00 AM

**"AN ITERATIVE TECHNIQUE FOR PRINTED WIRE ROUTING"**

F. RUBIN, *IBM CORP., POUGHKEEPSIE, N. Y.*

This paper describes an iterative method of routing which tries to avoid crossings and path adjacency while simultaneously controlling path length.

9:30 AM

**"A PROGRAMMABLE PRINTED WIRING ROUTER"**

C. S. SLEMAKER, R. C. MOSTELLER, L. W. LEYKING AND A. G. LIVITSANOS, *BURROUGHS CORP., CITY OF INDUSTRY, CALIF.*

This paper describes a cost function which helps a Moore-Lee router avoid finding paths that block unwired access pins.

10:00 AM

**"A SYSTEM FOR MULTI-LAYER PRINTED WIRING LAYOUT"**

J. C. FOSTER AND R. L. CALAFIORE, *BELL LABS, WHIPPANY, N. J.*

An interactive design station for routing multi-layer backplanes is described. The system uses a digitizer/plotter, storage scope and standalone computer. The overall philosophy and goals are explained.

## SESSION 12: LARGE SCALE SYSTEMS

CHAIRMAN: **R. TAYLOR**, *NICD, WASHINGTON, D. C.*

9:00 AM **"IPAD 1"** C. GARROCQ, *GENERAL DYNAMICS*

9:30 AM **"IPAD 2"** R. MILLER, *BOEING CORP.*

The IPAD 1 and IPAD 2 presentations concern NASA's activities in Design Automation for aerospace vehicle design.

10:00 AM

**"DESIGN AUTOMATION IN PRELIMINARY DESIGN"**

D. E. TIPPING, *MARTIN MARIETTA, ORLANDO, FLA.*

Preliminary design of tactical weapons systems using interdisciplinary computer aids provides insight into any automated preliminary design activity. The necessary attributes of these design automation tools is discussed.

## SESSION 13: SOFTWARE

CHAIRMAN: **J. SHERMAN**, *IBM CORP., SAN JOSE, CALIF.*

11:00 AM

**"GERMINAL: TOWARDS A GENERAL AND INTEGRATED SYSTEM FOR COMPUTER AIDED DESIGN"**

R. JACQUART, P. REGNIER AND F. R. VALETTE, *CERT/DERI COMPLEX AEROSPATIAL, TOULOUSE CEDEX, FRANCE*

GERMINAL is a system of tools for a project from conception to the finished product. Standard procedures, adding devices and management of the devices are discussed.

11:30 AM

**"USING SIMULATION TO EVALUATE SYSTEM PERFORMANCE"**

E. K. BOWDON SR., *UNIVERSITY OF ILLINOIS, URBANA, ILL.*

Effects of job scheduling algorithms on computer system performance and resources are demonstrated and evaluated by a simulation model of a hypothetical, graphically distributed network computer.

## SESSION 14: DESIGN SYSTEM NEEDS

CHAIRMAN: **C. E. RADKE**, *IBM CORP., POUGHKEEPSIE, N. Y.*

11:00 AM

**"INITIAL DESIGN OF AN ADVANCED DA SYSTEM"**

M. A. BREUER, AND A. D. FRIEDMAN, *UNIVERSITY OF SOUTHERN CALIFORNIA, LOS ANGELES, CALIF.*

This advanced DA system is intended to be capable of highly interactive design. It has several unique features which will greatly enhance the possibilities of automatic design which is superior to that of the design engineer.

11:30 AM

**"ENGINEERING DATA MANAGEMENT SYSTEM (EDMS) FOR COMPUTER AIDED DESIGN OF DIGITAL COMPUTERS"**

M. SOGA, C. TANAKA, K. TABUCHI, K. SEO, M. KUNIOKA, AND H. TSUJI, *MITSUBISHI ELECTRIC CORP., KANAGUWA, JAPAN*

This paper describes an automated design system with a data base constructed by the general data base system capable of handling network structure and its DA programs.

**1:30 PM**

**PANEL DISCUSSION – "THE FUTURE AND HISTORY OF DESIGN AUTOMATION"**

PANELISTS: DA WORKSHOP COMMITTEE AND SESSION ORGANIZERS

**3:30 PM**

**"CRITIQUE OF THE ELEVENTH ANNUAL DESIGN AUTOMATION WORKSHOP"**

# GAZELLE

## AN INTERACTIVE GRAPHIC LOGIC DESIGN SYSTEM

As presented at ACM '73, Atlanta, Ga., on August 29, 1973 by:

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International Business Machines Corp., Kingston, New York 12401

## INTRODUCTION

The "Gazelle" system is composed of a group of programs developed as tools* to aid the design engineer in the creation, simulation, analysis and test generation of digital logic. Gazelle is designed for use on an IBM 1130 computing system running under the "GLEAM" (Reference #1) multitask operating system. An IBM 2250 display console provides the engineer with the ability to interface with the computer in his development and simulation of a logic circuit.

The Gazelle system presents the same general format that has been used on machine printed logic sheets; one that the user is already familiar with. The logic page may be composed of from one to ninety-one logic blocks, from one to ninety-one left-edge connectors, from one to ninety-one right edge connectors, and wires to join the connectors and logic blocks to perform specific logic functions. The logic blocks are actually "macro" blocks, which represent circuits composed of the logic functions AND, OR, NOT, and DELAY.

The display light pen is used to perform operations upon logic circuits displayed on the screen. Information may also be added to the display by typing at the display console keyboard.

Gazelle is composed of many individual program phases which perform functions of the system. The selection of a phase is accomplished via the display and light pen. Each phase provides one or more functions which may be chosen by selecting the name of the function on the screen with the light pen.

*NOTE: This application program is an IBM internal tool and is not available for outside distribution.

## PHASES

The major phases of GAZELLE are:

Control is the prime hub of the GAZELLE program and is the initial display panel which the user sees (refer to Figure #1). In this phase the design number is determined and the next phase is selected.

Circuit is selected by the design engineer (see Figure #2) for designing "macro" logic blocks from the basic logic functions (AND, OR, NOT, DELAY, ETC.) or from combinations of existing macro logic blocks (see Figures #3 and #4). These circuits are retained in a special circuit library file for subsequent reuse.

Design is selected to design or alter logic pages using the same basic format as the machine printed logic sheets see Figure #5). These pages are composed of (macro) logic blocks, left-edge and right-edge connectors, and wires connecting these blocks and edge connectors.

Detail may be selected from the Design phase. It provides a means for entering title, logic block, (see Figure #6) left-edge and right-edge connector textual information via the display's alphameric keyboard.

New Page operation permits creating a new logic page and page number for an existing design.

COPY operation is used to create new logic pages from pages which already exist in the Gazelle logic files.

File is an operation which saves the circuit and detail information for the in-process logic page. This page becomes the "latest level" for this design.

DA-LINK is a means of interfacing with a central computer system (S/360 or S/370) via RJE/RJP or the SBCU. This phase includes a JCL compiler that generates a customized job control deck from user-supplied variables (see Figure #7).

-TDG- or Test Data Generation provides various features that enhance the basic simulation capabilities, and interface with the host system's test generation facilities (see Figure #8).

Simulation allows the designer to exercise the circuit functions on a logic page (see Figure #10) or card (see Figure #11). Values of "0", "1", "X" and "*" may be applied to the input pins (left-edge connectors) of the logic and the resultant value of each line will appear at the output pin of the logic block which is the source of that line. The resultant values are determined by Gazelle according to the mode of simulation the designer has selected. One of these enchancements is the "scope" feature which provides multibeam oscilloscope images of the simulation output (see Figure #9).

Activate will activate the circuits used in the selected Design and will list any circuits not defined in the Circuit Library.

Ckt-List will list all circuits used in the selected Design and provide a "where used" cross-reference table.

## FEATURES

This logic layout and evaluation system is designed to operate on the IBM 1130 computing system. The purpose of this family of programs is to provide a design engineer with a means of evaluating his design, via the 2250 display, prior to committing it to hardware. The system takes care of the many control and bookkeeping tasks that an overworked designer often resents and sometimes disregards:

The major features of this system are:

1. Graphic Access: The designer may have immediate access to his design files via the 2250 display console. He may display, plot or edit the file content. He may also reference various shared files in the same manner.

2. Multitasking: The application utilizes the GLEAM/1130 Multitask Control Program which permits the concurrent execution of several task programs. This feature allows natural interaction between man and machine for the creation and analysis of a design, yet provides a reasonably steady workload for the system.

3. Macro Facility: The designer can group collections of elemental (or micro) blocks (AND, OR, NOT, ETC.) and define a macro (for example a register stage), then design logic using both macro and micro blocks. The design may be saved on a disk file for later recall.

4. Design Control: Design files are maintained and updated by the file management routines within the 1130 system. The logic design data will be automatically reformatted for input to the existing Design Automation processors.

5. Logic Simulation: An interactive ternary timing simulator is available for establishing "good machine responses". Using this system, it is possible for the designer to sit at a 2250 display and determine if the logic does indeed perform the desired function. It is also possible to examine the performance of a logical network when variable delays are encountered on "parallel" lines. An option is provided to operate in binary mode (as a two-valued simulator) for improving run time.

6. Fault Simulation: A ternary fault simulator is also available for examining the effect of "stuck at 1" or "stuck at 0" faults in the logic.

7. Logical to Physical Transformation: The logic diagram is automatically converted to a physical form showing the logical point to point nets. This display is used to layout components with an eye toward simplification of wiring patterns. After component placement has been optimized the nets are formed into the actual wire paths.

8. Artwork Generation: The wire file is interpreted by a task which drives on-line plotting devices to produce artwork masters or numerical control tapes for device fabrication.

9. Remote Job Entry: Information is transmitted-to (and received-from) S/360 or S/370 via "RJE/RJP" over switched, voice-grade telephone lines, allowing the S/360 to also serve the designer. A high-speed coaxial line may also be used to interconnect the 1130 to an on-site S/360, S/370 via a Sensor Based Control Unit (SBCU).

The advent of medium and large scale integration has increased the cost of change. It is now imperative that the hardware function correctly the first time, or else the design costs and attendant delays become unbearable.

The designer can now create, evaluate and initiate the release procedures on a small system which has desirable facilities, capabilities, and cost attributes.

## MODES OF SIMULATION

Three modes of simulation exist within the GAZELLE simulator. With each of the modes, the delay blocks (D*) used to define higher level macros are taken into consideration. This means that if no delay blocks are used in a definition, a zero-delay simulation will occur. If one delay block is used in each function, unit-delay simulation will occur. When different number of delay blocks have been used in different functions, a variable delay simulation will occur. The more realistically the delays have been assigned to the function, the more realistic the simulation will become.

Also, for each of the modes, any of the four values of 0, 1, X or * can be applied to an input and simulated. 0 and 1 are binary values; X is the "unknown" or transition state between 0 and 1; * is "don't care" and acts as if the line doesn't exist at all.

Upon initial entry to the simulator and after reset, the active logic is set to the -X- or uninitialized state. The untied lines are set to the pre-selected untied line state, which can be any of the four values indicated above.

### 0-X Mode:

The significant characteristic of this mode is that state change within a function is assumed to occur instantaneously. Delay is considered if delay blocks have been used to define the function. The change from one state to another is assumed to always be known. Therefore, an -X- is not inserted during the change.

### 1-X Mode:

During simulation in the 1-X mode, a state change is assumed to go through a transition period of one unit of time (one unit of delay). The propagation of this unknown or transition state will cause certain loops to be set to the -X- state indicating a potential race or hazard condition.

### INF-X Mode:

For this mode, the transition from one state to another is assumed to take an infinite period of time. In actual usage, when a transition occurs, an -X- is applied to a line and allowed to propagate until stabilization occurs. This causes all "feedback" loops to be set to -X- before propagation of the intended signal. Wherever the -X- state would control a latch, the -X- will remain, indicating a potential race, hazard or oscillatory condition.

In general, the "0/X" mode is optimistic in that it will not indicate race or hazard conditions and "INF/X" is very pessimistic, indicating possible problem areas that in reality will not be problem areas. The "1/X" mode will be found to be the most useful and closely approximate actual hardware operation. This is the default mode upon initial entry to the simulator.

## FAULT SIMULATION

The Fault Simulator provides the user with a tool for applying a "stuck" condition on any line within the logic, simulating that "stuck condition and holding the value at the "stuck" level while other simulations are progressing.

To apply a value to a line, select FAULT (the option -FAULT- appears on the Page panel). FAULT will change to STICK, indicating that the option is active. The next line selected will be stuck at the level currently indicated by the "boxed" value. (The left edge lines of the page cannot be "stuck".) When a line has been "stuck" a diamond ( ) will appear around the line value and the option STICK will change to STUCK. If a simulation is performed at this point, the "stuck" value will be actively propagated and the results allowed to stabilize.

To "un-stick" a line, select STUCK. The word STUCK will change to FAULT and the diamond around the "stuck" value will be removed. If a simulation has not been performed so that the "stuck" condition has not been propagated, selecting STUCK will cause the previous line value to re-appear on the line. Selecting STICK will also cause a return to the FAULT word.

It should be recognized that application of the Fault feature can produce logic states that have not been caused by changes to P/I's. Care must be taken to recognize what effects, if any, the application of the Fault has had and not to confuse these changes with those that occur as a result of normal pattern propagation. Note also that RESET will not remove the "stuck" condition unless the option STUCK has been changed to FAULT.

The Fault Simulator is used to evaluate the effectiveness of the test patterns that have been generated, by observing the difference in the simulation results between the "good machine" and the "fault machine".

## SCOPE

SCOPE is an option on the test data generation (TDG) panel which converts the users simulation patterns into a thirty-one beam oscilloscope pattern on the display (see Figure #9). This option makes it possible for the user to immediately inspect any selected area of his simulation run. The user selects the lines to be "scoped" by having the scope line selector display the desired page, then selecting the desired net with the light pen. A flag (*) will be displayed on the chosen set. To deselect a previously chosen net, the user triggers the light pen on the flag (*). A pattern/time scale is provided on the display for the users convenience. He can use this scale to check values on one line against the values on any other line for the same pattern/time frame. In a situation where there is an unusually great amount of activity, it may not be possible to display the entire simulation run at one time. SCOPE will however display as much as it possibly can, and the user can scroll the display as he desires. All four simulation values are displayed; "0", "1", "X" (unknown), and "*" (don't care).

## CONCLUSIONS

A relatively small computing system can assist the engineer in performing logic design, simulation and test data generation.

Graphic computer-aided design methods improve the man-machine relationship. The combination of a small computer, disk storage units, high performance display, low cost on-line plotter and unit record I/O devices offer significant benefits to the user.

Even the small-sized system is enhanced by a multitasking operating system. The major benefit realized is accessability for the user. Any nonbusy facility can be immediately accessed by the designer; he doesn't need to wait for the current computer job to complete. The multitasking program attempts to keep all devices operating full time, thereby offering better system utilization.

Remote Job Entry (RJE) to a larger computer system via the telephone network or at higher speeds over dedicated coaxial cables allows the small system to handle extremely large designs for the user. The graphic system operates as a satellite to the larger system, providing the user with a power input/output facility, as well as performing some local computation; and the larger host system provides the main data base and performs the heavy computation which might be required. This distributed computing philosophy appears to be an optimum way to support computer aided design.

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# G A Z E L L E  LOGIC CONTROL

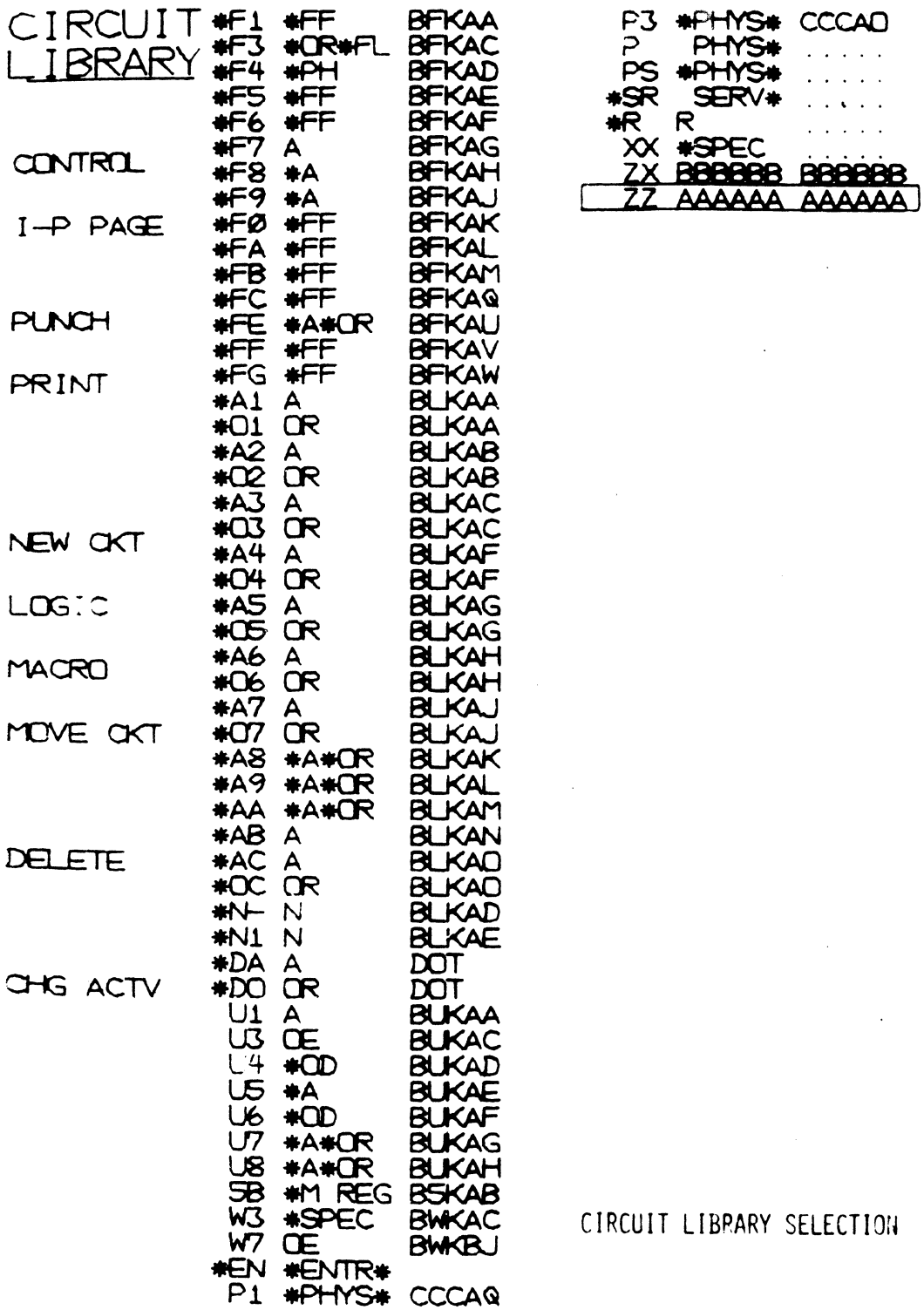
CART 9085 CART 2842 9115 9093 9071 6810
2509 2497 2513 2953 9831

CKT LIST
ACTIVATE
CIRCUIT

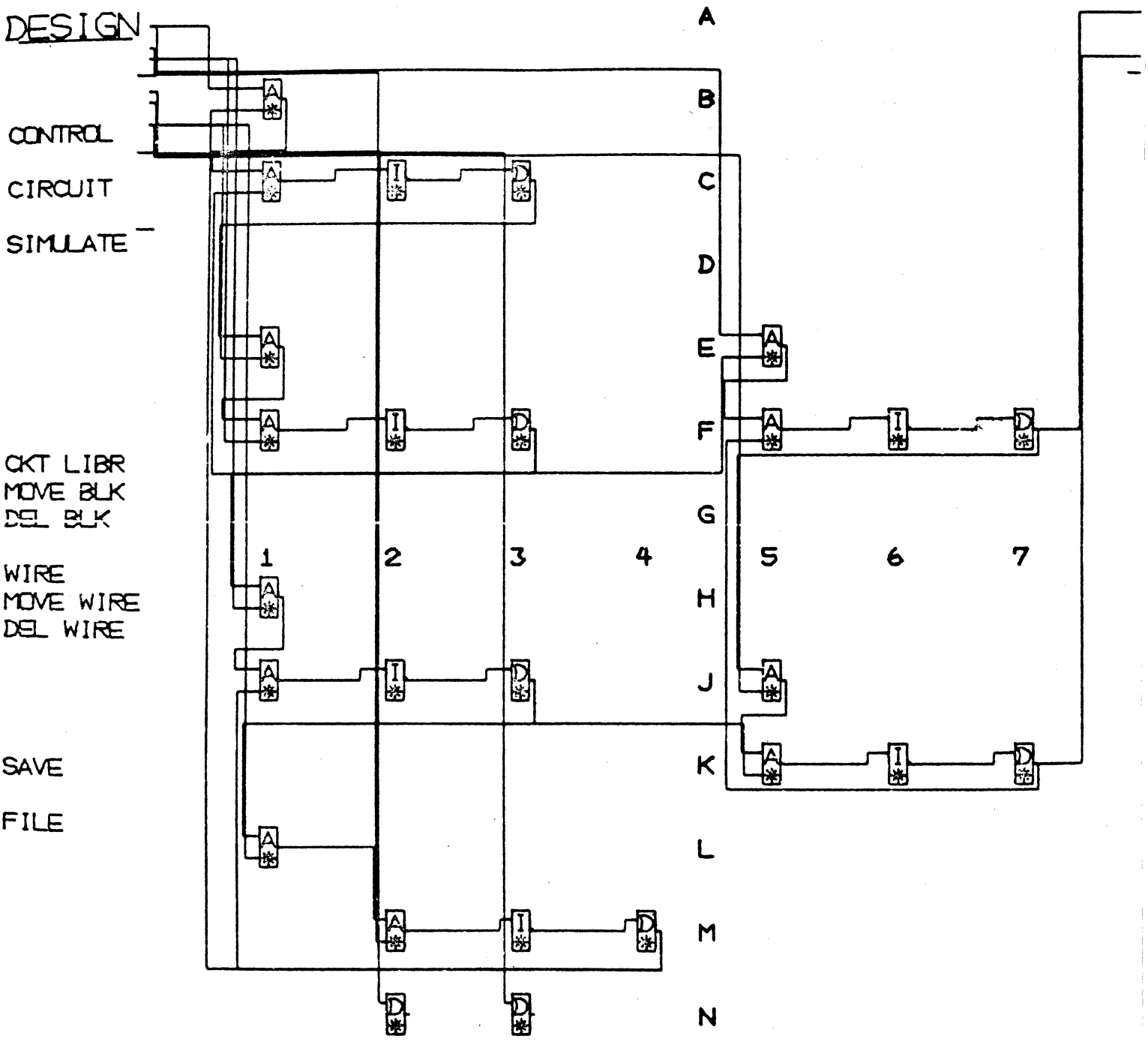
IN-PROCESS 9115-3 ←FILE

GAZELLE CONTROL PANEL (FIGURE 1)

LOGIC — PHYSICAL — D/A CARD
DESIGN NEW PAGE COPY PRINT PLACE WIRE LINK SIM -TDG-




CIRCUIT LIBRARY SELECTION (FIGURE 2)




MICRO-LOGIC CONSTRUCTION OF MACRO (FIGURE 3)

RESTART

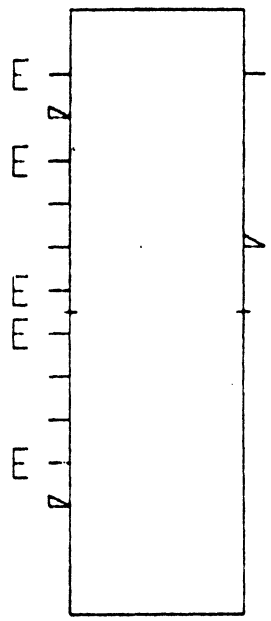
MACRO

CONTROL

DESIGN

CIRCUIT

FILE



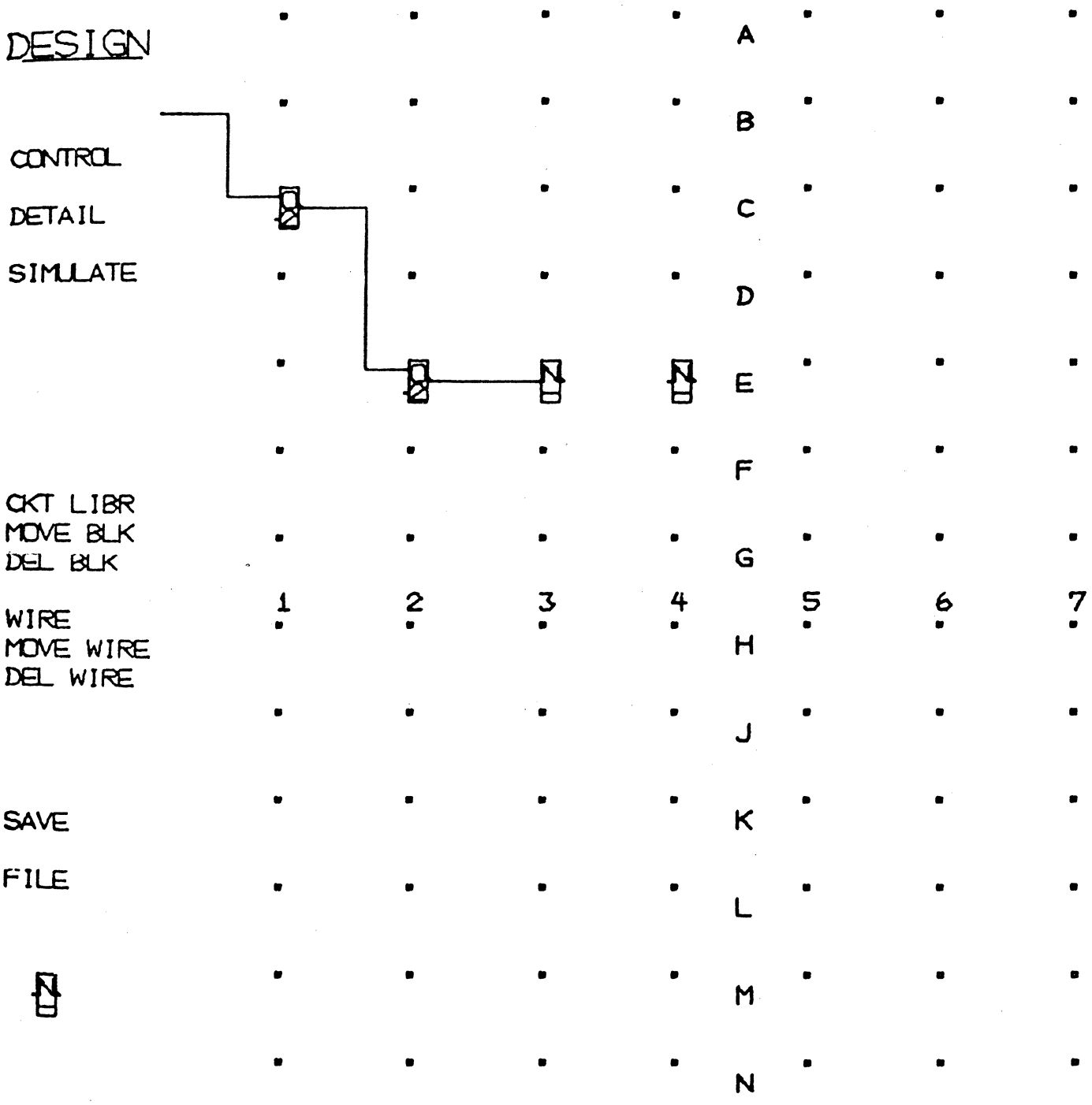
CIRC FUNC (ALD I
*OR*FL

CIRC TYPE (ALD I
BF-KAC

GAZELLE NAME
F3

ALTERNATE BLOCK
1 2 3 4

MACRO LOGIC BLOCK (FIGURE 4)




LOGIC DESIGN (FIGURE 5)

LISTED BLK RESTART

DETAIL

CONTROL

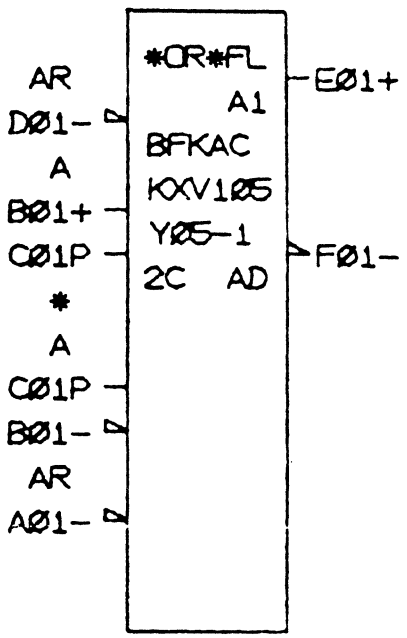
DESIGN

FILE

CIRCUIT

LOGIC

*CANCEL*=
NEXT ONE




DETAIL OF LOGIC BLOCK (FIGURE 6)

```
**** UPDATE LMT FROM GAZELLE ****

JOB NAME  ACEGD6                USER NAME  WG SMITH
PROBLEM NUMBER  123456    DEPT  720    BLDG  005

TODAY'S DATE  MONTH  06    DAY  08    YEAR  73


A2 TAPE NUMBER  K1234
DA RUN NO   123      DA CYCLE NO   321

RUN TYPE   C     'C' = CHANGE   'N' = NEW DESIGN
```

INTERFACE TO CENTRAL DA SYSTEM (FIGURE 7)

| | | | OUTPUT | | |
|---|---|---|---|---|---|
| CONTROL | RESTART | LIST-PROTO | QUE | PRINT | PUNCH | RJE |

-TDG- D/N 9085

| | |
|---|---|
| CONTROL | SCOPE |
| SIMULATE | TEST PATTERNS |
| DESIGN | GIF/BUGLIST |
| ALL EVENTS | TITES CONTROL |
| STORE SAVED PATTERNS | RELEASE SAVED PATTERNS |
| MYDAS | |

---

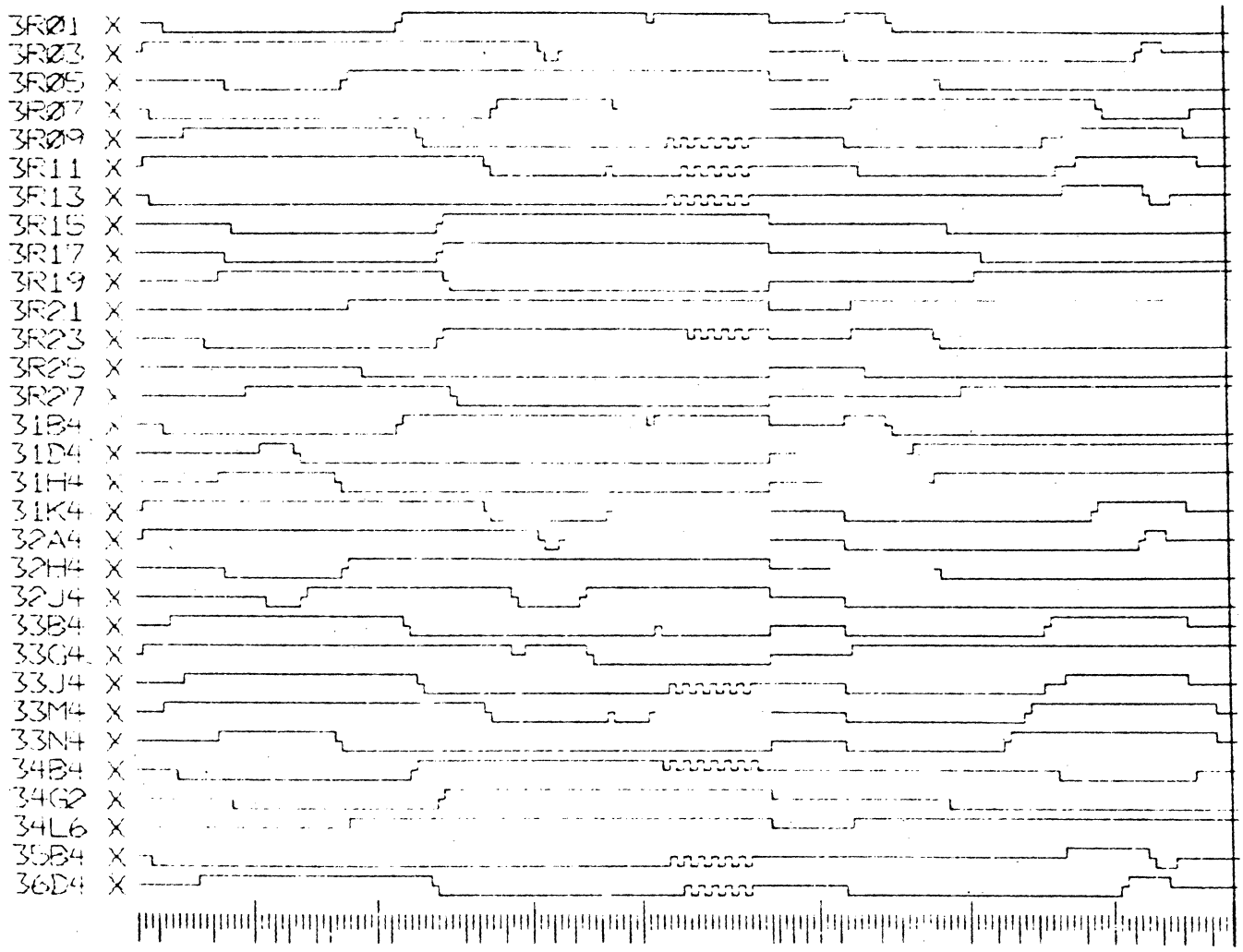
SELECT

- LIST
  - STORE FILE
  - EDIT FILE
- REPLAY
- EDIT
- SAVE SIM
- RESET SIM

TEST DATA GENERATION CONTROL (FIGURE 8)

PATTERNS FOR D/N 9085 PG 3

PATN Ø. Ø
TIME Ø. Ø

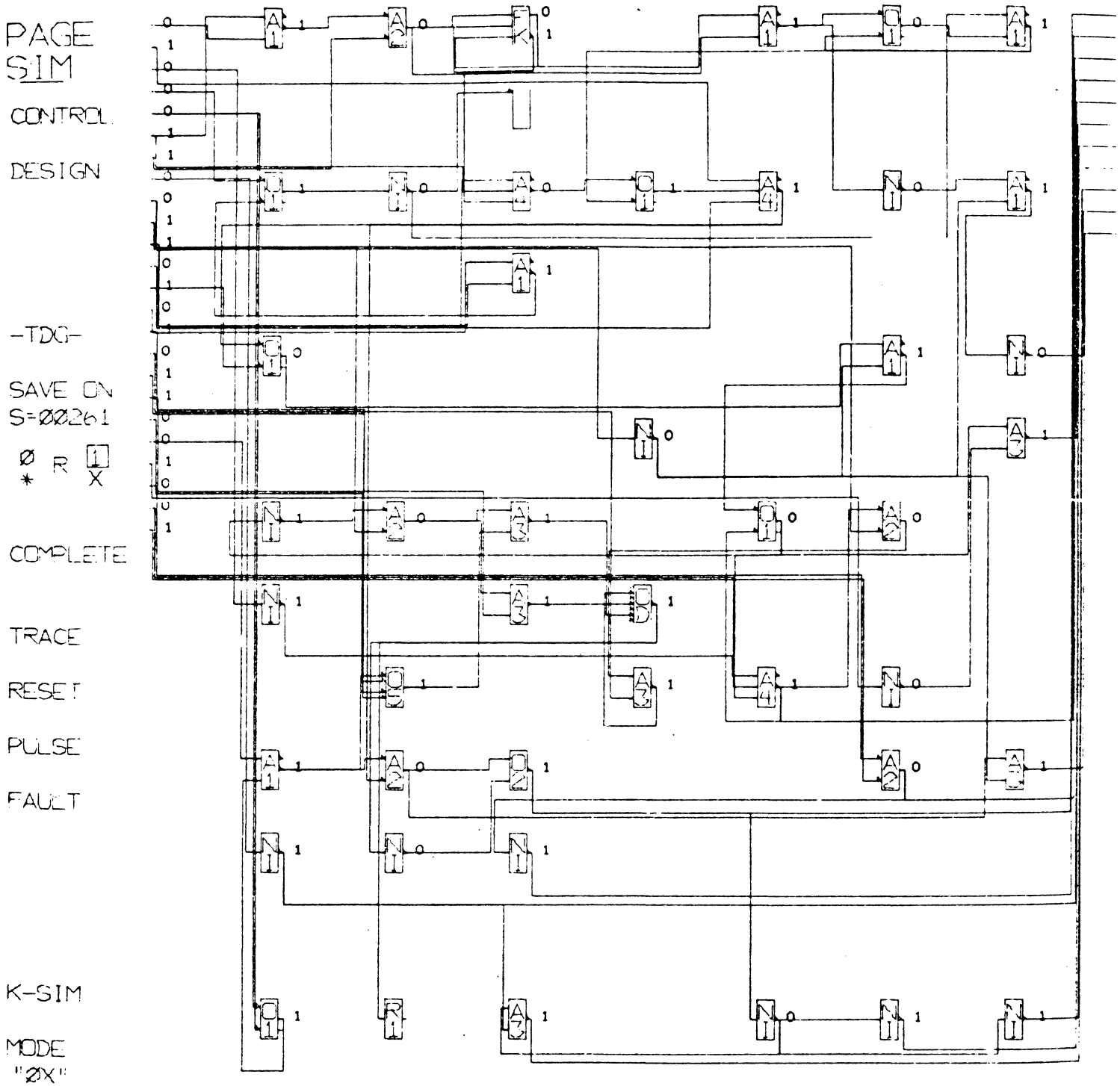



RESELECT
PATTERNS

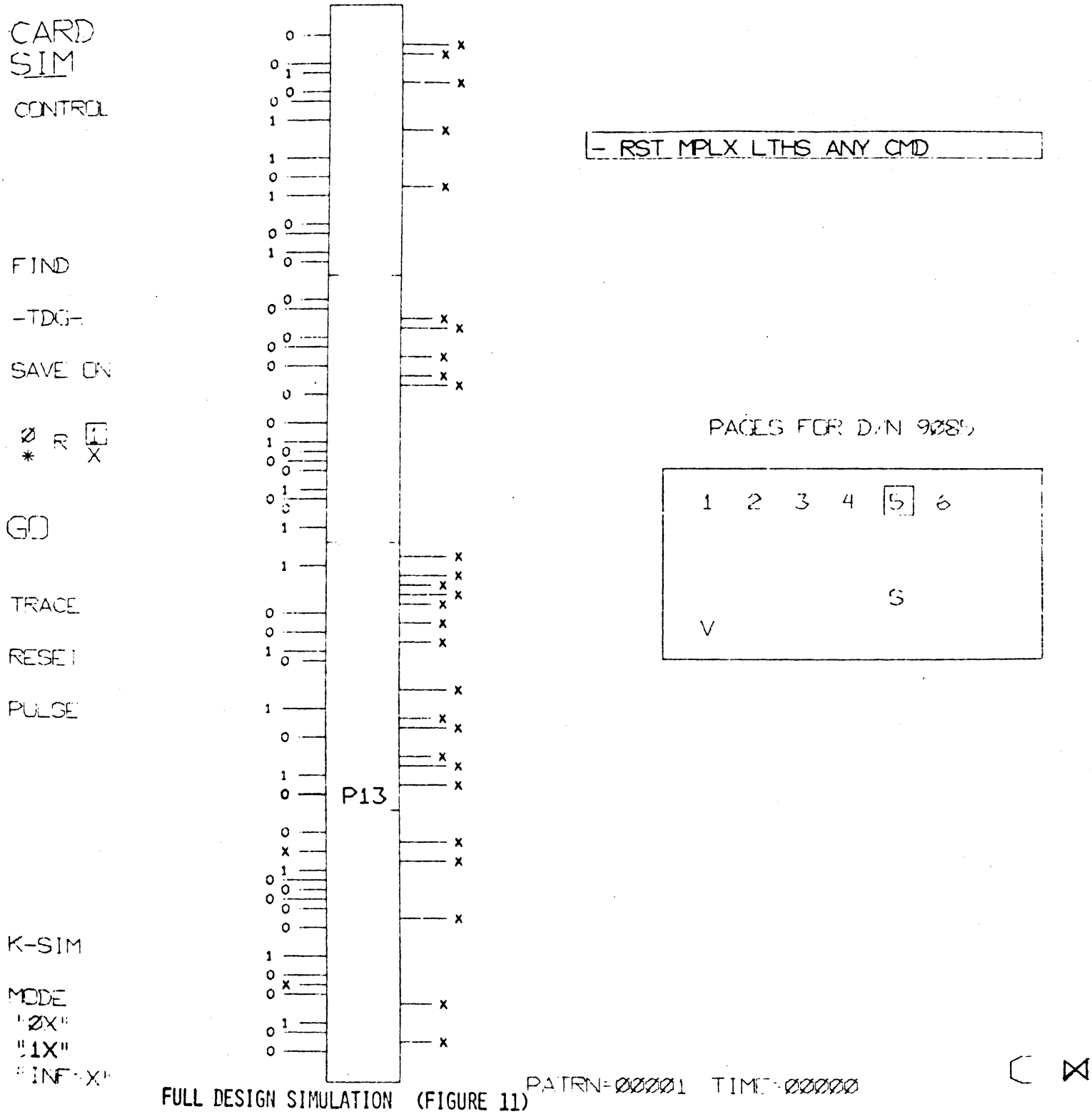
SCOPE PRESENTATION OF SIMULATOR OUTPUT (FIGURE 9)

TDG

SCALE - 5.




PAGE SIMULATION DISPLAY (FIGURE 10)
PATRN=00002 TIME=00006




FULL DESIGN SIMULATION (FIGURE 11)

# Bibliography on Algorithms for Shortest Path, Shortest Spanning Tree, and Related Circuit Routing Problems. (1957-1973)

by

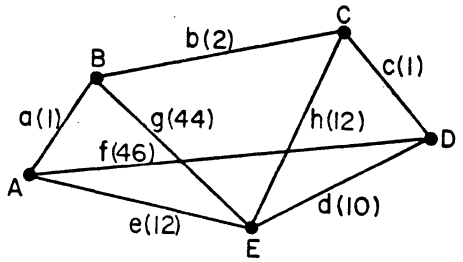
A. R. Pierce

Bell Laboratories
Murray Hill, N. J.

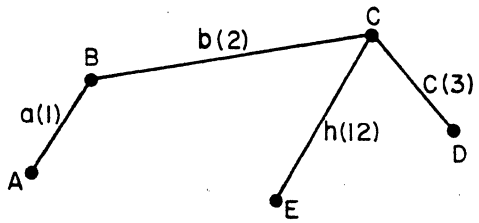
This bibliography contains over 300 references on algorithms and machine calculation techiques for solving the shortest path, k-th shortest path, and shortest spanning tree problems. Chapter 1 - Paths and Circuits - is divided into 4 sections, dealing respectively with shortest path, optimal path, Traveling Salesman and other related algorithms. Chapter 2 deals with spanning trees and chapter 3 covers the CAD of electronic systems that utilize minimum path or shortest tree algorithms.

These minimum cost problems enjoy a wide application in many different areas. Kruskal and Prim gave early methods for calculating shortest spanning trees. Other algorithms and numerous applications were soon to follow. For example, Lee's algorithm is frequently used to route printed circuit boards. Other best path calculations are used in highway research and planning. It is to be noted that wide applicability results because other variables such as "reliability", "flow", and "cost" can be used instead of "distance".

We now give some examples of the terms used. The length of a graph G, having edges of length $l(i,j)$ between vertices i and j, is $L(G)=\Sigma l(i,j)$, where the summation is over all edges. Consider the graph G below:




A path (A,D) is any of the subgraphs {abc} or {ed} or {f} or ... . The path {abc} is the "shortest" path, {ed} is the 2nd shortest path, ... , kth shortest path.




A subgraph spans a graph if it includes all the vertices of the graph. A subgraph is a tree if it is connected, and if removal of any edge makes it disconnected. Thus a spanning tree is a connected subgraph which includes all the verticies of the graph, and which is disconnected by removal of any edge. The tree t - pictured above - is the shortest spanning if the length l(t) is the minimum length of all spanning trees T of G. Frequently shortest or "minimum" (length) trees are referred to as mimimal trees.

A circuit is a path whose initial and final vertices are the same, but which otherwise never goes through the same vertex twice. The Traveling Salesman Problem is to determine a minimum spanning circuit of a graph.

Illuminating discussions with J. B. Kruskal, who provided some of the above examples, D. W. Hightower, and C. J. McCallum are gratefully acknowledged. Reviews and bibliographies by Dreyfus (1969), Frank and Frisch (1971), Pape (1969), and Wilson and Smith (1973) provided many useful references.

## CHAPTER 1 PATHS AND CIRCUITS.

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