acm

SIGDA NEWSLETTER

SPECIAL INTEREST GROUP ON DESIGN AUTOMATION

Volume 5 Number 2 June 1975

Contents:

ADDRESSES

CHAIRMAN:
Charles E. Radke
IBM Corporation (B99/951)
P. O. Box 390
Poughkeepsie, New York 12602
(914) 485-7775

VICE-CHAIRMAN:
David W. Hightower
Bell Labs 2B312A
Holmdel, New Jersey 07733
(201) 949-6549

SECRETARY/TREASURER:
Lorna Capodanno
Bell Labs 2C169
Murray Hill, New Jersey 07974
(201) 582-6909

EDITOR:
Robert J. Smith, II
P. O. Box 1028
Livermore, California 94550
(415) 447-1100 x 8053

TECHNICAL COMMITTEE:
David W. Hightower, Chairman

MEMBERSHIP COMMITTEE:
Lorna Capodanno, Chairman

PUBLICITY COMMITTEE:
Lorna Capodanno, Chairman

BOARD OF DIRECTORS:

John R. Hanne
Texas Instruments
P. O. Box 5012 (MS 907)
Dallas, Texas 75222
(214) 238-3554

Steven A. Szygenda
Department of Elec. Eng.
University of Texas
Austin, Texas 78712

Donald J. Humcke
Bell Labs 2C-318
Holmdel, New Jersey 07733
(201) 949-6253

Larry Margol
Micro Electronics Division
Rockwell Instruments
D/734-057
Box 3669
Anaheim, California 92803
(714) 632-8565

Charles W. Rose
Computing & Information Sci.
Case Western Reserve Univ.
Cleveland, Ohio 44106
(216) 368-2800

MEMBERSHIP

SIGDA dues are $3.00 for ACM members and $5.00 for non-ACM members. Checks should be made payable to the ACM and may be mailed to the SIGDA Secretary/Treasurer listed above, or to SIGDA, ACM Headquarters, 1133 Avenue of Americas, New York, N. Y. 10036. Please enclose your preferred mailing address and ACM Number (if ACM member).

SIG/SIC FUNCTIONS

Information processing comprises many fields, and continually evolves new subsectors. Within ACM these receive appropriate attention through Special Interest Groups (SIGs) and Special Interest Committees (SICs) that function as centralizing bodies for those of like technical interests ... arranging meetings, issuing bulletins, and acting as both repositories and clearing houses. The SIGs and SICs operate cohesively for the development and advancement of the group purposes, and optimal coordination with other activities. ACM members may, of course, join more than one special interest body. The existence of SIGs and SICs offers the individual member all the advantages of a homogeneous narrower-purpose group within a large cross-field society.

ACTIVITIES

1) Informal technical meetings at SJSS and FJCC.
2) Formal meeting during National ACM meeting + DA Workshop.
3) Joint sponsorship of annual Design Automation Workshop.
4) Quarterly newsletter.
5) Panel and/or technical sessions at other National meetings.

FIELD OF INTEREST OF SIGDA MEMBERS

Theoretic, analytic, and heuristic methods for:

1) performing design tasks,
2) assisting in design tasks,
3) optimizing designs through

the use of computer techniques, algorithms and programs to:

1) facilitate communications between designers and design tasks,
2) provide design documentation,
3) evaluate design through simulation,
4) control manufacturing processes.

CHAIRMAN'S MESSAGE

CHARLES E. RADKE

ELECTIONS

I had hoped that in this issue I could report on the outcome of the elections for new SIGDA officers. In case you had not noticed there was a delay. The slate of candidates had to be realligned slightly. If you read your election ballots (and hopefully voted) you would see the following list:

Chairman:

Dr. James G. Linders	University of Waterloo
Dr. Charles W. Rose	Case-Western Reserve University

Vice-Chairman:

Dr. Edward Hassler	Texas Instruments
Ms. Judith Brinsfield	Bell Laboratories

Secretary/Treasurer:

Mr. Donald J. Huncke	Bell Laboratories
Dr. Luther Abel	Digital Equipment Corporation
Mr. Carl Ellison	IBM Corporation

DA CONFERENCE

I know all of you are planning to attend the 12th Design Automation Conference at Boston (June 23-25, 1975). I will see you there! But if you wish to specialize or just can't make the June conference, plan to attend one of the other Workshops SIGDA is sponsoring:

September 3-5, 1975, New York, New York, USA - "Workshop on Computer Hardware Description Languages and Their Applications."

September 15-16, 1975, Waterloo, Ontario, Canada - "Workshop on Data Bases for Interactive Design."

These conferences provide the dialogue that all of us need in order to regenerate our creativity, problem solving, and development activity required by our employers especially during competitive times. But, and I emphasize, "but", I hope that you come prepared to contribute as well as absorb. There is much to be gained - the conference and workshop committees do their part - and they depend upon you to do your part.

SIGDA will have an open forum on either Monday (June 23) or Tuesday (June 24) evening at the DA Conference. Please look at the posted announcements for date, time, and place. SIGDA has been growing and has been contributing more to Design Automation as a technical discipline. Join the officers, meet them, and give them your views on "Design Automation and the Professional Societies." We hope the election results will also be in at that time so I can introduce the new officers.

Remember SIGDA is your "Special Interest Group." There will be a table at which attendees can sign up as members of ACM and SIGDA. Encourage your colleagues to sign up.

SIGDA NEWSLETTER:

I have been receiving favorable comments on our recent issues of the SIGDA Newsletter. The thanks goes to our Editor, Rob Smith, and those who are contributing. Thanks.

C. E. Radke

FROM THE EDITOR

While preparing the copy for this number, I began to wonder whether the material in the last few issues has been worth sending out. Are recipients of the Newsletter at all interested in the seemingly handpicked stuff?

This is the fifth issue I've pasted together; there has not been a single scrap of contributed material rejected or delayed. If you want changes made, help make them: where have all of those volunteered contributions been sent? (Not to me!) After some minutes of glue pot and such thoughts, I concluded that maybe the present state of affairs represents some sort of balance: no controversy, limited readership feedback and four issues per year.

The next issue will contain a challenge: Chung Cao and I have been working on a technique for producing minimum Steiner trees for networks of arbitrary size. Unfortunately, we have not yet been able to prove minimality. We will present a hypothetically minimum solution to a randomly generated 26 point net, hoping to obtain a still shorter network from some interested reader.

Hope to see you in Boston at the DA Workshop. (Workshop program details start on the following page.)

Rob Smith

SUCCESSFUL MISSOURI SYMPOSIUM ON ADVANCED AUTOMATION

Of particular note was the Symposium on Advanced Automation on April 14-16, 1975 sponsored by the College of Engineering of the University of Columbia-Missouri and the Atlantic Richfield Company. The symposium, focusing on five areas of import to automation, comprised a fruitful combination of research, applications, statement of needs, and survey papers. The five sessions in the program were I Microprocessors in Advanced Automation, II Automation and Communications, III Graphic Arts Industry, IV Automatic Testing, and V Automation and Simulation. This range provided a much needed forum for the cross-fertilization of ideas between industries and universities, and also among industries themselves. Areas discussed included among others, industrial control, electronics manufacturing, electric utilities, communications, food processing, teaching, printing and publishing, and medicine. Among the many excellent presentations, this reviewer particularly enjoyed the following three:

W. Wade Davis, Bendix Corporation, "Application of Field Programmable Read-Only Memories to Asynchronous Sequential Logic Design with Redundancy and Fault Testing".

K. Pfahl, Hallmark Cards, "A Case History: Automation of Color Reproduction by Color Scanning".

R. A. Williamson, The Foxboro Company, "Computers and Intelligent Process Communications".

Published proceedings and/or video tapes of the symposium may be obtained from Dr. Frank P. Mathur, Bioengineering/Advanced Automation Program, College of Engineering, University of Missouri-Columbia, Columbia, Missouri, 65201.

A. J. Frank
Bell Telephone Laboratories
Murray Hill, New Jersey

12th Design Automation Conference at Boston

Statler Hilton Hotel——Boston, Massachusetts June 23 - 25, 1975

Registration Fee

	Advance Registration	Registration at Conference
ACM, IEEE members	$50	$60
Nonmembers	$60	$70
Students*	N/A	$20

This fee includes two luncheons, coffee service and one copy of the Conference Proceedings. Early registration is recommended. All advance registration forms must be received no later than June 6, 1975. After that date, registrations will be accepted at the Conference registration desk.

*Full time students with card identification can register only at the conference for $20. The fee includes admission to the sessions and one copy of the Conference Proceedings. Luncheon tickets may be purchased separately.

Sightseeing for All

DAC will be in Boston soon after the opening of its American Bicentennial celebration. Boston 200 will officially begin Patriot's Day, April 18, 1975 — the 200th Anniversary of the Battle of Lexington and Concord. In a program called Citygame, new trials and exhibits will be opened. The Freedom Trail, featuring 18th Century Boston, will be expanded to include a new Tea Party Path, highlighting the Brig Beaver II, a replica of one of three original Tea Party ships, and a museum now open to the public at the Congress Street Bridge. There will be a Black Heritage Trail; a Medical Trail; highlighting Boston's famous medical institutions as well as trails on Literature, Religion, Women in History, Commerce and Finance, and Visual Arts. A Green Trail will lead participants through Boston's parks and gardens. A Water Trail will emphasize the New England Aquarium, the waterfront and harbor and the Charles River, and a Children's Trail will feature sites of particular interest to children.

A Boston 200 Official Guide book ($1.50), a Boston 200 Pasport book of bargain coupons ($3.00), and a Boston 200 Official Map ($1.50) are available from Boston 200, One Beacon Street, Boston, Massachusetts, 02108. Sample copies of these sightseeing aids will be on display at the DAC registration desk.

Advance Registration

Advance registration closes June 6, 1975. After that date, registrations will be accepted at the Conference registration desk. Your check must accompany this form. Kindly mail the form with a check made payable to "1975 D/A Conference" to the Registration Chairman:

J. Michael Galey
IBM Corporation
RO6-61A
Monterey and Cottle Roads
San Jose, California 95193

Name (last name first) _____

Company _____

Address _____

City/State _____

Zip _____

Use this form or facsimile for advance registration.

Enclosed is a check for advance registration (fee includes two luncheons, coffee service and one copy of the Conference Proceedings).

Member ACM or IEEE $50
Nonmember $60
ACM/IEEE Membership Number

Hotel Registration

Twelfth Design Automation Conference
June 23-25, 1975

Please mail this form or a facsimile.

All reservations will be confirmed. Please insure that your reservations are received prior to June 8 so as to take advantage of the pre-established rates.

Circle Daily Rate Desired

Single	$24	$26	$28	$30
Double	$32	$34	$36	
Twin	$36	$38	$40	

All rates subject to 5.7% Massachusetts Hotel Tax.

Name _____

Company _____

Address _____

City/State _____ **Zip** _____

Arrival Date _____ **Time** _____ A.M. P.M.

Departure Date _____ **Time** _____ A.M. P.M.

Send To: The Statler Hilton
Park Square
Boston, Massachusetts 02117

Attention: Front Office Manager
(Tel.) 617-426-2000

Monday, June 23

8:00 a.m. - 9:00 a.m.
"Heuristic Programming — A Tutorial"
R. Karp, University of California, Berkeley, California

9:00 a.m.
Welcome to Boston — H. Wall, Arrangements Chairman

9:05 a.m.
Introduction — R. Hitchcock, General Chairman

9:20 a.m.
Keynote Speaker — Harlan Mills, IBM Federal Systems Division, Gaithersburg, Maryland

10:20 a.m.
Announcements

11:00 a.m. - 12:00 Noon
"Software Engineering — Programming Productivity Techniques"
Janice Lourie, IBM Systems Science Institute, New York, New York,
Nitta Dooner, IBM T.J. Watson Research Center, Yorktown Heights, New York

Around the World With Design Automation I
Monday, June 23, 1:30-5:00 p.m.

Chairman: Jean-Claude Rault, Thomson-CSF, Paris, France

1:30-2:00 "On the Status of Design Automation in Canada" W.M. vanCleemput, University of Waterloo, Canada, R.F. Allum and J.G. Linders, Bell Northern Research, Ottawa, Canada

2:00-2:30 "An Integrated System for Computer Aided Design of Middle and Large Scale Computers" W. Rottman, Siemens AG, Munich, Germany, A. Hoyer, Computergesellschaft, Konstanz, Germany

2:30-3:00 "Design Automation of Electronics in Sweden" I. Hoglund, Asea-Hafo, Sweden, L.H. Fransson, Philips Teleindustri AB, Sweden, A.A. Almen and B. Magnhagen, Saab-Scania AB, Sweden, E. Kjelkerud and O. Thessen, The Royal Institute of Technology, Sweden

3:00-3:30 Break

3:30-4:00 "Set of Programs for Automated Digital Systems Design" M. Priban, M. Jakl, A. Janku, P. Kunc, J. Vesely, A. Boldis, Research Institut of Mathematical Machines, Prague, Czechoslovakia

4:00-4:30 "State of the Art and Trends in D.A. in Italy" L. Simoncinci, Giorgio Valle, and M. Tomljanovich, Selenia Industrie Elettroniche Associate SPA, Italy

4:30-5:00 "A New Algebraic Procedure for the Simulation of Large Digital Networks" L. Gilli, Instituto di Elettrotecnica del Politecnico di Torino, Italy, F. Olla, Olivetti SPA, Italy

Software Engineering I
Monday, June 23, 1:30-4:30 p.m.

Chairman: J. R. Lourie, IBM Systems Science Institute, New York, New York

1:30-2:00 "A Module Interface Specification Language" E.W. Thompson and R.F. Bridge, University of Texas, Austin, Texas

2:00-2:30 "The Application Software Engineering Tool" N.P. Dooner, IBM T.J. Watson Research Center, Yorktown heights, New York J.R. Lourie, IBM systems Science Institute, New York, New York

2:30-3:00 "John Hancock's Experience with Productivity Techniques" N.F. Bern, John Hancock Mutual Life Insurance Co., Boston, Massachusetts

3:00-3:30 Break

3:30-4:00 "The System for Business Automation" S.P. DeJong and M. Zloof, IBM T.J. Watson Research Center, Yorktown Heights, New York

4:00-4:30 "BAL: A General Purpose CAD System" G. Blain, A. Labartho, J.C. Rault, and P. Zamansky, Thomson-CSF, France

Simulation and Modeling
Monday, June 23, 1:30-4:30 p.m.

Chairman: H.K. Gummel, Bell Laboratories, Murray Hill, New Jersey

1:30-2:00 "Digital Logic Simulation Models and Evolving Technology" Cliff W. Hemming, East Texas State University, Commerce, Texas, John M. Hemphill, USAF Radiological Health Laboratory, Wright-Patterson Air Force Base,Ohio

2:00-2:30 "Operational Features of an MOS Timing Simulator" P. Kozak, H.K. Gummel and B.R. Chawla, Bell Laboratories, Murray Hill, New Jersey

2:30-3:00 "Computer Aided LSI Circuit Design: A Relationship Between Topology and Performance" Paul Losleben, National Security Agency, Ft. George Meade, Maryland

3:00-3:30 Break

3:30-4:00 "Three Levels of Accuracy for the Simulation of Different Fault Types in Digital Systems" E.W. Thompson and S.A. Szygenda, University of Texas, Austin, Texas

4:00-4:30 Panel

Tuesday, June 24

8:30 a.m. - 9:30 a.m.
"Diagnostic Test Generation — A Tutorial" S.G. Chappell, Bell Laboratories, Naperville, Illinois

Around the World With Design Automation II
Tuesday, June 24, 9:30 a.m.-12:00 Noon

Chairman: P. Arneberg, Kongsberg, Norway

9:30-10:00 "Test Generation Systems in Japan" S. Funatsu, N. Wakatsuki and T. Arima, Nippon Electric Co., Ltd., Tokyo, Japan

10:00-10:30 "A Simulation System for Implementation and Evaluation of Diagnostic Programs of a Special-Purpose Telecommunication Switching Processor" I. Alleva, M.G. Corti, R. Galimberti and F. Pescarolo, Societa Italiana Telecomunicazioni Siemens, Milano, Italy

10:30-11:00 Break

11:00-11:30 "Present and Future on P.C.B. Layout Design Automation System" A Gingliano and F. Bosisio, SIT Siemens, Italy

11:30-12:00 "Integrated Automation Program For An Electronic Switching System" P. Jabes, A. Ascagni, Stefanini, and F. Albertini, SIT Siemens, Italy

Printed Circuit Layout
Tuesday, June 24, 9:30 a.m.-12:00 Noon

Chairman: R.C. Jantz, Bell Laboratories, Murray Hill, New Jersey

9:30-10:00 "NOMAD: A Printed Wiring Board Layout System" M.J. Welt, Bell Laboratories, Holmdel, New Jersey

10:00-10:30 "Automatic Component Placement in the NOMAD System" Charles F. Shupe, Bell Laboratories, Holmdel, New Jersey

10:30-11:00 Break

11:00-11:30 "The Placement Problem as Viewed from the Physics of Classical Mechanics" Neil R. Quinn, California

11:30-12:00 "Autocorrelation Measurements of Printed Wiring Board Features" R.A. Davis, Bell Laboratories, Denver, Colorado

Software Engineering II
Tuesday, June 24, 9:30 a.m.-12:00 Noon

Chairman:	J.M. Galey, IBM Corporation, San Jose, California
9:30-10:00	"Current Trends in CAD Software Aspects" F-R. Valette, ONERA, Centre D'Etudes Et De Recherches De Toulouse, France
10:00-10:30	"Program Function Test Definition Using a Three Value Simulation" W. Jean Sherman, IBM Corporation, San Jose, California
10:30-11:00	Break
11:00-11:30	"Problem Oriented Approach to the Design of Special Purpose Systems Based on Micro Programmable Processes" Louise H. Jones, E.I. Dupont, De Nemours and Co., Wilmington, Delaware
11:30-12:00	"The Software Engineering Techniques of Data Hiding as Applied to Multi-Level Model Implementation of Logical Devices in Digital Simulation" E.W. Thompson and N. Billawala, The University of Texas, Austin, Texas

Mechanical Design Automation
Tuesday, June 24, 9:30-11:30 a.m.

Chairman:	J. Allan, University of Texas, Austin, Texas
9:30-10:00	"Computer Aided Design of Industrial Control Systems" F. Prunet, D. Floutier and J.M. Dumas, Universite Des Sciences Et Techniques Du Lenguedoc, France
10:00-10:30	"Computer Aided Plant Layout Design" A. De Mari, Fiat Direzione Automazione Informatica, Italy
10:30-11:00	Break
11:00-11:30	"Practical Results with CADSYS" D.E. Whitney, Charles Draper Laboratory, MIT, Cambridge, Massachusetts

Around the World With Design Automation III
Tuesday, June 24, 1:30-5:00 p.m.

Chairman:	M. Tomljanovich, Selenia, Italy
1:30-2:00	"A Case Study of an Operational CAD System for PCB Design" B.H. Phillips and G.L. Patterson, GEC Telecommunications, Ltd., Coventry, England
2:00-2:30	"A CAD System for Unified Hardware-Software Design" Vaclav Rajlich, Research Institute for Mathematical Machines, Czechoslovakia
2:30-3:00	"The Design of the Integrated CAD-System REGENT" G. Enderele and E.G. Schlechtendahl, Institut fur Reaktorentwicklung, Germany
3:00-3:30	Break
3:30-4:00	"Logic Design System in Japan" Tohru Moto-oka, University of Tokyo, Japan, Tadashi Kurachi, Tokyo Shibaura Electric Co., Ltd., Tokyo, Japan, Tsutomu Shiino, OKI Electric Industry Co., Ltd., Masakatsu Sugimoto, Fujitsu, Ltd., Japan
4:00-4:30	"Design Automation in Norway" P. Arneberg, Napensfabrikk, Norway, E. Aas, Norwegian Institute of Technology, Norway
4:30-5:00	Panel

Testing and Testers
Tuesday, June 24, 1:30-4:30 p.m.

Chairman:	E.G. Ulrich, GTE Laboratories, Inc., Waltham, Massachusetts
1:30-2:00	"A Statistical Method for Test Sequence Evaluation" G.R. Case, Sandia Laboratories, Albuquerque, New Mexico
2:00-2:30	"Random Test Generation Using Concurrent Logic Simulation" D.M. Schuler, E.G. Ulrich, T.E. Baker and S.P. Bryant, GTE Laboratories, Inc., Waltham, Massachusetts
2:30-3:00	"Real Time Diagnosis Using Single Pin Probe" L.M. Zobniw, IBM Corporation, Endicott, New York
3:00-3:30	Break
3:30-4:00	"An Emulator for an Automatic Test System" P. Wilcox and L. McCready, Bell Northern Research, Canada
4:00-4:30	"Predicting Fault Distinguishability in Digital Circuits - A New Tool in Design?" J. Fike, Southern Methodist University, Dallas, Texas

Interconnection
Tuesday, June 24, 1:30-4:30 p.m.

Chairman:	J.G. Brinsfield, Bell Laboratories, Whippany, New Jersey
1:30-2:00	"Computer Aids for Multilayer Printed Wiring Board Design" J.G. Brinsfield and S.R. Tarrant, Bell Laboratories, Whippany, New Jersey
2:00-2:30	"Prerouting Analysis Programs" J.C. Foster, Bell Laboratories, Whippany, New Jersey
2:30-3:00	"The Automatic Printed Wire Routing System of BACKIS" G.J. Miron and S.R. Tarrant, Bell Laboratories, Whippany, New Jersey
3:00-3:30	Break
3:30-4:00	"A System for Solution of the Placement Problem" P.L. Ciampi, Raytheon Company, Bedford, Massachusetts
4:00-4:30	"An Algorithm for Automatic Line Routing on Schematic Drawings" R.J. Brennan, Bell Laboratories, Holmdel, New Jersey

Architectural Design Automation
Tuesday, June 24, 1:30-5:00 p.m.

Chairman: J. Comeau, Carleton University, Ottawa, Ontario, Canada

1:30-2:00	"Computer-aided Space Planning" E. Teicholz, Harvard University, Cambridge, Massachusetts
2:00-2:30	"Data Structures for Environmental Design" J.M. Hamer and C. Reeder, Morganelli-Heumann & Associates, Los Angeles, California
2:30-3:00	"Integrated Designers Activity Support System for Architecture" Hideo Matsuka, Toshihiro Kawai, and Sakae Uno, Tokyo Scientific Center, IBM, Japan
3:00-3:30	Break
3:30-4:00	"CAMS: Computer Augmented Mapping System" R.W. Hessdorfer, Bundesforschungsanstalt fur Landeskunde und Raumordnung, Germany
4:00-4:30	"Computer Aided Design in the Department of Public Works of the Government of Canada" K. Robertson, Department of Public Works, Ottawa, Canada
4:30-5:00	Panel

Wednesday, June 25

8:30 a.m. - 9:30 a.m.
"Interactive Graphics in Automated Design - A Tutorial" S. Pardee, Bell Laboratories, Whippany, New Jersey

Partitioning and Placement
Wednesday, June 25, 9:30 a.m.-12:00 Noon

Chairman:	D. Schweikert, Bell Laboratories, Murray Hill, New Jersey
9:30-10:00	"An Iterative Algorithm for Placement and Assignment of Integrated Circuits" D. Schmidt and L. Druffel, Vanderbilt University, Nashville, Tennessee
10:00-10:30	"A Logic Partitioning Procedure by Interchanging Clusters" T. Ishiga, T. Kozawa, and S. Sato, Hitachi, Ltd., Tokyo, Japan
10:30-11:00	Break
11:00-11:30	"A New Approach to Structural Partitioning of Computer Logic" Hans. -J. Groeger, University of Karlsruhe, Germany
11:30-12:00	"A Heuristic Procedure for Ordering MOS Arrays" H. Yoshizawa, H. Kawanishi and K. Kani, Nippon Electric Company, Kawasaki, Japan

D.A. Data Base
Wednesday, June 25, 9:30 a.m.-12:00 Noon

Chairman:	S. Pardee, Bell Laboratories, Whippany, New Jersey
9:30-10:00	"The Evolution of an Integrated Data Base" J.C. Foster, Bell Laboratories, Whippany, New Jersey
10:00-10:30	"An Integrated CAD Data Base System" A.J. Korenjak and A.H. Teger, RCA Laboratories, Princeton, New Jersey
10:30-11:00	Break
11:00-11:30	"Issues in Relational Data Base Organization for CAD Procedures" Giorgio Valle, Universita Degli Studi Di Bologna, Bologna, Italy

Design Description and Verification
Wednesday, June 25, 9:30 a.m.-12:00 Noon

Chairman:	M. Breuer, University of Southern California, Los Angeles, California
9:30-10:00	"An Artwork Design Verification System" H.S. Baird and Y.E. Cho, RCA Laboratories, Princeton, New Jersey
10:00-10:30	"Modeling and Design Description of Hierarchical Hardware/Software Systems" C.W. Rose and M. Albarran, Case Western Reserve University, Cleveland, Ohio
10:30-11:00	Break
11:00-11:30	"Design Validation in Hierarchical Systems" Paul Losleben, National Security Agency, Ft. George Meade, Maryland
11:30-12:00	"Assembly Drawing and Bills of Material Creating System (ADMS)" Hiroyuki Mory, Nippon Electric Co., Ltd., Japan

1:30 - 2:30
Critique of '75 DAC
Plans for '76 DAC

2:30 - 3:30
Open Discussion of Key
DA Problems

	Monday	Tuesday	Wednesday
8:00 8:30	Heuristic Programming Tutorial	Diagnostic Test Generation Tutorial	Interactive Graphics Tutorial
9:00 9:30	Introductory Remarks And Keynote Address	**Session 4** Around The World with DA II **Session 5** Printed Circuit Layout **Session 6** Software Engineering II **Session 7** Mechanical DA	**Session 12** Partitioning and Placement **Session 13** DA Data Bases **Session 14** Design Description and Verification
	Coffee	Coffee	Coffee
11:00	Software Engineering Tutorial	Session 4 Cont'd Session 5 Cont'd Session 6 Cont'd Session 7 Cont'd	Session 12 Cont'd Session 13 Cont'd Session 14 Cont'd
12:00	Luncheon	Luncheon	Luncheon
1:30	**Session 1** Around The World with DA I **Session 2** Software Engineering I **Session 3** Simulation and Modeling	**Session 8** Around The World with DA III **Session 9** Testing and Testers **Session 10** Inter-connection **Session 11** Architectural DA	Critique of '75 DAC Plans for '76 DAC Open Discussion of Key DA Problems
3:00	Coffee	Coffee	
	Session 1 Cont'd Session 2 Cont'd Session 3 Cont'd	Session 8 Cont'd Session 9 Cont'd Session 10 Cont'd Session 11 Cont'd	
5:00	No Host Cocktail Party	No Host Cocktail Party	
6:30	Common Interest Groups ACM SIGDA Software Engineering Simulation & Modeling International DA	Common Interest Groups UEE Design Automation TC Testing Interconnection Architecture DA Mechanical DA	

DATA GENERATION EQUALS DOLLARS AND SENSE

—A SEMINAR— and 17th Joint Annual Meeting

Presented by the

ENGINEERING DATA MANAGEMENT

and

COMPUTER AIDED DESIGN SECTIONS

of the

Technical Documentation Division,

AMERICAN DEFENSE PREPAREDNESS ASSOCIATION

STATLER HILTON HOTEL
BOSTON, MASSACHUSETTS

APRIL 23, 24, 25, 1975

1975 MEETING
EDMS/CADTS
AMERICAN DEFENSE PREPAREDNESS ASSOCIATION
BOSTON, MASSACHUSETTS

WEDNESDAY, APRIL 23, 1975

Session Chairman: Lorna Burns, Hughes Aircraft Co.
Session Secretary: Richard E. Knob, Sperry Gyroscope

0900 **WELCOME - ADPA AIMS AND PURPOSE** Colonel Robert D. Worthen, USA (Ret), Assistant Director, APDA Advisory Service

0910 **ANNUAL REPORTS:** Joseph R. Meitz, Chairman, Engineering Data Management Section, General Motors Corp.

Arthur Thomson, Chairman, Computer-Aided Design Technology Section.

0930 **KEYNOTE SPEAKER:** O.C. Griffith, Chief Administrative Engineer, AiResearch Corporation, Phoenix, Arizona. "FROM THE OTHER SIDE OF THE FENCE".

1000 **COFFEE BREAK**

TECHNICAL SESSIONS

1015 **"WHAT SORT OF ENGINEERING DRAWING THE U.S. GOVERNMENT NEEDS?"**—William W. Thomas, RCA Corp. - A re-examination of the defense and space engineering drawing in design, evaluation, manufacturing, disbursement and logistic support.

1100 **"THE PHYSICAL CONFIGURATION AUDIT - A KEY ELEMENT OF TECHNICAL DATA PACKAGE IMPROVEMENT"**—Horace R. Lowers, Chief Engineer, U.S. Army Missile Command - Planning and conducting a typical Physical Configuration Audit (PCA) will be detailed, including the role of both contractor personnel and Government team. Results from several Army PCA's will be analyzed.

1145 **COMFORT BREAK**

1200 **LUNCH**

Session Chairman: Gerald F. McDonough, Caterpillar Tractor Co.
Session Secretary: Joseph V. Symanoskie, E Systems Inc., Melpar Division

1330 **"A SECOND GENERATION PC BOARD-CAD SYSTEM"**—H.G. Marsh, Manager, Product Support Function, Raytheon Co., Equipment Development Lab. The comparison of a batch mode and interactive PC board CAD system is made. The rational, savings and thruput times are analyzed.

1400 **"ASPECTS OF ENGINEERING SPECIFICATION PREPARATION AND JUSTIFICATION FOR STANDARDIZED FORMATS"**—Frank L. Lint, Consultant, Specification Branch, Technical Data Div., Naval Weapons Center, China Lake, CA. The differences of various standards; e.g., DSM 4120.3M, MIL-STD-490, and the individual practices that are imposed by different government agencies will be discussed.

1430 **"DATA BASE MANAGEMENT OF ENGINEERING DATA"**—Don L. Edmunds, Martin Marietta Data Systems, will deal with an Information Management System (IMS) data base technology to manage Engineering and Configuration Management functions of Planning, Scheduling, Requirements Identification, Part List generation. Cost savings advantages will be stressed.

1500 **COFFEE BREAK**

1515 **"PRODUCTIVITY OF COMPUTER DEPENDENT WORKERS"**—Harry Richter, IBM Corp.

1545 **"DESIGN AUTOMATION FOR DIGITAL CIRCUITS"**—Richard J. Summers, Westinghouse Defense and Electronic Systems Center, Systems Development Division - An operational system of software packages used to lower the cost and increase productivity for the design, manufacture, and test of digital circuits.

1615 **"THE NEW IMPROVED MIL-D-1000A AND MIL-STD-100B"**—Chester Nazian, Frankford Arsenal - a frank discussion of the why and wherefores of these documents.

1645 **ADJOURN**

1830 **INFORMAL RECEPTION-COCKTAILS**

1930 **BANQUET - SPEAKER WILL BE ANNOUNCED**

THURSDAY, APRIL 24, 1975

TECHNICAL SESSIONS

Session Chairman: Robert A. Timlin, Martin Marietta Aerospace
Session Secretary: Charles W. Gedney, Hydro-Space Challenger, Inc.

0830 WORKSHOPS (2)

(A) **"IMPROVING DOCUMENTATION TECHNIQUES"**—Discussion Leader, Robert Franciose, General Electric Company & Chairman ANSI Y14 Committee. Suggested topics for discussion (but not limited to):

- Time saving Techniques
- Documentation Requirements
- Metric Training
- Microfilm Applications
- Specification Relationships

(B) **"USING THE COMPUTER TO IMPROVE PRODUCTIVITY"**—Discussion Leader, Arthur Thomson, TRW Corp. Suggested topics for discussion (but not limited to):

- Configuration control
- Justification of the Computer as a data tool
- Computer Aided Design
- Displays vs Hardcopy

1030 COFFEE BREAK

1045 "INDUSTRY PANEL-REGARDING MIL-D-1000A & MIL-STD-100B"—Leader, Richard Graefe, McDonnell-Douglas Corp.Ted Golmis, Hughes Aircraft Corp. Joseph Meitz, General Motors Corp., Delco Electronics Division.

1115 "USAF PROJECT ACQUISITION COST EVALUATION"—Lt. Colonel Norris Krone, USAF, Assistant for Acquisition Cost Evaluation, Hqs Air Force Systems Command.

1200 LUNCH

Session Chairman: Charles D. Fisher, RCA Government Communications
Session Secretary: James D. Kay, Northrop Corp., Aircraft Division

1330 "CONTRACTORS' VIEW ON MANAGEMENT OF MAJOR WEAPON SYSTEMS ACQUISITION"—John F. Wood, Administrator, Business Practices, IBM Federal Systems Division. A frank discussion of the acquisition process for major weapon systems.

1415 "IMPACT OF SI METRICS ON DATA GENERATION"—Valerie Antoine, Director, Metric Planning, Litton Data Systems. This presentation will provide an overview of why U.S. metrication is inevitable; and will outline how SI Units are used in engineering data management. The frame-of-reference method of learning SI Units will be explained.

1500 GOVERNMENT PANEL - AN OVERVIEW - "COST STUDY OF UNREASONABLE CONTRACT REQUIREMENTS"—Donald R. Mitchell, OASD (I&L), Chairman - Panel members to be announced.

1530 CRACKERBARREL—Anonymous Questions - Answers

1600 ADJOURN

INQUIRIES: Inquiries concerning this meeting should be addressed to

Mr. L.B. Linsky, Raytheon Company, Equipment Development Labs, Box AA3, Wayland, Mass. 01778 (617) 358-2721, Ext. 403

Mr. R. Barta, IBM Corp., Avionics Systems (102B579) Owego, New York 13827 (607) 687-2121, Ext. 2547

Col. R.D. Worthen, U.S. Army (Ret.), American Defense Preparedness Association, 819 Union Trust Building, 740 15th Street, N.W., Washington, D.C. 20005 (202) 347-7250

WORKSHOP ON DATA BASES FOR INTERACTIVE DESIGN

September 15-16, 1975 at University of Waterloo, Ontario, Canada

N E W S R E L E A S E

The Workshop on Data Bases for Interactive Deisgn, sponsored by the ACM Groups SIGDA, SIGGRAPH, and SIGMOD is shaping up nicely. Papers and referees reports have been coming in and we can now predict an interesting symposium.

On the first day we will have invited talks by well-known speakers in the field to set the tone for the meeting. This session will be followed by sessions of refereed papers. These papers cover many aspects of design and corresponding data-base requirements and problems. Suggestions for enhancements and solutions are given. Graphical techniques and the relation of graphics to data-bases are discussed.

As well as refereed papers, there will be a session for informal presentations covering some of the most recent research work. Some people have contacted us and asked if they can give such a short informal presentation, and we will make available an opportunity for other participants who have some interesting results to report to do so at the meeting. Please send me a description, one paragraph, if you wish to give an informal talk and bring material (slides, foils, etc.) to the meeting.

As soon as all the papers have been reviewed we will inform the authors as to which papers have been selected for the symposium and we will publish the technical program.

Meanwhile plan on coming to Waterloo in the Fall, bring your ideas and results, and take part in this worthwhile symposium.

Robin Williams
Program Chairman
IBM
K54/282
Monterey and Cottle Roads
San Jose, California 95193

Information on making reservations and the detailed program will be sent out later to each SIGDA member.

CALL FOR PAPERS

Workshop on Computer Hardware Description Languages and Their Applications

September 3-5, 1975
New York City, New York USA

Increasing interest and attention have been given to the areas of computer-aided logic/system design and documentation. A good computer hardware description language (CHDL) can be used for describing, documenting, simulating and implementing digital systems. The 1973 and 1974 workshops have been held in New Jersey, and West Germany respectively. The Third Workshop on CHDL will be held the week before the 1975 COMPON (September 9-11, Washington, D.C.)

Papers in the following and related areas will be considered:

1. New concepts for description languages
2. Constructs and mechanisms in computer descriptive languages
3. Comparison of languages
4. Applications of languages in documentation, simulation and hardware implementation
5. Hardware compiler (translator) implementation
6. System simulation
7. Computer-aided logic synthesis, logic synthesizer implementation
8. Experience on using languages, simulators, translators and logic synthesizers
9. Analysis of Digital Systems
10. Different levels of CHDL
11. Future prognosis

Information regarding the Workshop can be obtained from:

Professor Stephen Y. H. Su
Workshop Chairman
Department of Electrical Engineering
The City College, City University of New York
New York, N.Y. 10031
Telephone: (212) 621-2392
(212) 621-2248 (secretary)

You are invited to submit 3 copies of the paper in 10 to 20 double-spaced typewritten pages to: Professor Donald L. Dietmeyer
Department of Electrical and Computer Engineering
University of Wisconsin
Madison, Wisconsin 53706
Telephone: (608) 262-3890, 262-3840

The deadling for submitting the papers is March 1, 1975. The papers will be reviewed by the referees.

There will be a session for presenting the most recent results. Authors who would like to talk in this session should submit two copies of the summary to Dr. Dietmeyer by June 1, 1975. Papers for this session will not be published in the Proceedings.

Call for Speakers

Workshop on Methods of Verification in Design Automation or Is the Design Correct?

October 8 - 10, 1975

Michigan State University, East Lansing, Michigan

Co-sponsored by IEEE Computer Society Technical Committees on Design Automation and Fault Tolerant Computing

The rapidly increasing complexity of digital technology has made it mandatory to verify the correctness of a design before committing to manufacturing. This need has, in turn, placed new demands on design automation. Thus, this year's workshop will focus on new methods of verification which have been or are being developed. The following sessions are planned:

Architecture and Logic Verification - Functional simulation, gate level simulation, Boolean comparison, architecture (RTL) - to - logic verification, etc. (Chairman: Steve Chappell, Bell Laboratories)

Microprogramming - Symbolic verification of microcode, interactive debugging/testing systems, verification via comparison to specification, etc. (Chairmen: William Carter, IBM and George Leeman, IBM)

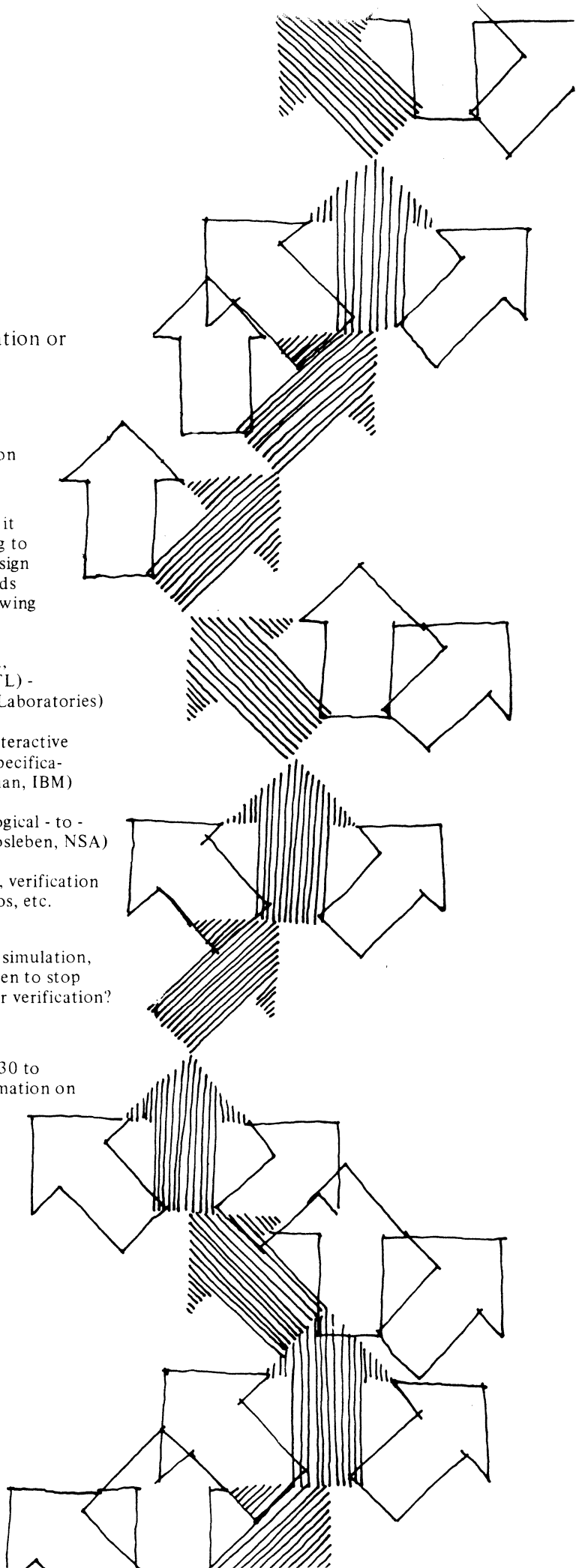
Implementation Verification - Delay and Timing analysis, logical - to - physical checking, shapes checking, etc. (Chairman: Paul Losleben, NSA)

Manufacturing Verification – Testing - DC Tests, AC Tests, verification of manually generated test patterns, testing of arrays, macros, etc. (Chairman: Gernot Metze, University of Illinois)

User Session - How are the programs actually used; e.g., for simulation, how are input patterns determined, how does one know when to stop simulating, etc.? What are the future requirements on DA for verification? (Chairman: Eckhard Schulz, Itek)

Speakers are asked to give a prepared but informal talk of about 30 to 45 minutes length, but a written paper is not required. For information on speaking or attending, contact:

Dr. Roy L. Russo
IBM T.J. Watson Research Center
Post Office Box 218
Yorktown Heights, New York 10598
Tel: 914- 945- 1643



COMPARATIVE ROUTER PERFORMANCE

by

Michael F. Kelly

The following draft describes proposed research to be performed by the author, who is working toward a Ph.D. in Electrical Engineering at the University of California, Davis.

Because of widespread interest in interconnection routing, this work may be of interest to SIGDA members. Reactions to and comments concerning the proposed research would be appreciated.

The author is currently with the Design Automation Project, Electronics Engineering Department (L-156), Lawrence Livermore Laboratory, P.O. Box 808, Livermore, California 94550.

I. INTRODUCTION

Much has been written about the printed circuit board interconnection or routing problem. Ever since Lee's paper in 1961 [1], there has been a quest for new techniques to meet the increasing demands of the electronics industry to put more components on a single PC board.

Several factors contribute to this density pressure. With the drop in the cost of IC's, the industry has gone to a throw away or depot maintenance philosphy. The trend in minicomputer packaging is representative. Consider the DEC PDP-11/05: on-site maintenance consists of swapping one of four cards, which in aggregate contain the entire CPU and memory. Another factor related to increasing component density is lower power dissipation per IC package e.g., CMOS, which allows higher density packaging without heat build-up.

Recently, the advent of the multi-function calculator and the microcomputer would seem to reverse this trend by incorporating large amounts of discrete logic into a single chip. However, just as changes in minicomputer packaging moved the routing problem from the backplane to the PC card, this latest trend merely moves the classical routing problem from the PC card to the chip substrate. Boards containing microprocessor chip sets still require potentially difficult interconnections.

There is one clear trend throughout these advances - routing constraints are increasing with technological advancement. In the past, economic considerations dictated whether routing would be done manually or the resources would be expended to automate the process. In many cases, today's routing problems are surpassing manual capability, making automated routing a technological necessity.

A multitude of automatic routers has been described in the literature, ranging from the original Lee's router to graph theoretical routing techniques. They can be conveniently divided into four broad categories:

1) maze-running routers
2) line probe routers
3) channel routers
4) topological or graph theoretical techniques.

Lee's router and Hitchcock's cellular router [2] typify the first category. Hightower's router [3] is a well known category 2 method. Hashimoto and Steven's router [4] for ILLIAC IV control boards is a category 3 router. The fourth category encompasses many techniques [5], for example the method of Akers et al [6], [7]. Still other techniques seem at first consideration to fall into none of these categories. The stepping-aperture methods of Lass [8] may be viewed as a solution improvement technique or a hybrid router, and hence falls into none of the categories suggested.

In view of this multitude of routing techniques and increasing performance demands, an important issue would seem to be router performance. However, little or nothing of any detail has been published on this topic. Thus, one finds that the question of which router works best, or, more realistically, which router works best in what situation, remains for the most part unanswered. The proposed research will investigate this question of router performance.

To begin to attack such a complex problem, several assumptions and simplifications will be made. Based on presently available literature, it seems safe to assume that there exists no single best router for all problems. Furthermore, one could hypothesize that as interconnection problems became more diversified (as well as more complex), it is unlikely that any existing algorithm will outperform all others in even a significant portion of cases. To simplify the investigation to manageable proportions, a suite of routers will be selected as representative of existing routers; a meaningful set of performance criteria will be defined and a collection of representative problems will be chosen.

The proposed research would first characterize PC board interconnection problem parameters. Next, an attempt will be made to correlate problem parameters with the anticipated performance of the members of the router suite. Next, a series of experiments will be conducted to determine the actual performance of the router suite on the representative problem collection, to test the validity of the correlation. Undoubtedly, these experiments will suggest modifications to the performance criteria, the problem parameters, or both. Finally an independent collection of routing problems will be used to test the significance of the modified criteria and parameters.

The underlying motivation for this work is to develop a system which, when given a routing problem, will automatically identify the characteristic problem parameters, select the most appropriate router, route the problem, and measure the performance criteria. If a less than satisfactory solution is obtained, this partially interconnected solution could then be automatically rerun as a problem. However, the system development itself is more a software engineering effort than engineering research. Hence this thesis will establish the fundamental relationships between routing technique and router performance necessary to this effort.

II. THESIS

1) Router Suite Selection

A serial router can be divided into three major parts:

1) Signal set decomposition,
2) Wire layout, and,
3) Clean-up.

Signal set decomposition involves transforming sets of electrically common pin connections into a single set of node-to-node connections or from - to's. Track layout is the process of actually routing the wires between the nodes. Clean-up reviews the results and attempts to correct errors and improve the overall quality of the route.

Signal set decomposition can be further divided into two processes:

a) from-to generation, and
b) from-to ordering.

Two well-known forms of signal set decomposition are derived from the definitions of minimum spanning trees and Steiner trees. The algorithm for generating a minimum spanning tree in a barrier-free environment is straightforward. However, there is no known algorithm for minimum Steiner Tree generation. Hence, to keep the conclusions of this research as general as possible, the minimum spanning tree algorithm will be used in from-to generation.

Parallel routing techniques, i.e., techniques that route point-to-point connections concurrently rather than one after another, have not yet been shown applicable to production PCB layout problems; thus this research will be concerned only with serial routers. Most serial routers include a method for determining the order in which from-to's will be routed; many ordering schemes have been proposed [9] and the topic is somewhat controversial [10]. This research will use several ordering methods, comparing the results obtained using various combinations of ordering and wire layout algorithms. Typical ordering methods use from-to characteristics such as rectilinear distance, primary rectangle area, and track width.

As discussed earlier, there are four general categories of routing algorithms. The first three categories contain the most widely used algorithms, while category 4 contains algorithms of a developmental or theoretical nature. To keep the scope of this investigation practical but pertinent, the suite of routing algorithms will be restricted to one programmed implementation of a technique from each of the first three categories. One purpose of this study is to correlate routing performance with distinct routing technqiues, so no hybrid or "multi-stage" routers will be included.

Lee's algorithm is the basis for the techniques included in category 1. A straightforward implementation of the original algorithm would be prohibitively expensive in terms of computer time and memory -- which are important performance criteria. Hence, an implementation of the cellular technique will be used since this method appears to improve performance in these areas while preserving other basic properties of the Lee algorithm.

Hightower's line search technique is the best known category 2 method. Hightower's technique has none of the fundamental performance drawbacks of Lee's. Other line-probe techniques have been described [11], but they use the same fundamental technique. Therefore, this study will use a Hightower line probe router.

In category 3, Hashimoto and Steven's channel router algorithm is restricted to rather limited component placement geometries, namely, those with highly regular arrays as on ILLIAC IV control boards. Other channel routing algorithms have been described for I.C. mask layout [12] but these too are restricted to regular component geometries and, even further, to groups of identical components. Since a variety of PC board geometries will be used in this study, a practical extension of the original channel routing algorithm will be used to lay out boards with relatively arbitrary geometries.

This study emphasizes basic router performance; therefore only a limited attempt will be made to improve the quality of board layouts produced by the router suite.

Following common practice, routing algorithms will be restricted to rectilinear or "Manhattan" routes, and all from-to routings that fail to connect will be entirely deleted from further consideration at the time of the failure. Further, no attempt will be made during clean-up to reduce congestion, to make Steiner connections or to improve the overall cosmetic condition of the layout.

However, each of the algorithms selected has inherent shortcomings that are manifested in the geometry of the resulting layout. It is recognized that any board layout system using these algorithms should incorporate

methods to deal with such shortcomings. For this reason, the clean-up processor used in this study will attempt to eliminate unecessary wire turns and vias.

In summary, the router suite will be composed of: 1) a minimum spanning tree signal set decomposition algorithm with a collection of ordering methods; 2) three routing techniques - a maze-runner, a line-probe and a modified channel router; 3) a turn and via elimination procedure.

2) Performance Criteria Selection

Router performance may be viewed from two perspectives: economic and technical. Economic performance criteria are generally based on the cost of an automatic wire layout compared to the cost of a manual layout of the same routing problem. This cost is reflected in both the resources expended to generate the layout and the production cost of the board itself. This study will include economic cost factors such as:

1) Number of non-completed connections. Connections that must be completed with insulated wire rather than etched lands add another manufacturing phase and hence increase expense.
2) Number of vias or feed-through holes. Vias add expense to the board drilling process and possibly to quality control of higher reliability boards if plated-through holes must be checked optically for defects not detected during continuity testing.
3) Computer time charges. This cost is measured in CPU time plus I/O time at the amortization rate of the computer system. The study will assume a rate of $1200 per hour of CPU plus I/O time on a CDC 7600. All experiments will be conducted using a single hardware/software system to minimize environmental side effects.
4) Computer memory requirements. This cost is actually reflected in the amortized system costs but since it does impact the minimum system size that can run a router it will be used to weight the computer time charges.
5) Land distribution among layers. A radically uneven distribution of lands among layers causes warping of the broad during soldering and reduces yield.

While economic performance is measured in dollars, technical performance is difficult to quantize. Hence, the technical criteria will be presented in physical units with only qualitative statements about their impact on the electronic quality of the layout. Factors which will be considered include:

6) Wire length. Obviously, wire length should be short to minimize signal degradation and noise.
7) Wire density or congestion. Wire spacing should be maximized to suppress crosstalk.

8) Number of wiring rule violations. Wiring rules govern such parameters as minimum track width, minimum wire spacing, minimum via size, etc. The rules are dictated by the desired electronic properties of the particular circuit and no engineering judgments will be made about the implications of the violations.

This list should not be considered complete, since the study itself is expected to indicate additional significant performance criteria.

3) Identification of Problem Classification Parameters

Problem classification is concerned chiefly with the physical geometry of the printed circuit board and its components. This study concerns interconnection routing, so component placement will be invariant for a particular problem. (See for example [13] and [14] which treat the influence of placement on restricted types of routers.)

One of the main purposes of the research is to identify problem characteristics relevant to router performance. The parameters listed below represent a partial enumeration of problem descriptors thought to be of interest. Admittedly, the list is probably not complete.

1) Board dimensions
   a) horizontal and vertical dimensions
   b) shape
   c) routable or unobstructed area
   d) number of layers
2) Number of edge connectors and test points
3) Number of components
4) Regularity of placement
5) Number of component package geometries
6) Number of active pins and nodes
   For this parameter, it may be useful to distinguish between nodes in a data path and those in a control circuit, since it appears at this time that data nodes are easier to route than the usually more randomly distributed control nodes [15].
7) Node distribution (clustering)
8) Ideal wire length distribution

Clearly, these parameters differentiate board-component configurations, yet some of them may have no correlation with routing technique or performance. Nevertheless, these parameters will be used as a starting point for the study, to determine which problem parameters do correlate technique with performance and are sufficiently sensitive to distinguish problem classes.

4) Selection of Representative Problems

The study will be conducted at the University of California Lawrence Livermore Laboratory, so most problems will be selected from existing LLL boards and new designs. It is quite probable that no single one of these boards is representative of a particular manufacturer's routing

problems. However, a wide variety of boards is available at the laboratory and a large number will be used in the study to represent a cross section of problems.

The Laboratory is not engaged in production of large numbers of identical electronic devices. Typically, only a few boards of each new design are produced. These devices span the entire scope of applications from control to data processing and communications. Hence, the Laboratory has developed a standard library of pre-loaded boards and the capability to produce custom boards. The available collection of board designs may be non-representative to the extent that less than 10% are single layer boards and less than 1% have four or more layers. Since the majority of industry boards are multi-layer [16] and most of these are two layer boards, it does not seem unreasonable to consider only two layer boards in this study. If it is determined that the initial selection is non-representative, the problem collection will be augmented to include single layer boards and multi-layer boards from other manufacturers.

During the proposed study a spectrum of boards from this collection will be investigated; most will have been manually routed. These problem boards will be re-routed using the suite of routers discussed previously, and the resulting layouts will be compared with each other and with the original designs.

5) Correlation Experiments

This study will attempt to determinine which problem-related characteristics correlate with routing technique performance. Each of the three areas involved (problem characteristics, performance criteria and routing technique), is not rigorously defined. The literature abounds with references to items in each area, but actual definitions (if indeed given) vary from author to author.

Perhaps the best defined area is that of routing technique. However, there are many variations on each basic technique and the performance of each variation certainly depends on its hardware and software environment. To limit ambiguity in definition, the routers used will be fundamental but still perform well enough to make the results of the study pertinent to the work of professionals in this field. In addition, some of the more important router parameters, e.g., from-to order and primary rectangle size, will be varied to determine the gross effects of parameter changes on router performance. However, it should be emphasized that it is not the purpose of this study to develop high-performance routers.

The question of hardware and software environment impact on router performance is a complex one; the proposed study deals with relative performance, so a uniform environment throughout the research avoids most of the effects of this problem.

Some router performance criteria such as computer run time, memory requirements, wire length and number of vias are widely accepted. Others are mentioned occasionally and some will be developed during the study. It may be difficult to define universal criteria since engineering goals and economic implications vary widely from problem to problem. The study thus will not deal with the relevance of criteria but will define as many reasonably meaningful criteria as possible, to make the results relevant to as many economic and technical situtations as practical.

No significant work is known to have been reported in the area of problem classification. This is surprising, since it is quite difficult to discuss router performance without reference to routing problems. The study will attempt to define a set of characteristic problem parameters which distinguish particular problems. Hopefully, these will at the same time correlate with routing technique performance observations. Each of the routers previously discussed will be used to process a selection of problems exhibiting a range of classification parameters. The results, expressed in terms of performance criteria values, will then be mathematically compared with the values of problem parameters for each router. Correlations between performance criteria and problem parameters will be sought. Hopefully, these correlations will depend on the router used. (The absence of correlation may be equally important; see [10].) A second, independent selection of problems will be processed using measurement and classification criteria revised after the first series of experiments. This phase of the study will seek the verification of the old criteria and the discovery of new ones.

It is difficult to hypothesize at this stage what the results might be. Some of the most likely findings are: 1) a low connection completion rate for the channel router applied to problems with irregular placement geometry; 2) high via count for the line-probe router for problems having irregular placement geometry; and 3) high computing costs for the maze-running router applied to problems with a high active pin density.

6) Experimental Results

The most significant results of the research may be expressed in terms of the problem feature/router performance correlations discussed above. However, certain factors which might influence the results will not be studied exhaustively; therefore these issues must at least be investigated; some qualitative conclusions concerning them should be reached. Two such factors will illustrate this aspect of the work.

The size of the problem sample and the number of samples is not yet well defined. Ten to fifteen reasonably diverse problems should be enough to insure that each sample represents a wide range in classification parameters. The number of samples, however, will depend on early experimental results. If correlations are immediately obvious and consistent across samples, the research can be concluded. But, if there is little correlation or consistence, the research will have to continue until either consistent findings are produced or lack of correlation is demonstrated.

The variation of router performance with router parameters is an issue the study seeks to avoid. Establishing a clearly defined suite of routers at the beginning and using them throughout the research will eliminate route parameter effects, but not avoid the issue of their potential impact on the research results. This question could be viewed as a relevant follow-on research topic, to be based on the findings of the proposed work. Due to the interrelationship of the two topics, a preliminary investigation of algorithm sensitivity to parametric variations will be pursued toward the end of the proposed work. At that time several important route parameters for each programed router will be varied. The effects both on router performance and on problem characteristic will be reported.

7) Modifications

Modifications to both the problem parameters and performance criteria will be considered after the initial problem selection has been processed and the results have been studied. Appropriate modifications to both parameters and evaluation criteria discussed above will be included in the following series of experiments.

8) Significance Tests

The significance of the research results will depend on their relevance to the general problem of routing. Relevance in turn depends on the solution of representative problems, the definition of practical performance criteria and the consistency of results.

The problems will encompass a range of parameters broad enough to make the study of interest to others in the field. The performance criteria selected for initial study include those suggested by a survey of relevant literature; others are thought to be measures of anticipated routing difficulty. Criteria will be added as their relevance is indicated by the ongoing research. Consistency of results must be established by obtaining similar correlations from selections of different problems with similar parameters.

The issue of router significance or relevance is difficult to treat at this time. Whether or not the performance of one router is important to the designer of another router can only be determined by comparing the actual structure of the routers. Since detailed structural features of routers are not often discussed in open literature, a comparison with existing "production quality" PC board routers is not practical. Rather, the structure for each of the routers used will be developed in a manner generally consistent with the descriptions available in technical references. In addition, the experiments related to variations in router parameters should indicate how representative the algorithm implementations may be.

III. CONCLUSIONS

The proposed research would be conducted in three phases. First a suite of routers would be selected and programed. This phase would also include definition of performance criteria and the identification of preliminary problem classification parameters.

During the second part, the selection of a representative set of existing problems would occur. These problems would be routed using the suite of routers, and a correlation analysis would be performed to compare router performance with problem classification.

During the final phase, modification and extension of the problem parameters and performance criteria would occur, as indicated by the phase 2 analysis. The phase 2 routing experiments would then be repeated, this time using an independent selection of problems. A comparison of the new results with previous ones would be used to check consistency. If the results of phase 3 are not conclusive but otherwise look promising, phase 3 experimentation may be continued, with still further revision of parameters and criteria being tested on yet another problem collection.

An estimate of the time required for the study is necessarily approximate, especially for the final research phase. Substantial work has already been done on the first phase, with approximately four more months until completion. The second phase should take about two months and the third phase at least three months. An additional month to two months will be necessary to compile the results in final form. Hence, approximately 10 to 11 months would be needed for the study. It is premature to anticipate the results of the study but the outcome of carefully planned and documented experiments will undoubtedly be of great interest to the design automation community. Increased technological demands on routing capability and the economic constraints of the industrial environment make the proposed study both timely and unique. Extensive computer facilities, a comprehensive design automation support system [17], and a broad spectrum of existing board-component geometries, all available at LLL, make the study possible.

The relevance of the study becomes clearer if one takes an overall look at current routing efforts. Interconnection routing is now an art rather than a science. Much ongoing work in the area of topological routers seeks to develop a systematic approach to the problem, but it appears that little emphasis is placed on the scope and character of the problems to be solved. Most board routing programs now in use are judged by performance on a very narrow spectrum of problems. Emphasis appears to be placed on developing a router implementation for a particular geometry, with the geometry being used in a large number of PCB designs.

Of course, there are many reasons for standard geometries beside the expense of router development. There are, however, situations in which standardization is not desirable or perhaps not even possible. This study seeks a correlation between the performance of currently available routers and a well defined, represenatative set of problems. This correlation could then be used to implement an adaptive, multi-stage router capable of processing a variety of geometries. Further, the correlation and the multi-stage work would easily lead to the development of better versions of existing techniques and possibly better routing algorithms.

IV. REFERENCES

1. Lee, C., "An Algorithm for Path Connections and Its Applications", IRE Trans. on E.C. (Sept. 1961).
2. Hitchcock, R., "Cellular Wiring and the Cellular Modeling Technique", Proc. Design Auto. Workshop (1969).
3. Hightower, D., "A Solution to Line Routing Problems on the Continuous Plane", Proc. Design Auto. Workshop (1969).
4. Hashimoto, A., and Stevens, J., "Wire Routing by Optimizing Channel Assignment Within Large Apertures", Proc. Design Auto. Workshop (1971).
5. Kodres, U. R., "Formulation and Solution of Circuit Design Problems Through the Use of Graph Methods", Proc. IECP Symp., Boulder, Colo. (1961).
6. Akers, S., and Hadlock, F., "Graph Theory Models of Electrical Networks and their Minimum Cross-Over Layouts", Conf. on Graph Theory and Computing, Kingston, Jamaica (Jan. 1969).
7. Akers, S., and Geyer, J., and Roberts, D., "IC Mask Layout with a Single Conductor Layer", Proc. Design Auto. Workshop (1970).
8. Lass, S., "Automated Printed Circuit Wiring with a Stepping Aperture", CACM (May 1969).
9. Adshead, H., "Optimizing Automatic Tracking of Multilayer Boards", AGARD Conf.: Computer Aided Design for Electronic Circuits, Copenhagen (May 1973).
10. Abel, L., "On the Ordering of Connections for Automatic Wire Routing", IEEE Trans. on Computers (Nov. 1972).
11. Mikami, K. and Tabuchi, K., "A Computer Program for Optimal Routing of Printed Circuit Conductors", Proc. IFIP Congress, Edinburgh (1968).
12. Kernighan, B., and Schweikert, D., and Persky, G., "An Optimum Channel Routing Algorithm for Polycell Layouts of Integrated Circuits", Proc. Design Auto. Wrokshop (1973).
13. Wilson, D., and Smith, R., "An Experimental Comparison of Force Directed Placement Techniques", Proc. Design Auto. Workshop (1974).
14. Rubin, F., "Printed Wire Routing for Multilayer Circuit Boards", Ph.D. Thesis, Syracuse Univ. (1972).
15. Sutherland, I., and Oestreicher, D., "How Big Should a Printed Circuit Board Be?", IEEE Trans. on Computers (May 1973).

16. Nakahara, H., "Computer-Aided Interconnection Routing: General Survey of the State-of-the-Art", Networks (1972).
17. Smith, R., and Matelan, N., "Software Organization for a Multi-Purpose Digital Design Automation System", Submitted to Fall 1975 IEEE Computer Conf. (Also available as UCRL-76688)

New Publication on Mathematical Software

The Association for Computing Machinery
announces a new quarterly

acm transactions on mathematical software (TOMS)

John R. Rice, Editor-in-Chief **Lloyd D. Fosdick, Algorithms Editor**

Associate Editors

Abe Bjork	W. J. Cody	M. Stuart Lynn
W. Stanley Brown	Patricia J. Eberlein	Joel Moses
B. F. Caviness	Morven Gentleman	M. J. D. Powell
Alan Cline	Thomas E. Hull	Joseph F. Traub

Scope: Significant research and development results in the area of

Fundamental Algorithms and Associated Software

Analysis of Mathematical Algorithms
Construction of Algorithms and Programs
Analysis of Programs
Critical Evaluation of Programs
Methodology of Evaluation and Analysis
User and Systems Interface with Algorithms
Dissemination and Maintenance of Programs

Within this scope, content material is expected to

Interface With Traditional Areas

Arithmetic Functions
Numerical Analysis
Polynomial Manipulation
Computational Linear Algebra
Pattern Recognition
Languages for Mathematical Software
Symbolic Algebraic Computations
Optimization and Nonlinear Programming
Statistical Computations
Sorting, Ordering, and Classifying
Symbolic Mathematical Algorithms
Operations Research

The content of papers in those areas that are primarily applications will be applicable to a reasonably wide class of problems and not just to the consideration that motivated the paper.

Papers will be of two kinds: (1) the usual technical variety, and (2) algorithms as in the highly valued Algorithms section of *Communications of the ACM*. The Algorithms section of *Communications* will be phased into TOMS and the algorithms will continue to be issued in ACM's looseleaf service: *Collected Algorithms from ACM*.

Quarterly • First Issue March 1975 • Projected 400 pages annually

ACM Transactions on Mathematical Software (TOMS) • Order Form

Association for Computing Machinery
P. O. BOX 12105
CHURCH STREET STATION
NEW YORK, NY 10249

I WISH TO ORDER TOMS:

__copies @ $15.00 ACM { Regular / Associate / Student } Member Rate: $____

__copies @ $40.00 Subscriber Rate: $_____

I understand the first issue of TOMS will be dated March 1975.

Signature_____

ACM MEMBER NO. | | | | | | | |

ACM SUBSCRIBER NO. | | | | | | | |

NAME & ADDRESS as it appears on ACM files (please print)

_____

_____

_____

_____

Orders without accompanying payment should be addressed to: ACM TOMS Order Department, 1133 Avenue of the Americas, New York, NY 10036

PROCEEDINGS FOR 9th, 10th and 11th DA WORKSHOP

The following is the rate schedule as agreed to by SIGDA and the DA Technical Committee of IEEE.

	COPIES		SIGDA & ACM Members	All Others	Amount
1)	_____	9th DA Workshop Proceedings (1972) @ $10.00 376 Pages	$10.00	$16.00	_____
2)	_____	10th DA Workshop Proceedings (1973) @ $10.00 288 Pages	$10.00	$16.00	_____
3)	_____	11th DA Workshop Proceedings (1974) 379 Pages	$12.00	$20.00	_____
		Member Number _____		TOTAL =	_____

Please send your order prepaid to:

ACM Inc.
P.O. Box 12105
Church Street Station
New York, New York 10249

Make your checks payable to Association for Computing Machinery (an added charge is made for billing).

JOIN SIGDA JOIN SIGDA JOIN SIGDA JOIN SIGDA JOIN SIGDA JOIN SIGDA JOIN SIGDA JOIN SIGDA

_____
Name (please type or print)

_____
Affiliation

_____
Mailing Address

_____
City State Zip

Annual membership dues are $3.00 for ACM members and $5.00 for others.

____ Enclosed annual dues.

____ Please send more info.

Mail to SIGDA
ACM INC.
P.O. Box 12105
Church Street Station
New York, NY 10249

Association for Computing Machinery
1133 Avenue of the Americas, New York, New York 10036