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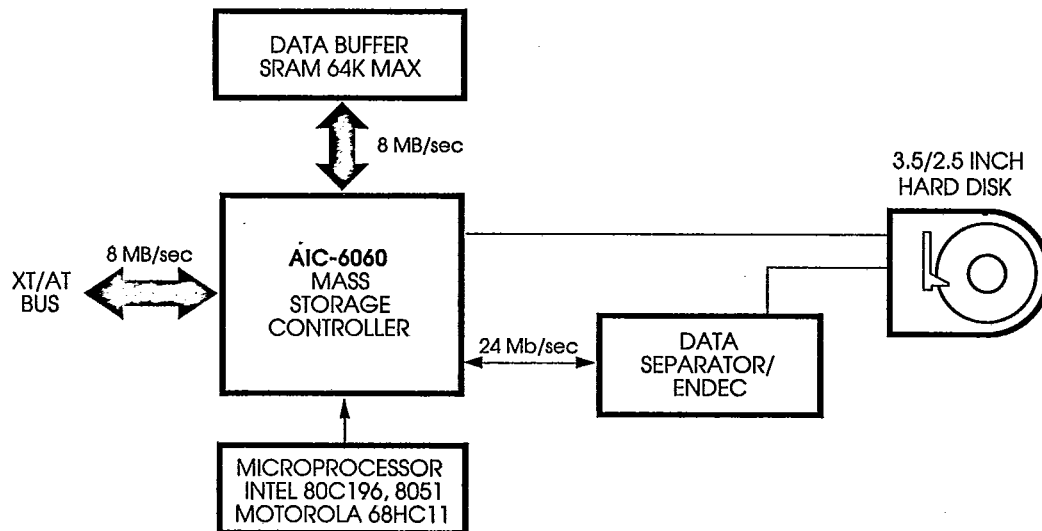
AIC-6060

Single-Chip PC XT/AT Mass Storage Controller

AIC-6060 Typical Application

FEATURES

Host Interface

- On-chip registers to emulate the IBM AT Task File, and XT Command Descriptor Block
- Supports 8- and 16-bit data transfers on the host bus
- On-chip 24 mA drivers for direct interface with XT/AT bus
- Up to 8 MBytes/sec data transfer
- 16-byte master/slave embedded controller configuration

Buffer Interface

- Additional divide-by-three clock
- Supports up to 64 KBytes of SRAM for direct buffer memory addressing
- Up to 8 MBytes/sec buffer memory throughput
- Buffer bandwidth independent of disk data rates

Peripheral Interface

- Supports NRZ rates up to 24 Mbits/sec
- Supports ST412/506, ST412HP, ESDI, and SMD disk interfaces
- Selectable 16-bit CRC or 32/56-bit ECC polynomial
- Supports 1:1 interleaving

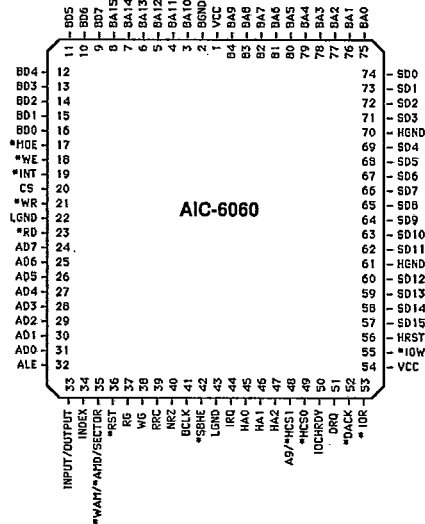### Technologies

- Low-power CMOS technology
- 84-pin PLCC and 100-pin QFP packages
- Programmable power-down capability
- Alternate source for the SH-260

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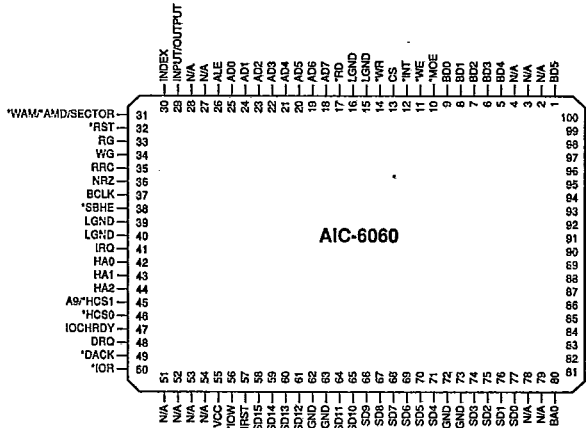
AIC-6060

AIC-6060 100-Pin QFP Package

AIC-6060 84-Pin PLCC Package

Overview

The AIC-6060 is a highly integrated, software-programmable VLSI chip that provides the majority of the circuitry necessary to build a PC XT/AT hard disk controller. The AIC-6060 offers pin-to-pin and functional compatibility with the SH-260 device, and can be used as a direct source alternative. With the use of the AIC-6060, all of the disk control functions can be embedded into the disk drive itself, thus eliminating the need for a separate disk controller board and offering cost and space reduction in the overall system.

The AIC-6060 is programmable to allow two hard disk cards or two embedded disk drives to be connected to the PC XT/AT host bus. Supporting disk data rates of up to 24 Mbits/second, the AIC-6060 design incorporates an advanced Winchester Drive Formatter, a dual-port Buffer Manager, and extensive circuitry for supporting the PC XT/AT interfaces.

The Formatter/Sequencer is a programmable state machine which sequences the disk interface control signals. It provides the flexibility necessary to interface to a wide variety of proprietary, embedded drive interfaces. The Formatter/Sequencer supports 16-bit CRC or 32/56-bit programmable ECC polynomial for Data Field error correction with high speed, hardware-assisted correction.

The Buffer Controller allows up to 64K of standard SRAMs to be directly addressed and used as a circular FIFO buffer for data storage during read/write operations. An additional divide-by-three clock is also featured for higher transfer speeds and flexibility.

The Host Interface supports data rates up to 8 MBytes/second and includes a 16-byte FIFO between the Host port and the data buffer for maximum data throughput. The chip's on-board 24 mA drivers allow it to connect directly to the XT/AT bus.

The AIC-6060 is a CMOS device and offers the reduced space and low power consumption requirements necessary for the embedded system environment. Programmable power-down capability is also provided. It is available in 84-pin PLCC package or 100-pin QFP package.

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