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8500 Series Disc Memory Unit OPERATION & MAINTENANCE MANUAL

DATAPOINT CORPORATION

686 WEST MAUDE AVENUE
SUNNYVALE, CALIFORNIA 94086

LIST OF EFFECTIVE PAGES

Changes, deletions, and additions to information in this manual are indicated by bars in the margins or by an asterisk near the page number if the entire page is affected. A bar by the page number indicates pagination rather than change of page content.

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PREFACE

This manual describes the AMCOMP 8500 Series Disc Memory Unit with the AMCODE adapter PC board. The disc memory unit is a fixed-head, head-per-track digital disc recording device of random access and high performance.

This manual is divided into six chapters as follows:

- Chapter 1 - General Information
- Chapter 2 - Installation and Checkout
- Chapter 3 - Operation and Interface
- Chapter 4 - Theory of Operation
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Chapter 1

GENERAL INFORMATION

1-1 INTRODUCTION

This chapter contains general information pertaining to the AMCOMP 8500 Series Disc Memory Unit (figure 1-1). The information in this chapter consists of general description, functional description, and physical description, including the description of major components within the disc memory unit. Table 1-1 lists the performance, electrical, environmental, and physical characteristics of the 8500 Series Disc Memory Unit.

1-2 GENERAL DESCRIPTION

The 8500 Series Disc Memory Unit is available in two models: the Model 8510 and Model 8530. The 8510 model is an 1800-rpm unit with an average access time of 16.7 milliseconds, and data transfer rate of 4.5M bits/sec. (See table 1-1 for details.) Model 8530 is a 3600-rpm unit with an average access time of 8.3 milliseconds and data transfer rate of 9M bits/sec. Both models are capable of storing up to 154,000 bits per track. One to four units may be used (daisy-chained) and individually addressed by a single external controller which may be supplied either by AMPCOMP or by the customer.

1-3 FUNCTIONAL DESCRIPTION

Data is recorded on both sides of the disc in addressable tracks with a single read/write head assigned to each track. Each disc may contain up to 256 tracks (16 tracks minimum). Track selection is accomplished by eight input address lines. When the input address bits from the controller are decoded, three of them yield the eight X-coordinates and four (least significant bits) the 16 Y-coordinates. Bit 7 of the input address is used for disc surface selection. The 8 X 16 addressing matrix (for each disc side) provides for the selection of one of 128 tracks.

Data on the tracks is recorded in sectors. The sector is defined as the minimum addressable record on the disc. Complete format flexibility permits variations in the size and number of sectors per track (table 1-1). Sectors are recorded on the disc with the customer specified format at the factory prior to shipment.

A write lockout assembly, available as a standard option, has 16 switches each of which protects a different group of 16 tracks. The lockout assembly is mounted on the front of the chassis directly behind the front, removable panel of the disc.

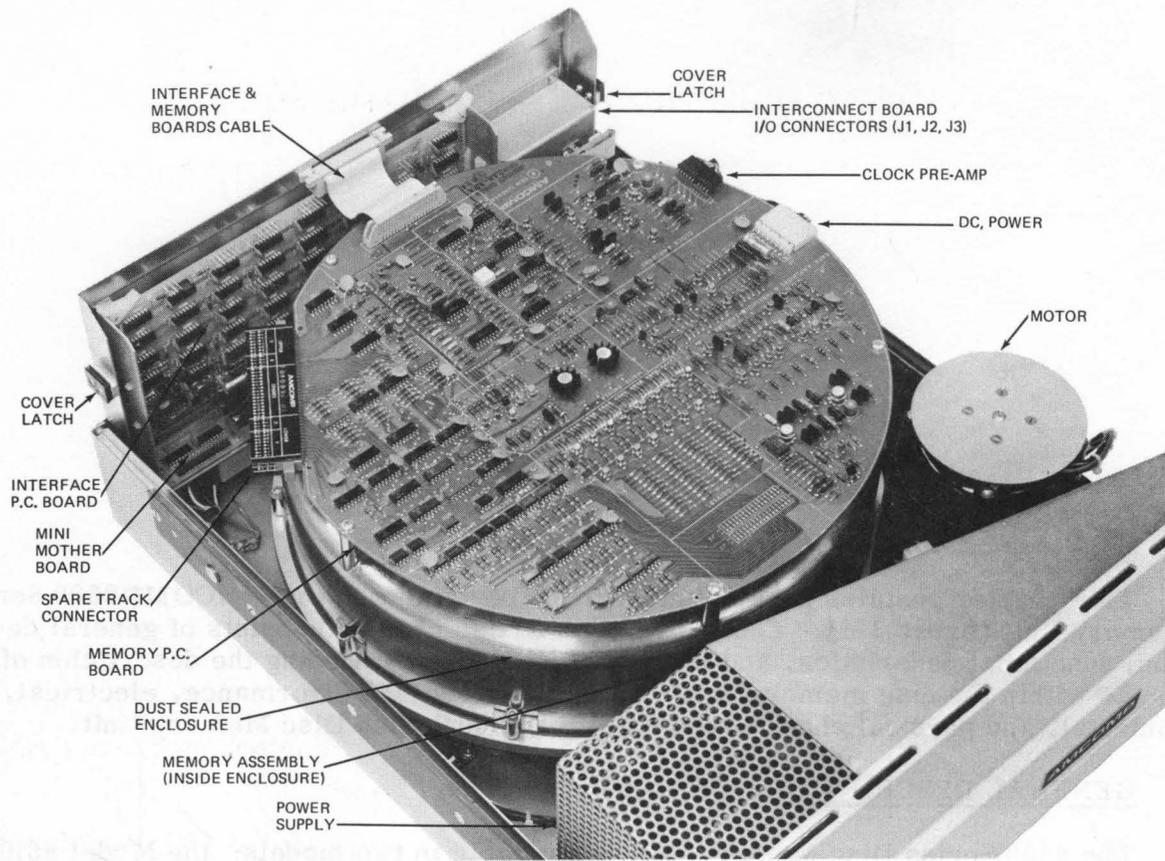


Figure 1-1. 8500 Series Disc Memory Unit

TABLE 1-1. SPECIFICATIONS AND CHARACTERISTICS

<u>Performance</u>		
Data Tracks	maximum minimum	256 plus 32 spares 16 plus 1 spare
Clock Tracks		1 set plus 1 spare jumper selectable
Bits per Track (unformatted)	maximum	154,000 (Model 8530, option -01*)
	minimum	146,000
	maximum	146,000 (Model 8530, option -02*)
	minimum	134,000
	maximum	134,000 (Model 8530, option -03*)
	minimum	125,000
	maximum	125,000 (Model 8530, option -04*)
	minimum	103,000
	maximum	152,000 (Model 8510, option -05*)
	minimum	140,700
	maximum	140,700 (Model 8510, option -06*)
	minimum	119,900
Storage capacity	maximum	40.2×10^6 bits (unformatted)
Recording Density (at 157,000 bits/track)	maximum	7795 bits/inch (innermost data track)
Rotational Speed		1816 $\begin{smallmatrix} +27 \\ -45 \end{smallmatrix}$ rpm (Model 8510)
		3632 $\begin{smallmatrix} +53 \\ -89 \end{smallmatrix}$ rpm (Model 8530)
Average Access Time		16.6 \pm 0.4 ms (Model 8510)
		8.3 \pm 0.2 ms (Model 8530)
Data Transfer Rate	maximum	9.93 MHz (Model 8530, option -01)
	minimum	8.20
	maximum	9.30 MHz (Model 8530, option -02)
	minimum	7.50 MHz
* Selection of options is done through test-point jumpering according to the list on AMCODE PC board schematic diagram 1940077.		

TABLE 1-1. SPECIFICATIONS AND CHARACTERISTICS (continued)

Performance (Cont'd.)

Data Transfer Rate	maximum	8.65 MHz (Model 8530, option -03)
	minimum	7.00 MHz
	maximum	8.06 MHz (Model 8530, option -04)
	minimum	5.80 MHz
	maximum	4.90 MHz (Model 8510, option -05)
	minimum	3.97 MHz
	maximum	4.50 MHz (Model 8510, option -06)
	minimum	3.36 MHz
Error Rate	recovable	1 error in 10^{11} bits read
	non-recovable**	1 error in 10^{12} bits read

Physical

Dimensions	panel height	8.72 in. (22.15 cm)
	width	19.00 in. (48.26 cm)
	width behind panel	16.88 in. (42.88 cm)
	depth	23.00 in. (58.42 cm)
	depth behind panel	22.19 in. (56.36 cm)
Weight		95 lbs. (42.8 kg)
Bearing Design Life		10 years
MTBF (Mean Time Between Failure)		10,000 hours for 8510 & 8530, 256-track models
MTTR (Mean Time to Repair)		60 minutes
Motor Start Time (to READY)	maximum	20 seconds

** A non-recovable error is defined as a single bit or many consecutive bits in error from which valid data cannot be recovered within three consecutive passes through the same data record.

TABLE 1-1. SPECIFICATIONS CHARACTERISTICS (continued)

<u>Power</u>		
AC	voltage	100, 120, 220, 240 Vac $\pm 5\%$, -10%
	frequency	50 or 60 Hz $\pm 5\%$, single phase
	start current (at 120-volt)	8.3 amps maximum
	run current (at 120-volt)	2.7 amps maximum
<u>Environmental</u>		
Temperature	operating	0 to 55°C
	non-operating on-site shipping/storage (properly packed)	0 to 65°C -30 to +65°C
Temperature Change	operating maximum for data reliability	10°C per hour maximum
Relative Humidity	operating	10% to 90% without condensation
	non-operating	0% to 90% without condensation
Vibration	operating and non-operating	0.080-inch (2.03 mm) double amplitude displacement, 5 to 35Hz; 5g acceleration maximum, 35 to 500 Hz
Shock	operating and non-operating	15g, 11 ms, 1/2 sine wave
Altitude	operating and non-operating	10,000 ft. (3,048 m) 25,000 ft. (7,620 m)
	Atmosphere	non-corrosive

1-4 PHYSICAL DESCRIPTION

All components of the basic 8500 Series Disc Memory Unit are mounted on a precision machined base casting (base plate). All the disc rotational components (disc, spindle, bearings), the read/write heads, and the clock preamplifier card are contained in a dust sealed enclosure which provides a clean, controlled operating environment.

The disc memory assembly, including the pulleys and belt, are mounted on the tray with four tough and rigid shock mounts. Mounted on the tray also are the input ac connector and the voltage selecting connector. The back panel mounts on the tray also and holds the I/O connectors and the mini mother board with connectors J1 and J2 (one spare) into which the interface logic board is plugged. A radio frequency interference (RFI) cover is used to enclose the electronics and thus reduce the possibility of emissions of stray magnetic fields and also susceptibility to them.

The basic disc electronics are packaged on two fiberglass printed circuit boards. One of them (AMCODE adapter board) mounts vertically at the back panel and plugs into a connector. The other (memory board) is mounted above the dust sealed enclosure. The memory board connects to the AMCODE board via an interconnection cable.

A label is located on the rear of the disc memory unit that identifies the type of power supply, number of sectors per track, maximum number of bits per sector, and the gap (in microseconds) between track origin and the first sector clock signal. The label format is shown below.

<u>60</u>	-	<u>1440</u>	-	<u>256</u>	-	<u>40</u>
60 Hz		sectors per track		bits per sector		gap

1-5 MECHANICAL ORGANIZATION

The disc is recorded on both sides as it rotates in a fixed horizontal plane between two head plates. Mounted on these plates are the read/write heads fixed in a head-per-track arrangement. The two head plates contain a maximum of 256 read/write heads, a clock head, and a maximum of 32 spare read/write heads of which 16 are guaranteed at time of shipment. Each head plate contains 48 read/write head assemblies. The top head plate contains, in addition to its read/write head assemblies, the clock head assembly. Mounted on each head assembly is a 3-point (3-head) transducer that is gimbaled in order to be aerodynamically stable when in flight. These transducers contact the disc (on both sides) when the disc is not rotating and fly 12 ± 5 micro inches away from the disc surface by the air produced when the disc reaches operating speed. The closeness of the heads to the disc results in recording sharp, well-defined magnetic regions and in reproducing strong, clean signals. The disc plating is nickel-cobalt with rhodium overcoat, making the disc surface impervious to contact damage.

The triple transducer head assembly used for the clock detects the recorded bit clock, sector clock, and track origin (timing signals). These clocks are recorded on two tracks simultaneously for the purpose of having one identical spare. Changing from one track to the next (spare) is accomplished by changing a wire wrap jumper.

The basic memory assembly consists of the base plate, spindle, disc, head plates, and motor. The memory assembly is supported by four shock mounts. The rotating assembly consists of the motor, a set of stepped pulleys, a seamless mylar belt, the spindle, and a 12-inch disc platter. The spindle and disc, together with the two head plates and clock preamplifier card, are in a dust sealed enclosure which is pressurized through a filtering system. The minimum required pressure for the 1800-rpm disc (model 8510) is 0.05 inches of water, and the pressure for the 3600-rpm disc (model 8530) is 0.20 inches of water. The maximum allowable particle count in the rotating assembly is less than five particles, 0.5 microns or larger over ten-minute period and a flow rate of 0.01 cubic feet/minute. The rotating assembly is driven by non-synchronous, capacitor start motor the features of which are small size, high reliability, maximum efficiency, and low starting current drain. It is capable of operating on 115 Vac at a frequency of either 50 Hz or 60-Hz. By using the stepped pulley, 3600 rpm or 1800 rpm rotation is provided at either the 50 Hz or 60-Hz input frequency. The motor is 1/15 horsepower either 1800 rpm or 3600 rpm. The 1800-rpm motor is used with the 1800-rpm disc unit, and the 3600-rpm motor is used with the 3600-rpm disc unit.

1-6 ELECTRONIC PACKAGING

The interface electronics and read/write electronics are contained in the AMCODE printed circuit (PC) board and the memory PC board, respectively. All electronic components are mounted on the circuit boards in generally functional groups of integrated circuits and discrete components. The memory PC board is modular and lends itself to easier field service.

In addition to AMCODE and memory PC boards, there are the clock preamplifier PC board and the mini mother PC board. The clock preamplifier board, located inside the dust sealed enclosure, amplifies and buffers the clock signals (bit clock, sector clock and track origin). The mini mother board (figure 1-1) contains the logic through which the binary address from the controller is decoded into octal and inputted to connector J3. The track capacity plug connects to connector J3 on the mini mother board. Each track capacity plug is specifically wired for only one disc size; the number of tracks for which the plug is patched appears on the plug itself.

Internal lead lengths are kept as short as possible to prevent noise pickup. Also, sensitive circuits are located as close as possible to the signal source so that stray pickup is eliminated. Substitution of data head with a spare is accomplished by two jumper wires on the spare track connector which connects to the memory board (paragraph 5-24).

Chapter 2

INSTALLATION AND CHECKOUT

2-1 INTRODUCTION

This chapter contains the information required to install and checkout the 8500 Series Disc Memory Unit. Included are instructions and data required to plan the installation, unpack and inspect the unit, complete installation, checkout the disc unit, and prepare it for normal operation. Instructions for packing the disc unit for reshipment are also included.

2-2 EQUIPMENT LOCATION

The 8500 Series Disc Memory Unit may be located adjacent to any other electronic data processing equipment provided the temperature, humidity and other environmental characteristics are within specified limits. Table 1-1 provides performance specifications and characteristics for the disc unit. The disc unit must not be located in a strong magnetic field since the disc may become magnetized and cause interference with the read/write operation.

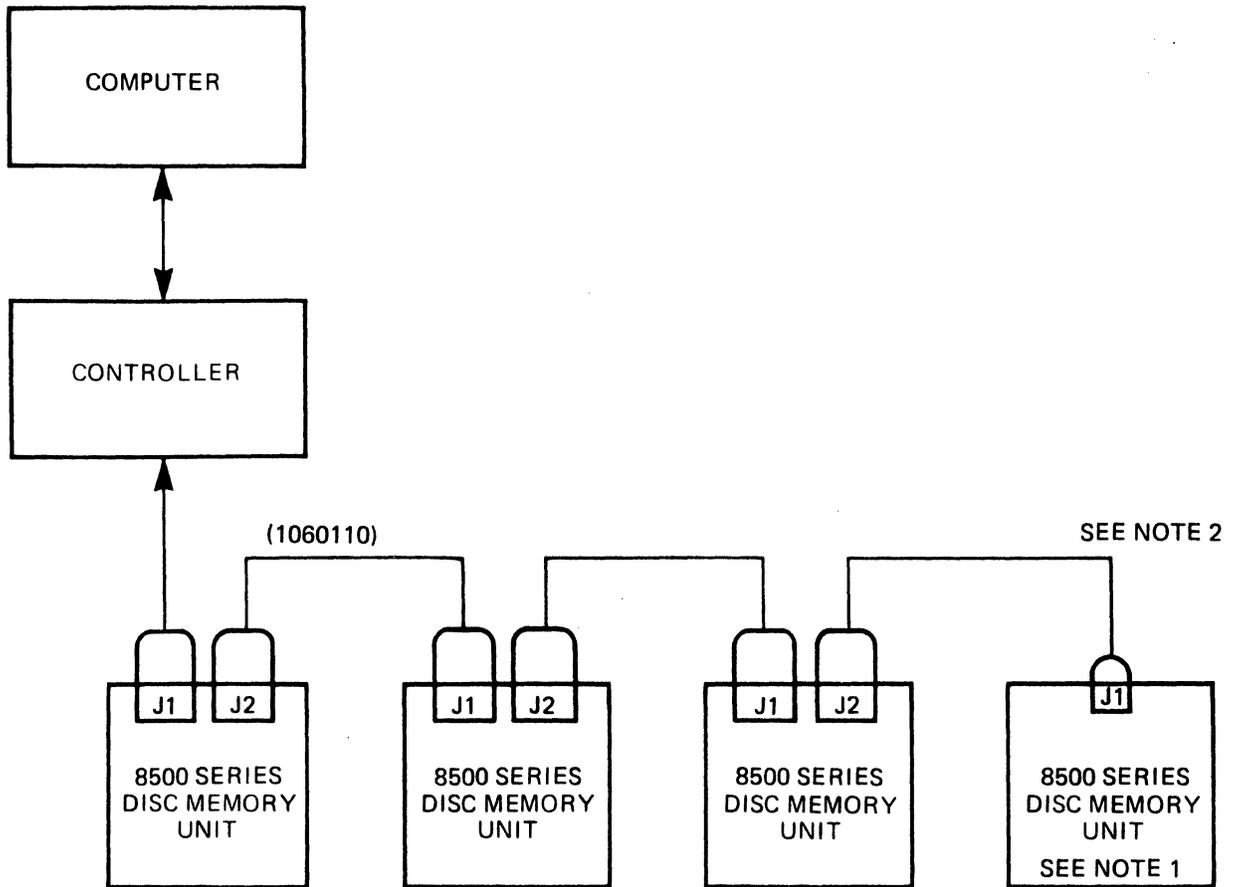
The disc units are designed to be mounted in an adequate 19-inch electronic rack cabinet. Each disc unit requires approximately 8.75 inches of vertical rack space. When a disc unit is mounted, the rack should be located on a firm surface. (Refer to figure 2-1 for mounting dimensions of the 8500 Series Disc Memory Unit.)

2-3 DAISY-CHAIN CONFIGURATION

Where more than one disc unit is to be connected in a daisy-chain configuration, the cabling is as shown in figure 2-2. The total length of any daisy-chain I/O cable must not exceed 30 feet. Signal line terminating networks, in resistor packs located on the memory circuit board, must be removed from each disc unit in the daisy-chain except the last one. The resistors are mounted in sockets to facilitate removal for daisy-chain operation. Refer to figure 3-6 for a schematic of resistor networks and line drivers, and to figure 2-3 for the physical location of resistor (terminating) networks and unit select jumper table. Where daisy chaining is done subsequent to the original installation by the acquisition of additional disc units, the daisy-chain I/O cabling must be purchased from AMCOMP, INC. or fabricated directly by the customer in the field. (Refer to table 2-1 for the input/output cable signal and pin assignments.)

2-4 UNPACKING AND INSPECTION

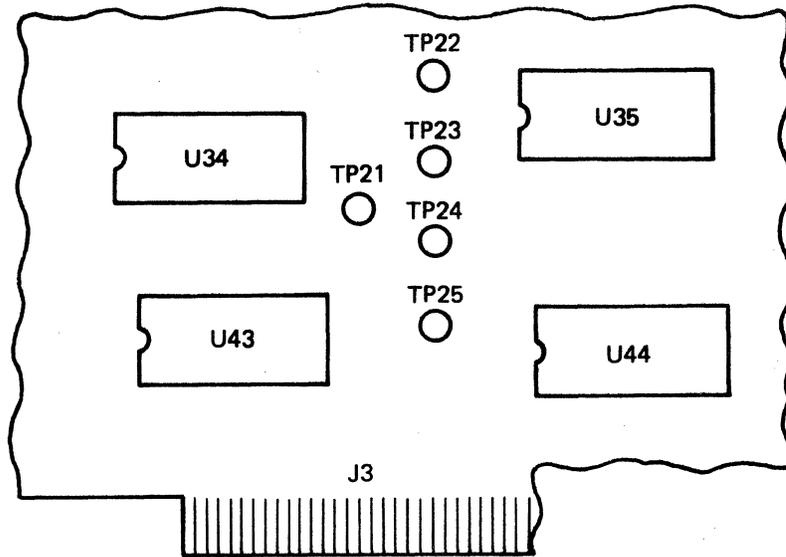
The disc unit is shipped in a special double packing case. The front panel is shipped separately from the disc unit but it is packed in the same packing case. As the equipment is unpacked, care should be exercised to prevent damage to the finished surfaces of the



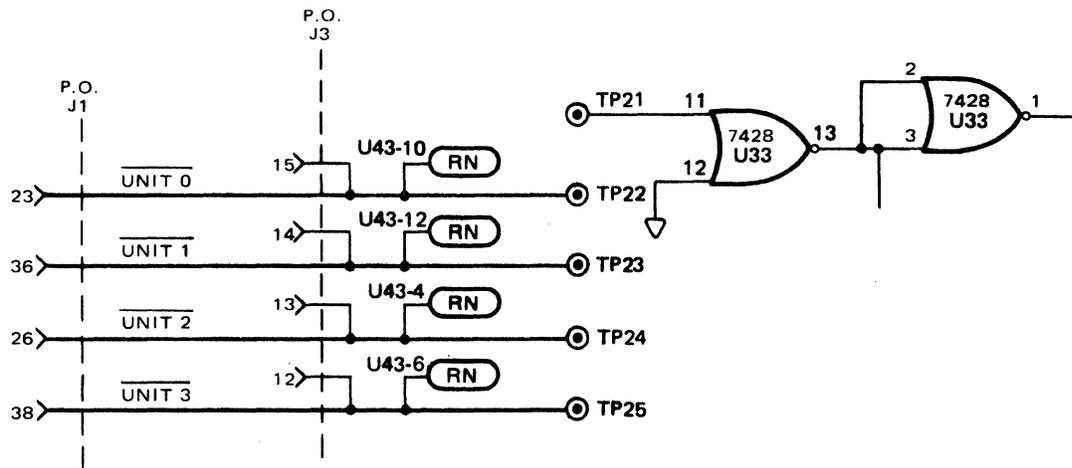
- NOTES:
- 1) TERMINATORS U8 and U9 MUST BE REMOVED FROM ALL BUT THE LAST DISC MEMORY UNIT IN DAISY-CHAIN
 - 2) MAXIMUM I/O CABLE LENGTH BETWEEN CONTROLLER AND LAST DISC MEMORY UNIT IN DAISY-CHAIN IS 30 FEET
 - 3) POWER TO THE DISC MEMORY UNIT WITH TERMINATORS (LAST UNIT) MUST BE ON WHILE THE OTHER DISC UNITS ARE IN OPERATION

Figure 2-2. Typical Daisy-Chain Cabling Arrangement

AMCODE
ADAPTER
BOARD
ASSEMBLY
(1040077)



AMCODE
ADAPTER
BOARD
SCHEMATIC
(1940077,
SHEET 2)



UNIT SELECT JUMPER CONNECTION TABLE		
FROM	TO	FUNCTION
TP 21	TP 22	Unit 0 Selected
TP 21	TP 23	Unit 1 Selected
TP 21	TP 24	Unit 2 Selected
TP 21	TP 25	Unit 3 Selected

Figure 2-3. Physical Location of Terminating Resistor Networks & Unit Selection Test Points

TABLE 2-1. INTERFACE INPUT/OUTPUT SIGNALS AND PIN ASSIGNMENTS (BACKPLANE CONNECTORS J1, J2)

PIN No.	SIGNAL DEFINITION	SIGNAL MNEMONIC	INPUT TO DISC	OUTPUT FROM DISC
1	Return			
18	Disc Ready	DISC RDY		X
34	Not connected			
35	Track Address 7	T7	X	
2	Track Address 6	T6	X	
19	Track Address 5	T5	X	
3	Track Address 4	T4	X	
20	Track Address 3	T3	X	
36	Track Address 2	T2	X	
37	Track Address 1	T1	X	
4	Track Address 0	T0	X	
21	Unit Select 3	UNIT 3	X	
5	Unit Select 2	UNIT 2	X	
22	Unit Select 1	UNIT 1	X	
38	Unit Select 0	UNIT 0	X	
39	Return			
6	Illegal Address	ILLEGAL ADD		X
23	Return			
7	Not Used			
24	Return			
40	Track Origin	TRACK ORIGIN or TO		X
41	Return			
8	Sector Clock	SECTOR CLK		X
25	Return			
9	Sector Write	SWD	X	
26	Return			
42	Read	READ	X	
43	Return			
10	Write	WRITE	X	
27	Return			
11	Read Data	RD DATA		X
28	Return			
44	Bus Terminated	BUS TERMINATED		X
45	Return			
12	Write Data	WR DATA	X	
29	Return			
13	Spare 1			
30	DC Ground			
46	Read Clock	RD CLK		X
47	Return			
14	Spare 2			
31	Return			
15	Write Clock in	WR CLK IN	X	
32	Return			

TABLE 2-1. INTERFACE INPUT/OUTPUT SIGNALS AND PIN ASSIGNMENTS (BACKPLANE CONNECTORS J1, J2) (continued)

PIN No.	SIGNAL DEFINITION	SIGNAL MNEMONIC	INPUT TO DISC	OUTPUT FROM DISC
48	Spare 3			
49	Return			
16	Write Clock out	WR CLK OUT		X
33	Return			
17	Shield Ground			
50	Shield Ground			

disc unit. All parts should be inspected for evidence of damage during shipment. If the packing case or any disc unit parts are damaged, advise AMCOMP, INC. and file a claim with the transfer company. The crated weight of the disc unit is approximately 115 pounds. The following procedure should be followed for unpacking and inspecting the disc unit.

- a. Inspect the packing case for evidence of in-transit damage. Contact the transfer company and AMCOMP, INC. if damage is evident. Specify nature and extent of damage.

CAUTION

The disc unit weighs approximately 95 lbs., and should be lifted by at least two persons.

- b. Open the outer and inner packing case and remove the contents. Check items removed against the shipping list to verify packing case contents. Contact AMCOMP, INC. in the event of a packing shortage.
- c. Remove additional packing material and verify that the serial number of the unit corresponds to that shown on the shipping invoice. The serial number can be observed at the rear panel of the disc unit on the AMCOMP product label. The product label also shows the disc unit part number and track format.

NOTE

The special packing case used by AMCOMP, INC. for shipment of the 8500 Disc Memory Unit is designed for one-time use only and should be discarded. If reshipment of the disc unit becomes necessary, a new packing case designed specifically for the 8500 Series Disc Memory Unit may be acquired from AMCOMP, INC. AMCOMP, INC. is not responsible for damage due to faulty packing which may occur to the 8500 Disc Memory Unit during reshipment.

- d. Visually inspect the exterior of the disc unit for evidence of any physical damage that may have occurred in transit. Inspect the cover for dents or abrasions.

- e. Check for broken or damaged switches and broken or loose wires on connectors. Check the power supply and front panel.
- f. Remove the top RFI shield cover and check the printed circuit wiring boards. Ensure that the board is unbroken and properly seated with all components mounted. Ensure that the mounting screws are tightened down.

NOTE

If any damage is discovered, notify AMCOMP, INC. and the transfer company immediately. Failure to notify AMCOMP, INC. of damage to the disc unit, and subsequent operation of the disc unit under these conditions, may void the warranty.

Before replacing the RFI shield cover, verify that the resistive termination networks are in place and that the select jumpers are installed properly.

2-5 DISC UNIT SELECTION

Disc units are normally shipped with the unit select 0 jumper installed. Refer to figure 2-3 for the physical location of the unit select test points and resistor network chips as well as for the jumper table and schematic of the unit select wiring. If another unit select line is desired, remove the installed jumper and install another jumper between the desired test points using a wire-wrap tool. When the proper unit select jumper is installed, replace the RFI shield and mount the front panel on the unit.

2-6 SHIPMENT PROTECTION

To aid in preventing shipment damage, the disc unit is equipped with three 5/16 - 18 x 2 ½-inch lock-down bolts in order to prevent movement within the shipping case during shipment. These lock-down bolts must be removed before the disc unit is placed in operation. The lock-down bolts are accessible from the bottom of the chassis assembly.

WARNING

Never attempt to operate the disc unit without first removing the three lock-down bolts.

2-7 DISC UNIT MOUNTING

When the disc unit is received it may be installed into an equipment cabinet using the supplied slides and mounting hardware. Remove the unit from the shipping frame and refer to figure 2-1 for mounting dimensions. Install the unit using appropriate mounting hardware. Connect the I/O cables (to/from external controller) and ac power line (figure 2-4). If the optional write lockout circuit is provided, make the appropriate switch settings and install the protective cover over the front panel switches.

2-8 CHECKOUT

Preoperational adjustments or alignments to the 8500 Disc Memory Units are not necessary. All adjustments and alignments are made at the factory prior to shipment. If

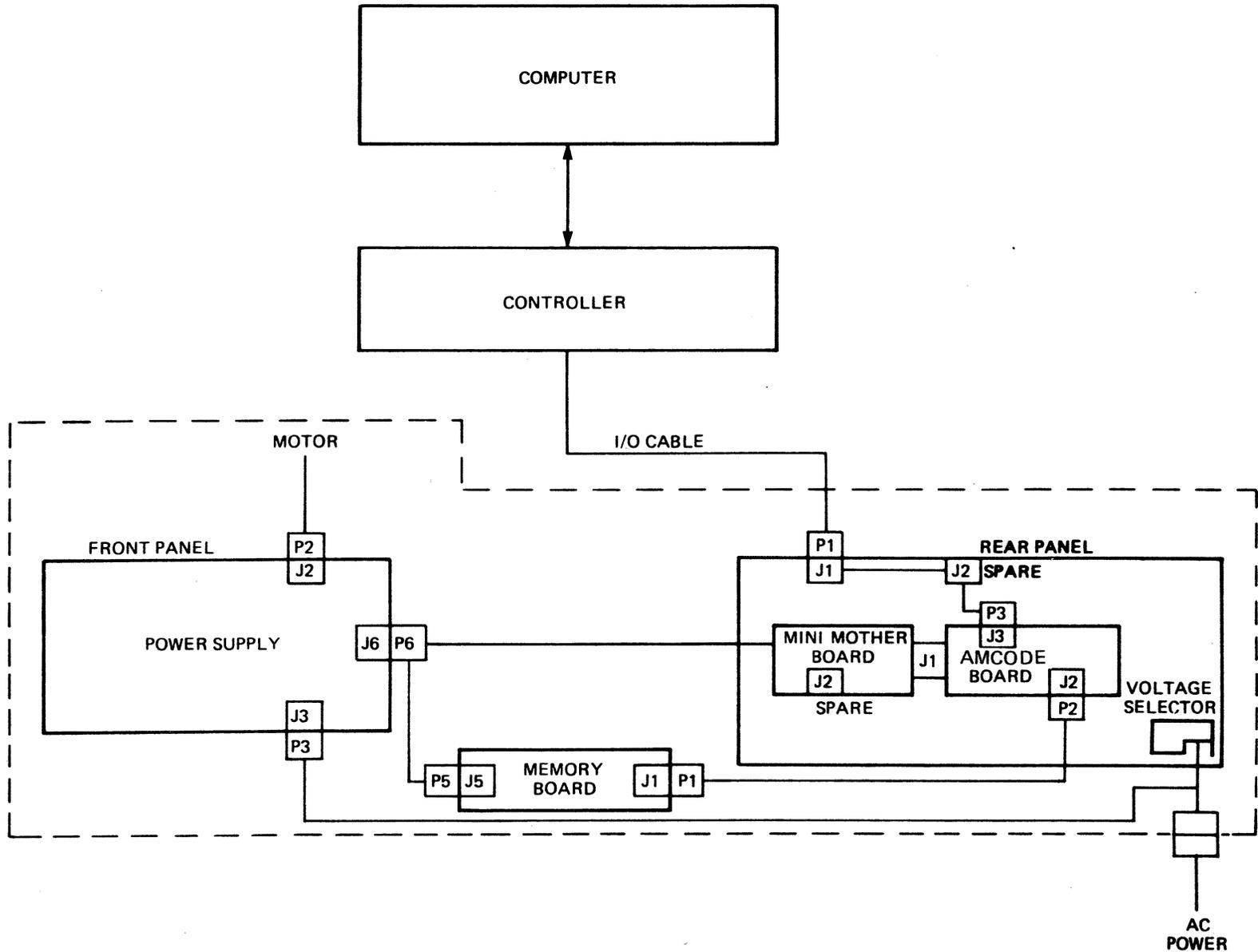


Figure 2-4. 8500 Disc Memory Unit Cabling

the procedures described in the preceding paragraphs have been followed carefully, the disc unit is ready to be put into operation.

Before applying primary power to the disc unit, ensure that the lock-down bolts have been removed, resistive terminating networks are installed correctly, the unit select jumper is installed properly, and the selected voltage matches the line voltage. Also ensure that all cables are connected properly and that the disc unit is mounted firmly.

The 8500 Series Disc Memory Unit is equipped with a lever action power switch on the front panel. The switch applies power to the disc drive motor and to the dc power supply. After the unit is installed, according to the instructions in the preceding paragraphs, turn on the power switch. Approximately 10 seconds later the disc will be at operating speed.

NOTE

Before turning power on, check line voltage. If voltage is not correct, make proper selection according to the following paragraph.

2-9 VOLTAGE SELECTION

Line voltages of 100, 120, 220, and 240 volts can be selected through a voltage selector PC board (figure 2-5) located in rear panel of the disc memory unit. To select an operating voltage perform the following steps:

1. Open cover door and rotate fuse-pull to left.
2. Select operating voltage by orienting PC board to position desired voltage on top left side. (Selected voltage should be visible when PC board is installed.)
3. Rotate fuse-pull back into normal position and re-insert fuse into holders, careful to install a fuse with correct value. (See value on label at back panel.)

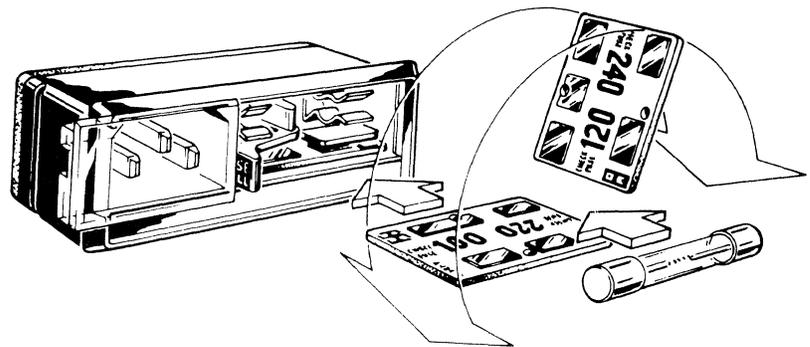
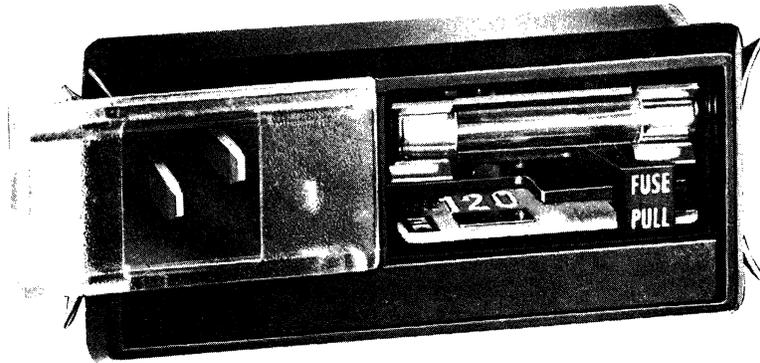
2-10 PACKING FOR RESHIPMENT

When reshipment of the 8500 Series Disc Memory Unit becomes necessary, the disc unit should be packed in a packing case that is of identical or of similar construction to the packing case in which the disc unit was delivered (figure 2-6). Specially designed packing cases for the 8500 Series Disc Memory Unit can be acquired from AMCOMP, INC., 686 West Maude Avenue, Sunnyvale, California 94086. Pack the disc unit for reshipment in accordance with the following procedure.

NOTE

It is not recommended that the disc unit be shipped in an equipment cabinet configuration. Reshipment must be in a container.

- a. Disconnect the input/output interface cable and power cord.
- b. Remove the disc unit from the equipment cabinet.



Operating voltage is shown in
Connector window.

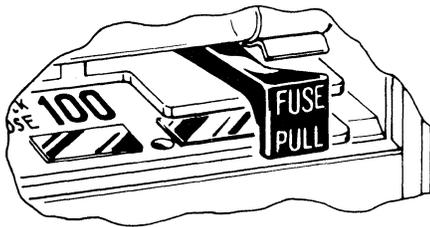


Figure 2-5. Voltage Selecting Connector

- c. Attach plywood to disc unit with screws using one backing plate at each screw location.
- d. Place a package of fresh dessicant on the plywood alongside the unit and wrap loosely the unit and plywood with a polyethylene sheet and tape. Avoid sliding the wrapped assembly across a surface to prevent the plywood mounting screws from cutting the polyethylene sheet.

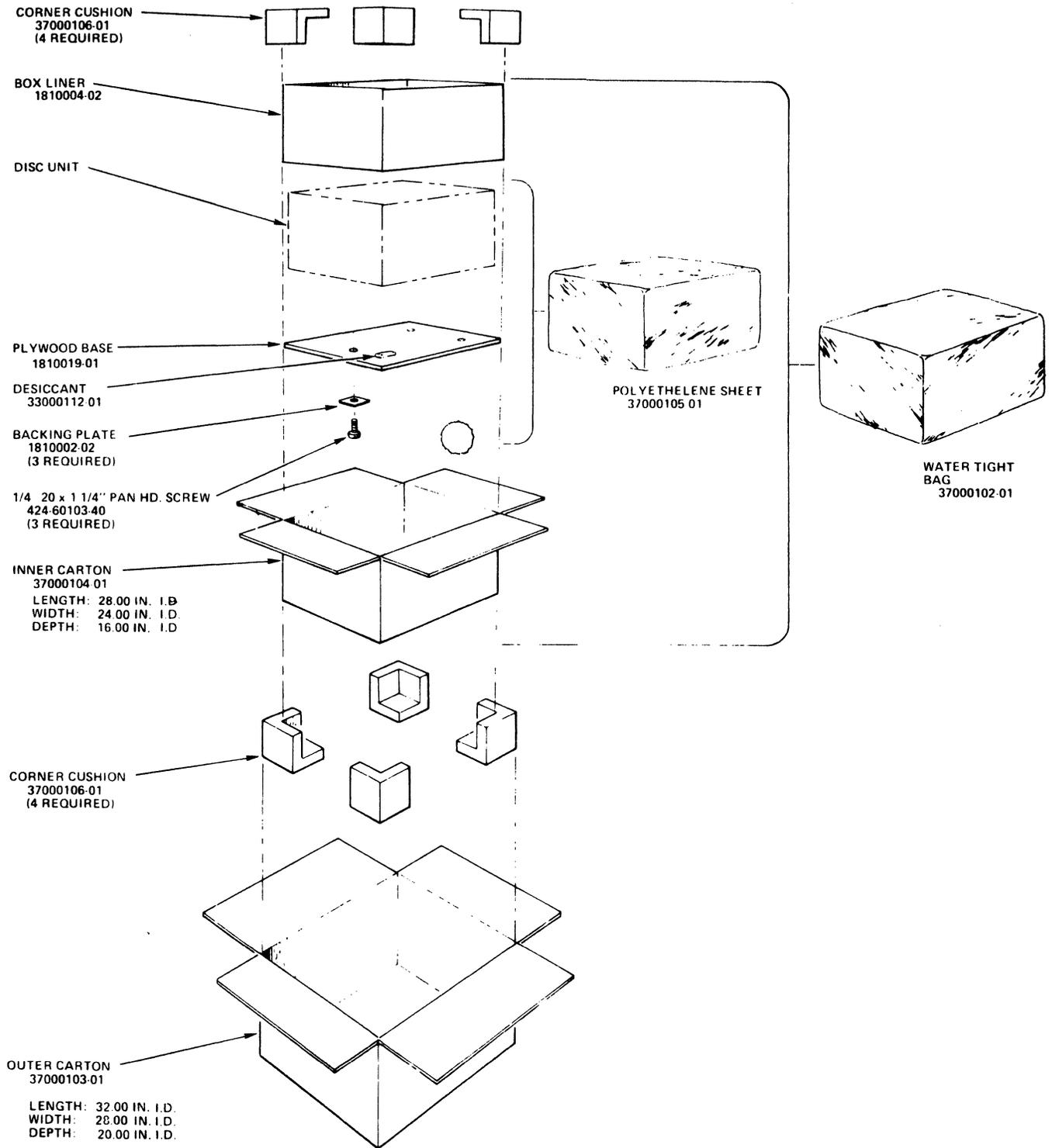


Figure 2-6. Disc Memory Unit Shipping Carton

- e. Place wrapped assembly inside inner carton. Place box liner inside carton on top of plywood and polyethylene sheet.
- f. After closing and taping the inner carton, place inside water tight bag, With a heating source, seal water tight bag except for one corner. With a vacuum cleaner or other vacuum source, suck air out of water tight bag so that bag collapses onto inner carton. Complete sealing the bag with heating source.
- g. Place the sealed package inside the outer carton using cushion corners Enclose manuals or other items as required.
- h. Place CAUTION label onto inner carton before sealing outer carton.

NOTE

AMCOMP, INC. is not responsible for damage, due to faulty packing, which may occur to the 8500 Series Disc Memory Unit during reshipment.

Chapter 3

OPERATION AND INTERFACE

3-1 INTRODUCTION

This chapter provides information concerning the interface requirements of the 8500 Series Disc Memory Unit. This information includes operation and timing considerations, interface signals, and interface logic levels.

3-2 OPERATION AND TIMING CONSIDERATIONS

The operation and timing considerations include basic timing, timing and control, write clock timing, track selection and timing, write mode and timing, and read mode and timing.

3-3 BASIC TIMING

When the track format for the 8500 Series Disc Memory Unit is being established, the following guidelines must be observed to ensure proper system operation:

1. Signal relationships with respect to the clocks are not variable.
2. Sector length can be same as track length.
3. A minimum of 32 bits of overhead is required per sector. This is controlled by the disc unit. No controller compensation is required. The controller transfers and receives only the actual number of data bits specified.
4. Spacing between sector clock N and track origin is as exact as it is between sector clock N-1 to sector clock N.
5. The disc unit is able to reliably read data 40 microseconds following a write operation, or track switching, or both simultaneously.
6. The gap between track origin and first sector clock signals are 40 microseconds.
7. Write clocks between track origin and first sector clock signals cannot be guaranteed with respect to number and phase.

3-4 TIMING AND CONTROL

Two types of timing and control signals are utilized in the 8500 Series Disc Memory Unit. These are the internal and the external timing and control signals. Internally generated signals are used within the disc unit and they are output from the disc unit to be used by

the controller. Externally generated signals are input to the disc unit to control track addressing, write, and read operations. The timing and control signals developed directly from the internal operation of the disc unit are track origin (TRACK ORIGIN), sector clock (SECTOR CLK), and write clock out (WR CLK OUT).

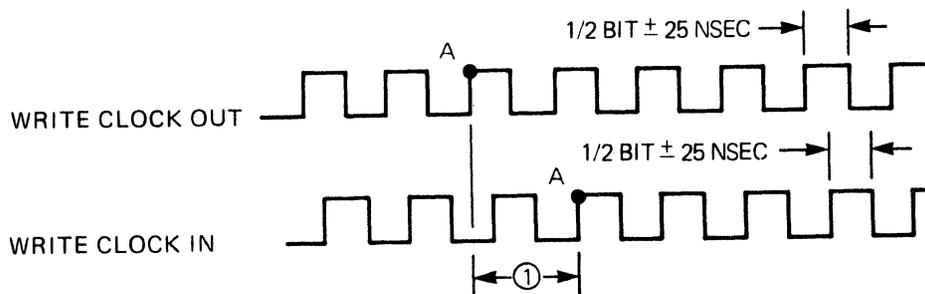
All internally generated timing and control signals are derived from a single clock track permanently recorded on the disc. Each recorded clock pulse on the disc is represented by a change in flux direction from the previously recorded clock immediately preceding it. The clock track is recorded at one half the data bit rate. The amplified, squared signal feeds a phase locked loop which multiplies the input signal frequency by a factor of two. This signal is identified as write clock out and it is sent to the external controller only to be returned to the disc unit. Write data (WR DATA) signal from the controller is clocked with the write clock in (WR CLK IN) signal which is the write clock out signal after being returned from the controller. The signal is processed to compensate for transmission line time delay between the disc unit and the controller (figure 3-1). Total distance between controller and disc unit must not exceed 30 feet.

The sector clock signal is detected from a single missing flux change on the disc clock track. This signal is output to the external controller and it is generated prior to each data sector on a disc track.

The track origin signal is produced once in each revolution of the disc by detecting the absence of two or more flux changes on the disc clock track.

3-5 WRITE CLOCK TIMING

The write clock out and write clock in signals are continuous clocks used to define each bit cell location. The write clock out signal is transmitted to the external controller and returned to the disc unit as write clock in. This feature allows the disc unit to be insensitive to cable and circuit delays. The timing relationships of the two clocks are shown in figure 3-1.



- ① ROUND TRIP CABLE, DRIVER/RECEIVER DELAY. ONCE ESTABLISHED MUST REMAIN CONSTANT $\pm 25 \text{ NSEC}$.

Figure 3-1. Write Clock Timing Diagram

3-6 TRACK SELECTION AND TIMING

Prior to any write or read operation, the appropriate track or head must be selected by the external controller. This process, known as addressing, is accomplished by eight binary address lines from the external controller to the disc unit. The read/write heads are organized logically, if not physically, in an 8X by 16Y matrix for each disc surface. The X-coordinates of the address are represented by the 8-line side of the matrix while the Y-coordinates of the address are represented by the 16-line side. At the junction of each X and Y line is a single addressable head.

To achieve the selection, three of the input address lines, T4, T5, and T6 are assigned to the X lines. These three lines are decoded to provide the eight X-coordinates; four of the input address lines, T0 through T3, are decoded to provide the 16 Y-coordinates. One input address line (bit 7) is used for disc surface selection. The address lines must remain stable for as long as the WRITE or READ signals are active (logical 0). If fewer than 128 tracks on each disc side are used the full addressing matrix is still valid and operational. If an address is given that is greater than the number of installed data tracks, the disc unit will output an illegal address command. In addition, provision is made in the internal X and Y select circuit so that a simple jumpering operation permits the selection of spare heads. A minimum of one spare (2 maximum) is provided for each 16 heads.

The track origin (TRACK ORIGIN) and sector clock (SECTOR CLK) output signals provide accurately the position of the rotating disc. The track origin signal occurs once per revolution to indicate the start of a disc revolution. The sector clock signal is recorded according to customer requirements and occurs at the beginning of each sector of data. Figure 3-2 provides the detailed timing relationship of the track origin and sector clock signals with respect to the write clock out signal.

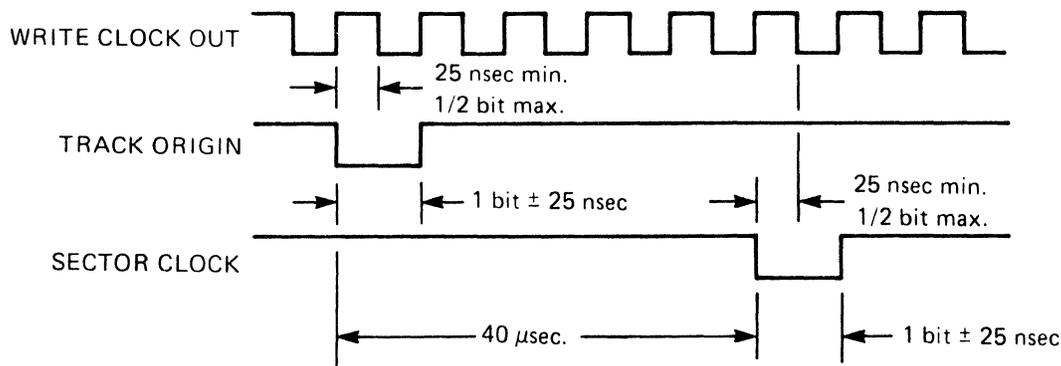
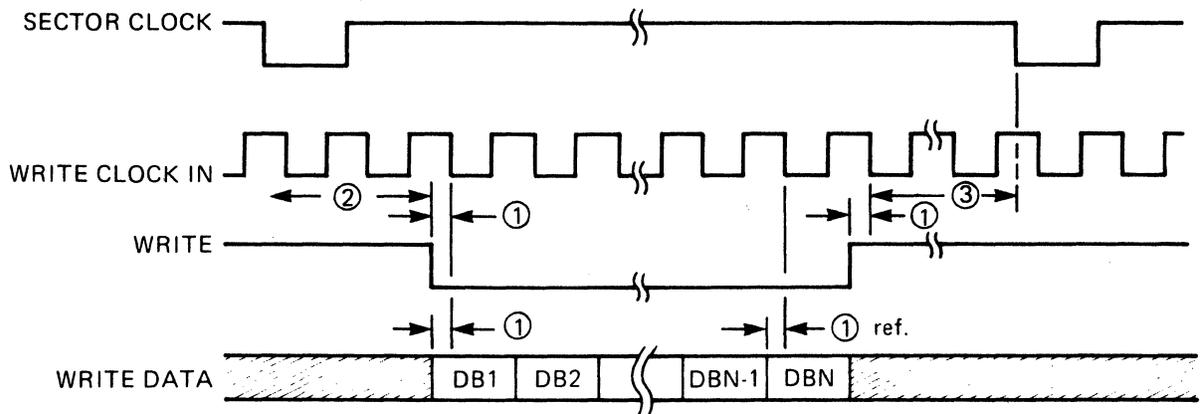


Figure 3-2. Basic System Timing Diagram

3-7 WRITE MODE OF OPERATION AND TIMING

The WRITE signal is generated by the external controller immediately upon receipt of the chosen sector clock signal. The WRITE signal is received by the disc unit with the falling edge of the write clock in (WR CLCK IN) signal. Simultaneously, upon generation of the WRITE command, the first data bit is placed on the write data line. Subsequent data bits will be generated synchronously with the write clock in signal. The write data is received by the disc unit with the falling edge of the write clock in signal. The WRITE command remains activated (logical 0) until the last data bit has been transferred, at which time the command is reset to a logical 1. If writing on more than one sequential sector is desired, the operation may be repeated at the next sector clock. Figure 3-3 provides the timing relationships for the writing. All operation timing shown is at the disc unit interface connector.

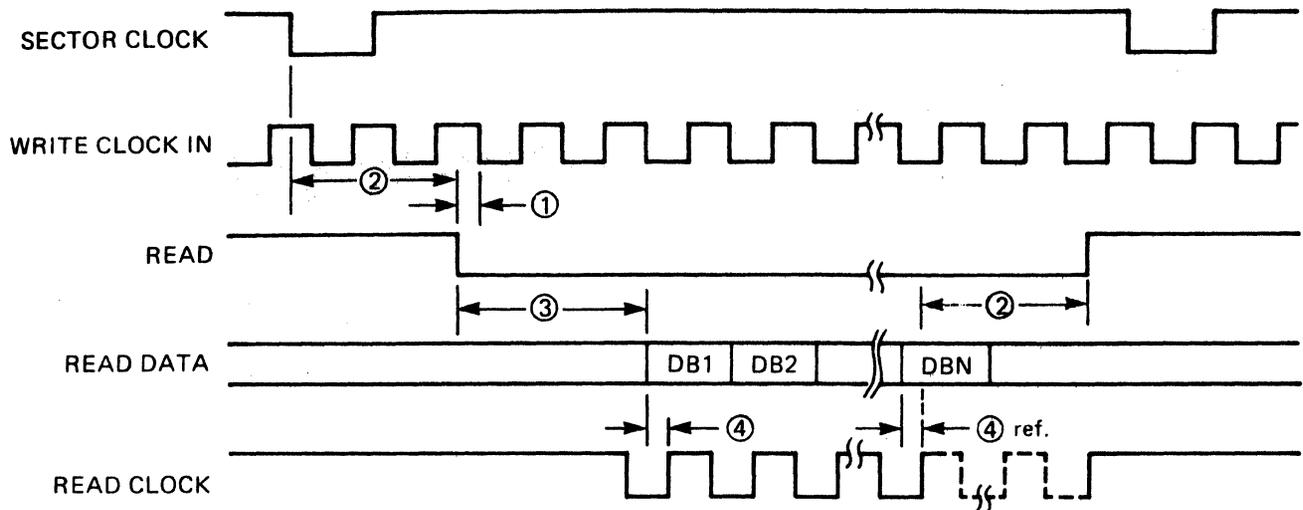


- ① 25 NSEC. MIN.; 1 BIT - 25 NSEC. MAX.
- ② TURN AROUND DELAY < 4 BITS. ONCE ESTABLISHED MUST BE CONSTANT ± 25 NSEC.
- ③ 36 BITS - ②

Figure 3-3. Write Mode Timing Diagram

3-8 READ MODE OF OPERATION AND TIMING

The READ command is generated by the external controller immediately upon receipt of the chosen sector clock signal. The READ command is received by the disc unit with the trailing edge of the write clock in signal. Typically, 20-bit times after receipt of the READ command, the disc unit generates the first read data bit and the read clock. The read data is received at the external controller with the rising edge of the read clock. The READ command remains activated (logical 0) until the last read data bit is received at the external controller, at which time the command is set to a logical 1. Depending upon signal turnaround delays, additional read clock signals are transmitted but they are ignored by the external controller. If more than one sequential sector is to be read, the operation is repeated at the next sector clock. Figure 3-4 provides the detailed timing relationships for the read mode. All timing shown is at the disc unit interface connector.



- ① 25 NSEC. MIN.; 1 BIT -25 NSEC MAX.
- ② TURN AROUND DELAY <4 BITS. ONCE ESTABLISHED MUST BE CONSTANT \pm 25 NSEC.
- ③ 24 ± 5 BITS.
- ④ 1/2 BIT +0/-20 NSEC

NOTE: 1) FOLLOWING RECEIPT OF DBN AND READ CLOCK N ADDITIONAL READ CLOCKS MAY OCCUR DUE TO TURN AROUND DELAY OF READ RESET. THESE CLOCKS SHOULD BE IGNORED.

Figure 3-4. Read Mode Timing Diagram

3-9 INTERFACE SIGNALS

The following paragraphs contain functional descriptions of the interface signals between the 8500 Disc Unit and external controller. These input/output signals are routed to and from the disc unit via a 50-pin connector. Figure 3-5 shows these signals between the controller and the disc unit.

3-10 UNIT SELECT

Four unit select lines are provided to support chaining up to four disc units on a single cable assembly. One line is assigned to a disc unit. Selection is made by the installation of a jumper according to figure 2-3. All disc units will be shipped with the unit select 0 jumper installed. The proper unit select line must be set to logical 0 to allow the disc unit to write, read or change track address. Following the end of a read operation, the unit stays selected for at least 1 μ sec. By adding a jumper from TP27 to TP28, when the unit is deselected, signals write clock out (WR CLK OUT), sector clock (SECTOR CLK), disc ready (DISC RDY), and TRACK ORIGIN are disabled (normal operation).

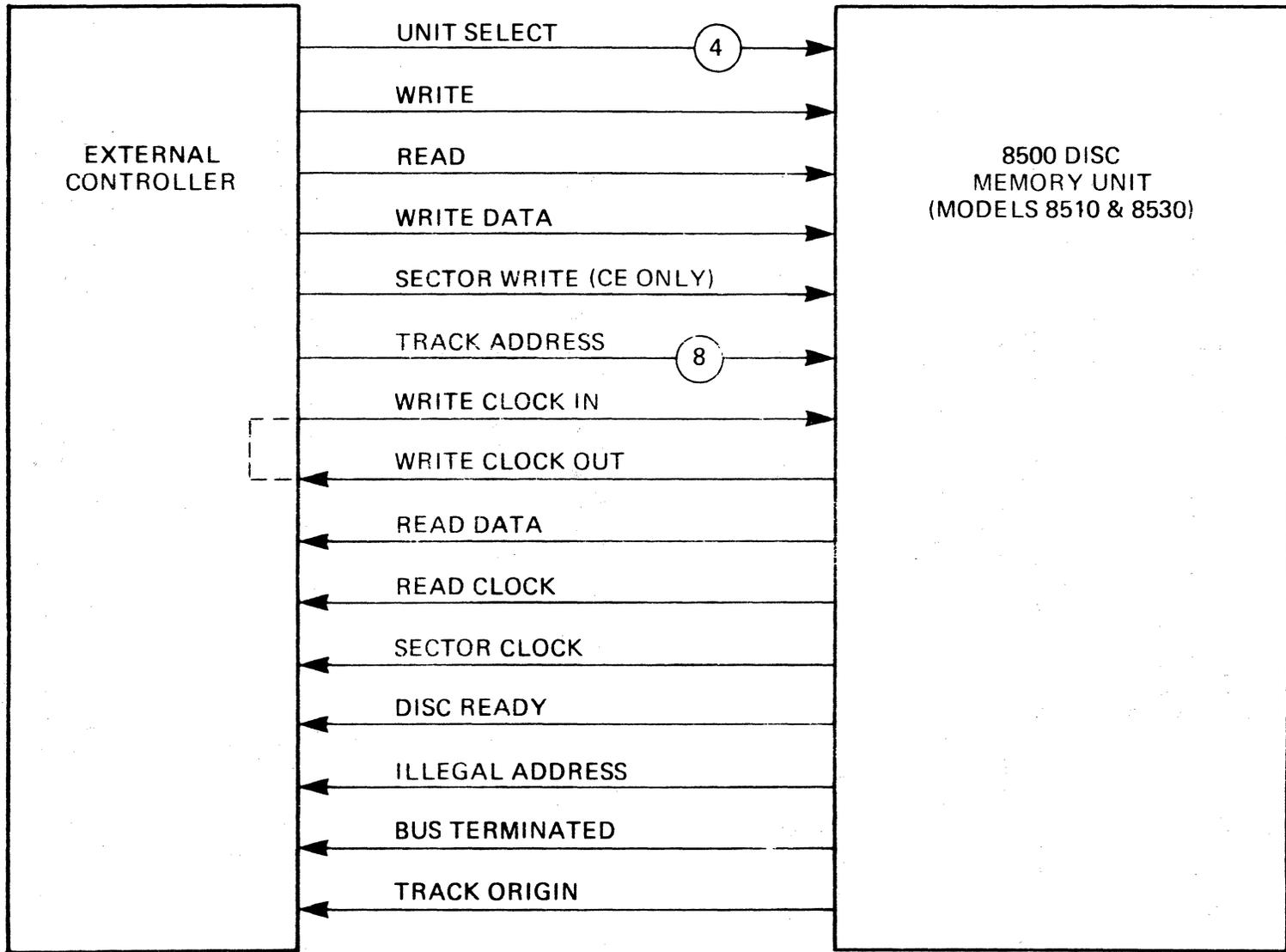


Figure 3-5. Disc Interface Signals

3-11 WRITE

When this signal to the disc is set to a logic 0, data on the write data (WR DATA) line is recorded on the selected disc track. The write (WRITE) signal must be set to a logic 0 synchronized with the sector clock (SECTOR CLK) signal (figure 3-3). The write signal remains at a logic 0 until the last bit of data has been transmitted and then is reset to a logic 1.

3-12 READ

When this signal to the disc is set to a logic 0, the read data (RD DATA) signal along with the read clock (RD CLK) signal are transmitted from the selected data head. The read (READ) signal is set to a logic 0 synchronized with sector clock (SECTOR CLK) signal (figure 3-4). The READ signal remains at a logic 0 until the last bit has been received and then is reset to a logic 1.

3-13 WRITE DATA (WR DATA)

This signal is input to the disc and carries the serial NRZ data to be recorded on the selected data head when the WRITE signal is a logic 0. The write data is transmitted with the write clock out (WR CLK OUT) signal and is received in the disc unit electronics with the write clock in (WR CLK IN) signal.

3-14 WRITE CLOCK IN (WR CLK IN)

This signal is the cable delayed version of the write clock out (WR CLK OUT) signal. Write data is received by the disc with this continuous clock. The write clock in signal must be present for a minimum of 36-bit period after sending the last write data (WR DATA) bit.

3-15 TRACK ADDRESS (TR A)

Eight lines to the disc unit provide the 8-bit binary address of the data head to which a write or read operation is to be performed. These lines must be present and stable as long as a write or read operation is performed. All eight lines are used regardless of the specific number of heads installed in the disc (256 maximum, 16 minimum).

3-16 SECTOR WRITE (SWD)

The clock format can be written with this line after the disc unit has been properly set up for initialization by a qualified customer engineer.

3-17 TRACK ORIGIN

The TRACK ORIGIN is a single pulse, one bit wide, defining the start of a disc revolution. This signal line, normally a logical 1, is pulsed to a logic 0 to indicate track origin.

3-18 READ DATA (RD DATA)

When READ signal is a logic 0, this signal line provides serial NRZ data from the selected data head in synchronism with the read clock (RD CLK) signal.

3-19 READ CLOCK (RD CLK)

This signal from the disc defines each bit of data to be read on the read data (RD DATA) output line. The read clock signal is present only when actual data is present on the read data line.

3-20 WRITE CLOCK OUT (WR CLK OUT)

The write clock out is a continuous clock signal defining each bit cell on the track. This signal is used to transmit write data to the disc unit and it is returned to the disc unit as write clock in (WR CLK IN) signal. The write clock out signal can be used to strobe the sector and track origin clocks into the controller.

3-21 SECTOR CLOCK (SECTOR CLK)

The sector clock is a single pulse, one bit wide signal that defines the start of a sector. All write and read commands are timed from the sector clock. This signal line, normally a logic 1, is pulsed to a logic 0 to indicate sector clock.

3-22 DISC READY (DISC RDY)

When this signal is a logic 0, the disc unit is ready to reliably transmit or receive data. In order to prevent a false disc-ready condition when the disc unit power is off, the DISC RDY signal is not terminated at the disc unit. The DISC RDY signal is set to a logic 1 under the following conditions:

- DC voltages below acceptable limits.
- Disc rotational speed below reliable operating range.
- BUS TERMINATED signal a logic 0.

3-23 ILLEGAL ADDRESS (ILLEGAL ADD)

This signal is set to a logic 1 when the received address exceeds the maximum address of the disc unit. In units equipped with write lockout feature, the ILLEGAL ADD signal is set to a logic 1 when the received address coincides with locked-out address as set by the lockout switches. When ILLEGAL ADD signal is a logic 1, it inhibits a write operation.

3-24 BUS TERMINATED

The BUS TERMINATED line senses the power to the disc interface terminations. A logic 0 on this line indicates a loss of power to the signal line terminations. All other interface lines should be considered invalid. The signal is not terminated in the controller.

3-25 INTERFACE LOGIC LEVELS

The logic is either 14-pin or 16-pin in-line packages with industrial operating temperatures ranging from 0°C to 70°C. All logic circuits are constructed with TTL integrated circuit chips of the small-scale and medium-scale integration type.

The signals to and from the disc are negative true except bus terminated (BUS TERMINATED) signal and illegal address (ILLEGAL ADD) signal. All signal lines are

terminated at both the controller and disc unit (figure 3-6) except the BUS TERMINATED signal which is terminated at the disc unit, and the DISC RDY signal which is terminated at the controller.

Interface logic levels are as follows:

Logic 0	0 vdc nominal +0.4 vdc maximum
Logic 1	+2.4 vdc minimum +2.7 vdc nominal +5.25 vdc maximum

Every line is driven to ground by an NPN transistor collector that is capable of sinking 48 ma and maintaining a maximum saturated output voltage of 0.4 volts.

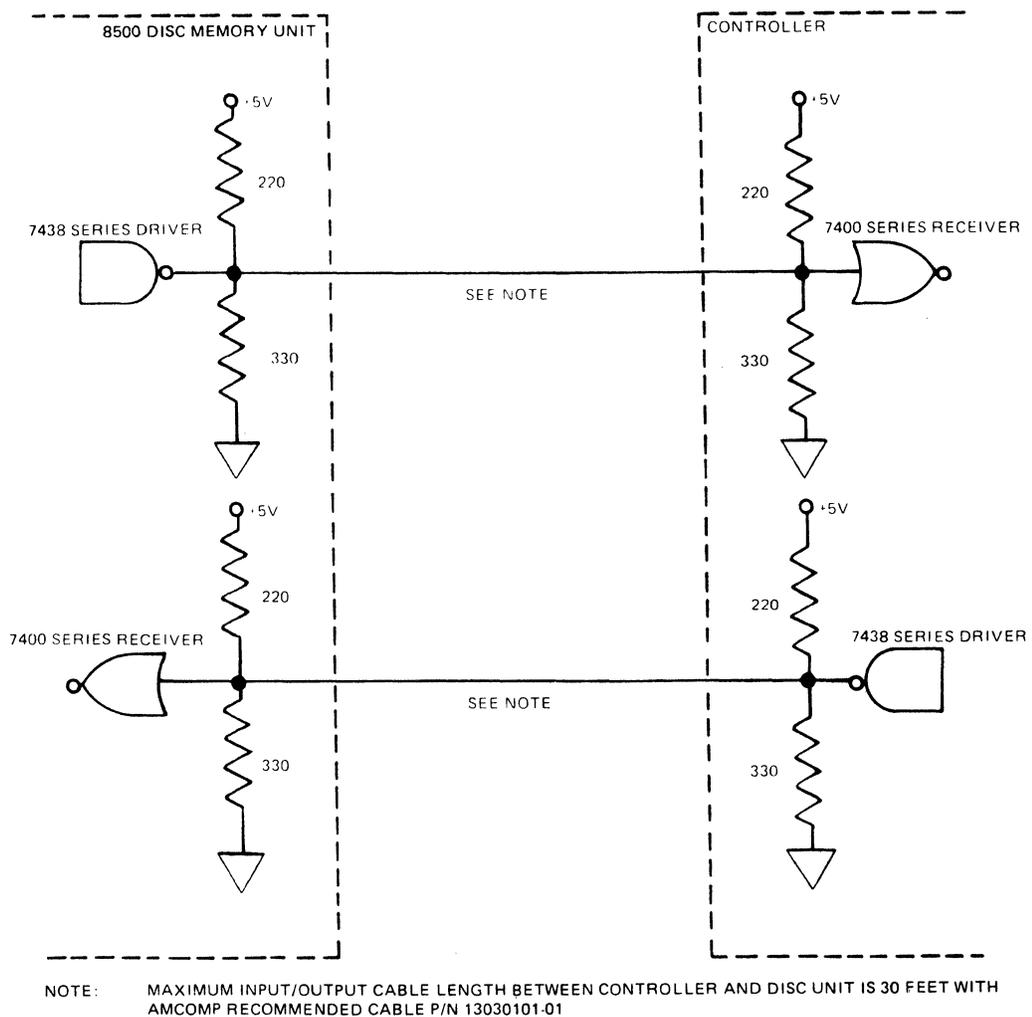


Figure 3-6. Typical Interface Driver Terminating Resistor Network Schematic Diagram



Chapter 4

THEORY OF OPERATION

4-1 INTRODUCTION

This section provides a detailed functional description of the circuits within the 8500 Series Disc Memory Unit. Individual electronic circuits are discussed only to the level of their contribution to overall functional data flow. For a detailed explanation of the theory of operation of discrete circuits or IC's, consult the appropriate source documentation. The material in this chapter must be read by maintenance personnel to gain a working understanding of the disc unit prior to performing any of the maintenance procedures contained in chapter 5. A brief description of disc and NRZI recording is also provided.

4-2 LOGIC DIAGRAM AND SIGNAL INFORMATION

Generally, all logic symbols appearing in the logic diagrams contained in this manual are drawn in compliance with MIL-STD-806 (latest revision). All logic units are identified by a reference designator, such as U1, U2, etc., indicating the integrated circuit where the element is located. In text, the pin number of the integrated circuit package follows its reference designator (i.e., U2-6). The assembly schematic and logic diagrams should be referred to when reading this chapter.

The signals from/to controller are low-true except for the BUS TERMINATED and ILLEGAL ADDRESS which are high-true. The signals within the disc unit are either low-true or high-true, depending upon the particular signal.

The low-true signals carry a bar across the top of the signal term (i.e., $\overline{\text{WR DATA}}$), while the high-true signals are presented plainly (i.e., WR DATA).

NOTE

The interface signals and their logic levels are described in chapter 3; their origin and destination are listed in table 2-1.

The disc unit internal logic is standard positive having the following levels:

Logic 0 (low) = 0 to +0.4 volts
Logic 1 (high) = 2.3 to +5.0 volts

The AMCODE adapter uses ECL logic in some of its circuits (1940077, Sheet 5). ECL logic levels are as follows:

Logic 0 (low) = -1.8 volts
Logic 1 (high) = -0.9 volts

4-3 KEY TO BASIC SYMBOLOGY

Figure 4-1 shows the gate as well as the JK and D-Type flip-flop symbols together with their truth tables.

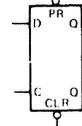
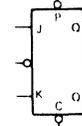
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Figure 4-1. Logic Symbols

4-4 FUNCTIONAL DESCRIPTION

The 8500 Series Disc Memory Unit functional block diagram (figure 4-2) shows the relationship between the functional elements of the disc unit.

All functions of the disc unit are selected and controlled by the external controller. Track addresses are input to select the appropriate track/head combination by signals on the eight track address lines TR-A-0 through TR-A-7. Read operations are initiated by the external controller utilizing basic timing signals derived from the disc unit.

4-5 DATA RECORDING

To write data on the disc, current is passed through the magnetic recording heads which are positioned near the surface of the disc. As the magnetic recording medium on the disc surface passes by the gap in the head (see figure 4-3), that portion of the disc surface becomes magnetized in a direction corresponding to the direction of the current in the head, and thus the data is encoded magnetically on the disc surface. When the current is reversed in the head, the direction of the magnetization is also reversed and there are therefore two possible states of magnetization on the disc surface. Note that in either direction the current in the head is sufficiently high to saturate the magnetic particles on the disc and erase all previous data.

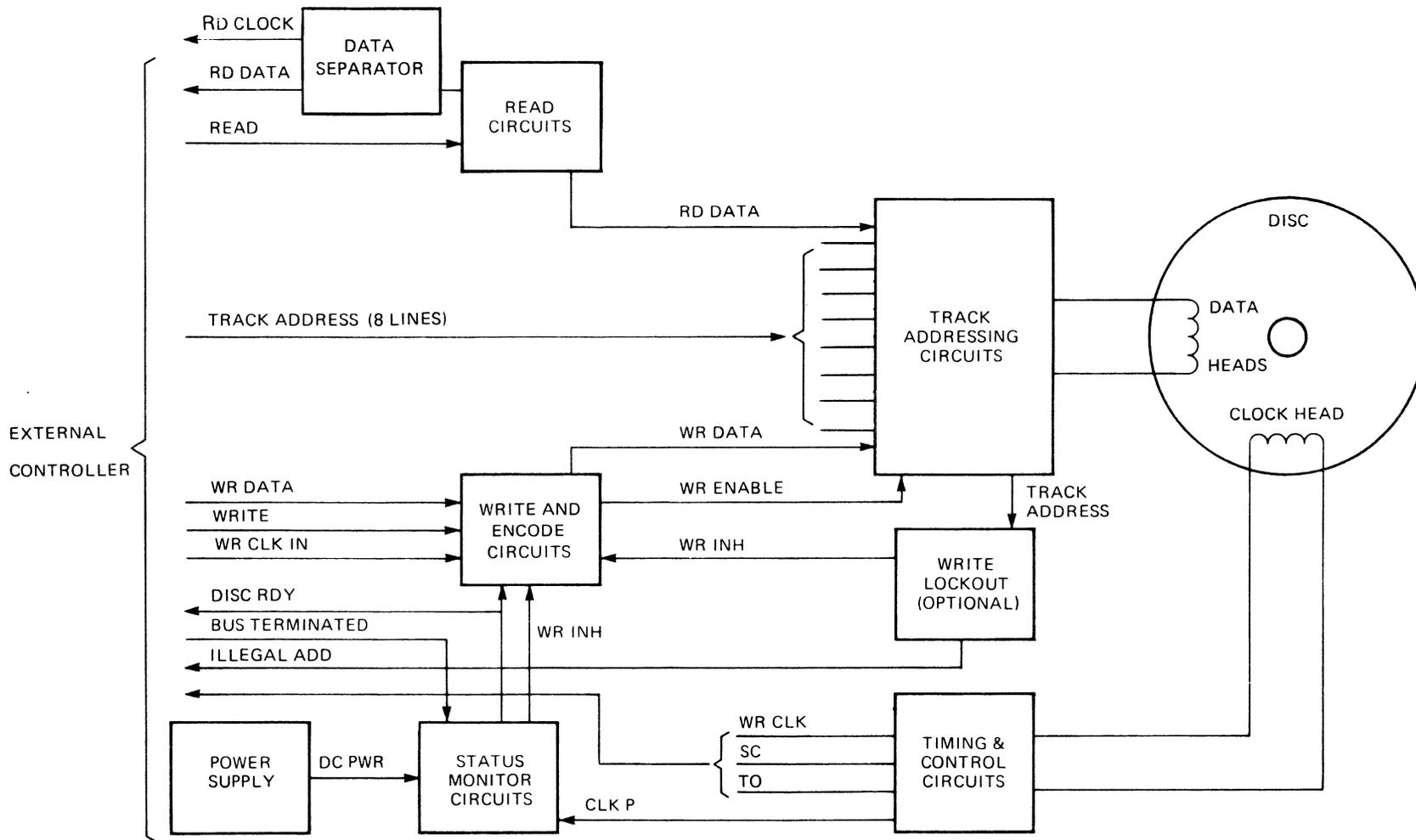


Figure 4-2. 8500 Series Disc Memory Unit Functional Block Diagram

In reading the stored data, any flux changes on the surface of the disc induce a voltage in the head as the disc surface passes under the head gap. There is no output from the head until a change in flux passes under the head. Each flux direction transition produces a Gaussian shaped voltage pulse, as shown in figure 4-3.

Each data bit is stored in a "bit cell" on the disc. The bit cell is the angular portion on the surface of the disc within which a data bit is stored and is normally measured in units of time. The time it takes the disc to rotate one bit cell is measured by the bit clock. In the 1800 rpm, 150,000 bit-per-track disc unit, this time is 222 nsec and in the 3600 rpm, 150,000 bit-per-track disc unit this time is 111 nsec.

Although all disc memories operate on these principles, there are several methods of encoding data bits into magnetic flux changes and vice-versa. One such method is the AMCODE method, described in the following paragraph.

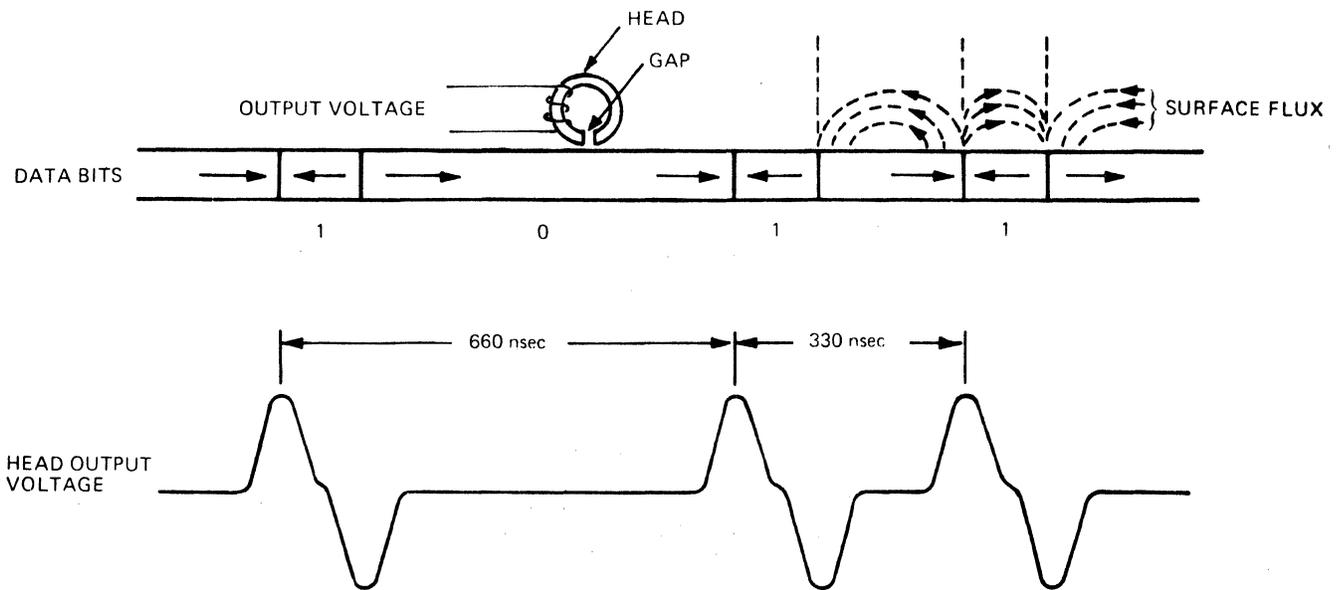


Figure 4-3. Magnetic Recording Details

4-6 DATA RECORDING BY THE AMCODE METHOD

The AMCODE method of data recording is basically MFM (modified frequency modulation) and allows data to be written on the disc such that the read data will be self clocked. AMCODE data recording also allows the maximum sector length to be unrestricted. Minimum sector length is 28 data bits.

The AMCODE data recording method (figure 4-4) causes the magnetization of the disc track to change polarity in the center of a bit cell for logic 1 data. A logic 0 causes the magnetization to change polarity at the end of a bit cell if the next bit is a logic 0 (if the next data bit is a logic 1 no change in polarity occurs).

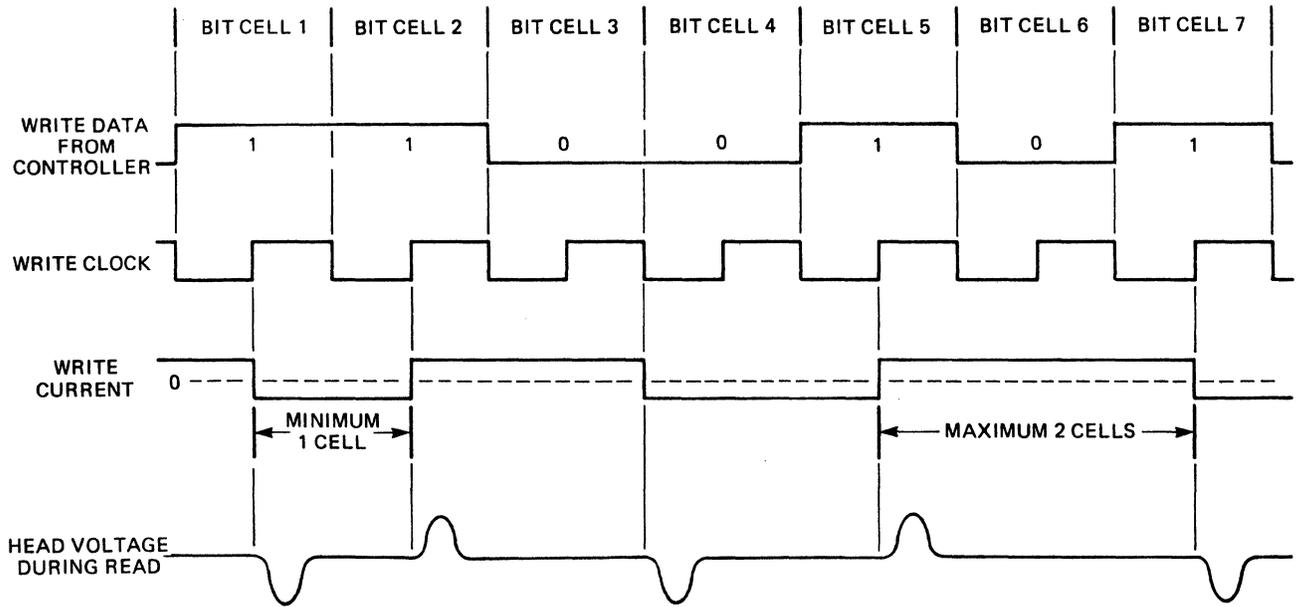


Figure 4-4. Construction of AMCODE Logic 0 and Logic 1 Data Bits.

As a result of writing the AMCODE pattern the maximum spacing between changes in magnetization is no greater than two clock periods, providing self clocking of the read data.

4-7 CIRCUIT DESCRIPTIONS

The electronics of the 8500 Series Disc Memory Unit are functionally divided into the timing and control circuits, track address circuits, write circuits, read circuits, and status monitor circuits. Figure 4-2 shows the relationship between the functional elements of the unit. The following paragraphs provide a detailed functional description of these circuits. Also included are descriptions of the power supply and the optional write lockout circuit.

4-8 TIMING AND CONTROL CIRCUITS

The timing and control circuits consist of the clock amplifier and a phase locked loop (PLL) that is used to extract the write clock out (WR CLK OUT), the track origin (TO) and sector marks (SM) signals from the recorded bit clock. The clock amplifier accepts the recorded bit clock from the disc clock track, processes the bit clock and applies the clock as a pulse train (CLK PLS) to the remainder of the timing and control circuits. CLK PLS is used to control the phase locked loop by comparing the CLK PLS with a 1/4 frequency feedback from the phase locked loop. This adjusts the WR CLK OUT and RD CLK frequencies to exactly twice that of the recorded bit clock regardless of the speed of the disc. RD CLK is output only during a read operation. Signals TO and SM are detected from the CLK PLS as an absence of flux changes on the recorded disc clock track. Signals TO and SM are output to the external controller to provide accurate position data on the disc. The following paragraphs provide a detailed description of the timing and control circuits.

4-9 CLOCK AMPLIFIER CIRCUITS

Refer to diagram ¹⁰⁴⁰⁰⁷~~104007~~ sheet 5. The bit clock, recorded on the disc at one-half the data frequency, is read directly from the disc and fed to the memory board circuit. Voltage induced in the clock track head is fed to the AC coupled amplifier, A1, on the clock preamplifier card. The clock preamplifier amplifies the bit clock by a factor of approximately 100 and also provides common mode noise rejection.

The amplified bit clock signal output of the clock preamplifier is then fed through connector J4 to the clock amplifier circuits located on the memory board. The bit clock is applied through a low pass filter network to the input of variable gain amplifier A1. Amplifier A1 on the memory circuit board is a differential amplifier with a variable gain that can be set between 10 and 100. The analog output of the variable gain amplifier is adjusted to provide 5 volts peak at TP9.

The analog outputs of differential amplifier A1 on the memory circuit board are applied to a differential amplifier consisting of Q5 and Q2. The outputs of Q5 and Q2 are applied through emitter followers Q4 and Q3 to rectifiers CR3 and CR1. The rectifier output is differentiated by C20 and R29 and applied to comparator U1 pin 1. The comparator output, internal to the chip, is allowed for high transition for every peak of the rectified signal. Also the comparator switches on noise peaks and when no signal pulses are present. To discriminate legitimate input pulses from noise a window is generated by the second comparator of U1. A noise threshold is established by the comparison of the ground reference versus the rectified signal at TP9 whose baseline is shifted to -2.1Vdc. The threshold is then an effective 40% of the peak value. The discriminated peaks appear at TP10 as high to low transitions. They trigger an output pulse at TP10 whose width is adjusted by R35. Refer to chapter 5 for adjustment procedure.

4-10 PHASE LOCKED LOOP

Refer to diagram 1940077 sheet 2. The phase locked loop (PLL) is used to generate write clock out (WR CLK OUT), track origin (TO) and sector clock (SC) from the information recorded on the clock track.

The PLL consists of a phase detector (PD), low pass filter (LP), voltage controlled oscillator (VCO), and a divide-by-4 counter.

The PD will generate a positive or negative error signal whenever the phase of the feedback frequency (Ffb) lags or leads that of the reference frequency (Fref) respectively. The error signal will be integrated by the LP and applied to the VCO which in turn will adjust its frequency output such that when divided by 8 the resulting frequency (Ffb) will exactly follow the Fref and reduce the error voltage to zero. If the data frequency which is the same as the WR CLK OUT frequency is defined F, the reference frequency Fref or CLK PLS will be F/2, the VCO output frequency will be F4 and the RD CLK frequency will also be F.

The frequency of VCO, U9, is controlled by the control voltage from filter and integrator U8.

The output of the VCO is applied to frequency divider, U18, which divides the F2 output of the VCO to 1F, generating the write clock signal, WR CLK OUT. The F/2 output of the frequency divider is applied to phase detector, U7, and the clock decode circuits.

4-11 CLOCK DECODER

Refer to figures 4-5 and 4-6, and to diagram 1940047 sheet 3. The phase locked loop (PLL) aligns the leading edge of feedback frequency (Ffb) and reference frequency (Fref) placing the leading edge of the input to U16-3 and U16-11 (B7) approximately in the middle of the negative going pulse of CLK PLS. Thus, U28 can detect the presence or absence of a pulse in CLK PLS well before the leading edges of Ffb. When a missing pulse is detected, the phase detector is disabled to prevent a false error signal from being generated at the output of the phase detector. The detected missing pulse is loaded in a 2-bit shift register to generate a track origin mark (TO) or a sector clock (SC), the former being encoded as two consecutive missing pulses and the latter as one missing pulse.

Being encoded at half frequency, TO or SC signals are decoded as 2-bit wide pulses and U27 limits them to a one-bit wide pulse centered about the leading edge of WR CLK OUT.

The clock track is recorded in such a way that closure or splicing occurs following a TO mark. Hence when TO has been detected, a one-shot (U26) is fired for 30 μ sec inhibiting any invalid sector clock (SC) or track origin (TO) from being decoded while the PLL is recovering from a possible phase change resulting from the splicing.

4-12 SELECTION MATRIX

The heads in both sides of the disc are arranged in an XY-matrix fashion made up of 16 differential head lines and 36 centertrap Y lines for a maximum of 288 heads of which 32 are used as spares. The Y lines are divided into 16 regular lines and 2 spare Y's for each disc side. Refer to schematic diagram 1940046 sheets 2 and 3 and block diagram, figure 4-7.

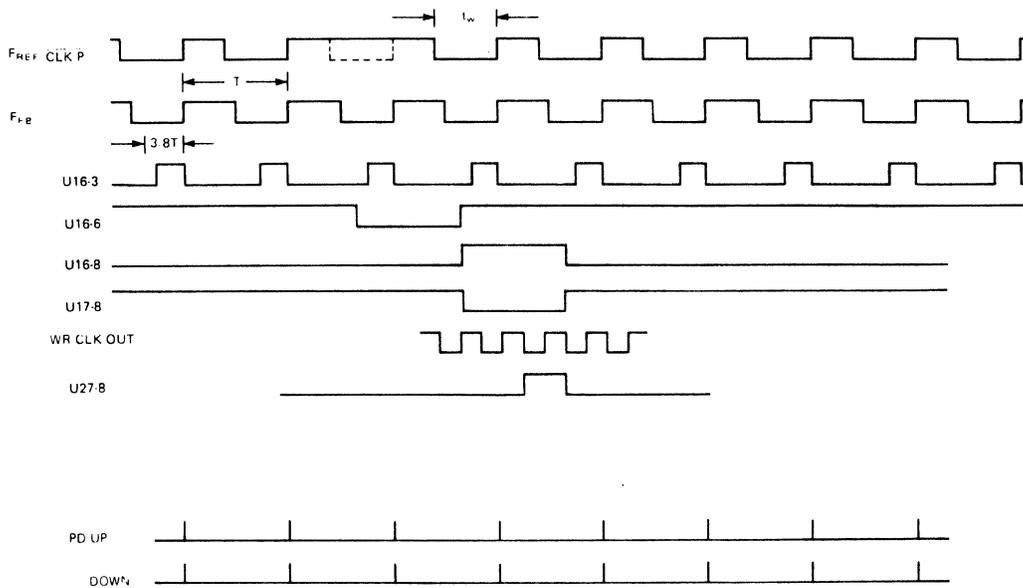


Figure 4-6. Clock Decoder Timing Diagram

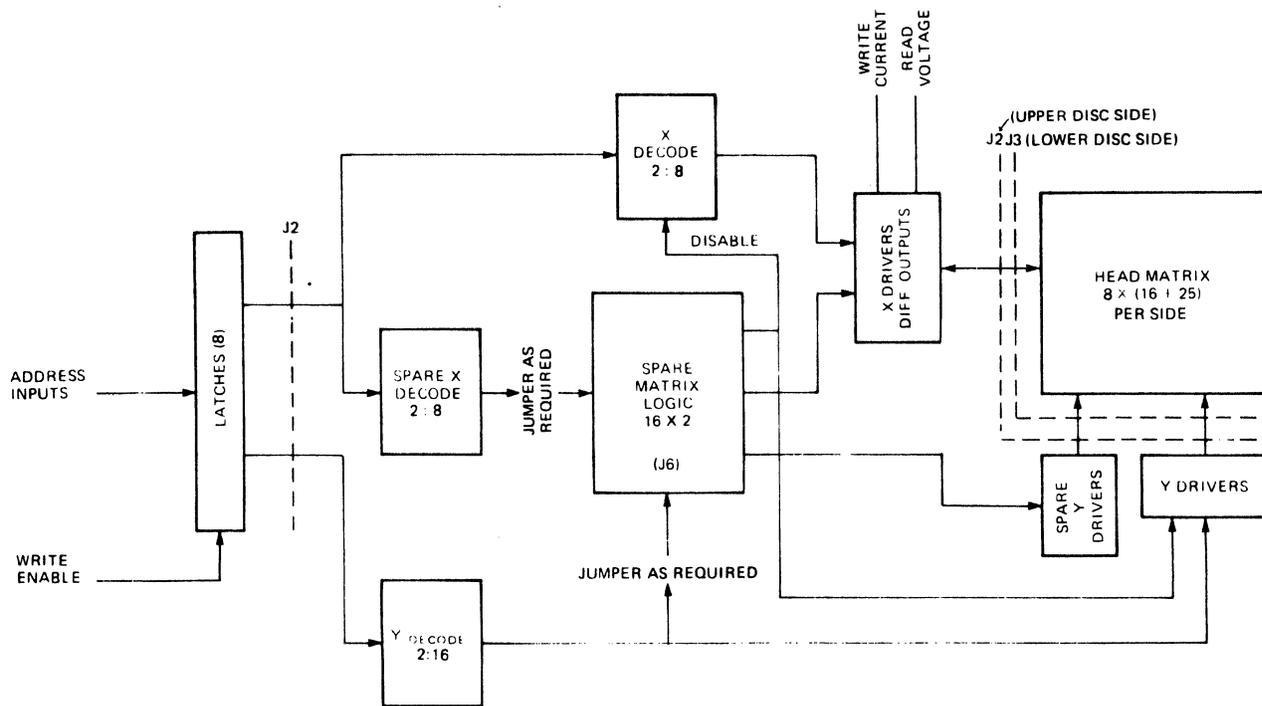


Figure 4-7. Address Selection Matrix Block Diagram

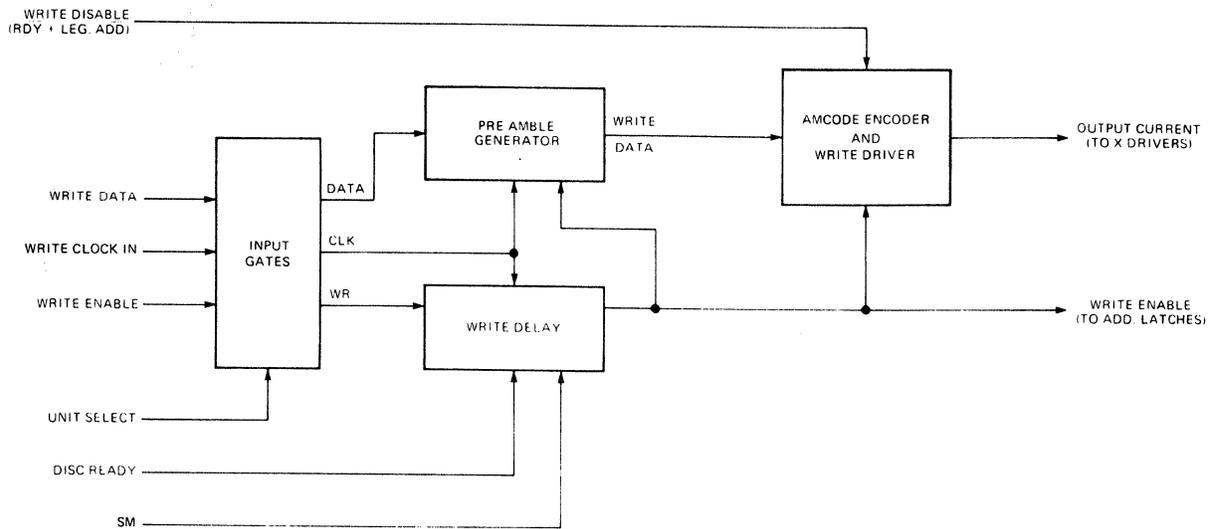


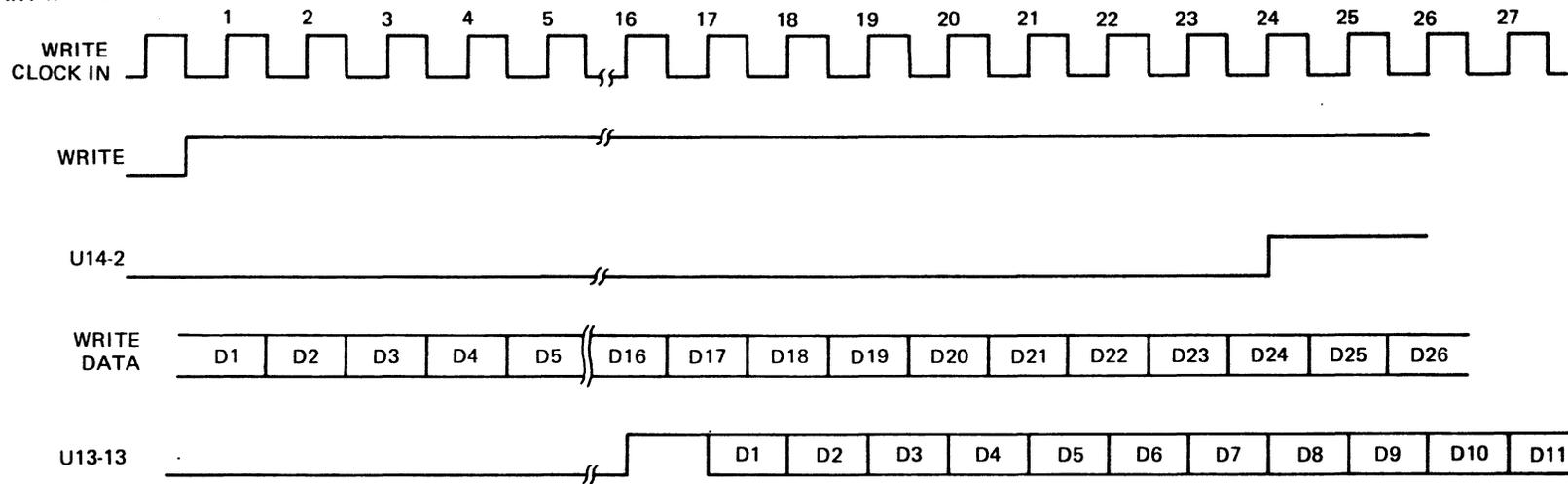
Figure 4-8. Write Mode Circuits Logic Block Diagram

The controlling signals, WR DATA, WR CLK IN and WRITE are gated by the write select line in sheet 3 of the AMCODE adapter board schematic (1940077). The preamble is used for threshold setting and phasing of the data separator VCO during a read operation. The preamble is generated by a shift register (1940077, Sheet 4) consisting of IC's, U31, U22, and U13 (the output at U13-3 is low for logic 1 and high for logic 0). The postamble bits are generated by delaying the write enable (WEN) for a longer period than is required to write the data bits on the disc. The write enable is delayed by a shift register consisting of IC's, U30, U39, and U40.

The output of the preamble shift register is applied to the AMCODE write encoder consisting of flip-flops U31 and U32 and gates U23-6, U23-8, and U23-12. Depending on the pattern, the two flip-flops gate one phase of the 1XOSC clock to flip-flop U32-2. When a 1 bit is to be written an output appears at DATA output U23-8 at the center of the bit cell. A 0 bit causes an output at CLK, U23-6 at the end of the cell. These outputs are clocked into flip-flop U32-2 by the 2XOSC clock which causes the flip-flop to generate an MFM pulse from U32-5 to the write driver.

A not ready condition will reset the write delay and shut off write current to the write driver. An illegal condition determined by the write lockout option will also disable the write driver.

A. START WRITE



B. END WRITE

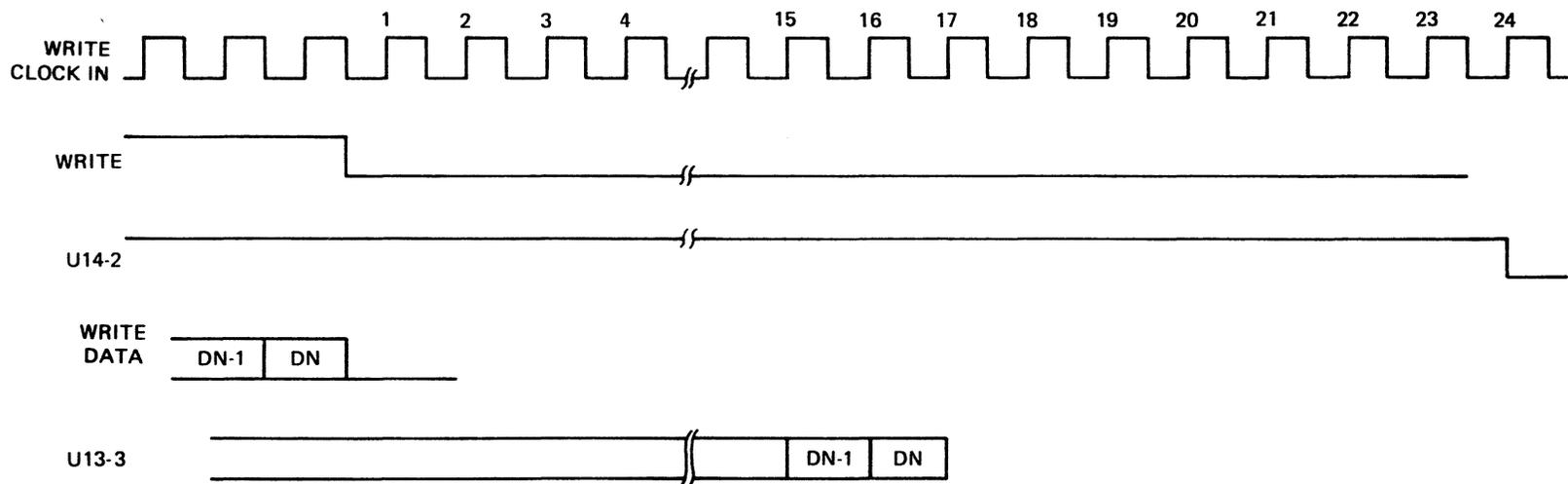


Figure 4-9. Write Mode Timing Diagram

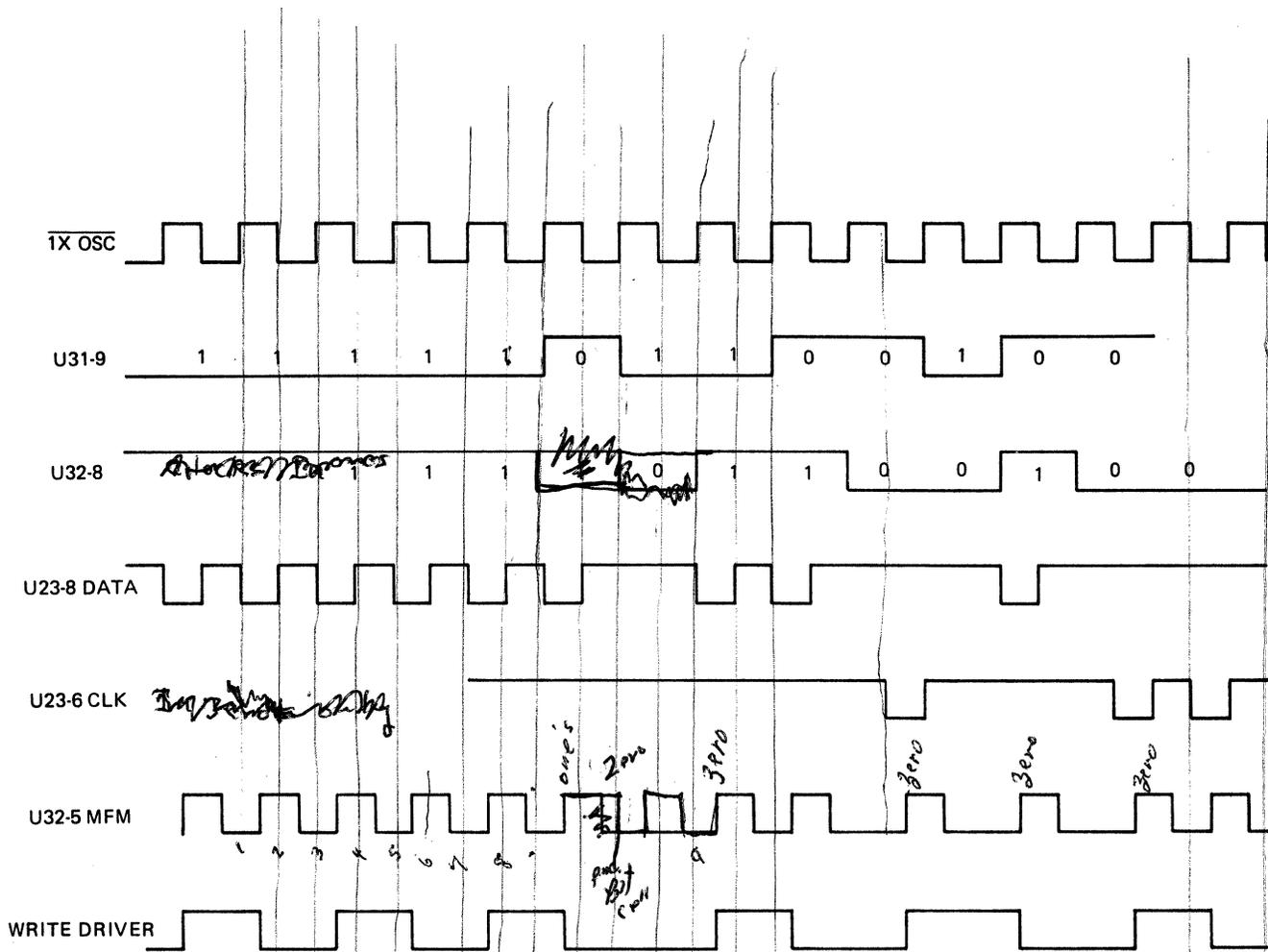


Figure 4-10. AMCODE write encode, Timing Diagram

4-14 READ MODE

Refer to AMCODE adapter board diagram 1940077, sheets 4 and 5 and figure 4-11. The read mode logic contains a read control section and a data separator. The read control section inhibits the preamble information originally written at the beginning of the sector from being sent to the controller. The data separator extracts NRZ data from the AMCODE data pattern and generates a read clock that is synchronized to the data. The read clock is continuously corrected in phase and frequency by the data.

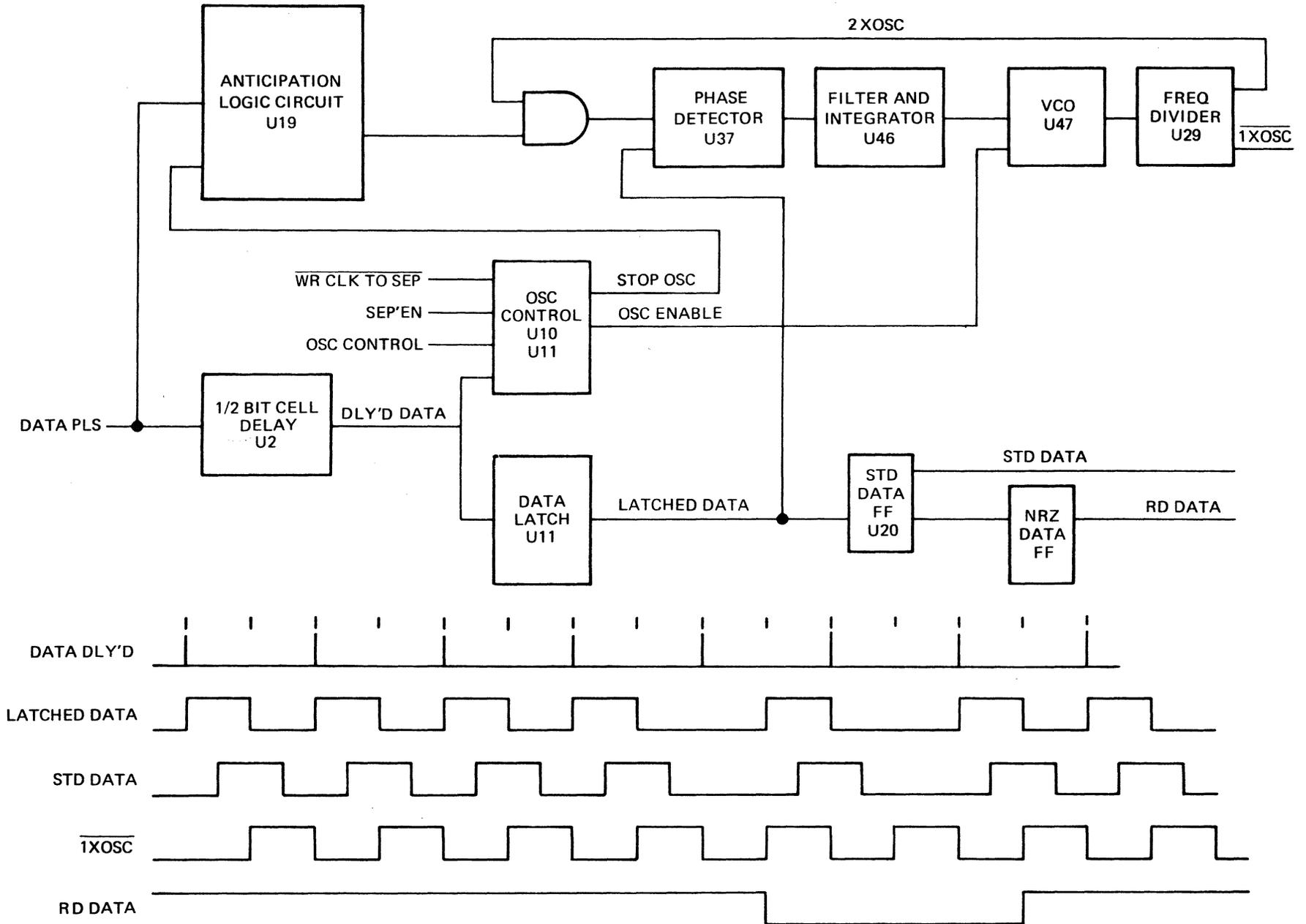


Figure 4-11. Data Separators, Simplified Diagram

When the read command signal READ is received, the DGAT and FETON signals are generated from shift register U15 and U24. DGAT and FETON are used to preset the read amplifier threshold current. After a delay of 9 bits, the data separator enable signal (SEPEN) is generated from shift register U15. Prior to the generation of the SEPEN signal, the data separator VCO was synchronized to the write clock by the WR CLK TO SEP signal to allow it to oscillate at the data frequency.

When the SEPEN signal is active, the OSC CONTROL signal is generated, which causes the VCO to be momentarily stopped. Since the VCO can be restarted in phase with a pulse train, it is restarted by the read data pulses which are the same frequency as the write clock but at a different phase. The VCO is now synchronized in phase and frequency with the read data. The output of the VCO, 4XOSC, is four times the input frequency and is divided to two times the frequency (2XOSC) and one times the frequency (1XOSC) by divider U29. The read data pulses (DATA PLS) are applied to delay line U2 and to anticipation logic circuit U19. The 2XOSC clock from the divider is applied to phase detector U37. The delay line delays the data pulses by one-half the bit cell time and applies them to latch data flip-flop U11. Delayed data pulses from the data latch are also applied to the phase detector.

Since a read data pulse does not occur for each 2XOSC pulse, the anticipation logic circuit allows the phase detector to sample a 2XOSC pulse only when a delayed data pulse from data latch flip-flop U11 is present. The delayed data pulses from the data latch flip-flop are also applied to STD DATA flip-flop U20 along with the 2XOSC pulses from the divider. The STD DATA flip-flop removes the effects of jitter in the data pulses and applies the data to NRZ data flip-flop U20.

The 1XOSC pulses strobe the data from the NRZ data flip-flop in NRZ form. The NRZ data is applied to ECL to TTL translator U21 which transmits the RD DATA to the external interface and to flag decoder U41 (1940077, sheet 4). The flag decoder detects the 0 bit that is written at the end of the preamble to generate the read clock enable (RD CLK EN) signal. The RD CLK EN signal enables read clock (RD CLK) signal which is sent to the internal interface from gate U42-11 (1940077, sheet 2).

4-15 READ MODE (DATA AMPLIFIER AND THRESHOLD SAMPLER)

Refer to memory board diagram 1940046 sheet 4 and figure 4-12. Once selected by the matrix decoder, the desired head voltage is applied to the input of the data amplifier. At the amplifier, the head signal is first preamplified by a factor of 100 and then passed through a low pass filter. ($F_{3db} = 8$ MHz typical at 3600 rpm.) After the low pass filter, the signal is further amplified by an amplifier which has a variable gain. The differentiator produces an output signal which crosses zero volts whenever the input signal reaches a peak value. The resulting signal is applied to a comparator or squaring amplifier, whose output signals change states whenever their inputs are at zero. To discriminate the desired peaks from the undesired ones due to noise and no-signal conditions, the output of

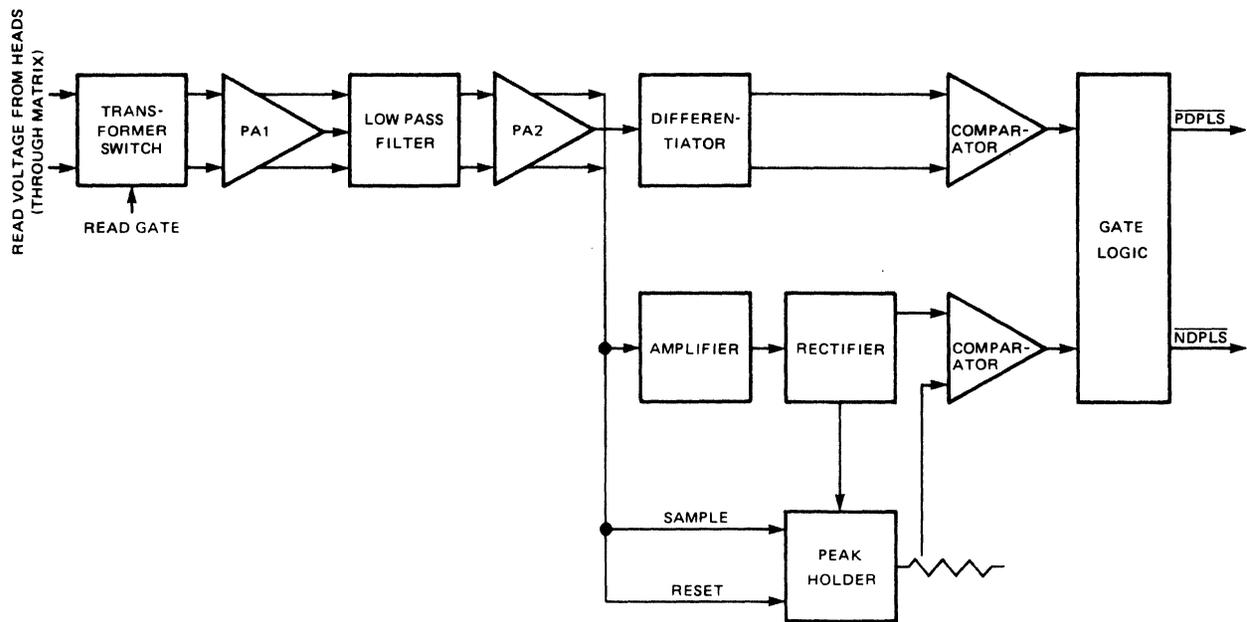


Figure 4-12. Read Circuit Amplifier

third amplifier is rectified and compared against a threshold by the threshold comparators. The outputs of the latter form a window about each peak and allows each to be captured by the output gates.

To obtain a threshold reference, which will remain a fixed percentage of the nominal peak values of the head signals, a peak sampling and holding circuit is used and it operates as follows: each data block is preceded by a preamble as discussed in the write mode section, which begins with a series of "ones". For a five-bit time period, a diode gate and an FET switch are turned on. Since current flow is to one direction by the diode gate, holding capacitor will charge up to the peak of the input signal and remain there. During the remainder of the preamble and data block, the charge on the capacitor through a buffer will be divided to 30% typically and used as a threshold. At the end of the read operation, the bottom half of the diode gate is turned on allowing current to flow in both directions and the capacitor is allowed to discharge.

4-16 READY CIRCUIT

Refer to schematic diagram 1940046 sheet 6 and figure 4-13. The ready circuit provides a disc-ready status whenever five conditions are met. These are the three DC power supplies which must be above their minimum tolerances, the disc must be up to speed and the I/O bus must be properly terminated. Five discrete comparators are used; their outputs are collector-Ored and level shifted. A voltage reference is developed and used, through appropriate attenuators, for trip point settings. The clock pulse ($\overline{\text{CLK P}}$) frequency is converted to a voltage and compared against a reference for the monitoring speed. All comparators use hysteresis to protect against transient switching noise. The circuit outputs a $\overline{\text{RDY}}$ signal to the interface logic and I/O bus, and also inhibits power to the write driver. The $\overline{\text{ILLEGAL ADD}}$ signal also inhibits power to the write driver but does not generate a not-ready condition.

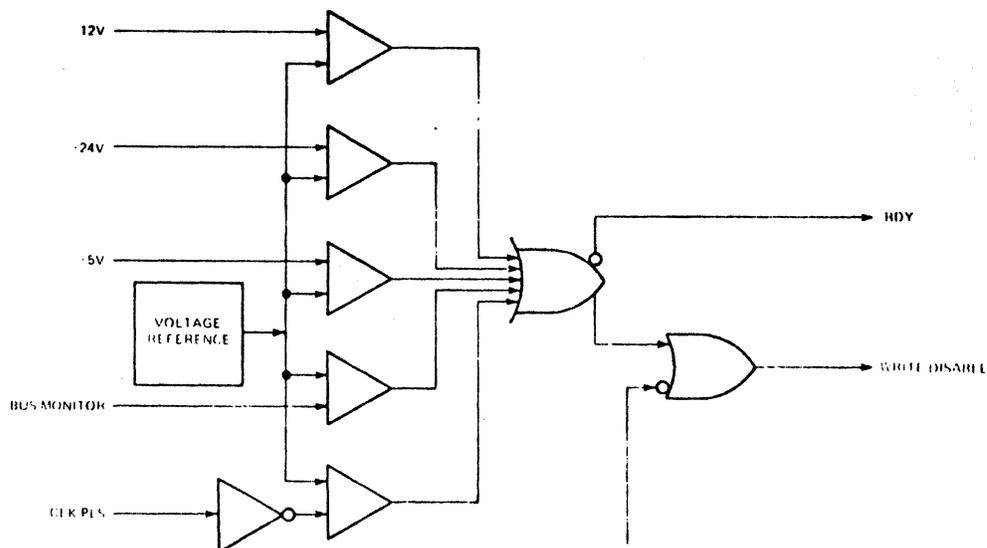


Figure 4-13. Ready Circuit

4-17 POWER SUPPLY CIRCUITS

The power supply provides +24 Vdc at 0.6 amps, +5 Vdc at 4.5 amps, -5.2 Vdc at 1.5 amps, and -12 Vdc at 0.6 amps. The +5 Vdc output of the power supply is adjustable to $\pm 1\%$ by a potentiometer on the power supply printed circuit board. Refer to the power supply schematic in chapter 6. The 24Vdc, -12 Vdc, and -5.2 Vdc outputs of the power supply are not adjustable. The +24 Vdc and -5.2 Vdc outputs are regulated within $\pm 3\%$ and the -12 Vdc output is regulated within $\pm 4\%$. The power supply circuit consists of transformer T1 and the heatsink assembly. Four regulator circuits and one rectifier are contained on a printed circuit board located on the heatsink assembly. Two rectifiers are mounted directly on the heatsink assembly.

A temperature sensitive switch located on the heatsink assembly will turn off the +5Vdc, +24Vdc, -12Vdc, and -5.2Vdc voltages in the event of a blower failure or if the disc unit overheats.

4-18 WRITE LOCKOUT CIRCUITS (OPTIONAL)

The optional write lockout feature circuits consist of 16 switches, mounted on the front panel of the chassis assembly, and 2-line to 4-line decoder/demultiplexer chips U1 and U2 mounted on the mini mother board (logic diagram 1040060). The inputs to the write lockout circuits are T4, T5, T6 and T7 from the address decode circuits U1 and U2 in the mini mother board. Each of the switches S1 through S16 protects a specific group of 16 tracks on the disc. Table 4-1 contains the assignments of the lockout switches according to the logic state of the inputs. For example, if switch S5 were on and any of tracks 64 through

79 were addressed by the external controller, the write lockout circuits would supply an illegal address command to the voltage monitor circuits in the disc unit. This would cause the voltage monitor circuits to inhibit writing on the disc by shutting off write current to the write amplifier circuits and would also provide an illegal address output to the external controller.

TABLE 4-1. WRITE LOCKOUT LOGIC INPUTS AND SWITCH ASSIGNMENTS

T7	T6	T5	T4	SWITCH	TRACKS PROTECTED	
					OCTAL	DECIMAL
0	0	0	0	S1	0-17	0-15
0	0	0	1	S2	20-37	16-31
0	0	1	0	S3	40-57	32-47
0	0	1	1	S4	60-77	48-63
0	1	0	0	S5	100-117	64-79
0	1	0	1	S6	120-137	80-95
0	1	1	0	S7	140-157	96-111
0	1	1	1	S8	160-177	112-127
1	0	0	0	S9	200-217	128-143
1	0	0	1	S10	220-237	144-159
1	0	1	0	S11	240-257	160-175
1	0	1	1	S12	260-277	176-191
1	1	0	0	S13	300-317	192-207
1	1	0	1	S14	320-337	208-223
1	1	1	0	S15	340-357	224-239
1	1	1	1	S16	360-377	240-255

Chapter 5

MAINTENANCE

5-1 INTRODUCTION

This chapter contains the information required to perform maintenance on the AMCOMP 8500 Series Disc Memory Unit. The chapter contains preventive maintenance information, checkout and alignment procedures, component replacement instructions, and troubleshooting procedures for isolation of malfunctions. Before using the information in this chapter, the maintenance technician must have a thorough knowledge of the material contained in chapter 4. Maintenance procedures described in this chapter are designed for use by experienced electronics equipment maintenance technicians. Any maintenance required on the 8500 Series Disc Memory Unit that is not described in this chapter should be performed only by a trained AMCOMP Customer Service representative or by experienced maintenance technicians who have received factory instruction on maintenance of the disc unit.

The disc unit is designed to operate at maximum capability with as little maintenance as possible. This chapter describes only the replacement of parts that are external to the sealed disc/head enclosure. The use of test equipment is kept to a minimum and only common tools are required in most cases. Recommended test equipment for checkout and alignment are listed in table 5-3.

5-2. PREVENTIVE MAINTENANCE

Diagnostic test routines should be employed as frequently as necessary to performance test the disc unit. Each 8500 Series Disc Memory Unit shipped from AMCOMP, INC. has had extensive diagnostic testing in the AMCOMP Quality Assurance Department.

No electronic preventive maintenance is required on the 8500 Disc Memory Unit. Cleaning and periodic replacement of various electromechanical subassemblies should be performed in accordance with the recommended mean time to failure (MTTF) replacement intervals (MILHDBK-217B). Table 5-1 lists the various electromechanical subassemblies along with their MTTF and recommended replacement intervals. Replacement procedures for each of the subassemblies are described in paragraph 5-12 in this chapter.

CAUTION

Turn off all power to the disc unit before attempting any cleaning procedures.

The 8500 Series Disc Memory Unit must be cleaned and the pre-filter be replaced as often as operating conditions require. In normal computer environments cleaning may not be necessary, but the disc unit should be inspected periodically for cleanliness. The

TABLE 5-1. SUBASSEMBLY RECOMMENDED REPLACEMENT INTERVALS

SUBASSEMBLIES	MEANTIME TO FAILURE	REPLACEMENT INTERVAL
Motor	19,000 hours	16,000 hours
Belt	19,000 hours	16,000 hours
Ground Brush	25,000 hours	16,000 hours
Pre-Filter	-	16,000 hours or when dirty

The 8503 Series Sealed Disc Memory Unit must be cleaned and the pre-filter be replaced as often as operating conditions require. In normal computer environments cleaning may not be necessary, but the disc unit should be inspected periodically for cleanliness. The pre-filter should be inspected at regular intervals and replaced if necessary (paragraph 5-20). Accumulations of dirt on the electronics or in the duct work can cause overheating and provide conducting paths for electricity. The exterior panels and painted or metal surfaces of the disc may be washed with mild detergent and a soft cloth. Abrasive cleaners should not be used. No cleaning of the interior of the disc unit should be attempted.

The drive belt may become dirty and may be cleaned using a soft cloth wet with isopropyl alcohol, or detergent and water. The following steps should be performed when cleaning the drive belt.

- a. Turn off the power to the disc unit, disconnect all power connectors and set the disc unit on a firm surface such as a work bench. Remove the RFI shield cover.
- b. Loosen the three 7/16-inch nuts holding the four shock mounts on the disc unit baseplate and remove the disc unit from the chassis assembly.
- c. Carefully, set the disc unit on its side and remove the seven screws holding the belt guard and remove the belt guard.
- d. Clean the drive belt using the soft cloth and the prescribed cleaning fluids. Precaution should be taken to rotate the disc in only the normal direction of rotation (counterclockwise when observing disc unit from bottom). The drive need not be removed.
- e. Replace the belt guard and remount the disc unit in its normal position by reversing the previous steps.

5-3 TROUBLESHOOTING

Table 5-2 is provided as a troubleshooting guide for correcting malfunctions and may be entered at any step.

TABLE 5-2. TROUBLESHOOTING PROCEDURES

SYMPTOM	PROBABLE CAUSE	TESTING AND REMEDY
1. Disc not rotating	<ul style="list-style-type: none"> a. No ac power b. Power switch c. Drive motor d. Drive belt 	<ul style="list-style-type: none"> a. Check ac power input. b. Check ac output at J3 pins 3, 8, and 9. If power is present, replace switch. c. Check rotation of drive motor. If motor is not rotating, replace according to para. 5-16. d. If motor is rotating, replace drive belt according to para. 5-15.
2. Disc is rotating properly but disc unit is not operating properly	<ul style="list-style-type: none"> a. No ac power to power supply b. Faulty power supply c. Faulty clock track input 	<ul style="list-style-type: none"> a. Pull heatsink assy out and unplug P4 (para. 5-21) and check ac input to power supply PC board. If power is not present, check connector J4 pins and transformer windings. If power is present, proceed to the next step. b. Remove and replace the heatsink assembly (with power supply card) according to para. 5-21. c. Spare clock and test preamp output (from sealed enclosure) at J3. If reading is good, replace memory board according to para. 5-13. If reading is false, call Customer Service.
3. Data errors	<ul style="list-style-type: none"> a. Incorrect timing input or output b. Memory board 	<ul style="list-style-type: none"> a. Check I/O test points according to table 5-4. If timing outputs are correct, check data amplitude according to para. 5-8 and 5-11. If signal amplitude on any track drifts to 25% of maximum amplitude (in largest amplitude head seen), substitute spare data head. If errors still occur, call Customer Service. b. Check for inputs to the board. If they are correct, but the outputs are incorrect, replace memory board according to para. 5-13.

TABLE 5-2. TROUBLESHOOTING PROCEDURES (continued)

SYMPTOM	PROBABLE CAUSE	TESTING AND REMEDY
	c. Static ground brush	c. Check for excessive noise, carbon on bottom of disc unit, or intermittent data error. If any of these conditions exist, replace static ground brush according to para. 5-17. If errors persist call Customer Service.

5-4 CHECKOUT AND ALIGNMENT

Checkout and alignment procedures for the 8500 Series Disc Memory Unit consist primarily of the checkout procedures necessary after replacing a logic board, sparing heads or replacing the power supply assembly. All spare memory board assemblies and power supplies have been factory adjusted; therefore, only verification of proper operation should be necessary. Acceptable limits for measurements are defined in each of the procedures. Recommended test equipment is listed in table 5-3. When the measured value of any parameter is within the specified acceptable limits, no adjustment should be made. Adjustments to any of the electronics should be performed only when absolutely necessary. If the measured value falls outside the specified acceptable limits, adjustment should be made in accordance with the relevant procedure. When any adjustment is made, the value set should be the exact value specified (to the best of the operator's ability) in the procedure. If the specified acceptable limits cannot be attained, call AMCOMP Customer Service.

TABLE 5-3. RECOMMENDED TEST EQUIPMENT

EQUIPMENT	FUNCTION
8584 Disc Test Unit	AMCOMP I/O simulator to the 8400/8500 Disc Unit
Dual-Trace Oscilloscope	Necessary for checkout and alignment.

5-5 PRINTED CIRCUIT BOARD CHECKOUT

The following paragraphs describe the checkout procedures used to check the memory board or AMCODE adapter board for proper operation after replacement. Each PC board should be replaced using the replacement procedure contained in paragraph 5-13 or 5-14. Before starting the checkout procedures, verify that all the necessary jumpers are connected properly. Table 5-4 is a jumper chart for the disc unit functions and for unit select lines. (Refer to chapter 2, figure 2-3 also for illustration on connection of unit select lines.) If any heads were spared on the previous memory board, this information

should be indicated on the spare track label for the disc memory unit attached at the rear of the disc unit (figure 5-1). Refer to paragraph 5-22 for head sparing procedures. After all the required jumpers have been properly installed, perform the following checkout procedures.

5-6 Clock Amplitude Check

When the clock track is written on the disc, in accordance with specified customer format at the AMCOMP factory, clock tracks accessible at TP7 and TP6 are written simultaneously. TP5 is a spare track. Only one clock track is used at a time for normal operation (table 5-4). Verify that either TP7 or TP6 is jumpered to ground (TP8) and perform the following checkout procedure.

- a. Connect an oscilloscope to TP9.
- b. Check for 5 volts peak-to-peak minimum clock track amplitude.
- c. If necessary adjust R13 for the correct clock track amplitude at TP9.

TABLE 5-4. DISC UNIT JUMPER CHART

AMCODE ADAPTER PC BOARD		
FROM (LOCATION)	TO (LOCATION)	FUNCTION
TP1 (18D)	TP2 (D18) TP3 (D18) TP4 (D18)	Connects MFM data to write driver Connects write data to write driver Connects sector write data to write driver
TP5 (23C)	TP6 (23C) GND (23C)	Write enable (WEN) reset by sector marks (SM) WEN not reset by SM
TP8 (19C)	TP9 (19C) GND (19C)	Write encoder enabled. Write encoder disabled.
TP10 (12B)	TP11 (12B) GND (12B)	Connects settling time one-shot (clock decode) Inhibits pulse insertion in PLL (clock decode)
TP13 (4D)	TP12 (4D) TP14 (4D)	Connects $2X$ OSC (std data clk) to $\overline{RD\ CLK}$ Connects $1X$ OSC (RD DATA CLK) to RD CLK
TP16 (4D)	TP15 (4D) TP17 (4D)	Connects Standard data to $\overline{RD\ DATA}$ Connects Read data to $\overline{RD\ DATA}$
TP18 (21C)	GND (21C)	Disables WEN delay at end of write.
TP19 (20B)	TP20 (20B)	Disables RD CLK EN circuit.

TABLE 5-4. DISC UNIT JUMPER CHART (continued)

AMCODE ADAPTER PC BOARD		
FROM (LOCATION)	TO (LOCATION)	FUNCTION
TP21 (7D)	TP22 (7D) TP23 (7D) TP24 (7D) TP25 (7D)	Unit 0 selected Unit 1 selected Unit 2 selected Unit 3 selected
TP26 (4C)	GND (4C)	Forces legal address
TP27 (4C)	TP28 (4C)	$\overline{\text{WR}}$ $\overline{\text{CLK OUT}}$, $\overline{\text{SECTOR CLK}}$, $\overline{\text{DISC RDY}}$, and $\overline{\text{TRACK ORIGIN}}$ gated by unit select.
J4-2 (28B)	J4-4 (28B)	Connects separator latch to $\overline{2XOSC}$
MEMORY PC BOARD		
FROM (LOCATION)	TO (LOCATION)	FUNCTION
TP3 (C39)	TP20 (B50)	Connects write current
TP4 (C39)	TP21 (C50)	To clock bus
TP5 (C39)	TP8 (C39)	Clock head 3 selected
TP6 (C39)	TP8 (C39)	Clock head 2 selected
TP7 (C39)	TP8 (C39)	Clock head 1 selected
TP15 (C45)	TP GND (C46)	Forces ready (RDY) condition
Resistor between TP17 and TP18 (D50)		Alters write current
TP19 (B50)	TP20 (B50)	Connects write current to data bus
TP22 (C50)	TP21 (C50)	Connects write current to data bus

5-7 Clock Frequency Duty Cycle Check

In order to check the clock accuracy perform the following steps:

- a. Vary R35 to set the voltage at TP16 to 1.0 Vdc .
- b. Check the pulses at TP10 and verify that they are low for $60 \pm 5\%$ of the period CLK PLS.

5-8 Data Amplitude Check

- a. Connect an oscilloscope to TP13 in the read amplifier. Indication should be about -2V.

NOTE

The external controller may be used to switch through the data heads for the test described in step b. If an external controller is not available, the maintenance technician may use the 8584 Disc Test Unit, if available, to perform the test.

- b. Sequence through all data tracks and find maximum data amplitude.
- c. Adjust R193 for maximum data amplitude; should be 5V peak-to-peak at TP13.

5-9 Data Threshold Check

To check the threshold circuitry perform the following steps:

- a. Connect one input of a dual-trace oscilloscope to TP14 (THRESHOLD) and the other input to TP13.
- b. Check and verify that the threshold level (TP14) is 40% of analog data signal (TP13). Check all data tracks using same data pattern if possible.
- c. If necessary, adjust threshold level with R133. Recheck all data channels after any adjustment.

5-10 Clock and Sector Writing

The writing of clocks and sectors requires the use of 8584 Disc Test Unit.

If a disc test unit is not available the following procedure should not be attempted. Connect the test unit to the disc unit and perform the following steps. The information in parenthesis is the location of the test point on the logic diagrams.

- a. Remove the following jumpers on memory board assembly:
 1. TP19 to TP20 (B50)
 2. TP21 to TP22 (C50)
 3. TP8 to TP7 (C39)

4. ~~TP6 to TP5 (C39)~~
- b. Add the following jumpers on memory board assembly.
 1. TP²¹~~22~~ (C50) to TP3 (C39)
 2. TP²⁰~~19~~ (B50) to TP4 (C39)
 3. TP15 (C45) to TP GND (C46)
 4. TP8 (C39) to TP7 (C39) to TP6 (C39)
 - c. If the disc unit is a Model 8510 (1800 rpm), connect a 100-ohm, 1/2-W resistor between TP17 (D50) and TP18 (D50). If the disc unit is a Model 8530 (3600 rpm), connect a 56-ohm, 1-W resistor between TP17 and TP18 (D50).
 - d. Remove the following jumpers on AMCODE adapter board assembly.
 1. TP1 (18D) to TP2 (18D)
 - e. Add the following jumpers on AMCODE adapter board assembly.
 1. TP1 (18D) to TP4 (18D)
 2. TP18 to GND.

5-11 POWER SUPPLY CHECKOUT

When the power supply assembly is replaced, the power supply output voltages must be checked prior to returning the disc unit to normal operation. Check the power supply voltages at connector P5 on the memory board as indicated in table 5-5.

TABLE 5-5. POWER SUPPLY VOLTAGE SPECIFICATIONS

MEMORY BOARD CONNECTOR (PLUG P5) PINS	VOLTAGE OUTPUT
1	+24 Vdc \pm 3% (23-28V to 24.72V)
2	Ground
4	-12 Vdc \pm 3% (11.64V to 12.36V)
5	Ground
6	Ground
7	Ground
8	+5 Vdc \pm 3% (4.85V to 5.15V)

5-12 REMOVAL AND REPLACEMENT PROCEDURES

The following paragraphs provide procedures for removing and replacing the various components of the 8500 Series Disc Memory Unit. Only those components which may be reached without entering the dust sealed enclosure may be replaced by other than a factory trained technician. (See figure 1-1 for assembly location.) Before attempting any of the procedures, they should be read thoroughly. When performing these procedures the maintenance technician should refer to the mechanical assembly drawings. Refer to the drawing list in chapter 6.

NOTE

The replacement of components which are contained within the sealed dust enclosure should be performed by factory trained maintenance technicians only.

5-13 MEMORY BOARD REMOVAL AND REPLACEMENT

To remove and replace the memory printed circuit board perform the following:

- a. Turn off all power to disc unit and disconnect all power cables.
- b. Release the two latches holding the RFI cover to chassis and pull out RFI cover.
- c. Disconnect the power connector P5, clock pre-amp connector J4 and I/O connector J1 from memory board assembly.
- d. Loosen five standoffs holding memory board assembly and carefully lift memory board assembly from I/O connector side until data head cable is visible. The memory board assembly may be raised to approximately 45° angle.
- e. Carefully disconnect two data cables from memory board assembly and remove memory board assembly from disc unit.
- f. Replace memory board assembly by reversing previous steps and perform checkout procedures as in paragraph 5-5.

NOTE

When replacing the memory board assembly make sure that the board is securely bolted down to the mounting standoffs. This is required for analog ground continuity to the base casting and subsequently to the disc.

5-14 AMCODE ADAPTER BOARD REMOVAL AND REPLACEMENT

To remove and replace the AMCODE adapter printed circuit board disconnect I/O connector P3, unfasten the extractor tabs that hold the board in place, and pull board upward to disconnect from connectors J1 and J3.

5-15 DRIVE BELT REPLACEMENT

To remove and replace the drive belt perform the following:

- a. Turn off all power to disc unit and disconnect all power connectors.
- b. Remove disc unit from electronics cabinet and place on flat stable surface such as work bench. Remove the disc unit from the tray assembly by unscrewing the four screws on each of the shock mounts and separating the disc unit from the tray assembly.
- c. Carefully set the disc unit on its side.
- d. Remove four mounting screws holding drive belt guard in place and remove drive belt guard from the disc unit.
- e. Rotate belt and pulley in a clockwise direction and slide belt off motor pulley.
- f. Remove grounding brush retainer bracket and free belt.
- g. Replace drive belt by placing belt over spindle pulley and reversing steps e and f.
- h. Verify motor pulley adjustment by turning motor pulley in clockwise direction, by hand, and observing belt tracking. Drive belt should nominally track in center of face of each pulley. Motor pulley should be adjusted if drive belt tracks off either edge of either pulley.
- i. If drive belt does not track properly, loosen motor pulley set screw and adjust motor pulley up and down until drive belt tracks at least 0.010 - inch from either edge of both pulleys.
- j. Place disc unit back in operation by performing steps a through d in reverse order.

5-16 MOTOR ASSEMBLY REPLACEMENT

- a. Turn off all power to disc unit and disconnect all power connectors.
- b. Remove disc unit from electronics cabinet and place on flat stable surface such as work bench. Remove the disc unit from the tray assembly by unscrewing the four screws on each of the shock mounts and separating the disc unit from the tray assembly.
- c. Carefully set the disc unit on its side.
- d. Loosen four flat head screws holding motor to disc assembly and remove motor from mounting.
- e. Rotate belt and pulley in clockwise direction and slide belt off motor pulley.

CAUTION

The grounding brush and spring may pop out when the grounding brush retaining bracket is removed.

- f. Remove grounding brush retainer bracket and belt is free.
- g. Loosen motor pulley allen set screw with appropriate wrench and remove pulley from motor shaft.
- h. Disconnect motor power plug P2 from front panel.
- i. Unscrew four flat head screws holding motor to disc base assembly and remove motor from mounting.
- j. To replace drive motor, reverse steps g through i and perform the following steps for replacing drive belt.
- k. To determine initial setting for motor pulley, measure distance between edge of spindle pulley and baseplate. Use the spindle pulley height as a reference. DO NOT ATTEMPT TO ADJUST SPINDLE PULLEY HEIGHT.
- l. Adjust motor pulley to same height as spindle pulley and tighten motor pulley.
- m. Replace drive belt by placing belt over spindle pulley and reversing steps e and f. (Rotate disc in counterclockwise direction only when viewed from bottom side.)

5-17 STATIC GROUND BRUSH REPLACEMENT

- a. Perform steps a through d of drive belt replacement procedure. Do not remove drive belt from pulleys.
- b. Remove two flat head screws in grounding brush retaining bracket.
- c. Remove grounding brush and spring and replace with new parts. The rounded end of grounding brush sits against retaining bracket.
- d. Replace two flat head screws.
- e. Replace drive belt guard by reversing steps a through d drive belt replacement procedure above.

5-18 MOTOR GROUND BRUSH REPLACEMENT

To remove and replace the motor ground brush perform the following:

- a. Remove four flat heat screws and brass screw in large retaining plate on top of drive motor.

- b. Remove large retaining plate and small retaining plate underneath.
- c. Remove grounding brush and spring and replace with new parts. The rounded end of the grounding brush sits against the brass screw in the center of the large retaining plate.
- d. Replace retaining plates, the four flat head screws, and the brass screw.

5-19 PRE-FILTER REPLACEMENT

The pre-filter is mounted in a housing located under the memory board. Perform steps a through e of paragraph 5-13 and remove polyurethane foam filter element by pulling the used filter from the filter housing and replacing with a new filter. Perform steps a through e of paragraph 5-13 in reverse order.

5-20 WRITE LOCKOUT ASSEMBLY REPLACEMENT PROCEDURE

On the rear of the disc unit remove the four mounting screws on the write lockout assembly, pull the assembly from the disc unit, and disconnect the lockout connector. To replace the write lockout printed circuit assembly, reconnect the lockout connector and mount the assembly on the rear of the disc unit using the four mounting screws.

5-21 POWER SUPPLY HEATSINK ASSEMBLY REPLACEMENT

The power supply heatsink assembly contains the power supply PC board, power supply regulators, and the heatsink. To replace the heatsink assembly perform the following procedure.

- a. Turn off power to the disc unit and disconnect all power and signal cables from the unit.
- b. Remove disc unit chassis assembly from electronics cabinet and place it on stable surface such as work bench.
- c. Remove front cover from disc unit by pulling ball studs mounted on front cover from clip fasteners on front panel assembly.
- d. Disconnect the connectors and loosen six screws on the dust cover behind the front panel and remove cover.
- e. Loosen the four screws holding the heatsink and power supply printed circuit board assembly and pull out assembly.
- f. Disconnect connector J5 (to electronics) and plug P4 (to transformer) and remove heatsink and card assembly.
- g. Reverse steps a through f to replace the heatsink assembly.

5-22 HEAD SPARING PROCEDURE

5-23 CLOCK HEAD SPARING

Three clock tracks are provided on the 8500 Series Disc Memory Unit. When the clock track is written either at the AMCOMP factory or by using the procedure in paragraph 5-10 of this chapter, the customer clock format is written on the TP7 and TP6 clock tracks. Only one of the recorded clock tracks is used for normal operation. This allows data recorded on the disc to be recovered if the clock head in use becomes faulty during normal operations. The TP5 clock track is a spare. If the clock head in use becomes faulty, remove the ground jumper (TP7 or TP6 to TP8) from the clock track in use and jumper the other clock head to ground. (Consult the label in figure 5-1 for the proper spare clock head.) Perform the procedure in paragraphs 5-6 and 5-7 prior to resuming normal operation.

5-24 DATA HEAD SPARING

Two spare data heads are assigned for each 16 data heads in use at the time of manufacture. The factory can use 1 per 16 before shipment. Available spare data heads are listed on figure 5-1. If data heads have been spared, this information should also be indicated on the label.

When a data head from the upper or lower head plate is faulty, first determine the XY address from the octal address of the faulty head (chart of figure 5-2). On the spare track connector (figure 5-2) locate the XY address of the upper or lower plate and wire-wrap them to the selected spare (1 through 16 spares for each side). After making use of a spare head perform the checkout procedures in paragraph 5-5 prior to returning the disc unit to normal operation.

NEW

CLOCK SPARES				TP		TP		TP									
8400-8500 UPPER				8500 LOWER			8400-8500 UPPER				8500 LOWER						
NO.	AVAILABLE	USED		OCT ADD	AVAILABLE	USED		OCT ADD	NO.	AVAILABLE	USED		OCT ADD	AVAILABLE	USED		OCT ADD
		X	Y			X	Y				X	Y			X	Y	
S1									S9								
S2									S10								
S3									S11								
S4									S12								
S5									S13								
S6									S14								
S7									S15								
S8									S16								

P/N 1260091-01
 DATE [] [] [] [] [] []
 REV [] [] [] [] [] []

Figure 5-1. Spare-Track Label

There are a total of 32 spare heads for a 256-track disc, or 16 spares maximum per surface. Spare heads for the lower disc surface cannot be used for the upper disc surface or vice versa.

UPPER HEAD PLATE									LOWER HEAD PLATE								
OCTAL ADDRESS	X ADDRESS	OCTAL ADDRESS	X ADDRESS	OCTAL ADDRESS	X ADDRESS	OCTAL ADDRESS	X ADDRESS	Y ADDRESS	OCTAL ADDRESS	X ADDRESS	OCTAL ADDRESS	X ADDRESS	OCTAL ADDRESS	X ADDRESS	OCTAL ADDRESS	X ADDRESS	Y ADDRESS
000	X0U	040	X2U	100	X4U	140	X6U	Y0U	200	X0L	240	X2L	300	X4L	340	X6L	Y0L
001	▲	041	▲	101	▲	141	▲	Y1U	201	▲	241	▲	301	▲	341	▲	Y1L
002		042		102		142		Y2U	202		242		302		342		Y2L
003		043		103		143		Y3U	203		243		303		343		Y3L
004		044		104		144		Y4U	204		244		304		344		Y4L
005		045		105		145		Y5U	205		245		305		345		Y5L
006		046		106		146		Y6U	206		246		306		346		Y6L
007		047		107		147		Y7U	207		247		307		347		Y7L
010		050		110		150		Y10U	210		250		310		350		Y10L
011		051		111		151		Y11U	211		251		311		351		Y11L
012		052		112		152		Y12U	212		252		312		352		Y12L
013		053		113		153		Y13U	213		253		313		353		Y13L
014		054		114		154		Y14U	214		254		314		354		Y14L
015		055		115		155		Y15U	215		255		315		355		Y15L
016		056		116		156		Y16U	216		256		316		356		Y16L
017		057		117		157		Y17U	217		257		317		357		Y17L
S1		S5		S9		S13		SY1U	S1		S5		S9		S13		SY1L
S2	X0U	S6	X2U	S10	X4U	S14	X6U	SY2U	S2	X0L	S6	X2L	S10	X4L	S14	X6L	SY2L
020	X1U	060	X3U	120	X5U	160	X7U	Y0U	220	X1L	260	X3L	320	X5L	360	X7L	Y0L
021	▲	061	▲	121	▲	161	▲	Y1U	221	▲	261	▲	321	▲	361	▲	Y1L
022		062		122		162		Y2U	222		262		322		362		Y2L
023		063		123		163		Y3U	223		263		323		363		Y3L
024		064		124		164		Y4U	224		264		324		364		Y4L
025		065		125		165		Y5U	225		265		325		365		Y5L
026		066		126		166		Y6U	226		266		326		366		Y6L
027		067		127		167		Y7U	227		267		327		367		Y7L
030		070		130		170		Y10U	230		270		330		370		Y10L
031		071		131		171		Y11U	231		271		331		371		Y11L
032		072		132		172		Y12U	232		272		332		372		Y12L
033		073		133		173		Y13U	233		273		333		373		Y13L
034		074		134		174		Y14U	234		274		334		374		Y14L
035		075		135		175		Y15U	235		275		335		375		Y15L
036		076		136		176		Y16U	236		276		336		376		Y16L
037		077		137		177		Y17U	237		277		337		377		Y17L
S3		S7		S11		S15		SY1U	S3		S7		S11		S15		SY1L
S4	X1U	S8	X3U	S12	X5U	S16	X7U	SY2U	S4	X1L	S8	X3L	S12	X5L	S16	X7L	SY2L

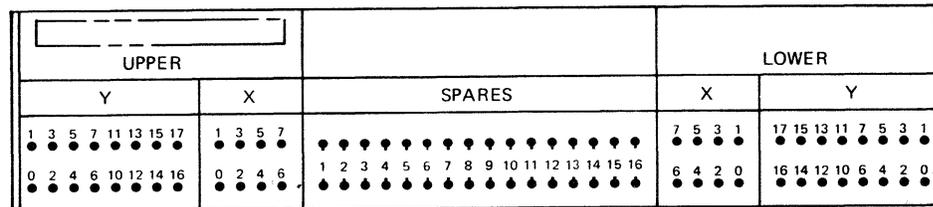


Figure 5-2. Address Decode Matrix and Spare-Track Connector (J6)

Chapter 6

DRAWINGS AND PARTS LISTS

6-1 INTRODUCTION

This chapter contains the drawings required to maintain the 8500 Series Disc Memory Unit. Lists of recommended site level spare parts and replaceable parts are also included in this chapter.

6-2 DRAWINGS

Table 6-1 lists the drawings contained in this chapter. All assembly diagrams, wiring diagrams, schematic diagrams and inter-connection diagrams required to maintain the 8500 Series Disc Memory Unit are contained in this chapter. Newer versions will always replace earlier versions of any element listed. Drawings applicable to the optional write lockout assembly are also included. If the disc memory unit this manual accompanies does not include these assemblies, the drawings for these assemblies should be ignored. All drawings listed in table 6-1 are also contained in the drawing tree shown in figure 6-1.

TABLE 6-1. DISC MEMORY UNIT DRAWINGS

DRAWING NUMBER	DRAWING TITLE
1040077	AMCODE Adapter PC Board Assembly
1940077	AMCODE Adapter PC Board Schematic
1040046	Memory PC Board Assembly
1940046	Memory PC Board Schematic
1040060	Mini Mother PC Board Assembly
1940060	Mini Mother PC Board Schematic
1240056	Rear Panel Interconnect PC Board Assembly
1940056	Rear Panel Interconnect PC Board Schematic
1930009	System Interconnect Diagram
1020085	Drive Motor Assembly
1020059	Front Panel and Power Supply Assembly
1930008	Octal Address Diagram
1040094	Power Supply PC Board Assembly
1940094	Power Supply PC Board Schematic
1020138	Heatsink Assembly
1930032	Heatsink Wire Diagram
1040003	Clock Preamp PC Board Assembly
1940003	Clock Preamp PC Board Schematic
1040070	Write Lockout PC Board Assembly
1940070	Write Lockout PC Board Schematic
1930019	Power Supply Wiring Diagram

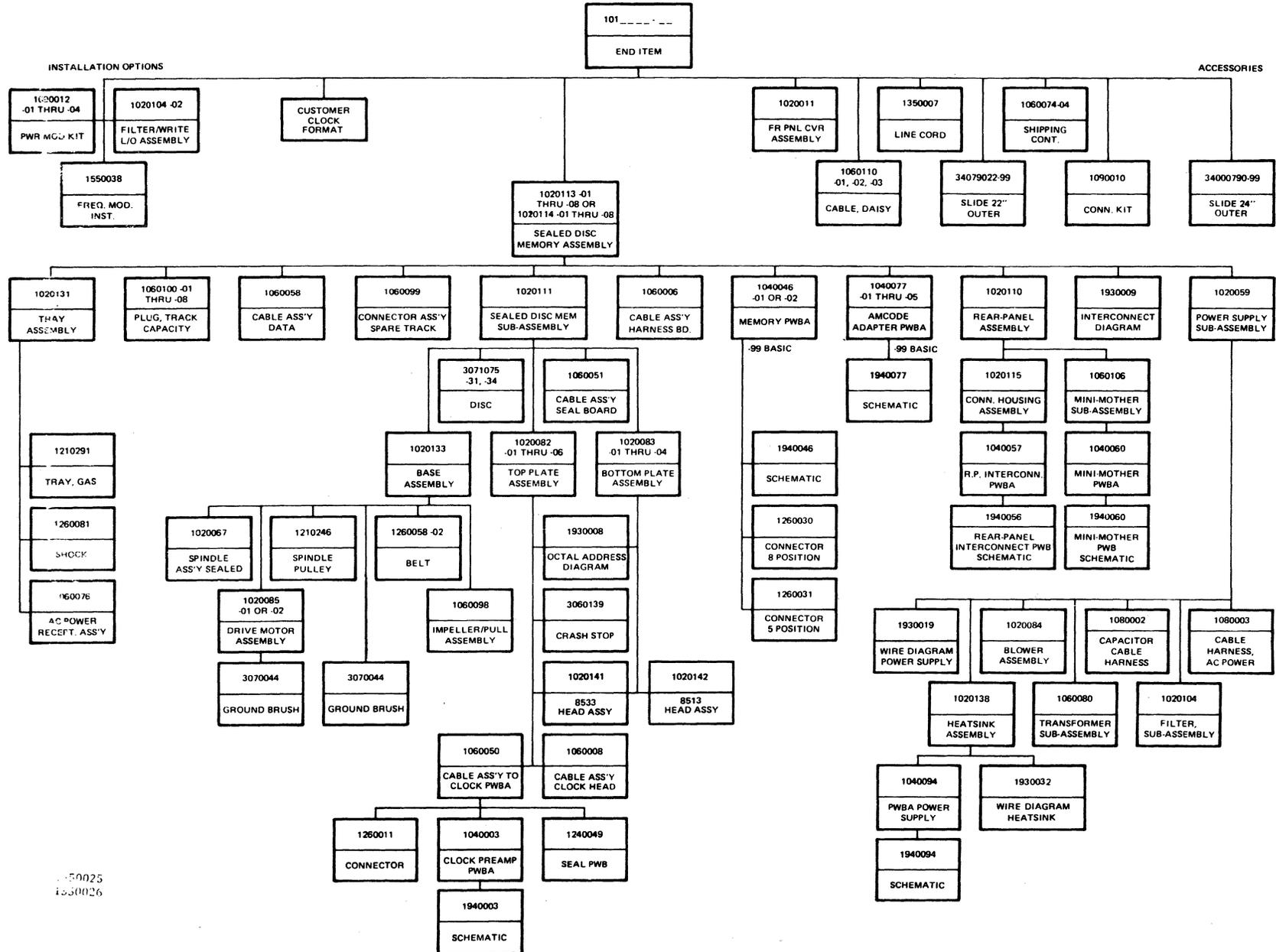


Figure 6-1. 8500 Series Disc Memory Unit, Drawing Tree

6-3 RECOMMENDED SITE LEVEL SPARE PARTS

Recommended site level spare parts are listed in table 6-2. The table includes the AMCOMP, INC. part number of each part, a description, and the recommended quantity of spares that should be maintained on site for each disc memory unit model.

TABLE 6-2. RECOMMENDED SITE LEVEL SPARES

PART NUMBER	DESCRIPTION	QUANTITY	
		MODEL 8510	MODEL 8530
1040046-XX	Memory PC Board Assembly (1)	1	1
1040047-XX	AMCODE Adapter PC Board Assembly (2)	1	1
1040003-01	Clock Preamplifier PC Board (3)	1	1
1020085-XX	Drive Motor Assembly (4)	1	1
1260058-02	Drive Belt (5)	1	1
1020138-01	Heatsink Assembly (power supply)	1	1
09220004-01	Fuse, 2.5A SLO BLO/F1 (6)	1	1
09230005-01	Fuse, 5A SLO BLO/F1 (7)	1	1
3070044-01	Ground Brush (8)	1	1
3070045-01	Ground Brush Spring (8)	1	1
1260064-01	Pre-filter	1	1
1040070-01	Write Lockout PC Board (9)	1	1
1260079-01	Track Sparing Connector	1	1
1040060-01	Mini Mother Board	1	1
1020104-XX	Filter (10)	1	1
1040078	Board Extender	1	1

- (1) Select assembly applicable to disc unit model; -01 for Model 8530, -02 for Model 8510.
- (2) Select assembly with desired speed and data transfer rate as follows: Frequency options -05, -06 for Model 8510 (1800 rpm); frequency options 01 through -04 for Model 8530 (3600 rpm). For these option selections, see table 1-1 and AMCODE PC board schematic diagram 1940077, sheet 1.
- (3) Can be replaced by factory trained technician only.
- (4) Select assembly applicable to disc unit model: -01 for Model 8510 (1800 rpm), -02 for Model 8530 (3600 rpm).
- (5) Part applicable to both models of disc unit.
- (6) Part applicable to input voltages of 200 Vac and 240 Vac.
- (7) Part applicable to input voltages of 100 Vac and 120 Vac.
- (8) Ground brush and spring may be used as one unit also. Part number is 1060095.
- (9) Only is disc unit is equipped with write lockout option.
- (10) Filters air from cooling fan to power supply: -01 plate and filter only, -02 write lockout switch assembly included.

REPLACEABLE PARTS LIST

Table 6-3 lists the parts that may become defective and thus be replaced. The table includes lists for the memory PC board, the AMCODE PC board, mini mother PC board, clock preamplifier PC board, heatsink assembly (power supply), power supply PC board, write lockout assembly and miscellaneous components.

TABLE 6-3. REPLACEABLE PARTS LIST

PART NUMBER	DESCRIPTION/LOCATION	QUANTITY	
		MODEL 8510	MODEL 8530
MEMORY PC BOARD COMPONENTS			
01383680-01	Capacitor, Mica, 68 pF, 500V, 5%/C42		1
01383680-01	Capacitor, Mica, 68 pF, 500V, 5%/C42, C20, C22	3	
01383101-01	Capacitor, Mica, 100 pF, 300V, 5%/C62		1
01383221-01	Capacitor, Mica, Silver, 220 pF, 500V, 5%/C46, C50	2	2
01383681-01	Capacitor, Mica, 680 pF, 500V, 5%/C2, C6, C10, C16	4	4
01400105-02	Capacitor, Fxd, Cer, .01 μ F, 100V, 20%/C5, C15, C17, C18, C19, C21, C23-C25, C27, C28, C30, C31, C33-C41, C51-C54, C56, C58, C59, C77-C79, C81, C82	34	34
01383331-01	Capacitor, Mica, 330 pF, 500V, 5%/C67, C68, C73, C74	4	
01383331-01	Capacitor, Mica, 330 pF, 500V, 5%/C2, C6, C10, C16		4
01400109-25	Capacitor, Fxd, Mold, .001 μ F, 200V, 10%/C60, C61	2	2
01400111-17	Capacitor, Fxd, Mold, .01 μ F, 200V, 10%/C4, C8, C9, C11, C65, C71	6	6
01444104-01	Capacitor, Fxd, Mold, .01 μ F, 100V, 10%/C1, C3, C7, C12-C14, C26, C29, C43, C55, C57, C66, C69, C70, C72, C75, C76	17	17
01500107-01	Capacitor, Fxd, Tant, 50 μ F, 25V, 10%/C47	1	1
01200103-23	Capacitor, Fxd, Tant, 6.8 μ F, 35V, 10%/C48, C49	2	2
01200103-13	Capacitor, Fxd, Mold, 1 μ F, 35V, 10%/C32, C44, C80	3	3
01383220-01	Capacitor, Mica, 22 pF, 500V, 5%/C20, C22		2
01383181-01	Capacitor, Mica, 180 μ F, 300V, 5%/C67, C68, C73, C74		4
01383470-01	Capacitor, Mica, 47 pF, 500V, 5%/C62		1
04122560-01	Resistor, Fxd, Comp, 56 ohms, 1/4W, 5%/R7, R8, R14, R15, R17, R26, R34, R36, R38, R40, R50, R52, R54, R115, R119, R127-R129, R137, R149, R150, R166, R172, R179, R180-R182, R184-R186, R187	31	31
04122391-01	Resistor, Fxd, Comp, 390 ohms, 1/4W, 5%/R29, R31-R33, R157, R169, R183	7	7

TABLE 6-3. REPLACEABLE PARTS LIST (continued)

PART NUMBER	DESCRIPTION/LOCATION	QUANTITY	
		MODEL 8510	MODEL 8530
MEMORY PC BOARD COMPONENTS (continued)			
04122681-01	Resistor, Fxd, Comp, 680 ohms, 1/4W, 5%/R49, R131, R132, R156, R158, R163, R178, R223	8	8
04122182-01	Resistor, Fxd, Comp, 1.8K, 1/4W, 5%/R9, R11, R12, R16, R19, R23, R41, R46, R53, R79, R120, R122, R134-R136, R138, R147, R148, R151, R155, R159, R162, R164, R165, R201	25	
04122182-01	Resistor, Fxd, Comp, 1.8K, 1/4W, 5%/R9, R11, R12, R16, R19, R23, R41, R46, R53, R79, R120, R122, R134-R136, R138, R147, R148, R151, R155, R159, R162, R164, R165, R191, R197, R201		27
04122392-01	Resistor, Fxd, Comp, 3.9K, 1/4W, 5%/R30, R39, R65, R69, R74, R80-R113, R121, R123, R126, R144-R146, R153, R154, R191, R196-R198, R205-R221, R225-R261, R264	105	
04122392-01	Resistor, Fxd, Comp, 3.9K, 1/4W, 5%/R30, R39, R65, R69, R74, R80-R113, R121, R123, R126, R144-R146, R153, R154, R196, R198, R205-R221, R225-R261, R264		103
04122153-01	Resistor, Fxd, Comp, 15K, 1/4W, 5%/R42, R44, R47, R61, R63, R77, R114, R118, R124, R139, R140, R152, R200, R262	14	14
04122273-01	Resistor, Fxd, Comp, 27K, 1/4W, 5%/R141-R143, R202, R222, R224	6	6
04122124-01	Resistor, Fxd, Comp, 120K, 1/4W, 5%/R66, R70	2	2
04122184-01	Resistor, Fxd, Comp, 180K, 1/4W, 5%/R48, R55	2	2
04132151-01	Resistor, Fxd, Comp, 150 ohms, 1/2W, 5%/R199	1	1
04132561-01	Resistor, Fxd, Comp, 560 ohms, 1/2W, 5%/R263	1	1
04132681-01	Resistor, Fxd, Comp, 680 ohms, 1/2W, 5%/R25, R27, R125	3	3
04132271-01	Resistor, Fxd, Comp, 270 ohms, 1/2W, 5%/R130	1	1
04250101-01	Resistor, Mtl, Film, 56.2 ohms, 1/2W, 1%/R116, R117		2
04220097-01	Resistor, Mtl, Film, 100 ohms, 1/4W, 1%/R189, R190, R194, R195		4
04734202-01	Resistor, Var, 2K, 1/2W, 4 Turns/R13, R133, R193	3	3
04400101-01	Resistor, Var, 5K, 1/2W, 4 Turns/R35	1	1
04132222-01	Resistor, Fxd, Comp, 2.2K, 1/2W, 5%/R203, R204	2	2
04220097-01	Resistor, Mtl, Film, 100 ohms, 1/4W, 1%/R4, R10, R18, R24	4	4

TABLE 6-3. REPLACEABLE PARTS LIST (continued)

PART NUMBER	DESCRIPTION/LOCATION	QUANTITY	
		MODEL 8510	MODEL 8530
MEMORY PC BOARD COMPONENTS (continued)			
04220129-01	Resistor, Mtl, Film, 215 ohms, 1/4W, 1%/R5, R22, R28, R175	4	4
04220169-01	Resistor, Mtl, Film, 562 ohms, 1/4W, 1%/R167, R171, R173, R177	4	4
04220193-01	Resistor, Mtl, Film, 1K, 1/4W, 1%/R6, R20, R57, R168, R170, R174, R176, R188, R192	9	9
04220209-01	Resistor, Mtl, Film, 1.47K, 1/4W, 1%/R43, R45, R62, R75	4	4
04220225-01	Resistor, Mtl, Film, 2.15K, 1/4W, 1%/R51, R64, R78	3	3
04220265-01	Resistor, Mtl, Film, 5.62K, 1/4W, 1%/R1, R2, R3, R21, R37, R58, R76, R160, R161	9	9
04220269-01	Resistor, Mtl, Film, 6.19K, 1/4W, 1%/R67, R73	2	2
04220285-01	Resistor, Mtl, Film, 9.09K, 1/4W, 1%/R56, R59, R60, R68, R72	5	5
04220101-01	Resistor, Mtl, Film, 110 ohms, 1/4W, 1%/R189, R190, R194, R195	4	
04220297-01	Resistor, Mtl, Film, 12.1K, 1/4W, 1%/R71	1	1
04250101-02	Resistor, Mtl, Film, 110 ohms, 1/2W, 1%/R116, R117	2	
06100101-24	Inductor, Fxd, 8.2 H, 10%/L5, L6, L8	3	
06100101-24	Inductor, Fxd, 8.2 H, 10%/L1, L2		2
06100101-20	Inductor, Fxd, 3.9 H, 10%/L5, L6, L8		3
06100101-27	Inductor, Fxd, 15 H, 10%/L1, L2	2	
06151000-20	Inductor, Shielded, 100 H/L3, L4, L7	3	3
02100102-01	Diode, IN 4454/CR1-CR5, CR9-CR25, CR27, CR28, CR30-CR119	114	114
02200108-12	Diode, Zener, IN 752A, 5.6V, 5%/CR8, CR26, CR29	3	3
02200109-01	Diode, Zener, 5.6V, 1%, .04W/CR7	1	1
05202905-01	Transistor, PNP 2N2905/Q19, Q20, Q62	3	3
05202906-01	Transistor, PNP 2N2906/Q13, Q14	2	2
05203906-01	Transistor, PNP 2N3906/Q11, Q22, Q26, Q43, Q61	5	5
05100104-01	Transistor, PNP 2N3646/Q15, Q25, Q28, Q42, Q60	5	5
05100101-01	Transistor, PNP 2N2222A/Q1-Q10, Q12, Q16-Q18, Q21, Q23, Q24, Q29-Q41, Q44-Q59	46	46
05300102-01	Transistor, Fet, 2N4393/Q27	1	1
03207400-01	IC, 7400/U20, U25, U29, U30	4	4
03207402-01	IC, 7402/U13-U16, U23, U27	6	6
03207442-01	IC, 7442/U19, U21	2	2

TABLE 6-3. REPLACEABLE PARTS LIST (continued)

PART NUMBER	DESCRIPTION/LOCATION	QUANTITY	
		MODEL 8510	MODEL 8530
MEMORY PC BOARD COMPONENTS (continued)			
03207405-01	IC, 7405/U6, U24, U26, U28	4	4
03200102-01	IC, 74H00/U2	1	1
03105453-01	IC, 75453/U31-U34, U36-U53	22	22
03204122-01	IC, 74122/U4	1	1
03200124-01	IC, 74S74/U7	1	1
03200239-01	IC, 74156/U10-U12, U17, U18, U22	6	6
03000102-01	IC, CA3046/U8, U9	2	2
03020733-01	IC, 733/A1-A3	3	3
03000105-01	IC, LM310/U35	1	1
03000114-01	IC, 521/U1, U3, U5	3	3
AMCODE PC BOARD COMPONENTS			
1040077-xx	AMCODE Adapter PC Board*		
01383330-01	Capacitor, Mica, 33pF, 500V, +5%/C12	1	
01383220-01	Capacitor, Mica, 22pF, 500V, +5%/C41, C12	2	
01383220-01	Capacitor, Mica, 22pF, 500V, +5%/C12, C41, C42		3(-03)
01200101-20	Capacitor, Tant, 39 μF, 10V, +10%/C13, C46-C48	4	4
01200103-23	Capacitor, Tant, 6.8 μF, 35V, 10%/C45	1	1
01383101-01	Capacitor, Mica, 100pF, 500V, +5%/C33, C35, C36	3	3
01383102-01	Capacitor, Mica, 1000pF, 100V, +5%/C7, C9, C18, C32, C34, C40	6	6
01383120-01	Capacitor, Mica, 12pF, 500V, +5%/C5, C6	2	2(-03)
01383120-01	Capacitor, Mica, 12pF, 500V, +5%/C5, C6, C12		3(-02)
01383181-01	Capacitor, Mica, 180pF, 500V, +5%/C1	1	1
01383050-01	Capacitor, Mica, 5pF, 500V, +5%/C50	1	2(-02)
01383050-01	Capacitor, Mica, 5pF, 500V, +5%/C43, C44		2(-02)
01416103-01	Capacitor, Cer, .01 μF, 25V, +80%/C2-C4, C8, C10, C11, C14-C17, C19-C21, C23-C31, C37, C49	26	26
01400108-12	Capacitor, Cer, .01 μF, 100V, +10%/C22	1	1
01383560-01	Capacitor, Mica, 56pF, 500V, +5%/C43, C44	2(-05)	
01383620-01	Capacitor, Mica, 62pF, 500V, +5%/C43, C44	2(-06)	
<p>* Select assembly with desired speed and data transfer rate as follows: Frequency options -05, -06 for Model 8510 (1800 rpm); frequency options 01 through -04 for Model 8530 (3600 rpm). For these option selections, see table 1-1 and AMCODE PC board schematic diagram 1940077, sheet 1.</p> <p>Note: The shown components and quantities are construed to be applicable to each option within the particular model. If this is not the case, the number in parenthesis indicates which option that particular component and quantity are applicable to.</p>			

TABLE 6-3. REPLACEABLE PARTS LIST (continued)

PART NUMBER	DESCRIPTION/LOCATION	QUANTITY	
		MODEL 8510	MODEL 8530
AMCODE PC BOARD COMPONENTS (continued)			
01383270-01	Capacitor, Mica, 27pF, 500V, +5%/C41, C42		2
01383100-01	Capacitor, Mica, 10pF, 500V, +5%/C43, C44		2(-03)
01383240-01	Capacitor, Mica, 24pF, 500V, +5%/C12		1(-04)
01383300-01	Capacitor, Mica, 30pF, 500V, +5%/C41, C42		2(-04)
04122100-01	Resistor, Fxd, Comp, 10 ohms, 1/4W, 5%/R7	1	1
04122102-01	Resistor, Fxd, Comp, 1K, 1/4W, 5%/R3-R5, R8, R9, R16, R18, R21, R29-R32	12	12
04122181-01	Resistor, Fxd, Comp, 180 ohms, 1/4W, 5%/R1, R25	2	2
04122221-01	Resistor, Fxd, Comp, 220 ohms, 1/4W, 5%/R2	1	1
04122331-01	Resistor, Fxd, Comp, 330 ohms, 1/4W, 5%/R15, R22, R23	3	3
04122392-01	Resistor, Fxd, Comp, 3.9K, 1/4W, 5%/R6, R12, R19, R20, R33	5	5
04220257-01	Resistor, Mtl, Film, 4.64K, 1/8W, 1%/R13, R14, R17, R27, R28	5	5
04220273-01	Resistor, Mtl, Film, 6.81K, 1/8W, 1%/R24, R26	2	2
04220349-01	Resistor, Mtl, Film, 42.2K, 1/8W, 1%/R10, R11	2	2
04741231-01	Resistor, Pack, 898-5-R220/330/U43, U44, U48	3	3
04501145-01	Resistor, Pack, 470/TN1-TN10	10	10
06151000-20	Inductor, 100 μ H/L1, L2, L3	3	3
02104454-01	Diode, IN4454/CR1-CR6	6	6
05203906-01	Transistor, 2N3906/Q1	1	1
12300004-01	Socket, 16-pin DIP/U43, U44, U48	3	3
03052741-01	IC, 74IC/U8, U46	2	2
03200101-01	IC, 74S00/U5, U17	2	2
03200104-01	IC, 74S02/U14	1	1
03200106-01	IC, 74S04/U6, U25	2	2
03200108-01	IC, 74S10/U23	1	1
03200124-01	IC, 74S74/U7, U16, U18, U27, U31, U32, U41	7	7
03200190-01	IC, 7428/U33, U34	2	2
03200201-01	IC, 7475/U35, U36	2	2
03200219-01	IC, 74164/U13, U15, U22, U24, U30, U39, U40	7	7
03204121-01	IC, 74121/U26	1	1
03207438-01	IC, 7438/U42, U45	2	2
03200251-01	IC, 74S124/U9	1	1
03200122-01	IC, 74S51/U4	1	1
03400106-01	IC, 10104/U1, U12, U28, U38	4	4

TABLE 6-3. REPLACEABLE PARTS LIST (continued)

PART NUMBER	DESCRIPTION/LOCATION	QUANTITY	
		MODEL 8510	MODEL 8530
AMCODE PC BOARD COMPONENTS (continued)			
03400107-01	IC, 10116/U47	1	1
03400109-01	IC, 10125/U21	1	1
03400110-01	IC, 10231/U10, U11, U19, U20, U29, U37	6	6
03400108-01	IC, 10124/U3	1	1
55000101-01	IC, Delay Line, 50 ns, 100 ohms/U2		3(-01 -02 -03)
55000104-01	IC, Delay Line, 100 ns, 100 ohms/U2		1(-04)
55000103-01	IC, Delay Line, 125 ns, 100 ohms/U2	1	
MINI MOTHER BOARD COMPONENTS			
1240060-04	Mini Mother Assembly	1	1
01446103-01	Cap, Cer, .01 μ F, 100V, 10%/C1, C2	2	2
04122391-01	Res, Fxd, Comp, 390 ohms, 1/4W, 5%/R1	1	1
07189065-01	Connector, Header, 34 Pin/J3	1	1
07100113-01	Connector, 56 Pin/J1, J2	2	2
03200239-01	IC, 74156/U1, U2	2	2
HEATSINK ASSEMBLY (P/N 1020138)			
1040094-01	Power Supply PC Board Assembly	1	1
02509622-01	Diode, Rectifier, 100V, 25A	1	1
08900103-02	Switch, Thermostat/S1	1	1
POWER SUPPLY PC BOARD (P/N 1040094)			
1020137-01	Transistor Sub-Assembly (NON TO-3)	1	1
1020143-01	Transistor Sub-Assembly (Dual TO-3)	1	1
1020144-01	Transistor Sub-Assembly (Single TO-3)	1	1
01200103-13	Capacitor, Tant, 1.0 μ F, 35V, 10%/C8-C10	3	3
01200103-23	Capacitor, Tant, 6.8 μ F, 35V, 10%/C7	1	1
01400101-52	Capacitor, Cer, 1000pF, 1000V, 10%/C1, C3, C5	3	3
01416103-01	Capacitor, Cer, .01 μ F, +80 -20%/C2, C4, C6	3	3
02204753-01	Diode, Zener - IN4753/CR3	1	1
02400101-01	Diode, IN4720/CR1, CR2	2	2

TABLE 6-3. REPLACEABLE PARTS LIST (continued)

PART NUMBER	DESCRIPTION/LOCATION	QUANTITY	
		MODEL 8510	MODEL 8530
POWER SUPPLY PC BOARD (continued)			
03052741-01	IC, 741/U1	1	1
03420723-01	IC, 723/U2, U3, U4	3	3
04122102-01	Resistor, Carbon, 1K, 1/4W, 5%/R2, R19	2	2
04122162-01	Resistor, Carbon, 1.6K, 1/4W, 5%/R14	1	1
04122362-01	Resistor, Carbon, 3.6K, 1/4W, 5%/R6	1	1
04142471-01	Resistor, Carbon, 470 ohms, 1W, 5%/R34	1	1
04122512-01	Resistor, Carbon, 5.1K, 1/4W, 5%/R9, R25, R39, R40	4	4
04122751-01	Resistor, Carbon, 750 ohms, 1/4W, 5%/R5	1	1
04122821-01	Resistor, Carbon, 820 ohms, 1/4W, 5%/R33	1	1
04122911-01	Resistor, Carbon, 910 ohms, 1/4W, 5%/R13	1	1
04122562-01	Resistor, Carbon, 5.6K, 1/4W, 5%/R32	1	1
04122514-01	Resistor, Carbon, 510 ohms, 1/4W, 5%/R22	1	1
04230185-01	Resistor, Mtl Film, 825 ohms, 1/4W, 1%/R30	1	1
04230193-01	Resistor, Mtl Film, 1K, 1/4W, 1%/R4, R15, R27	3	3
04230209-01	Resistor, Mtl Film, 1.47K, 1/4W, 1%/R16, R20	2	2
04230225-01	Resistor, Mtl Film, 2.1K, 1/4W, 1%/R17	1	1
04230245-01	Resistor, Mtl Film, 3.48K, 1/4W, 1%/R21	1	1
04230257-01	Resistor, Mtl Film, 4.64K, 1/4W, 1%/R11	1	1
04230269-01	Resistor, Mtl Film, 6.19K, 1/4W, 1%/R36	1	1
04230277-01	Resistor, Mtl Film, 7.5K, 1/4W, 1%/R28, R29	2	2
04230281-01	Resistor, Mtl Film, 8.25K, 1/4W, 1%/R31	1	1
04230289-01	Resistor, Mtl Film, 10K, 1/4W, 1%/R24, R35, R37	3	3
04230261-01	Resistor, Mtl Film, 5.11K, 1/4W, 1%/R3	1	1
04230293-01	Resistor, Mtl Film, 11K, 1/4W, 1%/R18, R41	2	2
04230301-01	Resistor, Mtl Film, 13.3K, 1/4W, 1%/R38	1	1
04230329-01	Resistor, Mtl Film, 26.1K, 1/4W, 1%/R23	1	1
04230309-01	Resistor, Mtl Film, 16.2K, 1/4W, 1%/R10	1	1
04370101-04	Resistor, Wire Wound, .56 ohm, 5W, 1%/R1, R8	2	2
04370101-06	Resistor, Wire Wound, .68 ohm, 5W, 1%/R12	1	1
04370101-11	Resistor, Wire Wound, 3 ohms, 5W, 1%/R26	1	1
04473202-01	Resistor, Variable, 1 Turn, 2K, 1/2W, 10%/R7	1	1
05400101-01	Transistor, Unijunction-2N6027/Q4, Q8, Q12, Q13	4	4
07210015-01	Connector, 12-position/P4	1	1
07220012-01	Connector, 9-position/J5	1	1
47080514-01	Contact, Socket	9	9
47080513-01	Contact, Pin	12	12

TABLE 6-3. REPLACEABLE PARTS LIST (continued)

PART NUMBER	DESCRIPTION/LOCATION	QUANTITY	
		MODEL 8510	MODEL 8530
CLOCK PREAMPLIFIER PC BOARD COMPONENTS			
1040003-01	Clock Preamplifier PC Board Assembly	1	1
01400101-52	Capacitor, Ceramic Disc, 1000pF, 1000V/C5-C7	3	3
01446103-01	Capacitor, Ceramic Disc, .01 μ F, 100V/C1, C4	2	2
01400108-12	Capacitor, Molded Cer, .01 μ F, 100V/C2, C3	2	2
47088295-01	Contact, Right angle/J4	5	5
04122101-01	Resistor, Carbon, 1/4W, 100 ohms \pm 5%/R3	1	1
04122511-01	Resistor, Carbon, 1/4W, 510 ohms \pm 5%/R10, R11	2	2
04122392-01	Resistor, Carbon, 1/4W, 3.9K \pm 5%/R1, R2, R4, R5-R7	6	6
04122103-01	Resistor, Carbon, 1/4W, 10K \pm 5%/R12-R14	3	3
04220169-01	Resistor, Mtl Film, 1/4W, 562 ohms \pm 1%/R8, R9	2	2
02100102-01	Diode, Signal-IN4454/CR1, CR2, CR7, CR8	4	4
02500105-01	Diode, Matched-IN4307/CR3-CR6	4	4
03020733-01	IC, 733/U1	1	1
WRITE/LOCKOUT (OPTIONAL)			
1040070-01	Write/Lockout PC Board Assembly	1	1
08100104-01	Switch, SPST	16	16
07189065-01	Connector, 34 Position	1	1
SUSTAINING GAS SYSTEM COMPONENTS			
08428009-02	Pressure Sensor Switch (S1)	1	1
10600094-02	Cylinder Assembly-Nitrogen Filled	1	1
19000102-01	Pressure Gauge, 0-5 psi	1	1
12100101-01	Indicator Lamp - LED (DSI)	1	1

TABLE 6-3. REPLACEABLE PARTS LIST (continued)

PART NUMBER	DESCRIPTION/LOCATION	QUANTITY	
		MODEL 8510	MODEL 8530
MISCELLANEOUS PARTS			
1260064-01	Pre-Filter	1	1
3070044-01	Brush (1)	1	1
3070045-01	Spring (1)	1	1
1260058-02	Belt	1	1
1260084-01	Shock Mount	4	4
1020085-XX	Drive Motor Assembly (2)	1	1
1020081-01	Heatsink Assembly (Power Supply)	1	1
1240056-01	Interconnect PC Board	1	1
1060076-01	Power Receptacle Assembly	1	1
09230005-01	Fuse, Ceramic, 5A SLO BLO/F1	1	1
09220004-01	Fuse, Ceramic, 2.5A SLO BLO/F1	1	1
<p>(1) Brush and spring may be used as one unit also. Part number is 1060095.</p> <p>(2) Select assembly applicable to disc unit model: -01 for Model 8510 (1800 rpm), or -02 for Model 8530 (3600 rpm).</p>			

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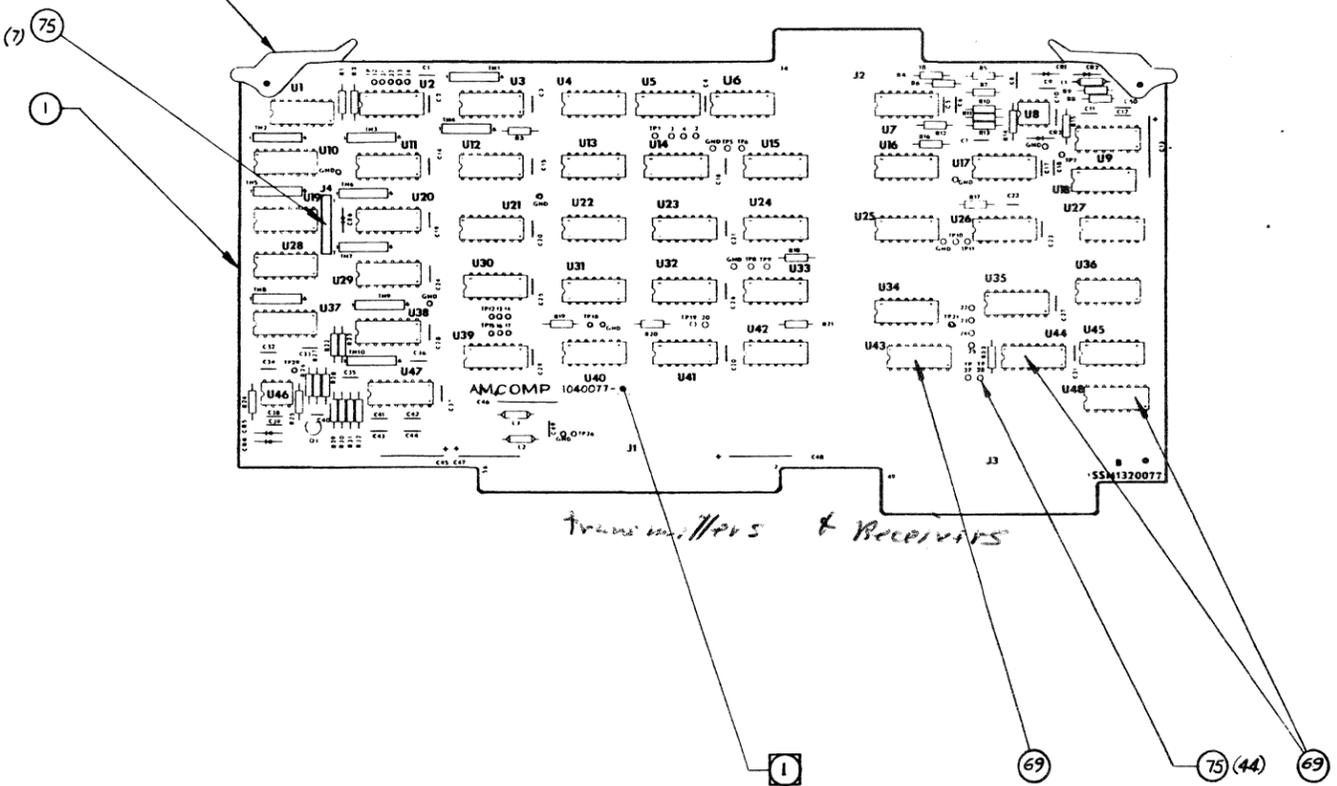
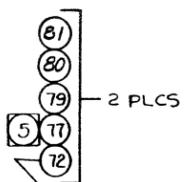
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REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
A		RELEASE PER 8500-023	2-18-77	J



Transmitters & Receivers

- NOTES:
- IDENTIFY WITH APPROPRIATE ASSY PART N° AND CURRENT M/L REV. PER 1550010. SEE TABULATION BLOCK.
 - MAXIMUM COMPONENT LEAD PROTRUDING ON CIRCUIT SIDE OF BOARD SHALL BE .060.
 - MAXIMUM COMPONENT HEIGHT ALLOWABLE SHALL BE .400.
 - SQUARE PAD DENOTES POSITIVE POLARITY OF CAPACITOR, CATHODE END OF DIODE.
 - TORQUE N°4 SCREWS TO 64 ± 4 IN.-OZ. MAX.
 - WORKMANSHIP SHALL COMPLY WITH QA 100000-00.

ASSY N°	FREQ RANGE (MHz)
1040077-06	3.36 - 4.5
1040077-05	3.97 - 4.9
1040077-04	5.8 - 8.06
1040077-03	7 - 8.65
1040077-02	7.5 - 9.3
1040077-01	8.2 - 9.93

(1)

TABULATION BLOCK

NOTICE
THIS DWG SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF AMCOMP, INC. HOWEVER, IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUB-CONTRACT.

UNLESS OTHERWISE SPECIFIED	SIGNATURE	DATE
DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS XXX±	<i>[Signature]</i>	10/20/76
	CHK <i>[Signature]</i>	3/25/77
	APP <i>[Signature]</i>	2/1/77
	APR	

QTY REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL

LIST OF MATERIAL	

AMCOMP
SUNNYVALE, CALIFORNIA

TITLE
PWBA AMCODE ADAPTER

SIZE **D** DRAWING NO. **1040077** REV **A**

SCALE 1/1 PROJ NO. 521-00 SHEET 1 OF 1

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
A		RELEASE PER 8500-023		>

JUMPER TABLE

FROM	TO	FUNCTION	STD 8500 AMCODE	EXT. ENCODE/DECODE	CLOCK WRITING
TP1	TP2	CONNECTS MFM DATA TO WRITE DRIVER	X		
TP1	TP3	CONNECTS WR DATA TO WRITE DRIVERS	X		
TP1	TP4	CONNECTS SECTOR WRITE DATA TO WRITE DRIVERS X	X		
TP5	TP6	WEN RESET BY SECTOR MARKS	OPT	OPT	A
TP5	GND	WEN NOT RESET BY SECTOR MARKS	NOR	NOR	NOR
TP7	---	VCO CONTROL VOLTAGE (CLOCK DECODER)	X		D.C.
TP8	TP9	WRITE ENCODER ENABLED	X		
TP8	GND	WRITE ENCODER DISABLED	X		
TP10	TP11	CONNECTS SETTLING TIME ONESHOT (CLOCK DECODE)	X	X	X
TP10	GND	INHIBITS PULSE INSERTION IN PLL (CLOCK DECODE)	X		D.C.
TP13	TP12	CONNECTS 2XOSC (STD DATA CLK) TO RD CLK	X		D.C.
TP13	TP14	CONNECTS 1XOSC (RD DATA CLK) TO RD CLK	X		D.C.
TP16	TP15	CONNECTS STD DATA TO RDATA	X		D.C.
TP16	TP17	CONNECTS RD DATA TO RDATA	X		D.C.
TP18	GND	DISABLES WEN DELAY AT END OF WRITE	X		D.C.
TP19	TP20	DISABLES RD CLK EN CIRCUIT	X		D.C.
TP21	TP22	UNIT 0 SELECTED	A/R	A/R	A/R
TP21	TP23	UNIT 1 SELECTED ONE OUT OF FOUR	A/R	A/R	A/R
TP21	TP24	UNIT 2 SELECTED	A/R	A/R	A/R
TP21	TP25	UNIT 3 SELECTED	A/R	A/R	A/R
TP26	GND	FORCES LEGAL ADD	NOR	NOR	NOR
TP27	TP28	WR CLK OUT, SECTOR CLK, SISC RDY, AND TRACK ORIGIN GATED BY UNIT SELECT	X	X	D.C.
TP29	---	VCO CONTROL VOLTAGE (DATA SEP)	X		D.C.
J4-2	J4-4	CONNECTS SEPARATOR LATCH TO 2XOSC	X	X	D.C.
TP30	TP32	-01, 146K-154K BITS / TRACK	A/R	AR	AR
TP30	TP31	-01, 134K-146K BITS / TRACK	A/R	AR	AR
TP30	TP31	-02,	A/R	AR	AR
TP30	TP34	-03,	A/R	AR	AR
TP30	TP31	-04,	A/R	AR	AR
TP30	TP32	-05,	A/R	AR	AR

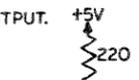
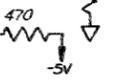
LEGEND: X=CONNECTION
 OPT=OPTIONAL CONFIGURATION
 NOR=NORMAL CONNECTION
 A/R=AS REQUIRED
 BLANKS=MUST BE OPEN
 DC=DON'T CARE

POWER AND GROUND TABLE

I.C. LOCATION	PIN NO.		
	+5V	GND	-5V
U1, U10-U12, U19, U20, U28, U29, U37, U38, U47	-	1, 16	8
U3, U21	9	16	8
U4, U5, U7, U13-U18, U22-U27, U30-U34, U39-U42, U45	14	7	-
U35, U36	5	12	-
U43, U44, U48	16	8	-
ALL (TN)	-	-	1

REFERENCE DESIGNATION

HIGHEST USED	NOT USED
C51	---
R33	---
U48	---
TP34	---

- NOTES:
UNLESS OTHERWISE SPECIFIED
- ALL RESISTORS ARE IN OHMS, 1/4W, 5%. +80% -20%, 25VOLTS.
 - ALL CAPACITORS ARE IN MICROFARADS ;
 - "X" INDICATES OPEN COLLECTOR OUTPUT.
 - "⊙" INDICATES TEST POINT.
 - (RN) INDICATES RESISTOR NETWORK = 
 - ALL TRANSISTOR ARE 2N3906.
 - ALL DIODES ARE 1N4454.
 - (TN) INDICATES TERMINATOR NETWORK: 
 - CUT BETWEEN PADS TO TROUBLESHOOT.
 - SEE VERSION TABLE.

TABULATION BLOCK

REF. DESIG.	-01	-02	-03	-04	-05
C41	27 PF	22 PF	30 PF	22 PF	22 PF
C42	27 PF	22 PF	30 PF	22 PF	22 PF
C43	---	10 PF	5 PF	56 PF	62 PF
C44	---	10 PF	5 PF	56 PF	62 PF
C12	12 PF	22 PF	24 PF	33 PF	33 PF
C50	5 PF	---	---	5 PF	5 PF
U2	50 NSEC	50 NSEC	100 NSEC	100 NSEC	125 NSEC
FREQ. RANGE (MHZ)	7.5-9.93	7-8.65	5.8-8.06	3.97-4.9	2.36-4.5

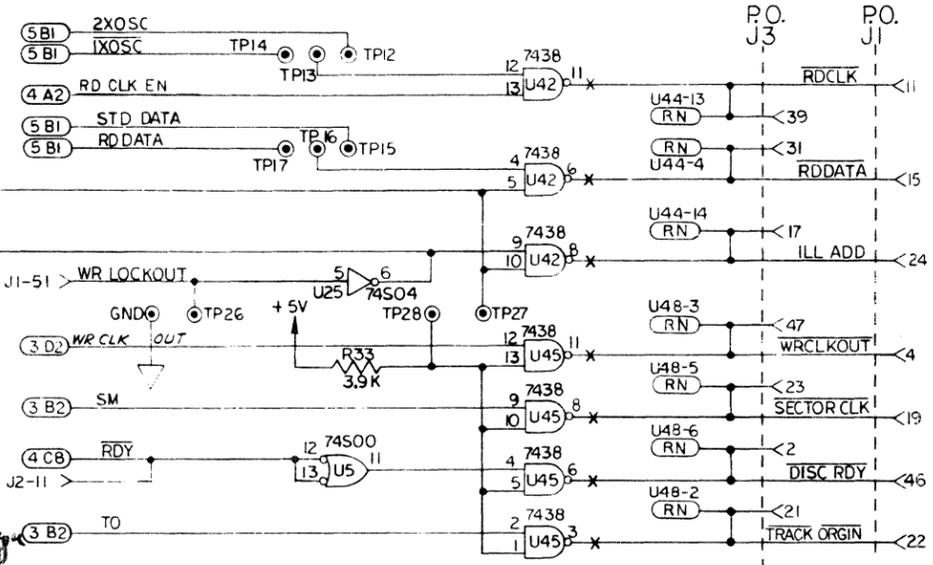
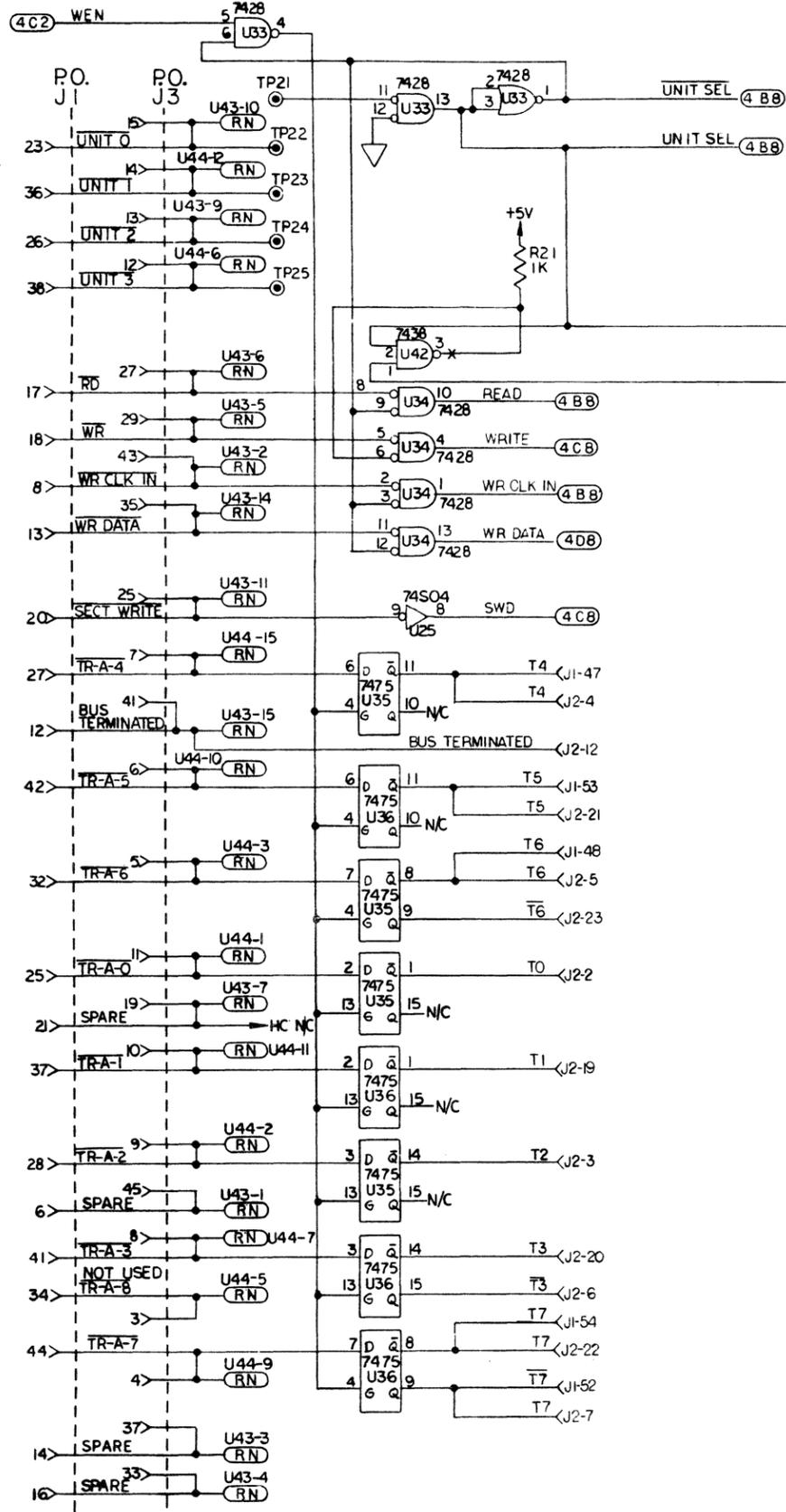
NOTICE
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UNLESS OTHERWISE SPECIFIED		SIGNATURE	DATE
DFT	5/11/77	<i>James A. ...</i>	5/11/77
CHK			
APP			
APP			
8500	1040077		
USED ON	NEXT ASSY.		

QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				
AMCOMP SUNNYVALE, CALIFORNIA				
TITLE SCHEMATIC DIAGRAM AMCODE ADAPTER BD				
SIZE	D	DRAWING NO.	1940077	REV A
SCALE		PROJ. NO.	1521-00	SHEET 1 OF 5

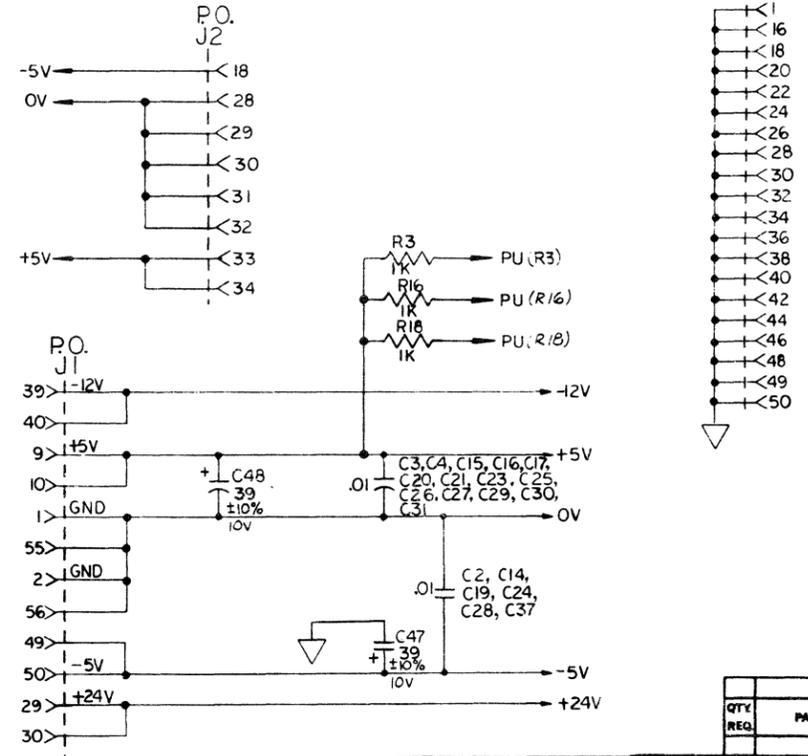
TRANSMITTERS & RECEIVERS

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
A		SEE SHEET 1		



SECTOR M

Track over



QTY	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				

NOTICE	UNLESS OTHERWISE SPECIFIED	SIGNATURE	DATE
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USED ON	NEXT ASSY.		
APPLICATION			

AMCOMP		SUNNYVALE, CALIFORNIA	
TITLE			
- SCHEMATIC -			
AMCODE ADAPTER			
SIZE	DRAWING NO.	REV	
D	1940077	A	
SCALE	PROJ. NO.	SHEET 2 OF 5	

one inhibit preceding zero

8 7 6 5 4 3 2 1

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
A		SEE SHT 1		

WRITE ENCODER writes 0 when 1X OSC is Low and 2 times osc. clocks end of bit cell.

Low for Logic "1"
High for Logic "0"

to write drivers

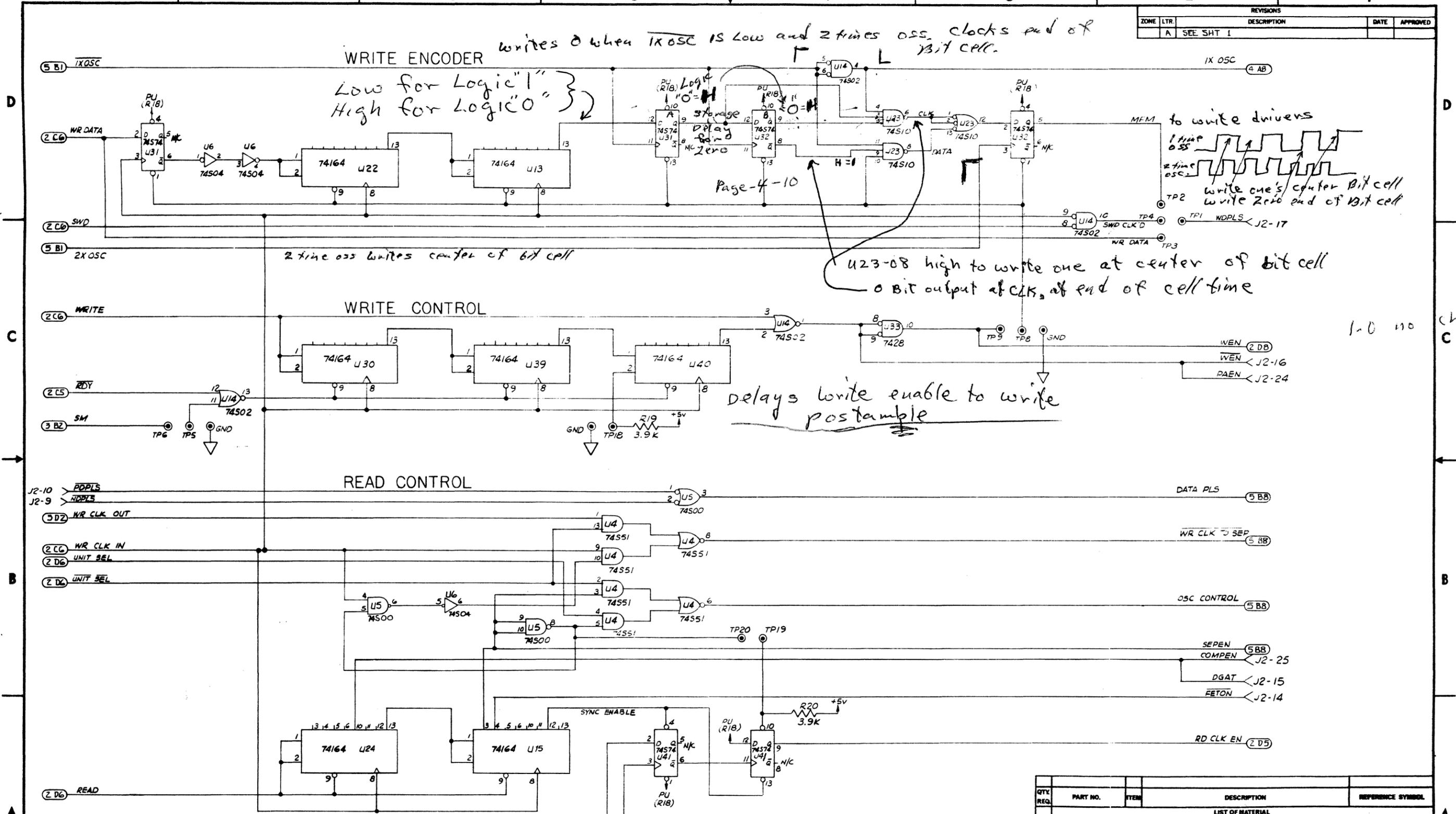
TP2
TP1 NDPLS < J2-17

U23-08 high to write one at center of bit cell
0 bit output at CLK, at end of cell time

2 time osc writes center of bit cell

delays write enable to write postamble

1-0 110 (change)

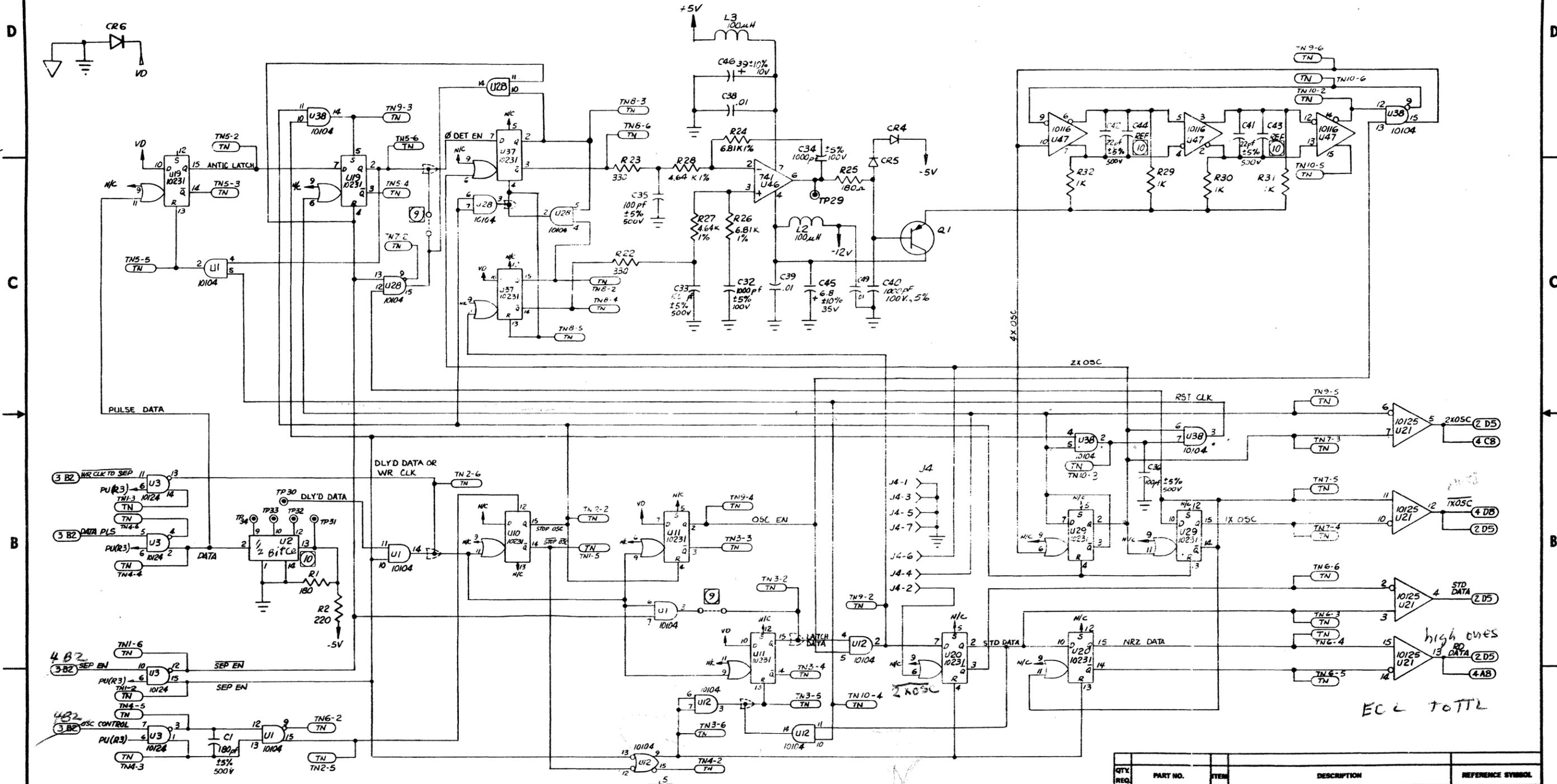


QTY REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				

<p>NOTICE</p> <p>THIS DRAWING SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH IT WAS PREPARED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF AMCOMP, INC. HOWEVER, IF THIS DRAWING IS SPECIFIED TO BE SHOWN TO ANY MEMBER OF GOVERNMENT THIS DRAWING MAY BE USED AS IS PROVIDED BY THE DATA CLAUSE FOR CONTRACT OR SUBCONTRACT.</p>	UNLESS OTHERWISE SPECIFIED	SIGNATURE	DATE	<p>AMCOMP</p> <p>SUNNYVALE, CALIFORNIA</p> <p>TITLE</p> <p>— SCHEMATIC —</p> <p>AMCODE ADAPTER</p> <p>SIZE D DRAWING NO. 1940077</p> <p>SCALE ~ PROJ. NO. SHEET 4 OF 5</p>
	DIMENSIONS ARE IN INCHES			
	DECIMALS TOLERANCES ON ANGLES			
	XXX'S XXX'S			
	MATERIAL	APP.	APP.	
	FINISH			
USED ON	NEXT ASSY.			
APPLICATION				

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
A	SEE SHEET 1			

DATA SEPARATOR



TTL to ECL

ECL TOTTL

Ⓜ: pull down resistors

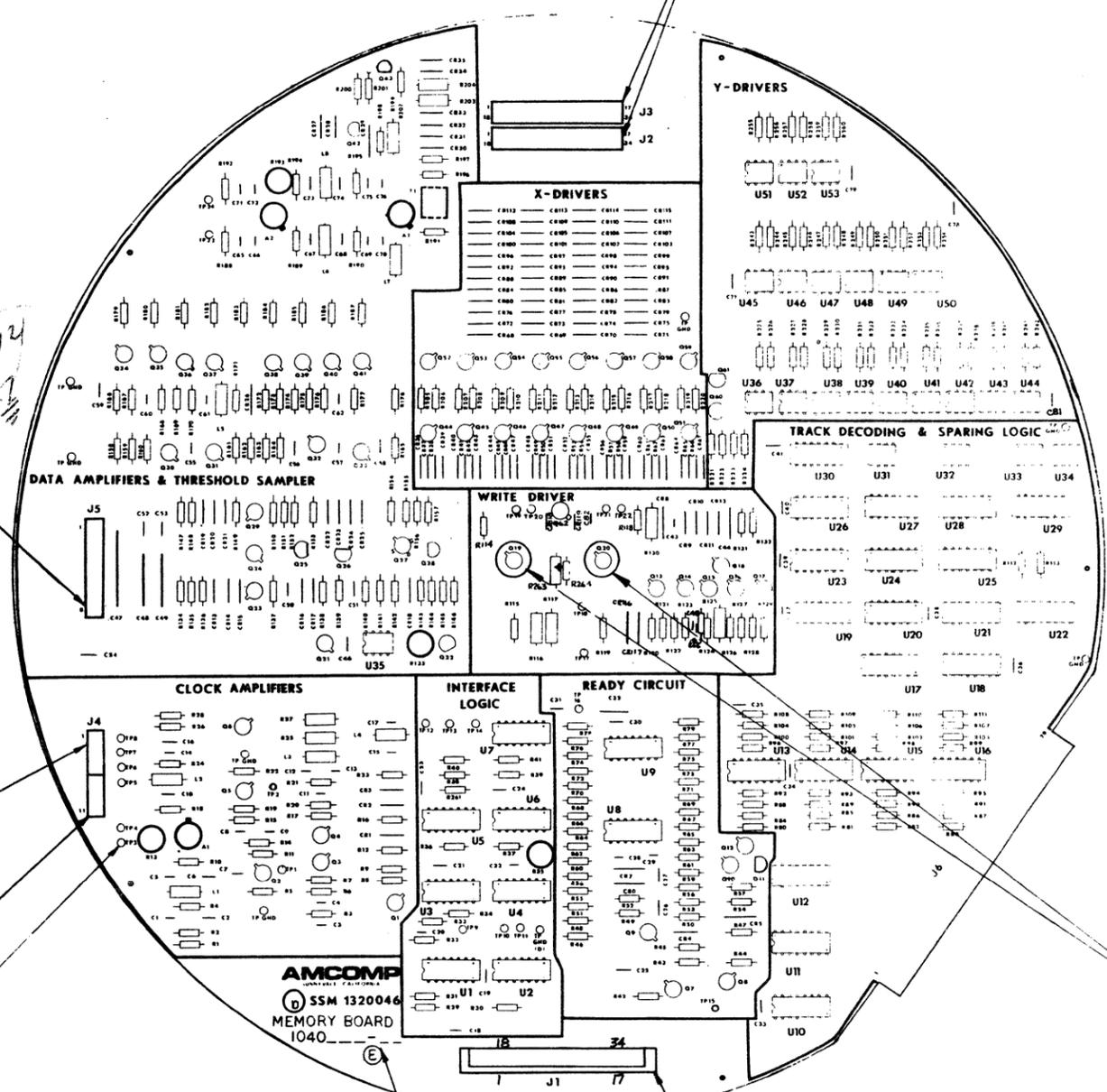
QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				
<p>AMCOMP SUNNYVALE, CALIFORNIA</p> <p>TITLE - SCHEMATIC - AMCODE ADAPTER</p> <p>SIZE D DRAWING NO. 1940077 REV A</p> <p>SCALE _____ PROJ. NO. _____ SHEET 5 OF 5</p>				

NOTICE
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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMALS AND ANGLES	SIGNATURE	DATE
MATERIAL		
FINISH		
USED ON		
NEXT ASSY.		
APPLICATION		

8 7 6 5 4 3 2 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
A		PREPRODUCTION RELEASE/8500-II	9/2/76	plb
B		SEE EO 50489	2/2/77	plb
C		SEE EO 51059 & RELEASE PER 0530-16	3/2/77	plb
D		SEE EO 51566	J.D.M. 7/27/77	plb



- 4 SQUARE PAD DENOTES EMITTER OF TRANSISTOR, POSITIVE POLARITY OF CAPACITOR, CATHODE END OF DIODE.
- 3 MAXIMUM COMPONENT LEAD PROTRUSION ON CIRCUIT SIDE OF BOARD TO BE .060.
2. MAXIMUM COMPONENT HEIGHT ALLOWABLE SHALL BE .400.
- ① IDENTIFY WITH PROPER ASSY PART NO. AND M/L REV. PER 1550010, SEE TABULATION BLOCK.
- NOTES:

32 PLC'S

AMCOMP
SSM 1320046
MEMORY BOARD
1040

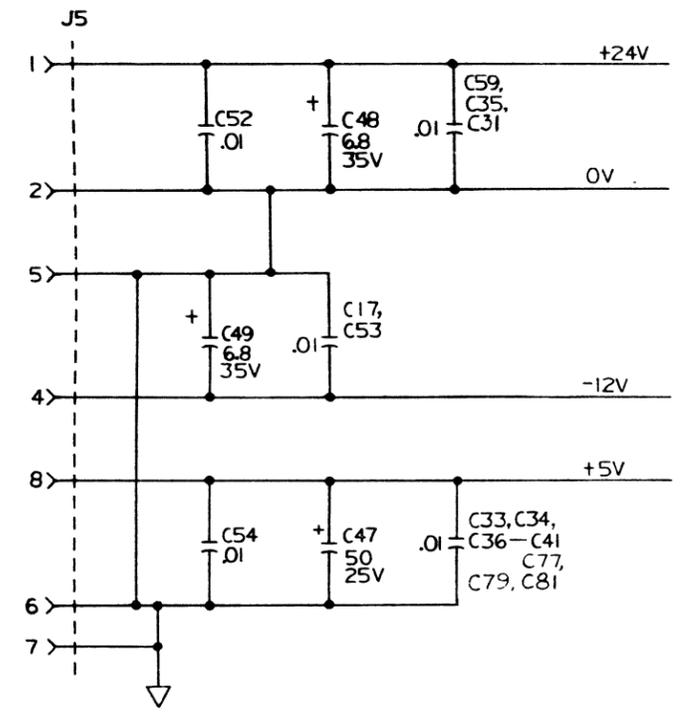
X24 X5 X12

QTY REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				
UNLESS OTHERWISE SPECIFIED			SIGNATURE	DATE
DIMENSIONS ARE IN INCHES			DFT. K.P. JACKSON	8-18-76
TOLERANCES ON ANGLES			CHK. J. DiManno	3-26-76
DECIMALS .005			APR.	
FRACTIONS 1/32			APR.	
MATERIAL			TITLE	
FINISH			PWBA MEMORY	
USED ON			SIZE	DRAWING NO.
NEXT ASSY.			D	1040046
APPLICATION			SCALE	PROJ. NO.
			1:1	SHEET 1 OF 1

NOTICE
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1800 RPM	1040046-02
3600 RPM	1040046-01
DESCRIPTION	PART NO.
TABULATION BLOCK	

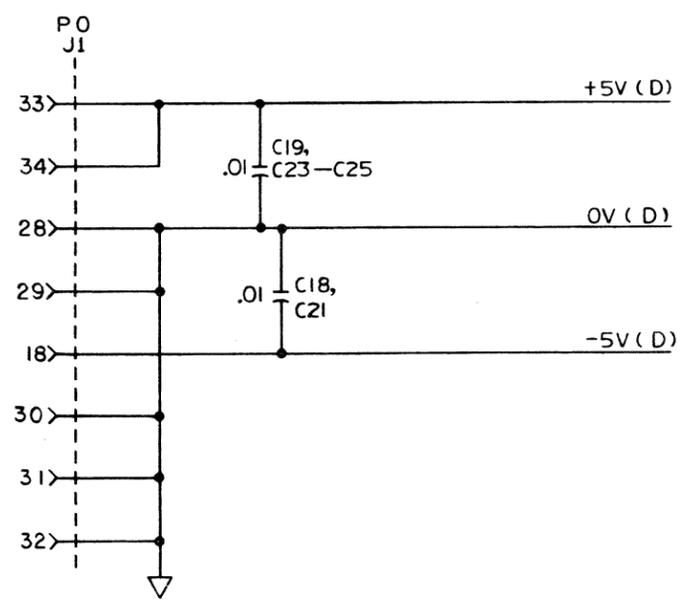
REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
A		PRE PROD RELEASE / 8500-11	8/12/76	AK
B		SEE ED50487	8/3/77	AK
C		SEE ED 51128	8/3/77	AK
D		SEE ED51058 & RELEASE PER B530-16	8/3/77	AK
E		SEE ED 51295	8/18/77	AK
F		SEE ED 51566	11/27-77	AK



J1	
PIN NO.	NOMENCLATURE
18	-5V (D)
19	T1
20	T3
21	T5
22	T7
23	T6 NOT USED
24	PAEN
25	COMPEN
26	N/C
27	N/C
28	0V (D)
29	0V (D)
30	0V (D)
31	0V (D)
32	0V (D)
33	+5V (D)
34	+5V (D)
1	N/C
2	T0
3	T2
4	T4
5	T6
6	T3
7	T7
8	N/C
9	NDPLS
10	PDPLS
11	PDY
12	BUS TERMINATED
13	CLK PLS
14	FETON
15	DATA
16	REN
17	WDPLS

VERSION TABLE					
-01 3600 RPM			-02 1800 RPM		
C20	22PF	500V 5%	C20	68PF	500V 5%
C22			C22		
C62	47PF	500V 5%	C62	100PF	300V 5%
C2			C2		
C6			C6		
	330PF	500V 5%		680PF	500V 5%
C10			C10		
C16			C16		
C73			C73		
C67			C67		
	180PF	300V 5%		330PF	500V 5%
C68			C68		
C74			C74		
L1			L1		
L2	8.2UH	10%	L2	15UH	10%
L5			L5		
L6	3.9UH	10%	L6	8.2UH	10%
L8			L8		
R189			R189		
R194			R194		
	100 OHMS	1/4W 1%		110 OHMS	1/4W 1%
R190			R190		
R195			R195		
R191			R191		
	1.8K	1/4W 5%		3.9K	1/4W 5%
R197			R197		
R116			R116		
	56.2K	1/2W 1%		110K	1/2W 1%
R117			R117		

- NOTES: UNLESS OTHERWISE SPECIFIED
- ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
 - ALL CAPACITORS ARE IN MICROFARADS.
 - ALL DIODES ARE IN4454.
 - ALL TRANSISTORS ARE 2N2222A.
 - "X" INDICATES OPEN COLLECTOR OUTPUT.
 - "⊙" INDICATES TEST POINT.
 - SHEETS 2 & 3, RESISTORS ARE 3.9K, 1/4W, 5%.
 - SEE VERSION TABLE.
 - FOR NORMAL OPERATING CONNECTIONS SEE JUMPER TABLE.



JUMPER TABLE		
FROM	TO	FUNCTION
T15	GND	FORCES RDY CONDITION
TP19	TP20	CONNECTS WRITE CURRENT TO DATA BUS
TP22	TP21	
TP3	TP20	CONNECTS WRITE CURRENT TO CLOCK BUS
TP4	TP21	
TP7	TP8	CLOCK HD 1 SELECTED
TP6	TP8	CLOCK HD 2 SELECTED
TP5	TP8	CLOCK HD 3 SELECTED
RESISTOR BETWEEN		
TP17 & TP18		ALTEPS WRITE CURRENT

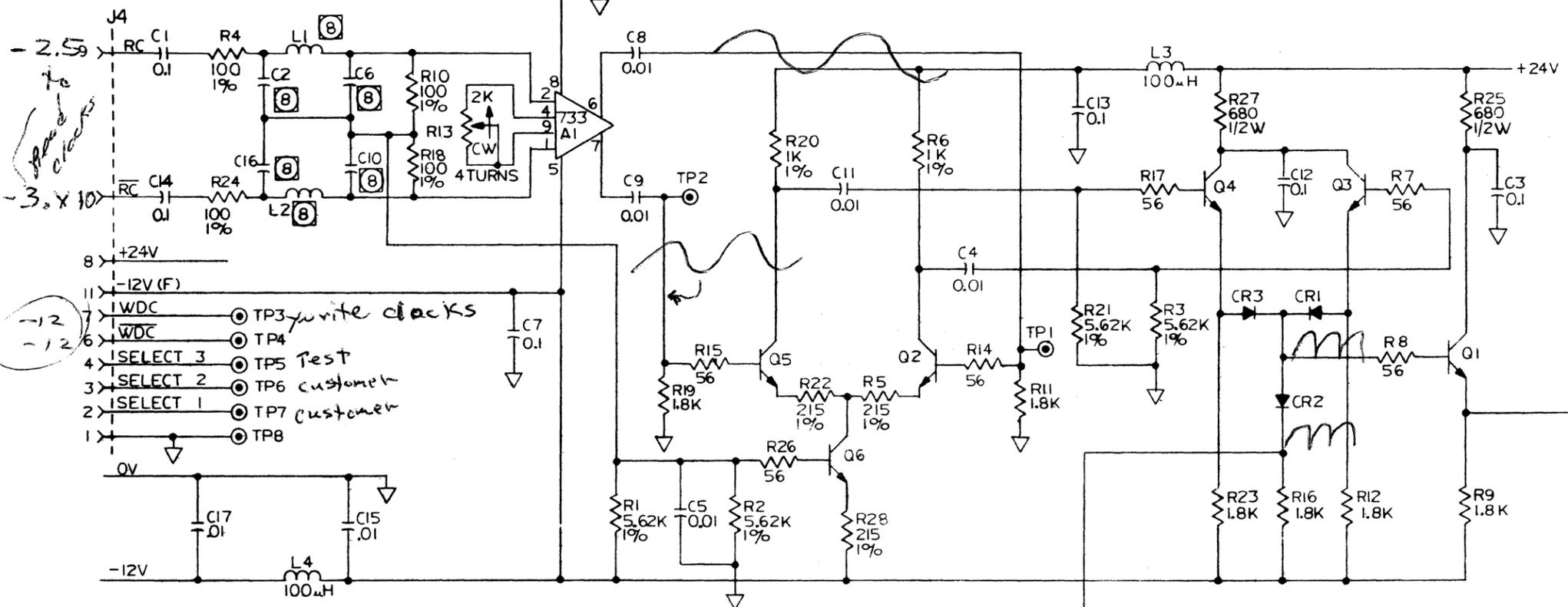
REFERENCE SYMBOLS	
HIGHEST USED	NOT USED
C81	C45, C63, C64
CR117	CR6
J6	---
L8	---
Q61	---
R262	---
TP24	---
U53	---

QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL																				
LIST OF MATERIAL																								
<table border="1"> <tr> <td>NOTICE</td> <td>UNLESS OTHERWISE SPECIFIED</td> <td>SIGNATURE</td> <td>DATE</td> </tr> <tr> <td>THIS DRAWING SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH IT WAS DESIGNED OR DISCLOSED BY WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF AMCOMP, INC. HOWEVER, IF THIS DRAWING IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DRAWING MAY BE USED AS IS PERMITTED BY THE DATA CLEARANCE PER CONTRACT OR SUB-CONTRACT.</td> <td>DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS ANGLES</td> <td>James A. Roberts</td> <td>8/12/76</td> </tr> <tr> <td></td> <td></td> <td>J. J. M.</td> <td>8-26-76</td> </tr> <tr> <td></td> <td></td> <td>APP. _____</td> <td>APP. _____</td> </tr> <tr> <td></td> <td></td> <td>APP. _____</td> <td>APP. _____</td> </tr> </table>					NOTICE	UNLESS OTHERWISE SPECIFIED	SIGNATURE	DATE	THIS DRAWING SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH IT WAS DESIGNED OR DISCLOSED BY WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF AMCOMP, INC. HOWEVER, IF THIS DRAWING IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DRAWING MAY BE USED AS IS PERMITTED BY THE DATA CLEARANCE PER CONTRACT OR SUB-CONTRACT.	DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS ANGLES	James A. Roberts	8/12/76			J. J. M.	8-26-76			APP. _____	APP. _____			APP. _____	APP. _____
NOTICE	UNLESS OTHERWISE SPECIFIED	SIGNATURE	DATE																					
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		J. J. M.	8-26-76																					
		APP. _____	APP. _____																					
		APP. _____	APP. _____																					
8500		1040046		FINISH																				
USED ON		NEXT ASSY.		APPLICATION																				
SCALE		PROJ. NO.		SHEET / OF 7																				

AMCOMP SUNNYVALE, CALIFORNIA	
TITLE SCHEMATIC DIAGRAM MEMORY PWBA	
SIZE D	DRAWING NO. 1940046
SCALE	SHEET / OF 7

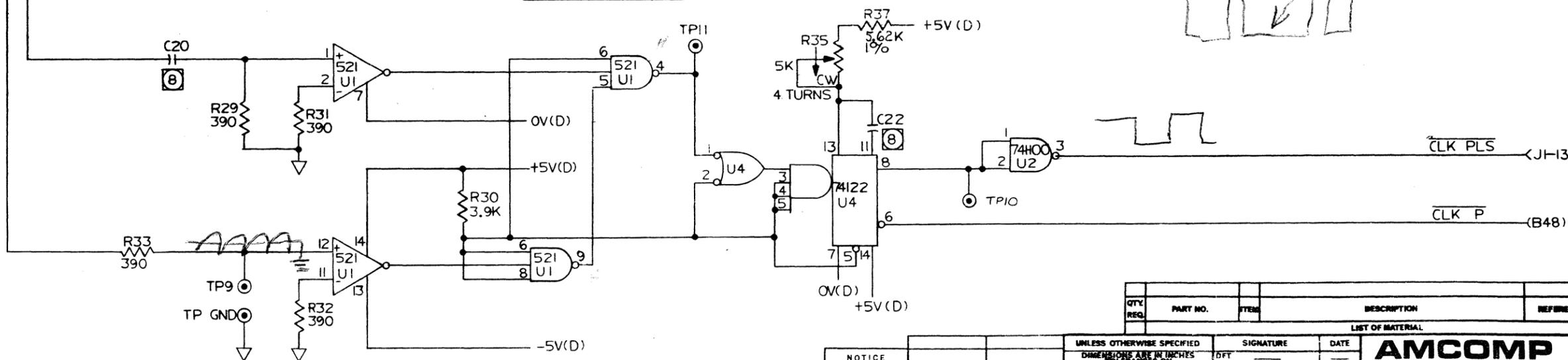
REVISIONS			
ZONE	LTR	DESCRIPTION	DATE
F		SEE SHEET 1	

CLOCK AMPLIFIERS



- 8 +24V
- 11 -12V (F)
- 7 WDC TP3 write clocks
- 6 WDC TP4
- 4 SELECT 3 TP5 Test
- 3 SELECT 2 TP6 customer
- 2 SELECT 1 TP7 customer
- 1 TP8

INTERFACE LOGIC



TP10 sector mark

QTY REQ	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				

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	DIMENSIONS ARE IN INCHES DECIMALS TO 3 ANGLES TO 10'	DFT		
	MATERIAL	APP		
	FINISH	APP		
USED ON	NEXT ASSY.			

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
F		SEE SHEET 1		

WRITE DRIVER

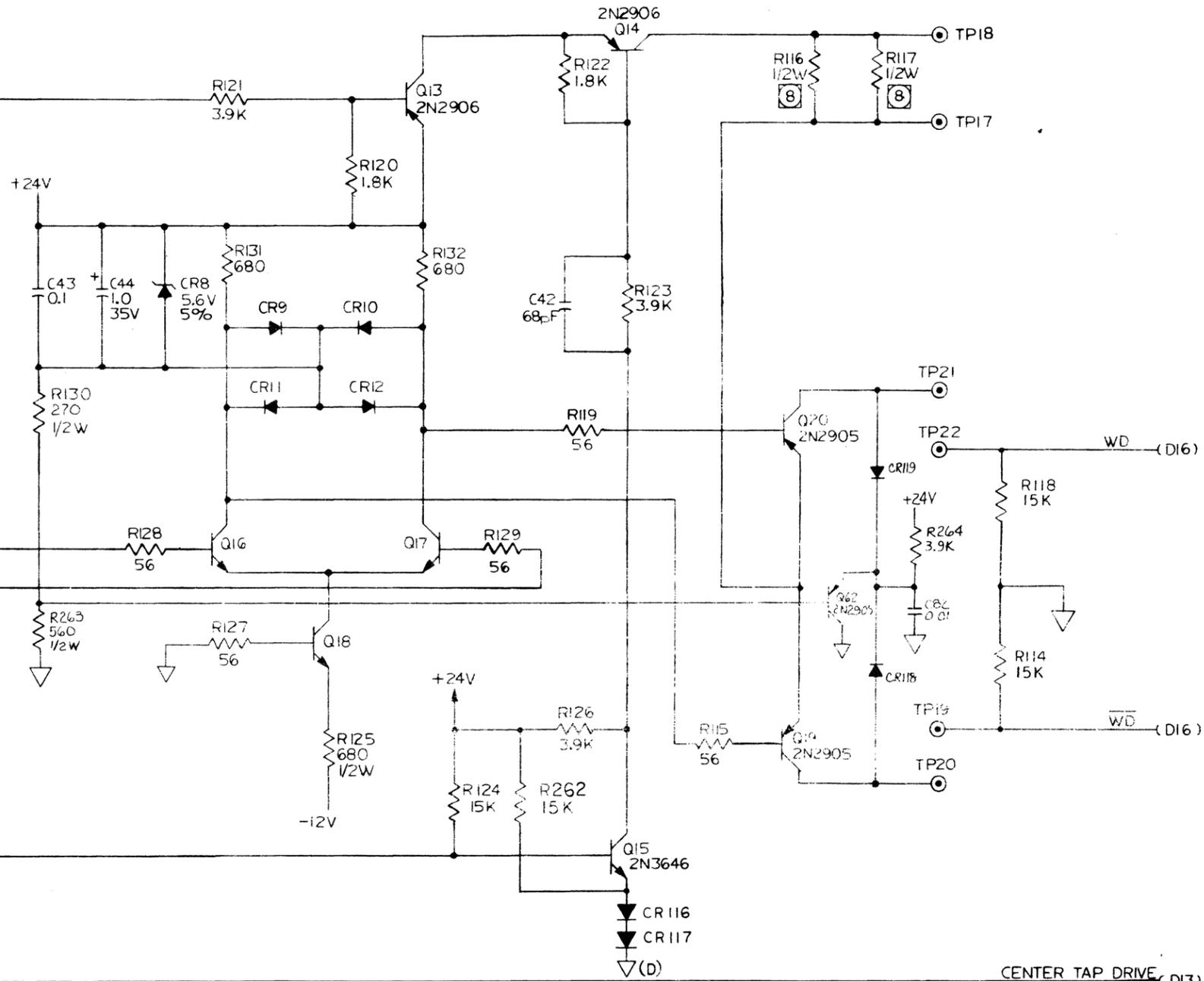
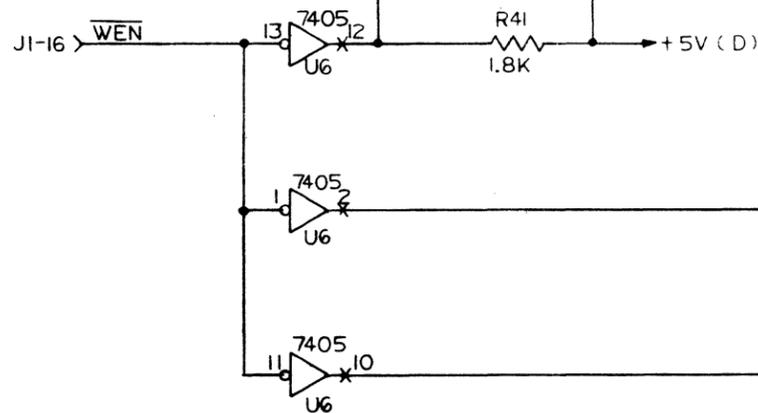
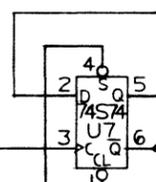
(D41) WRITE DISABLE

INTERFACE LOGIC

FMM

J1-17 WD PLS

J1-16 WEN



QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				

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	DIMENSIONS ARE IN INCHES	DFI: _____	_____
	TOLERANCES ON ANGLES	CHK: _____	_____
	DECIMALS	APP: _____	_____
	MATERIAL	APP: _____	_____
	FINISH		
	USED ON		
	NEXT ASSY.		
	APPLICATION		

AMCOMP
SUNNYVALE, CALIFORNIA

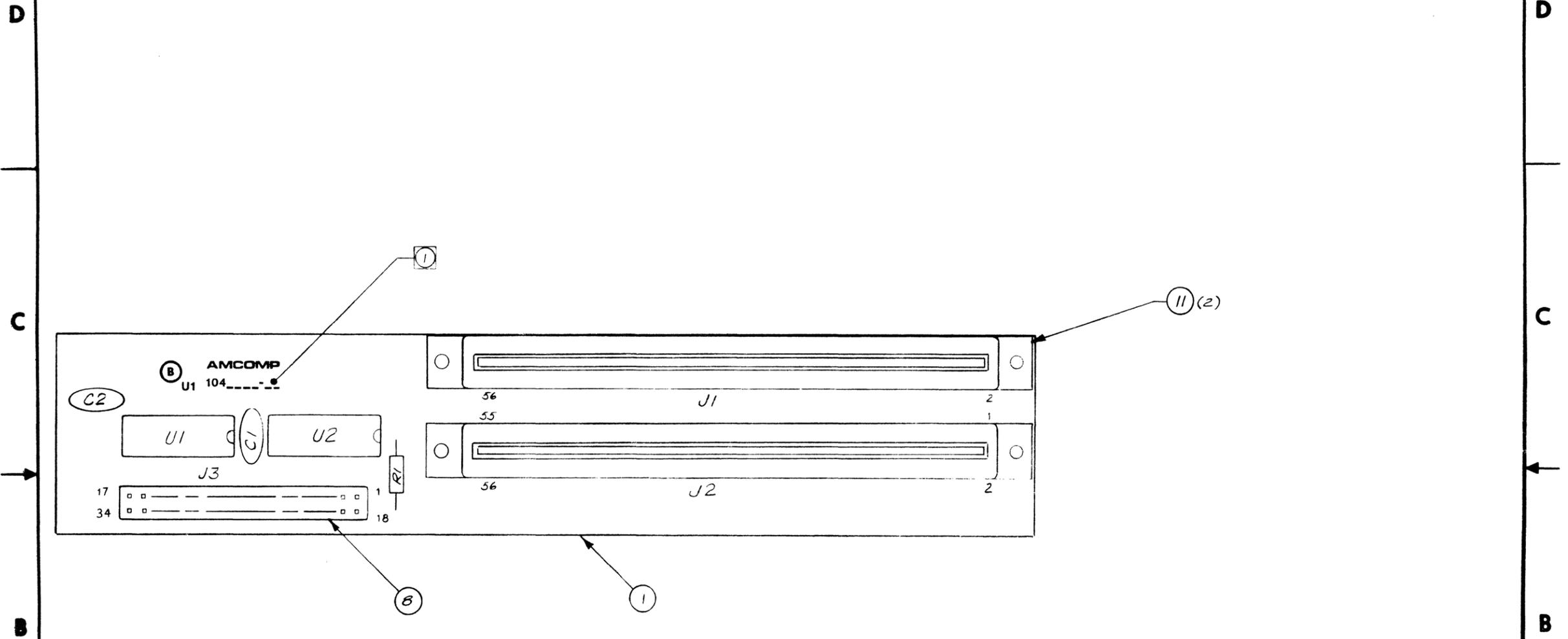
TITLE
**SCHEMATIC DIAGRAM
MEMORY PWBA**

SIZE **D** DRAWING NO. **1940046**

SCALE _____ PROJ. NO. _____ SHEET 7 OF 7

4 | 3 | 2 | 1

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	B	REVISED & REDRAWN SEE ED. 50078	7/29/76	Mo.
	C	RELEASE PER 8530-14	2/21/77	RCC-MO



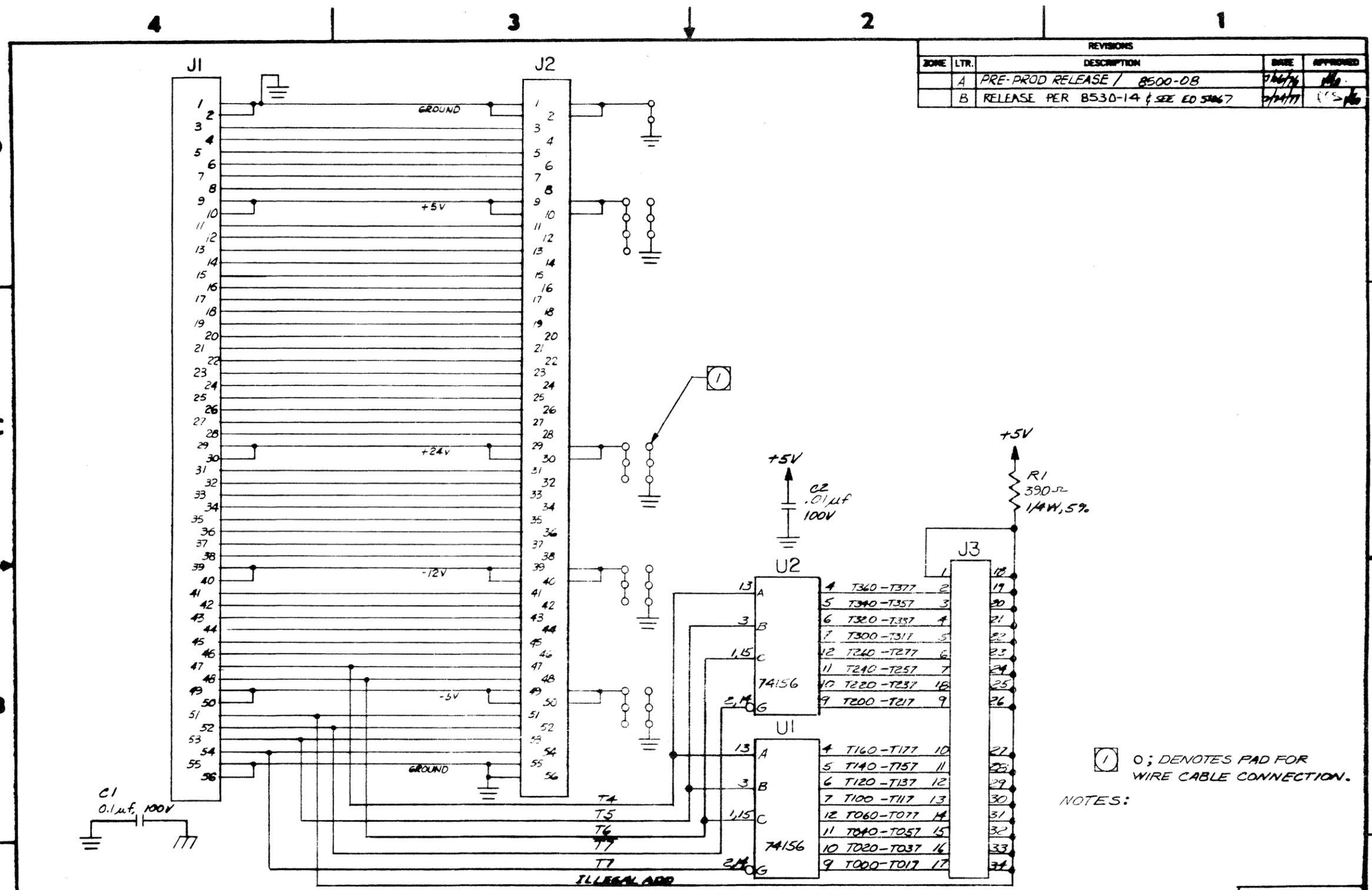
2. MAXIMUM COMPONENT LEAD PROTRUSION ON CIRCUIT SIDE OF BOARD SHALL BE .060

① IDENTIFY WITH ASSY PART NO. 1040060-01 & CURRENT M/L REVISION PER 1550010.

NOTES:

QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				

<p>NOTICE</p> <p>THIS DWG SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF DATA DISC, INC. HOWEVER, IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUB-CONTRACT.</p>	<p>UNLESS OTHERWISE SPECIFIED</p> <p>DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .XX=± .XXX=±</p>		<p>SIGNATURE</p> <p>DFT. <i>J. Hall</i> CHK. <i>W. Rona</i> APP. <i>L. Allen</i> APP.</p>		<p>DATE</p> <p>7/29/76 7/22/76 7/22/76</p>	<p>DATA DISC INCORPORATED</p> <p>TITLE</p> <p>MINI MOTHER PWBA</p>		
	<p>8500</p>	<p>1060090</p>	<p>FINISH</p>		<p>SIZE</p> <p>C</p>		<p>DRAWING NO.</p> <p>1040060</p>	<p>REV</p> <p>C</p>
	<p>USED ON</p>	<p>NEXT ASSY.</p>	<p>APPLICATION</p>		<p>SCALE</p>		<p>PROJ. NO.</p>	<p>SHEET 1 OF 1</p>
	<p>6-41/42</p>							



REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
A		PRE-PROD RELEASE / 8500-DB	7/24/76	[Signature]
B		RELEASE PER 8530-14 & SEE ED 5067	7/24/77	[Signature]

⓪; DENOTES PAD FOR WIRE CABLE CONNECTION.
 NOTES:

NOTICE
 INFORMATION CONTAINED HEREIN IS UNCLASSIFIED EXCEPT WHERE SHOWN OTHERWISE. DATE 08-01-2001 BY 60322 UCBAW/SJS/STP

USED ON	8500	1040060
PROJECT NO.		
APPLICATION		

DESIGNS OTHERWISE SPECIFIED	SIGNATURE	DATE
DRY T. [Signature]	7-24-76	
CHK. W. ROMA-	7-24-76	
APP. J. J. WITBANE	7-24-76	

LIST OF MATERIAL		
SCHEMATIC - MINI MOTHER BOARD		
SIZE C	DRAWING NO. 1940060	REV. B
SCALE ~	PROJ. NO.	SHEET 1 OF 1

4

3

2

1

HOLE SCHEDULE		
SYM	DIAMETER	QTY
UNCODED	.037 ±.003 DIAM	151
A	.375 ±.003 DIAM	4 (3)
B	.047 ±.003 DIAM.	1

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	A	PRE-PRODUCTION RELEASE 8400-86	5/19/76	WJL
	A1	PRODUCTION RELEASE 8400-101	8/9/76	KS

D

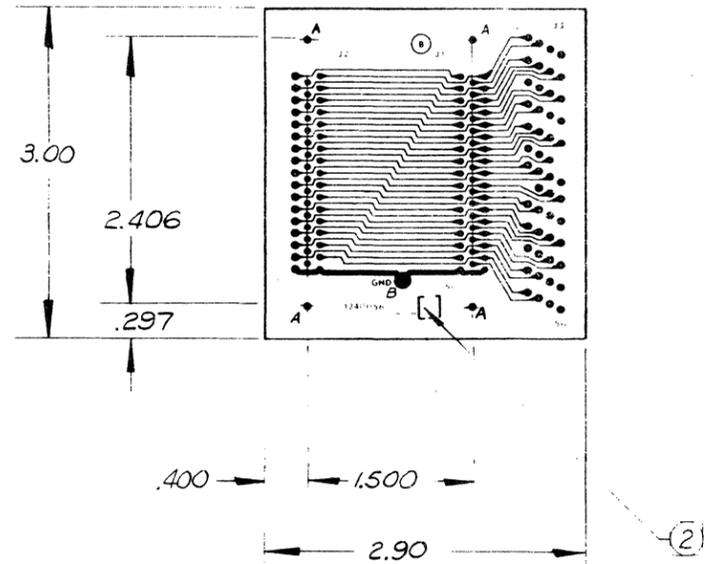
D

C

C

B

B



- (3) PLATED THRU HOLES OPTIONAL.
- (2) IDENTIFY WITH CURRENT REVISION OF THIS DRAWING, AND APPROPRIATE DASH NUMBER.
 1. MANUFACTURE PER SPEC 1550009, USING PRINTED WIRE MASTER 1310056. SHEETS 1 & 2, REVISION NOTED.

NOTES:

QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				

NOTICE
 THIS DWG SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF DATA DISC, INC. HOWEVER, IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY AGENCY OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAIM PER CONTRACT OR SUB-CONTRACT.

B	1240056-01
PWM REV.	PART NO
TABULATION BLOCK	

UNLESS OTHERWISE SPECIFIED	
DIMENSIONS ARE IN INCHES	SIGNATURE
TOLERANCES ON ANGLES	DATE
DECIMALS .XX ± .02	DFT. BOB SAKAI 4/7/76
XXX ± .010	CHK. W. ROMA 5/7/76
MATERIAL	APP. [Signature] 5/19/76
.062" 2/2	APP. [Signature] 5/7/76
FINISH	
USED ON	NEXT ASSY.
8400 B	1040057
8500	1040057
APPLICATION	

DATE	4/7/76
SIGNATURE	BOB SAKAI
DATE	5/7/76
SIGNATURE	W. ROMA
DATE	5/19/76
SIGNATURE	[Signature]
DATE	5/7/76
SIGNATURE	[Signature]

DATA DISC
INCORPORATED

TITLE
RP INTERCONNECT PWB

SIZE **C** DRAWING NO. 1240056 REV A1

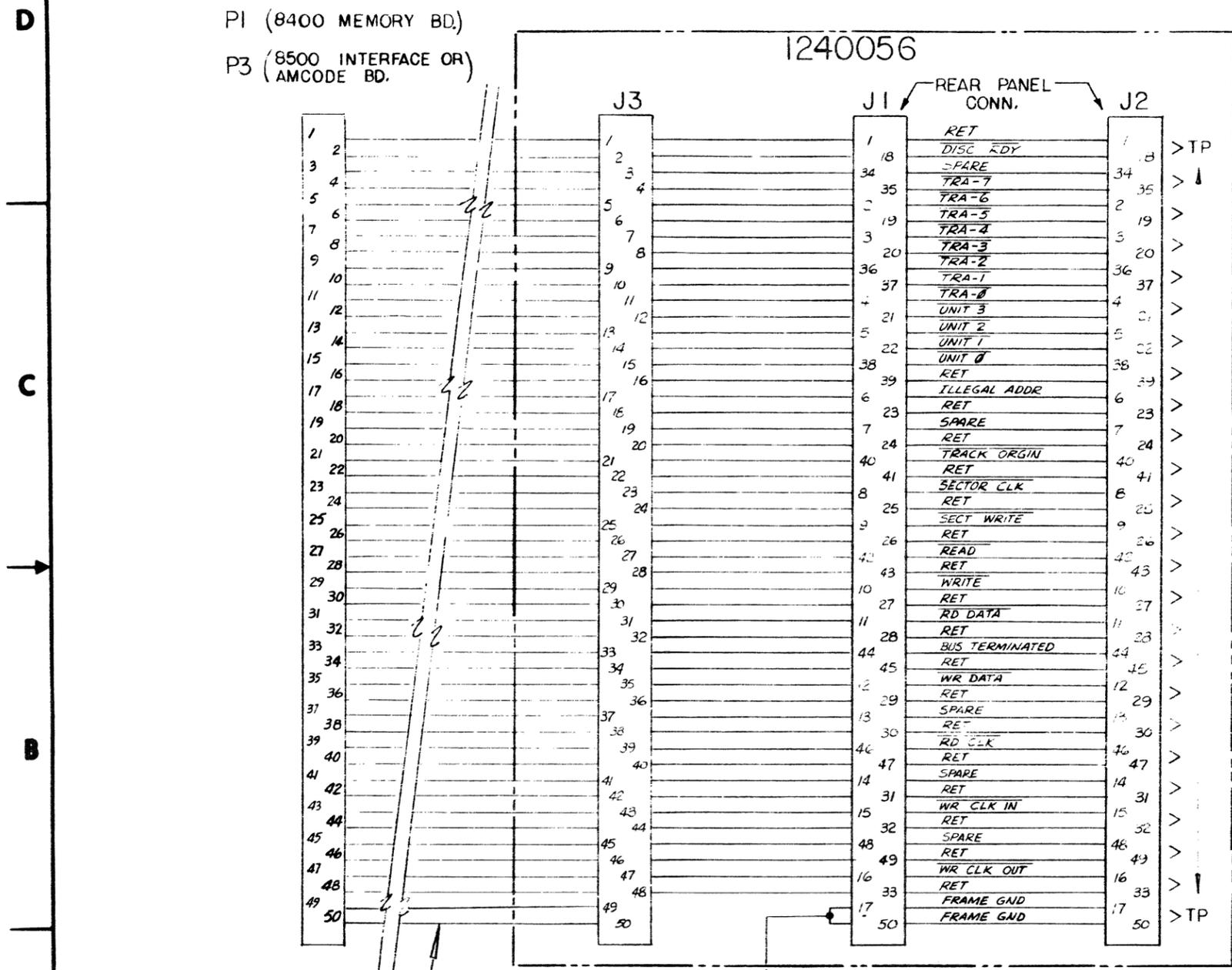
SCALE 1:1 PROJ. NO. SHEET / OF /

A

A

4 3 2 1

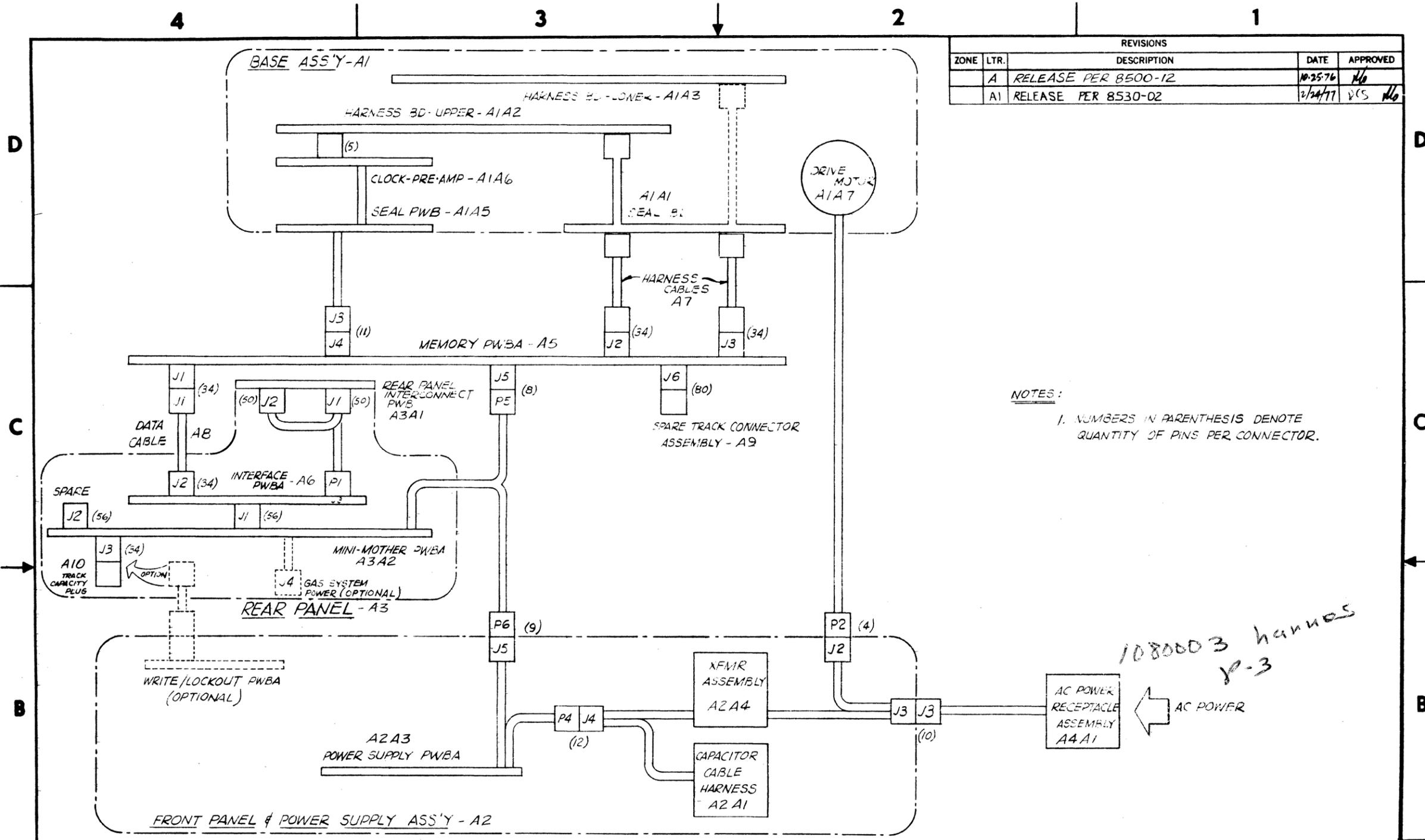
REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	A	PRE-PROD. RELEASE PER 8400-86	5/10/76	WJK
	A1	PROD. RELEASE 8400-101	8/19/76	CS
	A2	SEE EO 51554	5/12/77	WJK



NOTES
1. TP* DESIGNATES TWISTED PAIR.

CABLE ASSEMBLY (REF.)

QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				
<p>NOTICE: THIS DWG SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF DATA DISC, INC. HOWEVER, IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUB-CONTRACT.</p>				
<p>UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .XX±.2 .XXX±.2 ANGLES</p>		<p>SIGNATURE DATE</p> <p>DFT. BOB SAKAI 4.6.76</p> <p>CHK. W. Rima 5.6.76</p> <p>APP. R. [Signature] 5.3.76</p> <p>APP. [Signature] 5.4.76</p>		<p>TITLE</p> <p>— SCHEMATIC DIAGRAM — REAR PANEL INTERCONNECT PWB</p>
<p>MATERIAL</p> <p>8500 1040057</p> <p>8400 B 1040057</p> <p>USED ON NEXT ASSY.</p>		<p>FINISH</p>		
<p>APPLICATION</p>		<p>SIZE C DRAWING NO. 1940056</p>		<p>REV A2</p>
<p>SCALE ~</p>		<p>PROJ. NO.</p>		<p>SHEET / OF /</p>



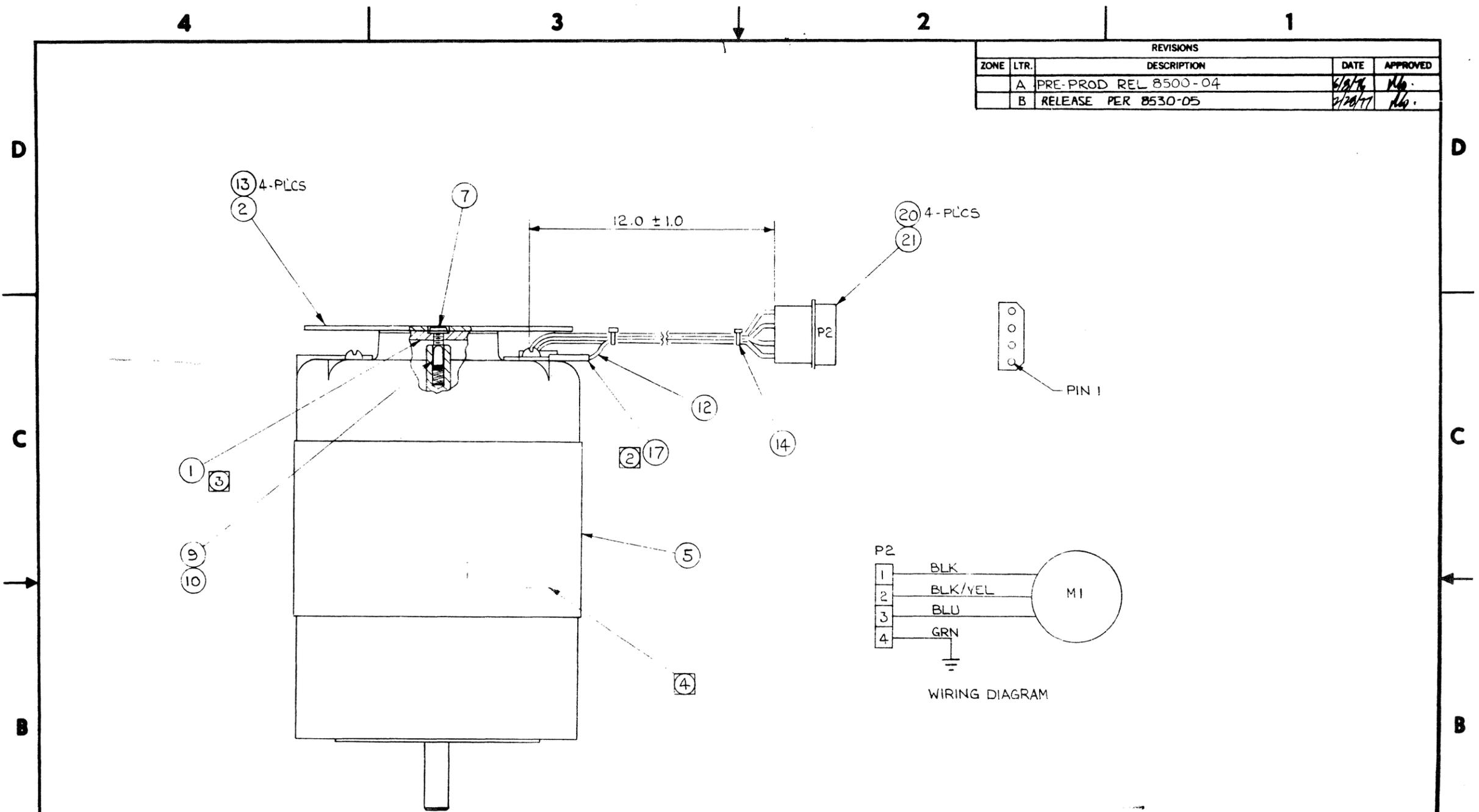
REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
A		RELEASE PER 8500-12	10-25-76	RS
A1		RELEASE PER 8530-02	2/24/77	RS

NOTES:
 1. NUMBERS IN PARENTHESIS DENOTE QUANTITY OF PINS PER CONNECTOR.

QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				
UNLESS OTHERWISE SPECIFIED		SIGNATURE		DATE
DIMENSIONS ARE IN INCHES		DFT. ROBERT SAKAI		2-4-76
TOLERANCES ON ANGLES		CHK. W. Burns		2-27-76
DECIMALS		APP. [Signature]		2-27-76
XXX±		APP. [Signature]		
MATERIAL		TITLE		
FINISH		DATA DISC INCORPORATED		
USED ON		SYSTEM INTERCONNECT DIAGRAM		
NEXT ASSY.		— 8500 —		
APPLICATION		SIZE C		DRAWING NO. 1930009
		SCALE		REV A1
		PROJ. NO. 8500		SHEET 1 OF 1

NOTICE
 THIS DWG SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF DATA DISC, INC. HOWEVER, IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUB-CONTRACT.

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
A		PRE-PROD REL 8500-04	8/27/76	RLG.
B		RELEASE PER 8530-05	2/20/77	RLG.

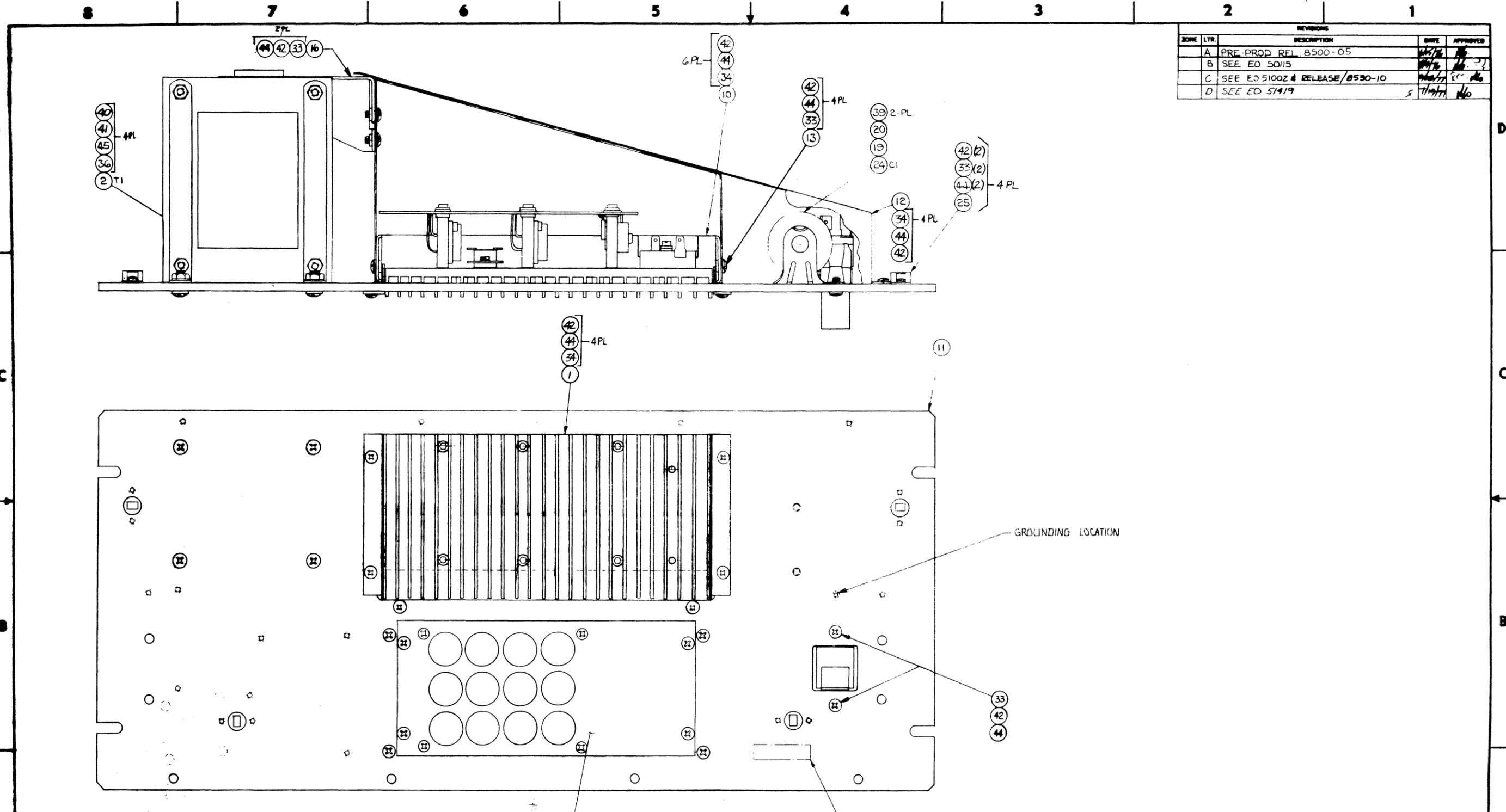


- NOTES:
1. WORKMANSHIP SHALL COMPLY WITH QA 100000-00.
 2. ASSEMBLE USING EXISTING SCREW IN MOTOR.
 3. REMOVE & DISCARD EXISTING END PLATE, 4 SCREWS & REPLACE WITH ITEMS 1 & 13.
 4. IDENTIFY WITH ASSY NO 1020085 & APPROPRIATE DASH NO WITH CURRENT M/L REV PER 1550010.

QTY REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				

NOTICE THIS DRAWING SHALL NOT BE REPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF DATA DISC, INC. HOWEVER, IF THIS DRAWING IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DRAWING MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUB-CONTRACT.	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMALS: .XX ± ANGLES: .XXX ±	SIGNATURE DFT. [Signature] CHK. [Signature] APR. [Signature] APP. [Signature]	DATE 8/27/76 8/28/76 8/29/76	 TITLE DRIVE MOTOR ASSY	
	MATERIAL 8503 1020133 8500 1020132	FINISH —	SIZE C DRAWING NO. 1020085 SCALE —		REV B SHEET 1 OF 1
	APPLICATION USED ON NEXT ASSY.	PROJECT NO.	PROJ. NO.		SHEET 1 OF 1
	APPLICATION		PROJ. NO.		SHEET 1 OF 1

REVISIONS			
ZONE	LTR.	DESCRIPTION	DATE
A		PRE-PROD. REL. 8500-05	
B		SEE EO 50115	
C		SEE EO 51002 & RELEASE/8530-10	
D		SEE EO 51419	

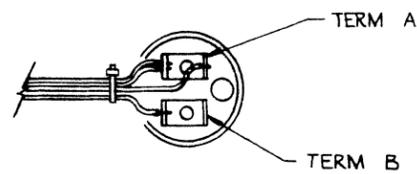


- NOTES:
1. WORKMANSHIP SHALL COMPLY WITH QA100000-00.
 2. IDENTIFY WITH ASSY NO 1020059 & APPROPRIATE DASH NO WITH CURRENT M/L REV.
 3. FOR WIRING DIAGRAM SEE DWG NO. 1930019.
 4. WIRES INDICATED TO BE CRIMPED 2 WIRES PER CONTACT (ITEM 50).
 5. ORIENTATION OF CLAMP ON CAPACITOR TO BE IN APPROX LOCATION SHOWN.

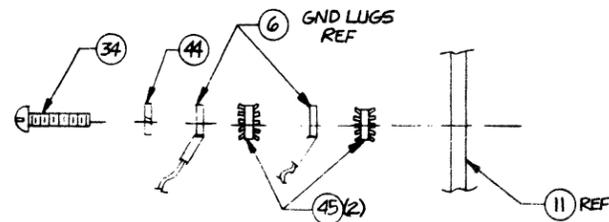
3
33
44
45
4 PL

QTY.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL																		
LIST OF MATERIAL																						
<table border="1"> <tr> <td>NOTICE</td> <td>UNLESS OTHERWISE SPECIFIED</td> <td>SIGNATURE</td> <td>DATE</td> </tr> <tr> <td rowspan="4"> <small>THIS DRAWING MAY BE USED FOR PRODUCTION ONLY IF THE ORIGINAL DRAWING IS AVAILABLE FOR REFERENCE. ANY CHANGES TO THIS DRAWING MUST BE APPROVED BY THE ORIGINAL DRAWING ENGINEER.</small> </td> <td> <small>DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED</small> DECIMALS FRACTIONS ANGLES </td> <td>DFT.</td> <td>2/9/70</td> </tr> <tr> <td>MATERIAL</td> <td>CHK.</td> <td>5/1/70</td> </tr> <tr> <td>FINISH</td> <td>APP.</td> <td>6/8/70</td> </tr> <tr> <td>USED ON</td> <td>NEXT ASSY.</td> <td>APP.</td> <td>2/7/77</td> </tr> </table>					NOTICE	UNLESS OTHERWISE SPECIFIED	SIGNATURE	DATE	<small>THIS DRAWING MAY BE USED FOR PRODUCTION ONLY IF THE ORIGINAL DRAWING IS AVAILABLE FOR REFERENCE. ANY CHANGES TO THIS DRAWING MUST BE APPROVED BY THE ORIGINAL DRAWING ENGINEER.</small>	<small>DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED</small> DECIMALS FRACTIONS ANGLES	DFT.	2/9/70	MATERIAL	CHK.	5/1/70	FINISH	APP.	6/8/70	USED ON	NEXT ASSY.	APP.	2/7/77
NOTICE	UNLESS OTHERWISE SPECIFIED	SIGNATURE	DATE																			
<small>THIS DRAWING MAY BE USED FOR PRODUCTION ONLY IF THE ORIGINAL DRAWING IS AVAILABLE FOR REFERENCE. ANY CHANGES TO THIS DRAWING MUST BE APPROVED BY THE ORIGINAL DRAWING ENGINEER.</small>	<small>DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED</small> DECIMALS FRACTIONS ANGLES	DFT.	2/9/70																			
	MATERIAL	CHK.	5/1/70																			
	FINISH	APP.	6/8/70																			
	USED ON	NEXT ASSY.	APP.	2/7/77																		
TITLE FRONT PANEL & PWR SUPPLY ASSY			DRAWING NO. 1020059																			
SCALE 1/1		SHEET 1 OF 1																				

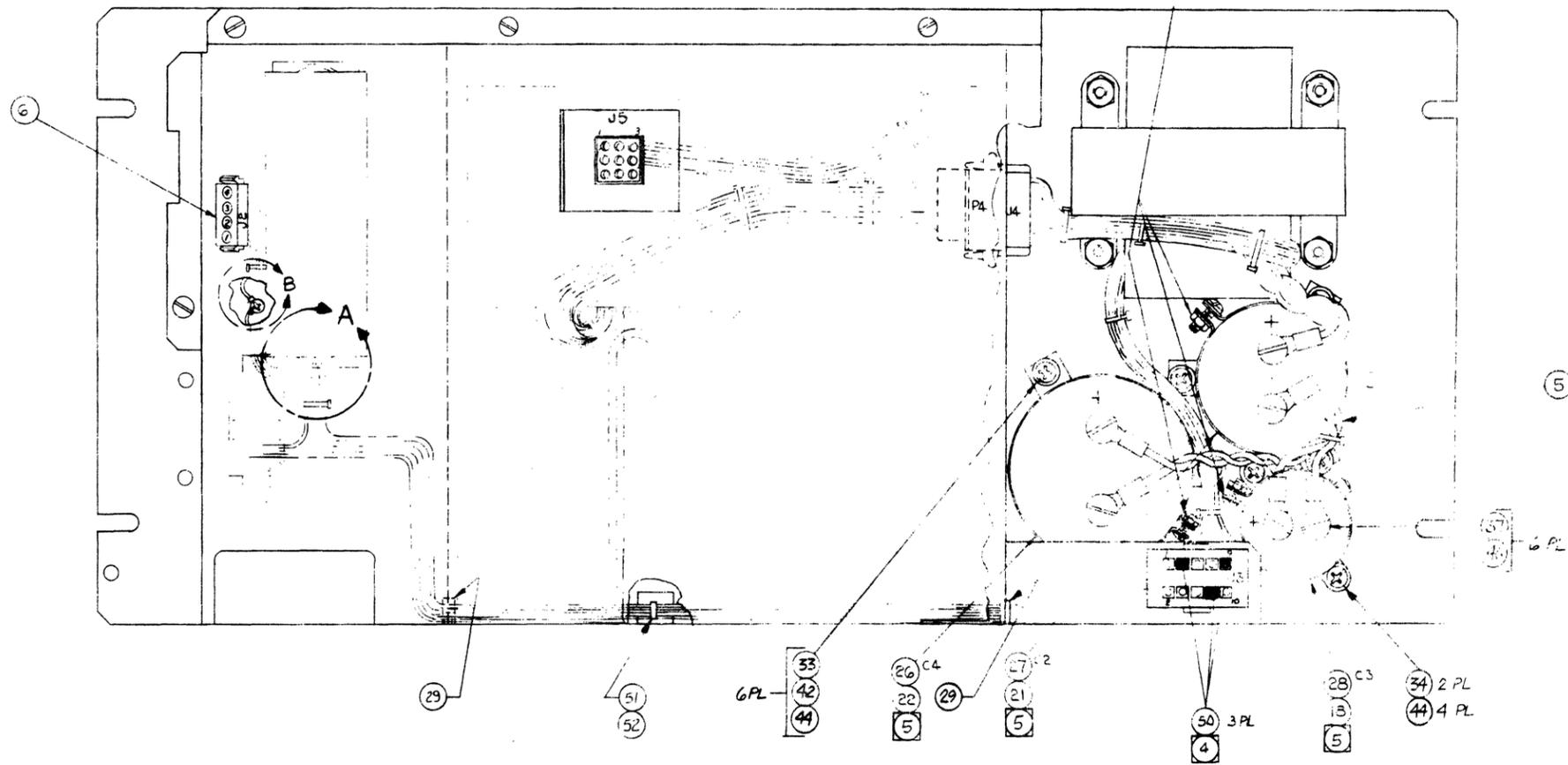
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
D		SEE SHEET 1		



DETAIL A
CI WIRING



DETAIL B
SCALE 2/1



WIRING TABLE	
FROM COMP-PIN & COLOR	TO COMP - PIN
T1-BLU	J4-6
T1-BLU	J4-5
T1-RED	J4-4
T1-RED	J4-3
T1-DRN	J4-2
T1-DRN	J4-1
T1-GRN	J3-3
J2-4	
T1-YEL	J3-9
SW1-YEL	
T1-VIO	J3-8
C1-A (VIO)	
B1-BLK	C1-A
J2-1 (BLK)	C1-A
J2-3 (BLU)	C1-B
C2+ BLK	J4-10
C2- RED	J4-9
C3+ BLU	J4-11
C3- BLK	J4-12
C4+ DRN	J4-7
C4- BLK	J4-8
T1 WHT	J3-6
T1 BLK	J3-5
T1 BLU	J3-7

REF

QTY REQ	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMALS TO 2 PLACES TOLERANCES ON MATERIAL				
SIGNATURE		DATE		
DFT.		CHK.		
APP.		XPR.		
FINISH		APPLICATION		
USED ON		NEXT ASSY.		
SCALE		PANEL NO.		
SIZE		DRAWING NO.		
D		1020059		
SHEET 2 OF 2		D		

NOTICE
THIS DRAWING SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH IT WAS PREPARED OR INCORPORATED IN ANY PRODUCT OR PART THEREOF WITHOUT THE WRITTEN CONSENT OF THE COMPANY. ANY REVISIONS TO THIS DRAWING SHALL BE INDICATED BY A REVISION SYMBOL AND A REVISION DESCRIPTION. THIS DRAWING IS THE PROPERTY OF THE COMPANY AND IS LOANED TO YOU BY THE COMPANY. IT IS TO BE KEPT IN CONFIDENCE AND NOT TO BE DISCLOSED TO ANY OTHER PARTY WITHOUT THE WRITTEN CONSENT OF THE COMPANY.



TITLE
FRONT PANEL
PWR SUPPLY ASSY

SIZE D DRAWING NO. 1020059

SCALE SHEET 2 OF 2

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
A		RELEASE/8500-12	10-2-76	16

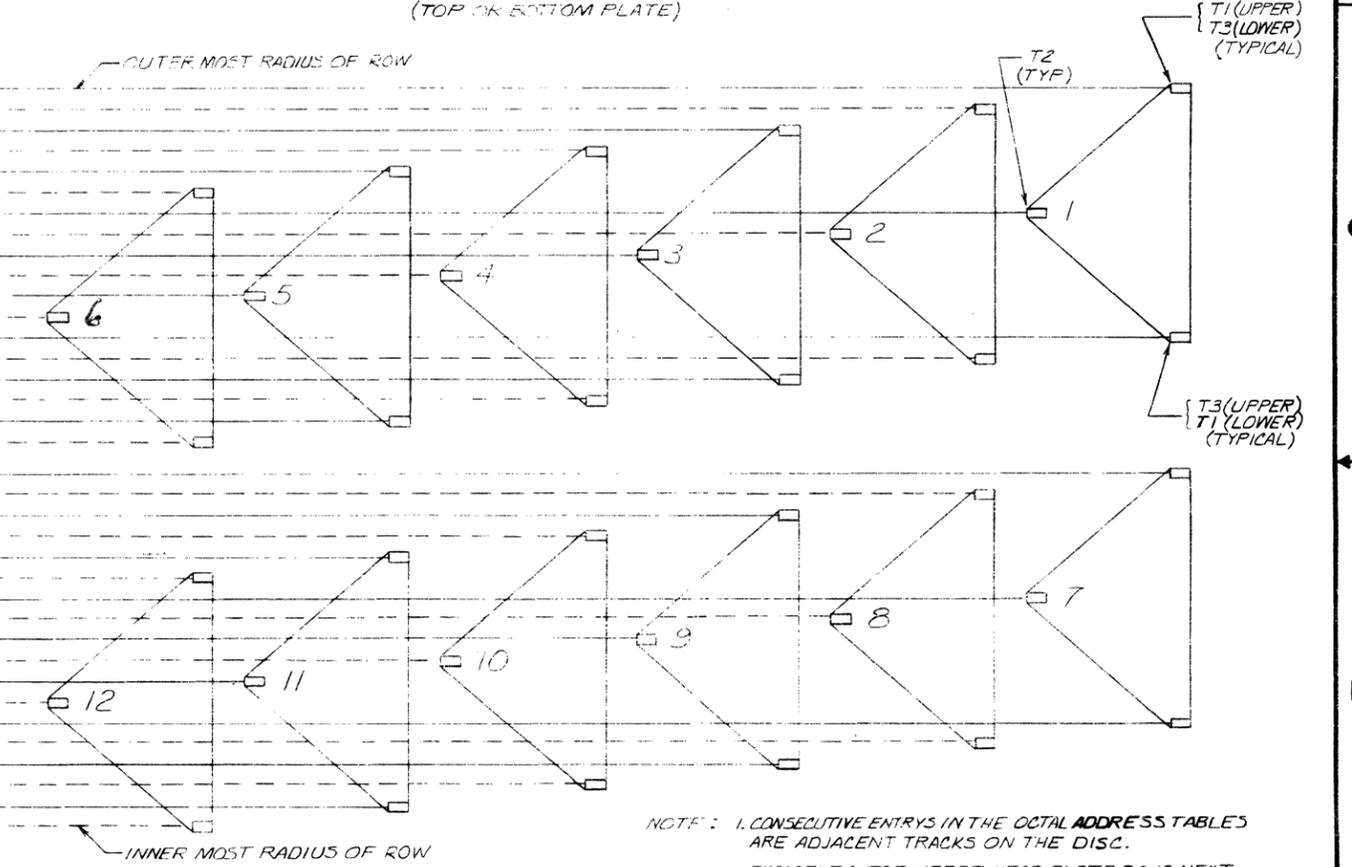
UPPER HEAD PLATE

LOWER HEAD PLATE

BRACKET & TRANSDUCER LOCATIONS WITHIN THE ROWS

(TOP OR BOTTOM PLATE)

UPPER HEAD PLATE								LOWER HEAD PLATE									
A ROW	B ROW	C ROW	D ROW	ADDRESS	A ROW	B ROW	C ROW	D ROW	ADDRESS	A ROW	B ROW	C ROW	D ROW	ADDRESS			
000	X0U	040	X2U	100	X4U	140	X6U	Y0U	200	X0L	240	X2L	300	X4L	340	X6L	Y0L
001		041		101		141		Y1U	201		241		301		341		Y1L
002		042		102		142		Y2U	202		242		302		342		Y2L
003		043		103		143		Y3U	203		243		303		343		Y3L
004		044		104		144		Y4U	204		244		304		344		Y4L
005		045		105		145		Y5U	205		245		305		345		Y5L
006		046		106		146		Y6U	206		246		306		346		Y6L
007		047		107		147		Y7U	207		247		307		347		Y7L
010		050		110		150		Y10U	210		250		310		350		Y10L
011		051		111		151		Y11U	211		251		311		351		Y11L
012		052		112		152		Y12U	212		252		312		352		Y12L
013		053		113		153		Y13U	213		253		313		353		Y13L
014		054		114		154		Y14U	214		254		314		354		Y14L
015		055		115		155		Y15U	215		255		315		355		Y15L
016		056		116		156		Y16U	216		256		316		356		Y16L
017		057		117		157		Y17U	217		257		317		357		Y17L
S1	X0U	S5	X2U	S9	X4U	S13	X6U	SY0U	S1	X0L	S5	X2L	S9	X4L	S13	X6L	SY0L
S2		S6		S10		S14		SY2U	S2		S6		S10		S14		SY2L
020	X1U	060	X3U	120	X5U	160	X7U	Y0U	220	X1L	260	X3L	320	X5L	360	X7L	Y0L
021		061		121		161		Y1U	221		261		321		361		Y1L
022		062		122		162		Y2U	222		262		322		362		Y2L
023		063		123		163		Y3U	223		263		323		363		Y3L
024		064		124		164		Y4U	224		264		324		364		Y4L
025		065		125		165		Y5U	225		265		325		365		Y5L
026		066		126		166		Y6U	226		266		326		366		Y6L
027		067		127		167		Y7U	227		267		327		367		Y7L
030		070		130		170		Y10U	230		270		330		370		Y10L
031		071		131		171		Y11U	231		271		331		371		Y11L
032		072		132		172		Y12U	232		272		332		372		Y12L
033		073		133		173		Y13U	233		273		333		373		Y13L
034		074		134		174		Y14U	234		274		334		374		Y14L
035		075		135		175		Y15U	235		275		335		375		Y15L
036		076		136		176		Y16U	236		276		336		376		Y16L
037		077		137		177		Y17U	237		277		337		377		Y17L
S3	X1U	S7	X3U	S11	X5U	S15	X7U	SY1U	S3	X1L	S7	X3L	S11	X5L	S15	X7L	SY1L
S4		S8		S12		S16		SY2U	S4		S8		S12		S16		SY2L

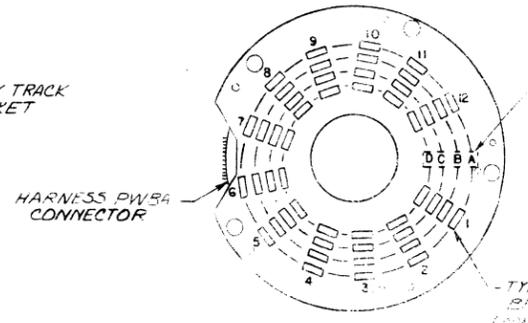
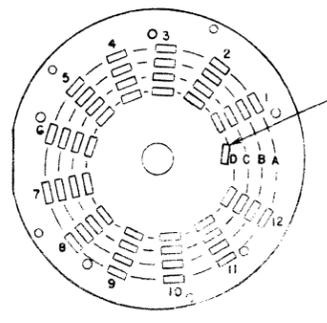


NOTE: 1. CONSECUTIVE ENTRIES IN THE OCTAL ADDRESS TABLES ARE ADJACENT TRACKS ON THE DISC.
EXAMPLE: FOR UPPER HEAD PLATE S4 IS NEXT TO S3 AND O40.

2. Y-Y ADDRESS NAMES USED IN THE OCTAL ADDRESS TABLES ARE ALSO THE LINE TITLES USED BETWEEN THE MEMORY PWBA AND THE HARNESS PWBA'S.

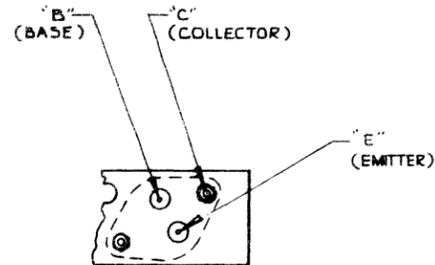
UPPER HEAD PLATE (HEAD BRACKET SIDE)

LOWER HEAD PLATE (HEAD BRACKET SIDE)

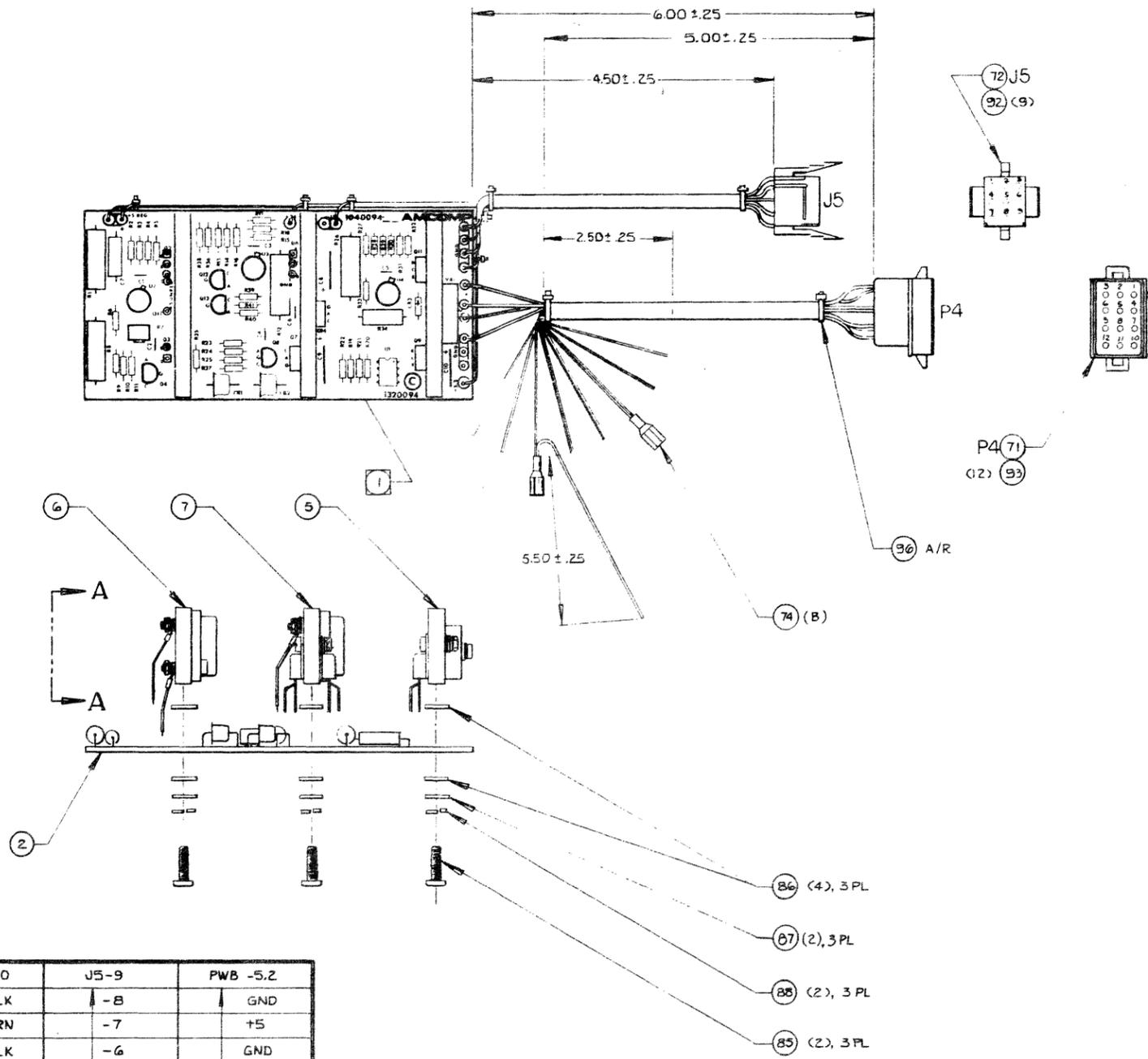


QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				
<p>NOTICE: THIS DWG SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF AMCOMP, INC. HOWEVER, IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUB-CONTRACT.</p>				
<p>UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS ANGLES</p>		<p>SIGNATURE DATE</p> <p>CHK. K. JACKSON 10-3-76</p> <p>APP. 11/10/76 11-3-76</p>		<p>AMCOMP SUNNYVALE, CALIFORNIA</p> <p>TITLE OCTAL ADDRESS DIAGRAM - 8500</p> <p>DRAWING NO. 1930008</p>
<p>8500 1020083</p> <p>3500 1020082</p> <p>USED ON NEXT ASSY.</p>		<p>FINISH</p> <p>SCALE NONE PROJ. NO. SHEET 1 OF 1</p>		

REVISIONS			
ZONE	LTR.	DESCRIPTION	DATE
A		RELEASE PER 8500-021	5/21/77



VIEW A-A
3 PL (Q2, Q3, Q6 REF)



NOTES:

- 1 IDENTIFY WITH ASSEMBLY PART NO. 1040094-01
4 CURRENT M/L REVISION LETTER PER 1550010.
2. MAXIMUM COMPONENT LEAD PROTRUSION ON
CIRCUIT SIDE OF BOARD SHALL BE .060
- 3 THIS INDICATES DOUBLE CRIMP WIRES.
- 4 WORKMANSHIP SHALL COMPLY WITH QA 100000-00.

84	ORN	Q3-C	PWB Q3-C/+5 UNREG
82	WHT	Q3-B	PWB Q3-B
82	WHT	Q3-E	PWB Q3-E
84	ORN	Q2-C	PWB Q2-C/+5 UNREG
82	WHT	Q2-B	PWB Q2-B
82	WHT	Q2-E	PWB Q2-E
76	BLK	P4-12	PWB GND
79	BLU	P4-11	PWB +
76	BLK	Q6-C	3 TERMINAL
76	BLK	P4-10	3 TERMINAL
77	RED	PWB -12	3 TERMINAL
77	RED	P4-9	3 TERMINAL
76	BLK	PWB GND	3 TERMINAL
76	BLK	P4-8	3 TERMINAL
78	ORN		3 TERMINAL
78	ORN	P4-7	3 TERMINAL
79	BLU	-6	PWB A.C.
79	BLU	-5	PWB A.C.
77	RED	-4	TERMINAL
77	RED	-3	TERMINAL
78	ORN	-2	TERMINAL
78	ORN	P4-1	TERMINAL

80	V10	J5-9	PWB -5.2
76	BLK	-8	GND
78	ORN	-7	+5
76	BLK	-6	GND
79	BLU	-5	+24
76	BLK	-4	GND
77	RED	-3	-12
76	BLK	-2	GND
78	ORN	J5-1	PWB +5
83	BLK	Q6-C	PWB Q6-C/-12 UNREG
82	WHT	Q6-B	PWB Q6-B
82	WHT	Q6-E	PWB Q6-E

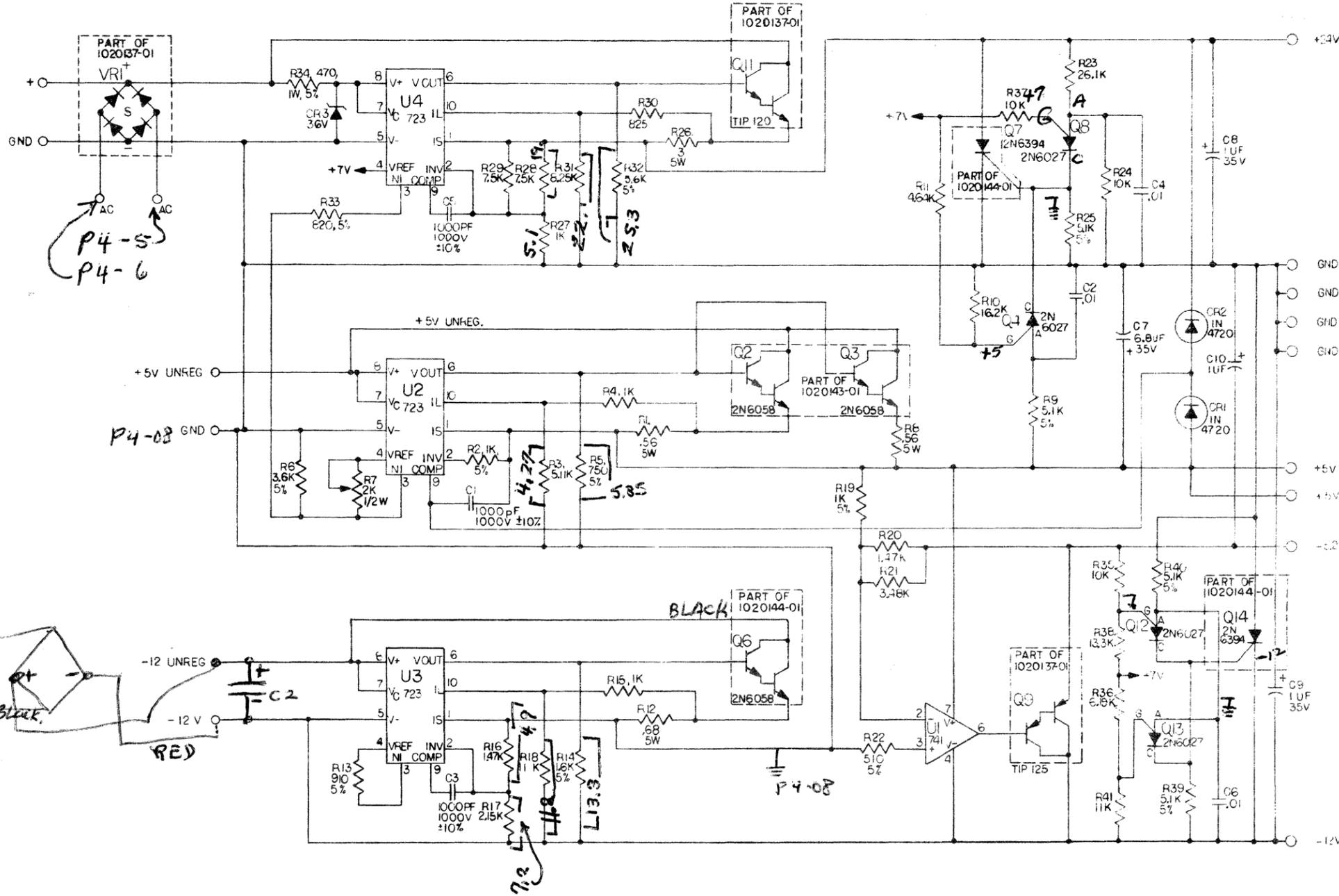
ITEM NO.	COLOR	COMP - PIN FROM	COMP TO	ITEM NO.	COLOR	COMP - PIN FROM	COMP TO
WIRE				WIRE LIST			

QTY REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				
NOTICE			UNLESS OTHERWISE SPECIFIED	
THIS DRAWING SHALL NOT BE			DIMENSIONS ARE IN INCHES	
DUPLICATED OR USED FOR			TOLERANCES ON	
ANY PURPOSE OTHER			DECIMALS	
THAN THAT FOR WHICH			ANGLES	
PROVIDED OR UNLESS			OTHERWISE	
INDICATED IN THIS DRAWING			SPECIFIED	
IN WHOLE OR IN PART			BY THE DRAWING	
WITHOUT WRITTEN			CONTRACT	
CONSENT OF AMCOMP, INC.			SPECIFIED TO BE GIVEN TO	
REPRODUCED OR TRANSMITTED			ANY MANNER	
IN ANY MANNER			WITHOUT THE WRITTEN	
CONSENT OF AMCOMP, INC.			CONTRACT	
REPRODUCED OR TRANSMITTED			IN ANY MANNER	
WITHOUT THE WRITTEN			CONSENT OF AMCOMP, INC.	
CONTRACT			REPRODUCED OR TRANSMITTED	
IN ANY MANNER			WITHOUT THE WRITTEN	
CONSENT OF AMCOMP, INC.			CONTRACT	

SIGNATURE	DATE
James A. Relator	4/21/77
Tom BATEMAN	5-4-77
	5-21-77

AMCOMP
SUNNYVALE, CALIFORNIA
TITLE
PWBA, POWER SUPPLY
SIZE
D
DRAWING NO.
1040094
SCALE
1/1
PROJ. NO.
1623-03
SHEET
1 OF 1

REVISIONS			
ZONE	LTR.	DESCRIPTION	DATE APPROVED
A		RELEASE PER B500-021	6/11/77 C-16



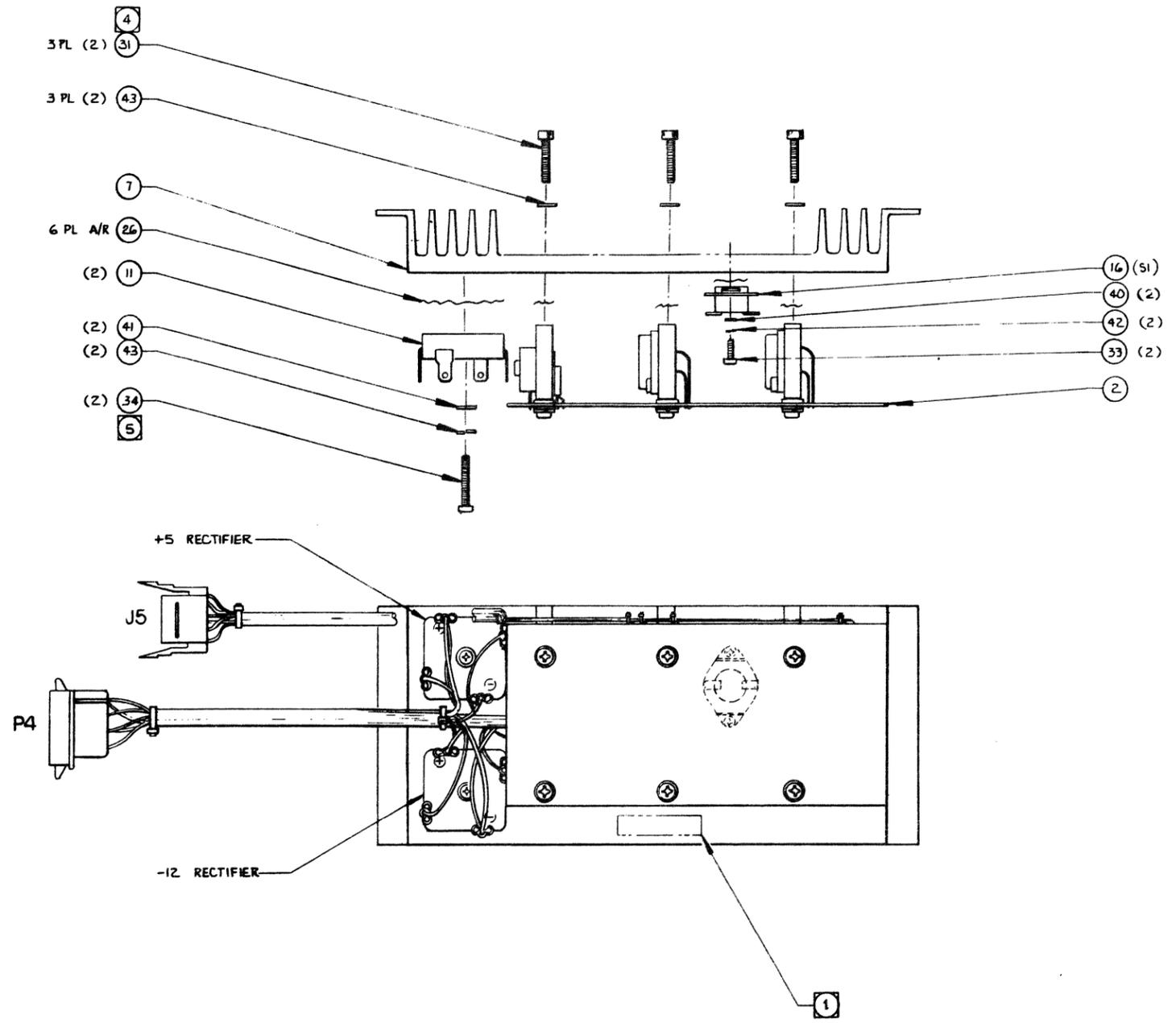
NOTES: UNLESS OTHERWISE SPECIFIED:
 1. ALL RESISTORS ARE IN OHMS, 1/4W, 1%
 2. ALL CAPACITORS ARE IN MICROFARADS, 25V.

REFERENCE DESIGNATIONS	
HIGHEST USED	NOT USED
C10	---
CR3	---
Q14	Q1, Q5, Q10
R41	---
U4	---
VR1	---

QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				
AMCOMP SUNNYVALE, CALIFORNIA				
TITLE SCHEMATIC, PWBA, POWER SUPPLY				
SIZE D		DRAWING NO. 1940094		REV A
SCALE: NONE PROJ. NO. 1623-03 SHEET 1 OF 1				

NOTICE	UNLESS OTHERWISE SPECIFIED	SIGNATURE	DATE
THIS DRAWING SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH IT WAS ORIGINALLY DESIGNED. ANY REPRODUCTION OR USE FOR OTHER PURPOSES WITHOUT THE WRITTEN CONSENT OF AMCOMP, INC. IS PROHIBITED. IF THIS DRAWING IS SPECIFIED TO BE SHOWN TO ANY MEMBER OF STAFF, THE USER SHALL BE RESPONSIBLE FOR OBTAINING THE NECESSARY PERMISSION FROM THE ISSUING OFFICE.	DIMENSIONS ARE IN INCHES DECIMALS ANGLES	<i>[Signature]</i>	3/15/77
		CHK R.W. BATEMAN	5-4-77
		APP [Signature]	5-4-77
		APP [Signature]	
	8500		
	USED ON	1040094-01	
	NEXT ASSY.		
	APPLICATION		

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
A		RELEASE PER 8500-021	5/24/77	RCS/ML
B		REVISED PER EO 51705	1/23/77	RCS/ML

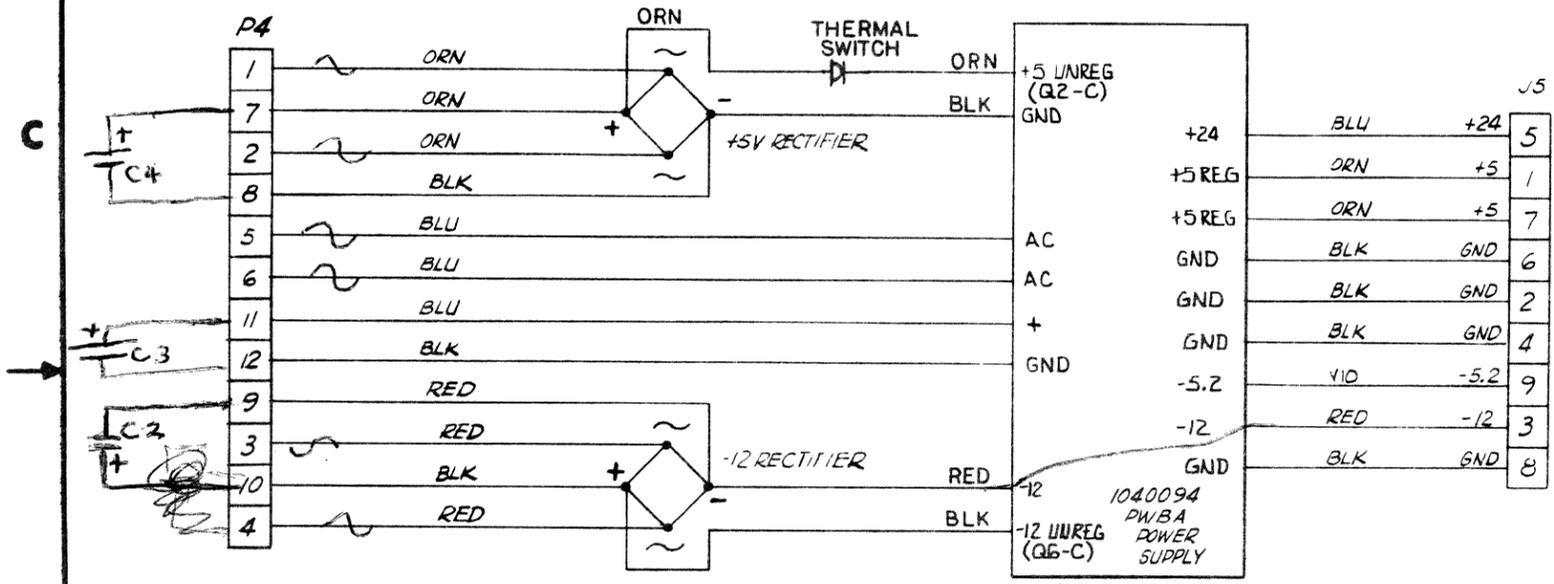


- NOTES:
- IDENTIFY WITH ASSEMBLY PART NO. 1020138-01 AND CURRENT M/L REVISION LETTER PER 1550010. APPROX WHERE SHOWN.
 - WORKMANSHIP SHALL COMPLY WITH QA 100000-00
 - FOR WIRING DIAGRAM SEE 1930032.
 - TORQUE TO 18 IN-LBS MIN.
 - TORQUE TO 15 IN-LBS MAX.

ORN	SI	PWBA +5 UNREG
BLK	PWBA G6-C	-12 RECTIFIER +
BLK	P4-10	-12 RECTIFIER -
RED	PWBA -12	-12 RECTIFIER -
RED	P4-9	-12 RECTIFIER -
BLK	PWBA GND	+5 RECTIFIER -
BLK	P4-8	+5 RECTIFIER -
ORN	SI	+5 RECTIFIER +
ORN	P4-7	+5 RECTIFIER +
RED	P4-4	-12 RECTIFIER ~
RED	P4-3	-12 RECTIFIER ~
ORN	P4-2	+5 RECTIFIER ~
ORN	P4-1	+5 RECTIFIER ~
WIRE COLOR	COMP/PIN FROM	COMP/PIN TO
WIRE LIST		

QTY REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL																																							
LIST OF MATERIAL																																											
<table border="1"> <tr> <td rowspan="4"> NOTICE THIS DWG SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF AMCOMP, INC. HOWEVER, IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUB-CONTRACT. </td> <td>UNLESS OTHERWISE SPECIFIED</td> <td>SIGNATURE</td> <td>DATE</td> <td rowspan="4"> AMCOMP SUNNYVALE, CALIFORNIA TITLE HEATSINK ASSEMBLY DRAWING NO. 1020138 SCALE 1/1 PROJ. NO. 1623-03 SHEET 1 OF 1 </td> </tr> <tr> <td>DIMENSIONS ARE IN INCHES</td> <td>DFP</td> <td>9/25/77</td> </tr> <tr> <td>TOLERANCES ON DECIMALS</td> <td>CHK</td> <td>5-4-77</td> </tr> <tr> <td>ANGLES</td> <td>APR</td> <td>5-4-77</td> </tr> <tr> <td colspan="2">MATERIAL</td> <td colspan="2">APPROVED</td> <td></td> </tr> <tr> <td colspan="2">FINISH</td> <td colspan="2">APPROVED</td> <td></td> </tr> <tr> <td colspan="2">APPLICATION</td> <td colspan="2">APPROVED</td> <td></td> </tr> <tr> <td>8500</td> <td>1020059</td> <td colspan="2"></td> <td></td> </tr> <tr> <td>USED ON</td> <td>NEXT ASSY.</td> <td colspan="2"></td> <td></td> </tr> </table>					NOTICE THIS DWG SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF AMCOMP, INC. HOWEVER, IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUB-CONTRACT.	UNLESS OTHERWISE SPECIFIED	SIGNATURE	DATE	AMCOMP SUNNYVALE, CALIFORNIA TITLE HEATSINK ASSEMBLY DRAWING NO. 1020138 SCALE 1/1 PROJ. NO. 1623-03 SHEET 1 OF 1	DIMENSIONS ARE IN INCHES	DFP	9/25/77	TOLERANCES ON DECIMALS	CHK	5-4-77	ANGLES	APR	5-4-77	MATERIAL		APPROVED			FINISH		APPROVED			APPLICATION		APPROVED			8500	1020059				USED ON	NEXT ASSY.			
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	DIMENSIONS ARE IN INCHES	DFP	9/25/77																																								
	TOLERANCES ON DECIMALS	CHK	5-4-77																																								
	ANGLES	APR	5-4-77																																								
MATERIAL		APPROVED																																									
FINISH		APPROVED																																									
APPLICATION		APPROVED																																									
8500	1020059																																										
USED ON	NEXT ASSY.																																										

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
A		RELEASE PER 8500-021	5/21/77	RCS/AB



NOTES:
 1. FOR POWER SUPPLY PW/BA SCHEMATIC SEE 1940094.

QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				

NOTICE
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UNLESS OTHERWISE SPECIFIED	SIGNATURE	DATE
DIMENSIONS ARE IN INCHES	DFT. <i>[Signature]</i>	3-1-77
TOLERANCES ON ANGLES	CHK. <i>[Signature]</i>	5-4-77
DECIMALS	APP. <i>[Signature]</i>	5-4-77
XXX±	APP.	
XXX±		
8500	1020138	
USED ON	NEXT ASSY.	
APPLICATION		

MATERIAL		DATE	
FINISH		DATE	

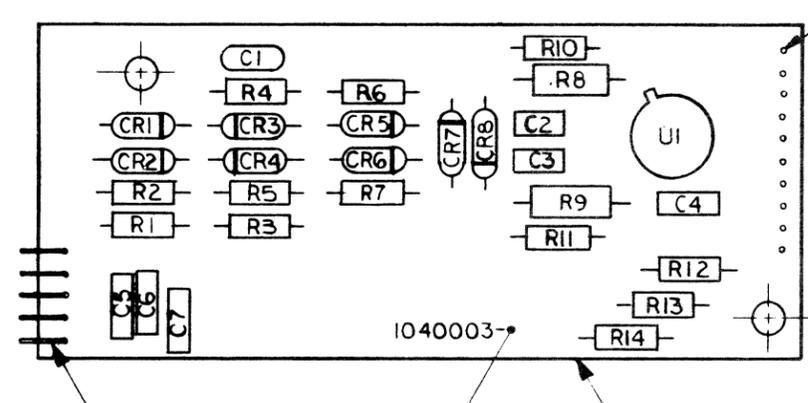
AMCOMP
 SUNNYVALE, CALIFORNIA

TITLE
**WIRING DIAGRAM
 HEATSINK ASSEMBLY**

SIZE **C** DRAWING NO. **1930032** REV **A**

SCALE — PROJ. NO. 1623-03 SHEET / OF /

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	D	REVISED & REDRAWN PER EO 8346	3/9/76	<i>[Signature]</i>
	E	SEE EO 8355	EAL 7/1/76	<i>[Signature]</i>



5. WIRE HOLES TO BE OPEN AND FREE OF SOLDER AFTER COMPONENT ASSY & SOLDERING.
4. MAXIMUM ALLOWABLE COMPONENT HEIGHT SHALL BE .280.
3. FOR SCHEMATIC SEE DRAWING NO. 1940015, SHT 5.
2. MAXIMUM COMPONENT LEAD PROTRUSION ON CIRCUIT SIDE OF BOARD SHALL BE .060.
1. IDENTIFY WITH PROPER ASSY PART NO. AND M/L REV.

NOTES:

QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				

NOTICE <small>THIS DRAWING SHALL NOT BE REPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR ENCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF DATA DISC, INC. HOWEVER, IF THIS DRAWING IS SPECIFIED TO BE GIVEN TO ANY AGENCY OF GOVERNMENT THIS DRAWING MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUB-CONTRACT.</small>		<small>UNLESS OTHERWISE SPECIFIED</small> <small>DIMENSIONS ARE IN INCHES</small> <small>TOLERANCES ON</small> <small>DECIMALS</small> <small>XX=.2</small> <small>XXX=.1</small>	<small>SIGNATURE</small> <small>DFT</small> <i>[Signature]</i> <small>CHK.</small> <i>[Signature]</i> <small>APP.</small> <i>[Signature]</i> <small>APP.</small> <i>[Signature]</i>	<small>DATE</small> <small>7/2/76</small> <small>3/9/76</small> <small>3/9/76</small>
	8500	1040050		
	8400	1040056		
	USED ON	NEXT ASSY.		

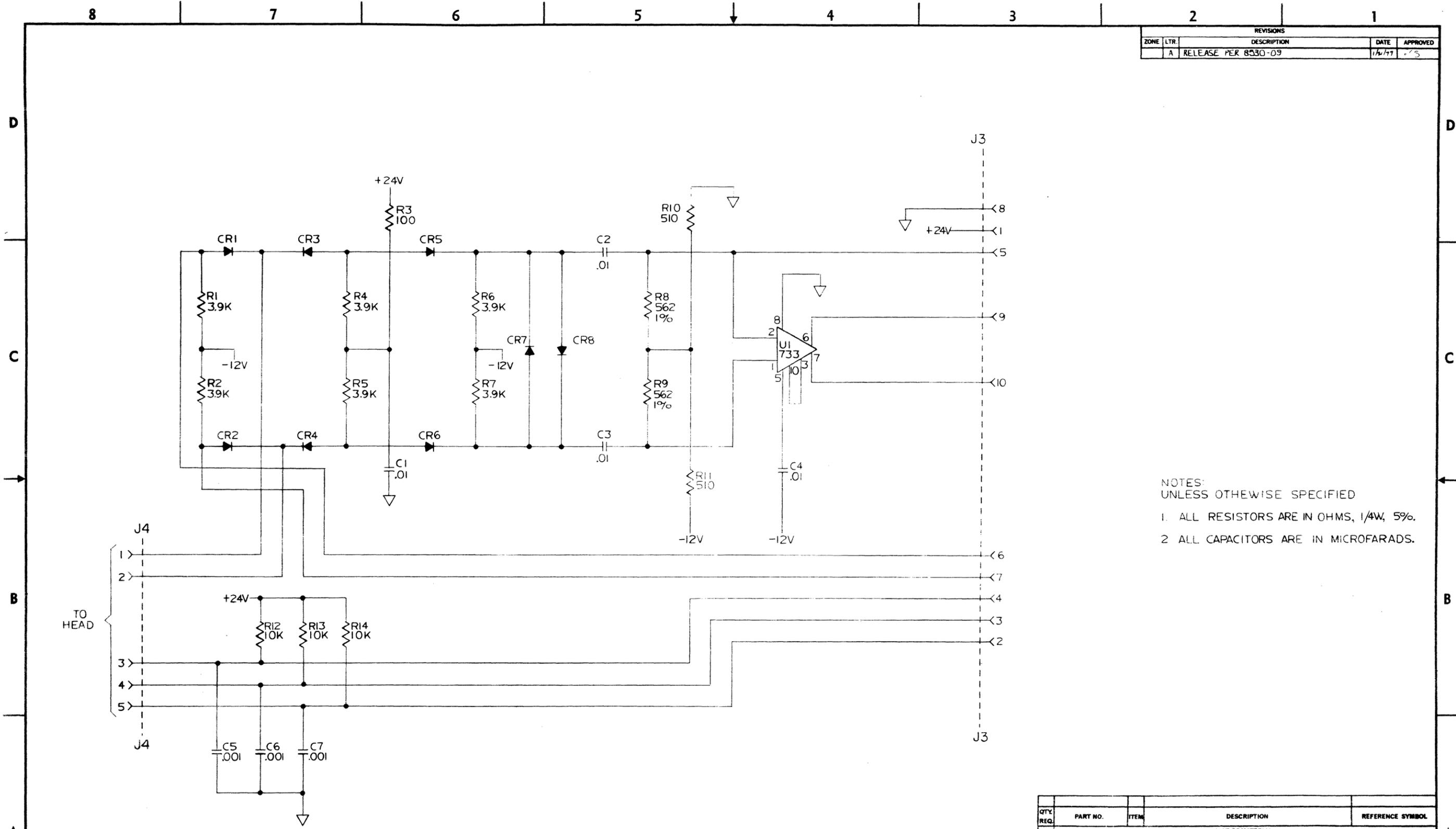
DATA DISC
INCORPORATED

TITLE
PWBA CLOCK PREAMP

SIZE **C** DRAWING NO. **1040003** REV **E**

SCALE **2/1** PROJ. NO. SHEET **1** OF **1**

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
A		RELEASE PER 8530-09	1/6/77	CS



- NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
 2. ALL CAPACITORS ARE IN MICROFARADS.

QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL																							
LIST OF MATERIAL																											
<table border="1"> <tr> <td>NOTICE</td> <td>UNLESS OTHERWISE SPECIFIED</td> <td>SIGNATURE</td> <td>DATE</td> <td rowspan="2"> AMCOMP SUNNYVALE, CALIFORNIA TITLE SCHEMATIC CLOCK PREAMP </td> </tr> <tr> <td>THIS DRAWING SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF AMCOMP, INC. HOWEVER, IF THIS DRAWING IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DRAWING MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUB-CONTRACT.</td> <td>DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS FRACTIONS ANGLES</td> <td>D.T. James A. Blanton</td> <td>1/15/77</td> </tr> <tr> <td colspan="2">APPLICATION</td> <td>FINISH</td> <td>SCALE</td> <td> <table border="1"> <tr> <td>SIZE</td> <td>DRAWING NO.</td> <td>REV.</td> </tr> <tr> <td>D</td> <td>1940003</td> <td>A</td> </tr> <tr> <td>SCALE</td> <td>PROJ. NO.</td> <td>SHEET 1 OF 1</td> </tr> </table> </td> </tr> </table>					NOTICE	UNLESS OTHERWISE SPECIFIED	SIGNATURE	DATE	AMCOMP SUNNYVALE, CALIFORNIA TITLE SCHEMATIC CLOCK PREAMP	THIS DRAWING SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF AMCOMP, INC. HOWEVER, IF THIS DRAWING IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DRAWING MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUB-CONTRACT.	DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS FRACTIONS ANGLES	D.T. James A. Blanton	1/15/77	APPLICATION		FINISH	SCALE	<table border="1"> <tr> <td>SIZE</td> <td>DRAWING NO.</td> <td>REV.</td> </tr> <tr> <td>D</td> <td>1940003</td> <td>A</td> </tr> <tr> <td>SCALE</td> <td>PROJ. NO.</td> <td>SHEET 1 OF 1</td> </tr> </table>	SIZE	DRAWING NO.	REV.	D	1940003	A	SCALE	PROJ. NO.	SHEET 1 OF 1
NOTICE	UNLESS OTHERWISE SPECIFIED	SIGNATURE	DATE	AMCOMP SUNNYVALE, CALIFORNIA TITLE SCHEMATIC CLOCK PREAMP																							
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APPLICATION		FINISH	SCALE	<table border="1"> <tr> <td>SIZE</td> <td>DRAWING NO.</td> <td>REV.</td> </tr> <tr> <td>D</td> <td>1940003</td> <td>A</td> </tr> <tr> <td>SCALE</td> <td>PROJ. NO.</td> <td>SHEET 1 OF 1</td> </tr> </table>	SIZE	DRAWING NO.	REV.	D	1940003	A	SCALE	PROJ. NO.	SHEET 1 OF 1														
SIZE	DRAWING NO.	REV.																									
D	1940003	A																									
SCALE	PROJ. NO.	SHEET 1 OF 1																									

4

3

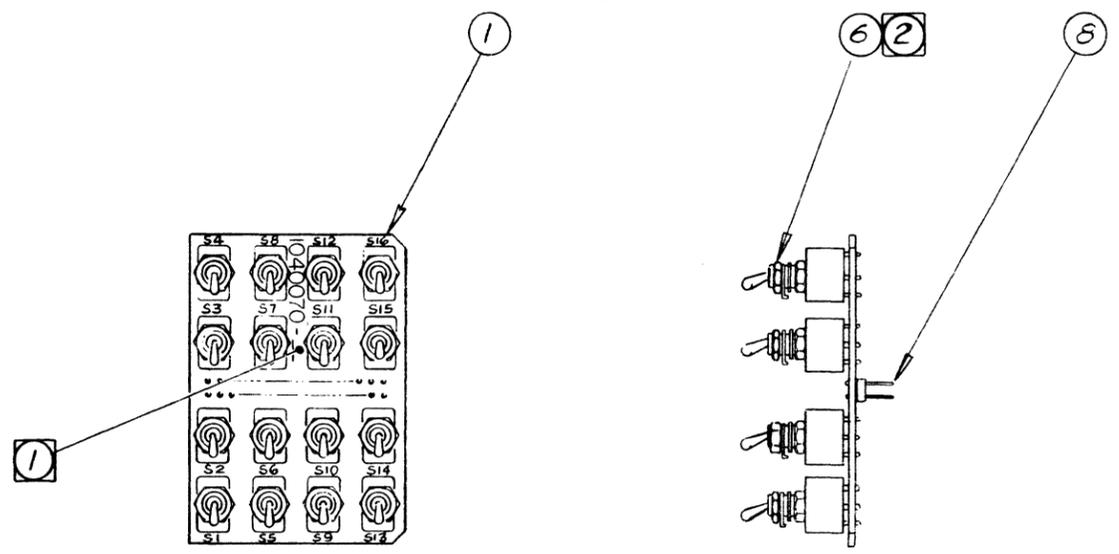
2

1

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	A	PRE-PRODUCTION RELEASE/8500-09	8/3/76	W.R.
	B	RELEASE PER 8530-01	3/16/77	RC

D
C
B
A

D
C
B
A



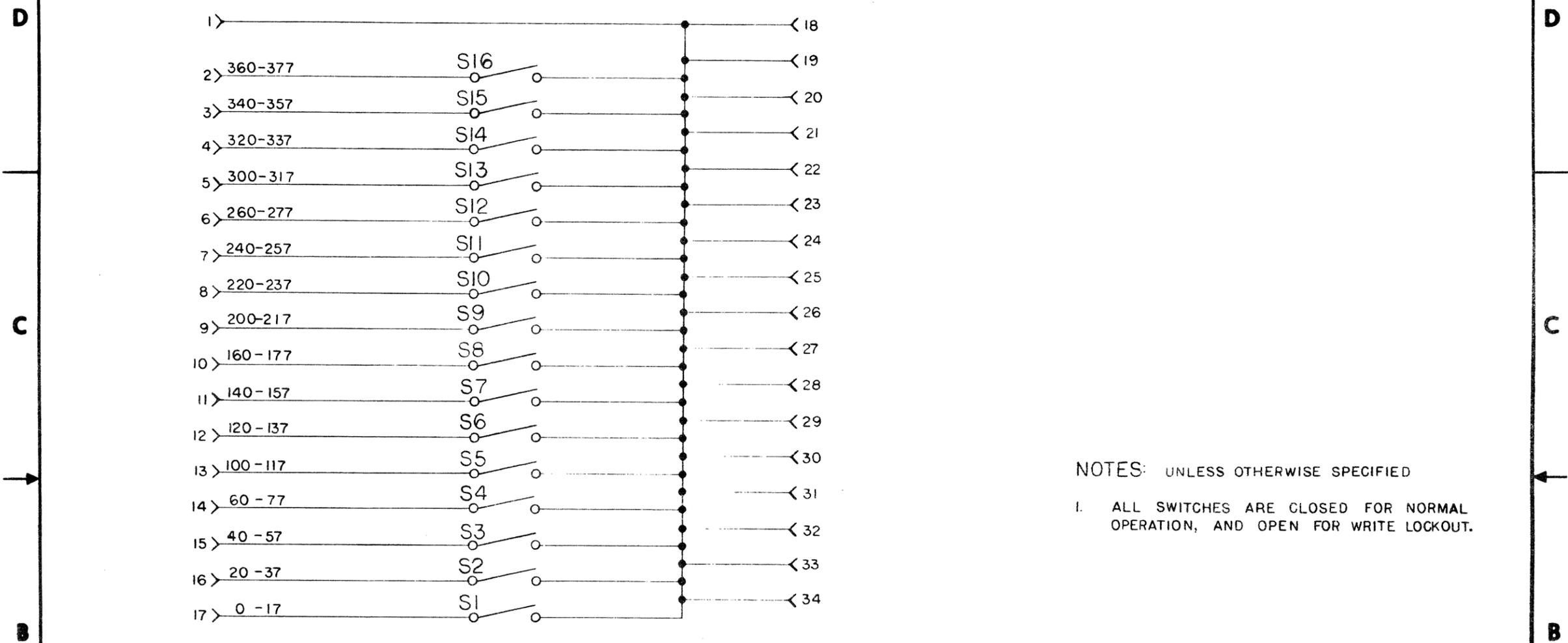
- NOTES:
- ② DO NOT DISCARD MOUNTING HARDWARE SUPPLIED WITH SWITCHES.
 - ① IDENTIFY WITH PROPER ASSEMBLY DASH N^o & M/L REVISION.

FOR COMPLETE LIST OF MATERIALS SEE 1040070-01

NOTICE		UNLESS OTHERWISE SPECIFIED		SIGNATURE		DATE		DATA DISC INCORPORATED	
THIS DWG SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF DATA DISC, INC. HOWEVER, IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUB-CONTRACT.		DIMENSIONS ARE IN INCHES		DFT. <i>Jakan</i>		7-21-76		TITLE PWB ASSEMBLY WRITE-LOCKOUT DRAWING NO. 1040070 SCALE 1:1 PROJ. NO. 1522 SHEET 1 OF 1	
		TOLERANCES ON DECIMALS ANGLES		CHK. <i>W. Ross</i>		7-22-76			
		MATERIAL		APP. <i>[Signature]</i>		7-22-76			
		FINISH		APP. <i>[Signature]</i>					
APPLICATION		USED ON 8500 NEXT ASSY. 1020104-02							

4 | 3 | 2 | 1

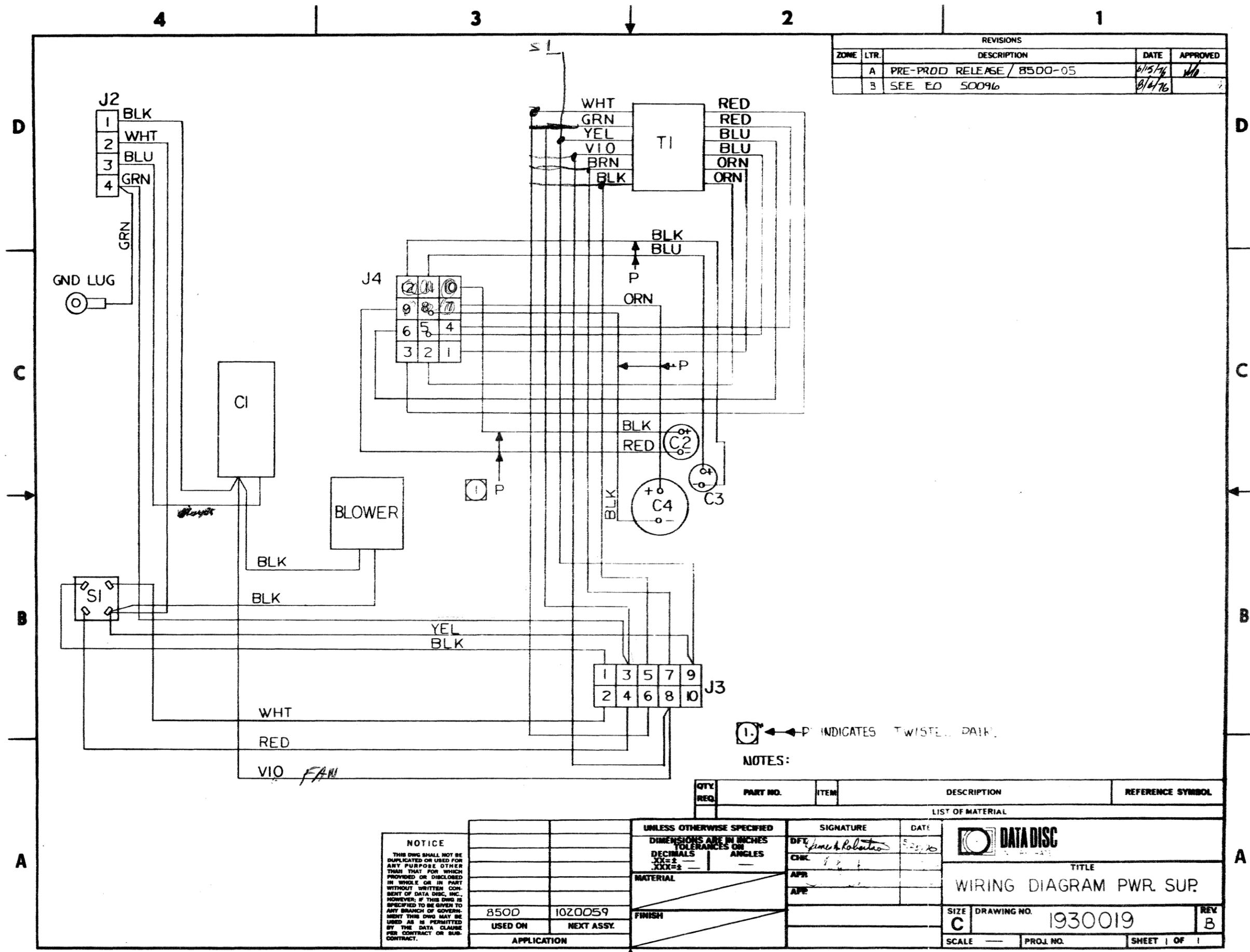
REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	A	RELEASE PER 8500-022	4/30/77	<i>[Signature]</i>



NOTES: UNLESS OTHERWISE SPECIFIED
 1. ALL SWITCHES ARE CLOSED FOR NORMAL OPERATION, AND OPEN FOR WRITE LOCKOUT.

QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL
LIST OF MATERIAL				

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	8500	1040070	FINISH				SIZE C
	USED ON	NEXT ASSY.					DRAWING NO. 1940070
	APPLICATION						SCALE PROJ. NO. 1614-00 SHEET 1 OF 1



REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
A		PRE-PROD RELEASE / 8500-05	6/15/76	[Signature]
B		SEE ED 50096	8/4/76	[Signature]

NOTES:
 (1) ← P INDICATES TWISTED PAIR.

NOTICE
 THIS DWG SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF DATA DISC, INC. HOWEVER, IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUB-CONTRACT.

8500	1020059
USED ON	NEXT ASSY.
APPLICATION	

UNLESS OTHERWISE SPECIFIED	
DIMENSIONS ARE IN INCHES	TOLERANCES ON ANGLES
DECIMALS	XXX=
MATERIAL	
FINISH	

SIGNATURE	DATE
DFY [Signature]	5-25-76
CHK [Signature]	
APR [Signature]	
APP [Signature]	

LIST OF MATERIAL	
DATA DISC	
TITLE	
WIRING DIAGRAM PWR. SUP.	
SIZE	DRAWING NO.
C	1930019
SCALE	PROJ. NO.
	SHEET 1 OF 1