

Amdahl 580 Systems

MANAGEMENT SUMMARY

Less than a week after IBM's introduction of its large-scale 3081 processor and entry-level 3033, the Model Group S, Amdahl Corporation announced a new family of large-scale processors, the 580 Series, and an entry level model to its 470V/7 product line, the 470V/7C. The new systems offer price/performance improvements over their IBM counterparts while maintaining Amdahl's high technology standards.

Amdahl's most powerful uniprocessor, the 580 Model 5860, was introduced on November 18, 1980. Like the 470 family of processors, it is fully compatible with the IBM System/370 instruction set as well as the entire 470 product line. It represents a large-scale growth path for existing Amdahl 470 users. Also announced was a tightly-coupled dual processor version of the 580, the Model 5880. An Amdahl spokesman told Datapro the 5880 differs very little from a pair of single-processor 5860s, and the 5860 can be field upgraded to the 5880.

The Model 5860 has twice the performance of Amdahl's former top-end system, the 470V/8, giving it an execution speed of approximately 13 MIPS (million instructions per second). The dual-processor Model 5880 is rated at about 22 MIPS, or about 3.5 times as powerful as the 470V/8. IBM's 3081, a dual-processor system in its basic configuration, is rated at about 10 MIPS. The new systems have 16 megabytes of main memory, expandable to 32 megabytes in 4-megabyte increments. Both systems are equipped with 16 block multiplexer channels per processor with an option for an additional 16 block multiplexer channels per processor. The block multi- ➤

Amdahl's new 580 Series of plug-compatible mainframes includes two models, the single-processor 5860, and the dual-processor 5880. Both systems have from 16 to 32 MB of memory, up to 32 block multiplexer channels on the 5860, 64 on the 5880, and range in price from \$3.8 million for a basic 5860 up to about \$7.5 million for a fully-configured 5880.

CHARACTERISTICS

MANUFACTURER: Amdahl Corporation, 1250 East Arques Avenue, Sunnyvale, California 94086, Telephone (408)746-6000.

MODELS: Amdahl 5860 (single processor), 5880 (dual processor)

DATE ANNOUNCED: November 18, 1980

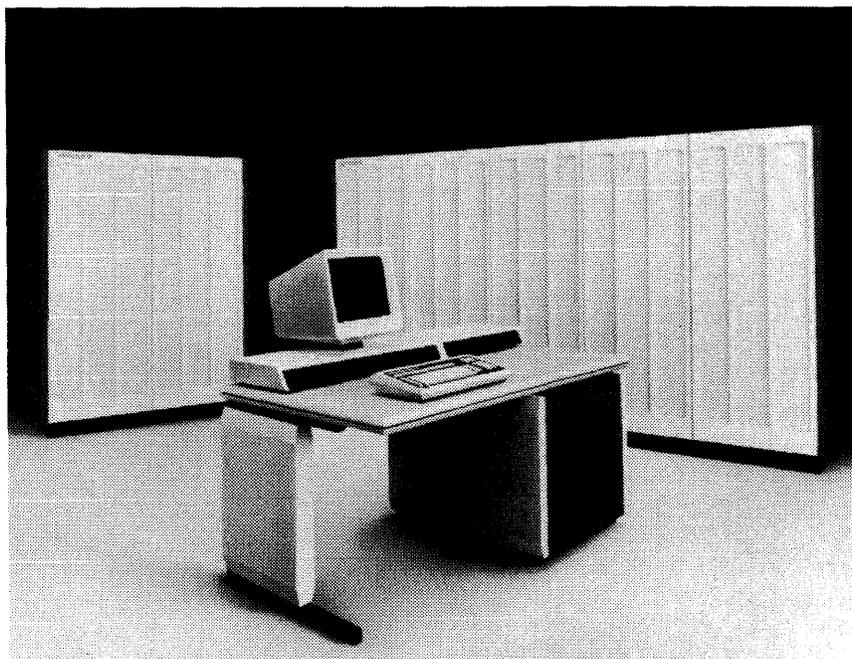
DATE OF FIRST DELIVERY: Model 5860, April 1982; Model 5880, 2nd quarter 1983

DATA FORMATS

All data formats, instruction formats, and other architectural features completely follow IBM System/370 architecture.

BASIC UNIT: 8-bit bytes. Each byte can represent 1 alphanumeric character, 2 BCD digits, or 8 binary bits. Two consecutive bytes form a "halfword" of 16 bits, while 4 consecutive bytes form a 32-bit "word."

FIXED-POINT OPERANDS: Can range from 1 to 16 bytes (1 to 31 digits plus sign) in decimal mode; 1 halfword (16 bits) or 1 word (32 bits) in binary mode. ➤



The Amdahl 580 Series of high-performance mainframes includes the single-processor 5860, shown here, with twice the power of Amdahl's 470V/8, and the dual-processor 5880, with 3.5 times the 470V 8's performance. The systems have from 16 to 32 megabytes of main memory, 18 to 34 channels per CPU, and improved price/performance over the IBM 3081.

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► plexer channels can also be configured as byte multiplexer or selector channels. Two byte multiplexer channels are provided on the 5860, and four byte multiplexer channels are provided on the 5880.

A basic 5860 with 16 megabytes of memory and 16 channels costs \$3,800,000, compared to a similarly equipped IBM 3081, which costs \$3,720,000. In terms of price per MIP the picture changes quite a bit. Using the previous performance estimates, the 5860 costs about \$292,000 per MIP, and the 3081 costs about \$372,000 per MIP, a sizeable difference. The cost per megabyte of memory is the same in both systems—\$25,000.

PROCESSORS AND PERIPHERALS

The performance increases of the 580 are made possible through improvements in system design, technology, and packaging, according to Amdahl. The processor incorporates a five-phase pipeline design which reduces the number of machine cycles per instruction. This technique produces a maximum execution rate of one instruction per cycle. The 470 systems, for comparison, execute one instruction per two cycles. The processor cycle time in the 580 is 24 nanoseconds. The memory cycle time is 280 nanoseconds. Data paths are eight bytes wide, compared to four bytes in the 470, and the 580 uses a dual-bus structure to interconnect all functional units. Two 32K high-speed buffers (HSB), using the 470 "non-store-through" technique, permit data to be modified in the buffer rather than in main storage. One HSB is used for rapid access to instructions and the other HSB is for fast access to data—a method Amdahl says reduces the interference between the instruction fetching and execution activities.

The system's block multiplexer channels all support the data streaming feature, and can transmit data at up to six megabytes per second. The initial Input/Output Processor (IOP), with 16 block multiplexer channels, has a maximum aggregate data rate of 50 megabytes per second. Higher data rates can be obtained by adding a second IOP. Up to 256 subchannels are available on every channel, and subchannel queuing is provided in high I/O contention situations. The two byte multiplexer channels are implemented in the 580 Console Complex, and have a 200 bytes-per-second data rate each.

Extensive use of LSI technology and component packaging contributes to the system's overall performance. The 580 systems, like the 470, are all air cooled. The LSI chips used in the 580 have a higher density than those in the 470, but generate about the same heat. High-speed 4K RAM modules are used for microcode control stores, registers, and HSBs. These RAMs, plus the LSI chips, are intermixed on 14-layer Multiple Chip Carriers (MCC) that can implement an entire system function. Up to 121 LSI chips and RAM modules can be mounted on each MCC. Only eight MCCs are needed for a basic 580, including five for the CPU, and one each for the IOP, Console Processor, and Memory Bus Controller (MBC). A ninth MCC is required when increasing the channels from 18 to the maximum 34. Up to 13 MCCs can be ►

► **FLOATING-POINT OPERANDS:** 1 word, consisting of 24-bit fraction and 7-bit hexadecimal exponent, in "short" format; 2 words, consisting of 56-bit fraction and 7-bit hexadecimal exponent, in "long" format; for 4 words in "extended precision" format.

INSTRUCTIONS: 2, 4, or 6 bytes in length, which usually specify 0, 1, or 2 memory addresses respectively.

INTERNAL CODE: EBCDIC (Extended Binary-Coded Decimal Interchange Code).

SYSTEM CONFIGURATION

The Amdahl 580 is built from several interrelated components. Each element is implemented in a Multiple Chip Carrier (MCC), which contains all logic and circuitry required, in a compact package. All functions are housed within the 580 mainframe, and include the following:

- **Instruction Unit (I-Unit),** which processes instructions and controls the CPU
- **Execution Unit (E-Unit),** which performs the required computations
- **Storage Unit (S-Unit),** which manages the system's operand storage and retrieval activities
- **Instruction Buffer (I-Buffer),** that provides high-speed buffer storage for instruction streams
- **Operand Buffer (O-Buffer),** that provides similar storage capabilities for operand data

These components make up the Central Processor (CPU). Additional 580 elements include:

- **Input/Output Processor (IOP),** which manages I/O requests and provides up to 16 block multiplexer channels, each of which can transfer data at up to 6 megabytes per second
- **Console Processor,** which monitors CPU functions, provides maintenance and diagnostic routines, and includes up to two byte multiplexer channels
- **Memory Bus Controller (MBC),** which controls data accesses to the Main Storage Unit (MSU), data bus transfers, and provides overall system coordination and timing facilities

A second IOP can be configured giving the 580 a maximum of 32 block multiplexer channels.

The 580 comes in the 5860, a uniprocessor, and the 5880, a tightly-coupled dual-processor configuration that Amdahl states is very similar to the 5860. Both systems have a maximum of 32 megabytes of memory, and the 5860 is field-upgradeable to the 5880. Memory and channels are shared by the two processors in the 5880. The 5860 is rated at twice the performance of the Amdahl 470V/8, and the 5880 is rated at 3.5 times the 470V/8.

TECHNOLOGY

As in the 470 series of processors, the 580 makes extensive use of large-scale integration (LSI) chips using high-performance emitter-coupled logic (ECL) circuitry. Up to 400 of these circuits can be contained on a single LSI chip, compared to only 100 circuits per chip on the 470. In spite of its obvious increased packing density, a 580 chip generates only slightly more heat than a 470 chip. The 580, like the 470, is air cooled. ►

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AMDAHL 580 PERFORMANCE COMPARISON

	470V/8	5860	5880	IBM 3081
SYSTEM CHARACTERISTICS				
Relative performance to 470V/8	1.0	2.0	3.5	1.5
Date announced	10/78	11/80	11/80	11/80
Date of first delivery	9/79	4/82	2nd qtr. 1983	4th qtr. 1981
Production status	Active	Active	Active	Active
Number of processors	1	1	2	2
Principal operating systems	MVS/SP, VM/370, VM/SP, ACP	MVS/SP, VM/SP, ACP 5880	MVS/SP, VM/SP	MVS/SP, VM/SP
Field upgradeable to	—	—	—	—
Basic system price (16MB)	\$2,775,000	\$3,800,000	\$7,500,000 (32MB)	\$3,720,000
PROCESSOR				
Cycle time, nanoseconds	26	24	24	26
BUFFER STORAGE				
Type	Bipolar RAM	Bipolar RAM	Bipolar RAM	Bipolar RAM
Cycle time, nanoseconds	52	N/A	N/A	N/A
Bytes, fetched per cycle	4	8	8	8
Capacity, bytes	64K	2 x 32K	4 x 32K	2 x 32K
MAIN STORAGE				
Type	Dynamic NMOS	Dynamic NMOS	Dynamic NMOS	MOS
Cycle time, nanoseconds	320	280	280	312
Parity checking	yes	yes	yes	yes
Error checking and correction	yes	yes	yes	yes
Bytes fetched per cycle	4	8	8	8
Minimum capacity, bytes	4M	16M	16M	16M
Maximum capacity, bytes	16M	32M	32M	32M
Memory increment size, bytes	4M	8M	8M	8M
I/O CHANNELS				
Block (optionally byte) multiplexer, std.	12	16	16	4
Block multiplexer only, std.	0	0	0	12
Byte multiplexer, standard	0	2	4	0
Block (optionally byte) multiplexer, optional	20	16	16	8
Maximum channel data rates				
Block multiplexer, bytes per second	3M	6M	6M	3M
Byte multiplexer, bytes per second	110K	200K	200K	40-75K
Aggregate data rate, bytes per second	18M	50-80M	50-80M	72M
Channel-to-channel adapter	yes	yes	yes	yes
Data Streaming	yes	yes	yes	yes

➤ accommodated in the LSI "stack," a 5.6 cubic foot enclosure with its two side walls made up of printed circuit boards for interconnecting the MCCs. The 580 employs a dual-bus design with eight-byte data paths. The A-Bus carries data from the console, IOP, and CPU to the MBC, which manages the system's memory activities. The B-Bus returns data to these three components from the MBC.

System compatibility is a key element of the Amdahl 580. To provide increased flexibility in this important area, the 580 uses Distributed Microcode on its Instruction Unit (I-Unit), Execution Unit (E-Unit), IOP, MBC, and the console. Amdahl claims this approach results in shorter control paths and reduced contention. The microcode control store, typically centralized, is now distributed to the same MCC as the functional unit it controls. The performance of each functional unit can then be customized for optimum performance. Another factor, I/O protocol compatibility, is reduced to a single PCB, the Channel Interface Handler. Modifications to accommodate protocol changes are made simply by updating the Channel Interface Handler. A new hardware/firmware product called Macrocode supports ➤

➤ A new high-speed 4K RAM module was developed by Amdahl to handle such functions as Distributed Microcode control storage, high-speed buffer (HSB) storage, and system registers.

Amdahl combines up to 121 RAM and logic chips on a Multiple Chip Carrier (MCC). This increased packing density, with almost three times the number of chips per MCC as the 470, permits the implementation of an entire system function on a single MCC. Each system MCC is arranged in a small (only about 5.6 cubic feet) stack with a maximum of 13 MCCs possible. Each of the two stack side walls incorporates a 12-layer printed circuit board for MCC-to-MCC interconnections. A minimum of 8 MCCs is required for a basic 580 system. Compared to the 470, with as many as 59 MCCs required, the 580 provides more internal data paths and increased reliability.

Tying all functional units together are two data buses, the A-Bus and B-Bus. Each bus moves unidirectionally, and has a 72-bits-wide data path. The two buses are integral parts of the stack side walls, and provide shorter data paths, simplified physical connections, and a reduction in the number of connections required among functional units. The A-Bus transports data from the Console, I/O Processor (IOP), and CPU to the Memory Bus Controller (MBC). The B-Bus returns data to these units from the MBC. ➤

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➤ the machine check and channel check capabilities of the 580. Amdahl indicated that Macrocode will play an important role in implementing future system compatibility techniques.

System reliability, availability, and serviceability are performed via several methods: 1) advanced error-checking and correction (ECC) circuitry, such as main memory ECC, buffer ECC, bus parity checking, E-Unit parity and residue checking, and instruction retry; 2) history RAMs which record bus and microcode transactions on an audit trail; 3) diagnostic circuitry integral with each MCC, and 4) improved component packaging, particularly in the MCC.

SOFTWARE AND SUPPORT

The 580 systems are completely compatible with IBM System/370 operating systems; in particular MVS/SP Releases 1, 2, and 3, VM/SP Release 1, and ACP, as well as all available Amdahl software products. Amdahl's Universal Timesharing System (UTS), based on the UNIX operating system developed by Bell Laboratories, will be available during the middle of 1981.

Centralized system maintenance and troubleshooting are provided by the 580 Console Complex. Console maintenance features include 1) Scan-In/Scan-Out to record and recreate a particular condition; 2) isolation of faulty components at the console; 3) execution of diagnostic routines by the console; 4) error logging; 5) access to Hardware History Tables to assist in fault analysis; 6) Dynamic Error Analysis to analyze the error logs; and 7) dynamic monitoring of selected I/O channels. The 580 can access the Amdahl Diagnostic Assistance Center (AMDAC) the same as 470 users.

It appears that the 580 has been well received by the data processing community so far, and Amdahl is leaving no doubts about the system's future potential. Memories larger than the present 32 megabytes are definitely in the wings, according to an Amdahl spokesman. The systems presently are designed with 16K memory chips, but improved availability and price for 64K chips could open the door to much larger memories, he said. The new Macrocode firmware has the potential for more sophisticated configurations, he added.

The initial deliveries of the 580 Model 5860 are scheduled for April, 1982, compared to fourth quarter 1981 for the IBM 3081. The larger 580 Model 5880 is scheduled for second quarter 1983. □

➤ CENTRAL PROCESSOR

Within the Amdahl 580 CPU, two instruction functions are continuously performed in parallel: instruction fetch (I-Fetch) and instruction execution.

Each processor cycle the I-Fetch component provides a double word of instruction flow and holds it in the

Instruction Word Buffer (IWB) in the I-Unit until needed for execution. With each cycle instructions are moved in and out of the IWB at the rate of one, two, or three half words of instruction data.

INSTRUCTION UNIT (I-Unit): The I-Unit controls instruction execution and processes system interrupts. Specific functions of the I-Unit include:

- Instruction fetching, decoding, and buffering
- Determining effective operand addresses
- Provide register access for operands
- Maintain overlapped pipeline processing technique via control of Storage Unit (S-Unit), Execution Unit (E-Unit), and I/O Processors (IPs)

After an instruction is fetched, a five-phase pipeline operation takes over. The pipeline concept, also used in the Amdahl 470, permits the I-Unit to have several instructions in various phases of execution simultaneously. With each processor cycle another instruction enters the pipeline from the IWB. The instruction preceding it moves into the next phase of execution. By the fifth processor cycle, at maximum execution rate, five instructions are in the pipeline simultaneously, in different execution phases. Since instruction flow involves five basic steps, at the maximum execution rate the result is an effective rate of one instruction per machine cycle. For comparison, the 470 executes at a maximum rate of one instruction per *two* cycles. This increased execution rate permits the 580 to execute twice as fast as Amdahl's previous top-end system, the 470V/8.

Extensive parity checking is performed throughout the I-Unit. All incoming instructions are checked for parity, and the results are checked again after completion of execution. All control registers and the program status word are checked each time they are used. In addition, parity is checked for the timer and the address generation function, and parity is also maintained for all program-referable data.

The 580 I-Unit is compatible with the IBM System/370 Principles of Operation opcodes. These elements are implemented within the CPU by a mixture of hardware, microcode, and a new class of firmware called Macrocode. Critical system functions are implemented in hardware for fastest execution, while other less critical functions can be implemented in microcode resident on the MCC used by the I-Unit. Macrocode is planned for future system enhancements, most likely to permit Amdahl to respond faster to IBM enhancements which are implemented in microcode.

STORAGE UNIT (S-Unit): All I-Unit data requests are processed by the S-Unit. Virtual-to-absolute address translations are performed in the S-Unit, which includes a Translation Lookaside Buffer (TLB) to facilitate rapid virtual-to-absolute translations. Data traffic between the CPU data buffers and main memory is controlled by the S-Unit. It also provides the bus interface between the CPU and the rest of the 580.

A double word of data is accessed each cycle by the S-Unit from its high-speed buffers (HSB). The four storage arrays in the S-Unit, the data array, the data select array, the tag array, and the TLB array, are accessed simultaneously during this activity. The data array has 512 32-byte lines organized within its primary and alternate partitions, and contains the actual data lines. The tag array mirrors the data array in organization, and contains TLB pointers that indicate the pages to which the data lines belong. The data select array facilitates the virtual address selection process. The TLB array contains the virtual-to-absolute address translations. ➤

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► Since the 580 processes I-Fetch and execution functions separately, two high-speed buffers (HSB) for instructions and operands are provided. Both the Instruction Buffer (I-Buffer) and the Operand Buffer (O-Buffer) have 32K bytes of storage, are two-way, set-associative, and are organized into primary and alternate partitions of 512 32-byte lines. If a line of requested data is not present within a HSB, the S-Unit sends a message to main memory requesting the desired line.

The high-speed TLB has 512 entries organized into primary and alternate portions of 256 translations to speed virtual-to-absolute address translations. Within each TLB entry is Segment Table Origin (STO) information which eliminates the need for a separate STO stack, as in the 470. Address translations conform to the System/370 structure.

EXECUTION UNIT (E-Unit): The E-Unit executes the arithmetic and logical instructions contained in the 580's instruction set. Operands and opcodes are received from/returned to either the O-Buffer or the I-Unit Register Facility as required by the specific instruction. Performance is enhanced within the instruction pipeline via concurrent activity on two separate instructions by the E-Unit Logic Unit and Checker (LUCK) and the various execution cycle processes (multiply, add, shift, pack, and decimal correct). LUCK and execution phase operations require one processor cycle. In addition, the 580 uses an eight-byte-wide data path, compared to a four-byte path in the 470. Amdahl has optimized certain logic algorithms used with frequently-executed instructions to improve execution speeds.

ADDITIONAL PROCESSOR FEATURES: Other features of the System/370 found in the Amdahl 580 processors include control registers, direct addressing, double word buffer, machine check handling, multiple bus architecture, channel command retry, channel indirect addressing, byte-oriented operand feature, console audible alarm, remote console, remote data link, console file, extended control mode, and program event recording.

Machine check handling analyzes errors and attempts recovery by retrying the failed instruction if possible. If retry is unsuccessful, it attempts to correct the malfunction or to isolate the affected task. Channels have the capability to perform channel command retry, a channel and control-unit procedure that causes a command to be retried without requiring an I/O interruption. Channel Indirect Addressing (CIA) is a companion feature to dynamic address translation, providing data addresses for I/O operations. CIA permits a single channel command word to control the transmission of data that crosses noncontiguous pages in real main storage. If CIA is not indicated, then channel one-level (direct) addressing is employed. The byte-oriented operand feature permits storage operands of most non-privileged operations to appear on any byte boundary. Instructions must appear on even byte addresses. The console audible alarm is a device activated when pre-determined events occur that require operator attention or intervention for system operation. Remote consoles are available in addition to the standard console. The remote data link allows establishment of communications with a technical data center to remotely diagnose system malfunctions. The console file is the basic microprogram loading device for the system, containing a read-only file device. The media read by this device contains all the microcode for field engineering device diagnostics, basic system features, and any optional system features. The extended control mode (EC) is a mode in which all features of the System/370 computing system, including dynamic address translation, are operational. Program event recording is a hardware feature used to assist in debugging programs by detecting and recording program events.

The optional Channel-to-Channel Adapter permits direct communication between an Amdahl 580 and an IBM System/370, 303X, or 3081 via a standard I/O channel. It can be attached to a block multiplexer channel and uses one control unit position on either channel. In an interconnection between an Amdahl 580 and an IBM processor, either system can be equipped with the Channel-to-Channel Adapter, and it is required on only one of the interconnected channels. Up to two CCAs can be implemented in a system.

The Two-Byte Interface, available as an option for all multiplexer channels, doubles the bandwidth of the data path between the channel and the control units which support this option.

OPERATIONAL MODE: Amdahl 580 operates in the Extended Control (EC) mode. In the EC mode, the Program Status Word (PSW) and the layout of the permanently assigned lower main storage area are altered to support Dynamic Address Translation and other new system control functions; therefore, virtual-storage-oriented operating systems must be used.

REGISTERS: Sixteen 32-bit general registers are used for indexing, base addressing, and as accumulators. Other program-visible registers are the same as in the System/370. Machine-dependent registers contained in the 580 processors are not visible to the user and may differ from the System/370.

INSTRUCTION REPERTOIRE: The Amdahl 580 instruction set consists of the complete System/370 Universal Instruction Set, including the five System/370 instructions for Dynamic Address Translation.

PHYSICAL SPECIFICATIONS: Environmental conditions for 580 processors are included in the following table.

Temperature Range	60° to 90° F (16° to 32° C)
Underfloor Temperature	50° to 66° F (10° to 19° C)
Relative Humidity Range	35% to 55%
	(noncondensing)
Maximum Wet Bulb Temperature	78° F (26° C)
Heat Output (BTUs/hr)	83,500
Power Consumption	35 to 40 KVA
Power Required	208V, 415 Hz
	208V, 60Hz
	230V, 50 Hz
	380V, 50 Hz
	415V, 50 Hz
	Both 4-wire and three-phase
Mainframe dimensions (L x W x H)	123" x 36" x 70"
	(312 cm x 91 cm x 178 cm)
Mainframe weight	4400 lbs
	(1998 kg)
Minimum configuration room dimensions (L x W)	256" x 128"
	(650 cm x 325 cm)

MAIN STORAGE

STORAGE TYPE: Dynamic NMOS; 16K chips

CYCLE TIME: 280 nanoseconds

CAPACITY: 16 to 32 megabytes, in 8-megabyte increments

CHECKING: Error checking and correction (ECC) circuitry in main memory performs automatic correction of all single-bit errors and detection of all double-bit and most other multiple-bit memory errors.

STORAGE PROTECTION: Storage protection facilities are comparable to those implemented in the IBM System/370. ►

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► **RESERVED STORAGE:** The 580 processors reserve an area in lower memory for such purposes as interrupt handling routines, CPU ID, channel ID, and machine check logouts.

The Amdahl 580 Main Storage Unit (MSU) uses four-way line interleaving and four-way quarterline (each quarterline is eight bytes in length) multiplexing to provide up to 32 megabytes of storage. The data bus paths are 72 bits (double word) wide, and transfer eight-byte messages, plus parity, between the MSU and the Memory Bus Controller (MBC) every cycle. The most common data bus transactions are MSU data fetches, and the 580's bus system has been optimized to support this activity.

MEMORY BUS CONTROLLER (MBC): The primary data traffic manager within the 580 is the MBC. A key element in the instruction execution process of the 580, the MBC receives requests from the CPU, I/O Processor, or console over the A-Bus. The MBC includes the following components:

- **Data Integrity Unit**, which assures that copies of a currently-accessed data line which also exist in other system elements, such as the MSU and the two HSBs, contain the same data.
- **Interrupt Router**, which directs external system interrupts to the CPU.
- **Timer Complex**, which provides System/370 timing facilities such as the time-of-day clock, clock comparator, CPU timer, and interval timer.
- **I/O Router**, which translates logical channel addresses to real addresses, formats them for IOP or console action, and facilitates channel reconfiguration.
- **Main Storage Controller (MSC)**, which provides the correct control signals for MSU memory requests, and generates error checking and correction (ECC) codes.

Once a request has entered the MSU from the MBC, the MSU accesses four quarterlines from one of the four interleaves present and latches them within the Main Storage Data-Out Register. The quarterlines (actually a 32-bit data line) are then routed over the B-Bus (move-in data path) to the appropriate component, such as the S-Unit, IOP, or console.

INPUT/OUTPUT CONTROL

The Amdahl 580 handles I/O activities with an Input/Output Processor (IOP) and 16 block multiplexer channels per CPU as standard. A second IOP is optional per CPU, and can provide an additional 16 block multiplexer channels. Each channel has 256 subchannels and can accommodate data transfer speeds up to 6.0 megabytes per second. The maximum aggregate data rate for the initial IOP with 16 channels is approximately 50 megabytes per second. Utilizing the second IOP increases the aggregate rate to approximately 80 megabytes per second.

The IOP is based on three components: 1) the I/O Controller (IOC), 2) the Bus Handler, and 3) the 16 Interface Handlers associated with the channels. An IOP, which includes the IOC and Bus Handler, is implemented on a single MCC. The IOC and Bus Handler are shared by the 16 channels.

Data flowing in and out of the IOP moves over the 580's two buses. The Bus Handler is the interface to the A-Bus and B-Bus for the IOP, and provides data buffering when needed. The IOC provides the processing capabilities of the IOP, and

manages the Bus Handler and the 16 Interface Handlers. Normal data transfer activities, including channel bus and tag manipulation, and data buffering, are done by the Interface Handlers.

Data and commands are fetched directly from the Main Storage Unit, rather than from a shared HSB. This reduces contention between the I/O subsystem and the CPU.

Subchannel Queuing, a new 580 feature, holds I/O activities that have been denied access to the system, typically a result of a busy device or channel. The held request is then released for processing once the desired device or channel frees up. The feature helps to reduce the CPU load.

CONSOLE INPUT/OUTPUT

The command center of the 580 is the Console Complex, which provides an operator's console interface, and is the primary means of conducting both local and remote system diagnostics. The Console Complex and its associated components are implemented in microcode and contained in a single MCC.

The Console Complex includes the following:

- **Microcoded CPU** with two megabytes of memory, capable of executing a subset of the Amdahl 580 instruction set
- **An I/O channel**, associated with one hard disk and two floppy disks
- **Up to two local and two remote CRT/keyboard units**, comparable to IBM 3277
- **A system scanning facility**
- **Modem control facilities** for access to Amdahl Diagnostic Assistance Center (AMDAC)
- **Microprocessor-based support processor**
- **A Bus Handler** for attachment to the system's A-Bus and B-Bus
- **Two byte multiplexer channels** (four provided in the 5880), each with an associated Interface Handler, which support data rates up to 200K bytes per second.

PERIPHERAL EQUIPMENT

The Amdahl 580 systems can utilize all IBM System/370, 303X, and 3081 input/output and mass storage devices, as well as their plug-compatible counterparts from independent vendors. Detailed coverage of many of these peripherals can be found in Volume 2 of DATAPRO 70.

COMMUNICATIONS CONTROL

Amdahl's 4705 Communications Processor, announced in October, 1980, is fully program-compatible with the IBM 3705-II and has approximately 1.8 times the power of the 3705-II. The 4705 has from 64K to 512K bytes of memory, in 64K-byte increments. Up to 352 communications lines can be connected, and the start/stop, BSC, and SDLC protocols are supported. The 4705 is compatible with most standard IBM communications software and access methods. For more details on the Amdahl 4705, please see Report C13-044-101 in Datapro's Data Communications service. ►

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► SYSTEM RELIABILITY

To ensure consistently high levels of reliability, availability, and serviceability in the 580, Amdahl has incorporated a wide range of features utilizing the 580's design, technology, and packaging.

- Sophisticated ECC circuitry, including Main Storage ECC, buffer ECC, parity checking in the buses and E-Unit, and instruction retry.
- History RAMs that provide an audit trail of system activities.
- Diagnostic circuitry contained within each MCC.
- Improved fault isolation from denser LSI design, which can implement an entire system function on a single MCC.
- Improved reliability through fewer overall connections in the LSI and MCC packaging.
- RAMs and LSI circuitry packaged on the same MCC.

SERVICE AND SUPPORT

Amdahl's commitment to the efficient maintenance of the 580 is reflected both in the 580 itself and Amdahl's field support organization.

The Console Complex is the hub of all diagnostic operations in the 580. Diagnostic functions are implemented in microcode for greater reliability, and include:

- Re-creation of a failed system condition through scan-in/scan-out records
- Isolation of defective Field Replaceable Units (FRUs) with an internal console-generated program
- An enhanced Maintenance Analysis Language to permit scanning the system trouble log and execute diagnostic routines as needed
- Access to history logs to aid in error diagnosis
- History logs analyzed by the Dynamic Error Analysis program
- Selective channel monitoring via the Integrated Channel Analyzer

AMDAHL DIAGNOSTIC ASSISTANCE CENTER (AMDAC): Located at Amdahl headquarters and at the East Coast support center, AMDAC is maintained 24 hours per day and 7 days a week by technical support specialists to solve difficult problems that cannot be resolved by field engineering on site. Via the modem in the Console Complex, an on-line telephone hookup can be established between AMDAC and the customer system. AMDAC maintains a variety of system consoles, any of which can perform standard diagnostic tests on the user's system. Program Temporary Fixes (PTFs) can also be implemented on a 580 via the Console Complex.

SOFTWARE

The Amdahl 580 can support IBM System/370 operating systems, particularly MVS/SP Releases 1, 2, and 3, VM/SP, and ACP. Support is included for such major IBM subsystems as HASP, ASP, TSO, TCAM, JES2, JES3, VTAM, RSCS, and CMS.

VIRTUAL MACHINE/PERFORMANCE ENHANCEMENT (VM/PE): This software product is designed to reduce system overhead when running the IBM MVS or SVS control program on the same computer as the IBM VM/370 control program. VM/PE Release 2.0 supports the latest releases of SVS, MVS, VM/370, and VM/BSE, includes support of dedicated channel I/O masking, and provides improved logic to reduce page zero swap overhead. VM/PE Release 2.1 provides a Performance Monitor that collects various data from data counters for future analysis in user programs.

UNIVERSAL TIMESHARING SYSTEM (UTS): Based on the UNIX Timesharing Operating System developed by Bell Laboratories, UTS provides a powerful, user-oriented timesharing environment. UTS can operate as a virtual machine under VM/370 or VM/SP. It features asynchronous processing, simplified I/O interfaces, a powerful text processor, full-screen processing capabilities, flexible hierarchical file structures, RJE functions, and system status reporting. UTS is currently planned for release in the second quarter of 1981.

AMDAHL INTERNALLY DEVELOPED SOFTWARE (AIDS) is a class of software designed to improve system performance and productivity of the DP staff. Software is developed for the AIDS program by Amdahl employees as software solutions to specific customer needs. AIDS are distributed on an "as is" basis, with no warranty.

PRICING

The Amdahl 580 systems are offered for purchase or for lease under two- or four-year operating lease plans. Leases may be renewed for 12-month periods. Lease payments must be made monthly in advance. Lease payments include the lessee charge, property taxes, and insurance, but not maintenance charges. The minimum lease term for a system upgrade is 12 months. Leases can be terminated after two years upon payment of 30 percent of the total remaining rental payments. A 90-day written notice is required for cancellation. For users wishing to purchase leased equipment, purchase credits of 50 percent of each monthly payment are allowed to a maximum aggregate credit of 50 percent of the purchase price. The purchase credit applies either to the original lessee or the current lessee.

Monthly maintenance charges are not included in lease charges. Maintenance is provided for 24 hours per day and 7 days per week.

Amdahl supplies its own versions of the supported IBM systems releases to Amdahl users and issues Amdahl corrections to the IBM Program Temporary Fix (PTF) tapes.

The Field Support Center (FSC), located in Sunnyvale, California, helps insure a smooth transition at installation time. The FSC also is chartered to analyze and correct problems in supported operating systems. ■

Amdahl 580 Systems

EQUIPMENT PRICES

	<u>Purchase Price</u>	<u>Monthly Maint.</u>	<u>2-Year Lease</u>	<u>4-Year Lease</u>
PROCESSORS AND MAIN MEMORY				
5860 CPU Complex; includes two 32K-byte buffer storage units, console with maintenance processor, power distribution unit; main memory and channels as listed below.				
With 16,777,216 bytes of main memory and:				
16 channels	\$3,800,000	\$ 9,850	\$110,375	\$ 88,300
24 channels	3,950,000	10,050	115,125	92,100
32 channels	4,100,000	10,250	119,875	95,900
With 25,165,824 bytes of main memory and:				
16 channels	4,000,000	10,250	116,125	92,900
24 channels	4,150,000	10,450	120,875	96,700
32 channels	4,300,000	10,650	125,625	100,500
With 33,554,432 bytes of main memory and:				
16 channels	4,200,000	10,650	121,875	97,500
24 channels	4,350,000	10,850	126,625	101,300
32 channels	4,500,000	11,050	131,375	105,100
5880 Dual CPU Complex; includes two 32K-byte buffer storage units, console with maintenance processor, power distribution unit; main memory and channels as listed below:				
With 33,554,432 bytes of main memory and: 36 channels (only configuration given)	7,500,000	N/A	N/A	N/A
8-Megabyte Memory Increment for 580 Series	200,000	400	7,200	5,750
Eight Channel Group for 580 systems	175,000	200	5,950	4,750
Channel to Channel Adapter for 580 processors	15,000	—	625	500

*Includes 24-hour/7-day service; applies to both purchased and leased systems.

	<u>Purchase Price</u>	<u>Monthly Maint. Cost for Purchase</u>	<u>2-Year Lease</u>	<u>4-Year Lease</u>	<u>Monthly 24-hour, 7-day Maint.</u>
4705 COMMUNICATIONS PROCESSOR					
4705-5 Processor with 64K bytes of memory, up to 64 lines	\$38,000	\$276	\$ 850	\$ 760	\$384
4705-6 Processor with 64K bytes of memory, up to 160 lines	49,300	297	1,165	1,040	412
4705-7 Processor with 64K bytes of memory, up to 256 lines	60,600	318	1,480	1,325	442
4705-8 Processor with 64K bytes of memory, up to 352 lines	71,900	339	1,830	1,600	471
MEMORY					
Additional 64K bytes	2,650	52	145	125	72
Additional 128K bytes	5,300	104	290	250	145

SOFTWARE PRICES

<u>Program Products</u>	<u>Monthly License Fee</u>	<u>Comments</u>
VM/Performance Enhancements		
Release 2.0	\$1,750	per installed system
Release 2.1	1,750	per installed system
Universal Timesharing System (UTS)	3,000	per installed system; 6-month minimum system
	<u>Monthly Program Support Charge</u>	<u>Monthly Additional Program Support Charge</u>
Local Programming Support		
VM/SP	\$ 975	\$585
MVS/SP	1,450	835