

"HANDBOOK OF SOLID-STATE LOGIC"

By Members of the Training Department

AMPEX CORPORATION

SECTION I: NUMBERING SYSTEMS

1. Any discussion of so-called "digital", "binary", "logic", or "computer" techniques usually starts off with a discussion of numbering systems.
 - 1.1 Electronic devices, particularly relays and solid-state (transistor) devices can be very efficiently and accurately operated ON or OFF. It is usually called switching mode of operation.
 - 1.2 A system was developed during the 19th century, called Boolean Algebra, after its inventor, an Englishman named George Boole. It defined rules for a system containing only two conditions - George did it or George did not do it. Statements were either TRUE or FALSE. It was an attempt to logically attack non-mathematical problems with the preciseness of classical algebra.
 - 1.3 What was a rather obscure theory gathering dust in a small volume on library shelves became a factor in modern electronics when telephone companies expanding their dial switching systems, needed something to rapidly evaluate the action of many two condition devices - relays.
 - 1.4 They discovered that the rules of Boolean Algebra could be used to simplify complex relay paths and minimize redundancy.
2. Our daily life is tied to a system based on ten discrete levels frequently attributed to the fact that we have ten fingers.
 - 2.1 Since, at the time that man began to require numbers to express quantities, feet were bare, a system based on 20 seems more logical - and at least one historical civilization used such a system.
 - 2.2 Even using only ten fingers, eleven events can be expressed, if the absence of any events (zero) is considered a valid happening.
 - 2.2-1 The ROMAN numbering system - I, II, III, etc. had no discrete symbol for zero events. The idea of zero came into "Western" (European) civilization from Asia through the Islamic civilization. At least one American Indian civilization understood the concept.

3. One man can then express, using his fingers, an amount of oranges, apples, or events.

											
COUNT	0	1	2	3	4	5	6	7	8	9	
EVENTS	1	2	3	4	5	6	7	8	9	10	11

3.1 If it is necessary to count more than the number of events, a second man will be required who uses a finger to indicate that the first man has gone back to the the closed fist - the fact that he had used all his fingers (digits) was remembered, or CARRIED to the second man.

3.1-1 Some primitive tribes have considered anything over ten events as "many".

3.2 Two men can express 20 events, and three men 30 events, in our system. Each additional man becomes more significant as he represents a greater number of hands, hence the least and most significant character, or bit.

5		Least Significant (L S)	- counted sevenths since the last time fists closed.
7		2nd Least Significant- (2 L S)	LS has reached maximum finger count seven times
0		3rd Least Significant- (3 L S)	2LS has not reached maximum finger count, or has reached it one time or more.
1		Most Significant (M S)	- 3LS has been through maximum count ten times and LS 1000 times.

3.3 The BASE or RADIX of our numbering system is TEN (10). The more significant position a digit occupies the larger the power of ten it represents. The number 1075 can be expressed as:

$$\begin{array}{r}
 5 \times 10^0 = 5 \times 1 = 5 \\
 7 \times 10^1 = 7 \times 10 = 70 \\
 0 \times 10^2 = 0 \times 100 = 000 \\
 1 \times 10^3 = 1 \times 1000 = 1000 \\
 \hline
 1075
 \end{array}$$

3.4 Note that the base ten system has ten digits, or discrete bits, 0-9, none of which represent 10.

3.4-1 Any system will utilize base ten digits to a value of RADIX less one.

4. With only eight fingers we could have developed a system based on a RADIX of 8 (octal). With 12 fingers -

RADIX 10	0	1	2	3	4	5	6	7	8	9	0	1	2	3
RADIX 8	0	1	2	3	4	5	6	7	0	1	2	3	4	5
RADIX 12	0	1	2	3	4	5	6	7	8	9	A	B	0	1
RADIX 2	0	1	0	1	0	1	0	1	0	1	0	1	0	1

4.1 Only the least significant digits are shown in the table above. Note that a system based on eight used the digits 0 through 7; the system based on two used zero and one; whereas for a system based on twelve it was necessary to provide two additional symbols.

4.2 Numbers in the base 10 system can be rapidly converted to numbers expressed to another RADIX.

a. Base 10 to base 10.

10	1075	Remainder	
10	107	5	LSD
10	10	7	-1075 (10)
10	1	0	
	0	1	MSD

b. Base 10 to base 12.

12	1075		
12	89	7	LSD 757 (12)
12	7	5	
	0	7	MSD

c. Base 10 to base 8.

8	1075		
8	134	3	LSD
8	16	6	
8	2	0	
	0	2	MSD

2063 (8)

d. Base 10 to base 2.

2	1075		
2	537	1	LSD
2	268	1	
2	134	0	
2	67	0	
2	33	1	
2	16	1	
2	8	0	
2	4	0	
2	2	0	
2	1	0	
	0	1	MSD

10000 110011 (2)

4.3 To convert back to RADIX 10 a base 10 to base 10 (1075_{10}).

$$\begin{aligned}
 5 \times 10^0 &= 5 \times 1 = 5 \\
 7 \times 10^1 &= 7 \times 10 = 70 \\
 0 \times 10^2 &= 0 \times 100 = 000 \\
 1 \times 10^3 &= 1 \times 1000 = \frac{1000}{1075}_{10}
 \end{aligned}$$

b. Base 12 to base 10 (757_{12}).

$$\begin{array}{r}
 7 \times 12^0 = 7 \times 1 = 7 \\
 5 \times 12^1 = 5 \times 12 = 60 \\
 7 \times 12^2 = 7 \times 144 = 1008 \\
 \hline
 1075_{10}
 \end{array}$$

c. Base 8 to base 10 (2063_8).

$$\begin{array}{r}
 3 \times 8^0 = 3 \times 1 = 3 \\
 6 \times 8^1 = 6 \times 8 = 48 \\
 0 \times 8^2 = 0 \times 64 = 000 \\
 2 \times 8^3 = 2 \times 512 = 1024 \\
 \hline
 1075_{10}
 \end{array}$$

d. Base 2 to base 10 (10000110011_2).

$$\begin{array}{r}
 1 \times 2^0 = 1 \times 1 = 1 \\
 1 \times 2^1 = 1 \times 2 = 2 \\
 0 \times 2^2 = 0 \times 4 = 0 \\
 0 \times 2^3 = 0 \times 8 = 0 \\
 1 \times 2^4 = 1 \times 16 = 16 \\
 1 \times 2^5 = 1 \times 32 = 32 \\
 1 \times 2^6 = 0 \times 64 = 0 \\
 0 \times 2^7 = 0 \times 128 = 0 \\
 0 \times 2^8 = 0 \times 256 = 0 \\
 0 \times 2^9 = 0 \times 512 = 0 \\
 1 \times 2^{10} = 1 \times 1024 = 1024 \\
 \hline
 1075_{10}
 \end{array}$$

4.4 RADIX 8 and RADIX 2 enjoy a peculiar relationship because 8 is the cube of 2.

a. Divide the binary version of 1075 into groups of 3, starting from LSD, and convert each of these groups into an equivalent base 10 digit.

$$\begin{array}{r}
 010 \quad 000 \quad 110 \quad 011_2 = 1075_{10} \\
 2 \quad 0 \quad 6 \quad 3_8 = 1075_{10}
 \end{array}$$

c. This ease of conversion is sometimes utilized in economically priced computers to convert the machine binary computations to a numbering system requiring less discrete digits, making it easier to interface with the human machine.

5. Can 1075 = 5701? It can if the least significant digit is clearly defined.



- 5.1 In binary counters, the schematic is usually drawn in such a way that the least significant digit is on the left.

6. Operations in Numbering Systems

- 6.1 Table 6.1 gives the values from one to 40, of digits to bases 10, 12, 8, 4, 3, and 2.

- a. Look for the patterns
 b. Try addition:

$$\begin{array}{rcl}
 12_{10} + 12_{10} & = & 24_{10} \\
 10_{12} + 10_{12} & = & \\
 14_8 + 14_8 & = & (4+4 = 0, \text{ carry } 1) \\
 30_4 + 30_4 & = & (3+1 = 0, \text{ carry } 1) \\
 1100_2 + 1100_2 & = & (1+1 = 0, \text{ carry } 1)
 \end{array}$$

7. SUMMARY

- 7.1 Counting need not be confined to the current system based on ten. Almost any base can be utilized, although more or less characters may be required. The system can be manipulated and valid conclusions reached.
- a. Our system of telling time is one using only part of base ten digits. The maximum number is 60-it runs from 00 hours, 00 minutes, 00 seconds, 00 frame to a maximum count of 23 hours, 59 minutes, 59 seconds, 29 frames. - One more frame generates a carry which puts the numbering system back to zero.
- b. The carry in the hours column could be used to advance a "day" counter to 1.
- 7.2 The section on gating logic discusses the two fingered world of electronic OFF/ON circuits. The rules for manipulating in such a system are covered in detail.
- 7.3 Additional information on methods of electronic counting - binary counters and decoders are covered in section or binary counters and shift registers.

TABLE 6.1 NUMBERING SYSTEMS

BASE 10	BASE 12	BASE 8	BASE 4	BASE 3	BASE 2
00 10 ⁰	00 12 ⁰	00 8 ⁰	000 4 ⁰	0000 3 ⁰	000000 2 ⁰
01	01	01	01	01	000001
02	02	02	02	02	000010 2 ¹
03	03	03	03	10 3 ¹	000011
04	04	04	10 4 ¹	11	000100 2 ²
05	05	05	11	12	000101
06	06	06	12	20	000110
07	07	07	13	21	000111
08	08	10 8 ¹	20	22	001000 2 ³
09	09	11	21	100 3 ²	001001
10 10 ¹	0A	12	22	101	001010
11	0B	13	23	102	001011
12	10 12 ¹	14	30	110	001100
13	11	15	31	111	001101
14	12	16	32	112	001110
1	13	17	33	120	001111
16	14	20	100 4 ²	121	010000 2 ⁴
17	15	21	101	122	010001
18	16	22	102	200	010010
19	17	23	103	201	010011
20	18	24	110	202	010100
21	19	25	111	210	010101
22	1A	26	112	211	010110
23	1B	27	113	212	010111
24	20	30	120	220	011000
25	21	31	121	221	011001
26	22	32	122	222	011010
27	23	33	123	1000 3 ³	011011
28	24	34	130	1001	011100
29	25	35	131	1002	011101
30	26	36	132	1010	011110

BASE 10	BASE 12	BASE 8	BASE 4	BASE 3	BASE 2
31	27	37	133	1011	011111
32	28	40	200	1012	100000 2^5
33	29	41	201	1020	100001
34	2A	42	202	1021	100010
35	2B	43	203	1022	100011
36	30	44	210	1100	100100
37	31	45	211	1101	100101
38	32	46	212	1102	100110
39	33	47	213	1110	100111
40	34	50	220	1111	101000

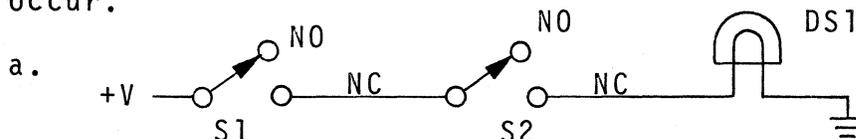
SECTION II: GATING LOGIC

1. Boolean Algebra is a method of expressing statements in the form of equations which can be manipulated. Often circuits can be simplified by cancelling out redundant terms. The results are expressed in terms easily simulated by electronic circuits:

	TRUE ONE (1)	OR	FALSE ZERO (0)
COMMON ELECTRONIC CONDITIONS	CLOSED		OPEN
	HIGH		LOW
	ON		OFF
	POSITIVE		NEGATIVE

2. TERMS AND SYMBOLS

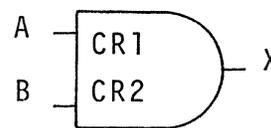
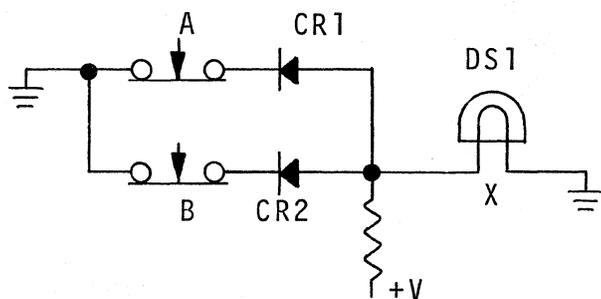
2.1 AND: all switches must be closed before an event can occur.



a. Closing S1 and S2 will turn lamp DS1 on.
 $S1 \text{ and } S2 = DS1$
 $(S1) (S2) = DS1 = S1 \cdot S2$

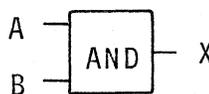
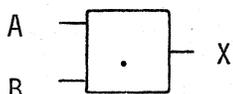
c. The algebraic symbol for multiplication is used. It is also referred to, in some texts, as juxtaposition, or conjunction.

d. When electronic components are used LOGIC symbols are employed to represent the AND function.

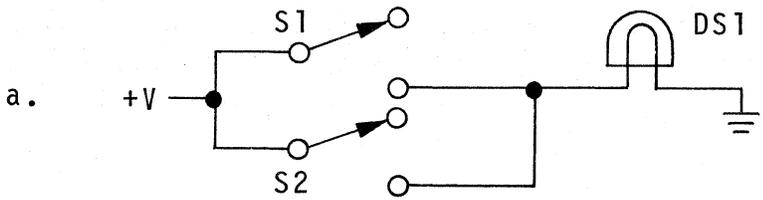


$$\begin{aligned} (A) \cdot (B) &= X = \text{LAMP ON} \\ A \cdot B &= X \\ A \ B &= X \\ (A) (B) &= X \end{aligned}$$

e. Other symbols:



2.2 OR: An output occurs when either of two switches, or both of them, are closed.



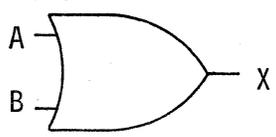
a. Closing S1 or S2 or both will turn DS1 ON.

$$S1 + S2 = DS1$$

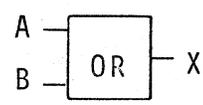
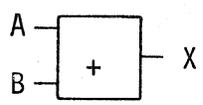
c. The algebraic symbol for addition is used to indicate the OR function.

d. It is also called DISJUNCTION.

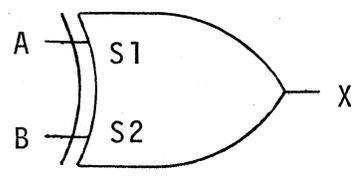
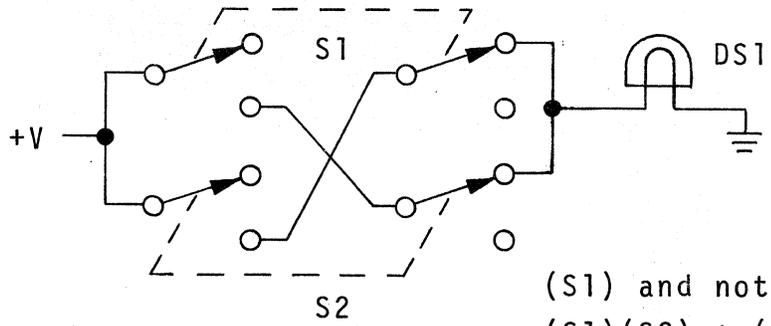
e. The standard symbol for "OR".



f. Symbols also used:



g. If the circuit is such that if one OR the other is closed, but not both for a result, it is called an EXCLUSIVE OR



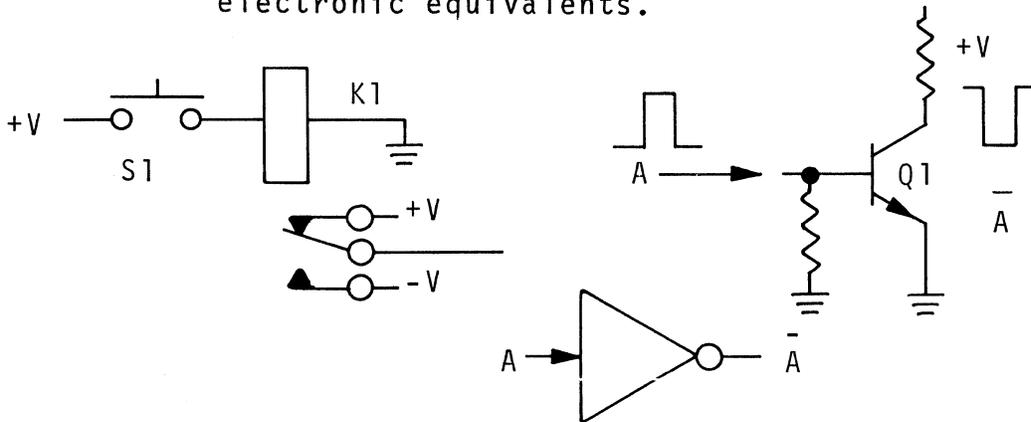
$$(S1) \text{ and not } (S2) \text{ OR } (S2) \text{ and not } (S1) = DS1$$

$$(S1)(S2) + (S2)(S1) = DS1$$

$$(A) (B) + (A) (B) = X$$

h. A later paragraph discusses this circuit in more detail

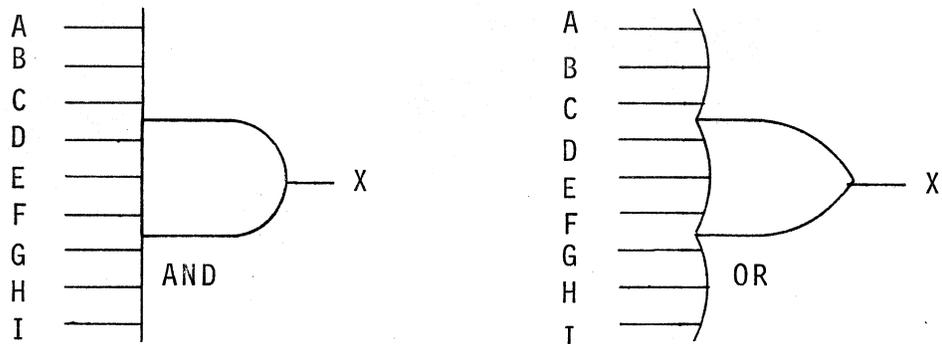
2.3 NOT: inversion, complement, phase reversal are common electronic equivalents.



- a. Operating the relay K1 inverts the positive voltage from S1 to a negative voltage.
- b. Across Q1, base to collector, the signal is inverted.
- c. In the equation, the inverted output is indicated by the bar over the "A".
- d. The small circle on the output of the amplifier symbol indicated that if the input is positive, the output will be negative.
- e. Older symbols:



2.4 When the gates discussed in paragraphs 2.1 and 2.2, have multiple inputs, the symbols are:



$(A)(B)(C)(D)(E)(F)(G)(H)(I)=X$ $(A)+B+C+D+E+F+G+H+I=X$

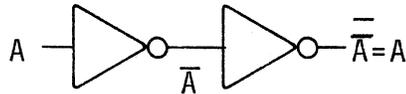
- a. The convenience of equations becomes apparent when dealing with multiple input gates.

3. LOGIC EQUATIONS

3.1 Useful in simplifying circuit requirements, Boolean Algebra has a set of axioms, similar to those in conventional algebra. Some are obvious.

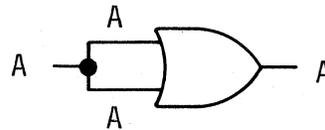
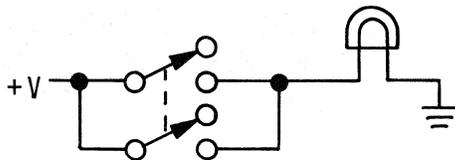
- a. $A + B = B + A$
- b. $A \cdot B = B \cdot A$
- c. $(A+B) + C = A + (B+C) = A + B + C$
- d. $(AB) \cdot C = (A) \cdot (BC) = A \cdot B \cdot C = ABC$

3.2 Double inversion equals no inversion or $\overline{\overline{A}} = A$

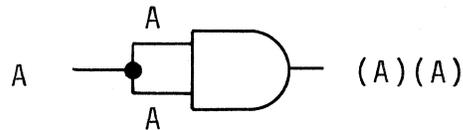
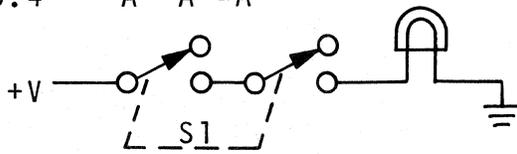


of course in practical electronic circuits, load requirements may make the double inversion necessary.

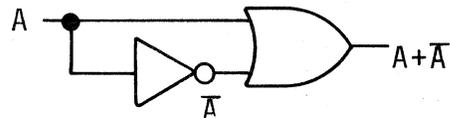
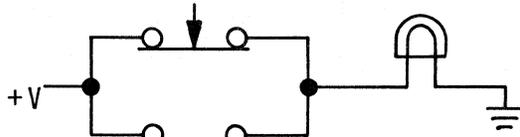
3.3 $A+A = A$



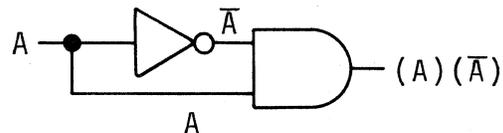
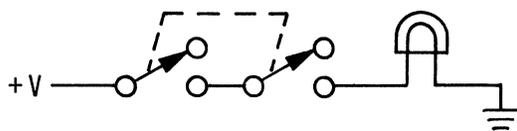
3.4 $A \cdot A = A$



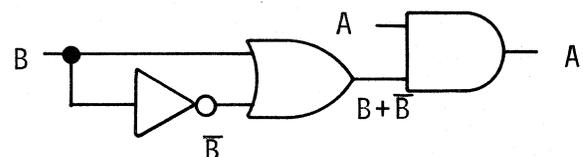
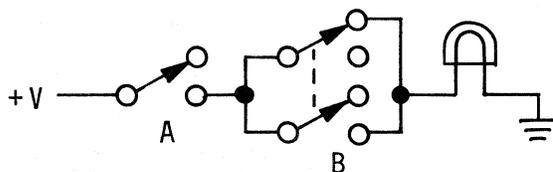
3.5 $A + \overline{A} = 1$



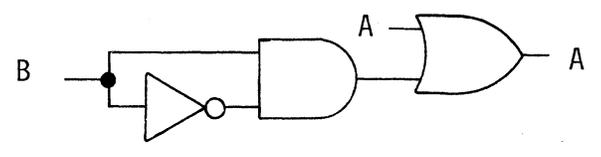
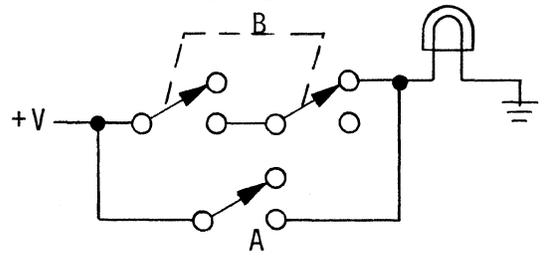
3.6 $A \cdot \overline{A} = 0$



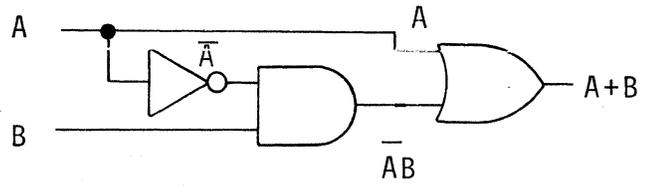
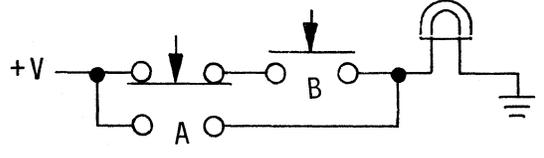
3.7 $A(B + \overline{B}) = AB + A\overline{B} = A$



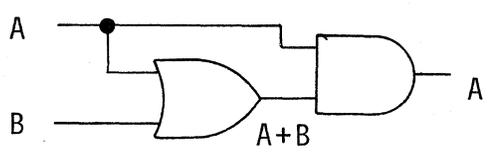
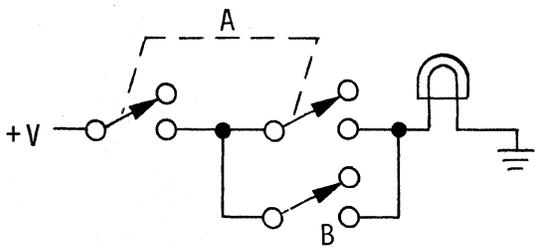
3.8 $A + B \cdot \bar{B} = A$



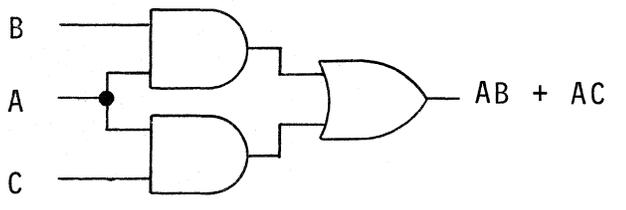
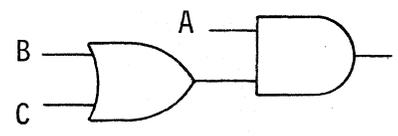
3.9 $A + \bar{A}B = A + B$



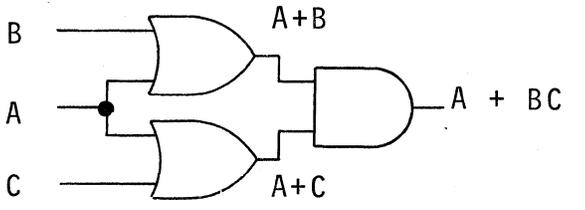
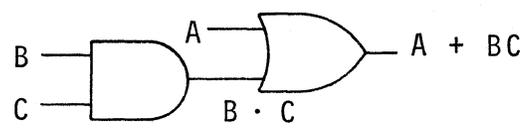
3.10 $A(A+B) = AA + AB = A + AB = A$



3.11 $A \cdot (B+C) = AB+AC$



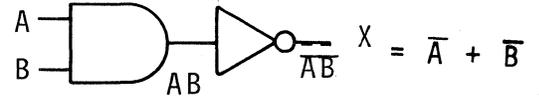
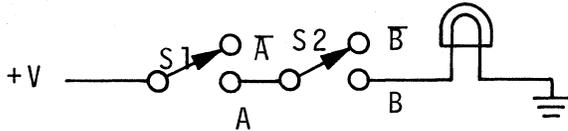
3.12 $A+BC = (A+B) \cdot (A+C)$



3.13 Performing the same action on both sides of an equation does not affect the equality.

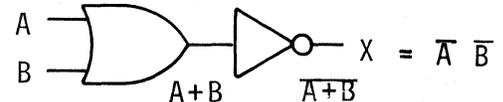
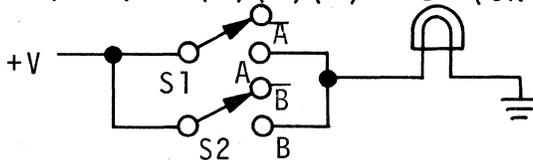
4. DEMORGAN'S THEOREM is useful in understanding logic circuits because of the inversion which occurs when using transistor gates.

4.1 $\overline{AB} = (\overline{A})(\overline{B}) = \overline{A+B}$ ($\overline{AND} = OR$)



If S1 or S2 is not closed, the lamp will not light; or X is low if A or B is low.

4.2 $\overline{A+B} = (\overline{A})(\overline{B}) = \overline{A \cdot B}$ ($\overline{OR} = AND$)



If S1 and S2 are not operated, the lamp will not light.

4.3 Up to this point the actual levels involved have been ignored. In practical circuits the value of "1" and "0" will be defined a specific voltage levels.

a. Positive Logic: The TRUE or one (1) condition is positive (HIGH) with respect to the FALSE, or ZERO (LOW) condition.

"1"	"0"
+4.5	GROUND
GROUND	-5.2V
+12	-12

In a typical equation $A \cdot B = X$, X will be high if A and B are high.

b. Negative logic assumes that the TRUE, or ONE (1) condition is negative with respect to the ZERO (0) condition.

1	0
GROUND	+4.5V
-5.2	GROUND
-12	+12

In the equation $A \cdot B = X$ when (A) and (B) are negative, (X) will be negative.

4.4 AMPEX training material will use positive logic, and equations will be written to indicate where the highs are occurring, unless otherwise indicated.

5. The examples of paragraphs 3 and 4 can be summarized by the following equations:

5.1 For (\cdot) read AND; $(+)$ read OR.

5.2 Basic Axioms

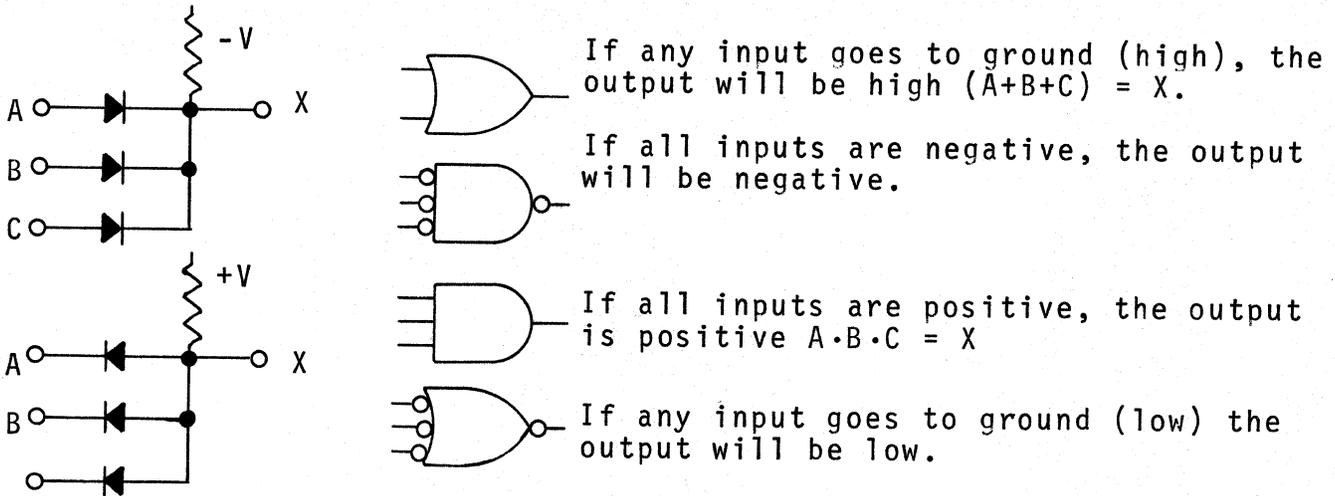
- a. $0 \cdot 0 = 0$
- b. $1 \cdot 1 = 1$
- c. $0 \cdot 1 = 1 \cdot 0 = 0$
- d. $0 + 0 = 0$
- e. $1 + 0 = 0 + 1 = 1$
- f. $1 + 1 = 1$

5.3 Theorems (proven from the basic axioms)

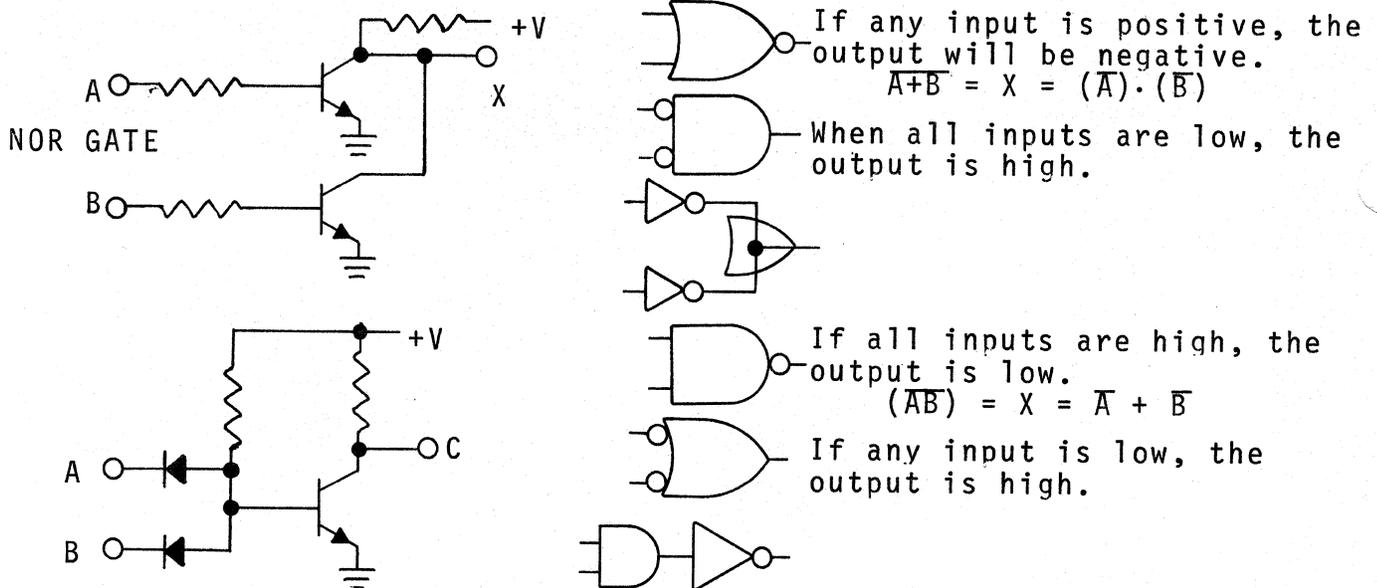
1.
 - a. $0 \cdot x = 0$
 - b. $1 \cdot x = x = x \cdot x$
 - c. $1 + x = 1$
 - d. $0 + x = x = x + x$
2.
 - a. $\overline{0} = 1$
 - b. $\overline{1} = 0$
 - c. $x \cdot \overline{x} = 0$
 - d. $x + \overline{x} = 1$
3.
 - a. $x + y = y + x$ Commutative Rule (Ref 3.1.a, 3.1.b)
 - b. $x \cdot y = y \cdot x$
4.
 - a. $xyz = (xy)z = x(yz)$ Associative Rule (REF 3.1.c, 3.1.d)
 - b. $x + y + z = (x + y) + z = x + (y + z)$
5.
 - a. $xy + xz = x(y + z)$ Distributive Rule (Ref 3.11)
 - b. $(x + y) \cdot (x + z) = x + yz$ Absorptive Rule (Ref 3.12)
6.
 - a. $x + xy = x$
Proof: $x(x + y) = x(1 + y) = x \cdot 1 = x$ (Ref 3.10)
 - b. $x(x + y) = x$
Proof: $x(x + y) = x \cdot x + x \cdot y = x + x \cdot y = x$
7.
 - a. $x + \overline{xy} = x + y$ (Ref 3.8)
 - b. $(x + y)y = xy$
8.
 - a. $\overline{x \cdot y \cdot z} = \overline{x} + \overline{y} + \overline{z}$ De Morgan's Theorem (Ref 4.0)
 - b. $\overline{x + y + z} = \overline{x} \cdot \overline{y} \cdot \overline{z}$
9.
 - a. $(x + y)(\overline{x} + z) = xz + \overline{xy}$ Expansion Theorem
 - b. $(xy) + (\overline{x}z) = (x + z)(\overline{x} + y)$

6. TYPICAL GATING CIRCUITS

6.1 Diode Logic



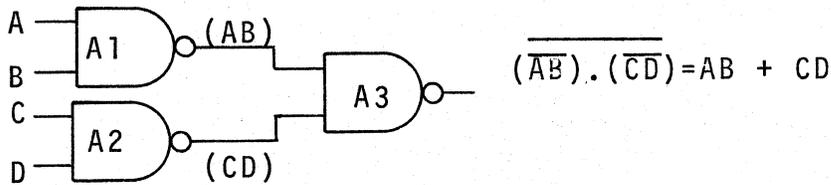
6.2 Transistor logic, or diode transistor logic is more common. This frequently involves inversion.

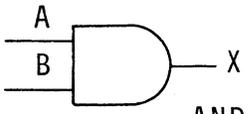
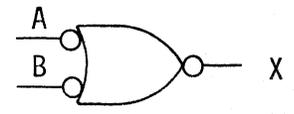
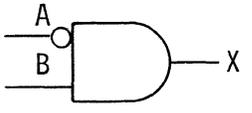
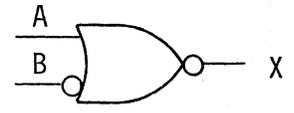
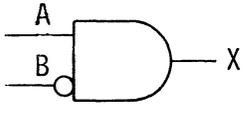
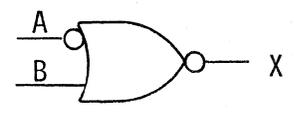
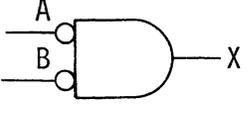
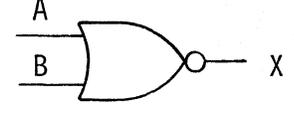
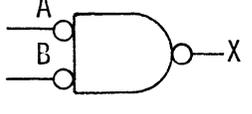
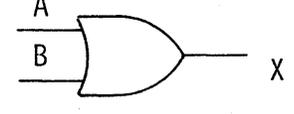
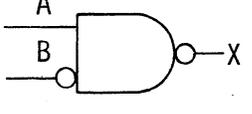
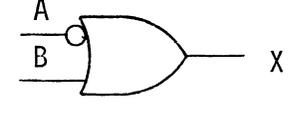
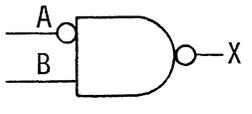
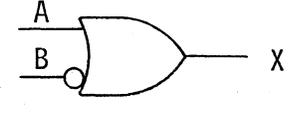
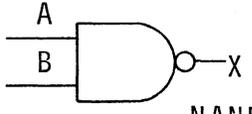
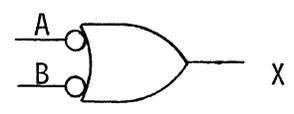


Most manufacturers use the symbol that indicates the function the integrated logic circuit is performing when the input is positive.

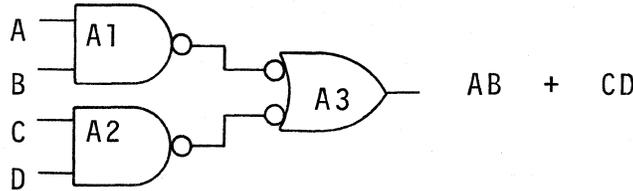
7. AMPEX drawings are currently using a system of FUNCTIONAL LOGIC drawings. This system utilizes the symbol which describes the particular function being performed by a group of gates.

6.1 a. Using manufacturer's symbols



AND	OR	A	B	X	HIGHS	LOWS
 AND		H	H	H	$(A)(B) = X$	$\bar{\bar{A}} + \bar{\bar{B}} = X_L$
		H	H	L	$(\bar{A})(B) = X$	$A + \bar{B} = X_L$
		H	H	L	$(A)(\bar{B}) = X$	$\bar{A} + B = X_L$
		H	H	L	$(\bar{A})(\bar{B}) = X$	$A + B = X_L$
		H	H	H	$A + B = X$	$(\bar{A})(\bar{B}) = X_L$
		H	H	H	$\bar{A} + B = X$	$(A)(\bar{B}) = X_L$
		H	H	H	$A + \bar{B} = X$	$(\bar{A})(B) = X_L$
 NAND		H	H	L	$\bar{\bar{A}} + \bar{\bar{B}} = X$	$(A)(B) = X_L$

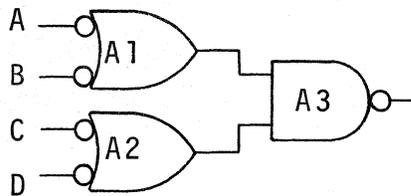
- 7.1 b. If the circuit driven by gate A3 requires a positive level to cause an event (relay closure, reversal of a flip-flop) the circuit, using functional logic, would be drawn:



- 7.2 The conditions - location of "ONE'S" - required to produce a negative output from A3 may be obtained by complementing the equation $AB+CD$

$$\overline{AB+CD} = (\overline{AB}) (\overline{CD}) = (\overline{A+B}) \cdot (\overline{C+D})_L$$

If the circuit driven by A3 requires a negative level, then the logic could be functionally indicated:

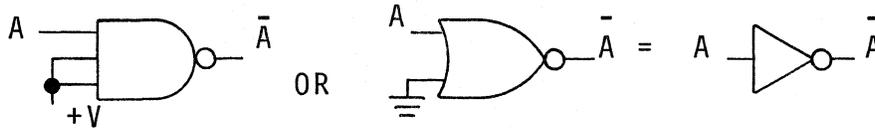


The equation is still $AB+CD$ although the functional logic drawing indicates that the complemented equation drives the following circuit.

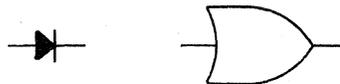
- 7.4 Note that the small circles indicate the relative polarity between input and output to perform the logic function.

- 7.5 See chart on page 10.

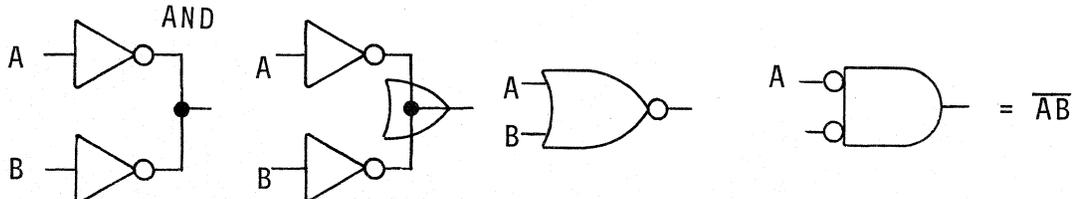
- 7.6 a. NAND and NOR gates are frequently seen on logic schematics with only one signal input. Other inputs may be tied to a voltage, ground, or left unconnected. These units are being used as inverters.



- b. A diode used for isolation may also be drawn as an OR GATE



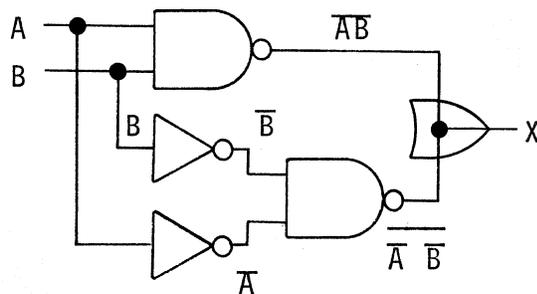
- 7.7 a. Two inverters may have their outputs tied together to form what is sometimes called a WIRED OR or WIRED AND



- b. In some cases it may be necessary to refer to the manufacturer's literature when using this configuration.
- c. In general, an input level which drives one of the outputs to ground controls the logic. The other output cannot rise or fall from ground.

7.8 EXCLUSIVE OR

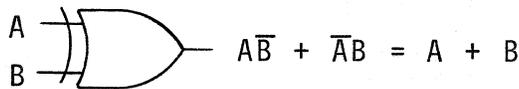
- a. The Boolean logic OR is now defined as A or B or both. It is inclusive. Frequently required is the function A or B, but not both, designated the EXCLUSIVE OR



A	B	X	
H	H	L	\overline{AB}
L	L	L	AB
H	L	H	AB
L	H	H	\overline{AB}

$$(\overline{AB})(\overline{AB}) = (\overline{A+B})(A+B) = \overline{AA} + \overline{AB} + \overline{BA} + \overline{BB} = \overline{AB} + \overline{BA} = A + B$$

- b. If all the circuitry is mounted on a single chip, or if a logic schematic has been simplified, it may be shown as an EXCLUSIVE OR.



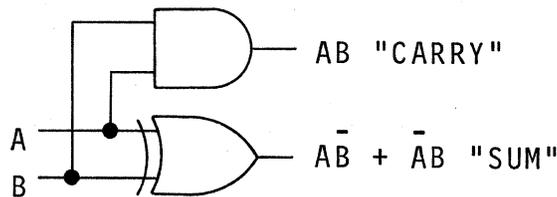
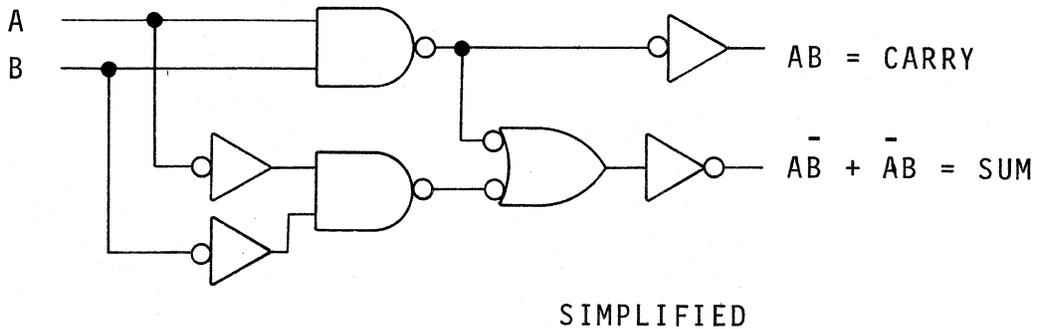
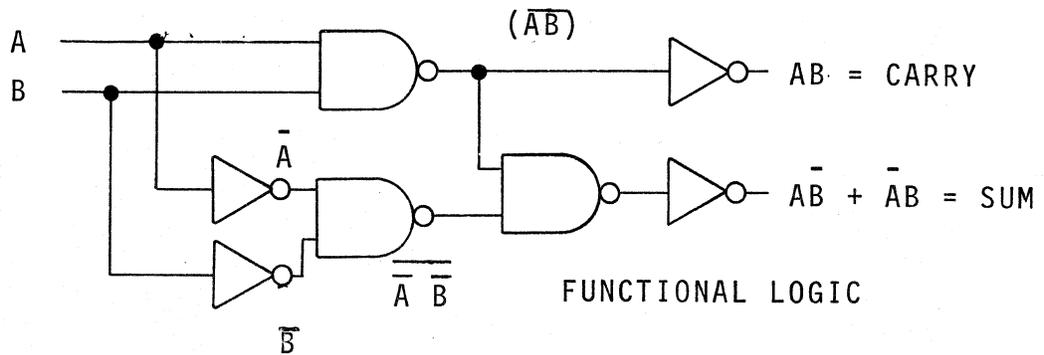
- c. It is also referred to as a half adder because of binary addition relationships:

$$\begin{aligned}
 0+0 &= 0 \\
 1+0 &= 1 \\
 0+1 &= 1 \\
 1+1 &= 0, \text{ carry } 1 \text{ to next most significant digit.}
 \end{aligned}$$

- d. It is called a 1/4 ADDER because it is ambiguous for the sum of both 0+0 and 1+1; the output, in the example given, is low in both cases.

e. In the case where the comparison of two conditions only is important, the half adder is sufficient. In the electronic tape timer, a low output can be used to indicate that switch settings agree with the outputs of the tape counters. The only concern is that conditions are the same, whether they be "ONES" or "ZEROS".

7.9 A "1/2 adder" must sense the difference between 0+0 ($\bar{A}\bar{B}$) and 1+1 (AB) and generate a carry to the next stage when the $A \neq B$ condition exists.



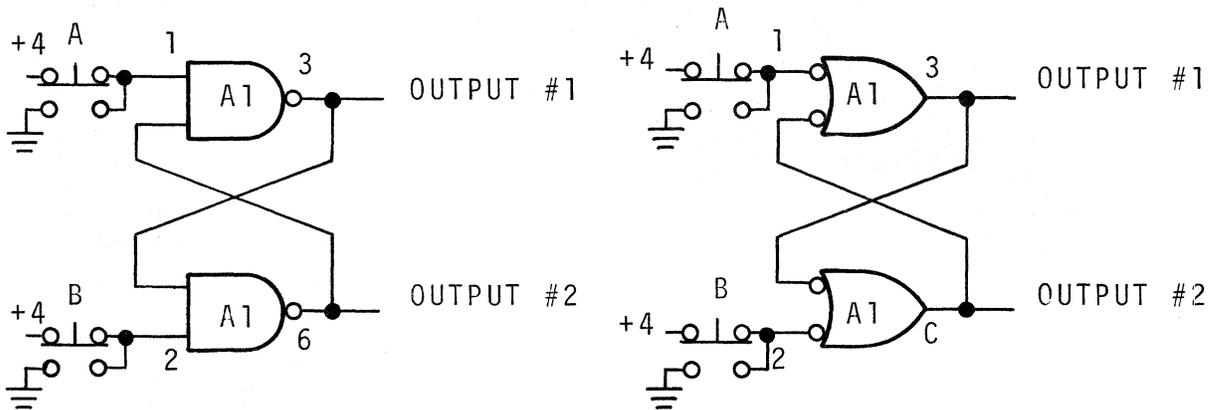
7.10 The "full adder" is two half adders-it includes provisions for a "CARRY" input.

SECTION III BISTABLE MULTIVIBRATOR, OR FLIP FLOP

1. The bistable multivibrator, or flip-flop is one of the most useful circuits in logic design

1.1 The unit may come as an integrated circuit, or consist of NOR and NAND gates.

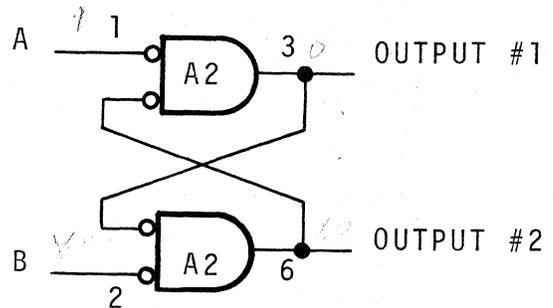
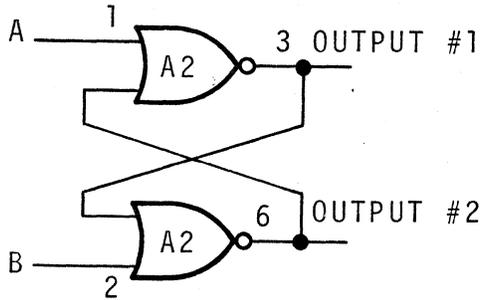
1.2 NAND R-S (RESET/SET) flip-flop.



- a. Pressing Switch A puts a low level into A1-3, and its output goes high (NAND GATE, any low in, output goes high).
- b. The output of A1-6, with two highs in, goes low.
- c. This is fed back to A1-3 to maintain its output high.
- d. Further pressing of switch A will have no effect.
- e. Pressing Switch B will reverse the flip flop.
- f. Pressing both switches will cause both outputs to go high, and is generally considered an ambiguous, or not allowed condition, although this mode of operation is occasionally used.
- g. The final state will depend on which side is released first.

A	B	OUTPUT 1	OUTPUT 2
HIGH	HIGH	NO CHANGE	IN OUTPUT
LOW	HIGH	HIGH	LOW
HIGH	LOW	LOW	HIGH
LOW	LOW	HIGH	HIGH

1.3 NOR R/S FLIP FLOP



A	B	OUTPUT 1	OUTPUT 2
LOW	LOW	MAINTAINS	PREVIOUS STATE
HIGH	LOW	LOW	HIGH
LOW	HIGH	HIGH	LOW
HIGH	HIGH	LOW	LOW (AMBIGUOUS)

1.4 The designators for the inputs depend on output levels. Unless in the ambiguous, or undefined condition, the outputs are always 180° out of phase.

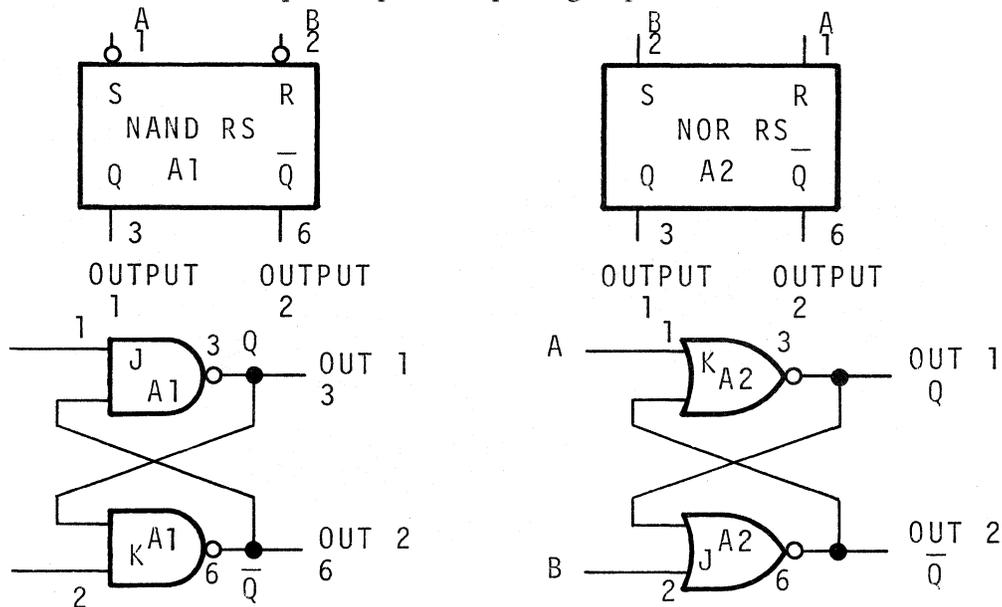
OUTPUT 1	OUTPUT 2
1	0
1	$\bar{1}$
SET	RESET
S	R
	CLEAR
TRUE	C
HIGH	FALSE
FUNCTION	LOW
Q	$\overline{\text{FUNCTION}}$
	\bar{Q}

1.5 The high level can now be defined in terms of an output high level

- a. SET: a level of either negative or positive polarity that places the Q output to a binary 1 state; in positive logic a high level called: SD, Set Drive; PJ, Preset J; S, Set; SJ, Set J; J.

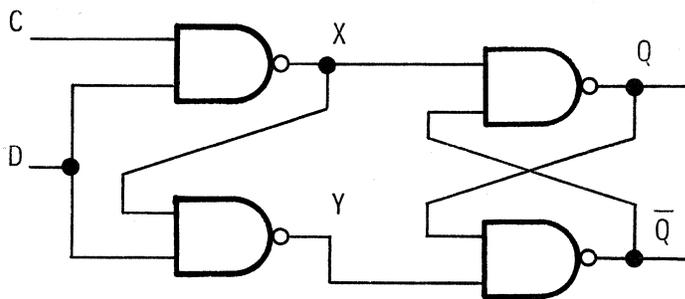
- b. RESET: a level of either polarity which puts the Q output in a binary zero condition called:
 CD, clear drive; RD, Reset Drive; C, Clear; PK, Preset K; RK, Reset K; R, Reset; K.
- c. CP, Clock Pulse, also called T for Toggle or Trigger input is a pulse which may put the flip flop in either state, depending on other conditions. In a J-K flip flop, it must usually go through a cycle; from negative to positive to negative (or just the opposite) with final output action occurring on the trailing edge of the pulse.
- d. PRESET: As commonly used, it may be a pulse or level of the proper polarity to place one or more flip flops, or even an entire unit—such as the EDITOR or EDITEC, to a predetermined desired state.

1.6 The RS flip flops of paragraphs 1.2 and 1.3 could be redrawn.



1.7 These circuits are sometimes referred to as "latches".

2.0 The buffered store RS flip flop (delay flip flop)

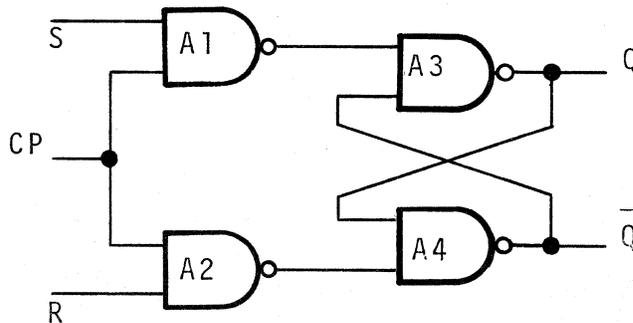


C	D	X	Y	Q
H	H	L	H	H
L	H	H	L	L
H	L	H	H	Q
L	L	H	H	Q

NO CHANGE
NO CHANGE

- a. "C" information is stored only when "D" is high.
- b. Information stored as long as "D" remains low.
- c. Q follows "C" when D is high.
- d. State of "C" stored when commanded by D.
- e. Sometimes called a delay flip flop since the transfer of "C" to Q depends on "D".

2.1 Reset-Set-Toggle flip flop (RST)



CP is a trigger which goes positive some time after S and R inputs have changed state:

S	R	Q	Q after CP
H	L	H	H
H	L	L	H
L	H	L	L
L	H	H	L

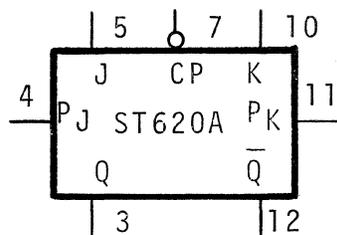
Q follows S on application of clock pulse.

3. The J-K flip flop, Signetics 620A.

3.1 The J-K flip flop is widely available and used in integrated circuit applications frequently. It can be used in any of the configurations discussed so far, and has other applications as well.

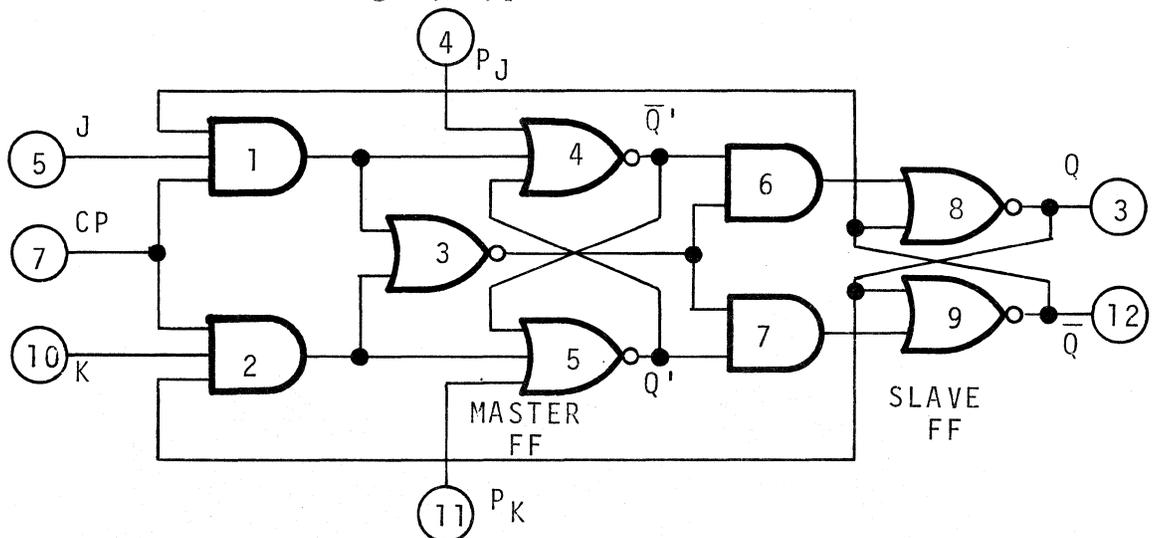
3.2 The discussion applies directly to the Signetics ST 620A used in the AMPEX HS-100B. Other J-K type flip flops will operate in a similar manner, but will follow specific level rules which may differ. While the particular J-K requires positive levels on the J and/or K inputs other types call for negative levels. The clock pulse is one that first goes positive then negative. In other units, just the opposite may be true. Refer to the manufacturers spec sheet for a particular type.

3.3 General Logic Diagram



a. The circle on the CP input indicates that a positive going pulse must be applied, with the output changing state when the pulse shifts from positive to negative. If a square wave was applied, the output would change state only on the negative transition of the signal, dependent, of course, on the conditions set up for other inputs.

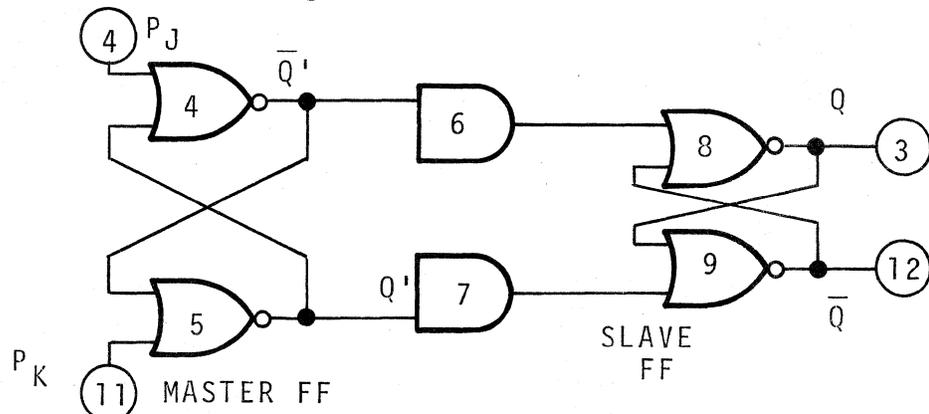
b. Detailed logic, typical JK (ST 620A)



3.4 If pin 7 is tied to ground (a low), then the output of gates 1 and 2 are low and have no effect on the MASTER FF. With two lows as inputs, gate 3 has a high output, and has no effect on Gate 6 and 7, which merely pass the output of the MASTER flip flop to the SLAVE F/F. The logic diagram can be simplified and a truth table developed for PJ and PK.

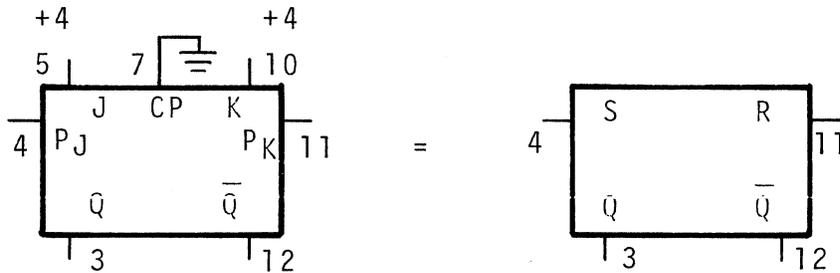
	PJ	PK	Q'	Q	
(1)	H	L	H	H	
(2)	L	L	Q ¹	Q	NO CHANGE
(3)	L	H	L	L	
(4)	H	H	L*	Q	NO CHANGE

*condition 4 is ambiguous for the master FF, but not for the Slave FF and the output.

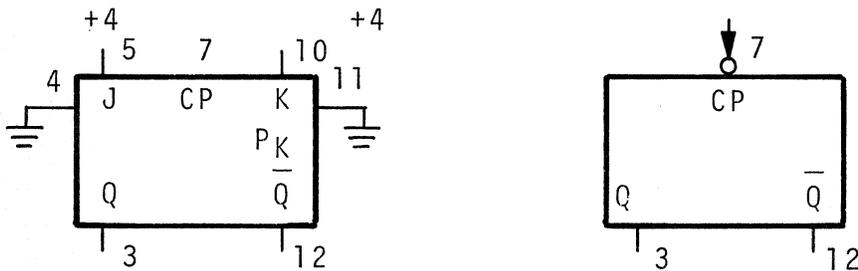


- (1) With PJ high and PK low, \bar{Q}' goes low; GATE 5 has two inputs low, so that Q^1 goes high. GATE 9 goes low. The two negative inputs to GATE 8 put its output high.
- (2) If both inputs PJ and PK go low there will be no change in state.
-In truth tables it is customary to enter "Q" when the inputs listed cause no change of state.
- (3) Taking PK High and PJ low reverses the flip-flop
- (4) If both PJ and PK are high Q and \bar{Q} go low, but there is no change in the output. The final state of Q will depend on which level goes positive first.

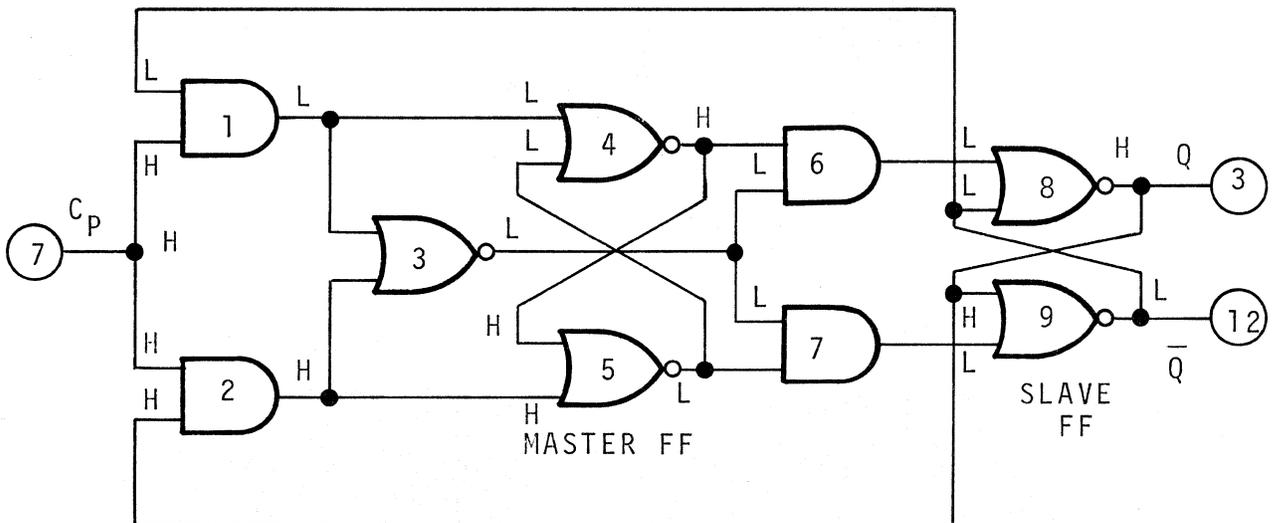
- 3.5 The PJ and/or PK inputs are frequently used to put the JK flip flop into a known PRESET condition.
- a. This mode of operation makes an RS type flip flop out of the JK.



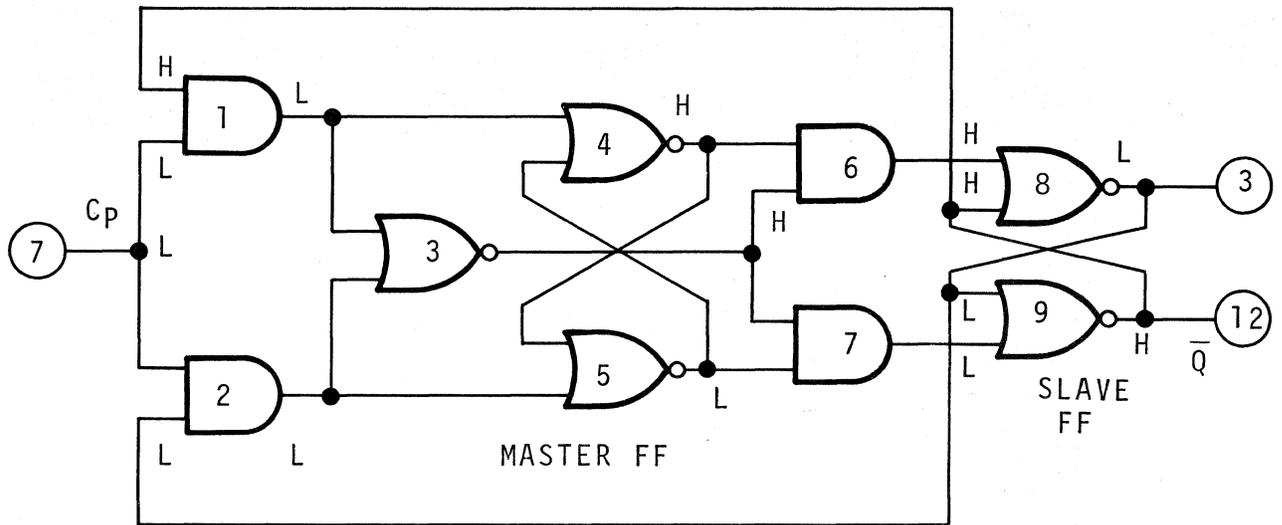
- 3.6 If only the CP input is used, a simple "divide-by-two" results.



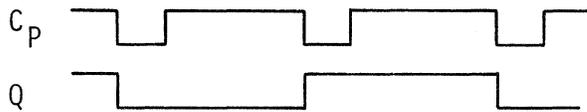
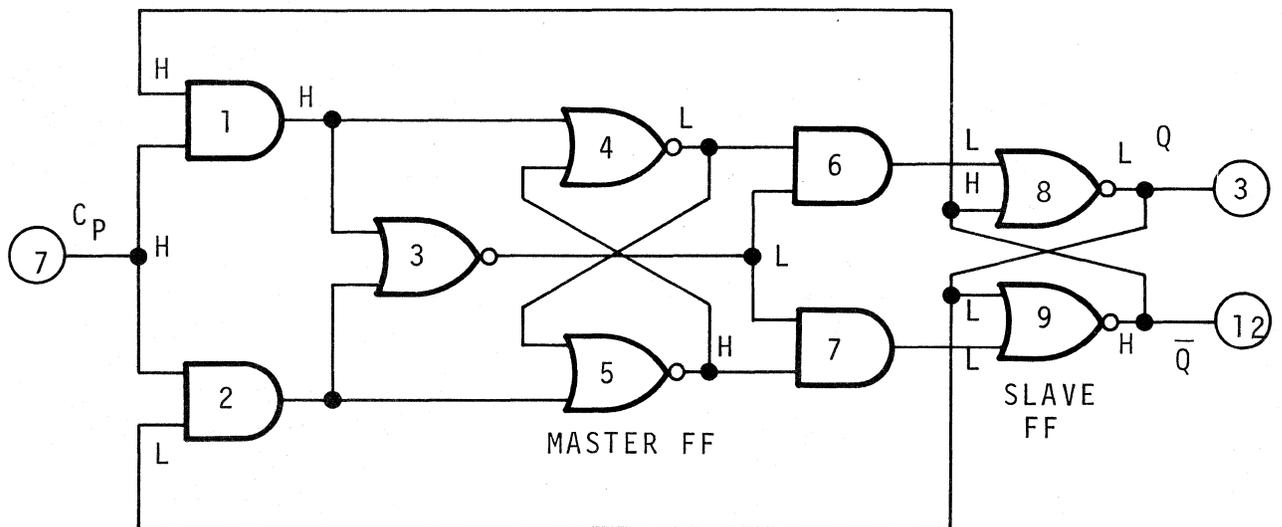
a.



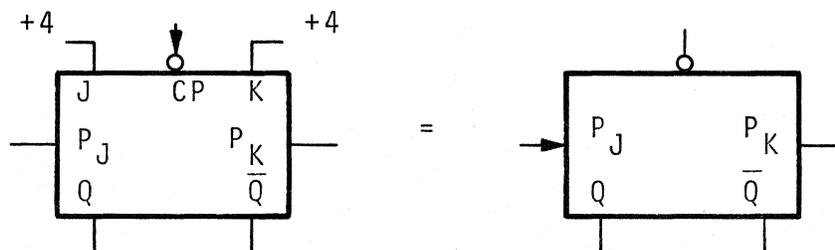
b.

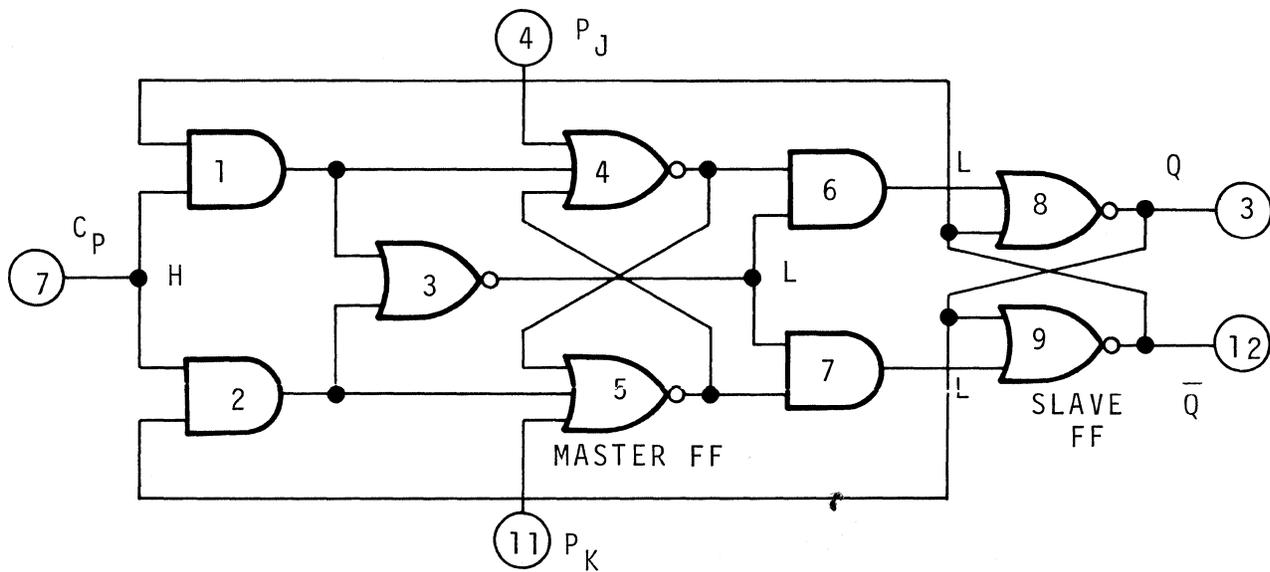


c.

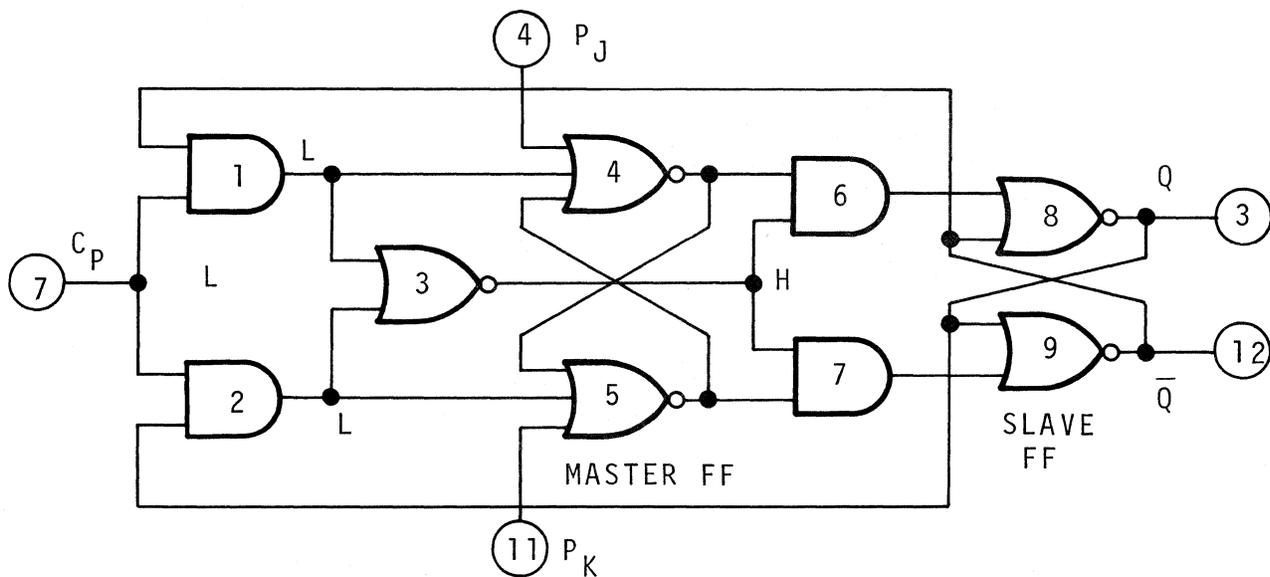


3.7 Using PJ, PK and the CP inputs, the circuit can act as an RST (Para 2.1) or CP can be used as an inhibit to prevent, during some duration of time, the PJ and PK inputs from affecting the output.



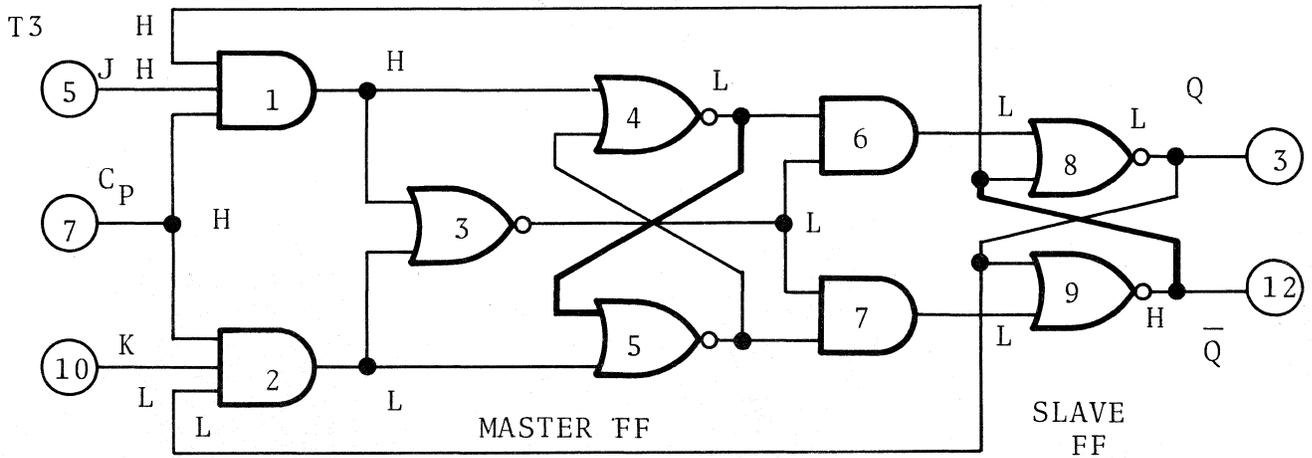
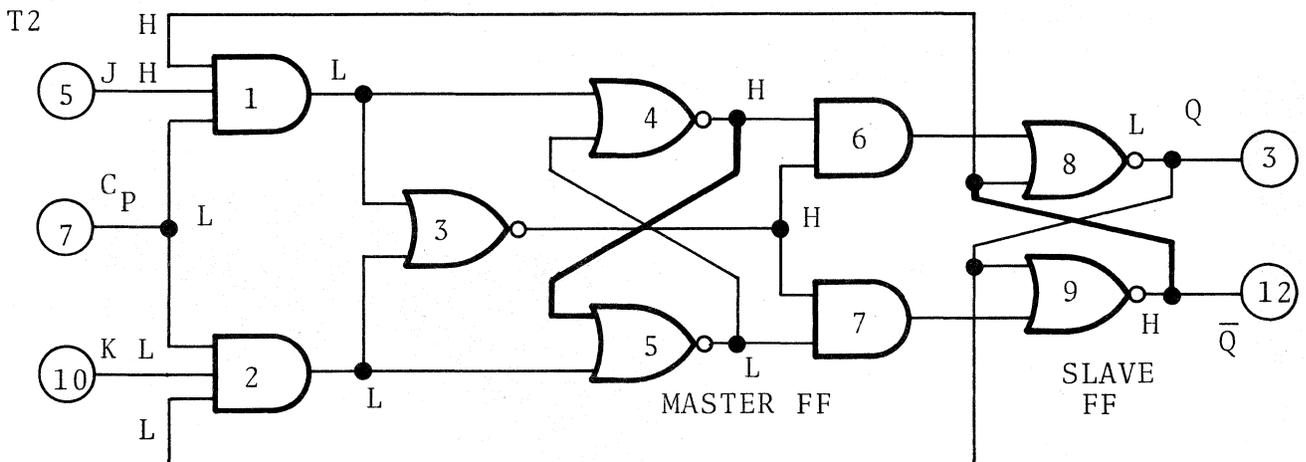
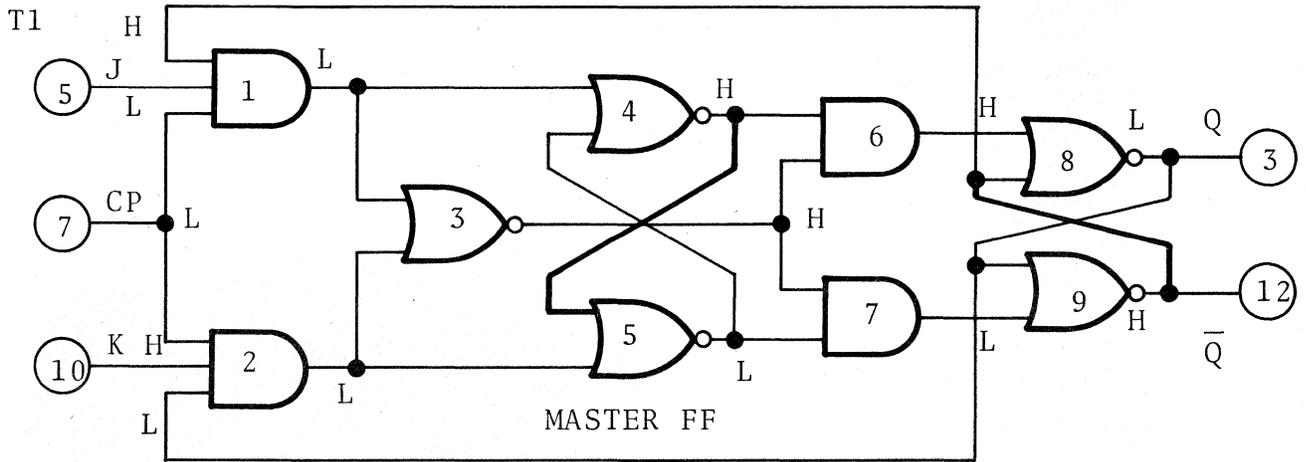
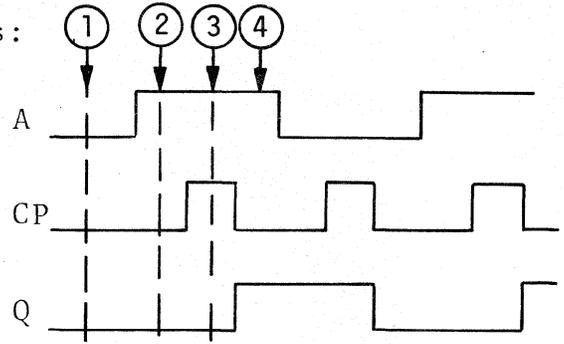
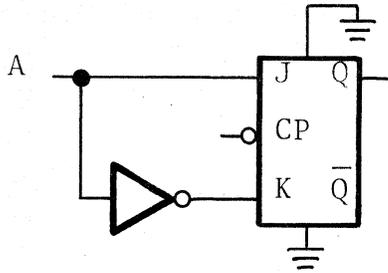


- a. The high condition of C_P will cause a high out of Gate 1 or 2 (depending on Q and \bar{Q}) inhibiting Gates 1 and 2.

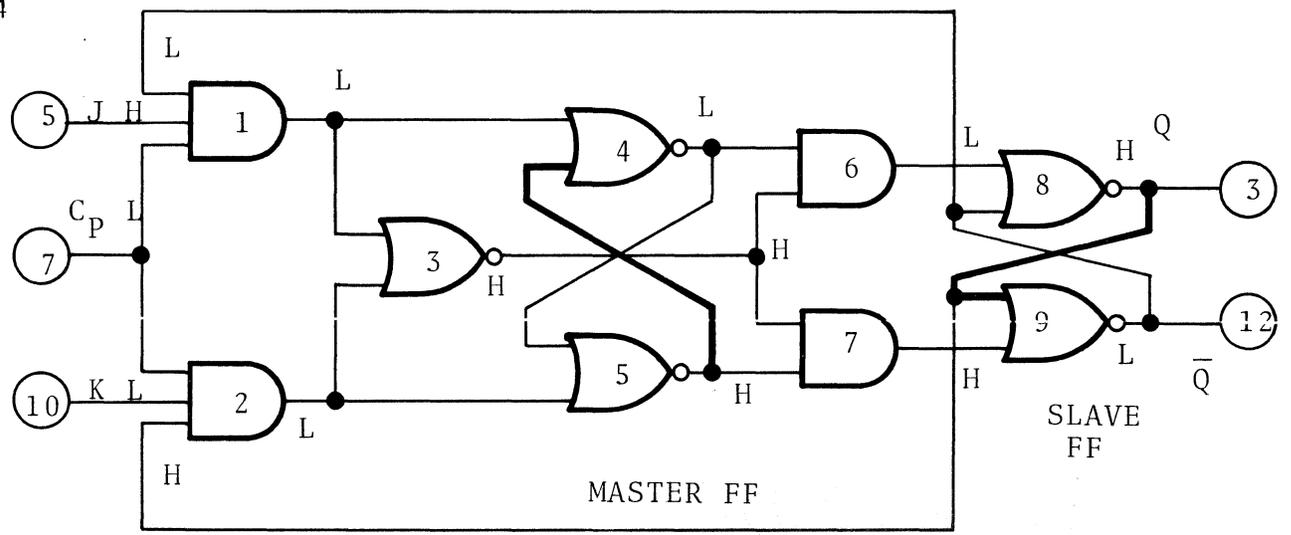


- b. When C_P goes low Q and \bar{Q} will follow P_J and P_K when they are 180° out of phase, and remain in their previous condition when ever $P_J = P_K$.

3.8 Using C_p , J, and K inputs:



T4



- 3.9
- As long as the Cp input is low, any changes in J and K are not felt in the flip flop.
 - When the clock pulse goes high, then the Master FF reacts to changes in J and K, but there is no effect on the slave FF or the output
 - At the time that the clock pulse goes from a high to a low, Q follows J.

J	K	Qt	Qt+1
H	H	L	H
H	H	H	L
H	L	H	H
H	L	L	H
L	H	H	L
L	H	L	L
L	L	L	L
L	L	H	H

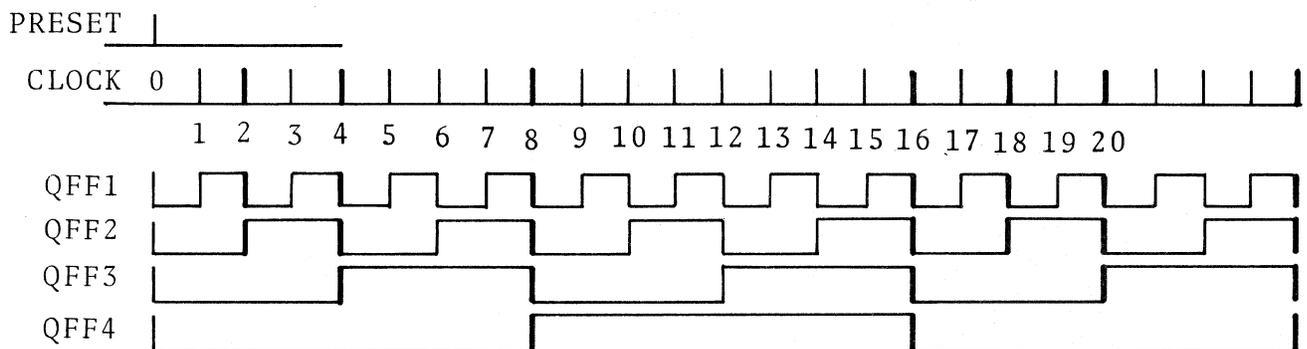
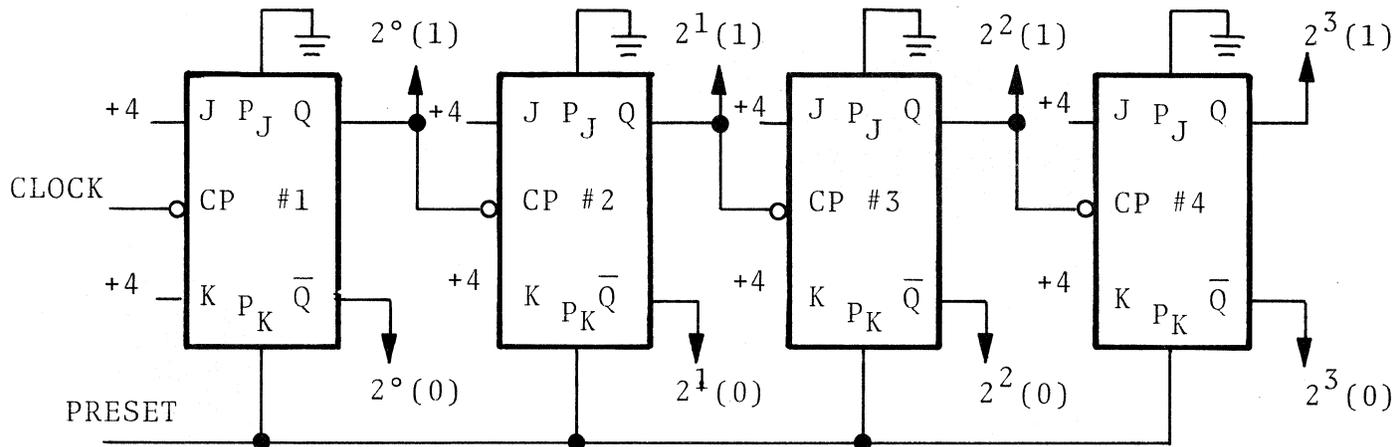
"TOGGLE"
OR ÷ 2

Qt clock pulse goes high
Qt+1 clock pulse goes from high to low

4. This section has covered the bi-stable multivibrator or flip-flop in a general way. Sections covering counters and shift registers will cover common applications.
- 4.1 The ST620A J-K flip-flop used as an example is typical but other versions may follow slightly different rules.
- 4.2 The following rules apply generally to the JK flip-flop.
- a. The J and K inputs must not change during the time that a clock pulse goes through a complete cycle.
 - b. The state of the master flip-flop is established by the leading edge of the clock pulse transition.
 - c. The trailing edge of the clock pulse transfers the Master flip-flop condition to the Slave flip-flop.
 - d. In the case of the ST620A the Pj and Pk inputs affect the output only when the clock pulse input is negative.
 - (1) In other types, the equivalent inputs may over-ride all other circuit inputs.

SECTION IV BINARY COUNTERS

1. In the Television system, it is frequently necessary to count specific events, number of frames, number of lines, etc.. The flip-flop can be configured as a counter to perform this function. It is also acting as a frequency divider.
2. The "ripple" binary counter. The ST620A discussed under JK FF, is used. Output changes state when CP moves Hi to Lo.



2.1 By tabling the conditions of the flip-flops, the similarity to the binary numbering system is apparent.

	Q FF1	Q FF2	Q FF3	Q FF4		1 2^0	2 2^1	4 2^2	8 2^3	16 2^4
PRESET	L	L	L	L		0	0	0	0	0
CP 1	H	L	L	L		1	0	0	0	0
2	L	H	L	L		0	1	0	0	0
3	H	H	L	L		1	1	0	0	0
4	L	L	H	L		0	0	1	0	0
5	H	L	H	L		1	0	1	0	0
6	L	H	H	L		0	1	1	0	0
7	H	H	H	L		1	1	1	0	0
8	L	L	L	H		0	0	0	1	0
9	H	L	L	H		1	0	0	1	0
10	L	H	L	H		0	1	0	1	0
11	H	H	L	H		1	1	0	1	0
12	L	L	H	H		0	0	1	1	0
13	H	L	H	H		1	0	1	1	0
14	L	H	H	H		0	1	1	1	0
15	H	H	H	H		1	1	1	1	0
16	L	L	L	L		0	0	0	0	1
17	H	L	L	L		1	0	0	0	1
18	L	H	L	L		0	1	0	0	1
19	H	H	L	L		1	1	0	0	1
20	L	L	H	L		0	0	1	0	1

2.2 If FF1 is defined as 2^0 , FF2 as 2^1 , FF3 as 2^2 , and FF4 as 2^3 .

- a. Looking at the outputs of the four stages after a certain number of clock pulses have occurred can be converted (High = 1, Low = 0) to an equivalent binary number defining the number of clock pulses.
- b. Using four stages any one of fifteen clock pulses can be uniquely defined. But at the sixteenth pulse, all flip-flops return to their "PRESET" state. All Q outputs are low.

- a binary counter can uniquely define a binary number equal to $2^N - 1$, where N equals the total number of flip-flops.
- in the case above, $2^4 - 1$ or $16 - 1 = 15$ pulses are uniquely defined by the four stage counter.

c. Each stage is dividing by two. Assuming a Clock Pulse rate of 15kHz, then:

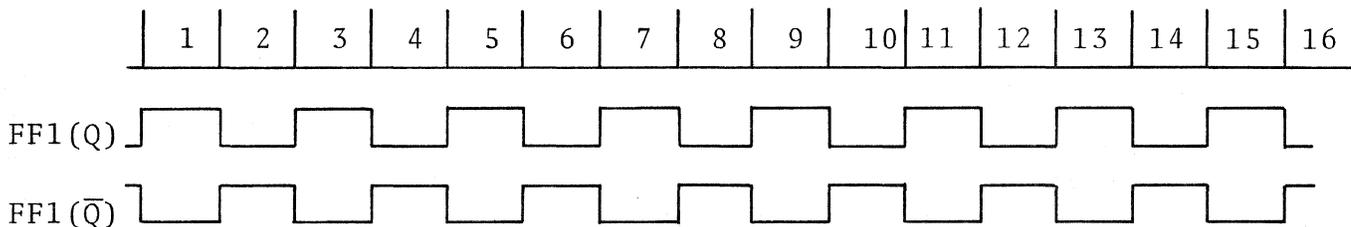
FF1 out = 7.5kHz
 FF2 = 3.75kHz
 FF3 = 1.875kHz
 FF4 = 9375kHz

- d. A flip-flop changes state only when the "Q" side of all previous stages move from a high to a low
- to determine the state of the flip-flops after the eighth pulse in, look at the binary equivalent of decimal 8-1000 (MSB on the left) and convert the zero's and ones to lows and highs.

3.0 Decoding the counter condition.

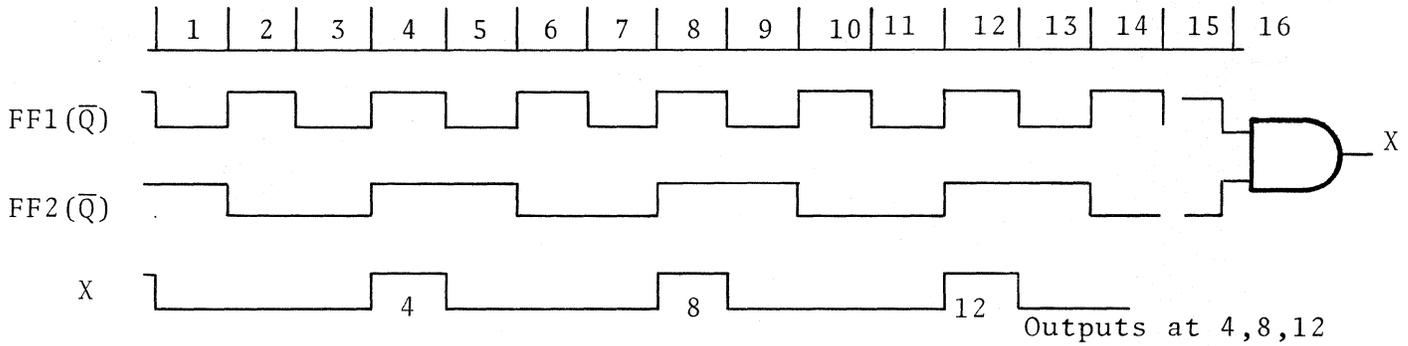
3.1 To determine the time at which the twelfth clock pulse is received, Binary 1100.

a. The Q output of FF1 is high on every other clock pulse.

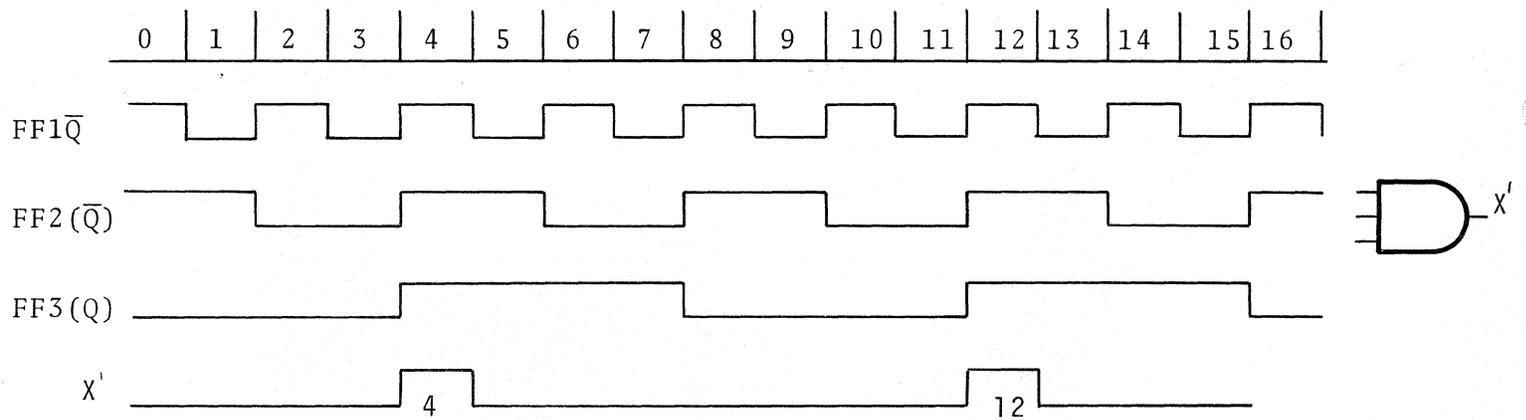


FF1 (\bar{Q}) is high on pulses 2,4,6,8,10,12 and 14

b. AND together FF1 (\bar{Q}) and FF2 (\bar{Q})

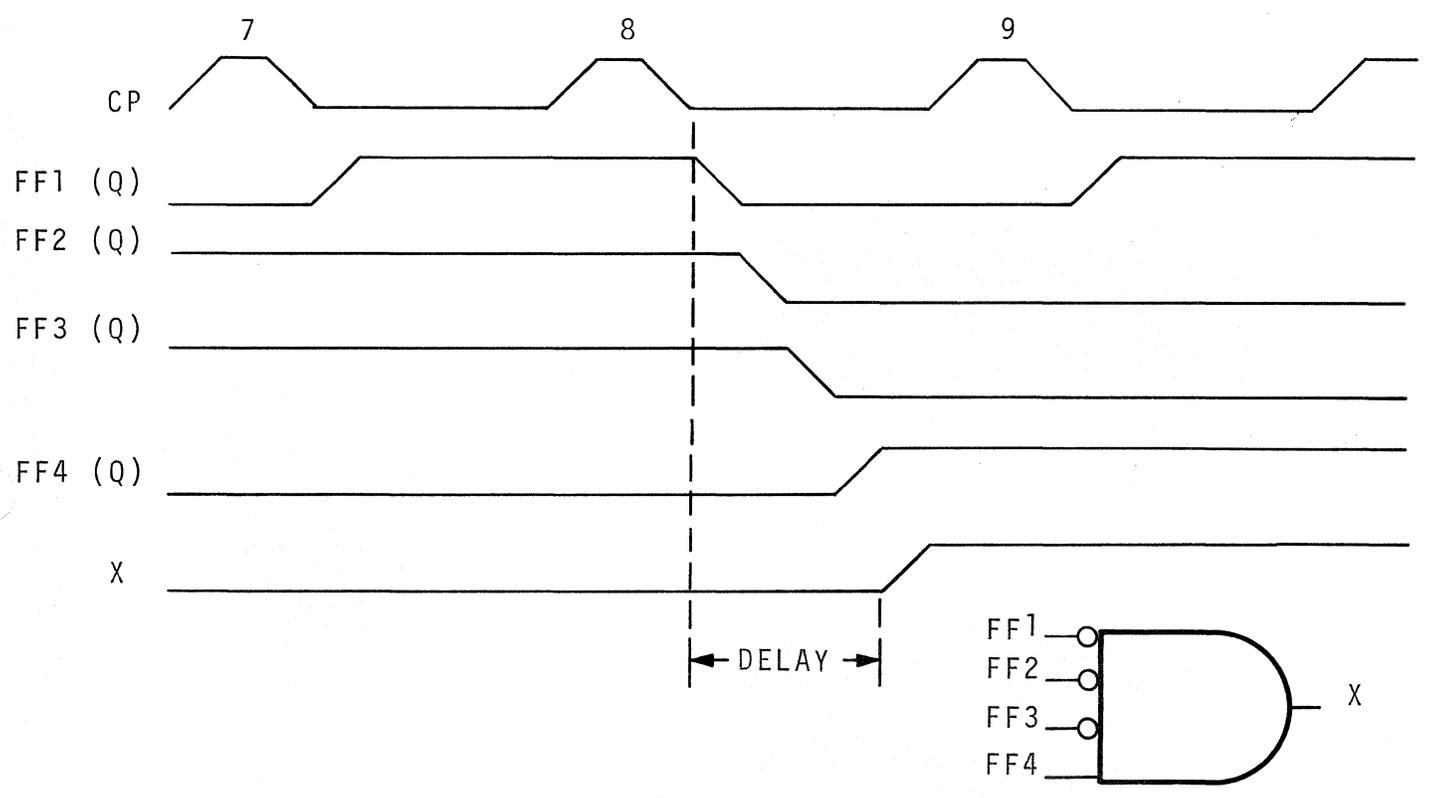


c. AND FF1 (\bar{Q}), FF2 (\bar{Q}) and FF3 Q



d. ANDing FF1(\bar{Q}), FF2(\bar{Q}), FF3(Q) and FF4(Q) will uniquely define clock pulse 12

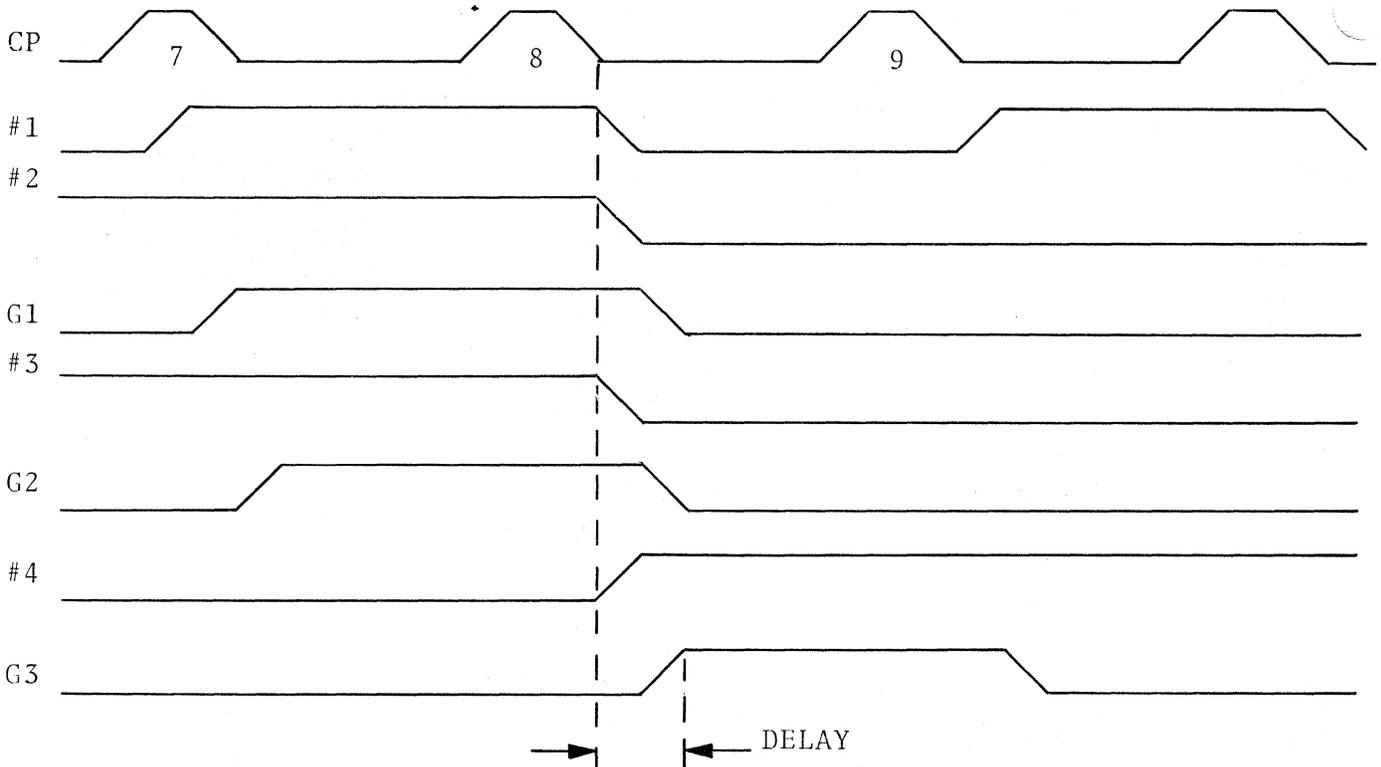
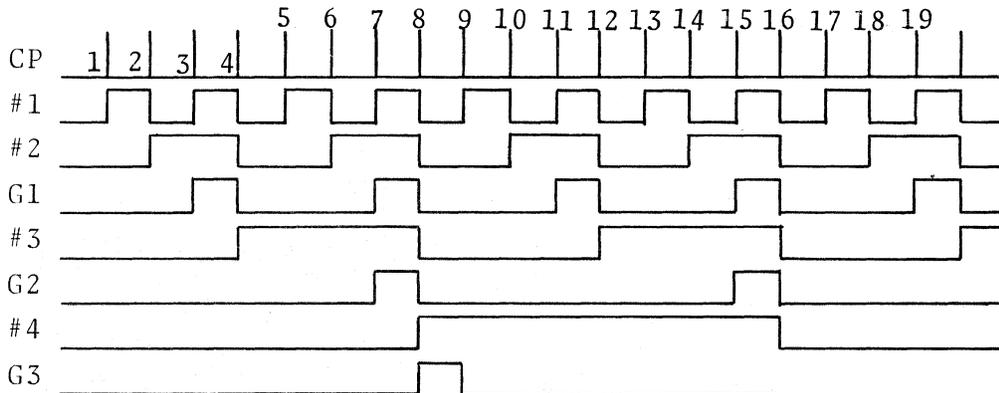
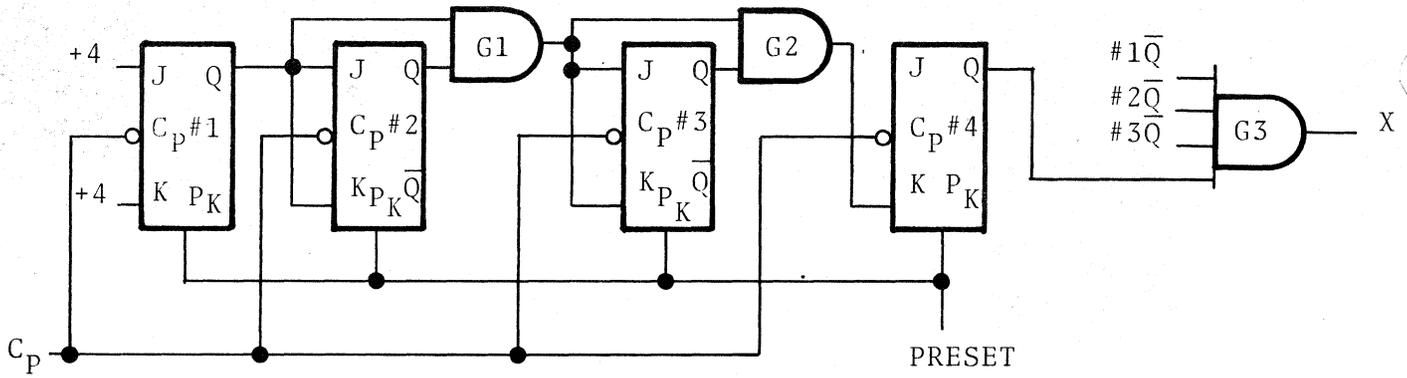
4.1 The "ripple" binary counter is relatively slow. Succeeding stages are changed when the previous stage Q output moves negative. But a definite time is required to affect the following stage. Worst case in this four stage counter would be the 8th pulse, where all four stages change state.



4.2 In the rather exaggerated case above an output pulse from the decode gate is delayed almost a full cycle with respect to the input pulse.

4.3 In some cases the delay, with respect to the frequency of the input pulses, is unimportant, but should be taken into account when examining timing relationships. In other cases special counter circuits have been devised to minimize the ripple delay.

4.4 When the amount of delay cannot be tolerated, the other circuits are necessary.



4.5 Compare this delay with that of the circuit in paragraph 4.1

SECTION 5: BINARY CODED COUNTERS

- 1.0. The counters discussed in the previous section were limited in that they could only divide by 2 so that outputs would always be directly related to a power of 2.
- 2.0. There is then no provision for divide by 3,5, or 10, among others. A requirement in the AVR-1 is to count 250HZ down to 25HZ - divide by 10.
- 2.2. To count to ten a four stage counter must be used, and a decode gate can be used to identify the tenth pulse received.

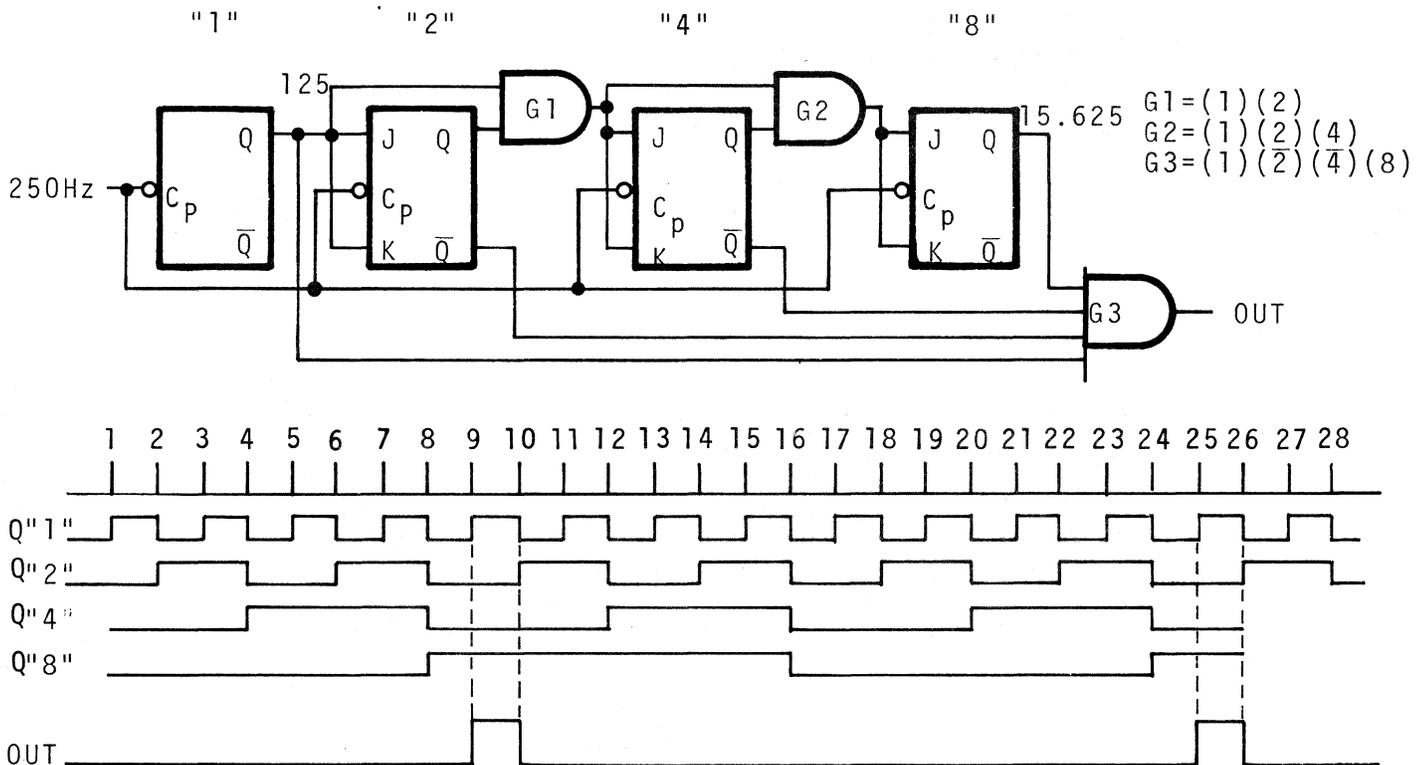


FIGURE 2.1

- 2.3. This decodes a binary ten, but the counter does not return to zero until the sixteenth pulse, so that the next output occurs 15 pulses later.

2.4.

To make it divide by ten, the output pulse must return the counter to the state it was in before the first pulse was received.

- A. One method would be to take the Gate 3 output back to clear inputs and zero the counter.
- B. However, the tenth clock pulse will return stage "1" to that state (\bar{Q} high); the "4" stage is already in that state.
- C. All that is necessary is to prevent the "2" stage from clocking, and to reset the "8" stage. Logic equations for controlling all the flip-flops can be written, and then the required gates put in.
 1. Stage 1 - Allowed to clock as a straight divide by 2.
 2. Stage 2 - Not allowed to clock if "8" is high
 3. Stage 3 - Clock whenever "1" and "2" are high.
 4. Stage 4 - Clock when "1", "2", and "4" are high or when "1" and "8" are high.

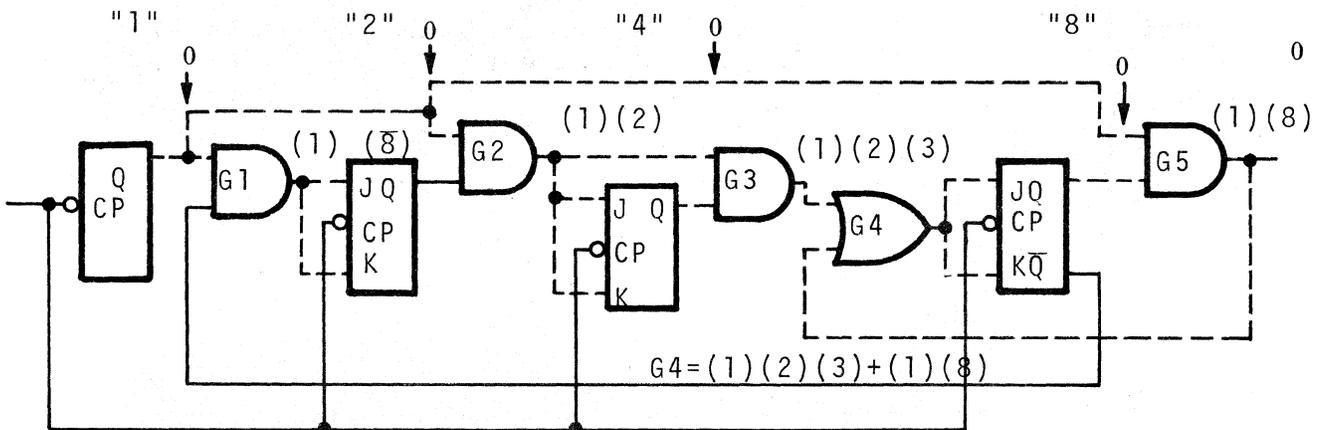
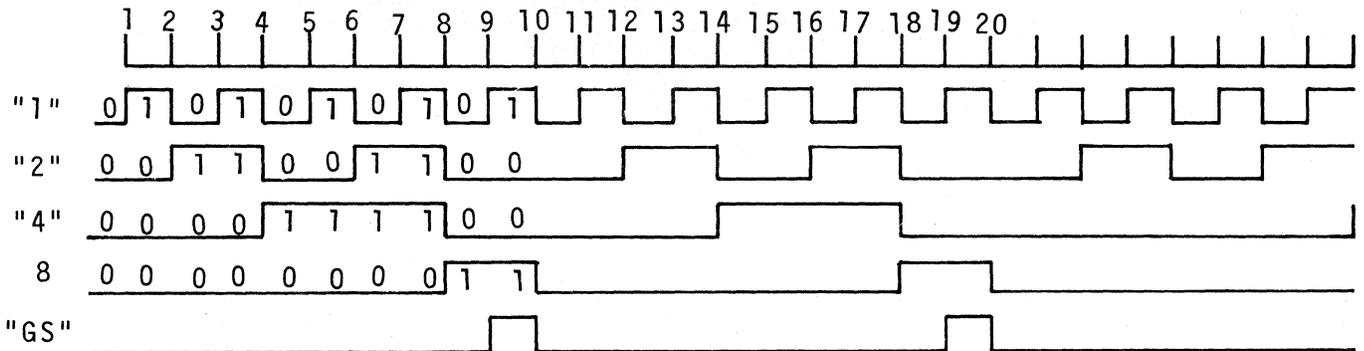


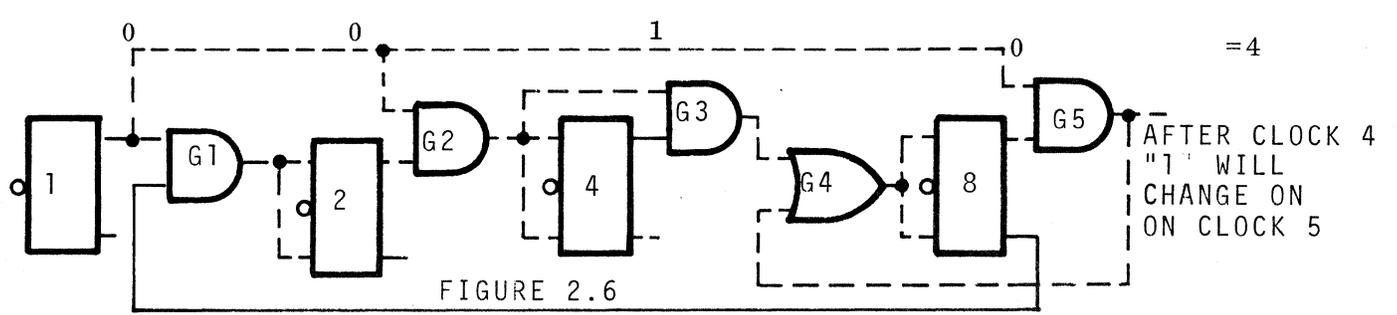
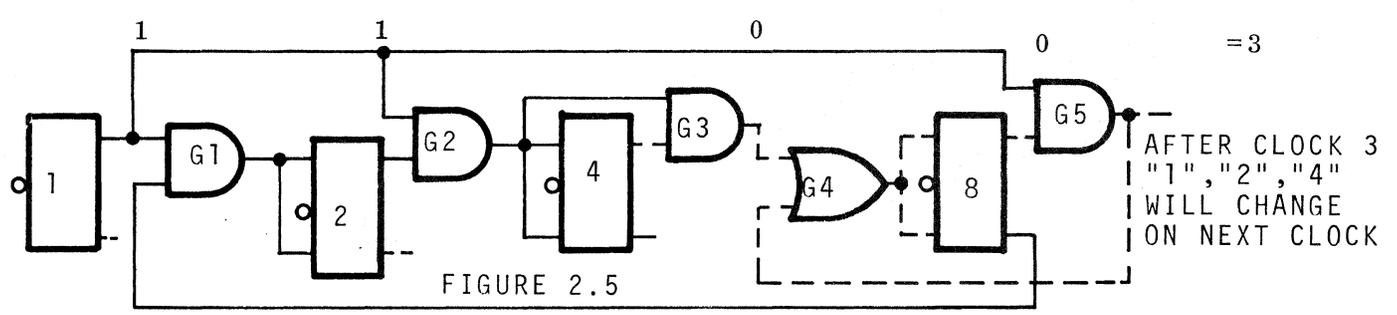
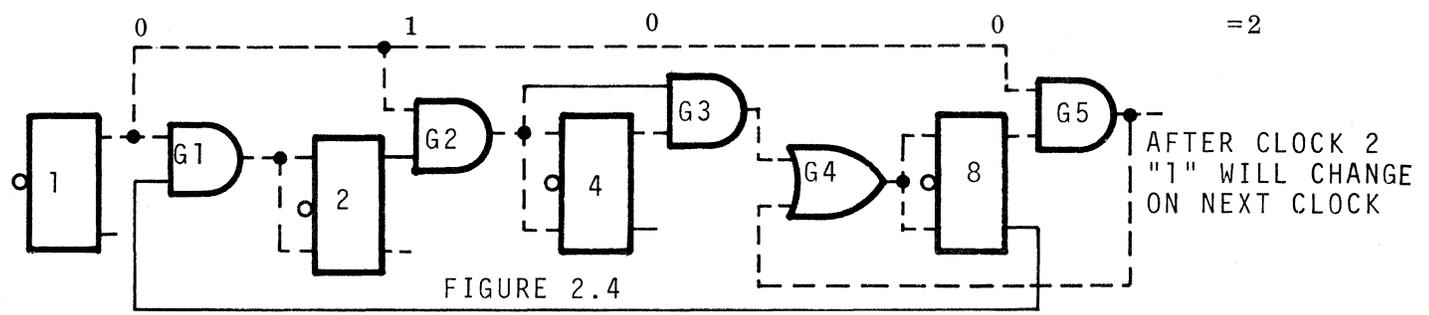
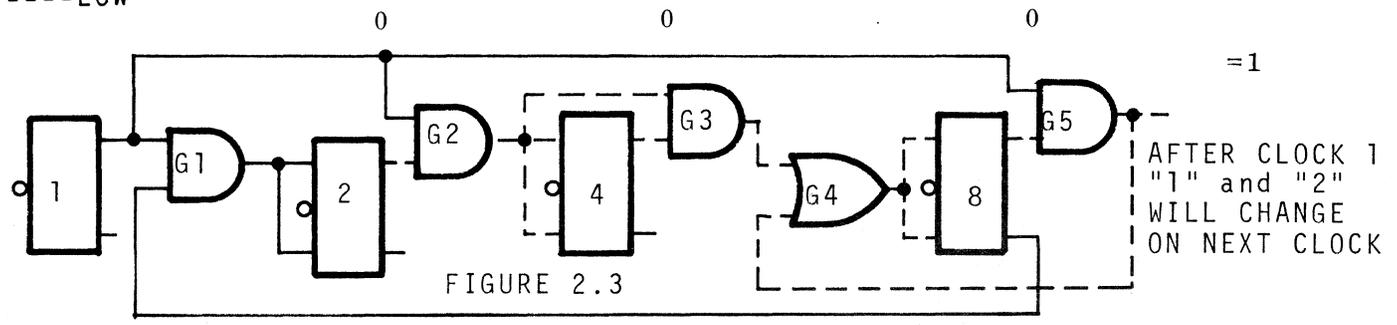
FIGURE 2.4

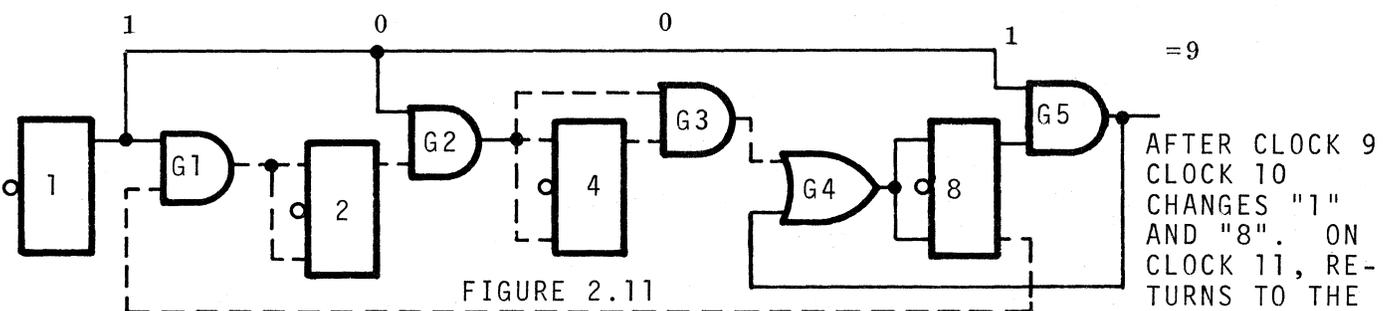
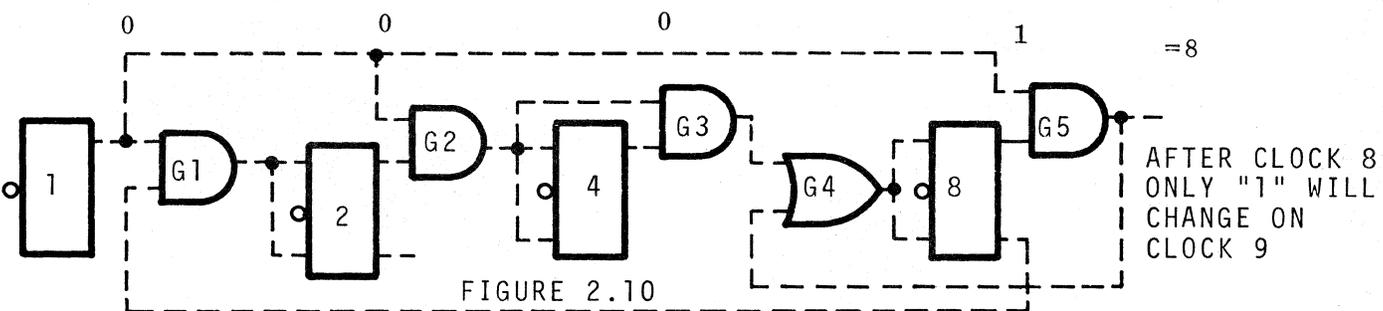
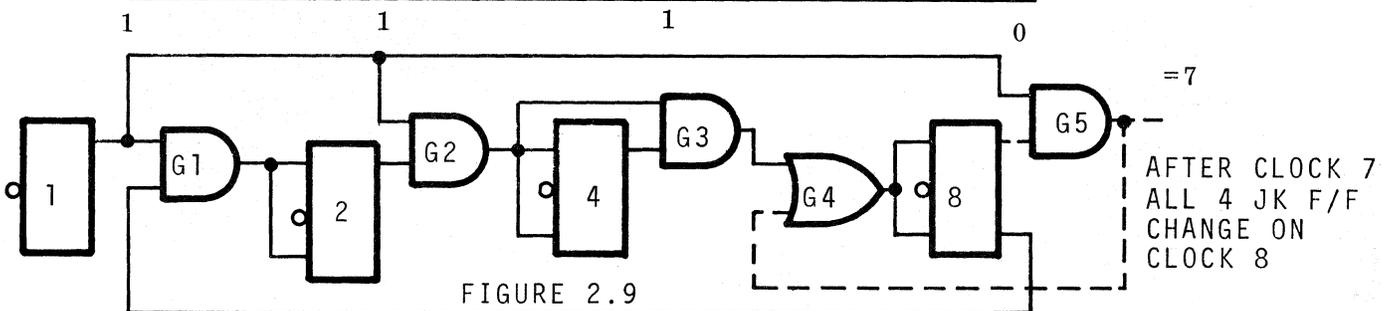
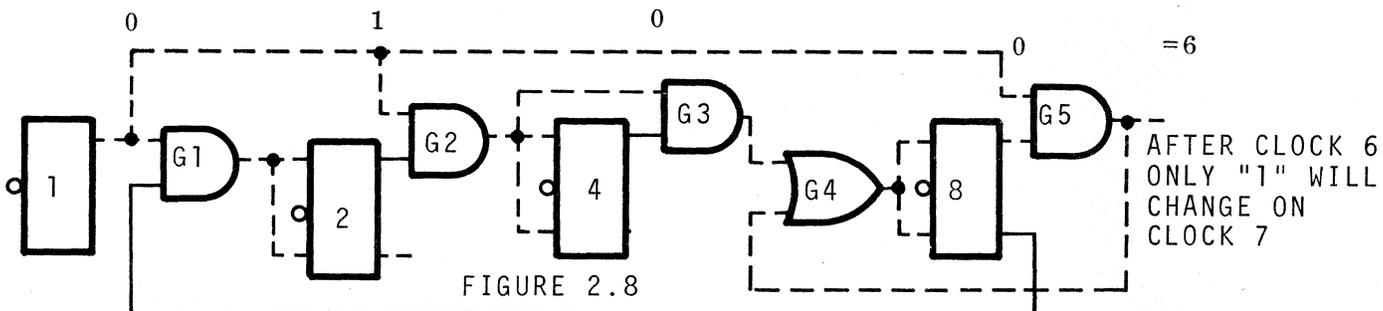
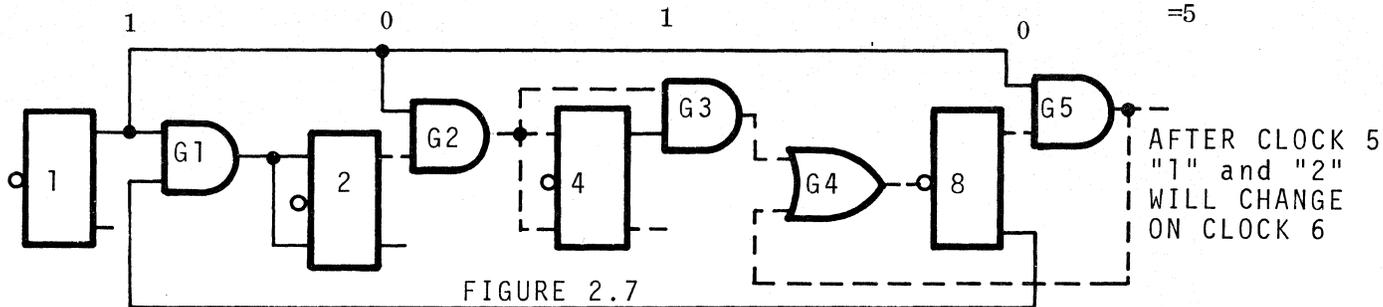


- D. Remember that the JK flip-flop acts as a divide by two only if the J and K inputs are high prior to the clock pulse.
- E. Figures 2.3 through 2.11 describe the state of the counter after each clock pulse.

2.5. This is sometimes called a "permuted" counter

— HIGH
 ---- LOW





- 2.6. The technique used here to develop a divide by ten can also be used to design a counter to divide by any factor.
- A. Briefly, feedback is applied to certain stages of a divide by 2 counter to return it to the initial reset state as soon as the desired count is reached in this example, ten.
- 3.0. Binary Coded Counters.
- 3.1. Another disadvantage of the binary counter is that it has a two finger mentality. A display of 111000010000 (LSD on right), representing 3600 seconds - one hour, can be used internally for computation, but would be impractical as a readout for those of us more familiar with our numbering system of ten discrete digits.
- 3.2. While elaborate decoding networks could be devised, a more frequently used system uses a binary code to describe decimal numbers. Each decimal number is separately coded.
- A. "49" in straight binary is 11001 (LSD on right) or $(2^0)(\bar{2}^1)(\bar{2}^2)(\bar{2}^3)(2^4)(2^5)$ from a 6 stage binary counter.
- B. To display this in decimal an AND GATE could drive the "4" nixie in one column and the "9" nixie in the next.
- C. To discretely display 00 through 49 - 50 decode gates would be required, each with 5 inputs. While logic analysis could probably reduce the number of gates, it is a complex system.
- 3.3. A binary coded decimal simplifies the problem. While several codes are possible, only the 8-4-2-1 will be discussed.

3.4.

Using a four stage counter with proper feedback to make it into a divide by ten, each of the ten digits of the decimal system can be defined.

A.	<u>BINARY</u>	<u>COUNTER STAGES</u>	<u>DECIMAL</u>
	8-4-2-1	1 - 2 - 4 - 8	
	0 0 0 0	$(\bar{2}^0)(\bar{2}^1)(\bar{2}^2)(\bar{2}^3)$	0
	0 0 0 1	$(2^0)(\bar{2}^1)(\bar{2}^2)(\bar{2}^3)$	1
	0 0 1 0	$(\bar{2}^0)(2^1)(\bar{2}^2)(\bar{2}^3)$	2
	0 0 1 1	$(2^0)(2^1)(\bar{2}^2)(\bar{2}^3)$	3
	0 1 0 0	$(\bar{2}^0)(\bar{2}^1)(2^2)(\bar{2}^3)$	4
	0 1 0 1	$(2^0)(\bar{2}^1)(2^2)(\bar{2}^3)$	5
	0 1 1 0	$(\bar{2}^0)(2^1)(2^2)(\bar{2}^3)$	6
	0 1 1 1	$(2^0)(2^1)(2^2)(\bar{2}^3)$	7
	1 0 0 0	$(\bar{2}^0)(\bar{2}^1)(\bar{2}^2)(2^3)$	8
	1 0 0 1	$(2^0)(\bar{2}^1)(\bar{2}^2)(2^3)$	9

- B. The number 49 would then be two coded groups 0100 - 1001.
- C. If the most significant digit, 4 in this case, is not going to exceed 5, then only 3 stage counter is needed in that position. It must return to zero when 5 is reached - a case is the tape timer, where 59 seconds is displayed in the largest number.
- D. A six-stage binary counter will define the numbers $2^6 - 1 = 64 - 1 = 63$.
- E. The binary coded counter requires seven flip-flops, but the decoding process is simpler. A T, I SN7441, to be described later, will convert a 4 wire binary coded decimal to a ten wire decimal output.

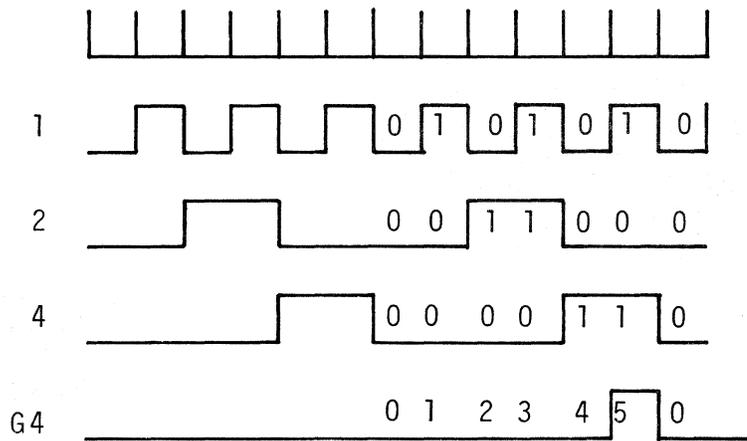
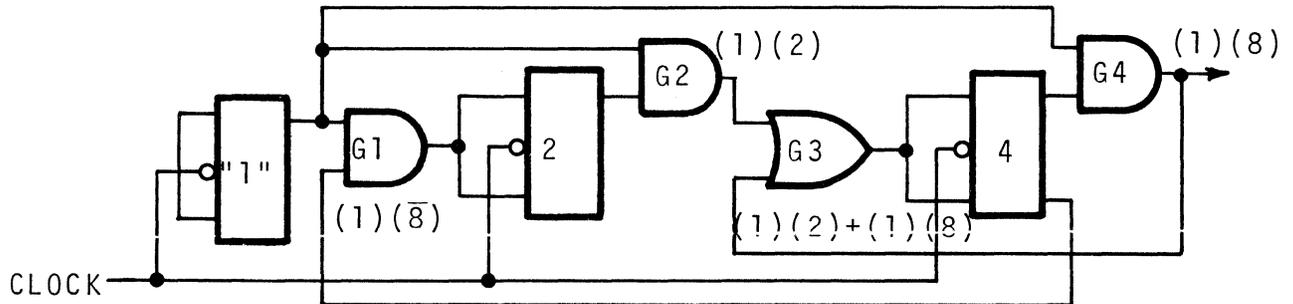
3.5.

The electronic tape timer schematically looks extremely complex; actually it is basically the same circuit repeated for frames, seconds, minutes and hours, where each requires two binary coded counters to describe the decimal numbers.

3.6.

The counter described in section 2.6-C is used for the least significant digit, since it can be anything from "0" to "9".

- 3.6. A. Tens of seconds and tens of minutes use only the digits "0" through 5, so a three stage counter will suffice.



- B. If this were the tens of seconds counter, then the pulse out of G4 would enable the Units of Minutes Counter J and K inputs to advance on the next clock pulse.

4.0. Counting backwards.

4.1. The tape timer must be able to count in reverse the decimal digits decreasing. The outputs to drive the display are always taken from the same side - the Q output.

4.2.

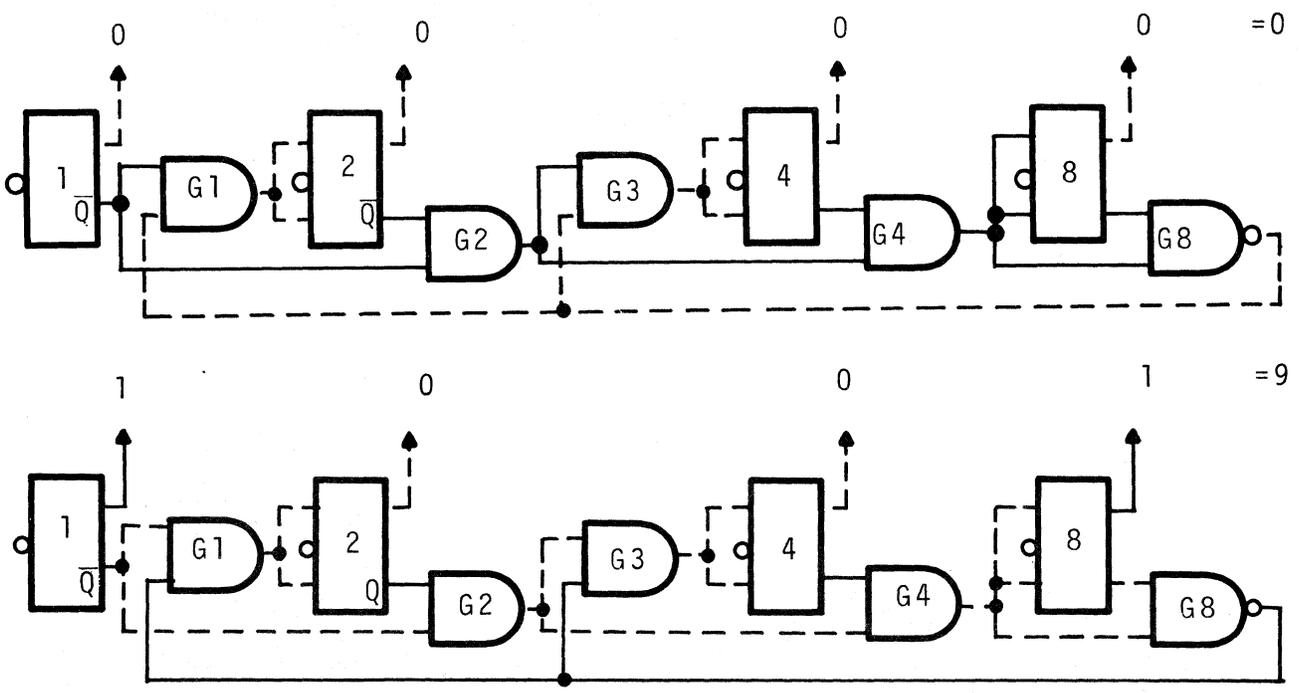
Compare the Q and \bar{Q} outputs of the binary coded counter when counting forward.

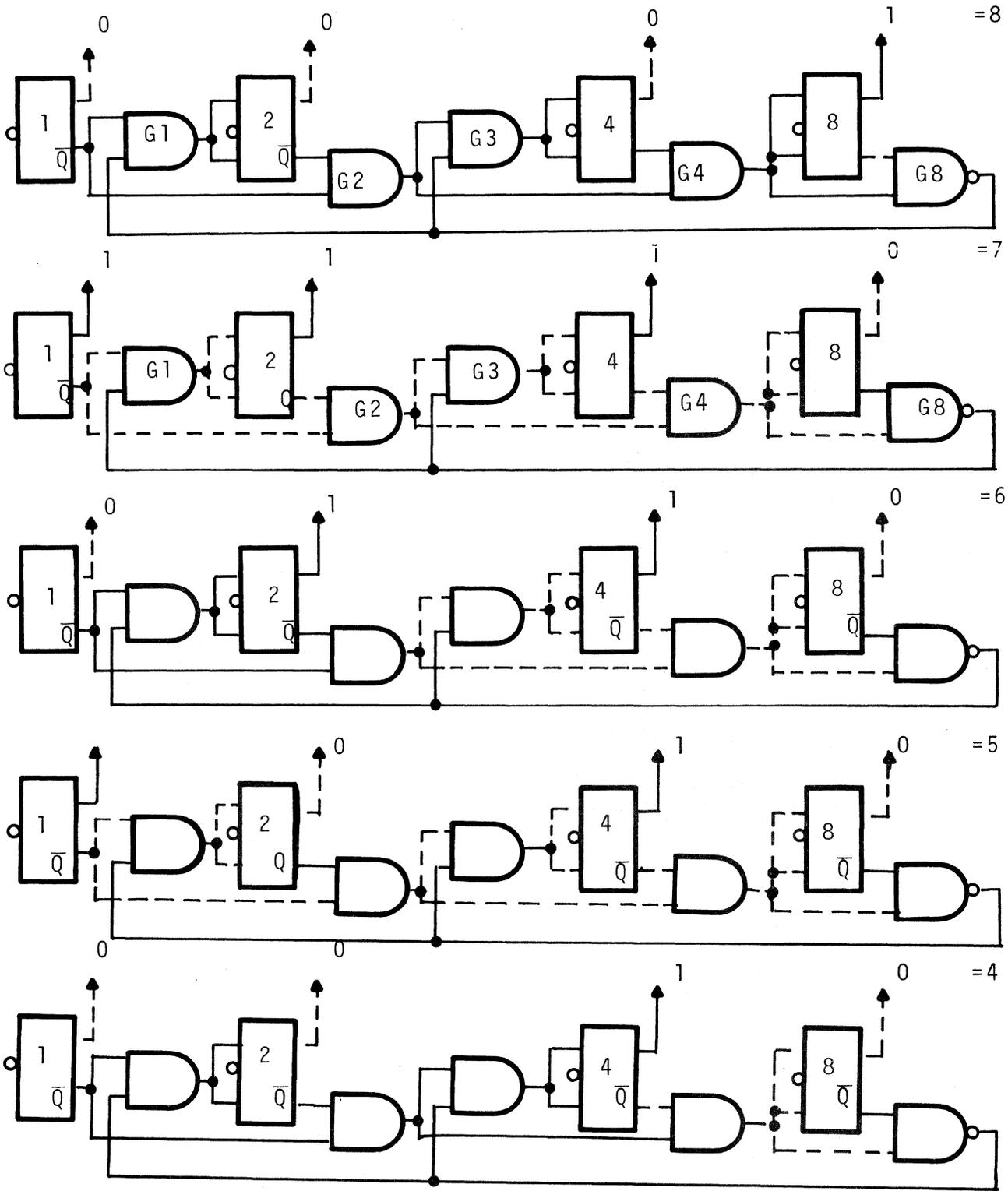
Q	DECIMAL	\bar{Q}	DECIMAL
8 4 2 1		$\bar{8} \bar{4} \bar{2} \bar{1}$	
0 0 0 0	0	1 1 1 1	15
0 0 0 1	1	1 1 1 0	14
0 0 1 0	2	1 1 0 1	13
0 0 1 1	3	1 1 0 0	12
0 1 0 0	4	1 0 1 1	11
0 1 0 1	5	1 0 1 0	10
0 1 1 0	6	1 0 0 1	9
0 1 1 1	7	1 0 0 0	8
1 0 0 0	8	0 1 1 1	7
1 0 0 1	9	0 1 1 0	6
0 0 0 0	0	1 1 1 1	15

4.3.

When counting in reverse, a feedback network utilizing the Q outputs is used which, with succeeding clock pulses progresses 1111, 0110, 0111, (15,6,7) etc. The outputs of the Q side to drive the decoder will progress 0000, 1001, 1000 (0,9,8) etc.

A. The \bar{Q} side is used because the Q sides are used when counting forward. If the counter always counted backwards, then suitable feedback could be arranged for that side.





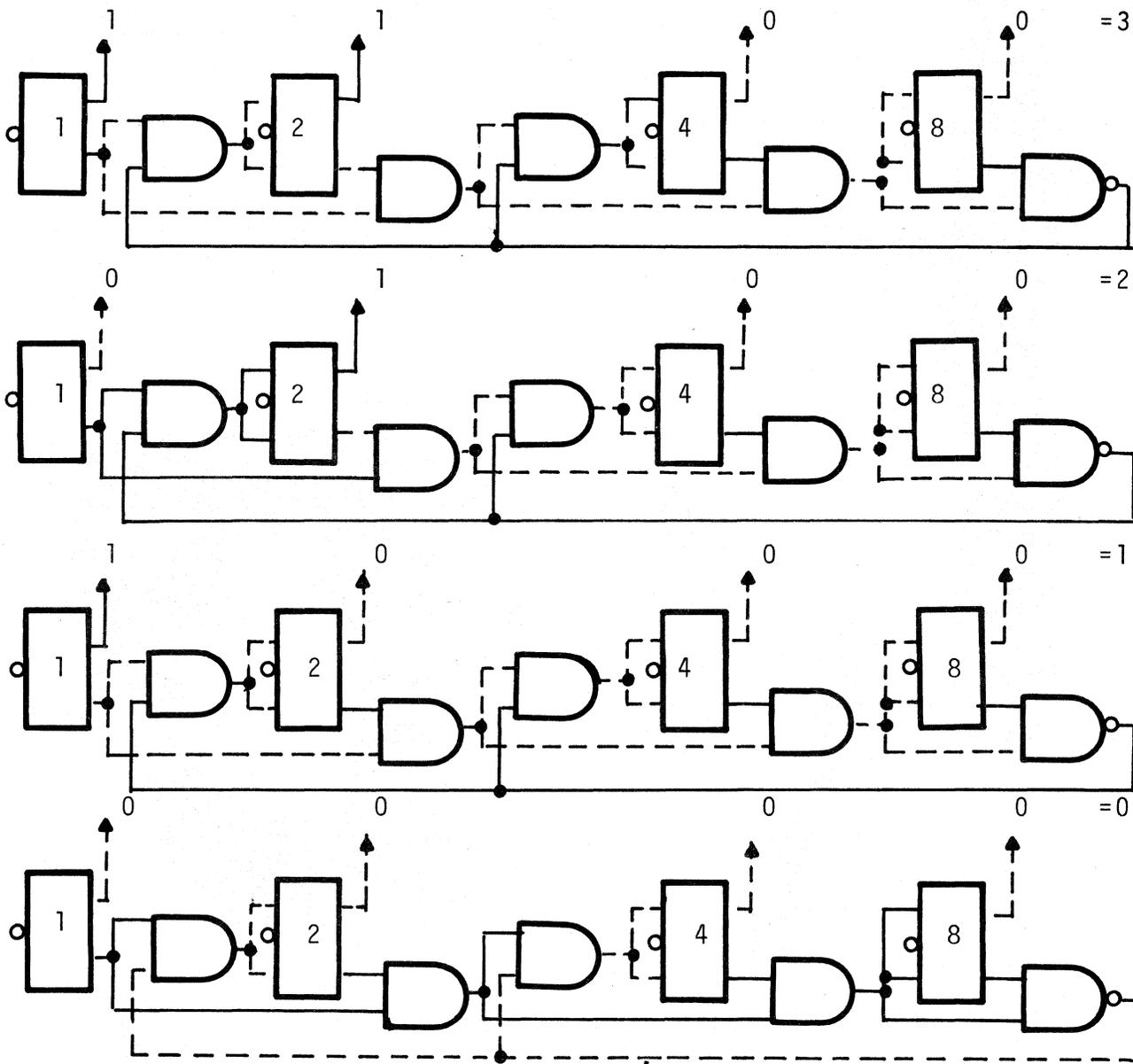
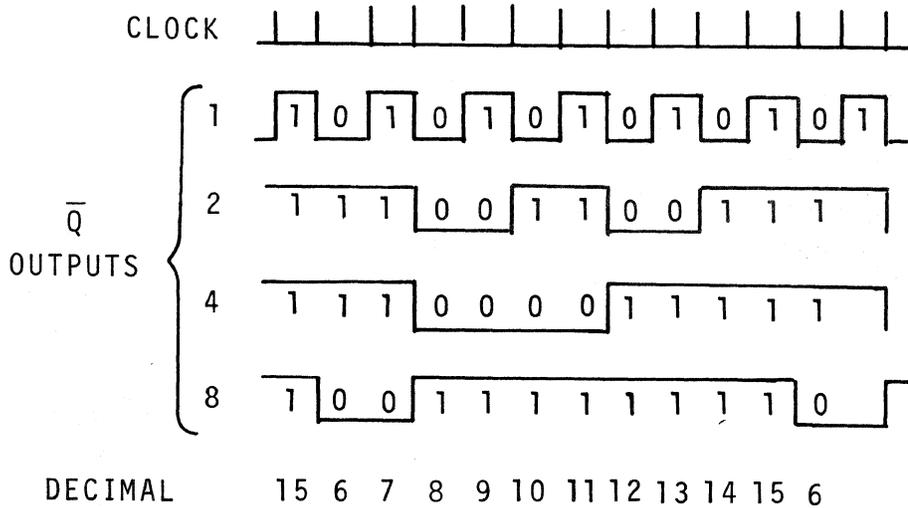
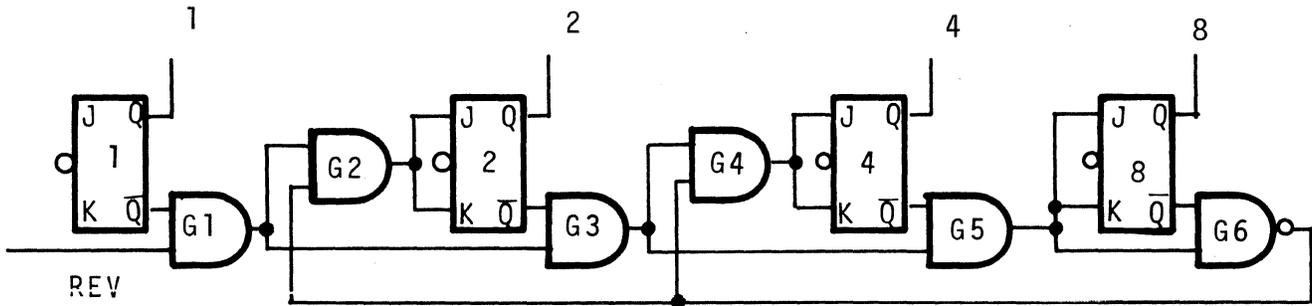


FIGURE 4.1
÷10 COUNTER, IN REVERSE MODE

4.4.



4.5.

The full counter, capable of counting in either direction on command would contain these gates and the feedback for a forward count.

5.0.

BCD to decimal decoder.

5.1.

The Texas Instruments SN7441AN, is a BCD to decimal decoder in single package capable of directly driving gas filled cold-cathode indicator tubes.

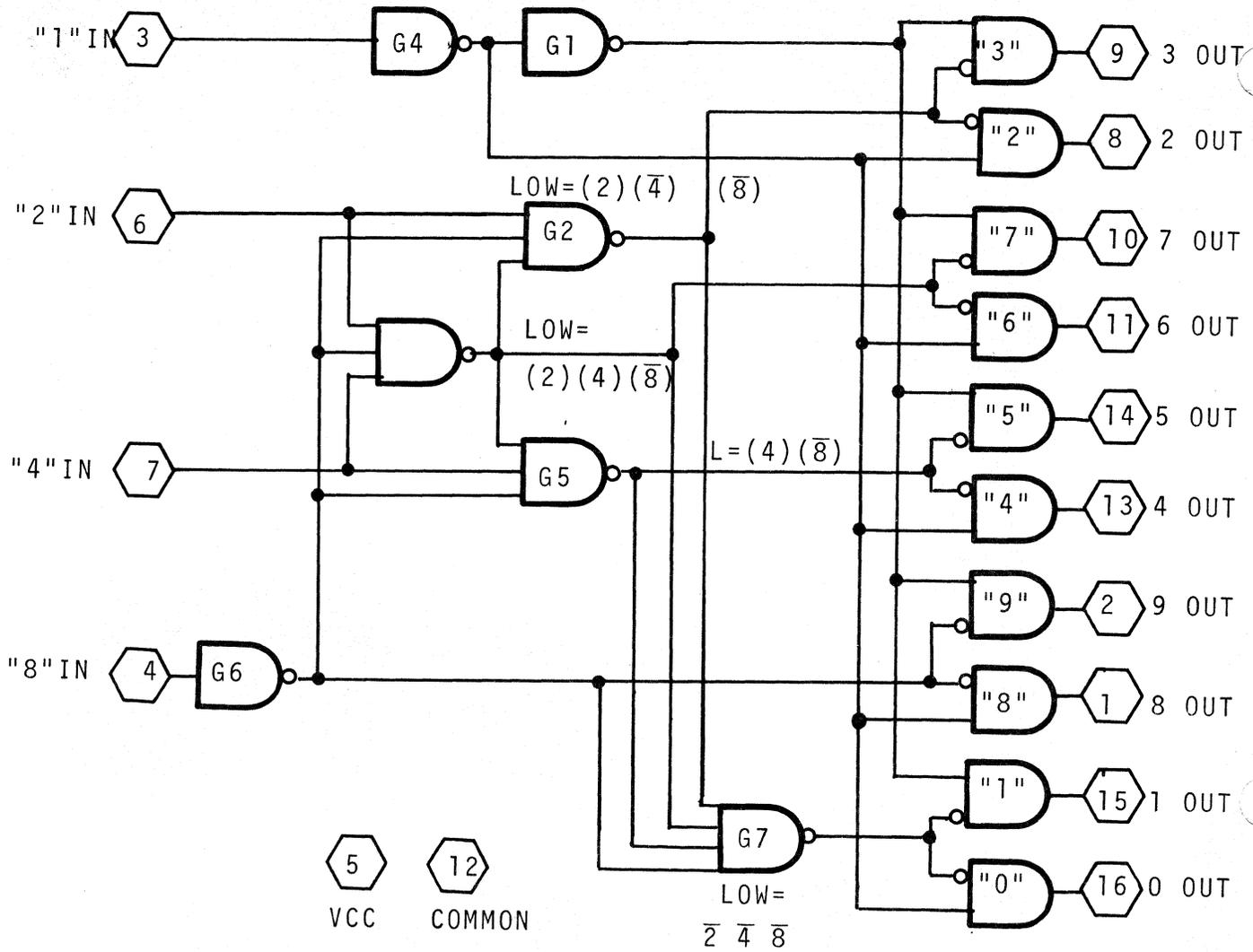


FIGURE 5.1
BCD TO DECIMAL DECODER

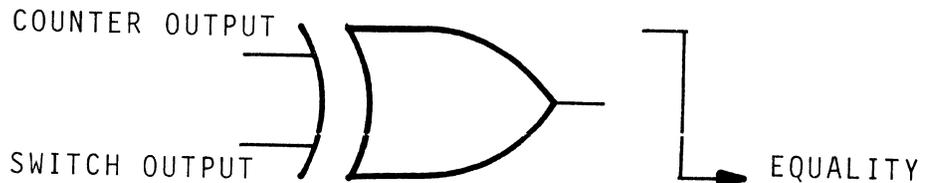
6.0.

Comparison Decoding

6.1.

- Another form of decoding involves comparing the output of two devices and producing an output.
- A. The tape timer external event capability, where switch outputs are compared with the contents of the tape timer or decoded tape address.
 - B. The RA4000 which compares a requested location with tape addresses code.
 - C. The frame counter on the HS100.

6.2. While again schematically it looks quite complicated, it is a simple circuit. The AVR-1 event comparator has some 81 gates, plus inverts and control logic. But the heart of it is an exclusive OR. Twenty-six separate bits in the binary coded "time word" must each be compared with a similar number of outputs from the switches.



- A. The output of an exclusive OR is High only when the inputs are different. If both the inputs are the same, the output is low. So whether searching for a "zero" or "one" in the comparison makes no difference - the output goes low when the input is identical.

7.0. CLEARING or Presetting the Counter.

7.1. Under certain conditions, such as turn on, it may be desirable to Reset the counter to zero, or even hold it at zero for some time.

- A. The clear (C_D) input is used. This input overrides the J K and Clock (C_p) inputs.
- B. If it is held negative, then all \bar{Q} outputs will be high, and Q outputs low - or the display will read zero.

7.2. To PRESET the counter to a previously determined count - either from a random selector such as thumbwheels, or from a fixed predetermined logic, the counter is first cleared using the CD inputs.

- A. Then lows are applied to the set (SD) inputs of those stages it is desired to put in a "1" state.



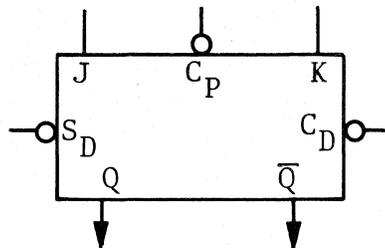
SECTION 6: THE SHIFT REGISTER

REV 2

1. In general, the state of a binary counter stage after a clock pulse depends on the condition of all previous stages prior to the clock pulse.
2. In a shift register, in general, the condition of a particular stage after the clock pulse depends only on the conditions existing at the output of the previous stage prior to the application of the clock pulse.
 - 2.1 The term "shift register" is frequently shortened to "register"
 - a. The clock pulses are usually called "shift pulses".
 - 2.2 The term "ring counter" usually describes a special application of the shift register.
 - 2.3 It can be used as a short term memory or storage device. Information can be retrieved without destruction.
 - 2.4 The register can convert "serial" information into "parallel" data.
 - a. The television tube could be considered a serial to parallel converter. The television signal is transmitted serially - any instant of time contains one bit of information; or a horizontal sync pulse is followed by 1/525th of the total information required to display a complete television frame or picture.
 - b. Because of phosphor persistence, the information presented serially over a period of 33 milliseconds seems to appear instantaneously. Continuous updating with new information produces the illusion of motion.
 - c. The waveform monitor, particularly when operated at a field rate, displays the same information in its serial format.
 - 2.5 The register can also convert parallel information into a serial format.
 - a. The television camera converts the scene in front of the lens into the serial television signal required for transmission.

- 2.6 As a memory device, the shift register may accept information in parallel form, hold (delay) it, and then transmit it in serial form or parallel. It can also accept serial information and store it, then read it out in either serial or parallel form.
- 2.7 The RA-4000 TIME CODE GENERATOR puts the information from a clock counter into a register in parallel form, then reads it out on to tape in serial form.
- a. The RA-4000 TIME CODE READER takes the serial information coming off of tape, puts it into a register; then the parallel outputs of the register drive a binary to decimal decoder and displays the output on a nixie readout.

3. Review of the J-K Flip-Flop



- 3.1 If both J and K are HIGH, the F/F acts as a divide by two whenever both J and K are high and the Clock Pulse shifts positive to negative.
- a. In the counter application J and K were tied together.
- b. If J and K are separately controlled, the Q follows J on the clock pulse transition.
- c. S_D and C_D override any other inputs.

3.2 TRUTH TABLE, typical J-K Flip-Flop

(Q_{n+1} is time after clock pulse has made plus-minus change)

	J	K	S_D	C_D	Q	Q_{n+1}	\bar{Q}	\bar{Q}_{n+1}
PRESET,	ANY	STATE	LOW	LOW	HIGH	HIGH	HIGH	HIGH (N.D.)
RESET, PARALLEL DATA INPUT	ANY	STATE	HIGH	LOW	LOW	HIGH	HIGH	HIGH
	ANY	STATE	LOW	HIGH	HIGH	HIGH	LOW	LOW
BINARY OR BCD COUNTER DIVIDE BY 2	HIGH	HIGH	HIGH	HIGH	HIGH	LOW	LOW	HIGH
	HIGH	HIGH	HIGH	HIGH	LOW	HIGH	HIGH	LOW
INHIBIT (STORE)	LOW	LOW	HIGH	HIGH	LOW	LOW	HIGH	HIGH
	LOW	LOW	HIGH	HIGH	HIGH	HIGH	LOW	LOW
SHIFT REGISTER OPERATION SERIAL	HIGH	LOW	HIGH	HIGH	LOW	HIGH	HIGH	LOW
	HIGH	LOW	HIGH	HIGH	HIGH	HIGH	LOW	LOW
	LOW	HIGH	HIGH	HIGH	HIGH	LOW	LOW	HIGH
	LOW	HIGH	HIGH	HIGH	LOW	LOW	HIGH	HIGH

3.3 The state of J and K must be established prior to the clock pulse transition from positive to negative.

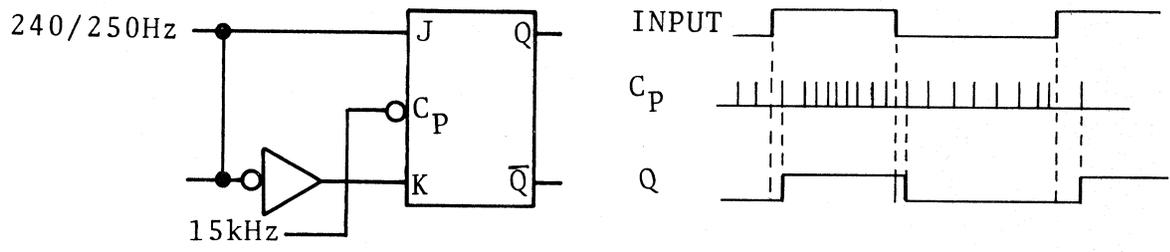
4. The J-K as a memory or delay device.

4.1 In the AVR-1 Control System, a flip/flop is set by hitting the PLAY button momentarily. The flip/flop remains set until STOP or SHUTTLE is commanded, remembering that the machine is to be in PLAY.

4.2 Another application, which is in a sense a one stage shift register is the retiming application. It is frequently necessary to retime a random event to a precise oscillator, or to external information.

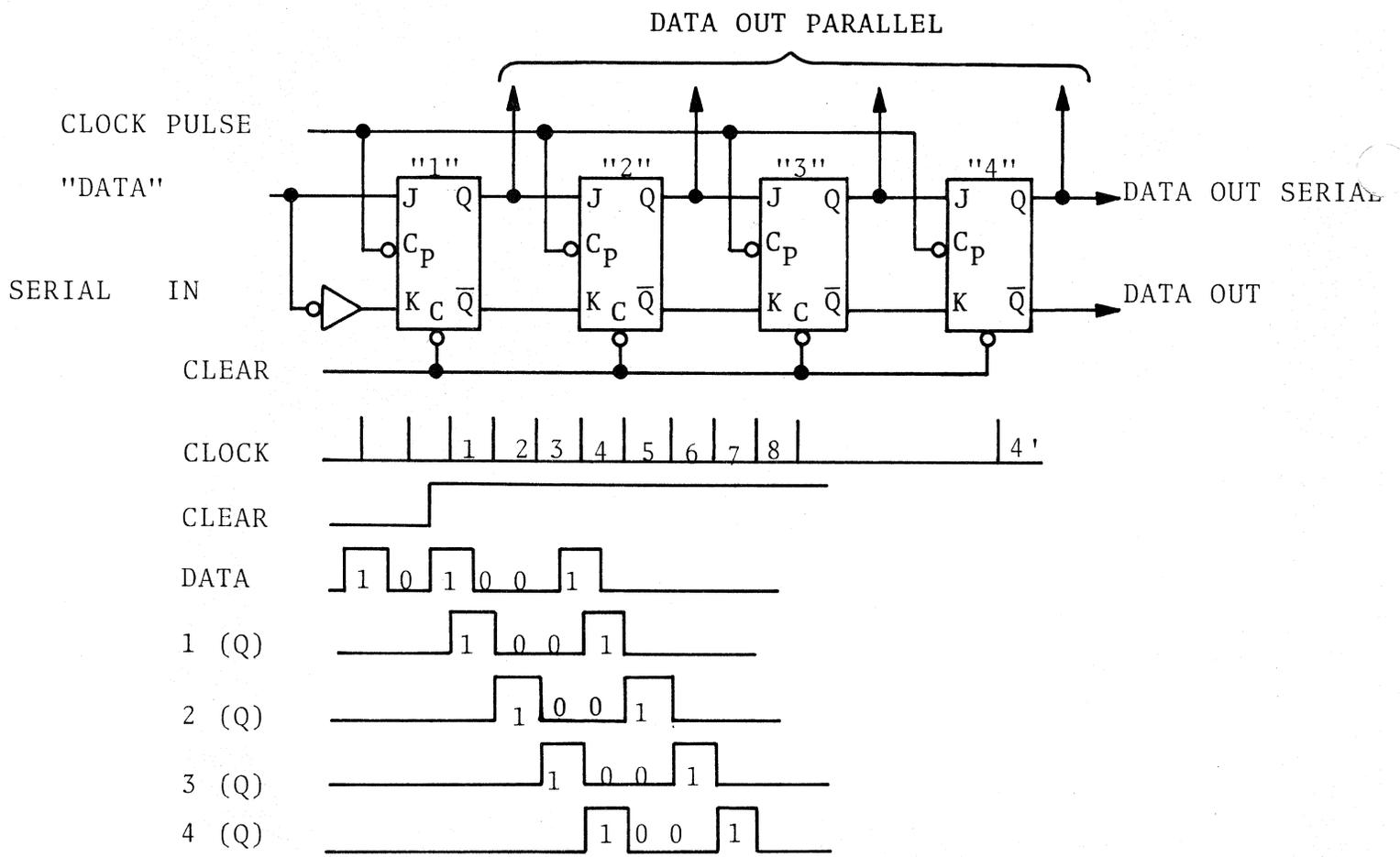
a. In the HS-100, the slow motion rate is determined by a free running oscillator operating at approximately the desired frame rate. The oscillator is retimed using vertical sync.

b. In the AVR-1 Blanking Switcher, the Headwheel tachometer signal is retimed so that each of its transitions occur during horizontal blanking - or each edge of the 240/250 Hz signal is delayed up to 64 microseconds.

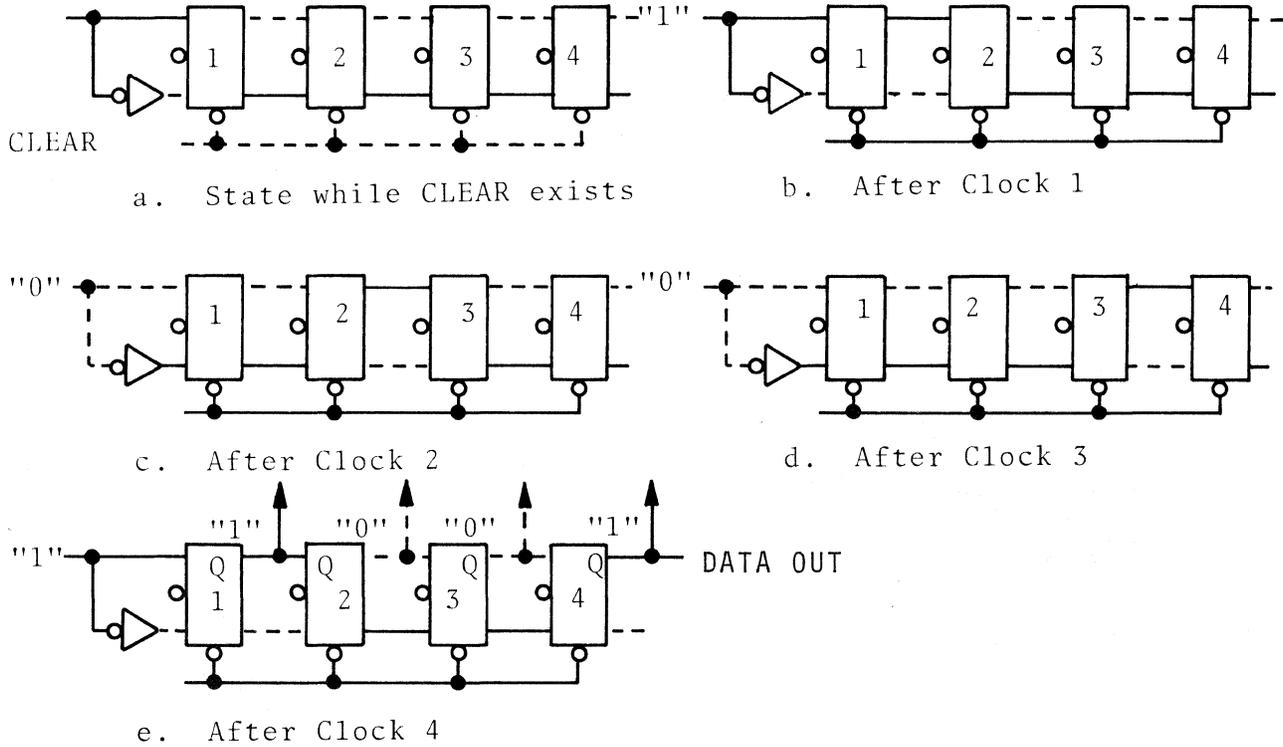


c. The above techniques are also referred to as "Time Quantizing".

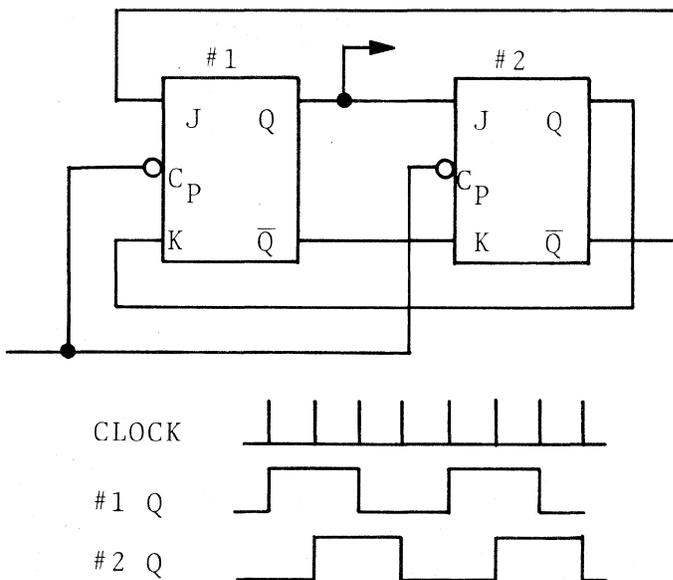
5. The basic shift register.



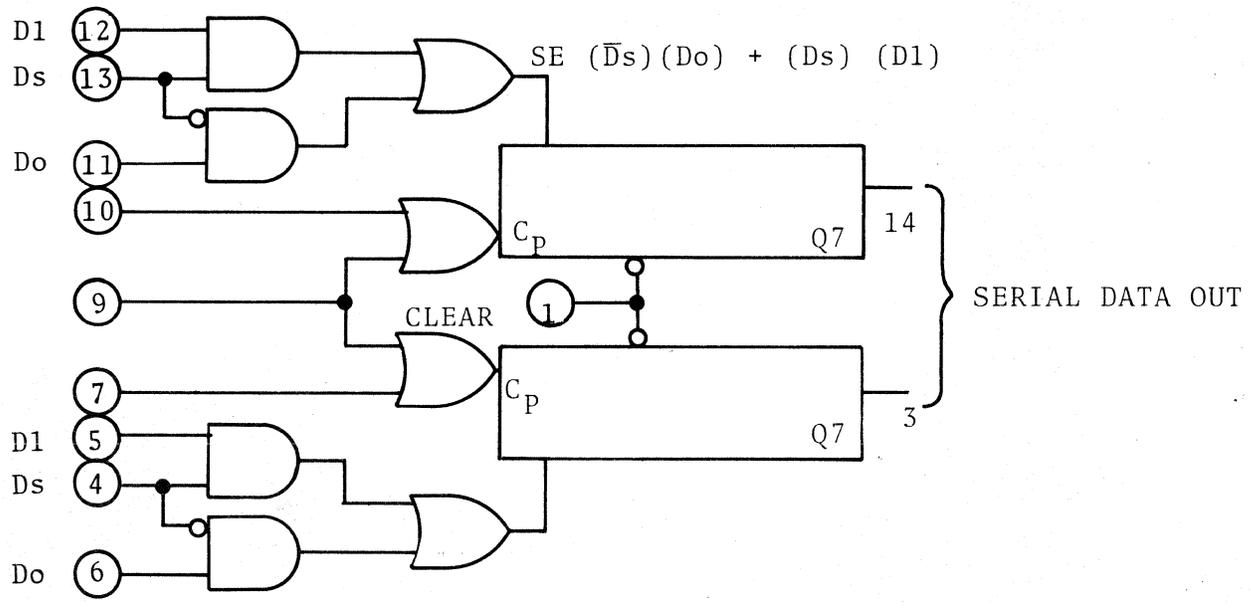
5.1 Step by Step Operation



6. To produce a two phase output with 90° between phases:

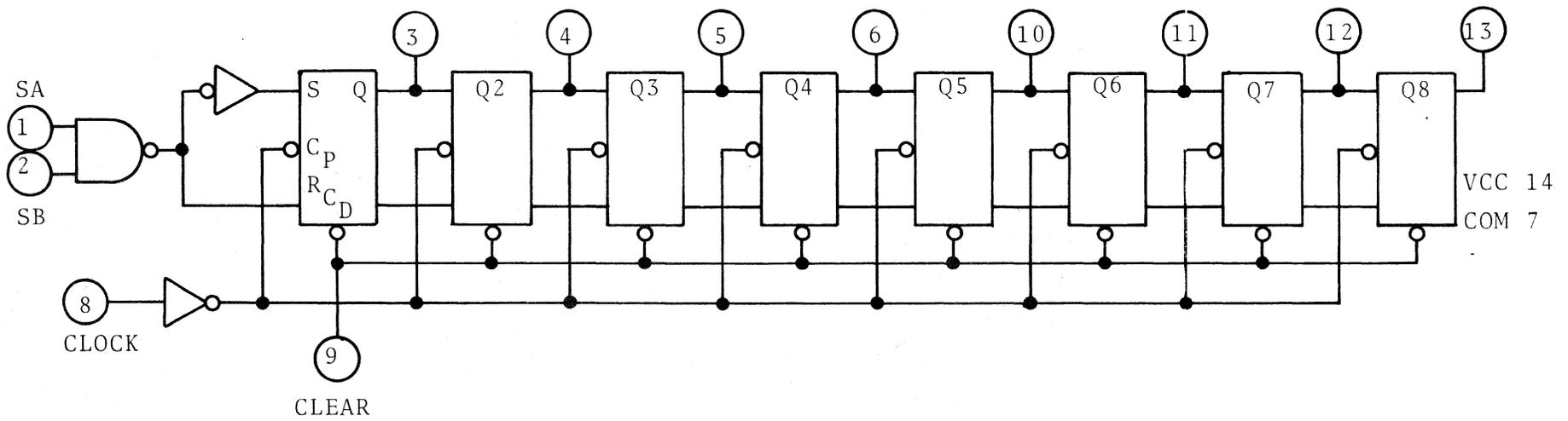


- 7. The Shift Register is available as an integrated circuit
- 7.1 Fairchild FC9328 Dual 8 Bit Shift Register, AMPEX P/N 586-303.



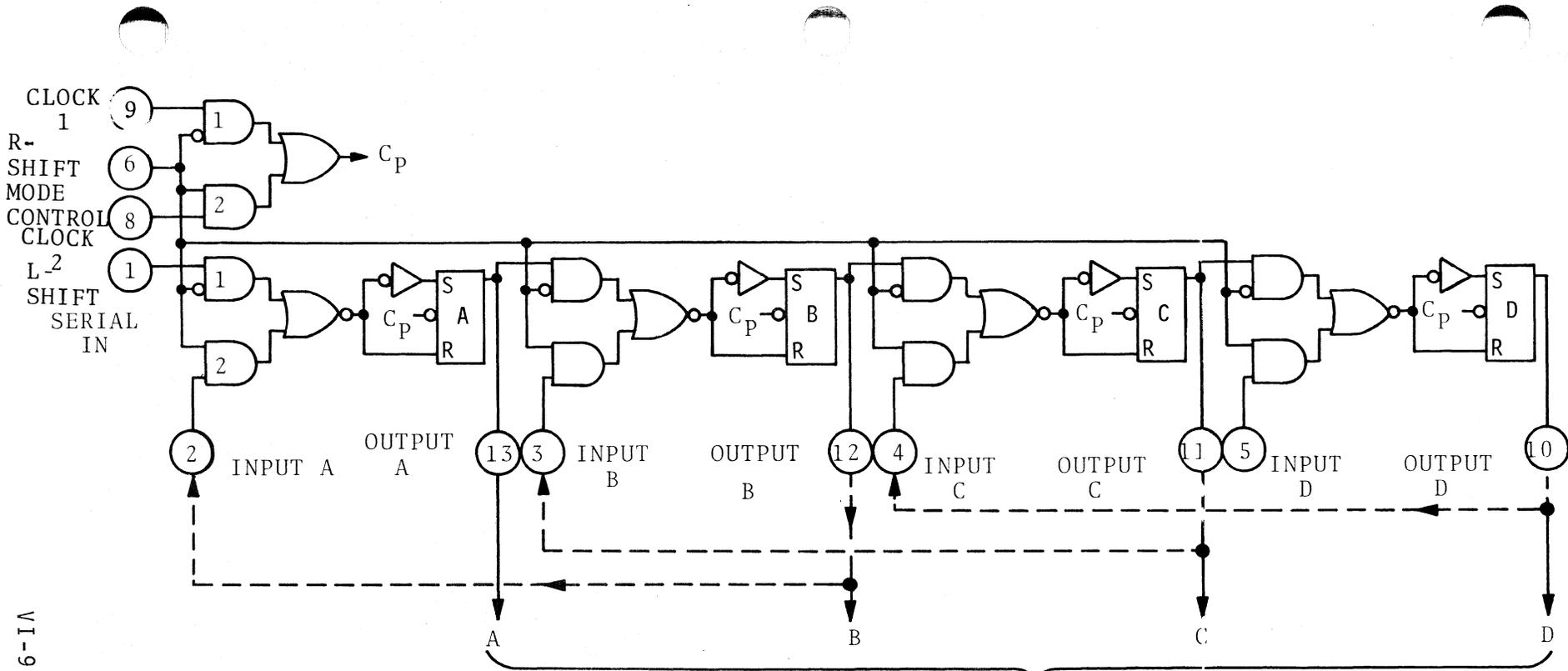
- a. Used in MK IV EDITOR (AVR-1)
- b. Includes two eight stage shift registers
- c. Serial in, serial out capability only
- d. The register shifts on the positive transition of the clock.
- e. A negative on the CLEAR holds all stages reset, and Q7 (the eighth stage) is low

7.2 The National Semiconductor DM8870, AMPEX P/N 586-450 serial in/parallel out register contain a single 8 bit register.



VI-7

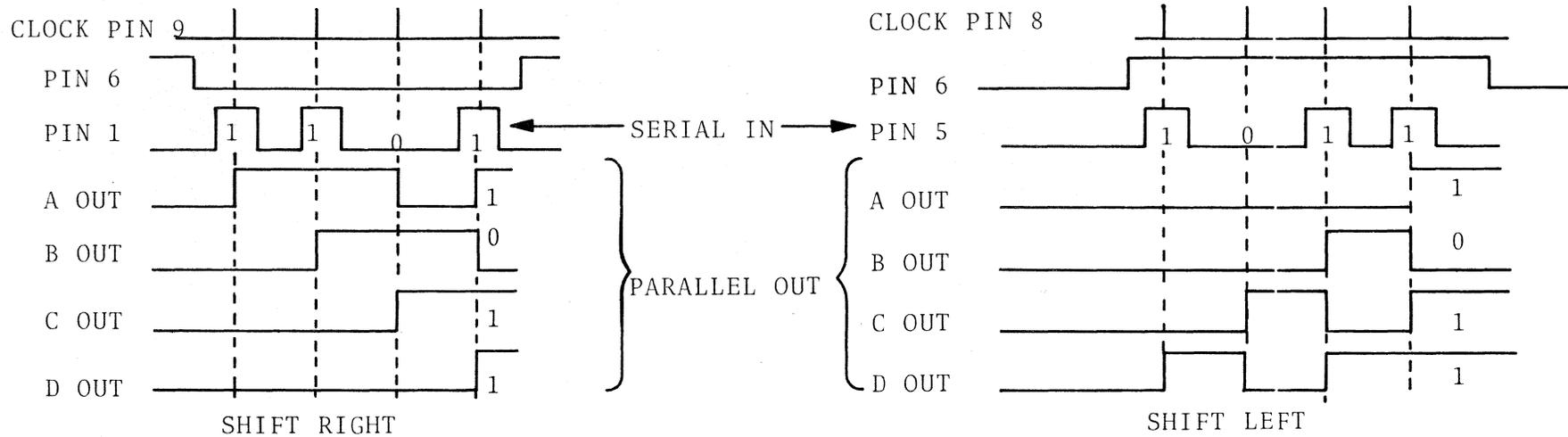
- a. Clocks on positive transition.
- b. Negative on CLEAR holds through Q8 low.
- c. Q8 output is equivalent to Q7 output on the Fairchild 9328.
- d. Used in MK IV EDITOR (AVR-1)



6-11

PARALLEL OUTPUTS

Texas Instruments SN 5495/7495 Four Bit right shift-left shift register
 NOTE: External connections required for shift left operation shown with dashed lines



8. The Texas Instruments SN 5495/7495 Four Bit Right Shift - Left Shift Register is a very flexible unit.
 - a. Serial in, serial or parallel out
 - b. Data may be shifted in from two directions
 - c. Clocked parallel input
 - d. Data transfer occurs when the clock pulse shifts from a high to a low.
- 8.1 In RA-4000 operation the format of serial time code information recovered from magnetic tape depends on the direction of tape travel - the most significant bits may be deserialize and standardize the format.
- 8.2 The SN7495 may be operated in a shift right-shift left mode to accomplish this.
 - a. If a low is applied to pin 6 "MODE CONTROL" , the number 1 gate are enabled. Clock pulses at pin 9 "CLOCK 1 RIGHT SHIFT" will move data appearing at pin 1 "SERIAL IN" to be shifted to the right, A-B-C-D.
- 8.3 If it is connected as shown, with the output of each stage connected to the input of the previous stage, data can be entered serially in the opposite direction.
 - a. With a high on pin 6 "MODE CONTROL" the Number 2 gates are enabled.
 - b. Clock pulses are applied to pin 8 "CLOCK 2 LEFT SHIFT" and serial data to pin 5 "INPUT D". The data is shifted on successive clock pulses from "D" to "C" to "B" to "A".
 - c. Outputs "A", "B", "C", and "D" provide parallel information
- 8.4 The register may also be connected for parallel input operation. Pins 2,3,4, and 5 are parallel inputs where the information will be entered when pin 6 "MODE CONTROL" is high, and a clock pulse occurs at pin 8 "CLOCK 2" input.
 - a. The data could then be shifted out serially by causing "MODE CONTROL" input to go low, and applying clock pulses to pin 9. Serial data would appear at pin 10, "OUTPUT D".

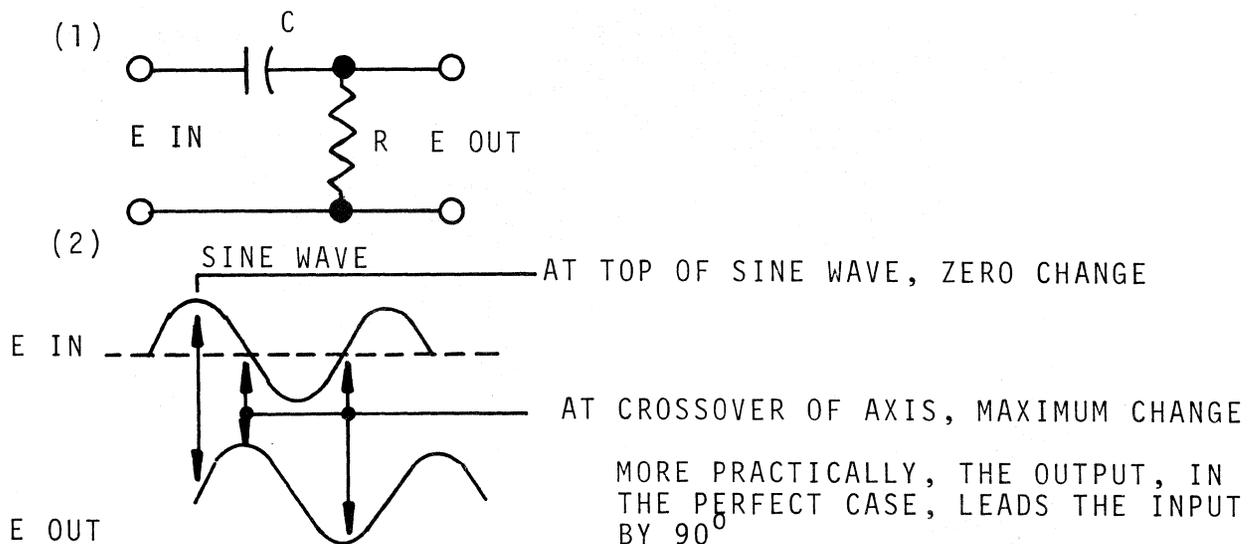
- b. If the serial data out at Pin 10 (OUTPUT "D") were to be fed back to serial data input pin 1 (SERIAL IN) the register would be in ring type configuration such that the same data could be continuously shifted and read out in parallel and/or serial format.
- c. In actual operation all of these modes and their distinct operations could be controlled by proper "time share" gating.

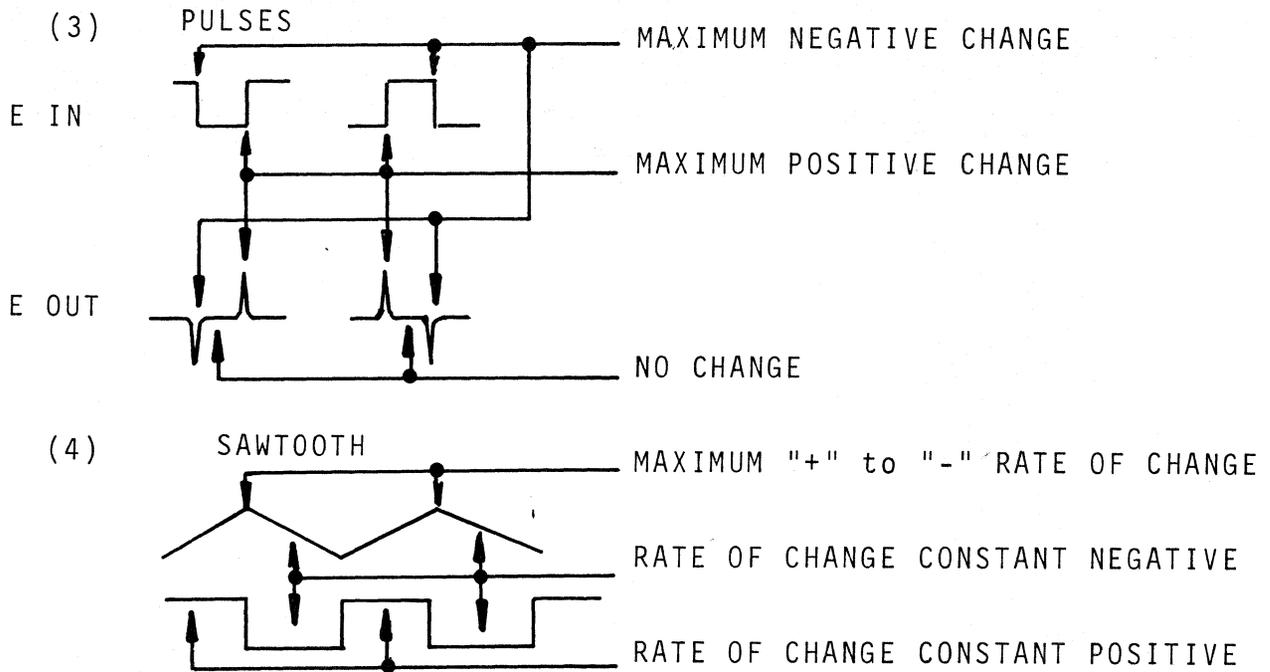


SECTION 7: PULSE CIRCUITS

NOTE: Some of us tend to forget the basic electronic circuits we learned. This series by the AMPEX Training Department is intended primarily as a rapid review and summary. For this section, we suggest you review the section on Resistance/Capacitance time constant concept in your favorite basic text.

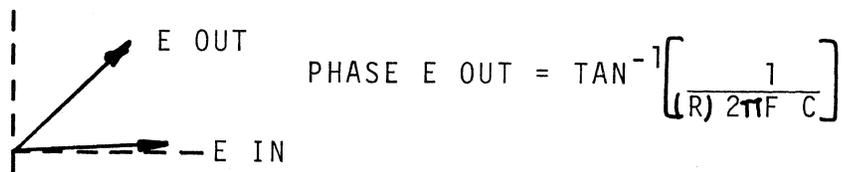
- 1.0. A common requirement in pulse circuits of the narrowing of a wide pulse, or defining the leading and trailing edge of a pulse. Frequently, a large amount of pulse delay is required, without the use of LC type delay lines.
- 1.1. The most frequently seen circuit is some variation of the RC (Resistance/Capacitance) network.
 - A. Some common names for such circuits are "delay"; "boxcar"; "pulse former"; "differentiator".
- 1.2. The term "differentiator" is derived from the calculus
 - A. It defines the process of measuring the rate of change of a waveform.
 - B. By the proper choice of resistance and capacitance, the mathematical process can be electrically simulated.





- 1.2. C. Theoretically differentiation is mathematically perfect if the time constant, equal to $R \times C$, is infinitesimal. Of course under these conditions the output voltage is also infinitesimal. The real value of a practical RC network will determine the amount of phase shift of a sine wave, or the width of the output pulse when a square wave is applied.
- D. It may be more familiar as the grid or base coupling circuit of a resistance coupled amplifier, but with the resistance and capacitance selected so as not to pass low frequencies. It is a high pass filter. "R" and "C" are selected on the basis of the lowest frequency that must be passed.

1.3 The circuit is sometimes used to deliberately introduce a specific amount of phase shift.

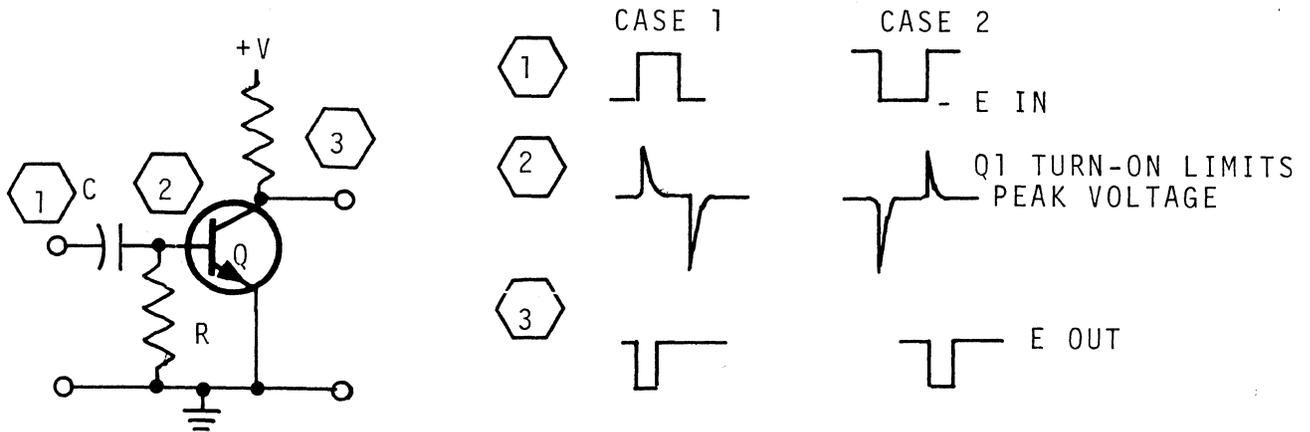


1.4 It is more frequently encountered in circuits requiring sharply defined pulses.

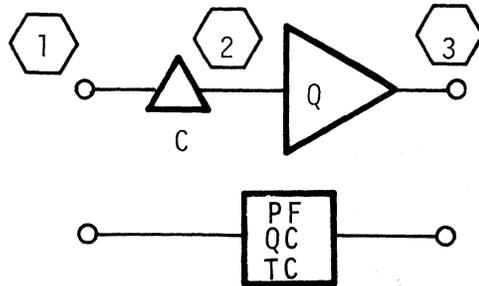
1.5

NPN Circuit.

A.

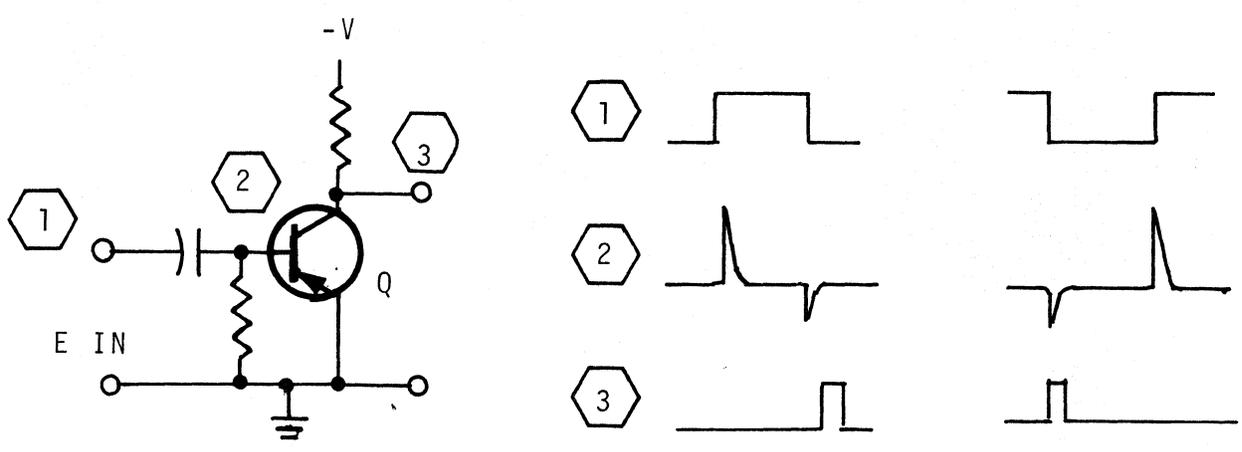


- B. The output pulse width equals approximately $0.7 RC$
- C. AMPEX Training Department block diagrams have used the following symbol:

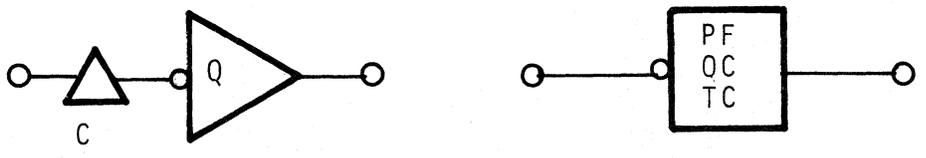


D. Case 2 represents delay.

1.6. A. PNP Circuit



B. Symbols used.

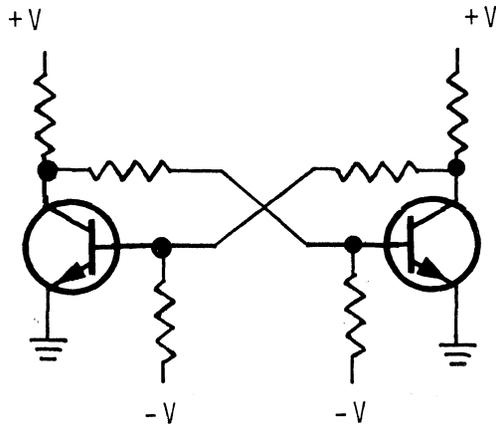


C. On block diagrams, the period of the final pulse is included only when it is important in understanding the circuit.

1.7. When the network is used with integrated circuits ("chips") all or part of the "R" in the RC equation may be internal to the chip, and must be taken into account, when computing the time constant to determine the pulse width. The multiplying factor may be included on the manufacturer's spec sheet.

2.0 THE MONO STABLE MULTIVIBRATOR

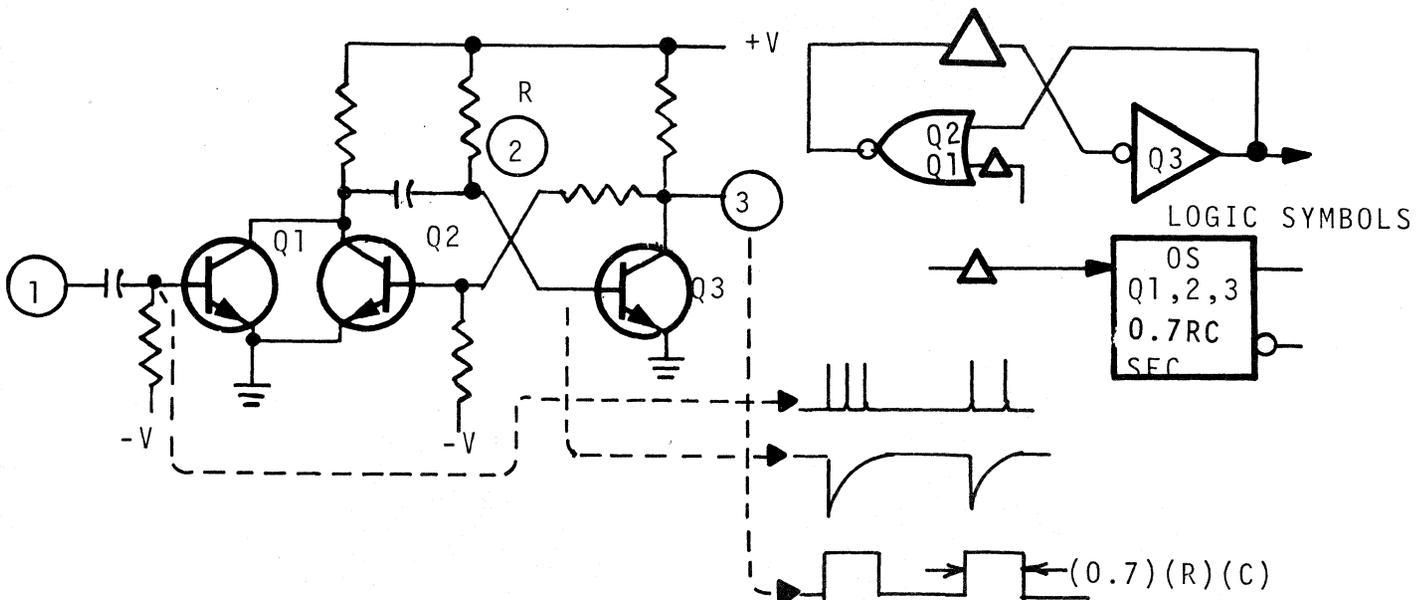
2.1. The flip-flop, or bi-stable multivibrator is basically two saturation type amplifiers with 100% feedback. It normally assumes one of two states indefinitely until triggered into a reverse condition. It is discussed in Section III.



2.2. If one of the feedback paths is changed to an RC differentiator network, the result is: a circuit designated:

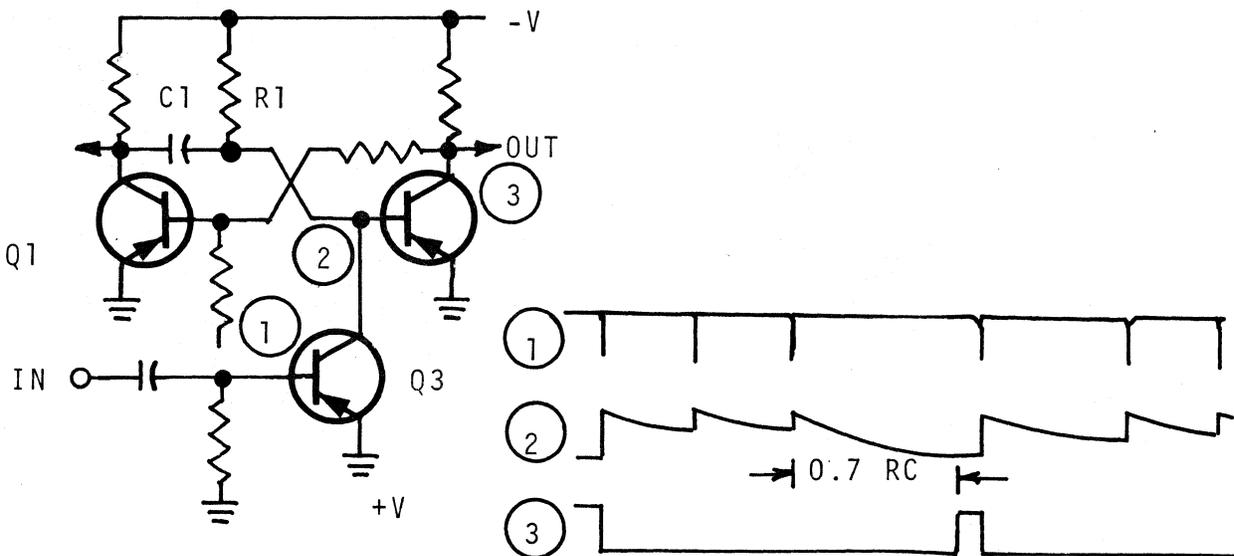
- A. ONE SHOT (O.S.)
- B. Single Shot (SS)
- C. Delay multivibrator, or delay multi
- D. Monostable multivibrator, or simply "mono"

2.4. Collector Driven One Shot



- A. In the stable state Q3 is conducting, and the output 3 is close to ground.
- B. Q1/Q2 are off, and their collectors are positive
- C. A positive trigger on the base of Q1 send its collector to ward ground
- D. The negative shift is differentiated by RC, and the pulse turns off Q3.
- E. The feedback from the collector of Q3 to the base of Q2 keeps it conducting for $0.7 RC$.
- F. Any input pulses during the active time of the one shot are ignored-the one shot in this case is non-retriggerable.
- G. Output may be taken from either side

- 2.5. If R is made variable, then the period of the one-shot can be adjusted.
- A. The "R" may include a transistor as the charging source, with some type of error signal controlling the current and therefore the period of the one shot
- 2.6. The trigger may be brought in on the base of Q2.
- 2.7. Retriggerable One-Shot

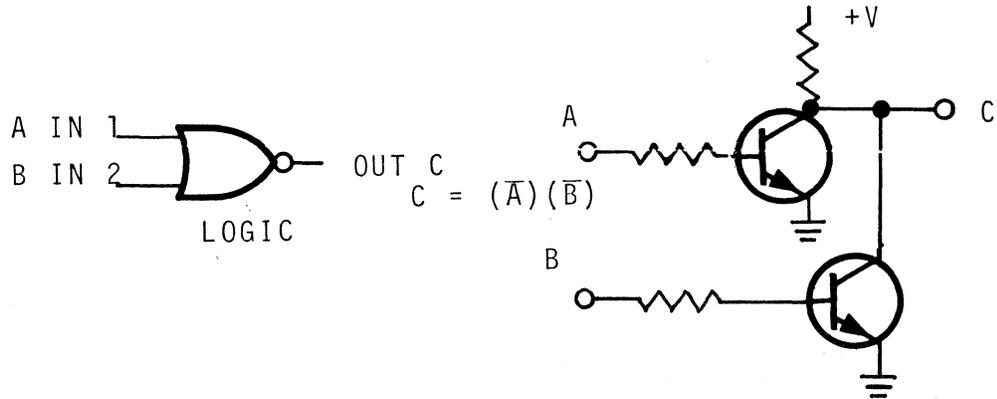


- A. Input pulse turns on Q3 and charges C, positive, and turning off Q2.
- B. C1 starts charging through R1 until sufficiently negative to turn on Q2.
- C. If the period ($0.7RC$) is longer than the period between input pulses, the one shot does not revert to its stable state.

- D. A missing pulse will allow it to revert to a stable state.
- E. It is sometimes called a pulse to dc converter.

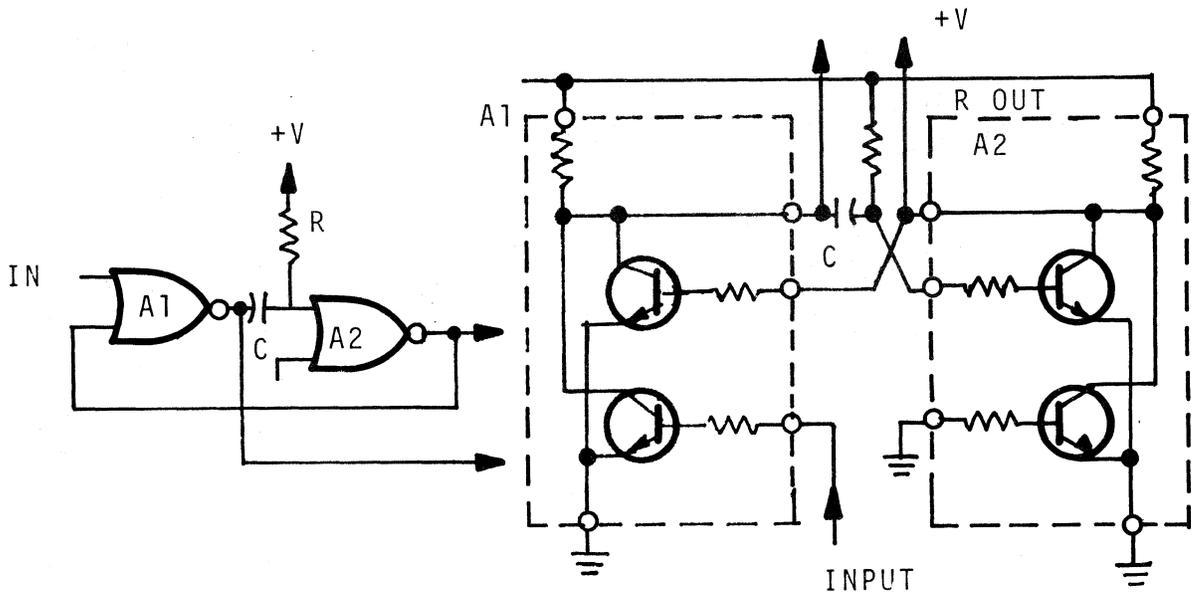
3.0. Nand/Nor Integrated Circuit One Shots

3.1. The FC 914 NOR Gate may be used as a one-shot



- A. If either input goes high, the output will swing low. If both inputs are low (near ground) the output will be high (near supply voltage)

3.2. One-Shot

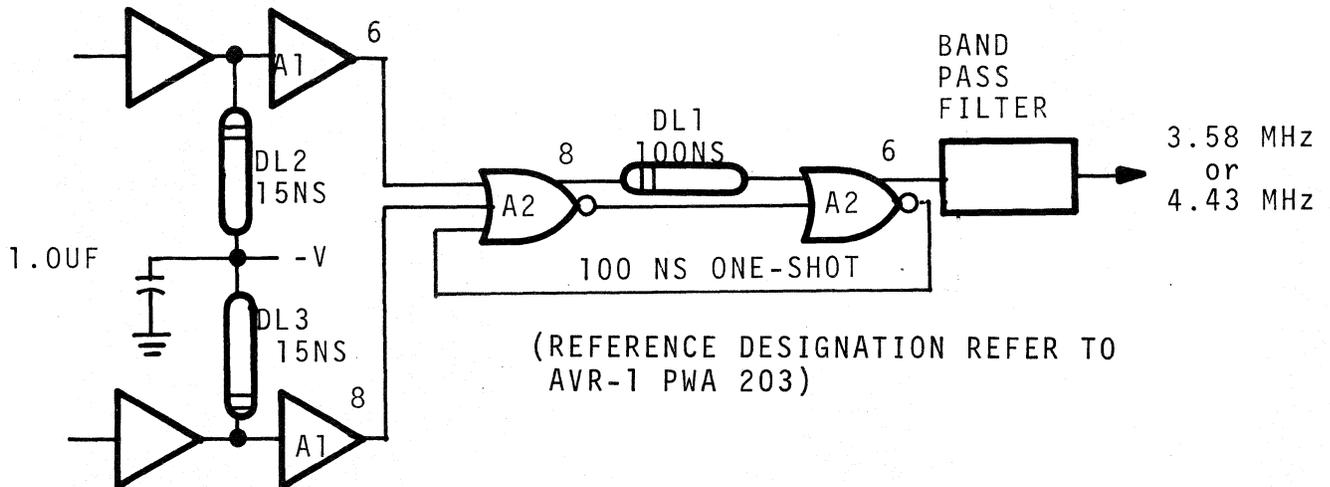


- A. The period of the One-Shot, using the FC914 is $0.33RC$.
- B. This will vary depending on the integrated circuit used, and its internal resistance.
- C. In general, it may be used in the same way as a one-shot using discrete components.
- D. Diode-Transistor logic circuits may also be used in a similar way.

3.3.

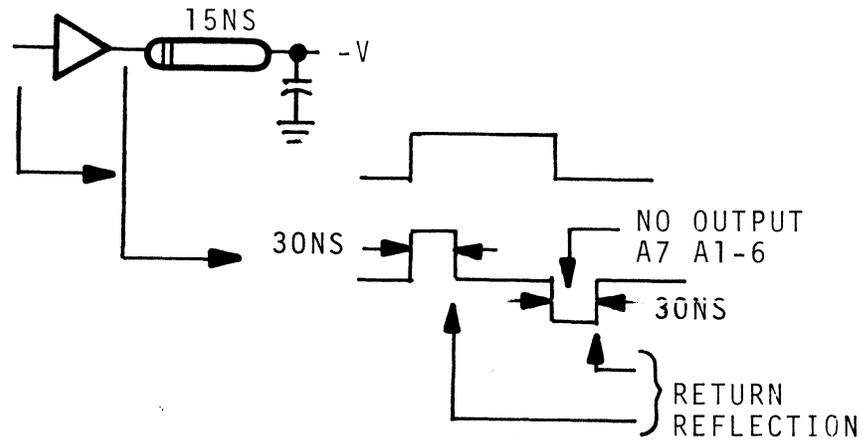
The system subcarrier phase shifter in the Universal Colortec (Model 1012) and the Reference Subcarrier Processor #1, Module 203 in the AVR-1 employ a different version of the differentiator. Delay lines are used instead of resistance and capacitance.

- A. The logic units are Motorola MECL 1204L, where a high is between ground and -0.7 volts, and a low is on the order of minus 2 volts.

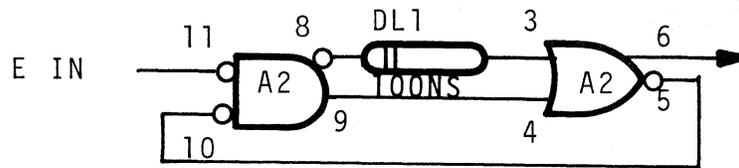


- B. Input pulses are at 1/2 television signal color subcarrier rate. The preceding circuit discussed later varies the timing of the positive transitions of the input pulse.
- C. DL2 and DL3 appear as shorted delay lines due to the 1.0ufd capacitor and the input frequency of 1.79 or 2.2 MHz.

C. Because of the bias at the end of the delay line A1-6 and A1-8 see only the positive going reflections.

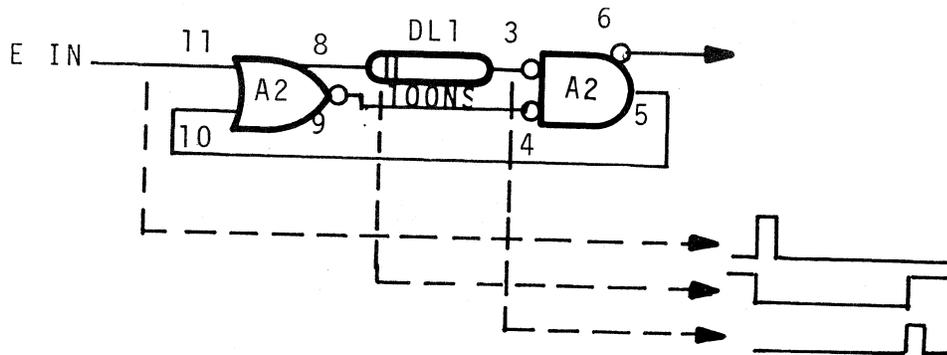


D. Initial (Stable) State



- Ein low
- A2 pin 10 also low
- Pin A2-9 high, keeping A2-8 low, and maintaining the stable state.

E. Unstable (triggered state)

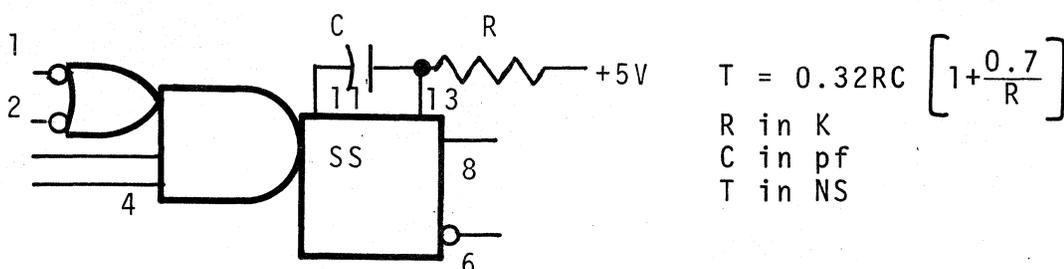


- Pin 11 goes high for 30 nano seconds
- Pin 8 goes high, but it is 100 nano-seconds later before A2-3 goes high
- The low out of A2-9 keeps A2-5 high, keeping A2-9 low.
- 100 nano seconds later A2-3 goes high, A2-5 goes low, and the one shot reverts to its stable state.

4.0. Integrated Circuit One-Shot

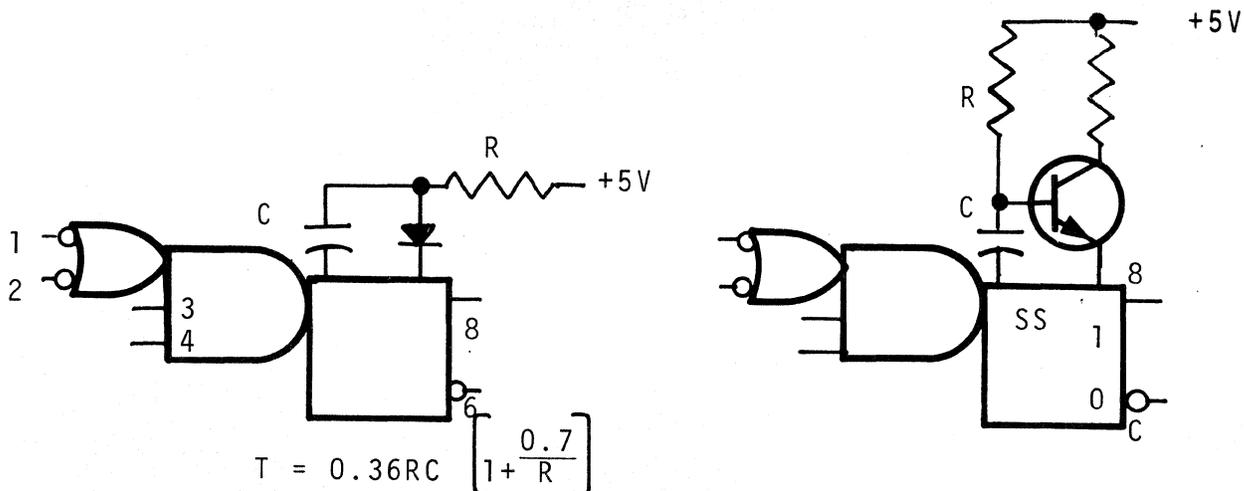
4.1. The Fairchild 9601 Retriggerable Monostable Multivibrator is a single "chip" that performs the one-shot function.

- A. An external resistor and capacitor determine the period.
- B. Inputs are d.c. coupled so that triggering is independent of input transition time.



C. For trouble shooting purposes, $T=0.32RC$ is adequate.

4.2. When electrolytic capacitors are used, Fairchild recommends a diode or transistor across the capacitor to prevent reverse voltage across it.



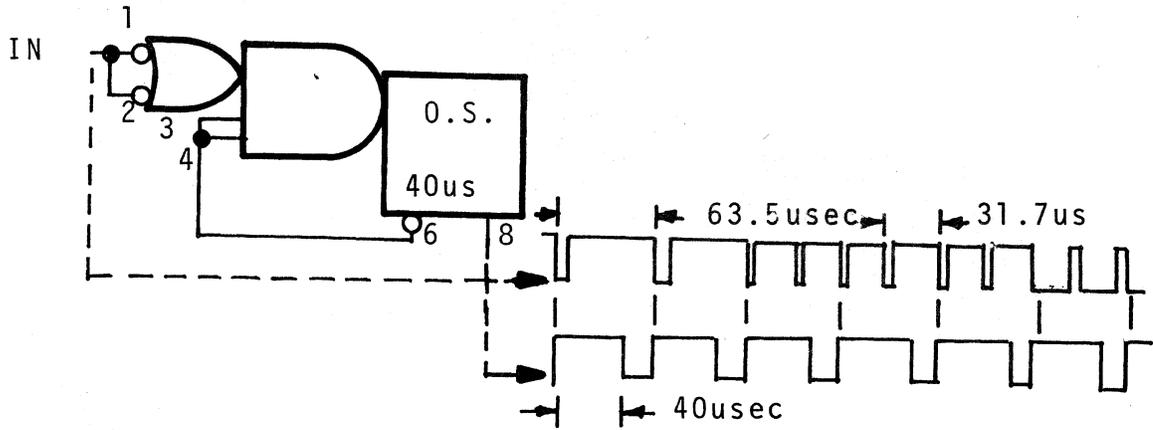
4.3.

General considerations for the FC9601

- A. If 3 and 4 are not used they are tied to +5V
 - B. If NOR inputs 1 and 2 are not used they are tied to ground.
 - C. If the period is longer than the input trigger period, the one-shot will continuously retrigger and the output will be a dc level.
- NOTE: Retriggering will not occur if the retrigger pulse comes within 0.32 CX RX (.7RC) after the initial trigger.

4.4.

Non-retriggerable connections.

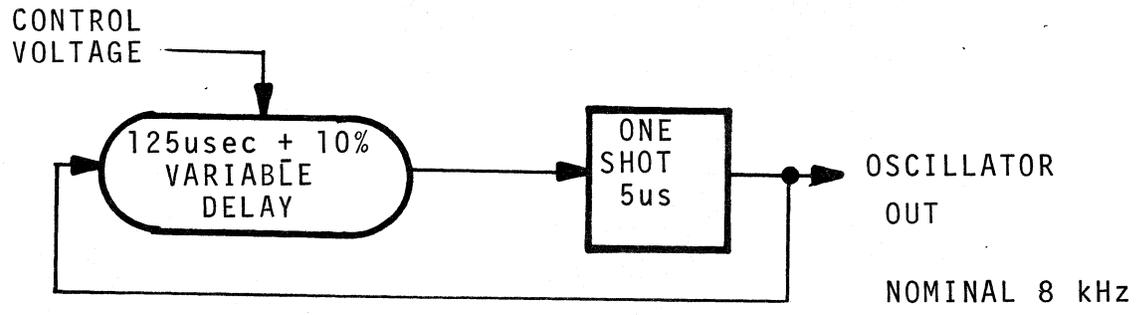


- A. This circuit is used in the Video Tape Recorder to identify the horizontal component of composite sync. It eliminates the half line information during the 7½ (625) or 9 line (525) vertical interval.

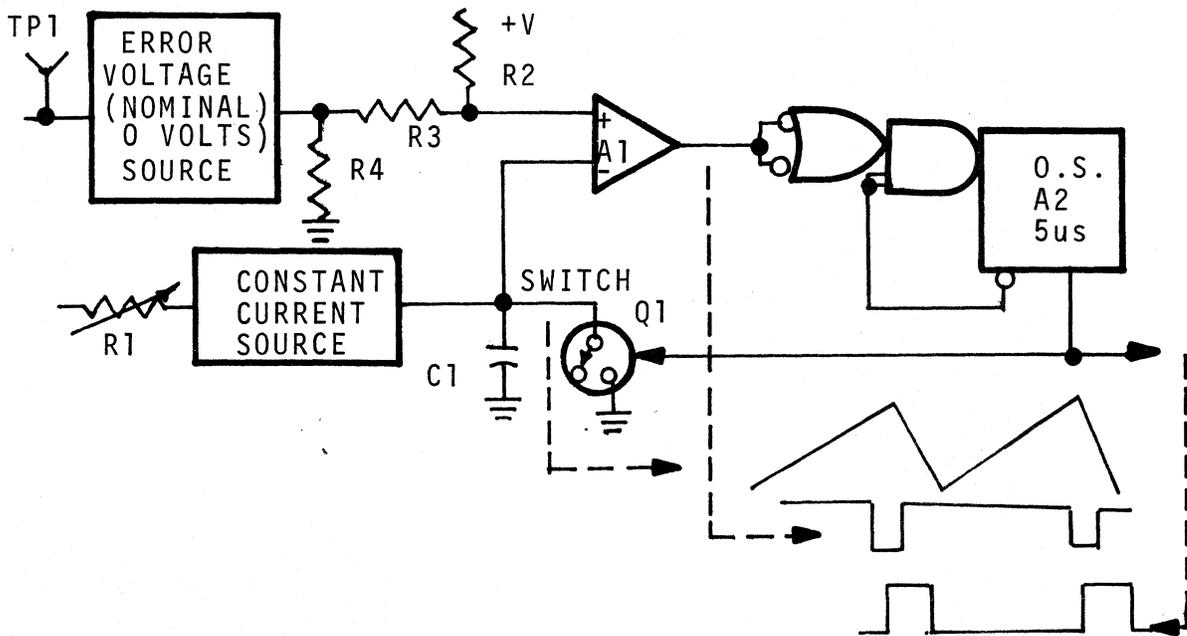
4.5.

Voltage Controlled Oscillator

- A. Basic circuit-the output of the one-shot is delayed by a period equal to the nominal period of the desired frequency, then retriggers the one-shot.



B. Typical Logic Circuit.

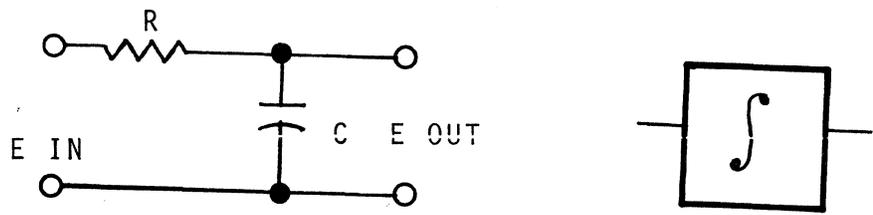


4 6.

- Circuit operation of voltage controlled oscillator.
- A 5 usec pulse from the one shot turns on transistor switch Q1, discharging C1 to ground.
 - At the end of the pulse, the capacitor starts charging at a linear rate, the ramp rate determined by the constant current source.
 - the constant current source may be adjustable (R1)
 - it would probably be adjusted so that the error voltage (TP1) equalled zero volts under some special control condition.
 - The positive going ramp (in the AVR-1 it is usually +5V) is the minus input to voltage comparator A1.
 - The positive input to the comparator is determined by voltage divider R2, R3, and R4.
 - when the error voltage is zero, then the divider is R2, and R3.
 - this determines the nominal operating frequency
 - When the ramp voltage exceeds the reference voltage, the output of A1 swings negative, triggering one-shot A2.
 - The action repeats.

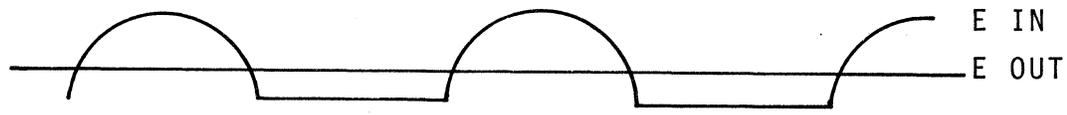
5.0. A less frequently encountered circuit is the "Integrator"-essentially the complement of the differentiator. Again the term is derived from the calculus.

5.1. The process is simulated electrically by a resistance capacitance network.

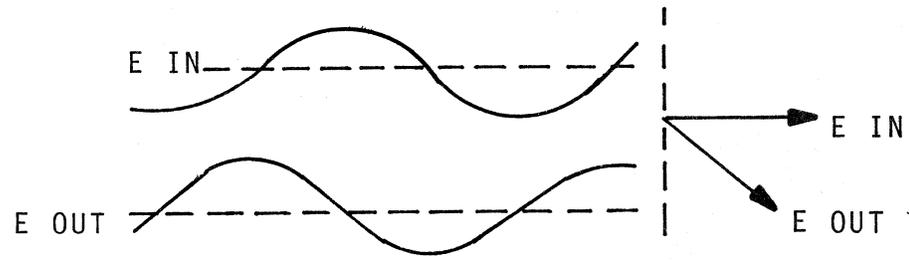


A. Again, the integration approaches mathematical perfection if R and C are infinite in value. Of course E out becomes infinitesimal.

5.2. It can also be considered a low pass filter-and the circuit is probably most familiar as an RC Power Supply Filter.

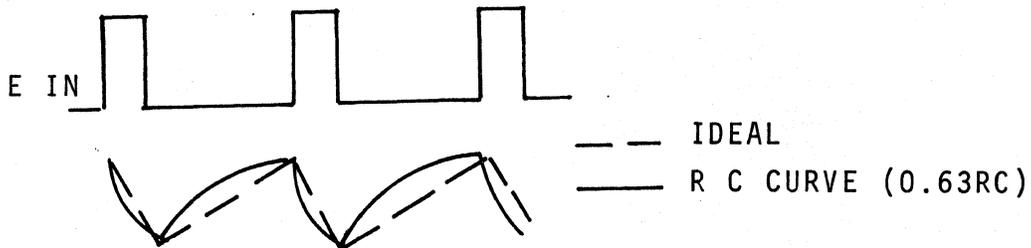


5.3. In the case of sine wave, a phase shift results.



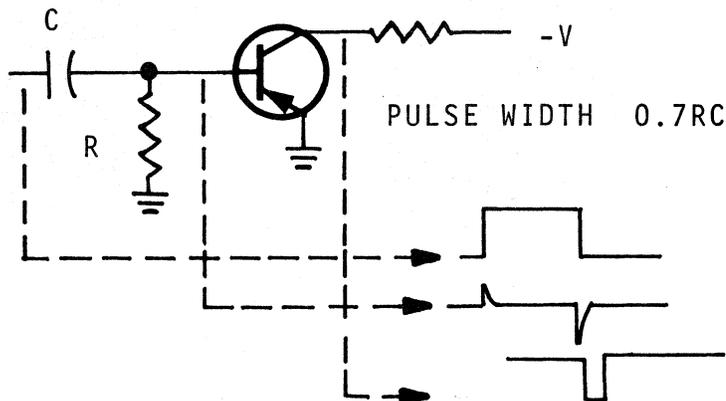
$$\phi \leq \tan^{-1} \left[-\frac{1}{(R)(2\pi F)(C)} \right]$$

5.4. The ramp generator is another example

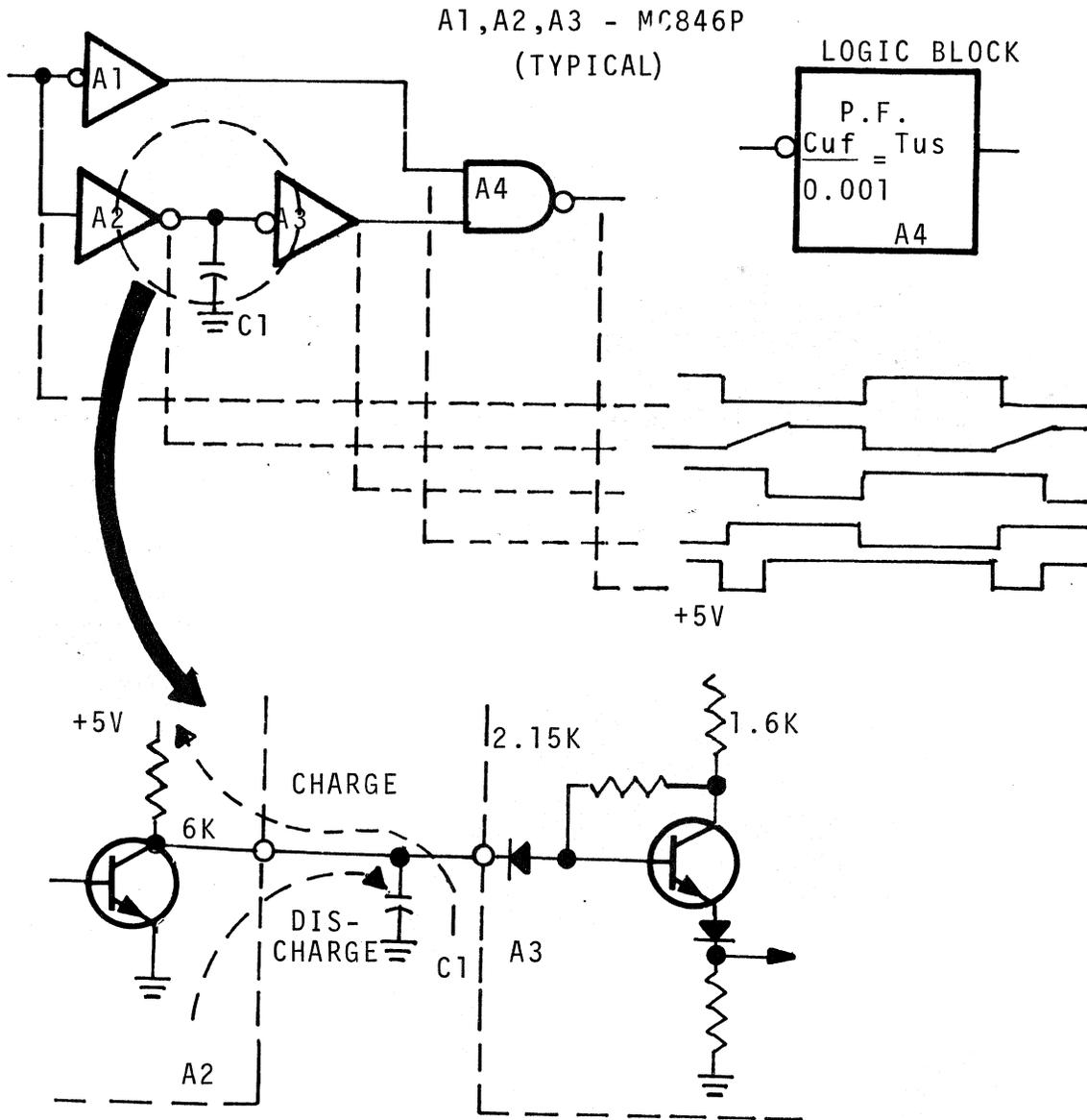


5.5. The AVR-1 uses a variation of the integrator circuit to perform the differentiator pulse former function.

A. Review of differentiator pulse former



B. AVR-1 Pulse Former

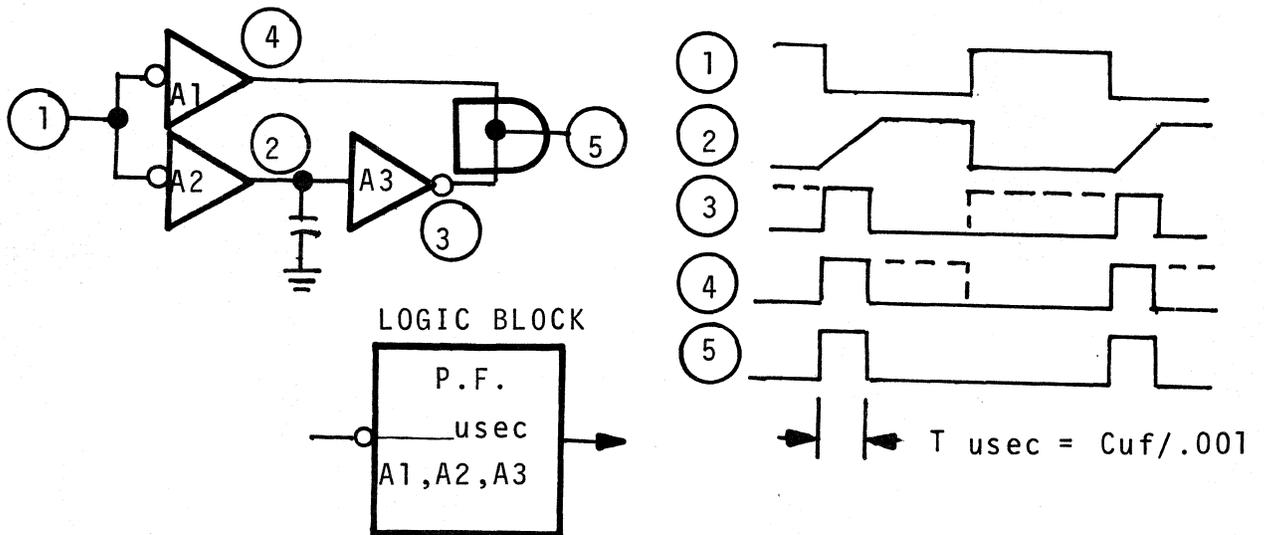


C. Circuit Operation

- Every negative transition of the input signal produces a pulse at the output.
- Pulse width approximately 1 micro second for every 1040pf of C1 in most applications
- As long as input to A2 is positive, its output transistor is conducting, keeping C1 at ground
- When the input to A2 swings negative, the output transistor turns off, and C1 starts charging towards +5V through 6000ohms, until positive enough to turn on the input transistor of A3, causing A3 output to go low, to ground.

5.6.

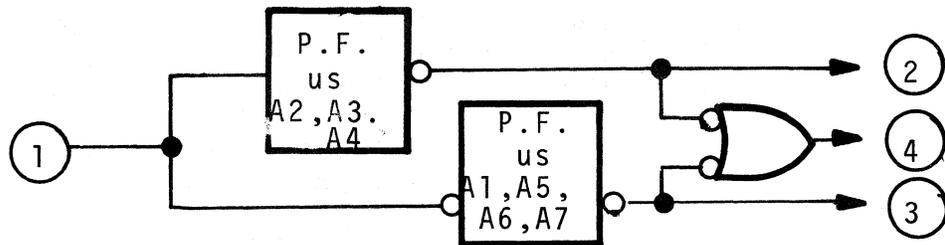
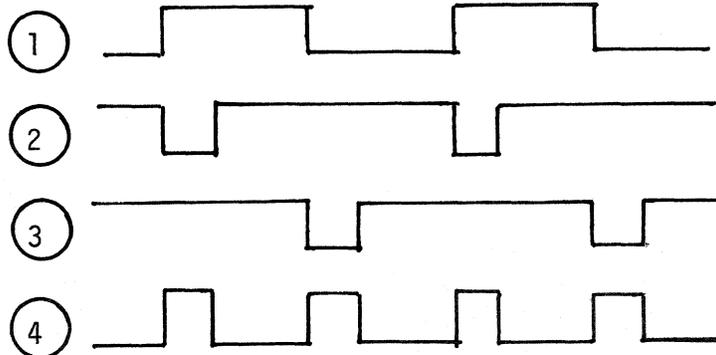
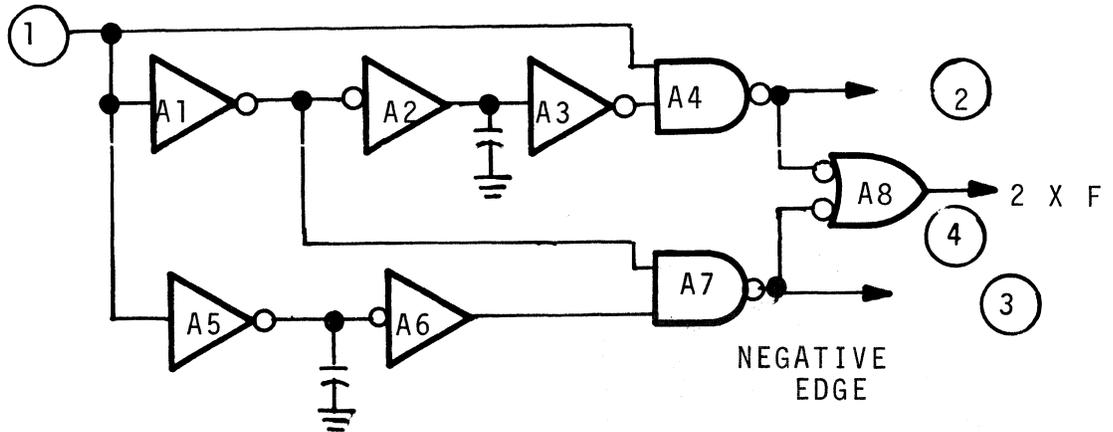
A variation of this circuit uses the "WIRED AND" gate



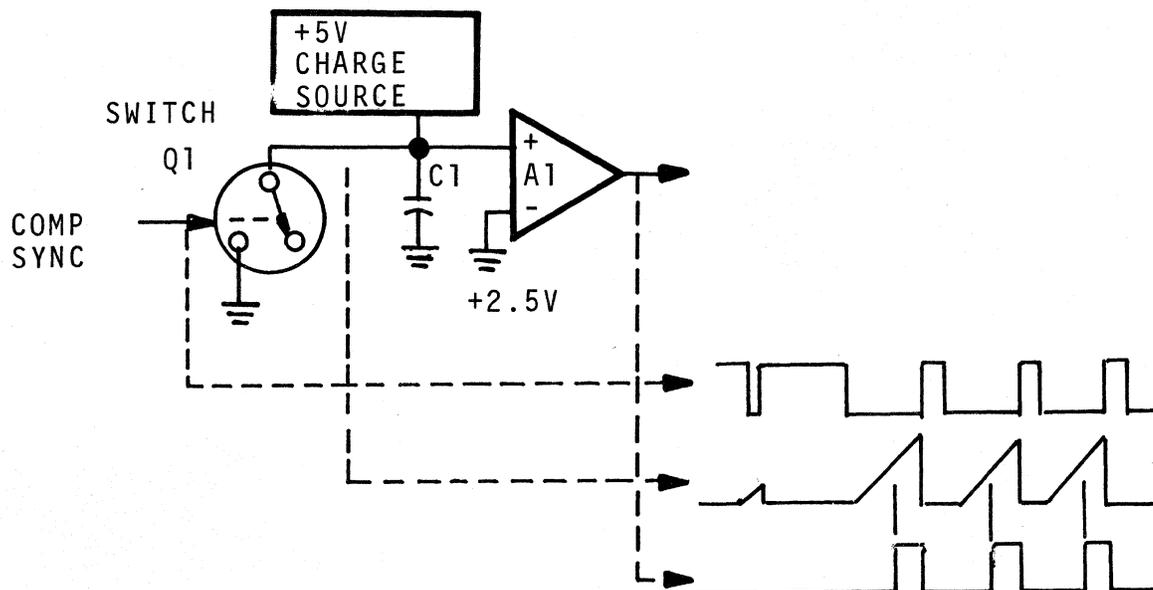
- A. The output of "WIRED AND" gate low when either A1 or A2 output low (ground)
- B. The circuit produces a positive pulse out for every negative transition of the input signal.

5.7.

The pulse former circuit may be utilized as a frequency doubler.

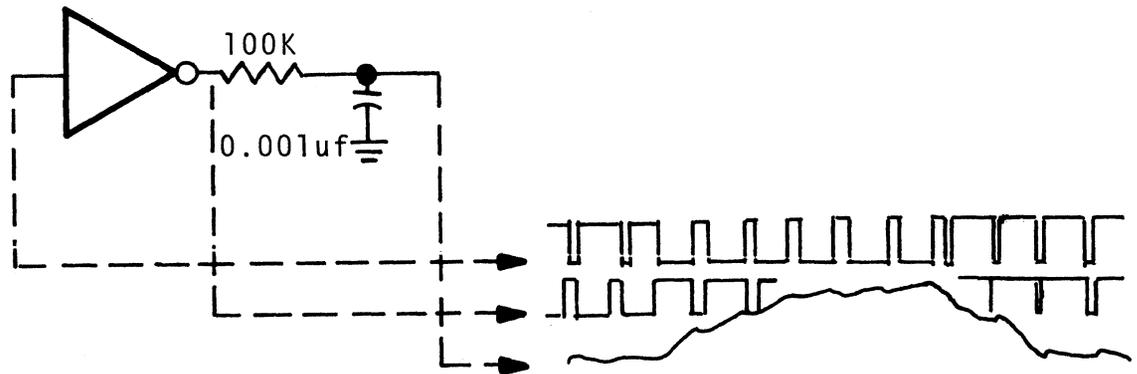


5.8. One method of pulse width discrimination uses the ramp generator.



- A. During the time that the composite sync signal is positive, switch Q1 operates and keeps C1 at ground.
- B. When a sync pulse swings negative, Q1 turns off and allows C1 to charge positive.
- C. During H sync time, it is allowed to charge for about 4.5 usec; during the 5 or 6 equalizing pulses, about 2.5 usec.
- D. During the serrated vertical pulse, C1 has about 27 usec to charge towards +5Volts.
 -Only during the vertical interval can C1 charge positive enough to exceed the +2.5V bias on the minus input to voltage comparator A1, and allow its output to swing positive.

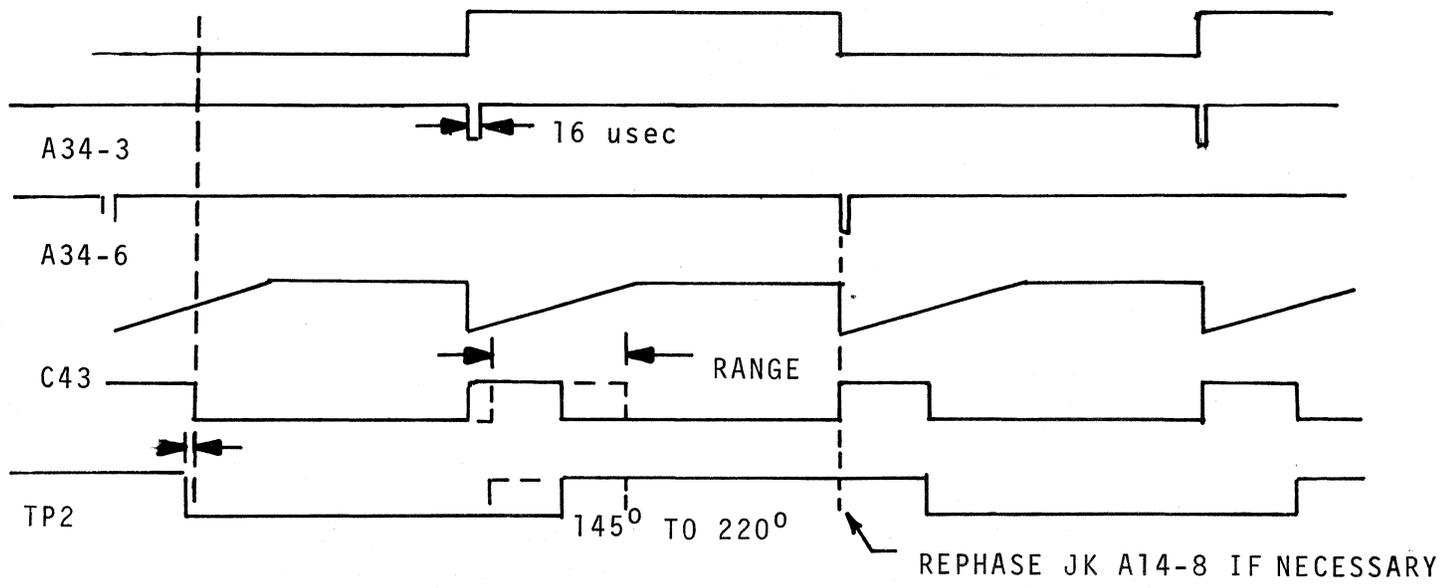
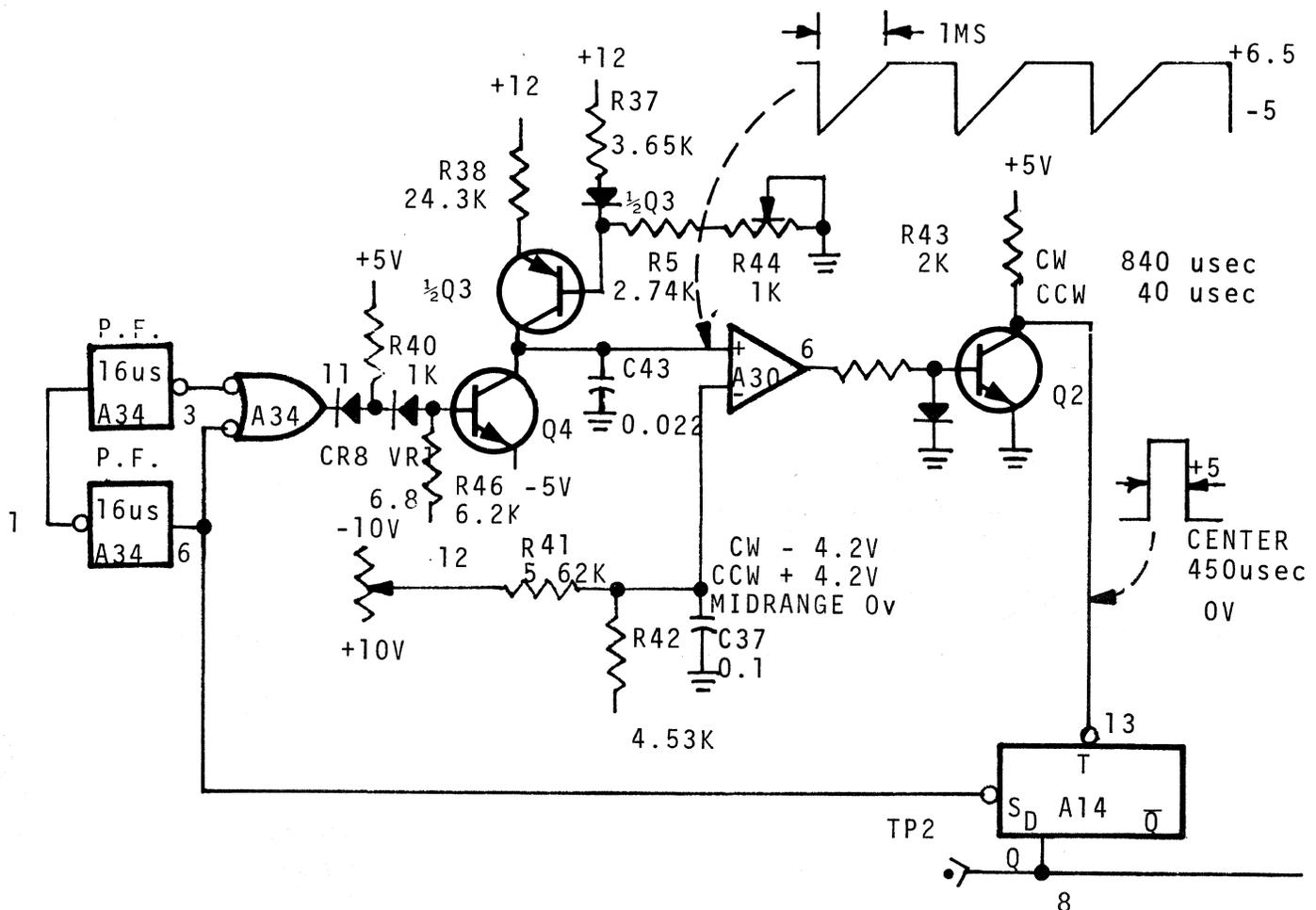
- 5.9. The integrator is in another way to recognize the vertical sync interval.



- A. The RC time constant is 100 usec.
 - B. During horizontal sync pulses (about 4.6 usec) and equalizing pulses (about 2.5 usec) the capacitor gets very little charge and during the following line or half line is completely charged
 - C. During the serrated vertical sync pulse it has about 27 usec to charge positive, but only 5 micro seconds to discharge, so that it produces a pulse representing the vertical pulse.
 - D. Or, the circuit has acted as a low pass filter, leaving only the fifty or sixty cycle component of the synchronizing signal.
- 5.10. In one case in the AVR-1 this circuit is used as a frequency discriminator, producing a D.C. voltage out which is proportional to the period of the input constant width pulses.
- 6.0. Phase shifter
- 6.1. The editor tach phase shifter or PWA 141 of the AVR-1 operates at 240/250HZ

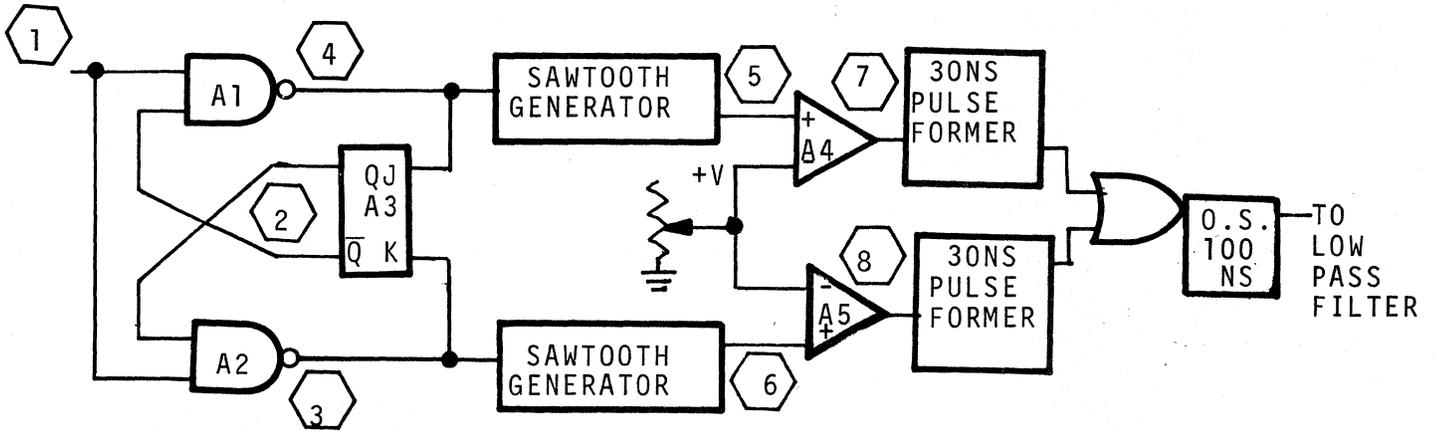
- 6.1.
- A. Two pulse formers and NOR GATE A34-11 produce a series of narrow pulses at twice tach frequency (480/500Hz) which, through, Q4 discharge C43 to -5 volts.
 - B. At the end of the pulse C43 starts charging through Q3 towards +6 volts.
 - 1. Requires about 1 millisecond, or 90° of tach. and is the "+" input to A30-6.
 - C. The negative input to A30-6 is a voltage from the EDIT TACH PHASE potentiometer on the EDITOR Control Panel. At the input to A-30, it varies continuously from +4.2V to -4.2Vdc.
 - D. At the center of the range it is zero volts.
 - E. As long as the "+" input to A30-6 is more negative than the "-" input, the output is negative.
 - 1. The output of A30 swings positive when the "+" input (ramp) voltage is more positive than the "-" input (variable dc voltage).
 - E. Q2 inverts the signal and the variable (now negative going because of the inversion) transition clocks J-K Flip-Flop A14-8, connected as a divide-by-two
 - G. A pulse from A34-6 to the "SD" input of A14-8 assures that output phase is correct.
 - 1. A negative level on the "SD" input overrides and other inputs and puts A14-8 (Q output) High.

6.2. Circuit:



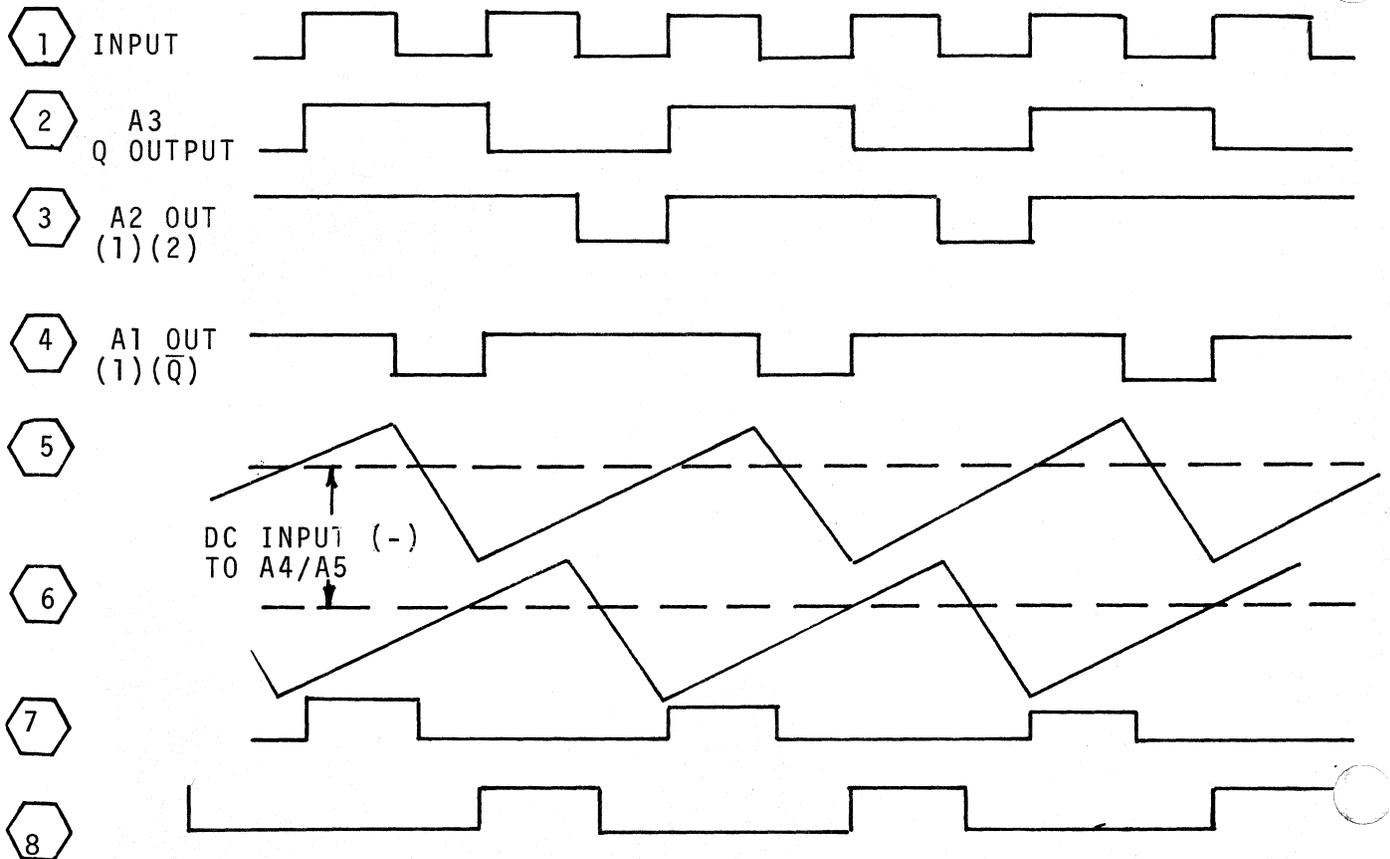
6.3.

A somewhat different version is used in the reference subcarrier phase shifter in the Universal Colortec and the AVR-1 Module 203.



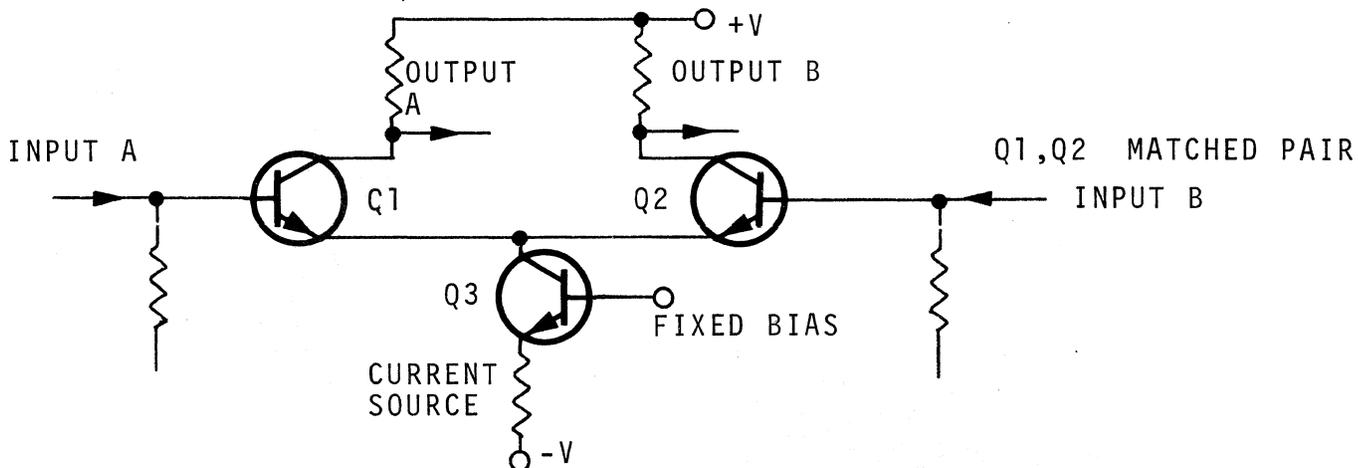
SIMPLIFIED CIRCUIT

- A. The input signal is subcarrier (3.58/4.43MHz) which has been squared up in a limiter.
- B. A3 is an AC coupled JK Flip-Flop. A positive transition on J causes Q to go high.

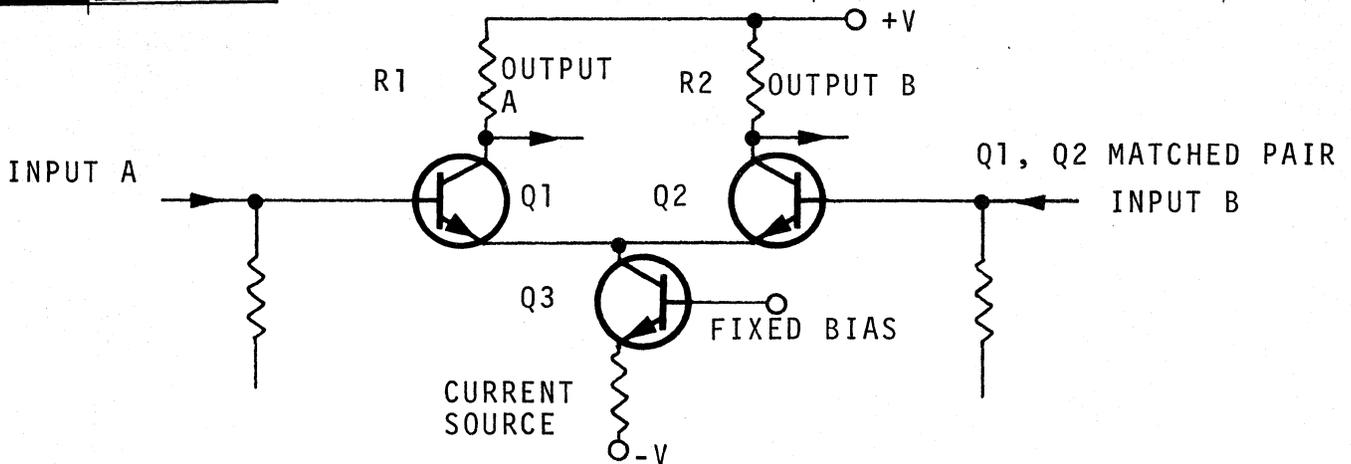


DIFFERENTIAL & OPERATIONAL AMPLIFIERS

I. Differential Amplifier - Basic Circuit



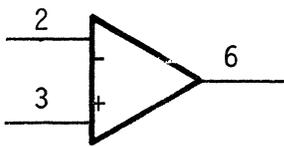
- A. Produces output proportional to input signals
 - 1. Signals of equal amplitudes and same polarities applied to input would cancel at outputs.
 - a. Example - Output taken at Output A with equal inputs at Input A & B
 - b. Input A is inverted to - A at Q1 collector
 - c. Input B sees Q2 as emitter follower with no inversion and Q1 as common base amplifier with no inversion
 - d. Signal at Q1 collector equals - A + B, signal at Q2 collector equals A - B
 - 2. Differential Amplifier used as phase splitter - driven single ended produces outputs of opposite polarity and amplified
 - a. Example: Signal at Input A is amplified and inverted by Q1 to produce - A, Q2 base tied to fixed bias.
 - b. Signal also sees Q1 as Emitter follower and is coupled to Q2 emitter where it is amplified by Q2 operating in common base configuration to produce amplified A at A2 collector.
 - 3. Differential Amplifier used in input circuits to reduce hum caused by different ground potentials between two chassis. (Common Mode Rejection)
 - a. Input A driven single ended from center conductor of unbalanced line. Output taken from Q2 collector. Input B connected to shield of unbalanced line.
 - b. Common Mode Signal (hum) would cancel at Q2 collector. (A - B)
 - c. Main line signal at Input A would be amplified and appear at Q2 collector free from hum.



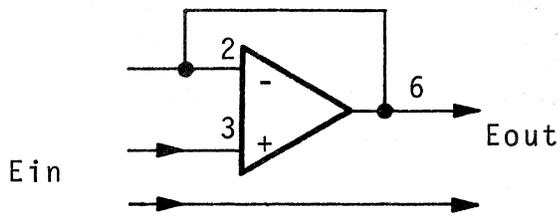
4. Differential amplifier used as reference amplifier. (Power Supplies)
 - a. Q2 base tied to stable voltage source (Zener Diode)
 - b. Q1 base connected to voltage sensing lead from Power Supply Output.
 - c. Q1 collector goes to drive series regulator transistor
 - d. Q1, Q2 bases will try to be at same potential - if any change at Q1 base it will be sensed and output from Q1 collector will be used to control series regulator transistor.
- B. Q3 acts as constant current source.
 1. Current that flows thru Q1, Q2 will be fixed and held constant by Q3
 - a. With current source total current divides at Q1, Q2 emitters and is equal to Q3 collector current.
 - b. Advantage to give better common mode rejection to supply changes
 - c. Gain will not change with common mode signals. Operating point of circuit constant.
 - d. Current determined by fixed bias and value of Q3 Emitter resistor. Input very high impedance.
 2. Differential amplifier used as switch
 - a. Reverse bias Q3 base - emitter junction - no current flows - acts as high isolation switch
 3. Differential amplifier as limiter
 - a. Sum of Q1, Q2 collector equals the emitter currents
 - b. Input A driven so Q1 takes all current, no current will flow thru Q2, maximum possible change equal to $I_c R_1$.
 - c. Emitter currents constant Q1, Q2 never driven into saturation
 - d. Limiting is symmetrical - limiting action equal for input positive and negative input excursions.
 4. Differential amplifier as amplitude modulator
 - a. RF applied to Input A. Input B tied to fixed bias
 - b. Modulating voltage applied to Q3 base controlling gain of Q1, Q2

II. Operational Amplifiers

- A. Generally high gain direct coupled amplifier
 - 1. Circuit action generally controlled by external components
 - 2. Works similar to differential amplifier
 - 3. Generally balanced input and single-ended output
 - 4. Features high input impedance and low output impedance
- B. Performs various analog functions
 - 1. Inverting and non-inverting amplifiers
 - a. Open loop gain very high and closed loop gain controlled by feedback resistors
 - 2. Current drivers
 - 3. Integration and differentiation
 - 4. Summing
 - 5. Reference amplifiers-power supplies
 - 6. Active filters
 - 7. Oscillators, modulators and synchronous detectors
- C. Typical Fairchild 741

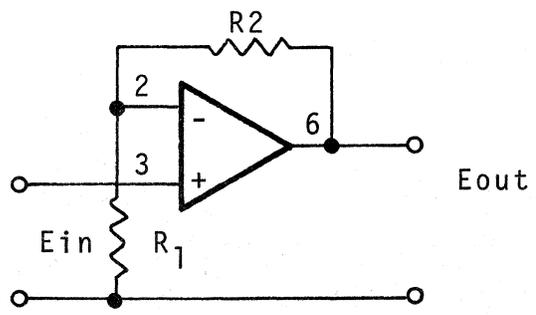


- 1. Has two inputs labeled + and -. + is the non-inverting input. - is the inverting input. It amplifies the difference between the voltages applied to its two input terminals
- 2. Various circuit functions that can be performed by operational amplifiers
 - a. Source follower amplifier (circuit action similar to transistor emitter follower).



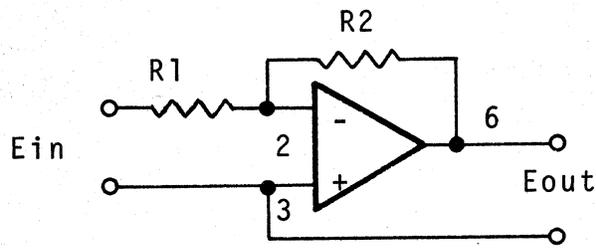
$E_{out} = E_{in} (1 - 1/A_o)$ A_o nearly unity

- 1. Gain unity
- 2. Input impedance very high (50 megohms)
- 3. Non-inverting
- b. Non-inverting amplifier



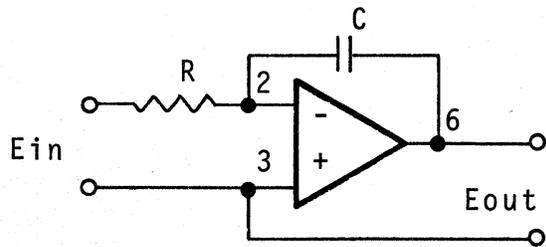
$1G = \frac{R_2 + R_1}{R_1}$

c. Inverting Amplifier



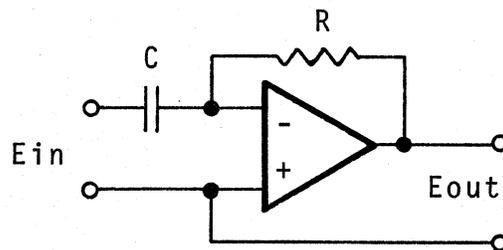
1. Gain = $R2/R1$

d. Integrating Amplifier (sawtooth generator)



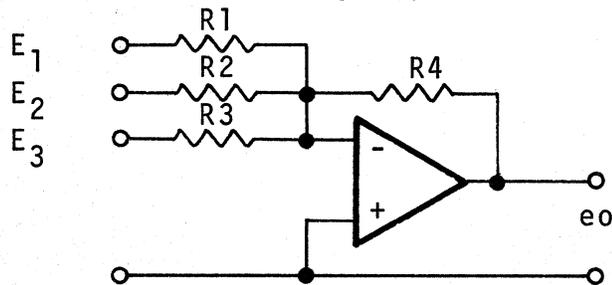
$$E_{out} = -\frac{1}{RC} \int E_{in} dt$$

e. Differential Amplifier



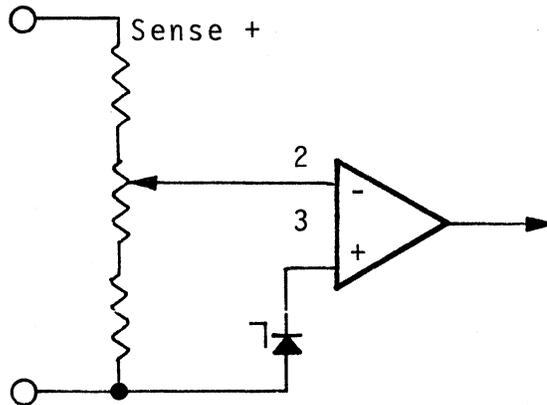
$$E_{out} = RC \frac{de_{in}}{dt}$$

f. Summing Amplifier

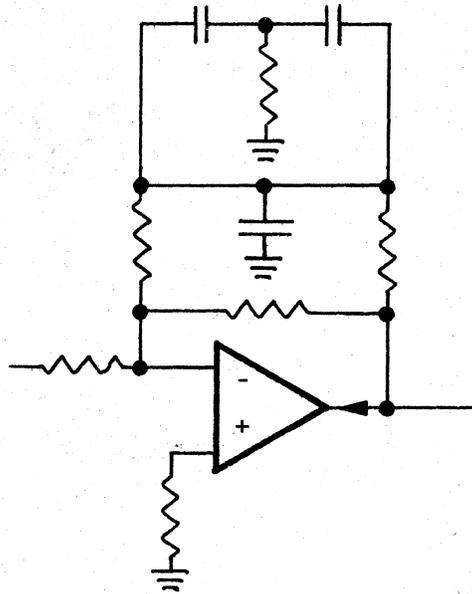


$$e_o = \left(e_1 \frac{R_4}{R_1} \right) + \left(e_2 \frac{R_4}{R_2} \right) + \left(e_3 \frac{R_4}{R_3} \right)$$

g. Common application of 741 as a reference amplifier in power supply.



1. Voltage from sense lead applied to reference amplifier.
 2. Reference amplifier amplifies difference between its input terminals and controls a series regulator.
 3. Two input terminals should be within a few millivolts of each other.
 4. Amplifier operating open loop-voltage gain very high.
 5. Small difference at input will result in large change in output.
 6. Voltage more than 15 millivolts between 2 and 3 indicates fault condition.
 7. Pin 2 more positive than 3-output towards negative side.
 8. Pin 2 more negative than 3-output towards positive side.
 9. Note that a short or partial short on the output will restrict the output swing. The amplifier may have a large voltage difference at the input but will be good if output is trying to swing toward correct supply.
- h. Band Pass Filter.
1. The 741 has internally controlled roll-off so that the voltage gain rolls off at 6db/octave.
 2. Frequency response can be controlled further by RC combinations in the feedback networks.
 - a. Example--Roll-off in control track reproduce amplifiers.
 - b. Example-10HZ Band Pass Filter in auto-tracking.



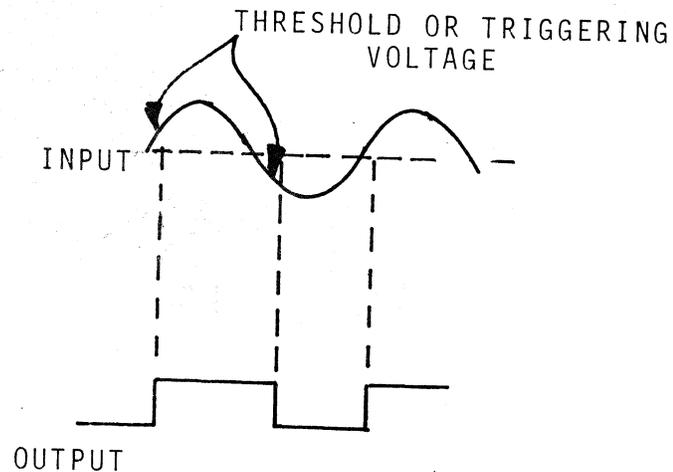
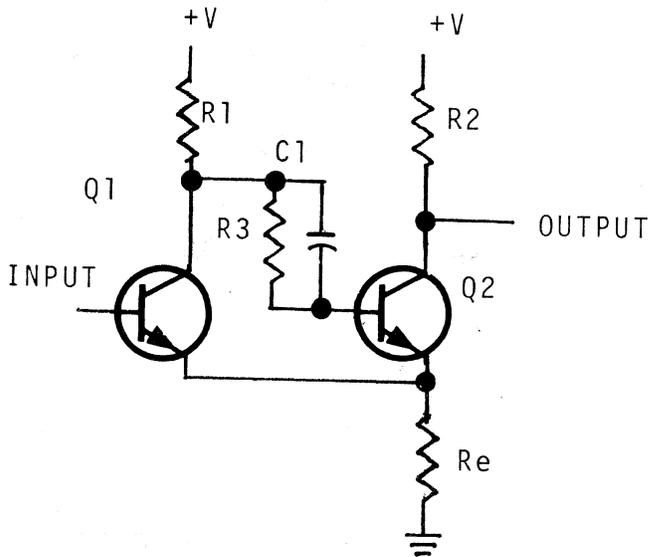
10 HZ B.P.F.

- i. Special operational amplifiers serve functions as balanced modulators-demodulators.
 1. Example-Encoding and decoding in color television which uses amplitude modulation suppressed carrier.

III. Digital applications of OP Amps

A. Schmitt Trigger - transistor model

1. Multivibrator that is used in squaring applications.
 - a. Converts waves with slow rise and delay times to waves having steep edges. (Sine waves to square waves).
 - b. Used to regenerate pulses at input of machines
2. Basic Circuit



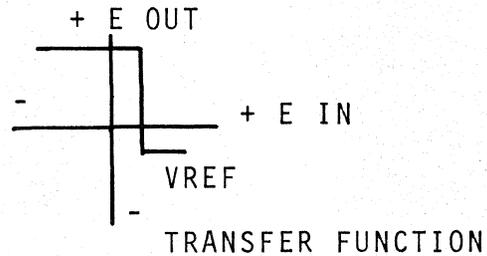
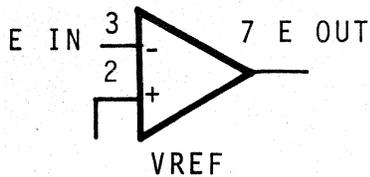
1

- a. Q1, Q2 alternate their conduction states in response to the input sine wave.
- b. Q1, Q2 have two states: they can be in full-on, or full-off.
- c. Static state Q1 biased off, Q2 biased on.
 1. Q2 biased on via R1, R3. Q2 collector ground.
 2. Current flow through RE helps reverse bias Q1 emitter (maintain at a positive potential).
 3. Positive going sine wave at input ultimately goes positive enough to overcome positive bias on Q1 emitter.
 4. Q1 collector voltage drops - coupled over to Q2 base via C1, R3 to turn off Q2, its collector voltage rises.
 5. A very rapid switching action ensues with Q1 turning full-on and Q2 turning full-off
 6. Circuit stays in this condition until input sine wave falls to a value more negative than the value associated with the first switching action.
 7. When the input voltage reaches this triggering voltage the Schmitt Trigger will reverse states.

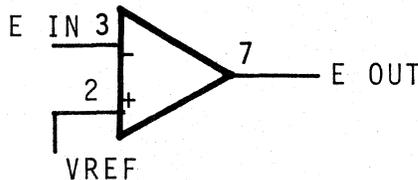
8. Difference between the two triggering voltages is called the voltage hysteresis.
9. Schmitt Trigger has two possible states on the output, a high or a low.

B. Differential Voltage Comparator

1. High gain differential input, single-ended output amplifier.
2. Compare signal voltage on one input with reference voltage on other input.
3. Produce digital one or zero when one input is higher than the other.
4. Uses
 - a. Schmitt trigger
 - b. Pulse height discriminator
 - c. Voltage comparator in A/D converter
 - d. Zero crossing detector
 - e. Threshold detector
5. Basic level detector circuit (Fairchild 710)



- a. When E_{in} exceeds V_{ref} the output switches positive or negative depending how the inputs are connected.
- b. Transfer function illustrates this.
 1. E_{in} more positive than V_{ref} , E_{out} goes to a low level.
- c. Auto-wipe circuit in VS-600 - example of voltage comparator in A/D converter.





SECTION II, APPENDIX A

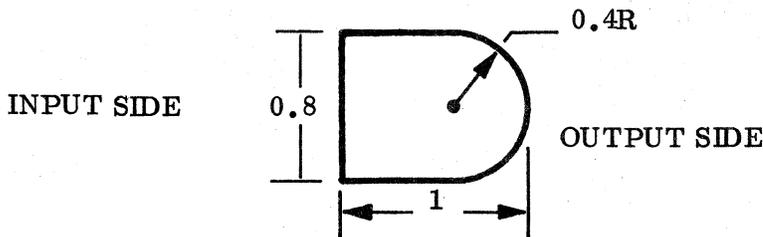
- I. This appendix is a summary of MIL STD 806, which establishes graphic symbols for use in logic diagrams for systems of two state devices.
 - A. The standard also references the following documents:
 - 1. MIL-STD-12 Abbreviations for use on drawings.
 - 2. USAS-Y32.2 Graphical symbols for Electrical and Electronic diagrams.
 - 3. USAS-Y32.16 Electrical and Electronic reference designation.

- II. Section 3 covers presentation techniques.
 - A. Symbol orientation weight of line or symbol size do not affect the meaning of the symbol (3.1,3.2, 3.3).
 - 1. Relative sizes of symbols are covered in section 7 of the standard.
 - B. The identification code specified is in general not used on AMPEX drawings (3.4).
 - C. Logic diagrams indicate direction of signal flow by symbol orientation. Arrows indicating signal flow are desirable . Signals leaving the logic diagram shall be terminated with a signal arrow.
 - 1. The standard specifically forbids arrows immediately adjacent to any graphic symbol input or output.
 - 2. Stylized waveforms, duration of delays, input and output pin numbers, and polarity notations should be used.

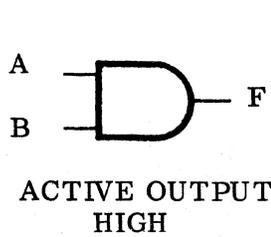
- III. Section 4 covers definitions.
 - A. A LOGIC SYMBOL is the graphic representation of the aggregate of all the parts implementing a logic function. (para. 4.1)
 - B. A LOGIC FUNCTION is a combinational, storage, delay, or sequential function expressing a relationship between variable signal inputs to a system or device and the resultant output(s). (para. 4.2)
 - C. A BASIC LOGIC DIAGRAM depicts logic functions with no reference to physical implementation. It should depict all logic relationships as simply as possible. (para. 4.3)
 - D. A DETAILED LOGIC DIAGRAM depicts all logic and non-logic functions, Spocket locations, pin numbers, test points, and other physical elements necessary to describe the logic. It is used primarily to facilitate the rapid diagnosis and localization of malfunctions. (para. 4.4)
 - E. A TABLE OF COMBINATIONS describes the active input/output conditions of the basic logic functions. (para. 4.5)
 - 1. HIGH (H) more positive and LOW (L) relatively less positive.

IV. Section 5 designated LOGIC SYMBOLS. The following summary includes details from Section 6, PRACTICE; Section 7, MECHANICAL AID; APPENDIX B, ASSIGNMENT OF LOGIC LEVELS TO BINARY LOGIC ELEMENTS.

- A. Logic devices are basically two state devices with inputs and outputs High or Low, regardless of actual voltages involved.
 - 1. In one device, +5V on the input causes the output to go to ground, whereas ground on the input causes the output to swing to -2 volts.
 - a. Or, with a HIGH (+5V) in, the output is high (Ground).
 - b. With a LOW (Ground) in, the output is LOW (-2V).
 - 2. The ACTIVE STATE (input or output) is indicated by the presence or absence of a small circle, which is never drawn by itself on a diagram (para. 5.3). It does not necessarily refer to a logic "1" or logic "0", or electrical reference states (app B, 20.1).
 - a. Active inputs or outputs of a function may be logical 1 in either the more positive state -HIGH (H) or the less positive LOW (L) state; or a logical zero either High or Low.
 - b. A small circle at the inputs(s) indicates that a relatively LOW input signal activates the signal. The absence of the circle indicates that a relatively HIGH input activates the device.
 - c. A circle on the output side indicates the active state output is LOW; its absence indicates the active output is HIGH.
 - d. The presence of an indicated active output does not necessarily provide a useful input to other elements. It may prevent the operation of some and enable others.
- B. The AND function is an element whose output is active when all its inputs are active. Any "non-active" input will produce a non-active output. (App. A, 20.1)
 - 1. The symbol below represents the AND function.

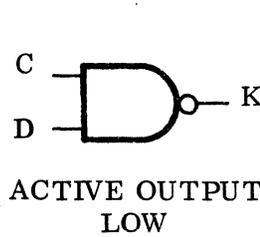


2. Use in logic diagrams



IN		OUT
A	B	F
L	L	L
L	H	L
H	L	L
H	H	H

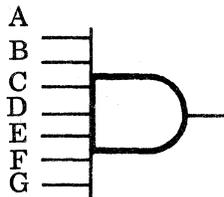
Output high if and only if all the inputs are high (para. 5.1.)



IN		OUT
C	D	K
L	L	H
L	H	H
H	L	H
H	H	L

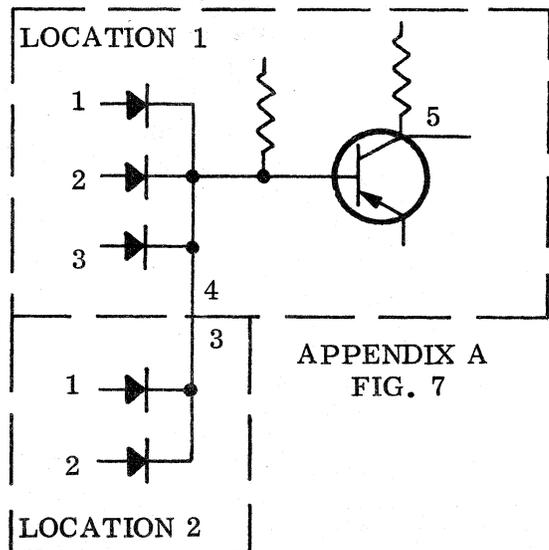
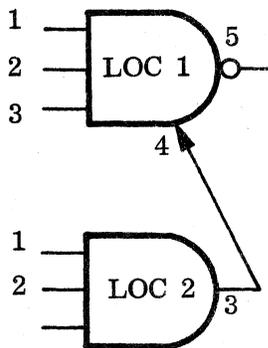
Output low if and only if all inputs high (para. 5.4) usually called NAND GATE, (although STD does not use this terminology).

3. Multiple inputs to a single AND function (para. 6.1).

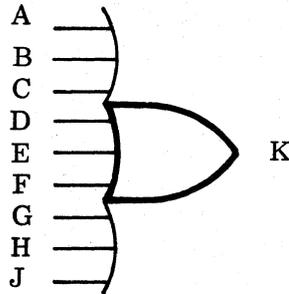


4. Where a circuit is used to add inputs to another AND circuit, and the connection to this second circuit to the first is made at other than a normal input or output of the first circuit the connection will be as shown below (para. 6.4) and will be labeled E to indicate an extension.

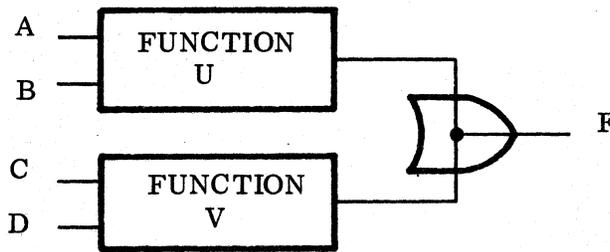
1. The E is omitted on AMPEX drawings.



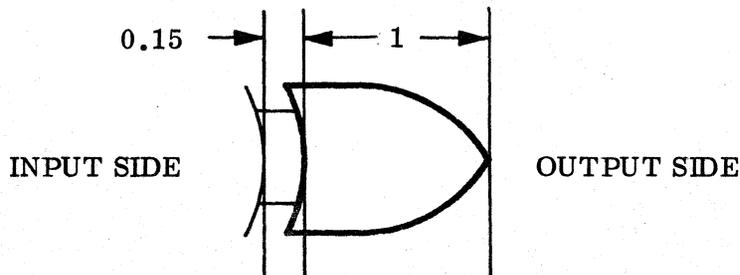
3. Multiple inputs to a single OR function (para. 6.1)



4. Dot OR



D. The symbol shown below represents the EXCLUSIVE OR function (para. 5.6)



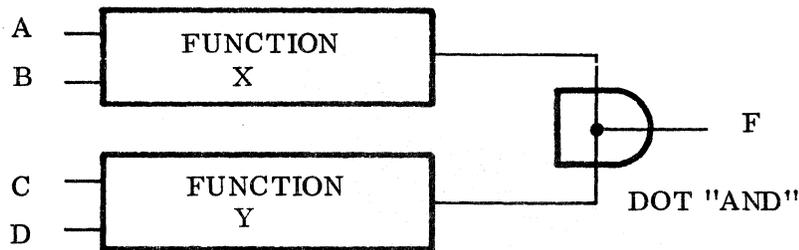
- The output is high (H) if and only if any one input is high and all other inputs are low.



INPUT		F
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

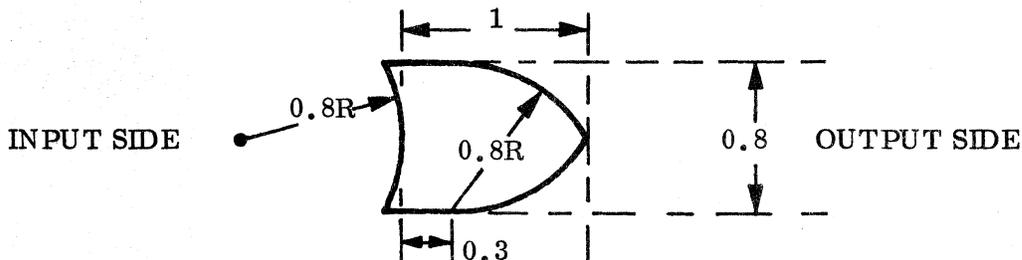
= A(H) and B(L) or
B (H) and A (L)

5. The letter R, when shown adjacent to a symbol, indicates that the output resistor is adjacent to or in the vicinity of the hardware's physical location described by the internal tagging of that symbol (para. 6.4). It is not used on AMPEX drawings.
6. When the AND function is performed by two functions if their outputs are connected, the branched connection be enveloped by a smaller sized AND symbol (para. 6.3).



C. The OR function is considered an element whose output is "active" when anyone or more inputs is "active". All OR inputs "non-active" will produce a "non-active" output (app. B, para 20.1).

1. The symbol below represents the INCLUSIVE OR function (para. 5.2, 7.1).



2. Use in logic diagrams



INPUT		OUTPUT
A	B	F
L	L	L
L	H	H
H	L	H
H	H	H

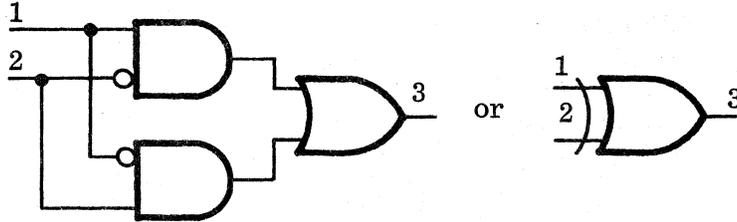
Output high (H) if and only if one or more of the inputs are high (H) (para. 5.2.1)



INPUT		OUTPUT
A	B	F
L	L	H
L	H	L
H	L	L
H	H	L

The output is low (L) if and only if any one or more inputs are high (H) (para. 5.5). Usually called NOR gate, although MIL STD 806 does not use this terminology.

2. Appendix A figure 11 shows another representation.



E. Appendix B covers assignment of logic levels to binary logic elements. Paragraph 20.3 and 20.4 indicates that logic value "one" is assigned to presence signals for devices that are in their electrically active high or low input/output prescribed active states. Two examples are given.

1. Consider a device whose active output (F) is a function of two input signals (A,B) which follows the activity tables shown.

		Electrical Truth Table			Activity Combinations		
A	B	A	B	F	A	B	F
		+2V	+2V	+2V	H	H	H
		+2V	-3V	-3V	H	L	L
		-3V	+2V	-3V	L	H	L
		-3V	-3V	-3V	L	L	L

a. If the +2V is considered the activating level and is assigned logic value 1 and the -3V is considered the inactive level with logic value 0, an AND function is indicated.

		AND Function Activity States		
A	B	INPUT		OUTPUT
		A	B	F
		1	1	1
		1	0	0
		0	1	0
		0	0	0

b. If the -3V level is considered ACTIVE, and assigned logic level 1, an OR function results; the active level indicators (small circles) must be used.

		OR Function Activity States		
A	B	INPUT		OUTPUT
		A	B	F
		0	0	0
		0	1	1
		1	0	1
		1	1	1

2. Consider a different device which follows the Electrical Truth table as follows (para 20.3a).

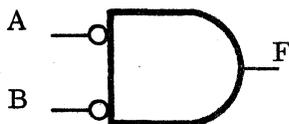
ELECTRICAL TRUTH TABLES							
		INPUTS		OUTPUTS	INPUTS		OUTPUTS
A	B	A	B	F	A	B	F
-3V	-3V	-3V	-3V	+2V	L	L	H
-3V	+2V	-3V	+2V	-3V	L	H	L
+2V	-3V	+2V	-3V	-3V	H	L	L
+2V	+2V	+2V	+2V	-3V	H	H	L



-if any input is high the output will be low.

- a. If input (A,B) -3V levels are considered activating inputs, and therefore assigned the logic value "1" and the +2V output level (F) considered the activated output (logic value "1"), the AND function results. The symbol combines the AND function symbol with input level indicators (electrically less positive than F).

AND TRUTH TABLE

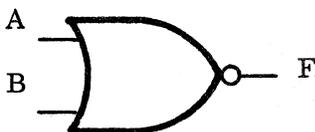


IN		OUT	
1	1	1	1
1	0	0	0
0	1	0	0
0	0	0	0

-The device performs the AND function and an inverting function.

- b. If input (A,B) +2V levels are considering activating inputs (logic value 1), and the -3V output level (F) considered the activated output (logic value 1), the OR function is performed. The symbol combines the OR symbol with an output level indicator (electrically less positive than A,B).

OR TRUTH TABLE

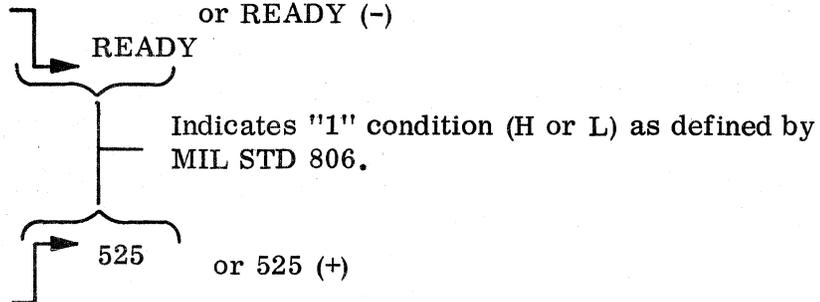


IN		OUT	
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	1

-The device performs the OR logic function plus inversion.

F. Paragraph 20.5 further defines the notation system. A given signal must be considered and when necessary notated in terms of three independently variable parameters for every point in the logic network.

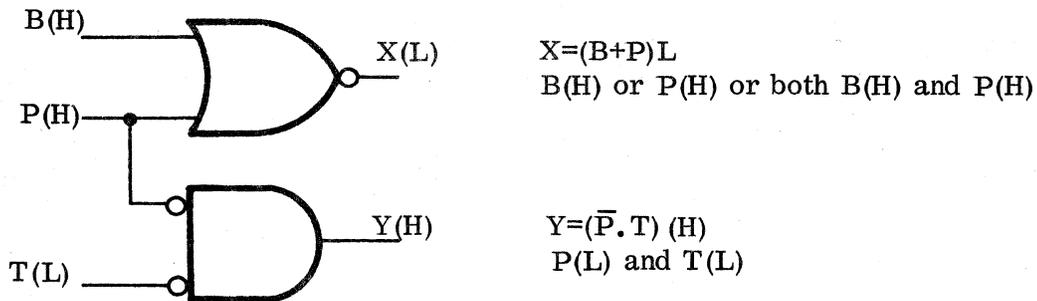
1. Logical state presence ("1") or absence ("0").
2. Electrical state, high or low.
3. Activity state, signal line condition, noted by graphic representation (presence or absence of small circles) or English notations (line name high or low).
 - a. Current AMPEX practice uses a waveform symbology rather than the terms HIGH (H) or LOW (L) which indicate active level for "English" notation, or the designation (+) or (-) or READY (-)



4. The paragraph demonstrates that the non-active (zero state) may be used to activate advice.

a. Given the following Table:

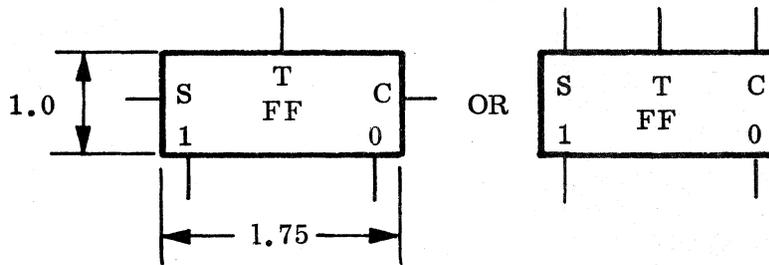
Activity State	Device States	
	+2V	-3V
B (H)	1	0
P (H)	1	0
T (L)	0	1
X (L)	0	1
Y (H)	1	0



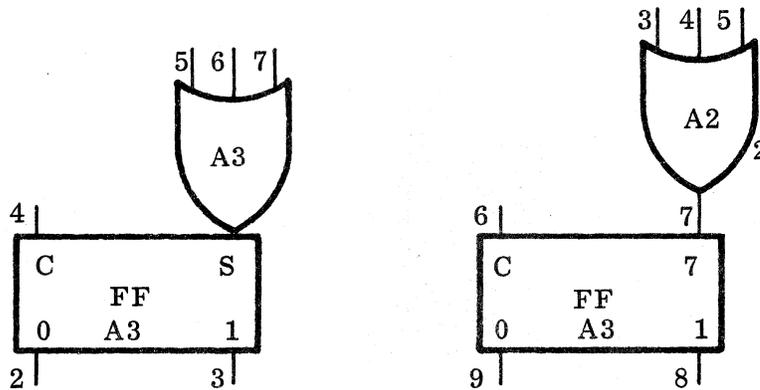
b. Line signal P is active or inactive in terms of previous definitions depending on what point in a logical network is being considered.

G. Paragraph 5.8 defines a FLIP-FLOP as a device which stores a single bit of information with three possible inputs, set (S), clear (reset) (C), and toggle (trigger) (T) and two possible outputs, 1 and 0.

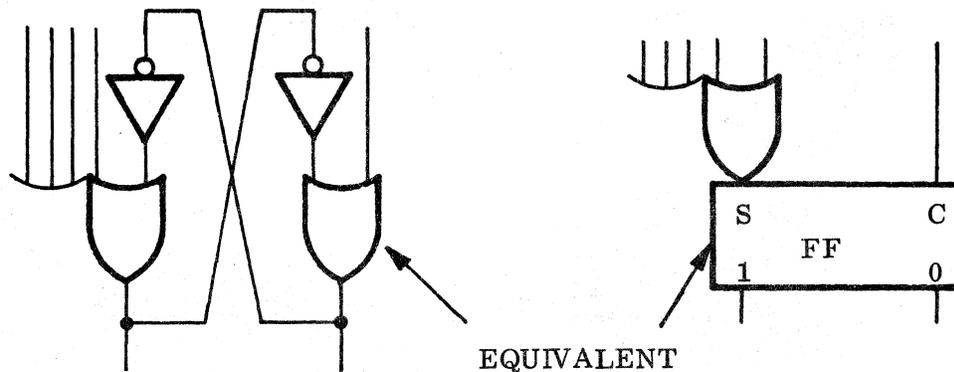
1. The two outputs are normally of opposite polarity. A "1" is stored in the flip-flop when the "1" output level is active and the "0" output level is inactive. A "0" is stored when the condition is reversed.
2. The Flip-Flop assumes the "1" state when an active signal appears at the "S" input regardless of the original state, and the "0" state when an active signal appears at the "C" input. It reverses its state when an active signal appears at the "T" input. "S" input shall be in proximity of the "1" output.



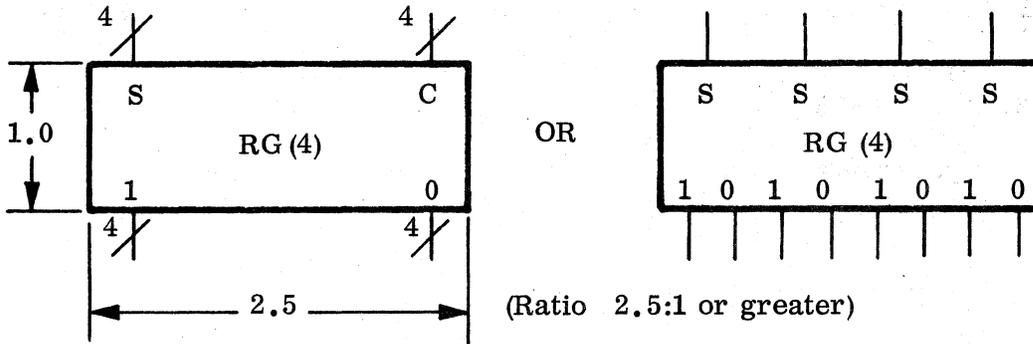
- a. It should be noted that the state of the art has produced a much wider variation in flip-flop nomenclature than is specified in MIL STD 806.
3. Multiple flip-flop inputs may be physically integral with the FF function or physically separated.



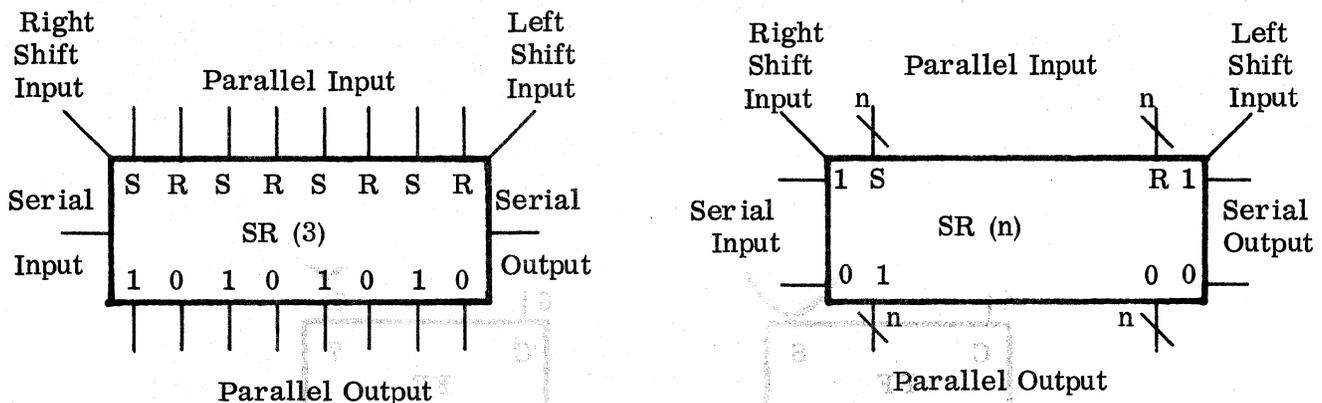
4. Appendix A, Figures 12 and 13 illustrate equivalent diagrams.



H. The binary register is a group of flip-flops used in parallel to store a number of characters (bits) (para. 5.9).

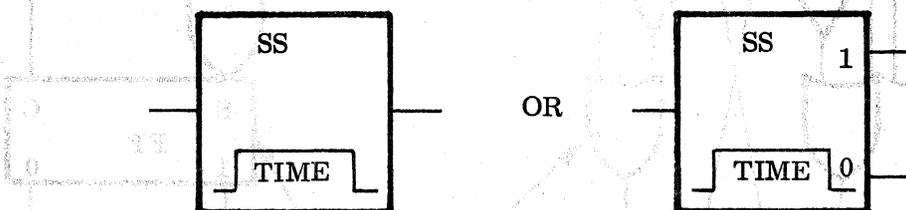


I. The Shift Register symbol represents a binary register with provision for displacing or shifting the content of the register one stage at a time by means of the "shift" input. Ratio of symbol is 2.5:1 or greater (para 5.10).



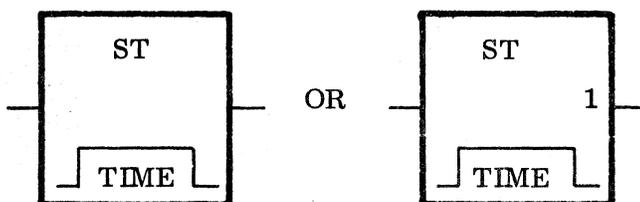
1. Current practice is to use "Q" for "1" and "Q̄" for "0" counter and shift registers. The MIL STD does not mention these designators.

J. The Single Shot (SS) (sometimes called One Shot-OS-or mono-stable multivibrator), when actuated, reverses state for the active time of the device. Unactuated state may be zero or one. Aspect ratio 1:1.

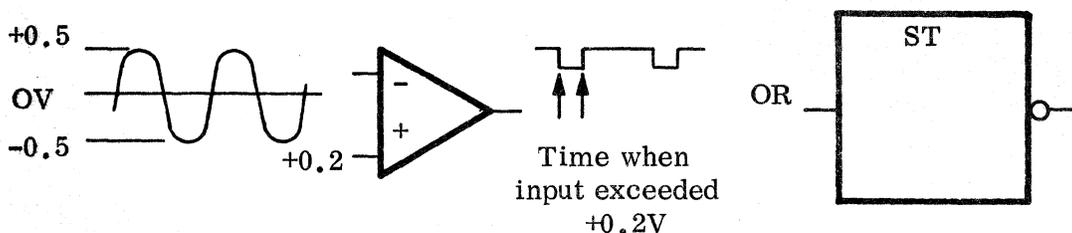


1. Current practice puts a bubble on the output which is low when the device is active.

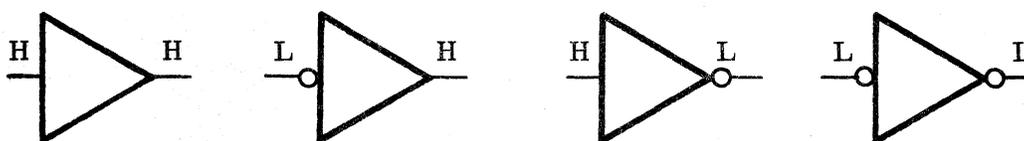
K. The Schmitt Trigger (ST) is actuated when the input signal crosses a certain threshold. Output characteristics are determined by the circuit characteristics, not the input signal. Unactuated state may be "zero" or "one" when actuated it reverses state as long as the input exceeds the threshold value. Ampex ratio is 1:1. (para 5.12)



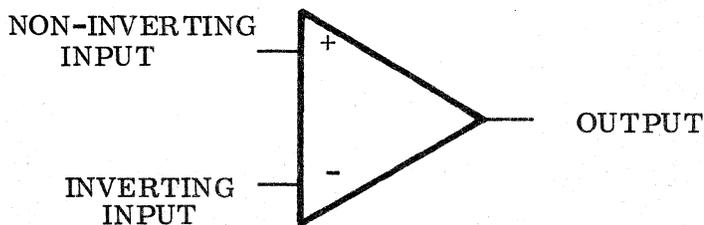
1. The Operational amplifier voltage comparator is now frequently used, and not usually drawn as a ST. This is not covered by MIL STD 806.



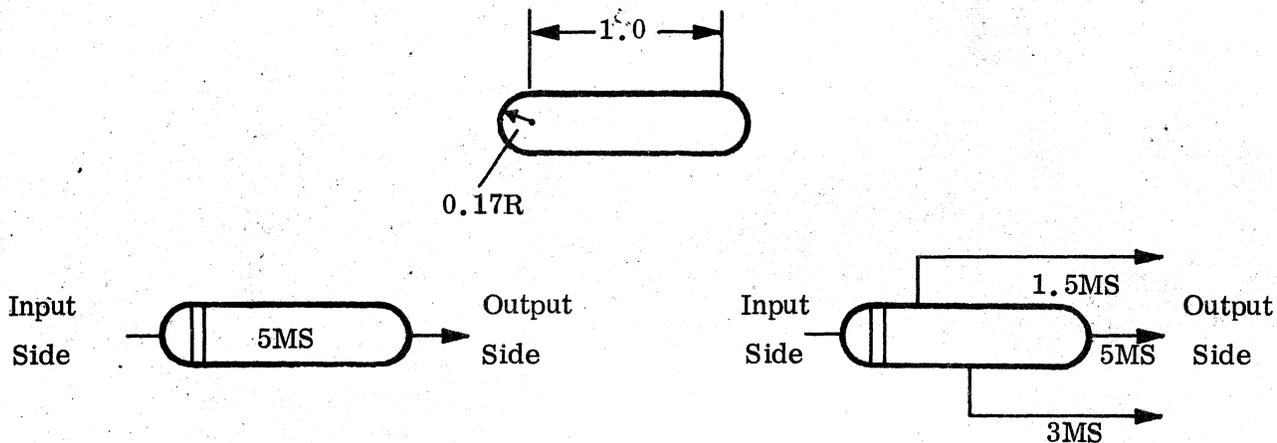
L. The amplifier symbol represents a linear or non-linear current or voltage amplifier, with one or more stages which may or may not produce gain or inversion. It includes level changers, inverters, pulse amplifiers, emitter followers, cathode followers, relay pullers, lamp drivers, etc. (para 5.14)



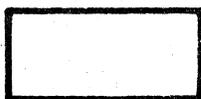
1. MIL STD 806 does not cover the operational amplifier, which may or may not invert, depending on which of two inputs is used.



M. The Time delay symbol

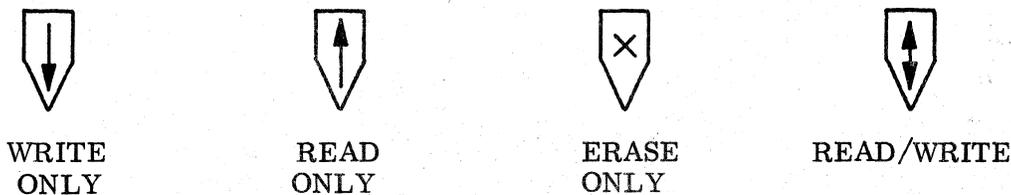


N. A general logic symbol is used for functions not otherwise specified in MIL STD 806. Aspect ratio is 2:1 or greater. (para 5.13)



O. Paragraph 6.6 covers stylized waveforms.

P. Appendix C, 30 or 7 shows the symbols for magnetic heads. (from MIL STD-15-1, item 61)



Q. Not presently referenced by the MIL STD 806 is USAS Y32.14, graphical symbols for logic stds.