

Macintosh PowerBook 100

Developer Note



Developer Note

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Preface

About this note

This developer note describes the Macintosh PowerBook 100 computer and its features that are new and different from those of the Macintosh Portable. This note assumes that you are already familiar with both the capabilities and programming requirements of Apple Macintosh computers, in particular the Macintosh Portable computer. If you are unfamiliar with Macintosh computers or would simply like more technical information on the hardware, you may want to obtain copies of related technical manuals. For information on how to obtain these manuals, see the following section.

For more information

To supplement the information in this document, you might wish to obtain related documentation such as *Guide to the Macintosh Family Hardware*, second edition; *Designing Cards and Drivers for the Macintosh Family*, second edition (third edition will soon be available), and *Inside Macintosh*, Volumes I through VI. Copies of these manuals are available through APDA (Apple Programmers and Developers Association). APDA offers convenient worldwide access to over 300 development tools, resources, and training products and to information for anyone interested in developing applications on Apple platforms. Customers receive the quarterly *APDA Tools Catalog*, featuring the most current versions of Apple development tools and the most popular third-party development tools. Ordering is easy; there are no membership fees, and application forms are not required for most of our products. APDA offers convenient payment and shipping options, including site licensing.

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Chapter 1 Macintosh PowerBook 100 Hardware

The Macintosh PowerBook 100 is a new notebook-class. battery-operated, portable computer. Although its internal architecture is based on the architecture of the backlit Macintosh Portable, the Macintosh PowerBook 100 is a smaller, lighter unit that is 8.5 inches deep, 11 inches wide, and 1.75 inches high and weighs about 5.3 pounds. The feature set and functional capabilities of the Macintosh PowerBook 100 are nearly identical to those of the Macintosh Portable, but the Macintosh PowerBook 100 does not include an internal floppy disk drive or a processor-direct expansion slot. Like the Macintosh Portable, the Macintosh PowerBook 100 supports RAM and modem card expansion, but expansion cards designed for the Macintosh Portable cannot be used in the Macintosh PowerBook 100, and vice versa.

Features

This section lists the major features of the Macintosh PowerBook 100 computer:

- Microprocessor: MC68HC000 running at 15.667 MHz.
- Read-only memory (ROM): 256 KB soldered to secondary logic board (no ROM expansion capability).
- Random-access memory (RAM): 2 MB of pseudostatic RAM soldered to secondary logic board.
- RAM expansion: Internal 70-pin connector allows RAM expansion in increments of 2 MB, 4 MB, or 6 MB via a RAM expansion card. (This same configuration will be used in future Macintosh portable computers.)
- Video display: Flat-panel, transmissive mode, Film SuperTwist Nematic (FSTN) LCD, 640 x 400 pixels, with CCFL (cold cathode fluorescent lamp) backlighting. Backlighting is controlled by the user (via a potentiometer located just under the display).
- Modem: Internal 20-pin connector for optional 2400-baud modem card with send fax (This same configuration will be used in future Macintosh portable computers.)
- Hard disk: One internal 40-pin SCSI (Small Computer System Interface) connector for built-in 20 MB hard disk; one external HDI-30 (high-density interface 30-pin) connector for external SCSI device.
- ♦ Note: Attaching a SCSI Disk Mode Adapter cable between the HDI-30 connector on the Macintosh PowerBook 100 and any Macintosh desktop computer allows the Macintosh to mount the internal hard disk of the Macintosh PowerBook 100 and use it as an external drive. For more information, see "SCSI Disk Mode" later in this note.
- I/O (input/output): One mini-DIN 8 serial port (RS-422) for connecting a printer, a modem, or another standard I/O device; one HDI-30 SCSI connector; one mini-DIN, 4-pin Apple Desktop Bus (ADB) port; one stereo mini-phonejack for monaural sound; and one HDI-20 floppy disk drive connector for an external floppy disk drive.

- Keyboard: Built-in 3.0-mm travel keyboard with 25-mm trackball pointing device (no built-in keypad option). The U.S. version has 63 keys, and the ISO European version has 64 keys.
- Battery: 2.5-ampere-hour SLA (sealed lead-acid), rechargeable battery. Battery backup provided by three 3.5-volt lithium batteries.

- Power jack: An external jack that provides the interface for the external wall-mounted power adapter.
- Weight: Approximately 5.3 pounds.
- Size: 11 inches wide, 8.5 inches deep, and 1.75 inches high.

Of the features listed, probably the most interesting to hardware and software developers are the RAM and modem expansion capabilities.

Machine identification

By using the Gestalt Manager, you can determine whether your application is running on a Macintosh PowerBook 100 or another Macintosh model. If the routine returns a machine selector code of 25, then your application is running on a Macintosh PowerBook 100.

Hardware overview

This section provides a functional description of the Macintosh PowerBook 100 computer's processor, memory, general logic, I/O interface, and expansion capabilities. The Macintosh PowerBook 100 computer includes most of the architectural features of the Macintosh Portable, such as a MC68HC000 microprocessor operating at 15.667 MHz,

a Super Woz Integrated Machine (SWIM) for floppy disk control, a Power Manager, custom integrated circuits, and a Versatile Interface Adapter (VIA). Also, like the Macintosh Portable, sound output is implemented using the Apple Sound Chip (ASC) and one Sony sound chip.

△ Important Memory sizes, addresses, and other data are specific to each type of Macintosh computer and are provided for informational purposes only. To ensure that your application software maintains compatibility across the Macintosh line and to allow for future hardware changes, you should use the Macintosh Toolbox and Operating System routines wherever provided. In particular, never use absolute addresses to access hardware, because these addresses are different on different models. △

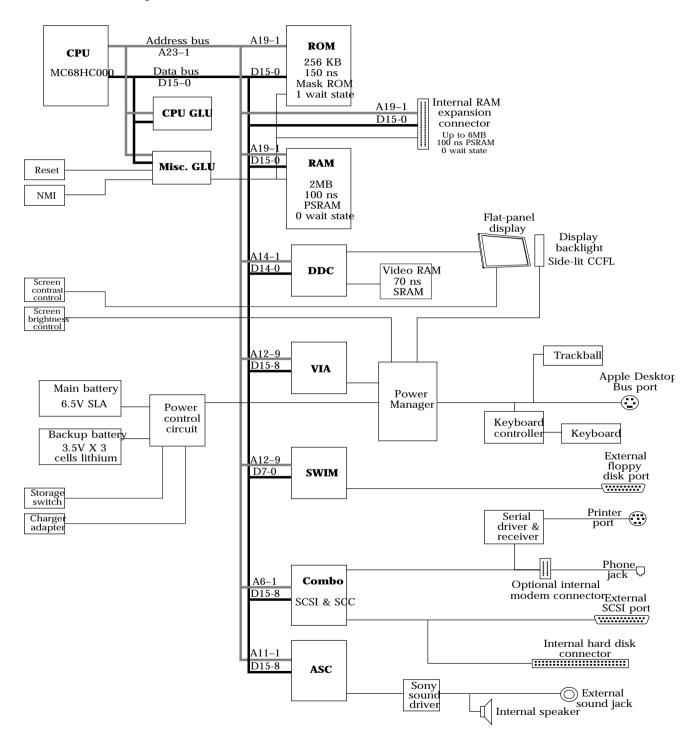
The Macintosh PowerBook 100 is a loosely coupled multiprocessor, the same as the Macintosh Portable. Its Power Manager is implemented with an 8-bit CMOS (complementary metal oxide semiconductor) microprocessor.

Since most of the Macintosh PowerBook 100 circuits are functionally identical to those of the Macintosh Portable, they are discussed only briefly in this document. More emphasis is placed on the RAM and modem expansion capabilities of the Macintosh PowerBook 100.

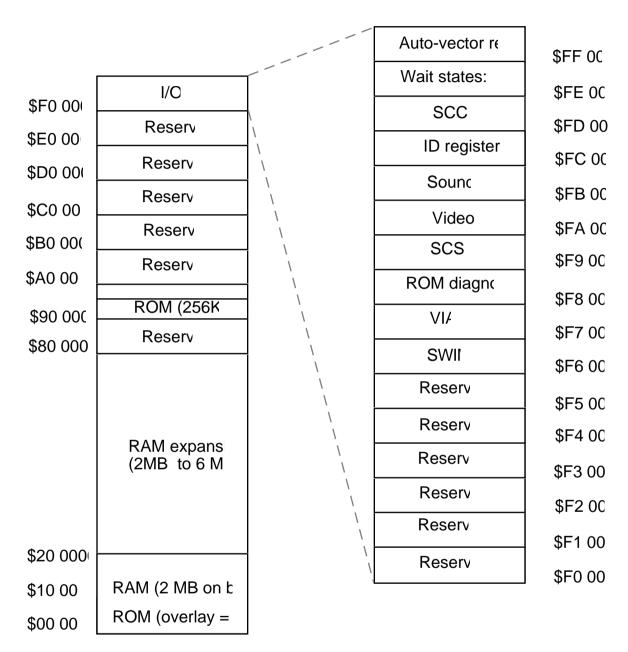
Figure 1-1 is a block diagram showing the relationships of the major components of

the Macintosh PowerBook 100. Figure 1-2 shows the memory map of the Macintosh PowerBook 100 computer.

■ Figure 1-1 Block diagram of the Macintosh PowerBook 100 computer



■ Figure 1-2 The Macintosh PowerBook 100 memory map



Main processor

The Macintosh PowerBook 100 uses a MC68HC000 microprocessor running at a system clock rate of 15.667 MHz. This is the same microprocessor that is used in the Macintosh Portable. Its primary advantage over a conventional 68000 microprocessor is reduced power consumption. The Macintosh PowerBook 100 is designed with a two-state variable wait state system, which effectively reduces power consumption during idle periods by varying the clock frequency between 979.187 kHz and 15.667 MHz.

Custom integrated circuits

This section describes the three ASICs (application-specific integrated circuits) that provide the Macintosh PowerBook 100 computer's internal logic functions.

CPU GLU logic chip

The CPU GLU Logic chip generates CPU clocks, /DTACK (data acknowledgment) signals, and sleep mode control signals and in addition serves as the interface to system ROM, RAM, SCC (Serial Communications Controller), SCSI, VIA, FPU (floating-point unit), SWIM, and DDC (Display Driver Chip) integrated circuits.

In addition, the CPU GLU Logic chip includes an ID register containing a unique ID that allows system software to determine that it is running on a Macintosh PowerBook 100 and not a Macintosh Portable. This is necessary because both the Macintosh PowerBook 100 and the Macintosh Portable have identical system ROMs.

DDC (Display Driver Chip)

The DDC provides the Macintosh PowerBook 100 computer's interface to the LCD (liquid crystal display). Its primary function is to keep the computer's main processor from having to refresh the screen (LCD display), thereby allowing the processor to do more useful work. The DDC generates horizontal and vertical synchronization pulses and all other signals necessary to make the flat-panel display work. It also supports its own video 32K x 8-bit SRAM (static RAM). In addition, the DDC limits the CPU from refreshing the display and thereby allows the CPU to do more useful work.

Miscellaneous GLU logic chip

The Miscellaneous GLU logic chip provides random logic functions such as modem–serial port multiplexing, pseudostatic RAM chip select and refresh, and the clock control logic functions associated with the Power Manager system.

ROM interface

The Macintosh PowerBook 100 uses the same ROM as the Macintosh Portable. The Macintosh PowerBook 100 is shipped with 256 KB of ROM permanently soldered to the main logic board. The Macintosh PowerBook 100 will accommodate a maximum of 4 MB of ROM on the main logic board, but it does not include a provision for internal or external ROM expansion. The ROM is arranged as a 128K x 16-bit array consisting physically of two 28-pin 128K x 8-bit devices with an access and cycle time of 150 ns.

RAM overlay: The ROM is located in the system memory map between addresses

\$90 0000 and \$93 FFFF. Immediately after the system is reset, the RAM overlay process is initiated, causing the starting address of the ROM to be located at \$90 0000 and overlaying the ROM image in RAM address space starting at \$00 0000. This process allows the main processor to address a standard default set of exception vectors as well as a starting address to begin executing code. Following the first access to the normal ROM address range, the ROM image at \$0000 0000 is cleared and replaced by RAM.

ROM wait states: Access to the ROM from the main processor requires two processor wait states. This relates to a bus cycle time of 382.97 ns.

RAM interface

The Macintosh PowerBook 100 is shipped with 2 MB of PSRAM (pseudostatic RAM) on the main logic board. The RAM is arranged physically as four 4-Mbit chips of 512K x 8-bits each with an access and cycle time of 100 ns. In addition, the Macintosh PowerBook 100 includes an expansion slot that accommodates an expansion card and allows RAM to be expanded by up to 6 MB. The RAM expansion feature is described in the next section.

The RAM array is nominally located in the system memory map between addresses

\$00 0000 and \$1F FFFF (for 2 MB of permanent RAM), except following a system reset,

at which time the first 1 MB in the memory map is overlaid by system ROM. However,

the overlay is removed following access to normal ROM space, and the RAM space is then accessible.

Because of the reduced chip count resulting from using the 4-Mbit RAM chips, there is less loading of the microprocessor's address bus and data bus lines in the Macintosh PowerBook 100 than there is in the Macintosh Portable. The address and data bus lines for the permanent RAM have no buffering, but buffering is provided on the address and data bus lines for the RAM expansion slot.

RAM wait states

Access to the RAM (both permanent and expansion) from the main processor requires no (zero) processor wait states, except during the 15-µs refresh cycle. The Miscellaneous GLU logic chip includes special circuitry that performs the refresh function. During sleep and shutdown, in which the main processor is powered off and there is no bus access, the PSRAM enters a self-refresh mode to save power.

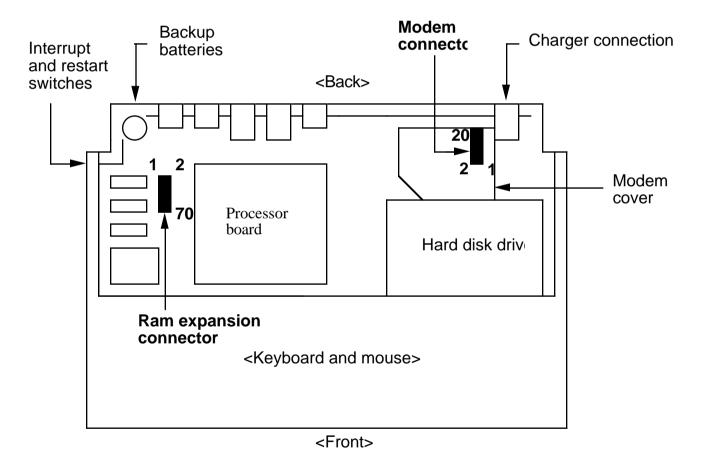
Battery backup

Both permanent and expansion RAM memories are backed up when the Macintosh PowerBook 100 is in the sleep or shutdown mode. This means that when the computer is not in use, the contents of the memory array are retained as long as the battery remains charged.

RAM expansion

The Macintosh PowerBook 100 computer's main logic board contains a 70-pin RAM expansion connector (slot) that supports RAM expansion card sizes of 2 MB, 4 MB, and 6 MB. The main logic board does not have to be modified to change the RAM configuration when an expansion card is installed. The location and pin orientation of the RAM expansion connector is shown in Figure 1-3.

■ Figure 1-3 Location of modem and RAM expansion connectors



Note: If you design your RAM expansion card correctly, it will also work in future Macintosh-family, 68030-based portable computers. A 68030-based machine has a 32-bit data bus, whereas the 68HC000 in the Macintosh PowerBook 100 has only a 16-bit data bus. You should design the expansion card as a 32-bit device, but if you correctly partition the data lines and chip select lines on the card, you can use the same card in either type of machine without loss of performance. The card should have 32 data lines coming out to its connector, and the chip select lines for the upper 16 data bits and the lower 16 data bits should be separated to allow for individual selection of either the upper 16 bits or the lower 16 bits of data. The separated chip select lines are necessary for the Macintosh PowerBook 100 because it can get access to only 16 bits at a time. A 68030-based machine does not require separated chip select lines because it has a 32-bit data bus; therefore, the lines are tied back together on the computer's main logic board.

As is the case with the permanent ROM, only 4-Mbit chips are used for expansion RAM. For example, a 2 MB RAM expansion card has four 4-Mbit PSRAMs (512K x 8-bit chips), a 4 MB RAM expansion card has eight 4-Mbit PSRAMs (512K x 8-bit chips), and a 6 MB card has twelve 4-Mbit PSRAMs (512K x 8-bit chips). Access and cycle times for these devices are 100 ns.

△ Important If you are designing a RAM expansion card for the Macintosh PowerBook 100, you do not have to include logic for address decode or chip select because all of the required signals (address, data, chip select, and control) are available at the RAM expansion connector. The Macintosh PowerBook 100 also provides address and data buffering to compensate for the extra loading caused by the RAM expansion card chips. △

The expansion RAM is located immediately above the permanent RAM in the system memory map. The mapping is done by the Miscellaneous GLU logic chip, which determines whether the Macintosh PowerBook 100 has 1 MB or 2 MB of permanent memory and then maps the expansion RAM to the appropriate location. (The PowerBook 100 is shipped with 2 MB of RAM.) If there is 2 MB of permanent RAM, the expansion RAM is mapped to occupy addresses from \$20 0000 to \$7F FFFF. For example, a 2 MB expansion card would occupy address space \$20 0000 to \$3F FFFF, a 4 MB RAM card would occupy address space from \$20 0000 to \$5F FFFF, and a 6 MB RAM card would occupy address space from \$20 0000 to \$7F FFFF. If only 1 MB of permanent RAM had been installed, all expansion RAM addresses would be shifted down by \$10 0000 into address space \$00 0000 to \$6F FFFF. The memory expansion address space is always available and, unlike the permanent memory, is not affected by the state of the overlay bit.

Software always sees both the permanent RAM and the expansion RAM in continuous locations on the bottom of the system memory map. There is no wraparound in the memory, and a /DTACK (data transfer acknowledge) signal is generated for any accesses within the address range of \$00 0000 to \$7F FFFF. You can get access to these address spaces, where there is no RAM, but the data will be meaningless, although a bus error will not occur.

RAM expansion connector signals

Table 1-1 provides the pin number, name, and description of each of the RAM expansion connector signals.

	Table 1-1	RAM	expansion	connecto	r signal	S
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Pin numbe	er Signal name	Signal description
1	GND	Ground
2	GND	Ground
3	A19	Address bit 19 (buffered)
4	A16	Address bit 16 (buffered)
5	A17	Address bit 17 (buffered)
6	A18	Address bit 18 (buffered)
7	A15	Address bit 15 (buffered)

8	/LW	Lower byte write strobe	
9	A13	Address bit 13 (buffered)	
10	/LW	Lower byte write strobe	
11	A8	Address bit 8 (buffered)	
12	A14	Address bit 14 (buffered)	
13	A7	Address bit 7 (buffered)	
14	A9	Address bit 9 (buffered)	
15	A6	Address bit 6 (buffered)	
16	A10	Address bit 10 (buffered)	
17	A5	Address bit 5 (buffered)	
18	A12	Address bit 12 (buffered)	
19	A4	Address bit 4 (buffered)	
20	/OE.RFSH	RAM output enable and refresh	
21	A3	Address bit 3 (buffered)	
22	A11	Address bit 11 (buffered)	
			(continued)

(continued)

■ Table 1-1 RAM expansion connector signals (continued)

Pin numbe	r Signal name	Signal description
23	A2	Address bit 2 (buffered)
24	/EXP.CS0	Chip select bit 0
25	A1	Address bit 1 (buffered)
26	D7	Data bit 7 (buffered) to and from main
logic boar	rd	
27	D0	Data bit 0 (buffered) to and from main
logic boar	rd	
28	D6	Data bit 6 (buffered) to and from main
logic boar	rd	
29	D1	Data bit 1 (buffered) to and from main
logic boa	rd	
30	D5	Data bit 5 (buffered) to and from main
logic boar		
31	D2	Data bit 2 (buffered) to and from main
logic boa		
32	D4	Data bit 4 (buffered) to and from main
logic boar		
33	GND	Ground
34	/EXP.CS1	Chip select bit 1
35	D4	Data bit 4 (buffered) to and from main
logic boar		
36	D3	Data bit 3 (buffered) to and from main
logic boar		
37	D2	Data bit 2 (buffered) to and from main
logic boar		
38	D3	Data bit 3 (buffered) to and from main
logic boar		
39	D0	Data bit 0 (buffered) to and from main
logic boar		Data hit 1 (harffana l) ta an l fanan an in
40	D1	Data bit 1 (buffered) to and from main
logic boa		Data hit 7 (huffared) to and from main
41 logic boar	D7	Data bit 7 (buffered) to and from main
42	D6	Data bit 6 (buffered) to and from main
logic boar		Data bit o (bullereu) to allu itolii ilialli
43	+5V	+5 V RAM power
40	⊤ J V	TO V IVAIN POWEL

44	D5	Data bit 5 (buffered) to and from main		
logic boar	d			
45	/EXP.CS5	Chip select bit 5		
46	+5V	+5 V RAM power		
47	/UW	Upper byte write strobe		
48	/UW	Upper byte write strobe		
49	nc	No connection		
50	/EXP.CS2	Chip select bit 2		
51	/EXP.CS4	Chip select bit 4		
52	nc	No connection		
53	D11	Data bit 11 (buffered) to and from main		
logic boar	d			
54	D12	Data bit 12 (buffered) to and from main		
logic board				
55	D14	Data bit 14 (buffered) to and from main		
logic board				
		(continued)		

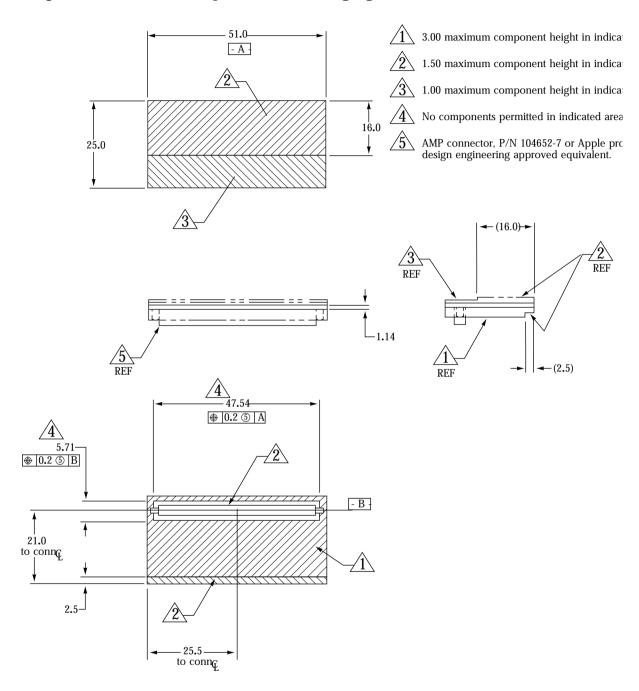
■ Table 1-1 RAM expansion connector signals (continued)

Pin numbe	r Signal name	Signal description		
56	D13	Data bit 13 (buffered) to and from main		
logic boar		,		
57	D8	Data bit 8 (buffered) to and from main		
logic boar	rd			
58	D14	Data bit 14 (buffered) to and from main		
logic boar	rd			
59	D9	Data bit 9 (buffered) to and from main		
logic boar	rd			
60	D15	Data bit 15 (buffered) to and from main		
logic boa	rd			
61	D10	Data bit 10 (buffered) to and from main		
logic boa				
62	D15	Data bit 15 (buffered) to and from main		
logic boar				
63	D13	Data bit 13 (buffered) to and from main		
logic boar				
64	D8	Data bit 8 (buffered) to and from main		
logic boar		_ , , , , , , , , , , , , , , , , , , ,		
65	D12	Data bit 12 (buffered) to and from main		
logic boar				
66	D9	Data bit 9 (buffered) to and from main		
logic boar				
67	D11	Data bit 11 (buffered) to and from main		
logic boar		_ , , , , , , , , , , , , , , , , , , ,		
68	D10	Data bit 10 (buffered) to and from main		
logic board				
69	GND	Ground		
70	/EXP.CS3	Chip select bit 3		

RAM expansion card design guide

Figure 1-4 is a design guide providing the physical information you will need to design a RAM expansion card for the Macintosh PowerBook 100 computer.

■ Figure 1-4 RAM expansion card design guide



Floppy disk interface

A SWIM chip (the same as that used in other Macintosh computers) is the control interface for an optional external floppy disk drive. A high-density interface

(HDI) 20-pin connector on the back of the computer provides the signal interface between the SWIM chip and the external drive.

Unlike the larger Macintosh computers, the Macintosh PowerBook 100 does not accommodate an internal floppy disk drive. Table 1-2 shows the pinout for the external floppy disk connector. Figure 1-5 is a diagram of the external HDI-20 connector.

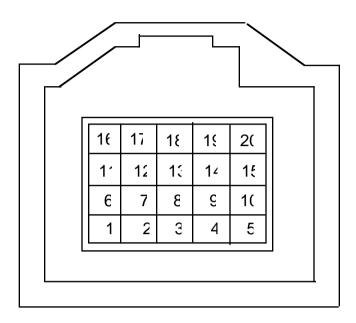
◆ *Note:* The floppy disk connector is not provided with +12 volts because the Apple floppy disk drive that connects externally to the Macintosh PowerBook 100 requires only +5 volts.

■ Table 1-2 Pinout for floppy disk external HDI-20 connector

Pin number	Signal name	Signal description
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	GND	Ground
5	nc	No connection
6	FD.+5V/0	Floppy +5 V power plane
7	FD.+5V/0	Floppy +5 V power plane
8	FD.+5V/0	Floppy +5 V power plane
9	FD.+5V/0	Floppy +5 V power plane
10	nc	No connection
11	PH0	Phase 0: state control line
12	PH1	Phase 1: state control line
13	PH2	Phase 2: state control line
14	PH3	Phase 3: register write strobe
15	/WREQ	Write data request
16	HDSEL	Head select
17	/ENBL2	External drive select
18	RD	Read data

19 W R Write data20 nc No connection

■ Figure 1-5 External HDI-20 connector diagram



SCC and SCSI interfaces

A custom chip called the Combo combines the functions of the SCC and the SCSI controller in a single device. This device, which is also used in several other Macintosh models, is completely software compatible with the SCC (85C30) and SCSI (53C80) chips it replaces.

SCC interface

The SCC portion of the combination SCC/SCSI device includes two independent ports for serial communication. Each port can be independently programmed for asynchronous, synchronous, or AppleTalk protocols. The Macintosh PowerBook 100 has one internal modem connector (Port A) and one external serial printer port (Port B), but unlike the Macintosh Portable, the Macintosh PowerBook 100 does not include an external modem port.

An 8-pin miniature DIN connector provides the SCC interface (Port B) to an

external printer or any other standard I/O devices requiring an RS-422 serial interface.

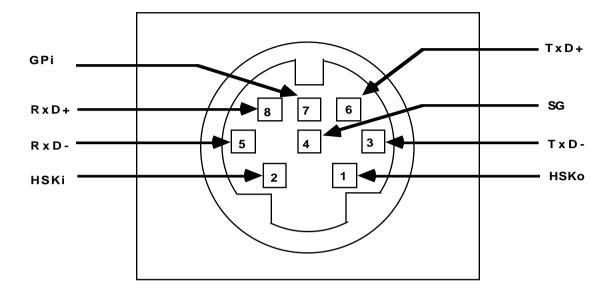
The connector is the same as those currently used on other Macintosh computers.

Table 1-3 shows the pinout for the external printer port. Figure 1-6 is a diagram of the mini-DIN 8 connector.

■ Table 1-3 External printer port pinout

Pin number	Signal name	Signal description
1	HSKo	Handshake output
2	HSKi	Handshake input
3	TxD-	Transmit data –
4	SG	Signal ground
5	RxD-	Receive data –
6	TxD+	Transmit data +
7	GPi	General-purpose input
8	RxD+	Receive data +

■ Figure 1-6 Mini-DIN 8 connector (serial port) diagram



SCSI interface

The SCSI portion of the Combo chip is completely compatible with the SCSI controller chip used on current members of the Macintosh family. It is designed to support the SCSI interface as defined by the American National Standards Institute (ANSI) X3T9.2 committee. In addition to the SCSI portion of the combined SCC/SCSI device, the interface consists of one 40-pin connector for the internal hard disk drive and one

HDI-30 SCSI connector for an external hard disk drive. The SCSI portion of the Combo chip connects directly to the internal and external SCSI connectors and can sink up to 48 mA of current through each of the pins connected to the SCSI bus. The data and control signals on the SCSI bus are active low signals that are driven by open drain outputs.

The Macintosh PowerBook 100 does not supply termination power; therefore, you cannot expect the SCSI bus to remain in a known state if all external SCSI devices are powered off or if no SCSI devices are connected. The normal termination requirement is a 200-ohm resistor to +5 volts and a 330-ohm resistor to ground on each of the active signal lines. The internal SCSI connector is an exception to this termination scheme, however, because the drive supplies its own termination scheme, a configuration consisting of a single-ended

1.3-kilohm pull-up resistor to +5 volts.

Table 1-4 shows the pinouts for internal 40-pin SCSI connector, and Table 1-5 shows the pinouts for the external HDI-30 SCSI connector. Figure 1-7 is a diagram of the external HDI-30 SCSI connector.

■ Table 1-4 Pinout for internal 40-pin SCSI connector

Pin number	Signal name	Signal description
1	/ID0	ID bit 0 to disk drive
2	/ID1	ID bit 1 to disk drive
3	/ID2	ID bit 2 to disk drive
4	DISK.+5V	+5 V to disk drive motor
5	DISK.+5V	+5 V to disk drive motor
6	GND	Ground
7	GND	Ground
8	/DB0	SCSI data bit 0
9	/DB1	SCSI data bit 1
10	/DB2	SCSI data bit 2
11	GND	Ground
12	/DB3	SCSI data bit 3
		(continued)

(continued)

■ Table 1-4 Pinout for internal 40-pin SCSI connector (continued)

Pin number	Signal name	Signal description
13	GND	Ground
14	/DB4	SCSI data bit 4
15	GND	Ground
16	/DB5	SCSI data bit 5
17	nc	No connection
18	/DB6	SCSI data bit 6
19	GND	Ground
20	/DB7	SCSI data bit 7
21	GND	Ground
22	/DBP	SCSI data bit parity
23	GND	Ground
24	+5V/0	+5 V power to disk drive logic
25	/ATN	SCSI attention
26	/BSY	SCSI busy
27	GND	Ground
28	/ACK	SCSI acknowledge
29	/RST	SCSI bus reset
30	/MSG	SCSI message
31	GND	Ground
32	/SEL	SCSI select
33	/I/O	SCSI input/output
34	/C/D	SCSI control or data
35	GND	Ground
36	/REQ	SCSI request
37	GND	Ground
38	GND	Ground
39	DISK.+5V	+5 V power to disk drive motor
40	DISK .+5V	+5 V power to disk drive motor

■ Table 1-5 Pinout for external HDI-30 SCSI connector

Pin number	Signal name	Signal description
1	/SCSI Disk M	Iode SCSI disk mode enabling
signal		G
2	/DB0	SCSI data bit 0
3	GND	Ground
4	/DB1	SCSI data bit 1
5	TERMPWR	Termination power (not supplied by
Macintosh		
		PowerBook 100)
6	/DB2	SCSI data bit 2
7	/DB3	SCSI data bit 3
8	GND	Ground
9	/ACK	SCSI acknowledge
10	GND	Ground
11	/DB4	SCSI data bit 4
12	GND	Ground
13	GND	Ground
14	/DB5	SCSI data bit 5
15	GND	Ground
16	/DB6	SCSI data bit 6
17	GND	Ground
18	/DB7	SCSI data bit 7
19	/DBP	SCSI data bit parity
20	GND	Ground
21	/REQ	SCSI request
22	GND	Ground
23	/BSY	SCSI busy
24	GND	Ground
25	/ATN	SCSI attention
26	/C/D	SCSI control/data
27	/RST	SCSI bus reset
28	/MSG	SCSI message
29	/SEL	SCSI select
30	/I/O	SCSI input/output

■ Figure 1-7 External HDI-30 SCSI connector diagram

2! 2! 27 2! 2! 30	
15 20 2, 22 25 24	
15 14 15 16 17 18	
7 8 9 1(1' 12	
1 2 3 4 5 6]

SCSI disk mode

This feature allows the internal hard disk in a Macintosh PowerBook 100 computer to be mounted and used as an external drive by any desktop Macintosh. You enter the SCSI disk mode by connecting the SCSI Disk Mode Adapter cable between the Macintosh PowerBook 100 computer's external HDI-30 SCSI connector and the desktop computer, and then restarting the system. The adapter cable grounds pin 1 of the HDI-30 connector, causing the Macintosh PowerBook 100 ROM code to look for a prespecified SCSI ID code. (You use the portable CDev in the Macintosh PowerBook 100 Control Panel to preselect the SCSI ID, and this ID is then stored in PRAM (parameter RAM); the default ID is 1 in case the PRAM is lost.) If the SCSI ID is valid, the Macintosh PowerBook 100 disables its SCSI controller chip to eliminate possible bus contention and powers up the internal hard disk. The hard disk remains powered up all the time, and the only thing displayed on the screen of the Macintosh PowerBook 100 is a SCSI icon with the ID number. The desktop system can now use the Macintosh PowerBook 100 hard disk for file transfers, system updates, disk repair, and so on.

If the computer awakes from the sleep mode and the system software senses that the SCSI Disk Mode bit is low, the screen will display a warning message telling the user to disconnect the SCSI Disk Mode Adapter cable because the SCSI disk mode can only be entered when the system is starting up. A system waking from the sleep mode remembers the old SCSI ID of the internal hard disk, and any attempts to access it with a different

ID will not work. There will be contention with the other desktop devices, and the

internal hard disk will not be powered on until the user disconnects the SCSI Disk Mode Adapter cable.

To exit the SCSI disk mode, press the Reset switch or the NMI switch. The Macintosh PowerBook 100 goes into a shutdown mode and is ready to be turned on for normal use.

Sound output interface

The Macintosh PowerBook 100 uses the Apple Sound Chip (ASC) and one Sony sound chip to drive the speaker or the external miniphone jack.

VIA interface

The Versatile Interface Adapter (VIA) in the Macintosh PowerBook 100 provides the same functions as the VIA in the Macintosh Portable. In general, it provides some I/O control, generates useful interrupts, and ensures compatibility with existing Macintosh software.

Video interface

The video interface consists of the DDC, which is similar to the video chip in the original Macintosh Portable, and video SRAM. The DDC generates the vertical and horizontal synchronization pulses necessary to make the flat-panel display work.

The 68HC000 microprocessor views the video interface as a continuous RAM array of 32 KB. The video interface is nominally 16 bits wide but is byte addressable similar to main memory. The first pixel displayed on the screen is the most significant bit of the byte found in the upper-left corner, and the last pixel displayed is the least significant bit of the byte found in the lower-right corner. Pixels displayed in between first and last are addressed in a similar manner. You can think of the video display as a linear array of bits.

Flat-panel display and backlighting

The Macintosh PowerBook 100 uses a 640 x 400-pixel FSTN flat-panel display. The display is supported by on-demand cold cathode fluorescent lamp (CCFL) backlighting similar to that used on the Macintosh Portable. But unlike the Macintosh Portable, display backlighting is not adjusted through the portable CDev but is adjusted manually by the user who simply slides a mechanical control (potentiometer) to adjust the amount of screen brightness. The Power Manager performs an A/D (analog-to-digital) measurement of the voltage output from the control and sends it to a software driver (called .Backlight). The software driver then tells the Power Manager to adjust its pulse-width-modulated (PWM) signal. The backlight circuitry filters the signal to a DC level and sends it to the CCFL inverter to control power to the backlight.

Power Manager

The Macintosh PowerBook 100 Power Manager is physically and functionally identical to the Power Manager used in the Macintosh Portable and described in the Power Manager sections of *Guide to Macintosh Family Hardware*, second edition. For a description of the operating system calls associated with the Power Manager's "sleep" function, see the Power Manager section of *Inside Macintosh*, Volume VI.

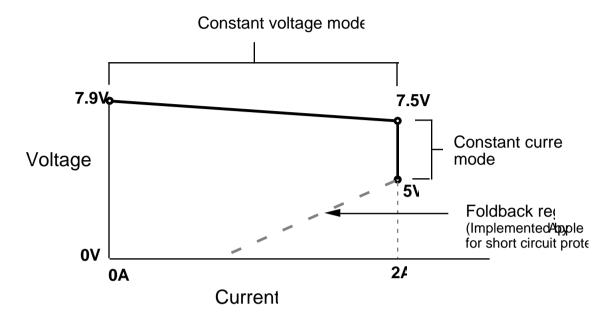
A/C power adapter

The A/C power adapter is designed to typically operate in a constant current and constant voltage mode. This means that the voltage supplied by the power adapter remains relatively constant and fluctuates only slightly (in the range of 7.9 volts to 7.5 volts) as a result of current supplied by the power adapter. Likewise, the current supplied by the power adapter remains relatively constant and fluctuates only slightly (in the range of 1.8 amps to 2.2 amps) as the result of voltage supplied by the power adapter. As the computer's battery approaches its fully charged state, the power adapter changes from a constant current mode to a constant voltage mode, at which point the voltage supplied by the power adapter slowly increases until the battery reaches its fully charged state. See Figure 1-8 for a typical example of A/C power adapter operation.

The A/C power adapter is designed to draw a maximum of 100 microamps of leakage current at 7 volts when A/C power is not supplied to the adapter (that is, the adapter is not plugged in). This design prevents excessive draining of the battery by always maintaining the battery voltage at the computer's power adapter terminal, regardless

of the state of the A/C power adapter (that is, whether the power adapter is or isn't plugged in).

■ **Figure 1-8** Typical A/C power adapter operating range



Modem interface

The main logic board includes a 20-pin modem connector. The location and pin orientation of the modem connector is shown in Figure 1-3. The connector accommodates an Apple modem card or a compatible third-party modem card. This section provides the information you will need if you are designing your own modem card and software.

Modem card electrical interface

The modem card connects to the Macintosh PowerBook 100 through a 20-pin dual in-line socket connector. The data is at CMOS levels (that is, $V_{IL}=0$ to 0.8 V; $V_{IH}=3.5$ to V+; $I_{OL}=1.6$ mA; and $I_{OH}=25$ $\mu A). Table 1-6 provides the pin number, name, type, and description of each signal available at the modem connector.$

■ Table 1-6 Modem connector signals

Pin nu	mber	Signal name	Signal type	Signal description	
1	MODEM.N5		-	that is controlled by host and modem circuitry. Pin 1 may	
float or go		1	to ground 500		
ms fo	llowing negation	n of MODEM	.PWR.	G	
			This signal is not used by the Apple		
mode	m.			, , ,	
2	MODEM.PWI	R Input	Active high	signal from Power Manager;	
see "I	see "Modem			Power-Control Interface"	
later	in this note.				
3	GND		Electrical ground.		
4	/MODEM.BU	SY	Output	Modem busy; active low	
signal asserted by modem				and sent to	
Powe	r Manager when	ever modem	is busy.		
5	US5V		+5 V power	; provides +5 VDC \pm 5% to	
mode				whenever computer has	
powe	r available.				
6	RxD	Output	Receive data	a; data received by modem	
and then				sent to computer via RxD	
pin o	n SCC.				
7	/RI.DETECT	Output	•	active low signal sent to	
Powe			Manager to	indicate that ring is present.	
If computer				is in "sleep" mode,	
assertion of this signal causes awake and power up modem.				computer to	
8	TxD	Input	Transmit da	ta; data and commands that	
are sent modem via TxD pin on SCC.				from computer to	
шоае	iii via 1xD pin o	on SCC.		(continued)	
				(continued)	

■ Table 1-6 Modem connector signals (continued)

Pin	Signal name	Signal type	Signal description	1	
9 sound	MODEM.SOU		Output	Audio output; analog	
sound high-impedance output			signal sent by modem to computer's		
sound circuitry.			· ·	-	
10 whose	/DTR	Input		ready; active low signal ends on state of &D	
comm	and.				
11	MS.ENABLE	Output	Modem sound	l enable; active high signal	
that			modem sends to computer's sound		
circuit	U			whenever modem's	
	monitor is on.	т.,	D 44	1 0 1 1 1	
12	/RTS	Input	Request to sen	id; active low signal sent by	
compu on SC				to modem via RTS pin	
13	RESET	Input	Reset: active h	nigh signal asserted after	
Power		mput		ches – 5 V power to	
modem or any time			Wallager 5 With	modem needs to be reset.	
14	CTS	Output	Clear to send;	active high signal asserted	
by modem			,	as default option,	
inverted, and sent to /CTS pin				on SCC.	
15 /MODEM.INSERT			Output	Modem inserted; active	
	gnal continuous			asserted by	
modei	n, and sent to Po				
		dem card is ii	nstalled in com	_	
16	GND		Electrical grou		
17	GND		Electrical grou		
18	MODEM.5V		+5 V power co	ontrolled by Power	
Manager and				provided to modem. This	
pin will float or go to MODEM.PWR signal goes low				ground 500 ms after (inactive).	
19	/DCD	Output	Data carrier de	etect; active low signal,	
driven by			modem, whose behavior		
depends on state of &C				command.	
20	MODEM.5V		Same as pin 18	8.	

Modem card hardware interface

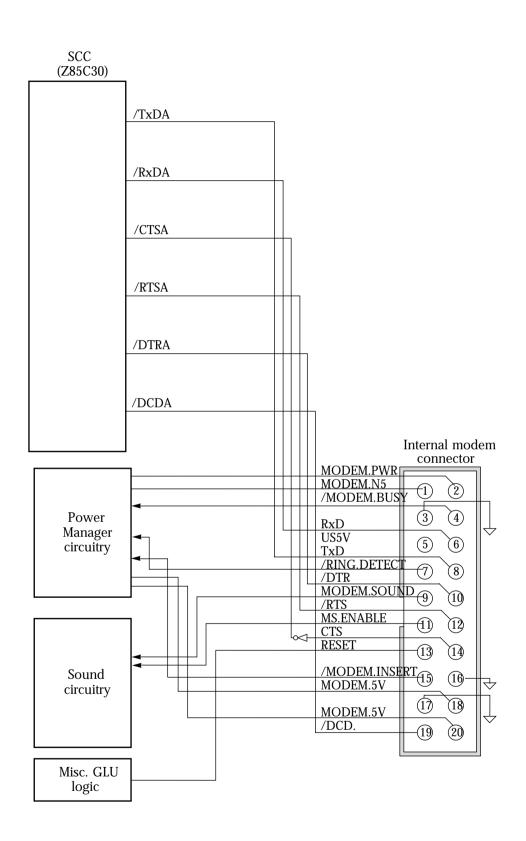
Figure 1-9 shows the hardware interface between a modem card installed in the modem connector and the Macintosh PowerBook 100. Notice that when a modem card is inserted in the internal modem connector, the card is automatically connected to channel A, the modem port.

◆ *Note:* The Macintosh PowerBook 100.does not have an external modem port. The printer port (Port B) is the only external RS-422 serial port on the Macintosh PowerBook 100.

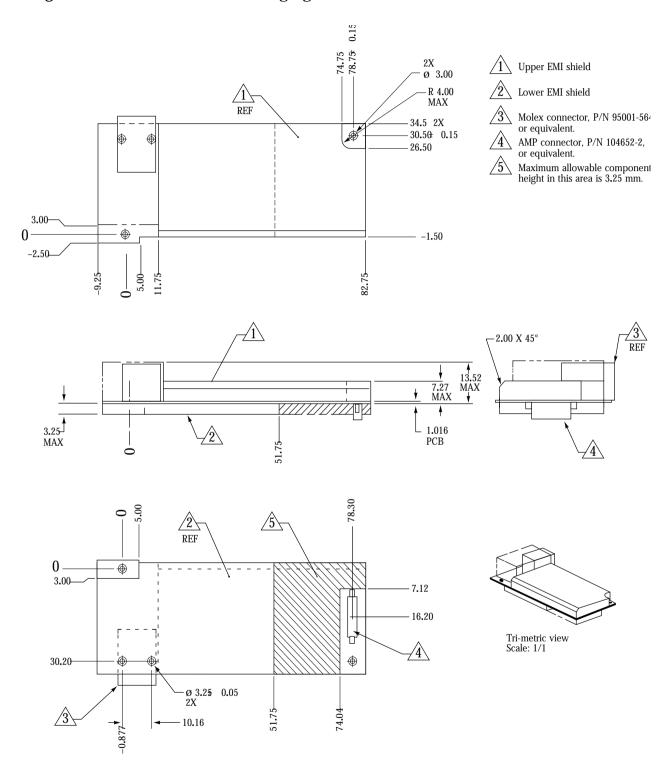
Physical design guide for a modem card

Figure 1-10 is a physical design guide giving you the mechanical specifications you will need, including card size and connector location, to design a compatible modem card for the Macintosh PowerBook 100 computer.

■ Figure 1-9 Interface between the modem card and the computer



■ Figure 1-10 Modem card design guide



Modem power-control interface

Two lines from the computer, US5V and MODEM.5V, provide +5 VDC power to the modem. US5V is always present unless there is a hardware shutdown (following a battery failure or if the computer's back-panel switch is turned off). MODEM.5V power is turned on or off depending on the current power mode of the modem and on how the serial port is used. For example, MODEM.5V is turned off when the computer enters the shutdown or sleep mode and when the serial driver is closed. The modem has two power modes: power on and standby.

Power on: This is the normal operating mode.

Standby: In this mode, MODEM.5V is switched off, all modem circuits are turned off, communication parameters are saved in EEPROM, and the only source of power is US5V. This mode has very low power consumption because only leakage current is drawn.

Two signal lines, MODEM.PWR and /MODEM.BUSY, control power to the modem connector from the Power Manager. /MODEM.BUSY is sent to the Power Manager to prevent the computer from removing power to the modem while the modem is using the communication channel to the computer. A modem card uses the /MODEM.BUSY signal to indicate to the computer that any of the following is true:

- The modem is executing its power-up sequence.
- The modem is off hook (for any reason).
- The modem is executing a command, where command execution begins with <CR> at the end of an AT command sequence or the repeat last command sequence ("a/" or "A/").
- ◆ *Note:* If the modem is executing any self-tests, it is considered to be executing a command and therefore busy.

The Power Manager controls the MODEM.PWR signal. If the Power Manager negates MODEM.PWR (signal goes low), it must wait at least 500 ms before turning off MODEM.5V. This gives the modem sufficient time to save the communication parameters in EEPROM before MODEM.5V is switched off. Three of the modem interface signals, /DTR, TxD, and /RTS, go to ground potential within 50 ns of the negation of MODEM.PWR.

Usually, the Power Manager does not negate MODEM.PWR if the modem has /MODEM.BUSY asserted. There are times, however, when the Power Manager must turn the modem off even though it is busy — for example, when the battery reserve voltage becomes too low. If this occurs, the modem stops its busy activity (for example, goes on hook) and performs the necessary activities for switching to standby. The modem can do one of two things if it is executing a command when MODEM.PWR is negated: either finish executing the command or abort execution and restore the state prior to the command, whichever takes less time.

Modem operation

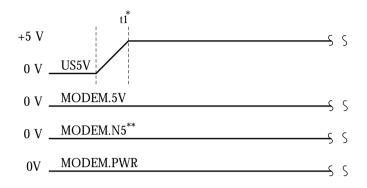
When MODEM.5V power is turned on, the modem leaves the standby mode and enters the power-on sequence. A positive RESET signal from the Power Manager resets the modem's microprocessor and begins the initialization sequence which includes a memory check, the restoration of communications parameters, and the generation of a beep.

If the modem is in standby and detects an incoming call (/RI.DETECT is asserted low), the computer acknowledges the call and powers up the modem to check whether the ring is valid. The Power Manager must power up the modem within 5 seconds after /RI.DETECT is asserted.

Power-up/power-down timing

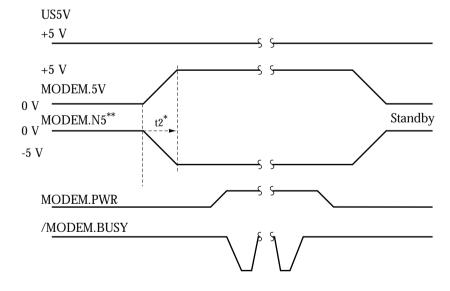
Timing diagrams for the modem's power-up and power-down sequences are shown in Figures 1-11 through 1-13.

■ Figure 1-11 Modem cold-start (initial power-up) timing diagram



 $^{^{*}}$ t1 = 2 ms (typical), 30 ms (maximum). After t1, maximum overshoot is less than 50 mV peak to peak.

■ Figure 1-12 Modem warm-start timing diagram



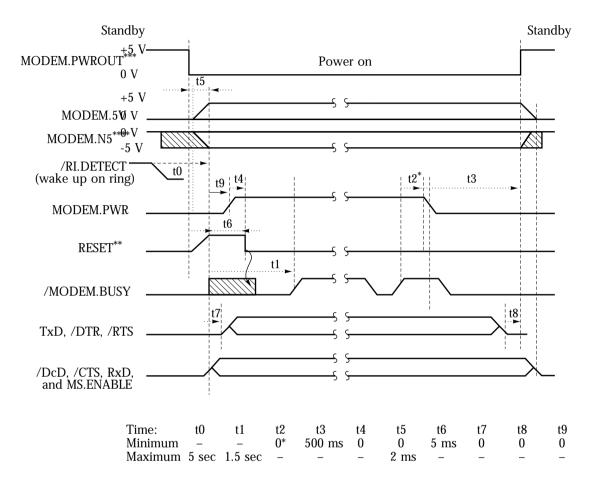
^{*} t2 = 35 ms (typical), 70 ms (maximum). After ?, maximum overshoot is less than 50 mV peak to peak.

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^{**} MODEM.N5, although shown in this diagram, is not used by the Apple modem.

^{**} MODEM.N5, although shown in this diagram s not used by the Apple modem.

■ Figure 1-13 Complete power-up/power-down sequence timing diagram



^{*} t2 > 0 may not be obeyed by the CPU.

^{**} RESET may rise with MODEM.5V, but not before.

^{***} MODEM.PWROUT is an external CPU signal that turns MODEM.5V on and off. US5V is always on and is not shown on this diagram.

^{*****}MODEM.N5, although shown in this diagram, is not used by the Apple modem.

Ring detection

The ring detect interrupt signal (/RI.DETECT) is asserted during most of the A/C cycle of a ring signal and is used to signal the computer that a ring is taking place. Both ringing and pulsing can trigger the ring detector. The microprocessor in your modem must be capable of distinguishing between ring and pulse dialing by detecting the frequency of the incoming signal. If the modem is turned off, the computer can determine whether the /RI.DETECT signal corresponds to a ring or a pulse by powering up the modem and reading the appropriate register or looking for the RING result code.

Modem card power requirements

A modem card must be able to operate on +5 VDC ± 5 percent. This voltage is provided through the modem connector by either the battery or a combination of battery and charger. Typically, a fully operational modem card has an optimized power consumption of 450 mW.

Current drawn from the two +5 VDC sources by the modem should not exceed

- 95 mA typical when in full operation (on line)
- 70 mA typical when in command state
- $\,\blacksquare\,$ 1 μA when in standby mode and there is no incoming ring signal

Telephone line electrical interface

Your modem card design should include a balanced, two-wire telephone interface that meets U.S. (FCC part 68), DOC, and JATE telephone line interface specifications. The physical interface consists of an RJ-11 telephone jack with six slots and four contacts. The two middle contacts are used for the TIP and RING signals; all others are unused.

Modem specifications

The following compilations of signal characteristics are provided for reference only.

Compatibility and modulation

	Full d	uplex			
Standard	Speed (bps)	Modulation	Baud		
CCITT V.22 bis CCITT V.22 1200 CCITT V.21 300/110 Bell 212A 1200 Bell 103 300/110		2400 DPSK FSK DPSK FSK	QAM 600 300/110 600 300/110	600	
Half duplex					
Standard	Speed (bps)	Modulation			
CCITT V.27ter CCITT V.29 9600/7200		4800/2400 half duple	half duplex		

Transmit carrier frequencies

V.22 bis/V.22/212A		7	ransmit carrier	
Originate		1200 Hz		
Answer		2400 Hz		
Bell 103	Mark	Space		
Originate	1270	1070		
Answer	2225	2025		
V.21	Mark	Space		
Originate	980	1180		
Answer	1650	1850		
V.29				
Carrier	1700 Hz			
V.27ter				

Guard tone frequencies and transmit levels (CCITT only)

1800 Hz \pm 20 Hz @ 6 \pm 1 dB below transmit carrier level 550 Hz \pm 20 Hz @ 3 \pm 1 dB below transmit carrier level

Answer tone frequency

V.22 bis/V.22/V.21 2100 Hz

Bell 103/212A 2225 Hz

Received signal frequency tolerance

Offset frequency $\pm 7 \text{ Hz}$

Calling tone

V.25 13 Hz

Keyboard overview

This section describes the keyboard layouts and the Caps Lock modification.

Keyboard layouts

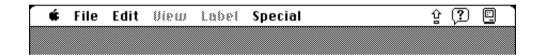
There are two versions of the keyboard, a U.S. (domestic) version with 63 keys and an ISO (international) version with 64 keys. Your application can use the Gestalt Manager to identify the keyboard by checking for a selector identification code of 12. The keyboard layouts are shown in Figure 1-14.

■ Figure 1-14 U.S. and ISO keyboard layouts

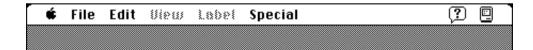
Caps Lock modification

The Caps Lock key on the Macintosh PowerBook 100 does not have a locking position to let a user know the current state of the key. To compensate for this, system software versions 7.0 and greater include a Caps Lock INIT that installs a special system menu containing the international Caps Lock icon. Figure 1-15 shows the international Caps Lock icon that appears next to Balloon Help when the Caps Lock key is in the "down" or engaged position. When you change the state of the Caps Lock key (Caps Lock "up"), the international Caps Lock icon disappears as shown in Figure 1-16, to let you know that the machine is no longer locked to all capital letters.

■ Figure 1-15 Caps Lock "down"



■ Figure 1-16 Caps Lock "up"



Clicking the Caps Lock icon, clicking anywhere else in the menu bar, or tracking over the menu with the cursor will have no effect if the Caps Lock key is engaged (down); the icon will never be highlighted nor will its menu be displayed.

THE APPLE PUBLISHING SYSTEM

This Apple manual was written, edited, and composed on a desktop publishing system using Apple Macintosh computers and Microsoft Word software. Proof and final pages were created on Apple LaserWriter printers. Line art was created using MacDraw® and Adobe Illustrator. PostScript®, the pagedescription language for the LaserWriter, was developed by Adobe Systems Incorporated.

Text type and display type are Apple's corporate font, a condensed version of ITC Garamond[®]. Bullets are ITC Zapf Dingbats[®].