B Mnemonics

Mnemonic	Description
A	
A1-A23	System address bits
ABUS	System address bus
ADX	Address
ARB	Bus arbitor
AUTO FEEDXT	Automatic line feed
B	
BCS	Buffer chip select
BERR	Bus error
BERREN	Bus error enable
BGACK	Bus grant acknowledge
BGC	Bus grant common
BGCAK	Bus grant common acknowledge
BM WINDOW	Bit map window
BMACK	Bit map acknowledge
BMCAS	Bit map column address strobe
BMRAS	Bit map row address strobe
BMR/W	Bit map read/write
BMSEL	Bit map select
BP	Bad parity
BRABUS 0-7	Bit map RAM address bus
BSR0RD	Bus status register 0 read
C	
CAS	Column address strobe
CASDIS	Column address strobe disable
CASEN	Column address strobe enable
CCK	Character clock
CD	Carrier detect
CLR 60HZ INT	Clear 60-Hz interrupt
CLRRFADD	Clear refresh address
CO	Carryout
COMMOSC	Communications oscillator
CPU	Central processing unit
CS	Chip select
CSR	Clear status register
CTS	Clear to send

D

D0-D15	System data bits
DADDWR	Direct memory access address counter write
DATAIN	Data in
DBLDEN	Double density
DBUS	System data bus
DCNTCS	Direct memory access word counter chip select
DCS	Disk controller select
DD	Disk data bus
DDBUS 0-7	Disk data bus 0-7
DDRIVE0	Disk drive 0
DFAULT	Data fault
DIALER EN	Dialer enable
DIALER TXD	Dialer transmit data
DINDEX	Disk index pulses
DISPEN	Display enable
DKBG	Disk bus grant
DKBGA	Disk bus grant acknowledge
DKRQ	Disk bus request
DMA	Direct memory access
DMAEN	Direct memory access enable
DMAR	Direct memory access read
DMAR/W	Direct memory access read/write
D/N CONNECT 1	Dial network connected to line 1
DREADY	Drive ready
DRQ	Data request
DRUN	Data run
DSCOMPL	Disk seek complete
DSR	Data set ready
DT DET	Dial tone detect
DTACK	Data transfer acknowledge
DTRK 0	Disk track 0

E

EE	Error enable
EN	Enable
ENCAS	Enable column address strobe
ENRAS	Enable row address strobe
EXP0-3BG	Expansion board 0-3 bus grant
EXP0-3RQ	Expansion board 0-3 request

F

FC	Function code
FDCS	Floppy disk chip select
FDDRIVE0	Floppy disk drive 0
FDDRQ	Floppy disk data request
FDDRQL	Floppy disk data request latched
FDINDEX	Floppy disk index
FDINTRQ	Floppy disk interrupt request
FDMOTOR	Floppy disk motor enable
FDPRESENT	Floppy disk present
FDRD	Floppy disk read
FDRE	Floppy disk read enable
FDREADY	Floppy disk ready
FDRST	Floppy disk reset
FDTRACK 0	Floppy disk track 0
FDWE	Floppy disk write enable
FDWPRT	Floppy disk write protect
FF	Flipflop
FWR	Fast write

G

GCRWR	General control register write
GND	Ground
GSR	General status register
GSRRD	General status register read

H

HAL	Hard array of logic
HDBCS	Hard disk buffer chip select
HDBRDY	Hard disk buffer ready
HDCS	Hard disk chip select
HDCTRLWR	Hard disk controller write
HDINTRQ	Hard disk interrupt request
HDL	Head load
HDRE	Hard disk read enable
HDRST	Hard disk reset
HDSEL0-2	Head select bits 0-2
HDSETRELAY	Handset relay
HDWDATA	Hard disk write data
HDWE	Hard disk write enable
HSYNC	Horizontal synchronization

I

ID	Identify
IDMAR/W	Identify DMA read/write operation
INIT	Centronics reset and initialize control signal
INT	Interrupt
INTA	Interrupt acknowledge
INTRQ	Interrupt request
I/O DTACK	I/O data transfer acknowledge
I/OEN	I/O enable
I/ORQ	I/O request
IPL	Interrupt priority level

K

KADDR	Kernel address
KBEN	Keyboard enable
KBINT	Keyboard interrupt
KBRST	Keyboard reset
KBRXD	Keyboard receive data
KBTXD	Keyboard transmit data

L

L1 A-LEAD	Line 1 A-lead
L1 HOLD	Line 1 hold
L1 MODEM	Line 1 modem
L1 RING	Line 1 ring
L2 A-LEAD	Line 2 A-lead
L2 HOLD	Line 2 hold
L2 MODEM	Line 2 modem
L2 RING	Line 2 ring
LA	Latched address
LA BUS	Local address bus
LBERR	Latched bus error
LCAS	Lower column address strobe
LDS	Lower data strobe
LINE SEL2	Line select 2
LMA	Latched map address
LMUXPAR	Lower multiplexed parity
LPACK	Line printer acknowledge
LPARIN	Lower parity interrupt
LPAROUT	Low parity output

L (continued)

LPBUSY	Line printer busy
LPDATAWR	Line printer data write
LPINT	Line printer interrupt
LPNOPAPER	Line printer out of paper
LPS	Latched page status
LPSELECT	Line printer select
LPSTATUSRD	Line printer status read
LPSTROBE	Line printer strobe
LWE	Latched write enable

M

MA	Mapped address
MA BUS	Mapped address bus
MCK	Modem clock
MCKSEL	Modem clock select
MEMEN	Memory enable
MFM	Modified frequency modulation
MMU	Memory management unit
MMUERR	Memory management unit error
MMUWR	Memory management unit write
MMUWREN	Memory management unit write/read enable
MMUWREND	Memory management unit write/read enable data
MODEM CK SEL	Modem clock select
MODEM RXCK	Modem receive clock
MODEM RXD	Modem receive data
MODEM TXCK	Modem transmit clock
MODEM TXD	Modem transmit data
MODEMCS	Modem chip select
MOSEN	Processor data transceiver enable
MPU	Microprocessing unit
MRAEN	Map RAM enable
MRAMEN	Map RAM enable
MREG WR	Miscellaneous control register write
MSG WAIT	Message waiting
MW	Memory write

N

NMI	Nonmaskable interrupt
NPC	Nonprocessor cycle
NRFBGC	Nonrefresh bus grant common

O

OSCENB	Oscillator enable

P, Q

PA BUS	Processor address bus
PAL	Programmable array of logic
PAS	Processor address strobe
PCK	Processor clock
PCLK	Processor clock
PD	Pumpdown
PD BUS	Processor data bus
PF	Page fault
PIE	Parity interrupt enable
PRD1-8	Line printer data bits

R

RAMEN	RAM enable
RAS	Row address strobe
RD	Read
RFBG	Refresh bus grant
RFRQ	Refresh bus request
ROMEN	Read only memory enable
RTCALE	Realtime clock address latch enable
RTCD0-4	Realtime data bits
RTCLE	Realtime clock latch enable
RTCR/W	Realtime clock read/write
R/W	Read/write

S

SUPV	Supervisory mode

T

T30-T120	Memory timing delay outputs in nanoseconds
TFER	Transfer request
TPD0-7	Serial controller data bus

U, V

UCAS	Upper column address strobe
UDS	Upper data strobe
UIE	User interrupt error
U/OERR	Disk DMA underrun or overrun error

W

WE	Write enable
WR	Write

X, Y, Z

XI/O EN	Expansion I/O enable
XPERR	Expansion parity error