

SERVICE MANUAL

HD SERIES MONITOR



**Electronic
Display
Division**

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5-017-1042

REV A

June, 1980



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Display
Division**

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PART I

OPERATING DATA

This part of the service manual provides data concerning the specifications, installation and operation of the HD Series CRT Display.

Section 1

GENERAL INFORMATION

1.1 MONITOR DESCRIPTION

The HD Series CRT display is designed for high density display of up to 6000 characters (nominal) to be used in word processing or phototypesetting applications. Either 15" or 17" screens may be configured in vertical (page) or horizontal (conventional) formats. A full typewritten page may be displayed with either size or either format option.

Some of the other features of the HD Series CRT display are:

1. An elevated line rate that is selectable from 26 to 36 kHz.
2. Regulated low voltage supplies with foldback current limiting.
3. Dynamic focus circuitry.
4. Standard P4 and P39 phosphors available with other phosphors available upon request for special applications.
5. Circuit components mainly located on three printed wiring assemblies (PWA), the low voltage PWA, the video PWA and the horizontal and vertical PWA.
6. Displays may be operated with either standard or inverted video.
7. Wire frame chassis with a 5° faceplate angle for both vertical (page) and horizontal (conventional) format frames.

1.2 CUSTOMER INPUT SIGNAL REQUIREMENTS AND CIRCUIT CHARACTERISTICS

1.2.1 Input Signal and Power Connector

24 pin male connector, Molex P/N 03-06-1242 (Ball E.D.D. P/N 1-034-0378).
Required pins are: Molex P/N 02-06-1101 with 18-24 AWG (Ball E.D.D. P/N 1-034-0289).

or: Molex P/N 02-06-1131 with 24-30 AWG.

1.2.2 Video Input Signal Requirements and Video Amplifier Characteristics

Amplitude: -1.75 V to -0.9 V (ECL level for ECL, digital video PWA)
Bandwidth: no more than 3 db down at 50 MHz minimum
Rise/Fall Times; 7 ns at 35 Vp-p
Video Input Impedance: 270 Ω \pm 5% min. resistance, 30 pF max. shunt capacitance.
Inverted Video: provided by reversing video input polarity from that of conventional video.

1.2.3 Horizontal Sync Signal Requirements and Circuit Characteristics

Input Levels: Low (logic 0) 0 to 0.5 VDC
High (logic 1) 2.4 to 5.5 VDC
Horizontal Frequency: selectable from 26 through 36 KHz, frequency tolerance $\pm 3\%$.
Polarity: may be either positive or negative going
Deflection Flyback Time: minimum 7 μ s line blanking
Input impedance: 1 k Ω minimum resistance; 60 pF maximum shunt capacitance

1.2.4 Vertical Sync Signal Requirements and Input Characteristics

Nominal Vertical Deflection Rate: selectable from 40 through 80 Hz
Polarity: negative going
Deflection Flyback Time: minimum 500 μ s field blanking
Input Impedance: 1 k Ω minimum resistance; 60 pF maximum shunt capacitance

1.3 CUSTOMER INPUT POWER REQUIREMENTS

Frequency: 50/60 Hz
AC Voltage: See interconnection diagram, Figure 6.1.
Nominal Power: 105 watts at 36 kHz, conventional scan

1.4 CRT DISPLAY CHARACTERISTICS

1.4.1 Display Characteristics

CRT Diagonal Measure: 15 or 17"
U.L. Implosion Protection: shell bond
High Voltage (nominal): 18 kV

1.4.2 Resolution

6336 characters
Page (vertical) format: 98 characters by 66 lines
Conventional (horizontal) format: 132 characters by 48 lines
Character Cell: 11 X 16 dots

1.4.3 Light Output

P4: 40 foot lamberts
P39: 20 foot lamberts

1.4.4 Linearity

Within 12 dots horizontal or vertical at 120 dots per inch reference

1.4.5 Geometry

Within $\pm 1\%$ of vertical height

1.5 ENVIRONMENTAL SPECIFICATIONS

	<u>Operating Range</u>	<u>Non-operating Range</u>
Ambient Temperature	10°C to 40°C	-40°C to 65°C
Humidity	5% to 90%(non-condensing)	5% to 90%(non-condensing)
Altitude	10,000 ft. max.	40,000 ft. max.

1.6 PHYSICAL DIMENSIONS

1.6.1 Outline Drawing

Refer to Figure 1.1

1.6.2 Weight

HD - 15"(both formats) 271bs. (12.2 kg.)

HD - 17"(both formats) 301bs. (13.6 kg.)

1.7 X-RADIATION

The HD Series CRT display meet the x-radiation requirements as set forth in UL Standard 478 (Electronic Display Processing Units and Systems).

1.8 USER OPERATING CONTROLS

An external brightness control is available. The brightness control R1 is connected to the horizontal and vertical PWA via pins 1, 3, and 4 of J107. Its value should be 50 k Ω .

1.9 SERVICE CONTROLS

During normal operation the following internal controls do not require adjustment. The controls are listed according to the PWA they are located on. For the location of the printed wiring assemblies refer to Figure 1.2.

Low Voltage PWA

Voltage Adjust

Voltage Limit Adjust (Set in factory)

ECL, Digital Video PWA

Contrast

Horizontal and Vertical PWA

Horizontal Oscillator Adjust

Horizontal Data Centering

Width

Horizontal Dynamic Focus

DC Focus

Vertical Height
Vertical Centering
Maximum Brightness Limit

1.10 GENERAL SALES OFFICES

Contact one of our general sales offices listed below for more information:

Campbell, California (408) 374-4120
Upland, California (714) 985-7110
Downers Grove, Illinois (312) 960-4434
Burlington, Massachusetts (617) 273-0608
Ocean, New Jersey (201) 922-2800
Lewisville, Texas (214) 436-2383

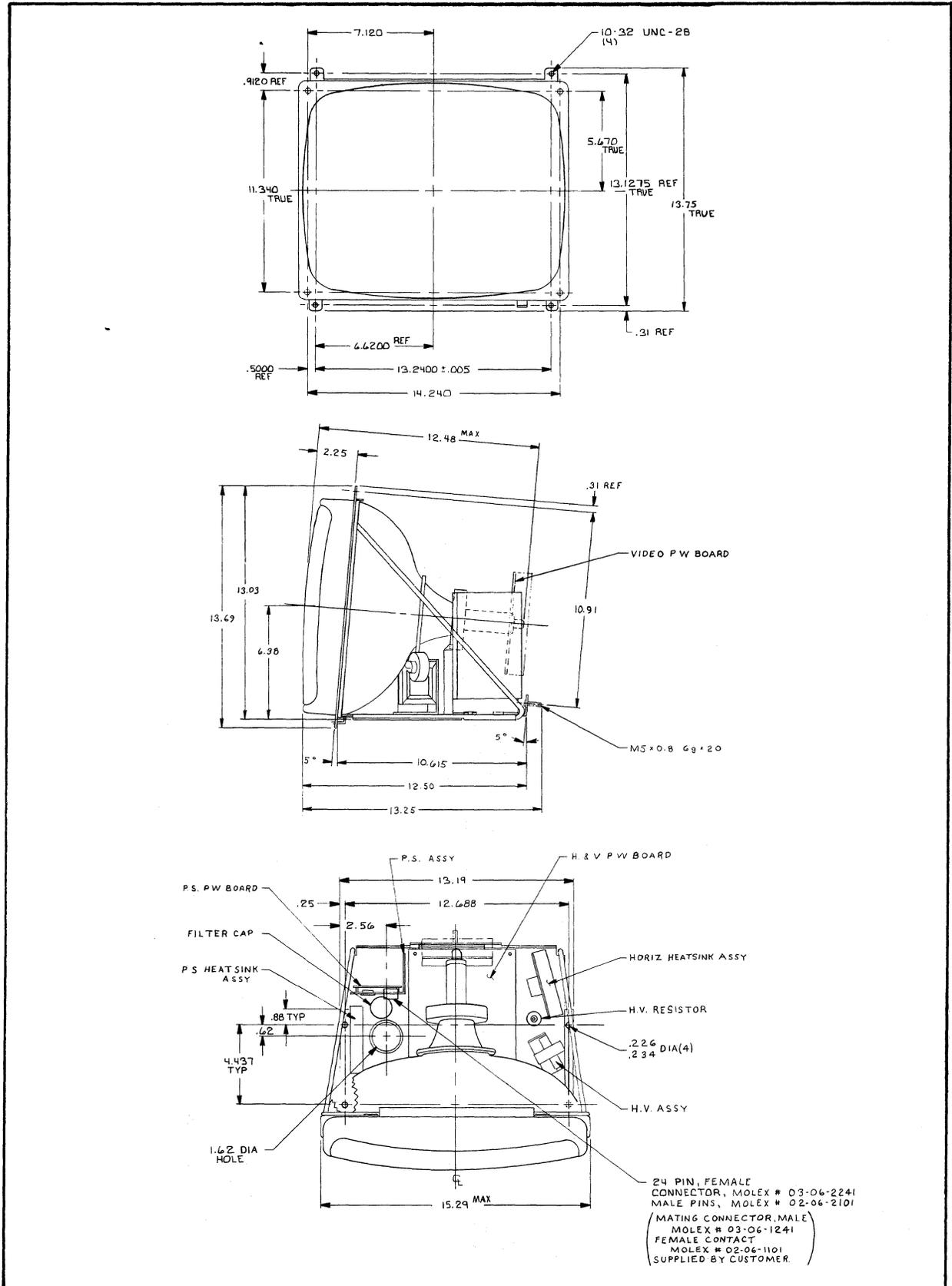


Figure 1.1 Outline Drawing

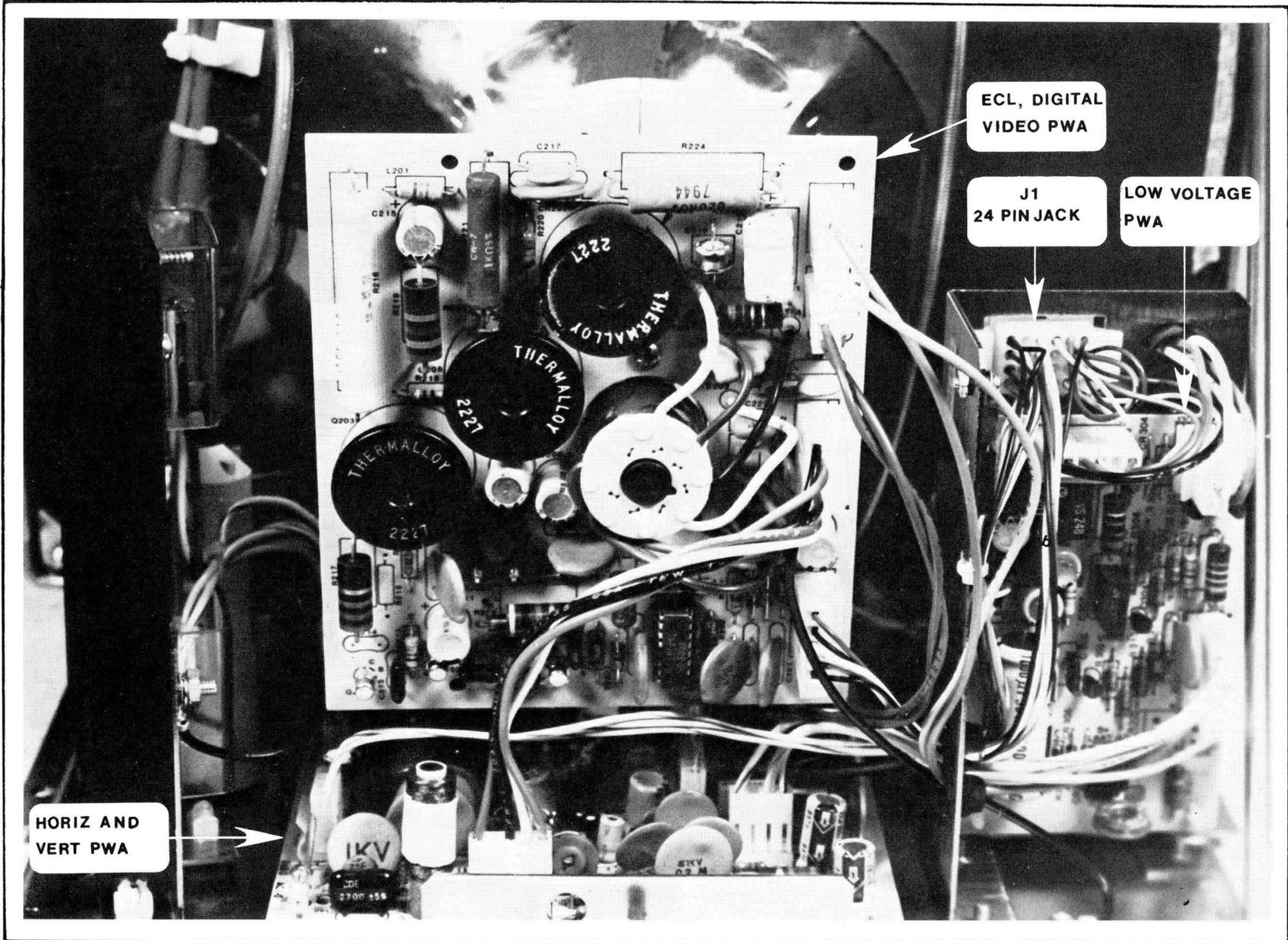


Figure 1.2 PWA Location

Section 2

INSTALLATION

2.1 MECHANICAL

Refer to Figure 1.1 for outline drawing. The HD Series CRT display provides four 15/64" holes on the bottom of the chassis for mounting of the unit.

2.2 ELECTRICAL

The HD Series CRT display operates from ac voltages from an external transformer if a 24 pin jack is being used to input the signals. Refer to the interconnection diagram, Figure 6.1, for the specific voltages that must be applied to the monitor.

2.3 LOCATION

The monitor operates satisfactorily in an area where the ambient temperature is from 10°C to 40°C.

2.4 GROUNDING TECHNIQUES

2.4.1 Power Ground

Connect ac power ground to pins 22 and 23 of J1, the 24 pin jack. These two pins connect to pin 2 of J301 on the low voltage PWA.

2.4.2 Signal Ground

The ECL, digital video PWA uses a floating ground that is connected to pin 2 of J205. DO NOT USE THIS AS CHASSIS GROUND.

Section 3

OPERATION

3.1 GENERAL

After the direct drive signals (consisting of horizontal sync, vertical sync, and video) and power have been applied to the monitor the internal contrast and external brightness controls are adjusted for the best looking displays.

3.2 BRIGHTNESS CONTROL

The brightness control is used to adjust the raster just beyond visual cutoff. Maximum contrast ratio can then be obtained.

3.3 CONTRAST CONTROL

The contrast control is used to vary the difference in brightness between the dark and light portions of the picture as dictated by the peak luminance specification.

PART II

SERVICE DATA

Sections 4 through 6 are qualified service technicians.

The HD Series CRT Display has no end user serviceable parts inside.

WARNING

*SERVICING OF MONITOR SHALL BE
DONE ONLY BY QUALIFIED SERVICE
TECHNICIANS USING PROPER SAFETY
PROCEDURES AND SAFETY PRECAUTIONS.*

SECTION 4

CIRCUIT DESCRIPTION

For block diagram refer to Figure 4.3. For schematics refer to Section 6.

4.1 LOW VOLTAGE PWA

4.1.1 General

The low voltage regulator PWA supplies a regulated +70 VDC and +35 VDC for both the digital video, ECL PWA and the horizontal and vertical PWA. The low voltage regulator PWA also provides foldback current limiting. Power inputs of either 100, 120, 220 or 240 VAC can be applied to the monitor. See the interconnection schematic, Figure 6.1, for details about power input connections.

4.1.2 +70 VDC Output

Low voltage, transformer T1 applies the ac line voltage to full wave, bridge rectifier CR301 through J301-2 and J301-4. Filter capacitor C1 filters the unregulated dc voltage out of CR301 to produce a relatively constant +80 VDC. Diode CR304 and resistors R303 and R304 keep the base-emitter voltage on pre-regulator Q301 constant so that Q301 acts as a constant current source for Q302, Q303, and Q304. R305 sets the magnitude of the constant current. Diode CR304 also provides temperature compensation for the base-emitter junction of Q301.

Darlington pair configuration transistors Q303 and Q6 are the series control elements for the regulator. Transistor Q303 supplies the base current drive to Q6 necessary to maintain the required output load current. Together Q303 and Q6 interpret the signal from error amplifier Q302 and make the necessary adjustment in their conduction level to keep the +70 VDC output constant.

Zener diode VR301 supplies a +24 VDC reference voltage for the emitter of error amplifier Q302. Voltage adjust R314 taps a voltage to the base of Q302 that is proportional to the +70 VDC output through the voltage divider network that consists of R313, R314, R315, R316, CR303 and CR305. This positive voltage and the +24 VDC reference voltage at the emitter of Q302 determine the bias on the base-emitter junction and, therefore, the current through Q302. Because Q301 supplies a constant current and foldback current limiter Q304 is normally off, the variation in current through Q302 directly determines the amount of current in Q303 and Q6 and, consequently, the +70 VDC output. Capacitor C305 provides negative ac feedback from the collector to the base of Q302 to prevent high frequency oscillation. Diodes CR303 and CR305 provides temperature compensation for the base-emitter junction of Q302. Voltage limit adjust R316 sets the upper limit to the +70 VDC output. R318 and C307 provide high frequency feedback to Q302 for better high frequency regulation characteristics.

Foldback current limiter Q304 is normally off because of the base bias set by R309 and R311. When the output load impedance decreases to such an extent that the output load current through R312 becomes excessive, the additional voltage drop across R312 causes the voltage to the base of Q304 to increase and the voltage to the emitter of Q304 to decrease.

This forward biases the base-emitter junction of Q304, turning the transistor on and causing it to draw some of the constant current out of Q301.

This decreases the current available to Q303 and Q6 tending to turn them off, increasing their series resistance and, therefore, decreasing the regulator output voltage and current. When the load current decreases sufficiently, Q304 turns off, and the regulator returns to normal operation. The RC time constant of R310 and C306 inhibits foldback current limiter Q304 during the initial surge current of monitor turn-on.

4.1.3 +35 VDC Output

The center tapped voltage from low voltage, transformer T1 feeds through J301-6 and R301 to the collector of transistor Q5. Diode CR302 provides arc protection for Q5. Capacitor C301 filters it to produce a relatively constant dc voltage at the collector of Q5. Resistors R302 and R319 form a voltage divider network that produces a voltage at the base of Q305 that is proportional to the regulated +70 VDC output. The voltage at the emitter of Q5 is the +35 VDC regulated output. Capacitor C302 filters the circuit. C303 and C304 provide a low impedance to the base of Q5.

4.2 ECL, DIGITAL VIDEO PWA

4.2.1 General

The ECL, digital video PWA accepts an ECL (emitter coupled logic) level, video signal converts it to a TTL (transistor-transistor logic) level, video signal, amplifies it and finally applies it to the cathode of the CRT for modulation of the electron beam.

4.2.2 ECL to TTL Conversion

The ECL level, digital, video signal inputs differentially through J205-5 and J205-6 to pins 11 and 10 of U201, respectively. Integrated circuit U201 is an ECL level (-1.75 V to -0.9 V) to TTL level (0.2 V to 5.0 V) translator. Diodes CR201, CR202, CR205 and CR206 protect U102 and the external input circuits against voltage transients. Diodes CR203 and CR204 provide dc bias for the ECL input. The use provides the -5.2 VDC supply that routes through J205-3 to pin 8 of U201. Resistor R204 and zener diode VR201 drop down the +35 VDC supply to +5.1 VDC for application to pin 9 of U201. Capacitors C201, C202, C203, C204 and C205 filter the various voltages involved in the translator circuitry.

4.2.3 Digital Video Amplification

The TTL level, digital video signal outputs from pin 12 of U201 and feeds through speed-up capacitor C208 and resistor R207 to the base of transistor Q201. The signal appears inverted and amplified at the collector of Q201. It feeds through speed-up capacitor C210 and resistor R210 to the base of Q202. The signals appear at the base of Q204 inverted and amplified after feeding through speed-up capacitor C213 and resistor R213. The supply voltage of +12 VDC for Q201 and Q202 feeds through R209 and R212 to the respective transistor collectors. Zener diode VR202 regulates the +12 VDC and capacitors C206 and C207 filter it. Resistors R206 and R208 are dropping resistors.

Transistors Q203 and Q204 connect in cascode arrangement. Transistor Q203 amplifies and inverts the digital video signal at its base. The signal at its collector feeds through R215, R217 and C124 to the emitter of Q203 and then to the collector of Q203 with no inversion in polarity. Resistor R218 couples the signal to the base of Q205. Emitter followers Q205 and Q206 provide isolation for the video circuitry and current gain for driving the CRT. The signal at the emitter of Q206 couples through R225 to the cathode of the CRT where it modulates the electron beam.

The supply voltage for transistors Q203, Q204, Q205 and Q206 is +70 VDC; it routes into the PWA from J201-4. Zener diode VR203 regulates the +20 VDC that gain adjust R211 applies to the base of Q203 through R214. The setting of R211 determines the white level of the digital video signal. Capacitor C214 and inductor L201 provide high frequency peaking. Because the impedance of C214 decreases with increasing frequency it shunts higher frequencies around R217. Because the impedance of inductor L201 increases with frequency, it helps to maintain a constant collector load for Q203 by compensating for stray output capacitance that becomes significant with increasing frequency. Diode CR207 protects Q206 against arcing in the CRT, and subsequent high voltage transients, by maintaining the collector-to-emitter voltage of Q206 at a maximum of about +70 VDC. Arc capacitors C218, C223, C224, C225 and C226 short any high voltage transients to ground to protect external circuitry. The filament voltage of 6.3 VAC for the CRT enters the PWA from the high voltage transformer T2 via J201-1 and J201-2. It then outputs via solder points E201 and E208 to the CRT socket.

C219 and R226 provide current limiting to extinguish arc capacitor C218 if it arcs. R227 and C220 provide high frequency ac ground for grid G1 of the CRT. C221 and C222 provide ac bypassing for grids G1 and G2. R231 is a voltage dropping resistor for the filament supply to the CRT.

4.3 HORIZONTAL AND VERTICAL PWA

4.3.1 General

The horizontal and vertical PWA performs the following functions:

1. Synchronization of horizontal and vertical oscillators to produce a stable picture.
2. Variable delay of horizontal sync pulse for proper timing and horizontal data centering.
3. Overvoltage, x-ray protection through use of Schmidt trigger.
4. Horizontal frequency adjustment.
5. Horizontal width control.
6. DC focus control.
7. Dynamic horizontal focus control.
8. Vertical height control.
9. Vertical centering.

10. Brightness control.

11. Maximum brightness limit control.

4.3.2 Horizontal Section (Refer to Figure 4.1 for Timing Diagram)

NOTE: All voltages mentioned below are approximate and vary 10 to 20% depending on the horizontal frequency of the monitor. All signals are periodic at the horizontal frequency. For example, if the horizontal frequency is 35 KHz, the period of the signal is 28.6 μ s.

The horizontal sync pulse inputs through J104-2, coupling capacitor C101 and resistor R103 to the base of Q101. To trigger the horizontal oscillator a negative polarity sync pulse is required at the input side of C104. To get this a jumper connects the input side of C104 to either the emitter or the collector of Q101, the specific connection depending on whether the input horizontal sync has positive or negative going pulses, respectively. Capacitor C104 and resistor R106, R107 and R187 differentiate the horizontal sync pulse. The trailing edge of the pulse produces a negative spike of about 8 V that triggers the horizontal oscillator, Q110 and Q111. Transistor Q110 and Q111 are arranged to act as a unijunction transistor in relaxation oscillator configuration. The negative spike at the base of Q110 and the collector of Q111 turns these "normally off" transistors on. This effectively grounds the top of C102 and almost instantaneously reduces the voltage across this capacitor to zero. As soon as the voltage at the base of Q110 reverses, C102 begins to charge up to the supply voltage of +35 V through R108 and R109. When the voltage across C102 reaches 8 V, however, another horizontal trigger spike turns on Q110 and Q111 and the cycle repeats. By varying the supply voltage to the emitter of Q110, horizontal frequency adjust R108 varies the charging rate of C102, and, thereby, the free-running frequency of the oscillator. This determines the peak-to-peak amplitude of the voltage ramp before it is reset to zero when Q110 and Q111 are triggered back on.

Integrated circuit timers U101 and U102 provide a variable delay for proper timing between horizontal scanning current and video application to the CRT cathode. A fixed amount of delay comes from U102; the delay introduced by U101 is made variable by horizontal data centering control R111, whose effect on the display is to move the data on the raster to the left or to the right. More delay causes the data to be shifted to the left on the raster and vice versa for less delay. Resistors R110 and R113 and capacitor C103 differentiate the ramp voltage at the emitter of Q110 producing a negative going spike of about 6 V at pin 2 of integrated circuit, timer U101. The timer acts as a monostable multivibrator triggered at the horizontal rate. A negative voltage spike, that is 1/3 less than the supply voltage at pin 6 or less than about 3.7 V, sets an internal flip-flop in the timer and causes the output at pin 3 to go high. The negative voltage spike also removes a short applied across C105 and C106 at pin 7 of U101. This allows the voltage across C105 and C106 to increase exponentially through R111 and R112. After a time equivalent to 1.1 (R111+R112) (C105+C106) or about 1/3 to 2/3 a horizontal line period depending on the setting of R111, the voltage at pin 6 and pin 7 reaches 2/3 the supply voltage at pin 8 or about

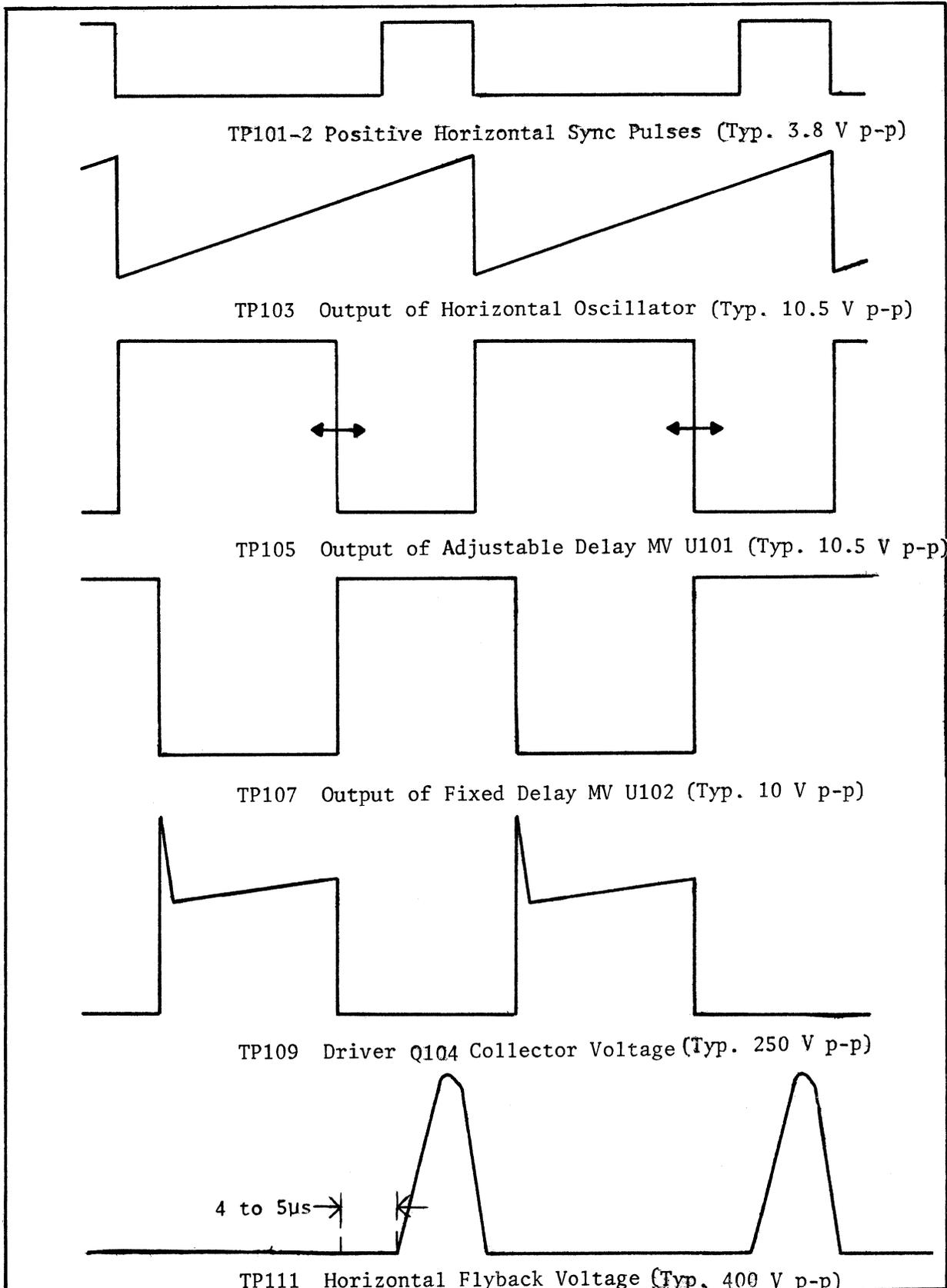


Figure 4.1 Horizontal Timing

7.3 V. This causes the internal flip-flop to be reset, discharges C105 and C106, and causes the output at pin 3 to return to its normally low state. C107 has a voltage across it equal to 2/3 the supply voltage at pin 8 or about 7.3 V; the comparator circuit inside the timer uses this voltage as a reference.

C108 and R116 differentiate the 12 V positive gate pulses at pin 3 of U101 producing positive and negative voltage spikes at pin 2 of U102. As with U101 integrated circuit, timer U102 is connected as a one shot multivibrator. A negative voltage spike that goes below 3.7 drives the output at pin 3 high. The output stays high for a time equivalent to $1.1(C109)(R117)$ to about 1/2 the horizontal line period. At this time the charge on C109 reaches 7.3V and the output goes back to its normally low state. C110 stores a reference voltage of 7.3 V.

The positive output gate from pin 3 of U102 couples through R121 to the base of horizontal driver and buffer Q104 causing the transistor to switch between cut-off and saturation with approximately a 50% duty cycle. This switching generates a 100 V square wave at the collector of Q104 due to the inductive load presented by driver transformer T101. The 40 V overshoot that occurs on the positive edge of the square wave when Q104 cuts off results from the inductive kickback of T101. Speed-up diode CR103 conducts when Q104 is turning off to aid in removing stored base charge and, thereby, provide faster switching.

The signal at the top of the secondary of T101 is an in-phase, voltage stepped down version of approximately 10 V p-p of the signal at the collector of Q104. The signal feeds through R134-J101-1 and R133-J101-5 to heat sink mounted, matched horizontal output transistors, Q1 and Q2, respectively. When Q104 conducts, energy stores in T101. The voltage at the secondary is phased so that Q1 and Q2 are off. When the primary current of T101 is interrupted by Q104 cutting off, the secondary voltage reverses polarity. Q1 and Q2 conduct due to the positive voltage at their bases. Their collector currents slowly increase in a sawtooth pattern during the remaining period of the horizontal line scan. The typical combined collector current of Q1 and Q2 that goes to the horizontal deflection yoke is about 8 A depending on the length of horizontal scan. Transformer T102 equalizes the switching times and currents of Q1 and Q2 providing correcting feedback between their emitters.

The collector current of Q1 and Q2 flows through the horizontal deflection yoke via J101-2 and J101-6, respectively. The part of the adjustable width control L101 that is placed in series with the horizontal deflection yoke varies the amount of deflection current that flows through the yoke and, thereby, the width of the raster. Part of the width control L101 is placed in parallel with the horizontal deflection yoke to maintain a constant load to Q1 and Q2 as the horizontal width is varied; this helps maintain a constant high voltage to the CRT anode. C125 provides "S" shaping of the horizontal deflection current waveform to compensate for "stretch" at the left and the right side of the CRT; it also prevents dc currents from flowing in the width coil and the yoke. The metal foil, linearity sleeve that is inserted between the yoke and the CRT provides linearity correction at the beginning of the horizontal scan.

4.3.3 Horizontal Deflection Theory

With no current going through the horizontal deflection yoke the electron beam is

approximately at the middle of the CRT screen. When Q1 and Q2 conduct upon application of the horizontal drive pulse, electrons flow from ground up through Q1 and Q2 and down through the horizontal deflection yoke. This deflects the electron beam from the middle to the right side of the screen. When the horizontal drive pulse goes low, Q1 and Q2 turn off, horizontal scan ends, and retrace begins.

The resonant circuit made up primarily of the horizontal deflection yoke and C118 starts to ring at its natural frequency and generates a positive flyback voltage pulse of about 340 V p-p and 6 μ s duration. The current through the yoke, which was maximum at the end of scanning, decreases to zero as the stored energy in the magnetic field transfers to C118 trying to keep the current through the yoke in the same direction. When the current becomes zero, the electron beam is again in the middle of the CRT screen. At this point C118 is maximally charged positive. It begins to discharge and causes electrons to flow up through the horizontal deflection yoke. This deflects the electron beam to the left side of the screen. When C118 discharges completely the electron beam is at far left of the screen and the current through the yoke is maximum. Because the capacitor can no longer supply energy, the yoke's magnetic field starts to collapse, the current through the yoke starts to decrease and the electron beam starts to move toward the middle of the CRT screen. At this point the polarity on the yoke reverses with it being negative at E103. Therefore, efficiency diodes CR104 and CR105 conduct until the electron beam is near the middle of the screen. Just before the current reduces to zero, transistors Q1 and Q2 receive another horizontal drive pulse and starts to conduct, the current through the yoke reverses, the electron beam starts to move from the middle to the right of the screen and another cycle starts.

4.3.4 "Turn-on" and "Turn-off" Protection Circuit

The unused reset function at pin 4 of U101 connects via R119 to the intersection of zener diodes VR101 and VR104. This inhibit circuit provides protection against random drive pulses to the horizontal output transistors Q1 and Q2 during "turn-on" and "turn-off". Normally several ac cycles are necessary after "turn-on" to bring the +35 VDC line and the +70 VDC line up to their operating voltages. Because of the selected component values for this inhibit circuit, one-shot delay multivibrator U101 is disabled until the regulator voltage exceeds about 1/2 its normal voltage. This dc supply voltage is adequate for stable operation of the horizontal circuit.

During "turn-off" this inhibit circuit also offers protection against CRT spot burn. After ac power is removed the regulator filter capacitors are rapidly discharged by the load current, so that the two supply line voltages decay rapidly to less than 1/2 their normal output. At this point, U101 becomes disabled. Consequently, the horizontal output transistors Q1 and Q2 and associated high voltage circuitry become disabled. This results in a reduction of discharge current from the regulator filters to approximately 1/3 its former rate. The energy retained by the regulator filter mainly serves to operate the vertical deflection circuit for a significantly longer period. The energy of the CRT beam then distributes along the vertical axis of the CRT to prevent spot burn, while the electrons stored on the CRT aquadag capacitance discharge to ground through bleeder resistor R2.

4.3.5 Acceleration Grid, Focus Grid and Dynamic Focus Transistor Voltages

The horizontal flyback voltage routes through lamp fuse DS101 to the half-wave voltage doubler and the half-wave rectifier. The half wave voltage doubler supplies voltage for the acceleration grid G2 and the focus grid G4 of the CRT. The half wave rectifier supplies voltage to the collector of vertical, dynamic focus transistor Q106. Fuse lamp DS101 minimizes loading to Q1 and Q2 should diodes CR116, CR117 or CR118 develop high leakage currents or their external CRT leads draw excessive current or become short-circuited. Normally this lamp is barely on, but it glows brighter and eventually burns out should excessive current be drawn through it.

Capacitors C121, C152 and C153 and diodes CR117 and C118 make up the half wave voltage doubler. Through resistors R137, R138, R139, R140 and R141, it supplies voltage for acceleration grid G2 and focus grid G4. R140 is the dc focus control that adjusts the dc level the horizontal and vertical focus voltages vary around. A sample of the horizontal flyback voltage feeds down through C142 to the resonant LC combination of capacitor C143 and horizontal dynamic focus control L102, which varies the peak-to-peak amplitude of the horizontal focus voltage. The combination is resonant at 1/2 the horizontal frequency and receives another positive flyback pulse every time its voltage decreases to zero to give a resultant parabolic voltage. Jack J105-1 connects the complete focus signal to the digital video, ECL PWA. From here it connects to the focus grid G4 of the CRT through R230.

R137 and R138 form a voltage divider for the +800 V at the top of C153. A voltage of about +700 V routes through J105-5 to the digital video, ECL PWA. From here it connects through R229 to the acceleration grid G2 of the CRT.

Diode CR116 and capacitors C122 and C123 make up a half wave voltage doubler that provides a voltage of about 100 V to the collector of vertical, dynamic focus, transistor Q106. CR116 conducts to charge capacitors C122 and C123 positively whenever the horizontal flyback voltage at its anode is greater than the voltage on C122 and C123. This keeps C122 and C123 charged to the peak of the horizontal flyback voltage of about +350V. This voltage connects through R186 to the collector of vertical dynamic focus transistor Q106.

4.3.6 Brightness Grid G1

Diode CR106 conducts when the voltage on the bottom of the horizontal flyback transformer T2 is phased negative. C154 stores a negative voltage of about -105 V. The supply voltage of +70 VDC feeds through R183 to the brightness controls. Brightness control R1 taps a negative voltage to the brightness grid G1 of the CRT. The voltage on G1 can vary the number of electrons that reach the CRT screen and, thereby, the brightness of the data. Maximum brightness limit R179 controls the adjustment range of external brightness control R1.

4.3.7 CRT Anode Voltage

The horizontal flyback current flows from the primary of flyback transformer T2 through J106-6. The supply voltage of +70 VDC connects to J106-7 through R130. The current in the primary of T2 caused by the flyback voltage induces a high

voltage in the secondary of T2 for the anode of the CRT. Diode CR1 rectifies this high voltage and the aquadag capacitance of the CRT filters it. Bleeder resistor R2 discharges the aquadag capacitance after the monitor turns off.

4.3.8 Overvoltage, X-Ray Protection

Transistor Q102, Q103 and associated components comprise a dc Schmidt trigger, regenerative circuit that provides overvoltage, x-ray protection. Transistor Q102 is normally off; Q103 is normally on. If the +70 V supply voltage rises approximately 5% above its normal value, transistor Q102 switches on. This action raises the base voltage for Q103 and turns it off. This raises the emitter voltage of Q102 and turns it on harder. The negative transition that results at the collector of Q103 disables monostable multivibrator U102. As a result horizontal deflection is lost and high voltage to the CRT anode is removed. Normal operation does not resume until the +70 supply drops sufficiently to trigger Q103 back on.

4.3.9 Vertical Section (Refer to Figure 4.2 for Timing Diagram)

The vertical sync pulse feeds through J104-5, resistor R184 and coupling capacitor C127 to pin 4 of integrated circuit, timer U103, which acts as an astable multivibrator triggered at the vertical rate. Resistor R143 and R144 and capacitor C127 differentiate the pulse producing positive and negative voltage spikes. Dropping resistor R142 supplies voltage for pin 8 of U103 from the +35 VDC line. Zener diode VR102 and VR103 regulate the voltage from pin 8 at +15 VDC. C128 stores a reference voltage of approximately 10 V (or 2/3 of the voltage at pin 8) for the comparator circuit inside timer U103. When a negative sync voltage spike appears at reset pin 4, the voltage at pin 3 and pin 7 goes low. After about 300 μ s the voltage at pin 4 goes back to its quiescent state, the voltage at pin 3 goes high and the voltage at pin 7 begins increasing as C130 charges through CR114, R148, and R151. Vertical height control R151 adjusts the slope frequency of U103. The setting of R151 determines what the peak voltage (typically 7 V) of the sawtooth at pin 7 will be when the next vertical sync voltage spike resets the sawtooth voltage to zero. The fall time of the vertical sawtooth at pin 7 is determined by the time to discharge C130 to ground through R147. Some additional time delay is introduced by RC filter R146 and C129 to yield a fall time of about 250 to 300 μ s. The vertical sawtooth ultimately determines the height of the raster by controlling the amount of current through the vertical deflection yoke. The negative temperature coefficient of temperature sensitive resistor R149 provides temperature compensation for the height of the linear ramp voltage.

Emitter follower Q109 provides current drive for the sawtooth voltage that feeds from pin 7 of U103 to the base of Q109. Inductor L103 and resistor R167 couple the sawtooth to the base of Q4 and the emitter of Q107, respectively. Transistors Q3 and Q4 make up a class A, complementary-symmetry (PNP-NPN), output amplifier that supplies the vertical deflection yoke with current. At the beginning of vertical scan Q3 is conducting maximally and Q4 is conducting minimally and vice versa at the end of scan. Vertical centering control R159 adjusts the base bias voltage for Q107. This provides a means of varying the current through the vertical yoke to position the raster vertically. R161 and C133 couple negative feedback from the emitter of Q4 to the base of Q107 to match the

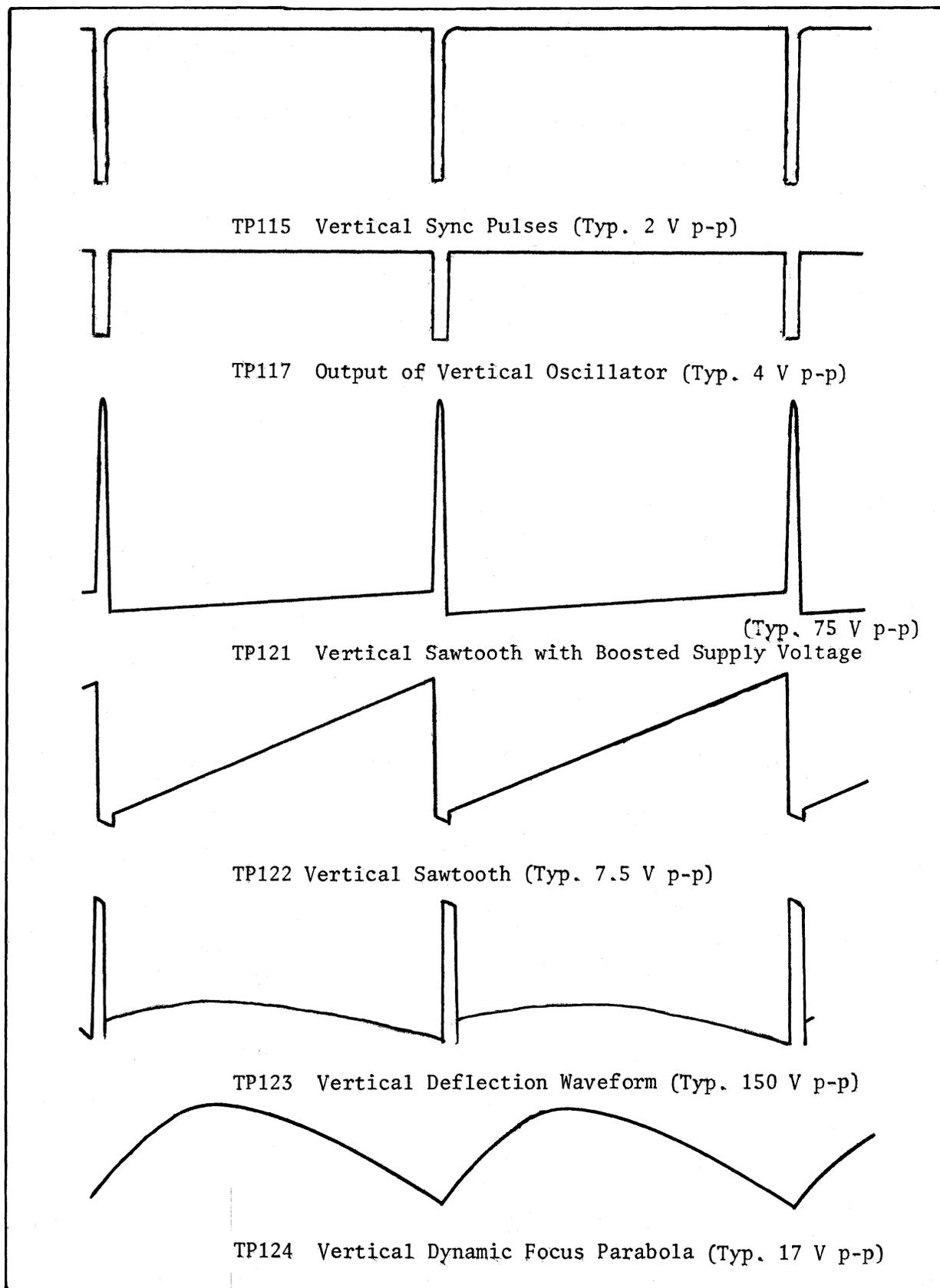


Figure 4.2 Vertical Timing

beginning and ending slopes of the sawtooth. Thermistor R163 provides temperature compensation for the base-emitter junction of Q107. Diode CR110 and CR112 provide temperature compensation for Q3 and Q4, respectively. Diode CR119 protects Q3 during vertical flyback.

The negative vertical gate pulses from pin 3 of U103 couple through R153 and C131 to the base of voltage doubler, PNP, transistor Q108. These pulses turn Q108 on at the start of vertical retrace. This results in a positive voltage pulse of approximately 60 V being coupled through C134 to the collector of Q107 and emitter of Q3. A pulse of about 130 V results here. Therefore, transistor Q107 conducts more; this results in a negative pulse at the base of Q3, which turns it on harder and supplies the vertical deflection yoke with the necessary current and voltage for fast vertical retrace.

4.3.10 Dynamic Focus Voltage

C137 integrates the sawtooth voltage to produce a parabolic voltage, which couples through C138 and R173 to the base of vertical, dynamic focus transistor Q106. The amplified and inverted parabolic voltage that appears at the collector of Q106 is coupled through C145 and R180. It combines with the horizontal, dynamic focus voltage, which C144 couples in, to produce the final dynamic focus voltage. The dynamic focus voltage rides on a dc level made adjustable by dc focus control R140.

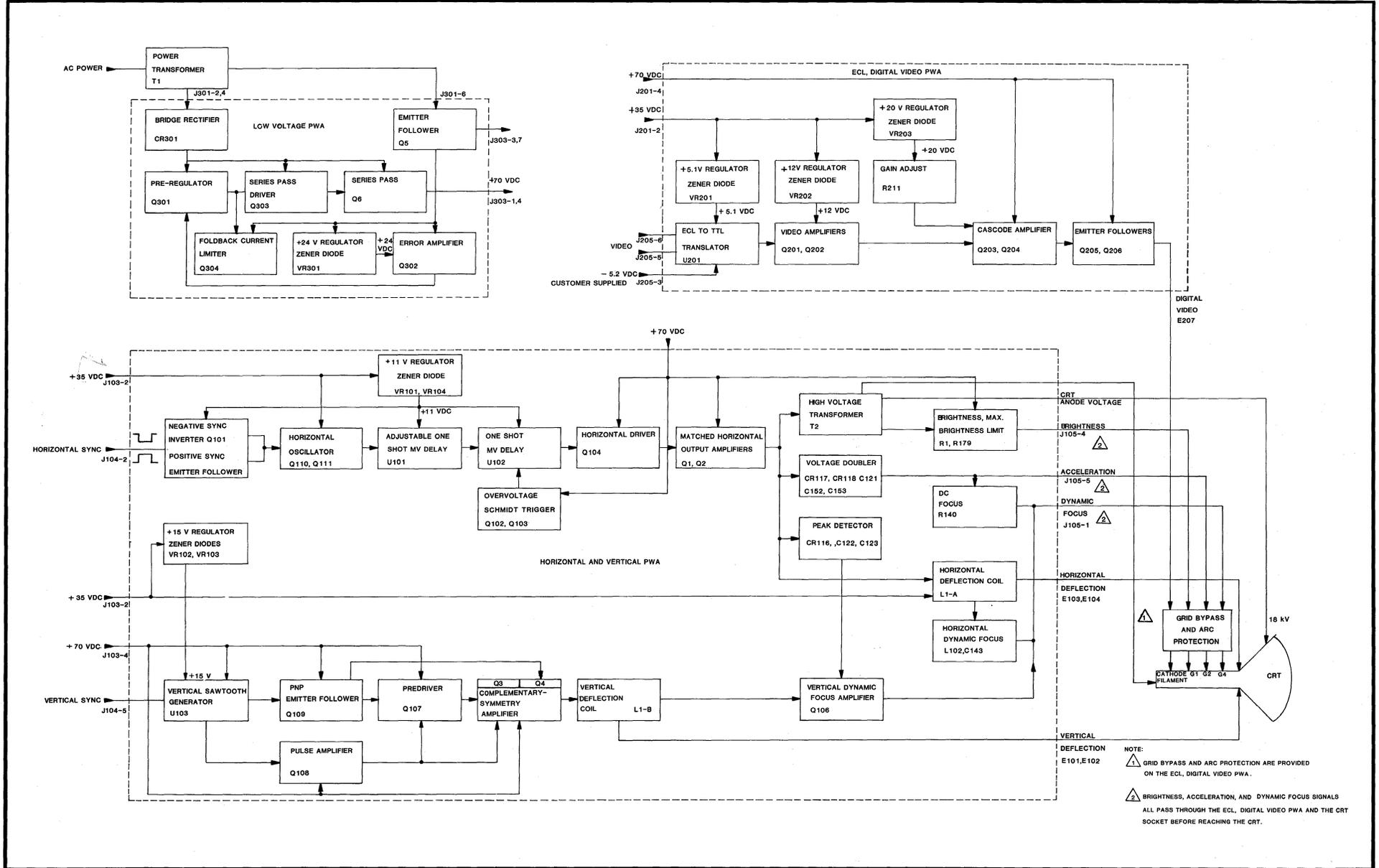


Figure 4.3 HD Series Block Diagram with ECL, Digital Video PWA

Section 5

ADJUSTMENT PROCEDURE AND TROUBLESHOOTING

5.1 ADJUSTMENT PROCEDURE

5.1.1 General

This section describes the adjustment procedure to be used for initial set-up or after component replacement.

NOTE: If problems with horizontal or vertical deflection have been found, then the plug leading from the CRT to J202 on the digital video, ECL PWA should be disconnected until it is assured that the correct deflection waveforms to the horizontal or vertical yokes are present. When J202 is disconnected, no filament voltage (6.3 V VAC) is available for the CRT, no electron beam is present, and, therefore, the CRT is protected against spot burn.

5.1.2 Introduction and Preliminary Adjustment

1. Position centering ring tabs to 6 o'clock and 12 o'clock positions. Refer to Figure 5.1. The line scan for your monitor must be horizontal for the proper orientation for this adjustment.

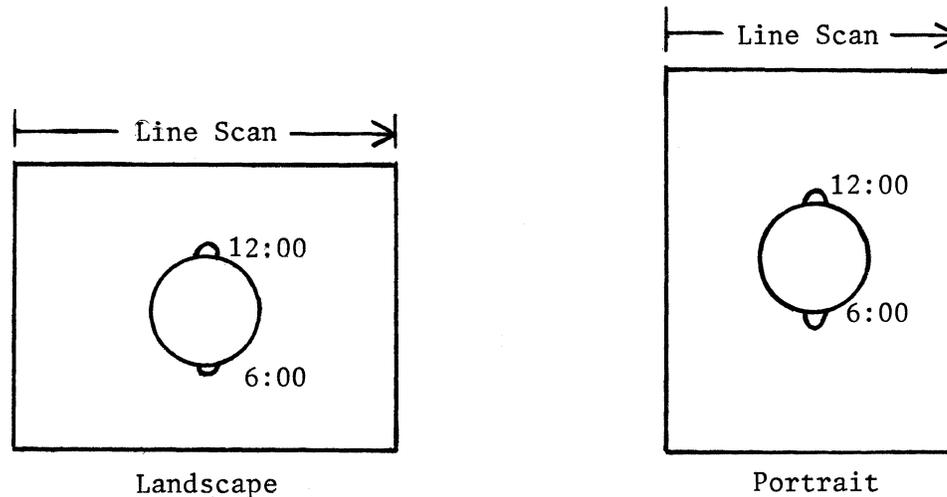


Figure 5.1 Centering Ring Tabs Reference Positions

2. Position linearity sleeve so that there is approximately 0.1" space between the calibration mark on the linearity sleeve and the rear of the plastic yoke collar, i.e., about 3/8" of aluminum foil should be visible. (Foil is on inside surface of sleeve.)
3. Rotate yoke slightly so edge of raster is visible after power is applied in section 5.1.3. This is required because after final set-up the CRT is overscanned both horizontally and vertically such that the raster is not visible. The video border extends out to the maximum dimensions of the CRT faceplate. In addition after final set-up the external brightness control pot adjustment range is limited by the brightness limit control R179 so that the raster is not visible, even though the external brightness pot is turned to max. It is recommended that a video linearity test pattern (crosshatch) from the generator be selected during initial adjustment and installation of the yoke magnets.

It should be noted that vertical height control R151 and vertical centering control R159 on the horizontal and vertical PWA are used to orient the raster in the vertical direction. The magnetic centering ring tabs on the yoke are adjusted in such a way as to introduce a magnetic vector that shifts the raster in a horizontal direction only.

It is the intent of the final adjustment procedure to provide the appropriate white background width with black characters at 30 FL at optimum focus and geometry and with the external brightness control adjusted to some intermediate setting. Maximum CW setting of the external brightness control should provide 45 footlamberts (fl) light output. Maximum CCW setting of the control should reduce the light output to 8 fl or less. The white background width should be slightly larger than the CRT bezel such that the raster is never seen by the operator.

5.1.3 Power-up Procedure

1. Connect the monitor to a video generator. Do not turn the unit on yet.
2. Connect a dc digital voltmeter between circuit ground and the +70 V bus.

NOTE: If your monitor utilizes an isolation network between circuit ground and chassis (i.e., a floating ground) the voltmeter ground should be connected to circuit ground and not the chassis. A convenient place for hook-up to circuit ground is on the ground lug of the filter capacitor C1.

3. Connect a resistor decade box between the two post that are used to mount selected resistor R126 on the horizontal and vertical PWA. Set the decade box to 13.7 K Ω nominal value. (The horizontal deflection amplifier does not energize without this resistor.) On later models R126 is a factory adjusted trimpot that is not to be readjusted.
4. Set the video generator for a crosshatch test pattern or similar linearity pattern.
5. Turn-on power to the monitor and the video generator.

6. Measure the voltage on the +70 V bus (TP301) on the low voltage PWA to check that it is near its nominal value.
7. Measure the voltage on the +35 V bus (TP302) to check that it is near its nominal value.

5.1.4 Low Voltage PWA Adjustment Procedure

1. Set +70 V adjust R314 to mid-range. (This control is intended to provide a fine adjustment of approximately ± 1 V to take care of any long term drifts of the monitor or the tolerance of service voltmeters.)
2. Slowly bring the voltage on the +70 V bus (TP301) upward by varying voltage limit adjust R316. Use an oscilloscope or neon bulb test indicator to check that the horizontal deflection stage is operating. Increase the regulated voltage above +70 V and note the threshold voltage that the horizontal deflection state disables. The threshold shut-down voltage should be greater than 71.5 V and less than 74.0 V. If necessary, select a different value on the decade box. (The shut-down voltage is approximately inversely proportional to the value of the resistor.) After the decade box value is set, turn-off the monitor, remove the decade box, and solder in the appropriate fixed value of resistance for R126 and repeat step 2 to insure proper operation of the shut-down circuit.
3. Reset voltage limit adjust R316 to its final value of +70 V.

5.1.5 Digital Video ECL PWA Adjustment Procedure

1. Set video gain adjust R211 to mid-range. This is a preliminary adjustment.

5.1.6 Horizontal and Vertical PWA Adjustment Procedure

1. After the monitor has been operating for at least 5 minutes, adjust horizontal data centering control R111 to horizontally center the video data on the raster. If necessary, vary horizontal frequency adjust R108 to synchronize the horizontal oscillator and lock-in the picture horizontally.
2. Attach the oscilloscope probe to the banded end of CR104 (TP111) to monitor the horizontal flyback pulse. (Set the trigger mode to internal sync and the time base to $10\mu\text{s}/\text{div.}$) Note the duration of the horizontal line period. Refer to the horizontal flyback pulse in Figure 5.2. Disable the incoming horizontal sync signal. Adjust the free running period of the horizontal oscillator $2\mu\text{s}$ longer than the synchronized horizontal line period by means of horizontal frequency adjust R108. Reconnect the horizontal sync signal.
3. Recheck the centering of video data on the raster and use R111 to recenter, if necessary. Adjust the horizontal width control L101 so the raster width overscans the faceplate. This is a preliminary adjustment. Use a cross-hatch test pattern.
4. Adjust vertical centering control R159 to position the first data line at the extreme top of the faceplate. Adjust vertical height control R151 to

adjust the length of vertical scan such that the last data line is positioned at the extreme bottom of the faceplate. This is preliminary adjustment.

5. Horizontally center the raster by adjusting the centering tabs.

NOTE: The centering ring tabs on the deflection yoke are used to shift the raster (not video) to the left or right as required to provide optimum horizontal centering. To shift the raster to the left or right without introducing any vertical displacement, the tabs of the rings should be moved symmetrically to the left or right as required. Initially the tabs should be oriented at 12:00 and 6:00. To shift the raster further, move the tabs to the 1:00 and 5:00 positions. To shift the raster still more, move the tabs to the 2:00 and 4:00 positions, etc. To move the raster in the opposition direction, move the tabs to the 11:00 and 7:00 positions, etc. Maintain symmetry about the horizontal center to avoid moving the raster in the vertical direction.

6. Attach the oscilloscope test probe to the point of intersection of L102, C142, C143, and C144 (TP124). Adjust the slug in L102 for a negative horizontal parabola of 275 V p-p. Do Not include the amplitude of the added flyback pulse. The slug should initially be adjusted to the lower end of the coil. The final adjustment is reached with the slug partially extending out the lower end of the winding. Turn power to monitor off and then back on. Check that the phase of the horizontal parabola has not shifted, i.e., the waveform has not flipped over. If it has, repeat adjustment. Refer to the negative horizontal focus parabola in Figure 5.2.

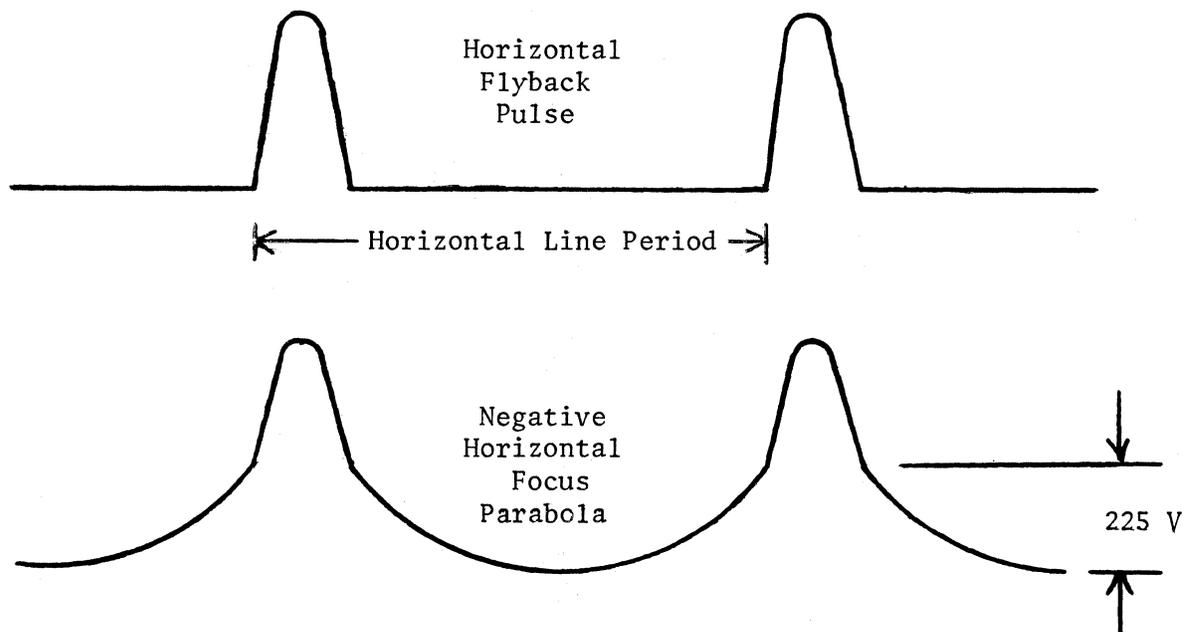


Figure 5.2 Waveforms for Step 2 and 5 of Section 5.1.6

7. Set the video generator to output an alphanumeric test pattern to be used for the focus adjustments. Vary dc focus adjust R140 from CW to extreme CCW. Check that the control is effective. As R140 is varied observe the dots in the corners appear as ellipses whose long axes appear to rotate. Optimum focus is obtained with the long axes of the corner dots in the vertical direction, i.e., optimum horizontal resolution.
8. Attach magnets for best operating geometry and focus. The geometry outline should be a rectangle with a tolerance of $\pm 0.1''$. Switch between the cross-hatch and alphanumeric test patterns as required.
9. Disconnect the video input to the monitor. Set video gain adjust R211 to maximum CCW. Set the external brightness control to maximum CW. Set brightness limit control R179 for a raster brightness of 5 fl, i.e., no video.
10. Reconnect the video generator and set its output so that a white field without characters is displayed. Set video gain adjust R211 on the digital video, ECL PWA for a light output of 45 fl.
11. Adjust the external brightness control maximum CCW. Check the CRT. The light output should be 8 fl or darker.
12. Readjust the external brightness for 30 fl light output. This is a reference for final set-up and the geometry and resolution check.
13. Set the height of the white field to appropriate height by adjusting vertical centering control R159 and vertical height control R151 as per step 4 of Section 5.1.6.
14. Set the width of the white field to appropriate width by adjusting L101. Horizontally center white field by adjusting centering ring tabs in a symmetrical setting about the horizontal axis as per step 5 of section 5.1.6. If slightly more width is required, withdraw linearity sleeve an additional 0.1".
15. Apply epoxy cement to voltage limit adjust R316 on the low voltage PWA.

5.2 TROUBLESHOOTING

In the event of failure or malfunction of the monitor there is a series of simple steps you can carry out to isolate the fault to a particular PWA. (Refer to Figure 5.3) Once the fault is isolated to a particular PWA your service expertise and experience come heavily into play when isolating the fault to a particular component. The hints given below should help you.

5.2.1 Horizontal Section (Horizontal and Vertical PWA)

If the monitor fault seems to be in the horizontal section and the waveform at the collector of Q104 (TP109) is normal, then the horizontal output transistors Q1 and Q2 are trouble suspects. Note Q1 and Q2 are factory selected and must be replaced as matched pair (part number 1-015-1227). If the low voltage PWA is not folding back and the supply voltages are normal, other significant tests or waveforms of the horizontal output stages are:

1. Horizontal flyback pulse at the collector of Q1 (TP111).
2. Radiated pulse from high voltage flyback transformer T2. (Hold a 10:1 oscilloscope probe approximately 2" away from T2).
3. Check parabolic waveform voltage across "S" shaping capacitor C125.
4. Measure the dc current to the horizontal output stages by measuring the voltage drop across R130. Typical current of 0.5 A dc should result in a voltage drop of 0.6 VDC. The current at high brightness should run somewhat higher.
5. Check lamp fuse DS101 with an ohmmeter. Typically its resistance should be 100Ω or less. DS101 is used to fuse the voltage source circuitry for G2 and G4. If DS101 is blown, a trouble in the voltage source circuitry or an internal short in the CRT is the probable cause. To determine where the problem is disconnect the CRT socket and replace DS101. If DS101 still blows the problem is in the voltage source circuitry and not the CRT.

Other voltages in the circuit are:

CRT, G1 (pin 4 of J105): variable with brightness control from -100 V to +5 VDC.

CRT, G2 (pin 5 of J105): +600 VDC.

CRT, G4 (pin 1 of J105): variable with focus parabola from 0 to 700 VDC.

If the low voltage PWA is folding back, disconnecting the plug to J102 on the horizontal and vertical PWA and the plug to J201 on the ECL, digital video PWA may bring the supply voltage lines back up.

5.2.2 Vertical Section (Horizontal and Vertical PWA)

If the monitor fault seems to be in the vertical section and the waveforms at the collector of Q107 (TP121) and the base of Q4 (TP122) are normal, then vertical output transistors Q3 and Q4 are trouble suspects. Voltage waveforms at TP123

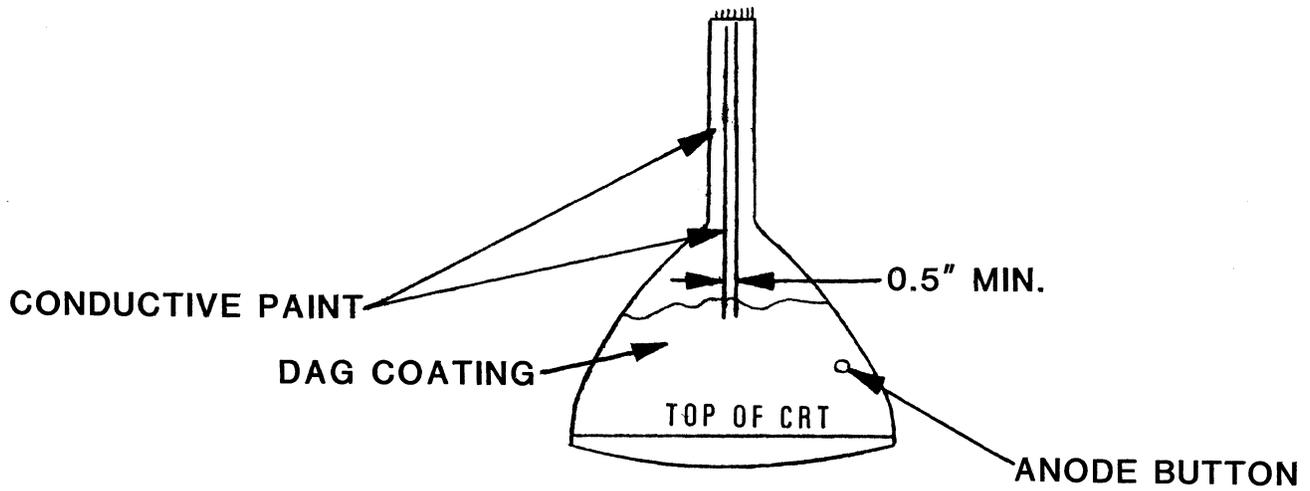


Figure 5.4 Conductive Paint Application When Installing New CRT

2. Reverse the removal procedure of Section 5.3 to complete the installation of the CRT.

Section 6

SERVICE DATA

6.1 GENERAL

This section contains information on ordering and returning parts; information on how to identify a PWA; a chassis mounted component parts list; and waveforms for the high voltage PWA, the input composite video PWA, the output video PWA and the horizontal and vertical PWA; the component layouts and parts lists for all PWA's; and schematics for all PWA's.

If a part you have ordered has been replaced with a new or an improved part, our customer service representative will contact you.

Any change information concerning the HD Series CRT Display is located at the rear of the manual.

6.2 ORDERING PARTS

Most parts contained in the monitor are available commercially from electronic parts outlets. When it is necessary to order spare or replacement parts from Ball E.D.D., include the part description, part number, model number, and serial number of the monitor as listed on the serial number plate and, if applicable, the schematic reference number listed in the parts list. Orders for these parts should be sent to:

Ball Electronic Display Division
P.O. Box 43376
St. Paul, Minnesota 55164

For rapid service: Telephone area (612) 786-8900
or
TWX area (910) 563-3552

6.3 RETURNING PARTS

When the monitor requires service or repair in accordance with the enclosed warranty, contact factory for a return material authorization (RMA). Upon obtaining a RMA return the unit or part to:

Ball Electronic Display Division
4501 Ball Road N.E.
Circle Pines, Minnesota 55014

ATTN: Customer Service

Telephone area (612) 786-8900
TWX area (910) 563-3552

Unnecessary delays may be avoided when parts are returned to Ball Electronic Display Division using the following procedures:

- (1) Package the unit or part in accordance with the method of shipment. Enclose a list of the material being returned and the reason for returning it.
- (2) Send the unit or part, transportation prepaid, to the address stipulated for returning parts.

All equipment and parts described in the warranty will be replaced, provided our examination discloses that the defects are within the limits of the warranty. If damages or defects are not within the limits of the warranty, necessary repairs will be made. The customer will be charged in accordance with the flat rate pricing schedule that applies at the time of repair.

6.4 PWA IDENTIFICATION

The board assembly part number has a 6-002-XXXX prefix. The last four digits of the board assembly part number are stamped on the component side of the board.

Do not confuse the PWA number with the numbers etched on the conductor side of the printed wiring board. The PWA number is always located on the component side of the PWA.

6.5 CHASSIS MOUNTED COMPONENT PART LIST

REFERENCE SYMBOL	DESCRIPTION	PART NUMBER
C1	Filter Capacitor, 1500 μ F, 125V	1-012-2313
J1	Assembly, 24 Pin Female (includes wiring and plugs P104, P107, P205, and P301)	1-041-0108
L1	Deflection Coil	1-023-0249
Q1,Q2	Transistors, Matched Pair, B1213	1-015-1227
Q3	Transistor, PNP, FT417B	1-015-1220
Q4	Transistor, NPN, SJE-5300	1-015-1216
Q5	Transistor, NPN, T220, Darlington, TIP110	1-015-1237
*T2	Assembly, High Voltage Transformer (R1, CR1, and other attached parts)	6-003-0707
Miscellaneous		
	Linearity Sleeve (Yoke)	1-023-5081
	Assembly, CRT Socket with Contact Pins	6-004-0848

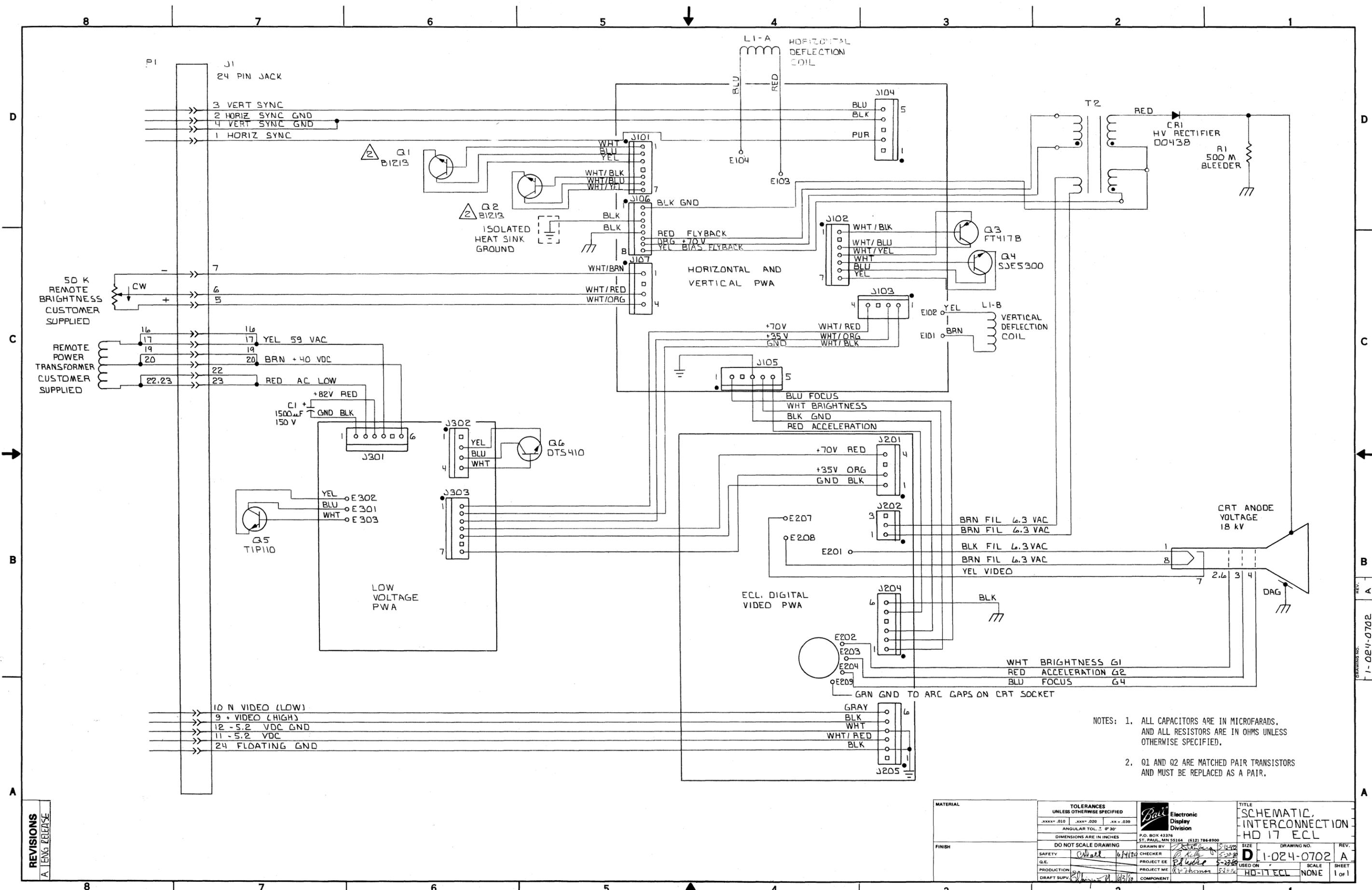
* See Section 6.6.

6.6 REPLACEMENT COMPONENTS AFFECTING PRODUCT SAFETY

Product safety must be considered whenever a component is replaced in the monitor. *The critical components that affect x-radiation are shaded on the schematics and indicated on the parts list when an asterick preceding the reference symbol designator. These components must be replaced only with Ball Electronics Display Division approved parts.

6.7 WAVEFORMS

The waveforms in Figure 6.5 and 6.6 were taken with about a 0.65 V peak-to-peak separate video, character test pattern applied to pins 9 and 10 of J1. The horizontal frequency used was 34.72 kHz; the vertical frequency was 77.42 Hz. The Tektronix 465 oscilloscope was used to view the waveforms. If present, the hollow white arrow indicates the zero volt reference level.



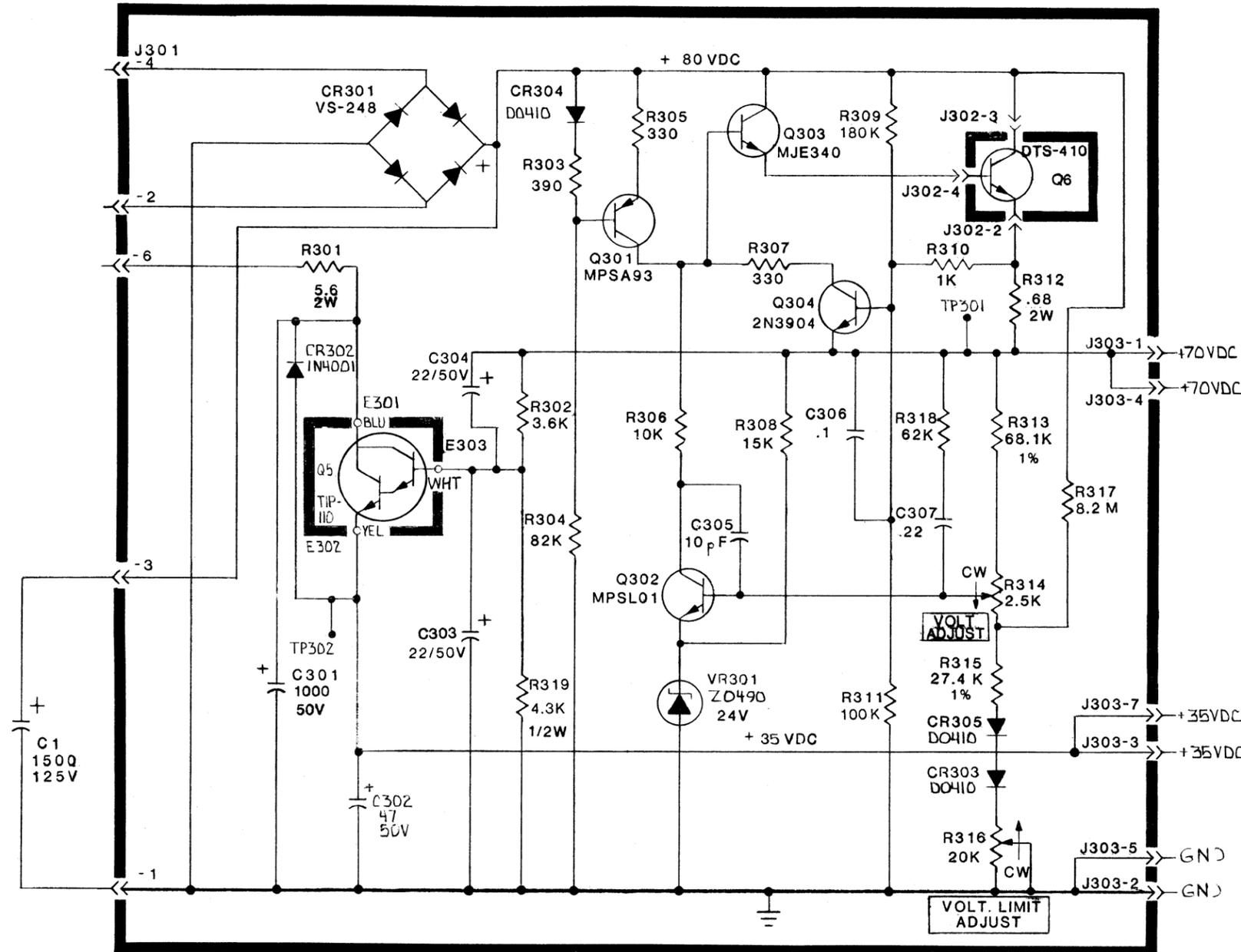
- NOTES: 1. ALL CAPACITORS ARE IN MICROFARADS, AND ALL RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
2. Q1 AND Q2 ARE MATCHED PAIR TRANSISTORS AND MUST BE REPLACED AS A PAIR.

REVISIONS
A. LENG RELEASE

MATERIAL	TOLERANCES UNLESS OTHERWISE SPECIFIED			TITLE SCHEMATIC, INTERCONNECTION HD 17 ECL
	.xxxxx ± .010	.xxxx ± .020		
FINISH	ANGULAR TOL. ± 0° 30'		P.O. BOX 43376 ST. PAUL, MN 55164 (612) 786-8900	DRAWING NO. D 1-024-0702 A
	DIMENSIONS ARE IN INCHES			
DO NOT SCALE DRAWING			DRAWN BY PROJECT EE PROJECT ME COMPONENT	REV. SCALE SHEET 1 of 1

Figure 6.1 HD Series Interconnection Schematic with ECL, Digital Video PWA

- NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN ohms ($\frac{1}{2}$ W) 5%.
 2. ALL CAPACITORS ARE IN MICROFARADS.

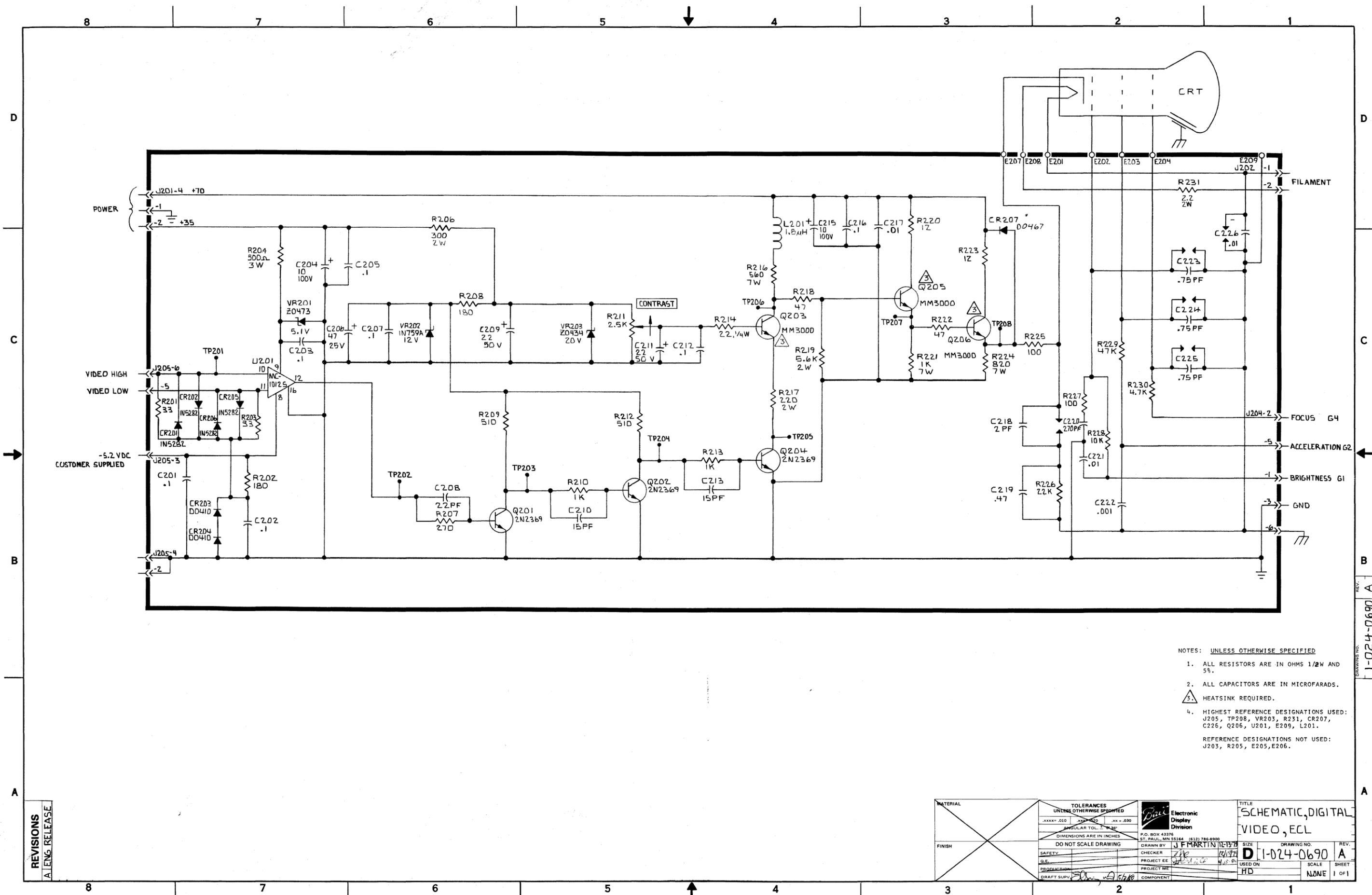


REVISIONS
A ENG RELEASE

 BALL BROTHERS RESEARCH CORP. ELECTRONIC DISPLAY DIVISION P.O. BOX 3270 ST. PAUL, MINNESOTA 55108	TITLE	
	SCHEMATIC PWA POWER SUPPLY	
SIZE	DRAWING NO.	REV.
HD	C 1-024-0643	A
USED ON	SCALE	SHEET
	NONE	1 OF 1

Figure 6.2 Low Voltage PWA Schematic

DRAWING NO. 1-024-0643 REV. A



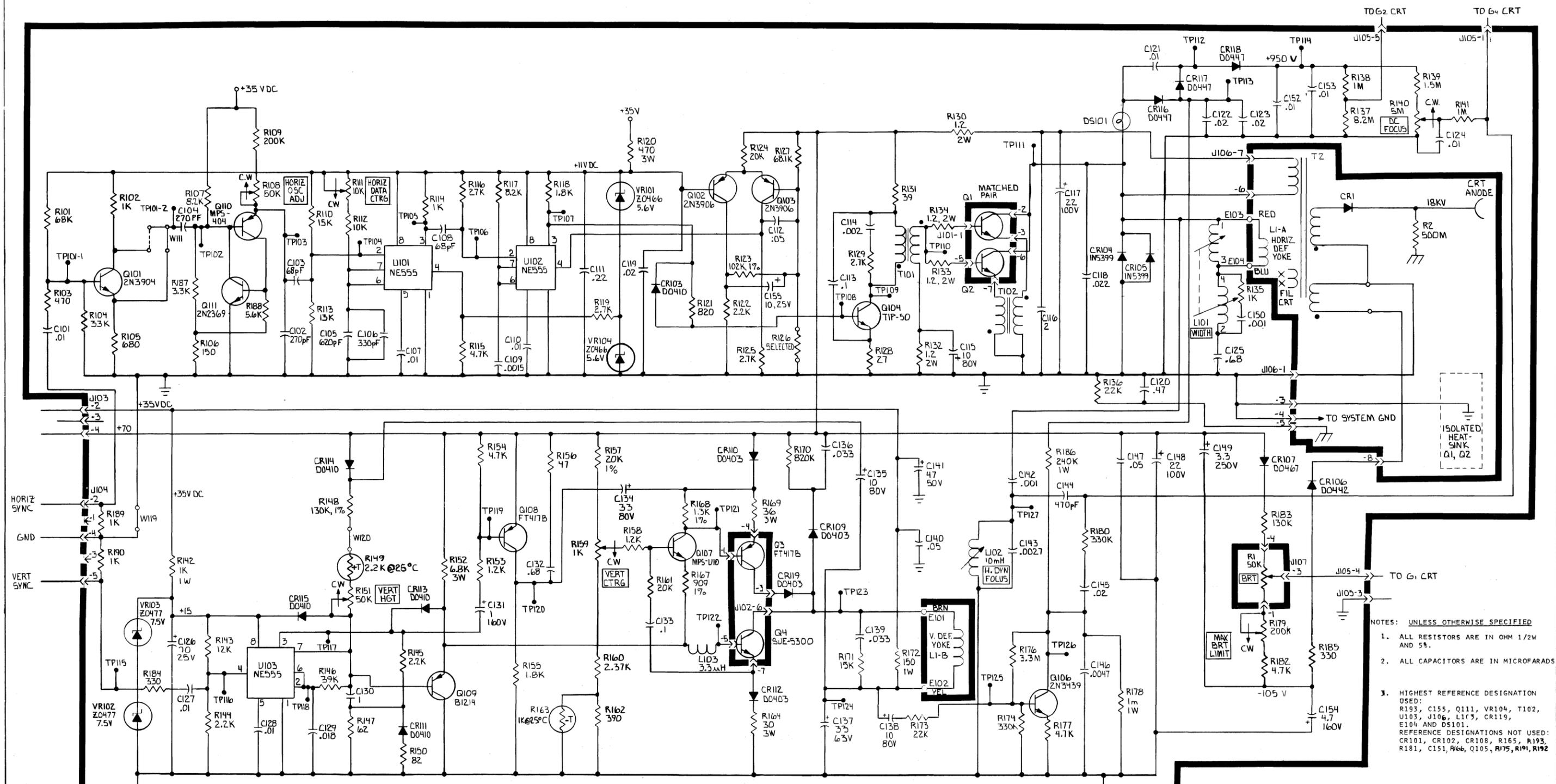
- NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS 1/2W AND 5%.
 2. ALL CAPACITORS ARE IN MICROFARADS.
 3. HEATSINK REQUIRED.
 4. HIGHEST REFERENCE DESIGNATIONS USED: J205, TP208, VR203, R231, CR207, C226, Q206, U201, E209, L201.
- REFERENCE DESIGNATIONS NOT USED: J203, R205, E205, E206.

REVISIONS
A ENG. RELEASE

MATERIAL	TOLERANCES UNLESS OTHERWISE SPECIFIED		TITLE
	.xxx - .010 .xx - .030 ANGULAR TOL. 2° - 30° DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWING		SCHEMATIC, DIGITAL VIDEO, ECL
FINISH	SAFETY	P.O. BOX 43378 ST. PAUL, MN 55164 (612) 786-8900 DRAWN BY J.F. MARTIN 11/13/78	SIZE D DRAWING NO. 1-024-0690 REV. A
	G.E. PROJECT EE PROJECT ME DRAFT SURV.	CHECKER PROJECT EE PROJECT ME COMPONENT	USED ON HD SCALE NONE SHEET 1 OF 1

REV. A
1-024-0690

Figure 6.3 ECL, Digital Video PWA Schematic



- NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHM 1/2W AND 5%.
 2. ALL CAPACITORS ARE IN MICROFARADS
 3. HIGHEST REFERENCE DESIGNATION USED:
 R193, C155, Q111, VR104, T102, U103, J106, LI3, CR119, E104 AND DS101.
 REFERENCE DESIGNATIONS NOT USED:
 CR101, CR102, CR108, R165, R193, R181, C151, R166, Q105, R175, R191, R192

	TITLE	SCHEM H4V DEFL CRT
	34.72 KH, LONG H. SCAN 77.42 H, SHORT V. SCAN	DRAWING NO. 1-024-0648
USED ON HD	SCALE NONE	SHEET 1 OF 1

Figure 6.4 Horizontal and Vertical PWA Schematic

NOTE: Hollow white arrow indicate zero volt reference level.

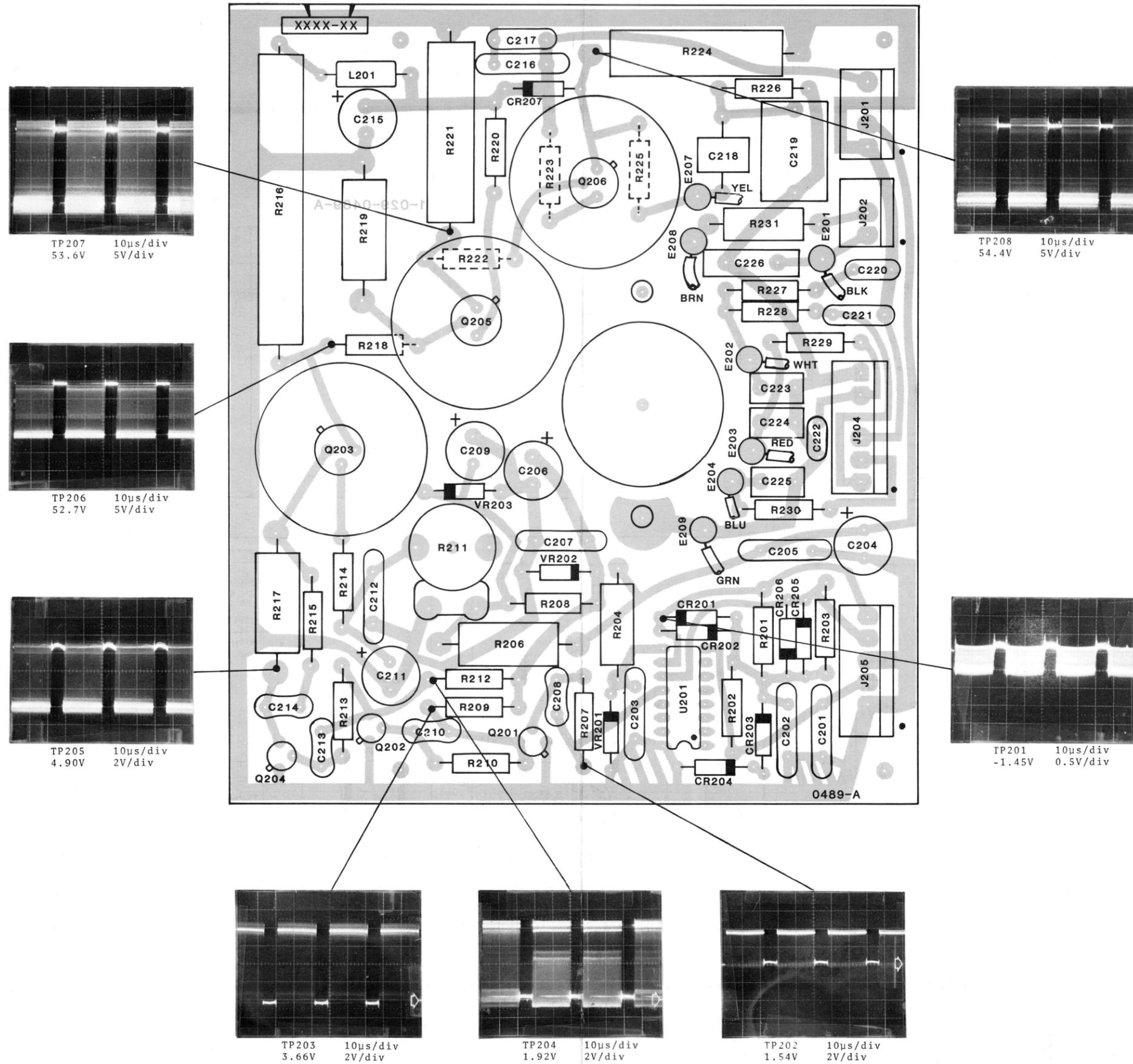


Figure 6.5 ECL, Digital Video PWA Waveforms

NOTES:

1. Hollow white arrows indicate zero volt dc levels.
2. Vertical rate waveforms (2ms/div) were taken with J101 disconnected, thereby disabling horizontal output transistors Q1 and Q2.

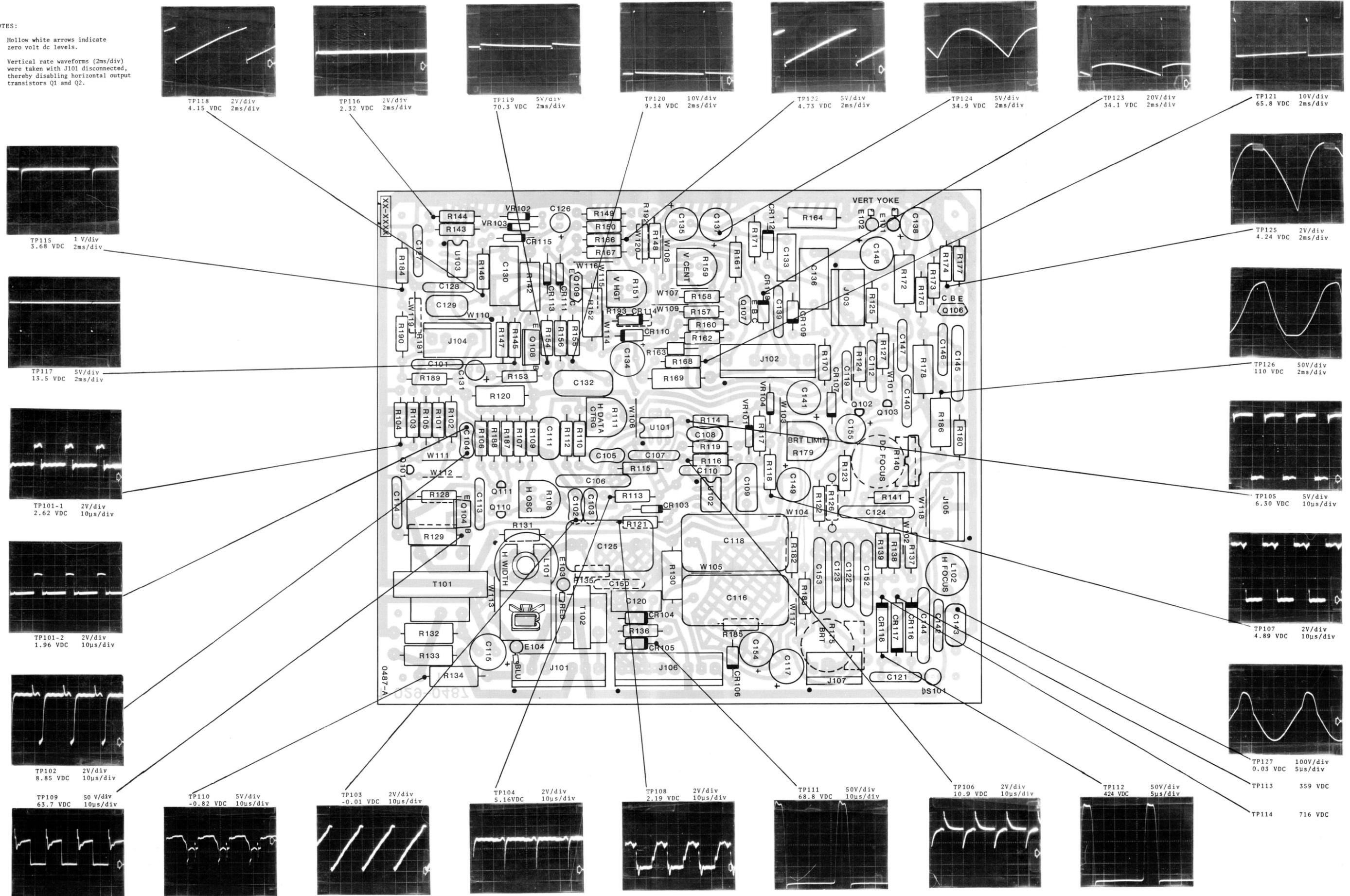
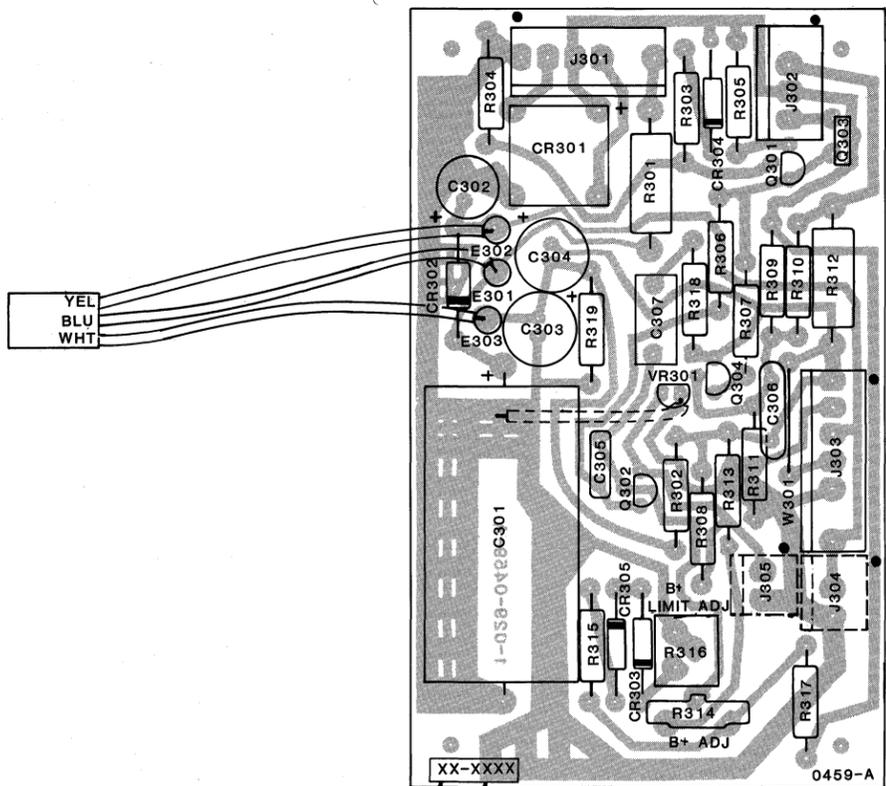


Figure 6.6 Horizontal and Vertical PWA Waveforms



REVISION LEVEL IDENTIFIER
 LAST FOUR DIGITS OF PWA NO.

PARTS LIST

REF SYM	DESCRIPTION	PART NUMBER
C301	1000µF-50	1-012-2281
C302	47µF-50	1-012-2157
C303	22µF-50	1-012-2193
C304	22µF-50	1-012-2193
C305	10pF-500-5	1-012-2407
C306	.1µF-100-10	1-012-2370
C307	.22µF-200-10	1-012-0930
CR301	DIODE BRIDGE, VS248	1-021-0494
CR302	IN4001	1-021-0497
CR303	D0410	1-021-0410
CR304	D0410	1-021-0410
CR305	D0410	1-021-0410
E301	TERMINATION POINTS XSTR SOCKET LD, BLU	
E302	XSTR SOCKET LD, YEL	
E303	XSTR SOCKET LD, WHT	
J301	CONNECTOR 6 CONT, 12346A	1-039-0180
J302	4 CONT, 234A	1-039-0170
J303	7 CONT, 123457A	1-039-0181
J304	NOT USED	
J305	NOT USED	
Q301	TRANSISTOR MPSA93	1-015-1202
Q302	MPSL01	1-015-1170
Q303	MJE340	1-025-0128
Q304	2N3904	1-015-1144
R301	RESISTOR 5.6-2-10	1-011-1610
R302	3.6K-1/2-5	1-011-2283
R303	390-1/2-5	1-011-2260
R304	82K-1/2-5	1-011-2316
R305	330-1/2-5	1-011-2258
R306	10K-1/2-5	1-011-2294
R307	330-1/2-5	1-011-2258
R308	15K-1/2-5	1-011-2298
R309	180K-1/2-5	1-011-2324
R310	1K-1/2-5	1-011-2270
R311	100K-1/2-5	1-011-2318
R312	.68-2-10	1-011-2217
R313	68.1K-1/2-1	1-011-2546
R314	VAR, 2.5K-1/4-20	1-011-5636
R315	27.4K-1/2-1	1-011-2522
R316	VAR, 20K-1/2-20	1-011-5712
R317	8.2M-1/2-5	1-011-2364
R318	62K-1/2-5	1-011-2313
R319	4.3K-1/2-5	1-011-2285
VR301	ZENER Z0490, 24V	1-021-0490
W301	MISCELLANEOUS JUMPER WIRE	1-029-0459
	SOCKET XSTR	1-045-0165
	JUMPER WIRE	1-041-0105
	JUMPER WIRE	1-045-0305
	SLEEVING (.07 FT)	2-052-0135

NOTES

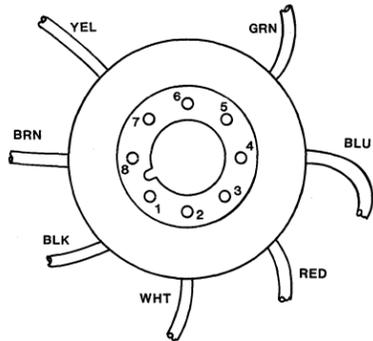
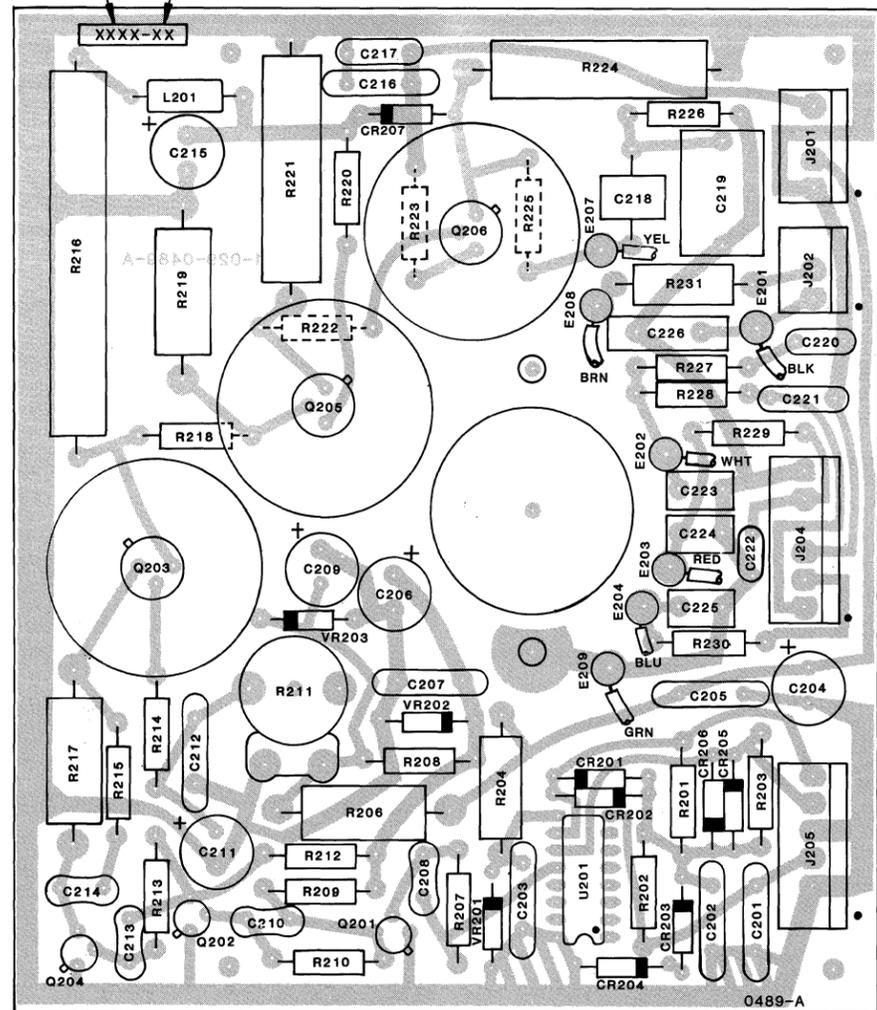
1. RAISE R301 AND R312 1/4 INCH OFF PWB.
2. JUMPER WIRE (1-045-0305) AND SLEEVING (2-052-0135) IS SOLDERED TO CONDUCTOR SIDE OF PWB.

REVISIONS	DATE	BY	DESCRIPTION
1	10/10/60	W.C.	INITIAL RELEASE

TOLERANCES UNLESS OTHERWISE SPECIFIED		Ball Electronic Display Division	TITLE ASSEMBLY, PWA POWER SUPPLY	
XXX.010	XXX.020		XX.050	
DIMENSIONS ARE IN INCHES		NO. 001 40078	ST. PAUL, MINN 55104 (612) 766-0200	
DO NOT SCALE DRAWING		DRAWN BY KUYAWA	CHECKED BY T. W. KELLER	DATE 4/1/60
SAFETY		PROJECT OR	PROJECT OR	SCALE
LIA ENG	4-5-60	PROJECT OR	PROJECT OR	2/1
COMPONENT		PROJECT OR	PROJECT OR	1 of 1

Figure 6.7 Low Voltage PWA Component Layout and Parts List

PWA NO. LAST FOUR DIGITS REVISION LEVEL IDENTIFIER



PARTS LIST

REF SYM	DESCRIPTION	PART NUMBER	REF SYM	DESCRIPTION	PART NUMBER
CAPACITOR					
C201	.1µF-100-20	1-012-2370	Q205	MM3000	1-015-1211
C202	.1µF-100-20	1-012-2370	Q206	MM3000	1-015-1211
C203	.1µF-100-20	1-012-2370	RESISTOR		
C204	10µF-80	1-012-2260	R201	33-1/2-5	1-011-2234
C205	.1µF-100-20	1-012-2370	R202	180-1/2-5	1-011-2252
C206	47µF-25	1-012-2165	R203	33-1/2-5	1-011-2234
C207	.1µF-100-20	1-012-2370	R204	500-3-5	1-011-2706
C208	22pF-500-5	1-012-2418	R205	NOT USED	
C209	22µF-50	1-012-2195	R206	300-2-5	1-011-2467
C210	15pF-500-5	1-012-2412	R207	270-1/2-5	1-011-2256
C211	22pF-50	1-012-2193	R208	180-1/2-5	1-011-2252
C212	.1µF-100-20	1-012-2370	R209	510-1/2-5	1-011-2263
C213	15pF-500-5	1-012-2412	R210	1K-1/2-5	1-011-2270
C214	NOT USED		R211	VAR 2.5K-1/4-20	1-011-5741
C215	10µF-80	1-012-2260	R212	510-1/2-5	1-011-2265
C216	.1µF-100-20	1-012-2370	R213	1K-1/2-5	1-011-2270
C217	.01µF-500-20	1-012-0740	R214	22-1/4-5	1-011-2680
C218	2pF-230V ARC GAP	1-012-0111	R215	NOT USED	
C219	.47µF-100-10	1-012-1007	R216	560-7-5	1-011-2675
C220	270pF-1000-10	1-012-0395	R217	220-2-5	1-011-2653
C221	.01µF-500-20	1-012-0740	R218	47-1/2-5	1-011-2238
C222	.001µF-1000-20	1-012-0540	R219	5.6K-2-5	1-011-2654
C223	.75pF-1000 ARC GAP	1-012-0110	R220	12-1/2-5	1-011-2224
C224	.75pF-1000 ARC GAP	1-012-0110	R221	1K-7-5	1-011-2660
C225	.75pF-1000 ARC GAP	1-012-0110	R222	47-1/2-5	1-011-2238
C226	.01µF-1000 ARC GAP	1-012-0112	R223	12-1/2-5	1-011-2224
DIODE					
CR201	IN5282	1-021-0497	R224	820-7-5	1-011-2541
CR202	IN5282	1-021-0497	R225	100-1/2-5	1-011-2246
CR203	D0410	1-021-0410	R226	22K-1/2-5	1-011-2302
CR204	D0410	1-021-0410	R227	100-1/2-5	1-011-2246
CR205	IN5282	1-021-0497	R228	10K-1/2-5	1-011-2294
CR206	IN5282	1-021-0497	R229	47K-1/2-5	1-011-2310
CR207	D0467	1-021-0467	R230	4.7K-1/2-5	1-011-2286
CONNECTOR					
J201	4 CONT, 124A	1-039-0168	R231	2.2-2-10	1-011-0120
J202	3 CONT, 12A	1-039-0164	COIL		
J203	NOT USED		U201	MC10125	1-025-0124
J204	6 CONT, 12356A	1-039-0193	TRANSISTORS		
J205	6 CONT, 23456A	1-039-0192	Q201	2N2369	1-015-1212
ZENER					
VR201	Z0473, 5.1V	1-021-0473	Q202	2N2369	1-015-1212
VR202	IN759, 12V	1-021-0481	Q203	MM3000	1-015-1211
VR203	Z0434, 20V	1-021-0434	Q204	2N2369	1-015-1212
MISCELLANEOUS					
E201	CRT SOCKET, BLK LD		CRITICAL DIMENSIONS		
E202	CRT SOCKET, WHT LD		DO NOT SCALE DRAWING		
E203	CRT SOCKET, RED LD		SAFETY		
E204	CRT SOCKET, BLU LD		LVA ENGR: [Signature]		
E205	NOT USED		CHECKER: [Signature]		
E206	NOT USED		PROJECT ME: [Signature]		
E207	CRT SOCKET, YEL LD		PROJECT ME: [Signature]		
E208	CRT SOCKET, BRN LD		PROJECT ME: [Signature]		
E209	CRT SOCKET, GRN LD		COMPOSER:		
CRITICAL DIMENSIONS					
DO NOT SCALE DRAWING					
SAFETY					
LVA ENGR: [Signature]					
CHECKER: [Signature]					
PROJECT ME: [Signature]					
PROJECT ME: [Signature]					
COMPOSER:					

NOTES

1. RAISE R204, R206, R216, R217, R219, R221, R224 AND R231 1/4 INCH OFF PWB.
2. PLACE TRANSIPAD UNDER Q203, Q205 AND Q206.

REVISIONS
A ENG. RELEASE
7-10-80/15/AVI R. C. [Signature]

TOLERANCES UNLESS OTHERWISE SPECIFIED		Ball Electronic Display Division	TITLE	
XXXX .010	XX .005		PWA HD VIDEO/ECL	
ANGULAR TOL 2° 30'		ST PAUL, MN 55104 (612) 788-2800	SIZE	DRAWING NO.
DIMENSIONS ARE IN INCHES		DRAFTSMAN	REV.	
DO NOT SCALE DRAWING		CHECKER	DATE	
SAFETY		PROJECT ME	SCALE	
LVA ENGR: [Signature]		PROJECT ME	211	
CHECKER: [Signature]		COMPOSER		
PROJECT ME: [Signature]				
PROJECT ME: [Signature]				
COMPOSER:				

Figure 6.8 ECL, Digital Video PWA Component Layout and Parts List



INSTALLATION AND OPERATING MANUAL

MALFUNCTION REPORT

Dear Customer:

We are trying to manufacture the most reliable product possible. You would do us a great courtesy by completing this form should you experience any failures.

1. Type Unit _____ Serial No. _____
Module (if applicable) _____

2. Part failed (Name and Number) _____

3. Cause of failure (if readily available) _____

4. Approximate hours/days of operation to failure _____

5. Failure occurred during:
Final Inspection Customer Installation Field Use

6. Personal Comment:

Customer _____
Address _____
Signed _____
Date _____

Ball Electronic Display Division
P.O. Box 43376
St. Paul, Minnesota 55164
Telephone 612-786-8900 TWX 910-563-3552



LOST OR DAMAGED EQUIPMENT

The goods described on your Packing Slip have been received by the Transportation Company complete and in good condition. If any of the goods called for on this Packing Slip are short or damaged, you must file a claim **WITH THE TRANSPORTATION COMPANY FOR THE AMOUNT OF THE DAMAGE AND/OR LOSS.**

IF LOSS OR DAMAGE IS EVIDENT AT TIME OF DELIVERY:

If any of the good called for on this Packing Slip are short or damaged at the time of delivery, **ACCEPT THEM, but only if the Freight Agent makes a damaged or short notation on your Freight Bill or Express Receipt and signs it.**

IF DAMAGE OR LOSS IS CONCEALED AND DISCOVERED AT A LATER DATE:

If any concealed loss or damage is discovered, notify your local Freight Agent or Express Agent **AT ONCE** and request him to make an inspection. This is absolutely necessary. Unless you do this, the Transportation Company will not consider any claim for loss or damage valid. If the agent refuses to make an inspection, you should draw up an affidavit to the effect that you notified him on a certain date and that he failed to make the necessary inspection.

After you have ascertained the extent of the loss or damage, **ORDER THE REPLACEMENT PARTS OF COMPLETE NEW UNITS FROM THE FACTORY.** We will ship to you **and bill you for the cost.** This new invoice will then be a part of your claim for reimbursement from the Transportation Company. This, together with other papers, will properly support your claim.

Remember, it is extremely important that you **do not give the Transportation Company a clear receipt if damage or shortages are evident upon delivery.** It is equally important that you call for an inspection if the loss or damage is discovered later. **DO NOT, UNDER ANY CIRCUMSTANCES, ORDER THE TRANSPORTATION COMPANY TO RETURN SHIPMENT TO OUR FACTORY OR REFUSE SHIPMENT UNTIL WE HAVE AUTHORIZED SUCH RETURN.**

IMPORTANT

EQUIPMENT RETURN TO BALL ELECTRONIC DISPLAY DIVISION

1. Receive return authorization from the plant unless the unit was sent to you upon evaluation or rental.
2. Return prepaid.
3. Be sure a declared value equal to the price of the unit is shown on the bill of lading, express receipt, or air freight bill, whichever is applicable. This would cover claim for shipping damage on return.



WARRANTY

Ball Electronic Display Division certifies that each monitor will be free from defective materials and workmanship for one year from date of shipment to the original customer. The only exception will be the receiving tubes and solid state devices (transistors, diodes, etc.). Receiving tubes will carry a 90 day warranty, and the picture tube will have the standard one year warranty. With solid state devices, we will reflect the manufacturers' warranty.

Ball Electronic Display Division agrees to correct any of the above defects when the monitor is returned to the factory prepaid. Written authorization must be obtained and confirmed in writing by the Customer Service Department before returning the monitor to the factory.

Under this warranty, Ball Electronic Display Division will provide the necessary components required by the customer to correct the monitor in the field. The components will be shipped, prepaid, on a billing memo which will be cancelled upon receipt of the defective components at the factory. When ordering components for repair or replacement, the model number and serial number must be included on the customer request.

This warranty is invalid if the monitor is subject to mis-use, abuse, neglect, accident, improper installation or application, alteration or negligence in use, storage, transportation or handling and where the serial number has been removed, defaced or changed.

