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ABSTRACT and CONTENTS

This document specifies the special functions and branch conditions in the Data Communications Computer.

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p/c-n.r	page
SFBCDC/S- 28	1

Branch Conditions

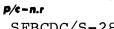
Ø	Never branch
1	Always branch
2	X=Ø
3	x≠ø
4	X<∅
5	x≥ø
6	x>ø
7	$Y \geq \emptyset$
1Ø	Y<Ø
11	RØ<Ø
12	RØ≥Ø
13	x≼ø
14	X= -1
15	X≠ -1
16	z≥ø
17	z<ø
2Ø	Always branch
21	$Y \land 7 \neq \emptyset$ (Y (15) \(Y (14) \(Y (13) = 1 \)
22	BL=Ø
23	BL≠Ø
24	Y (15) =Ø
25	Y(15)≠Ø

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p/c-n.r	Page
SFBCDC/S-28	2

Branch Conditions - 2

26	Attention latch $l = \emptyset$ (also resets the latch)
27	Undecoded
3Ø	Undecoded
31	Undecoded
32	Special flag $A = \emptyset$
33	Special flag A $\neq \emptyset$
34	Attention latch $2 = \emptyset$ Also resets
35	Attention latch $3 = \emptyset$
36	Attention latch $1 \neq \emptyset$
37	Undecoded
4Ø	Undecoded
41	Undecoded
42	Local memory parity error = 1 (resets the latch)
43	Undecoded
44	Undecoded
45	Undecoded



page 3

SFBCDC/S-28

Special Conditions

ø	No activity
1	LCY 1
2	LCY 2
3	LCY 3
4	LCY 4
5	LCY 8
6	LCY 12
7	Undecoded
1Ø	LCYØ
11	LCL Z (CCFZA)
12	LCH Z (CCFZB)
13	<pre>SKZ - Reference scratchpad with address in Z (SPFZ)</pre>
14	ALERT
15	POT
16	PIN
17	Undecoded
2Ø	Undecoded
21	Unusable
22	Undecoded
23	Undecoded
24	Undecoded
25	Undecoded



p/c-n.r sfbcdc/s-28

page

Special Conditions - 2 Reset T.U. (or other device attached 26 to I/O connector) Undecoded 27 Set special flag A ЗØ Occurs at end Reset special flag A of instruction 31 Undecoded 32 Undecoded 33 Undefined 34 Undecoded 35 Undecoded 36 Undecoded 37 Store 4ø 41 Store 42 Store Memory Reference Store 43 Fetch 44 Fetch 45 Fetch 47 Undecoded 6ø Undecoded 61 Undecoded 62

Memory Reference

Fetch

Fetch

64

65

5

Undefined means that the signal is brought off the card in the low true sense to be used as a special function if needed or, in the case of branch conditions, an input to the branch condition gate is brought to a pin for use if needed.

Undecoded means that the condition is presently not wired on the board.

Unusable means to avoid conflict with the TP's, this function is not used in the Model 1.

There exist two Always Branch conditions to reduce the number of diodes in the MC5 bit in the ROM.

Attention Latches operate as follows: They are set at the end of the global cycle with K2. They are cleared at the end of the interval in which branch is tested, unless the set exists simultaneously, in which case the latch is set. This means if the latch was set, the branch was unsuccessful and attention was sent, the latch will still be set at the end of the branch instruction.

Special Flag A is set and cleared with special function at the end of state A or state B depending on whether or not VCY is set.



p/c-n.r SFBCDC/S-28 page 6

Parity error latches are set upon receipt of an error and cleared upon branching, like the attention latches.

ALERT, POT, and PIN are discussed in MPPI/S-16, "Microprocessor Pot/Pin Interface."