

SUPER BEE COMPUTER TERMINAL



**BEEHIVE MEDICAL ELECTRONICS, INC.
870 WEST 2600 SOUTH
SALT LAKE CITY, UTAH**

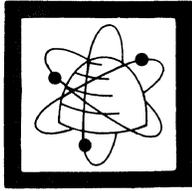
WARRANTY

Beehive Medical Electronics, Inc. certifies that each terminal will be free from defective materials and workmanship for 90 days from date of shipment to the original customer.

B.M.E.I. agrees to correct any of the above defects when the terminal is returned to the factory prepaid. Return authorization must be obtained and confirmed in writing by the Field Service Department before returning the terminal to the factory.

Under this warranty, B.M.E.I. will provide the necessary components required by the customer to correct the terminal in the field. The components will be shipped, prepaid, on a billing memo which will be cancelled upon receipt of the defective components at the factory. When ordering components for repair or replacement, the model number and serial number must be included on the customer request.

This warranty is invalid if the terminal is subject to misuse, abuse, neglect, accident, improper installation or application, alteration or negligence in use, storage, transportation or handling and where the serial number has been removed, defaced or changed.



Beehive Terminals

Beehive Medical Electronics, Inc.

MALFUNCTION REPORT

Dear Customer:

We are trying to manufacture the most reliable product possible. You would do us a great courtesy by completing this form should you experience any failures.

1. Type Unit _____ Serial No. _____

Module (if applicable) _____

2. Part failed (Name and Number) _____

3. Cause of failure (If readily available)

4. Approximate hours/days of operation to failure _____

5. Failure occurred during:

Final Inspection Customer Installation Field Use

6. Personal Comment:

Customer _____

Address _____

Signed _____

Date _____

Beehive Medical Electronics, Inc.
c/o Field Service Department
870 West 2600 South
P.O. Box 19244
Salt Lake City, Utah 84120

RETURNING PARTS/EQUIPMENT
FOR REPAIR

When the terminal requires service or repair in accordance with the enclosed warranty, unnecessary delays may be avoided when parts or equipment are returned to B.M.E.I. using the following procedures:

1. Contact B.M.E.I.'s Field Service Department for Return Authorization. An R.A. Number will be issued and used for future reference.
2. Package the unit or part in accordance with the method of shipment. Enclose a list of the material being returned and the reason for returning it. Reference the Return Authorization Number on the shipping label. If the number is not visible, the Receiving Department may refuse to accept the shipment.
3. Send the unit or part, transportation prepaid, to the address stipulated for returning parts and equipment.

All equipment and parts described in the warranty will be replaced provided B.M.E.I.'s examination discloses that the defects are within the limits of the warranty. If damages or defects are not within the limits of the warranty, the customer will be notified of the extent of repairs required and the cost. The unit will be repaired and returned upon agreement and receipt of a written purchase order number.

When returning parts and/or equipment for repair, please use the following address:

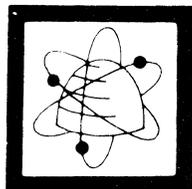
Beehive Medical Electronics, Inc.
870 West 2600 South
Salt Lake City, Utah 84119

SUPER BEE COMPUTER TERMINAL

SERVICE MANUAL

MARCH 1974

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OPTION CONFIGURATION FOR: _____

SERIAL NUMBER: _____

FUNCTION	BACK PANEL	PROCESSOR BOARD	INTERCONNECT BOARD	SWITCH BOARD	INTERNAL
HALF/FULL DUPLEX	SWITCH HDX _____ FDX _____				
LOWER CASE INHIBIT	SWITCH ENBL L. C. ___ INHBT L. C. ___				
I/O BAUD RATE SELECT	SWITCH 1 ___ 16 ___ 2 ___ 32 ___ 4 ___ 64 ___ 8 ___				
I/O BAUD RATE MULTIPLIER	SWITCH 110 _____ 150 _____				
AUTO EFFECIENT PAGING	SWITCH AUTO EFF PAGE _____ RRLF _____				
PSEUDO POLL		STRAP IN _____ OUT _____			
BACK SEARCH BLOCK TRANSMIT		STRAP IN _____ OUT _____			
PARITY TEST		STRAP IN _____ OUT _____			
ASYNC / SYNC OPERATION		STRAP IN _____ OUT _____			
SEND CONTROL CODES		STRAP IN _____ OUT _____			
GO-OFF-LINE		STRAP IN _____ OUT _____			
EXT CLOCK		STRAP IN _____ OUT _____			
STORE SPECIAL FUNCTIONS		STRAP IN _____ OUT _____			
PRINTER BAUD RATE SELECT				STRAP 1 ___ 16 ___ 2 ___ 32 ___ 4 ___ 64 ___ 8 ___	
PRINTER BAUD RATE MULTIPLIER				STRAP 110 _____ 150 _____	
TTL KMIT CLOCK				STRAP 1 ___ 8 ___ 2 ___ 16 ___ 4 ___	
POWER OPTION					STRAP IN _____ OUT _____

SECTION I

GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides a general equipment description and installation and operation instructions for the SUPER BEE Computer Terminal. Section I provides a general description and the specifications of the terminal and Section II provides basic operating procedures. Installation procedures are given in Section III. This manual provides the operator with sufficient information to obtain a thorough understanding of the operational characteristics of the equipment.

1.2 PRODUCT DESCRIPTION

The SUPER BEE Computer Terminal shown in Figure 1-1, is a self-contained, operator controlled remote display terminal with a detached ANSI keyboard. The terminal is designed for use in serially transmitting information to, and receiving information from, an interconnected data source. The terminal will operate to exchange data at any of several preselected transmission rates; 9600 baud maximum.

The SUPER BEE employs a 12-inch (measured diagonally) rectangular television type monitor which is implemented to display up to 25 lines with 80 characters. Each character is generated from a 5- by 7-dot matrix with two-dot spacing between adjoining characters.

The SUPER BEE Terminal has a detached keyboard interfaced to the display unit by means of a flexible 4-foot cable. The keyboard employs the N-key roll-over feature. When any alphanumeric key is held down for longer than half a second, it automatically repeats at a rate of approximately 30 characters per second. Some of the control keys also auto repeat, however auto repeat has been inhibited where not meaningful.

Interfacing is accomplished via the rear panel connectors. The Input/Output and Printer connectors are connected in parallel and will interface most standard serial ASCII printers. The printer data can be transmitted at a separate baud rate from that of the terminal and may

be adjusted from 110 to 9600 baud. A Video connector is provided for connection to a remote display monitor. The output from this connector is a composite video signal capable of driving 1000 feet of 50-ohm coaxial cable.

1.3 PERFORMANCE CHARACTERISTICS

1.3.1 Modes of Communication

Half-Duplex/Full-Duplex Transmission

The SUPER BEE Terminal may be operated off-line or on-line. A rear panel switch allows the operator to select either half-duplex (HDX) or full-duplex (FDX) communications. Full-duplex operation allows data to be transmitted with each keyboard entry wherein the terminal's receiver input is enabled for immediate computer reply of the transmitted data (echoplex) to verify proper receipt of data. Half-duplex data transfer is generally used for sending precomposed messages, either a few lines at a time (block mode) or an entire memory dump at a time (page mode). While transmitting data in either the page or block modes, both the keyboard and the receiver inputs are disabled. Operation in the off-line mode allows the operator to edit the message before block transmission of the data. Operation in the on-line mode enables the transmitter and the receiver.

Synchronous or Asynchronous Transmission

The SUPER BEE Terminal allows the selection of either serial synchronous or serial asynchronous transmission. During synchronous operation, the word structure consists of eight bits; seven data bits and a parity bit. Synchronization is accomplished by receiving and identifying two or more sync codes at the beginning of a transmission; synchronous operation is not possible during conversational type transmission (character by character). The asynchronous word structure consists of a start bit, seven data bits, a parity bit, and one or two stop bits (One stop bit if baud rate switch is in

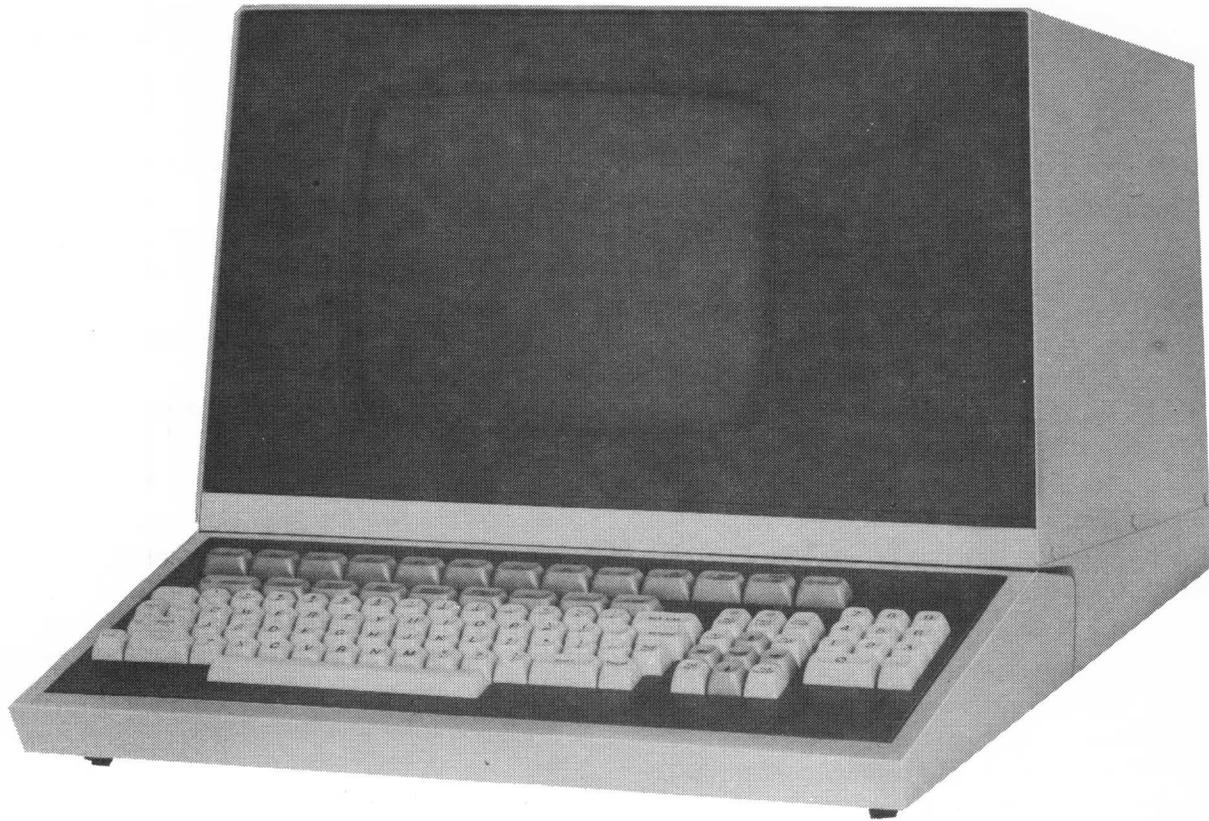


Figure 1-1
SUPER BEE Computer Terminal

X150 position and 2 stop bits when in X110 position).

Data Compression

Delete codes are used in data compression to eliminate the transmission of trailing spaces. Transmission of only operator-entered data is possible by placing a delete code after the data to be transmitted. (Data on the line after a delete code is not transmitted.) When a delete code is encountered during transmission, a Carriage Return and Line Feed (CR-LF) are sent as a record separator and a CR-LF are performed by the terminal. Transmission continues at the first character location in the next line.

Conversational Transmission

During conversational transmission, the CRT terminal must be on-line. Received alphanumeric characters are stored in memory and displayed. Received control codes or ESC sequence codes cause the unit to perform the appropriate function and are not stored in memory or displayed. An exception is the "NEW LINE" code which is acted upon and displayed as a space. Keyboard-generated alphanumeric characters are transmitted to the computer. In full-duplex operation, control codes and ESC sequence codes are transmitted but not acted upon until echoplexed to the terminal.

Block Transmission

Block transmission is used to allow the operator to prepare data off-line and then transmit the data as a unit. The transfer can be initiated either from the keyboard or the I/O or the printer. A block transfer is initiated from the keyboard by depressing the ENTER key.

If the terminal is strapped for the Pseudopoll on and ETX search off, the following sequence is performed:

- a. The cursor is positioned in the first character location in the memory or in format mode, the first character location in the first unprotected field.
- b. The terminal transmits a DC1 code on the I/O and waits to receive an ETB (Control W) from the I/O.

- c. Upon receipt of the ETB, data is transmitted out on the I/O until an ETX code is transmitted, at which time transmission is stopped.

A block transfer initiated remotely from the I/O requires the ETX code to be received and the cursor to be positioned at the location where desired transmission will commence upon the receipt of an ETB (Control W). The transfer proceeds as though it were initiated from the keyboard. When Pseudopoll is configured to off, the data transmission begins as soon as the Clear-to-Send signal is received from the I/O.

If the ETX search is configured to on, a reverse search is made for the most recent ETX code in the memory. When located, the cursor is positioned at the first character location in the next line. The transfer will begin from that point.

When the terminal is strapped for pseudopolling off, it is the CPU's responsibility to see that an ETX is placed in memory before sending the terminal an ETB.

When a NEW LINE code or DELETE code is encountered in the memory during a block transfer and while operating in the Character mode, a CR-LF function is performed and is transmitted to the I/O and the printer's I/O. There should not be an ETX code stored after a DELETE code in the same line. When the DELETE code or a protected location in the memory is sensed, the CR-LF function codes are transmitted to the I/O and the printer I/O internally, a TAB function is performed.

The block transfer operations are performed the same for a PRINT command except that when an ETX is sensed, the CR-LF codes are transmitted in place of the PRINT command. The terminal can also be configured to switch to off-line (local) after printing.

When the CPU ends transmission of a block of data while in synchronous mode and the terminal is to remain on-line, the following codes can be used to re-establish sync with the computer:

Cursor Sense: will start a sync search, after sending out the cursor address, until the CPU sends out a new block of data.

Print: Without go-off-line, will reply with fewer sync codes and go into sync search.

Baud Rate Selection

Transmission rates are switch-selectable at the rear of the terminal. The baud rate switch has seven positions 1, 2, 4, 8, 16, 32, and 64. The baud rate multiplier switch has two positions; 110 times or 150 times. The selected position causes the selected baud rate to be multiplied by 110 or 150. The switches produce rates of 150, 300, 600, 1200, 2400, 4800, and 9600 baud for 10-bit word operation; or 110, 220, 440, 880, 1760, 3520 and 7040 baud for 11-bit word operation.

1.3.2 Operating Modes

The SUPER BEE Computer Terminal normally operates in one of three modes; the Character mode, the Program Entry mode, and the Format mode. In each mode, the SUPER BEE can be operated either on-line or off-line.

Character Mode

Character mode is selected upon power-on or depression of the RESET key. In this mode, the monitor displays all characters and reacts to all control codes. Depression of RESET key automatically returns the terminal from any other mode to Character mode.

Character Mode (Off-Line) - Characters entered from the keyboard are stored in the terminal memory and displayed but not communicated to the I/O port. Control and escape sequence codes are dependent upon appropriate strapping. Characters received at the I/O port are ignored.

Character Mode (On-Line) Characters entered from the keyboard are transmitted from the I/O port as they are entered. If operated half duplex (HDX), the characters are stored in the memory and displayed as they are entered. When operated full duplex (FDX), the characters are transmitted to the I/O port only, and are stored in the memory and displayed if a remotely connected data source echoes each transmitted code.

Program Entry Mode

A Program Entry mode is selectable from the keyboard or from a remote data source initiated by an escape sequence code. When in the Program Entry mode, the terminal does not respond to control and escape codes, but stores these codes in memory and displays their associated character or symbol. NEW LINE and ENTER functions are exceptions. They are displayed in normal video and acted upon. The Program Entry mode is intended to display control characters and escape sequence characters prior to transmission or after receipt of a transmission. Programming from the terminal is made possible through the implementation of the Program Entry mode.

Program Entry Mode (Off-Line)- Characters entered from the keyboard are stored in the terminal memory and displayed but not transmitted to the I/O port. Control codes are displayed as special symbols and are not acted upon, with the exception of NEW LINE and ENTER. Escape function characters are displayed in reverse video and are not acted upon.

Program Entry Mode (On-Line)- The terminal operates the same as that for the Program Entry mode (off-line), with the exception that data entered from the keyboard is transmitted to the I/O port. The transmitted control escape and sequence codes are dependent upon appropriate strapping.

Format Mode

A Format mode is selectable from the keyboard or from a remote data source initiated by an escape sequence code. In the Format mode, the terminal display has protected fields in which the cursor can be positioned, but no data may be entered. If desired, unprotected fields may be delimited by use of brackets or reverse video to indicate the area for data entry.

Format Mode (Off-Line)- Characters entered from the keyboard are stored in the unprotected locations in the terminal's memory and displayed but are not transmitted to the I/O port. Select-

able edit functions (INSERT LINE and DELETE LINE) are inoperative in Format mode.

Format Mode (On-Line)- Operation in this mode is the same as that for Format mode (Off-Line), except that data entered from the keyboard is transmitted to the I/O port. A CR-LF is transmitted at the end of each field as a field delimiter.

Print-On-Line Mode

The Print-On-Line mode is a selectable keyboard function or initiated from a remote data source. The I/O baud rate is slaved to the selected printer baud rate of the SUPER BEE when the terminal is operating in the Print-On-Line mode. The data sent to or received by the terminal is both displayed on the terminal and printed by the printer. Data transmitted from the terminal is sent to both the I/O port and the printer port at the selected printer baud rate. The CPU will supply null codes for the "Line Full" on the print when the terminal in Print-on-Line mode.

1.3.3 Display Organization

The display is organized on a page basis, where the page contains 25 lines with 80 character positions in each line. Any of the 96 USASCII codes can be displayed on the monitor in a line-page organization. If a line in the memory has less than 80 characters, the displayed line contains blanks or spaces filled to the 80th character.

Upon power-up or depression of the RESET key, the Character mode is selected. In this mode of operation, the CRT monitor displays all characters and reacts to all control codes. A keyboard or I/O code selectable Program Entry mode prevents the terminal from reacting to control and escape function codes, and displays instead the control symbols and escape function codes as reverse video characters. In the Format mode of operation, protected areas of the display cannot be erased or overwritten.

When it is required that data serve as alarm or status indicators or direct attention, video can be displayed as follows: (1) normal

video (white characters on a black background); (2) normal video blinking; (3) reverse video (black characters on a white background); and (4) reverse video, blinking. These functions are initiated by an escape sequence operation which stores a single video control character in memory and which is displayed as a space. The reverse video and/or blink field is terminated by the end of the line or by either the NEW LINE or Line-Blink-Off codes. Additionally, all level video and blink control codes in memory may be reset with space codes by the Page-Blink-Off command.

1.3.4 Memory Organization

The memory in the SUPER BEE terminal is organized in such a manner that only the display characters and receiving control codes are stored in memory. This means that if only 10 characters are written on a line, only 10 memory locations are used for display of that line. The other 70 spaces on that line are not stored. This technique is known as "efficient paging." The total number of memory locations is 2048. This means, for instance, that through the use of efficient paging, 256 lines of 7 characters each can be stored (The maximum number of lines is limited to 256). Only 25 lines of memory data can be displayed at one time; however, the memory can be scrolled up or down to bring any 25-line window of the memory data into view.

When a CLEAR operation is performed the entire memory is filled with space codes and the cursor is positioned home. The memory is then organized as 80 characters per line and displayed as an entire blank screen. As data is entered, display characters replace the space character as defined by the cursor location. The memory organization remains the same until a "NEW LINE" code is entered into the terminal. The "NEW LINE" code is stored into the display memory at the cursor location and terminates the display of that particular line. (The remaining part of that line is displayed as blanks that occupy no memory locations.) The code entered immediately following the "NEW LINE" code in memory is displayed as the first character on the next

line. If the 80 character by 25 line format must be retained, the Carriage Return-Line Feed (CR-LF) functions may be keyed in to move the cursor to the first character position on the next line. After all 2048 memory locations are used up, the memory continues to receive data and scrolls up. At the end-of-memory indicator, when a new character is received, a line of data is lost from the top of the memory.

The cursor is always displayed on screen and if any cursor control is given which would move the cursor off the display, the display will be scrolled up or down so that the cursor will remain displayed on the screen. With efficient paging, the cursor may be positioned to an undefined location on a particular line by moving it to the right of the New Line (N/L) position. When this happens, data cannot be entered on this portion of the line to the right of where the N/L code was entered. If insertions are to be made in a particular line, the cursor must be positioned to a character located to the left or under the N/L position. Any time the cursor is under the N/L position, the terminal automatically operates as though in the Insert Character mode.

1.3.5 Memory Overwrite

When data input has filled all memory locations, Cursor Right and Cursor Down are inhibited to prevent the cursor from moving through end-of-memory. If the last line of memory appears as the first line of the display, Scroll Up, Next Page, Cursor Right and Cursor Down functions are inhibited so that they do not move the cursor beyond the end of the 2048 memory locations. Line Feed (LF), Horizontal Tab (HT), and simply writing data will cause Memory Overwrite to occur. When memory overwrite does occur, the first line of memory is filled with DEL codes and made available for additional data. Care must be taken that these DEL codes do not cause mistakes if the memory is to be retransmitted, as DEL codes are interpreted as CR-LF codes and will cause the ETX code to be missed if preceded by a DEL code in the same line.

1.3.6 Space Overwrite (SPOW)

The space bar normally writes a space code in memory and advances the cursor one character position to the right. However, following the operation of a Carriage Return (CR), the space code re-acts to perform a Cursor Right function but does not write a space. The SPOW latch is reset by performing a NEW LINE, Line Feed, HOME or TAB function.

1.3.7 Character Overwrite

When an error is made in entering a character (e.g., a misspelled word) a correction can be made by overwriting the character. The cursor is returned to the character in error by using Cursor Right, Left, Up or Down functions to locate the cursor directly under the character to be corrected. The correct character can then replace the old character. The use of Delete Character or Insert Character functions may be required to allow for a fewer or greater number of characters.

1.3.8 Special Function Keys

Eight special function sequence keys (F-1 through F8) are provided to allow the user to call up routines unique to the user. Any of the eight escape sequence codes (ESC and p through ESC and w), when generated by the keyboard, are stored as a two-code sequence starting at the cursor's location in the memory. When the terminal is configured to "store special function", the two-code sequence is stored in page memory. When the terminal is configured to "send special function", the two-code sequence followed by an ETX is stored in memory and the ENTER function is performed. During the ENTER function, if the terminal is configured for psudeopolling, the "Request For Service" code DC1 is sent and the terminal waits for an ETB to begin transmission.

1.3.9 Printer Port

The serial printer port operates at RS232C logic levels and outputs negative-true data. The SUPER BEE terminal has two printer communication modes: (1) Print-On-Line, and (2) Print. In the Print-

On-Line mode, the I/O baud rate is slaved to the selected printer baud rate of the SUPER BEE. Data sent to or received by the SUPER BEE terminal is both displayed on the terminal and printed by the printer. Data transmitted from the terminal is sent to both the I/O port and the printer port at the selected printer baud rate. The Print-On-Line mode is selectable from the keyboard or from a remote data source, initiated by an escape sequence code. The Print mode provides the capability of receiving data from the remote data source at a baud rate different from that of the printer. In this mode, the CRT terminal buffers between the printer and the remote data source. The Print mode is selectable from the keyboard or from a remote data source, initiated by an escape sequence code.

1.3.10 Input/Output Port

The I/O port operates at RS232C logic levels and outputs and receives negative-true data. The I/O port outputs data to and inputs data from the remote data source when the terminal is in the on-line condition.

1.3.11 I/O Processor Board Strapping

There are eight strappable options available on the SUPER BEE I/O Processor board. These options are implemented by installing the appropriate jumper on the 16-pin strapping pad (S1). A brief summary of these strapping selections is provided in the following paragraphs.

Send Control Codes

All escape codes entered by the keyboard will be performed and transmitted. With the control codes strap installed, all escape sequences are performed locally only, but not transmitted.

Go-Off-Line

At the end of a block transmit, an ETX is transmitted and the on-line mode is maintained. With a go-off-line strap installed, the unit goes off-line at the end of transmission and no ETX is transmitted.

Store Special Functions

Without this strap installed, special function codes are transmitted. With this strap installed, special functions are stored only and not transmitted.

External Clock

The SUPER BEE uses its own internal clock. However, with this strap installed, it provides for the use of external clocks provided by a modem or other interface.

Synchronous or Asynchronous Operation

The SUPER BEE is configured to operate asynchronously. With this strap installed, the terminal operates in the synchronous mode and generates words of eight bits. While operating in the asynchronous mode, the length of the generated word is determined by the multiplier toggle switch position. In the 110 position, an 11-bit word is generated. A 10-bit word is generated in the 150 position.

Block Transmit

With this strap installed, the SUPER BEE is configured to perform a block transmit. (This strap is installed as shipped from the factory.) Without this strap the SUPER BEE is configured to do a page transmission.

Pseudopolling/Immediate Block Transmit

Operation of the ENTER key or any of the eight special-function keys stores an ETX and positions the cursor at the beginning of the text. In the pseudopolling mode, a request for service code (DC1 octal 21) is transmitted and the terminal waits to receive a clear-to-transmit code (ETB octal 27) before transmission of the text begins.

Parity Test

SUPER BEE checks incoming data for even parity when operating asynchronously and odd parity when operating synchronously. With this strap installed, no parity check is made. Transmitted data is in the same sense as received data, with the exception that data is transmitted with a mark parity bit with strap installed. A parity error symbol (reverse video, backward question mark) is displayed whenever an invalid character is sensed by the parity test.

1.4 ACCESSORIES

The following accessories are available for use with the SUPER BEE Computer Terminal:

- a. Current loop adapter, part number 112-0606, (requires terminal to include interconnect Board, part number 112-0609, and Interface assy. part number 112-0605).
- b. Acoustic soupler cable, part number 112-0031.
- c. Nova computer serial I/O cable, part number 112-0040.
- d. Hewlett-Packard 2000-Series serial I/O cable, part number 112-0048
- e. Printer cable, part number 112-0106.

1.5 SPECIFICATIONS

Specifications of the SUPER BEE Computer Terminal are given in Table 1-1.

Table 1-1. SUPER BEE Computer Terminal Specifications

CHARACTERISTIC	DESCRIPTION
Power Requirements	115/230 Vac (± 10 percent), 50/60 Hz, single phase, 180W maximum, 225 VA maximum.
Display Size Standard Optional	12 inches (305 mm) rectangular. 15 inches (381 mm) rectangular.
Active Display Size Standard Optional	6- $\frac{1}{2}$ inches x 7- $\frac{1}{2}$ inches (165 mm x 190 mm) approx. 8 inches x 10 inches (203 mm x 254 mm) approx.
Display Format	25 lines of 80 characters.
Character Type Standard	5 x 7 dot matrix (7 x 10 scan), approximately 0.08 x 0.20 inches.
Character Set	224 displayable as follows: 32 control characters 64 upper case ASCII set 32 lower case ASCII set (with descenders shifted down two scans) 96 escape sequence control codes.
Page Overflow	Upward scroll - No loss of data until memory overflow.
Memory Overflow	Wrap around and first line of data is lost from memory.
Communications Interface	Per EIA Standard RS232C.

Table 1-1. SUPER BEE Computer Terminal Specifications (Continued)

CHARACTERISTIC	DESCRIPTION
Printer Interface	Per EIA Standard RS232C.
Video Port	Composite video for remote monitor.
Signal Characteristics Transmit Mark Space Receive Mark Space	<p>–15 volts +10 volts</p> <p>–3 to –25 volts +3 to +25 volts</p>
Transmission Rates 11 bit 10 bit	<p>110, 220, 440, 880, 1760, 3520, and 7040 150, 300, 600, 1200, 2400, 4800 and 9600</p>
Transmission Code	8-bit USASCII.
Baud Rate Selection	Switch selectable.
Parity	Asynchronous-even/none (Parity Bit= Mark) Synchronous-odd/none (Parity Bit = Mark)
Refresh Rate	60 Hz (50 Hz optional)
Display Memory	MOS shift registers
Memory Organization	Efficient Paging
I/O Controller	Microprocessor
Program Memory	MOS ROM
Video	Standard, Blinking, Reversed and Blinking Reversed
Character Generation	MOS ROM
Erase Functions	<p>Clear Memory Erase to end of line (end of field in format mode) Erase to end of memory (unprotected fields in format mode)</p>

Table 1-1 SUPER BEE Computer Terminal Specifications (Continued)

CHARACTERISTIC	DESCRIPTION
Edit	Page Mode or Line Mode Insert Line Delete Line Insert Character Delete Character
Operation Modes	Character Format On-Line Program Entry Print-On-Line Page/Line Edit Insert Character
Format	Enable field protection
Transmission Modes	Half Duplex or Full Duplex 11 Bits Asynchronous 10 Bits Asynchronous 8 Bits Synchronous Block/Page Data Compression (Format and Non-Format modes)
Printer Mode	ON LINE/OFF LINE
Strapping Options	Printer Baud Rate Auto Efficient Paging Internal Clock Multiplier Internal/External Clock Parity Pseudopolling Go-Off-Line Block/Page Transmit Store Special Functions
Bell	Audible alarm when Control G is received, and on the 72nd character of a line when keyboard data is being entered.
Cursor Type	Non-destructive blinking underscore.

CHARACTERISTIC	DESCRIPTION
Cursor Controls	Horizontal tab (forward and back) Cursor up Cursor down Cursor left Cursor right Home Carriage return Line feed New line Format tab (forward and back)
Cursor Address	Positions cursor to the character number and line number specified.
Cursor Sense	Cursor location transmitted upon request.
Space Overwrite (SPOW)	Space bar functions as cursor-right key which inhibits Space Code generation (Non-destructive).
Operator Controls Keyboard/ Rear Panel	Brightness Control (thumb wheel) FDX/HDX Switch (full-/half-duplex) Lower Case Character inhibit switch I/O Baud Rate Switch Contrast Control Power Switch
Function Keys	PRINT ENTER ERM EOL PREV PAGE NEXT PAGE SCROLL UP SCROLL DOWN TAB TAB SET TAB CLEAR
Special Function Keys	8 special function keys (F1 through F8)

Table 1-1 SUPER BEE Computer Terminal Specifications (Continued)

CHARACTERISTIC	DESCRIPTION
Dimensions Width Height Depth (w/Keyboard) Depth (less Keyboard) Depth (Keyboard only) Weight Monitor Keyboard Operating Temperature	20 inches (508 mm) 16 inches (406.4 mm) 26-½ inches (673 mm) 17-¼ inches (438 mm) 12-½ inches (317 mm) 55 pounds (25 kg), approx. 10 pounds (4.54 kg), approx. +5-°F to 104°F (+10°C to +40°C)

1.6 IDENTIFICATION

An identification plate located on the bottom cover plate of the terminal provides the terminal model number, serial number, weight, voltage and current requirements, and frequency and power classification.

SECTION II OPERATION

2.1 INTRODUCTION

This section provides operating instructions for the SUPER BEE Computer Terminal. The operating instructions include descriptions of the operator controls and indicators, general operating procedures and operating instructions. The general operating procedures provide information for operating personnel. The operation instructions provide information that allows a programmer to vary the operational format to the extent presented herein.

2.2 OPERATOR CONTROLS AND INDICATORS

The operator controls and indicator are defined in Tables 2-1 and 2-2 and are depicted in Figures 2-1 and 2-2. Table 2-1 describes the keyboard controls and indicators and Table 2-2 describes the monitor rear panel controls. Figure 2-1 depicts the keyboard and Figure 2-2 depicts the monitor rear panel.

**Table 2-1. SUPER BEE Computer Terminal Keyboard,
Controls and Indicators**

KEY OR CONTROL	FUNCTIONS
CONTROL AND FUNCTION KEY GROUP	
F1 through F8	Eight special function keys that generate two-code sequences which are entered in the memory when the terminal is on-line. Functions are undefined unless terminal is appropriately strapped.
FMT (Format)	Terminal is placed in Format mode. Key includes indicator that lights when the terminal is in Format mode. In this mode, the cursor is moved to first unprotected memory location. When the key is pressed and unlatched, the terminal is placed in Character mode and indicator extinguishes.
ON-LINE	Terminal is placed in the On-Line Character mode, and the key indicator lights. The transmit and receive circuitry, and keyboard are enabled. If synchronous I/O has been selected, the terminal will wait for synchronization from the computer. The terminal will not go on-line in response to a command from the computer.
PROG ENTRY	Lights key indicator, resets Format (FMT) mode, sets Program Entry mode to on. When this mode is on, all printing characters as well as control codes and escape sequence codes display their assigned characters. The escape sequence codes are displayed as reverse video and only the New Line and ENTER functions can be performed. When the key is pressed and released, Program Entry mode and the key indicator are turned off.

Table 2-1. SUPER BEE Computer Terminal Keyboard,
Controls and Indicators (continued)

KEY OR CONTROL	FUNCTION
CONTROL AND FUNCTION KEY GROUP (continued)	
PRINT ON LINE	<p>Sets the terminal to Print-On-Line mode and lights the key indicator. All printing characters and control functions that are received or transmitted by the terminal are applied to the printer I/O. In this mode, the I/O baud rate can assume the printer's baud rate. This function can be used as a high-low baud rate selection switch when a printer is not slaved to the terminal. When the key is pressed and released, the key indicator is turned off and the Print-On-Line function is reset. The I/O baud rate is restored to the I/O switch setting.</p>
RESET	<p>Resets the terminal mode of operation to Character off-line mode. The cursor is moved to the home position. The following functions or modes are reset to the off condition: FMT, ON-LINE, PROG ENTRY, PRINT-ON-LINE, PAGE EDIT, INS CHAR, page blink, and SPOW. The keyboard is enabled and the protect latch is set. (Note: The RESET function does not erase the display screen.)</p>
ENTER	<p>When the terminal is in Character mode, an ETX is written at the present cursor location, then the cursor returns to home or to the first character on the next line below the preceding ETX (strap option). The terminal is placed on-line and starts transmitting data from the cursor position to the next ETX. When the ETX is read and transmitted, the transmission stops and the cursor is located in the next character location following the ETX. If the unit is strapped for pseudopolling sequence, an ETX is written at the present cursor location and the terminal is placed on-line. However, before transmission starts, the terminal transmits a DCI (Control Q code) on the I/O and enables the data receiver to accept an ETB (Control W) from the I/O before initiating transmission.</p> <p>When the terminal is in the Format mode, the same sequence occurs as that which occurs in the Character mode, except that only data in the unprotected fields are transmitted.</p> <p>When the terminal is in the Program Entry mode, the same sequence occurs as that for the Character mode.</p>
PRINT	<p>When the terminal is in the Character mode, an ETX is stored at the cursor location when the command is received. The same sequence occurs as that for the Character mode ENTER command, except that data is outputted through the printer I/O. The ETX is transmitted as a CR-LF. In pseudopolling, the printer does not have to respond with an ETB (Control W).</p> <p>In the Format mode, the same sequence occurs as that for the Character mode, except that only data in the unprotected fields are transmitted to the printer. A CR-LF is generated between every unprotected field.</p>

**Table 2-1. SUPER BEE Computer Terminal Keyboard,
Controls and Indicators (continued)**

KEY OR CONTROL	FUNCTION
CONTROL AND FUNCTION KEY GROUP (continued)	
PRINT (cont.)	<p>In the Program Entry mode, the special character is displayed in reverse video and the cursor moves to the next descending character location in the memory.</p>
ERM (Erase to End of Memory)	<p>When the terminal is in the Character mode, all memory locations from the cursor to the end of the memory are filled with space codes.</p> <p>In the format mode, all unprotected memory locations from the cursor to the end of the memory are filled with space codes.</p> <p>In the Program Entry mode, the code J is displayed in reverse video and the cursor moves to the next descending memory location.</p>
EOL (Erase to End of Line)	<p>When the terminal is in the Character mode, all memory locations from the cursor location to the end of the current line or New Line code are filled with space codes.</p> <p>In the Format mode, all memory locations from the cursor location in an unprotected field to the end of that field are filled with space codes.</p> <p>In Program Entry mode, the code K is displayed in reverse video and the cursor moves to the next memory location.</p>
NEXT PAGE	<p>When the terminal is in Character or Format modes, the display is moved up 25 lines and the cursor is repositioned at the first character location of the display in Character mode. In Format mode, the cursor is repositioned to the first unprotected character location on that page. When the last line of the memory is the first line of the display, the command is ignored and the contents of the memory are unchanged.</p> <p>In the Program Entry mode, the code U is displayed in reverse video and the cursor moves to the next descending memory location.</p>
PREV PAGE	<p>When the terminal is in the Character or Format modes, the display moves 25 lines down with the cursor repositioned at the first character location of the display. In the Format mode, the cursor is repositioned to the first character location in the first unprotected location on that page. When the first line of the memory is displayed, the command is ignored and the contents of the buffer remain unchanged.</p> <p>In the Program Entry mode, the code V is displayed in reverse video and the cursor moves to the next descending memory location.</p>
SCROLL DOWN	<p>When the terminal is in the Character or Format modes, the display moves down one line. The command will be ignored if the first line of the memory is displayed. The cursor location stays in the same column</p>

Table 2-1. SUPER BEE Computer Terminal Keyboard,
Controls and Indicators (continued)

KEY OR CONTROL	FUNCTION
CONTROL AND FUNCTION KEY GROUP (continued)	
SCROLL DOWN (cont.)	<p>and line in which it is currently displayed until that line reaches the last line of the display. Then the cursor is moved up one line at a time for each line scrolled down and the contents of the memory remain unchanged.</p> <p>In the Program Entry mode, the code T is displayed in reverse video and the cursor moves to the next descending memory location.</p>
SCROLL UP	<p>When the terminal is in the Character or Format modes, the display moves up one line. The command is ignored when the last line of the memory is the top line of the display. The cursor stays in the same column and line to which it is located until that line reaches the top of the display. Then the cursor moves down one line for each line scrolled up and the contents of the memory remain unchanged.</p> <p>In the Program Entry mode, the code S is displayed in reverse video and the cursor moves to the next descending memory location.</p>
CLEAR	<p>When the terminal is in the Character mode, all memory locations are reset to space codes, all tabs are cleared, and cursor moves to the home position.</p> <p>In the Format mode, all unprotected locations of the memory are reset to space codes, and the cursor is moved to the first unprotected location in the memory.</p> <p>In the Program Entry mode, the code E is displayed as a reverse video character and is not acted upon.</p>
ESC (Escape)	Control key that generates the initial code in an escape code sequence.
CTRL (Control)	When pressed with any alpha key, the code structure of the alpha key is changed by forcing the seventh bit to 0. This allows operation of the control codes assigned to columns one and two of the ASCII Code Chart.
LF (Line Feed)	<p>When the terminal is in the Character and Format modes, the cursor is positioned one line down in the same column and the SPOW latch is reset to a destructive space bar. If the cursor's position in the next descending line would be beyond the end of the memory, then memory overwrite will occur, and the first line in the buffer will be lost. Also, if the terminal has been configured for Automatic Efficient Paging, and the command preceding the Line Feed is a RETURN, a NEW LINE code will be stored and displayed (strap option) at the location in the memory where the cursor was located when the RETURN was generated.</p>

**Table 2-1. SUPER BEE Computer Terminal Keyboard,
Controls and Indicators (continued)**

KEY OR CONTROL	FUNCTION
CONTROL AND FUNCTION KEY GROUP (continued)	
LF (Line Feed) (cont.)	In the Program Entry mode, the Line Feed control J symbol is displayed and the cursor moves to the next descending character location in the buffer.
NEW LINE	In Character, Format and Program Entry modes, the special character can be displayed or not displayed; however, it will be stored in memory. The SPOW latch is reset so that the space bar becomes destructive. When the cursor is positioned beyond the NEW LINE character of a given line, characters cannot be entered in the memory nor will they be displayed.
RETURN	When the terminal is in Character and Format mode, the cursor is caused to reposition on the first character location of the current line. Return sets the SPOW latch to a non-destructive space bar. In Program Entry mode, the code € is displayed and the cursor moves to the next descending character location in memory.
TAB	In the Character mode, the cursor is positioned at the next tab location or the first character location of the next descending line. SPOW latch is reset to a destructive space bar. In the Format mode, the cursor is positioned in the first character location of the next following unprotected field. SPOW is reset. In Program Entry mode, the tab's special character (⌘) is displayed and the cursor moves to the next descending character location in memory.
BACK TAB	In Character mode, the cursor is positioned at the next most previous tab location in the memory or the first character position of the preceding line if no tab locations are present. In Format mode, the cursor is repositioned to the first character location of the current unprotected field or, if already positioned there, to the first character location of the most previous unprotected field. If located in the first character position of the first unprotected field, this command is ignored. In Program Entry mode, this function's code special character (') is displayed in reverse video and the cursor moves to the next descending character location in the memory.
BREAK	When pressed, a 400-millisecond (approx.) one-shot signal is transmitted. This function is not active in the off-line (local) mode.

**Table 2-1. SUPER BEE Computer Terminal Keyboard,
Controls and Indicators (continued)**

KEY OR CONTROL	FUNCTION
CONTROL AND FUNCTION KEY GROUP (continued)	
<p>INS CHAR (Insert Character)</p>	<p>When the terminal is in the Character mode, operation sets the insert character mode latch. A character inserted at the cursor location moves the text one character to the right. The cursor also moves one character position to the right as each character is inserted. If that page edit latch is set, the character that was at the cursor location is moved to the next descending location in the memory and this operation can be repeated to the end of the memory. If in the Line Edit mode, this operation ends on the first line to contain at least two (2) spaces at the end of the line. One space code will exist between all words. Should a NEW LINE code exist in the memory beyond the cursor location, an automatic INS LINE occurs when the NEW LINE code is wrapped around the end of the line. All data appearing below the NEW LINE code is scrolled down one line. Should the data be scrolled down out of the memory, the last character of data is lost for each insert operation.</p> <p>In the Format mode, the character inserted at the cursor location causes the character at that location to be shifted right one location in the unprotected field. All data to the right of the cursor will be shifted one character to the right. Should the unprotected field be full and the cursor location be other than the last character position of the unprotected field, the last character in the field will be lost upon character insertion. If the cursor is in the last character position of the unprotected field when the insertion is made, the cursor will tab to the first character location of the next unprotected field where character insertion will continue.</p> <p>In the Program Entry mode, the code Q is displayed in reverse video and the cursor moves to the next descending character location in the memory.</p>
<p>PAGE EDIT</p>	<p>In the Character mode, resets the page edit latch or press the ESC key followed by the O key. The page edit latch may also be reset by an ESC followed by receipt of O from the I/O.</p>
<p>DEL CHAR (Delete Character)</p>	<p>When the terminal is in the Character mode, the character at the cursor location is deleted and characters on that line to the right of the deletion are shifted left one character. A space code is inserted in the memory's last location on that line, and the cursor does not move. If a line below the cursor location is terminated by a NEW LINE code with the page edit latch set, the memory between the cursor and the new line code shifts left one character location. As the new line code is shifted left until it wraps around to the most previous line, an automatic DEL LINE will occur.</p>

**Table 2-1. SUPER BEE Computer Terminal Keyboard,
Controls and Indicators (continued)**

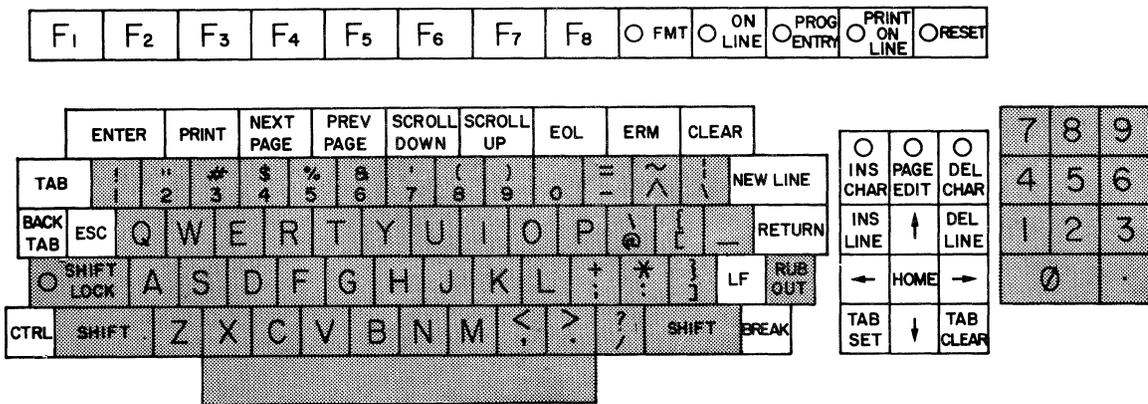
KEY OR CONTROL	FUNCTION
CONTROL AND FUNCTION KEY GROUP (continued)	
<p>DEL CHAR (Delete Character) (cont.)</p>	<p>In the Format mode, as characters are deleted, a space code is inserted in the last location of the current unprotected field. Page Edit is effective only in multi-lined fields, where it operates as explained in Character mode above.</p> <p>In the Program Entry mode, this function's code P is displayed in reverse video and the cursor moves to the next descending character location in the memory.</p>
<p>INS LINE (Insert Line)</p>	<p>When the terminal is in the Character mode, this function causes the line on which the cursor is located to be moved down one line. The NEW LINE code is stored at the first character location of the inserted line, which causes the last character in the memory to be lost.</p> <p>In the Format mode, this function is disabled.</p> <p>In the Program Entry mode, the code L is displayed in reverse video and the cursor moves to the next descending character location in the memory.</p>
<p>DEL LINE (Delete Line)</p>	<p>When the terminal is in the Character mode, this function causes the line on which the cursor is located to be deleted from the memory. Space codes are inserted at the end of the memory to replace all characters of that line. The memory is shifted up one line to fill in where the line has been deleted.</p> <p>In the Format mode, this function is disabled.</p> <p>In the Program Entry mode, the code M is displayed in reverse video and the cursor moves to the next descending character location in the memory.</p>
<p>HOME</p>	<p>When the terminal is in the Character mode, this function repositions the cursor to the first character location of the memory. It does not alter the contents of the memory. The SPOW latch is reset to a destructive space bar.</p> <p>In the Format mode, the cursor is repositioned to the first unprotected location of the memory. The SPOW latch is reset.</p> <p>In the Program Entry mode, code H is displayed in reverse video.</p>
<p>TAB SET</p>	<p>When the terminal is in the Character mode, a tab is set at the cursor character location for all lines in the memory.</p>

**Table 2-1. SUPER BEE Computer Terminal Keyboard,
Controls and Indicators (continued)**

KEY OR CONTROL	FUNCTION
CONTROL AND FUNCTION KEY GROUP (continued)	
TAB SET (cont.)	<p>In the Format mode, tab sets are not recognized.</p> <p>In the Program Entry mode, the code 1 is displayed in reverse video and the cursor moves to the next descending character location in the memory.</p>
TAB CLEAR	<p>When the terminal is in the Character mode, this function clears the tab set located at the cursor character location on all lines of the memory.</p> <p>In the Format mode, TAB CLEARs are not recognized.</p> <p>In the Program Entry mode, the code 2 is displayed in reverse video and the cursor moves to the next descending character location in the memory.</p>
↑ (Cursor Up)	<p>In the Character and Format modes, this command repositions the cursor up one line and remains in the same column as previously located. If the cursor is on the first line, the command is ignored.</p> <p>In the Program Entry mode, the function code A is displayed in reverse video and the cursor moves to the next descending character in the buffer.</p>
↓ (Cursor Down)	<p>In the Character and Format modes, this command repositions the cursor down one line in the same column as previously located. If the cursor is located on the last line of the memory, the command is ignored.</p> <p>In the Program Entry mode, the code B is displayed in reverse video and the cursor moves to the next descending character location in the memory.</p>
→ (Cursor Right)	<p>When the terminal is in the Character and Format modes, the cursor is moved one character location to the right. If the cursor is located in last character position of a line, it is positioned to the first character position of the next descending line. If the cursor is in the last character location in the memory, the command is ignored.</p> <p>In the Program Entry mode, the code C is displayed in reverse video and the cursor moves to the next descending character location in the memory.</p>
← (Cursor Left)	<p>When the terminal is in the Character and Format modes, the cursor is moved one character location to the left. If the cursor is in the first character location of a line, then it is repositioned to the last character position of the preceding line. If the cursor is located in the HOME position, then the command is ignored.</p> <p>In the Program Entry mode, the code D is displayed in reverse video and the cursor moves to the next descending character location in the memory.</p>

Table 2-1. SUPER BEE Computer Terminal Keyboard, Controls and Indicators (continued)

KEY OR CONTROL	FUNCTION
ALPHANUMERIC KEY GROUP	
Alphabetical and Numerical Keys	Generate character codes corresponding to letter, numeral or symbol engraved on key. Keyboard layout is similar to that of standard typewriter, including space bar, shift and shift lock (which is lighted). Keys generate upper and lower case letters, using shift keys.
11-key Numeric Pad	Numerical key group arranged for convenient generation of large numeric entries. Keys perform the same functions as those for numerical keys on alphanumeric keyboard. This group is unaffected by setting of the shift lock key or the lower case inhibit switch.
RUB OUT	<p>When the terminal is in the Character mode, the code is encountered in a block transmit, a Carriage Return-Line Feed function is performed and a CR-LF is transmitted. In the Format mode, the code is stored and displayed as a dot. When the code is encountered in a block transmit, the cursor is positioned at the first character location of the next unprotected field (TAB). A CR-LF is transmitted.</p> <p>In the Program Entry mode, the code is displayed as a dot.</p>

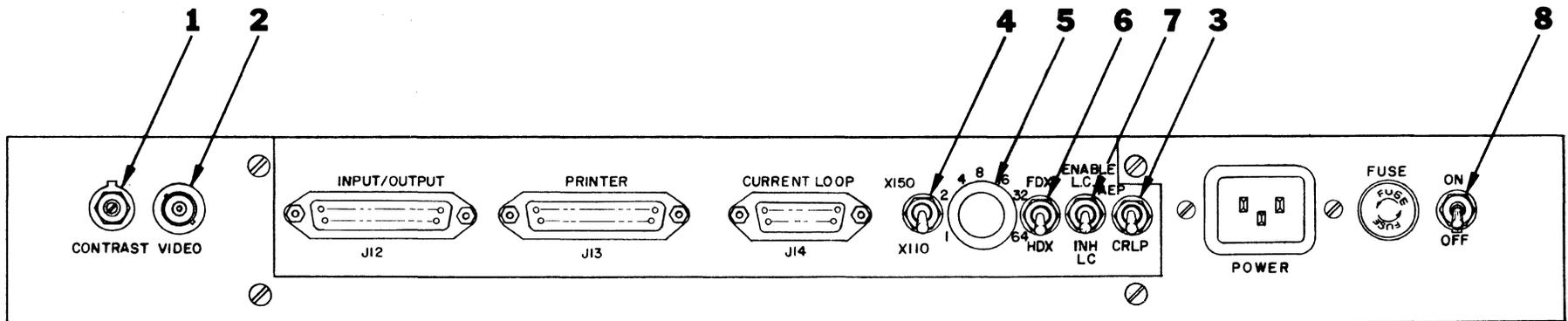


- Control and Function Key Group
- Alphanumeric Key Group

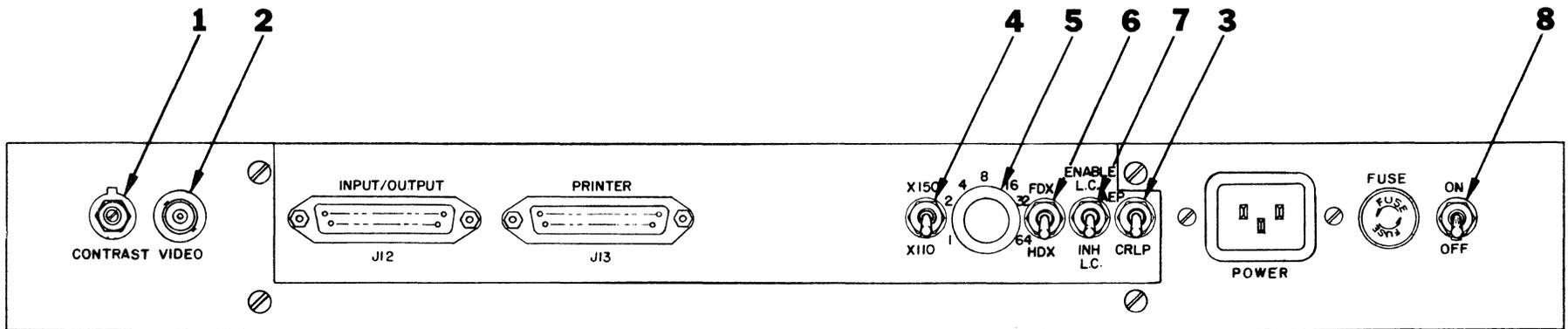
Figure 2-1
Keyboard Controls and Indicators

Table 2-2. Monitor Rear Panel Controls

INDEX No.	CONTROL	FUNCTION
1	CONTRAST	Adjustment that sets contrast level of video on display.
2	VIDEO Output	Outputs composite video signal to remote monitor.
3	AUTO EFF PAGE-CRLF Switch	<p>When set to AUTO EFF PAGE (auto efficient paging), the CR-LF code sequence generates a NEW LINE function.</p> <p>When set to CR-LF, the CR-LF code sequence is performed normally.</p>
4	I/O Baud Rate Multiplier Switch	When set to 150, the selected baud rate is multiplied by 150. When set to 110, the selected baud rate is multiplied by 110.
5	I/O Baud Rate Select Switch	Seven-position selector switch that selects basic rates of 1, 2, 4, 8, 16, 32, and 64. Basic rate is multiplied by either 110 or 150, determined by position of Multiplier Switch.
6	HDX-FDX Switch	Selects half-duplex (HDX) or full-duplex (FDX) operation, in conjunction with the RESET key.
7	INH LC Switch	When set to INH LC (inhibit lower case), the alpha character codes selected from the keyboard are stored in the memory and transmitted out on the I/O as upper case codes. Lower case characters received by the I/O are displayed as lower case. When the switch is set to the Off position (up), the keyboard generates all upper and lower case characters.
8	Power ON-OFF Switch	Applies ac power to terminal.



a. Rear Panel Controls - with Current Loop Adapter



b. Rear Panel Controls

Figure 2-2
Rear Panel Controls

2.3 TURN-ON PROCEDURES

The proper turn-on procedure for the terminal is as follows:

- a. On the monitor rear panel, set the POWER switch to ON. The light in the RESET key should illuminate, indicating power is on. Allow a warm-up period of approximately five minutes.
- b. Adjust the CONTRAST control, located on the lower rear panel, clockwise (CW) to its stop.
- c. Adjust the BRIGHTNESS control knob, located in the upper left area of the keyboard, clockwise (CW) until the raster scan lines barely disappear from the display.
- d. A blinking cursor (underscore) should be visible in the top left corner of the display. Check all indicators to verify that only the RESET indicator is illuminated. Hold the E key down until several E characters are displayed on the monitor. Adjust the contrast control until the characters are sharp and provide the operator with maximum eye comfort.
- e. Depress the CLEAR key to clear displayed data, then perform the operator checkout procedures.

2.4 OPERATOR CHECKOUT PROCEDURES

To test the functional capabilities of the terminal, perform the operator checkout procedures given in paragraphs 2.4.1. through 2.4.7. Before proceeding with the procedures, ensure that the POWER switch is in the ON position, the indicator on the RESET key is illuminated, the screen is clear and the cursor is located at the home position (upper left corner), and that the indicators on the alternate action keys are extinguished.

2.4.1 Alternate Action Keys Checkout

Perform the initial setup as follows:

- a. Set the rear panel HALF DUPLEX/FULL DUPLEX switch to HDX.
- b. Depress the RESET key. The terminal is now set up so that all lighted keys should toggle by manual operation.

Perform the checkout on the action keys listed follows:

PRINT-ON-LINE
PROG ENTRY
ON-LINE
FMT (Cursor moves to end of memory,
indicated by end of memory mark)
INS CHAR
PAGE EDIT
SHIFT LOCK

- a. Depress the key and observe that the indicator lights illuminate.
- b. Depress the key a second time and ensure that the indicator is extinguished. Each key should be left in the off position to prevent confusion while checking operation of the other keys.

2.4.2 ESC Code Sequences Checkout

Before performing the checkout, depress the RESET key followed by the PROG ENTRY key and ensure that the indicator lights. The checkout is performed by depressing the function keys PRINT, TAB SET and TAB CLEAR. The corresponding escape codes (0, 1 and 2) will be displayed in reverse video. If these codes appear on the monitor, the program

entry mode is functioning correctly. The control codes are displayed as their corresponding special symbols (i.e., CR is € and LF is ≡).

2.4.3 Cursor Movement Checkout

Before performing the checkout, depress the RESET key, followed by the CLEAR key. Ensure that the cursor is located in the home position and the display is blank. Perform the checkout as follows:

- a. Depress and hold the Cursor Down (↓) key until the end-of-memory mark (EOM - a block of reverse video) and the cursor are visible on the same line.
- b. Depress and hold the Cursor Right (→) key until cursor movement is inhibited by the EOM mark.
- c. Depress the Cursor Up (↑) key to cause the EOM to move down as the cursor reaches the top line.
- d. Depress and hold Cursor right (→) key. When positioning the cursor right beyond the end of the first line, the cursor moves to the beginning of the next line.
- e. Depress and hold Cursor Left (←) to cause the cursor to wrap back around to the next line above.
- f. Depress the HOME key to move the cursor to the character zero and line zero position.

2.4.4 Tab Checkout

Perform the initial setup as follows:

- a. Depress the RESET key followed by the CLEAR key. This will clear all previously set tab position.

- b. The TAB and BACK TAB should appear, when operated, as a Cursor Down and Cursor Up, respectively.

- c. Set several tabs by positioning the cursor to a character position and pressing the TAB SET followed by a depression of a character key to aid in locating the position where the tab was set.

Perform the checkout as follows:

- a. Operate the TAB key through several lines to assure that the tabs which have been set are effective on each line.
- b. Using the BACK TAB key, move back to the home position, checking to assure that the tabs are set in the same position on all lines, and that the home position may be reached.
- c. Alternately operate the TAB and TAB CLEAR keys until the TAB key performs a Cursor Down and the BACK TAB key performs a Cursor Up at the first character position of each line. This indicates that all tabs have been cleared.

2.4.5 Scrolling And Erase Functions Checkout

Perform the initial setup as follows:

- a. Depress the RESET key followed by the CLEAR key.
- b. Depress the ESC key followed by the lower case e. The screen will fill with DEL codes.

c. Depress the EOL key to erase the DEL codes to the end of the current line.

d. Depress the ERM key to erase all DEL codes to the end of memory.

e. Type "PAGE n", where n is the current page number (i.e., Page 1 for this page).

f. Depress the NEW LINE key until these characters are scrolled up off the top of the display.

g. Repeat steps e and f for pages 2, 3, 4 and 5.

h. Depress the HOME key to position the cursor on the first line of text.

Perform the checkout as follows:

a. Depress and hold the SCROLL UP key to cause the characters to move up the screen and the next page characters will move up into view. Continue to scroll up until the end of memory mark appears on the top line of the display.

b. Depress and hold SCROLL DOWN key until the home position is on the top line of the display.

c. Operate the NEXT PAGE key to move the window in memory down a page at a time until the last page is reached.

d. Operate the PREV PAGE key to move the window in memory up a page at a time until the home position is the first line on the display.

2.4.6 Enter and Print Checkout

Perform the initial setup as follows:

a. Depress the RESET key followed by the CLEAR key.

b. Type a message text consisting of several lines.

c. Depress the following keys in the order given:

ESC

ENTER (Stores an ETX (J) but does not act upon it)

NEW LINE

d. Type another message text consisting of several lines.

Perform the checkout as follows:

a. Depress the ENTER key, the cursor will move to the home position. If back search block transmit strap installed the cursor moves to the first character on the line following any previous ETX. Transmission will begin at the cursor and end with the next ETX. (If pseudopolling has been selected, the cursor will remain at the previously described location, a Request-For-Service code is transmitted, and will wait indefinitely to receive a Clear-To-Transmit code before transmission begins.

b. Depress the RESET key, position the cursor under the last ETX (J).

c. Depress the PRINT-ON-LINE key, followed by the ENTER key. Transmission will proceed at the preselected printer rate. If this is the same as the I/O rate, transmission will not be noticeably different.

d. Connect and test the printer at this time if a printer is to be used with the terminal. Pseudopolling has no meaning to the printer. Transmission in step b is not sent to the printer, but is a copy of data being sent to the I/O port.

e. Position cursor under the last ETX (J).

f. Depress the PRINT key. The cursor will either move to the home position or to the line after the previous ETX, and then transmit the data to the printer.

2.4.7 Format Checkout

Perform the initial setup as follows:

a. Depress the RESET key followed by the CLEAR key.

b. Select the Program Entry mode.

c. Hold down the space bar for several characters.

d. Depress the Cursor Down key (↓) until several capital B's are displayed in reverse video.

e. Repeat steps c. and d. until several lines are displayed on the monitor.

f. Depress RESET key and then depress the FMT key to enter Format mode.

g. Depress the CLEAR key. The cursor should be in the first unprotected position. From this point, data may be entered.

Perform the checkout as follows:

a. Type several characters until the cursor skips over the protected area.

b. Continue to fill in the form until the last character entered causes the cursor to move to the home position.

c. TAB and BACK TAB to the first unprotected location in several fields, to ensure that these functions operate properly in format mode.

2.5 CONTROL AND EDIT FUNCTION OPERATIONS

The control functions may be generated from the Keyboard or by receipt of commands from the I/O port. Table 2-3 provides the sequence of operation for each control function when generated from the keyboard or when received from the I/O port. Figure 2-3 depicts the ASCII codes for each control function of character generated from the keyboard or received from the I/O.

Table 2-3. Control and Edit Function Operations

FUNCTION	OPERATION
RESET	<p>When depressed, resets the terminal's mode of operation to the Character off-line mode. The cursor is moved to the home position. The following functions or modes are reset to the off conditions:</p> <ul style="list-style-type: none"> a. FORMAT b. ON-LINE c. PROG ENTRY d. PRINT ON LINE e. PAGE EDIT f. INSERT CHAR g. Page Blink h. SPOW (Space bar now destructive) <p>The keyboard is enabled and the protect latch is set.</p> <p style="text-align: center;"><u>NOTE</u></p> <p style="text-align: center;">The RESET function does not erase the display screen.</p>
CLEAR	<p>Keyboard operation. Depress CLEAR, or ESC followed by E. I/O port. Receipt of ESC, E.</p>

Table 2-3. Control and Edit Function Operations (Continued)

FUNCTION	OPERATION
HOME	Keyboard operation. Depress HOME, or ESC followed by H.
Cursor Up (↑)	Keyboard operation. Depress Cursor Up (↑), or ESC followed by A. I/O port. Receipt of ESC, A.
Cursor Down (↓)	Keyboard operation. Depress Cursor Down (↓), or ESC followed by B. I/O port. Receipt of ESC, B.
Cursor Right (→)	Keyboard operation. Depress Cursor Right (→), or ESC followed by C. I/O port. Receipt of ESC, C.
Cursor Left (←)	Keyboard operation. Depress Cursor Left (←), or ESC followed by D. I/O port. Receipt of ESC, D.
RETURN	Keyboard operation. Depress RETURN, or CTRL followed by M. I/O port. CTRL and M.
LF (Line Feed)	Keyboard operation, Depress LF, or CTRL followed by J. I/O port. Receipt of CTRL and J.
NEW LINE	Keyboard operation. Depress NEW LINE, or CTRL followed by underscore (—). I/O port. Receipt of CTRL with underscore (—).
TAB	Keyboard operation. Depress TAB, or ESC followed by I. I/O port. Receipt of CTRL and I.
BACK TAB	Keyboard operation. Depress BACK TAB, or ESC followed by reverse slant bar (\\). I/O port. Receipt of ESC with reverse slant bar (\\).
Cursor Address	I/O port only. Receipt of ESC, F sets the terminal ready to receive six decimal digit characters (3 column and 3 line). The cursor is then positioned to any column (000 through 079) and line (000 through 255) in the memory, specified by the six decimal digit address characters. It is possible to overwrite the entire memory with delete codes if the line number is too large for the number of lines stored in memory. The character numbers larger than 79 position the cursor in column 79.
Cursor Sense	When a two character sequence (ESC and a) is received from the I/O, the terminal is conditioned to transmit an eight character code sequence. (ESC,

Table 2-3. Control and Edit Function Operations (Continued)

FUNCTION	OPERATION
Cursor Sense (cont.)	F and three decimal digit column address: (000 through 079) and three decimal digit line address: (000 through 255).
FMT (Format On)	Keyboard operation. Depress FMT, or ESC followed by W. If the light is on when these keys are pressed, the Format off will be performed. (Only from keyboard.) I/O port. Receipt of ESC, W.
ENTER	Keyboard operation. Depress ENTER, or CTRL followed by C. I/O port. Receipt of CTRL, displays ETX symbol only, does not perform ENTER function.
PRINT	Keyboard operation. Depress PRINT, or ESC followed by 0 (zero). I/O port. Receipt of ESC, 0 (zero).
SCROLL UP	Keyboard operation. Depress SCROLL UP, or ESC followed by S. I/O port. Receipt of ESC, S.
SCROLL DOWN	Keyboard operation. Depress SCROLL DOWN, or ESC followed by T. I/O port. Receipt of ESC, T.
NEXT PAGE	Keyboard operation. Depress NEXT PAGE, or ESC followed by U. I/O port. Receipt of ESC, U.
PREV PAGE (Previous Page)	Keyboard operation. Depress PREV PAGE, or ESC followed by V. I/O port. Receipt of ESC, V.
EOL (Erase to End of Line)	Keyboard operation. Depress EOL, or ESC followed by K. I/O port. Receipt of ESC, K.
ERM (Erase to End of Memory)	Keyboard operation. Sequentially depress ERM, or ESC followed by J. I/O port. Receipt of ESC, J.
RUB OUT	Keyboard operation. Depress RUB OUT. I/O port. Code received by I/O.
INS CHAR (Insert Character)	Keyboard operation. For on condition, depress INS CHAR, or ESC followed by Q. For off condition, depress INS CHAR, or ESC followed by R. (These keys toggle the condition.) I/O port. Receipt of ESC, Q for on condition, and receipt of ESC R for off condition.

Table 2-3. Control and Edit Function Operations (continued)

FUNCTION	OPERATION
DEL CHAR (Delete Character)	Keyboard operation. Depress DEL CHAR, or ESC followed by P. I/O port. Receipt of ESC, P.
PAGE EDIT	Keyboard operation. Depress PAGE EDIT, or ESC followed by N. If on when keys are pressed, light condition toggles. If on when ESC, O is pressed, light condition turns off. I/O port. Receipt of ESC, N. Receipt of a second ESC, N will not toggle condition off. Receipt of ESC, O will turn condition off.
INS LINE (Insert Line)	Keyboard operation. Depress INS LINE, or ESC followed by L. I/O port. Receipt of ESC, L.
DEL LINE (Delete Line)	Keyboard operation. Depress DEL LINE, or ESC followed by M. I/O port. Receipt of ESC, M.
TAB SET	Keyboard operation. Depress TAB SET, or ESC followed by 1. I/O port. Receipt of ESC, 1.
TAB CLEAR	Keyboard operation. Depress TAB CLEAR, or ESC followed by 2. I/O port. Receipt of ESC, 2.
FMT (Format)	Keyboard operation. For the off condition, depress FMT, or ESC followed by X. For the on condition, FMT or ESC followed by W toggles the condition. I/O port. Receipt of ESC, X.
PROG ENTRY (Program Entry)	Keyboard operation. For the on condition, depress PROG ENTRY, or ESC followed by Y. For the off condition, depress PROG ENTRY. (The keys will toggle the condition.) I/O port. For the on condition, receipt of ESC, Y. For the off condition, receipt of ESC, Z.
PRINT ON LINE	<u>NOTE</u>
	In the off condition, the code Z is stored in reverse video.
	Keyboard operation. For the on condition, depress PRINT ON LINE, or ESC followed by f. (These keys will toggle the condition.) For the off condition, depress PRINT ON LINE, or ESC followed by g. I/O port. For the on condition, receipt of ESC, f. For the off condition, receipt of ESC, g.

BIT 7 6 5 4 3 2 1	CONTROL CHARACTERS		DISPLAYABLE CHARACTER						ESCAPE SEQUENCE					
	000	001	010	011	100	101	110	111	010	011	100	101	110	111
0000	NUL ␣	DLE ␣	SP	0	@	P	\	P		PRINT ␣		CHAR DEL P	BACK TAB I	F 1 P
0001	SOH ␣	DC1 ENTER ␣	!	1	A	Q	a	q		TAB SET I	↑ A	CHAR INS ON O	CURS SENSE a	F 2 q
0010	STX ␣	DC2 ␣	//	2	B	R	b	r		TAB CLR 2	↓ B	CHAR INS OFF R	KEYBOARD ENABLE D	F 3 r
0011	ETX ␣	DC3 ␣	#	3	C	S	c	s			→ C	SCROLL UP S	KEYBOARD DISABLE C	F 4 s
0100	EOT ␣	DC4 ␣	\$	4	D	T	d	t			← D	SCROLL DOWN T	* d	F 5 t
0101	ENQ ␣	NAK ✓	%	5	E	U	e	u			CLEAR E	NEXT PAGE U	EOS DEL e	F 6 u
0110	ACK OFF LINE ✓	SYN ␣	&	6	F	V	f	v			CURS ADDR F	PREV PAGE V	PRINTER ON LINE f	F 7 v
0111	BEL ␣	ETB (XMIT) ␣	/	7	G	W	g	w				FORMAT ON W	PRINTER OFF LINE g	F 8 w
1000	BS ␣	CAN ␣	(8	H	X	h	x			HOME H	FORMAT OFF X	h	x
1001	HT ␣	EM ␣)	9	I	Y	i	y				PROG ENTRY ON Y	i	y
1010	LF ␣	SUB ␣	*	:	J	Z	j	z			ERM J	PROG ENTRY OFF Z	ON LINE j	z
1011	VT ␣	ESC ␣	+	:	K	[k	{			EOL K	END Protect I	OFF LINE k	{
1100	FF ␣	FS ␣	,	<	L	\	l				LINE INS L			:
1101	CR ␣	GS ␣	-	=	M]	m	}			LINE DEL M	Start Protect I	m	}
1110	SO ␣	RS ␣	.	>	N	^	n	~			PAGE EDIT ON N		n	~
1111	SI ␣	US NEW LINE ␣	/	?	O	-	o	DEL L			PAGE EDIT OFF O	Video Control _	o	DEL L

Note: 1. Shaded Area is applicable to Super Bee only. Unshaded area is applicable to Super Bee and Mini Bee.
 2. Lower case code will display upper case characters on Mini Bee.

Figure 2-3. ASCII Code Chart

2.6 OPERATION CODES

The SUPER BEE code structure consists of 32 ASCII control codes, 96 ASCII alphanumeric characters, and 96 escape sequence control codes. A switch is provided on the rear of the terminal so that all lower-case alphabetic characters are translated into their upper case equivalents.

The operation codes provide the necessary functions that are not defined in the control and edit group functions. These functions may be generated from the keyboard, received at the I/O port, or may be internally generated by present circuitry. Table 2-4 lists the codes and describes their functions.

Table 2-4. Operation Codes

CODE	OPERATION
ETX-CONTROL C (003)	When this code is recognized from the keyboard or I/O, the code is stored and displayed at the cursor's location and marks the end of a block in the memory. The ENTER function is initiated when entered from the keyboard.
ACK-CONTROL E (006)	This code, when recognized from the Keyboard or I/O, sets the terminal to LOCAL, disables the I/O data transmitter/receiver, and enables the keyboard. When a block of data is ended while terminal is in Synchronous mode and is to remain on-line the following codes can be used: <u>Cursor Sense</u> : will start a sync search after sending out the cursor address until the CPU sends out a new block of data. <u>Print</u> : without go-off-line, will reply with four sync codes and go into sync search.
BELL-CONTROL G (007)	When this code is recognized, an audible alarm is generated. The audible alarm is also generated when the 72nd character is entered in the line from the Keyboard, but is not generated from the I/O at the 72nd character location.
BACK SPACE CONTROL H (010)	When this code is recognized from the Keyboard and I/O, the cursor is moved back one character location in the memory. The command is ignored if the cursor is located at the first position of the memory. The contents of the memory are unchanged.
DCI-CONTROL Q (021)	This code is sent to the I/O in the pseudopolling mode to indicate a request for service.
SYN-CONTROL V (026)	Four SYN codes precede all synchronous transmissions and at least two SYN codes are required to establish synchronization on the receiver.
ETB-CONTROL W (027)	When this code is received from the I/O, a block transmit is initiated.

Table 2-4. Operation Codes (Continued)

CODE	OPERATION
<p>ESC-CONTROL [</p> <p>ESC-b (Keyboard Enable)</p> <p>ESC-c (Keyboard Disable)</p> <p>ESC-[(End Protect)</p> <p>ESC-] (Start Protect)</p> <p>ESC-e (EOS Delete)</p> <p>ESC- (underscore)</p>	<p>This is the initial code in an escape sequence control function.</p> <p>This two code sequence from the I/O enables the keyboard.</p> <p>This two character code sequence disables the Keyboard from generating any characters or control functions except the RESET function. The keyboard may subsequently be enabled normally by the RESET key or from the I/O by an ESC and b.</p> <p>When this two-code sequence is recognized from the Keyboard or I/O, it resets the protect latch and inserts an 0 in the eight bit position of each character stored in the memory after the reset. In Format mode, the 0 in the eighth bit indicates an unprotected character location in the memory. In the Program Entry mode, the characters in the unprotected locations are displayed as reverse video characters.</p> <p>When this two-code sequence is recognized from the Keyboard or I/O, it sets the protect latch and a 1 is inserted in the eighth bit position of each character stored in the memory after it is set. In the format mode, the 1 in the eighth bit indicates a protected character location in the memory.</p> <p>When this two-code sequence is recognized from the Keyboard or I/O, all the characters in the memory from the cursor's location to the end of memory are replaced with delete codes in a Character mode. In the Format mode all the unprotected characters in the memory from the cursor's location to the end of memory are replaced with delete codes. In the Program Entry mode, the code e is displayed in reverse video and the function is not performed.</p> <p>When this two-character code sequence is recognized from the Keyboard or I/O, the terminal is ready to receive one of the following video control characters:</p> <ul style="list-style-type: none"> space - video reset Ø - video blink 1 - video reverse 2 - video blink reverse 3 - video line reset <p>In the Character mode or Format mode, all special video functions are terminated by the end-of-line or a new line code and its special symbol is displayed. In the Program Entry mode, the function is not performed.</p>

Table 2-4. Operation Codes (continued)

CODE	OPERATION
Video Reset	Replaces all the blink function codes in the memory with protected or un-protected space codes and sets the eighth bit of each code depending upon the state of the protect latch.
Video Line Reset	Code is stored in the memory at the cursor's location and restores to the normal video the memory's characters from that location to the end of the line.
Video Blink	Code is stored in the memory at the cursor's location and starts blinking the remaining characters in that line when in the Character mode or Format mode.
Video Reverse	Code is stored in the memory at the cursor's location, then the next character and following characters to the end of the line are displayed in reverse video when in Character mode or Format mode.
Video Blink Reverse	Code is stored in the memory at the cursor's location, then the next character and following characters to the end of the line are displayed in blinking reverse video when in Character mode or Format mode.
BREAK	When this key is depressed, a 400 millisecond (approx.) one-shot spacing signal is transmitted. This function is not active in the local mode.
CTRL (Control)	When this is depressed together with any alpha key, it changes the code structure of that key by forcing the seventh bit to "o." This allows operation of the control codes assigned to column one and two of the ASCII Code Chart.
SPOW Latch	<p>Set by the RETURN function and reset by the following functions:</p> <p style="margin-left: 40px;">LINE FEED NEW LINE TAB HOME</p>

2-7 TIMING CONSIDERATION

Certain SUPER BEE functions require longer than one character time at high transmission rates. The number of field characters required to fill these intervals are given in Table 2-5. Although any character may be used, the

NULL character (000 Octal) is suggested since this code will be completely ignored and will not affect the AUTO-NEW LINE feature of the terminal, i.e., the CR and LF may be separated by NULL codes and the N/L code will still be stored at the position where the CR was performed.

TABLE 2-5
TIMING CONSIDERATIONS

FUNCTION	TIME REQ'D MICRO SECONDS	LOW RATES	FIELD CHARACTER REQUIRED			
			4800 ASYNC	4800 SYNC	9600 ASYNC	9600 SYNC
ERM Delete (ESC and e)	2500	0	1	1	3	3
ERM (ESC and J)	2500	0	1	1	3	3
Insert Line (ESC and L)	2500	0	1	1	3	3
Delete Line (ESC and M)	100 ms	*	48	60	96	120
Delete Char (ESC and P)	2500	0	1	1	3	3
Scroll Up (ESC and S)	1000	0	0	0	0	1
Scroll Down (ESC and T)	1000	0	0	0	0	1
Next Page (ESC and U)	20 ms	*	10	12	20	24
Prev Page (ESC and V)	5ms	*	2	3	5	6
Back Tab (ESC and I)	10 ms	*	5	6	10	12
Clear (ESC and E)	2500	0	1	1	3	3

* Calculate for each baud rate as required

Repetitive usage of the same code should be avoided if another method can be determined. Cursor addressing is preferable to multiple cursor or page movements.

SECTION III INSTALLATION

3-1 INTRODUCTION

This section contains information on unpacking, receiving inspection, connection of the communications interface, physical placement of the terminal and preliminary selection of functional control settings for the specific requirements of a given user.

3-2 UNPACKING

The SUPER BEE Computer Terminal is ready for operation after removal from its shipping container. There are no tiedowns or packing materials inside the unit that need to be removed. Store the carton for future use. The Keyboard interconnection cable is stowed in the rear at the Keyboard housing during shipping.

3.3 INSPECTION FOR IN-SHIPMENT DAMAGE.

The SUPER BEE is inspected and tested prior to shipment from the factory. Upon receipt carefully remove all components from the shipping container and check each item against the packing slip to ensure completeness of your order. Visually inspect all items for any possible shipping damage. All shipping containers have been custom engineered to protect their contents. Special care has been taken to prevent damage under normal shipping conditions; therefore, damage to contents should not occur unless the package has been mishandled. Mishandling will be evident upon inspection of the shipping container. If damage is found after visual inspection, take care not to destroy the evidence. If necessary, take pictures of the damaged container. If damage is noted, please contact the Transport Carrier as soon as possible.

3.4 STANDARD ITEMS (FURNISHED)

Standard items furnished with each SUPER BEE Terminal are as follows:

- a. CRT Monitor
- b. Detachable Keyboard w/cable
- c. Power cord
- d. Operator's Manual

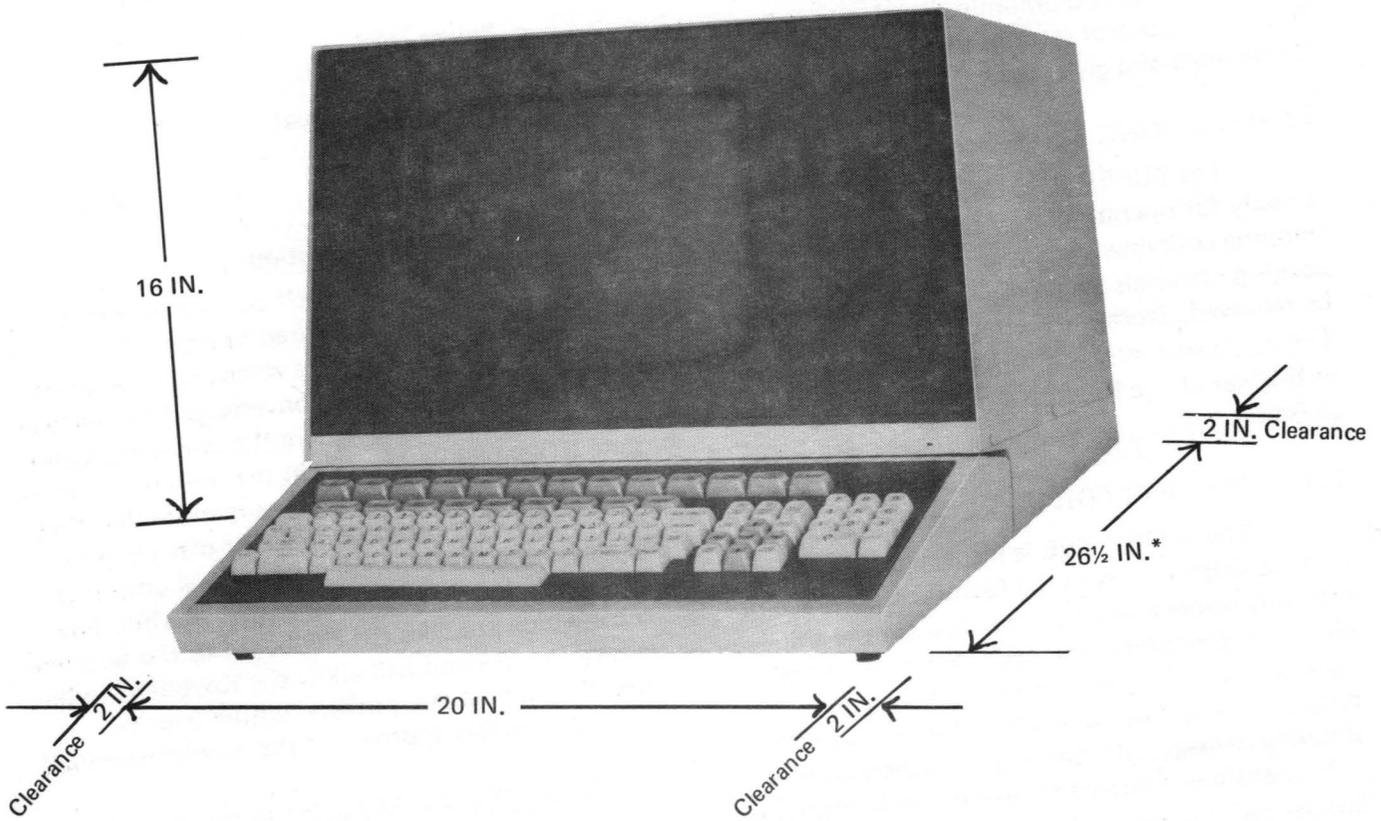
3.5 INSTALLATION

3.5.1 Placement for Operation

The SUPER BEE is self-contained and can easily be moved and relocated to alternate operating positions without removing or altering any hard wiring. Select a convenient, level surface and place the terminal where the power cord and data I/O cables will not be in the way of the operator. Route the cables in such a manner that they will not be inadvertently pulled or disturbed by nearby personnel. Rotate the terminal until it is conveniently oriented for operator viewing. The cable which attaches the Keyboard to the terminal is very flexible and will allow the Keyboard to be placed in almost any position within four feet (122 centimeters approx.) of the viewed terminal.

CAUTION: Avoid placing terminal on long plush carpet or soft spongy material where base may come in contact with mounting surface, thereby shutting off or impeding air circulation.

The CRT Monitor is provided with an internal muffin whisper fan. Air is drawn in through a perforated bottom panel and exhausted out through slots in the rear of the monitor housing. It is important, therefore, that the CRT Monitor never be placed in a position where free air circulation is restricted. To maintain efficient air circulation, maintain at least 2 inches (51 millimeters) of clearance at the rear and sides of the Monitor (see Figure 3-1). As noted above, don't place the Monitor on long, plush carpet or



*Without Keyboard 17¼ inches

Figure 3-1
SUPER BEE Mounting Requirements

spongy material where the base plate might come in contact with the mounting surface and restrict the air circulation. Never allow paper or other material to be stored under the terminal where it may cover fan screen and restrict air flow . Care must be used to ensure that the fan screen does not become bent and interfere with the fan.

3.5.2 Power Connection

The International Electrotechnical Commission (IEC) recommends that instrument panels and cabinets be grounded to protect operating and servicing personnel. The SUPER BEE is shipped with a shielded three-conductor power cord which, when plugged into an

appropriate outlet, grounds the instrument through the offset pin. To operate the SUPER BEE from a two-contact outlet, use a three-conductor to two-conductor adapter. Preserve the safety feature by grounding the adapter pigtail lead.

3.5.3 Data Interface Connections

All data source interconnections are made via the rear panel Input/Output connector (refer to Figure 2-2). The Input/Output connector mates with ITT Cannon solder pin connector (part no. DM-25P). Data source pin connections are listed in Table 3-1 and defined in the following paragraphs.

TABLE 3-1 DATA SOURCE INTERFACE CONNECTIONS

PIN NO.	FUNCTION	RS232 CIRCUIT
1	Frame Ground	AA
2	Transmitted Data	BA
3	Received Data	BB
4	Request to Send	CA
5	Clear to Send	CB
7	Signal Ground	AB
8	Received Line Signal Detector	CF
15	Terminal Signal Element	DB
16	Output Clock (TTL Level)	*
17	Receiver Signal Element	DD
20	Data Terminal Ready	CD
24	Output Clock (RS232C)	

* Not RS232 (Optional – 1X thru 16X Data Output Clock, strap selectable, not present unless strapped.)

CAUTION

If the terminal is to be operated in conjunction with a data phone or data modem, special care should be taken to ensure that the interfaces are per EIA Specification RS232C. The logic levels called out in this specification may cause serious damage to communication interfaces designed strictly for standard DTL or TTL integrated circuit logic levels. The same precaution should be made when connecting hard wire to any communications I/O.

Frame Ground (AA)

This conductor, where used, is electrically bonded to the machine frame.

Transmitted Data (BA)

This circuit transfers data from the terminal to the data set for transmission to the external device. The terminal holds circuit BA in the mark condition during any-time interval between characters or words, or when no signals are to be transmitted.

Received Data (BB)

This circuit transfers data from the data set to the terminal. Signals on this circuit are generated by the data set in response to data signals received from the external device. The data set holds this line in the mark condition when the line is idle or the carrier is not detected.

Request To Send (CA)

Signals on this circuit are generated by the terminal to condition the local data set to transmit. The "on" condition is maintained whenever the terminal has information ready for transmission or being transmitted. The terminal transmits data on circuit BA (Transmitted Data) only when the "on" condition is maintained on circuits CA, CB and CD. In half-duplex service, the "off"

conditions holds data set in the Receive Data condition, and the "on" condition holds the data set in the Transmit Data condition.

Clear To send (CB)

Signals on this circuit are generated by the data set to indicate that it is prepared to transmit data. The "on" condition on circuit CA (Request to Send) is delayed as long as may be required to establish a connection to a external device. When circuit CA is turned off, circuit CB is also turned off.

Signal Ground (AB)

This conductor established the common ground reference for all interface lines.

Terminal Ready (CD)

Terminal Ready is high whenever power is on.

Received Line Signal Detector (CF)

The signal on this line indicates that the data set has established the carrier and the data set is about to input data to the terminal.

Transmitter Signal Element Timing (DB)

Signals on this circuit are used to provide the data terminal with signal transmit element timing information.

Receiver Signal Element Timing (DD)

Signals on this circuit are used to provide the data terminal with received signal element timing information.

3.5.4 Printer Interface Connections

Printer interface connections are listed in Table 3-2.

Table 3-2. Printer Interface Connections

PIN NO.	FUNCTION
1	Frame Ground
3	Data to Printer
7	Signal Ground
20	Printer Ready
25	Printer Status

3.5.5 Current Loop Adapter

An optional 15-pin connector is provided on the back panel of the terminal to provide for the current loop adapter. The adapter will make the terminal compatible with two basic interface modes. A modified TTY interface for some mini computers features an open collector output and photoisolated input and should be within 50 ft. of the terminal. A single or balanced current loop interface can be used up to 2000 ft. away, and with a twisted, shielded, two-pair cable and a slower baud rate, it may be useable up to 6,000 ft. away.

3.5.6 Video Output Connection

This is a BNC connector to drive a remote monitor located up to 1,000 feet (304 meters) from the SUPER BEE Terminal using 50-ohm coaxial cable (RG-58/V).

3.5.7 I/O Processor Board Strapping

The eight strapable options available on the SUPER BEE I/O Processor Board (Refer to Section 1.3.11) are implemented by installing the appropriate jumper on the 16-pin strapping pad (S1) located on the I/O Processor Board. A summary of these strapping selections is provided in the following paragraphs. Figure 3-2 illustrates the strapping locations.

Send Control Codes (PIN 1 AND 16)

With no strap installed, all escape codes will be performed and transmitted. With this strap installed, all escape sequences are performed locally only ~~but~~ transmitted.

Go-Off-Line (PINS 2 and 15)

With no strap installed, an ETX is transmitted at the end of a block transmit and the on-line mode is maintained. With this strap installed, the unit goes off-line at the end of transmission and no ETX is transmitted.

Store Special Functions (PINS 3 and 14)

With no strap installed, special function codes are transmitted. With this strap installed, special functions are stored only and not transmitted.

External Clock (PINS 4 and 13)

With no strap installed, SUPER BEE uses its own internal clock. With this strap installed, it provides for the use of external clocks supplied by a modem or other interface.

Synchronous or Asynchronous Operation (PINS 5 and 12)

With no strap installed, the SUPER BEE is configured to operate asynchronously. When operating in the synchronous mode, the generated word is eight bits. However, while operating in an asynchronous mode, the length of the generated word is determined by the multiplier toggle switch position. In the 110 position, an 11-bit word is generated. A 10-bit word is generated in the 150 position.

Back Search Block Transmit (PINS 6 and 11)

With no strap installed, SUPER BEE is configured to do a block transmission from the first character in in the text. With a strap installed, SUPER BEE is configured to perform a back search to any previous ETX and start to transmit from that character to the next ETX. This strap is installed as shipped from the factory.

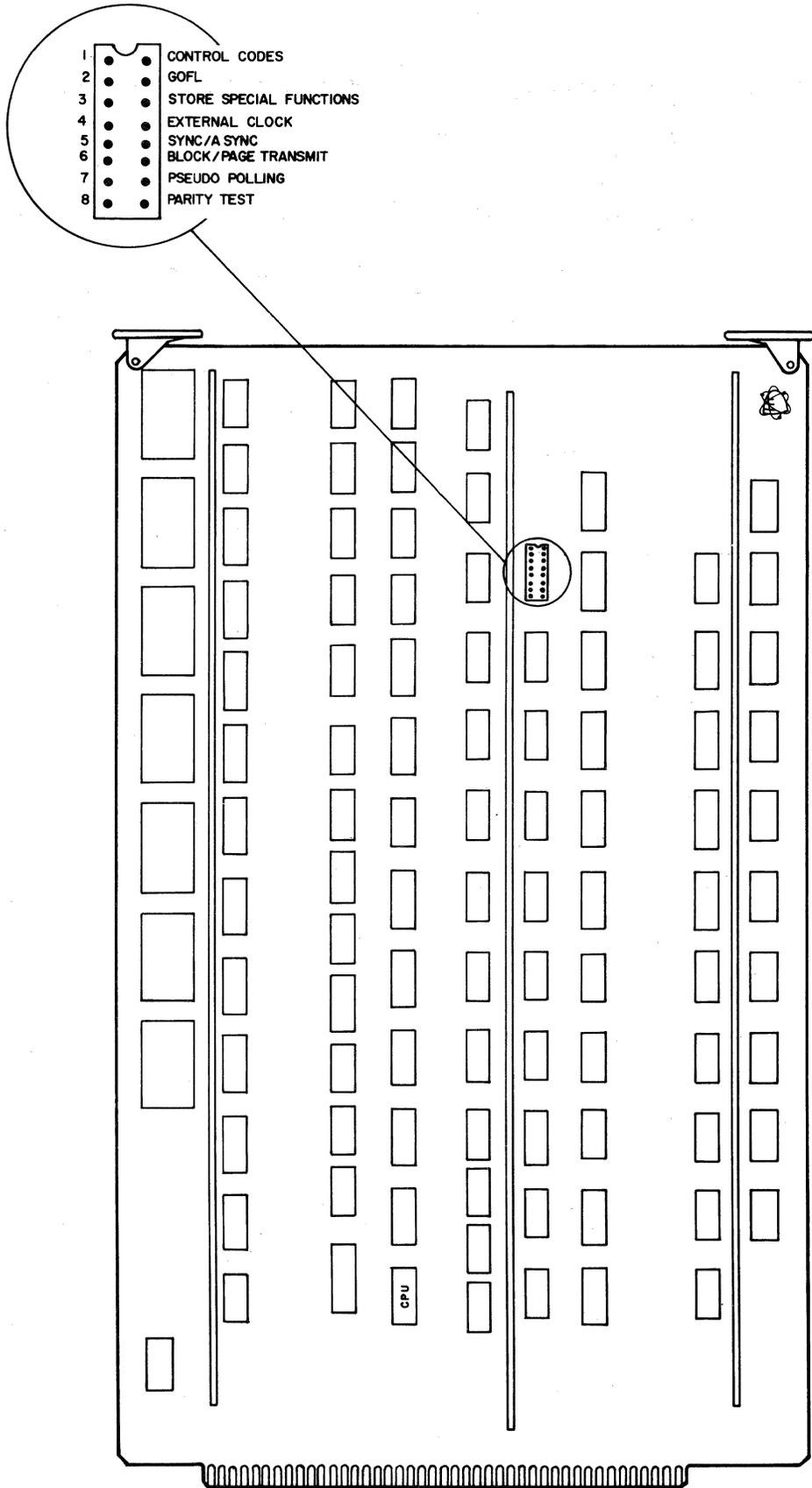


Figure 3-2
I/O Processor Board Strapping Locations

Pseudopolling/Immediate Block Transmit (PINS 7 and 10)

With no strap installed, SUPER BEE will do an immediate block transmit if "Clear-to-Send" is true (if so strapped on pin 6 to 11 block/page transmit). If strap is installed, SUPER BEE waits for an ETB (Control W) before transmitting.

Parity Test (PINS 8 and 9)

With no strap installed, SUPER BEE checks incoming data for even parity when operating asynchronously and odd parity when operating synchronously. If an invalid character is sensed during parity check, the character is replaced on the display by a parity error symbol (reverse video backward question mark). With this strap installed, no parity check is made. Transmitted data is in the same sense as received data, with the exception that data is transmitted with a mark parity bit with strap installed.

3.5.8 Printer Baud Rate and TTL Transmit Clock Strapping

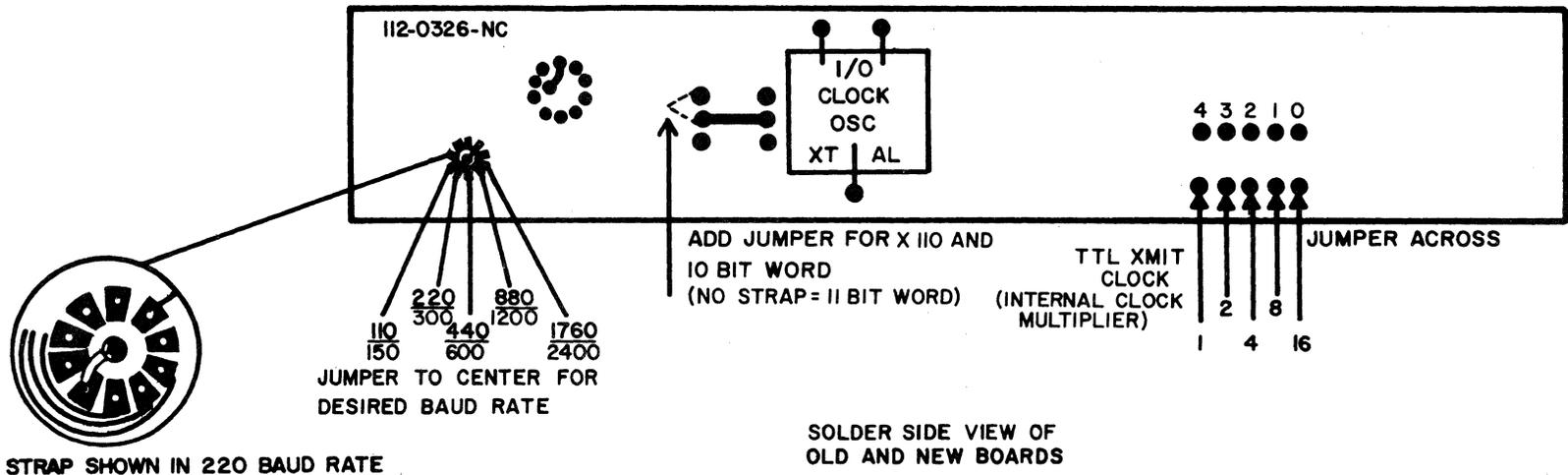
The switch board of the Interface assembly includes the components and strapping to deter-

mine and produce the TTL transmit clock, 10-or-11-bit word, baud rate multiplier and baud rate for the printer port only (see Figure 3-3).

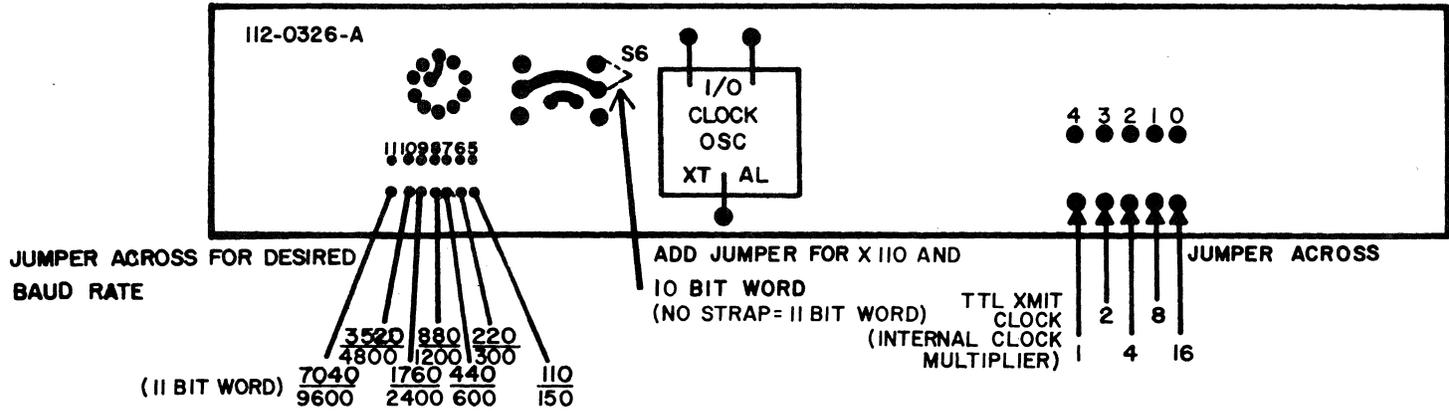
The printer TTL logic level, if unstrapped, is not present. If desired, selection of a TTL transmit clock can be made by strapping one of five pins to produce one to 16 times the internal clock baud rate. (1, 2, 3, 8 or 16).

The printer RS-232 level baud rate is determined by strapping one of the pins on the switch board. A baud rate of 1, 2, 4, 8, 16, 32 or 64 can be selected by strapping the appropriate pins.

The determination of 10-or-11-bit word structure is made by strapping the appropriate connector pins. If no strp is added, the printer port will output 11-bit words. With a strap added, the output will be a 10-bit word. This strapping feature also provides the baud rate multiplication. With no strapping (11-bit word) multiplies the baud rate by 150. By strapping (10-bit word), it multiplies the rate by 110. The baud rate can vary, therefore, from 110 to 9600 baud.



SOLDER SIDE VIEW OF OLD AND NEW BOARDS



THE BULK OF NON RELATED CIRCUITY HAS BEEN OMITTED FROM THESE DRAWINGS, ONLY THAT ARE NEEDED TO IDENTIFY LOCATION REMAIN.

Figure 3-3
Printer Baud Rate and Internal
Clock Multiplier Strapping

SECTION IV THEORY OF OPERATION

4.1 INTRODUCTION

This section contains the theory of operation for the SUPER BEE Computer Terminal. The section is presented as a functional description at a basic and an intermediate block diagram level, and at a detailed description level referencing appropriate logic diagrams.

4.2 GENERAL FUNCTIONAL DESCRIPTION

The SUPER BEE consists of seven major functional components; Power Supply, Keyboard, Monitor, Display Board, Input/Output (I/O) Processor Board, Interconnect Board and Interface Assembly. Figure 4-1 shows the physical location of the major components (Keyboard not shown). These functions are depicted in Figure 4-2 and described briefly in the following paragraphs.

4.2.1 Interconnect Board

The Interconnect Board provides a means of logically interconnecting the terminal's sub-assemblies. This board serves as the point of distribution for power, and directs the interchange of signals between the subassemblies.

4.2.2 Power Supply

The Power Supply provides the required regulated dc voltage to the terminal. This sub-assembly can be modified to operate on 230 Vac power where required.

4.2.3 Keyboard

The Keyboard is the manual input device used by the operator to communicate with the terminal. The Keyboard is similar to a standard teletype, but has been expanded to facilitate the expanded capabilities of the SUPER BEE.

4.2.4 I/O Processor Board

The I/O Processor Board contains the micro-processor, control program memory, transmit and

receive logic, various mode controls and logic for accepting keyboard information. Appropriate data and controls are transferred to the Display Board.

4.2.5 Display Board

The Display Board generates basic timing for the terminal and controls all logic required for generation, control and storage of video information.

4.2.6 Monitor

The Monitor consists of a 12-inch television-type CRT screen and its supporting circuitry. It displays the data developed on the Display Board.

4.2.7 Interface Assembly

The Interface Assembly interfaces the I/O Processor Board with an external data source and a Printer. It also generates certain control signals used to facilitate these input/output operations. An optional current loop adapter is included where required.

4.3 INTERMEDIATE FUNCTIONAL DESCRIPTION

The subassembly components of the SUPER BEE are functionally interdependent. Therefore, the isolation of various functions to the responsible sub-assembly is difficult. The following paragraphs describe in part, some of the functions of each subassembly (refer to Figure 4-3).

4.3.1 Interconnect Board

The Interconnect Board logically connects the Keyboard, Monitor, I/O Processor Board, Display Board, and Interface Assembly with each other (see Figure 4-4). It distributes dc power (+5, +15, -12) from the Power Supply to each of these assemblies. The -5V and -9V are generated on the Interconnect Board and sent to the Display and I/O Boards respectively. The Interconnect Board contains the "Bell" speaker and the Elapsed Time Indicator (opt). It also provides circuitry for "Remote Video".

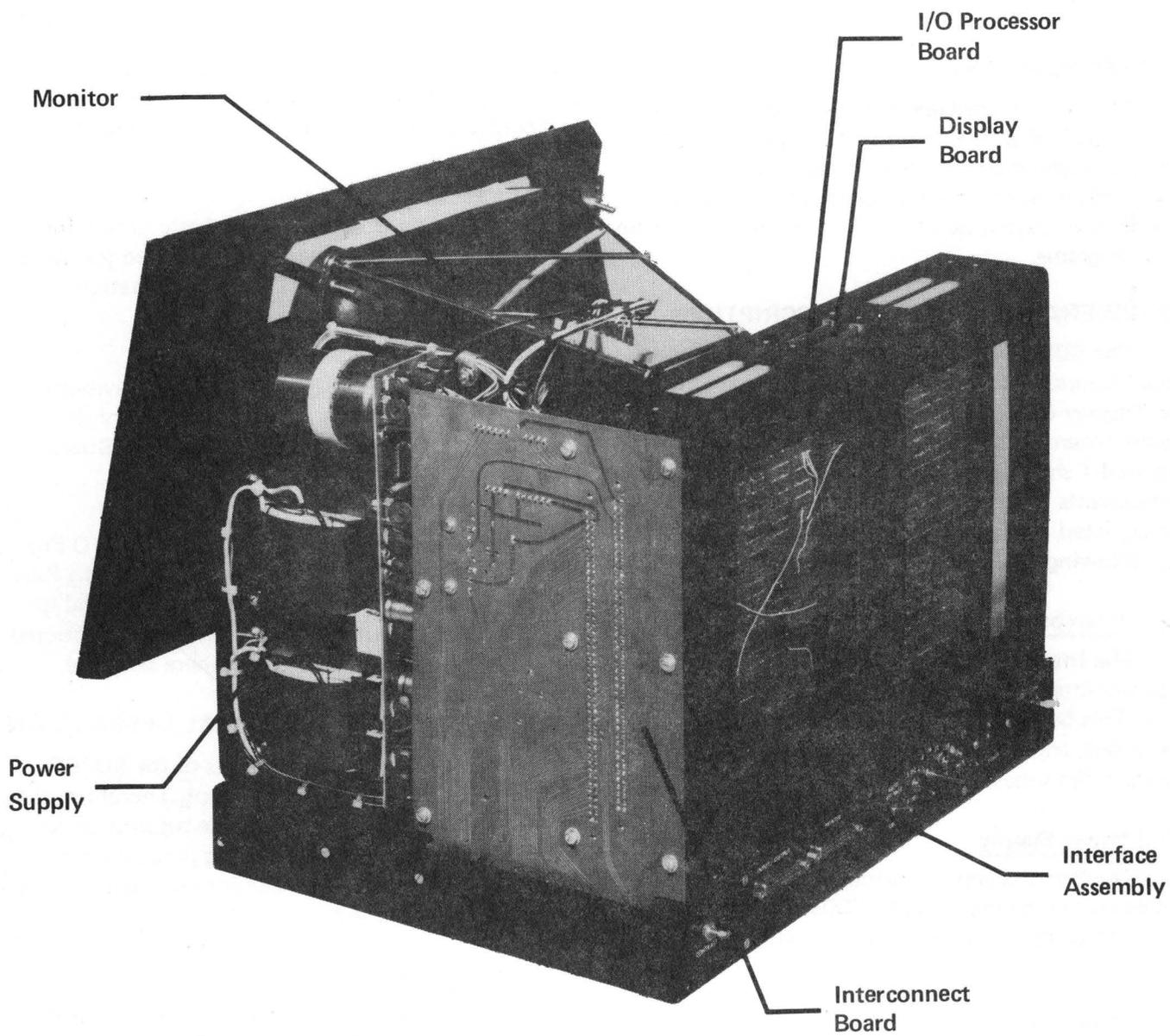


Figure 4-1
SUPER BEE Major Components

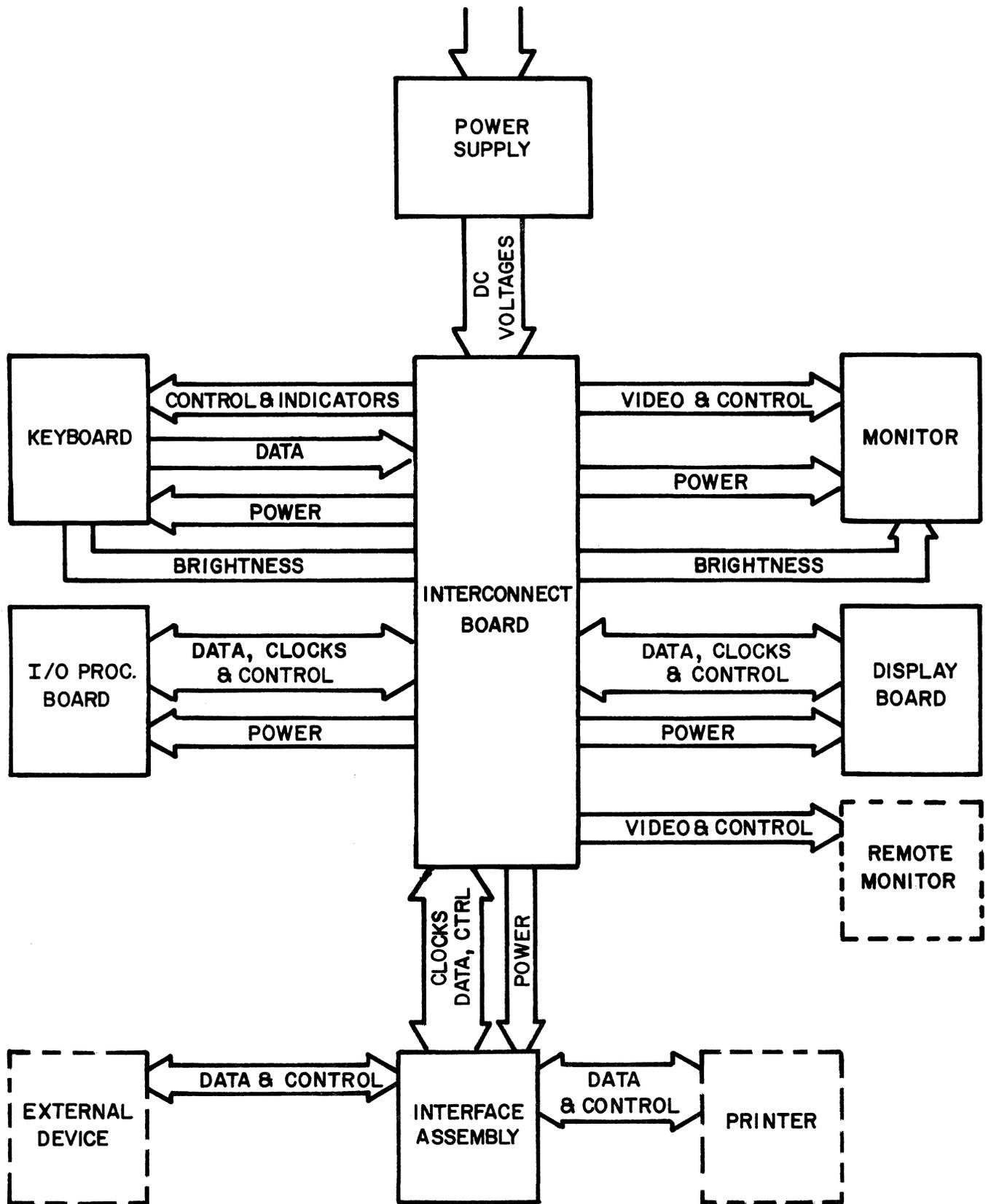


Figure 4-2
Basic Block Diagram

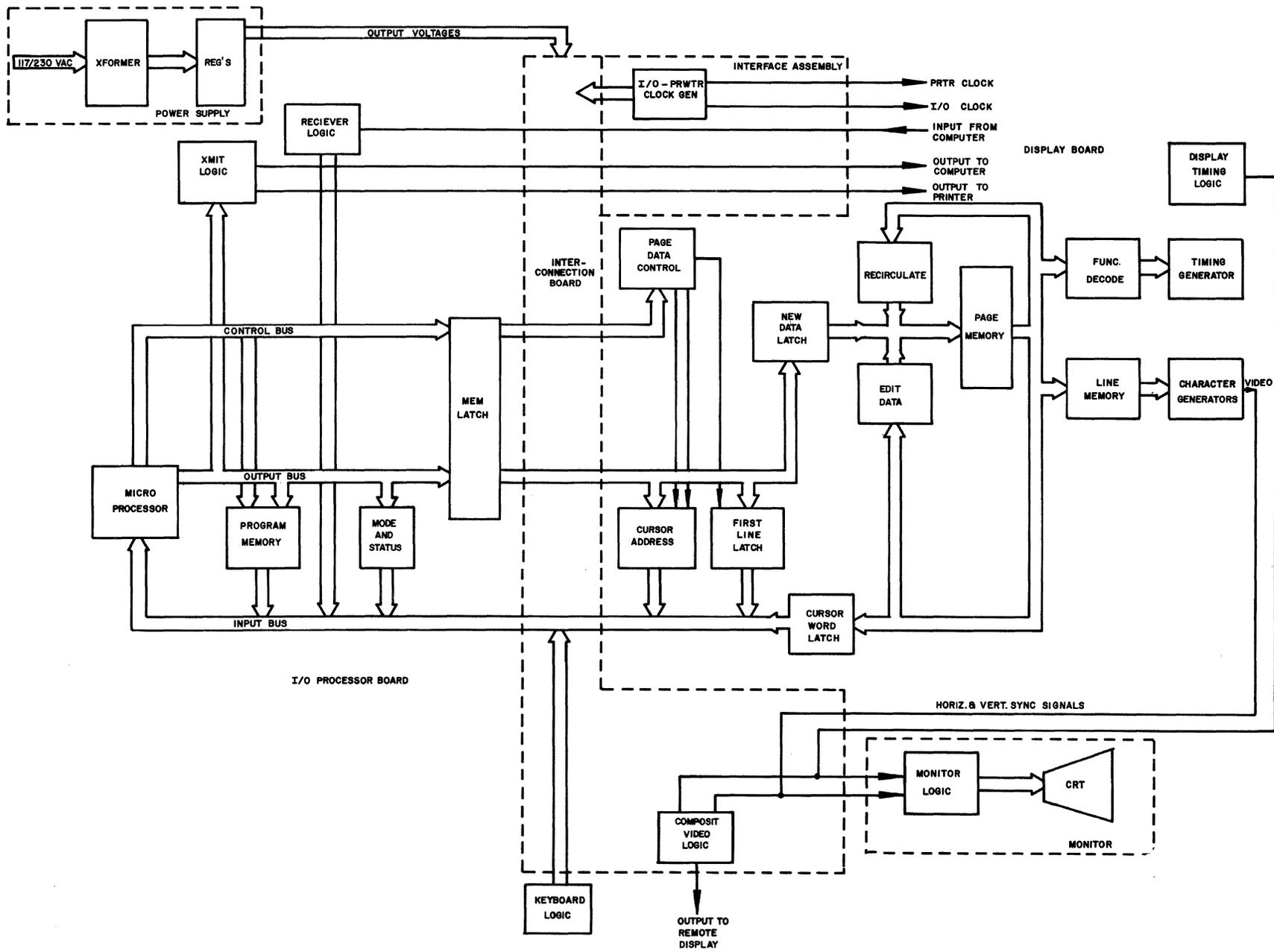


Figure 4-3
Intermediate Functional Block Diagram

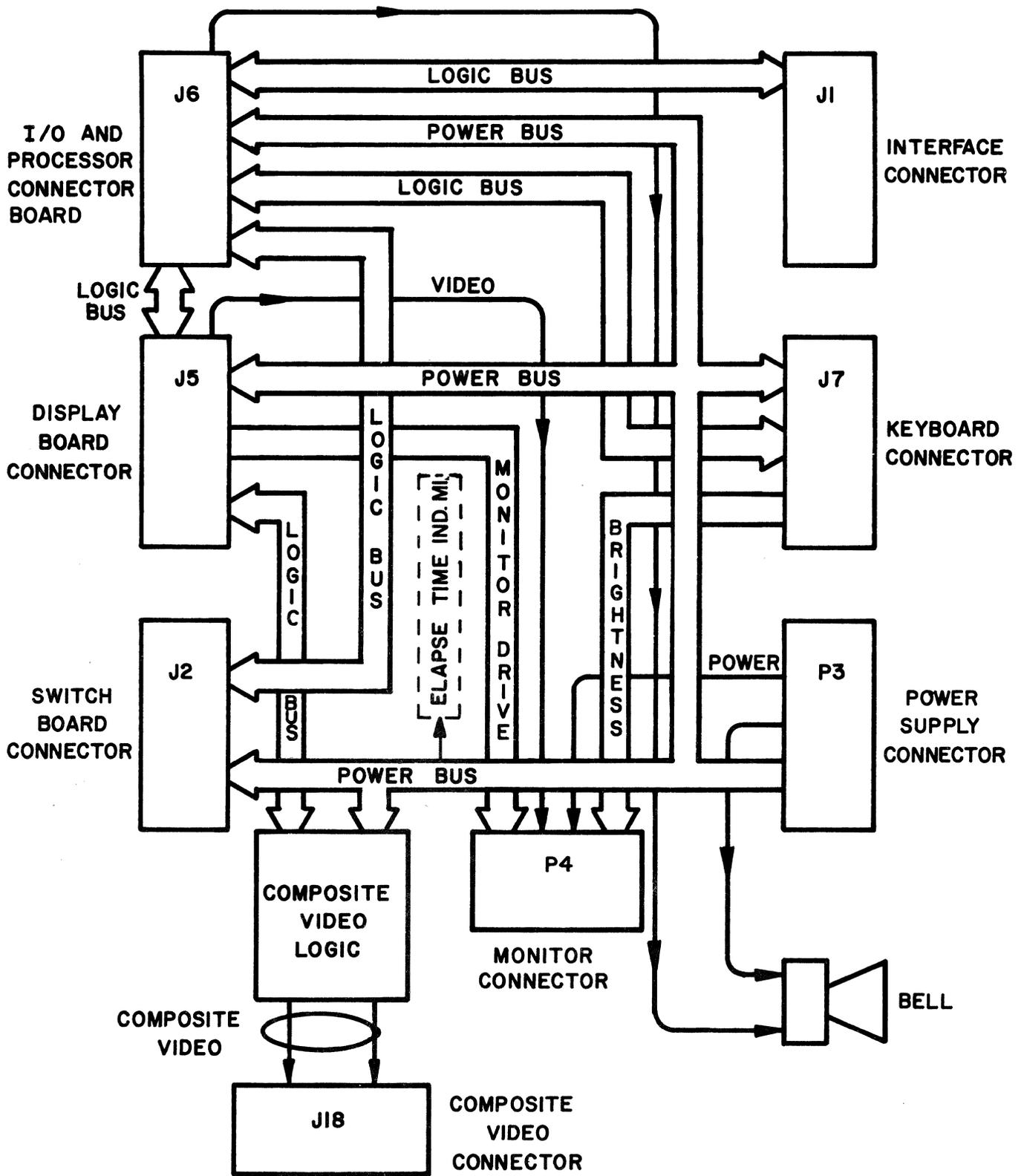


Figure 4-4
Interconnection Board Block Diagram

4.3.2 Power Supply

The Power Supply provides +5, +15, and -12Vdc voltages to the terminal from a 117 Vac source at 50/60 Hz. It will accept a 230 Vac source with ac option strapping (refer to Figure 4-5). These dc voltages are overvoltage and overcurrent protected.

4.3.3 Keyboard

The Keyboard contains the key switches and supporting circuitry to generate the appropriate character and control codes to be displayed or transmitted by the SUPER BEE (see Figure 4-6). In addition, it provides eight special function keys, power-on Indicator, mode indicators and the Monitor brightness control. The Keyboard is compatible with ANSI standards (logical pairing). The characters are encoded into 8-bit ASCII codes. Figure 2-3 defines the SUPER BEE codes available. Figure 2-1 shows the Keyboard key arrangement.

4.3.4 I/O Processor Board

The I/O Processor Board contains the receive and transmit logic, mode and status control, Keyboard control logic, and controller logic (see Figure 4-7). The controller consists of a microprocessor and the program memory.

The micro-processor contains an Intel 8008-1 Micro-Processor unit and associated logic for interfacing with the other functions. Appendix A details the parallel central processor unit (CPU) which basically includes an instruction register, memory arithmetic-logic unit (ALU), and input/output buffers on a single metaloxide semiconductor (MOS) chip. Instructions and data stored in the program memory are utilized by the micro-processor to control the operation of the terminal. The instructions and data are stored in the memory in the form of 256 eight-bit bytes.

The micro-processor loads 8 bits of data from the output bus and 4 bits from the control bus into the memory latch, which retains the data until synchronized with the page memory located on the Display Board. The page data control will decode the 8 bits and determine how they will be used. The micro-processor can read from the cursor address and first line latch back into the memory to aid in defining cursor character number or cursor line number. Thus a SCROLL DOWN is performed by the micro-processor by reading the contents of the first line latch,

decrementing and depositing it back into the first line latch through the mem latch.

The mode and status latch contains information indicating the mode in which the terminal is operating and the status of various signals. The status latch indicated the availability of conditions within the hardware; such as Receiver Done, Transmitter Busy, and KBD Done.

The transmit logic serializes data from the output bus and sends the serial data to an external device and/or printer. The serial data may be either a 10-or 11-bit asynchronous word or an 8-bit synchronous word (see Figure 4-8). The data is transmitted at rates up to 9600 baud. The receive logic receives serial data from the data source (computer) and converts the data into 8-bit parallel words. The parallel data is then applied to the micro-processor and program memory for processing. Serial data may be received synchronously or asynchronously at up to 9600 baud. The receive logic translates RS232C data and converts it to an 8-bit parallel byte. At this time, the receive logic indicates to the micro-processor that data is available for the input bus. The micro-processor obtains the data from the input and utilizes it as either a character to be deposited into the page memory, a control function, or as an escape sequence which will be decoded and acted upon as specified by the program memory.

4.3.5 Display Board

The Display Board contains the cursor control, CRT display logic and display memory. The cursor control consists of the data buffer, page control, cursor address and next line latch (see Figure 4-9). It generates the cursor and related functions. Functions that are controlled by the cursor control include the Erase-to-End-of-Line (EOL) and Erase-to-End-of-Memory (EOM). The data buffer receives and retains the 12 bits of data output by the micro-processor until synchronized with the page memory. The page data control decodes the four control bits which determines how the eight data bits are to be used. The data is applied to the cursor address logic to define the cursor character number or the cursor line number. The micro-processor can read from the cursor address back into the micro-processor. Similarly, the eight bits can be directed to the first line latch, becoming the number of the line to be displayed at the top of the page.

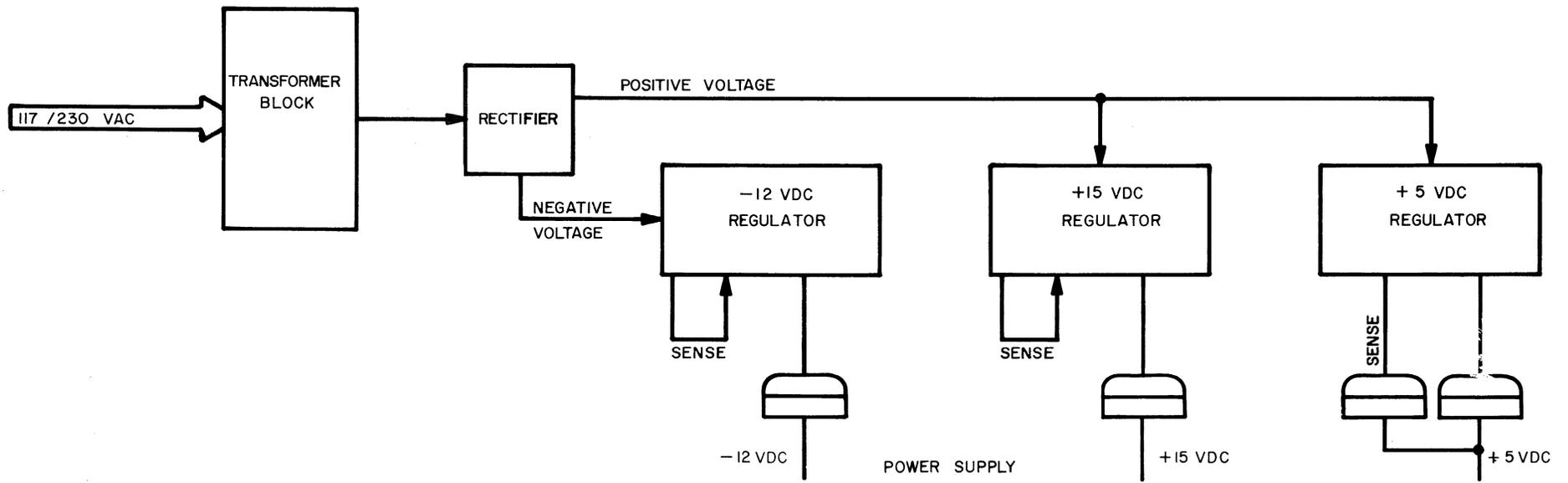
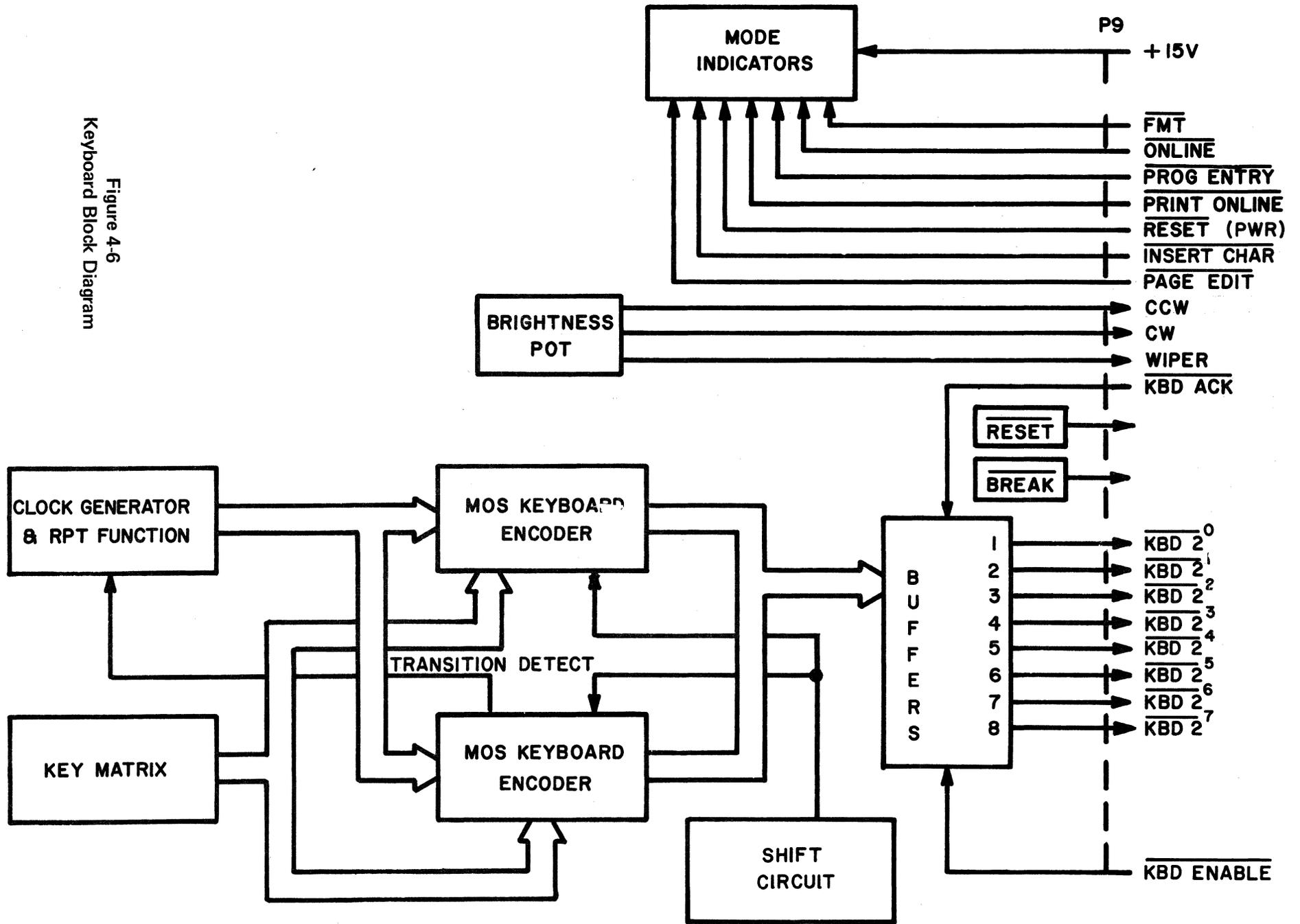


Figure 4-5
Power Supply Block Diagram

Figure 4-6
Keyboard Block Diagram



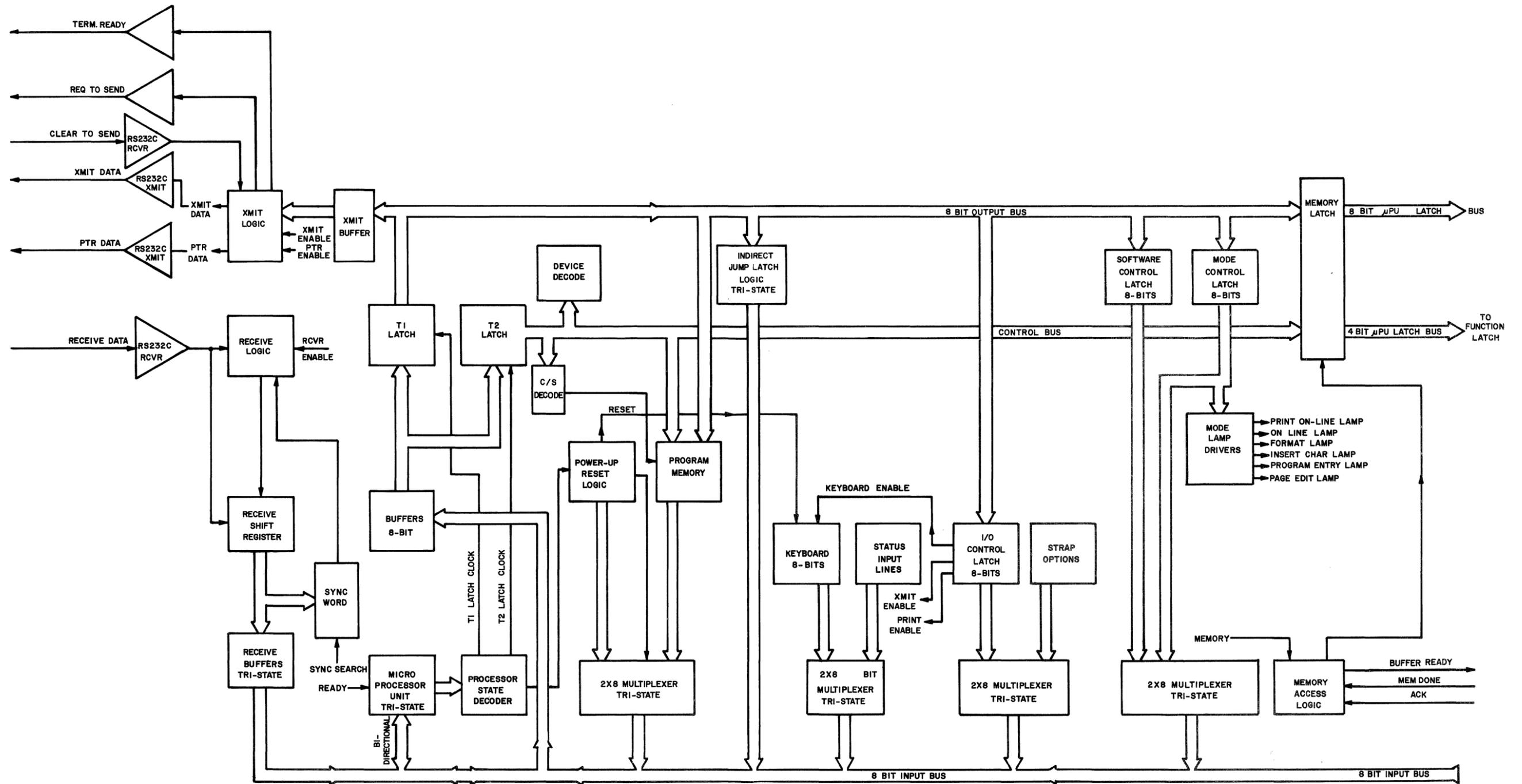


Figure 4-7
I/O Processor Block Diagram

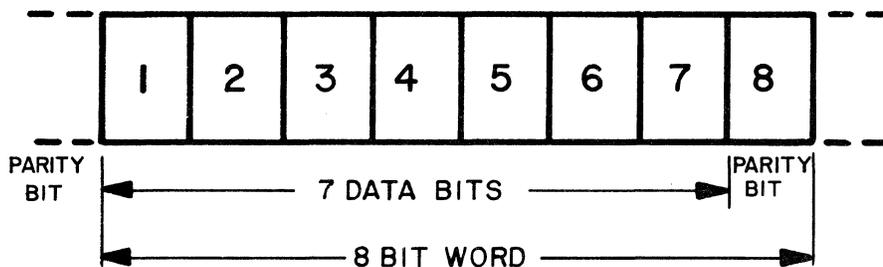
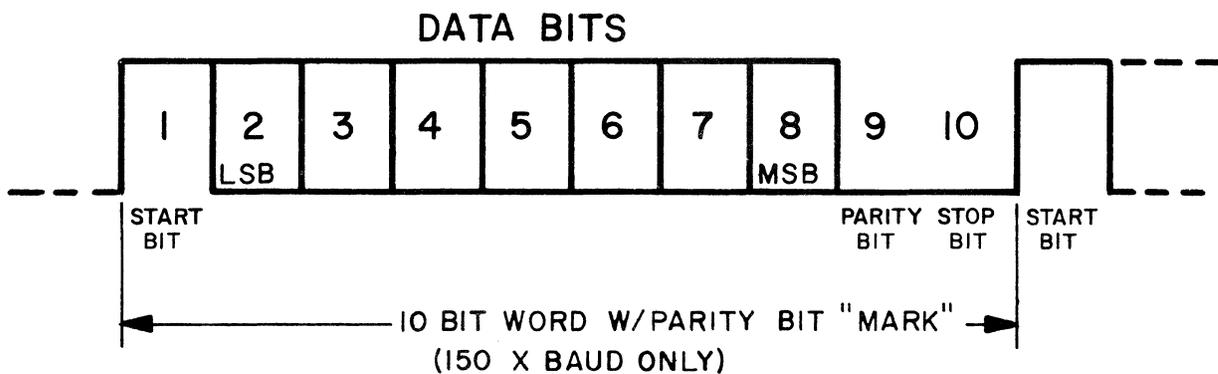
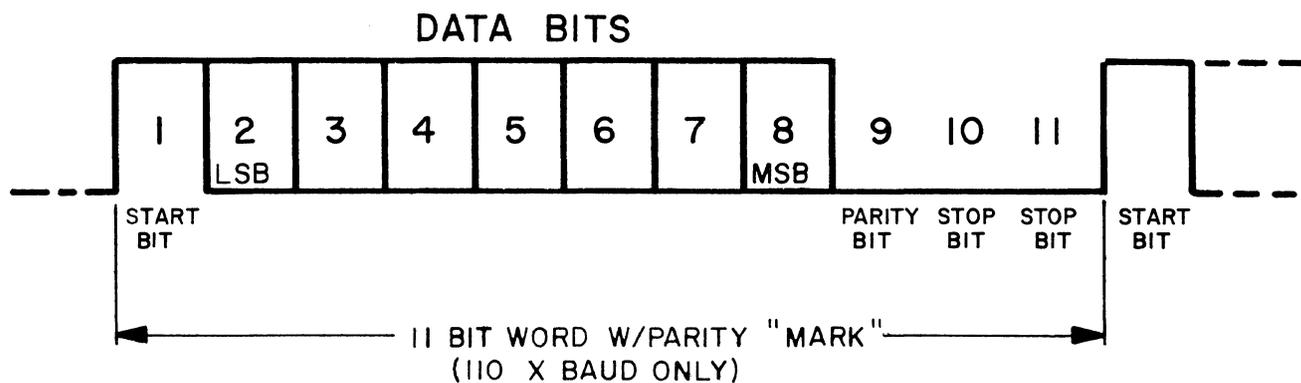


Figure 4-8
Input/Output Word Structure

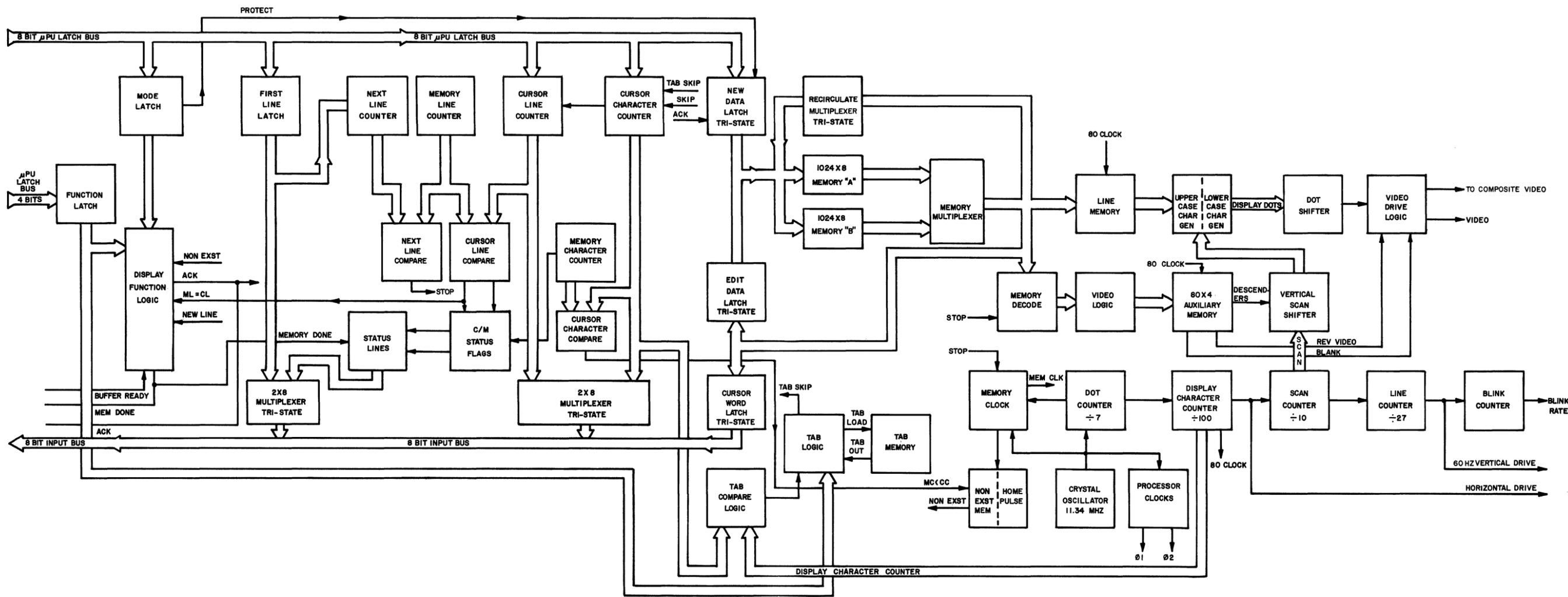


Figure 4-9
Display Board Block Diagram

This data can also be read back into the micro-processor.

The display memory consists of the new data latch, the recirculate logic, the edit latch, the page memory and the cursor word latch. Information to be displayed on the monitor screen is stored in the display memory. The page memory is a recirculating shift register that stores 2048 eight-bit words and provides a recirculate path through the recirculate logic. To update the page memory when the page reaches the cursor locations, the new data latch is enabled to output its data onto the memory input bus. The new data is entered into the memory and replaces the data which was lost by inhibiting the recirculate latch. Therefore, the capability exists for over-writing a character in the memory with a new character. At the cursor time, the other data in the page memory is loaded into the cursor word latch to be read by the micro-processor. The edit data latch delays the recirculating data by one bit. For example, to insert a character, the character is written and the remainder of the page memory is recirculated through the edit latch. The decode logic decodes any special controls that may be on the display; e.g., blinking, reverse video. The decode logic includes the new line decode, which defines the end of a display line when the terminal is in Auto Efficient Paging mode.

The timing generator generates the timing required to provide digital horizontal sync and digital vertical sync on the CRT. In addition, it specifies the amount of time allotted to each dot, character, scan and line of the display. The main timing chain contains logic for generation, timing and control of the SUPER BEE Display, including cursor control, display and character generation, line memory, page memory and edit functions.

4.3.6 Monitor

The Monitor (Figure 4-10) utilizes the vertical and horizontal and video output signals developed on the Display Board to produce a full screen of information consisting of 25 lines of 80 characters each. Brightness and contrast adjustments are provided by external potentiometers located on the Keyboard and back panel respectively. The Monitor is powered by +15 Vdc (115 Vac for optional 15-inch monitors). Appendix B presents general and detailed data for the Monitor assembly.

4.3.7 Interface Assembly

The Interface Assembly consists of two subassemblies; Connector Board - A1 and Switch Board - A2 (see Figure 4-11).

The Connector Board is a direct feed-thru of all standard RS232 data and control signals between the I/O board and an external I/O device and printer.

The Switch Board contains a baud rate selector switch which, in conjunction with a multiplier switch, allows choice of fourteen different baud rates from 110 to 9600. The position of the multiplier switch also determines 10- or 11-bit word transmission. Other switch options are FDX/HDX, AUTO EFF PAGE/CRLF, and LOWER CASE ENABLE/INHIBIT. In Addition, TTL XMIT Clock and Printer Clock signals at strappable rates, are generated on the Switch Board. An optional current loop adapter can be provided to allow for a modified TTY of single or balanced current loop interface.

4.4 DETAILED CIRCUIT DESCRIPTION

The following paragraphs provide detailed descriptions of the functions within the SUPER BEE Computer Terminal. Figures 4-2 through 4-12 depict the function in block, schematic and logic forms. Figures 4-12 is located at the end of this section.

The micro-processor instructions require one, two, or three machine cycles for complete execution. The first cycle is always an instruction fetch cycle (PCI). The second and third cycles are for data reading (PCR) or I/O operations (PCC).

4.4.1 Instruction Fetch Cycle

At time T1 of the cycle, there is an output of the lower 8 bits of the address from which the next instruction is retrieved. The lower 8 bits from the micro-processor are buffered and applied to the input of the T1 and T2 latches. The output on the state lines of the micro-processor is the code for T1 time and is decoded on the state decoder. The result is a low on the T1 output which is applied to the clock input of T1 latch, and the lower 8 bits of the address are loaded into the T1 latch. The micro-processor then sequences to output the next 8-bit word, which is the upper 6 bits of the address. The micro-processor also sequences the cycle control decoding to identify an instruction fetch

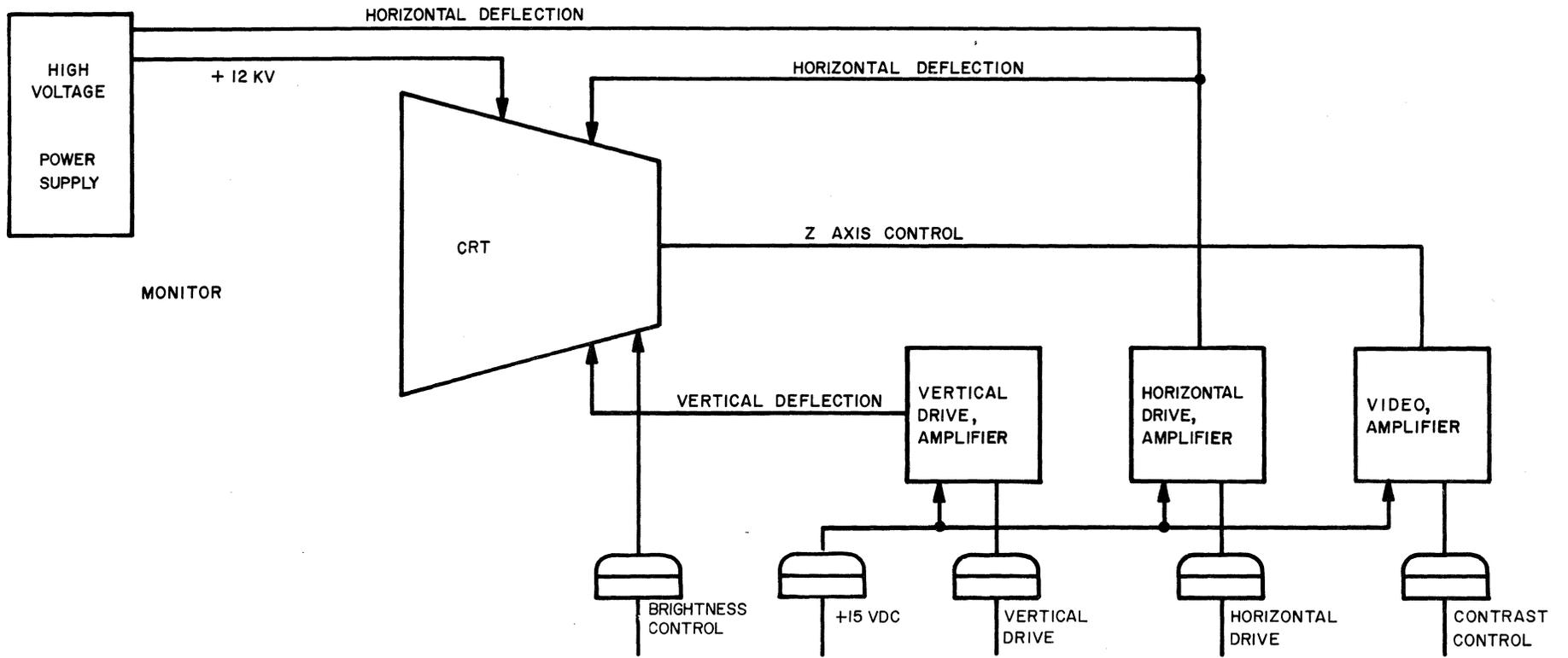


Figure 4-10
Monitor Assembly Block Diagram

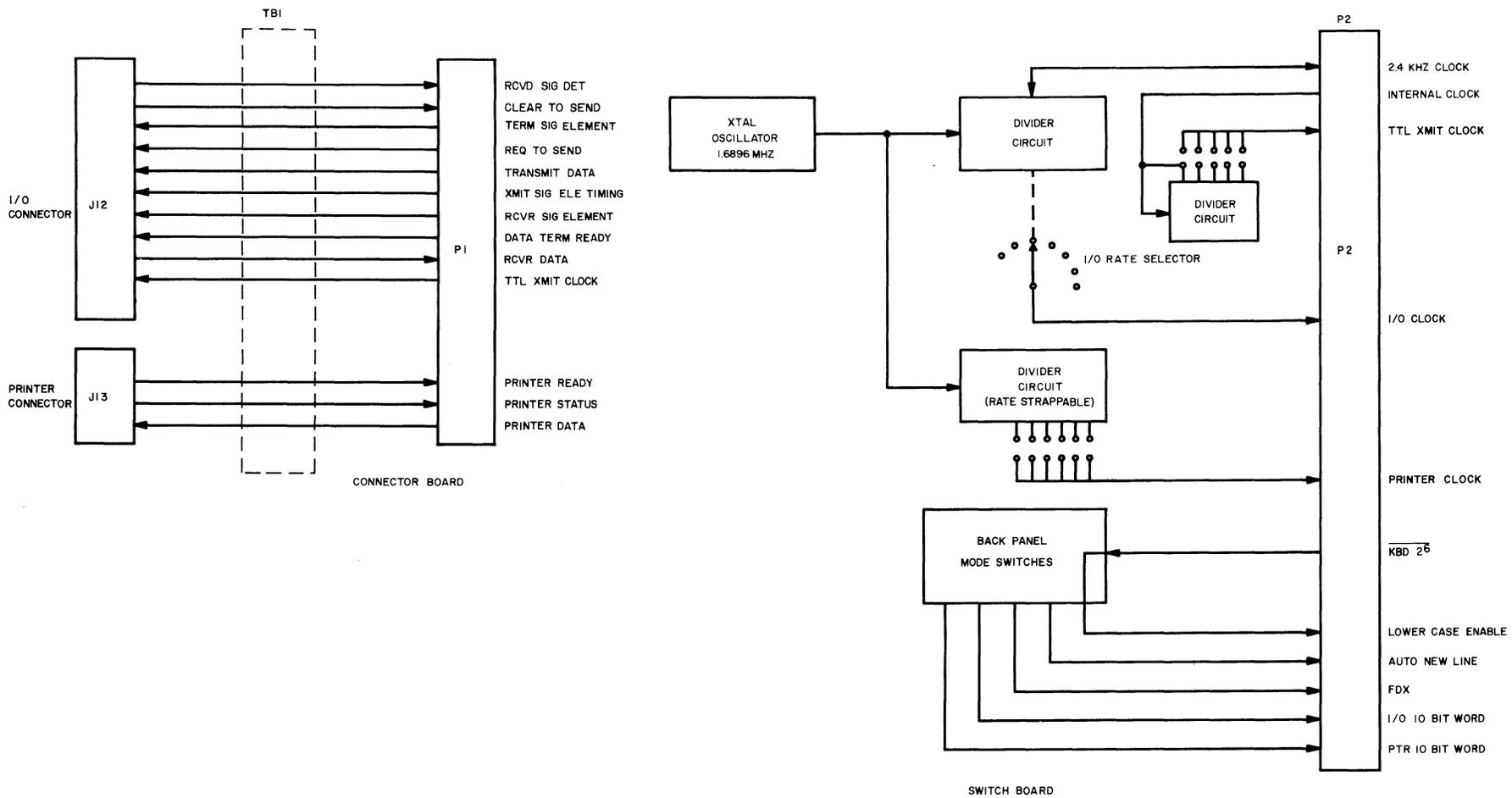


Figure 4-11
Interface Assembly Block Diagram

cycle. The T2 time code is on the state line at this time and is sent to the state decoder. The state decoder has a low on the T2 output which is applied to the T2 latch clock input which loads the data output, at time T2, into the T2 latch.

The lower 4 bits of the T2 latch are applied to the ROM decoder that determines which of the ROM's is being addressed. In turn, the appropriate chip select signal is enabled. The data from the T1 latch is applied to the address inputs of each program memory and the desired program memory is then selected. The data stored at that address is applied to the memory multiplexer. The memory multiplexer is enabled at time T3. The data in the memory is applied to the input bus and read back into the micro-processor as an instruction. The processor then goes to times T4 and T5 unless the micro-processor jumps from the time T3 back to another time T1 to read additional data bytes from memory (data fetch) or to execute an I/O cycle.

4.4.2 Data Fetch Cycle

If the instruction requires additional bytes of memory as data, the micro-processor fetches additional data from subsequent memory locations. This is accomplished in the same manner as it did for the first byte of the instruction.

4.4.3 I/O Control Cycle

The contents of the register are latched into the T1 latch and the device number is loaded into the T2 latch during time T2. Four bits of the T2 latch are decoded by the I/O decoder, directing a strobe to the approximate I/O device at time T3. If the device number is above 17, the T1 latch and the lower 4 bits of the device number from the T2 latch are applied to the memory latch. This results in a 12-bit word that leaves the I/O Processor Board and goes to the Display Board. If unused data is already in the memory latch, the processor must wait until that data is used. This is accomplished by dropping the ready line to the processor. The ready line may also drop, strapping processor operation, if inputs from memory are attempted before the memory logic has processed all output data addressed to it.

The RESET key sets the appropriate flip-flop in the power-up reset logic to generate the Jam

Reset signal. The Jam Reset signal is applied to the memory multiplexer, which is switched to look at the fixed instruction Restart 10. This instruction is applied to the input bus. At the same time, an interrupt is given to the micro-processor which looks at the instruction and uses it to initiate the reset routing.

4.4.4 Indirect Jump Circuitry

The indirect jump circuitry, which is associated with the micro-processor circuitry, enable an address or a data word to be executed. The sequence of events would be to first address the indirect jump latch as an I/O device and store a number in it. The second byte of the following instruction is received from the indirect jump latch, instead of from the program memory, and causes that instruction to be modified.

4.4.5 Mode Latch and Software Latch

The mode latch indicates in which mode the SUPER BEE is operating. The bits in the mode latch are: bit 1, Format; bit 2, Insert Character; bit 3, Program Entry; bit 4, Page Edit; bit 5, Print On Line; bit 6, On Line; bit 8, Protect. The Protect bit is stored in the program memory as bit 8 whenever new data is placed into the memory. Similarly, the software latch is used as a one-byte scratch pad. The software latch and the mode control latch outputs are multiplexed back to the input buss.

4.4.6 I/O Control Latch

The I/O control latch holds control bits to control the I/O circuitry. The control bits are designated as follows: bit 4, I/O Receive Enable; bit 5, Printer Enable; bit 6, Sync Search (this must go low and then high again to cause the hardware to go into Sync Search); bit 7, I/O Transmit Enable; and bit 8, Keyboard Enable. The I/O control latch is multiplexed with the selectable straps. There are eight selectable straps; send control codes, pseudopolling, sync/async, external clock, store special functions, block transmit, and go-off line. These functions are also multiplexed through a multiplexer back onto the micro-processor input bus so that the status of the I/O control features and of the strapable options can be sampled in order to make decisions when jumping to subroutines.

4.4.7 Keyboard and Status Word Multiplexer

Data to be displayed or transmitted is generated at the Keyboard. The characters are encoded into 8-bit codes compatible with ANSI standards (logical pairings). The Keyboard lines enter the Keyboard and status word multiplexer. The eight Keyboard data lines are multiplexed with the status input lines to indicate the status of various devices (i.e., receiver buffer empty, transmit buffer full, etc.). The capability exists for dumping onto the input bus either the Keyboard lines or the status input lines.

4.4.8 Receiver/Transmitter Functions

The receive logic receives serial data from the computer and converts the data into 8-bit parallel words. Serial data may be received synchronously or asynchronously up to 9600 baud. The receiver is enabled by the I/O control latch with the I/O receiver enable signal. Data is received into a standard EIA RS232 line receiver where the data is converted to TTL levels and applied to the receiver bits. The incoming character is clocked into the receiver and, upon completion of the character, is dropped into the receiver buffer. The receiver indicates to the micro-processor that the input function has been performed and that the receive buffer is full. The receive buffer holds the character coming in until the processor is ready for inputting. The buffer is sampled and the received character is sent into the micro-processor where it is used as either a character to be deposited into the page memory, a control function, or an escape sequence which will be decoded and acted upon as specified by the program memory.

When the operator desires to output a character, the data in the T1 latch is clocked into the transmit buffer. When the Clear-to-Send signal is received, the character is transferred into the transmitter shift register, the start bit is generated and the transmitter counter is initialized. The character is then transmitted out serially, at the selected baud rate, by the transmit clock which can be strapped to an internal, crystal-controlled source or to an external source. The serial data may be either a 10- or 11-bit asynchronous word, or an 8-bit synchronous word. The data is transmitted at rates up to 9600 baud. Whether a 10- or 11-bit word has been selected will determine when to indicate that the character is complete so that the transmitter is empty and capable of outputting another character.

The data that is transmitted from the transmitter shift register is applied to a line driver which translates the data to standard RS232 levels and applies the data to the system. When the terminal is in Print-On-Line mode, any incoming or outgoing data is applied to the printer connector.

4.4.8 Timing

The timing source is a crystal oscillator that operates at 11.34 MHz. This is used to derive the timing for the display memory and display circuitry, and for generating the micro-processor phase clocks. The crystal is accurate to within 0.1 percent of its center frequency over the operating conditions of the terminal. The processor timing is derived from a divide-by-15 circuit giving the processor clocks, $\phi 1$ and $\phi 2$, a rate of 156 KHz. The appropriate outputs of the micro-processor clock counter are strobed into flip-flop to give both $\phi 1$ and $\phi 2$ four dot-width each, with $\phi 2$ following three dot-widths after $\phi 1$. Since both clocks are required to drive the processor and its associated circuitry, the terminal cannot operate without the clocks operating properly. The page memory clocks are obtained from either a divide-by-3 circuit (at a frequency of 3.78MHz) or from the video clock. The video timing is derived from a chain of counters which count the 11.34 MHz oscillator rate down to 60 Hz and lower. The 60 Hz frequency is the page refresh rate.

4.4.10 Character Generation and Display

A page is broken into 27 character lines, two of which are used for the vertical retrace. Each line is made up of 10 horizontal scans for character display (61.8 milliseconds per scan) (See Figure 4-13). Each scan is broken down into 100 character times, 80 of which are displayed and 20 of which are used for horizontal retrace. Each character time consists of seven dot times, five of which are used to display the character and two dot times are used to separate characters. Rates below 60 Hz are generated and are used to blink the cursor and to blink characters on the display.

The first counter in the video timing chain is the dot counter, and is actually used as a shift register. Feedback from the outputs to the inputs ensures that two zeros will always be circulating in the chain and that all other bits will be

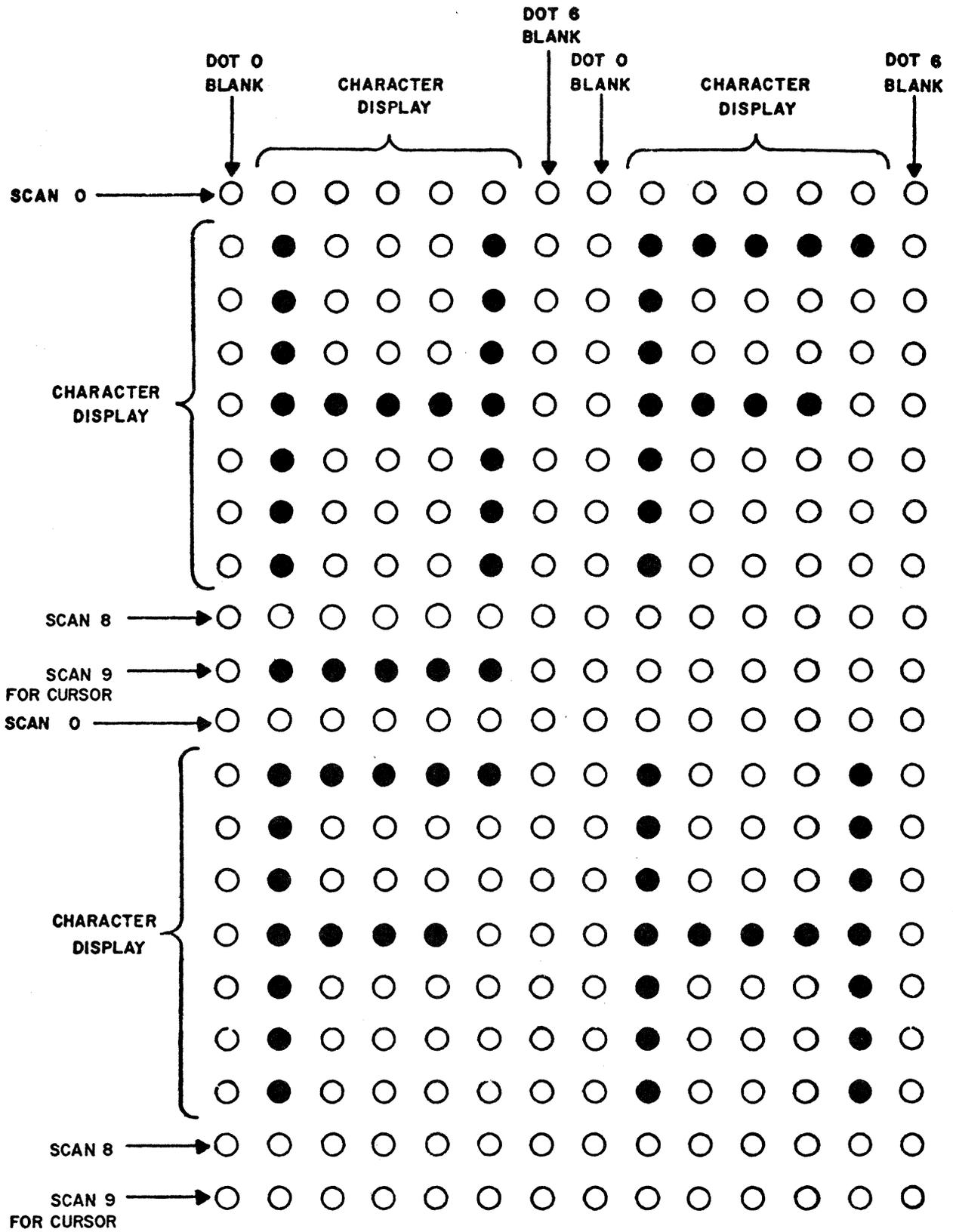


Figure 4-13
Character Dot Matrix

ones, with zeros being on the same two adjacent outputs after every seven oscillator clock pulses. Each output then corresponds to a specific pair of display dots, dot 6 and 0 being the dots between characters.

The trailing edge of the dot counter output of dots 5 and 6 drives the character counter. The character counter indicates a binary count corresponding to the character presently encoded in the line memory outputs and on the character generator inputs. The counter employs two 4-bit binary counters tied together. On the rising edge of the clocks following the binary count of 79, the counter is preset to the value of -20 and the sign bit C80 is then used to inhibit clocking of the line memory for 20 character times which corresponds to the 20 character times used for horizontal retrace. Therefore, the count modulus of the counter is 100 and goes from -20 to 79.

The output of the character counter drives the scan counter. The scan counter is a decade counter. The outputs of the scan counter are channeled through an adder which passes the scan number to the character generator. The last scan (scan 9) from the scan counter is the scan during which data from the page memory is loaded into the line memory and during which the cursor is displayed.

The line counter is composed of a 5-bit counter and has a modulus of 27. The output of the line counter overflows at a 60Hz rate, and from this the vertical drive for the CRT is derived. Additional ripple counters are used to divide the 60Hz frequency down to 1.875Hz for the cursor blink rate and 0.9375Hz for the data blink rate on the display.

Two different types of CRT's can be driven by the SUPER BEE circuitry; an analog monitor which decodes composite video signals available at the video port on the back panel, or a digital monitor similar to that used within the terminal. The digital monitor uses separate signals for the video, vertical and horizontal drive pulses. The video is driven by standard TTL logic with 3.5 volts being the white level and 0.5 volts being the black and blanking levels.

Blanking may be obtained from any of five places. First, blanking can come from vertical drive.

Second, during the vertical retrace time, the screen is blanked. Third, the C80 sign bit time is also blanked, which also is the corresponding time of the horizontal drive. Fourth, the blink circuitry will cause blanking to appear because certain codes in the memory cause certain portions of the display to blink on and off. Characters that control blinking are also blanked. Finally, the Monitor can be blanked by decoding the new line symbol and blanking the display line following that symbol.

The horizontal drive circuit outputs a positive-going pulse which starts when the character counter reads -16 and ends when it reaches the count of 24. The vertical drive provides a negative-going pulse which starts at line 25 and ends at line 0.

In order to generate video for the CRT, the following is done: on command from the video timing circuitry, the main memory is slaved to the video character rate of 1.6MHz for enough time to transfer 80 character codes from the page memory to the line memory. This occurs on scan 9. Once the transfer is complete, the page memory assumes the fast clock rate. The line memory is recirculated nine times and on each of the 10 passes of the line memory, corresponding to the 10 scans of the CRT, the character generator codes stored in the line memory are presented to the character generator inputs with scan number from the scan shifter. The character generator outputs a set of five bits on five parallel lines, each bit representing one dot to be displayed on the screen. The bits are chosen according to the character decoded from the ASCII input scan number. For example, in the letter H on the first scan, the first and fifth bit would be a one while the second, third, and fourth bits are zeros. This would be true on scan 1, 2, 3, 5, 6, and 7, and while on scan 4, all five bits would be a one forming the character H. All bits of all characters are zeros on scan 0. The display is blanked by the blanking circuitry to place spacing between the lines of text on the CRT display.

Certain characters (i.e., the lower case g, j, p, q, and y) have tails that drop below the ordinary line of text. This is handled in the display circuitry by subtracting 2 (by one's complement addition) from the scan number given to the character generator so that when the character generator is in the eighth and ninth scans of the display, it simulates the sixth and seventh scans.

The 5-bit output of the character generators are loaded into a parallel-to-serial shift register with zeros

to separate characters from each other and is then shifted out to become the video on the CRT after passing through the blanking and reversing circuits. The shift register used in this case is a synchronous load device dumping the data of the parallel load inputs into the register on the rising clock edge when the load shift input is low. Since the load shift input is low for both dots five and six in this circuit, the hardwired zero of the first stage actually appears at the output twice before the other bits appear, providing two-dot spacing between characters on the display.

4.4.11 Page Memory

The page memory is composed of two banks of shift registers. Each bank is eight bits wide and contains 1024 bits. These are multiplexed so we have a total of eight bits wide by 2048 bits long. These banks shift on alternate pulses of the memory clock, the output of the non-shifting bank being multiplexed into the memory bus.

Unless data in the page memory is being modified, the data on the memory bus is gated into the memory input bus through non-inverting gates to be read into the opposite bank from which it originated. This occurs on the trailing edge of the memory clock pulse which brought it out of the multiplexer. Since the banks are each 1024 bits long and the multiplexer buffers a character at its input, we have a total of 2049 memory clock pulses required for a full circulation of the memory. Twenty-seven full circulations occur every time the page is refreshed on the screen. The refresh occurs 60 times per second and results in the minimum average clock frequency of 3.31938MHz.

To write a piece of new data into the page memory, the control circuitry waits until the data to be replaced appears on the memory bus. It then enables the new data latch, which contains the data to be written onto the memory input bus. It disables the recirculate gate, which otherwise would put the memory output bus data into the memory input bus. The trailing edge of the memory clock which brought up the data to be replaced will write the new data into its place in the shift register. Essentially, the character presently appearing at the front of the memory is replaced with a new character to be loaded into the memory.

If the new data to be loaded into the memory is to be inserted between existing data without losing

the existing data, then the edit data latch is enabled into the memory bus after the new data latch instead of the recirculate gates. The edit data latch always holds the most recent character on the memory bus. During the memory clock period just following the writing of the new data, the latch holds the data which lost its place to the new data and writes the displaced data into the place just following the new data. It then picks up the next character from the memory bus. Thus, the edit data latch acts as an effective one character delay or lengthens the page by one character. Therefore one more character can be inserted into a location and delay all other data by one character location from where it was previously located.

When the page memory is completely filled with data, it is necessary to drop the first line to make room at the bottom of the memory. To accomplish this, the first line must be erased with delete codes. This is accomplished by disabling all inputs to the memory input bus while the new locations are being loaded into the shift register. The pull-up registers on the memory input bus ensure that delete codes are loaded into the page memory. The cursor point in memory is recirculating at a speed much too fast for the processor to time up to and read the data that the cursor is under. Therefore, the data in the memory bus at the cursor time is gated into the cursor word latch and is held there until the next cursor occurs. This provides sufficient time for the processor to read the word where the cursor is stored.

Several decoders are used to identify special characters at the output of the page memory. For example, the new line code is decoded and is used in the memory character counter circuitry. One decoder monitors the lower four bits of the memory bus and the second decoder monitors bits four through seven. Bit eight designates a character as protected or unprotected in the Format mode or as an escape character in Program Entry mode. The negative input and subsequent outputs from these two decoders provide unique decodes for most characters. For example, the space code, which is octal 40, is useful in the control of line mode instructions. The control circuitry needs to know when two or more space codes occur in a row. Gating is used to decode the space code on the memory bus and a latch is used to indicate two or more in a row. The g, j, p, q and y

codes are decoded as a group and are used to set a bit in the extension of the line memory identifying these codes as requiring descenders. The codes enable the scan shifter circuitry to shift the scans. Octal codes 20, 21, 22 and 23 are decoded to start and stop the reverse video and the blink functions. Whenever one of these four codes appears, the flip-flop that control the blink function are clocked to appropriate states (unless in the Program Entry mode).

4.4.12 Cursor Character and Line Counter

The cursor character counter and cursor line counter provide a means for controlling the cursor location. The cursor character counter indicates to the cursor what character position it is on for a given line, and the cursor line counter defines which line it is on. The cursor character and cursor line counters can be preset to any specific character in any specific line by the micro-processor.

4.4.13 Memory Character and Line Counters

The memory character counter and the memory line counter provide a means of keeping track of the memory location. The memory character counter indicates which character in memory is present at the input of the memory, and the memory line counter further identifies that character. The memory is organized then into a character and line scheme. The memory character counter and memory line counter are clocked by the same clock that clocks the memory. When they are the same binary configuration, the cursor location equals the memory location. This comparison is NRC (non requested cursor) and will load the word in memory into the cursor word latch.

The cursor can be located at any time in the memory, simply by taking the cursor character latch and the cursor line latch and loading them onto the micro-processor input bus.

4.4.14 Home Counter

The home counter keeps track of the memory location for the sole purpose of identifying the end-

of-memory. At its overflow, the memory line and character counters are reset and several status flags are set indicating the cursor location relative to end-of-memory.

The first line counter is loaded by software with the number of the line to be displayed as the top line of the display. This is loaded into the next line counter during vertical retrace, and is incremented as the display works its way down the screen. The output of the next line counter is compared against the output of the memory line counter, generating the stop signal when the outputs are equal, and stopping the memory clock until the next scan 9. At this point, the first character of the next line to be displayed is sitting at the output of the memory.

4.4.15 Current Loop Adapter

The current loop adapter is dual purpose.

a. A modified TTY interface for some mini-computers features an open collector output and photoisolated input. The computer should be written 50 ft. of the terminal.

b. A single or balanced current loop interface can be used up to 2000 ft. away. With twisted, shielded 2 pair cable and slower baud rates. It may be useable up to 6000 ft.

A photoisolated input and 20 ma current driver is required at the other end. An operational amplifier bipolar output (+15 to -20 volt) drives about 20 ma of current through the loop. Up to 1000 ohm of loop resistance can be tolerated. (Note - the amplifier output can drive an RS232 input if desired).

In either a or b mode above, the receive line data is internally buffered and or'ed with data from the RS232 connector. Data can be input on either but not simultaneously. Data is output simultaneously on both.

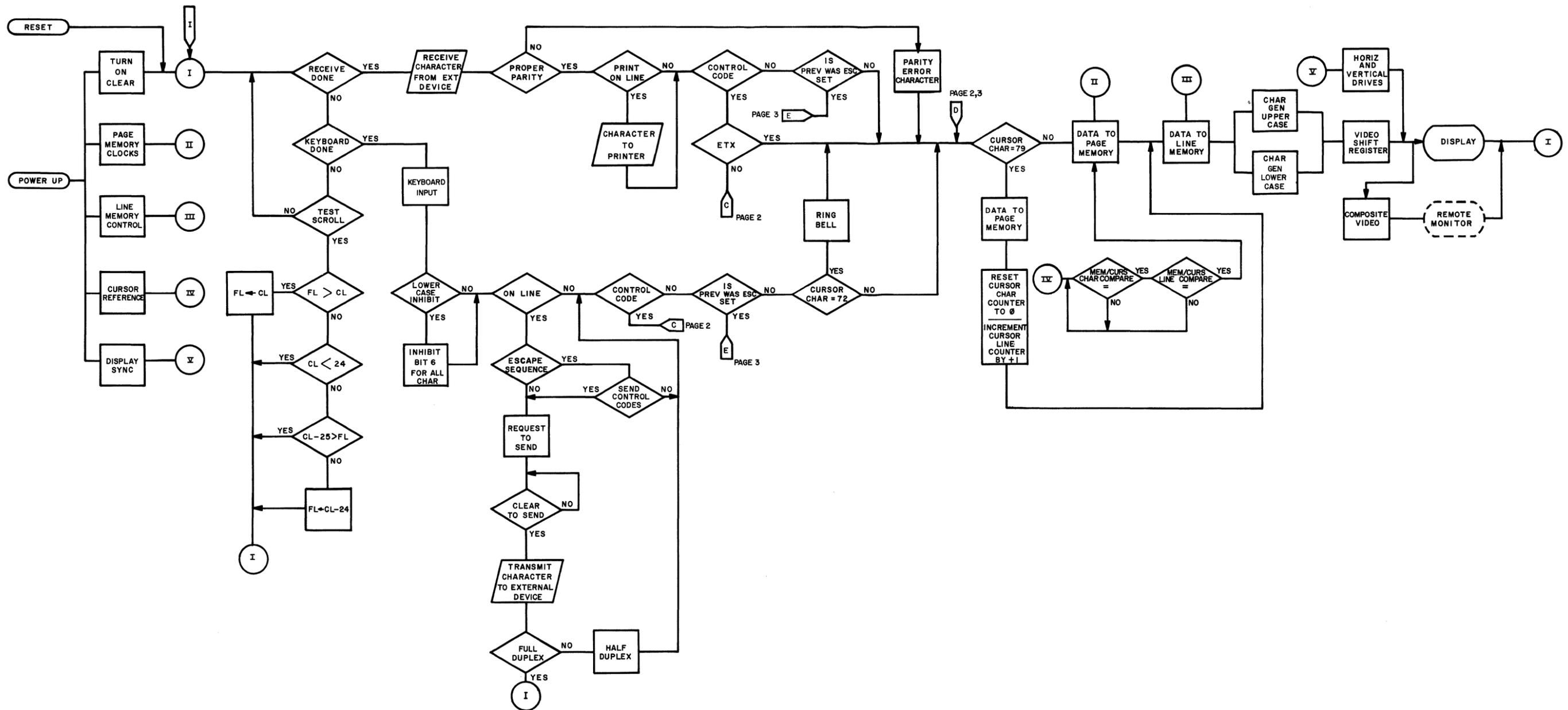


Figure 4-12 (Page 1)
Functional Flow Diagram

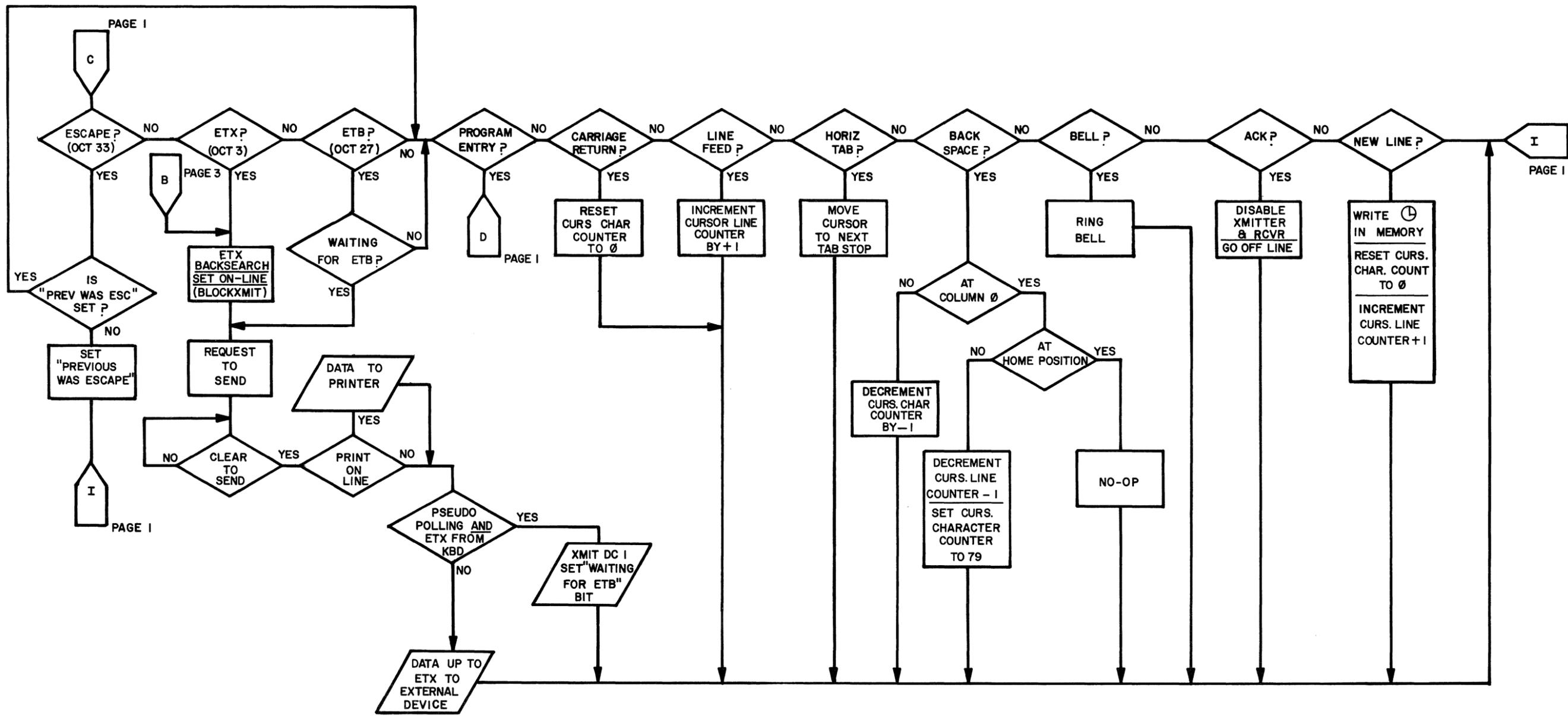


Figure 4-12 (Page 2)
Functional Flow Diagram

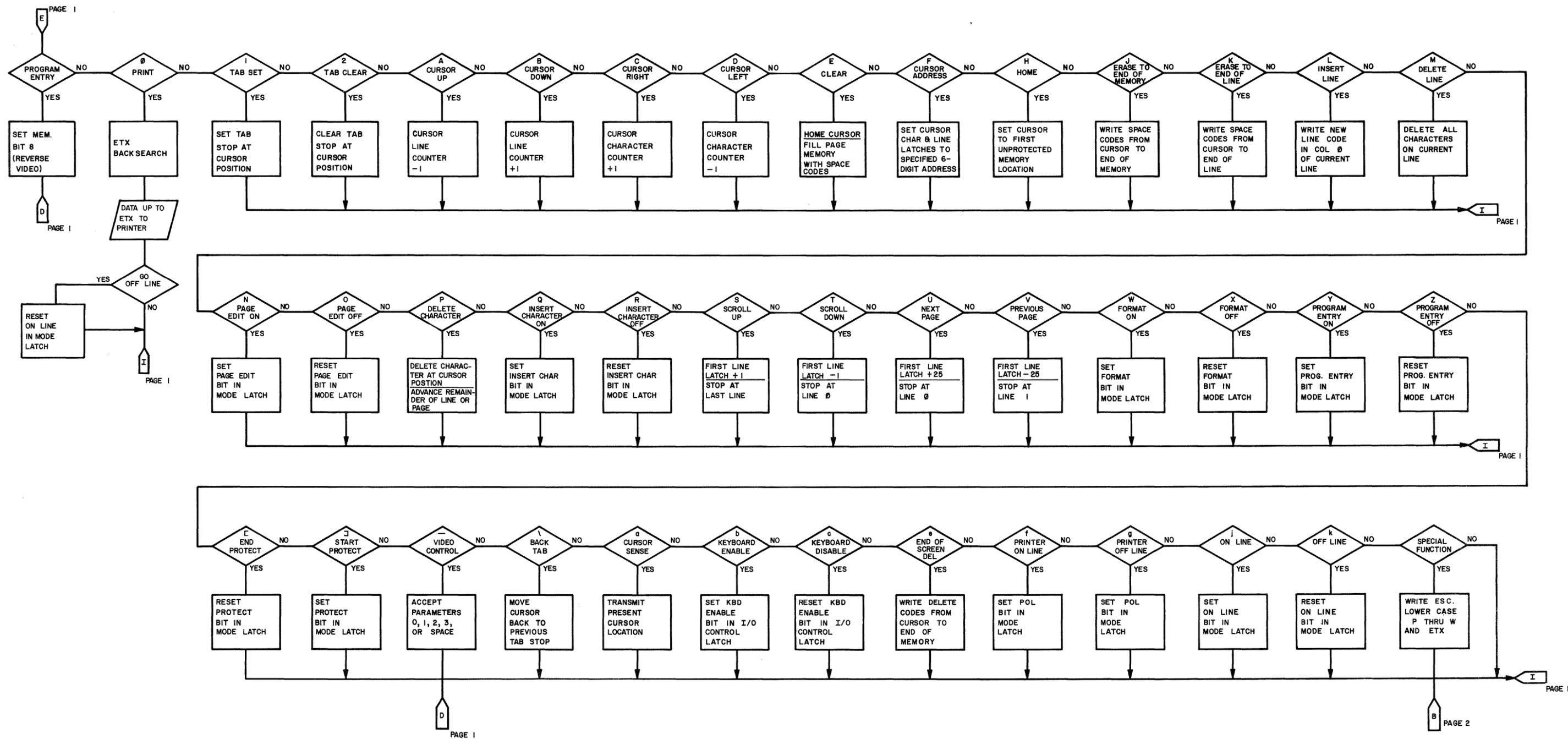


Figure 4-12 (Page 3)
Functional Flow Diagram

SECTION V MAINTENANCE

5.1 INTRODUCTION

This section contains information to aid in the maintenance of the SUPER BEE Terminal. Preventive and corrective maintenance procedures are specified as well as troubleshooting aids and techniques.

5.2 PREVENTIVE MAINTENANCE

No scheduled periodic maintenance is required. However, several precautions can be taken periodically to ensure proper operation. Care should be exercised to see that there is proper air circulation for the fan. The terminal should not be placed on a shag carpet or other soft surface that could impede the air entrance to the fan. Special care must be taken to ensure that no paper or other loose articles are placed under the terminal. The degree of dust density in the air should be considered in selecting the location of the terminal, since there is a possibility of foreign matter clogging the fan filter. In the event that this should occur, the filter must be vacuumed out. The dust can be removed while the filter is still in the unit. In more severe instances, the fan filter can be replaced. This is done by turning the terminal on its side and removing the four screws in the fan filter, and then the filter itself.

The plexiglass window may require periodic cleaning. The absite coating makes the plexi-glass highly scratch resistant and it may be wiped with a soft cloth.

The interior of the unit may be vacuumed or wiped free of dust. Accumulation of dirt causes overheating and component breakdown. Dirt acts as an insulating blanket and prevents efficient heat dissipation. A small brush is very useful for dislodging dirt; a cotton-tipped applicator is good for narrow or hard to get places.

5.3 CORRECTIVE MAINTENANCE

This section provides corrective maintenance information to aid in servicing the SUPER BEE Terminal. It is suggested that the configuration sheet and the turn-on procedure be consulted before performing the corrective maintenance described here.

5.3.1 Troubleshooting Aids

The following troubleshooting aids are provided in this manual to assist in the troubleshooting of functional failures.

- Circuit Schematics
- Basic Block Diagram
- Intermediate Block Diagram
- Detail Block Diagram
- Functional Flow Diagram
- Interconnect Diagram
- Timing Diagrams
- Glossary of Terms
- Troubleshooting Flow Diagrams
- Disassembly/Assembly Procedures
- Adjustment Procedures
- ASCII Code Sheet
- Configuration/Strapping Information
- Character Dot Matrix
- Pictures of Wave Shapes

5.3.2 Troubleshooting Equipment

The following is a list of tools and standard equipment required to repair a SUPER BEE Terminal.

- V/O Multimeter
- Oscilloscope
- Assorted Electronic Hand Tools

A Full Duplex Echoplex Test connector may be required to test the terminal in FDX. This speci-

ally wired connector may be assembled to mate with J2 (See Figure 5-1). This connector tester allows the terminal to be operated and tested independent of an external data device. The basic set-up for the test is as follows:

- FDX (Full Duplex Mode)
- On-line
- Baud Rate - Any Setting

The operator enters data from the Keyboard as if the terminal were on-line to a computer. If data is displayed on the screen properly, then the SUPER BEE is transmitting and receiving data properly. The test connector is wired as follows (Refer to Figure 5-1):

- Connects transmitted data line out of the terminal to received data line into the terminal, Pin 2 to Pin 3 of J2.
- Connects Request-To-Send control line out of the terminal to Clear-To-Send line into the terminal Pin 4 to Pin 5 of J2.
- Connects Receive-Line-Signal-Detector line into Data-Terminal-Ready, Pin 8 to Pin 20 of J2.

5.3.3 Preliminary Troubleshooting Considerations

The most common problems occurring in the SUPER BEE Terminal are switch, control or operation-related. A simple procedure may be followed to help determine if the problem is control and/or operation-related or internal circuitry related by checking the following:

- Illegal Operation (Refer Section II)
- Improper Baud Rate Setting
- Wrong Transmit or Receive Mode (HDX/FDX)
- Loose Interconnect Cable

NOTE: Because the Power Supply output voltages may affect the terminal in various ways, manifesting itself differently each time, it is suggested that the output voltages be verified good in accordance with the Power Supply adjustment procedures (refer to Section 5.3.4 or Appendix C).

An index of troubleshooting flow diagrams is given in Table 5-1. This index lists the apparent failures and references the user to the proper flow diagram. To derive the maximum benefit from Table 5-1, the following procedure is recommended;

1. Find the apparent trouble in the Troubleshooting Flow Diagram Index.
2. Proceed to the specified troubleshooting flow diagram in the diagram section and begin the troubleshooting procedure.
3. If an adjustment procedure is referenced in the troubleshooting flow diagram, perform the adjustment and return to the flow diagram to complete the troubleshooting process.
4. Reference is made to Timing Diagrams and Wave Shapes which are contained in the Diagrams Section (Section VI) of this manual.

TABLE 5-1. TROUBLESHOOTING FLOW DIAGRAM INDEX

Apparent Failure	Troubleshooting Flow Diagram
GENERAL	
1. Power indicator off, but raster present on CRT screen	5-1A
2. No raster present, but power indicator on	5-1B
3. No raster present and power indicator off	5-1C

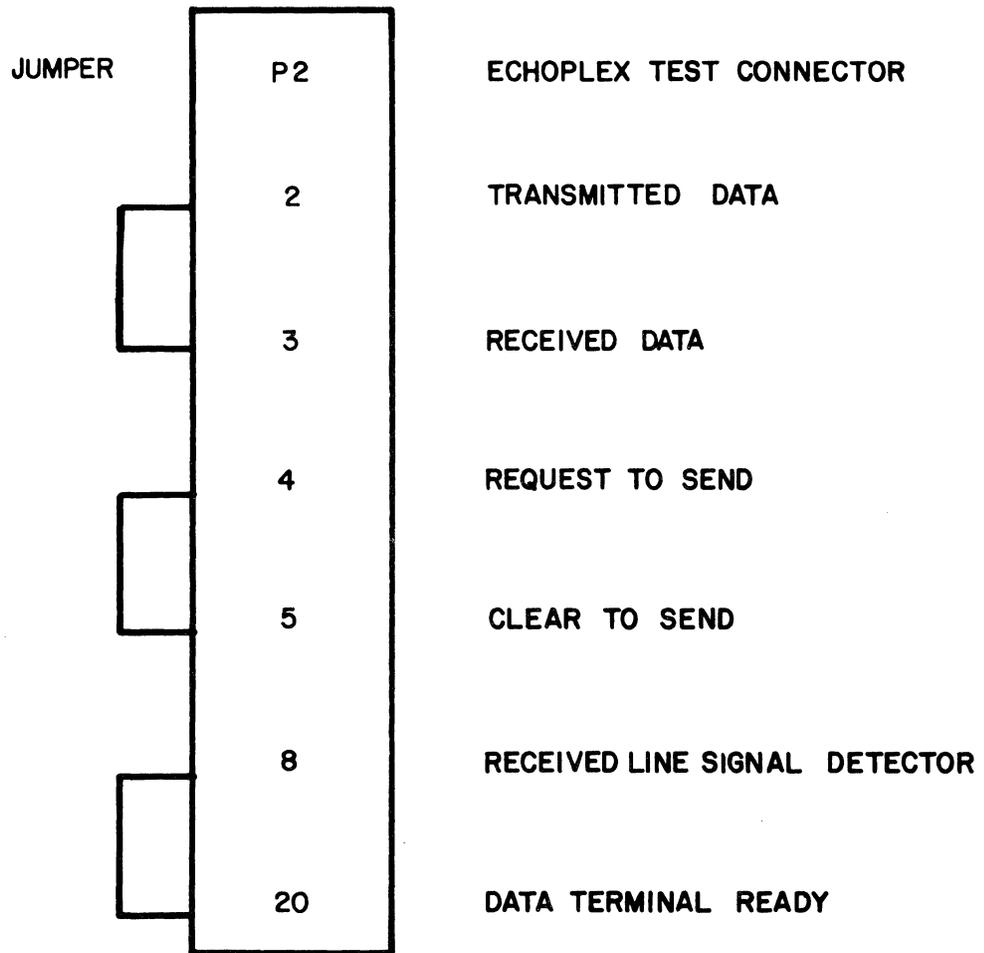
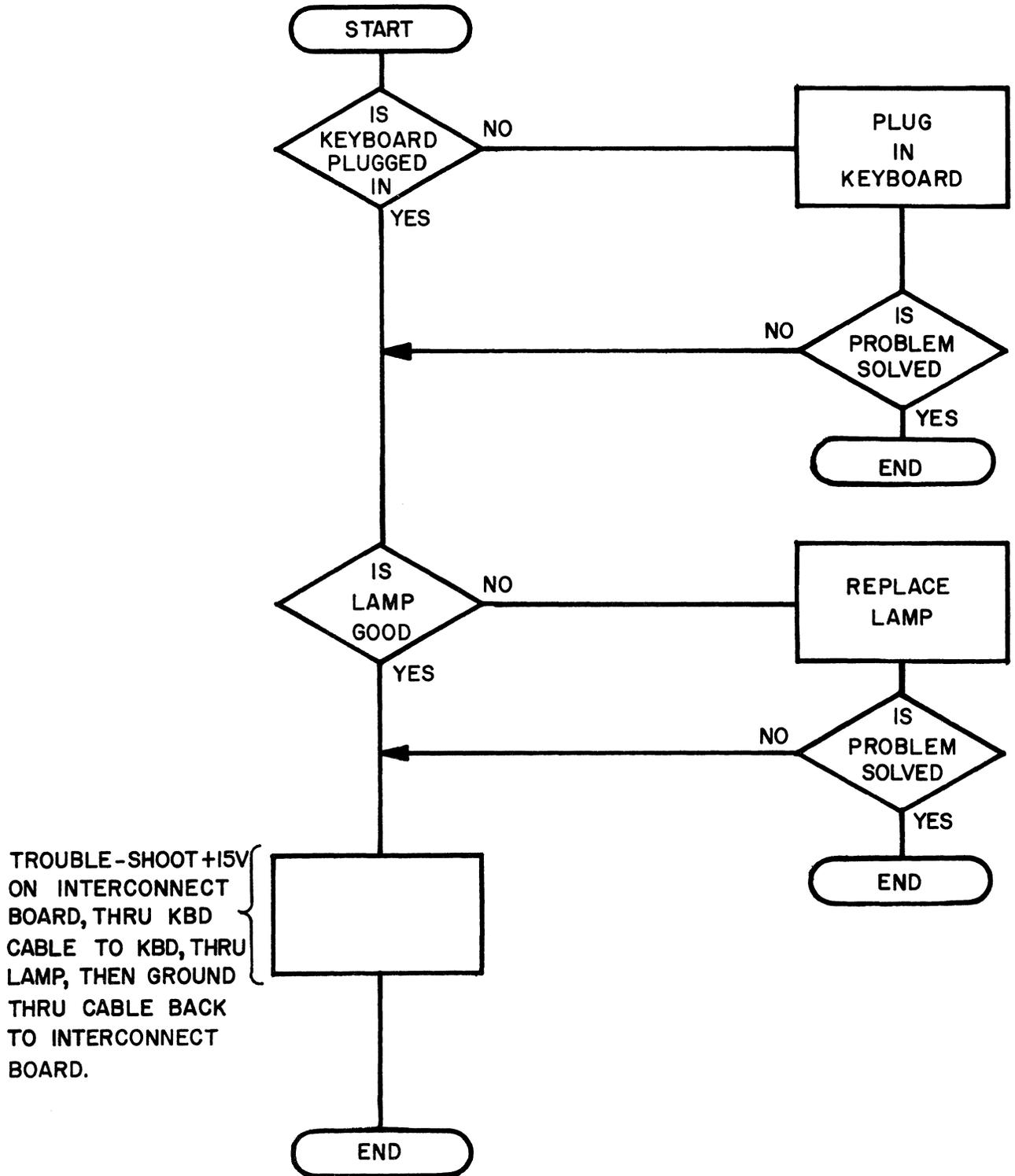
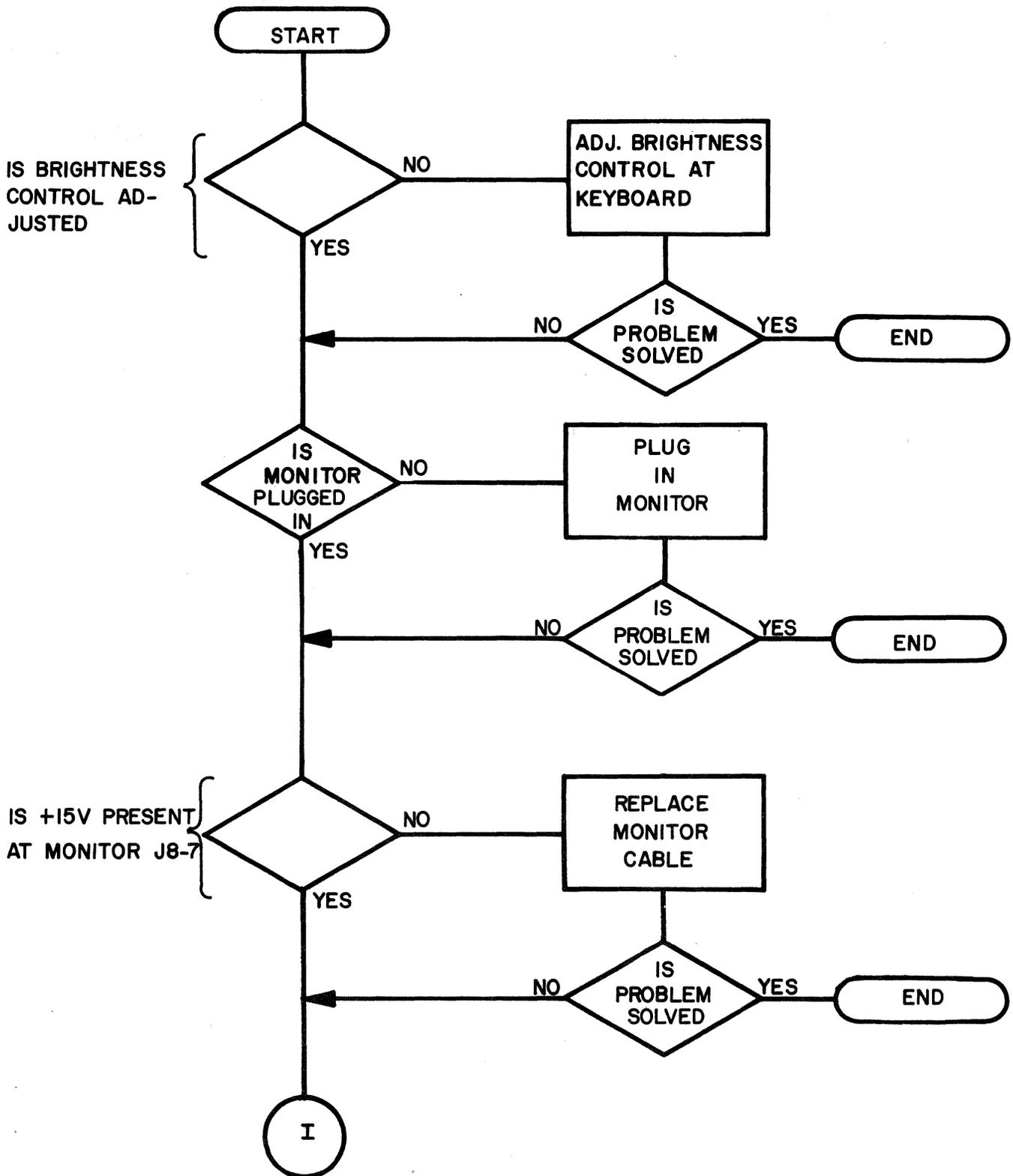


Figure 5-1. Echoplex Connector

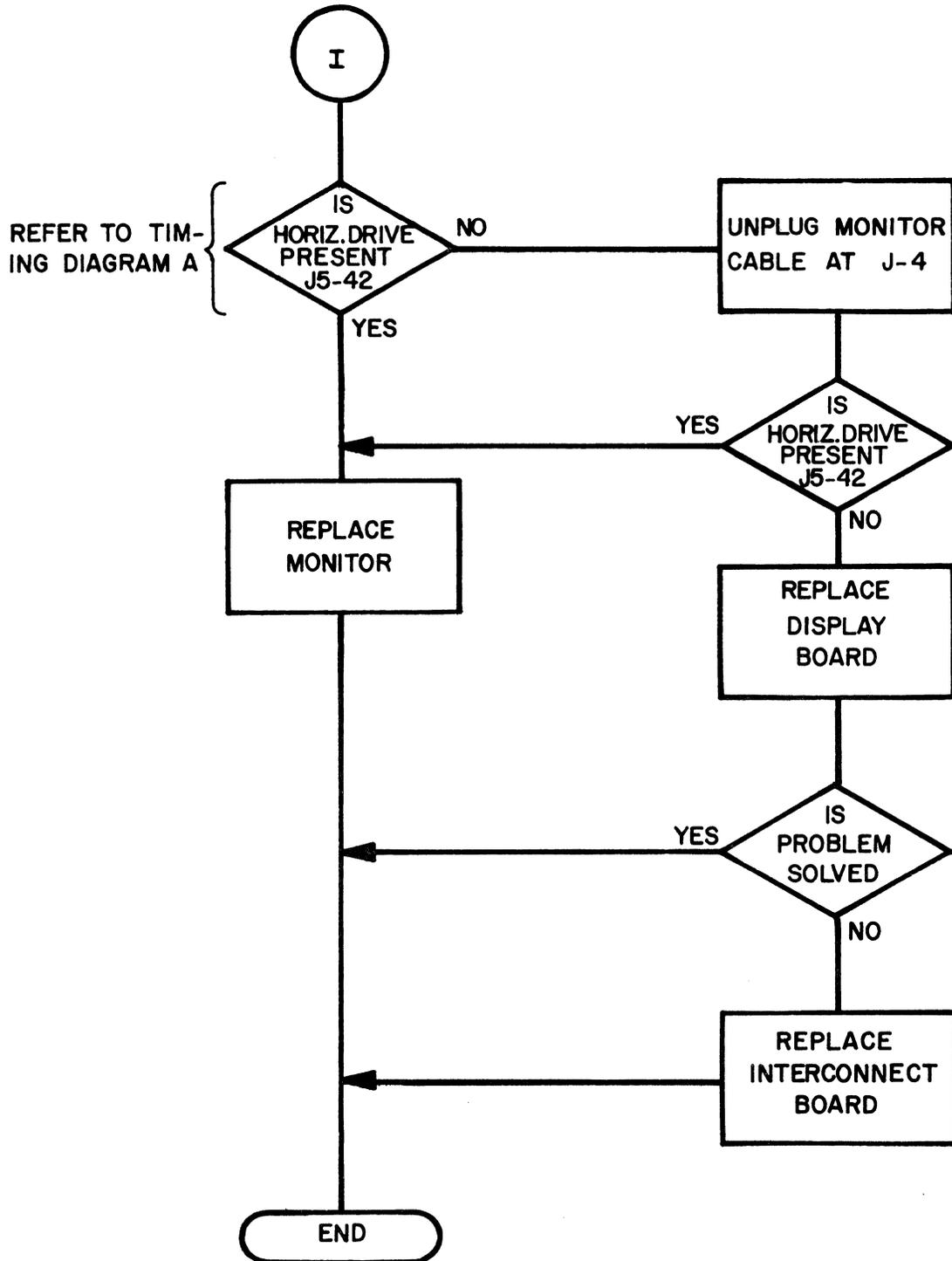
TABLE 5-1. TROUBLESHOOTING FLOW DIAGRAM INDEX (Continued)

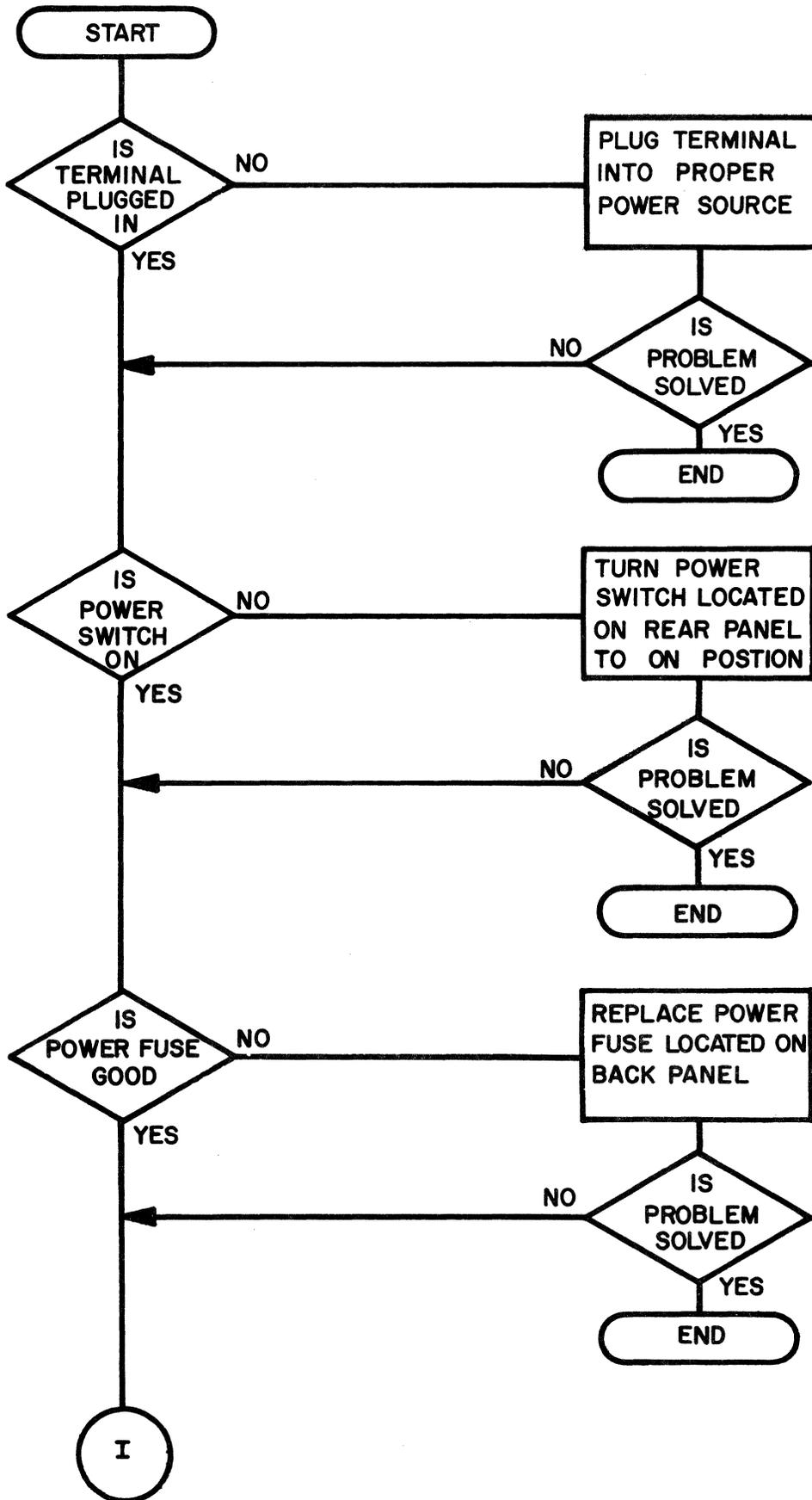
Apparent Failure	Troubleshooting Flow Diagram
OFF LINE	
1. Cursor not in the home position and random characters on screen or multiple cursors	5-2A
2. No character displayed when written nor cursor advance	5-2B
3. Wrong character displayed	5-2C
4. Improper escape functions	5-2D
5. Improper control function	5-2E
ON LINE	
1. No data being transmitted or received	5-3A
2. Transmits invalid data and/or improper parity	5-3B
3. Receives invalid data and/or improper parity	5-3C
4. No break function	5-3D
DISPLAY	
1. All displayed characters out of focus	5-4A
2. Rolling display	5-4B
3. Display too tall/short for screen size	5-4C
4. Height of displayed characters uneven	5-4D
5. Display too wide/narrow for screen size	5-4E
6. Display not centered	5-4F
7. Tilted display	5-4G
8. Others	
A. Single vertical line	5-4H
B. Physical damage	5-4H
C. Dot in center of screen	5-4H
D. Uneven intensity/Focus	5-4H
E. Burned phosphor	5-4H
F. Uneven display dimensions	5-4H
G. Excessive H. V. arching	5-4H
9. Remote video failure (Super Bee Display ok)	5-4J
MISCELLANEOUS	
	5-5A
	5-5B



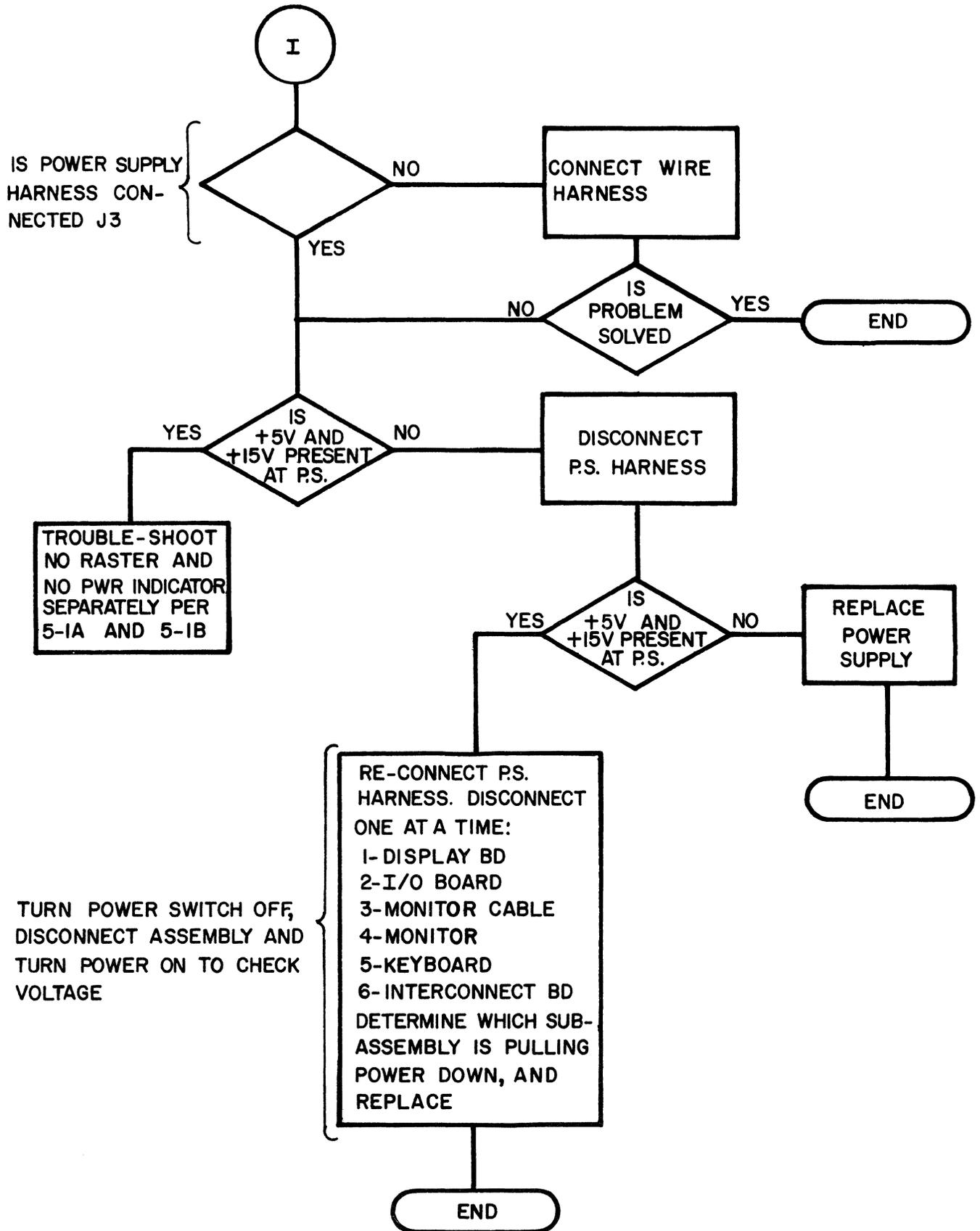


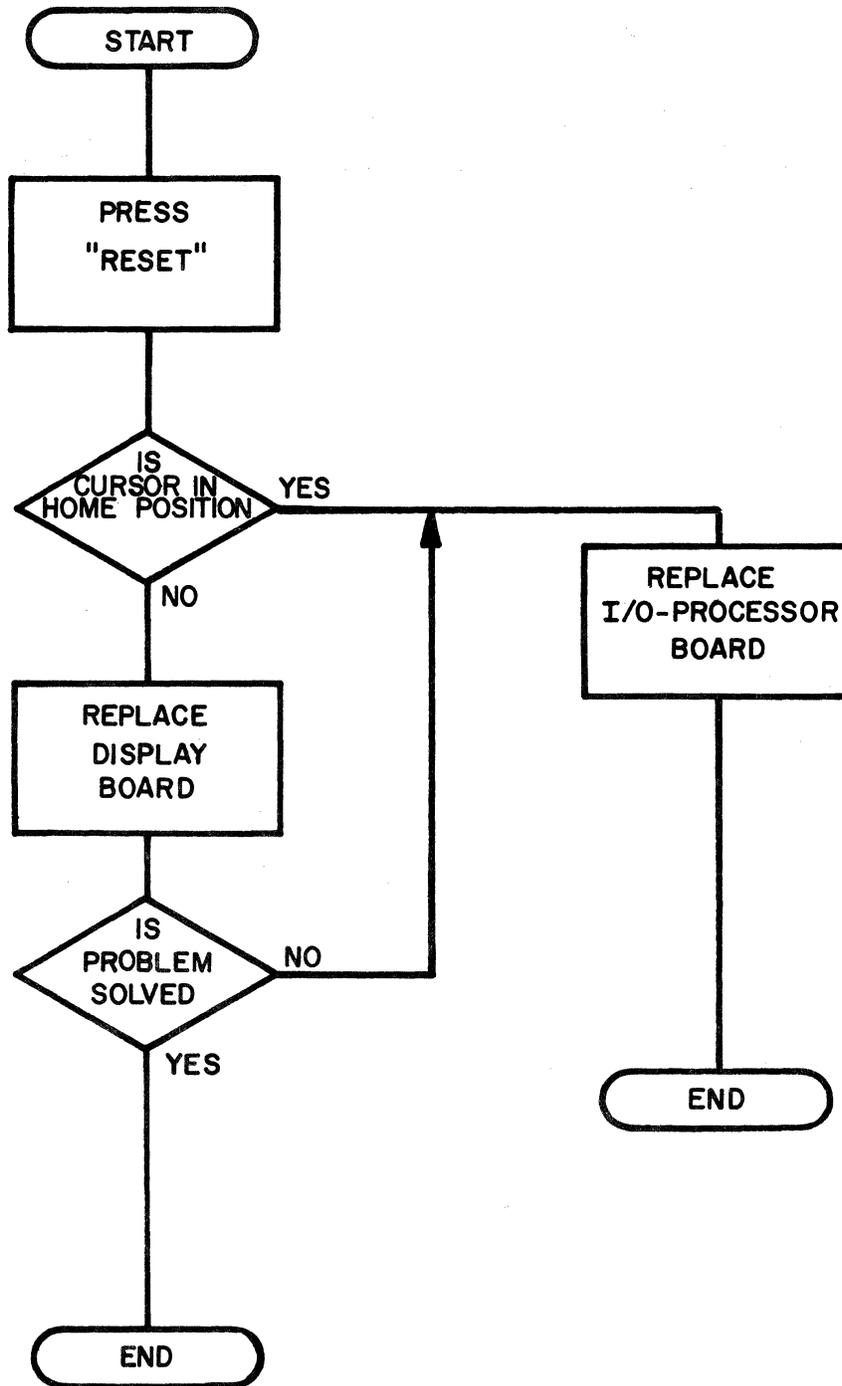
5-1B (CONT)

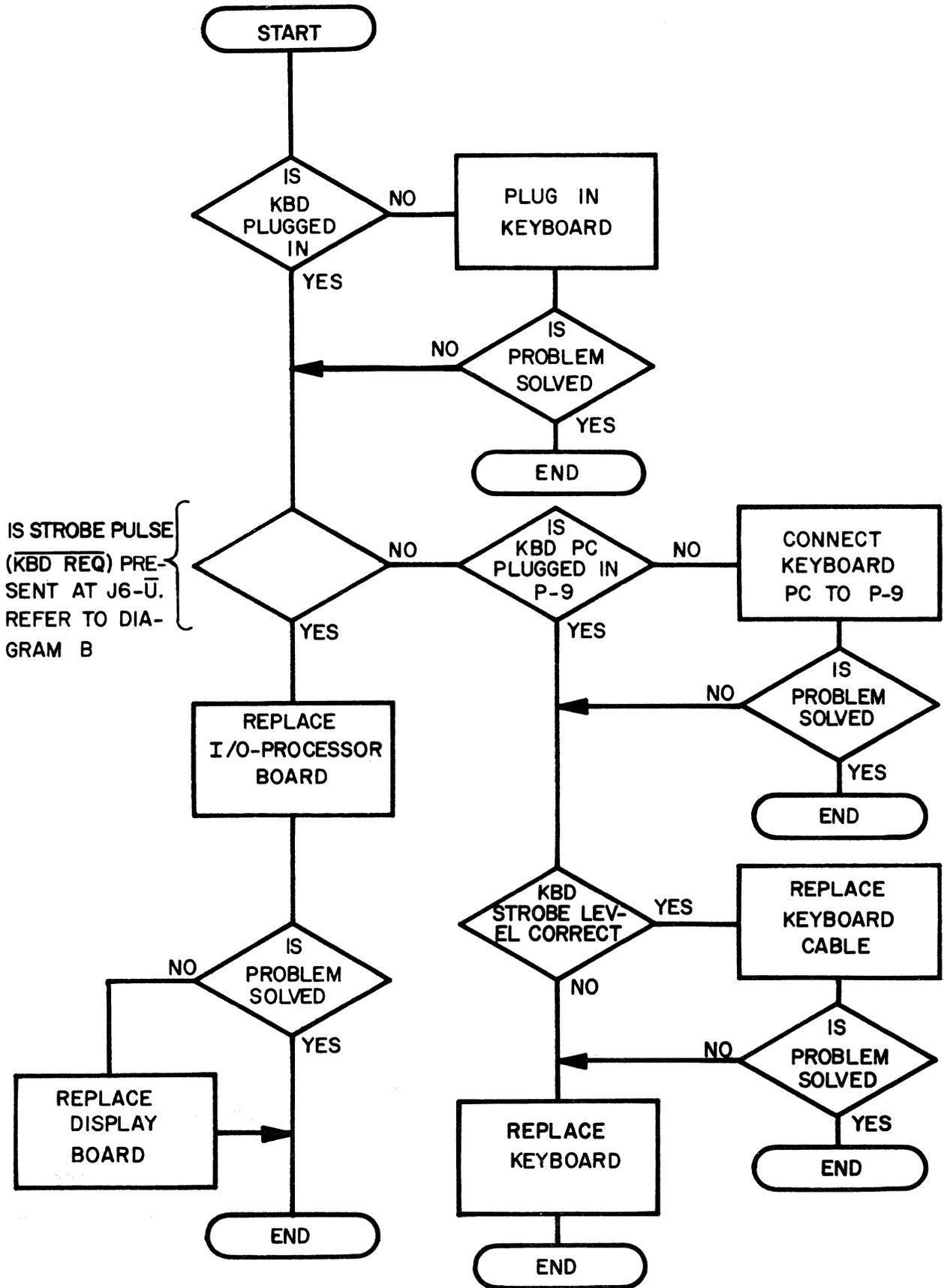




5-1C (CONT)

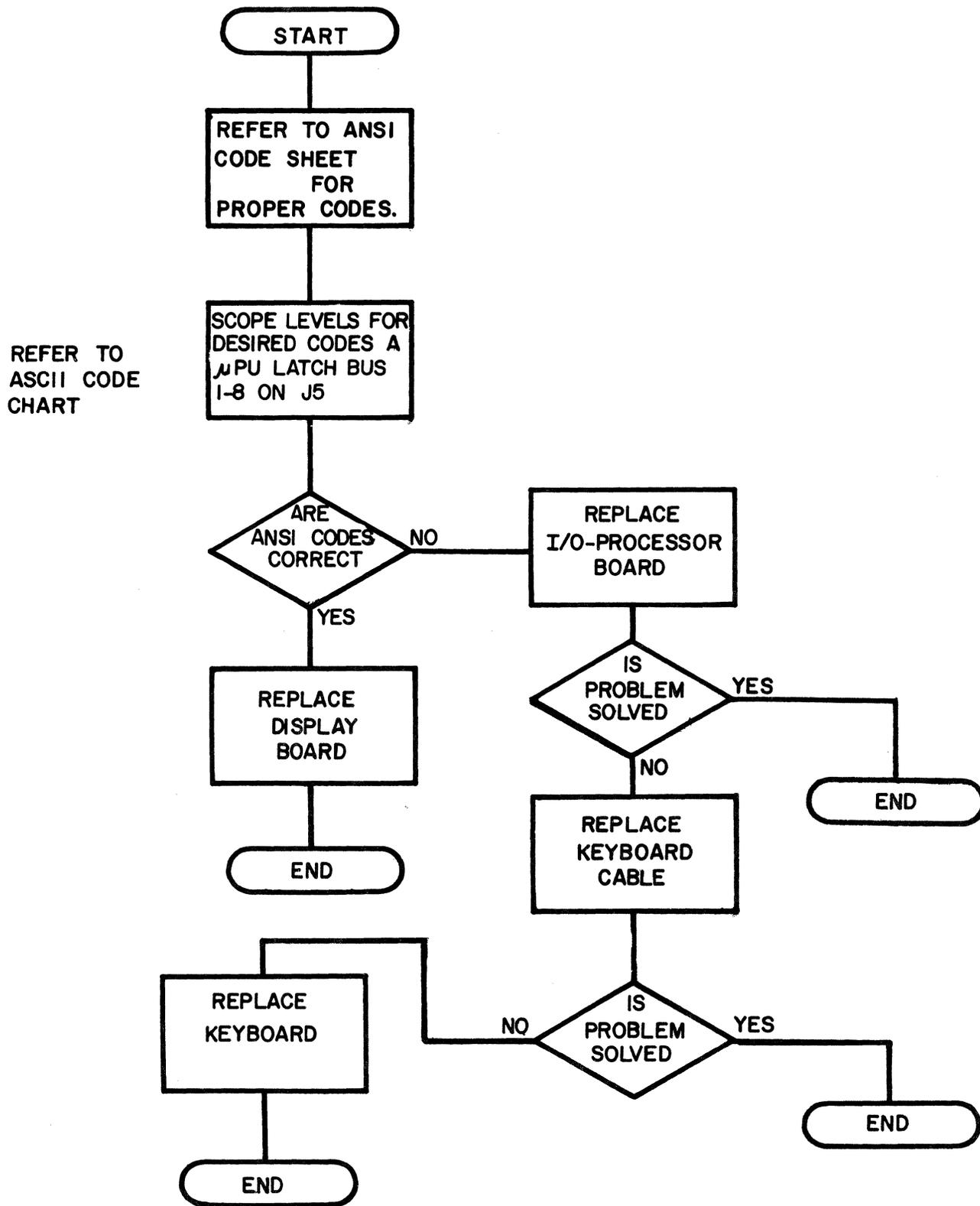




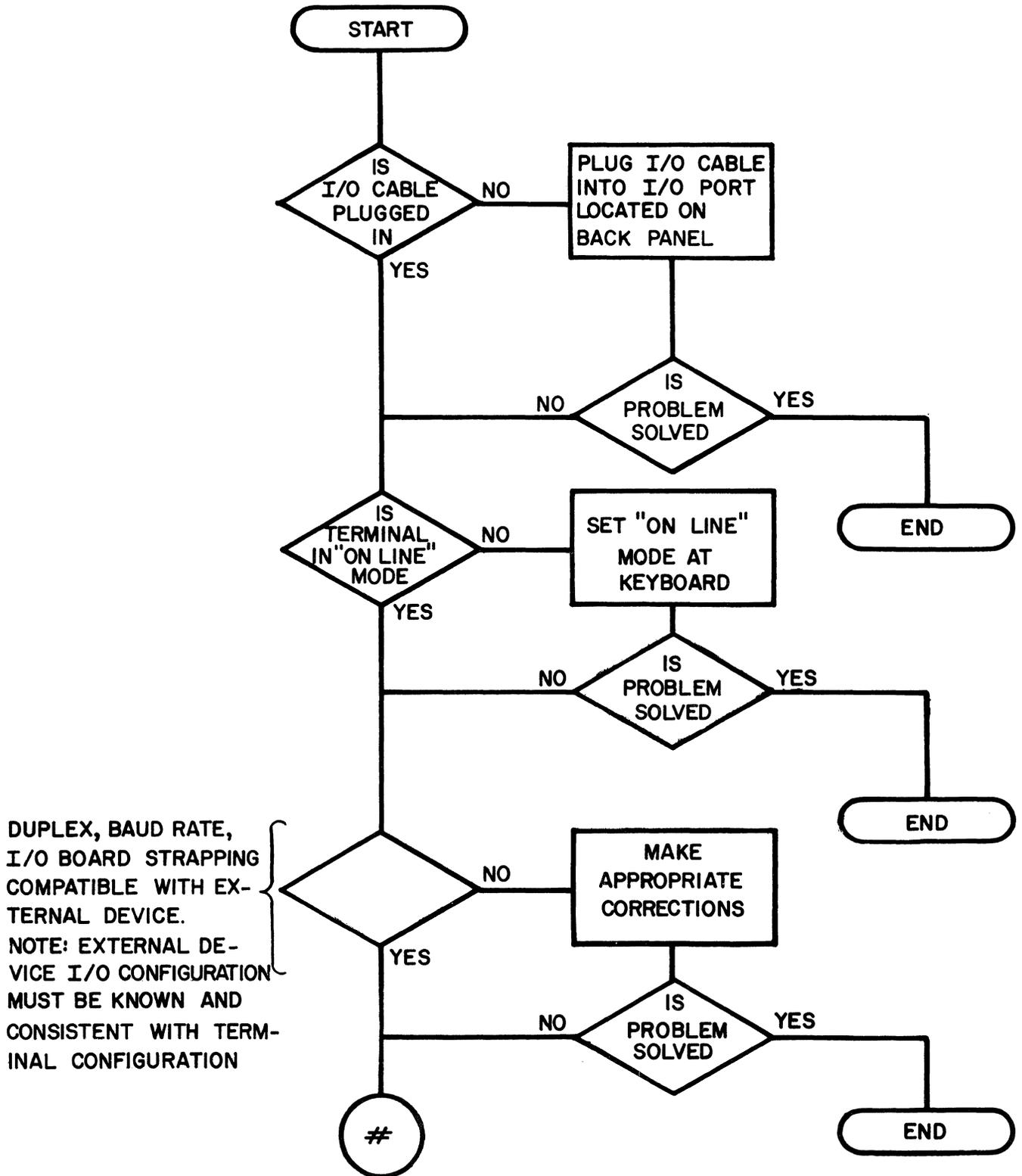


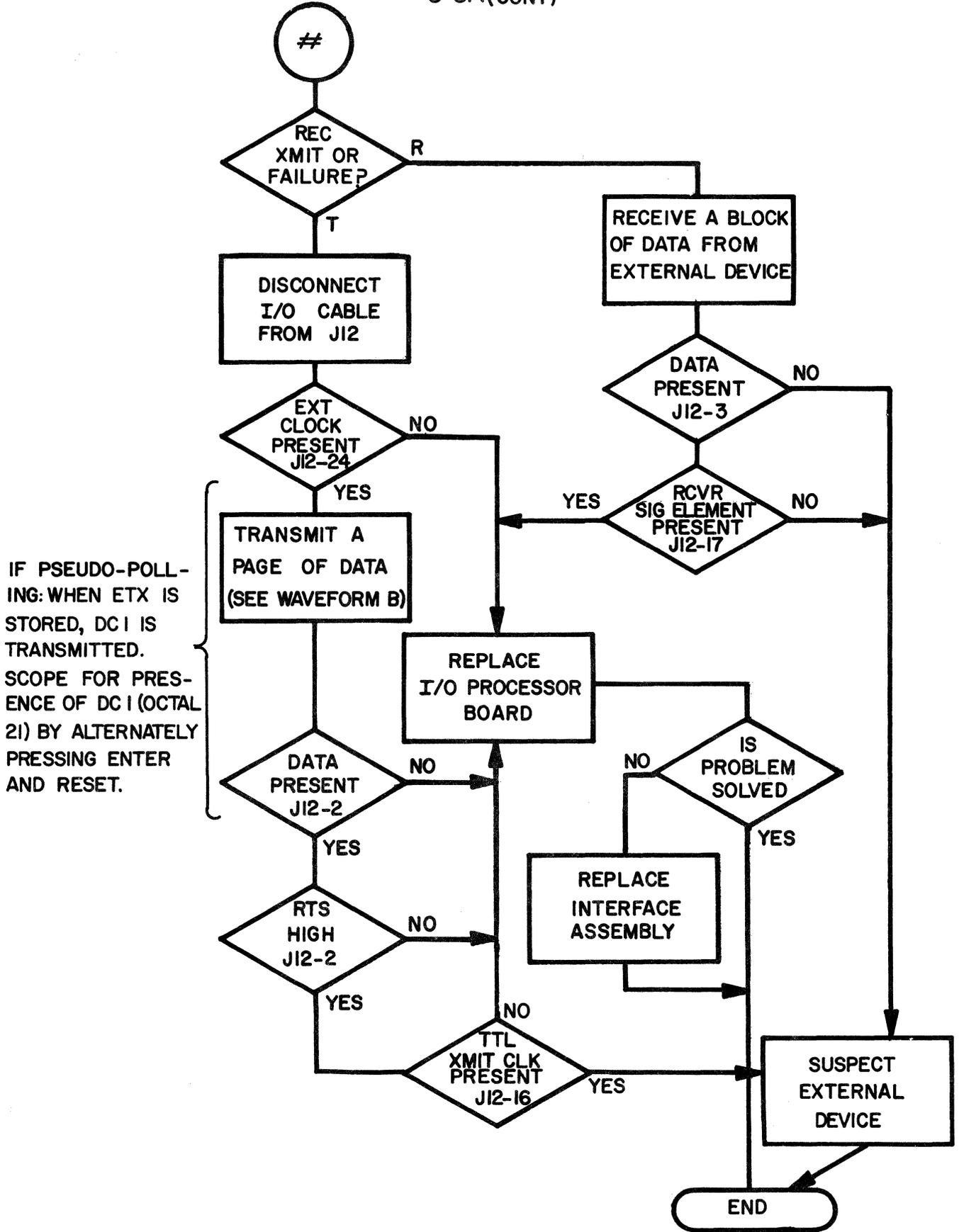
5-2C, 5-2D, 5-2E

PREREQUISITE FOR 5-2D AND 5-2E: VERIFY PROPER DISPLAY OF ALPHA-NUMERIC CHARACTERS.

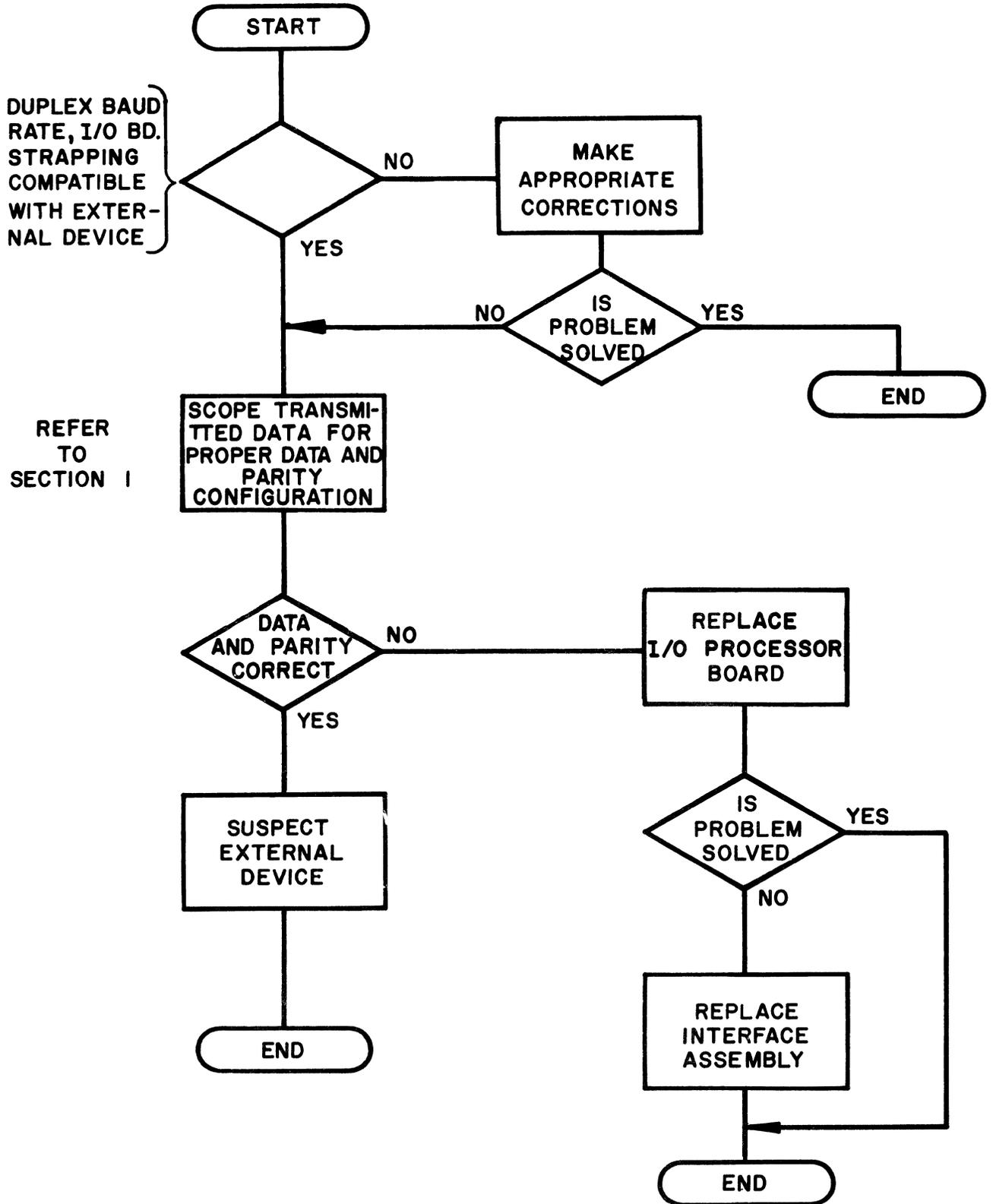


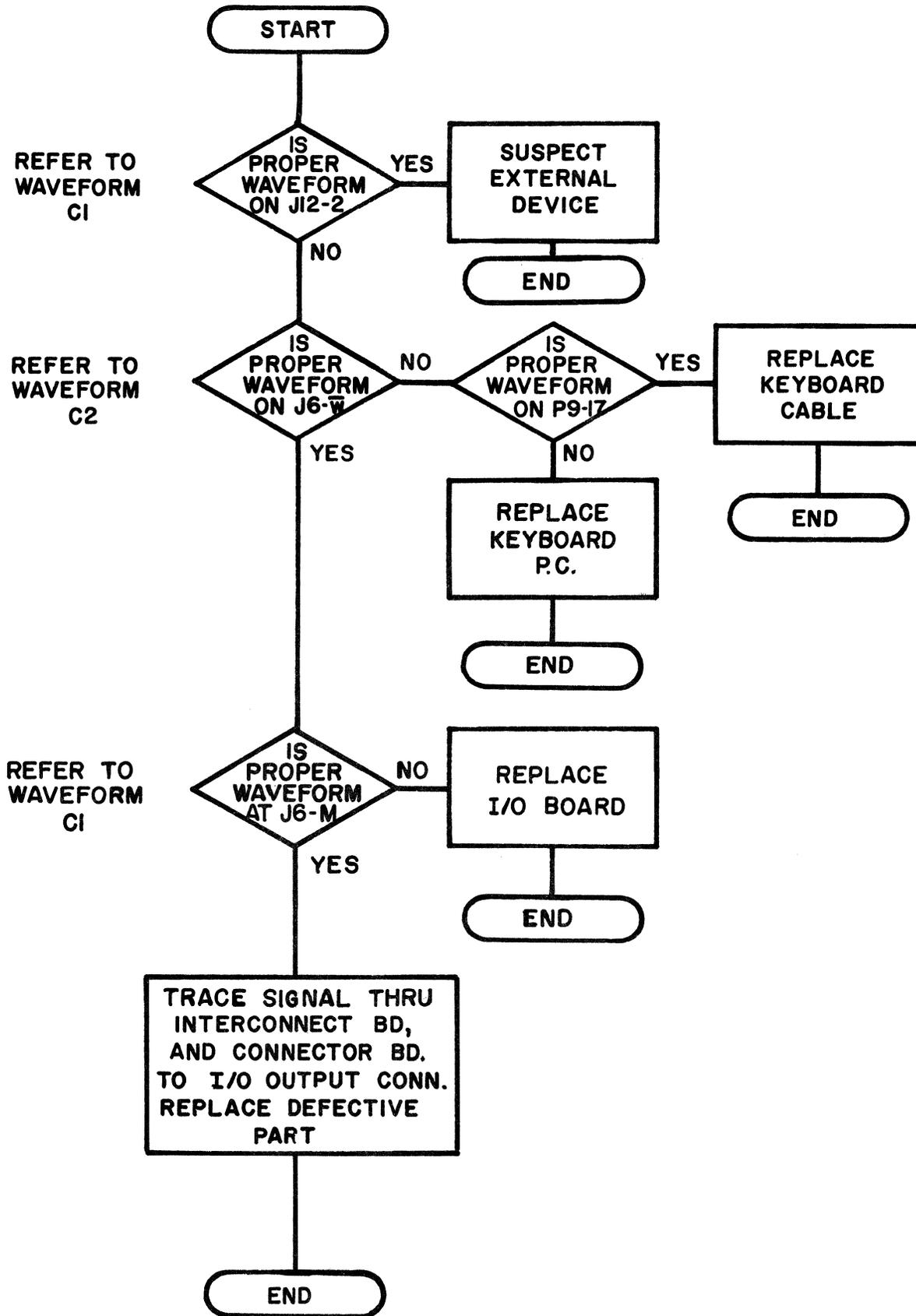
PREREQUISITE: VERIFY PROPER OPERATION OF THE TERMINAL IN "OFF LINE" MODE.

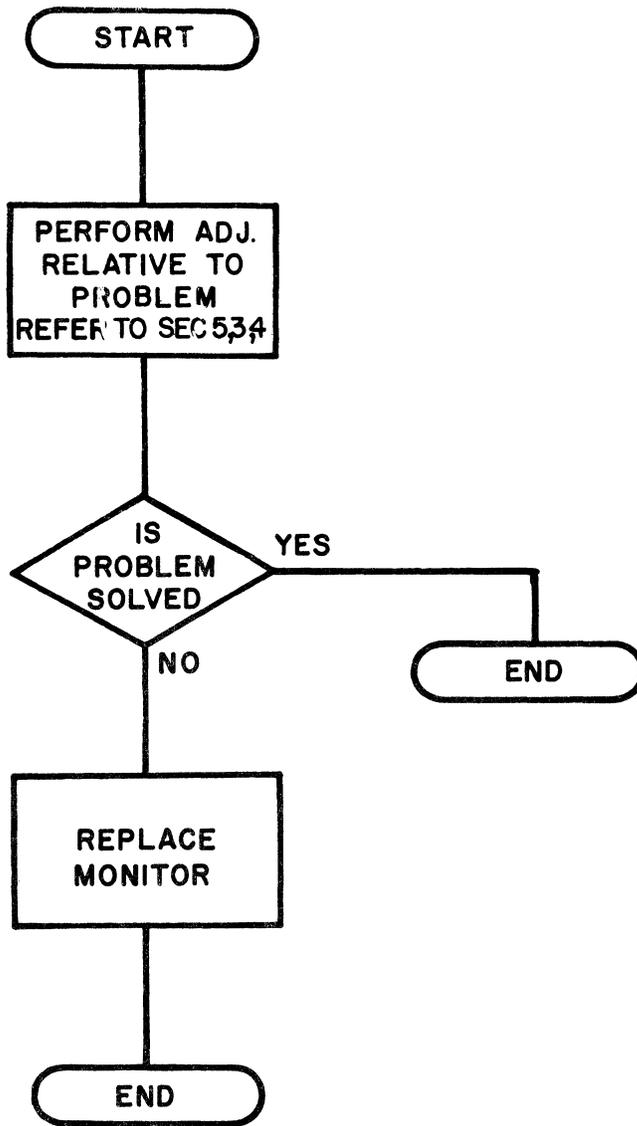


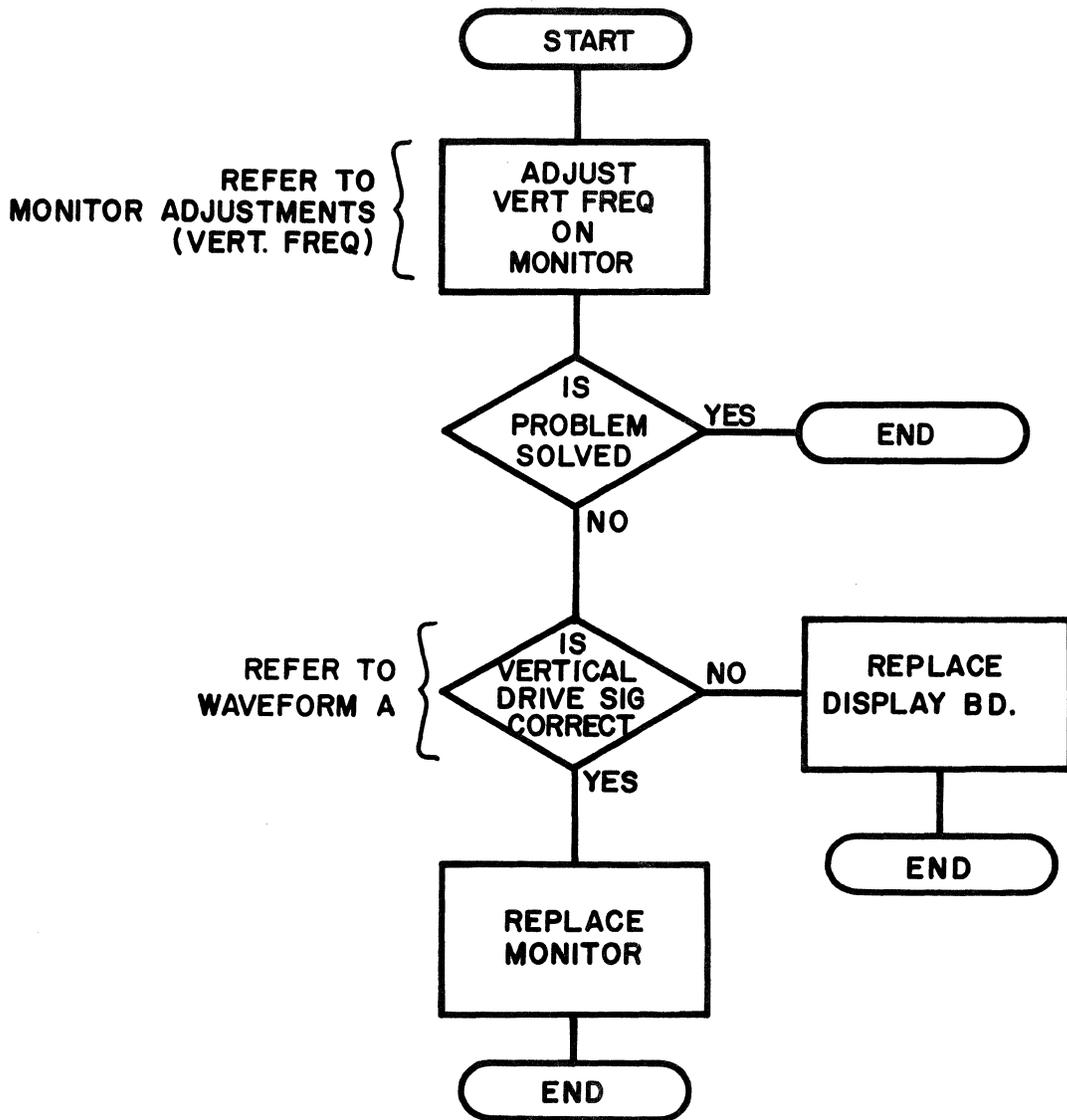


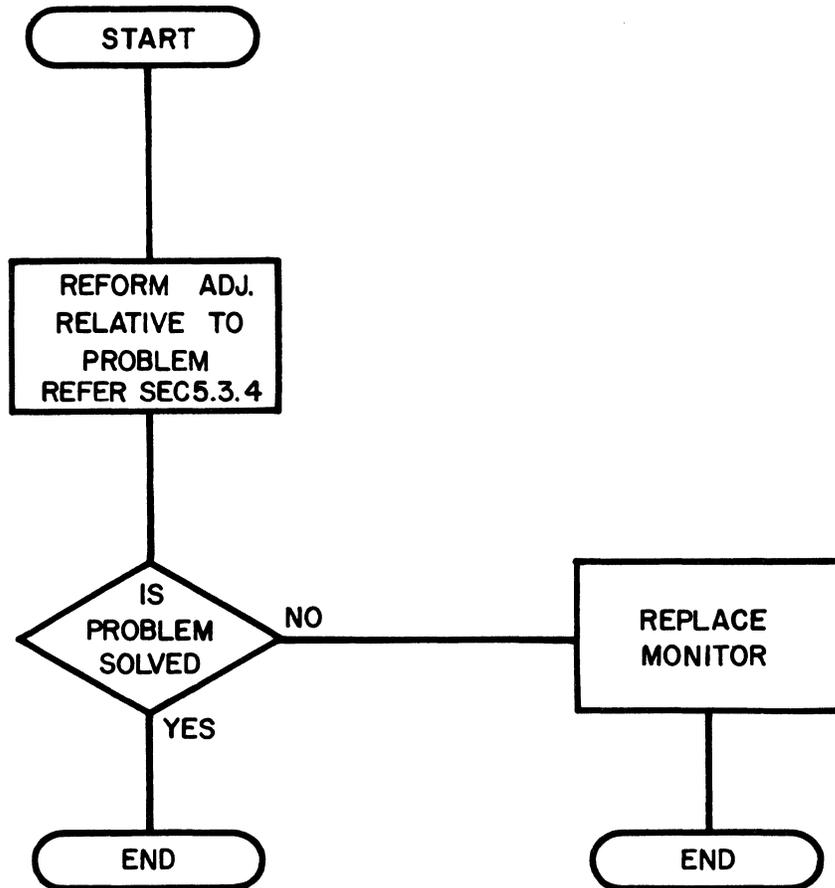
PREREQUISITE: VERIFY PROPER OPERATION OF TERMINAL IN "OFF LINE" MODE.



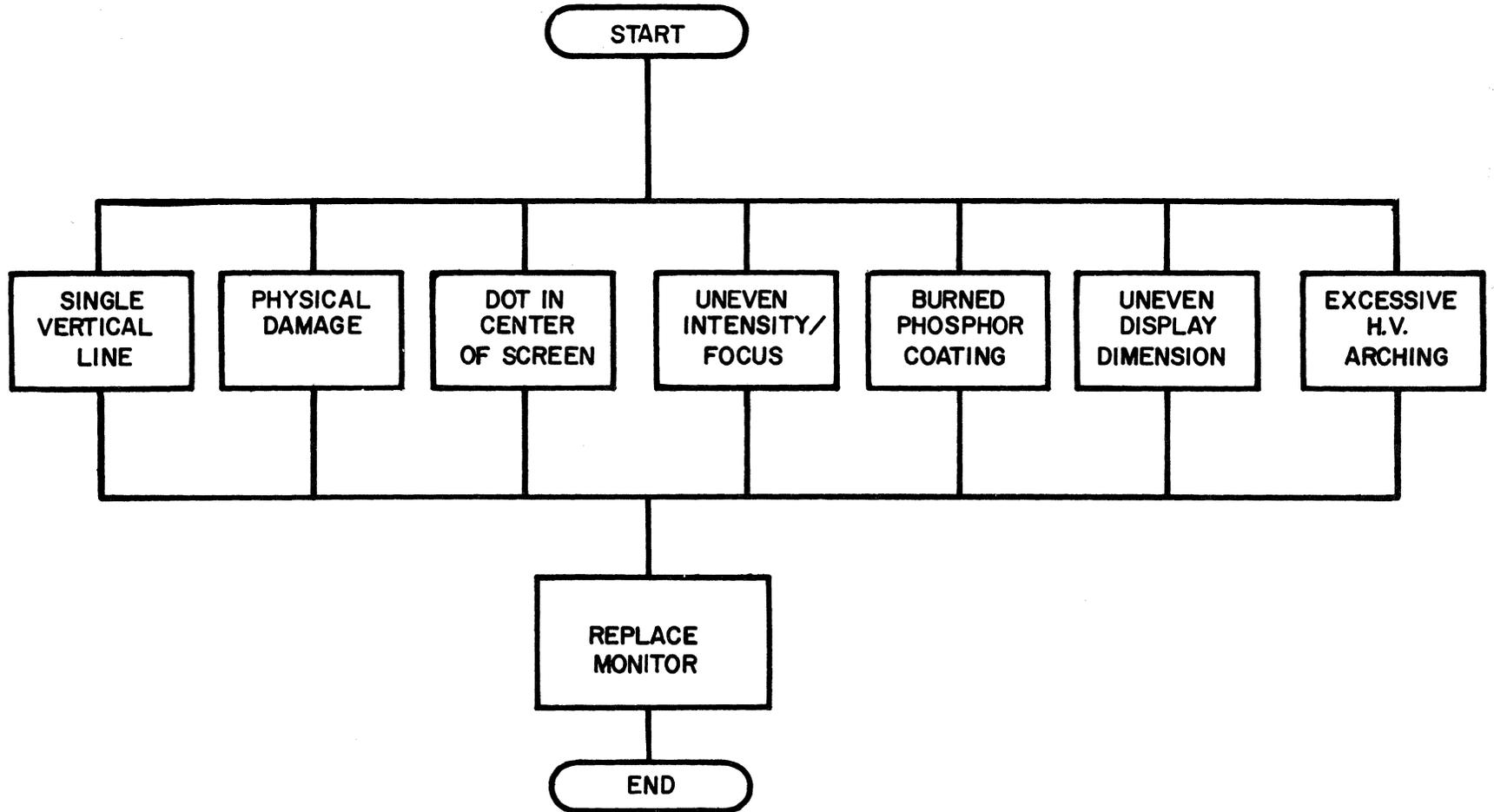


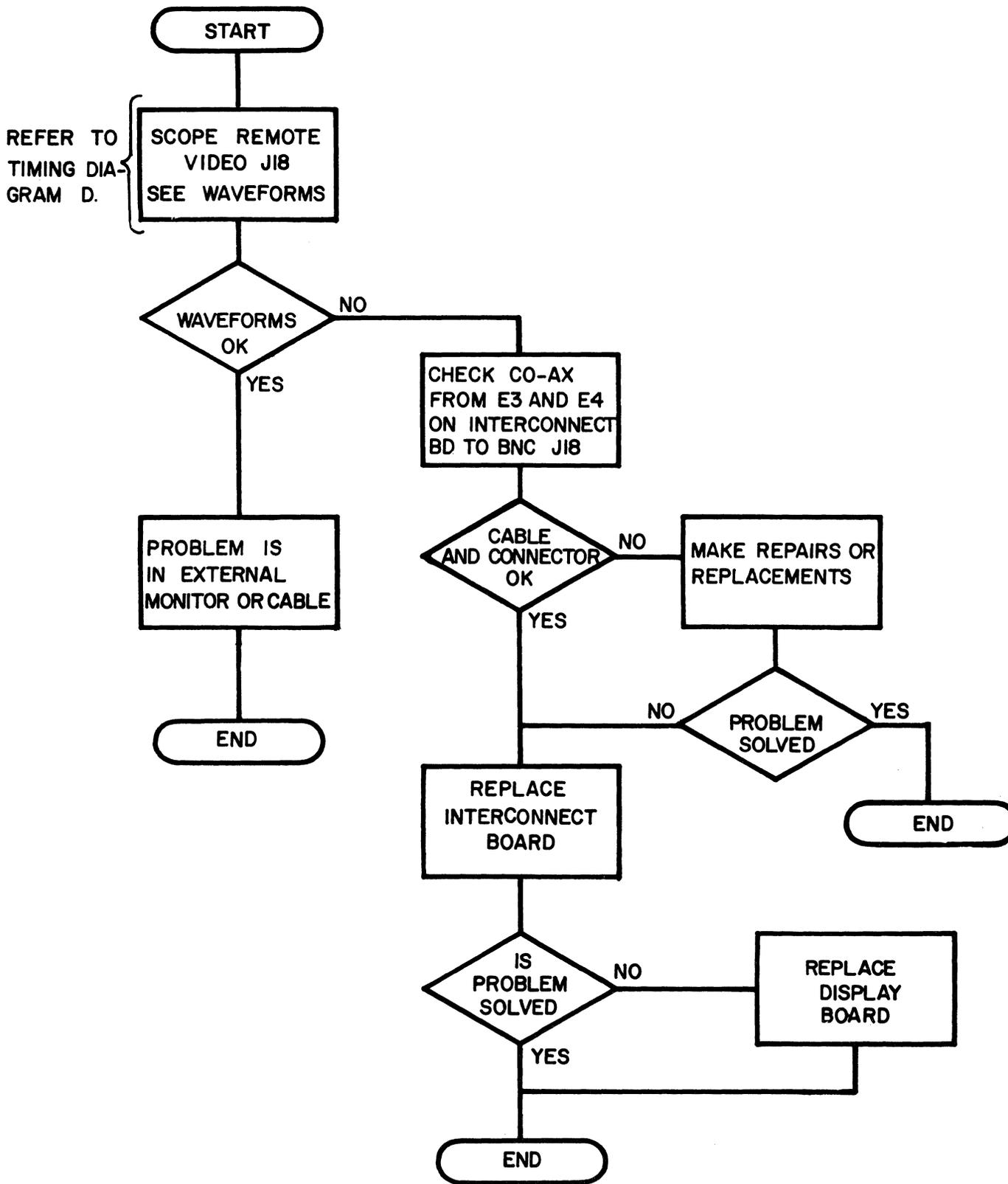




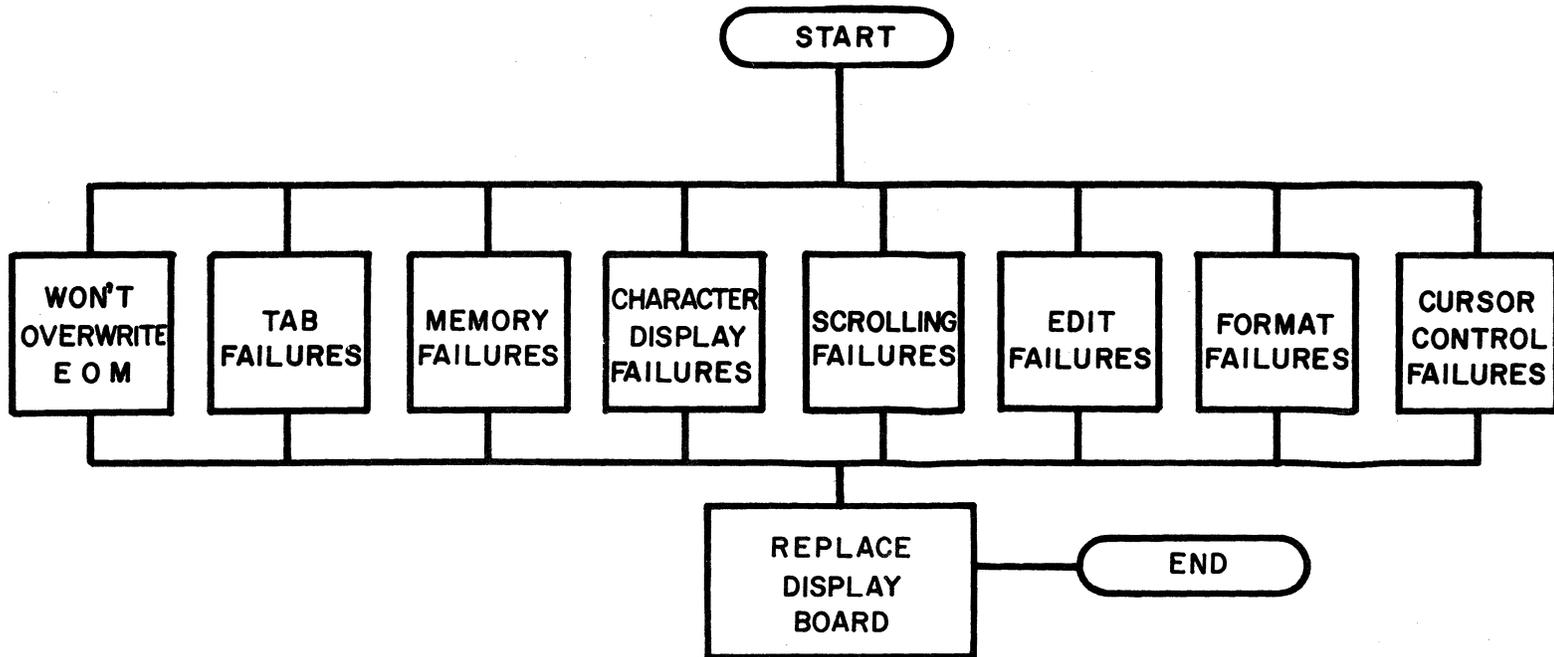


5-20



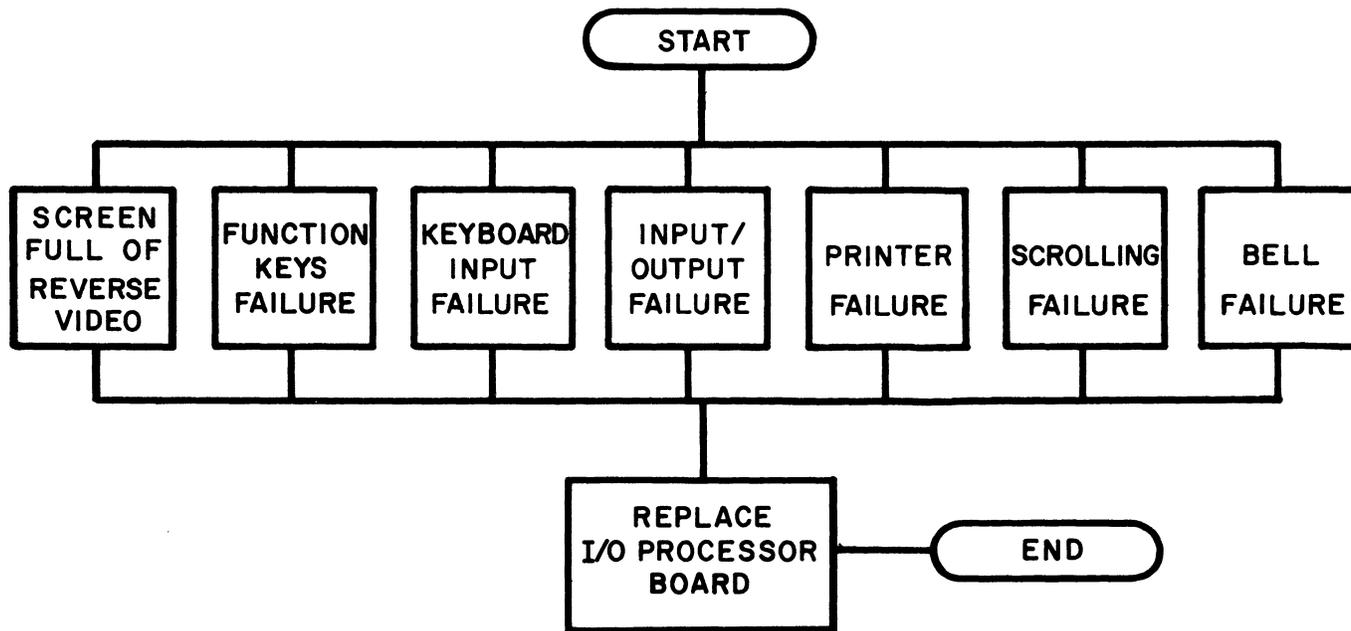


5-22



5-5A

This is an attempt to group various functional failures under the most probable circuit board the defect may be located in.



This is an attempt to group various functional failures under the most probable circuit board the defect may be located in.

5.3.4 Adjustment Procedures

Power Supply Adjustments

The Power Supply for the SUPER BEE is now available from a second source, Scintillonics Inc. Though identical in form, fit and function, some variations in adjustment exist. Detailed data on the Scintillonics Power Supply is provided in Appendix C.

To adjust the +5 Vdc voltage level, the meter should be connected between point A of Figure 5-2, and a good chassis ground. The voltage at this point should be +5 Vdc \pm 0.2V. If it is not, rotate the adjustment lug on R7 (point B) until the voltage is within specified limits.

To adjust the +15Vdc voltage level, connect the meter between point C and a good chassis ground. The voltage at this point should be +15 Vdc \pm 0.2V. If it is not, rotate the adjustment lug on R17 (point D) until the voltage is within specified limits.

To adjust the -12 Vdc voltage level, connect the meter between point E and a good chassis ground. The voltage at this point should be -12 Vdc \pm 2V. If it is not, rotate the adjustment lug on R27 (point F) until the voltage is within specified limits.

The overload protection adjustment is aligned and clamped at the factory and should not be changed. However, adjustment can be made by connecting the meter between point G and a good chassis ground and should read approximately 3 Vdc. The desired setting should be obtainable by rotating the lug on R33, point H.

Monitor Adjustments

The following adjustments should be made while the monitor is in the SUPER BEE Terminal.

The adjustment described here are in reference to Figure 5-3 and 5-4, and consist of the following sections:

- Brightness
- Contrast
- Vertical Adjustments
- Horizontal Adjustments
- Focus
- Centering

Figure 5-3 shows the physical location of the specific adjustments on the Monitor PC board, while Figure 5-4 shows the CRT mounted adjustments.

WARNING: The Monitor employs high voltages. Care should be used in making any adjustments as power will be applied to the Monitor.

The brightness control (located on the SUPER BEE Keyboard assy.) should be positioned to a point where the white raster on the CRT is extinguished. Fill the screen of the CRT with characters from the Keyboard (i.e., all E's) and adjust the contrast control for the sharpest display of the characters in the upper left hand side of the screen.

The vertical frequency control R 116 (Figure 5-3) is set to the approximate mechanical mid-point initially. This adjustment will correct for a rolling display and should be adjusted to correct that symptom alone. No discrete measurement is necessary, except for a visual observation as to the steadiness of the display.

Fill the screen once again with characters if none exist. The vertical height control R 124 (Figure 5-3) should be adjusted 6½ inches from the top of the characters on the first row to the bottom of the characters on the last row in the center of the display.

The vertical linearity control R 121 (Figure 5-3) should be adjusted so the characters on the first row are equally as tall as the characters on the last row. Their height should be approximately 0.18 inches.

If the screen is blank, fill it with a character and adjust the horizontal width coil L 101 (Figure 5-3) for 7½ inches from the left margin to the right margin of the displayed characters.

The horizontal linearity is adjusted to correct for the compression of the display on the left hand side of the screen. To correct this, loosen the clamp securing the yoke and slide the cardboard sleeve (horizontal linearity sleeve, refer Figure 5-4, point D) in or out to give uniform width to the characters on the right and left-hand borders of the display.

Adjust the Focus control R 107, Figure 5-3, for best over-all display focus. It may be necessary to readjust the contrast control and repeat this step.

Centering of the display is accomplished by rotating the tabbed ring magnets on the CRT behind the deflection yoke, refer to Figure 5-4 points A

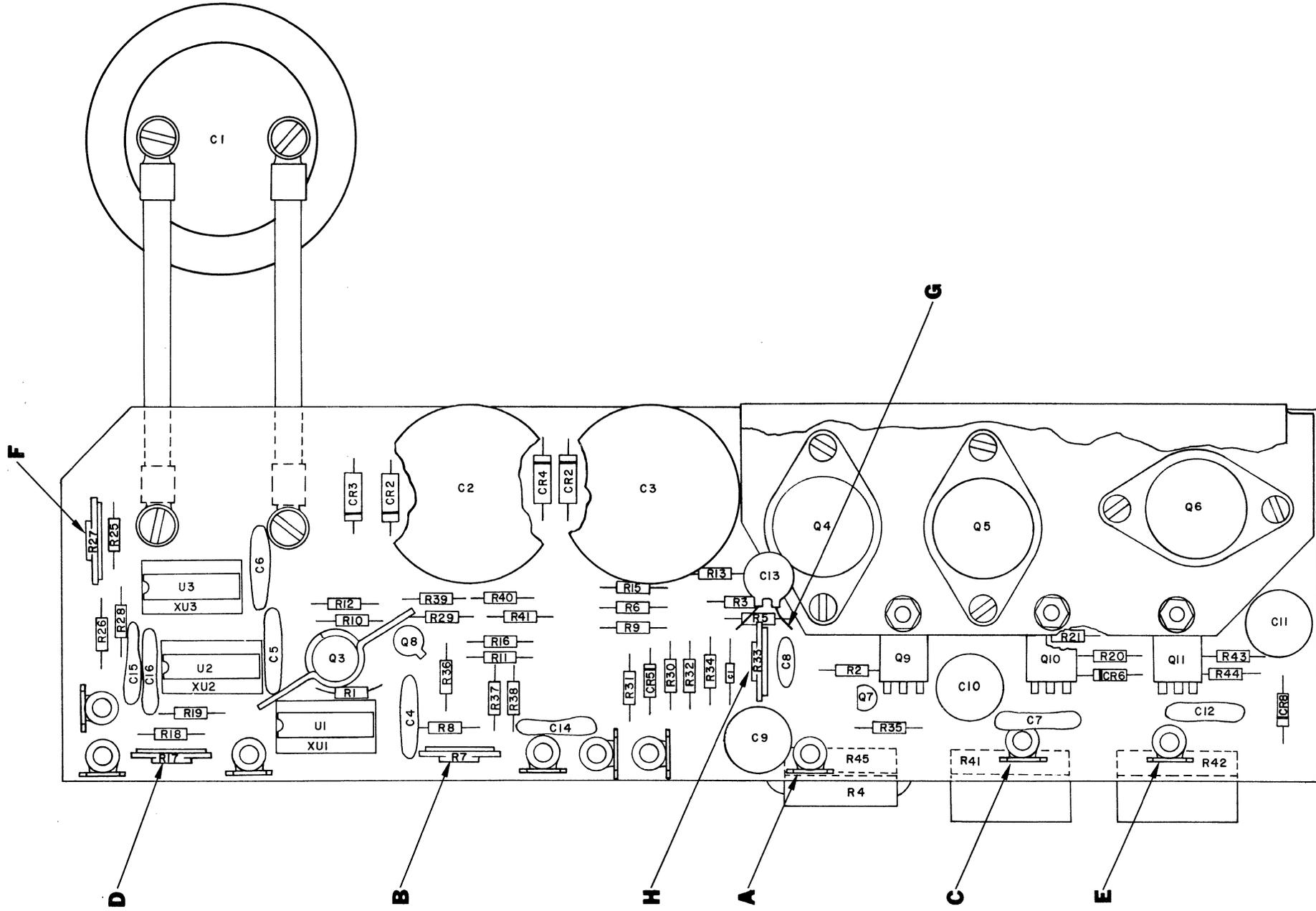


Figure 5-2. Power Supply Adjustments

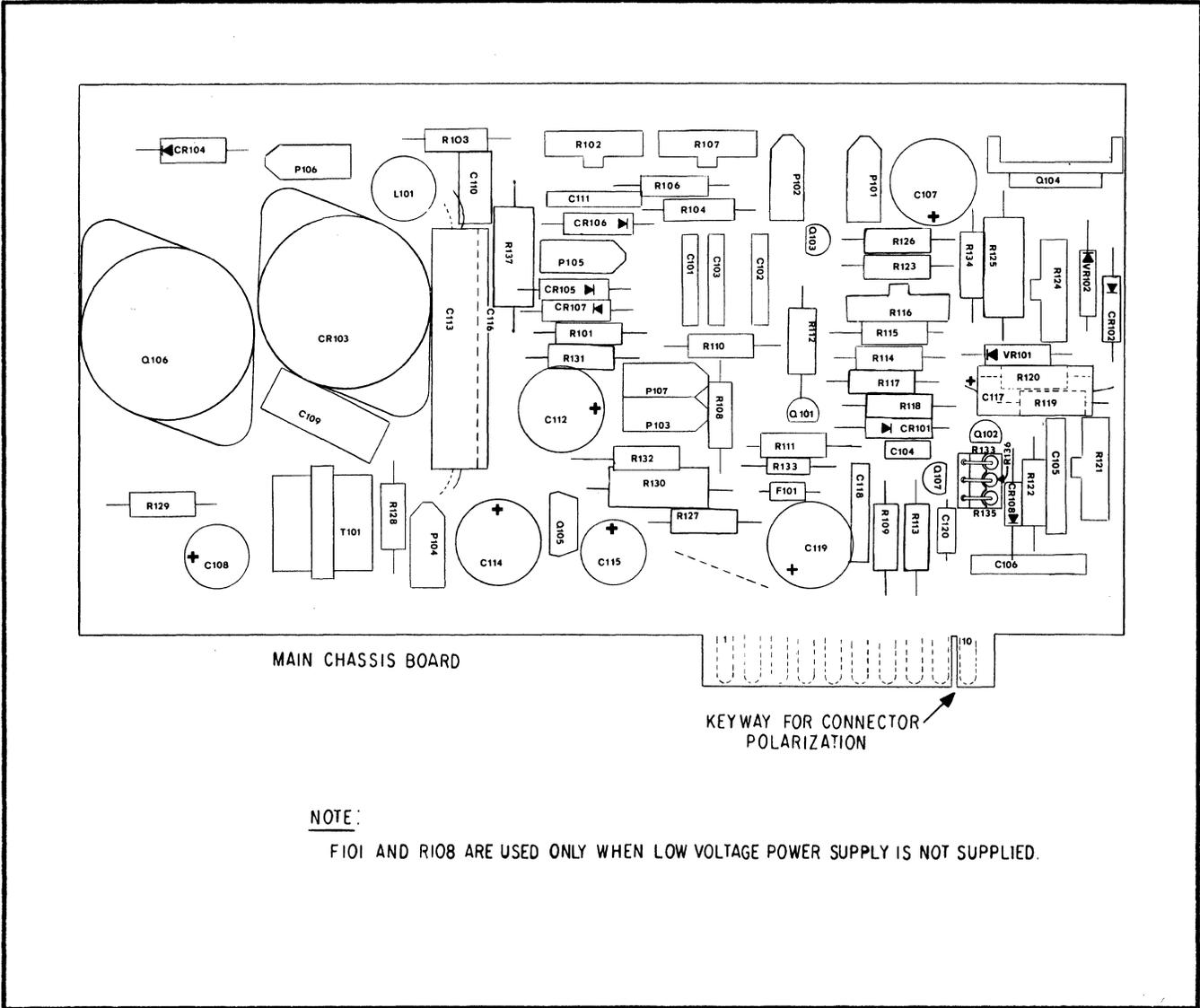


Figure 5-3. Monitor P.C. Card Adjustments

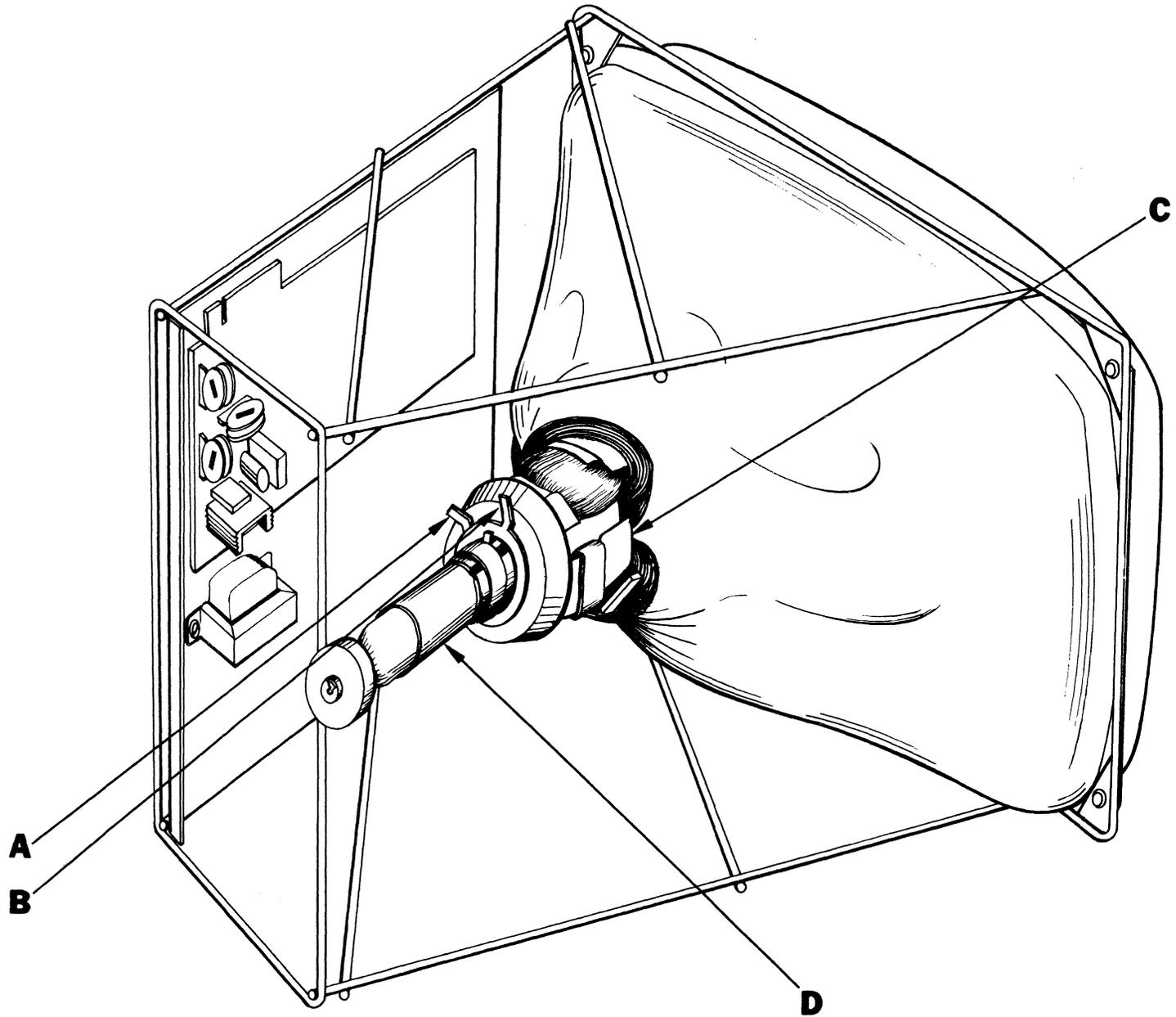


Figure 5-4. Monitor Yoke Adjustments

and B. If the display as a whole is tilted, correction may be accomplished by rotating the entire yoke, point C.

Keyboard Adjustment

The keyboard requires no adjustment. If there is an apparent failure, refer to Section 5.3.3 of this manual.

Super Bee I/O Processor and Display Board Adjustment

The only adjustable components on the SUPER BEE I/O Processor and Display Boards are associated with specific operation to be performed by the terminal. If there is an apparent failure, refer to Section 5.3.3 of this manual.

5.3.5 Removal and Replacement Procedures

The procedures presented here are disassembly steps. To assemble the SUPER BEE, these procedures should be executed in the reverse order. Before attempting any internal disassembly, it is advisable to remove both the I/O Processor Board, Display Board, Keyboard interconnection cable and disconnect power cable.

WARNING: These Procedures should not be attempted with any electrical power connected or terminal circuits energized.

Cover Removal

1. Remove the six No. 6 bolts attaching the cover to the chassis; three bolts on the right and three on the left.
2. Lift the cover up and off the terminal.

I/O Processor Board and Display Board Removal

1. Remove two bolts attaching the circuit card retainer to the card housing (card cage) and remove retainer.
2. Grasp the card extractors on the exposed end of either card and pull card firmly.
3. Stow the card in an area protected from further disassembly activity.
4. Repeat steps 2 and 3 on second circuit board.

Power Supply Removal

1. Turn the terminal upside down, placing it

on a protected surface (i.e., carpet or pad).

2. Remove seven (No. 6) bolts in the sides of the base, disconnect fan plug and lift off bottom cover.

3. Remove four large (No. 8) bolts in front left corner (looking front to back); holes are provided through base and frame.

4. Turn terminal right side up.

5. Remove connectors P3 and P4 from Interconnect Board. Screw driver may be used to separate connection.

6. Cut and remove cable ties securing Power Supply and Monitor cables, move Monitor cable clear of Power Supply.

7. Remove two bolts attaching Interconnect Board to Power Supply; located on front edge of circuit board.

8. Slide Power Supply forward and out (counter clockwise) sufficient to allow access to the power plug at bottom right.

9. Disconnect power plug and remove Power Supply from terminal.

Monitor Removal

1. Remove the edge (J-12) connector from the Monitor circuit card located on the top of the Monitor assembly by removing the two holding clamps at each end of the connector and pull the connector away. Look inside the edge (J-12) connector and ensure the polarity key is intact and in position.

2. Turn the terminal so the face is toward you.

3. Remove the plexiglass face and the bezel by pulling it directly out from the terminal

4. Remove the four bolts which connect the front plate to the Monitor, remove the front plate and spacers. Bolts may be temporarily replaced to hold CRT while completing disassembly. On 15-inch CRT terminals, remove 4 bolts mounting monitor mounting plate to supports and lift out Monitor.

5. With the terminal front to your right, locate two bolts on the lower edge of the Monitor circuit board, one on each side of the Monitor identification plate; Remove these bolts.

6. Lift the Monitor assembly directly away from the terminal.

NOTE: A replacement Monitor is shipped with four bolts holding CRT in its frame. These bolts must be removed and replaced by the longer bolts and spacers when mounting in terminal.

Interconnector Board Removal

1. With the terminal front on your left, locate and remove six bolts along right side of circuit board; two rows of 3 each.

WARNING: Caution must be taken not to remove two bolts holding heat sink assembly.

2. Remove two small screws in chassis frame directly below Interconnect Board. Screws must be removed carefully such that the spacers and connector Jack (J7) remain attached to circuit board.

3. Rotate top of Interconnect Board to the left and lift the board out of the chassis sufficient to allow access to the two connectors at the bottom of the board and to cable to video connection (J18).

4. Disconnect two connectors from Interconnect Board connectors (P1 and P2), un solder connection of video cable at lower right corner and remove board.

NOTE: Care must be used in removing Interconnect Board to avoid damaging speaker attached to the board.

Fan Removal

1. Turn terminal upside down on a protected surface.

2. Remove 7 bolts (No. 6) attaching bottom cover to base.

3. Lift bottom cover, disconnect fan connector (J14), and lift off bottom cover and fan assembly.

4. Remove 4 bolts (No. 6) attaching filter, finger guard and fan to bottom cover.

5. Remove Fan assembly.

Interface Assembly Removal

1. Turn terminal on its side or top.

2. Remove the 4 bolts through chassis into Interface Assy.

3. Turn top of Interface Assy inward and toward chassis bottom and list assembly away from terminal.

Keyboard Circuit Board Removal

1. With Keyboard cable disconnected from terminal, turn Keyboard upside down on protected surface.

2. Remove three locknuts located in holes along front edge using nut driver.

3. Turn Keyboard rightside up, lift front of Keyboard circuit board assembly up and pull forward.

4. Remove Keyboard circuit assembly from housing. Remove connector P28 from circuit board edge connector.

5. To remove and/or replace Keyboard cable assembly, cut cable tie inside housing and remove cable.

6. To remove Keyboard circuit board, remove seven bolts around outside of board

NOTE: Caution must be used to not remove two bolts attaching brightness potentiometer on right rear of board (looking at bottom of assembly).

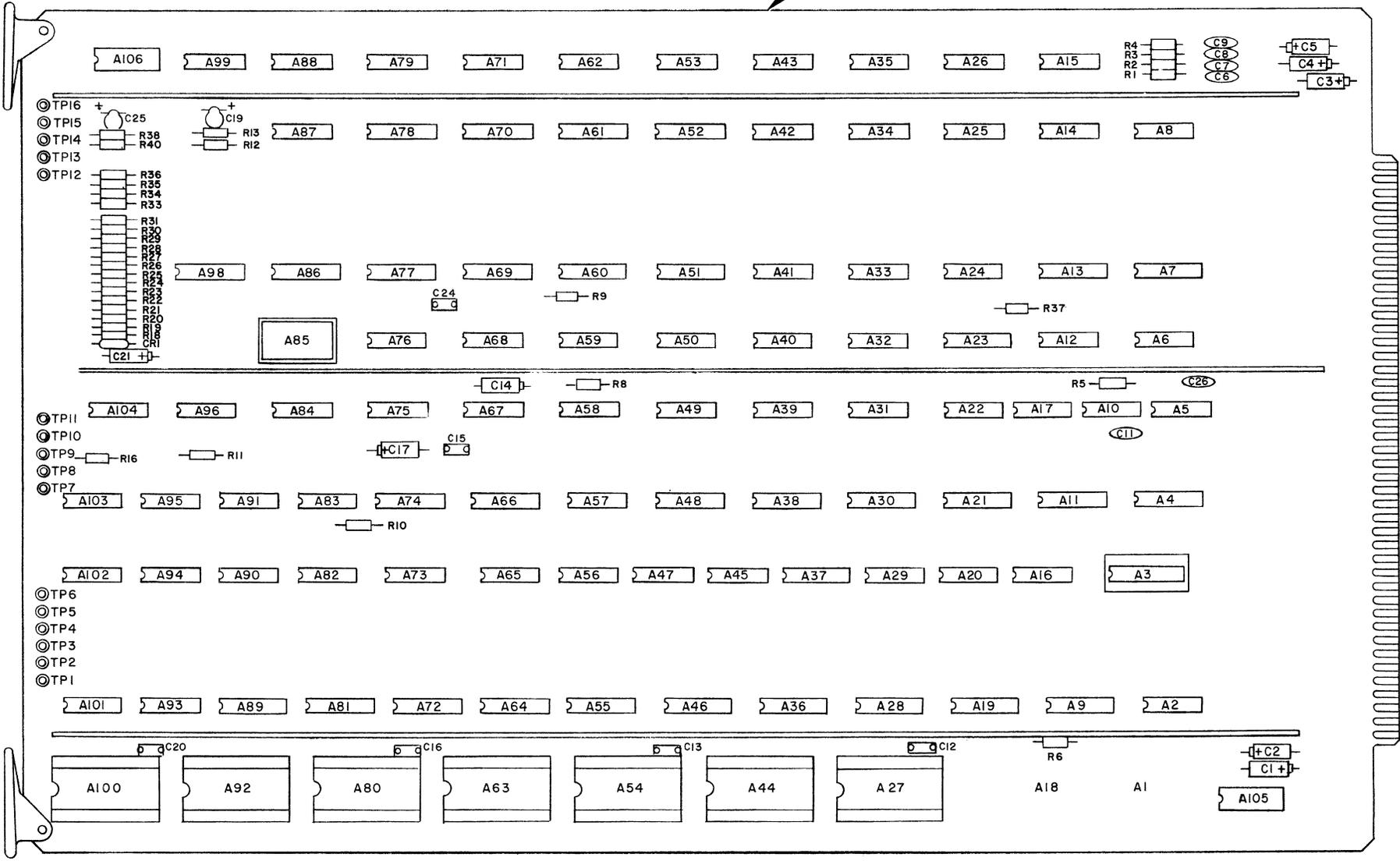
7. Remove Keyboard cover panel from Keyboard circuit board assembly.

NOTE: If Keyboard circuit board assembly is to be replaced, grounding strap must be removed from P.C. board by removing grounding lug, and replacing strap to same position on the replacement board.

SECTION VI

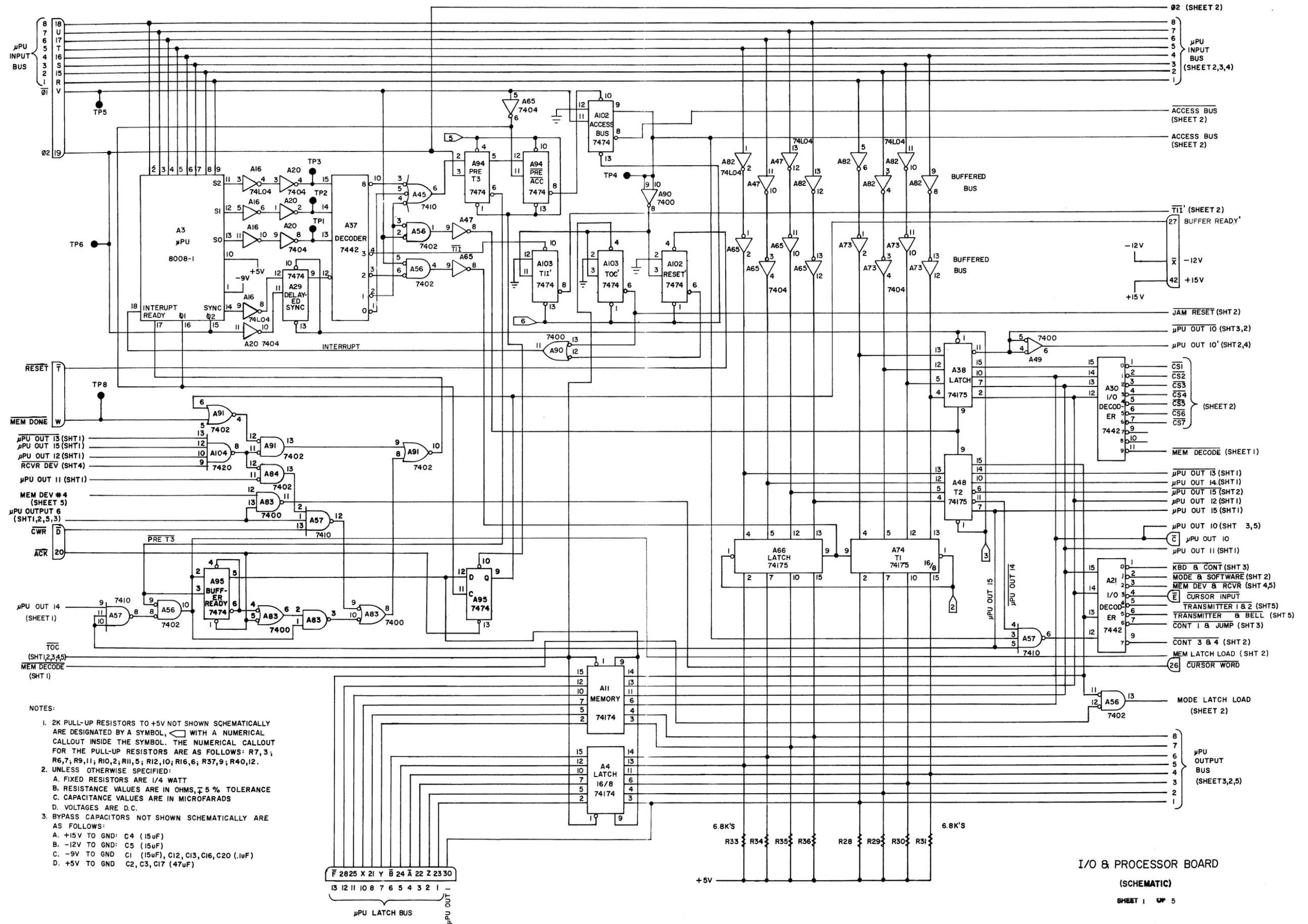
DIAGRAMS

1A1A1

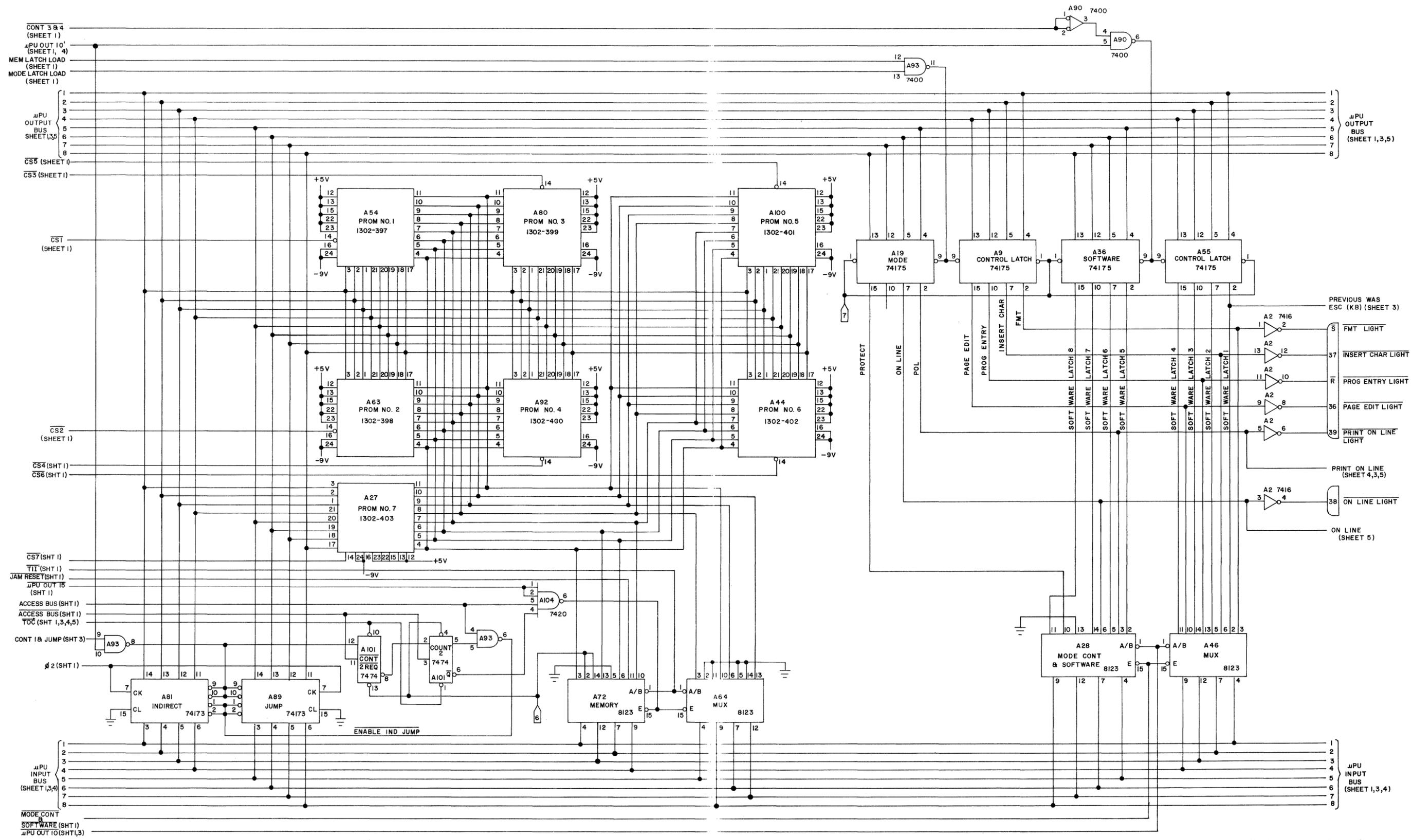


6-3/6-4

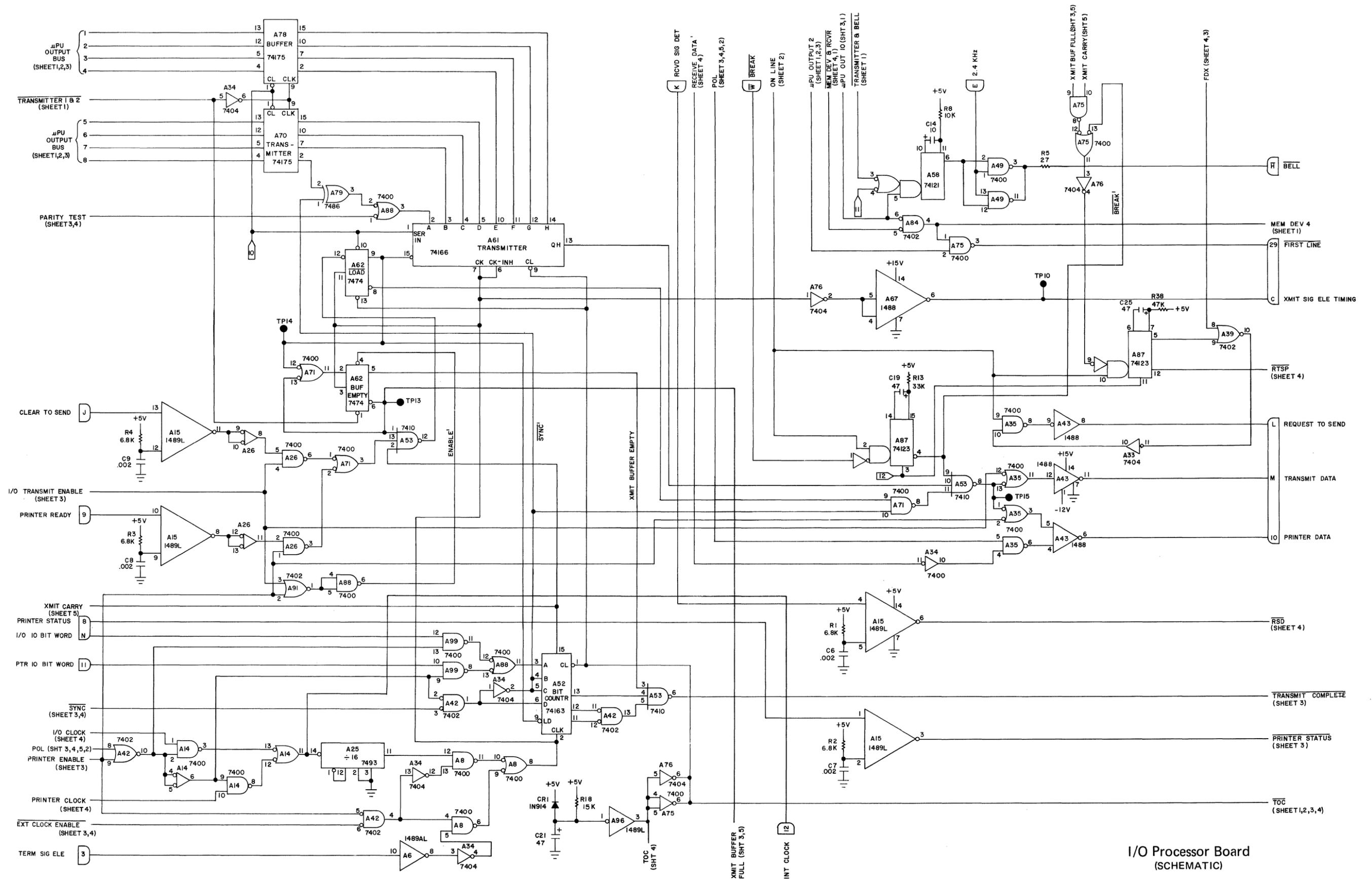
SUPER BEE I/O Processor Board



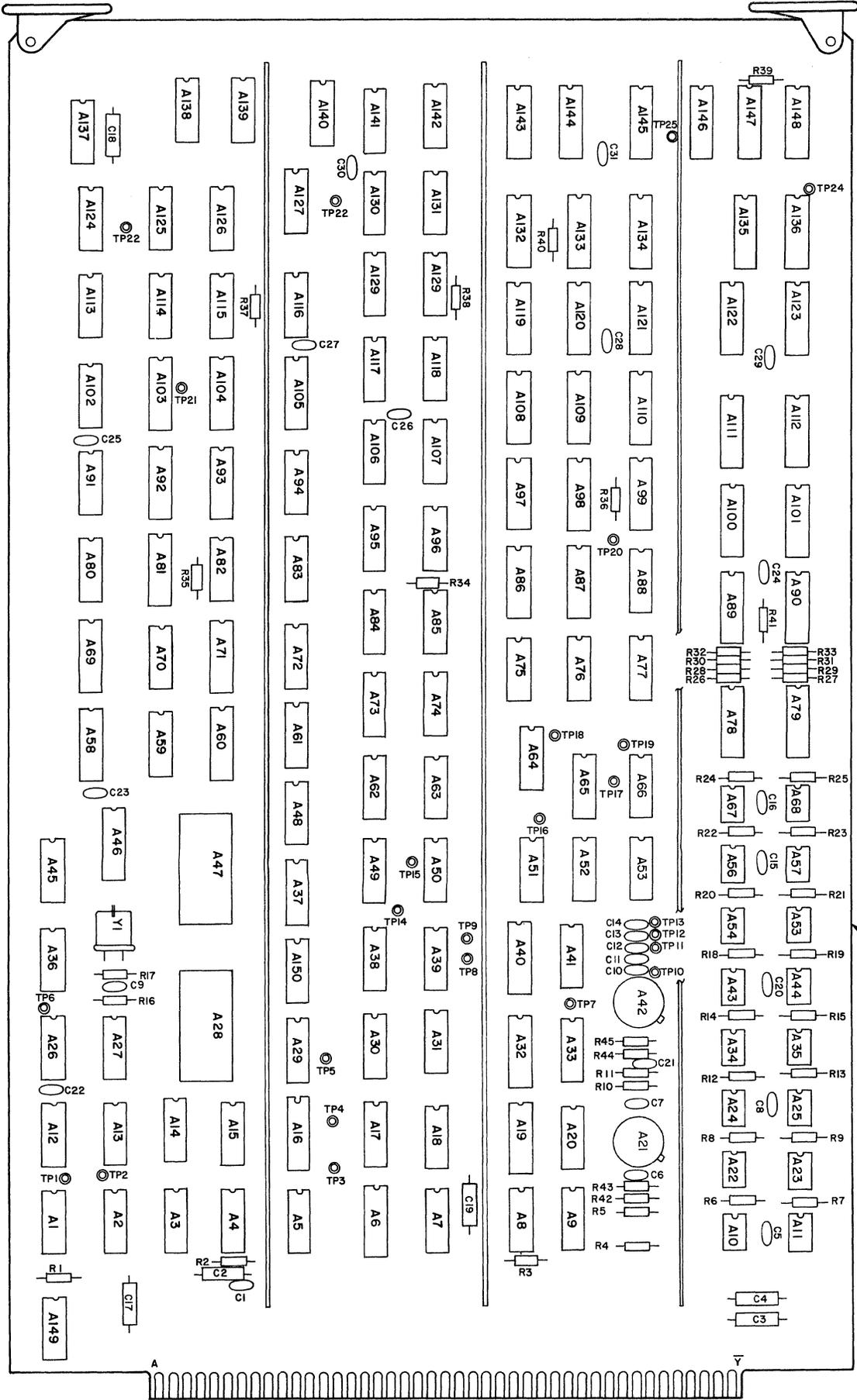
- NOTES:
- 2K PULL-UP RESISTORS TO +5V NOT SHOWN SCHEMATICALLY ARE DESIGNATED BY A SYMBOL, \square WITH A NUMERICAL CALLOUT INSIDE THE SYMBOL. THE NUMERICAL CALLOUT FOR THE PULL-UP RESISTORS ARE AS FOLLOWS: R7,3; R6,7; R9,11; R10,2; R11,5; R12,10; R16,6; R37,9; R40,12.
 - UNLESS OTHERWISE SPECIFIED:
 - FIXED RESISTORS ARE 1/4 WATT
 - RESISTANCE VALUES ARE IN OHMS, $\pm 5\%$ TOLERANCE
 - CAPACITANCE VALUES ARE IN MICROFARADS
 - VOLTAGES ARE D.C.
 - BYPASS CAPACITORS NOT SHOWN SCHEMATICALLY ARE AS FOLLOWS:
 - +5V TO GND: C4 (15 μ F)
 - 12V TO GND: C5 (15 μ F)
 - 9V TO GND: C1 (15 μ F), C12, C13, C16, C20 (1 μ F)
 - +5V TO GND: C2, C3, C17 (47 μ F)



I/O Processor Board
(SCHEMATIC)

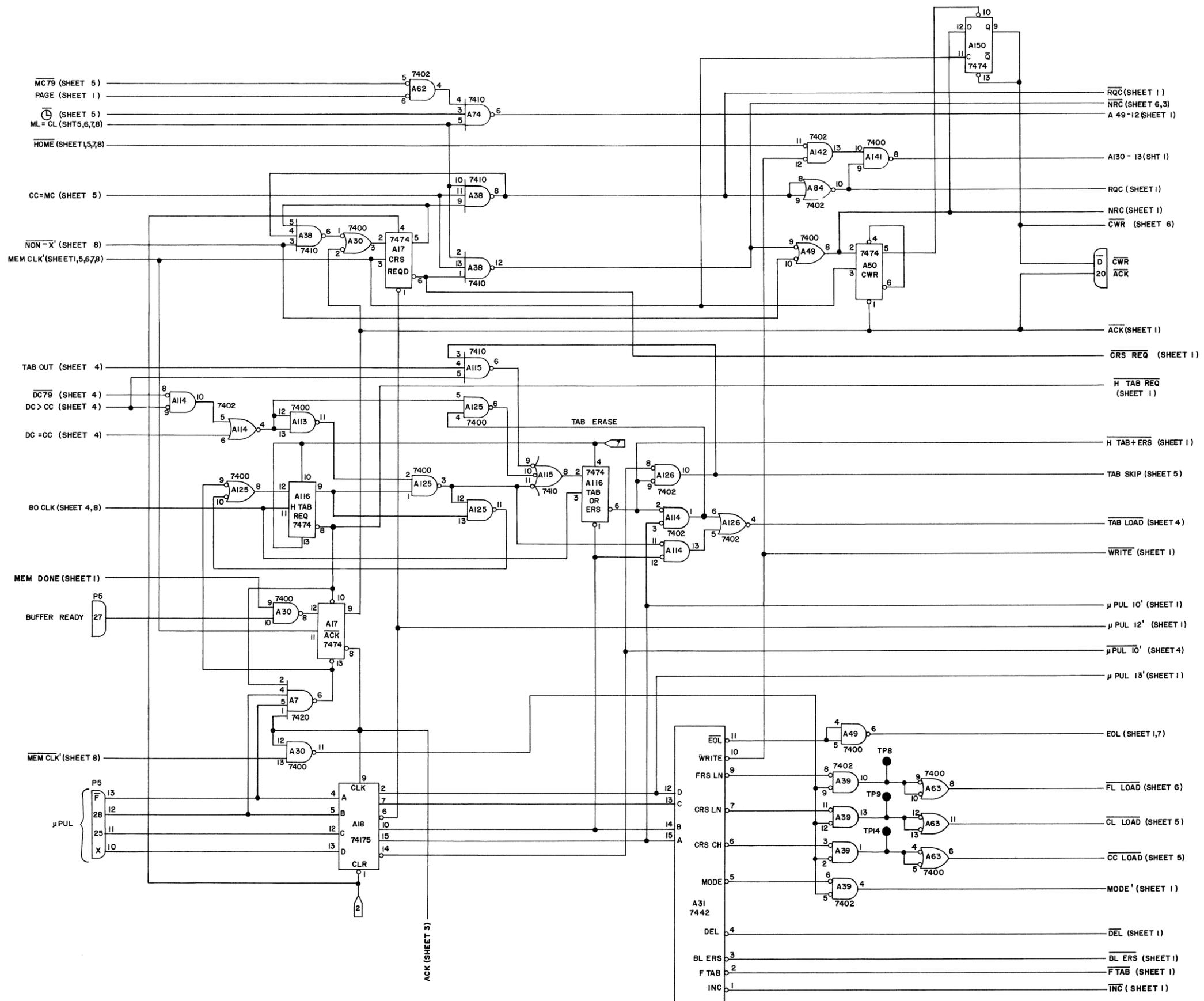


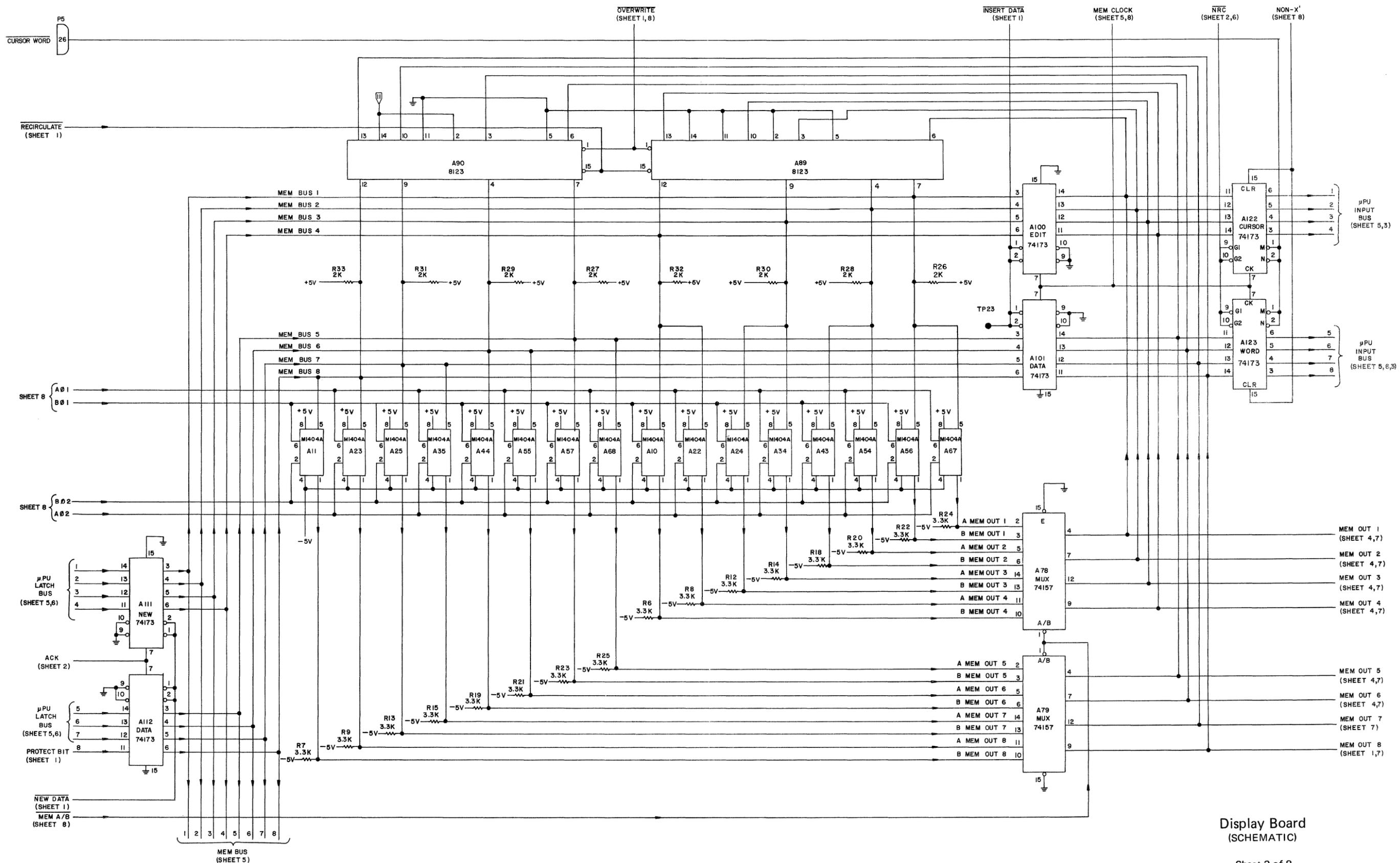
I/O Processor Board
(SCHEMATIC)



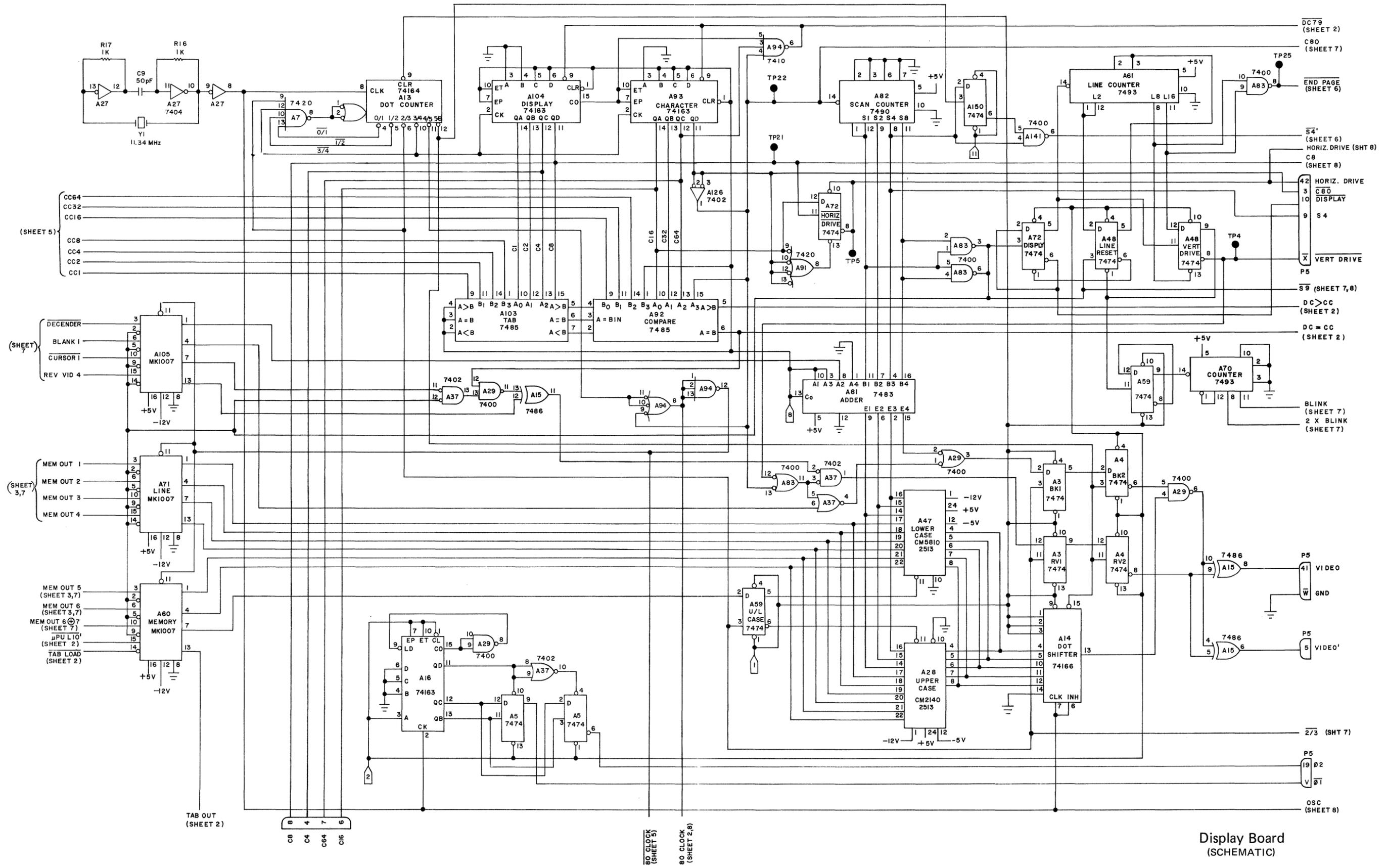
SUPER BEE Display Board

1A1A2

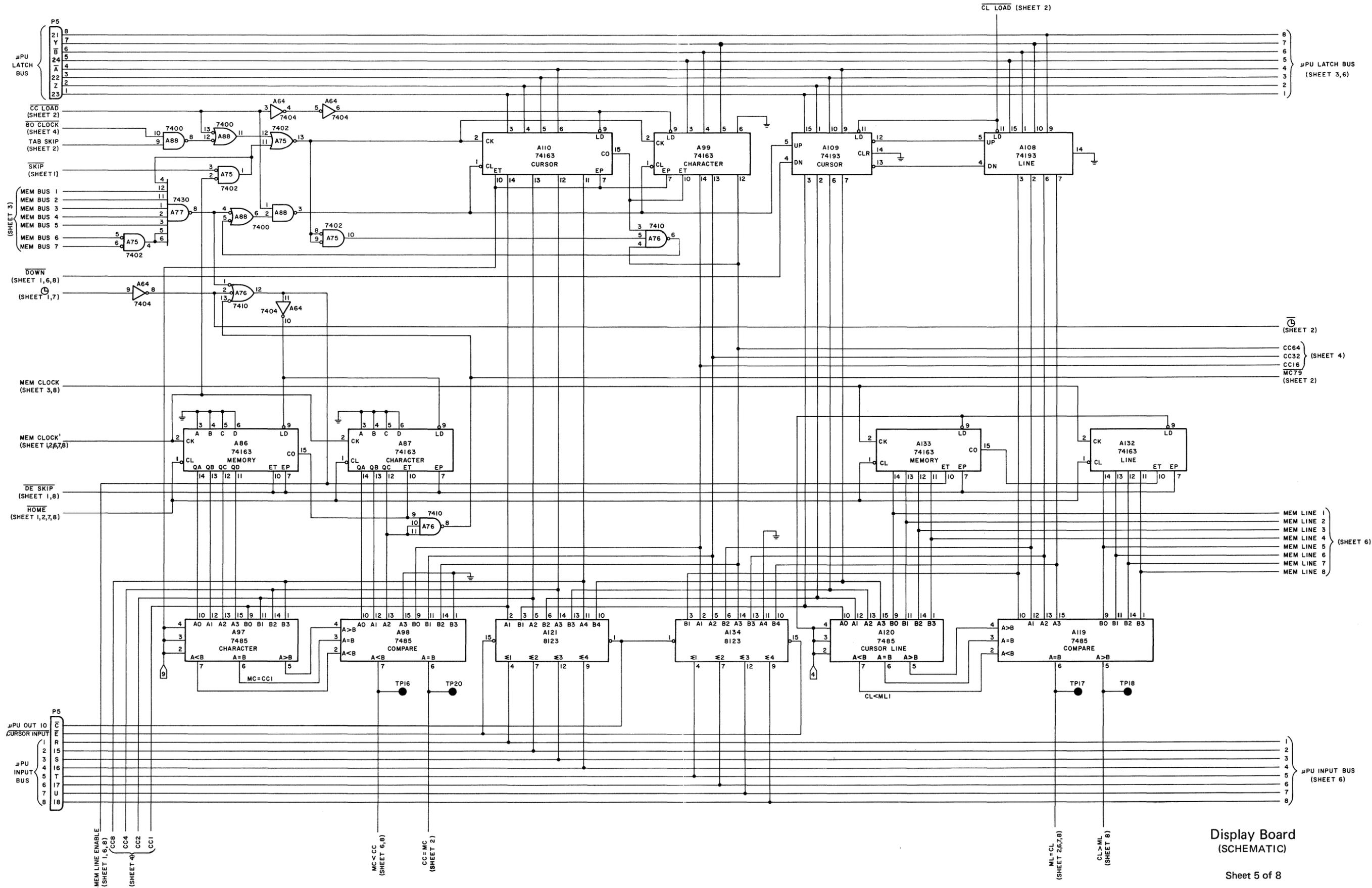




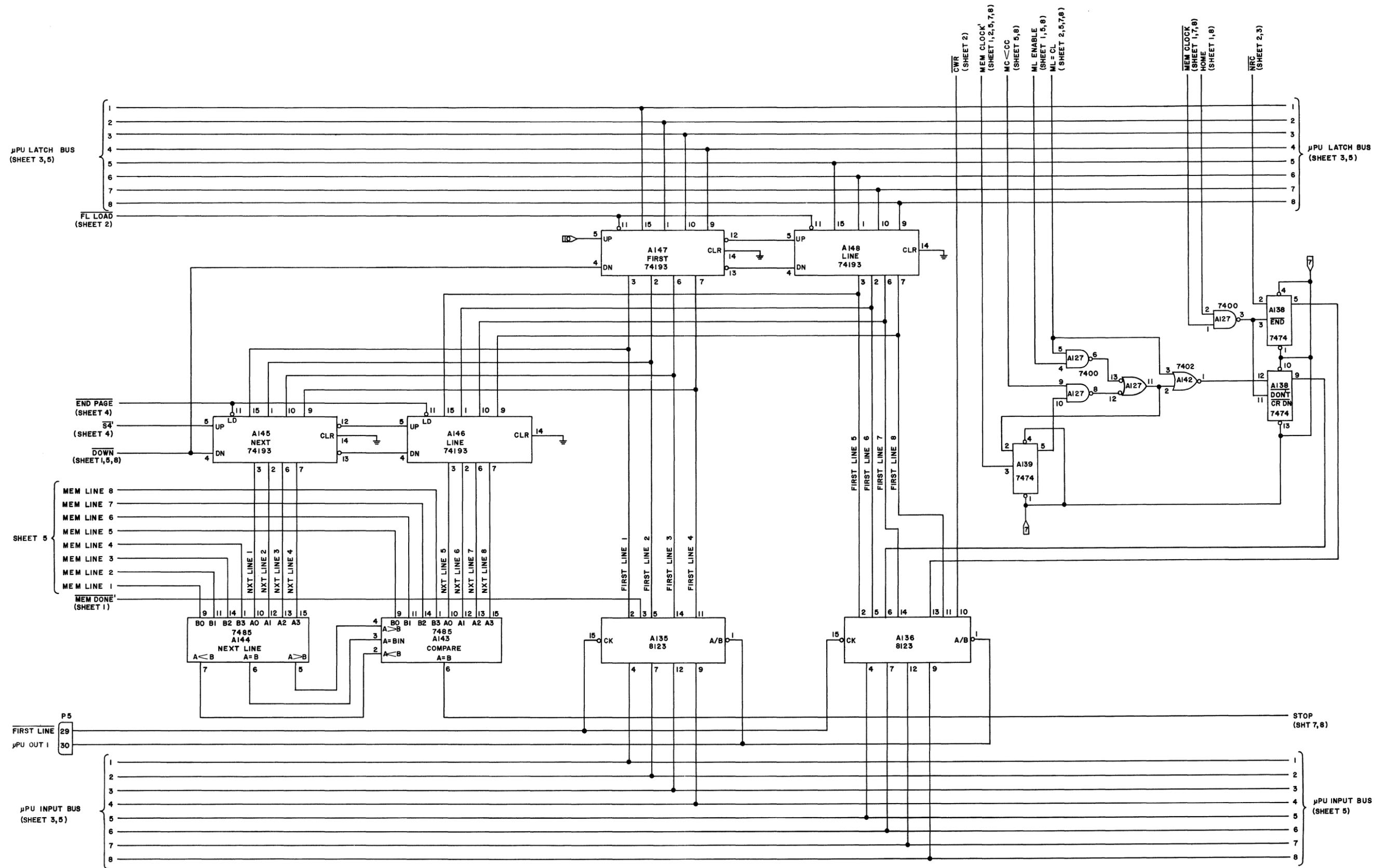
Display Board (SCHEMATIC)



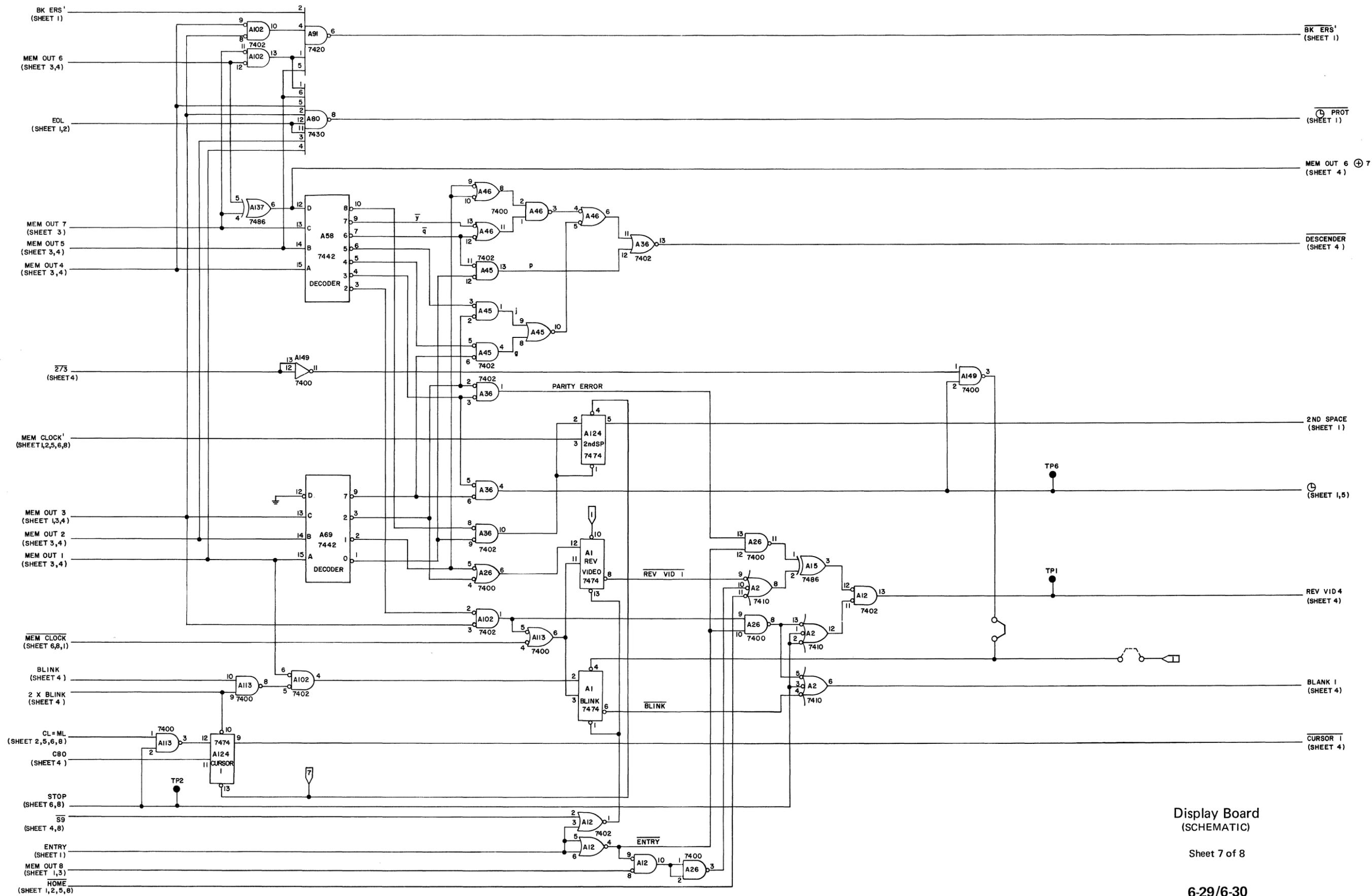
Display Board
(SCHEMATIC)



Display Board
(SCHEMATIC)

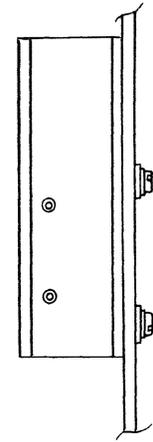
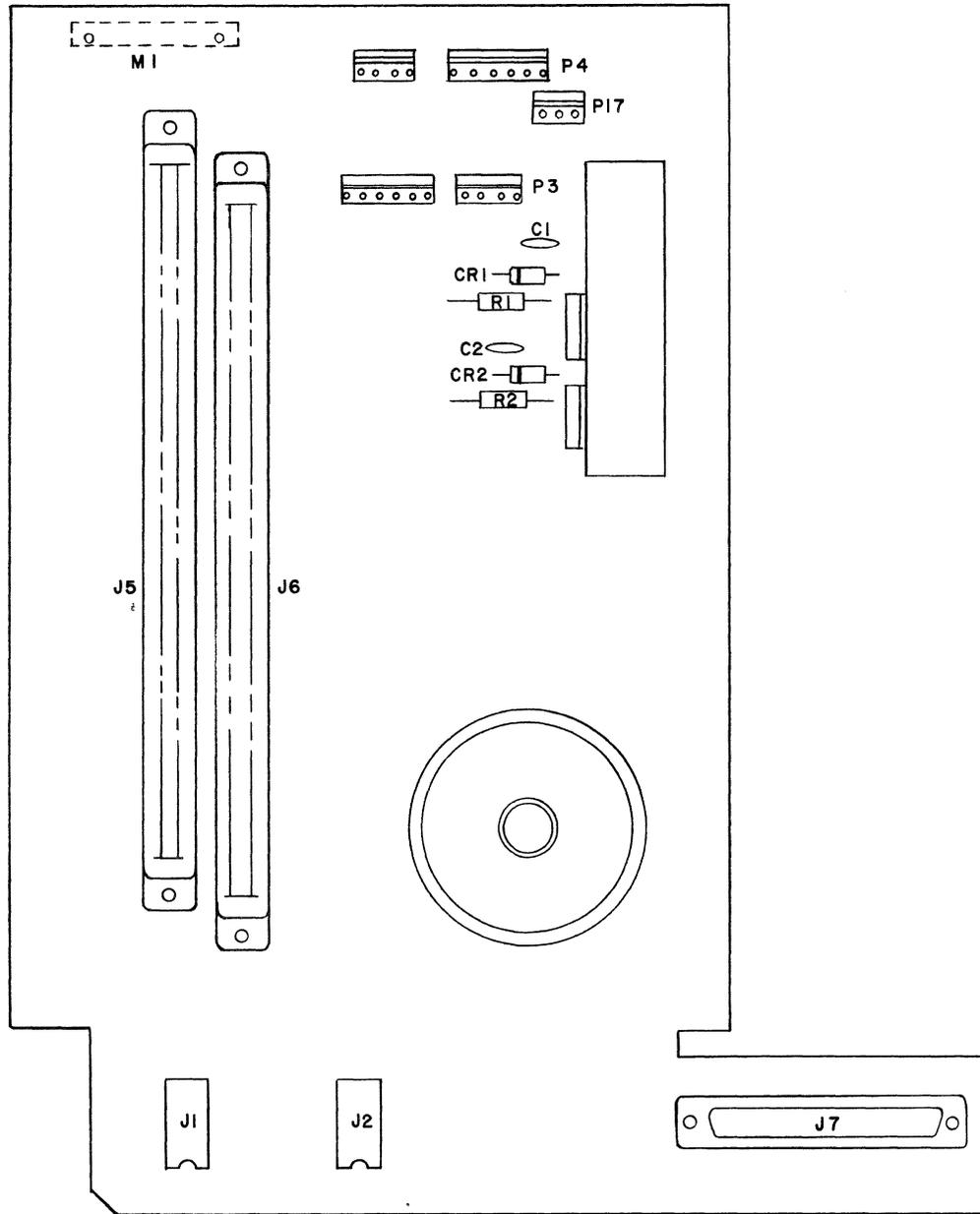


Display Board
(SCHEMATIC)

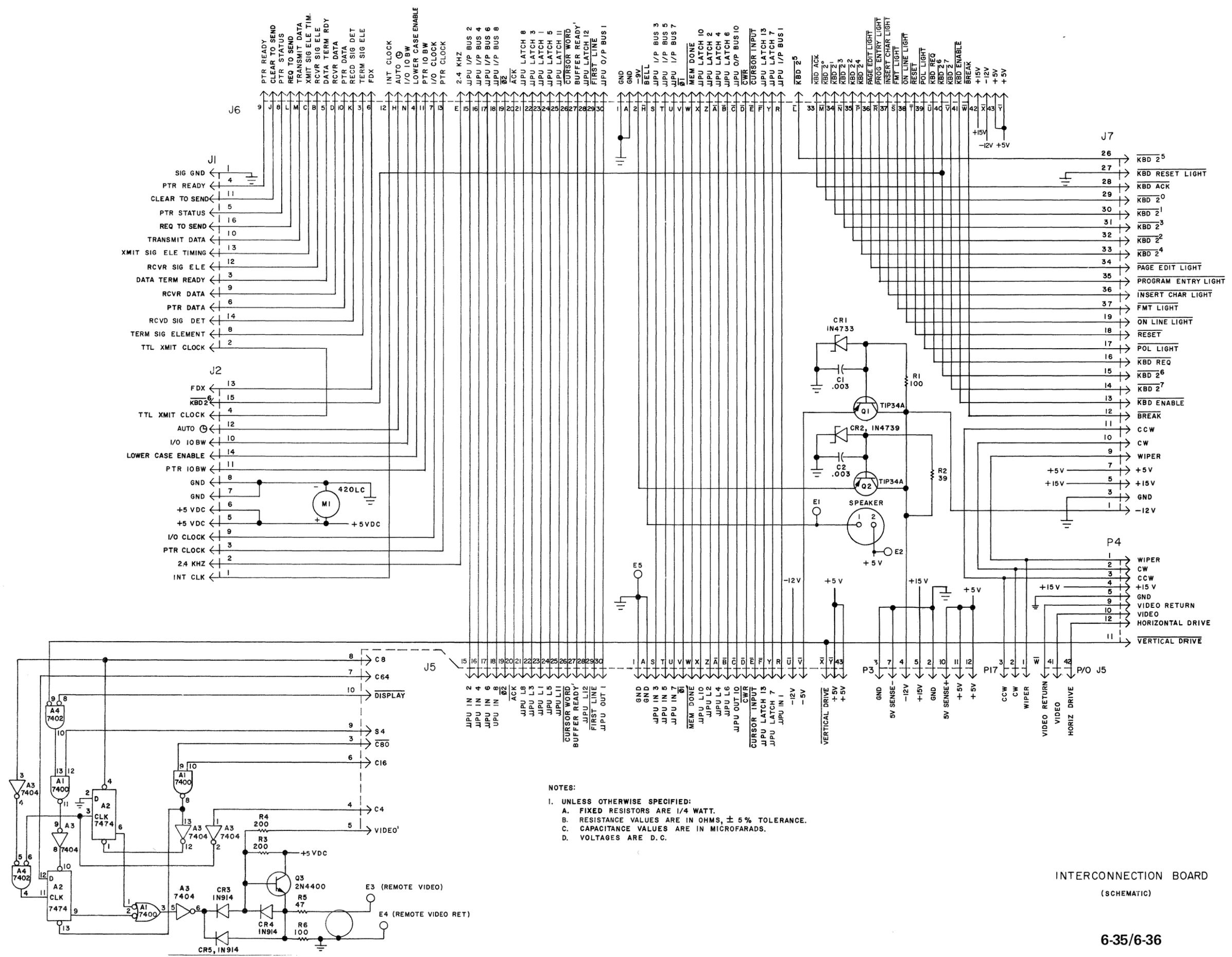


Display Board
(SCHEMATIC)

6-33/6-34

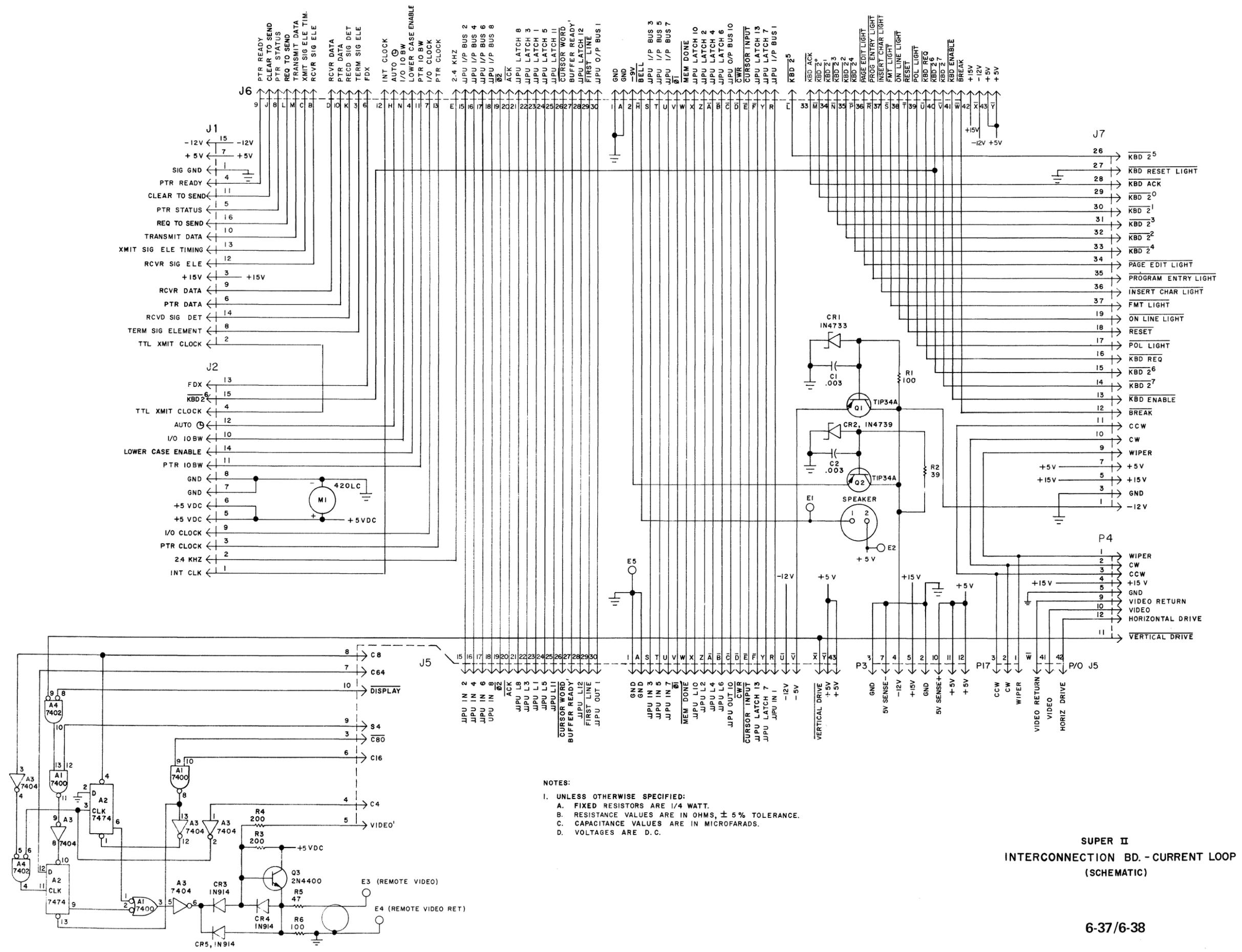


SUPER BEE Interconnection Board



NOTES:
 1. UNLESS OTHERWISE SPECIFIED:
 A. FIXED RESISTORS ARE 1/4 WATT.
 B. RESISTANCE VALUES ARE IN OHMS, ± 5% TOLERANCE.
 C. CAPACITANCE VALUES ARE IN MICROFARADS.
 D. VOLTAGES ARE D.C.

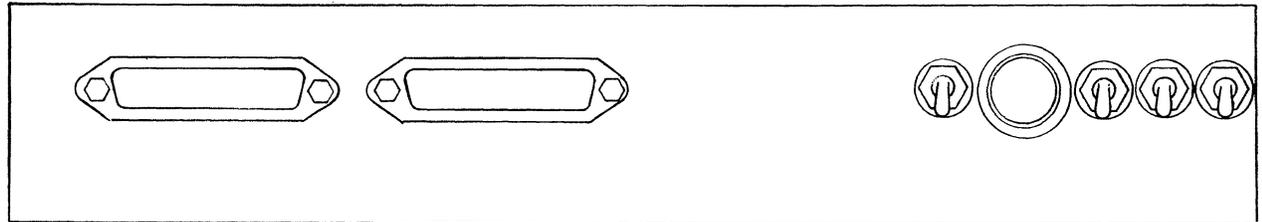
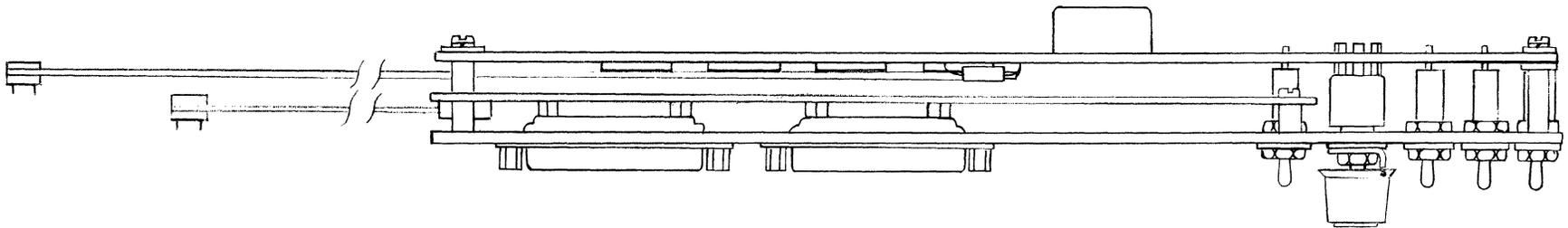
INTERCONNECTION BOARD
 (SCHEMATIC)



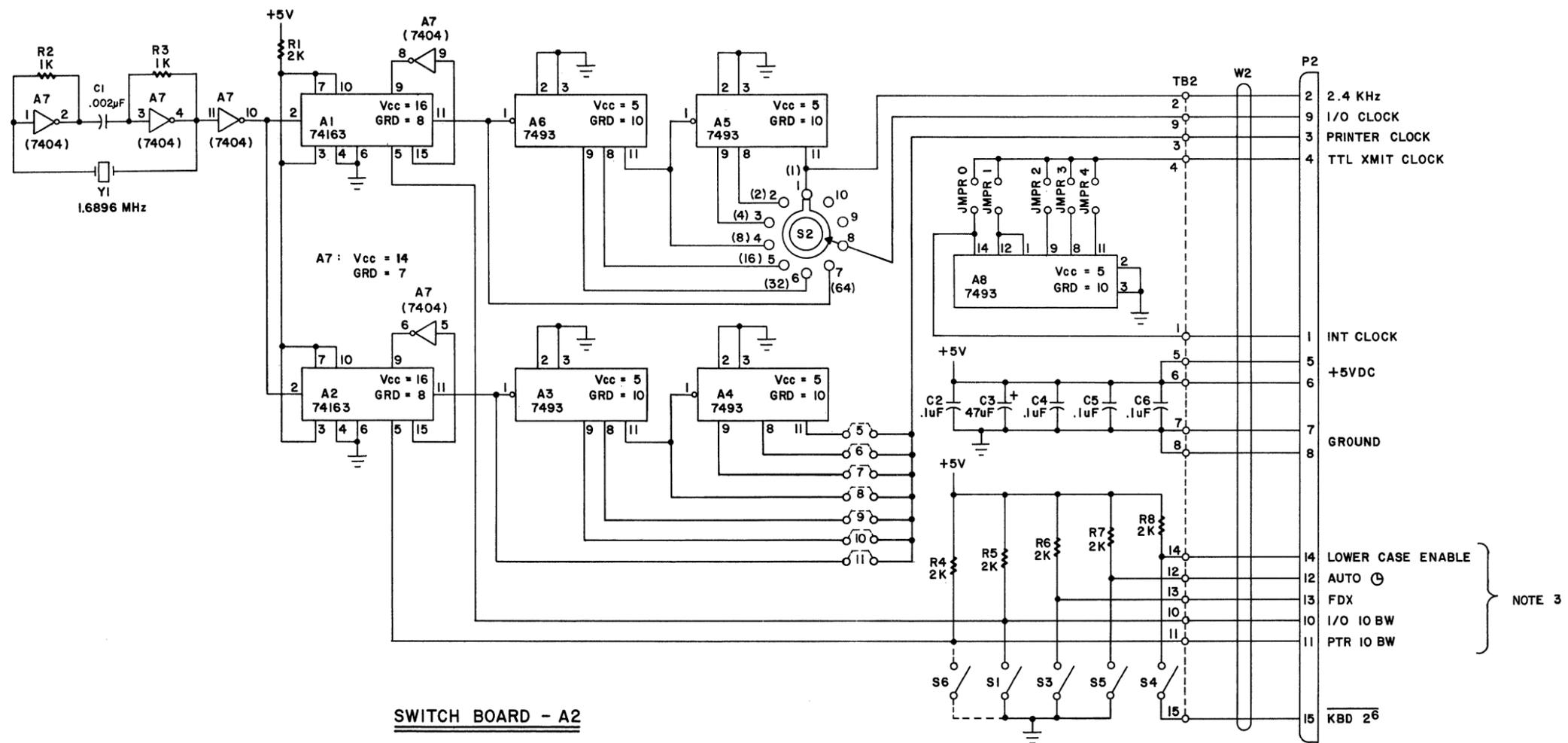
NOTES:
 1. UNLESS OTHERWISE SPECIFIED:
 A. FIXED RESISTORS ARE 1/4 WATT.
 B. RESISTANCE VALUES ARE IN OHMS, ± 5% TOLERANCE.
 C. CAPACITANCE VALUES ARE IN MICROFARADS.
 D. VOLTAGES ARE D. C.

**SUPER II
 INTERCONNECTION BD. - CURRENT LOOP
 (SCHEMATIC)**

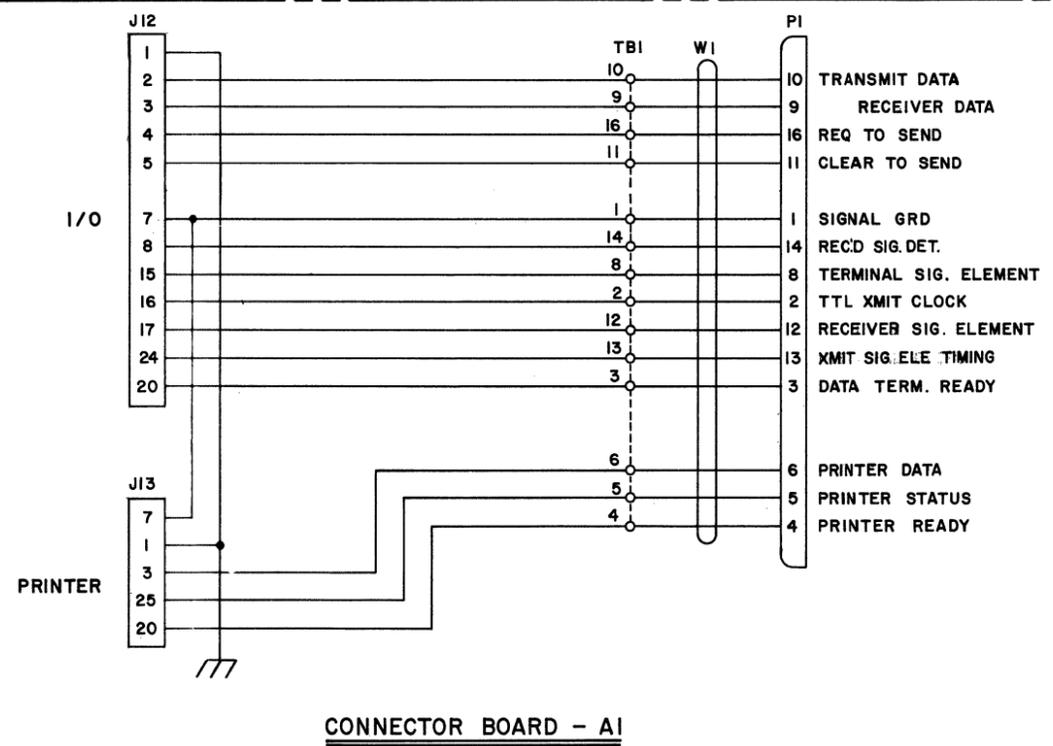
6-39/6-40

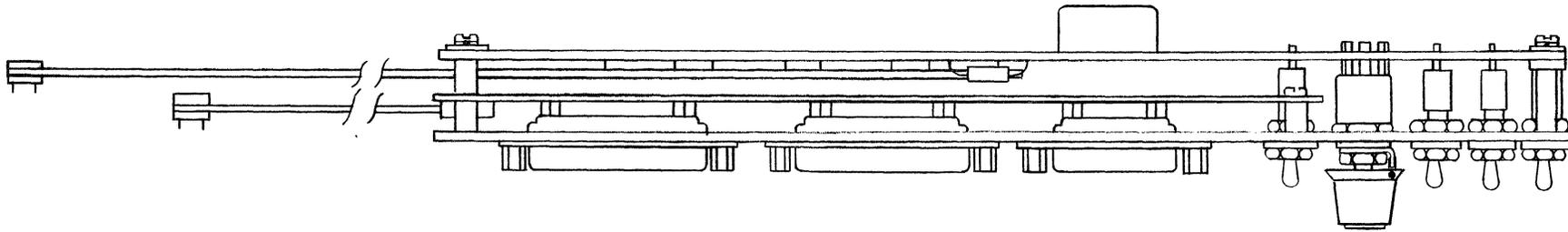


Interface Assembly

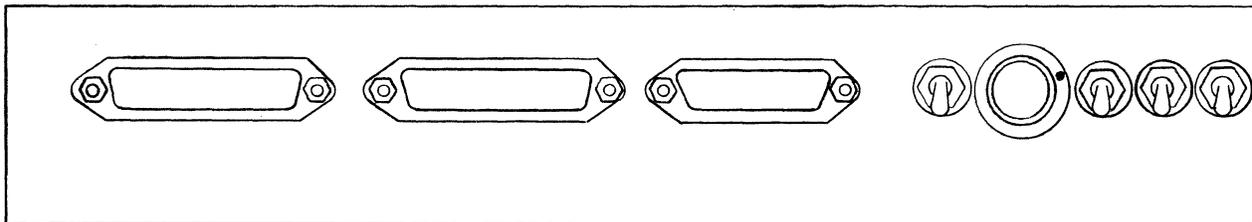


- NOTES:
1. S6 IS NOT WIRED FOR THIS ASSEMBLY.
 2. S2 IS SHOWN AS VIEW FROM THE REAR.
 3. THESE SIGNALS ARE PRESENT WHEN RESPECTIVE SWITCH IS IN THE OPEN POSITION.

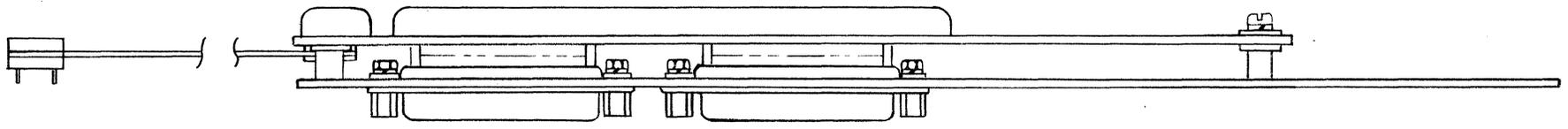




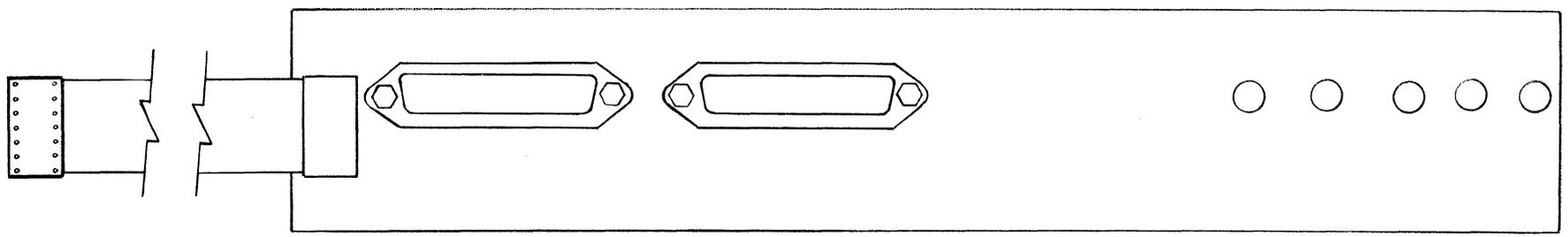
643



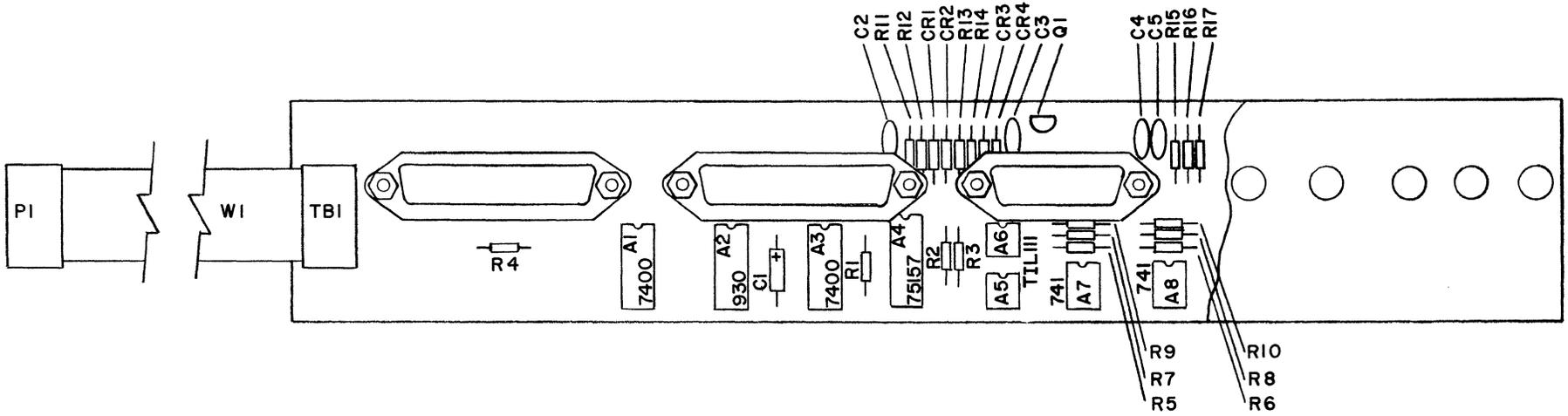
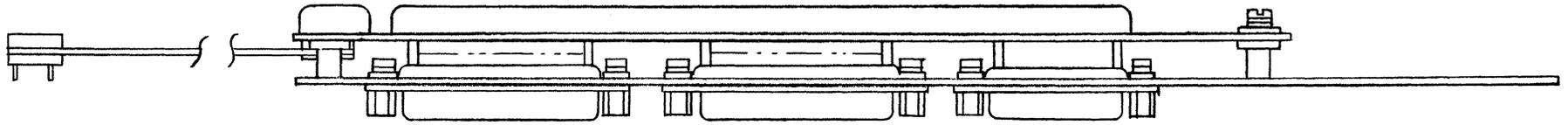
Interface Assembly With Current Loop Adapter



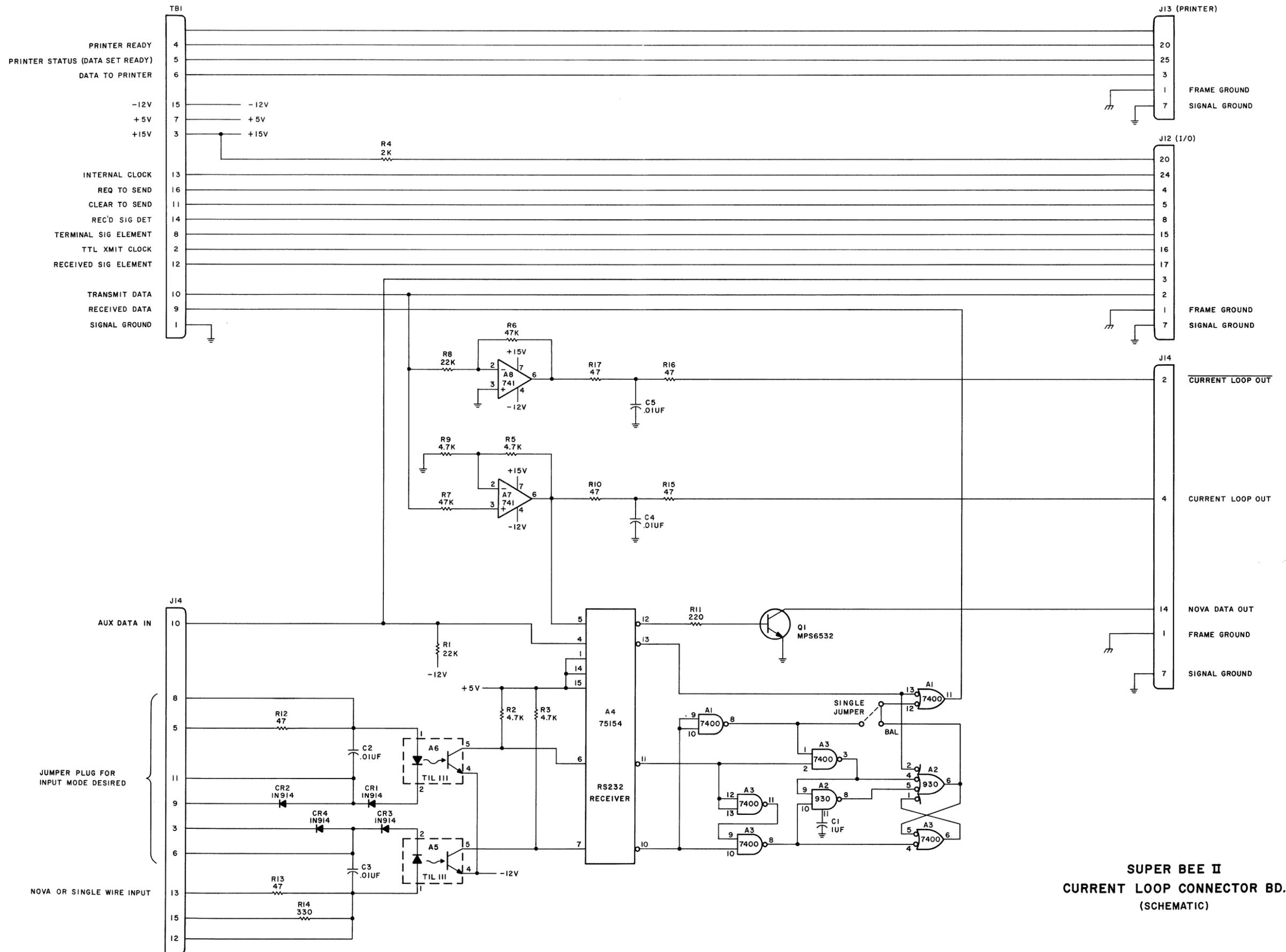
6-44



Connector Board

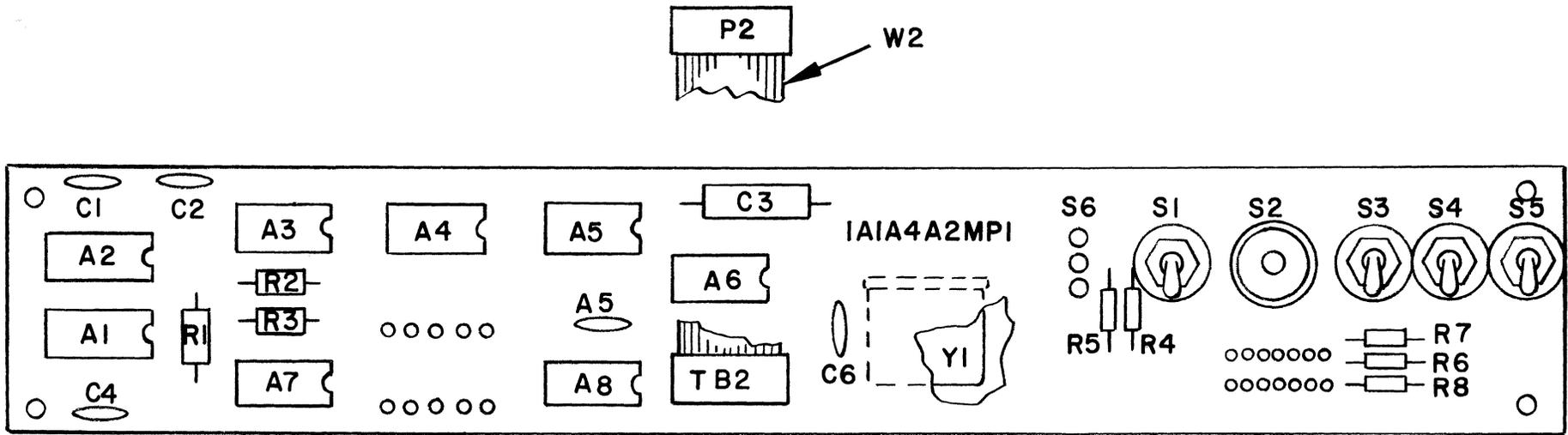


Connector Board With Current Loop Adapter



**SUPER BEE II
CURRENT LOOP CONNECTOR BD.
(SCHEMATIC)**

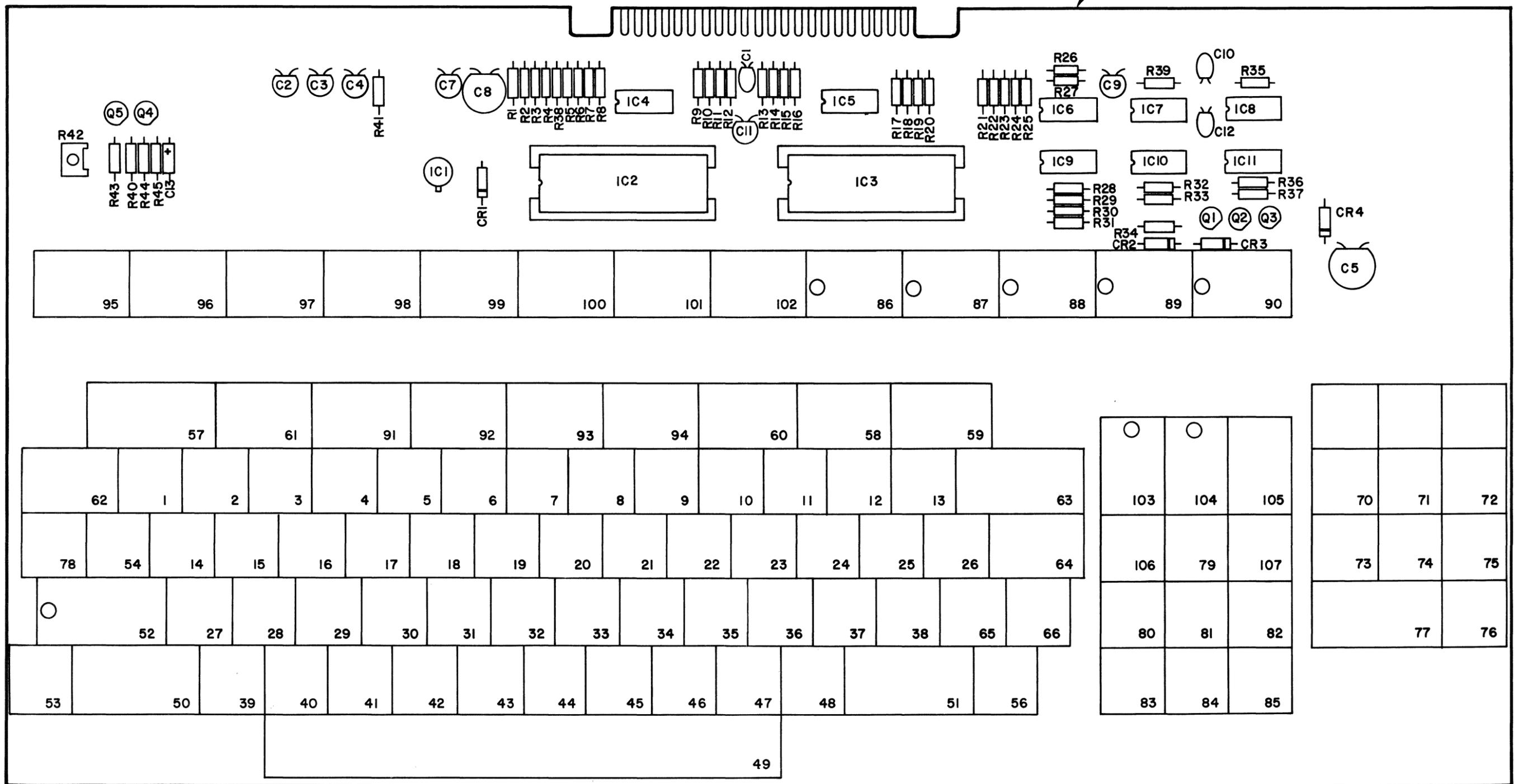
6-49/6-50



1A1A4A2

Switch Board Assembly

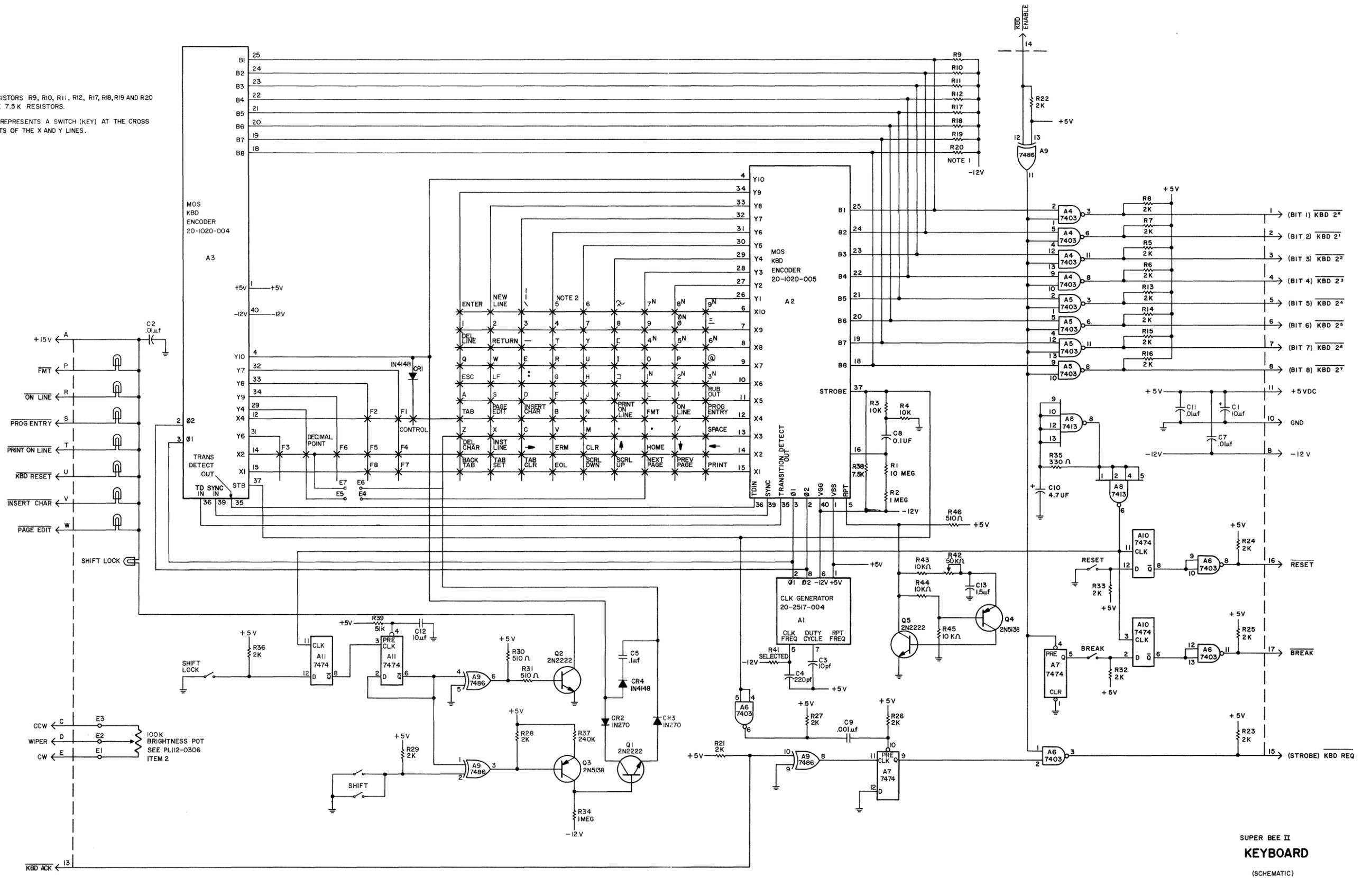
1A2A1A1



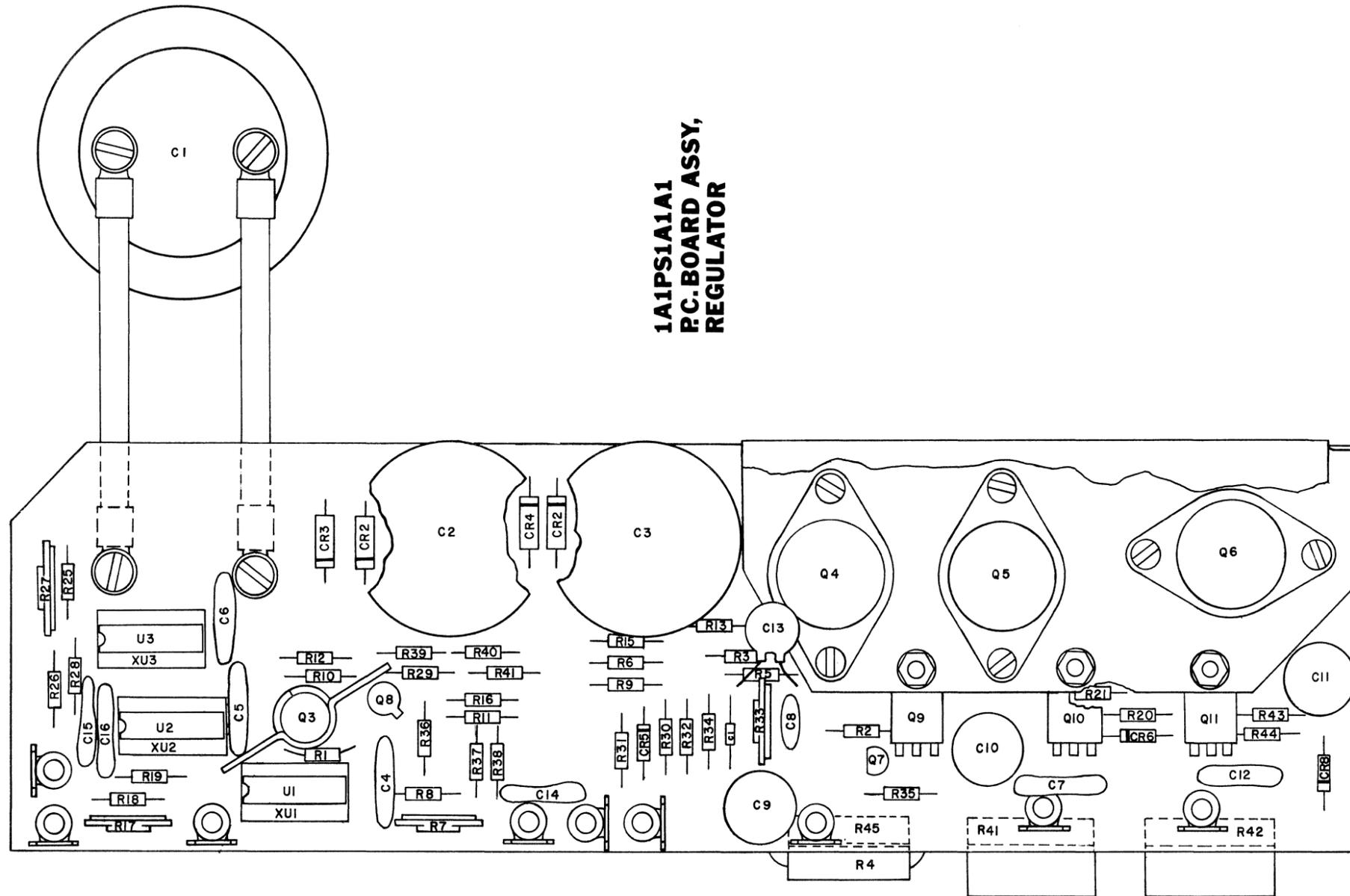
Keyboard Assembly

6-51/6-52

- NOTES:
- RESISTORS R9, R10, R11, R12, R17, R18, R19 AND R20 ARE 7.5 K RESISTORS.
 - * REPRESENTS A SWITCH (KEY) AT THE CROSS POINTS OF THE X AND Y LINES.

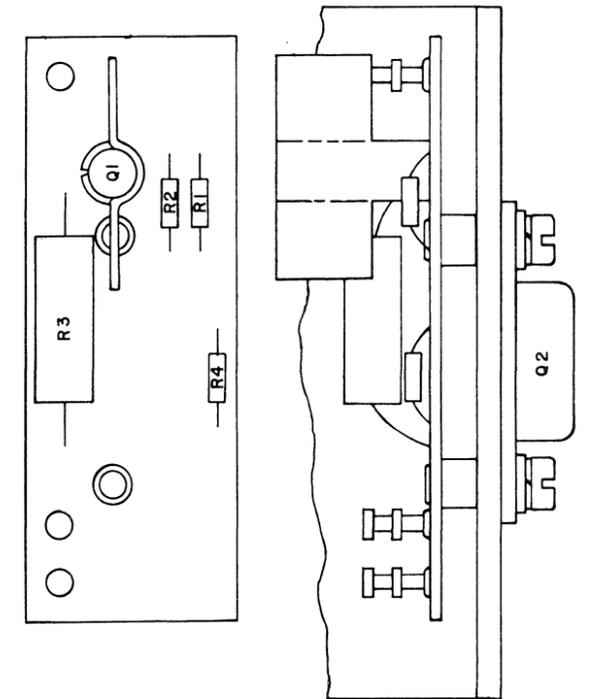


SUPER BEE II
KEYBOARD
(SCHEMATIC)

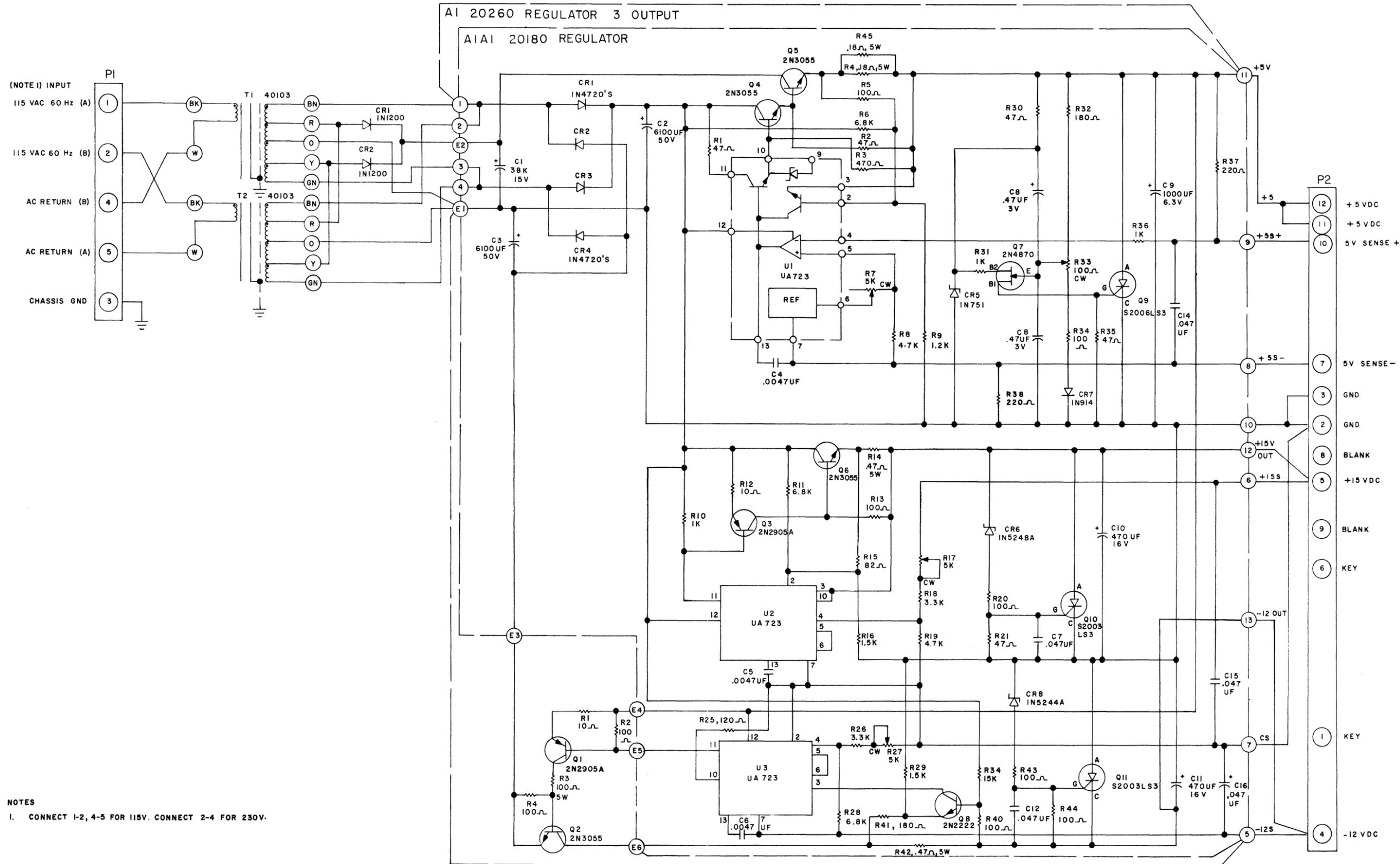


**1A1PS1A1A1
P.C. BOARD ASSY,
REGULATOR**

**1A1PS1A1
REGULATOR,
3 OUTPUT**



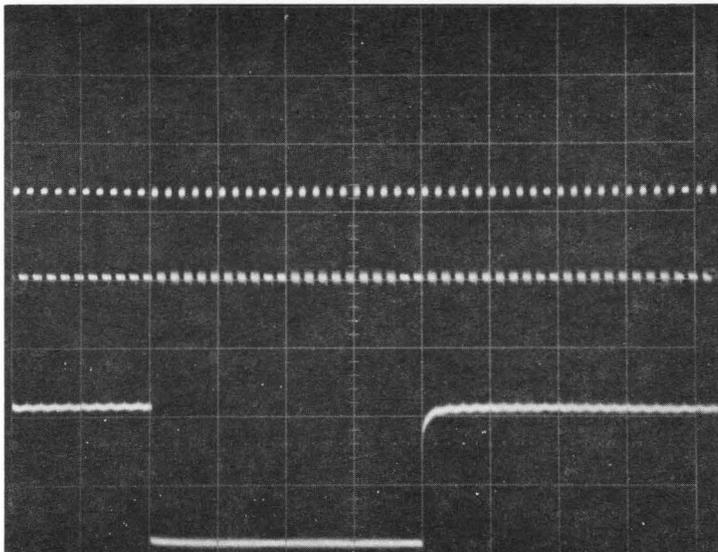
3 Output Regulator and Regulator P.C. Board Assembly



NOTES
 1. CONNECT 1-2, 4-5 FOR 115V. CONNECT 2-4 FOR 230V.

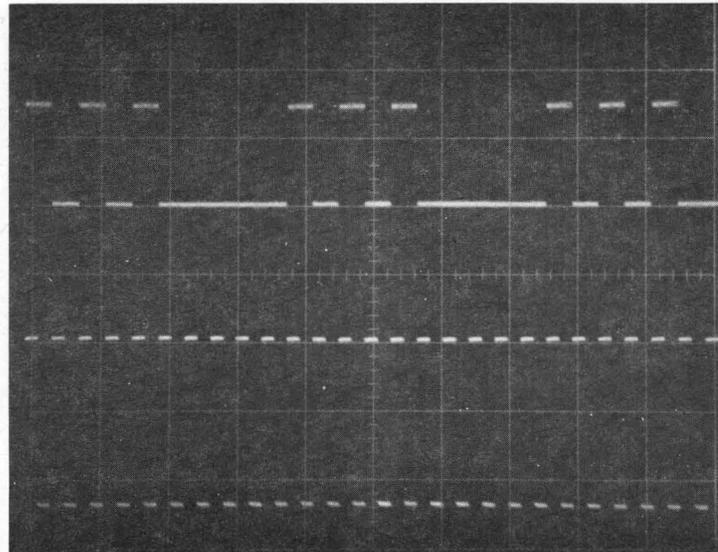
Elexon Power Supply
 (SCHEMATIC)

6-57/6-58



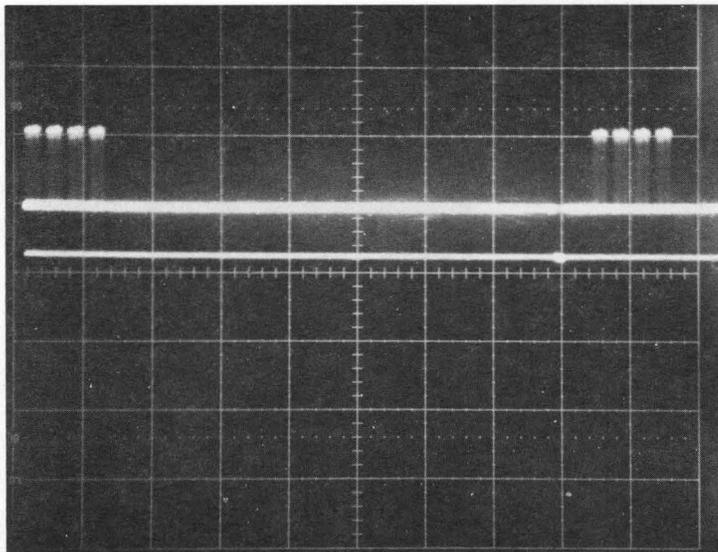
Horizontal Drive/Vert. Drive
 .2 msec/Div. uncal, 2v/Div.
 Ext Trigger End Page

WAVEFORM A



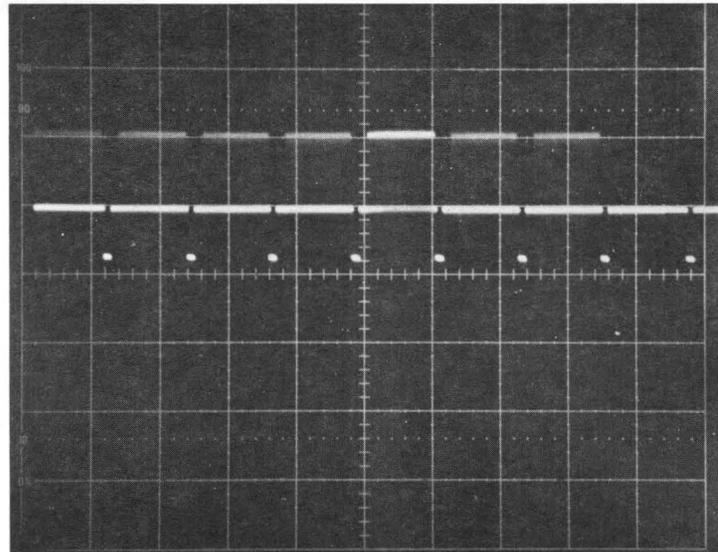
Xmit Data TP15
 2v/Div. .2 msec/Div. uncal.
 Trigger Xmit Data

WAVEFORM B



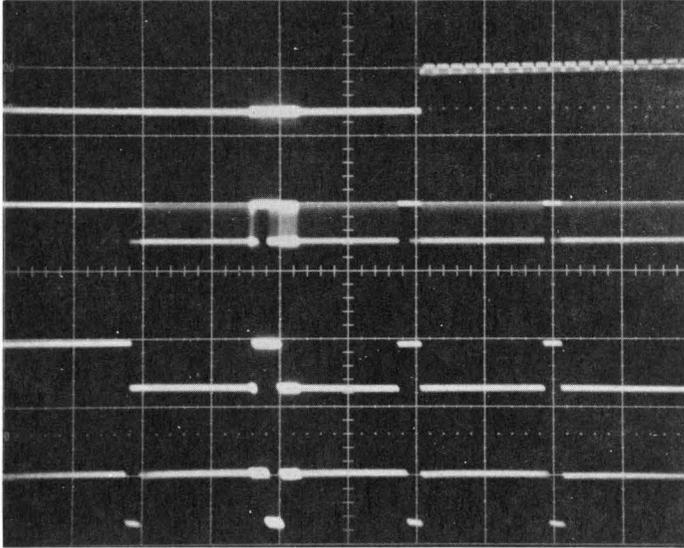
Remote Video
 2 micro sec./Div. 2v/Div

WAVEFORM D₁



Remote Video Blow up
 50 msec/Div. 2v/Div

WAVEFORM D₂

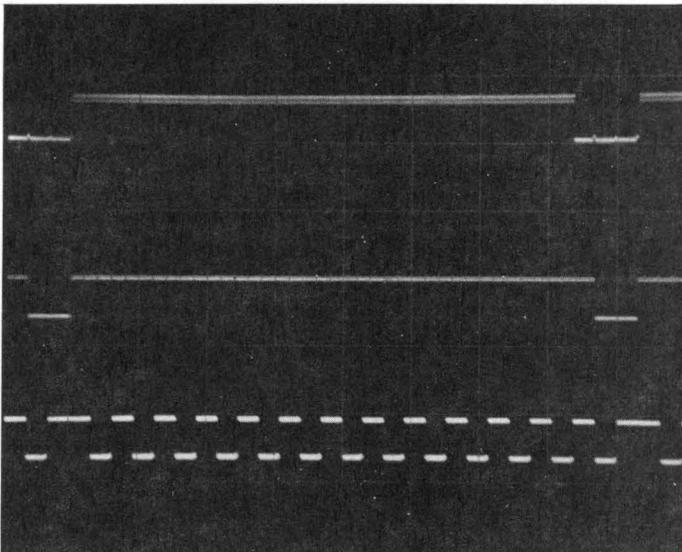
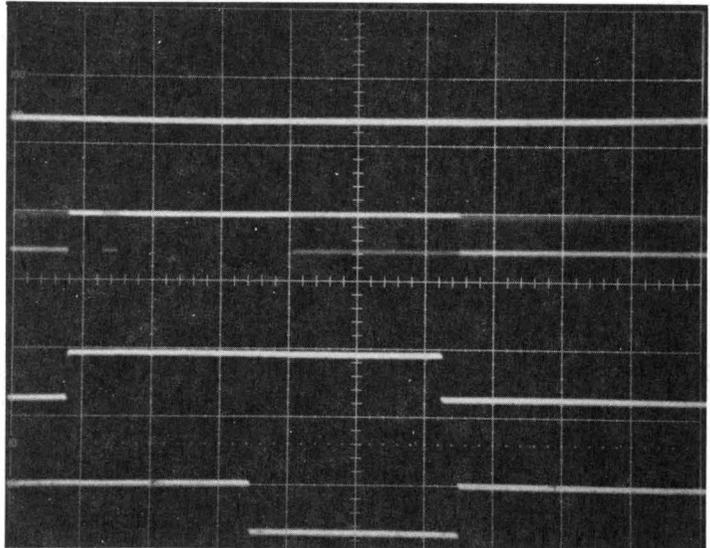


Ch I End Page
 Ch II Mem Clk
 Ch III Stop
 Ch IV $\overline{S9}$
 .2 msec/Div uncal
 5v/Div
 Trigger Ch I
 (Intensified area blown up in
 WAVEFORM F)

WAVEFORM E

CH I Mem CLK
 CH II Stop
 CH III $\overline{S9}$
 .2 msec/Div uncal
 5v/Div
 Delayed Sweep
 EX Trigger End Page

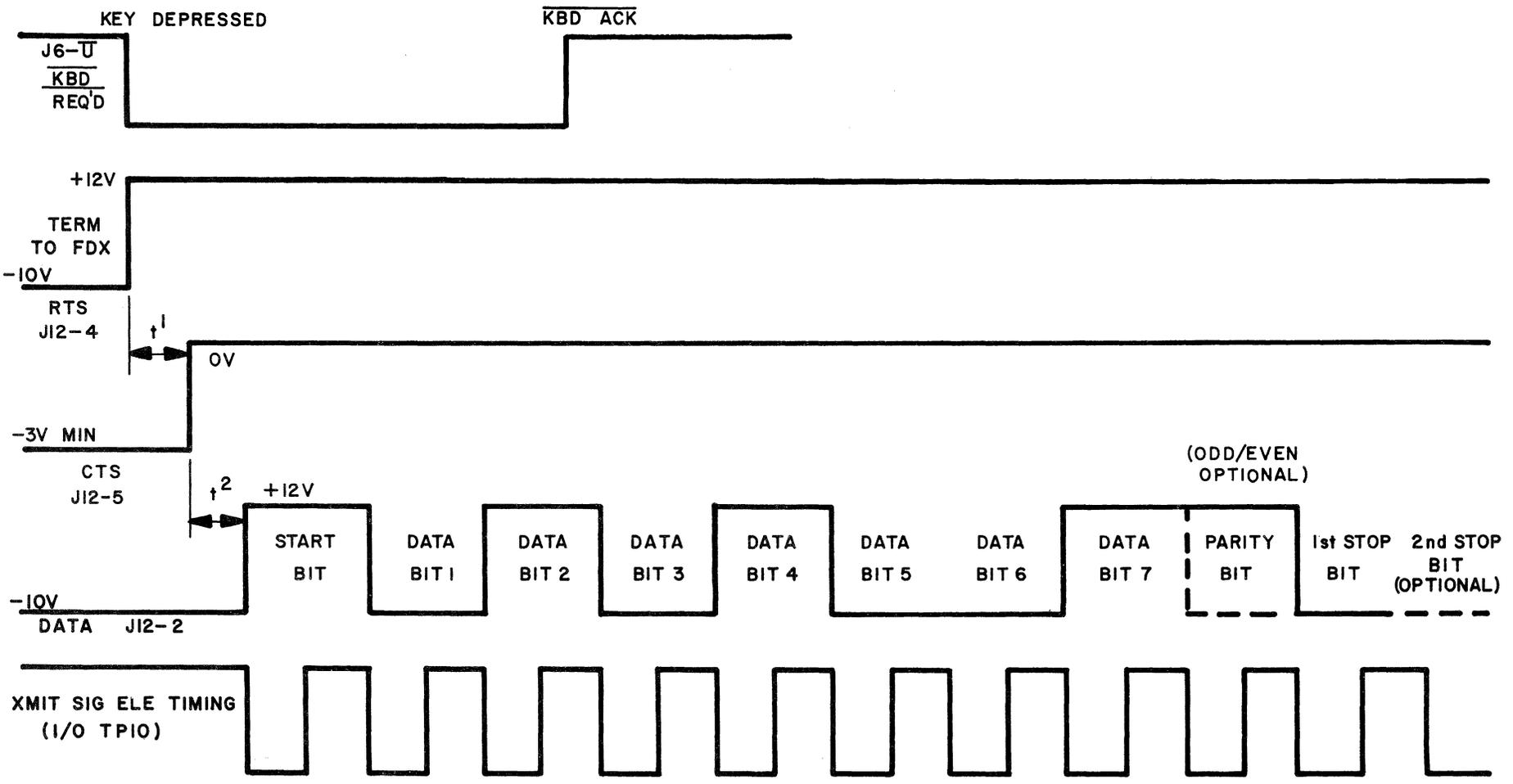
WAVEFORM F



CH I End Page
 CH II $\overline{\text{Vert Drive}}$
 CH III Display
 .2 msec/Div
 5v/Div
 Trigger CH I

WAVEFORM G

6-61

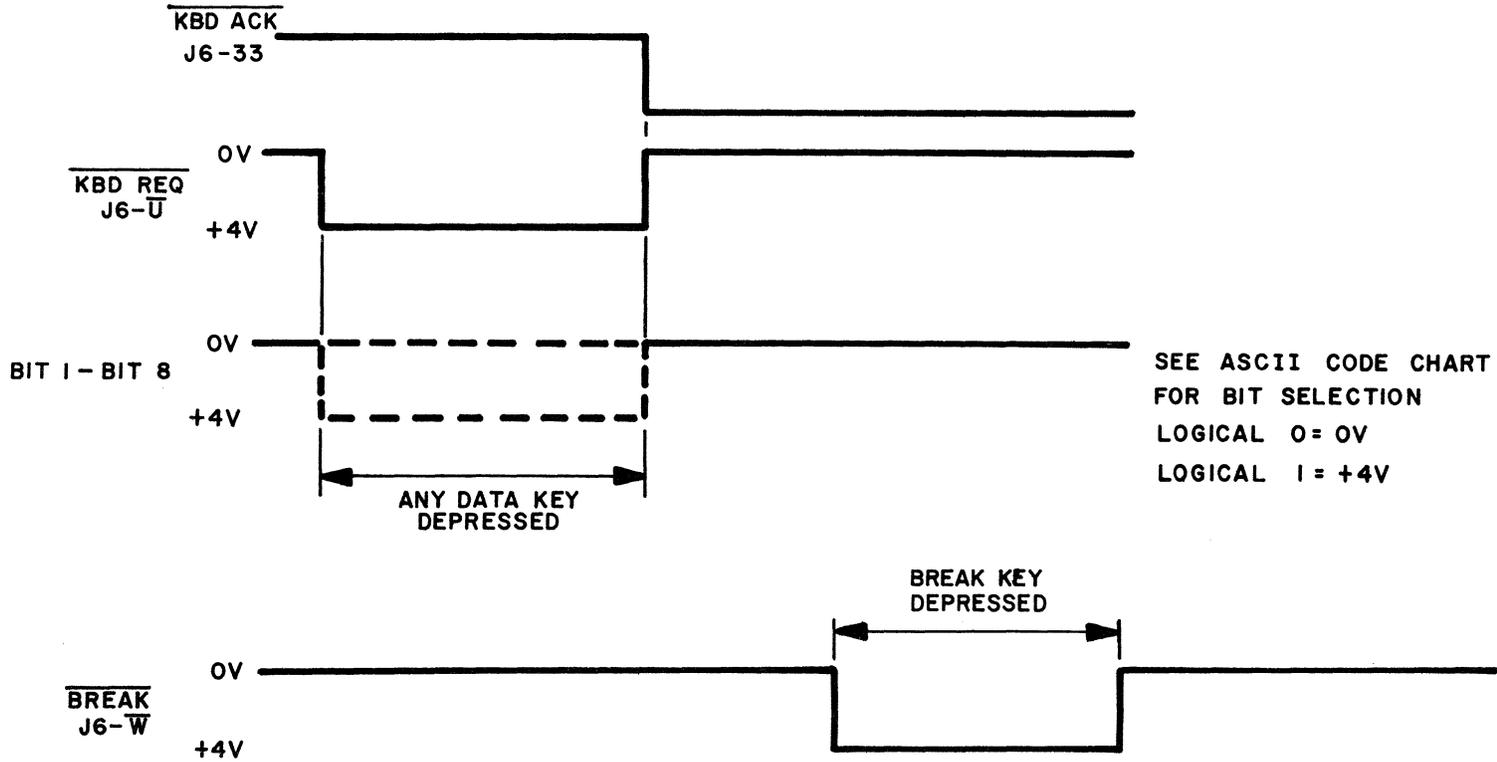


TERMINAL IN FDX
 t^1 = DETERMINED BY MODEM ≈ 200 MSEC
 t^2 = LESS THAN ONE CHARACTER TIME AT THE
 SPECIFIED BAUD RATE.
 DATA = THE NUMBER FIVE

TIMING DIAGRAM
 A

KEYBOARD INTERFACE TIMING DIAGRAM

6-62

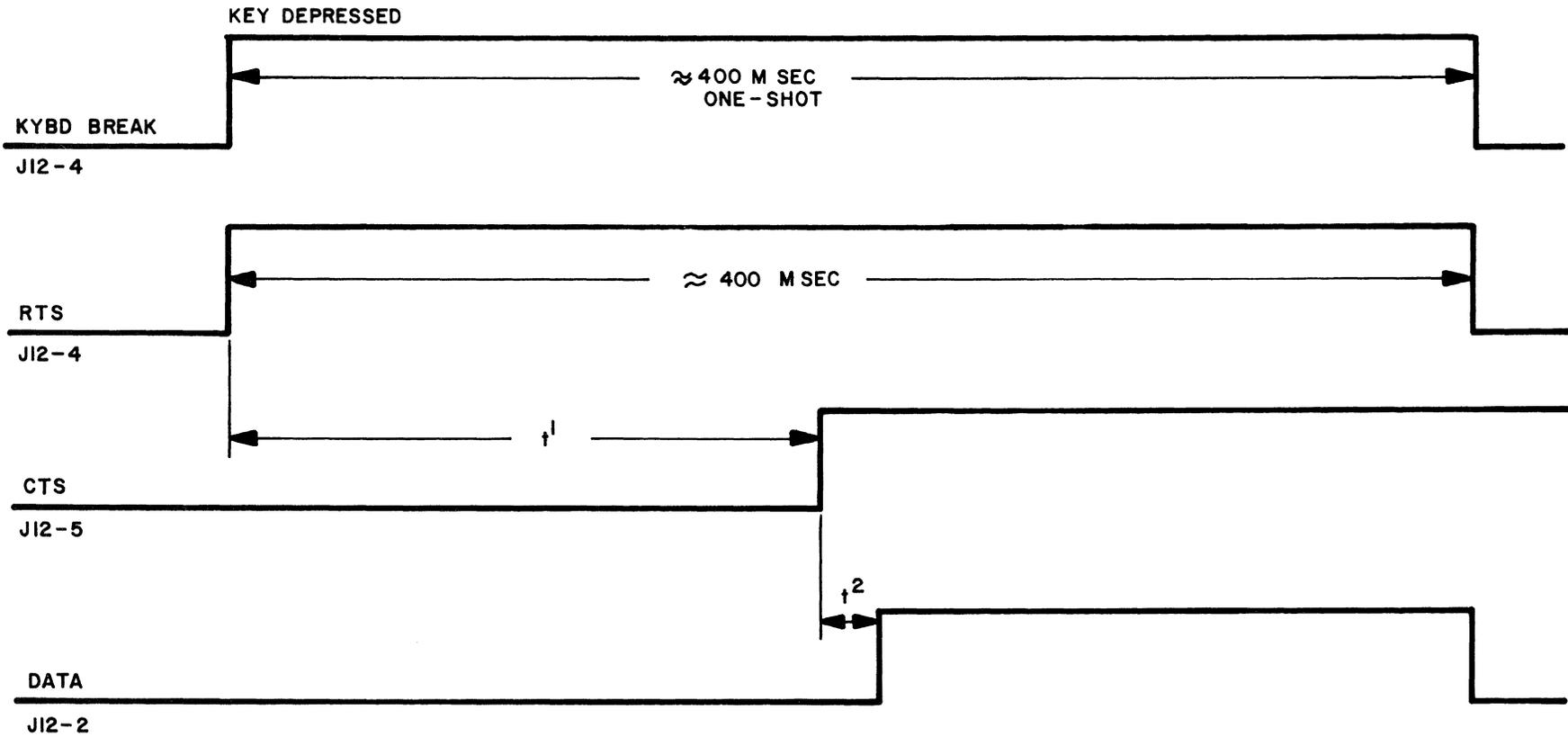


SEE ASCII CODE CHART
FOR BIT SELECTION
LOGICAL 0 = 0V
LOGICAL 1 = +4V

TIMING DIAGRAM
B

NOTE: VOLTAGES INDICATED ARE
NOMINAL AND MAY VARY
 ± 1.0 VOLTS.

6-63/6-64



TERMINAL IN HDX AND ONLINE

$t^1 = \approx 200$ MSEC (DETERMINED BY MODEM)

$t^2 =$ LESS THAN ONE CHARACTER TIME AT THE SPECIFIED BAUD RATE

TIMING DIAGRAM
C

SECTION VII

GLOSSARY OF TERMS

GLOSSARY OF TERMS

<u>A/B</u>	<u>A Clock versus B Clock</u> : When low, memory bank A gets clocked next, B when high.
A MEM OUT 1-8	<u>A Memory Output Buss Bits 1 through 8</u> : Eight-bit character code at A memory bank output.
AØ1, AØ2	<u>A Phase 1 & 2</u> : High voltage clocks driving memory bank A.
<u>ACK</u> (ACK)	<u>Acknowledge</u> : High (Low)-going pulse lasting for one memory clock period, generated whenever functions are output to the display control logic.
<u>ACCESS BUS</u> (Access Bus)	<u>Access Bus</u> : High (Low)-going pulses to allow information onto the uPU Input Bus.
AUTO Ⓛ	<u>Automatic New Line Code</u> : A high level will cause the processor to convert a Carriage Return/Line Feed (CR/LF) into a New Line code. A low level will allow the normal CR/LF function to occur. The signal originates from the auto new line switch on the back panel.
B MEM OUT 1-8	<u>B Memory Output Bus Bits 1 through 8</u> : Eight-bit character code at B memory bank output.
BØ1, BØ2	<u>B Phase 1 & 2</u> : High voltage clocks driving memory bank B.
<u>BELL</u>	<u>Bell</u> : A 2.4kHz signal to activate the bell at character position 72 or when a Control G is decoded.
<u>BK ERS</u> (BK ERS)	<u>Blink Erase</u> : This signal goes high (low) for one circulation of the memory while the Blink Erase function is performed.
<u>BK ERS'</u>	<u>Blink Erase Prime</u> : Low-going pulse identifying the blink codes to be erased by the Blink Erase function.
BLANK 1	<u>Blank Data 1</u> : Characters loaded into line memory while this signal is high will not be displayed.
BLANK 2, 3	<u>Blank Data 2, 3</u> : High (low)-going signals identifying characters at line memory outputs to be blanked.
<u>BLINK</u>	<u>Blink Data</u> : Characters loaded into line memory while this signal is low will blink on the display.
BLINK RATE	<u>Blink Rate Clock</u> : A 1.875 Hz clock.
<u>BREAK</u>	<u>Break</u> : Low going signal which triggers a one-shot pulse lasting approximately 400 msec and interrupts data transmission.
BUFFER READY	<u>Buffer Ready'</u> : A high-going pulse that tells the display board that new data and control data has been stored in the uPU latch bus for the display boards use.
C8	<u>Display Character Counter 8</u> : Bit 3 of the display character counter.

$\overline{\text{C80}}$	<u>Display Character 80</u> : Low for the 20 of every 100 display character times originating horizontal retrace.
CC CLK	<u>Cursor Character Clock</u> : On the rising edge of this signal, the cursor character counter is incremented, loaded or cleared, depending on the state of the load and clear inputs.
$\overline{\text{CC LOAD}}$	<u>Cursor Character Load</u> : Low-going pulse to load cursor character counter. Usually 88 nsec in duration, but sometimes 530 nsec or longer.
$\overline{\text{CL LOAD}}$	<u>Cursor Line Load</u> : Low-going pulse to load cursor line counter. Usually 88 nsec in duration, but sometimes 530 nsec or longer.
CL=ML	<u>Cursor Line Count Equal to Memory Line Count</u> : High-going signal indicating that the cursor is on the same line as the current memory location.
CL>ML	<u>Cursor Line Count Greater than Memory Line Count</u> : High-going signal indicating that the cursor is below the current memory location.
CLEAR TO SEND	<u>Clear to Send</u> : RS-232 Level control signal - When this signal is high, greater than +3.0, or open the terminal is free to transmit to a modem or CPU.
$\overline{\text{CONT. 1 \& JUMP}}$ (CONT 1 & JUMP)	<u>Control One and Jump</u> : Low (high)-going signal which enables the I/O control latch (and the indirect jump latch) to load from the uPU output bus.
$\overline{\text{CONT. 3 \& 4}}$	<u>Control Three and Four</u> : Enables the software control latch to load in conjunction with uPU Out 10'.
$\overline{\text{CRS REQ}}$	<u>Cursor Requested</u> : Goes low when Increment Cursor, Field Tab, Blink Erase, Delete Character, Write Character, Erase-to-End-of-Line, Erase-to-End-of-Screen, or Erase-to-End-of-Field functions are output to the display control logic; goes high when either the cursor is encountered or when it becomes evident that no cursor will ever be encountered.
$\overline{\text{CS1}}, \overline{\text{CS2}}, \overline{\text{CS3}}$ $\overline{\text{CS4}}, \overline{\text{CS5}}, \overline{\text{CS6}},$ $\overline{\text{CS7}}$	<u>Chip Select (Number)</u> : Selects which programmed memory chip is to be enabled.
CURS CHAR 1 - 7	<u>Cursor Character Counter Bit 1 through Bit 7</u> : The binary output of the cursor character counter.
CURS LINE 1 - 8	<u>Cursor Line Counter Bit 1 through Bit 8</u> : The binary output of the cursor line counter.
$\overline{\text{CURSOR 1}}$	<u>Display Cursor 1</u> : The cursor will be displayed on the line loaded while this signal is low.
$\overline{\text{CURSOR 2}}$	<u>Display Cursor 2</u> : Low when cursor will be displayed somewhere on the current display line.
$\overline{\text{CURSOR INPUT}}$	<u>Cursor Input</u> : A low pulse will enable the cursor character number or cursor line number on to the uPU input bus.

CURSOR WORD

Cursor Word: A low-going pulse which enables the 8 bits representing the character above the cursor on to the uPU input bus. Signal source is I/O processor board.

CWR'

Cursor Word Ready': A low-going pulse from the display board which allows the processor to run to input the character under the cursor. If the signal is high when trying to input the character, the ready line to the processor will drop, stopping the processor. This signal works in conjunction with Mem Done and Buffer Ready.

DATA TERM READY

Data Terminal Ready: RS-232 Level Control signal, which is +14 Vdc whenever power is on and which indicates to a modem or CPU that the terminal is ready to receive data (if Request-to-Send is low).

DC=CC

Display Character Count Equal to Cursor Character Count: High-going signal indicating that the cursor is in the same vertical column as the character at the line memory output.

DC>CC

Display Character Count Greater than Cursor Character Count: High-going signal indicating that the character in the Line Memory Output is greater than the cursor column position.

DC 79

Display Character 79: Low-going decode designating the last character on any display line.

DE SKIP

Memory Reference Counters Inhibit: Low-going signal to inhibit the home, memory character and memory line counters for one memory clock pulse at the conclusion of the Delete Character function.

DEL
(DEL)

Delete Character: Goes low (high) when Delete Character function is requested; stays low until a different function is output to the display control circuitry.

DESCENDER 1

Descender Code 1: Low-going signal identifying g, j, p, q and y codes in memory.

DESCENDER 2

Descender Code 2: Low-going signal identifying g, j, p, q and y codes at line memory output.

DISPLAY
DOT 1-5

Display Dot 1 through 5: Five-dot representation of that portion of the current character at the level of the current scan.

DOWN

Memory Reference Down Count: Low-going signal generated at the conclusion of each memory scroll to relate between the memory and the cursor home and character counters.

ENABLE'

Enable Prime: Resets transmit buffer empty flip-flop.

ENABLE IND. JUMP

Enable Indirect Jump: Enables the indirect jump latch to output the uPU input bus.

END PAGE

End of Page: Low-going pulse lasting for the 3 line times prior to the display of the top line.

<u>ENTRY</u> (ENTRY)	<u>Program Entry Mode</u> : Set high (low) when the terminal is in Program Entry mode.
<u>EOL</u> (EOL)	<u>Erase to End of Line</u> : Goes low (high) when Erase-to-End-of-Line function is requested; stays low until a different function is output to the display control circuitry.
<u>EXT. CLK ENABLE</u>	<u>External Clock Enable</u> : A low signal disables the internal clock and enables the receiver to use the external clock.
<u>F TAB</u>	<u>Field Tab</u> : Goes low when Field Tab function is requested; stays low until a different function is output to the display control logic.
<u>FDX</u>	<u>Full-Duplex</u> : A high level will cause the terminal to transmit and receive in the full-duplex mode. A low level will cause the terminal to operate in the half-duplex mode.
<u>FIRST LINE</u>	<u>First Line</u> : Low going pulse which enables first line latch and status word 2 multiplexer onto the uPU input bus.
<u>FL LOAD</u>	<u>First Line Load</u> : Low-going pulse to load first line counter, usually 88 nsec duration but sometimes 530 nsec or longer.
<u>FMT LIGHT</u>	<u>Format Light</u> : A low level will turn the keyboard Format light on.
FORMAT	<u>Format Mode</u> : Set high when the terminal is in Format mode.
<u>FP1</u>	<u>Format Protect 1</u> : Low-going pulse identifying protected characters in memory, except when the Delete Character function is being executed.
<u>FP2</u>	<u>Format Protect 2</u> : Low-going pulse identifying protected characters in memory when executing the Delete Character, Erase-to-End-of-Field and certain other functions.
<u>H TAB</u>	<u>Horizontal Tab</u> : Low-going pulse generated when Tab Clear, Tab Set, Tab Erase or Horizontal Tab functions are output to the display control logic, and lasting long enough to insure that the horizontal tab control logic can recognize it.
<u>H TAB + ERASE</u>	<u>Horizontal Tab or Tab Erase</u> : Low-going signal indicating that a Horizontal Tab or Tab Erase function is being executed.
<u>H TAB REQ</u>	<u>Horizontal Tab Requested</u> : Low-going signal indicating that a Tab Clear, Tab Set, Tab Erase or Horizontal Tab function is to be performed.
<u>HOME</u> (HOME)	<u>Home Location</u> : High (low)-going pulse identifying the last position in memory.
HORIZ DRIVE	<u>Horizontal Drive</u> : High-going pulse to synchronize the horizontal sweep of the CRT monitor.
<u>INC</u>	<u>Increment Cursor</u> : Goes low when Increment Cursor function is requested and stays low until a different function is output to the display control logic.
INS CHAR	<u>Insert Character Mode</u> : Set high when the terminal is in Insert Character mode.

<u>INSERT CHAR LIGHT</u>	<u>Insert Character Light</u> : A low level will turn the keyboard insert character light on.
<u>INSERT DATA</u>	<u>Insert Data Latch Enable</u> : Low-going signal enabling the insert data latch onto the memory input bus.
<u>INT. CLOCK</u>	<u>Internal Clock</u> : Output clock to switchboard to provide TTL transmit clock to external devices (strappable).
I/O 11 BIT WORD	<u>I/O 11 Bit Word</u> : Indicates that data has two stop bits at the end of each byte.
I/O CLOCK	<u>I/O Clock</u> : Baud rate selected clock which clocks the data into the receiver.
I/O RCVD DATA	<u>I/O Received Data</u> : RS-232 Level data received via the I/O connector from a modem or CPU.
I/O RECEIVER ENABLE	<u>I/O Receiver Enable</u> : A high signal enables the receiver buffer. $\overline{\text{Empty}}$ flag which, when admitted onto the uPU input Bus, indicates that the received data is ready to be entered.
I/O TRANSMIT ENABLE	<u>I/O Transmit Enable</u> : A high signal indicates that the data is to be transmitted out at the proper time.
JAM RESET	<u>Jam Reset</u> : Low-going pulse interrupts uPU and forces an octal 05 on to the uPU input bus, which reinitializes the software.
<u>KBD 2⁰</u>	<u>Keyboard 2⁰</u> : The least significant bit of A. 8-bit parallel keyboard output. $\overline{\text{The output}}$ is negative logic (i.e., a low level equals the true state).
<u>KBD 2¹</u>	<u>Keyboard 2¹</u> : The second least significant bit from the keyboard.
<u>KBD 2²</u>	<u>Keyboard 2²</u> : The third least significant bit from the keyboard.
<u>KBD 2³</u>	<u>Keyboard 2³</u> : The fourth least significant bit from the keyboard.
<u>KBD 2⁴</u>	<u>Keyboard 2⁴</u> : The fifth least significant bit from the keyboard.
<u>KBD 2⁵</u>	<u>Keyboard 2⁵</u> : The sixth least significant bit from the keyboard. If lower case enable is "not true" and if KBD 2 ⁵ is "true", KBD 2 ⁵ gets converted to the "not" state.
<u>KBD 2⁶</u>	<u>Keyboard 2⁶</u> : The seventh least significant bit from the keyboard.
<u>KBD 2⁷</u>	<u>Keyboard 2⁷</u> : The eighth least significant bit from the keyboard.
<u>KBD & CONT.</u>	<u>Keyboard and Control</u> : Enables keyboard or I/O control multiplexers onto the uPU output bus.
<u>KBD ACK</u>	<u>Keyboard Acknowledges</u> : A low-going pulse which acknowledges the receipt of a character from the keyboard.
<u>KBD REQD</u>	<u>Keyboard Request</u> : A low-going level which tells the processor that the keyboard has a character waiting to be input.

<u>KEYBOARD ENABLE</u>	<u>Keyboard Enable</u> : A high-going level which allows the keyboard to input character to the processor. A continuing low level totally locks the keyboard.
LINE 1, 2	<u>Display Line Counter Outputs 1, 2, 8, 16</u> : Bits 1, 2, 4, and 5 of the binary display line number.
LINE RESET	<u>Display Line Reset</u> : Resets the display line counter.
<u>LOWER CASE ENABLE</u>	<u>Lower Case Enable</u> : A low level will cause all lower case characters from keyboard to be converted to upper case characters. The switchboard is the signal source.
MC=CC	<u>Memory Character Count Equal to Cursor Character Count</u> : High-going signal indicating that the cursor is in the same vertical column as the current memory location.
MC<CC	<u>Memory Character Count Less than Cursor Character Count</u> : High-going signal indicating that the cursor position is to the right of the current memory location.
<u>MC 79</u>	<u>Memory Character 79</u> : Low-going decode identifying the 80th character of any line having 80 characters.
<u>MEM A/B</u>	<u>Memory A versus Memory B</u> : Memory blank A is seen at the memory output when this signal is low, memory bank B is seen when signal is high.
MEM BUS 1-8	<u>Memory Output Bus Bits 1 through 8</u> : Eight-bit character code at memory input.
MEM CHAR 1-7	<u>Memory Character Counter Bit 1 through Bit 7</u> : The binary output of the memory character counter.
<u>MEM CLK</u> (MEM CLK)	<u>Memory Clock</u> : Clock for the display memory.
MEM CLK'	<u>Memory Clock Prime</u> : Buffered version of MEM CLK.
<u>MEM. DEV. & RCVR</u>	<u>Memory Device and Receiver</u> : In conjunction with uPU Out 10'. Enables the receiver buffer onto the uPU input bus, also enables MEM DEV 4.
MEM DEV. No. 4	<u>Memory Device Number 4</u> : Selects the cursor word latch to output onto the uPU input bus at the proper time. (See <u>Cursor Word</u>)
<u>MEM. DECODE</u>	<u>Memory Decode</u> : When combined with uPU Out 13 generates Mode Latch Load.
<u>MEM DONE</u> (MEM DONE)	<u>Memory Done</u> : A low (high)-going pulse allows the processor to run by raising the ready line during any input from the display. If this signal is high (low), indicating that the memory is not done, the ready line will drop and the processor will wait until memory gets done before inputting a cursor word, cursor line number, cursor character number first line or status word number 2. Signal source is the display board.

MEM. LATCH LOAD	<u>Memory Latch Load</u> : Allows memory latch to load after $\overline{\text{PRE 13}}$ is decoded from the uPU.
MEM LINE 1-8	<u>Memory Line Counter Bit 1 through Bit 8</u> : The binary output of the memory line counter.
MEM OUT	<u>Memory Output Bus Bits 1 through 8</u> : Eight-bit character code at memory output.
MEM OUT $6 \oplus 7$	<u>Memory Output Bus Bit 6 Exclusive or 7</u> : The exclusive or function of bits 6 and 7 on the memory output bus. High enables upper case, low enables lower case.
ML ENABLE	<u>Memory Line Enable</u> : High-going pulse, one memory clock period in duration, identifying the end of each line of memory.
MODE'	<u>Mode Latch Clock</u> : High-going pulse to load certain mode latch bits into a secondary mode latch. Usually 88 nsec duration, but sometimes 530 nsec or longer.
$\overline{\text{MODE \& SOFTWARE}}$	<u>Mode Control and Software Control</u> : Enables mode control and software control multiplexers onto the uPU input bus.
MODE LATCH LOAD	<u>Mode Latch Load</u> : Allows the mode control latch to load data from the uPU output bus.
$\overline{\text{NEW DATA}}$	<u>New Data Latch Enable</u> : Low-going signal enabling the new data latch onto the memory input bus.
$\overline{\text{NON-X'}}$ $\overline{(\text{NON-X'})}$	<u>Non-existent Prime</u> : High (low)-going pulse indicating that the cursor is not in memory.
$\overline{\text{NON-X1}}$	<u>Non-Existant 1</u> : Low-going pulse indicating that the cursor is below the end of memory.
$\overline{\text{NON-X2}}$	<u>Non-Existant 2</u> : Low-going pulse indicating that the cursor is to the right of the memory.
$\overline{\text{NRC}}$	<u>Non-Requested Cursor</u> : Goes low for one memory clock period whenever the cursor position is encountered in memory, except when the cursor requested flip-flop is set.
NXT LINE 1-8	<u>Next Line Counter Bit 1 through Bit 8</u> : The binary output of the first line counter.
$\overline{01}$	<u>Phase 1</u> : Processor clock Phase 1, Freq. equals 758 kHz. Signal source is the display board.
02	<u>Phase 2</u> : Processor clock phase 2, Freq. equals 758 kHz. Signal source is the display board.
$\overline{0/1}, \overline{1/2}, \overline{2/3},$ $\overline{3/4}, \overline{4/5}, \overline{5/6}$	<u>Double Dots 0 and 1, 1 and 2, 2 and 3, 3 and 4, 4 and 5, 5 and 6</u> : A sequence of low-going pulses, each low for two out of every seven oscillator pulses.

<u>ON LINE LIGHT</u>	<u>On Line Light</u> : A low level will turn the keyboard On-Line light on.
OSC	<u>Oscillator</u> : An 11.34 MHz clock.
<u>OVERWRITE</u>	<u>Memory Scroll</u> : Low-going signal indicating that the end of memory has been overwritten. First line of data is lost.
PAGE	<u>Page Edit Mode</u> : Set high when the terminal is in Page Edit mode.
<u>PAGE EDIT LIGHT</u>	<u>Page Edit Light</u> : A low level will turn the keyboard Page Edit Light on.
PARITY ERROR	<u>Parity Error</u> : High-going signal identifying parity error codes (octal 32) in memory.
PARITY TEST	<u>Parity Test</u> : A high signal enables the receiver to test for proper parity, and the transmitter to send proper parity. A low signal ignores parity.
PREVIOUS WAS ESC.	<u>Previous was Escape</u> : A flag which indicates the previous code from the keyboard was an escape code.
<u>PRE T3</u>	<u>Pre T3</u> : Low-going signal generating access bus, also is used to load memory bus when the processor has selected a display function.
<u>PRINT ON LINE LIGHT</u>	<u>Print on Line Light</u> : A low level will turn the keyboard Print On Line light on.
PRINTER CLOCK	<u>Printer Clock</u> : Baud rate strappable clock which clocks the data into the receiver and/or out of the transmitter to the printer.
PRINTER DATA	<u>Printer Data</u> : RS-232 Level data transmitted from the terminal to printer via the printer connector. NOTE: transmit data and printer data cannot be transmitted simultaneously.
PRINTER ENABLE	<u>Printer Enable</u> : A high signal enables the terminal to output data to the printer.
PRINTER READY	<u>Printer Ready</u> : High-going pulse which indicates printer is ready to receive data (similar to Clear-to-Send). (RS232)
<u>PRINTER STATUS</u>	<u>Printer Status</u> : Printer is On Line and operating correctly.
<u>PROG. ENTRY LIGHT</u>	<u>Program Entry Light</u> : A low level will turn the keyboard Program Entry light on.
PROT BIT	<u>Protect Bit</u> : Set high when bit 8 (MSB) of new data written into memory is to be set high.
PTR 10 BIT WORD	<u>PTR 10 Bit Word</u> : Indicates that printer data has one stop bit at the end of each byte.
<u>RCVD. SIG. DET.</u>	<u>Received Signal Detect</u> : Goes high (+3Vdc or greater) when modem has established a carrier. Allows data from modem to be received by the terminal. A low level (1-3 Vdc or less) prevents terminal from receiving an RS-232 signal.

<u>RCVR BUFFER EMPTY</u>	<u>Receiver Buffer Empty</u> : A low-going signal which indicates that the receiver buffer is full and ready to enter onto the uPU input bus.
<u>RCVR. DEV.</u>	<u>Receiver Device</u> : Enable the receiver buffer to load onto the uPU input bus and resets the receiver buffer full flip-flop.
RCVR. SIG. ELE.	<u>Receiver Signal Element</u> : RS-232 level clock received from the external data source via the I/O connector. This clock is synchronized with I/O received data.
RECEIVER CLOCK	<u>Receiver Clock</u> : Internal baud rate dependent on external clock which clocks data into the receiver.
<u>RECIRC</u>	<u>Recirculate Gates Enable</u> : Low-going signal enabling the recirculate multiplexers onto the memory input bus.
REQUEST TO SEND	<u>Request to Send</u> : RS-232 Level control signal which is normally at - 11Vdc goes to +14Vdc, when terminal wants to transmit data.
<u>RESET</u>	<u>Reset</u> : A low-going pulse coming from the keyboard "Reset" key which interrupts the processor and restarts the firm-ware program.
REV VID 1, 2, 3, 4,	<u>Reverse Video Data 1 - 4</u> : Characters loaded into line memory while these signals are high, low, high and low respectively, will be displayed in reverse video.
REV VIDEO 5, 7, 8	<u>Reverse Video 5, 7, 8</u> : When high, low, high will reverse the video display of data currently at the line memory outputs.
<u>RTSP</u>	<u>Request to Send Pulse</u> : A low pulse of approximately 300 msec (minimum 200 msec) which loads an octal 10 into the bit counter.
SCAN 1, 2, 4, 8	<u>Display Scan Counter Outputs 1, 2, 4, 8</u> : Binary number of the current scan number within each line.
<u>SCAN 9</u>	<u>Display Scan 9</u> : Low-going signal identifying the last scan of each line.
<u>SKIP</u>	<u>Move Cursor Forward</u> : Low-going signal used to move the cursor through memory in execution of Increment Cursor, Field Tab and Write functions.
<u>SKIP'</u> (SKIP')	<u>Move Cursor Forward Prime</u> : High (low)-going signal indicating that the cursor is moving through memory in the course of a Field Tab function.
SP	<u>Space Code</u> : High-going signal identifying space codes (octal 40) in memory.
<u>START DEL</u>	<u>Start Delete</u> : Low-going signal to initiate execution of the Delete Character function; one memory clock period in duration.
STOP	<u>Stop Clocking Memory</u> : High-going signal synchronizing the memory to the display.
<u>SYNC</u> (SYNC)	<u>Synchronous</u> : A low (high) signal enables the Sync. code to allow the bit counter to run.
<u>SYNC. SEARCH</u>	<u>Synchronous Search</u> : Prevents the bit counter from running until a Sync. code is received. (Synchronous mode only)

T SCROLL	<u>Test Scroll</u> : A low signal indicates that 2 bits have been received and will not have time to perform a scroll. A high signal tests for scroll.
$\overline{T11}$	<u>T-One Interrupt Prime</u> : A or B input selector for the memory multiplexer. A low signal selects the A input which is an octal 15 and resets the software program. A high signal selects the memory data.
TAB ERASE	<u>Tab Erase</u> : High-going signal indicating that a Tab Erase is being executed.
$\overline{TAB LOAD}$	<u>Tab Memory Load</u> : Low-going pulse enabling alteration of the bits in the tab memory.
TAB OUT	<u>Output of the Tab Memory</u> : Low level indicates tab is set, high indicates clear.
TAB SKIP	<u>Horizontal Tab Move Cursor Forward</u> : High-going signal enabling increment of the cursor character counter for the Horizontal Tab function.
TERM SIG. ELE.	<u>Terminal Signal Element</u> : External clock which clocks the data into the transmitter. (RS-232)
\overline{TOC} (TOC)	<u>Turn On Clear</u> : A high (low) pulse of approximately 300 msec to establish an initialized condition on the I/O processor board when the terminal is powered up.
$\overline{TRANSMIT BUFFER FULL}$	<u>Transmit Buffer Full</u> : A high signal indicating the transmitter buffer is full.
$\overline{TRANSMIT COMPLETE}$	<u>Transmit Complete</u> : A low pulse indicating that the transmitter has clocked out 8, 10, or 11 bits and is ready to receive the next byte from the uPU output bus.
TRANSMIT DATA	<u>Transmit Data</u> : RS-232 level data transmitted from the terminal to a modem or CPU through the I/O connector.
$\overline{TRANSMITTER 1 \& 2}$	<u>Transmitter One and Two</u> : Enables the uPU output bus to load across the transmitter buffer and into the transmitter. Also, resets the transmitter buffer empty flip-flop.
$\overline{TRANSMITTER \& BELL}$	<u>Transmitter and Bell</u> : A low-going pulse which triggers a one-shot for the bell circuit.
uPU INPUT BUS	<u>uPU Input Bus</u> : Tri-State processor data lines which have output data during T1 and T2 times and input data on them at T3 time. These lines go to display board.
uPU INPUT BUS BITS 1-8	<u>uPU Input Bus</u> : Input (Output) bus to (from) the central processor chip (uPU).
uPU L10', 11', 12', 13'	<u>uPU Latch Bit 10', 11', 12', 13'</u> : Latched forms of uPU I 10, 11, 12, 13.
uPU LATCH BUS 10-13	<u>uPU Latch Bus Control Bits 10, 11, 12, 13</u> : Four-bit control codes temporarily stored in the I/O board for use by the display board upon demand.
uPU OUTPUT BUS BITS 1 to 8	<u>uPU Output Bus Bits 1 thru 8</u> : Outputs from the uPU thru the T1 latch to the memory latch, etc.

$\overline{\text{uPU OUT 1}}$	<u>uPU Out 1</u> : Data stored in the least significant bit location of T1 latch. This data is updated every time the 8008-1 processor cycle through a T1 time. Signal source is the I/O processor board.
uPU OUT 9	<u>uPU Out 9</u> : Output from T2 latch to I/O decoder to generate chip selects.
uPU OUT 10	<u>uPU Out 10</u> : Control data store in next least significant bit location of the I/O processor T2 latch. This signal is used to select between cursor character number (low) or cursor line number (high) and available to display board on demand.
uPU OUT 11-13	<u>uPU Out 11</u> : Output from T2 latch to I/O decoders used to generate various functions on the I/O processor board and available on demand to the display board.
uPU OUT 15:	<u>uPU Out 15</u> : A high pulse used to (help) generate the memory multiplexer enable at proper time.
$\overline{\text{VERT DRIVE}}$	<u>Vertical Drive</u> : Low-going pulse to synchronize the vertical sweep of the CRT monitor.
VIDEO	<u>Video Drive</u> : Drive signal for the CRT electron gun; high for white, low for black.
VIDEO'	<u>Video Drive</u> : Same as Video but for Composite Video.
$\overline{\text{WRITE}}$	<u>Write</u> : Goes low when Write function is requested; stays low until a different function is output to the display control logic.
X-MIT BUFFER EMPTY	<u>Transmit Buffer Empty</u> : High-going signal which indicates that the transmitter has received a new data word.
X-MIT CARRY	<u>Transmit Carry</u> : Carry Out from transmit bit counter which indicates either a 10-or 11-bit word has been clocked out.
XMIT SIG. ELE. TIMING	<u>Transmit Signal Element Timing</u> : RS-232 level clock transmitted to the external data source via the I/O connector. This clock synchronizes the transmit data from the terminal to the external data source.
2ND SP	<u>Second Space Code</u> : High-going signal identifying those space codes in memory which are preceded by space codes.
2X BLINK	<u>2 Times Blink Rate Clock</u> : A 3.75 Hz clock.
$\frac{80 \text{ CLK}}{(80 \text{ CLK})}$	<u>80 Pulse Clock</u> : High (low)-going signal clocking 80 times for every display scan.
⌚	<u>New Line Code</u> : High-going signal identifying new line code (octal 37) in memory.
$\text{⌚} \overline{\text{PROT}}$	<u>New Line Protect</u> : Low-going pulse identifying new line codes when executing the Erase-to-End-of-Line function.

APPENDIX A

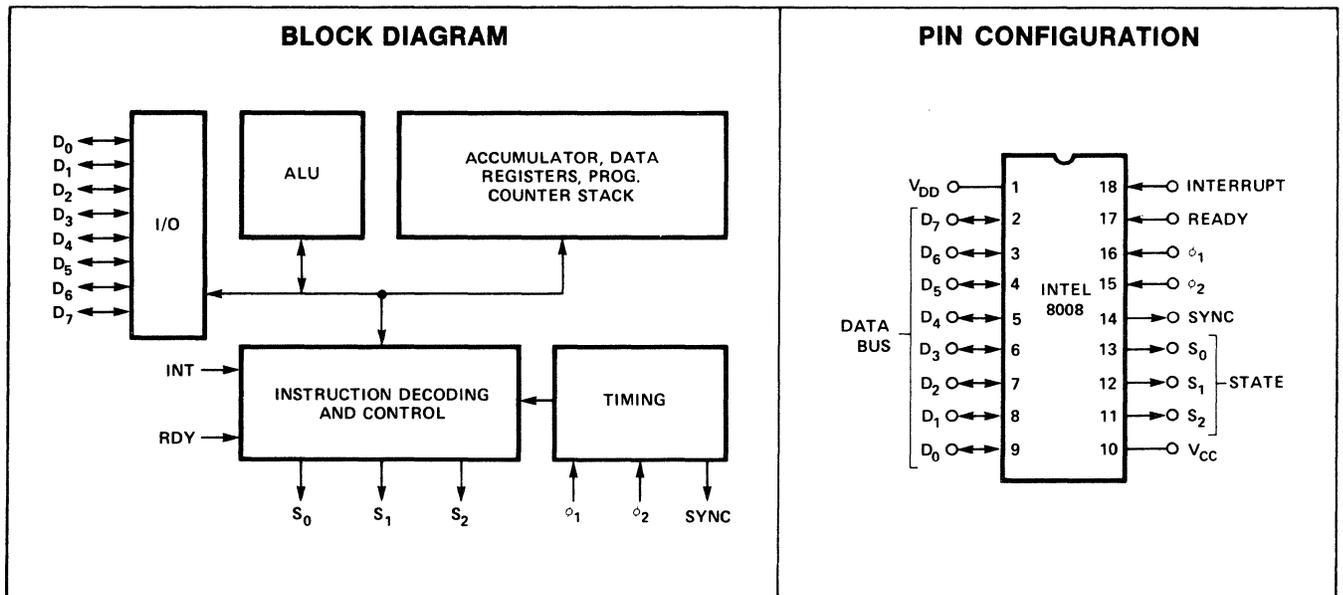
EIGHT BIT PARALLEL CENTRAL PROCESSOR UNIT

8 BIT PARALLEL CENTRAL PROCESSOR UNIT

The 8008 is a complete computer system central processor unit which may be interfaced with memories having capacities up to 16K bytes. The processor communicates over an 8-bit data and address bus and uses two leads for internal control and four leads for external control. The CPU contains an 8-bit parallel arithmetic unit, a dynamic RAM (seven 8-bit data registers and an 8x14 stack), and complete instruction decoding and control logic.

Features

- 8-Bit Parallel CPU on a Single Chip
- 48 Instructions, Data Oriented
- Complete Instruction Decoding and Control Included
- Instruction Cycle Time — 12.5 μ s with 8008-1 or 20 μ s with 8008
- TTL Compatible (Inputs, Outputs and Clocks)
- Can be used with any type or speed semiconductor memory in any combination
- Directly addresses 16K x 8 bits of memory (RAM, ROM, or S.R.)
- Memory capacity can be indefinitely expanded through bank switching using I/O instructions
- Address stack contains eight 14-bit registers (including program counter) which permit nesting of subroutines up to seven levels
- Contains seven 8-bit registers
- Interrupt Capability
- Packaged in 18-Pin DIP



I. INTRODUCTION

The 8008 is a single chip MOS 8-bit parallel central processor unit for the MCS-8 micro computer system. A micro computer system is formed when the 8008 is interfaced with any type or speed standard semiconductor memory up to 16K 8-bit words. Examples are INTEL's 1101, 1103, 2102 (RAMs), 1302, 1602A, 1702A (ROMs), 1404, 2405 (Shift Registers).

The processor communicates over an 8-bit data and address bus (D_0 through D_7) and uses two input leads (READY and INTERRUPT) and four output leads (S_0 , S_1 , S_2 and Sync) for control. Time multiplexing of the data bus allows control information, 14 bit addresses, and data to be transmitted between the CPU and external memory.

This CPU contains six 8-bit data registers, an 8-bit accumulator, two 8-bit temporary registers, four flag bits, and an 8-bit parallel binary arithmetic unit which implements addition, subtraction, and logical operations. A memory stack containing a 14-bit program counter and seven 14-bit words is used internally to store program and subroutine addresses. The 14-bit address permits the direct addressing of 16K words of memory (any mix of RAM, ROM or S.R.).

The control portion of the chip contains logic to implement a variety of register transfer, arithmetic control, and logical instructions. Most instructions are coded in one byte (8 bits); data immediate instructions use two bytes; jump instructions utilize three bytes. Operating with a 500kHz clock, the 8008 CPU executes non-memory referencing instructions in 20 microseconds. A selected device, the 8008-1, executes non-memory referencing instructions in 12.5 microseconds when operating from an 800kHz clock.

All inputs (including clocks) are TTL compatible and all outputs are low-power TTL compatible.

The instruction set of the 8008 consists of 48 instructions including data manipulation, binary arithmetic, and jump to subroutine.

The normal program flow of the 8008 may be interrupted through the use of the "INTERRUPT" control line. This allows the servicing of slow I/O peripheral devices while also executing the main program.

The "READY" command line synchronizes the 8008 to the memory cycle allowing any type or speed of semiconductor memory to be used.

STATE and SYNC outputs indicate the state of the processor at any time in the instruction cycle.

II. PROCESSOR TIMING

The 8008 is a complete central processing unit intended for use in any arithmetic, control, or decision-making system. The internal organization is centered around an 8-bit internal data bus. All communication within the processor and with external components occurs on this bus in the form of 8-bit bytes of address, instruction or data. (Refer to the accompanying block diagram for the relationship of all of the internal elements of the processor to each other and to the data bus.) For the MCS-8 a logic "1" is defined as a high level and a logic "0" is defined as a low level.

A. State Control Coding

The processor controls the use of the data bus and determines whether it will be sending or receiving data. State signals S_0 , S_1 , and S_2 , along with SYNC inform the peripheral circuitry of the state of the processor. A table of the binary state codes and the designated state names is shown below.

S_0	S_1	S_2	STATE
0	1	0	T1
0	1	1	T1I
0	0	1	T2
0	0	0	WAIT
1	0	0	T3
1	1	0	STOPPED
1	1	1	T4
1	0	1	T5

B. Timing

Typically, a machine cycle consists of five states, two states in which an address is sent to memory (T1 and T2), one for the instruction or data fetch (T3), and two states for the execution of the instruction (T4 and T5). If the processor is used with slow memories, the READY line synchronizes the processor with the memories. When the memories are not available for either sending or receiving data, the processor goes into the WAIT state. The accompanying diagram illustrates the processor activity during a single cycle.

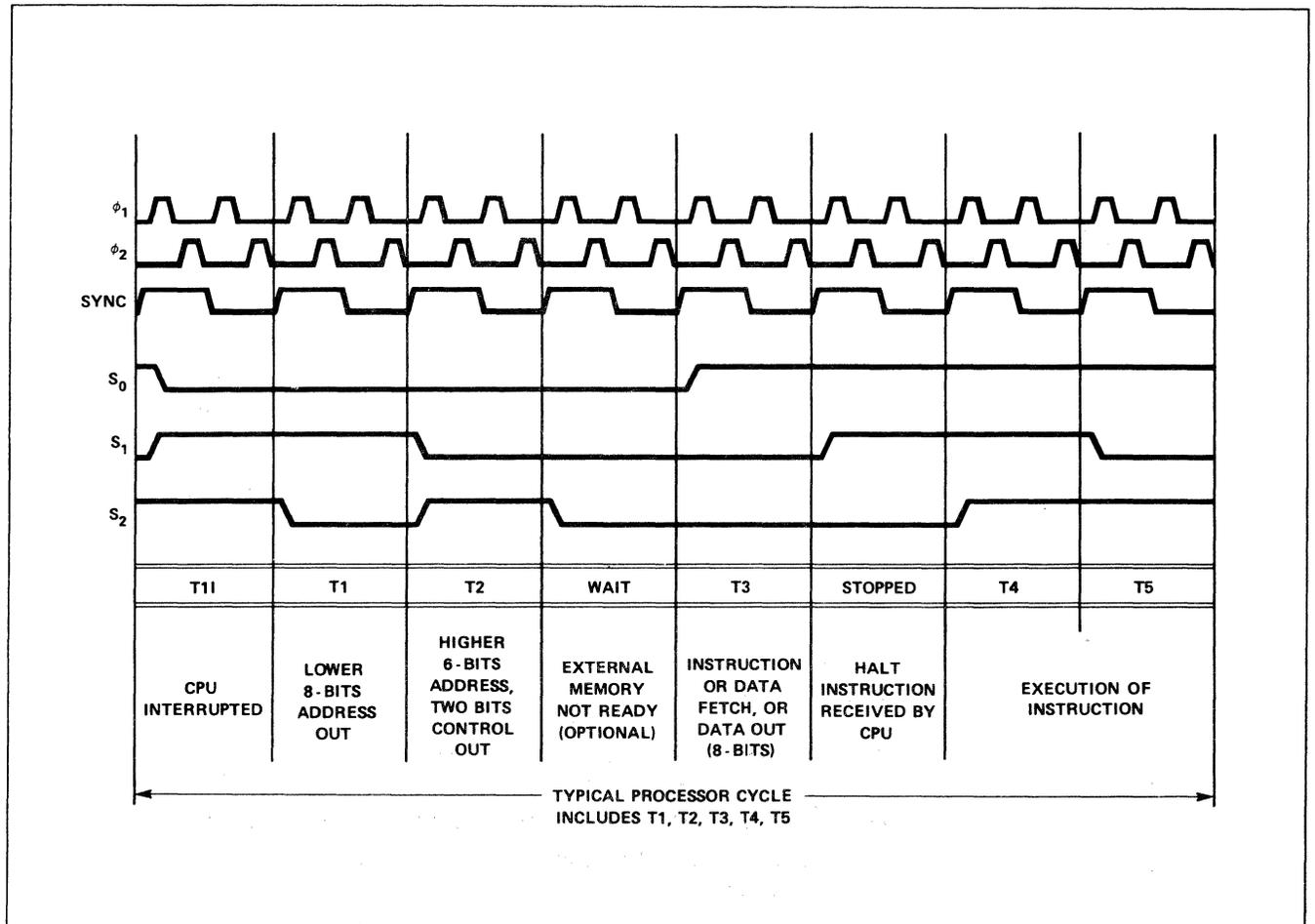


Figure 1. Basic 8008 Instruction Cycle

The receipt of an INTERRUPT is acknowledged by the T11. When the processor has been interrupted, this state replaces T1. A READY is acknowledged by T3. The STOPPED state acknowledges the receipt of a HALT instruction.

Many of the instructions for the 8008 are multi-cycle and do not require the two execution states, T4 and T5. As a result, these states are omitted when they are not needed and the 8008 operates asynchronously with respect to the cycle length. The external state transition is shown below. Note that the WAIT state and the STOPPED may be indefinite in length (each of these states will be 2n clock periods). The use of READY and INTERRUPT with regard to these states will be explained later.

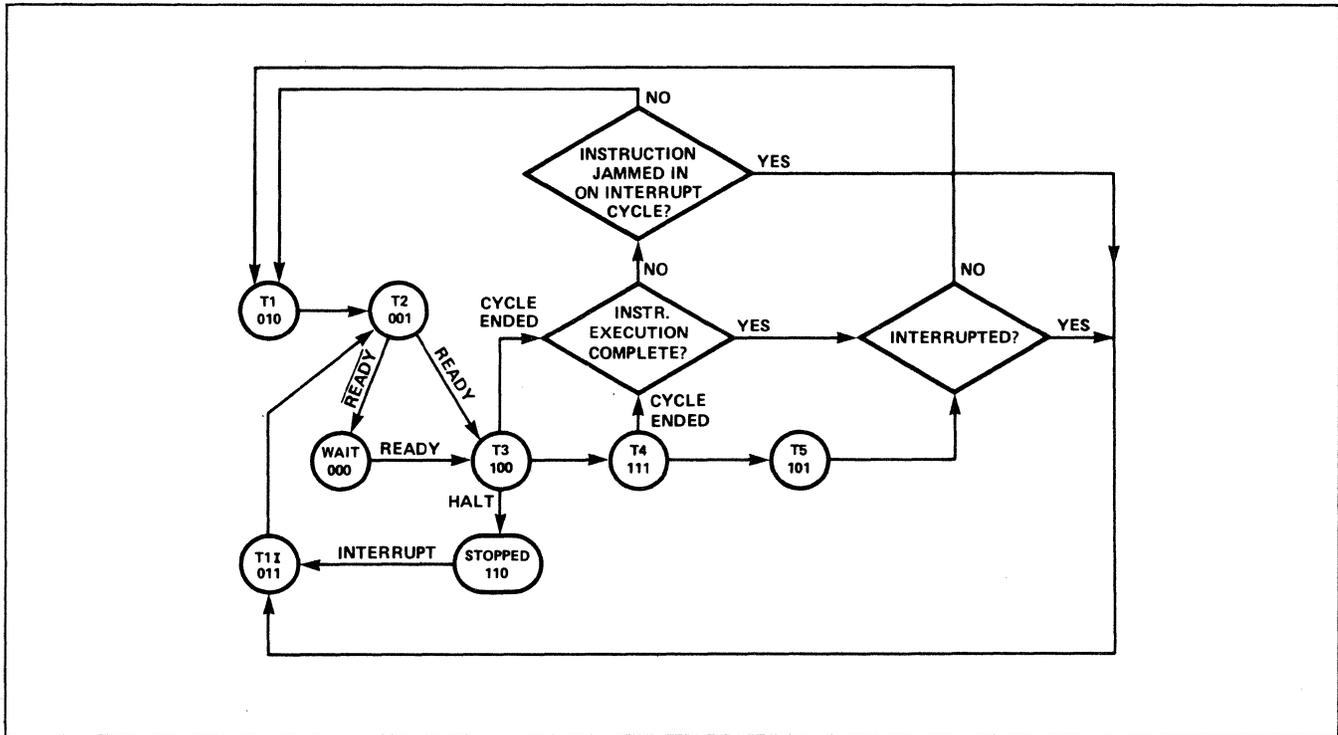


Figure 2. CPU State Transition Diagram

C. Cycle Control Coding

As previously noted, instructions for the 8008 require one, two, or three machine cycles for complete execution. The first cycle is always an instruction fetch cycle (PCI). The second and third cycles are for data reading (PCR), data writing (PCW), or I/O operations (PCC).

The cycle types are coded with two bits, D_6 and D_7 , and are only present on the data bus during T2.

D_6	D_7	CYCLE	FUNCTION
0	0	PCI	Designates the address is for a memory read (first byte of instruction).
0	1	PCR	Designates the address is for a memory read data (additional bytes of instruction or data).
1	0	PCC	Designates the data as a command I/O operation.
1	1	PCW	Designates the address is for a memory write data.

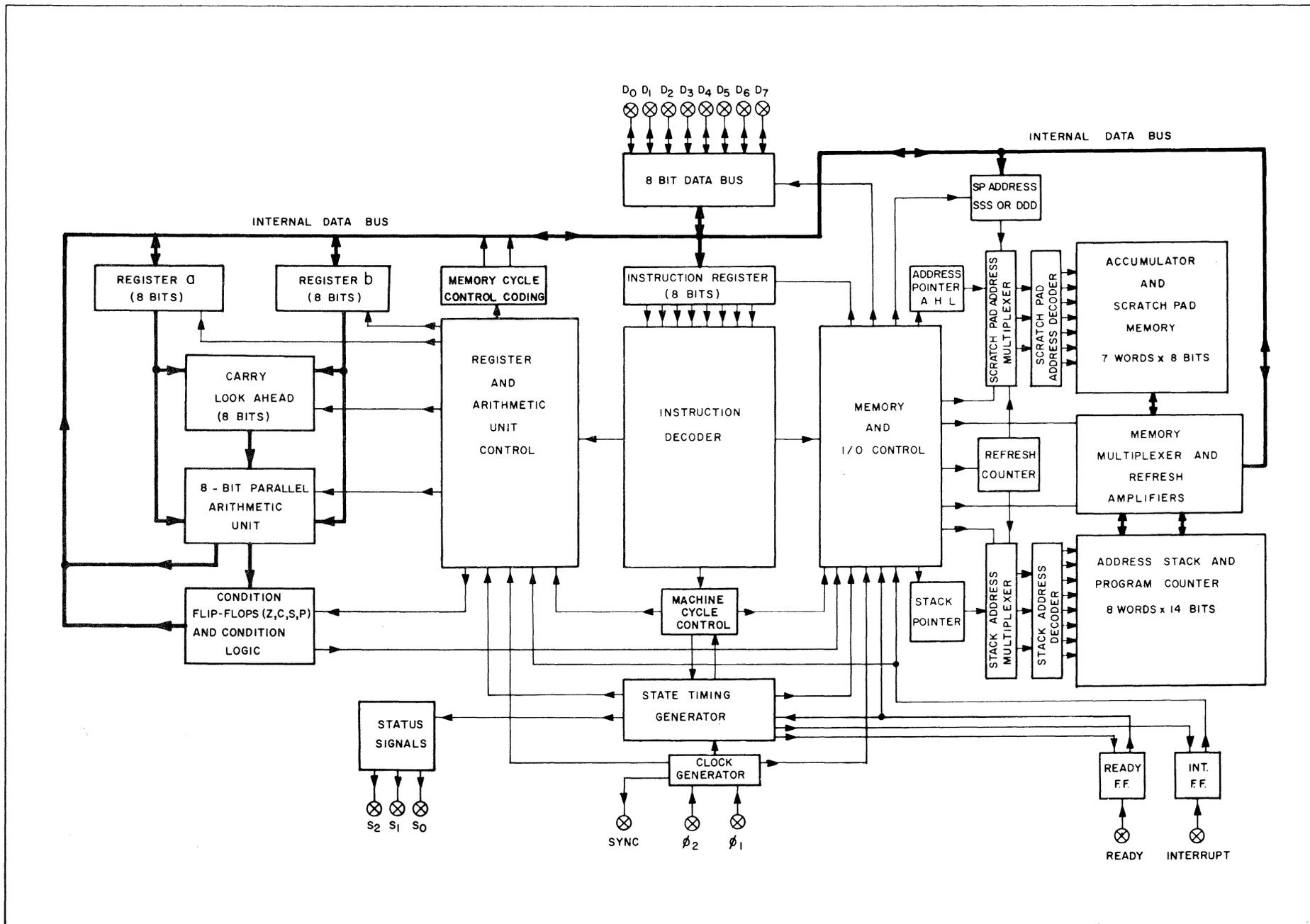


Figure 3. 8008 Block Diagram

III. BASIC FUNCTIONAL BLOCKS

The four basic functional blocks of this Intel processor are the instruction register, memory, arithmetic logic unit, and I/O buffers. They communicate with each other over the internal 8-bit data bus.

A. Instruction Register and Control

The instruction register is the heart of all processor control. Instructions are fetched from memory, stored in the instruction register, and decoded for control of both the memories and the ALU. Since instruction executions do not all require the same number of states, the instruction decoder also controls the state transitions.

B. Memory

Two separate dynamic memories are used in the 8008, the pushdown address stack and a scratch pad. These internal memories are automatically refreshed by each WAIT, T3, and STOPPED state. In the worst case the memories are completely refreshed every eighty clock periods.

1. Address Stack

The address stack contains eight 14-bit registers providing storage for eight lower and six higher order address bits in each register. One register is used as the program counter (storing the effective address) and the other seven permit address storage for nesting of subroutines up to seven levels. The stack automatically stores the content of the program counter upon the execution of a CALL instruction and automatically restores the program counter upon the execution of a RETURN. The CALLs may be nested and the registers of the stack are used as last in/first out pushdown stack. A three-bit address pointer is used to designate the present location of the program counter. When the capacity of the stack is exceeded the address pointer recycles and the content of the lowest level register is destroyed. The program counter is incremented immediately after the lower order address bits are sent out. The higher order address bits are sent out at T2 and then incremented if a carry resulted from T1. The 14-bit program counter provides direct addressing of 16K bytes of memory. Through the use of an I/O instruction for bank switching, memory may be indefinitely expanded.

2. Scratch Pad Memory or Index Registers

The scratch pad contains the accumulator (A register) and six additional 8-bit registers (B, C, D, E, H, L). All arithmetic operations use the accumulator as one of the operands. All registers are independent and may be used for temporary storage. In the case of instructions which require operations with a register in external memory, scratch pad registers H & L provide indirect addressing capability; register L contains the eight lower order bits of address and register H contains the six higher order bits of address (in this case bit 6 and bit 7 are "don't cares").

C. Arithmetic/Logic Unit (ALU)

All arithmetic and logical operations (ADD, ADD with carry, SUBTRACT, SUBTRACT with borrow, AND, EXCLUSIVE OR, OR, COMPARE, INCREMENT, DECREMENT) are carried out in the 8-bit parallel arithmetic unit which includes carry-look-ahead logic. Two temporary registers, register "a" and register "b", are used to store the accumulator and operand for ALU operations. In addition, they are used for temporary address and data storage during intra-processor transfers. Four control bits, carry flip-flop (c), zero flip-flop (z), sign flip-flop (s), and parity flip-flop (p), are set as the result of each arithmetic and logical operation. These bits provide conditional branching capability through CALL, JUMP, or RETURN on condition instructions. In addition, the carry bit provides the ability to do multiple precision binary arithmetic.

D. I/O Buffer

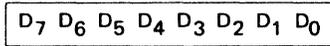
This buffer is the only link between the processor and the rest of the system. Each of the eight buffers is bi-directional and is under control of the instruction register and state timing. Each of the buffers is low power TTL compatible on the output and TTL compatible on the input.

IV. BASIC INSTRUCTION SET

The following section presents the basic instruction set of the 8008.

A. Data and Instruction Formats

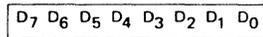
Data in the 8008 is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.



DATA WORD

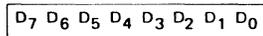
The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

One Byte Instructions

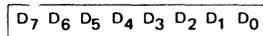


OP CODE

Two Byte Instructions

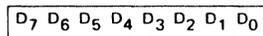


OP CODE

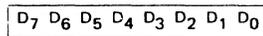


OPERAND

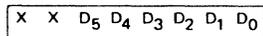
Three Byte Instructions



OP CODE



LOW ADDRESS



HIGH ADDRESS*

TYPICAL INSTRUCTIONS

Register to register, memory reference, I/O arithmetic or logical, rotate or return instructions

Immediate mode instructions

JUMP or CALL instructions

*For the third byte of this instruction, D₆ and D₇ are "don't care" bits.

For the MCS-8 a logic "1" is defined as a high level and a logic "0" is defined as a low level.

B. Summary of Processor Instructions

Index Register Instructions

The load instructions do not affect the flag flip-flops. The increment and decrement instructions affect all flip-flops except the carry.

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	DESCRIPTION OF OPERATION
(1) Lr1r2	(5)	1 1 D D D S S S	Load index register r ₁ with the content of index register r ₂ .
(2) LrM	(8)	1 1 D D D 1 1 1	Load index register r with the content of memory register M.
LMr	(7)	1 1 1 1 1 S S S	Load memory register M with the content of index register r.
(3) LrI	(8)	0 0 D D D 1 1 0 B B B B B B B B	Load index register r with data B . . . B.
LMI	(9)	0 0 1 1 1 1 1 0 B B B B B B B B	Load memory register M with data B . . . B.
INr	(5)	0 0 D D D 0 0 0	Increment the content of index register r (r ≠ A).
DCr	(5)	0 0 D D D 0 0 1	Decrement the content of index register r (r ≠ A).

Accumulator Group Instructions

The result of the ALU instructions affect all of the flag flip-flops. The rotate instructions affect only the carry flip-flop.

ADr	(5)	1 0 0 0 0 S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator. An overflow (carry) sets the carry flip-flop.
ADM	(8)	1 0 0 0 0 1 1 1	
ADI	(8)	0 0 0 0 0 1 0 0 B B B B B B B B	Add the content of index register r, memory register M, or data B . . . B to the accumulator with carry. An overflow (carry) sets the carry flip-flop.
ACr	(5)	1 0 0 0 1 S S S	
ACM	(8)	1 0 0 0 1 1 1 1	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator. An underflow (borrow) sets the carry flip-flop.
ACI	(8)	0 0 0 0 1 1 0 0 B B B B B B B B	
SUr	(5)	1 0 0 1 0 S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator with borrow. An underflow (borrow) sets the carry flip-flop.
SUM	(8)	1 0 0 1 0 1 1 1	
SUI	(8)	0 0 0 1 0 1 0 0 B B B B B B B B	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator with borrow. An underflow (borrow) sets the carry flip-flop.
SBr	(5)	1 0 0 1 1 S S S	
SBM	(8)	1 0 0 1 1 1 1 1	
SBI	(8)	0 0 0 1 1 1 0 0 B B B B B B B B	

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE						DESCRIPTION OF OPERATION		
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂		D ₁	D ₀
NDr	(5)	1	0	1	0	0	S	S	S	Compute the logical AND of the content of index register r, memory register M, or data B . . . B with the accumulator.
NDM	(8)	1	0	1	0	0	1	1	1	
NDI	(8)	0	0	1	0	0	1	0	0	
		B	B	B	B	B	B	B	B	
XRR	(5)	1	0	1	0	1	S	S	S	Compute the EXCLUSIVE OR of the content of index register r, memory register M, or data B . . . B with the accumulator.
XRM	(8)	1	0	1	0	1	1	1	1	
XRI	(8)	0	0	1	0	1	1	0	0	
		B	B	B	B	B	B	B	B	
ORr	(5)	1	0	1	1	0	S	S	S	Compute the INCLUSIVE OR of the content of index register r, memory register m, or data B . . . B with the accumulator.
ORM	(8)	1	0	1	1	0	1	1	1	
ORI	(8)	0	0	1	1	0	1	0	0	
		B	B	B	B	B	B	B	B	
CPr	(5)	1	0	1	1	1	S	S	S	Compare the content of index register r, memory register M, or data B . . . B with the accumulator. The content of the accumulator is unchanged.
CPM	(8)	1	0	1	1	1	1	1	1	
CPI	(8)	0	0	1	1	1	1	0	0	
		B	B	B	B	B	B	B	B	
RLC	(5)	0	0	0	0	0	0	1	0	Rotate the content of the accumulator left.
RRC	(5)	0	0	0	0	1	0	1	0	Rotate the content of the accumulator right.
RAL	(5)	0	0	0	1	0	0	1	0	Rotate the content of the accumulator left through the carry.
RAR	(5)	0	0	0	1	1	0	1	0	Rotate the content of the accumulator right through the carry.

Program Counter and Stack Control Instructions

(4) JMP	(11)	0	1	X	X	X	1	0	0	Unconditionally jump to memory address B ₃ . . . B ₃ B ₂ . . . B ₂ .
		B ₂								
		X	X	B ₃						
(5) JFc	(9 or 11)	0	1	0	C ₄	C ₃	0	0	0	Jump to memory address B ₃ . . . B ₃ B ₂ . . . B ₂ if the condition flip-flop c is false. Otherwise, execute the next instruction in sequence.
		B ₂								
		X	X	B ₃						
JTc	(9 or 11)	0	1	1	C ₄	C ₃	0	0	0	Jump to memory address B ₃ . . . B ₃ B ₂ . . . B ₂ if the condition flip-flop c is true. Otherwise, execute the next instruction in sequence.
		B ₂								
		X	X	B ₃						
CAL	(11)	0	1	X	X	X	1	1	0	Unconditionally call the subroutine at memory address B ₃ . . . B ₃ B ₂ . . . B ₂ . Save the current address (up one level in the stack).
		B ₂								
		X	X	B ₃						
CFc	(9 or 11)	0	1	0	C ₄	C ₃	0	1	0	Call the subroutine at memory address B ₃ . . . B ₃ B ₂ . . . B ₂ if the condition flip-flop c is false, and save the current address (up one level in the stack.) Otherwise, execute the next instruction in sequence.
		B ₂								
		X	X	B ₃						
CTc	(9 or 11)	0	1	1	C ₄	C ₃	0	1	0	Call the subroutine at memory address B ₃ . . . B ₃ B ₂ . . . B ₂ if the condition flip-flop c is true, and save the current address (up one level in the stack). Otherwise, execute the next instruction in sequence.
		B ₂								
		X	X	B ₃						
RET	(5)	0	0	X	X	X	1	1	1	Unconditionally return (down one level in the stack).
RFc	(3 or 5)	0	0	0	C ₄	C ₃	0	1	1	Return (down one level in the stack) if the condition flip-flop c is false. Otherwise, execute the next instruction in sequence.
RTc	(3 or 5)	0	0	1	C ₄	C ₃	0	1	1	Return (down one level in the stack) if the condition flip-flop c is true. Otherwise, execute the next instruction in sequence.
RST	(5)	0	0	A	A	A	1	0	1	Call the subroutine at memory address AAA000 (up one level in the stack).

Input/Output Instructions

INP	(8)	0	1	0	0	M	M	M	1	Read the content of the selected input port (MMM) into the accumulator.
OUT	(6)	0	1	R	R	M	M	M	1	Write the content of the accumulator into the selected output port (RRMMM, RR ≠ 00).

Machine Instruction

HLT	(4)	0	0	0	0	0	0	0	X	Enter the STOPPED state and remain there until interrupted.
HLT	(4)	1	1	1	1	1	1	1	1	Enter the STOPPED state and remain there until interrupted.

NOTES:

- (1) SSS = Source Index Register } These registers, r_i, are designated A(accumulator-000),
DDD = Destination Index Register } B(001), C(010), D(011), E(100), H(101), L(110).
- (2) Memory registers are addressed by the contents of registers H & L.
- (3) Additional bytes of instruction are designated by BBBB BBBB.
- (4) X = "Don't Care".
- (5) Flag flip-flops are defined by C₄C₃: carry (00-overflow or underflow), zero (01-result is zero), sign (10-MSB of result is "1"), parity (11-parity is even).

C. Complete Functional Definition

The following pages present a detailed description of the complete 8008 Instruction Set.

Symbols	Meaning		
< B2 >	Second byte of the instruction		
< B3 >	Third byte of the instruction		
r	One of the scratch pad register references: A, B, C, D, E, H, L		
c	One of the following flag flip-flop references: C, Z, S, P		
C ₄ C ₃	Flag flip-flop codes		
	00	carry	Condition for True
	01	zero	Overflow, underflow
	10	sign	Result is zero
	11	parity	MSB of result is "1"
			Parity of result is even
M	Memory location indicated by the contents of registers H and L		
()	Contents of location or register		
∧	Logical product		
⊕	Exclusive "or"		
∨	Inclusive "or"		
A _m	Bit m of the A-register		
STACK	Instruction counter (P) pushdown register		
P	Program Counter		
←	Is transferred to		
XXX	A "don't care"		
SSS	Source register for data		
DDD	Destination register for data		
	Register # Register Name		
	(SSS or DDD)		
	000 A		
	001 B		
	010 C		
	011 D		
	100 E		
	101 H		
	110 L		

INDEX REGISTER INSTRUCTIONS

LOAD DATA TO INDEX REGISTERS – One Byte

Data may be loaded into or moved between any of the index registers, or memory registers.

Lr₁r₂ (one cycle – PCI)	11	DDD	SSS	(r ₁)←(r ₂) Load register r ₁ with the content of r ₂ . The content of r ₂ remains unchanged. If SSS=DDD, the instruction is a NOP (no operation).
LrM (two cycles – PCI/PCR)	11	DDD	111	(r)←(M) Load register r with the content of the memory location addressed by the contents of registers H and L. (DDD≠111 – HALT instr.)
LMr (two cycles – PCI/PCW)	11	111	SSS	(M)←(r) Load the memory location addressed by the contents of registers H and L with the content of register r. (SSS≠111 – HALT instr.)

LOAD DATA IMMEDIATE – Two Bytes

A byte of data immediately following the instruction may be loaded into the processor or into the memory

LrI (two cycles – PCI/PCR)	00	DDD	110	(r) ← <B ₂ > Load byte two of the instruction into register r.
		<B ₂ >		
LMI (three cycles – PCI/PCR/PCW)	00	111	110	(M) ← <B ₂ > Load byte two of the instruction into the memory location addressed by the contents of registers H and L.
		<B ₂ >		

INCREMENT INDEX REGISTER – One Byte

INr (one cycle – PCI)	00	DDD	000	(r) ← (r)+1. The content of register r is incremented by one. All of the condition flip-flops except carry are affected by the result. Note that DDD≠000 (HALT instr.) and DDD≠111 (content of memory may not be incremented).
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DECREMENT INDEX REGISTER – One Byte

DCr (one cycle – PCI)	00	DDD	001	(r)←(r)–1. The content of register r is decremented by one. All of the condition flip-flops except carry are affected by the result. Note that DDD≠000 (HALT instr.) and DDD≠111 (content of memory may not be decremented).
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ACCUMULATOR GROUP INSTRUCTIONS

Operations are performed and the status flip-flops, C, Z, S, P, are set based on the result of the operation. Logical operations (NDr, XRr, ORr) set the carry flip-flop to zero. Rotate operations affect only the carry flip-flop. Two's complement subtraction is used.

ALU INDEX REGISTER INSTRUCTIONS – One Byte

(one cycle – PCI)

Index Register operations are carried out between the accumulator and the content of one of the index registers (SSS=000 thru SSS=110). The previous content of register SSS is unchanged by the operation.

ADr	10	000	SSS	(A)←(A)+(r) Add the content of register r to the content of register A and place the result into register A.
ACr	10	001	SSS	(A)←(A)+(r)+(carry) Add the content of register r and the contents of the carry flip-flop to the content of the A register and place the result into Register A.
SUr	10	010	SSS	(A)←(A)–(r) Subtract the content of register r from the content of register A and place the result into register A. Two's complement subtraction is used.

ACCUMULATOR GROUP INSTRUCTIONS - Cont'd.

SBr	10	011	SSS	$(A) \leftarrow (A) - (r) - (\text{borrow})$ Subtract the content of register r and the content of the carry flip-flop from the content of register A and place the result into register A.
NDr	10	100	SSS	$(A) \leftarrow (A) \wedge (r)$ Place the logical product of the register A and register r into register A.
XRr	10	101	SSS	$(A) \leftarrow (A) \vee (r)$ Place the "exclusive - or" of the content of register A and register r into register A.
ORr	10	110	SSS	$(A) \leftarrow (A) \vee (r)$ Place the "inclusive - or" of the content of register A and register r into register A.
CPr	10	111	SSS	$(A) - (r)$ Compare the content of register A with the content of register r. The content of register A remains unchanged. The flag flip-flops are set by the result of the subtraction. Equality ($A=r$) is indicated by the zero flip-flop set to "1". Less than ($A < r$) is indicated by the carry flip-flop, set to "1".

ALU OPERATIONS WITH MEMORY – One Byte (two cycles – PCI/PCR)

Arithmetic and logical operations are carried out between the accumulator and the byte of data addressed by the contents of registers H and L.

ADM	10	000	111	$(A) \leftarrow (A) + (M)$ ADD
ACM	10	001	111	$(A) \leftarrow (A) + (M) + (\text{carry})$ ADD with carry
SUM	10	010	111	$(A) \leftarrow (A) - (M)$ SUBTRACT
SBM	10	011	111	$(A) \leftarrow (A) - (M) - (\text{borrow})$ SUBTRACT with borrow
NDM	10	100	111	$(A) \leftarrow (A) \wedge (M)$ Logical AND
XRM	10	101	111	$(A) \leftarrow (A) \vee (M)$ Exclusive OR
ORM	10	110	111	$(A) \leftarrow (A) \vee (M)$ Inclusive OR
CPM	10	111	111	$(A) - (M)$ COMPARE

ALU IMMEDIATE INSTRUCTIONS – Two Bytes (two cycles – PCI/PCR)

Arithmetic and logical operations are carried out between the accumulator and the byte of data immediately following the instruction.

ADI	00	000	100	$(A) \leftarrow (A) + \langle B_2 \rangle$ ADD
ACI	00	001	100	$(A) \leftarrow (A) + \langle B_2 \rangle + (\text{carry})$ ADD with carry
SUI	00	010	100	$(A) \leftarrow (A) - \langle B_2 \rangle$ SUBTRACT
SBI	00	011	100	$(A) \leftarrow (A) - \langle B_2 \rangle - (\text{borrow})$ SUBTRACT with borrow
NDI	00	100	100	$(A) \leftarrow (A) \wedge \langle B_2 \rangle$ Logical AND
XRI	00	101	100	$(A) \leftarrow (A) \vee \langle B_2 \rangle$ Exclusive OR
ORI	00	110	100	$(A) \leftarrow (A) \vee \langle B_2 \rangle$ Inclusive OR
CPI	00	111	100	$(A) - \langle B_2 \rangle$ COMPARE

ROTATE INSTRUCTIONS – One Byte

(one cycle – PCI)

The accumulator content (register A) may be rotated either right or left, around the carry bit or through the carry bit. Only the carry flip-flop is affected by these instructions; the other flags are unchanged.

RLC	00 000 010	$A_{m+1} \leftarrow A_m, A_0 \leftarrow A_7, (\text{carry}) \leftarrow A_7$ Rotate the content of register A left one bit. Rotate A_7 into A_0 and into the carry flip-flop.
RRC	00 001 010	$A_m \leftarrow A_{m+1}, A_7 \leftarrow A_0, (\text{carry}) \leftarrow A_0$ Rotate the content of register A right one bit. Rotate A_0 into A_7 and into the carry flip-flop.
RAL	00 010 010	$A_{m+1} \leftarrow A_m, A_0 \leftarrow (\text{carry}), (\text{carry}) \leftarrow A_7$ Rotate the content of Register A left one bit. Rotate the content of the carry flip-flop into A_0 . Rotate A_7 into the carry flip-flop.
RAR	00 011 010	$A_m \leftarrow A_{m+1}, A_7 \leftarrow (\text{carry}), (\text{carry}) \leftarrow A_0$ Rotate the content of register A right one bit. Rotate the content of the carry flip-flop into A_7 . Rotate A_0 into the carry flip-flop.

PROGRAM COUNTER AND STACK CONTROL INSTRUCTIONS

JUMP INSTRUCTIONS – Three Bytes

(three cycles – PCI/PCR/PCR)

Normal flow of the microprogram may be altered by jumping to an address specified by bytes two and three of an instruction.

JMP (Jump Unconditionally)	01 XXX 100 <B ₂ > <B ₃ >	$(P) \leftarrow \langle B_3 \rangle \langle B_2 \rangle$ Jump unconditionally to the instruction located in memory location addressed by byte two and byte three.
JFc (Jump if Condition False)	01 0C ₄ C ₃ 000 <B ₂ > <B ₃ >	If $(c) = 0$, $(P) \leftarrow \langle B_3 \rangle \langle B_2 \rangle$. Otherwise, $(P) = (P)+3$. If the content of flip-flop c is zero, then jump to the instruction located in memory location $\langle B_3 \rangle \langle B_2 \rangle$; otherwise, execute the next instruction in sequence.
JTc (Jump if Condition True)	01 1C ₄ C ₃ 000 <B ₂ > <B ₃ >	If $(c) = 1$, $(P) \leftarrow \langle B_3 \rangle \langle B_2 \rangle$. Otherwise, $(P) = (P)+3$. If the content of flip-flop c is one, then jump to the instruction located in memory location $\langle B_3 \rangle \langle B_2 \rangle$; otherwise, execute the next instruction in sequence.

CALL INSTRUCTIONS – Three Bytes

(three cycles – PCI/PCR/PCR)

Subroutines may be called and nested up to seven levels.

CAL (Call subroutine Unconditionally)	01 XXX 110 <B ₂ > <B ₃ >	$(\text{Stack}) \leftarrow (P), (P) \leftarrow \langle B_3 \rangle \langle B_2 \rangle$. Shift the content of P to the pushdown stack. Jump unconditionally to the instruction located in memory location addressed by byte two and byte three.
CFc (Call subroutine if Condition False)	01 0C ₄ C ₃ 010 <B ₂ > <B ₃ >	If $(c) = 0$, $(\text{Stack}) \leftarrow (P), (P) \leftarrow \langle B_3 \rangle \langle B_2 \rangle$. Otherwise, $(P) = (P)+3$. If the content of flip-flop c is zero, then shift contents of P to the pushdown stack and jump to the instruction located in memory location $\langle B_3 \rangle \langle B_2 \rangle$; otherwise, execute the next instruction in sequence.
CTc (Call subroutine if Condition True)	01 1C ₄ C ₃ 010 <B ₂ > <B ₃ >	If $(c) = 1$, $(\text{Stack}) \leftarrow (P), (P) \leftarrow \langle B_3 \rangle \langle B_2 \rangle$. Otherwise, $(P) = (P)+3$. If the content of flip-flop c is one, then shift contents of P to the pushdown stack and jump to the instruction located in memory location $\langle B_3 \rangle \langle B_2 \rangle$; otherwise, execute the next instruction in sequence.

In the above JUMP and CALL instructions $\langle B_2 \rangle$ contains the least significant half of the address and $\langle B_3 \rangle$ contains the most significant half of the address. Note that D_6 and D_7 of $\langle B_3 \rangle$ are "don't care" bits since the CPU uses fourteen bits of address.

RETURN INSTRUCTIONS – One Byte

(one cycle – PCI)

A return instruction may be used to exit from a subroutine; the stack is popped-up one level at a time.

RET	00	XXX	111	(P) \leftarrow (Stack). Return to the instruction in the memory location addressed by the last value shifted into the pushdown stack. The stack pops up one level.
RFc (Return Condition False)	00	0C ₄ C ₃	011	If (c) = 0, (P) \leftarrow (Stack); otherwise, (P) = (P)+1. If the content of flip-flop c is zero, then return to the instruction in the memory location addressed by the last value inserted in the pushdown stack. The stack pops up one level. Otherwise, execute the next instruction in sequence.
RTc (Return Condition True)	00	1C ₄ C ₃	011	If (c) = 1, (P) \leftarrow (Stack); otherwise, (P) = (P)+1. If the content of flip-flop c is one, then return to the instruction in the memory location addressed by the last value inserted in the pushdown stack. The stack pops up one level. Otherwise, execute the next instruction in sequence.

RESTART INSTRUCTION – One Byte

(one cycle – PCI)

The restart instruction acts as a one byte call on eight specified locations of page 0, the first 256 instruction words.

RST	00	AAA	101	(Stack) \leftarrow (P), (P) \leftarrow (000000 00AAA000) Shift the contents of P to the pushdown stack. The content, AAA, of the instruction register is shifted into bits 3 through 5 of the P-counter. All other bits of the P-counter are set to zero. As a one-word "call", eight eight-byte subroutines may be accessed in the lower 64 words of memory.
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INPUT/OUTPUT INSTRUCTIONS

One Byte

(two cycles – PCI/PCC)

Eight input devices may be referenced by the input instruction

INP	01	00M	MM1	(A) \leftarrow (input data lines). The content of register A is made available to external equipment at state T1 of the PCC cycle. The content of the instruction register is made available to external equipment at state T2 of the PCC cycle. New data for the accumulator is loaded at T3 of the PCC cycle. MMM denotes input device number. The content of the condition flip-flops, S,Z,P,C, is output on D ₀ , D ₁ , D ₂ , D ₃ respectively at T4 on the PCC cycle.
------------	----	-----	-----	--

Twenty-four output devices may be referenced by the output instruction.

OUT	01	RRM	MM1	(Output data lines) \leftarrow (A). The content of register A is made available to external equipment at state T1 and the content of the instruction register is made available to external equipment at state T2 of the PCC cycle. RRMMM denotes output device number (RR \neq 00).
------------	----	-----	-----	--

MACHINE INSTRUCTION

HALT INSTRUCTION – One Byte

(one cycle – PCI)

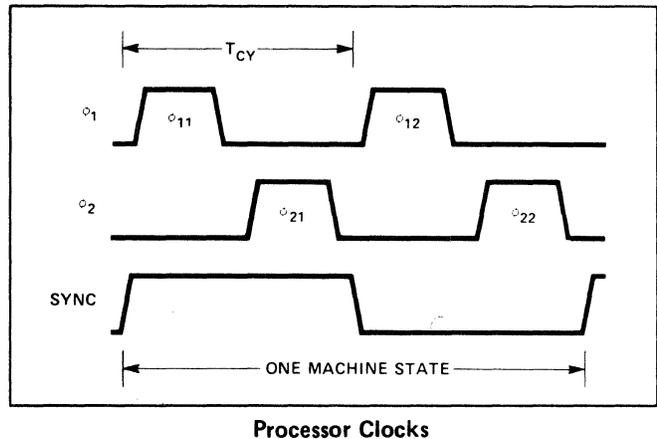
HLT	00	000	00X	On receipt of the Halt Instruction, the activity of the processor is immediately suspended in the STOPPED state. The content of all registers and memory is unchanged. The P-counter has been updated and the internal dynamic memories continue to be refreshed.
	11	111	111	

D. Internal Processor Operation

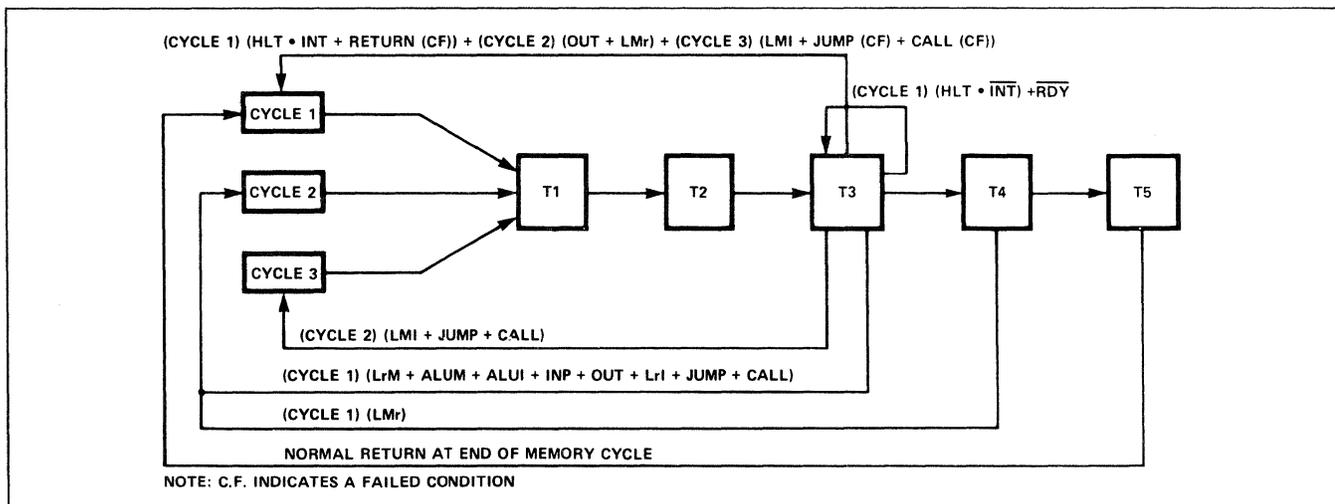
Internally the processor operates through five different states:

Internal State	Typical Function
T1	NORMAL Send out lower eight bits of address and increment program counter.
T1	INTERRUPT Send out lower eight bits of address and suppress incrementing of program counter and acknowledge interrupt.
T2	WAIT Send out six higher order bits of address and two control bits, D ₆ and D ₇ . Increment program counter if there has been a carry from T1.
T3	NORMAL Wait for READY signal to come true. Refresh internal dynamic memories while waiting.
T3	STOPPED Fetch and decode instruction; fetch data from memory; output data to memory. Refresh internal memories.
T4 and T5	STOPPED Remain stopped until INTERRUPT occurs. Refresh internal memories.
T4 and T5	EXECUTE Execute instruction and appropriately transfer data within processor. Content of data bus transfer is available at I/O bus for convenience in testing. Some cycles do not require these states. In those cases, the states are skipped and the processor goes directly to T1.

The 8008 is driven by two non-overlapping clocks. Two clock periods are required for each state of the processor. ϕ_1 is generally used to precharge all data lines and memories and ϕ_2 controls all data transfers within the processor. A SYNC signal (divide by two of ϕ_2) is sent out by the 8008. This signal distinguishes between the two clock periods of each state.



The figure below shows state transitions relative to the internal operation of the processor. As noted in the previous table, the processor skips unnecessary execution steps during any cycle. The state counter within the 8008 operates as a five bit feedback shift register with the feedback path controlled by the instruction being executed. When the processor is either waiting or stopped, it is internally cycling through the T3 state. This state is the only time in the cycle when the internal dynamic memories can be refreshed.



Transition State Diagram (Internal)

The following pages show the processor activity during each state of the execution of each instruction.

INTERNAL PROCESSOR OPERATION

INDEX REGISTER INSTRUCTIONS

INSTRUCTION CODING				OPERATION	# OF STATES TO EXECUTE INSTRUCTION	MEMORY CYCLE ONE (1)				
D ₇ D ₆	D ₅ D ₄ D ₃	D ₂ D ₁ D ₀				T1 (2)	T2	T3	T4 (3)	T5
1 1	D D D	S S S		Lr ₁ r ₂	(5)	PC _L OUT (4)	PC _H OUT	FETCH INSTR. TO IR & REG. b	SSS TO REG. b (6)	REG. b TO DDD
1 1	D D D	1 1 1		LrM	(8)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	→	
1 1	1 1 1	S S S		LMr	(7)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	SSS TO REG. b	→
0 0	D D D	1 1 0		Lrl	(8)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	→	
0 0	1 1 1	1 1 0		LMI	(9)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	→	
0 0	D D D	0 0 0		INr	(5)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	X	ADD OP - FLAGS AFFECTED
0 0	D D D	0 0 1		DCr	(5)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	X	SUB OP - FLAGS AFFECTED

ACCUMULATOR GROUP INSTRUCTIONS

1 0	P P P	S S S		ALU OP r	(5)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	SSS TO REG. b	ALU OP - FLAGS AFFECTED
1 0	P P P	1 1 1		ALU OP M	(8)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	→	
0 0	P P P	1 0 0		ALU OP I	(8)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	→	
0 0	0 0 0	0 1 0		RLC	(5)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	X	ROTATE REG. A CARRY AFFECTED
0 0	0 0 1	0 1 0		RRC	(5)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	X	ROTATE REG. A CARRY AFFECTED
0 0	0 1 0	0 1 0		RAL	(5)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	X	ROTATE REG. A CARRY AFFECTED
0 0	0 1 1	0 1 0		RAR	(5)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	X	ROTATE REG. A CARRY AFFECTED

PROGRAM COUNTER AND STACK CONTROL INSTRUCTIONS

0 1	X X X	1 0 0		JMP	(11)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	→	
0 1	0 C C	0 0 0		JFc	(9 or 11)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	→	
0 1	1 C C	0 0 0		JTc	(9 or 11)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	→	
0 1	X X X	1 1 0		CAL	(11)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	→	
0 1	0 C C	0 1 0		CFc	(9 or 11)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	→	
0 1	1 C C	0 1 0		CTc	(9 or 11)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	→	
0 0	X X X	1 1 1		RET	(5)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	POP STACK	X
0 0	0 C C	0 1 1		RFc	(3 or 5)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	POP STACK (13)	X
0 0	1 C C	0 1 1		RTc	(3 or 5)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	POP STACK (13)	X
0 0	A A A	1 0 1		RST	(5)	PC _L OUT	PC _H OUT	FETCH INSTR. TO REG. b AND PUSH STACK (0→REG. a)	REG. a TO PC _H	REG. b to PC _L (14)

I/O INSTRUCTIONS

0 1	0 0 M	M M 1		INP	(8)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	→	
0 1	R R M	M M 1		OUT	(6)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b	→	

MACHINE INSTRUCTIONS

0 0	0 0 0	0 0 X		HLT	(4)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b & HALT (18)		
1 1	1 1 1	1 1 1		HLT	(4)	PC _L OUT	PC _H OUT	FETCH INSTR. TO IR & REG. b & HALT (18)		

NOTES:

- The first memory cycle is always a PC_L (instruction) cycle.
- Internally, states are defined as T1 through T5. In some cases more than one memory cycle is required to execute an instruction.
- Content of the internal data bus at T4 and T5 is available at the data bus. This is designed for testing purposes only.
- Lower order address bits in the program counter are denoted by PC_L and higher order bits are designated by PC_H.
- During an instruction fetch the instruction comes from memory to the instruction register and is decoded.
- Temporary registers are used internally for arithmetic operations and data transfers (Register a and Register b.)
- These states are skipped.
- PCR cycle (Memory Read Cycle).
- "X" denotes an idle state.
- PCW cycle (Memory Write Cycle).
- When the JUMP is conditional and the condition fails, states T4 and T5 are skipped and the state counter advances to the next memory cycle.

MEMORY CYCLE TWO					MEMORY CYCLE THREE				
T1	T2	T3	T4	T5	T1	T2	T3	T4	T5
REG. L OUT (8)	REG. H OUT	DATA TO REG. b	X (9)	REG. b TO DDD					
REG. L OUT (10)	REG. H OUT	REG. b TO OUT							
PC _L OUT (8)	PC _H OUT	DATA TO REG. b	X	REG. b TO DDD					
PC _L OUT (8)	PC _H OUT	DATA TO REG. b	→		REG. L OUT(10)	REG. H OUT	REG. b TO OUT		

REG. L OUT (8)	REG. H OUT	DATA TO REG. b	X	ALU OP - FLAGS AFFECTED					
PC _L OUT (8)	PC _H OUT	DATA TO REG. b	X	ARITH OP - FLAGS AFFECTED					

PC _L OUT (8)	PC _H OUT	LOWER ADD. TO REG. b	→		PC _L OUT(8)	PC _H OUT	HIGHER ADD. REG. a	REG. a TO PC _H	REG. b TO PC _L
PC _L OUT (8)	PC _H OUT	LOWER ADD. TO REG. b	→		PC _L OUT(8)	PC _H OUT	HIGHER ADD. REG. a (11)	REG. a TO PC _H	REG. b TO PC _L
PC _L OUT (8)	PC _H OUT	LOWER ADD. TO REG. b	→		PC _L OUT(8)	PC _H OUT	HIGHER ADD. REG. a (11)	REG. a TO PC _H	REG. b TO PC _L
PC _L OUT (8)	PC _H OUT	LOWER ADD. TO REG. b	→		PC _L OUT(8)	PC _H OUT	HIGHER ADD. REG. a	REG. a TO PC _H	REG. b TO PC _L
PC _L OUT (8)	PC _H OUT	LOWER ADD. TO REG. b	→		PC _L OUT(8)	PC _H OUT	HIGHER ADD. REG. a (12)	REG. a TO PC _H	REG. b TO PC _L
PC _L OUT (8)	PC _H OUT	LOWER ADD. TO REG. b	→		PC _L OUT(8)	PC _H OUT	HIGHER ADD. REG. a (12)	REG. a TO PC _H	REG. b TO PC _L

REG. A TO OUT (15)	REG. b TO OUT	DATA TO REG. b	COND ff OUT (16)	REG. b TO REG. A					
REG. A (15) TO OUT	REG. b TO OUT	X (17)							

12. When the CALL is conditional and the condition fails, states T4 and T5 are skipped and the state counter advances to the next memory cycle. If the condition is true, the stack is pushed at T4, and the lower and higher order address bytes are loaded into the program counter.
13. When the RETURN condition is true, pop up the stack; otherwise, advance to next memory cycle skipping T4 and T5.
14. Bits D₃ through D₅ are loaded into PC_L and all other bits are set to zero; zeros are loaded into PC_H.

15. PCC cycle (I/O Cycle).
16. The content of the condition flip-flops is available at the data bus: S at D₀, Z at D₁, P at D₂, C at D₃.
17. A READY command must be supplied for the OUT operation to be completed. An idle T3 state is used and then the state counter advances to the next memory cycle.
18. When a HALT command occurs, the CPU internally remains in the T3 state until an INTERRUPT is recognized. Externally, the STOPPED state is indicated.

V. PROCESSOR CONTROL SIGNALS

A. Interrupt Signal (INT)

1) INTERRUPT REQUEST

If the interrupt line is enabled (Logic "1"), the CPU recognizes an interrupt request at the next instruction fetch (PCI) cycle by outputting $S_0 S_1 S_2 = 011$ at T11 time. The lower and higher order address bytes of the program counter are sent out, but the program counter is not advanced. A successive instruction fetch cycle can be used to insert an arbitrary instruction into the instruction register in the CPU. (If a multi-cycle or multi-byte instruction is inserted, an interrupt need only be inserted for the first cycle.)

When the processor is interrupted, the system INTERRUPT signal must be synchronized with the leading edge of the ϕ_1 or ϕ_2 clock. To assure proper operation of the system, the interrupt line to the CPU must not be allowed to change within 200ns of the falling edge of ϕ_1 . An example of a synchronizing circuit is shown on the schematic for the SIM8-01 (Section VII).

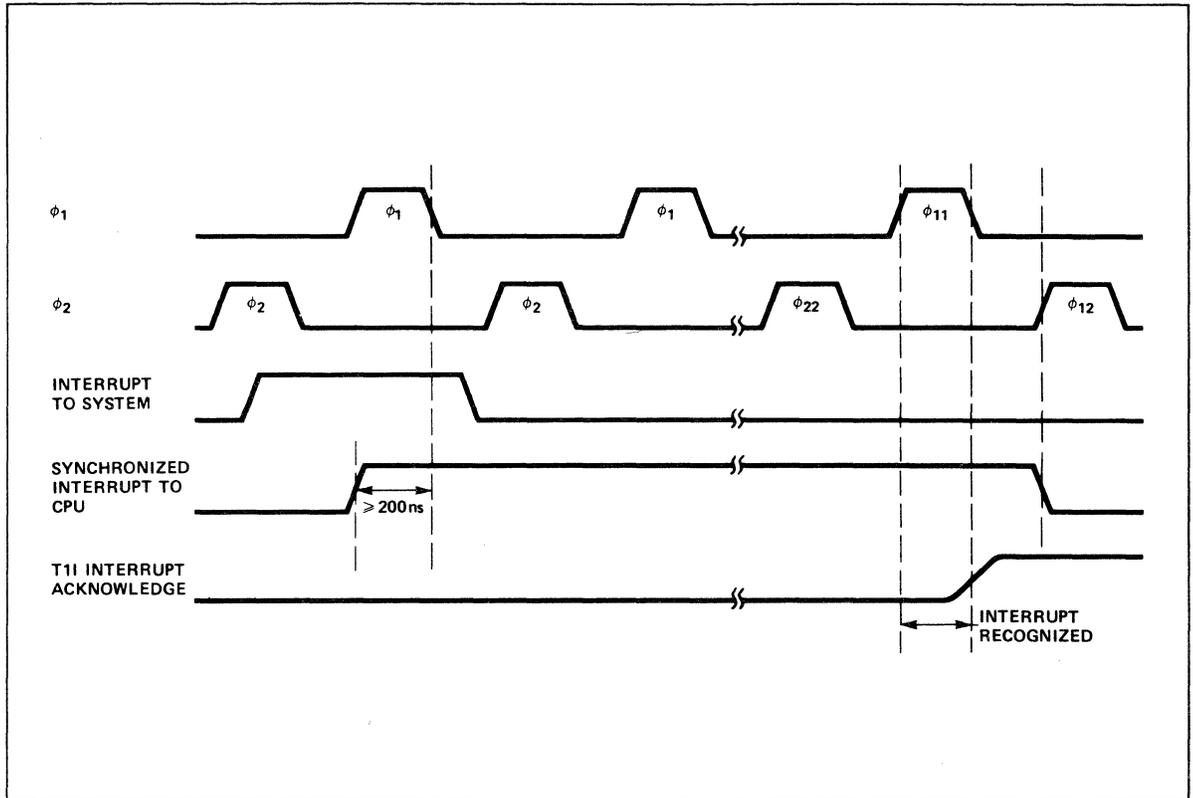


Figure 4. Recognition of Interrupt

If a HALT is inserted, the CPU enters a STOPPED state; if a NOP is inserted, the CPU continues; if a "JUMP to 0" is inserted, the processor executes program from location 0, etc. The RESTART instruction is particularly useful for handling interrupt routines since it is a one byte call.

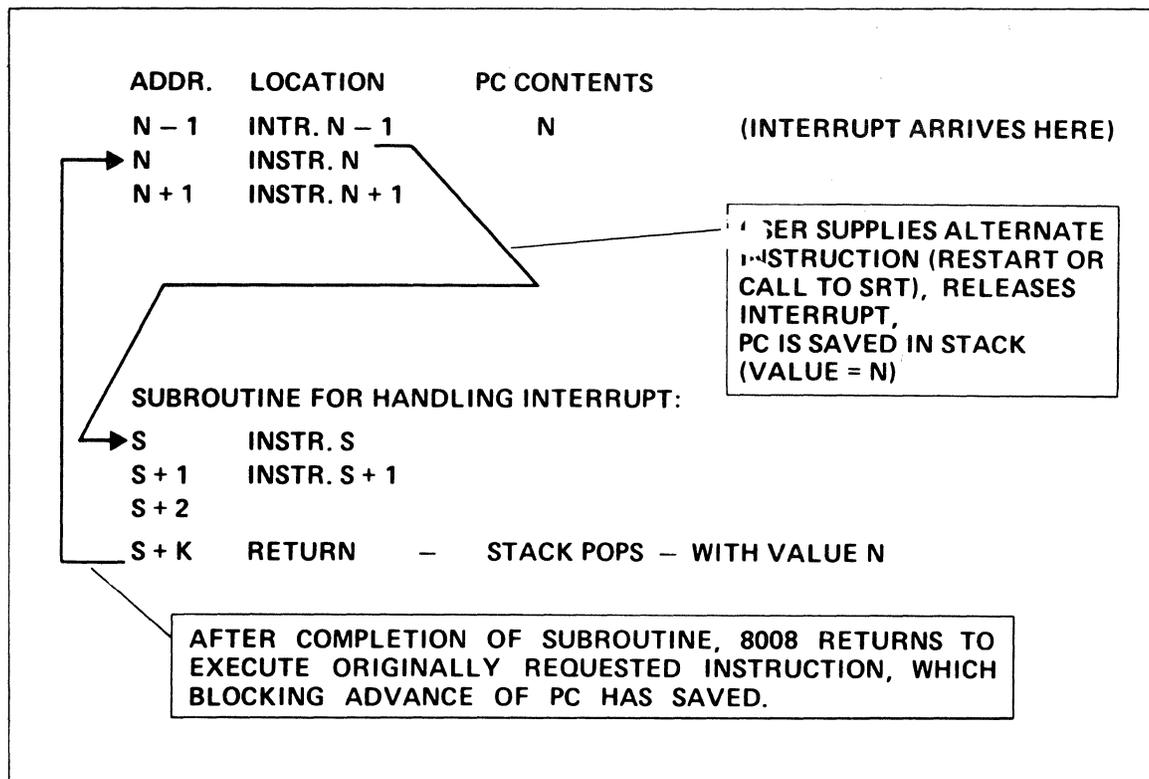


Figure 5. 8008 Interrupt

2) START-UP OF THE 8008

When power (V_{DD}) and clocks (ϕ_1, ϕ_2) are first turned on, a flip-flop internal to the 8008 is set by sensing the rise of V_{DD} . This internal signal forces a HALT (00000000) into the instruction register and the 8008 is then in the STOPPED state. The following sixteen clock periods after entering the STOPPED state are required to clear (logic "0") memories (accumulator, scratch pad, program counter, and stack). During this time the interrupt line has been at logic "0". Any time after the memories are cleared, the 8008 is ready for normal operation.

To reset the flip-flop and also escape from the stopped state, the interrupt line must go to a logic "1"; it should be returned to logic "0" by decoding the state T11 at some time later than ϕ_{11} . Note that whenever the 8008 is in a T11 state, the program counter is not incremented. As a result, the same address is sent out on two successive cycles.

Three possible sequences for starting the 8008 are shown on the following page. The RESTART instruction is effectively a one cycle call instruction, and it is convenient to use this instruction to call an initiation subroutine. Note that it is not necessary to start the 8008 with a RESTART instruction.

The selection of initiation technique to use depends on the sophistication of the system using the 8008. If the interrupt feature is used only for the start-up of the 8008 use the ROM directly, no additional external logic associated with instructions from source other than the ROM program need be considered. If the interrupt feature is used to jam instructions into the 8008, it would then be consistent to use it to jam the initial instruction.

The timing for the interrupt with the start-up timing is shown on an accompanying sheet. The jamming of an instruction and the suppression of the program counter update are handled the same for all interrupts.

EXAMPLE 1:

Shown below are two start-up alternatives where an instruction is not forced into the 8008 during the interrupt cycle. The normal program flow starts the 8008.

a.	8008 ADDRESS OUT	INSTRUCTION IN ROM	
	0 0 0 0 0 0 0 0 0 0 0 0 0 0	NOP (LAA 11 000 000)	} Entry Directly To Main Program
	0 0 0 0 0 0 0 0 0 0 0 0 0 0	NOP	
	0 0 0 0 0 0 0 0 0 0 0 0 0 1	INSTR ₁	
	0 0 0 0 0 0 0 0 0 0 0 0 1 0	INSTR ₂	
b.	8008 ADDRESS OUT	INSTRUCTION IN ROM	
	0 0 0 0 0 0 0 0 0 0 0 0 0 0	RST (RST = 00 XYZ 101)	} A Jump To The Main Program
	0 0 0 0 0 0 0 0 X Y Z 0 0 0	INSTR ₁	
	0 0 0 0 0 0 0 0 X Y Z 0 0 1	INSTR ₂	
	·	·	
	·	·	

EXAMPLE 2:

A RESTART instruction is jammed in and first instruction in ROM initially ignored.

	8008 ADDRESS OUT	INSTRUCTION IN ROM	
	0 0 0 0 0 0 0 0 0 0 0 0 0 0	INSTR ₁ (RST = 00 XYZ 101)	} Start-up Routine
	0 0 0 0 0 0 0 0 X Y Z 0 0 0	INSTR _a	
	0 0 0 0 0 0 0 0 X Y Z 0 0 1	INSTR _b	
	·	·	
	·	·	
	0 0 0 0 0 0 0 0 n n n n n n	RETURN	} Main Program
	0 0 0 0 0 0 0 0 0 0 0 0 0 0	INSTR ₁ (INSTR ₁ executed now)	
	0 0 0 0 0 0 0 0 0 0 0 0 0 1	INSTR ₂	
	·	·	
	·	·	

Note that during the interrupt cycle the flow of the instruction to the 8008 either from ROM or another source must be controlled by hardware external to 8008.

START-UP OF THE 8008

B. Ready (RDY)

The 8008 is designed to operate with any type or speed of semiconductor memory. This flexibility is provided by the READY command line. A high-speed memory will always be ready with data (tie READY line to V_{CC}) almost immediately after the second byte of the address has been sent out. As a result the 8008 will never be required to wait for the memory. On the other hand, with slow ROMs, RAMs or shift registers, the data will not be immediately available; the 8008 must wait until the READY command indicates that the valid memory data is available. As a result any type or any combination of memory types may be used. The READY command line synchronizes the 8008 to the memory cycle. **When a program is being developed, the READY signal provides a means of stepping through the program, one cycle at a time.**

**APPENDIX
B**

**BALL
MONITOR
(TVB 12)**

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GENERAL INFORMATION

1.1 MONITOR DESCRIPTION

The TV monitor is a solid-state unit for use in industrial and commercial installations where reliability and high quality video reproduction are desired.

The monitor features printed circuit board construction for reliability and uniformity. All circuits of the TV monitor are transistorized. The synchronization circuits have been custom designed to accept vertical and horizontal drive signals thus enabling the interfacing of this monitor with industrial or simple sync sources. This feature simplifies the user's sync processing and mixing and allows the unit to operate without requiring composite sync. The electronic packaging has been miniaturized for compatibility with small volume requirements.

1.2 ELECTRICAL SPECIFICATIONS

Input Data Specifications

	Video	Vertical Drive Signal	Horizontal Drive Signal
Input Connector	(Necessary Accessory-Available) Printed circuit board card edge connector - Viking #2VK10S/1-2 or Amphenol #225-21031-101		
Pulse Rate or Width	Pulse Width: 100 nsec or greater	Pulse Rate: 47 to 63 pulses/ sec	Pulse Rate: 15,000 to 16,500 pulses/ sec
Amplitude	Low = Zero $+0.4$ -0.0 volts (See Section 1, para. 1.5) High = 4 ± 1.5 volts (See Section 4, para. 4.4)		
Signal Rise & Fall Times (10% to 90% amplitude)	Less than 20 nsec	Less than 100 nsec	Less than 50 nsec
Input Signal Format	See Fig. 1		

Data Display Specifications

Input Impedance

	Minimum Shunt Resistance	Maximum Shunt Capacitance
(a) Video Input:	3.3 k ohms	40 pF
(b) Vertical Drive Input:	3.3 k ohms	40 pF
(c) Horizontal Drive Input:	470 ohms	40 pF

Video Amplifier

(a) Bandwidth:	12 MHz (-3 dB)
(b) Rise and Fall Times (10% to 90% amplitude):	Less than 35 nsec. (linear mode)
(c) Storage Time:	15 nsec, maximum (linear mode)

Retrace and Delay Times

(a) Vertical:	900 μ sec retrace, maximum
(b) Horizontal:	7 μ sec retrace plus 4 μ sec delay, maximum

Display Specifications

Cathode Ray Tube

Nominal Diagonal Measurement (inches)	Phosphor	*Resolution (TV Lines)	
		Center	Corner
5	P4	650 at 80 fL	550 at 80 fL
9	P4	750 at 40 fL	650 at 40 fL
12	P4	900 at 40 fL	800 at 40 fL
12	P39	900 at 20 fL	800 at 20 fL

*Resolution is measured in accordance with EIA RS-375 except Burst Modulation (or Depth of Modulation) is adjusted for 100 percent.

Geometric Distortion

The perimeter of a full field of characters shall approach an ideal rectangle to within $\pm 1.5\%$ of the rectangle height.

Power Requirements

Power Specifications for Monitors Incorporating a Low Voltage Power Supply

	CRT SIZE		
	5 inches	9 inches	12 inches
Input Connector	Receptacle, Molex #03-06-1041 Supplied with Unit Mating Plug, Molex #03-06-2041 - Necessary Accessory (Available)		
Input Voltage	105 V to 130 V rms (120 V nominal); 50/60 Hz Optional: 220 V/240 V rms $\pm 10\%$, 50/60 Hz		
Input Power			24 W (Nominal)
Output Voltages		+15 V DC (short circuit protected) +12 kV DC; 12.6 V rms	

Power Specifications for Data Monitors Using an External DC Power Supply

Note: Any power transformers must be well removed from the CRT and/or be of low external flux field design.

	CRT SIZE		
	5 inches	9 inches	12 inches
Input Voltage	12 ± 0.2 V DC	15 ± 0.2 V DC	
Ripple	Less than 10 millivolts p-p		
Input Current	650 mA DC, nominal		900 mA DC, nominal
	*1.0 A DC, maximum		*1.5 A DC, maximum
Output Voltages	+12 V DC +9 kV DC	+12.6 V DC, +12 kV DC	
*Brightness and Contrast adjusted for worst case conditions.			

1.3 ENVIRONMENTAL SPECIFICATIONS

Temperature (Chassis or Custom Unit)

Operating Range: 5°C to 55°C Ambient

Storage Range: -40°C to 65°C

Humidity

5 to 80 percent (Noncondensing)

Altitude

Operating Range: Up to 10,000 feet

X-Ray Radiation

These units comply with DHEW Rules-42-CFR-Part 78

1.5 CONTROLS

Customer Access - Necessary Accessories (Available)

- (1) Contrast, 500 ohm potentiometer carbon composition
≥1/8 Watt
- (2) Brightness, 100 kilohm potentiometer ≥1/8 Watt
Optional: The Brightness Control can be mounted
on the printed circuit board as an
internal set up control.

Internal Set Up Controls

- (1) Height
- (2) Vertical Linearity
- (3) Vertical Hold
- (4) Focus
- (5) Width
- (6) Low Voltage Adjust

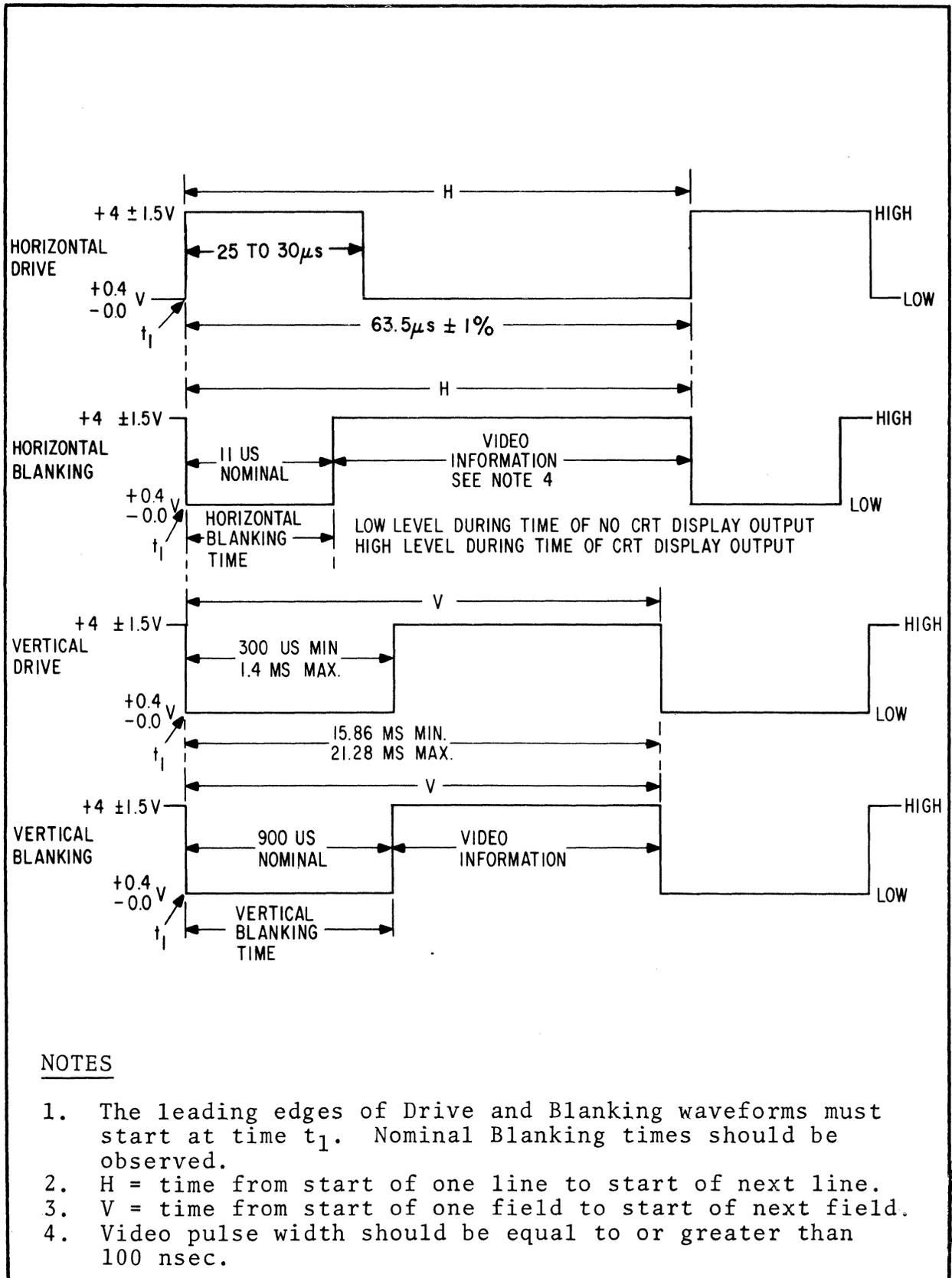


Fig. 1 Synchronization and Blanking Generator Waveforms for the TV Series

Section 2 OPERATING PROCEDURES

2.1 INSTALLATION

Power for the TV monitor series can be supplied in one of two methods, depending upon the model. For the model which has a self-contained, low voltage, power supply, plug the monitor into a 120 volt (220/240 V, optional) AC power source. For the model which requires external DC power, consult the schematic for terminal locations and voltage values.

The video and synchronization signals are fed to their appropriate connections as indicated on the schematic.

Mount the monitor so that the ambient temperature surrounding the monitor does not exceed 55°C.

2.2 GROUNDING TECHNIQUES

The method of interconnecting and grounding the equipment is a function of the signal frequency; any optimum grounding depends largely on the system in which the equipment is used.

The following grounding technique is recommended when installing a TV Data Display Monitor.

The vertical/video, horizontal drive, vertical drive, and CRT arc bypass are all returned to the TV chassis plate ground through single molex connections. Normally, it is assumed that the frame and chassis plate of the monitor will be installed in a system where they will be an integral part of system ground. If this is true,

then further grounding should not be necessary. However, the mating of the monitor's frame with the system or the generator's signal source ground must be electrically good. Good electrical metal-to-metal contact must be assured.

Where strong radiated noise and signal fields inhibit the monitors's operation or where a signal's waveform is deteriorated by long or poorly selected cabling, low or high frequency shielded cable should be used. When using shielded cable, careful attention must be given to proper grounding of the outer conductor. Improper grounding can cause annoying ground loops. In some cases, transistor failures can be traced to poor grounding techniques.

The TV monitor has provisions at the printed circuit board card edge connector to pick up the ground returns for the vertical/video, horizontal drive, and vertical drive circuits. If these connections must be used, it is likely that the single molex connection associated with each ground return may have to be opened to minimize ground loops. Reducing the number of ground connections reduces the number of possible ground loops with the ultimate being one system ground connection at the source.

IMPORTANT -- One pin on the printed circuit board edge connector is to be used specifically for the CRT arc bypass and must not be used as a signal ground return (see schematic).

2.3 VIDEO LEAD ROUTING

The video lead probably will carry high frequency signals and should be given the following considerations:

- A. To minimize distributed capacity and capacitive pickup of nearby radiated fields, route the video leads separately and away from all other wiring.
- B. Make the lead length as short as possible, consistent with the packaging requirements.
- C. Ideally, the video line should meet the requirements of a terminated coaxial system; i.e., the video line should exhibit a constant impedance from source to load. An effective method of testing the video line is as follows:
 - a. Establish a configuration and keep the foregoing requirements in mind.
 - b. Drive the source end of the video line with the output of TTL logic or an equivalent pulse generator capable of providing pulses with rise and fall times of typically 10 nanoseconds and pulse widths of approximately 100 nanoseconds. Any convenient duty cycle and repetition rate may be used. The generator should be capable of supplying +2.5 volt pulse into a shunt impedance of 3.3 k ohms (resistive) and 40 pF (capacitive).
 - c. Observe the pulse at the receiving end of the video line with a low capacitance (less than 5 pF) oscilloscope probe. Adjust the routing and termination of the video line to maintain rise and fall times of 20 nanoseconds or less and overshoots within 10 percent of the pulse amplitude.

2.4 INITIAL TURN-ON PROCEDURE

The TV monitor was tested and aligned before shipment and should not require further adjustment after installation. First, connect the video and synchronization signals to the monitor; next apply power to the unit. Proceed as follows when turning the monitor on for the first time.

- (1) Place the power switch (external or internal) in the ON position. Adjust the brightness and contrast controls for desired effect and stabilize the picture with the vertical hold control. Allow the monitor to warm up for 15 minutes before proceeding to the next step.

- (2) Adjust the height control and width coil for the desired raster height and width. Adjust the focus control to produce optimum focus over the entire area of the CRT.

2.5 NORMAL MONITOR OPERATION

After the monitor has been adjusted, turn on the power and adjust contrast and brightness. Note that some models may have the brightness control as an internal setup control. In that case, make the adjustment as indicated in Section 2.4.

Section 3 THEORY OF OPERATION

3.1 VIDEO AMPLIFIER

The video amplifier consists of Q101 and its associated circuitry.

The incoming video signal is applied to the monitor through the contrast control through R109 to the base of transistor Q101.

Transistor Q101 and its components comprise the video output driver with a gain of about 17. Q104, operating as a class B amplifier, remains cutoff until a DC-coupled, positive-going signal arrives at its base and turns on the transistor. R111 adds series feedback which makes the terminal-to-terminal voltage gain relatively independent of transistor variations as well as stabilizes the device against voltage and current changes caused by ambient temperature variations.

The negative going signal at the collector of Q101 is DC-coupled to the cathode of the CRT. The class B biasing of the video driver allows a larger video output signal to modulate the CRT's cathode and results in a maximum available contrast ratio.

The overall brightness at the screen of the CRT is determined by the negative potential at the grid and is varied by the brightness control.

3.2 VERTICAL DEFLECTION

Transistor Q102 is a programmable unijunction transistor, and together with its external circuitry, forms a relaxation oscillator

operating at the vertical rate. Resistor R115, variable resistor R116 and capacitors C105 and C106 form an RC network providing proper timing.

When power is applied, C105 and C106 charge exponentially through R115 and R116 until the voltage at the junction of R116 and C105 equals the anode "A" firing voltage. At this time, one of the unijunction's diodes that is connected between the anode and anode gate "G" becomes forward biased allowing the capacitors to discharge through another diode junction between the anode gate and the cathode "K" and on through R120.

R117 and R118 control the voltage at which the diode (anode-to-anode gate) becomes forward biased. This feature "programs" the firing of Q102 and prevents the unijunction from controlling this parameter. Therefore, the changing of firing points from one device to another, together with the temperature dependency of this parameter, is no longer a problem as it can be with conventional unijunction transistors.

The vertical oscillator is synchronized externally to the vertical interval from the vertical drive pulse at R113. At the time of the vertical interval, an external negative pulse is applied through R113, C104, and CR101 to the gate of Q102, causing the firing level of the unijunction to decrease.

The sawtooth voltage at the anode of Q102 is directly coupled to the base of Q103. Q103 is a driver amplifier and has two transistors wired as a Darlington pair; their input and output leads exit as a three-terminal device. This device exhibits a high input impedance to Q102, and thereby maintains excellent impedance isolation between Q102 and Q104.

The output waveform from the unijunction oscillator is not suitable, as yet, to produce a satisfactory vertical sweep. Such a waveform would produce severe stretching at the top of the picture and compression at the bottom. C105 and C106 modify the output waveform to produce satisfactory linearity. The sawtooth waveform output at Q103 is coupled through R122, the vertical linearity control R121, and on to C106 where the waveform is shaped into a parabola. This parabolic waveform is then added to the oscillator's waveform and changes its slope. Slope change rate is determined by the position of the variable resistor R121.

Q103 supplies base current through R123 and R124 to the vertical output transistor, Q104. Height control R124 varies the amplitude of the sawtooth voltage present at the base of Q104 and, therefore, varies the size of the vertical raster on the CRT.

The vertical output stage, Q104, uses a power type transistor which operates as a class A amplifier. No output transformer is required since the output impedance of the transistor permits a proper impedance match with the yoke connected directly to the collector. C107 is a DC-blocking capacitor which allows only AC voltages to produce yoke current. L1 is a relative high impedance compared to the yoke inductance. During retrace time, a large positive pulse is developed by L1 which reverses the current through the yoke and moves the beam from the bottom of the screen to the top. Resistor R126 prevents oscillations by providing damping across the vertical deflection coils.

3.3 HORIZONTAL DEFLECTION

To obtain a signal appropriate for driving Q106, the horizontal output transistor, a driver stage consisting of Q105 and T101,

is used. The circuitry associated with Q105 and Q106 has been designed to optimize the efficiency and reliability of the horizontal deflection circuits.

A positive going pulse is coupled through R127 to the base of Q105. The amplitude and duty cycle of this waveform must be as indicated in the electrical specifications (Section 1.2) for proper circuit operation.

The driver stage is either cut off or driven into saturation by the base signal. The output signal appears as a rectangular waveform and is transformer-coupled to the base of the horizontal output stage. The polarity of the voltage at the secondary of the driver transformer is chosen such that Q106 is cut off when Q105 conducts and vice versa.

During conduction of the driver transistor, energy is stored in the coupling transformer. The voltage at the secondary is then positive and keeps Q106 cut off. As soon as the primary current of T101 is interrupted due to the base signal driving Q105 into cut off, the secondary voltage changes polarity. Q106 starts conducting, and its base current flows. This gradually decreases at a rate determined by the transformer inductance and circuit resistance.

The horizontal output stage has five main functions: to supply the yoke with the correct horizontal scanning currents; develop a "C" VDC supply voltage for use with the CRT; develop a "B" VDC supply voltage for the video output stage; and develop a "D" VDC for the CRT bias.

Q106 acts as a switch which is turned on or off by the rectangular waveform on the base. When Q106 is turned on, the supply voltage

plus the charge on C113 causes yoke current to increase in a linear manner and moves the beam from near the center of the screen to the right side. At this time, the transistor is turned off by a positive voltage on its base which causes the output circuit to oscillate. A high reactive voltage in the form of a half cycle negative voltage pulse is developed by the yoke's inductance and the primary of T2. The peak magnetic energy which was stored in the yoke during scan time is then transferred to C109 and the yoke's distributed capacity. During this cycle, the beam is returned to the center of the screen.

The distributed capacity now discharges into the yoke and induces a current in a direction opposite to the current of the previous part of the cycle. The magnetic field thus created around the yoke moves the scanning beam to the left of the screen.

After slightly more than half a cycle, the voltage across C109 biases the damper diode CR103 into conduction and prevents the flyback pulse from oscillating. The magnetic energy that was stored in the yoke from the discharge of the distributed capacity is released to provide sweep for the first half of scan and to charge C113 through the rectifying action of the damper diode. The beam is then at the center of the screen. The cycle will repeat as soon as the base voltage of Q106 becomes negative.

C113, in series with the yoke, also serves to block DC currents through the yoke and to provide "S" shaping of the current waveform. "S" shaping compensates for stretching at the left and right sides of the picture tube because the curvature of the CRT face and the deflected beam do not describe the same arc.

L101 is an adjustable width control placed in series with the horizontal deflection coils. The variable inductive reactance allows a greater or lesser amount of the deflection current to flow through the horizontal yoke and, therefore, varies the width of the horizontal scan.

The negative flyback pulse developed during horizontal retrace time is rectified by CR104 and filtered by C110. This produces approximately "D" VDC which is coupled through the brightness control to the cathode of the CRT (V1).

This same pulse is transformer-coupled to the secondary of transformer T2 where it is rectified by CR2, CR106, and CR105 to produce rectified voltages of approximately 12 kV (9 and 12 inches) or 9 kV (5 inches), "C" VDC, and "B" VDC respectively. 12 kV or 9 kV is the anode voltage for the CRT, and "C" VDC serves as the source voltage for grids No. 2 and 4 (focus grid) of the CRT. The "B" VDC potential is the supply voltage for the video output amplifier, Q101.

3.4 LOW VOLTAGE REGULATED SUPPLY (Optional on some models)

Some models use a series-pass, low voltage regulator designed to maintain a constant DC output for changes in input voltage, load impedance and temperature. Also included is a current limiting circuit designed to protect transistors connected to the "A" VDC output of the regulated supply from accidental output short circuits and load malfunctions.

The low voltage regulator consists of Q201, Q202, Q1, VR201, and their components. Q203 and its circuitry control the current limiting feature.

The 120 VAC primary voltage (220/240 V, optional) is stepped down at the secondary of T1 where it is rectified by a full wave bridge rectifier CR1. Capacitor C1 is used as a filter capacitor to smooth the rectified output of CR1. Transistor Q1 is used as a series regulator to drop the rectified voltage to "A" VDC and to provide a low output impedance and good regulation. Resistor network R207, R208 and R209 is used to divide down the "A" VDC voltage to approximately +6 VDC and apply this potential to the base of Q202. A reference voltage from zener diode VR201 is applied to the emitter of Q202. If the voltages applied to the base and emitter of Q202 are not in the proper relationship, an error current is generated through Q202. This error current develops a voltage across R202 which is applied to the base of emitter follower Q201 and then applied to the base of Q1 to bring the output voltage back to its proper level. R201 and C201 provide additional filtering of the rectified DC voltage.

Operation of this regulator may be better understood by assuming a certain operation condition has caused the output voltage to increase above normal. This positive increase of voltage is transferred to the base of Q202 where it is compared to the zener voltage of VR201. The increase of forward bias of Q202 causes the collector voltage to drop as a result of the increased collector current through R202. This voltage is directly coupled to the base of Q1 through Q201 where it causes Q1 to conduct less and brings the regulated voltage back to its proper state.

The short circuit protection or current limiting action can be explained as follows. Assume the "A" VDC bus becomes shorted to ground. This reduced output voltage is sensed by the base of Q202 turning that transistor off because of the reverse bias across its emitter and base junction. Simultaneously, the increased current

through R204 increases the forward voltage drop across the base and emitter junction of Q203 and turns it on. Prior to the short circuit condition, Q203 was cut off. The increased collector current through R202 decreases the collector voltage of Q203 which is detected by the base of Q201 and direct-coupled to the base of Q1 causing that conductor to conduct less. This closed loop operation maintains the current available to any transistor connected to the "A" VDC bus at a safe level during a short circuit condition. Circuit breakers and fuses are often used for this purpose; however, in the majority of cases, these devices are not fast enough to protect transistors.

Section 4 PRELIMINARY ADJUSTMENTS

4.1 SYNCHRONIZATION AND DRIVE SIGNALS

Apply horizontal and vertical drive signals to the horizontal and vertical drive terminals as indicated on your schematic. Adjust their levels to a nominal +4 V peak-to-peak. The duty cycle of each signal must be adjusted as described in Section 1.2.

The horizontal drive signal is required to initiate horizontal scan and high voltage, and should be connected before applying power to the monitor.

4.2 LOW VOLTAGE SUPPLY

For units which have a self-contained, low voltage power supply, set the DC voltage by variable resistor R208 as indicated on the schematic. This voltage can be monitored at the junction of R114 and R130.

Monitors that use an external DC supply must supply the voltage as specified in Section 1.2.

4.3 BRIGHTNESS

Normally, the monitor will be used to display alphanumeric or other black and white information. Moreover, the video polarity is usually white characters on a black background.

The brightness control should be adjusted at a point where the white raster is just extinguished. The CRT will then be at its cutoff point, and a maximum contrast ratio can be obtained when a video signal is applied.

4.4 VIDEO CONTRAST

Q101 is designed to operate linearly when a +2.5 V signal is applied to its base. Some models incorporate a 500 ohm external contrast control to maintain this level. This control, or a fixed resistor, should be adjusted for a typical signal level of +2.5 V peak-to-peak when measured at the video input terminal of the printed circuit board edge connector. (Refer to the schematic.)

In all cases, the output DC impedance of the video signal source must be 500 ohms, or less.

4.5 VERTICAL ADJUSTMENTS

There is a slight interaction among the vertical frequency, height, and linearity controls. A change in the height of the picture may affect linearity.

- (1) Apply video and synchronization signals to the monitor.
- (2) Set the vertical frequency control, R116, near the mechanical center of its rotation.
- (3) Adjust the vertical height control, R124, for desired height.

- (4) Adjust the vertical linearity control, R121, for best vertical linearity.
- (5) Remove the vertical drive signal from the unit. Or, alternatively, use a short jumper lead, and short the vertical drive input terminal of the printed circuit card edge connector to ground.
- (6) Readjust the vertical frequency control, R116, until the picture rolls up slowly.
- (7) Restore vertical drive to the monitor.
- (8) Recheck height and linearity.

4.6 HORIZONTAL ADJUSTMENTS

Raster width is affected by a combination of the low voltage supply, width coil L101, and the horizontal linearity sleeve located on the neck of the CRT beneath the yoke.

- (1) Apply video and synchronization signals to the monitor. Insert the horizontal linearity sleeve about $\frac{2}{3}$ of its length under the yoke. (If you received a monitor from the factory in which the placement of the linearity sleeve has been determined, make a mark on the sleeve and reinsert the sleeve to this mark when removal of the yoke and linearity sleeve are required.)

If the linearity sleeve is inserted farther than necessary, excessive power will be consumed, and the horizontal output circuitry could be overstressed.

- (2) Adjust the horizontal width coil, L101, for the desired width.
- (3) Insert the linearity sleeve farther under the yoke to obtain the best linearity. Although this adjustment will affect the raster width, it should not be used solely for that purpose. The placement of the linearity sleeve should be optimized for the best linearity.
- (4) Readjust L101 for proper width.
- (5) Observe final horizontal linearity and width, and touch up either adjustment if needed.

No horizontal hold control is used in this monitor. The raster should be properly locked and centered when the horizontal drive signals as described in Section 1.2 are used.

4.7 FOCUS ADJUSTMENT

The focus control, R107, provides an adjustment for maintaining best overall display focus. However, because of the construction of the gun assembly in the CRT, this control does not have a large effect on focus.

4.8 CENTERING

If the raster is not properly centered, it may be repositioned by rotating the ring magnets behind the deflection yoke.

The ring magnets should not be used to offset the raster from its nominal center position because it would degrade the resolution of the display.

If the picture is tilted, rotate the entire yoke.

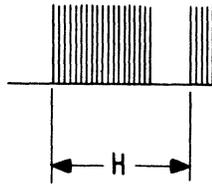
Section 5
TROUBLESHOOTING AND MAINTENANCE

5.1 TROUBLESHOOTING GUIDE

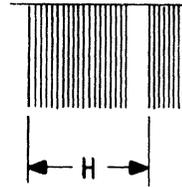
<u>SYMPTOM</u>	<u>POSSIBLE REMEDY</u>
1. Screen is dark	Check "A" bus Q106, Q105, CR2
2. Loss of video	CR105, Q101
3. Power consumption is too high	Check horizontal drive waveform; Check proper placement of horizontal linearity sleeve; Q105, Q106
4. Low voltage bus incorrect (for units with a low voltage supply)	Q202, Q203, Q1 Note: Low voltage supply will indicate low or "0" volts due to its current limiting action if a short is evident in the "A" volt line.

The voltage waveforms are shown in Fig. 2, and Fig. 3 is the interconnecting cabling diagram. Figure 4 shows the circuit board component locations.

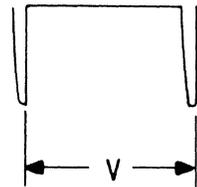
WAVEFORMS



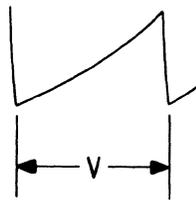
Q101-B
2.5V P-P



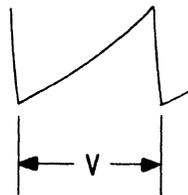
VI-CATHODE
20V P-P



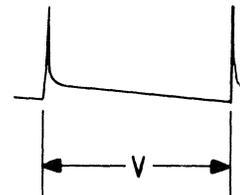
CR101-ANODE
3V P-P



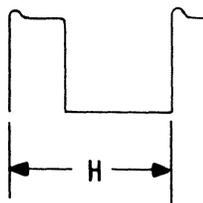
Q103-B
4.5V P-P



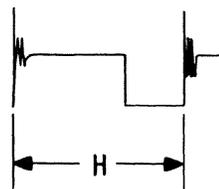
Q104-B
1.2V P-P



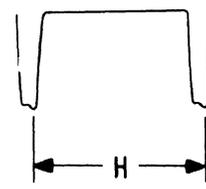
Q104-C
45V P-P



Q105-B
3V P-P



Q105-C
30V P-P



Q106-C
170V P-P

Fig. 2 Voltage Waveform

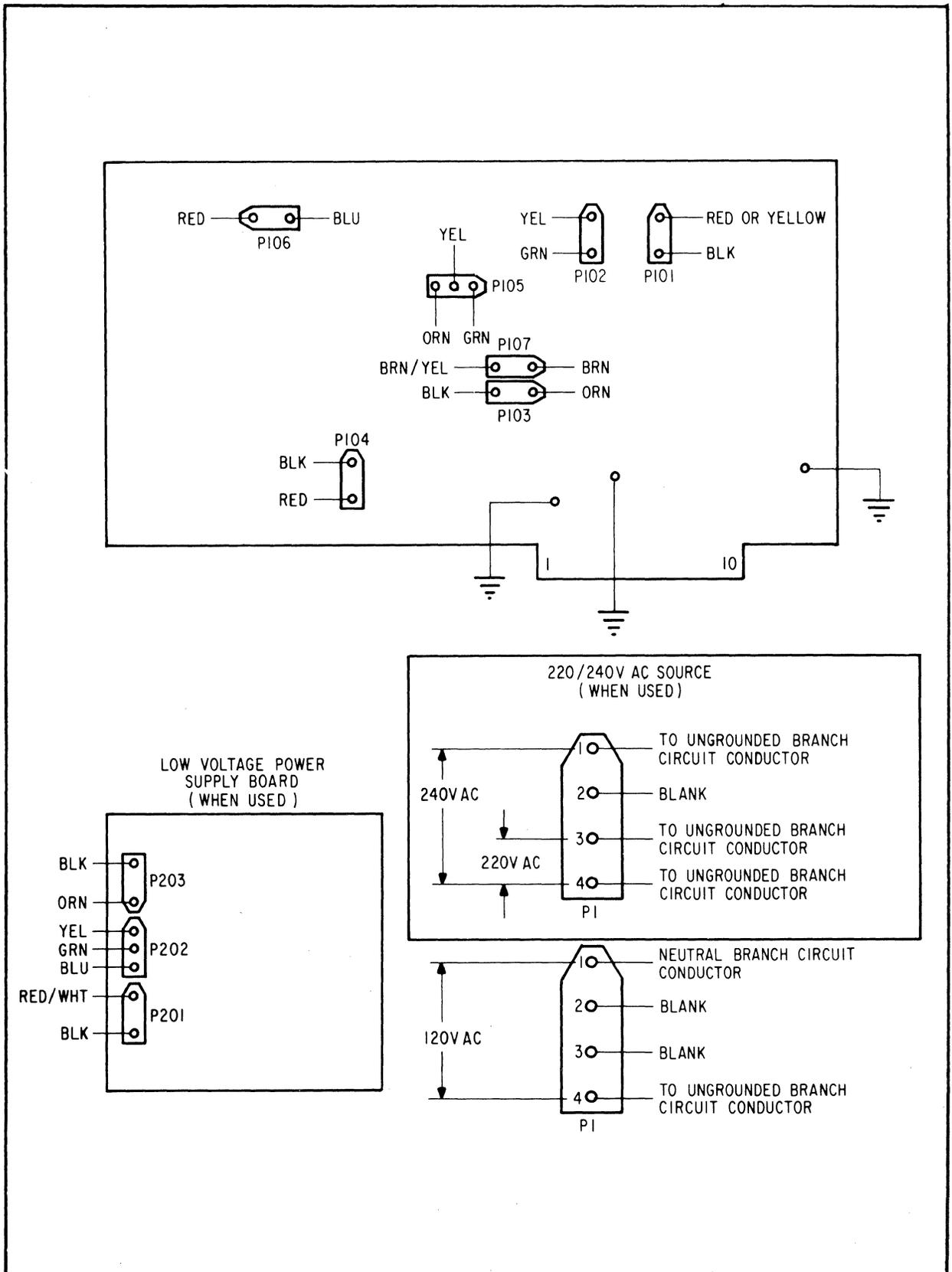


Fig. 3 Interconnecting Cabling Diagram

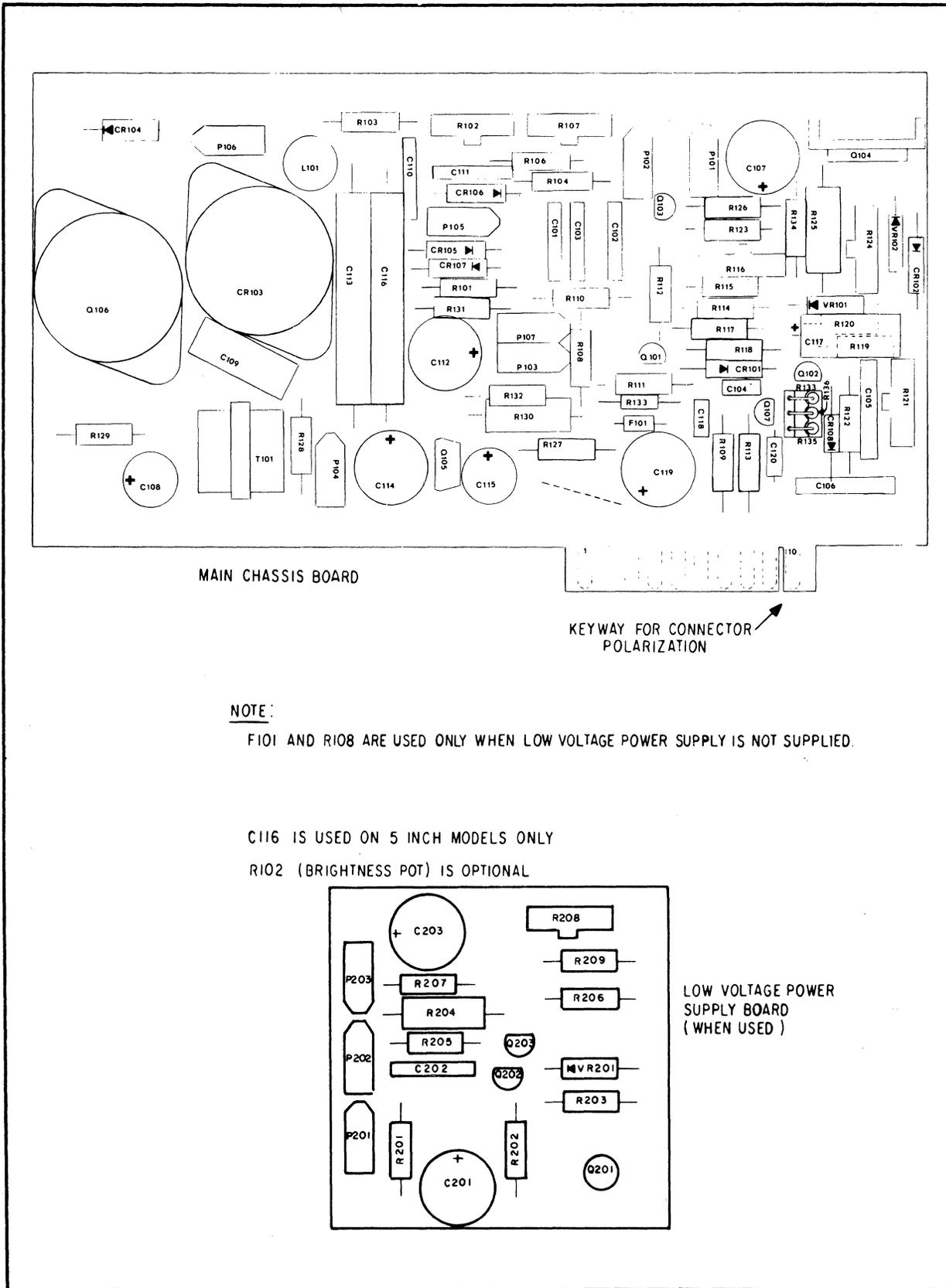
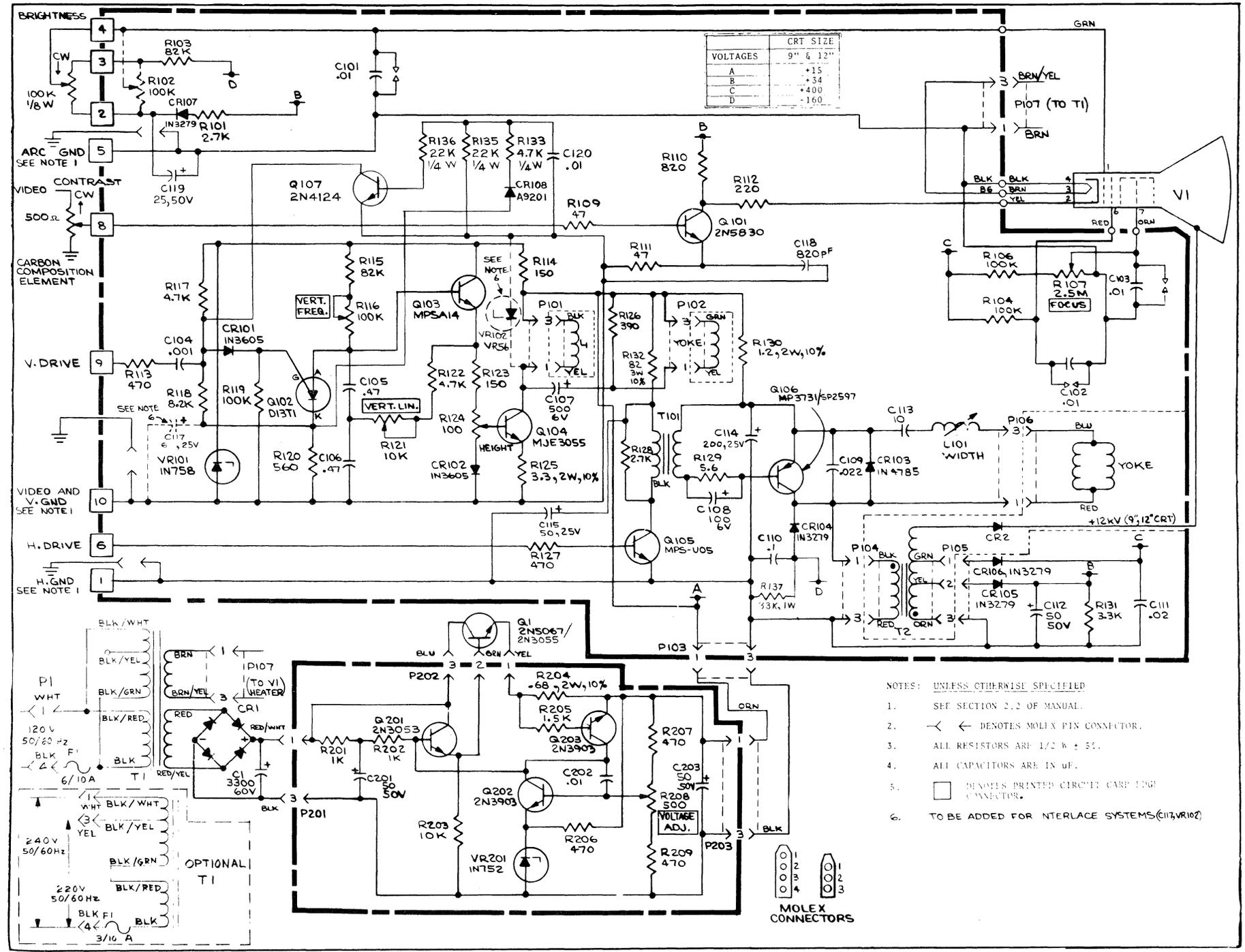
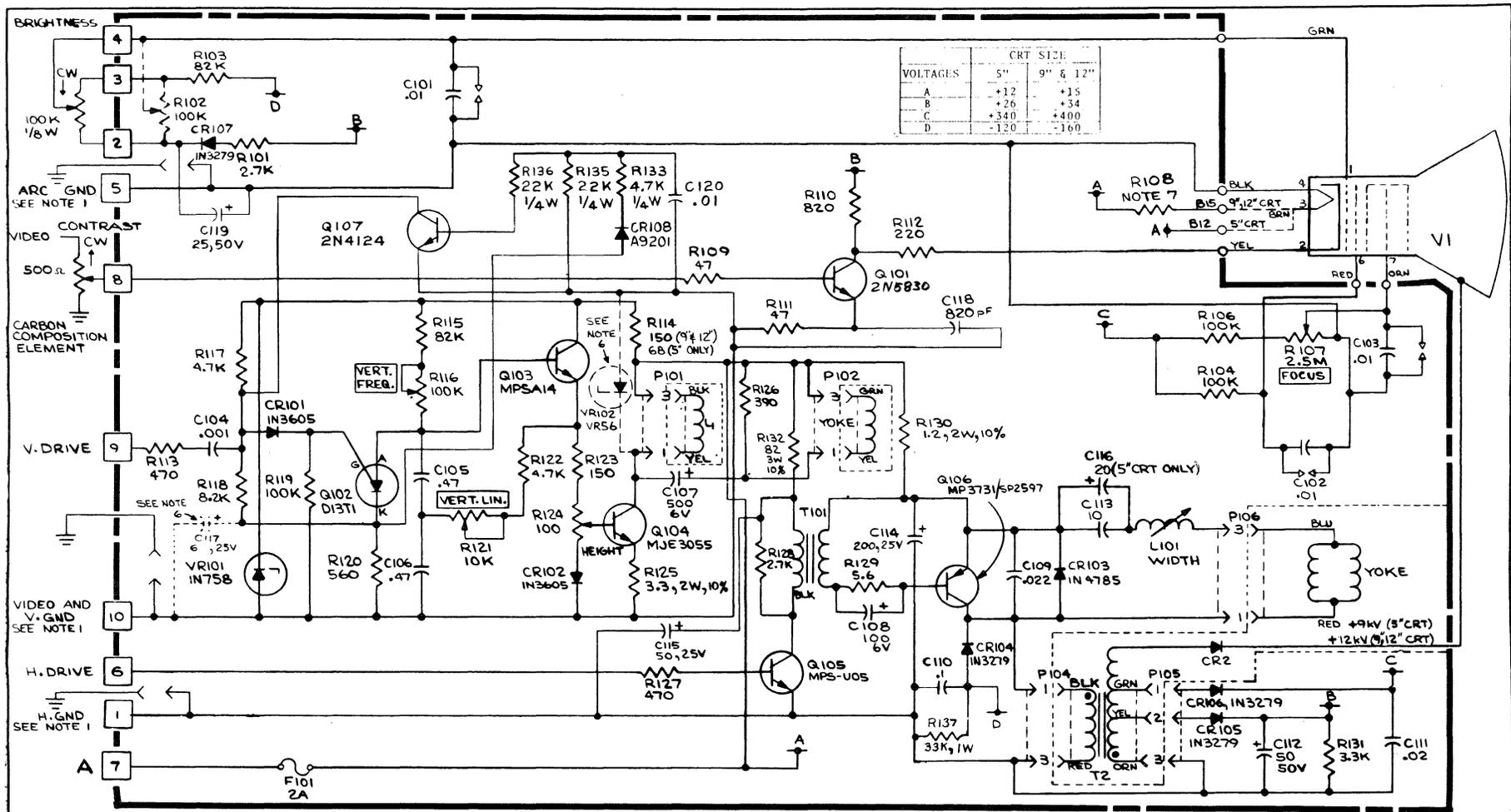


Fig. 4 Circuit Board Components Location

Fig. 5 Schematic, TV 9 and 12 With Power Supply
B-31

Not applicable to Mini-Bee or Super Bee





NOTES: UNLESS OTHERWISE SPECIFIED

1. SEE SECTION 2.2 OF MANUAL.
2. <- <- DENOTES MOLEX PIN CONNECTOR.
3. ALL RESISTORS ARE 1/2 W ± 5%.
4. ALL CAPACITORS ARE IN µF.
5. □ DENOTES PRINTED CIRCUIT CARD EDGE CONNECTOR.
6. TO BE ADDED FOR INTERLACE SYSTEMS (C117, VR102)
7. FOR PROPER VALUE REFER TO PARTS LIST, SECTION 6 OF INSTRUCTION MANUAL.

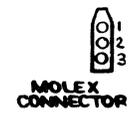


Fig. 6 TV5, 9 and 12 Without Power Supply

APPENDIX C

SECOND SOURCE

(SCINTILLONICS)

POWER SUPPLY DESCRIPTION

TECHNICAL INFORMATION AND THEORY OF OPERATION
POWERBEE

MANUFACTURER: Scintillonics, Inc.
P.O. Box 701
600 Industrial Park
Fort Collins, Colorado 80521
Phone: (303) 482-4752

Scintillonics, Inc. P/N: 1172-01

Beehive Medical Electronics, Inc. P/N: 610-0318-02

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 - 6.1 Sense Connection
 - 6.2 Voltage Adjustments
 - 6.3 Overvoltage Protection Circuit (OVP)
 - 6.4 Overload Protection
7. Maintenance
8. Corrective Maintenance

1. GENERAL

Powerbee is a series regulated multiple output power supply with overload and overvoltage protection. It is designed to operate without forced air cooling and features all silicon semiconductors. The components are mounted in a black anodized aluminum chassis.

2. THEORY OF OPERATION

The following description is for the +5 VDC supply, but can be applied directly to the +15 V and -12 V supplies.

Powerbee is built around three equivalent circuits, each one with its own raw filter supply consisting of a rectifier bridge, BR1, and filter capacitors (computer grade). A ceramic disc capacitor, C3, is used to bypass high frequency noise and transients. The positive output terminal is taken directly from the filter capacitors, C1 and C2, and fed to the load, which leaves the negative side with the series pass transistors, Q4, Q5 and Q6.

An operational amplifier, IC1, is used to compare the sampled output voltage with the reference voltage provided by zener diode, CR1. The sensor and temperature compensating block (ref. block diagram) consists of R7, R8, R9, R10 and CR2. CR2 is used forward biased and is in thermal equilibrium with zener diode CR1. R9 and R10 determine the rate of compensation. Output voltage adjustment is done with potentiometer R2 which divides the zener voltage of CR1. R1 is a biasing resistor. The output from IC1 is fed into an amplifier, Q1, which provides the base drive for the current regulator Q3. The constant current source and Q3 combined provide the driving element for the pass transistors.

The constant current source and the output current limit function are accomplished by resistor R5 and PNP transistor Q2. R5 determines the foldback point of the output current and together with Q2 supplies the base of Q4, Q5, Q6, and collector Q3, with a constant current.

In short circuit mode, Q2 is off and R6 supplies the base current to the pass transistors.

An electrolytic capacitor, C5, is connected across the output to prevent high frequency oscillations. The SCR crowbar, except for the zener diode CR3 which is connected to the + sense for the +5 V supply, is also tied directly across the output.

3. SPECIFICATIONS

Powerbee conforms to the Super Bee Power Supply specifications specified by B.M.E.I.

3.1 INPUT POWER

Voltage: 103 - 127 VAC at 47 to 66 Hz

or 207 - 253 VAC at 47 to 66 Hz

3.2 OUTPUT POWER

Positive 5 VDC @ 7.0 A

Positive 15 VDC @ 2.5 A

Negative 12 VDC @ 2.5 A

3.3 TYPICAL OUTPUT PARAMETERS

Monitored at output (DC) connector.

<u>Output</u>	<u>+5VDC</u>	<u>+15VDC</u>	<u>-12VDC</u>
Load regulation, 0-100%	1.5 mV	18.0 mV	18.0 mV
Line regulation, $\pm 10\%$	1.0 mV	1.0 mV	1.0 mV
Ripple peak-to-peak	2.0 mVpp	2.0 mVpp	2.0 mVpp
Overvoltage protection trigger level	6.1 V	19.2 V	15.6 V
Short circuit current	1.3 A	1.2 A	1.1 A

3.4 DIMENSIONS

Powerbee conforms to Scintillonics drawing no. 1172-201.
The maximum physical size is 9.50" L X 10.00" H X 3.25" W.

4. MOUNTING

Powerbee is provided with two (2) sets of mounting holes, of which one set is used for the Mini Bee terminal and the other set for all other applications.

5. CONNECTIONS

As per B.M.E.I. drawing 610-0318-02 with AC input (connector 1, plug), and DC output (connector 2, receptacle).

<u>Connector 1</u>		<u>Connector 2</u>	
<u>Pin</u>	<u>Function</u>	<u>Pin</u>	<u>Function</u>
1	115 VAC (A)	1	Key
2	115 VAC (B)	2	Ground
3	Chassis ground	3	Ground
4	AC return (A)	4	-12 VDC
5	AC return (B)	5	+15 VDC
		6	Key
		7	5 VDC Sense -
		8	Blank
		9	Blank
		10	5 VDC Sense +
		11	+ 5 VDC
		12	+ 5 VDC

To connect for 230 VAC operation, connect Pin 2 to Pin 4, and connect 230 VAC high side to Pin 1 and AC return to Pin 5.

6. OPERATION

6.1 SENSE CONNECTION

Powerbee can not be operated without remote sensing.

Failure to connect sense will result in an output voltage of approximately 0.9 V at +5 V output pins. This is also a double test that the +5 V OVP circuit (overvoltage protection circuit) operates normally.

6.2 VOLTAGE ADJUSTMENTS

All outputs operate independently of each other and can be adjusted separately. The +5 V output is adjustable from approximately 4.7 V to maximum 6.5 V or until the OVP threshold is reached, through turning the potentiometer, R2, clockwise (CW). The +15 V output has a voltage range from 11.0 V to 16.0 V (potentiometer R22). The -12 V output is decreased from approximately -9.0 V to -14.0 V when adjusting R42 CW.

6.3 OVERVOLTAGE PROTECTION

Each output is protected with a SCR crowbar overvoltage protection (OVP) circuit with preset threshold voltages, typical values are in section 3.3.

In triggered condition, the OVP circuit reduces the output voltage to approximately 0.9 V and the output ripple increases to approximately 5 mV peak-to-peak.

Test procedure: Determination of trigger level for the +5 V output is accomplished simply through adjusting R2 CW until SCR1 triggers. On the +15 V (-12 V) output, adjust R22 (R42) CCW for an output voltage of approximately 13.0 V (-10.0 V). A 2.2K ohm resistor is thereafter paralleled with R28 (R48). The voltage will increase to approximately 16.5 V (decrease to -12.5 V). R22 (R42) can now be adjusted CW until the SCR's trigger and the threshold voltages measured.

NOTE: It is important to keep load current constant during test. If not kept constant, the foldback current limit circuit will reduce the output voltage which then will never reach threshold value.

6.4 OVERLOAD PROTECTION

The output current is limited to 150% or less of rated load current, by a current limit foldback circuit. The foldback point (FB) is set by R5, R25 and R45. These resistor values are a function of the pass transistors gain and are determined in test by SCINTILLONICS, INC.

Short circuit protection is accomplished with the same FB circuit and the short circuit current is approximately 1.0 A.

Overload or short circuit operation over an extended period of time will not effect the power supply and the supply will recover instantly to normal operating mode when the overload conditions are removed.

7. MAINTENANCE

The power supply is a long lasting supply designed to be maintenance free other than the general precautionary practices.

It should be noted, however, that as mechanical shock may damage the transformer shielding effectiveness, careful handling is of importance.

8. CORRECTIVE MAINTENANCE

A malfunction will normally be detected at the output of the power supply by output parameters which are sub-standard to the power supply specifications.

Should repair become necessary, it is recommended to send the unit to SCINTILLONICS, INC., or an authorized repair agent for repair or replacement.

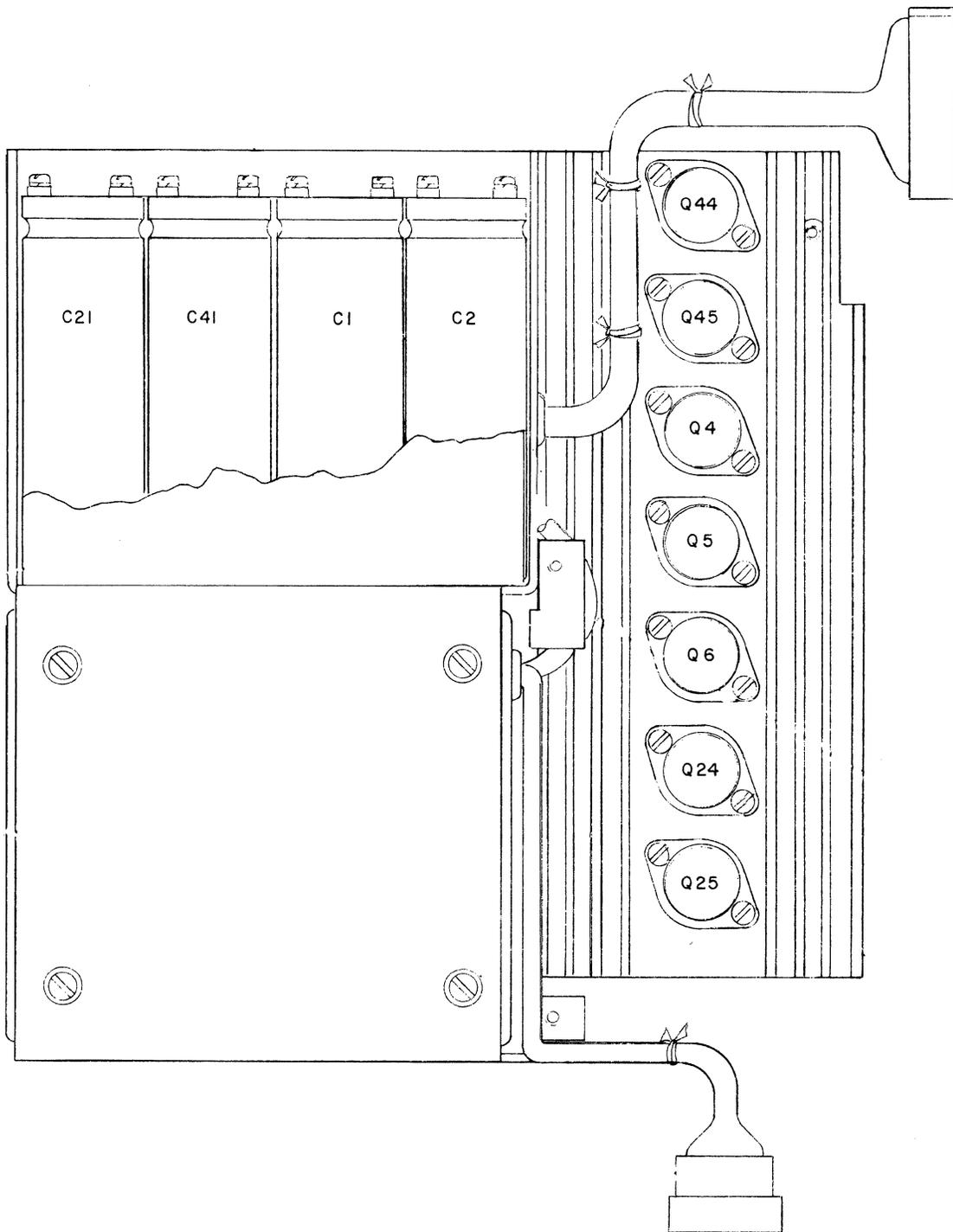


Figure C-1 Powerbee Power Supply

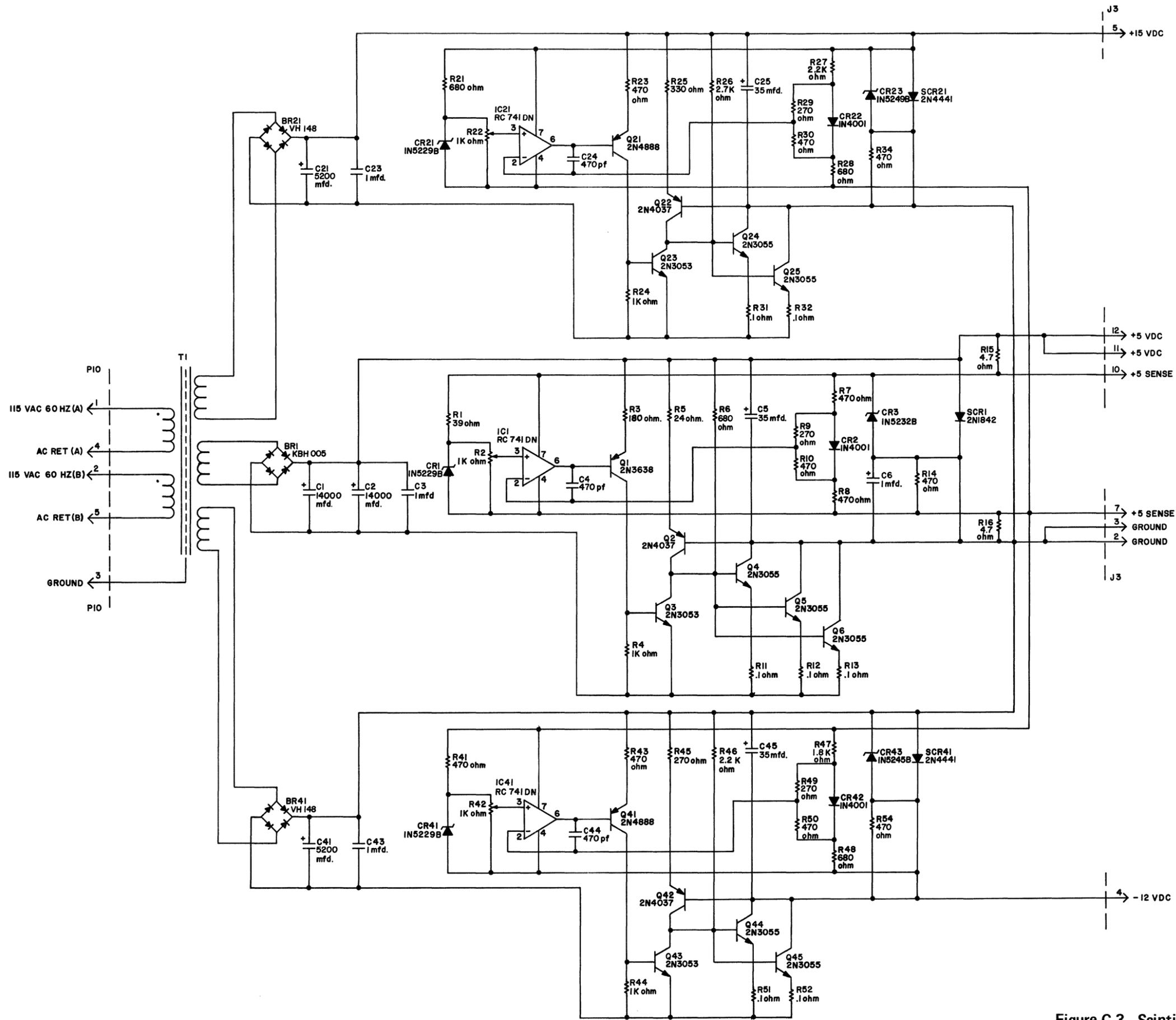


Figure C-3 Scintillonics Powerbee