Brcwn University Graphics System[1]

GLOSSARY

The Brown University Graphics Prcject

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Abstract

This glossary provides informal definitions of some of the more commonly used terms connected with the Brown University Graphics System (BUGS). More detailed information can be found in the META 4 manual, the Vector General manual, and the relevant BUGS publications.

ALU - The Arithmetic/Logic Unit is that part of the CPU which performs general purpose arithmetic and logical operations.

BUGSASM - The Bugs ASseMbler is designed to assemble programs for the two BUGS processors, the META 4A and META 4B. It was created by making numerous changes to a copy of Waterloo's Assembler G for the IBM S/360. This means that BUGSASM can only run on a S/360 and then only under CMS. This fact, although preventing stand-alone BUGS operation, offers the programmer the extensive Assembler G features, particularly in terms of macro generation.

Board - A board is the basic unit of Read Only Memory in the META 4 and has removable adhesive-bonded metallic "bit-patch" patterns, representing bit positions in sequential instructions. A bit patch is binary "1" and the absence of a bit patch is binary "0". There are 32 32-bit ROM instructions per board; sixteen boards fit in one volume.

BOGUS - Brown Operating Graphics University System is the operating system software for BUGS and is comprised of LEVEL0, LEVEL1 (GMS), and any system graphics packages which may be written.

BUGS - Brown University Graphics System is the whole system - hardware, firmware, software, and the basic philosophy behind the system. BUGS was formerly known as 12M, now an obsolete mnemonic.

Bus - A bus (alternate spelling, "buss") is a data transfer path having several sources or destinations connected in common to it. In a typical application, one of many locations on the common bus is selected as a data source, and one location is selected to receive the data.

CPC - A Channel Program Command is the LEVEL0 facility by which LEVEL1 performs I/O to local units, and is initiated by the EXCP extended instruction. A CPC consists of a command, flags, a data address, and a data length. CPC's are similar in format and use to S/360 channel command words (CCW's).

Clipping - Clipping, which is also called scissoring and windowing, is the process of eliminating (portions of) lines not inside the currently defined window on the image space.

Clipping Divider - Clipping divider is a term coined by Ivan Sutherland to denote a special purpose processor capable of clipping to a specified window and perspective division for the 3 dimensional case, using homogeneous coordinate representation. See Sproull and Sutherland, FJCC 1968 for the original article.

Configuration - A configuration refers to the manner in which the components of a computing system--CPU, memory, and peripherals--are connected together. The BUGS configuration includes two META 4's which share core, a card reader, a megabyte disk, a typewriter console, and the Vector General.

Control dial - A control dial (of which there is an array of ten attached to the VG) is a dial used to provide analog numerical information to a display system such as the Vector General.

Control Storage - Control Storage, or control store, is the very high speed storage which contains the firmware for a microprogrammable machine such as the Meta 4. Control storage can be either Read Only Memory or Writeable Control Store, although only ROM is available on the Meta 4. The instruction cycle time for most micro-instructions in the Meta 4 is 90 nanoseconds. See also microprogram.

Control Unit - A special purpose processor which interfaces one or more I/O devices to a multiplexor or selector channel and which directly controls those I/O devices.

Data Tablet - A data tablet is an analog mechanical device giving X, Y, and possibly Z coordinate values into analog input registers of a display system such as the Vector General.

DBR/BP/SBP - The registers used to specify the whereabouts of the data structure to be interpreted by an ETC instruction in the Meta 4B.

Diddle - A diddle is arother name for a control dial.

Disk, Clear - On a clear disk, you can seek forever.

Display Processor - A display processor is a processor whose principal responsibility is graphic data processing for attached display console(s). Typical activities for such a processor are processing graphic device interrupts and providing more advanced features not found in the display console's hardware such as fancy display ("plotting") instructions like conic generation or crosshatching. See Meta 4B.

Doctor Memory - Doctor Memory is a storage maintenance system which provides associative access to disk records through the use of extended instructions. This provides a sort of virtual memory for data on BUGS.

DSC - Digital Scientific Corporation is a small computer company whose chief product is the META 4.

Emulator - An Emulator is a microprogrammed interpreter for a particular target machine, e.g., our "extended S/360" Meta 4A. See also simulator.

ETC instruction - A META 4B instruction used for initiating the interpretation of a data structure by the SIMALE and/or the Vector General.

Event - An event in BUGS terminology is the occurrence of some significant condition, such as an I/O interrupt or a program error, which should suspend execution of the current program and cause an independent event handling routine to be entered.

EXCP - EXecute Channel Program is the extended instruction by which LEVEL1 initiates a sequence of CPC's at a local I/O unit.

Extended Instruction - An extended instruction is an instruction which is executed in software by the operating system instead of by the firmware or hardware. The software is given control because an operation exception is generated by the firmware for extended instructions. Extended instructions are much slower than the equivalent firmware or

hardware implementations would be, but they allow you to change the instruction definitions and/or implementations easily as needed. WAIT, POST, and EXCP are examples of extended instructions in the Meta 4A.

Extended Machine - An extended machine provides the user with a "more useful" target machine by simulating or emulating it on a simpler machine. By this definition, a microprogrammable machine can be said to provide an extended machine to the software, and it is clear that many levels of extension are possible, with each simulator/interpreter running on the extended machine provided by the lower level. See also LEVELs.

Firmware - Firmware is the microprogrammed instruction sequence residing in control store. See microprogram.

FRIEND - FRIEND is either (1) the S/360 interface test program supplied by IBM, or (2) a LEVEL1 program which allows the system debugger to send channel commands to local I/O units and to test the multitasking features of LEVEL0.

Fudd - Fudd is the system debugger which allows examination and alteration of all software accessible stores (e.g., main store, general purpose registers, etc.).

Function Keys - A programmed function keyboard, used in conjunction with a graphics display system, consists of an array of function keys or function switches. When one of these function keys is pressed, an interrupt is sent whose meaning is determined by the program currently running.

Gate - A gate is a logic circuit, having one or more input lines, which performs a specific (Boolean) logic function on these inputs.

GMS - Graphics Monitor System, which is the LEVEL1 portion of BOGUS, provides interactive and program callable command execution of facilities to create and manipulate files, and to run and debug user programs. GMS is (intentionally) very much similar to IBM's Cambridge Monitor System (CMS) running under Control Program-67 (CP) on S/360-67 and provides a significant portion of the CMS facilities.

Homogeneous Coordinates - A 2 space (x,y) point can be represented by a 3 space (x,y,w) homogeneous triple, (w, the homogeneous coordinate, is 1 typically); a 3 space vector similarly can be expressed as (x,y,z,w). Homogeneous coordinate formulation is particularly advantageous in graphics because it allows composition of translation, rotation, scale, and perspective factors in one 4x4 homogeneous matrix which can then be applied at once to a homogeneous vector. See Clipping Divider.

Host Machine - A host machine, or host computer or simply host, is the (possibly microprogrammable) computer on which a target machine is implemented.

IC - An Integrated Circuit is an interconnected array of resistors and transistors fabricated on a single semiconductor crystal or "chip" to implement various digital or linear functions.

ICP - InterConnected Processing can refer to a multiprocessor configuration with at least a minimum of inter-processor communication and possibly some data conversion. As used on the BUGS project it also means a research area into high level communication between the tasks running in the two or more processors, a run-time environment giving the user sophisticated control over the distribution of his program modules, and, ideally, dynamic (i.e., online) changes in processor/task allocation.

Immediate - Immediate is the name given to an event routine which, once entered, must run to completion without being interrupted before another routine can be given control. This is in contrast to a parallel routine.

Interface - The S/360 Interface connects the Meta 4A to a S/360 multiplexor channel (see also 090, 091). The interface, together with the Meta 4A firmware, functions in accordance with IBM's Channel to Control Unit specifications and is non-specific, that is, interpretation of channel commands is left to Meta 4A software. The interface allows data transfer between the S/360 and the Meta 4A at rates up to 100-200K bytes per second, depending on other channel activity.

IPI - The Inter-Processor Interrupt is a non-supportable DSC product which allows two META 4 processors to interrupt each other. Information which is to be passed from the interrupting processor to the interrupted processor must be stored in predefined locations in the common core as the IPI has interrupt capabilities only.

IPL - Initial Program Load is the process by which the firmware (or hardware) causes the initial part of an operating system or other program to be loaded into main memory so that the program can then proceed under its own control. On the Meta 4A an IPL is initiated by pressing the IPL button on the Control Panel.

Joystick - A joystick is an analog mechanical device used to enter X, Y, and Z coordinate values into the analog input registers of a display system such as the Vector General.

LEVELs - BOGUS has an "extended machine" or structured approach to the design of its operating system, which allows each "level" to run on the extended machine provided (simulated) by the lower levels.

LEVEL0, the lowest level, provides:

1. Generalized event handling effected by both immediate and parallel execution of event handler routines;
2. LEVEL1-controlled event signalling;
3. Advanced I/O capabilities, supporting S/360 CCW-like CPC chains to "intelligent" I/O units;
4. Free memory management.

LEVEL1 is GMS.

LEVEL2 is currently the level on which user programs run.

Light Pen - A light pen is a photosensitive pen-like device used to indicate a particular position or element displayed on a CRT display scope such as the Vector General or the Mod 3.

Link - A hardware/firmware device providing a means of communication between the Meta 4A and a multiplexor channel of the S/360.

LSD - Language for Systems Development is a PL/I-like higher level language which will eventually generate code for both

the S/360 and the Meta 4A, and in particular will provide a powerful higher level language for use by sophisticated graphics applications.

LSI - Large Scale Integration is a type of integrated circuit (IC) technology which has a very high density of circuit elements, and thus enables more complex circuitry to be put on a single integrated circuit "chip".

Matrix Multiplier - A matrix multiplier is a special purpose processor, typically with multiple parallel processing elements, designed to optimize the product-sum operations involved in working with matrices. Matrix multipliers are of particular use in calculating graphic transformations (see Homogeneous Coordinates).

MECL - MECL is the Motorola trade name for their line of Emitter Coupled Logic. Emitter coupled logic is characterized by small logic voltage swings and non-saturating transistors which allow very high speed operation (e.g., 1-4 nanosecond propagation delay typically). The use of MECL in the SIMALE enables the SIMALE to have the short cycle time (20 nanoseconds) that it will have.

META 4 - A META 4 is a microprogrammable processor manufactured by Digital Scientific Corporation. In BUGS there are two META 4's, the Meta 4A and the Meta 4B, which share core and which are connected via an inter-processor interrupt (IPI).

Meta 4A - The Meta 4A (sometimes shortened to "M4A") is a general purpose local processor with a S/360-like instruction set. The Meta 4A runs user written or system provided routines, controls the display processor (Meta 4B), provides capabilities for stand-alone graphics, and controls I/O to local peripherals and the S/360-67.

Meta 4B - The Meta 4B (sometimes "M4B") is the display processor component of BUGS. In addition to controlling the Vector General and providing general purpose processing capabilities, the Meta 4B also provides the user with graphic data display instructions, graphic device interrupt handling facilities, and other capabilities not implemented in the display unit's hardware.

M4SIM - Meta 4 SIMulator is a simulator which simulates the META 4's host operational characteristics to facilitate the debugging of microcode.

Microprogram - A microprogram is a program structured sequence of commands which resides in control storage and can be translated by hardware into hardware controls of gates, registers, busses, core, and other logical components, and as such controls the operation of a processor.

MODU(LE) - MODU is the type designation given to GMS files containing a relocatable loadable program image, or "load module." A program must be in MODU format to be loaded and executed by GMS.

MOS - Metallic Oxide Semiconductor is a type of integrated circuit (IC) technology characterized by the storing of information by the presence or absence of a charge. In order to maintain the information contained in MOS, it must periodically be refreshed. However, MOS still requires less power than core memory, which together with its faster access time and its more compact size is making MOS increasingly used in building memory units.

MSR - The Machine Status Register, target register 0 on the Meta 4A, contains the condition code, a settable/testable flag, the instruction length code, wait bit, privilege bit, as well as bits to enable arithmetic overflow, stack overflow, local I/O interrupts, S/360 initial select interrupts, and parity interrupts. Together with the PC, the MSR is similar in function to the S/360's PSW.

MULTIPAC - Software package supplying Meta 4A/Meta 4B communications, Meta 4B control, and Meta 4B I/O unit monitoring.

NIP or GMSNIP - The Nucleus Initialization Program is loaded upon Initial Program Load (IPL) and has the responsibility of loading the LEVEL0 and LEVEL1 programs into memory and starting them up.

Null Meta 4B - The Null Meta 4B was an interim display processor which made the Meta 4B look like the Vector General, and

thus provided access to the display scope until the full M4B was implemented.

Panel, Control - The control or programmer's panel, the lower of the two black panels on the Meta 4A, allows the user to examine and change registers and core locations, to IPL, to stop and start his program, etc.

Panel, Microprogrammer's - The microprogrammer's panels on the Meta 4A and Meta 4B allow manual control of the microprogram. In particular they provide such capabilities as examining and modifying the firmware registers, entering and executing a single micro-instruction from the panel, starting the microprogram at any given point, and executing a micro program a single step at a time.

Parallel - Parallel is the name given to an event routine which can run independently of and concurrently with all other routines in memory. LEVEL0 supports an "arbitrary" number of parallel routines at any given time. See, immediate routine.

PC - The Program Counter is target register 1 on the Meta 4A and contains the address of the next instruction to be executed.

Peel - To peel is to physically change a ROM bit from 1 to 0, or by extension, to change an unpeeled section of ROM to microcode.

Pen Tracking - Pen tracking, or light pen tracking, is a graphics technique whose principal (and defining) capability involves displaying a position-indicating pattern, sensing the position of the light pen relative to the pattern, and updating both the pattern and the state of program itself to correspond to the new position of the pen as it is moved across the screen.

Pipelining - Pipelining is the overlapping of the sub-operations involved in the decoding and execution of an instruction with those of other instructions. This enables several instructions to be "executed" in parallel and allows the total execution time for a program to be (hopefully significantly) less than the total of the execution times of the individual instructions.

Procedure stack - A save area stack used for maintaining procedure invocations and returns in the Meta 4E.

Q-interpreter - A host program which maintains and interprets "assembly-language" instructions in the Meta 4A and Meta 4B. Other names are emulator, firmware, and microprogram.

Register - A register is a storage unit whose contents can be directly used in high speed arithmetic and logical operations.
The META 4 has an Arithmetic/Logic Unit (ALU) which operates on data from two busses, the A and B busses, and puts the result on a third bus, the D bus.

A destination register is a register which has been selected to be loaded from the Arithmetic/Logic Unit output bus, which on the META 4 is the D bus.

A source register is a register from which data is routed to the Arithmetic/Logic Unit.

A single bus register is a register that can be selected as a source on only one input bus because it is physically connected to only that bus.

A double bus register is a register which can be selected as a source on either input bus. All the non-memory and I/O registers in the META 4's in BUGS are double bus registers.

An I/O register has its contents available to external peripheral equipment, typically via an interconnecting cable, and as such has its function determined by the device to which it is attached. In the META 4, I/O registers come in pairs. (V1, V2 is an example of an I/O register pair.)

A memory register is a register which is directly coupled to the memory controller. In the META 4 there is a memory register pair. One register is used for the address of the memory location being referenced, and the other contains the data being read from or stored into that location.

A target register is a register which corresponds to a particular register in the emulated machine. Target registers are loaded and read, therefore, by user programs running on the emulated machine.

ROM - Read-Only Memory is control storage which cannot be modified dynamically. ROS (Read-Only Storage) is an alternate name for ROM. See also WCS.

Routine - A routine is defined in BUGS as a program, logically separate and distinct from all other programs, which is entered upon an interrupt, subroutine call, or via initiation by a parallel routine. All routines must start with an ENT instruction and end with a RET instruction to maintain the stack frame.

Scratch Pad Memory - Scratch pad memory is fast local storage usually available only to the microprogram.

SIMALE - The Super Integral Multipurpose Arithmetic Logic Expediter is a very high speed microprogrammable parallel processing computer which was designed to provide the M4B display processor with special purpose vector/matrix manipulation hardware. Its principal function in BUGS is to serve as a matrix multiplier and clipping divider; however, it is also sufficiently general to provide other special purpose support such as floating point arithmetic. This speed and flexibility is attributable to the SIMALE's four parallel processing elements, and its pipeline processing of instructions in its writeable control store (WCS), and to its use of MECL logic.

Stack Frame - The Stack Frame is a logically "infinite" section of memory used by LEVEL0 to maintain the dynamic link of program execution. When each routine is entered, it should execute an ENT instruction, which causes a register save area and n bytes of automatic storage to be allocated in the Stack Frame for this routine. This new area is then chained back to the previous one, and will be freed when the corresponding RET instruction is executed at the end of the routine.

Target Machine - A target machine is the computer as it appears to the user. See also Host Machine.

TTL - Transistor-Transistor Logic, also called T-squared L (T^2L), is a generic type of digital integrated circuit which is characterized by saturating transistors and large logic voltage swings. TTL is somewhat slower than emitter coupled

logic (see MECL), with 10-20 nanosecond propagation delay typical.

UCB - A Unit Control Block is a block of halfwords used to contain information about a local I/O unit. It contains the unit address, current USH, and any other information needed by the LEVEL0 I/O support routines.

USH - The Unit Status Halfword is the 16 bits of status data received from a local I/O unit upon its interrupting the Meta 4A CPU. The bits specify such things as Operation Complete, Data Error, Unit Busy, etc.

V1, V2 - V1 and V2 are the I/O register pair in the Meta 4B used to communicate with the Vector General. V1 as a destination register is used to send out display orders, and as a source register contains the interrupt request bits. V2 as a destination register is used to acknowledge interrupts and indicate the next Vector General register to be read. V2 as a source register contains the contents of the last register read.

Vector General - Vector General refers to either the company which makes the Vector General Graphics Display System, or the display itself (generally the latter). The Vector General display (VG) is a moderately powerful display unit driven by the M4B. In addition to the normal character and vector drawing capabilities, the Vector General has some local register operations as well as hardware scaling, translation, limited clipping, and depth cueing. Attached to the Vector General in BUGS are an alphanumeric keyboard, a light pen, a joystick, a data tablet, ten control dials (diddles), and thirty-two lightable function keys.

Viewport - A viewport is a section of a display screen, typically rectangular, on which the user is currently displaying data. Usually the image of the user's data space contained in a window is mapped onto an associated viewport for display to the user.

Volume - A volume is the mounting unit in which RCM is physically contained in the META 4. Each volume contains sixteen boards, and as such, there are 512 32-bit RCM instructions per volume. The META 4 can have up to four volumes.

WCH - A Wait Control Halfword is the mechanism by which a routine can wait for the occurrence of some event before continuing with execution. A WCH is similar in use to an Event Control Block (ECB) in the OS/360.

WCS - Writeable Control Store is control store which, unlike Read-Only Memory, can be dynamically modified.

Window - A window is a subsection, typically rectangular, of the picture data space which the user wishes to display. See clipping, clipping divider.

XBD Address - An index-base-displacement address used to generate main store addresses for instructions.

090, 091 - 090 and 091 are the S/360 device addresses at which BUGS is attached to the S/360. Device 090 is a device attachable to a CMS virtual machine which has the characterisitics of a tape drive, and as such can be used to transmit large blocks of data. Device 091 is defined in CP as a 1052 operator's console which can be used as a CP-67/CMS terminal.

1130 - The IBM 1130 is a local processor with only one accumulator and three index registers. By installing the proper ROM, the Meta 4A can emulate an 1130 instead of running as the Meta 4A. The Meta 4A ran as an 1130 until late spring 1972.

2250 - 2250 refers to one of the IBM family of cathode ray tube (CRT) graphic display consoles. 2250 Display Unit Models 1 and 3 (the 2250 Model 2 died a premature death) are attached via a 2840 control unit to a S/360. The 2250 Display Unit Model 4 is attached to an 1130. All 2250's must rely on their mainframe for all but exceptionally rudimentary intelligence.

2840 - The IBM 2840 Display Control is the control unit necessary to attach up to four 2250 Model 3's to a S/360 (via a multiplexor or selector channel).

2870 - The IBM 2870 Multiplexor Channel controls transfer of data between I/O devices and main storage in either burst or