9370 SYSTEMS MEMORY

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

- INTRODUCTION AND OPERATION
- FUNCTIONAL DETAIL
- CIRCUIT DETAIL
- ADJUSTMENTS
- MAINTENANCE PROCEDURES
- INSTALLATION PROCEDURES
- RELIABILITY IMPROVEMENT NOTICES
- OPTIONAL FEATURES
- MODIFICATIONS (BRANCH LIBRARIES)

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✓ CHANGES OR ADDITIONS

On "Revised" pages, the check mark (✓) shown to the left of items or subject titles indicates changes or additions since last issue.

NOTE

Pages for Sections VII, VIII and IX will be furnished when applicable.

INDEX

INTRODUCTION

Refer to Figure I-1.

System Memory is a small, fast, Disk Storage type unit designed as an extension of Main Memory capable of an average access of 17ms. It has one rotating disk providing 2M 8-bit characters of storage using the head-per-track principle with non-return-to-zero type of recording. The Unit is self-contained requiring an external A.C. power source and external Input/Output control. Internal circuitry is of the integrated type.

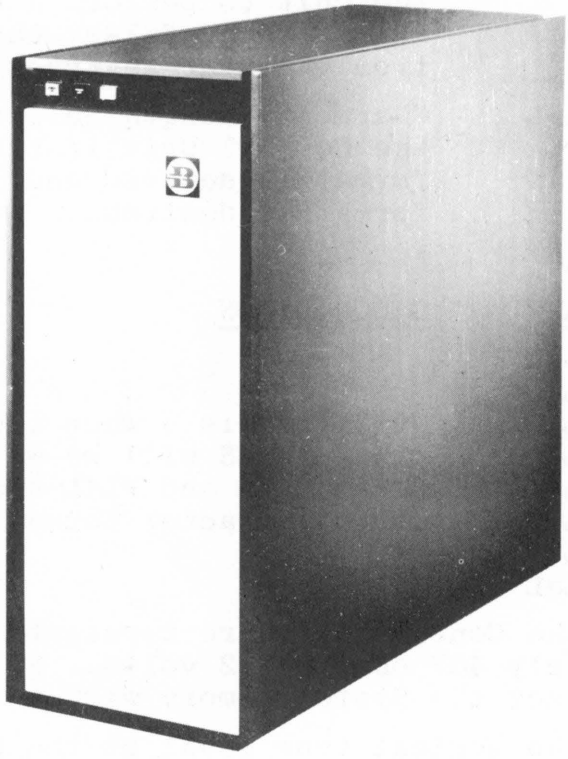


FIGURE I-1
SYSTEM MEMORY STORAGE UNIT

LINES FROM THE DISK FILE CONTROL

CABLE TERMINATOR AAFA0

LINE	PIN #	NAME	DESCRIPTION
1	$ R	T01L	Track Select Lines - when true select one of one hundred tracks using binary coded decimal representation 00 through 99.
2	$ S	T02L	
3	$ T	T04L	
4	$ U	T08L	
5	$ V	T10L	
6	$ W	T20L	
7	$ C	T40L	
8	$ F	T80L	

LINE	PIN #	NAME	DESCRIPTION
9	$ F	DSSL	Disk Head Group Select - when false the first group of one hundred heads is designated. When true, the second group of 100 heads is designated.
10	$ L	WISL	Write Information Status - when true, conditions the System Memory for a Write operation. When false, the System Memory is conditioned for a Read operation.
11	$ M	ITSL	Information Track Select - when true, causes the Unit to perform a Read or Write operation. When false, the Unit is reading from the address track.
12	$ N	CLSL	Character Length Select - tied to true in the Control Unit if the 8-bit character format is desired and false if the 6-bit format is desired.

CABLE TERMINATOR AADA0

LINE	PIN #	NAME	DESCRIPTION
13	$ R	WL1L	
14	$ S	WL2L	
15	$ T	WL3L	Write Levels - when true, designate that binary ONES will be written on the disk. Lines WL3L and WL4L are not used when the 6-bit character format is used.
16	$ U	WL4L	
17	$ V	WL5L	
18	$ W	WL6L	
19	$ C	WL7L	
20	$ D	WL8L	

All lines from the Control Unit are terminated with 133 ohms to ground and approximately 407 ohms to -2 volts. 95 ohms coaxial cable is used to inter-connect the System Memory with the Control Unit.

Logical true - the logical true level at the System Memory end of the cable should be between +2.0 and +2.85 volts.

Logical false - the logical false level at the input shall be between -0.6 volts and -0.35 volts. No input current is required in the false condition. A false condition exists if the input line is open. The input will seek a level of approximately -0.5 volts with no input current present.

LINES TO THE DISK FILE CONTROL

CABLE DRIVER AABA0

LINE	PIN #	NAME	DESCRIPTION
1	$ C	RL1L	
2	$ D	RL2L	
3	$ E	RL3L	Read Levels - when true, indicate that binary ONES were read from the disk. Lines RL3L and RL4L are not used with the 6-bit character format is used. During address read, these lines contain the address information.
4	$ F	RL4L	
5	$ G	RL5L	
6	$ H	RL6L	
7	$ P	RL7L	
8	$ Q	RL8L	

LINE	PIN #	NAME	DESCRIPTION
9	$ I	FCLP	File Character Clock Pulse - during Write the presence of the clock pulse indicates that the System Memory has accepted the character on the WLnL lines and the Control Unit may change the data. Duration of the pulse is two-bit clock times. During Read, the presence of the Clock pulse indicates that a character is present on the RLnL lines. Duration of the pulse is two-bit clock times. The data on the RLnL lines is present for 6-bit clock times after the beginning of the pulse for the 8-bit character format and for 4-bit times when using the 6-bit character format.
10	$ J	LPCP	Longitudinal Parity Clock Pulse - when true indicates that the last (parity) character of a segment is being transferred during a Read operation. LPCP is coincident with the last FCLP. During Write, LPCP is true for the last two characters of the segment.
11	$ K	SACP	Segment Address Clock Pulse - when true indicates that a segment address is being read. Duration of SACP is 4 to 5 bit times.
12	$ M	SURL	Storage Unit Ready Level - when true indicates that the System Memory is Ready.
13	$ R	EUI1L	System Memory Identification Level 1 - tied to true.
14	$ S	EUI2L	System Memory Identification Level 2 - false.
15	$ L	INXD	Index Clock Pulse - when true indicates end of track; duration is 650 $\pm$ 100 nanoseconds.

Logical true - the true output of the line driver at the System Memory end of the cable shall be between +2.1 and 2.85 volts, depending on the output load. Maximum true output current is 45ma.

Logical false - the logical false level is defined as a range of +0.13 to -0.6 volts.

The output of the line driver consists of an emitter follower and a 1K resistor tied to -2 volts. The false output voltage depends on the type of load. The driver is capable of supplying a false current of 18ma to a load which is tied to a voltage more negative than the output of the driver.

GLOSSARY

A49L	Track Address > 49 level used in Group Select Decoding.
ACRL	Address Character Read Level true during Address Read when SnAF's = 12.

ADRF	Address Read Flip-flop true for all ones written in Address Track.
AEFF	Address Enable Flip-flop when true permits counting of Address Character Flip-flops.
BCLP	Bit Clock Pulse
BSFL	Begin Segment Level is true at completion of Address Read.
C1ML	True for one million character option.
C1FF	Address Character Counter 1's Flip-flop
C2FF	Address Character Counter 2's Flip-flop
CCEL	Character Clock Enable Level is true when the circulating clock bit is in S1BF.
CCFF	Character Clock Flip-flop is true for one bit time and indicates the stack-up register contains a full character.
CCFL	Character Clock Flip-flop Level is the buffered output of CCFF.
CDFF	Clock Detect Flip-flop is true during dead space.
CDDL/	Clock Detect Level-Not is true during dead space.
CDDM	Clock Detect Delay Multi is false with continuous clock pulses. CDDM times out in dead space and produces InXP.
CLSL	Character Length Select true for 8-bit character format.
DSSD	Disk Side/Group Select Driver. In System Memory is gated with A49L to decode address to one of four groups of heads.
EWSL	Enable Write Shift Level. True to enable the shift of character bits thru the stack-up register during Write.
FCLF FCLP	File Clock Flip-flop and Pulse. During a Write, the level goes true to signal control that System Memory has accepted the character on the WLnL. The level goes false 3-bit times later. During a Read, the level goes true to signal Control that a new character is on RLnL lines. The level goes false 2-bit times later and specifies sampling time for Control.
HFSL	Head Flying Switch Level true for heads flying. Maintenance Panel Head/Retract Switch is in head position.
HGSL-01 HGSL-02 HGSL-03 HGSL-04	Head Group Select Levels. True when selected as result of matrix decoding of A49L, DSSD.
IARL	Information Amplifier Reset Level true to condition InRFF.
ICCR	Inside CCW Read Driver output "1".

ICCR/	Inside CCW Read Driver output "0".
ICCW	Inside CCW Write Driver output "1".
ICCW/	Inside CCW Write Driver output "0".
IIFF	Inhibit Information Flip-flop set between all segments and during dead space to inhibit circulating information.
InRF	Information Read Flip-flop true for every "1"s bit written on info track.
InXP	Index Pulse true for at least 600 nanoseconds occurring at dead space.
ITFF	Information Track Flip-flop true after address coincidence.
ITSD	Information Track Select Driver buffered output of ITSL.
ITSL	Information Track Select Level true indicates address coincidence and causes unit to perform Read or Write operation. When false, Unit is reading address track.
ITSS	Information Track Select Driver output switches.
IWLL	Inhibit Write Load Level is true during parity character time when Address Character Counter = 3.
ISCR	Inside CW Read Driver output "1".
ISCR/	Inside CW Read Driver output "0".
ISCW	Inside CW Write Driver output "1".
ISCW/	Inside CW Write Driver output "0".
LPCP	During a Write, the output is true during the last character and the L.P. Character. During a Read, the output is true coincident with FCLF for the L.P. Character.
LWIL	Load Write Information Level. True when the Character Clock is circulated into S2BF during a Write to enable a character to be loaded into the stack-up register.
OCCR	Outside CCW Read Driver output "1".
OCCR/	Outside CCW Read Driver output "0".
OCCW	Outside CCW Write Driver output "1".
OCCW/	Outside CCW Write Driver output "0".
OSCR	Outside CW Read Driver output "1".
OSCR/	Outside CW Read Driver output "0".
OSCW	Outside CW Write Driver output "1".
OSCW/	Outside CW Write Driver output "0".
RFFL	Reset Flip-flop Level true during INXP and during Power Up sequence.
RLnL	Read Lines from System Memory to I/O Control when true indicates that binary ones were read from Disk. They also carry address information during Address Read 1, 2, 3, 4, 5, 6, 7, 8.

RSRL	Reset Stack-up Register Level. True at Character Clock Time.
RSBL	Reset Stack-up Buffer Level true at Character Clock Time.
SnAF	Stack-up Register "A" Flip-flop 1, 2, 4, 8. Most Significant portion of character.
SnAS	Buffer Register Most Significant portion of character. Cross coupled switch output.
SnBS	Buffer Register Least Significant portion of character. Cross coupled switch output of SnBF's.
SA = 12	Stack-up "A" Register = 12. True at the completion of an Address Character Read.
SACF	Segment Address Clock Flip-flop. True at the beginning of Address Read.
SACP	Segment Address Clock Pulse buffered output of SACF.
SRIL	Shift Read Information Level used to shift character bits in stack-up register on Read and Address Search.
SSBL	Set Stack-up Buffer Level true to set Read buffers to corresponding stack-up register Output Lines.
SSTP	Selected Strobe Pulse. True for each bit time after one of four clock outputs are selected during Read.
SURL	Storage Unit Ready Level. True when Unit is up to speed and heads are flying.
TnnD	Driver output of Track Select Lines from external. Decoded to select one of 50 tracks and one of four head groups.
TS (00-50) TS (10-60) TS (20-70) TS (30-80) TS (40-90)	Track Select Decoding Levels and are true if neither term is selected.
TSUL-nn/	Track Select Units Level true when not selected.
WICF	Write Info Control Flip-flop. True indicates Write operation, False indicates Read operation.
WIFF	Write Information Flip-flop set to Write a "1" bit RESET to write "0".
WISD	Write Information Status Driver-output of WISL received from external to condition System Memory for Write operation.
WLnL	Write Levels when true designate a binary ones to be written on Disk.

Functional Detail

GENERAL DESCRIPTION

System Memory is a free-standing self-contained Unit.

DIMENSIONS

20" Wide
46" Long
45" High

A.C. POWER REQUIREMENTS INPUT

120/208	60 cycle
115/230	60 cycle
220, 230 or 240 volts	50 cycle

Power Supply outputs, all non-adjustable with a ± 5% tolerance are: -2, -12, -24, +4.5 and +12 VDC; 24 VAC.

With reference to Figure II-1, note the Maintenance Panel and its associated switches; the circuit breaker, the drive motor, squirrel cage blower, the CW Head Support Assembly, and the window for viewing CW face of disk.

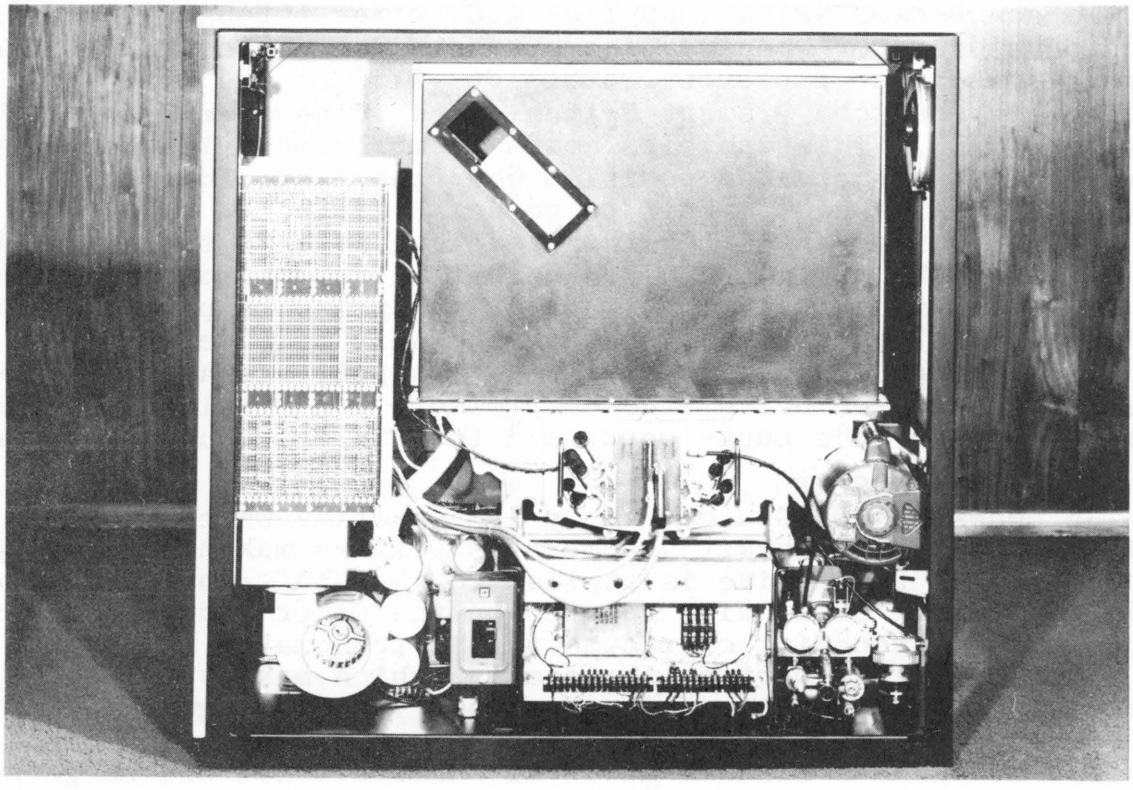


FIGURE II-1
SYSTEM MEMORY - RIGHT HAND VIEW

Functional Detail

CONTROLS & INDICATORS - FRONT PANEL

A.C. Power On Switch
A.C. Power Off Switch
Not Ready indicator

NOTE: 24 A.C. Supply and backplane blower are not affected by A.C. On/Off Switches. These are controlled only by unit circuit breaker.

MAINTENANCE PANEL

Touch Reset Button - Resets touch circuitry
Head-Retract Switch - in retract position inhibits heads from flying
D.C. On Indicator - when on indicates D.C. applied to backplane
D.C. Lockout removes input A.C. Power from D.C. Supply
Motor-On Switch - when off removes A.C. Drive Motor Power
Running Time Meter - monitors drive motor running time

AIR PRESSURE & REGULATION

Positive air pressure is utilized to fly the heads and pressurize the enclosure. Pressures maintained are as follows: 22 PSI $\pm$ 2 to the head actuators and approximately .7 inch of water in the enclosure. The sediment filter bowl serves as the air pressure tank.

The compressor switch supplies A.C. power through its contacts to the compressor motor whenever the pressure decreases to 35 PSI and removes it when the pressure reaches 60 PSI.

The Air Pressure Present Switch opens whenever manifold pressure drops to 30 PSI. This inhibits heads from flying. The Ready Switch returns to its un-actuated position when the manifold pressure drops below 25 PSI which causes Unit to go Not-Ready.

The fan which ventilates the backplane is also the source of positive air for the enclosure. Fan operation is monitored with an airflow switch. Without airflow, this switch prevents power from being applied; during operation, it causes the Unit to Power Off.

Referencing Figure II-2, note power supply sub-assembly; pedestal, shaft and associated drive; the compressor; the final filter; the electronic cards; the purge port; and the CCW Head Support Assembly.

DISK DRIVE & ENCLOSURE

The pedestal for System Memory is a casting which provides a housing for the drive shaft assembly as well as making up part of the enclosure. The belt drive is applied to the shaft on one side of the housing, with the disk being mounted on the other side. Also on the shaft are dual grounding contacts and the tachometer reluctance pick-up. Mounted to that part of the casting which makes up the enclosure are the head castings, one on each side. These are guided into place with dowell pins and bolted on. Each head casting houses eight information heads plus a clock head. The enclosure has one purge port and there are windows for viewing both disk faces.

HEAD FLYING, HEAD ASSEMBLIES

FLYING HEAD PRINCIPLES

The following description covers the principles which enable the Disk Head Assembly to be operated at approximately 95 microinches from

the disk surface.

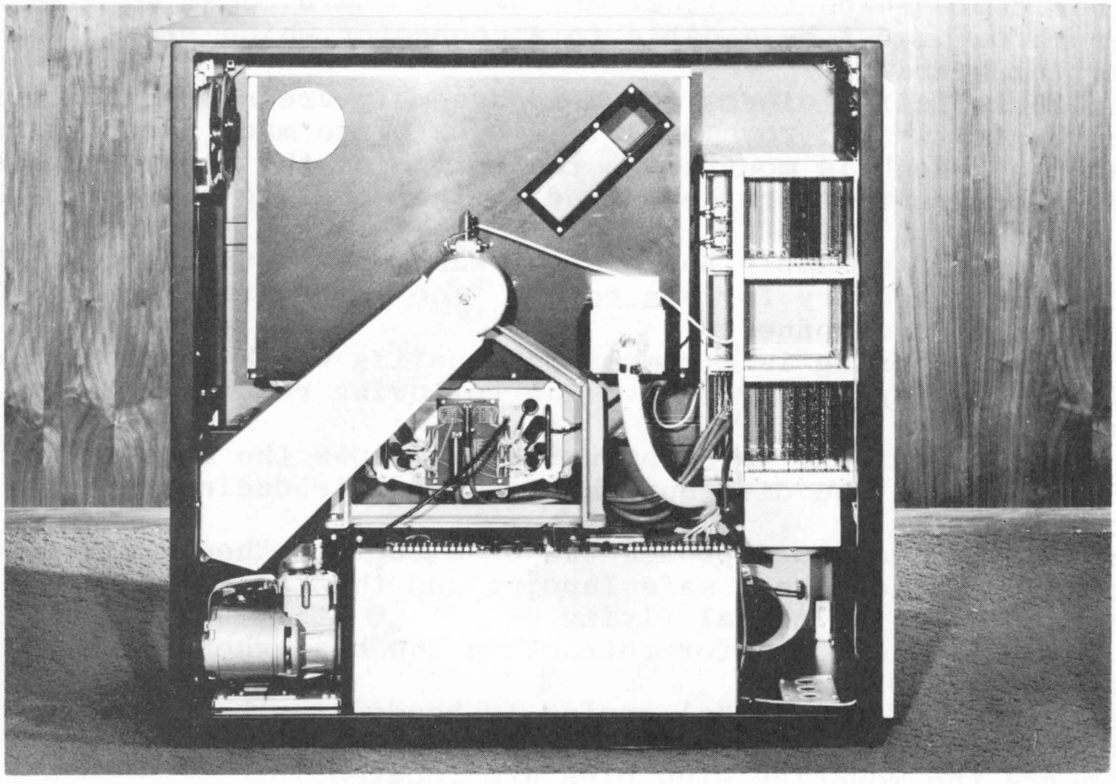


FIGURE II-2
SYSTEM MEMORY - LEFT HAND VIEW

The velocity and force of the air layer developed by a rotating disk increases linearly along the disk radius toward the outer edge. An "airborne" head is repelled by this force and therefore "flys" on top of the air layer. It can be seen that the flying gap of a head mounted near the outer edge would tend to be greater than the gap of a head closer to the disk hub. To overcome the repellant force of this laminar air, a calibrated amount of air pressure is applied to the head actuator assembly. With a compliant head mounting, such as the Gimbal spring, the head can make small self-adjustments in attitude while it is being "landed" (forced into "flying" position). By utilizing these principles, an extremely small head to disk gap can be achieved.

Rigid standards must be maintained in the finish of the disk to prevent turbulence in the laminar air. The head must have the proper aerodynamic shape and surface finish to "fly" parallel with the disk. It must ride the laminar air cushion without fluttering or creating its own turbulence. A beveled leading edge gives the head assembly its "flying" capabilities.

HEAD ASSEMBLIES

Thirteen individual heads for an information head assembly or six individual heads for a clock head assembly are mounted in a "shoe" made

of a special compound. Adjacent core separation is 40 - 45 mils and 110 - 115 mils for information and clock heads, respectively. Two "touch" pins are embedded in each shoe. A specially designed etched circuit board, upon which the head assembly is mounted, permits connection of cable leads to either end of the board. The head assembly leads are brought out by a cable to a connector which plugs into the head casting board.

The 26 isolation diodes per head assembly are connected to the board circuitry in two rows of 13. A back plate made of the same compound as the "shoe" is mounted on the bottom of the circuit board. This plate covers the core leads and is the mounting point for the Gimbal spring

A clock head assembly follows the same description except that it only requires circuitry for six cores. The leads are also brought out in a cable to a connector.

The Gimbal spring is a compliant mounting which connects the head assembly to its support bracket. The following requirements are met by this device:

1. It provides a flexible mounting which allows the head to follow undulations in the disk surface without introducing any skew factor.
2. Permits the head to approach the disk surface "heel" first, at a small angle, to make a safe landing and then align itself parallel with the disk for normal flying.
3. It supplies the force for retracting the head when the actuator pressure is released.

The center of the Gimbal spring is bonded to the head back plate and the outside is riveted to the support bracket at the same two points where the mounting stud pins are located.

Figure II-4 shows the two clock head assemblies and Figure II-5 shows the four different types of information head assemblies. All the "upper" heads are the eight information heads mounted nearest the rear of the Unit. The "lower" heads are the eight information heads mounted nearest the front of the Unit and the two clock heads.

DISK LAYOUT

1	Disk/System Memory
2	Head Groups/Face
50	Tracks/Head Group
100	Segments/Track
100	Characters/Segment
8	Bits/Character

Refer to Figure II-3 for disk layout.

One bit and one address timing track provide timing for the entire Storage Unit. One set of spare clock tracks are written during manufacture of the Unit as protection against a clock head failure in the field.

Information is recorded NRZ, by bit, least significant bit first. An odd parity, longitudinal check character is written immediately after the 100th information character. System Memory has a bit rate of 2.4 Mc, character transfer rate of 300 Kc.

Functional Detail

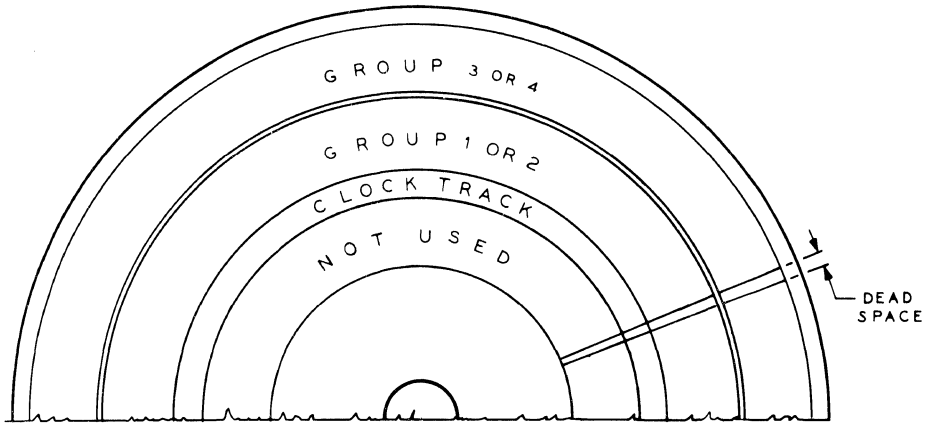


FIGURE II-3
DISK FORMAT

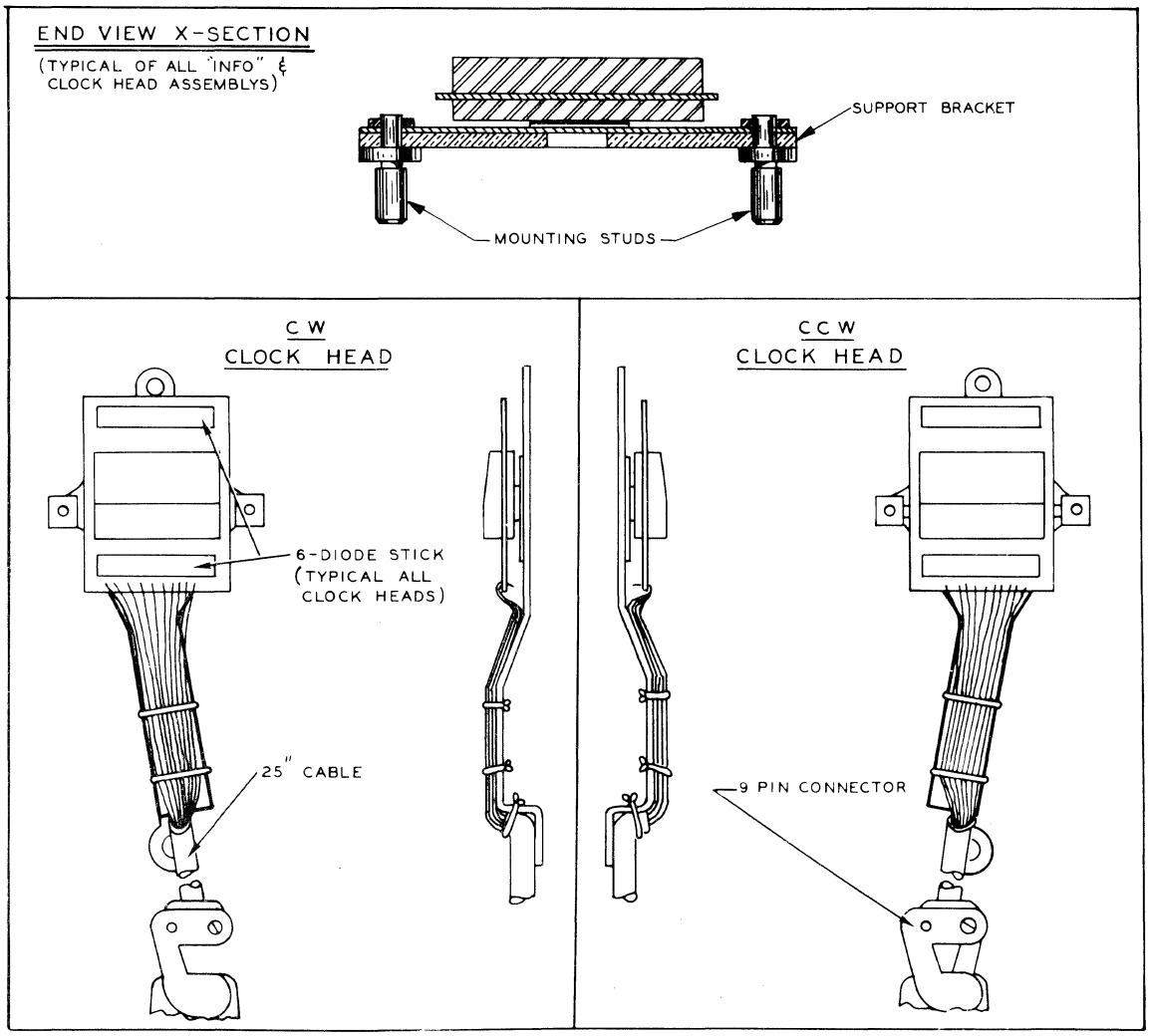


FIGURE II-4
CLOCK HEADS

Functional Detail

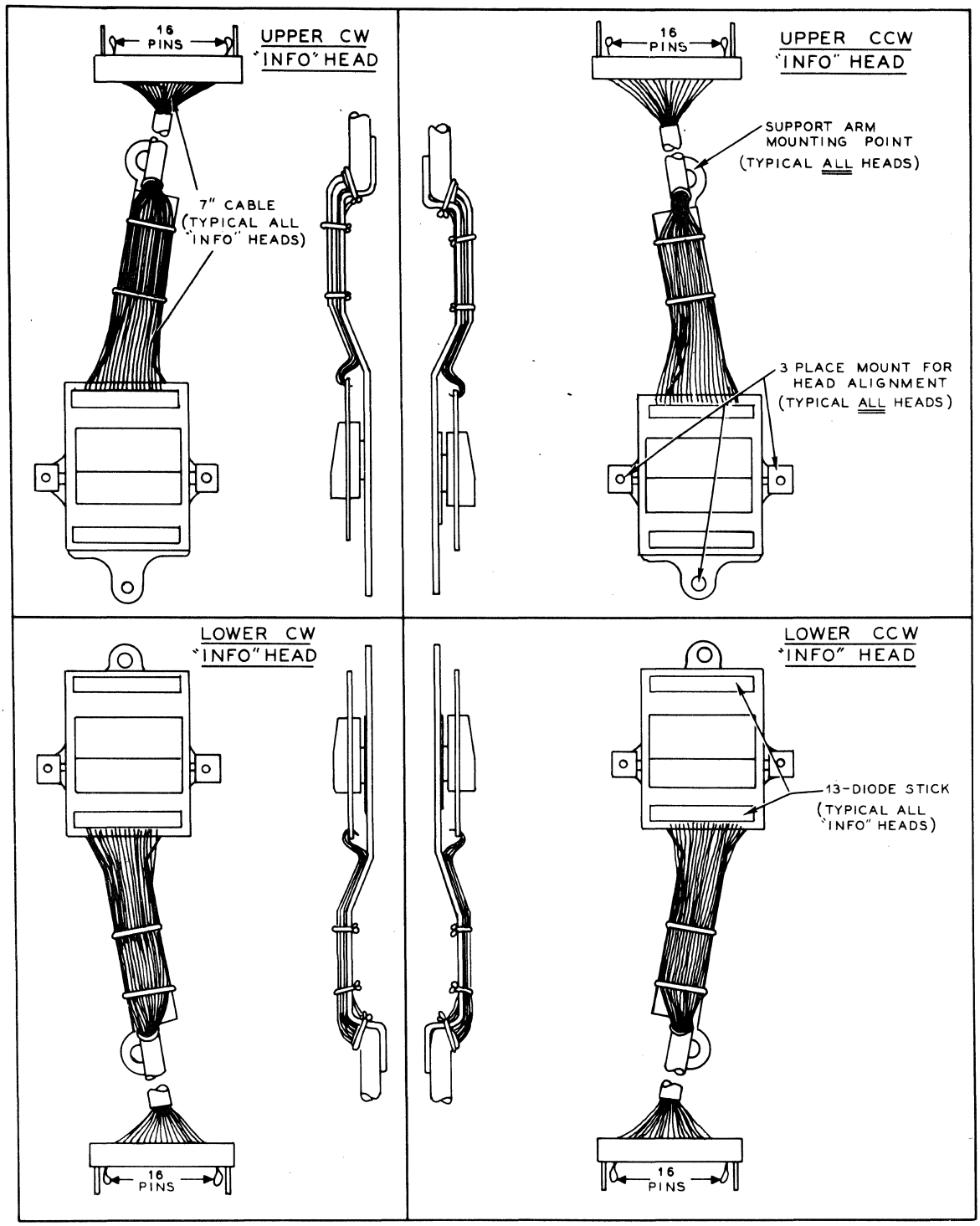


FIGURE II-5
INFORMATION HEADS

Functional Detail

Segments on a given track are separated by a space which is 8-bits long. Each segment is identified by its own address which is written in the address track, least significant character first. These addresses range from 00 → 99. Each track besides having 100 information segments also has one maintenance segment and a 10-20μs dead space. Maintenance segment addresses are just prior to dead space with the actual segment just after dead space.

Referring to Figure II-6, note the relationship of the address characters to information characters of previous segment; the address mark preceeding the address characters; the fact that every address is comprised of four characters, each having the "A" portion with a decimal value of 12, the "B" portion having decimal significance. Example Address is = 00. The Address Mark consists of a "1" bit written on the address track just prior to the Least Significant Address Character. This "1" bit identifies the beginning of an address. The reading of a valid address generates one Segment Address Clock Pulse (SACP), two File Clock Pulses (FCLP), Address Enable Flip-flop (AEFF) to be set, and Begin Segment File Level (BSFL) to come true.

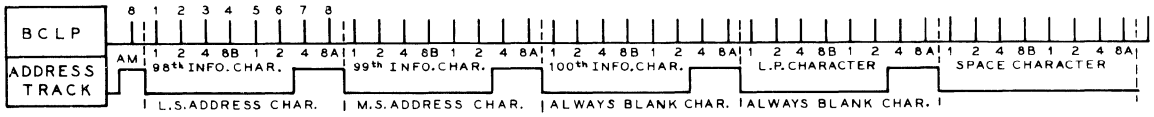


FIGURE II-6
ADDRESS/INFORMATION RELATIONSHIP

UNIT SYSTEM READY

System Memory is considered to be System Ready when the following conditions are obtained:

1. Power On
2. Disk up to speed (approximately 1745 RPM)
3. Reserve pressure not less than 30 PSI
4. Heads flying, i.e., Head Retract Switch in Fly position
5. Touch circuit in the Fly Ready status.

HEAD SELECTION

Since there is only one set of timing tracks for both sides of the disk, the center taps of the clock heads are tied to ground, forward biasing the head diodes to provide continuous clock pulses.

Information Heads are grouped 50 to a group, 2 groups per disk face. All four groups of heads are in parallel so that during Head Selection one head is selected in each group. Track Select Lines (TnnL) and Disk Side Select Level (DSSL) are decoded to produce one of four Head-Group Select Levels (HGSL-01, -02, -03 and -04). Each group of heads has its own individual read group select and write driver. The status of the Write Information Control Flip-flop (WICF), true for a Write, false for a Read, along with one of the HGSL will select one of the four heads for either a Read or Write operation.

Functional Detail

BASIC WRITE

Information is recorded serially by bit, 100 information characters plus the LP check character per segment. Information is received from Control, character by character, on the Write Lines (WLnL). The Character Clock (CCFF) utilized to shift information into the stackup register during a Write is the result of circulating a Clock Bit through the stackup register. After address coincidence is achieved, Begin Segment File Level (BSFL) is true for one bit time.

BSFL = CCFL · C1FF · C2FF · AEFF

On the initialization of a Write operation, S8AF and S4AF are set to one. This will result in a 1-bit being written immediately prior to information.

S8AF = BSFL · WICD
S4AF

Refer to Chart II-1.

CHART II-1.

S8AF Set to 1
S4AF Set to 1
S2AF = 0
S1AF = 0
S8BF = 0
S4BF = 0
S2BF = 0
S1BF = 0

At each successive bit time with Enable Write Shift Level true (EWSL) the two bits are shifted serially down through the stackup register. Information Track Flip-flop is set immediately following the shift of a "1" into S1AF.

ITFF = WICF · ITSD · S1AF

This remains true for duration of the segment.

Since information is shifted out serially through S1BF, when the "1" set into S4AF is in S1BF, the circulating clock bit is in S2BF. These conditions cause Enable Write Shift-Not (EWSL/) to become true.

EWSL/ = S2BF · S4BF/ · S8BF/ · S1AF/ · S2AF/ · S4AF/ · S8AF/

With EWSL/ being true, Character Clock Enable Level is true causing the status of S1BF, which is the "1" state, to be written with the next CCFF (clock) at the beginning of the Addressed Segment.

CCEL = EWSL/ · WICF
CCFF = CCEL

Coincident with this CCFF, the first information character from the WLnL is loaded into the stackup register. At the next bit time the circulating clock bit is set into S8AF.

S8AF = CCFL · WICF

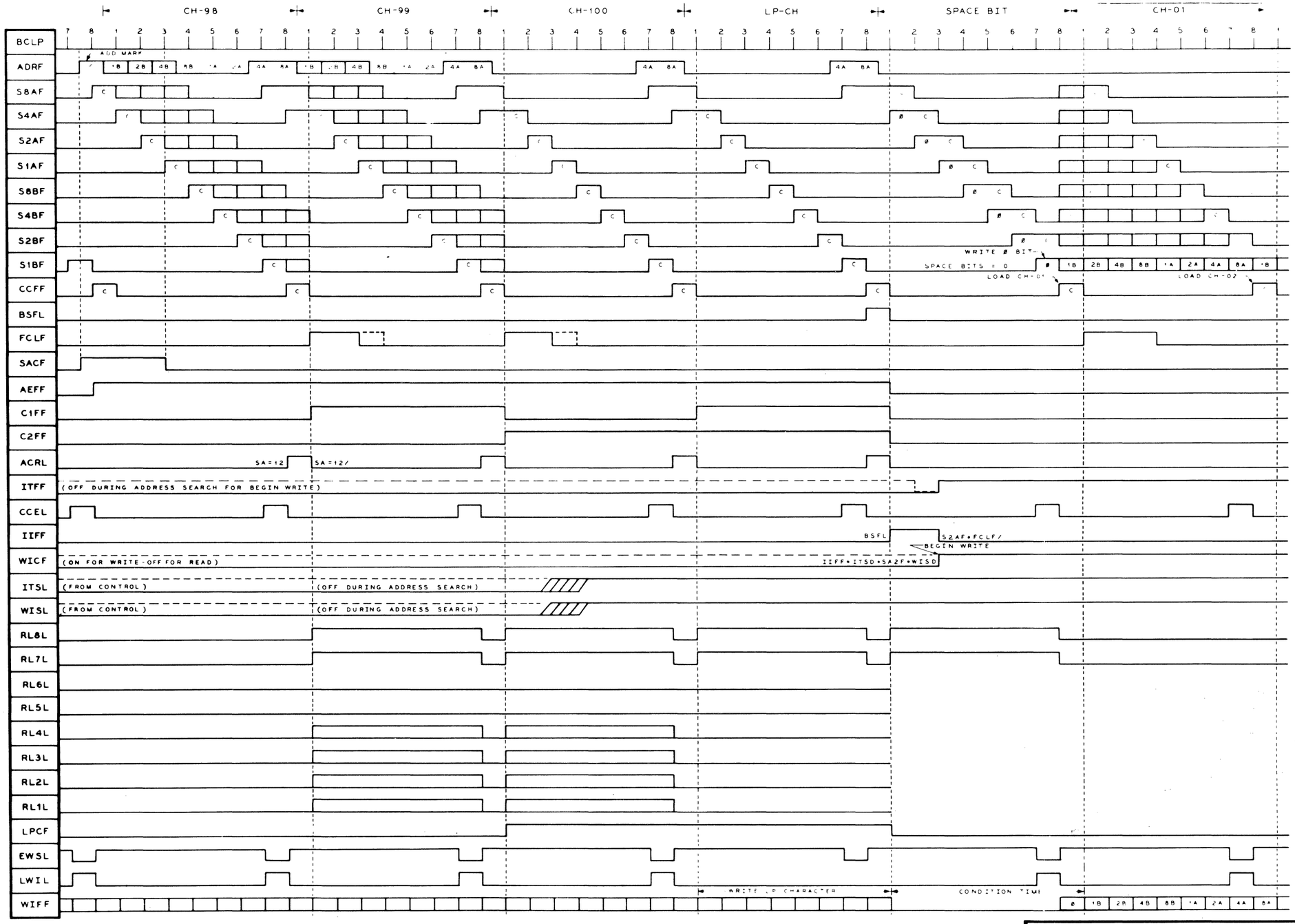


FIGURE II-7
BASIC WRITE

CCFF will generate a File Clock Pulse (FCLF) to notify Control to make the next character available on the WLnLs. At the time the 98th character is loaded into the stackup register, an address mark will generate a Segment Address Clock (SACP). Address Enable Flip-flop (AEFF) is set as a result of this SACP. Address characters will be counted with C1FF and C2FF.

The Longitudinal Parity Clock Pulse (LPCP) will be true when the second address character is read.

LPCP = C2FF · WICF

This signals Control that character 100 is now in the stackup register and the next character to be made available on the WLnL should be the LP character. After writing this LP character, inhibit information is set with the following BSFL and with Control removing Write status, a one segment write is now completed.

BASIC READ

Upon obtaining address coincidence, Information Track Select Level comes true and with WISD/ from Control, a Segment Read is initiated.

As was noted during the Write operation of a given segment, information is recorded as a continuous string of bits always preceeded by a "1" bit. All information as it is being read is first sensed by the Information Read Flip-flop (INRF) and then shifted through the stack-up register at each successive bit pulse time. The initial "1" bit, as it shifts down the stack-up register into S1BF, will permit the first CCEL for this segment read.

CCEL = S1BF · CCFF/ · WICF/

As a result of this CCEL, CCFF becomes set indicating the stack-up register contains the first complete eight-bit character of information.

Set Stack-up Buffer Level (SSBL) coming true sets the contents of the one character stack-up register into the cross-coupled switch Stack-up Buffer making the information available on the Read lines.

SSBL = CCFF · WICF/ · BCLP

Coincident with SSBL, FCLF becomes set signaling Control that a character is available on the Read lines. For successive characters the circulating clock bit is set into S4AF at CCFF time.

S4AF = CCFF · WICF/

The last character of the segment, the longitudinal check character, is flagged as such by LPCP to Control.

LPCP = ITFF · IIFF · WICF/

This completes a one segment Read.

POWER SUPPLIES

The Power Supply is a self-contained unit which may be supplied by various manufacturers. The Test & Field Reference Documents supplied with each S.M. will contain all pertinent data.

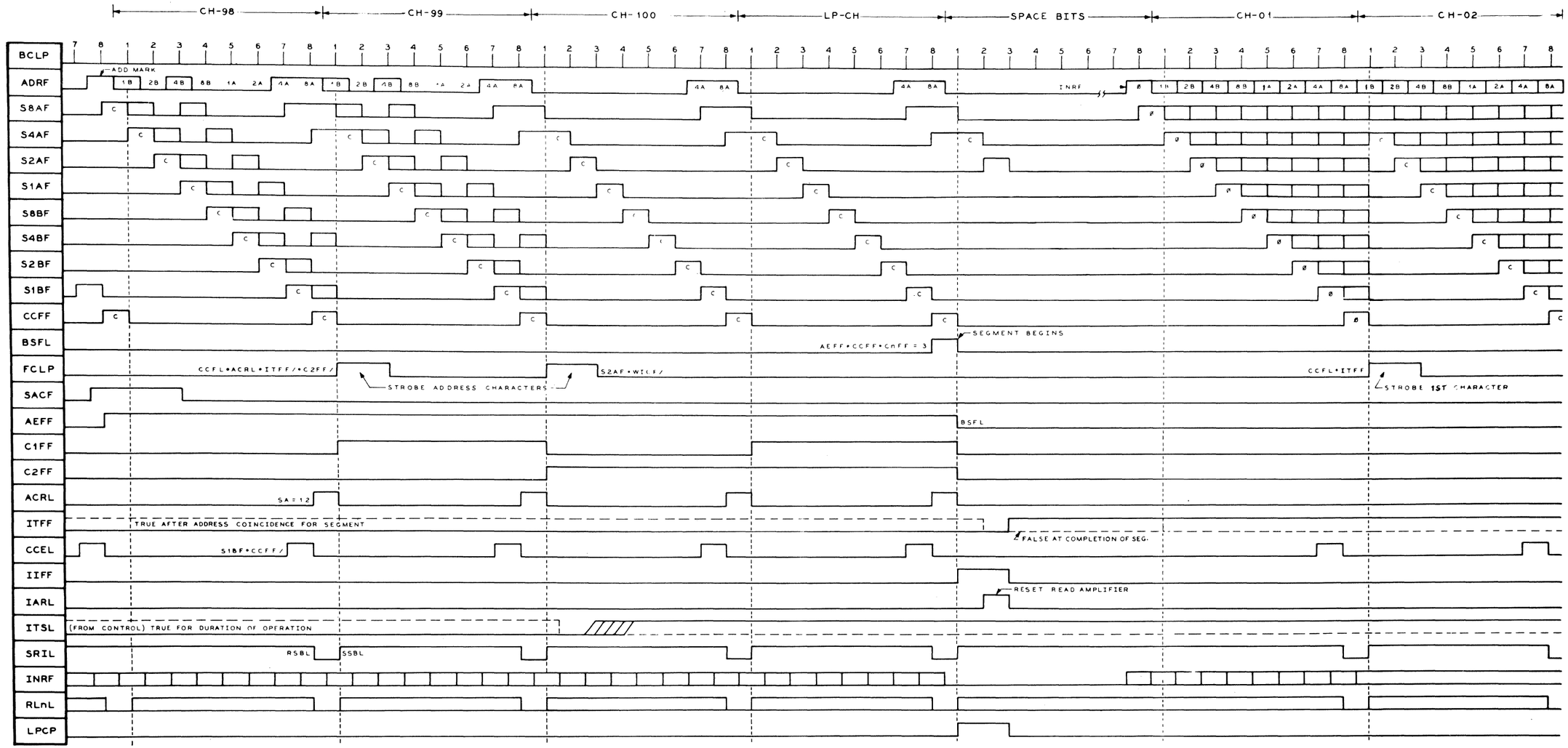


FIGURE II-8

BASIC READ

Circuit Detail

BIG PICTURE

Shown in Figure III-2 is a block diagram of System Memory. Included are all of the lines between Control and System Memory, the cards with their locations, and the backplane locations of many logical levels for quick reference.

As shown in the block diagram, the heads are divided into four groups (G01, G02, G03 and G04) each group with their own Write Driver and Read Group Select.

There are two clock head assemblies, one of which is not connected except for its touch circuit. The other has the center taps tied to ground so that BITLs and ADRLs are always available at the input of the Clock Read Amps.

During a Write or Read operation, one of the fifty Center Tap lines is switched to ground by one of the center tap select circuits controlled by the Track Decode Matrix. This grounds one head center tap in each head group.

If a Read operation is involved, one of the four heads is selected by activating one Read Group Select Circuit as determined by the Track Decode Matrix. This routes the desired read signal to the Information Read Amp, through INRF and into the Stack-up Register. When the Stack-up Register is filled, the information is shifted to the Stack-up Buffer (SnAS and SnBS) which places the information on the Read Lines (RLnL's) to await a memory cycle while the Stack-up Register begins filling with the next character.

If a Write operation is involved, one of the four heads is selected by activating one Write Driver Circuit as determined by the Track Decode Matrix. This routes the information from WIFF to the desired head. WIFF varies as the bits are shifted serially from the Stack-up Register which receives eight bit characters in parallel on the Write Lines (WLnL's) from Control.

DISK WRITE DRIVER

The Disk Write Driver package is made up of two identical current control circuits operating in parallel and four identical Write Driver circuits operating independently. These Write Drivers are two identical halves operating 180^{o} out of phase. Refer to schematic in Field Test & Reference Documents.

Figure III-1 is a simplified drawing of one section of the Disk Write Driver Card.

The output of only one "and" circuit can be true at any one time turning on the associated transistor. This drops the base of the Driver transistor near ground turning it on and switching write current to the head.

The amount of current supplied is determined by the current regulators Q1 and Q2. The base voltage of these transistors is maintained at -15V by the 9V Zener diodes CR23A and CR23E.

READ GROUP SELECT

The Read Group Select package is made up of four identical switching circuits whose purpose is to allow a read signal from only one of the four "selected" heads to reach the information read amplifier.

Circuit Detail

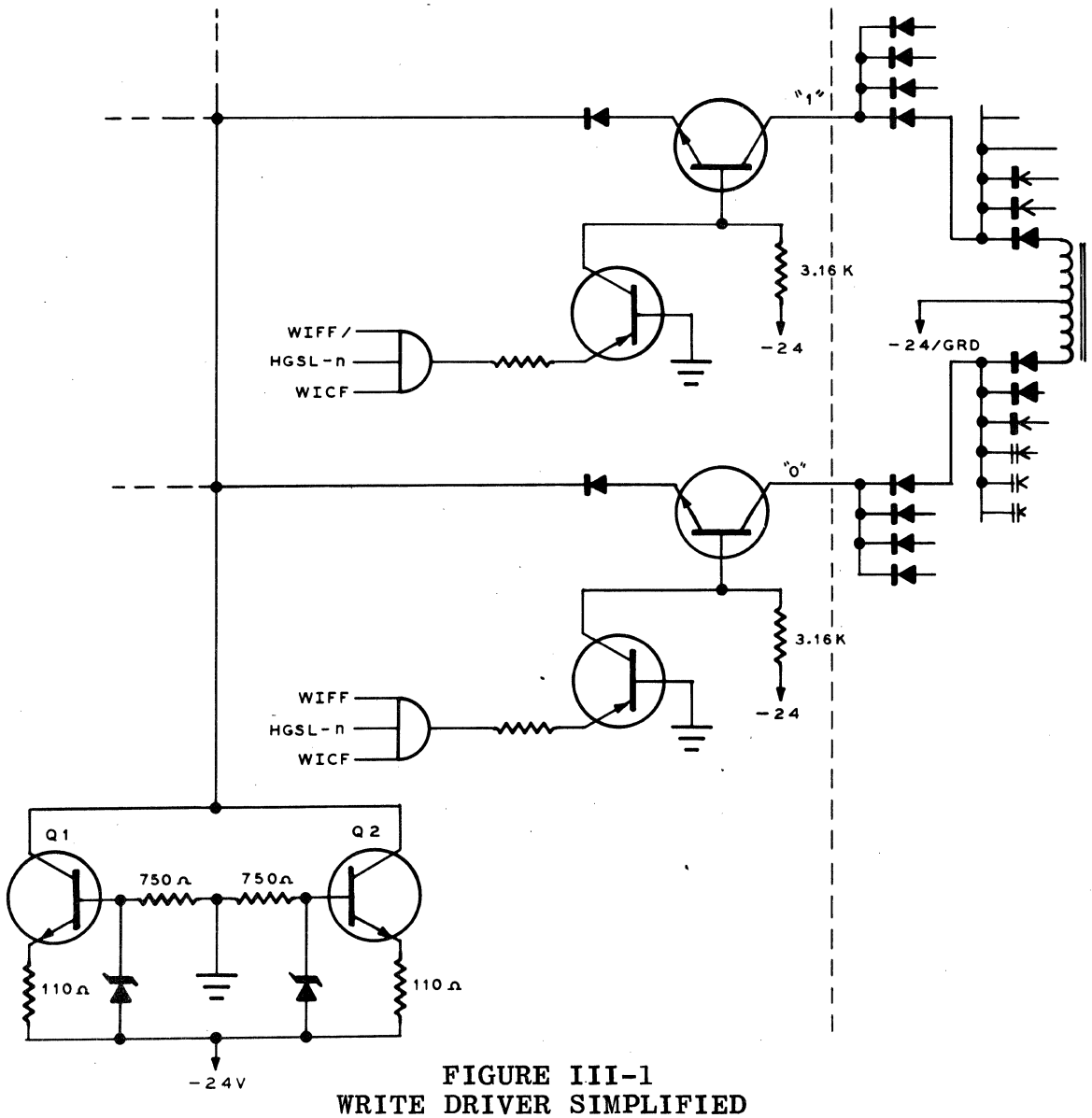


FIGURE III-1
WRITE DRIVER SIMPLIFIED

Refer to schematic in Field Test & Reference Documents.

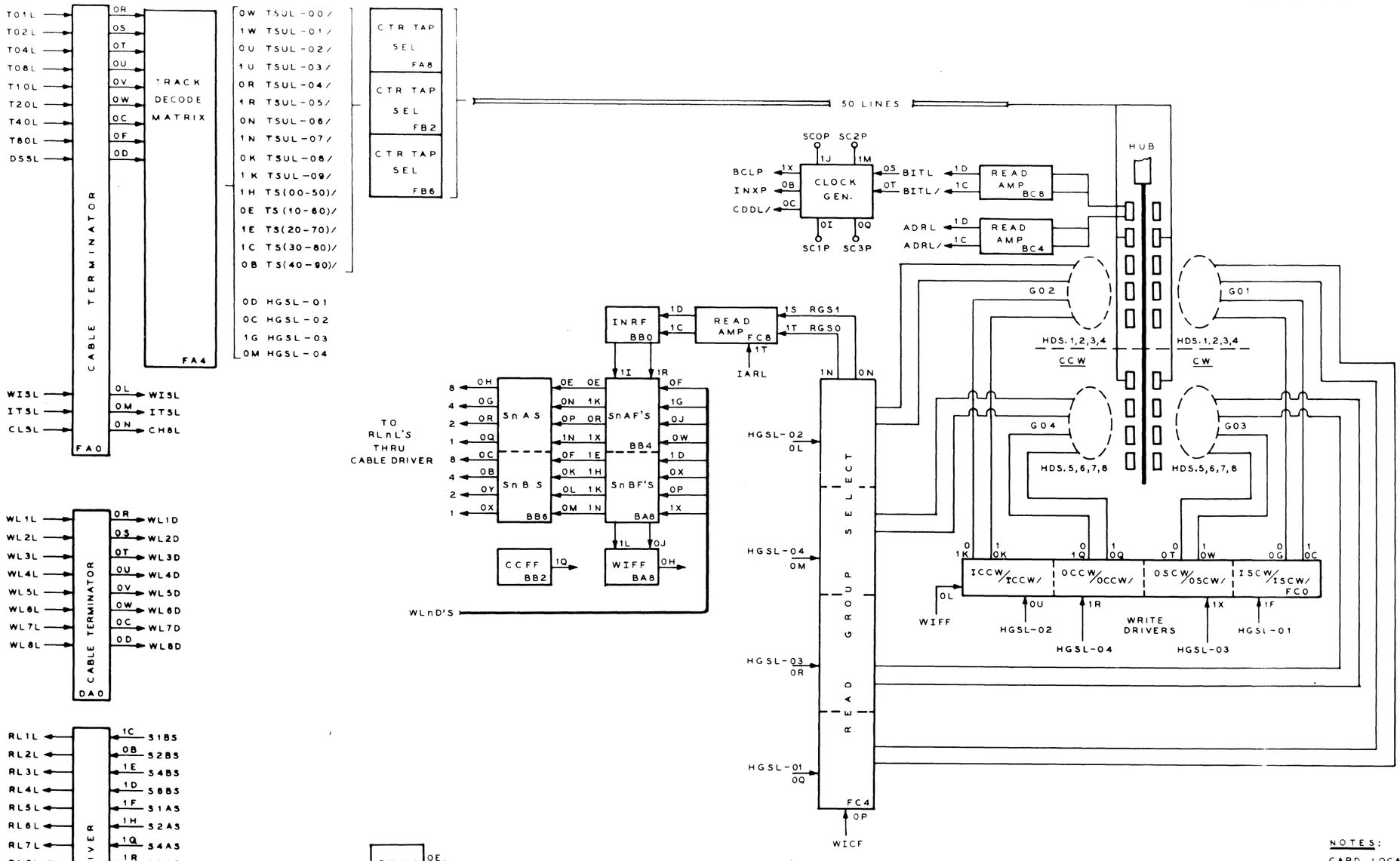
Four head center taps are grounded by any one Center Tap Select Line, each being in a different head group. The head group desired is determined from the decoding of tracks (see Track Decode Matrix) and represented by HGSL-01, HGSL-02, HGSL-03 and HGSL-04.

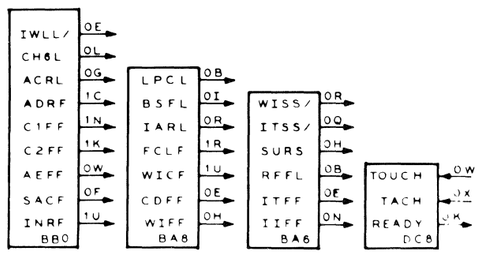
When one HGSL line is true, as for example HGSL-01, and a Read operation is in progress, Q3 turns off turning Q4 on. This applies a voltage to the junction of R14D and R15D forward biasing the associated head diodes and CR28E and CR29E allowing the Read Signal to appear at the package outputs RGS1 and RGS0.

HEAD SELECTION

Each Center Tap Select Line picks up one head (out of 50) in each head group, selecting four (out of 200) heads. The selection of one of these four heads is accomplished by actuating one of four Read Group

Circuit Detail





NOTES:

CARD LOCATIONS SHOULD BE PROCEEDED BY AA
EX. BC0 IS ACTUALLY AABC0
PIN LOCATIONS LISTED DO NOT INCLUDE CARD LOCATION
EX. ID ON BC8 IS ACTUALLY AABC8-9D

FIGURE III-2

BLOCK SCHEMATIC

Selects or one of four Write Drivers. Refer to schematic in Field Test and Reference Documents.

The current paths for reading and writing can be seen on the simplified circuit in Figure III-3.

With the Clock Head Center Taps tied to ground and the 1.3K, 4.2K divider resulting in a tendancy toward a -6V level, the Clock Head diodes are forward biased resulting in a constant reading of clocks.

In the unselected state, the Information Head Center Taps are returned to -24 thru 17.8K back-biasing all the diodes. The input to the Information Read Amplifier is clamped at +.3V. In the selected state, the Center Tap of four heads are returned to ground. The read diodes are still back-biased thru the 1.3K and 46.4K to +4.5 until one of the Read Group selects supplies a -14V level.

In the Write operation the read diodes are back-biased. The write current is supplied from the -24V thru the write current control, the Write Drivers, the Write Diodes, the Head diodes and the head winding to ground. This is explained further under Disk Write Driver.

CLOCK GENERATOR

The Clock Generator Package, the schematic included in Field Test & Reference Documents, has three outputs; BCLP's, CDDL1 and INXP. Most of the circuitry is devoted to the generation of BCLP's. This is accomplished by taking the BITL and BITL/ levels and developing four equal pulses; SC0P, SC1P, SC2P and SC3P. Refer to Timing Diagram, Figure III-4. These are then fed to four flip-flops (SnFF's) tied together so as to latch in a configuration incidating coincidence between INRF and SCnP. The output of these flip-flops are then ANDED with SCnP's so as to gate the second pulse set after coincidence was achieved. For Example: The first INRF (Ø bit) after address coincidence of a Read operation produces a true output at CAG-001. If this true level is coincident with SC2P, SCFF will be set forcing CAG-001 false preventing any further change to SnFF's.

The true output of S2FF is ANDED with SC0P to produce BCLP's. The gates for SC1P, SC2P and SC3P are all held false by the off state of S0FF, S1FF and S3FF.

This set of pulses is then used throughout the read-of-one segment. A reset of the SnFF's occurs between segments and a new latchup is accomplished during the reading of the next Ø bit.

During Write and Address Read, the SnFF's are clear and BCLP's are formed from SC0P's

The remainder of the circuitry is devoted to generation of CDDL/ and INXP's. As long as SC0P's are coming at BITL rate, Q10 is following, Q9 is off, producing CDDL/, Q02 is off, and Q11 is on producing a ground at CDDM and INXP. At each SC0P, Q10 turns on and discharges C8B preventing the turn on of Q9 and everything else remains static. When SC0P's cease, as in dead space, C8B charges up sufficiently to turn on Q9, producing CDDL and C2 turns on, grounding C24A. Drive to Q11 is removed while C24A charges up thru R22 turning off for approximately 600 nanoseconds, producing INXP.

Circuit Detail

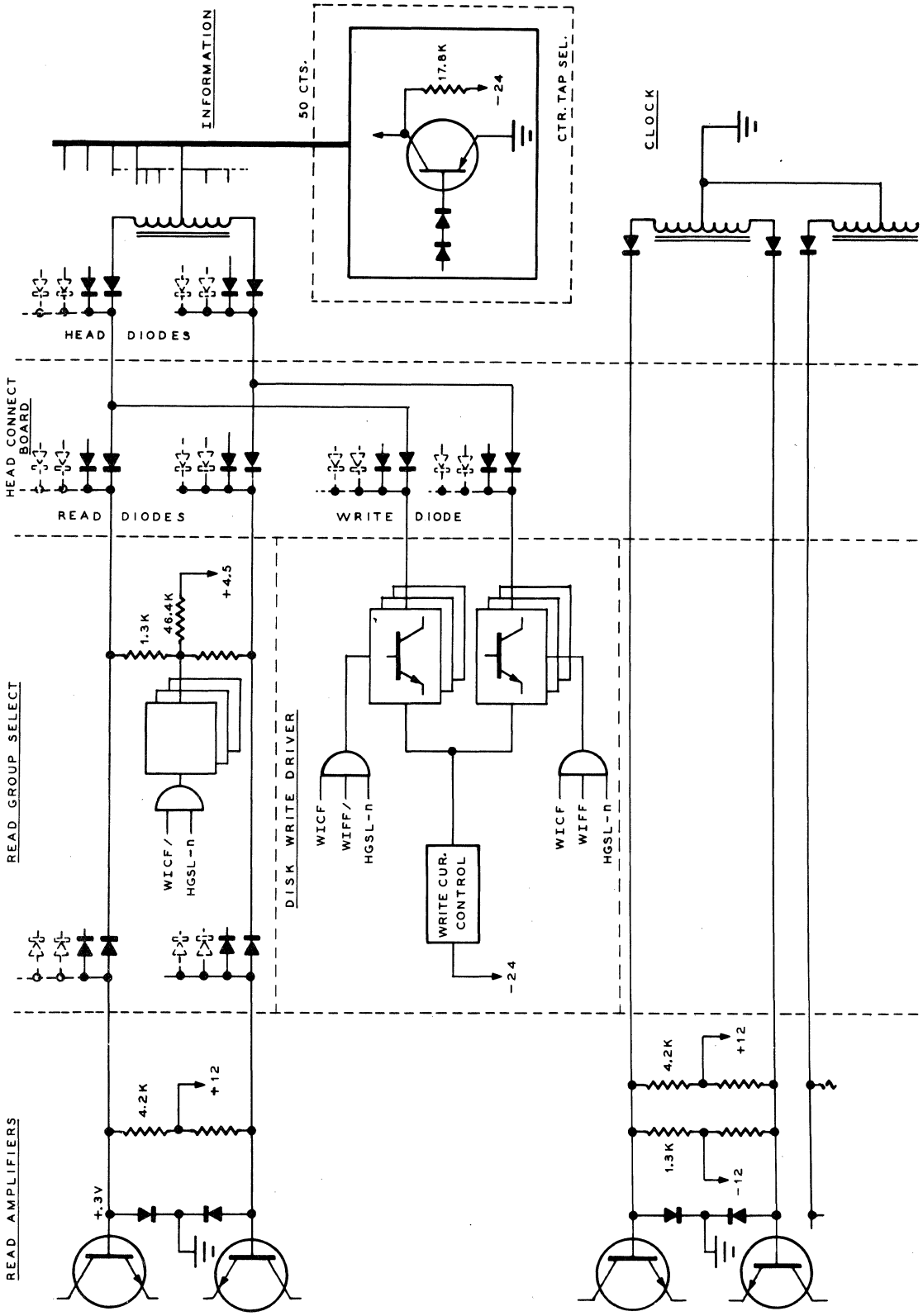


FIGURE III-3
READ/WRITE SIMPLIFIED

Circuit Detail

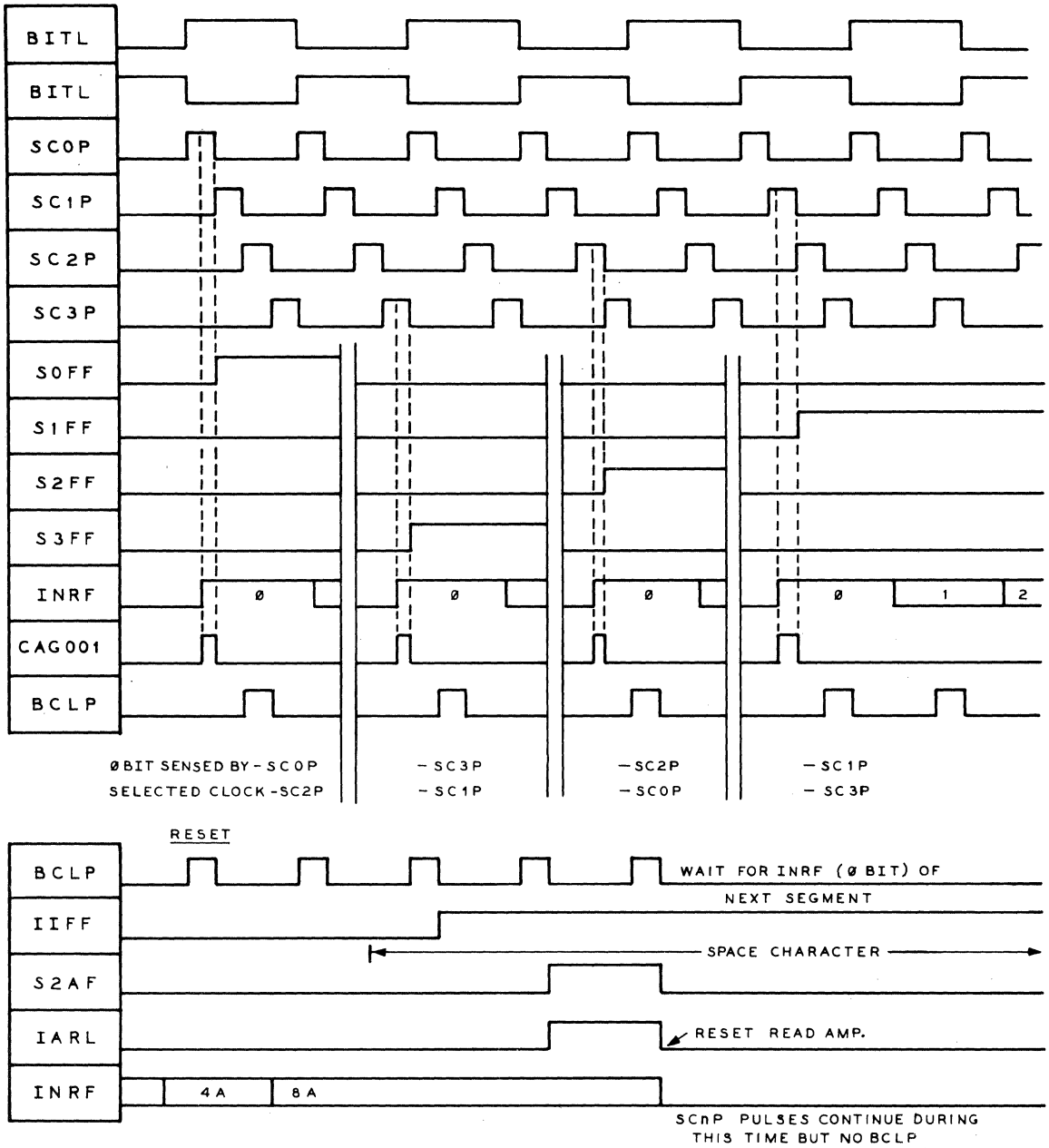


FIGURE III-4
FOUR PHASE CLOCK TIMING

Circuit Detail

Refer to Figure III-5.

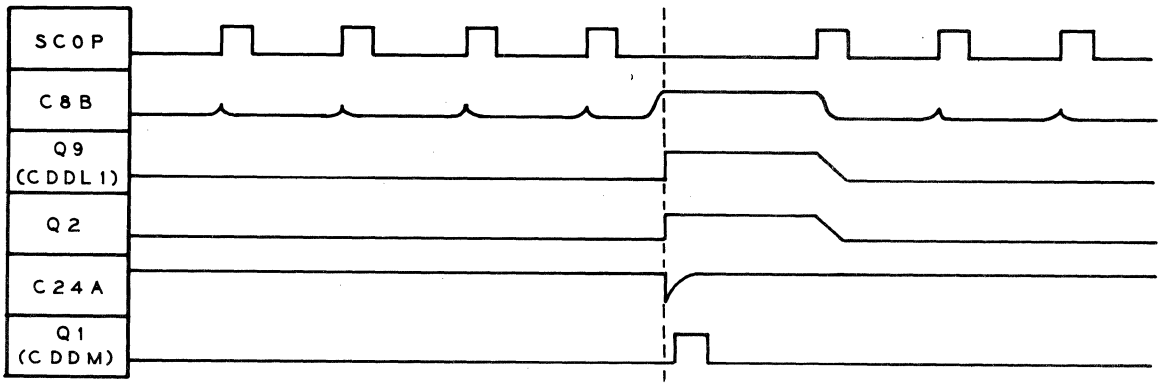


FIGURE III-5
DEADSPACE TIMING

TOUCH & TACH

The Touch and Tach package is comprised of four basic circuits; the Ready Driver, the Air Solenoid Driver, the Tach Circuit and the Touch Circuit. Refer to Field Test & Reference Documents for schematic.

The Ready Driver, (Q12) when on, supplies a ground to turn on the Not Ready indicator. When the input is true (SURL) Q12 is held off.

The Air Solenoid is picked when Q11 is on supplying the ground path provided other conditions are met. (Fly/Retract switch in Fly position and reserve pressure not less than 30 PSI) This is accomplished by the off state of Q10 and the on state of Q9, Q5 and Q4. Q4 can be turned off by either the Tach circuit or the Touch circuit.

The Touch circuit in its normal state of no touch has Q6 on and Q7 and Q8 off. The base of Q6 sets at about +1V providing a voltage source to the Touch pins. When a Touch occurs, the base of Q6 goes to ground, Q6 turns off and Q7 turns on. Q8 turns on, latching the circuit in this condition thru R31D. Reset is accomplished by temporarily grounding the collector of Q6.

The Tach circuit amplifies the negative output of the variable reluctanct pickup thru Q1. Q2 turns on for the duration of each negative pulse, partially discharging C29D which recovers at a rate dependent upon the setting of R1. As long as C29D remains sufficiently charged, the positive potential on the emitter of the Unijunction Transistor (Q3) keeps it turned on, discharging C31C and holding Q4 off.

When the reluctance pickup pulses come frequently enough to keep C29D discharged, the UJT (Q3) is cut off. This allows C31C to charge up providing a positive voltage to the emitter of Q4, turning it on.

Adjustments

ELECTRICAL

✓ BIT CLOCK PREAMP

1. Scope settings

   Time Base - 5 MS/CM

   Sync - External positive on Tach pickup (ADC8X)

   Trace A - Monitor "BCLP" bit clock (ABC9L)

2. While displaying a complete revolution of the disk, adjust the lowest amplitude flux change to 2.5V O→P minimum for the Clock Signal Reference.

✓ ADDRESS PREAMP

1. Scope settings

   Time Base - 5 MS/CM

   Sync - External positive on Tach pickup (ADC8X)

   Trace A - Monitor Address Clock (ABC5L)

2. While displaying a complete revolution of the disk, adjust the highest amplitude flux change to the amplitude recorded on the maintenance information chart.

✓ INFORMATION PREAMP

1. Scope settings

   Time Base - 5 MS/CM

   Sync - External positive on Tach pickup (ADC8X)

   Trace A - Monitor "INRL" Information (AFC9L)

2. Write 7's at the highest amplitude address as specified by the maintenance information chart supplied with the unit.

3. Select the high amplitude reference address as reflected on the maintenance information chart.

4. While displaying a complete revolution of the disk, adjust the highest amplitude flux change to the level recorded for the Information Signal Reference on the maintenance information chart.

✓ FOUR PHASE CLOCK GENERATOR

1. Scope settings

   Time Base - .1μs/CM

   Sync - ~~External positive on "BCLP" (ABC9L)~~ Internal on SCOP

   Trace A - Monitor "SCOP" (ABC1J)

   Trace B - Monitor "SC3P" (ABC0Q)

   Mode - Add

2. Using the pot located on the Clock Generator Card, adjust the SC3P pulse so that ~~the lowest point of~~ the "dip" between the second set SC3P and SCOP pulses ~~reach the baseline~~ is mid-sine wave. Refer to Figure IV-1. ~~When adjusted this way, the first set of pulses will have a less pronounced "dip" than the second set.~~

Adjustments

FIGURE IV-1
FOUR PHASE CLOCK GENERATOR

Note: The pulse width of each phase of the clock generator should be approximately 100 nanoseconds at the +1 volt level.

TACHOMETER ADJUSTMENT

1. Scope settings

   Trace A - Monitor Tach pickup (ADC8X)

   Trace B - Monitor solenoid driver (ADC8G)

   Sync - Internal positive

   Time Base - 5 MS/CM

2. Cap air pressure system as defined under TOUCH CIRCUIT CHECK, Section V, Steps 1, 2, 3 and 4. This is a precautionary measure to allow the air solenoid to be picked and dropped without danger of a crash.

3. With all other switches in their normal positions, place the MOTOR/ON switch in the OFF position. At normal speed - 1770 RPM - the tach pulses will be recurring every 34 MS. As the disk speed drops, the time between tach pulses will increase. When this time reaches 36.5 MS (about 1660 RPM) ADC8G should drop to -24 volts dropping the air solenoid. Adjust if necessary using the pot on the Touch and Tach card at (ADC8).

4. When the tach adjustment has been checked and adjusted as required, reconnect the air pressure system and check the air pressure regulator as described in the mechanical adjustment section.

MECHANICAL

COMPRESSOR SWITCH

This switch (JAAC) is located on the air pressure manifold. Its function is to monitor the reserve air pressure portion of the manifold. There are two adjustments on this switch; one to control the point at which the compressor is turned on as the reserve pressure drops and one to stop the compressor when the maximum pressure has been reached. The following procedure should be used for these adjustments:

CAUTION

Be careful when making this adjustment due to the presence of 110 VAC near the adjustment screws.

1. Retract the heads and drop DC power.

2. Low pressure "cut in" - slowly reduce the reserve air pressure using the safety relief valve. When the pressure falls to 31 PSI +0 -1, the compressor should start. The "cut in" pressure is controlled 11/32" hex nut at the top of the switch assembly - Refer to Figure IV-2. The switch actuation point can be raised or lowered by increasing or decreasing the tension on the spring respectively.

3. The "cut out" adjustment is controlled by the phillips head screw which is recessed in the center of the assembly - Refer to Figure IV-2. This screw actually controls the range of pressure built up before the compressor is cut out. With the "cut in" set for 31 PSI, the range should vary between 13 to 22 PSI. The adjustment for the System Memory should be for a range of 17 PSI giving a "cut out" pressure of 48 PSI. Turning the screw in a clockwise direction will increase the "cut out" pressure without affecting the "cut in" pressure.

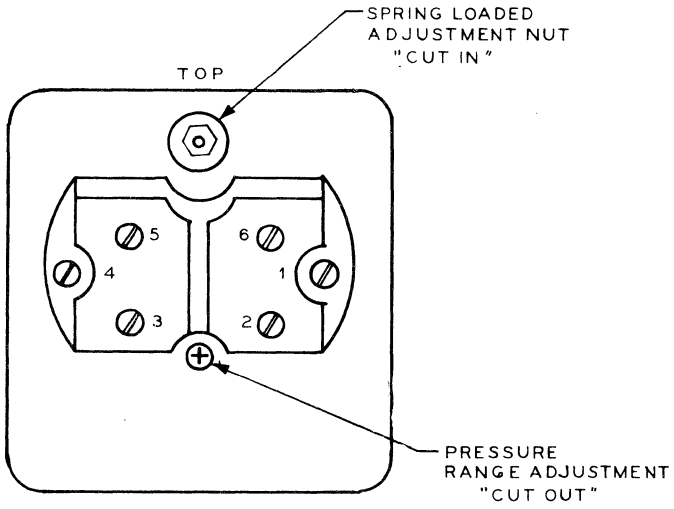


FIGURE IV-2
COMPRESSOR START SWITCH

AIR PRESSURE PRESENT SWITCH

This switch is also used to monitor the reserve air pressure level and will cause the heads to retract if for some reason the reserve level were to drop to 26 PSI or less before the compressor recycled to build the pressure back up again.

The switch actuating assembly consists of a spring loaded shaft which will hold the microswitch in its normally open position when the air pressure level behind the shaft is sufficient to overcome the spring. The spring tension is adjusted using the knurled collar located directly below the microswitch. To verify this adjustment, proceed as follows. Refer to Figure IV-3.

Adjustments

1. Scope settings

   Trace A - Monitor solenoid driver (ADC8G)

   Sync - Internal negative - auto trace

2. Place Head/Retract Switch in the RETRACT position.

3. Turn the air pressure regulator fully counter-clockwise.

4. Place Head/Retract Switch in the HEAD position.

5. Slowly bleed the pressure from the reserve pressure manifold. When the pressure reaches 26 PSI, the switch should close causing the solenoid driver output transistor to turn off and drop the solenoid.

6. When the air pressure present switch adjustment has been checked and adjusted if required, readjust the air pressure regulator as described below.

AIR PRESSURE READY SWITCH

This switch is a check on the air pressure regulator to insure that the pressure supplied to the heads does not fall below the specifield pressure required to fly the heads. The operation of this switch is the same as the air pressure present switch described below. The adjustments for this switch are as follows:

1. Scope setting

   Trace A - Monitor "HFSL" head fly switch (ADD45).

2. While observing the level "HFSL" decrease the pressure to the heads to less than 16 PSI. "HFSL" should drop from +4.5 volts to ground. Adjust the switch by turning the knurled collar clockwise to raise the point at which the microswitch will react and counter-clockwise to lower the pressure required to open or close the switch. Refer to Figure IV-3.

AIR PRESSURE REGULATOR

The air pressure regulator is required to maintain the pressure within 2 PSI of the specified level as stated below. There is also a metered orifice installed in the body of the regulator eliminating the need for a separate flow control valve. The metered orifice will insure that it takes approximately seven seconds to apply full pressure to the heads. The correct setting should be 16.0 +2 -0 PSI. To adjust a regulator equipped with a knurled locking collar, loosen the knurled locking collar at the base of the adjustment knob, and turn the knob clockwise to increase the pressure and counter-clockwise to decrease the pressure applied to the heads. To adjust a regulator equipped with a "push-pull" locking ring, pull the ring out, make the adjustment as described above, then push the ring in to lock the adjustment knob. Refer to Figure IV-3.

Adjustments

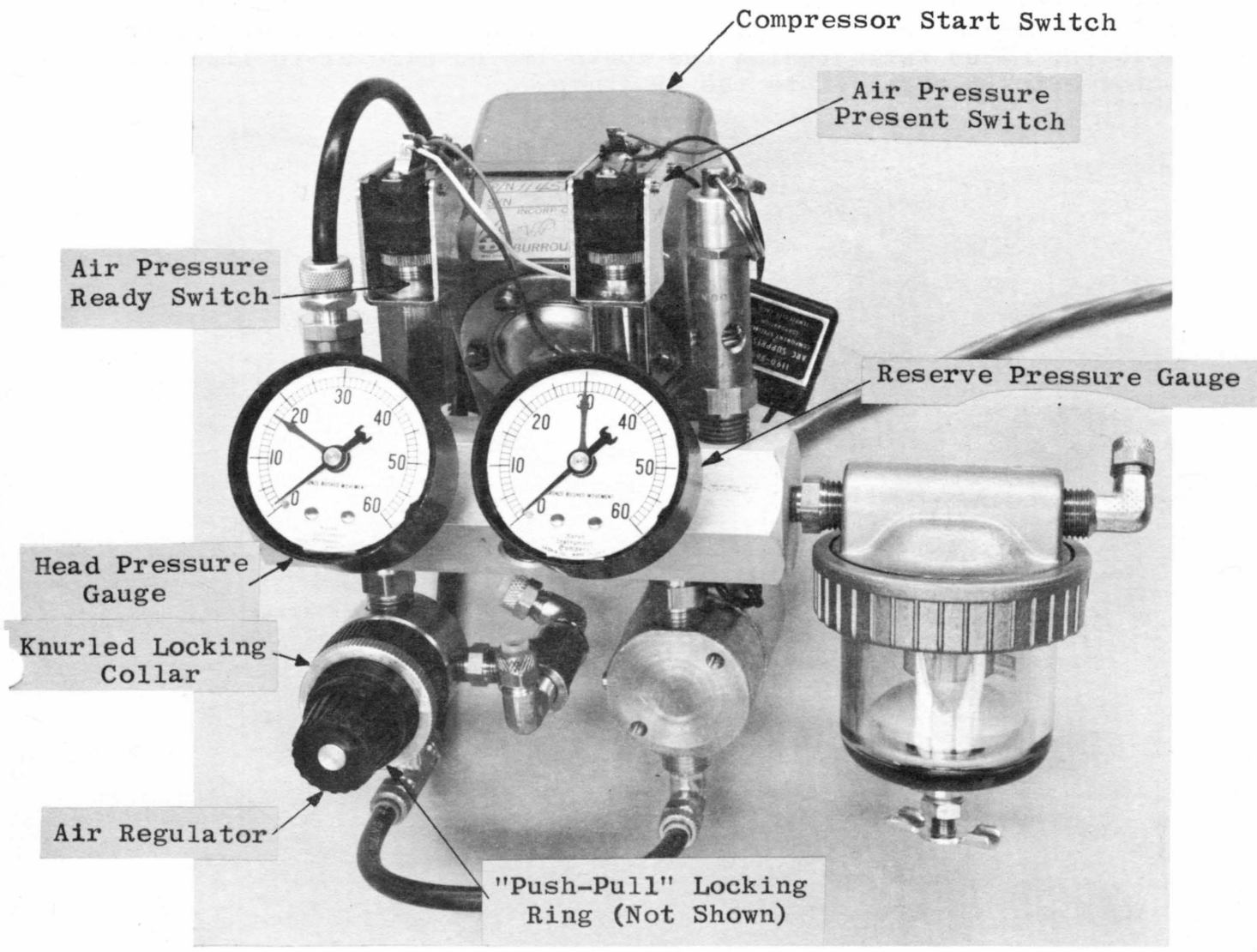


FIGURE IV-3
AIR MANIFOLD

BELT TENSION ADJUSTMENT

Correct belt tension can be verified in any one of the following methods:

1. Monitor the "Tach" signal at (ADC8X) to insure that the tach pulses are occurring every 34 MS (1725 RPM).
2. Turn the motor off and allow the disk to come to a complete stop. When the motor power is again applied, the disk should come up to speed smoothly without any sound of slippage or squealing.
3. With the disk stopped and the motor turned off, the application of 1-1/2 pounds of pressure should cause a deflection of about .3 inches.

The belt tension can be increased or decreased by loosening the

lock bolts which hold the motor bracket to the slotted adjustment bracket and moving the lower part of the motor bracket either forward or backward. When retightening the lockbolts be careful to line up the motor bracket parallel to the SM frame.

Maintenance Procedures

MONTHLY PREVENTATIVE MAINTENANCE

FILTER

There are two fiberglass disposable filters located in the left hand skin. They should be checked frequently and changed at least once a month or when necessary.

Since the filters are readily accessible, power need not be dropped during changing.

PRESSURE REGULATOR

The pressure regulator should be checked by monitoring the gauge monthly and each time the heads are actuated. (Allow five minutes for the regulators to stabilize after the heads have been actuated.)

If the pressure exceeds the +2 -0 tolerance, refer to Section IV for adjustment procedure.

INFORMATION AND CLOCK PRE-AMPS

Pre-amp settings must be checked on a monthly basis. Refer to Section IV for procedure when verifying these settings.

PURGE UNIT

If there is a Purge Unit on site, perform the following check monthly:

1. Remove both top hoses from the stop bracket. Leave the intake hose between the stops.
2. Disconnect the tube connected to the bottom part of the pressure gauge. (Tube from upper part of Purge Unit.)
3. Start the blower and read the gauge.
4. Remove the fiberglass pre-filters from the intakes and read the gauge again.
5. Change the pre-filters if the difference in readings is more than .4.

AIR FLOW CONTROL VALVE

The Air Flow Control Valve regulates the speed at which the heads travel from their retracted positions to their flying positions. It should be checked monthly. Refer to Section IV.

DRIVE SHAFT GROUND BRUSH

Check the ground brush mounted on the brush bracket for wear of the silver contacts. Replace as necessary with part number 1144 4239.

QUARTERLY PREVENTATIVE MAINTENANCE

BELTS

The disk drive belt should be checked quarterly to insure against excessive slippage or wear. Refer to Section IV for adjustment procedure.

PURGE UNIT

If there is a Purge Unit on site, perform the following check quarterly:

1. Remove both top hoses from the stop bracket. Leave the intake hose between the stops.
2. Remove the pre-filters.
3. Start the blower and read the gauge.
4. Change the absolute filter if the gauge reads more than 2.

5. First remove the two upper hoses.
6. The absolute filter is replaced with a Cambridge Absolute Filter, Model 1A-200-2 or equivalent.
7. The absolute filter must seat properly against the back-up plate gasket to insure dust-proof seating.
8. After installing a replacement filter, the upper (clean air side) part of the filter and the Purge Unit must be thoroughly cleaned by vacuuming and wiping with Freon TF and lint-free wipers.
9. After the initial cleaning, put pre-filters in position and run the Purge Unit for 72 hours.
10. Stop the Unit and wipe out the upper part by reaching through the openings.
11. Run the Unit another 10 minutes.
12. Replace the upper hoses.

SEMI-ANNUAL PREVENTATIVE MAINTENANCE

DISK ENCLOSURE PRESSURE

Check the air pressure inside each enclosure using the sensitive pressure gauges issued to each district. The pressure should be about .8 to 1.0 inch of water. If the pressure has fallen below .7 inch of water, replace the absolute filter.

ANNUAL PREVENTATIVE MAINTENANCE

FANS

The two cabinet exhaust fans located on the rear frame should be oiled annually using the following procedure:

Oil	EDD Part #1183 8596
Oil Injector	EDD Part #1183 8588

1. Remove air from oil injector by holding the needle up and pressing on the plunger.
2. Place the needle at the center of circle marked on the gold label.
3. Position the needle at an angle of approximately 45^{o} to the label surface and point it toward the center of the rubber cap. (These fans are lubed by inserting the oil injector needle through a self-sealing rubber cap located in the center of the motor hub.)
4. Pierce the label and the concealed self-sealing rubber cap located under the label.
5. Insert the needle approximately 1/4".
6. Depress the plunger of the oil injector approximately 1/16" to force the oil to flow. Rotating the fan will relieve air pressure and allow oil to flow into the oil chamber.

TOUCH PROCEDURE

When a Storage Module goes Not Ready as the result of a "touch", the field engineer should be aware of the potentially hazardous condition which exists.

DO NOT immediately attempt to re-fly the heads by hitting the Touch Reset button. If the "touch" had damaged the disk, more widespread damage will result.

The field engineer should proceed as follows: Using a trouble-light or flashlight, carefully check the disk faces for scratches.

If the disk face is scratched, the module must be returned to the factory for repair and a replacement ordered.

If the disk face is not scratched and there are no other visible signs of damage, proceed as follows: Reduce the pressure regulator by three turns counter-clockwise. Depress the Touch Reset button and fly the heads. Adjust the regulator to normal setting. If a "touch" occurs, one of the heads can be assumed to be flying incorrectly. The module must be shut down and, using a Purge Unit, the disk enclosure should be opened and the heads examined.

If the regulator is restored to normal without another "touch" occurring, the original "touch" possible was caused by a small dirt particle which did not scratch the disk or noise on the touch circuit. Normal operation may be resumed, keeping a check for pressure regulator drift.

INSTRUCTIONS FOR REPAIRS WITHIN THE DISK ENCLOSURE

REMOVAL AND REPLACEMENT OF A HEAD (Refer to Figure V-6)

CAUTION

Before proceeding with the head replacement, switch adjacent head plugs to verify that repair will be made on the correct head assembly. Since all head plugs are accessible, every attempt should be made to utilize spare heads, conditions permitting.

Removal Procedure

1. Prepare the Purge Unit for use. The two tubes at the top of the Purge Unit blow filtered air out. The single tube at the bottom is an intake to the absolute filter. Remove the output tubes from the plates on which they rest and start the Purge Unit. This will blow filtered air through the output tubes to clean them. Run the Purge Unit for at least 30 minutes.
2. Move the module to a room/area where there is a minimum or no air movement.
3. Attach the hose to the vacuum cleaner for normal cleaning and carefully clean the disk enclosure, window and head casting.
4. Stop the Purge Unit after it has run 30 minutes. Do not subject the Purge Unit to any rough handling after purging.
5. Remove the purge port plate and the window from the left hand side of the disk enclosure.
6. Use Freon TF and a lint-free wiper to clean the exposed flanges of the purge ports and the flanges of the purge tubes. Mount the purge adapter, part number 1147 4061.
7. Attach both output tubes from the Purge Unit to the purge ports and start the Purge Unit.
8. Unlatch and remove the two cable connectors from the Head Distribution Board. The head casting may now be removed from the Unit.
9. To remove the head assembly from the support casting, perform the following steps in sequence:
   a. Remove the screw holding the head assembly bracket.
   b. Remove the nut from the mounting stud bolt.
   c. Grasp the head assembly bracket at the two side alignment studs. USE NO TOOLS. Carefully pull the head assembly away

from the support casting. Push cable grommet out from the head side of casting and retain same.

Replacement Procedure

1. If more than one head was removed, the heads must be replaced in reverse sequence to their order of removal.
2. Carefully clean the new replacement head with Freon TF and a lint-free wiper. Extreme care must be taken in the following:
   a. Fragile connector
   b. Fragile leads
   c. Mounting bracket must not be bent
   d. Head is bonded to gimbal spring - do not stress
   e. Head flying face must not be scratched
3. Place connector through casting, replacing grommet from head side of casting resealing with RTV 108.
4. Grasp the head assembly by the two side alignment studs and carefully insert them fully in the guide slots. NO FORCE IS REQUIRED.
5. Very carefully check to insure the head is fully seated before replacing the mounting stud nut.

CAUTION

If the alignment studs are not fully inserted and the head not correctly seated, the head will not fly properly and a crash will result.

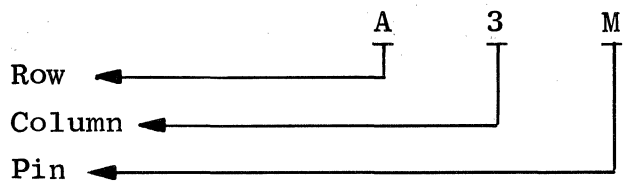
6. Place the mounting stud nut and use a torque wrench to tighten it to four inch-lbs. Check again for correct seating of the head.
7. Place the pan head screw in the arm of the mounting bracket. Note that this will place tension on the arm. This is normal. Use a torque wrench to tighten the screw to 13 inch-lbs.
8. Replug the head assembly cable connector. The large and small guide pins determine the orientation. Great care must be exercised to insure that the delicate wire form contact pins are not bent causing a short to an adjacent pin.
9. Use Freon TF and a lint-free wiper to wipe down the heads and other areas that have been contaminated by handling. Place the head support assembly in position and loosely secure. Remove one of the positive blowers from the window and secure it back to the Purge Unit. With positive air still blowing into the cavity, tighten head casting. Connect purger intake hose to the window and purge the Unit statically for approximately ten minutes. With purger still connected, bring disk to speed with heads retracted and continue purge for another ten minutes. With maintenance switch, alternately fly and retract heads for another ten minutes. This is to insure any loose particles to be removed from the disk enclosure. Retract heads and first remove the exhaust hose and return to Purge Unit. Using Freon TA, clean window surfaces.
10. Replace the window assembly by inserting all the holding screws loosely with the Purge Unit still blowing.
11. When all the window assembly screws have been replaced, tighten them evenly.
12. Turn off the Purge Unit.
13. Remove the hose from the purge port and secure it on the bracket.
14. Wipe the purge port flange and re-secure same.

ETCHED CARDS

Card Pin Etching is placed on both sides of the Card. Refer to Figure V-1. Each Card has 25 connections on each side. Therefore, it is possible to have 50 connections on the backplane wiring, two vertical columns of 25 each. The contacts on the Card are lettered A through Z with O being omitted. The Card sides are either EVEN or ODD; but in locating the Card, the EVEN side is referenced. Each Card has six positions allotted for either Voltage or Ground. 0A and 1A are tied to +4.5V, 1B and 1Y are Ground and 0Z and 1Z to -2V. The remaining 44 positions are used for signals to and from the Card.

Each Card can hold up to 32 Chips. They are mounted eight to a column with four columns. The columns are designated zero (0) through three (3) with 3 being nearest the connector etching. The rows are in alphabetical order A through H.

Each Chip contains 14 Pins which serve as connections to and from the integrated circuits within the Chip to the Etched Card. There are seven Pins on each side of the Chip. One side is A through G and the other side is lettered H through P with I and O omitted. Pin E is Ground, Pin M is +4.5V and Pin L is -2V. The following format is used to locate a specific Chip and Pin within that Chip:



Therefore, for location A3M, this Chip would be in the upper right hand corner of the Card near the Connector Etching.

CTUL INTEGRATED CIRCUITS

Figure V-2 shows the various types of Chips used in the System.

As indicated, the FA-0 (Flip-flop) has one element per Chip. The BA-0/1 and IA-0/1 (Buffer and Inverter) have two per chip numbered zero and one. The remaining six types of gate Chips can have up to four gates per Chip, depending on the gate configuration required, which are numbered 0 to 3.

HEAD CASTINGS - OUTSIDE

Figure V-3 shows the layout of the Head Castings viewed from the outside. The cable grommets are numbered with the eight information head numbers and "C" for the clock head.

HEAD CASTINGS - INSIDE

Figure V-4 shows the layout of the Heads on the casting viewed from inside. Should it be necessary to replace a head, carefully note the routing of the head cable.

Maintenance Procedures

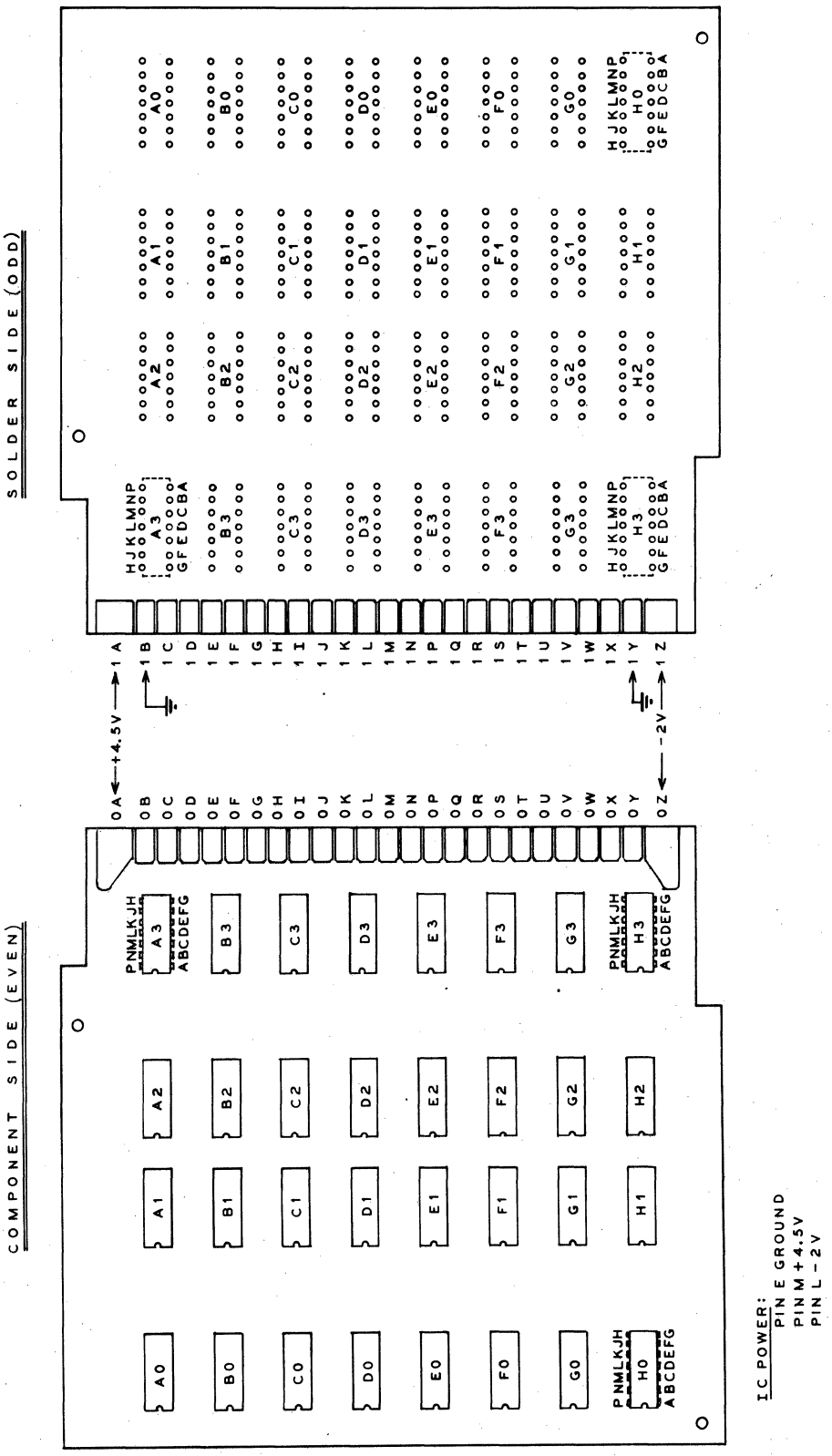


FIGURE V-1
ETCHED CARDS

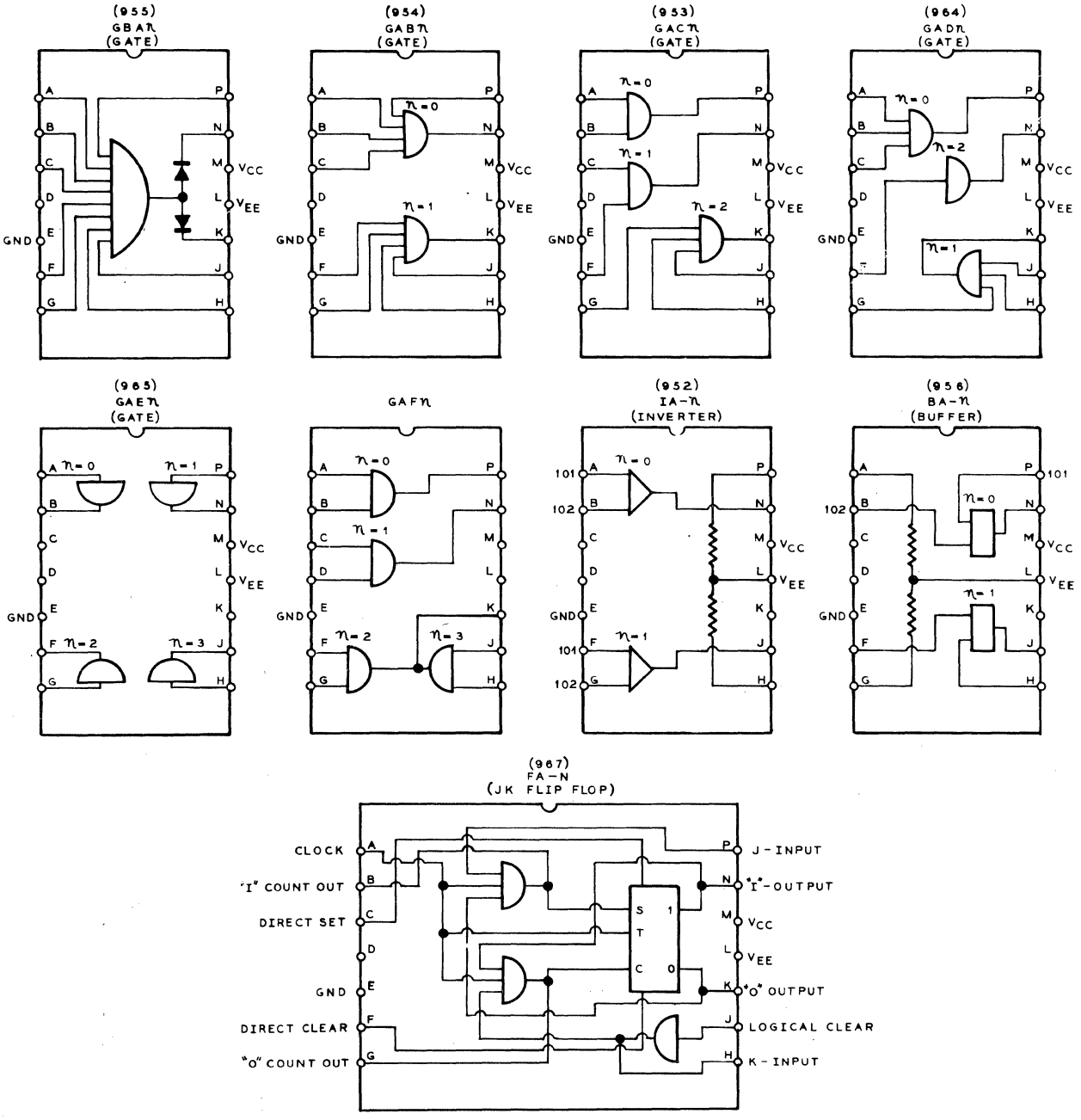


FIGURE V-2
CTUL INTEGRATED CIRCUITS

COMPONENT LOCATIONS

Figure V-5 shows the cards locations in the System Memory by row and column.

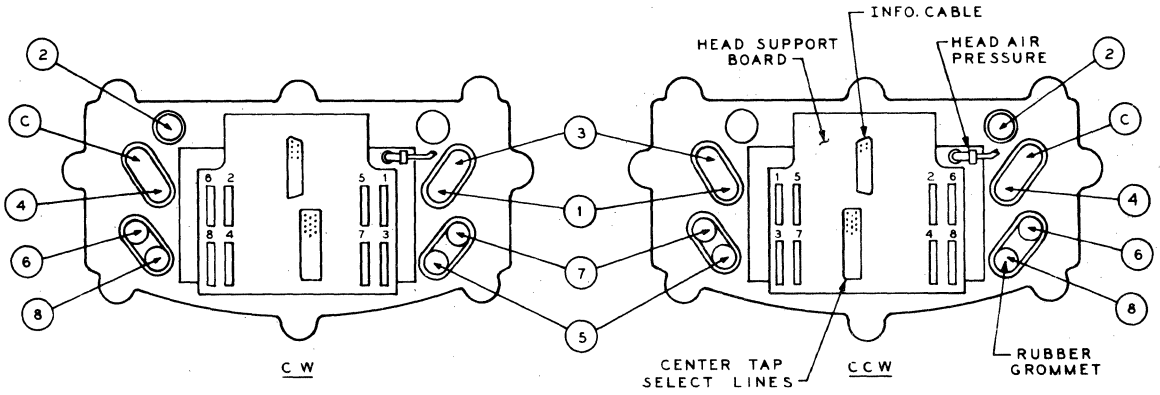


FIGURE V-3
HEAD CASTINGS - OUTSIDE

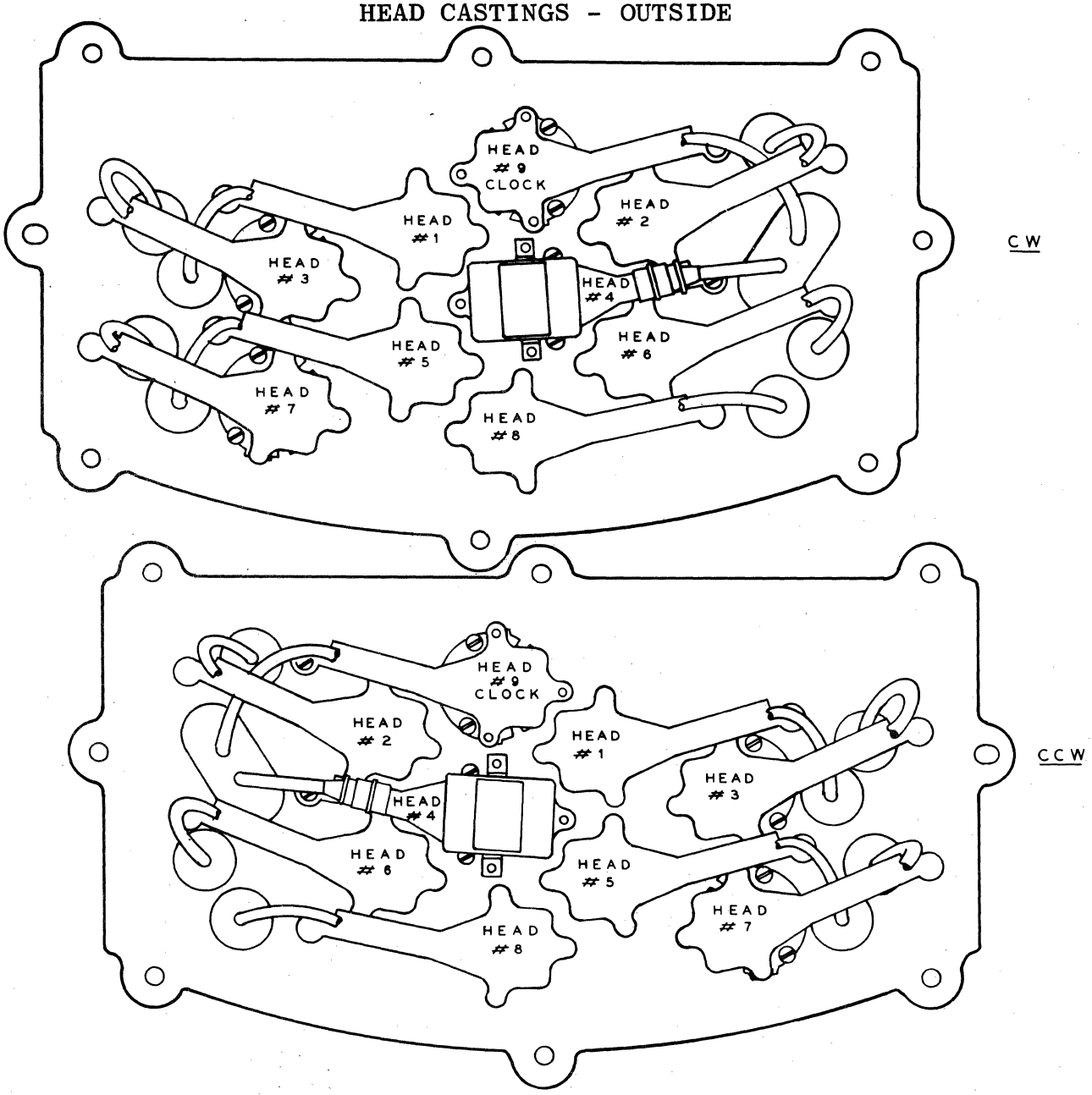


FIGURE V-4
HEAD CASTINGS - INSIDE

Maintenance Procedures

A	D 8	D 6	D 4	D 2	D 0	C 8	C 6	C 4	C 2	C 0	B 8	B 6	B 4	B 2	B 0	A 8	A 6	A 4	A 2	A 0	A
B			CLOCK CABLE CARD			BIT RD. AMP 1125 1626		ADD RD. AMP 1125 1626		CLOCK GEN. 1123 8086		REG. BUFF. & DR. 1123 7419	SHIFT REG. #2 1123 7500	SHIFT REG. #1 1123 7476	ADD CONTROL FF 1123 8185	SHIFT CONT. & WRFF 1123 8045	S. M. CONTROL 1123 7989			CABLE DR. 1148 3559	B
C	D 8	D 6	D 4	D 2	D 0	C 8	C 6	C 4	C 2	C 0	B 8	B 6	B 4	B 2	B 0	A 8	A 6	A 4	A 2	A 0	C
D			POWER SUPP & TACH CABLE			TOUCH & TACH 1145 1150														CABLE TERM 1148 3518	D
E	D 8	D 6	D 4	D 2	D 0	C 8	C 6	C 4	C 2	C 0	B 8	B 6	B 4	B 2	B 0	A 8	A 6	A 4	A 2	A 0	E
F	HRWL CABLE	C.T. CABLE CCW	C.T. CABLE CW			INFO. RD. AMP 1125 1626		RD. GROUP SEL. 1125 1675		WRITE DRIVER 1123 8128		C.T. SELECT 1123 8466		C.T. SELECT 1123 8466		C.T. SELECT 1123 8466		TRACK DEC. MTX. 1123 9183		CABLE TERM 1148 3518	F

FIGURE V-5
COMPONENT LOCATIONS

Maintenance Procedures

CONTROL ADDRESS

1	9	9	0	0	⊠

DSSD | TRACK

TRACK EVEN	TRACK ODD	DSSD	HEAD POSITION	TYPE	SPARE CORE POSITION #4
00⇒22		0	2	LCW	YES
	01⇒25	0	1	UCW	
24⇒48		0	4	LCW	
	27⇒49	0	3	UCW	YES
50⇒72		0	2	LCCW	YES
	51⇒75	0	1	UCCW	
74⇒98		0	4	LCCW	
	77⇒99	0	3	UCCW	YES
00⇒22		1	6	LCW	YES
	01⇒25	1	5	UCW	
24⇒48		1	8	LCW	
	27⇒49	1	7	UCW	YES
50⇒72		1	6	LCCW	YES
	51⇒75	1	5	UCCW	
74⇒98		1	8	LCCW	
	77⇒99	1	7	UCCW	YES

HEAD IDENTIFICATION CHART

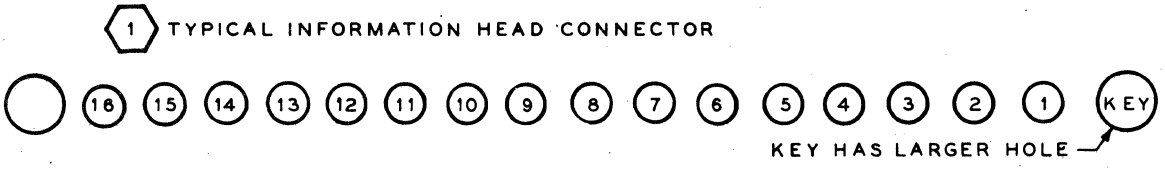


FIGURE V-6
HEAD LOCATING CHART

Installation Procedures

INSTALLATION

After positioning the System Memory Unit and verifying that the A.C. power is correct, place the head/retract switch in the retract position. Apply A.C. and D.C. power to the Unit. Allow a one hour warm-up period. Verify the following voltages at there respective test points:

-24 Volts	AAFC0I, AAFB6V, GAAE1, KAB10
+12 Volts	AABC9K, AADC8Q, AAFC9K
-12 Volts	AABC4J, AADC8D, AAFB6G
+4.5 Volts	AAFC0Y, AADD4V, AABA0R, KABA2

Fly the heads after the time lapse noting time necessary to bring heads into position. Monitor for proper air pressure indications, adjust if necessary and run appropriate test routines.