



SYSTEMS DESIGN SPECIFICATION

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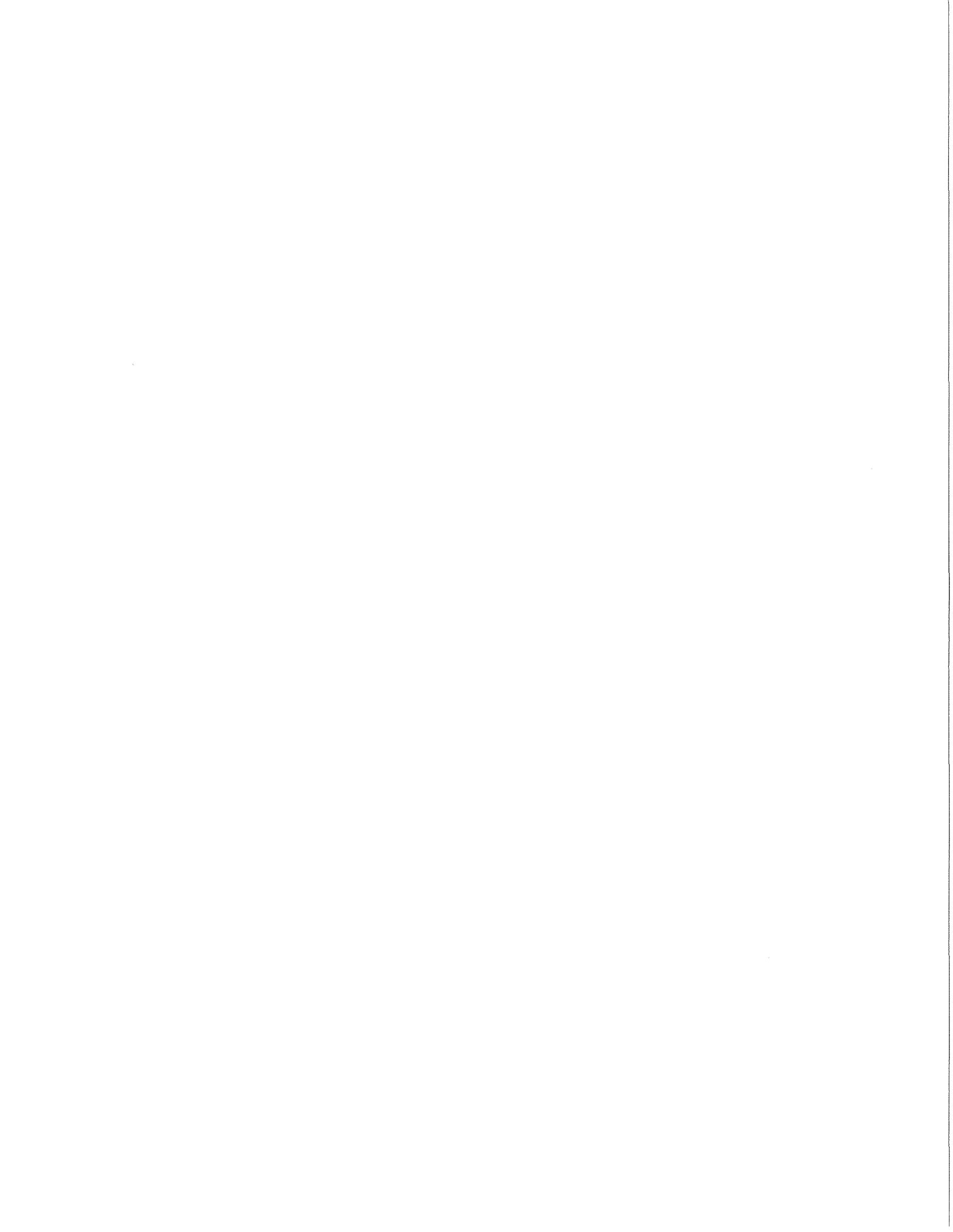
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RELATED DOCUMENTS

1993 5279	V500 Architecture Specification
1993 5204	V500 Execute Module Specification
1993 5212	V500 Fetch Module Specification
1993 5220	V500 Memory Control and Cache Module Specification
1993 5238	V500 Memory Module Specification
1993 5253	V500 I/O Subsystem Specification
1993 5295	V500 System Maintenance Controller Specification
1993 5337	Fault Detection Design Recommendations
1937 1045	OMEGA Processor Family Specification
3398 2091	STG Functional Specification for Remote Support
3398 2075	Dialog Block Protocol for Remote Support
3398 2067	Message Block Protocol for Remote Support
3398 2059	Eight-bit Data Comm Protocol for Remote Support
-	V500 Design Guidelines
-	V500 Diagnostic Test Plan
-	V500 Environmental Control Module Specification



1 FUNCTIONAL ATTRIBUTES

The functional attributes listed in this section define the major capabilities of the V500 Maintenance Subsystem.

The following terms will be used to indicate the major components of the Maintenance Subsystem throughout this document:

MAINTENANCE SUBSYSTEM All of the components of the Maintenance Subsystem, including those listed below.

MAINTENANCE PROCESSOR (MP) The component of the Maintenance Subsystem which performs high level control functions and provides the operator interface. The MP for the V500 Maintenance Subsystem is initially the B25 workstation. The MP will migrate to the Advanced Workstation (AWS) when it becomes available.

SYSTEM MAINTENANCE CONTROLLER (SMC) The component of the Maintenance Subsystem which provides a real time interface between the MP and processor modules in the same cabinet as the SMC. The SMC for the V500 Maintenance Subsystem is 80186 microprocessor based and resides in the processor backplane.

ENVIRONMENT CONTROL MODULE (ECM) Components of the Maintenance Subsystem which monitor and control system power and cooling. Two types of ECM are required, master and slave. The master module handles communication with the Maintenance Processor; each slave module controls a specific power subsystem (e.g. one power cabinet).

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-----1 FUNCTIONAL ATTRIBUTES (Continued)MAINTENANCE DISK(S)

Disk file unit(s) connected to the MP and used for storing all program and data files used by the Maintenance Subsystem. The primary disk unit for the V500 Maintenance Subsystem is the Winchester disk peripheral of the B25 or AWS. A minidisk unit is also provided, due to limited capacity of the Winchester disk, and as an initial boot and update path.

Note that the terms Maintenance Subsystem, and Maintenance Processor are not interchangeable.

1.1 OPERATOR INTERFACE

This category includes those functions that are required by system users (operators, software developers, etc), but not those that are required exclusively for field maintenance or hardware debug.

- a. Operator Display Terminal (ODT). This is the primary means by which the Operating System (MCP) accepts keyboard input, and displays output messages. The V500 does not have a dedicated maintenance console; the Maintenance Processor performs a dual role as both the maintenance console and the ODT. These functions are performed concurrently.

The Maintenance Subsystem may also be configured with two MPs to meet system fault tolerance, or user, requirements. In this configuration only one MP acts as the Maintenance Subsystem controller (and also performs ODT functions), the other performs ODT functions only. If the controlling MP fails, the other MP will recognize the failure and take over it's functions.

When the system is configured with two MPs, one may be dedicated to maintenance functions only, while the other continues to function as the system ODT, thus facilitating on-line system maintenance.

- b. Operator Console. The Maintenance Subsystem supports the following operator control functions:
 - i. System Initialization
(See 1.1.1 for a more detailed breakdown of this function.)
 - ii. System Configuration Control
 - iii. Date and Time Clock. This clock maintains the current Date and Time, passing it to the MCP during a HALT/LOAD. After the system is halt/loaded, the MCP maintains it's own independent date and time clock.
 - iv. System Status Display

Simplicity of operation will be enhanced by the use of menu(s) for common operator control functions.

1.1 OPERATOR INTERFACE (Continued)

c. Programmer Console. The Maintenance Subsystem supports the following functions for software debug:

- i. Memory Access (Read, Write, and Clear system memory.)
- ii. Program State Access (OMEGA structure access will be supported).
- iii. Single Instruct
- iv. System Status Display
- v. Stop on OP, on Instruction Address, or on other conditions considered appropriate for the programmer environment.

As with the Operator Console functions, menus are used to enhance usability wherever this is appropriate.

1.1.1 SYSTEM INITIALIZATION AND CONFIGURATION

The V500 Maintenance Subsystem provides the means by which the operator brings up the system from power-off to the MCP running state. The procedures involved are quick and simple to execute. Standard initialization command sequences are pre-programmed to allow "single keystroke" HALT/LOAD, etc., and menu operation is emphasized.

The following functions are provided:

1. Control Store LOAD.
2. Control Store VERIFY.
3. Set Options:
 - a. MCP unit
 - b. ALT unit
 - c. Memory size
 - d. Memory configuration
- #4. Load ODT DLP firmware (Uniline or equivalent).
- #5. Load Disk Controller firmware.
6. Load Bootstrap for MCP loading.
7. Load Bootstrap for ALT loading.
8. Set MP DATE and TIME.
- #9. Memory dump to tape (via Control state program).
- #10. Add/Subtract processors from the active list.
11. Single Keystroke System boot.

Functions or features marked with a pound sign (#) will not be included in the first release. Later availability is not yet scheduled.

1.2 MAINTENANCE INTERFACE

This category includes those functions that are required for hardware maintenance or debug only. Two distinct levels of maintenance are supported. The first level assumes minimal system knowledge, and is geared to fault isolation to the FRU level, with as little operator interaction as possible. This interface is largely menu driven. The second level (which includes debug) is intended for more highly trained personnel seeking to pinpoint functional failures, and keyword commands are utilized for control in addition to menus.

1.2.1 FIELD MAINTENANCE - PRIMARY LEVEL

Primary Level Field Maintenance is concerned with physical level fault isolation, and requires a minimal operator skill level. Features provided for this level of maintenance are designed to facilitate rapid isolation of a fault to a Field Replaceable Unit (FRU). The FRU is normally a circuit board, mechanical component, or power module. Functional analysis of the problem is secondary to rapid isolation and replacement of a failing FRU.

Interfaces are provided within the Maintenance Subsystem, and between the Maintenance Subsystem and the Host System, which permit the implementation of diagnostics and other tests capable of isolating hardware problems to the FRU level with minimum operator interaction.

A software driven diagnostic flow is incorporated which permits primary fault isolation to be accomplished automatically (without operator interaction) when an error is detected.

Initial problem diagnosis in the field will most often be performed via a REMOTE link. For this reason, priority is given in the Maintenance Subsystem design to facilitate this process (See Sections 1.4 and 2.4). The automatic diagnostic process mentioned above will reduce the number of transactions required, via the REMOTE link, by performing primary fault diagnosis before the remote connection is made.

1.2.1 FIELD MAINTENANCE - PRIMARY LEVEL (Continued)

Specific capabilities include:

- a. Error detection logic within each system module (e.g. circuit card), which outputs a signal to the Maintenance Subsystem when an error occurs.
- b. Module self-tests are provided for the processor, and these are executed on power-up, as part of the diagnostic flow, and in response to a specific operator request.
- c. Central system diagnostic tests are resident on the maintenance disk and are automatically invoked on the occurrence of an irrecoverable error.
- #d. A SYSTEM TEST flow is provided, and is resident on the Maintenance Disk. Execution is initiated by a single console command. The flow verifies error free operation of all components required to Halt/Load the system (including the fact that a copy of the MCP is resident on the system disk), using a "bottom-up" diagnostic approach, selectively executing diagnostic tests. It is utilized when system status is uncertain.

Error messages from test routines include identification of the suspect physical modules, or guidance as to the means by which an accurate diagnosis may be made (e.g. what other tests should be executed).

e. TEST FUNCTIONS

Test Chain(s)

Test RAM(s)

Test Memory

Path Tests

Module Function (Microcoded) Tests

Control State IO and Processor Tests

MP-driven On-line IO Tests

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1.2.2 FIELD MAINTENANCE - SECONDARY LEVEL, AND DEBUG

Secondary Level Field Maintenance (second level support), and System Debug are concerned with functional level fault diagnosis, and assume a higher operator skill level than required for Primary Level Maintenance.

Tools provided for use at this level assume the user has a knowledge of the system architecture, and wants to isolate a problem beyond the FRU level.

Specific functions provided include:

a. PRIMITIVE CONTROL FUNCTIONS.

CLEAR : Clear all machine state
Clear selected modules
Clear a selected chain
Clear the SMC

CLOCK : Clock all modules
Clock a selected chain
Clock selected modules
Clock burst (chain or modules)

SET AND DISPLAY STATE :
All chain and RAM elements individually
Set pattern in any chain

b. MEMORY CONTROL FUNCTIONS

Clear all, or a part of memory to zero

Read and Write memory

Set all, or a part of memory to a pattern

1.2.2 FIELD MAINTENANCE - SECONDARY LEVEL, AND DEBUG (Continued)

c. SYSTEM CONTROL FUNCTIONS

Load and verify module control stores

Single Instruct

Single Clock

TERM/HALT

RUN/<SPCFY>

INIT/PA

Static and Dynamic Record

- d. STOP ON EVENT. Stop events will be specified as the V500 architecture becomes more clearly defined. The operator interface is via a menu similar to the Maintenance Panel on the B4900.

The stop logic compare and enable functions are implemented in the individual processor modules, via dedicated maintenance chains. Two interrupt lines to the SMC are provided from each processor. An option is available to permit modules to stop themselves when a stop condition occurs. If this option is not enabled, module and processor halts, in response to the occurrence of a stop event, will be under the control of the SMC.

1.2.3 MAINTENANCE PLAN

The architecture of the Maintenance Subsystem takes into consideration the need for a complete maintenance capability in all areas of the system hardware.

Internal errors detected within each processor card trigger the Maintenance Subsystem to perform a problem analysis and record procedure. If applicable, a recovery procedure is initiated. The error is logged, and the faulty card is indicated in the error report.

1.2.3 MAINTENANCE PLAN (Continued)

The result of the error analysis will be displayed on the maintenance console in a form indicating the nature of the error, and the name and location of the failing module or card. A failure history file is also maintained on the maintenance disk.

Performance-driven maintenance features include auto-diagnosis of hardware problems and automatic dial-up of the Remote Support Center. All maintenance functions and diagnostic capabilities are available remotely. Auto-answer is provided as an optional feature if it is required to support corporate remote support strategy.

Specific plans for the major subsystems are described in the following paragraphs.

a. MAINFRAME POWER and COOLING

The Maintenance Subsystem interfaces to the power and cooling modules through intelligent, self testing, Environmental Control Modules. These modules monitor and control power and cooling, and report their status on request, or automatically if an error occurs. In the case of a power module failure, the report from the ECM indicates the failing module.

The ECMs are designed to handle critical power problems independently of the Maintenance Subsystem if necessary to protect the system from damage.

If the ECM module itself fails, it is designed to fall into a "hard wired" control mode, in which power is locked into nominal and cannot be varied. If control is still not possible, power is automatically taken down. A clear signal is driven to the processor when a power-down is imminent.

The repair philosophy for the power and cooling subsystems is to replace the failing module.

b. MAINTENANCE SUBSYSTEM

The components of the Maintenance Subsystem utilize resident SELF TESTS as the primary means of fault isolation. The Self Tests execute automatically on Power Up and whenever requested by the operator.

1.2.3 MAINTENANCE PLAN (Continued)

They include a basic test of the maintenance disk(s).

The SMC incorporates a LED display panel (visible from the card frontplane) which provides an indication of its status, including the results of any self test failure. The SMC Self Test is executed as a low priority task during normal operation.

All ODT displayed error messages will contain a specific indication of which hardware component (FRU) is suspect.

More extensive, non-resident, tests for each of the Maintenance Subsystem components are stored on the maintenance disk, and may be executed under operator direction. Default execution of these tests may be initiated by the Maintenance Subsystem itself in the event that an internal error is detected and resident self tests complete without error.

c. PROCESSOR (including MEMORY and IOTs)

The designs of the central system modules include extensive error detection logic. This logic permits many problems to be diagnosed by the Maintenance Subsystem to the card or module level, based only on the location and type of error reported. When a processor error is detected, an extended processor result descriptor is written into system memory to alert the MCP to the occurrence of the problem, and if applicable, a recovery is attempted. It is anticipated that recovery will be possible for at least 60% of all transient processor errors (excluding memory storage boards, where the recovery rate is expected to be close to 100%). (At least 80% of all errors are expected to be transients).

The designs of the central system modules further incorporate extensive provisions for testability. These provisions include implementation of shift register paths for static state access and testing, as well as accessibility of control signals and data as required for module self-testing.

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1.2.3 MAINTENANCE PLAN (Continued)

If a recovery is not possible or fails, diagnostic tests are automatically invoked by the Maintenance Subsystem. These tests, all resident on the maintenance disk, include:

- i. PATH tests. These tests use shift register paths to set up and observe state. They provide excellent coverage for stuck-at faults.
- ii. MODULE FUNCTION tests. These tests consist primarily of microcode used to perform self-testing at full speed to aid in diagnosis of intermittent and timing-sensitive faults. Modules which have no control store, are self-tested by means of microcode in other modules, or in some cases by cycling under conditions initiated by the maintenance processor.
- iii. CONTROL STATE CONFIDENCE tests. These tests execute the medium systems instruction set to verify correct operation of the entire processor, including the functional microcode.

The tests are executed in the order that best suits the type of problem reported.

Clock and Voltage margins may be applied under the direct control of the Maintenance Processor to aid in the isolation of intermittent problems.

d. I/O COMPONENTS HOUSED IN THE MAINFRAME

To avoid system downtime for I/O module maintenance, all testing is planned to be done in the on-line environment, without interfering with operational components.

A few DLPs incorporate a Self Test capability that will permit the isolation of most failures in these modules to the FRU without external stimulation. These tests are executed automatically at power-up, whenever the module is cleared, or when the system sends the Self Test IO descriptor to the DLP. It is the responsibility of the Operating System to confirm a good Self Test result, before allowing a module to be added to the system configuration.

1.2.3 MAINTENANCE PLAN (Continued)

Testbus diagnostics are available for DLPS that do not have Self Test capability. These diagnostics reside on system disk, and are issued via the SMC in the on-line environment, under control of the on-line test bus driver program. Off-line capability also exists.

In addition to Self Test, and Test Bus diagnostics, MP driven tests are available which run in parallel with normal system I/O operations. Failing devices are "saved" (deleted from the MCP configuration), and are then tested by the MP in a manner which simulates normal operation (i.e. the MP initiates I/O operations via main memory, using the same I/O control block mechanism as the MCP).

Normal State tests (PTD driven) are also available to be executed in the system mix.

Control state PTD tests are also available for critical path devices.

e. I/O COMPONENTS HOUSED OUTSIDE OF THE MAINFRAME

Peripheral devices (including controllers) continue to include more Self Test capability. This applies particularly to OEM devices. As a result, off-line testing of these devices is the preferred form of fault diagnosis. Peripheral self test results should be, but presently are not, accessible by the maintenance processor for remote support. A means for the maintenance processor to acquire the results of peripheral self tests is needed.

Where such self test capability is not available, Normal State PTD driven tests are available. In some cases Normal State Confidence Tests are also available.

MP driven tests that execute in parallel with, but independently of, the MCP exist for critical peripherals.

1.3 FAULT HANDLING AND RECOVERY

The MP plays a role in the processor error recovery process, and handles extended error logging and analysis functions via its own Maintenance Log (MPLOG). This log supplements the MCP MLOG, and improves system availability through real time error analysis and fault prediction.

The MPLOG is restricted to "hardware" errors. Software errors are still handled exclusively by the operating system, which also stores all MPLOG data.

Hardware fault isolation in a multiple processor environment requires the ability to run diagnostics on a suspect module, without interrupting the operating system.

The MP displays "warning" or system status messages on the ODT when the occurrence of recoverable errors reaches a pre-defined frequency threshold for specific problem types.

The MP may initiate a call to a remote support center for hardware support.

An automatic on-line (MP driven) diagnostic process is provided, which permits preliminary diagnosis of system problems to be made without operator intervention.

Detection of an error by the processor causes an Interrupt to the SMC, which initiates a SNAP. The MP stores the SNAP picture in system memory, and on its own disk. The MCP keeps the SNAP picture for all errors.

The SMC or the MP (depending on the complexity of the analysis) determines from the SNAP information if an instruction retry should be attempted. The decision is based on the type and location of the error, the state of the RETRY flag in the Execute Module, and the recent error history of the processor, among other factors.

If a retry cannot be attempted, an error message is displayed on the ODT and the processor is not restarted. # In a multiple processor configuration, a Processor RD is written into memory indicating the nature of the failure. This RD is interpreted by the MCP via one of the surviving processors, and further action (e.g. job termination, and processor initialization), is handled at the operating system level.

1.3 FAULT HANDLING AND RECOVERY (Continued)

If a retry can be attempted, the MP will initialize the processor to the appropriate starting point, place it in single instruct mode, and cause the failing OP to be re-executed. If the OP executes without error, the MP logs the successful recovery, and places the processor in normal run mode. If the OP fails again immediately, two further retries are attempted. If a successful execution cannot be made, the error is assumed to be hard, and it is handled as if no retry were possible.

1.4 REMOTE INTERFACE

The MP has a Remote Interface and appropriate software to permit the system to be accessed from a remote center, both in active and passive modes.

The physical connection is a single data comm link for both hardware and software support.

A security mechanism is designed into the remote interface. This consists of a keylock arrangement and software security. Remote transmissions are also encoded.

Remote capabilities include bidirectional file transfer, the ability to switch the line back and forth between data and voice modes while maintaining the logical and physical connection, and message exchange between the RSC workstation and the target system ODT/maintenance console or local terminal.

Data communication transmission mode and line speed will be configurable from the maintenance console via a "Remote Configuration" menu.

The AWS incorporates a built-in modem, with auto-call. Auto-answer may be available for performance driven maintenance. Local regulations may prohibit the use of a built-in modem at some International sites; in this situation, the remote connection will be via a RS232 port, and auto-call and answer features will be dependent on local modem capabilities.

1.4 REMOTE INTERFACE (Continued)

The Maintenance Processor is powered independently of the rest of the mainframe, and is able to remain powered-on even when the mainframe is powered-off. The system may be powered-on via the remote link in this situation. This capability may be extended to peripheral units that are able to interface to the ECM net (i.e. have their own ECM slave equivalent). Local switches in each cabinet will remote power-on of any unit.

The remote interface will use a subset of the Burroughs Dialog Block protocol as described in the following specifications:

- # 3398 2075 Dialog Block Protocol for Remote Support
- 3398 2067 Message Block Protocol for Remote Support
- 3398 2059 Eight-bit Data Communications Protocol
for Remote Support

This protocol is currently being used on the A9 system, and is specified for the A3 and A15.

A terminal emulation protocol will also be available (poll/select) to maintain compatibility with the B2900/B3900/B4900 remote interface, and allows communication with existing Medium System Support Centers.

Additional high level protocols (such as X.25), necessary for future communications particularly in International regions, will be defined and implemented as required to support Corporate maintenance goals.

1.5 ENVIRONMENTAL MONITORING AND CONTROL

The Maintenance Subsystem monitors and controls key environmental factors as follows:

MONITORS AND REPORTS,

- i. POWER VOLTAGES (AC/DC, STEADY STATE, and TRANSIENTS)
- ii. AIR TEMPERATURE (at various locations within the cabinet)

CONTROLS,

- i. DC VOLTAGE LEVELS (ON/OFF, and CONTINUOUSLY VARIABLE MARGIN ADJUSTMENT)

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1.6 RELIABILITY

The Maintenance Subsystem, as one of the most crucial system components, is designed to be extremely reliable. The subsystem may be configured to be fault tolerant, and in this configuration a minimum availability of 99.995% is guaranteed. This availability is achieved with a MTBF of 20,000 hours, and a MTTR of 1.0 hour or less, where a failure is defined as loss of all Maintenance Subsystem capability.

A failure in the Maintenance Subsystem will not cause a system crash (for the most probable failure modes), but may precipitate a controlled system interrupt.

1.7 # MULTI-PROCESSOR INTERFACE

The Maintenance Subsystem is configurable to support from one to four processors. This implies that a capability to perform maintenance functions on a single processor, while concurrently performing ODT, and monitor and control functions for up to three others.

2 DESIGN ATTRIBUTES

2.1 GENERAL DESCRIPTION

The V500 Maintenance Subsystem utilizes six distinct types of hardware modules, some of which may be duplicated depending on the system configuration (number of processors) or fault tolerance requirements.

The six modules are:

MODULE	NUMBER IN MINIMUM CONFIGURATION	NUMBER IN MAXIMUM CONFIGURATION
1. MAINTENANCE PROCESSOR	1	2
2. SYSTEM MAINTENANCE CONTROLLER	1	2
3. 20MB 5 1/4" ** WINCHESTER DISK DRIVE *	1	2
4. SINGLE 640KB 5 1/4" MINI-DISK *	1	2
5. ENVIRONMENT CONTROL MOD (MASTER)	1	2
6. ENVIRONMENT CONTROL MOD (SLAVE)	2	TBD

* DISK CAPACITY IS UNFORMATTED
 ** REQUIRES 2 10MB DRIVES ON THE B25

A B25 workstation is used as the Maintenance Processor (MP), and therefore keyboard and display functions are included. The B25 will be superceded by the AWS (Advanced Work Station). The AWS will then replace the B25 as the Maintenance Processor.

2.1 GENERAL DESCRIPTION (Continued)

The MP provides overall control of the Maintenance Subsystem, communicating with the other subsystem components through external interfaces, as follows:

1. A high speed serial network interface to the SMC. This is the RS422 cluster port on both the B25 and AWS.
2. The AWS and B25 have a parallel port to the Winchester disk, which is also utilized for the mini-disk.
3. An RS232 interface provides the Remote Port. The AWS may have an optional built-in modem, otherwise an external modem will be required.
4. Another RS232 interface is available. # It may be used to provide a redundant path for ODT functions through the I/O Subsystem, or as a communication path between two MPs in a dual configuration.
5. A Centronics Printer interface. Utilization is TBD.

The System Maintenance Controller (SMC) is a microprocessor (80186) based module, which provides high speed interface to one or two processors (if they are housed in the same cabinet), the IOPs, DTMs, and Memory Storage Boards. The SMC is an interrupt driven real time processor. A parallel interface is provided to the I/O bus to allow for high speed memory access, and to permit the Maintenance Subsystem to be accessed as an I/O Channel by the operating system.

The TESTBUS interface required for DLP maintenance is also included in the SMC. It may be driven by the system or the MP.

One MP can handle up to four processors (maximum V500 configuration), but a second MP may be installed as a fault tolerance option. In this case, the second MP monitors the state of the first while the first continues to perform all normal MP functions. If the first MP dies, this is detected by the second MP which takes over control.

There are two RS422 busses on a system configured with two MPs. Each MP is connected to a separate bus, and the SMCs and ECMs are connected to both (dual ported). This provides a level of protection against the failure of any one bus taking down the system.

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2.1 GENERAL DESCRIPTION (Continued)

The Winchester disk drive contains the program and data files to perform all the normal system initialization and troubleshooting functions assigned to the Maintenance Subsystem (see Section 1 of this document). This permits rapid system initialization, and automatic execution of diagnostics under programmatic control when a failure is detected. The MP also maintains an error log (MPLOG) on the Winchester, and provides for temporary storage of up to two SNAP pictures per system processor.

The mini-disk serves as a backup to the Winchester in the event that no path is available to system tape or disk (the normal backup media). It also provides an alternate means of loading and running UIO diagnostics.

The Environment Control Modules are intelligent units which provide the control and monitor interface between the MP and the Power and Cooling Subsystem. They also provide hardwired control in the event of a MP failure or a catastrophic environmental problem, to ensure the protection of the mainframe logic. A single Master ECM in each processor cabinet communicates with as many Slave ECMs as are required to control system, and potentially peripheral, power.

2.2 MAINTENANCE SUBSYSTEM INTERFACING

Although the MP maintains overall control of the Maintenance Subsystem, the "intelligence" is shared with the SMC. This permits the SMC to handle some complex processor and memory interfacing and monitoring tasks with minimum MP involvement, freeing up the MP to handle the other interfaces more efficiently. The Maintenance Subsystem interfaces are therefore grouped into MP controlled and SMC controlled types.

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2.2.1 MP INTERFACES

INTERFACE DEVICE	MAXIMUM NUMBER	GENERAL DESCRIPTION	BANDPASS (/SEC,MAX)
1. REMOTE PORT	1	RS232	1200 BAUD Min.
	1	MODEM OUT (AWS)	1200 BAUD Min.
2. MINI-DISK	1	PARALLEL	TBD
3. WINCHESTER	1	PARALLEL	TBD
4. ECM	2		
SMC	2		
MP	1	RS422 BUS	1.8 Mbits
5. PRINTER	1	CENTRONICS	
6. TBD	1	RS232 (SPARE)	9600 BAUD Max.

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2.2.2 SMC INTERFACES

INTERFACE	MAXIMUM NUMBER	GENERAL DESCRIPTION	BANDPASS (/SEC)
1. MP	2	RS422	1.8 Mbits
2. PROCESSOR STATE (CHAINS)	2	See Section 3	SYSTEM CLOCK RATE
3. PROCESSOR ERR./STOP	2	See Section 3	N/A
4. PROCESSOR CLOCK CONTROL	2	See Section 3	N/A
5. I/O BUS	1	32 BITS DATA/8 ECC nn BITS CONTROL	50 MBYTES
6. TESTBUS	1	2-WIRE BDI	19.2K BITS

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2.3 SYSTEM ARCHITECTURE

Figure 2.1 illustrates the integration of the Maintenance Subsystem components into a large V500 system configuration.

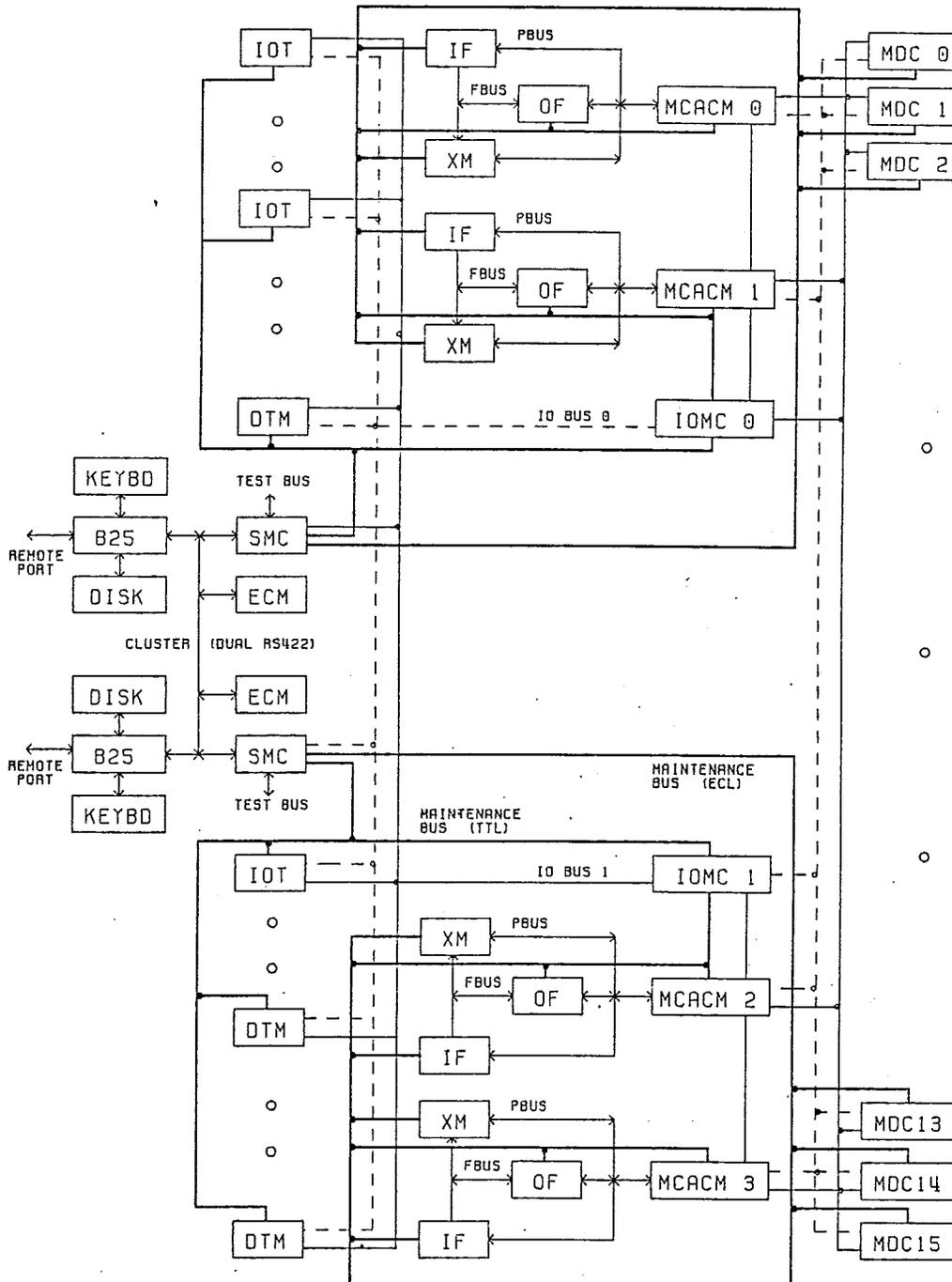
The configuration shown is a four processor, dual cabinet system with two Maintenance Processors (the maximum, fault tolerant configuration).

Figure 2.1 illustrates the system architecture utilizing a B25 as the Maintenance Processor. In this configuration, one B25 performs the Maintenance Processor role for the whole system, communicating with all four processors, and associated ECMs, via the cluster. This B25 performs ODT functions concurrently with the MP functions when the system is running under MCP control.

The second B25 performs only as an ODT as long as the first B25 continues to function as the MP. It monitors network activity, via the SMC, to determine if the MP is still alive. If the MP B25 dies, the second B25 automatically takes over its role, initiates the diagnostic process, and reports the problem to the operator.

FIGURE 2.1

V500 CENTRAL SYSTEM ARCHITECTURE



2.4 MP ARCHITECTURE

Figure 2.2 illustrates the configuration of the B25 Maintenance Processor. The design is based on the 80186 microprocessor, and includes the following features:

- a. 512KB RAM
- b. nnKB ROM
- c. External Interfaces:
 - 2x RS232
 - 1x RS422 Cluster Port
 - 1x Centronics Printer
- d. Integrated Self Test
- e. Time of Day Clock
- f. 20MB Winchester/640KB minidisk subsystem
- g. 15" Color monitor with graphics controller
(optional - TBD) (Not shown in Figure 2.2)

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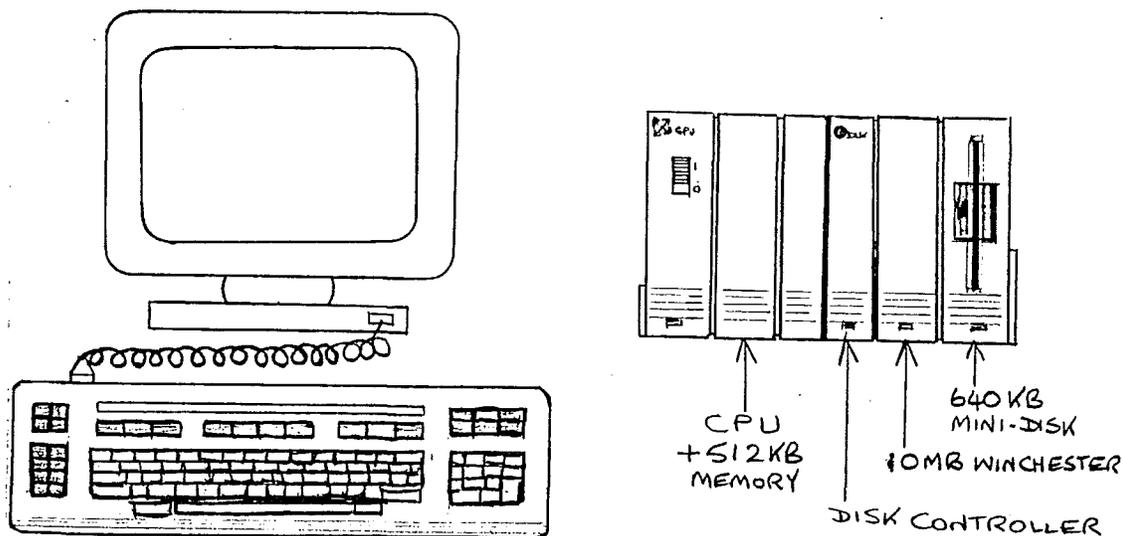
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FIGURE 2.2

V500 MAINTENANCE PROCESSOR (B25)



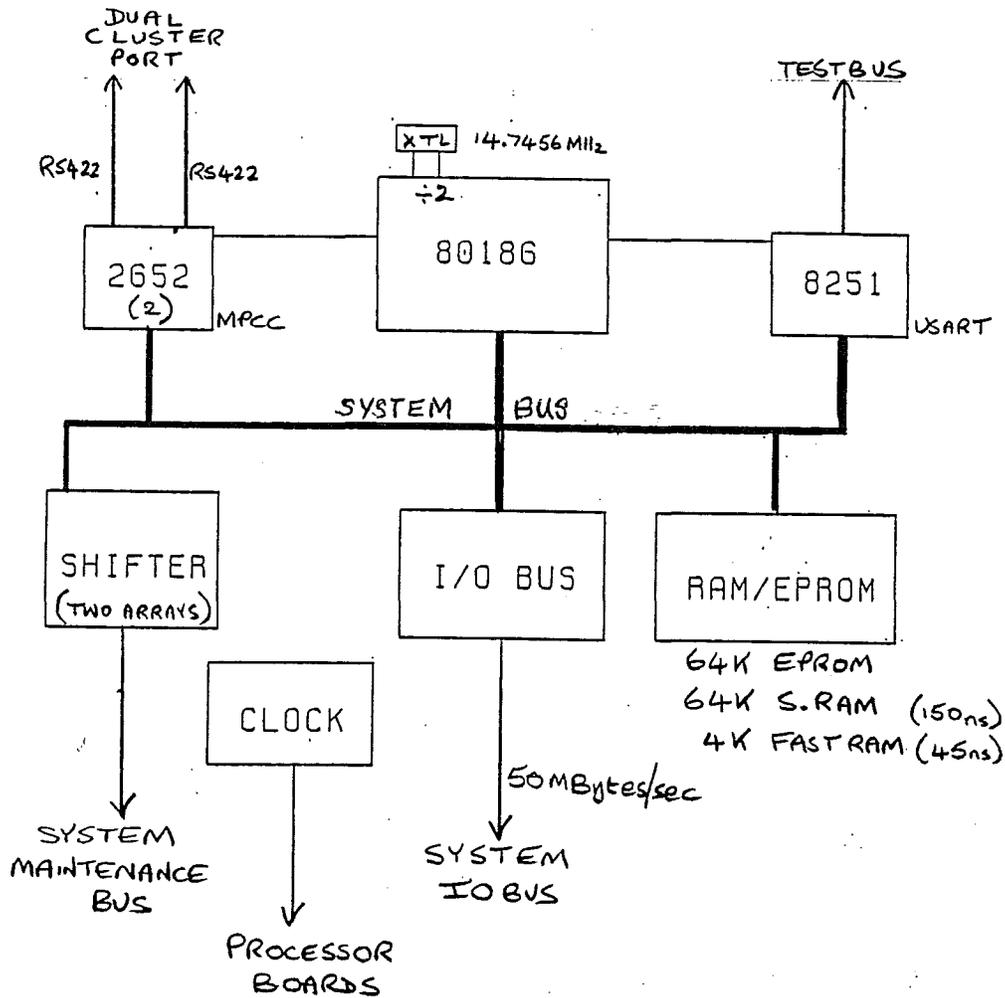
2.5 SMC ARCHITECTURE

Figure 2.3 illustrates the basic architecture of the System Maintenance Controller.

- a. The SMC is microprocessor based, which allows for greater operational flexibility, and an offloading of some control functions from the MP.
- b. The SMC shares the interface to the IOMC with the IOPs/DTMs, permitting direct system memory access by the Maintenance Subsystem, which enhances both normal and diagnostic performance.
- c. The SMC can interface to two processors (as long as they share a common cabinet), thus the processor status and clock control interfaces are expanded.
- d. The Maintenance Bus is divided into an ECL bus and a TTL bus to handle module interface requirements.
- e. The DLP TESTBUS is driven from the SMC.
- f. The SMC contains the system clock generation logic, which is implemented as a logically separate function within the module.
- g. The SMC has dual RS422 ports, enabling independent connection to two B25s.

FIGURE 2.3

V500 SMC MODULE BLOCK DIAGRAM



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2.6 FAULT TOLERANCE

The MP and SMC are reliable components but are not individually fault tolerant. Fault tolerance can be achieved at the subsystem level by adding redundant modules into the configuration as discussed in Section 2.3.

Some redundancy options are only applicable to dual cabinet systems, so a fully fault tolerant system includes two CPUs, each housed in a separate cabinet. Each CPU has its own SMC and MP (although only one MP is active at a time).

The Maintenance Subsystem components with the lowest predicted availability are the B25 and the Winchester Disks. In the event of a failure of one of these components, system operation may continue through the use of backup components, although throughput may suffer. (Another B25 may be installed as an ODT, and Mini-Disk and/or system tape is accessible by the MP as Winchester disk backup).

2.7 MAINTAINABILITY

Each of the Maintenance Subsystem components listed in Section 2.1 will be maintained in the field on a replacement basis (each component is an FRU), with the exception of the B25, which will be maintained on a module replacement basis.

The B25, SMC, and ECM include integral self test capability. Each of these units executes a self test on power-up, system clear, or when initiated under operator/software control. An indication of the status of each unit is available independently of the state of the other subsystem components. The SMC and ECMS use LEDs; the B25s use a combination of LEDs and on-screen messages.

The Winchester and Mini-Disks are testable with operator initiated diagnostics. The test results are displayed on the B25 screen.

The MP/SMC interface is also tested by a MP resident diagnostic. In the event that the MP cannot communicate with the SMC or the Winchester disk, an appropriate message is displayed on the B25.

Extensive disk-resident Maintenance Subsystem diagnostics are available to assist in the isolation of problems not located by either the self-test or the resident diagnostics.

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3 MAINTENANCE ATTRIBUTES OF V500 HARDWARE

This section describes the hardware features of the V500 system that are utilized by the Maintenance Subsystem to perform its various tasks.

3.1 STATE ACCESS

Shift chains provide access either directly (on the chain) or indirectly (can be gated onto the chain) to all state within the V500 processor, including the Memory Control Modules, Memory, DTMs, and IOTs.

Each card has a maximum of two chains. One may be designated the Maintenance Chain and if so, it is reserved for maintenance functions only, primarily implementation of Maintenance Panel compare logic. The other chains, collectively referred to as Data Chains, provide access to all remaining state.

One SMC provides the maintenance interface to all processor modules within a single cabinet. Thus, in some multi-processor configurations one SMC interfaces to two independent processors. Fault tolerance may be achieved in dual cabinet systems, as each cabinet has its own SMC, permitting the system to continue operation in the event that one SMC fails (this capability is system software dependent).

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3.2 INTERRUPT SYSTEM

A major function of the SMC is to monitor the processor, memory control, and IOTs for error conditions. This is done through an interrupt mechanism, in which each processor module has its own unique ERROR interrupt signal to the SMC.

The outputs of the various error detection circuits within each processor card are clocked into an Error Register, which includes a bit for each kind of error that can be detected within the card. The outputs of the register elements are then or'd together and driven to the SMC as the module ERROR signal. The elements of the error register are contained on the card data chain.

Whenever possible, the elements are grouped together on the chain. The ERROR signal is also used internally within each module to disable the module clock, thus freezing the module on the occurrence of an error. A bit is made available on the maintenance chain to allow this automatic clock stop function to be disabled for debug or maintenance.

When an error interrupt signal is received by the SMC, it will begin an error handling process appropriate to the error type. This process may include bringing the remaining modules in the failing processor to a controlled halt, performing a SNAP, and attempting a recovery.

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3.3 SYSTEM MEMORY ACCESS

The SMC interfaces to the I/O Memory Concentrator via the I/O Bus. This allows the Maintenance Subsystem to access the system memory at high speed in both off-line and on-line modes.

In the off-line mode, this permits more thorough and rapid testing of the memory and the IOT, DTM and IOMC modules. The program LOAD function can be handled much more efficiently through this interface than through the use of the memory shift chains.

In the on-line (MCP) mode, this interface permits the implementation of a communication path between the Operating System and the Maintenance Subsystem. This path is used for such things as writing the Processor SNAP picture into memory after an error has occurred (this must be done without stopping normal memory operation in a multi-processor system).

The on-line interface also provides a path for the Operating System to access the Winchester Disk (for updates, etc.), and other Maintenance Subsystem components, such as the B25 (for ODT functions) and Remote Port.

3.4 CLOCK CONTROL

The SMC controls activation of the clock within each of the processor modules. Control is on a card by card basis with each card having its own clock enable line.

The clock may be activated in either of two modes:

1. Normal Mode
2. Maintenance Mode

In Normal mode, all clocks within selected modules are activated or deactivated as a single group. In Maintenance Mode, clocks are controlled at the card or module level.

This mechanism permits the Maintenance Subsystem to control the system on a clock by clock basis at the card, module, and system level.

While a module is receiving clocks in Normal mode, a Maintenance chain may be placed in shift mode, thus permitting access to this chain to take place without interrupting normal processor operation.

The SMC also maintains control of the system clock frequency via a register in the clock generator. Maximum deviation from nominal that can be accomplished is T.B.D.

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3.5 STOP LOGIC

Stop logic is implemented via the Maintenance Shift chains. There is a register on a Maintenance Chain corresponding to any function for which stop logic is desired. The register is loaded with a value which is constantly compared to the value of the function being monitored. If an equal condition occurs, and if the enable toggle is set, a STOP signal is gated to the SMC.

The stop condition active levels within each module are OR'd together with other modules and bussed to the SMC as two STOP signals, STOP-AND and STOP-OR.

When a module STOP signal is received by the SMC, it will bring the processor to an orderly halt.

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3.6 SMC-PROCESSOR INTERFACE

The SMC interfaces to the processor modules via two backplane Maintenance Busses. One bus is implemented in ECL and interfaces to the XM, FETCH, MEMORY CONTROL/CACHE, and MEMORY STORAGE modules. The other bus is implemented in TTL, and interfaces to the IOT and DTM modules. The IOMC contains both ECL and TTL logic and is interfaced to both the TTL and ECL busses.

The two busses are logically the same, although the implementation varies slightly due to packaging and loading differences.

Functions, handled via the interface, fall into two broad categories: CLOCK and CLEAR control, and STATE ACCESS via shift chain manipulation. These functions are controlled at the module level, a module being a card or group of cards that has a distinct functional identity.

Within a module, clock functions may be performed at the card or module level. Clear functions may be performed at the module or chain level.

One SMC provides the maintenance interface to a single processor cabinet, which may contain one or two processors.

The SMC Processor Interface is further defined in the SMC Engineering Design Specification (see "Related Documents").

4 MAINTENANCE ATTRIBUTES OF SYSTEM SOFTWARE

The architecture of the V500 Maintenance Subsystem permits it to interact with the Operating System software to perform certain key functions.

Many of these functions rely on the ability of the SMC to emulate a DTM, and thus communicate with the MCP as a regular I/O device.

4.1 SYSTEM ODT

During normal system operation (when no maintenance is being performed), the primary function of the Maintenance Processor is to act as a system ODT.

The SMC appears to the system as a single I/O channel, to which are attached multiple units of various types. These units include the Winchester disk, the Remote Port, the TESTBUS, the SMC itself, and the MP/ODT. Multiple concurrent I/Os are permitted on this channel (under MCPX). Thus, I/Os for the ODT are initiated on the appropriate channel and unit in the normal manner.

The MP optionally incorporates a color monitor which is utilized by the systems software to enhance console output displays. The operator is able to select various color combinations according to local preference.

The utilization of the Maintenance Subsystem to provide the ODT function eliminates the need for a Console or Uniline DLP when only one ODT is required. If more than one ODT is included in the configuration, then a Uniline DLP is required for each additional unit.

Fault tolerant configurations that incorporate two B25s (MPs) may use them both to support the ODT function.

It is planned that the Maintenance Processor will support an additional RS232 interface to an ET1100 or equivalent device in the future.

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4.1 SYSTEM ODT (Continued)

The ODT Automatic Display (AD) function is enhanced by the use of multiple screen buffers in the MP. The number of pages utilized (max. 5), and their format, is determined by the MCP based on operator input to an extended AD command. Each page type is pre-formatted by the MCP, and contains a page type identifier. The MP keeps each page updated in its memory, but only displays a page (other than the one currently selected) at a specific operator request (hitting a Function Key), or if an automatic page rotation scheme has been defined (this is an MP function). Thus, the operator has "instant" access to various system status reports (MCP Control Messages, I/O Status, or whatever) without being locked into a fixed display sequence. Other display pages are used for maintenance functions.

When the system is configured with two or more ODTs, it is possible to "SAVE" the MP ODT (logically remove it from the system), and utilize it exclusively for maintenance functions, while the other ODT(s) continue to perform the normal on-line function. It is not, however, a requirement that the ODT be saved in order to perform on-line maintenance, as the MP may perform both ODT and maintenance functions concurrently.

The "HALT/LOAD" ODT may be designated during each HALT/LOAD by the selection of an "ALT ODT" option in the initialization menu.

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4.2 REMOTE PORT

The system Remote Port is an RS232 serial interface to the MP. It is accessible to the system in normal mode as a unit on the maintenance channel. In off-line mode, it is controlled directly by the MP. Security, data encryption/decryption, and message protocols, are handled by the MP.

An optional modem module is available for the maintenance subsystem (AWS configurations only). If this modem is not included in the configuration, one must be supplied from elsewhere before the remote port can be utilized.

4.3 MAINTENANCE DISK ACCESS

The Maintenance (Winchester) Disk is accessible to the system as a unit on the maintenance channel. However, the system does not have direct access to the disk itself, but has its commands interpreted by the MP, which is responsible for directory maintenance and all other disk management functions. The interface is used for whole file transfer and removal, and directory enquiries only, and is primarily intended as an on-line update path for maintenance subsystem software.

4.4 SNAP

SNAP pictures are written into a reserved area of system memory by the SMC. Two SNAP pictures for each processor are saved on the Maintenance Disk (the first and last for the most recent error event for each processor), and will be passed to the MCP in response to the appropriate request. In order to reduce total SNAP time, SNAP pictures are buffered in the MP, and not written to the disk until the system has been restarted.

The implementation of program level selective SNAP ENABLE is TBD.

4.5 ERROR LOGGING

Errors detected by the processor are defined as either "hard" or "soft". A hard error is one that can only be caused by an actual hardware failure (e.g. a bus parity error). A soft error is one that (in the absence of a hard error) is assumed to be caused by a software error, and therefore does not imply any hardware failure (e.g. an invalid address).

Hard errors are handled by the Maintenance Subsystem directly. The error handling process includes stopping the processor with the error (possibly more than one processor if the error involves shared resources), performing a SNAP and analyzing the error indicators, writing a processor RD in system memory, and attempting an instruction retry (if this is viable).

Soft errors are handled by system software through a soft interrupt mechanism. The error handling process may involve a SNAP (initiated by a soft request), but this is the extent of maintenance subsystem involvement. Soft errors are not recoverable via instruction retry.

Both types of errors result in entries in the MLOG. Hard errors will also be logged and analyzed by the MP.

Details of the proposed fault handling mechanism may be found in the V500 Fault Recovery Guidelines.

The increased error detection logic in the processor makes it possible for the MP to make available to the MCP more specific diagnostic information than can be contained in the currently defined processor RD. To take advantage of this potential, the MP will provide extended RD information available to the MCP on request. It is assumed that the MCP will make such a request as part of the normal RD handling procedure.

The MP passes information on non-fatal environmental problems (e.g. power brown-out, temperature change) detected by the Environment Control Modules to the MCP via the processor SNAP mechanism. These SNAPS are handled by the MCP in a manner similar to other non-critical problem reports (e.g. soft memory errors). This is the mechanism by which the MCP is provided with an "early warning" of problems that may subsequently require a power down.

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4.6 FATAL MCP ERRORS

The incidence of "red light" processor halts is expected to be extremely low on the V500, due to the improved error handling capability of the Omega operating system. Meaningful error messages are displayed on the ODT by the MCP in almost all error situations.

Specific situations in which the MCP cannot communicate an error report to the operator are to be defined, and a means established whereby the maintenance subsystem can perform this function. A design goal is to make a meaningful error report available to the operator in all failure situations where sufficient hardware to do so remains functional.

4.7 SOFTWARE DEBUG AIDS

The complex structure of the Omega software environment make it desirable to utilize the intelligence of the maintenance subsystem to provide a meaningful analysis of a program or system software state for debug. The contents of such an analysis, the preferred display format, and any interactive commands required, are to be defined.

4.8 SYSTEM INITIALIZATION

The maintenance subsystem is responsible for verifying the operational state of the system before initialization, and performing initialization steps up to the point of loading and initiating execution of the system boot program. A meaningful error message is provided whenever a problem is encountered, including, where applicable, a recommended course of action for recovery. Once the system boot program begins execution, it (and succeeding levels of system software) assumes responsibility for providing error information to the operator.

Loading of any DLP or I/O controller firmware files required to begin execution of MCP code is a function of the maintenance subsystem. Such files are maintained on the maintenance disk, and are updateable by either mini-disk file transfer, or on-line file transfer from the system disk.

Once the system configuration has been defined, system initialization can be accomplished by the operator with a single keystroke. (The system configuration need only be defined at installation, or whenever the hardware required for initialization is reconfigured).

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4.9 SYSTEM CRITICAL PATH TEST

The need to provide a means to rapidly isolate a problem which prevents the system from being initialized (and hence MCP level diagnostics from being utilized), is satisfied by a combination of a free-standing pre-boot diagnostic program, and the incorporation of a diagnostic capability into the bootstrap program itself.

A pre-boot system critical path test is provided as a part of the standard maintenance subsystem software, which may be optionally executed every time the system is halt/loaded (execution time is less than 60 seconds). This program verifies the correct operation of those system components required to begin execution of the bootstrap program only. Thus it is restricted to checking the maintenance subsystem itself, the processor, and a portion of main memory.

If the system critical path test can be executed successfully, sufficient hardware is functional for the bootstrap program to execute, and responsibility for providing error messages in case of a problem will be assumed by it.

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5 MAINTENANCE SOFTWARE ARCHITECTURE & DEVELOPMENT

The maintenance software is divided into two distinct systems, the SMC and the MP. The MP software is designed to run in the environment of a relatively sophisticated operating system; operator interface and non-time-critical functions are performed in the MP. The SMC provides chain and clock level processor interface; time-critical functions such as SNAP and event stop are also controlled by the SMC.

5.1 MP SOFTWARE ARCHITECTURE

The Maintenance Processor handles the bulk of the software for the Maintenance Subsystem. The screen of the MP serves as both system and maintenance ODT; user input to both the maintenance and the functional system are through the MP keyboard. Operator input for maintenance is analyzed in the MP. A few functions, such as interrogation of MP files or certain MP software variables, are handled entirely in the MP. Most functions will require translation into commands to be sent to the SMC. This translation is a large percentage of the MP software.

Functions of the MP include system initialization, diagnostic testing, setting up low-level processor clock and chain commands, error logging, and remote diagnostic interface. All maintenance data files, including control store data, test data, screen formats, and register/RAM directories, are resident on the MP's Winchester or floppy disks.

In most instances, the MP is only performing one function at a time, but it must be able to handle concurrency. For example, when passive remote software is being run, the MP must be handling the ODT function, processing the remote interface, and still be able to respond to interrupts if a processor STOP or ERROR condition occurs.

The maintenance processor software is divided into 4 levels:

LEVEL	LANGUAGE	DESCRIPTION
IO DRIVERS	Assembly	Lowest level - hardware specific routines. Generally come with the operating system (BTOS).
OPERATING SYSTEM (BTOS)	PL/M	Task scheduling, memory & file management, etc.
GENERAL PROCEDURES	PL/M	Scanner, display routines, etc. Utilize standard BTOS procedures where possible.
APPLICATIONS	PL/M	State access, system initialization, diagnostic test drivers, etc.

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5.1.1 IO DRIVERS

The IO Drivers are extensions of the operating system which provide device-specific interfaces to the hardware. They are written in assembly language and are called by higher-level routines with a standard set of parameters. These routines are largely included with the B25 Operating System (BTOS).

5.1.2 OPERATING SYSTEM

The B25 and AWS run BTOS (the B20 operating system) as their native operating system. BTOS is a multitasking, priority-based interrupt-driven operating system, as is needed for the several concurrent MP functions.

The MP software is being designed to ship on the B25 initially. For the AWS, low-level modules may have to be modified. The new I/O handlers should come as part of the AWS software package. The similarity between B25 and AWS should make the conversion relatively straightforward.

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5.1.3 GENERAL PROCEDURES

MODULE	FUNCTIONS
File Handler (BTOS)	Create file Open/close file Read/write sector Display directory Diskette copy (Mini-Disk) Diskette format (Mini-Disk) File copy
Scanner (BTOS-Executive)	Accept & parse input commands; Accept & parse forms mode input
Screen	Write formatted displays Write messages
DLP	Initialize channels Handle DLP buffer allocation Receive data from host Send data to host
ODT	Test Read Write
Remote Link	Test Read Write
Disk	Test Read Write
Host Control	Clear interface Send data Report error status

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5.1.4 APPLICATIONS

The applications software in the MP is broken into functional modules as follows:

Maintenance Executive, including:

Command Analysis

Initialization of Software variables

Primitive SMC commands:

Read/write/display chains

Clock/clear chains

Read/write RAMS

Read/write system memory

Testing:

Load/initiate control state tests

Load/initiate module tests

Path test diagnostic driver

Test bus driver

Host system-level commands:

Set/display system configuration variables

Clear system memory

System control & status display
SI, SC, INIT, HALT, RUN, <SPCFY>, etc

System initialization - CS load/verify, load MCP

Set/display conditional stop logic

Error logging/reporting

5.1.4 APPLICATIONS (Continued)

Other interfaces (non-SMC)

Remote port interface

Environmental control

Disk boot from system tape

Floppy disk as host system resource

File transfer, system to MP Winchester disk

MP video as system ODT

In addition to programs, certain data files are necessary to support these functions.

These files include:

Module Directory (MODDRY) - State Access

Ram Directory (RAMDRY) - Ram Access

Message Directory - Memory Access
System Control
Program Load
Stop Logic

Screen Files - (Menus) - Initialization,
- Stop Logic,
- System Configuration, etc.

Control Store Data

Diagnostic test index - for automatic mode of
running diagnostic tests

Diagnostic test error message file - Card replace info.

Test Data - Processor diagnostic tests
Microcoded module tests
Control state confidence
tests
DLP testbus diagnostic tests

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5.2 MP SOFTWARE DEVELOPMENT SYSTEM

Software development will be done on the B20/B25 under BTOS. The language PL/M has been chosen for several reasons:

1. It is used for B20 system software development by Convergent Technologies and Burroughs.
2. The language is well structured.
3. Modules can be separately compiled and linked; in addition, Assembly code can be linked directly to PL/M modules to provide functionality or speed not obtainable through the language itself.
4. PL/M is very close to Pascal; therefore, existing code modules written in Pascal could be converted to PL/M with a minimum of effort.
5. PL/M is more memory efficient on the B20 than PASCAL.

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5.3 SMC SOFTWARE

The main functions of the SMC software are to accept, interpret, and perform commands received from the MP; and to respond to interrupts from the processor, either maintenance mode error or stop logic, or normal state DLP-type commands. Because of the need to respond to several types of interrupts and process them in a timely fashion, it has been determined that a simple kernel operating system is needed to facilitate SMC software development. The VRTX system, currently being used by the Data Comm section in Pasadena, has proven to be an efficient, compact, reliable and simple-to-use operating system.

The SMC will be driven by an 80186 microprocessor. The software modules are as follows:

I/O HANDLERS/PDFs

Maintenance Bus

IO BUS

Test bus

Cluster

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5.3 SMC SOFTWARE (Continued)

TASKS

Self-test

Initialization

Decode commands from MP

DTM Emulator

Memory Access

Quick program load

Processor Fault Handler

Interrupt decoder

SNAP

Retry control

Processor Chain & Clock Controller

Processor Ram Loader & Tester

OPERATING SYSTEM (VRTX)

5.4 SMC SOFTWARE DEVELOPMENT SYSTEM

Software for the SMC will be developed on INTEL MDS's. Some time-critical functions will be written in Assembler. Other portions of the code can be written in PL/M (supported by Intel).

The use of VRTX requires a PL/M interface library to be supplied by Hunter & Ready. Such a library is already available within the plant.