B 9499-3 DISK PACK ELECTRONIC CONTROLLER (MODEL 206)

TECHNICAL MANUAL
VOLUME 3:

THEORY OF OPERATION

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1. BASIC PRINCIPLES

INTRODUCTION

This manual provides reference documentation which describes the normal operation, sequences, and circuitry of the model 206 Disk Pack Electronic Controller (DPEC). The following is a list of related literature:

Model 206 Disk Pack Electronic Controller Function and Operation, form number 1084365.

Model 206 DPEC Illustrated Parts Catalog, form number 1104189.

Model 206 DPEC Test and Field Documentation.

Model 206 Disk Pack Drive Function and Operation, form number 1084324.

Model 206 Disk Pack Drive Theory of Operation, form number 1084332.

GENERAL DESCRIPTION

The 206 DPEC is a hard-wired controller that includes all the hardware for synchronizing the interfaces between the B 1700 Disk Pack Control (DPC) and the 206 Disk Pack Drive (DPD).

The controller is designed for a maximum configuration of one by eight spindles of disk pack drives. All DPEC's are capable of one by eight operation with no modifications. Standard 25-wire interface (parallel) is used between the DPC (host system) and the DPEC.

The DPEC acts upon I/O instructions from the B 1700 host system, performs the operation specified by the I/O descriptor and, upon completion, generates a result descriptor containing the operation completed and any error status information.

BLOCK DIAGRAMS

The following paragraphs and figures describe and illustrate the block diagrams of the sections of the DPEC. Figure 1-1 contains an introduction to the block diagram legend and an index.

NOTE

In the following discussions both TRUE and FALSE, as well as LOW and HIGH, are being used. Because of the logic symbology used with the DPEC, a LOW level signal (approximately 0.0 volt) must not be considered as being either a TRUE or FALSE level unless the source of the signal is known.

When referring to the schematic diagrams, any time a signal name is followed by a slash, the active level of that signal will be a LOW. If the signal name has no slash, it is to be considered a HIGH active signal.

When using the block diagrams, it must be remembered that "signals are shown HIGH active regardless of their actual sense" (state). If the actual sense of the signal is required, refer to the schematics in the test and field documents.

SYSTEM BLOCK DIAGRAM

Figure 1-2, block diagram B2, is the B 1700, 206 DPEC, and 206 disk pack drive interface.

LOGIC OVERVIEW

Figure 1-3, block diagram B3, is an overall view of the DPEC logic. The individual blocks contained in this diagram will be discussed in the following paragraphs.

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NOTES:

1. In this set of block diagrams, signals are almost always shown high active regardless of their actual sense.

2. Groups of signals are often shown as a single line with a diagonal cross hatch and a number indicating the number of signals referred to. Signal names are also written in a shorthand form. For example, DATAnn (nn=00-15) 16, represents sixteen wires whose names are DATA00 through DATA15.

3. The page numbers written inside blocks (e.g. P39, or P78) refer to the schematic page(s) where this logic block is shown in detail. Occasionally reference is made at the right or left margin to interconnecting block diagram pages (e.g. B1 or B19).

Figure 1-1. Block Diagram Legend and Index

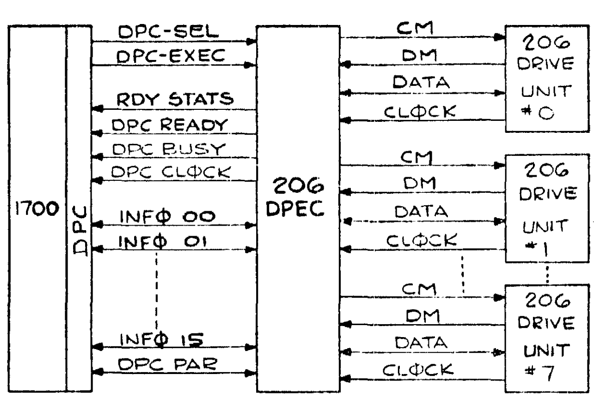

Figure 1-2. System Block Diagram

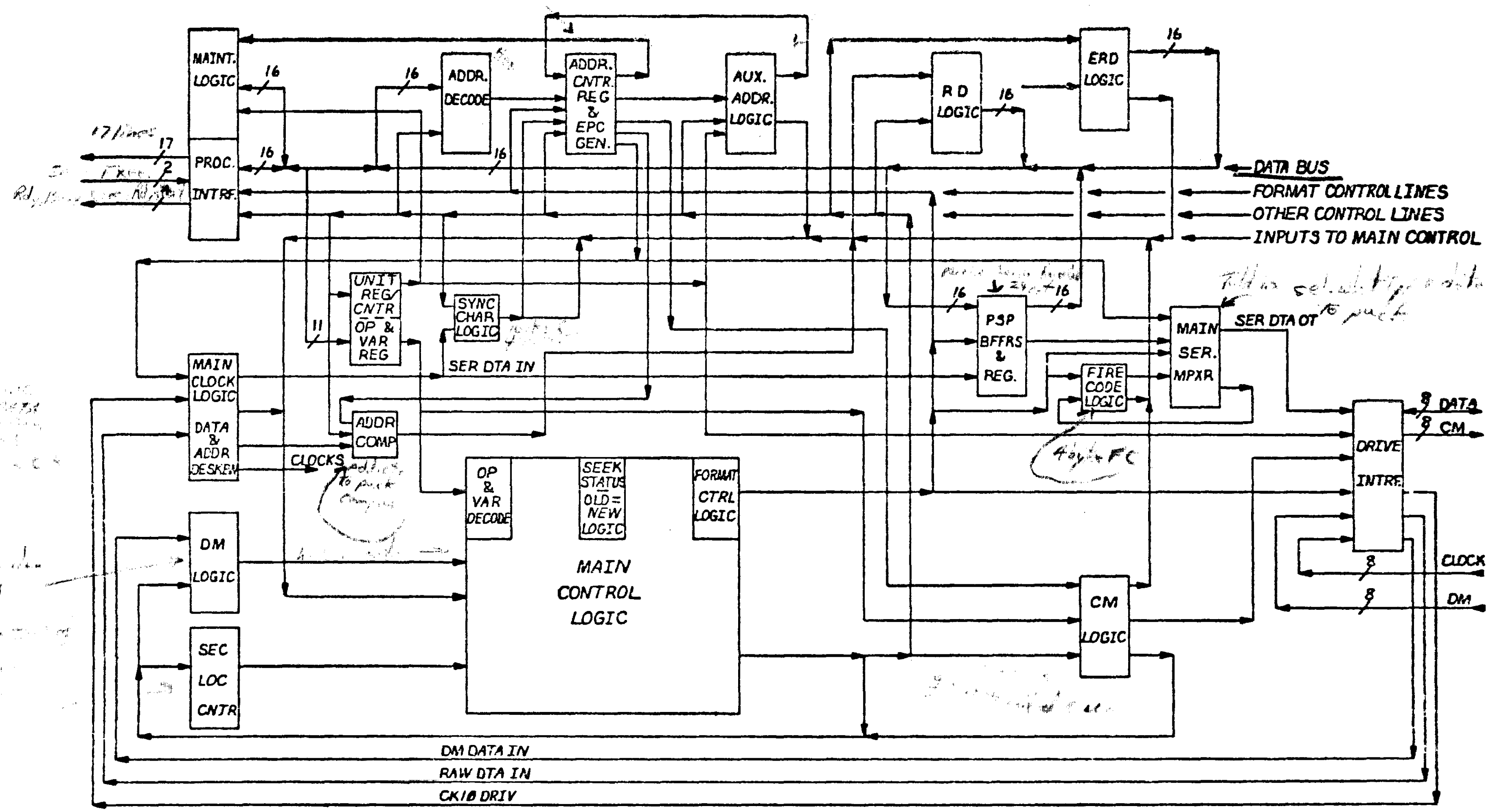

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Figure 1-3. Logic Overview

PROCESSOR INTERFACE

This block diagram illustrates the receivers and transmitters used for the actual communication between the DPEC and the DPC (see figure 1-4). The interface lines are parallel lines INFO 00 through INFO 15, DPC PAR, DPC SEL, DPC EXEC, DPC READY, DPC BUSY, RDY STATUS, and DPC CLOCK.

Data coming from the DPC to the DPEC is received by four DM8837 and three DM8096 circuits and used as part of the 16 lines driving a common internal bus. There are eight sources driving this bus. The internal bus lines are designated DATA 00 through DATA 15.

Two 74180 integrated circuits are used to check the parity on the data lines.

MAINTENANCE BLOCK

Each DPEC contains maintenance control facilities to simulate a DPC when the DPEC is in a local mode (see figure 1-5). All local operations on the DPEC are performed using the maintenance control panel mounted on the card in location F. All information is entered using 16 vertical pushbuttons. The switches are used to place information on the switch bus lines through the switch bus register. The display drivers are then used to illuminate the appropriate LEDs on the data display. The outputs from the switch bus register latches are also used as input information to the read/write memory integrated circuits that form the maintenance memory. The maintenance memory has a capacity of 256 bits, and is divided into 16 words of 16 bits each. Four memory address display LEDs and display drivers are used to indicate which one of the 16 maintenance memory words is being accessed.

When the DPEC is in local mode, 15 control switches are enabled. These switches are used to control the maintenance logic. (Refer to the 206 DPEC Function and Operation manual, form number 1084365, section 4.)

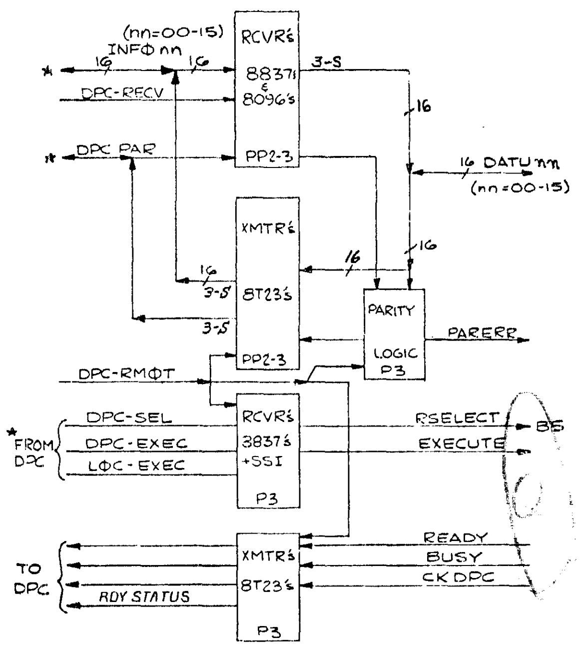

Figure 1-4. Processor Interface

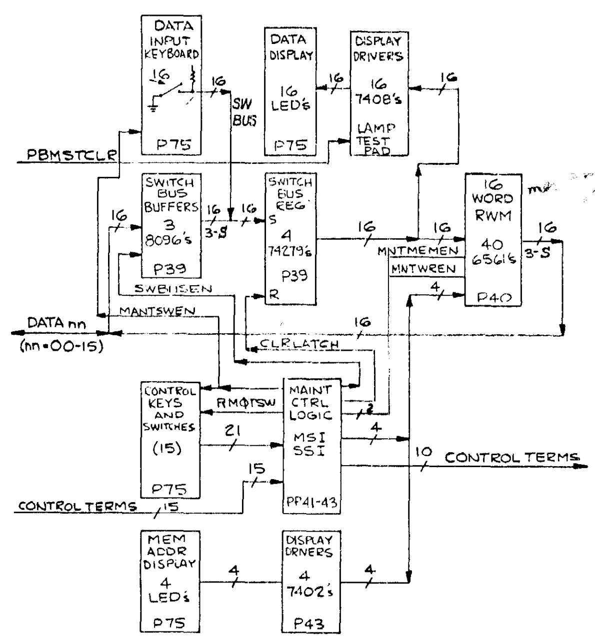

Figure 1-5. Maintenance Block

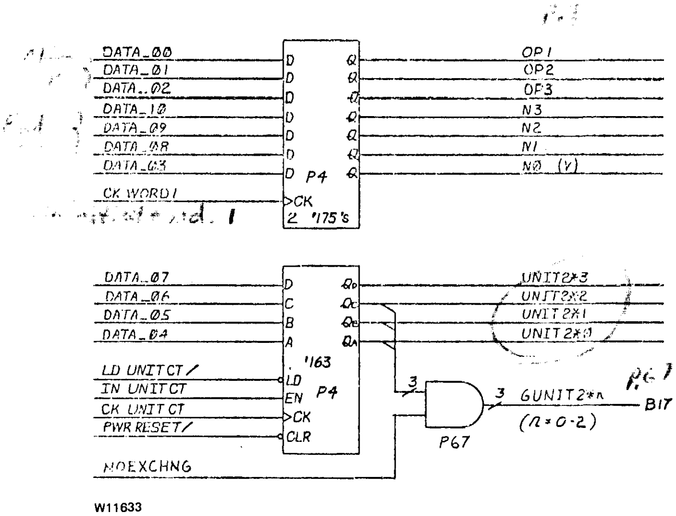

Figure 1-6. OP and VARIANT Reg, Unit Reg/Counter

OP AND VARIANT REG, UNIT REG/COUNTER

A series of D-type flip-flops are used to store data bus information for the appropriate OP code and VARIANT information which is available on the bus at clock word 1 time (CK WORD 1) (see figure 1-6).

Unit designation information (UNIT 2*n) is obtained from the internal data bus lines through a synchronous 4-bit counter. The outputs from the counter are unit designations 0 (FIRST SPINDLE) through unit designation 7 (EIGHTH SPINDLE).

ADDRESS DECODER

The 16 parallel lines of address data are loaded into three 74157 integrated circuits. The cylinder, head, and sector will be calculated by a division process (see figure 1-7). During the time that the control logic has the AD445 term TRUE, the address decode circuitry will be determining the cylinder address. During the time AD90 is TRUE, the address decode circuitry will be determining the proper head address. Any remainder, after the head division process has been performed, will be the sector number.

The five 74195 registers will provide the final cylinder, head, and sector information as decoded from the input data.

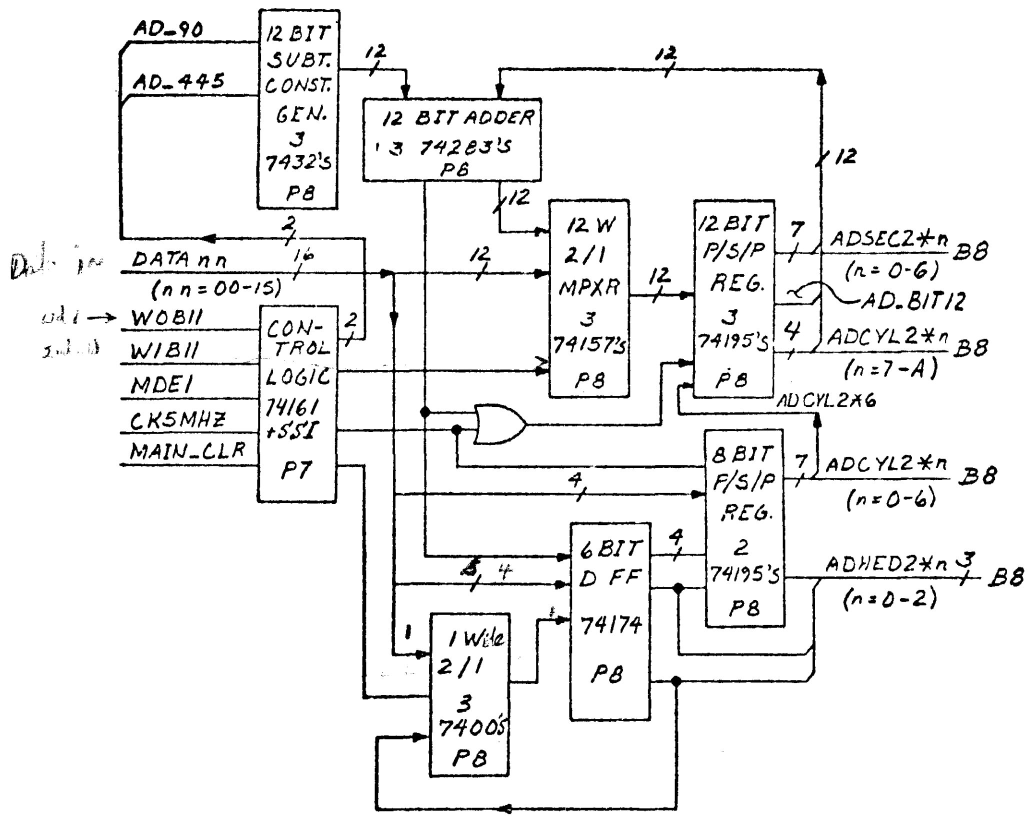

Figure 1-7. Address Decoder

ADDRESS COUNTER, REGISTER, AND EPC GENERATOR

The address counter is used primarily to isolate the address decoder output logic until it is ready to be used to supply serial header information to other sections of the DPEC (see figure 1-8).

A 24-bit parallel-to-serial register is used to convert the parallel address counter data (AC) to the serial header (SER HEDR) data.

The SER HEDR information is also used as an input to generate the address error protection code (EPC character). When the pack is initialized, the address EPC character will be written at the end of the address portion of each sector.

The seven word, three-to-one multiplexer (consisting of four 75153 integrated circuits) is used to provide the sector interlace that is used on the model 206 disk pack drive.

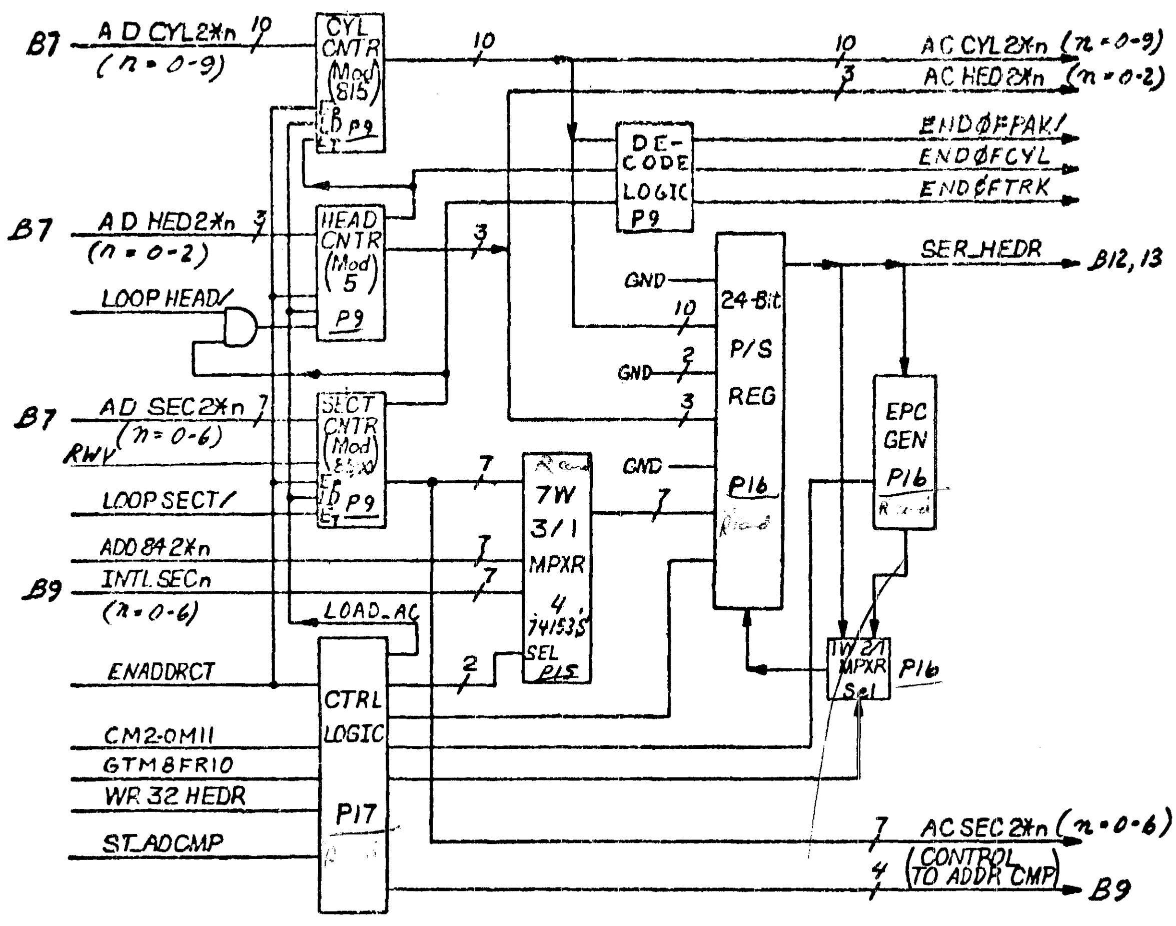

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Figure 1-8. Address Counter, Register and EPC Generator

AUXILIARY ADDRESS LOGIC AND ADDRESS COMPARE REGISTER

The 84-adder is used when addressing a spare sector on any track on head 4 (see figure 1-9). The value of the N variant (1-5) is added to the 84-adder to address the appropriate spare sector.

The sector address multiplexer is used to select either spare sector information (84-adder) or address counter sector information (AC SECT 2*n). The term SEL 84 ADR will determine which is used.

The output of the disk location counter (DISK LOC CNTR) will be sequential sector information. The INTERLEAVE LOGIC will be used primarily during the initialize operation. This logic will be used to provide the proper sequence of sectors required for the interleave pattern that must be written on the disk pack. The model 206 disk pack uses an interlaced format. Beginning at a reference point on the pack called index, the first four sectors will be numbered 45, 0, 46, and 1. The last four sectors, prior to returning to index, will be numbered 88, 43, 89, and 44. (Refer to the 206 DPEC Function and Operation manual, form number 1084365.)

When the desired sector address (AC SEC 2*n or 84 ADDER) and INTERLEAVE sector number are equal, the term DSK LOC EQ will be TRUE, indicating the desired sector on the pack has been located.

The disk location decoder is used to sample the disk location counter and produce the term LOC 89/ when the final sector count for a particular track is reached. (LOC 80-89/ will be TRUE when the last five sectors are being read. It is a test point, not a logic term.)

The address compare register is a series of four 7474 D flip-flops used to latch conditions of ADDRESS EQUAL, CYLINDER/HEAD EQUAL, SECTOR EQUAL, and EPC (ERROR PROTECTION CODE) EQUAL.

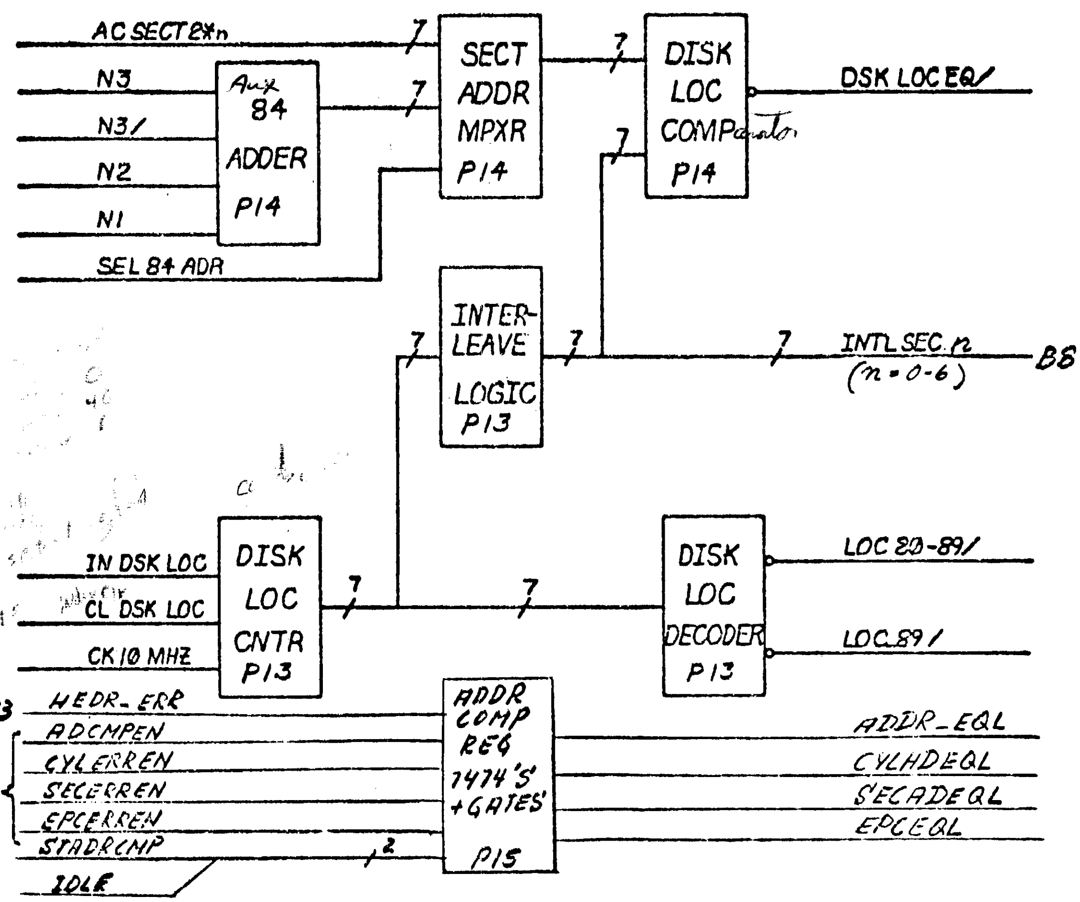

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Figure 1-9. Auxiliary Address Logic and Address Compare Register

PSP BUFFERS AND REGISTER

READ OPERATION

Serial data from the drive (SERDTAIN) is loaded into the 16-bit parallel-serial-parallel register at LDPSPREG time. This information is then available to the read buffer, which consists of four D-type flip-flops. The read buffer is a tri-state output device. The tri-states are high, low, or high impedance. The high impedance state is necessary to isolate the read buffer from the internal bus lines (see figure 1-10).

WRITE OPERATION

The 16-bit write buffer contains a series of D-type flip-flops used to transfer the internal data bus information into the parallel-serial-parallel register. The parallel data input is clocked into the write buffer at LDWRBFFR (load write buffer) time. The serial output from the parallel-serial-parallel register (PSPSEROT) will be clocked by the 10 megahertz clock (CK10MHz).

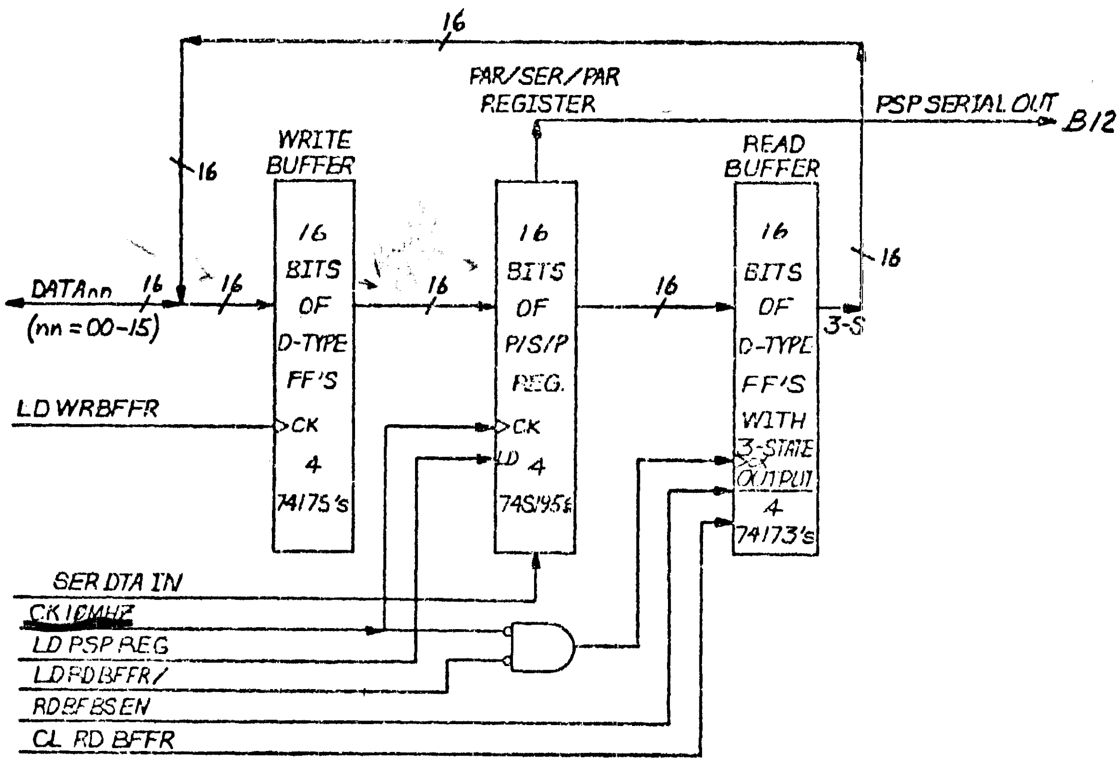

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Figure 1-10. PSP Buffers and Register

FIRE CODE LOGIC

32 bit

A series of three 8-bit parallel load shift registers, two quadruple D-type flip-flops, and four exclusive OR circuits form the Fire code generation circuit (see figure 1-11).

Serial data (FIRE IN) is used as the input to the Fire code generator to produce the actual Fire code characters that are written at the end of each sector of data on a pack.

Three flip-flops and an exclusive OR are used to check the Fire code that is read from a sector (SRDTDLYD) and it is compared with the FIRE OUT signal from the Fire code generator. If the two signals are the same, no Fire code error exists. If any of the 180 bytes are found to be incorrect, the Fire code characters will not compare, and the term FIRCDERR will be TRUE, indicating a Fire code error has been detected.

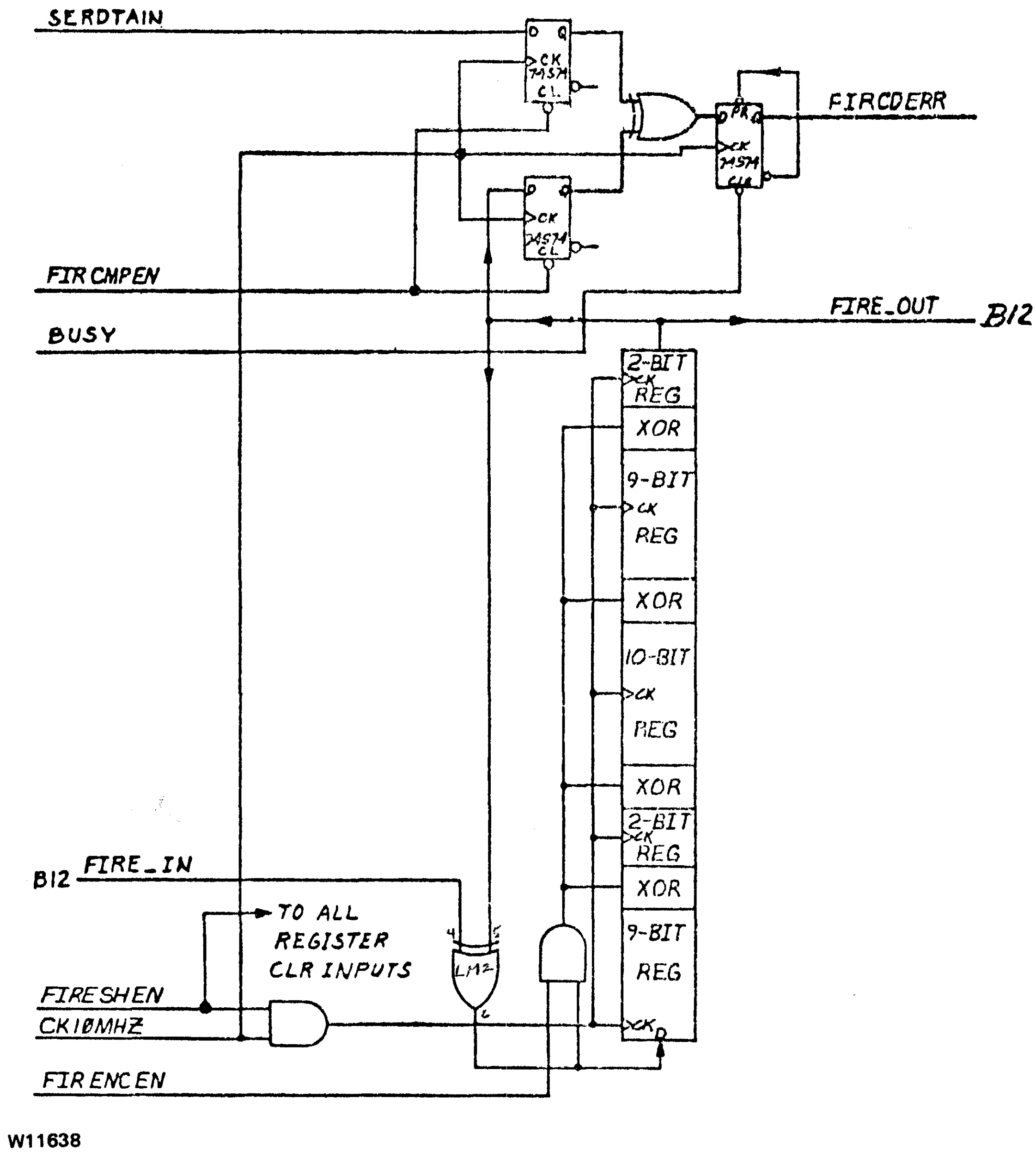


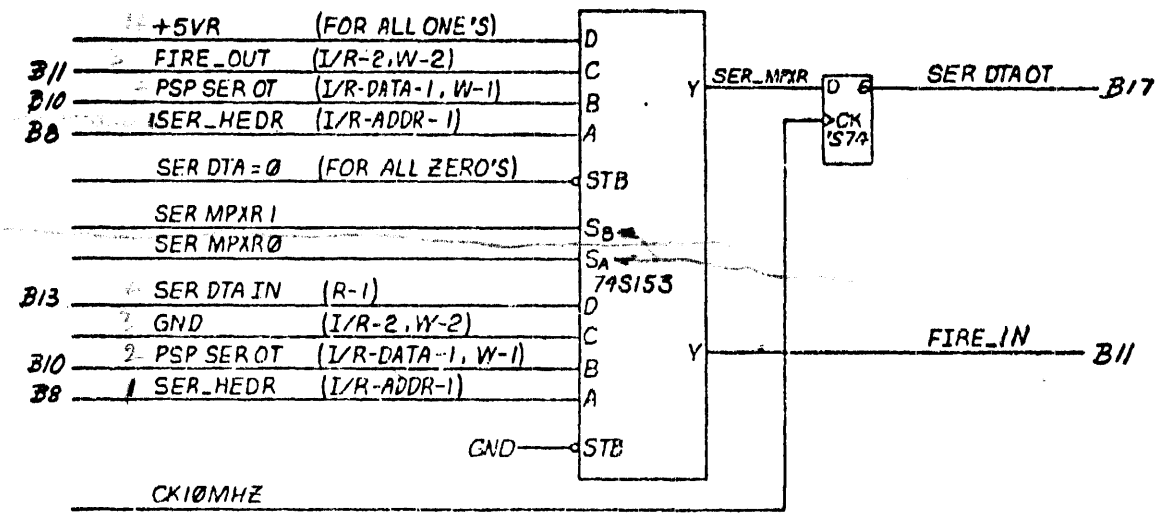
Figure 1-11. Fire Code Logic

MAIN SERIAL MULTIPLEXER

The outputs from the main serial multiplexer are FIRE IN and SER DTAOT (see figure 1-12). Depending on the combination of input strobe and select polarities, various input lines will be displayed at the outputs of the multiplexer.

The SER DTAOT output can contain SER HEDR, PSP SEROT, FIRE OUT, or an all "1's" pattern. The term SER DTA=0 is required as a strobe to obtain an output. The combination of SERMPXR0 and SERMPXR1 will determine which one of the inputs will be seen at the output. When SER DTA=0 is LOW, and both SERMPXR0 and SERMPXR1 are LOW, the SERDTAOT will contain SER HEDR information. When SERMPXR0 is HIGH and SERMPXR1 is LOW, PSPSEROT will be seen at the output. When both SERMPXR0 and SERMPXR1 are HIGH, all "1's" will be seen at the output because +5VR is applied to the 1C-3 input at RS0-3. The 10 megahertz clock is used to clock the SER DTAOT.

The FIRE IN output can contain SER HEDR, PSP SEROT, all "0's" or SRDTDLYD. The SERMPXR0 and SERMPXR1 terms will be used to select the inputs that will be used.



DEFINITIONS:

1. -1 REFERS TO THE 180-BYTE DATA FIELD TIME.
2. -2 REFERS TO THE 4-BYTE FIRE CODE TIME.
3. R REFERS TO READ AND VERIFY OPS.
4. W REFERS TO WRITE OP.
5. I/R - INITIALIZE AND RELOCATE OPS.
6. DATA AND ADDR SPECIFY WHAT IS TO BE WRITTEN.

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Figure 1-12. Main Serial Multiplexer

MAIN CLOCK AND DATA SYNC LOGIC

The basic clock frequency generated in the DPEC is 20 megahertz. This frequency is then divided by 2 to produce a symmetrical 10 megahertz clock (see figure 1-13).

The drive clock integrity logic is used to ensure that the 10 megahertz clock from the disk pack drive is within nominal tolerances. The terms DRIVCKOK and DRIVCKOK/will be monitored to verify that this condition is maintained.

Three pairs of matched 7440 buffers are used to distribute the 10 megahertz DPEC clock throughout the DPEC. Three 74S74 flip-flops and an exclusive OR are used to deskew the serial header compare information.

RAWDTAIN (data from the disk pack drive) is clocked and compared to clocked SER HEDR information by the 74S86 exclusive OR. If both RAWDTAIN and SER HEDR are in sequence, the term HDR ERR (header error) will be LOW, indicating that no error condition exists.

After being processed by two 74S74 flip-flops, RAWDTAIN becomes SERDTAIN. This processing is performed to eliminate any noise spikes on the data lines.

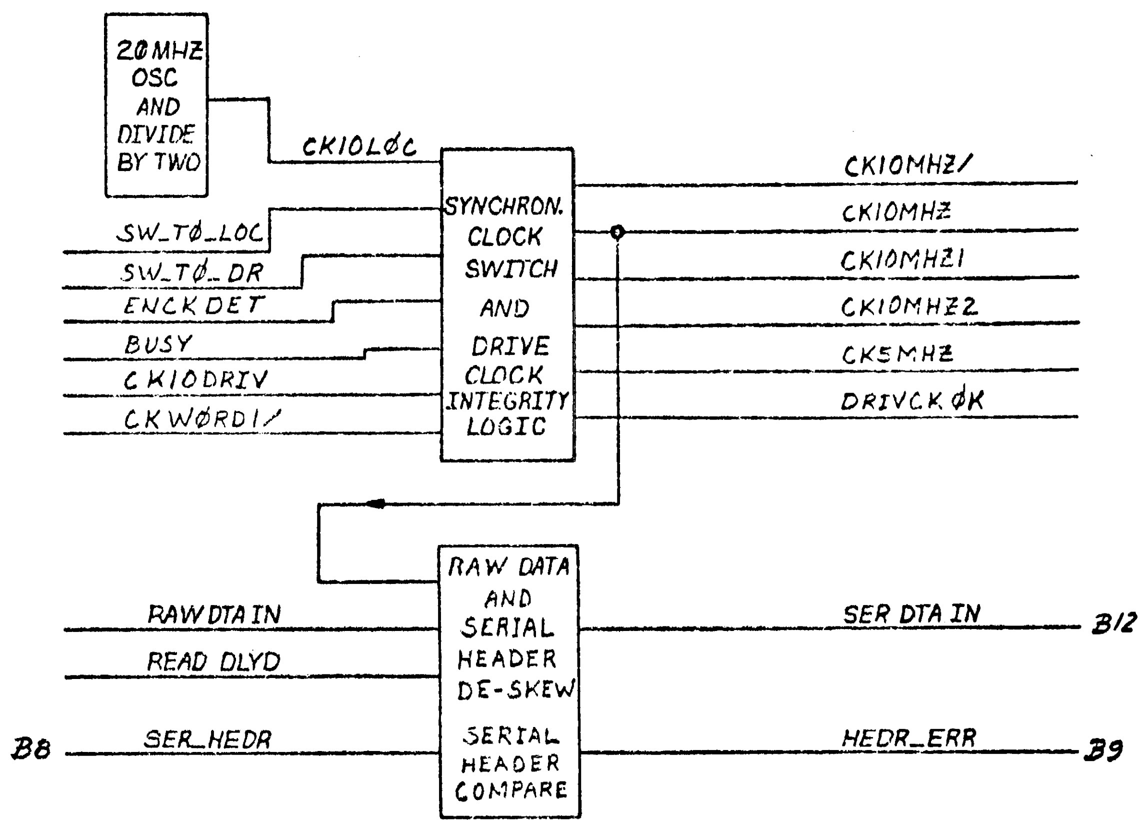

Figure 1-13. Main Clock and Data Sync Logic

SYNC CHAR LOGIC

A 74195 shift register integrated circuit is used to detect the 4-bit character preceding the address header (see figure 1-14). SERDTAIN is used as the JK input to the shift register and is clocked by the 10 megahertz clock. The term ENSNCDET (enable sync detect) will also be required to enable this circuit. Immediately after this condition takes place, STADRCMP (start address compare) will be TRUE. On the following clock pulse, ADSNCSTF will be TRUE, indicating that the address sync start flip-flop has been reset. (The note on the schematics and block diagrams "NOTE DOUBLE INVERSION" refers to the use of the reset state of a flip-flop, indicating a TRUE condition. A LOW TRUE into the flip-flop produces a LOW TRUE output from the set side of the flip-flop.)

The second time a 4-bit sync character is detected, the DTSNCSTF flip-flop will be set, indicating that the data sync character has been detected. STDAXFR will also go TRUE at this time, indicating the start of data transfer.

The term LDSECLOC/(load sector location counter, LOW TRUE) will be generated at the start address compare time.

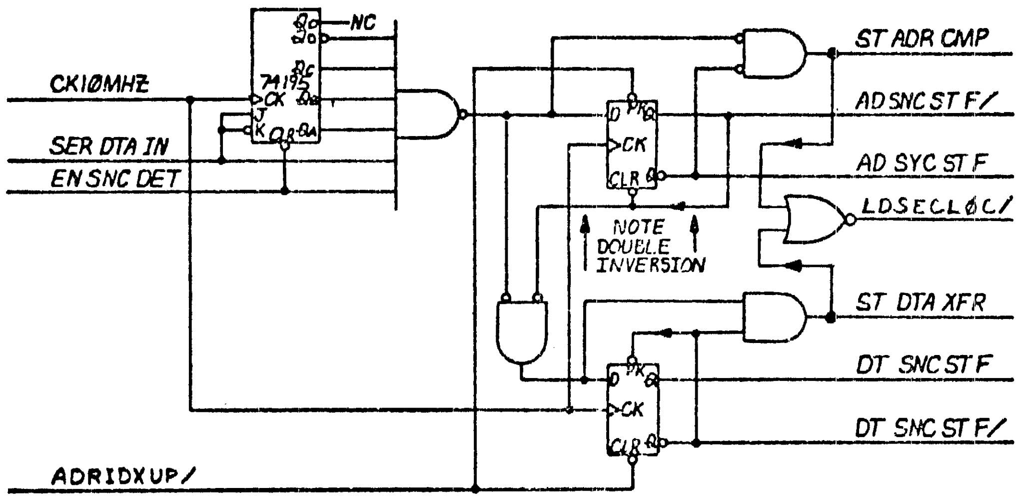

Figure 1-14. Sync Char Logic

CM LOGIC

The controller message (CM) data multiplexer and selectors (four 74153 integrated circuits) are used to select ACHED, ACCYL, PLO, and UNIT terms to produce eight CML lines (09-16). These eight lines will furnish one-third of the inputs to the 24-bit parallel-to-serial shift register (see figure 1-15).

The terms CM R/W/ (read), CM R/W (write), and CM ADD M/ (address mark) are used as inputs to the SHORT CM DATA multiplexer. These terms plus CMODE 01 and OFFSETEN will be used as inputs to the 74165 shift register to produce the first eight bits of the CM message.

The outputs from the CM data multiplexer (CML09-CML16) are used as inputs to the second eight bits of the 24-bit shift register.

The final eight bits of the CM message will be obtained from the last 8-bits data multiplexer. These bits will contain the high-order address counter cylinder information and enable write data.

The three shift registers are in series, and their output is used as the D input to the CM parity generator.

The CM BUF output is obtained from the deskew flip-flop. The D input to this flip-flop is either CM SEL, the 24-bit shift register output, or the parity generator output.

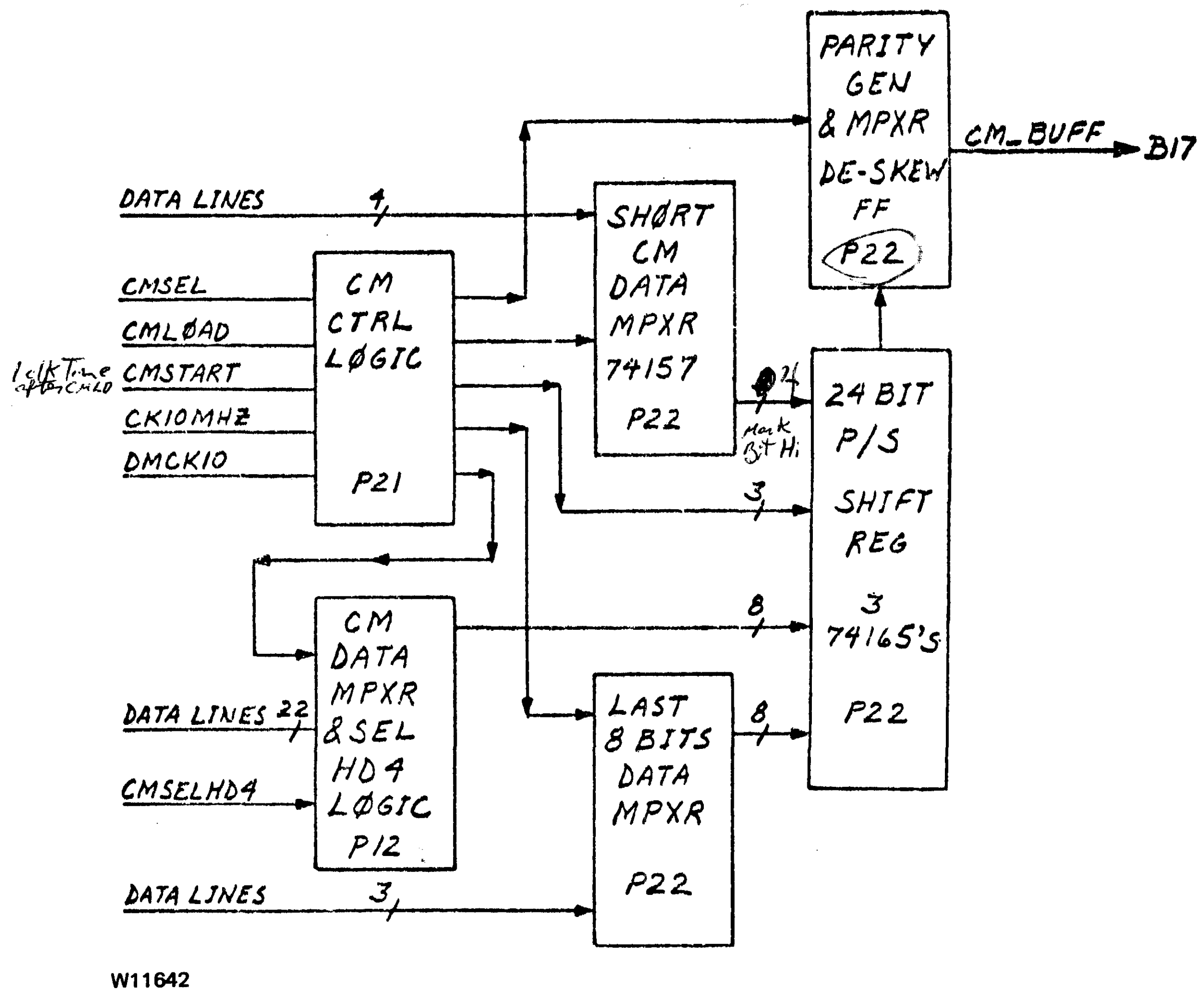

Figure 1-15. CM Logic

DM LOGIC

The 206 disk pack drive communicates with the 206 DPEC by sending a serial drive message (DM). A DM can only be sent while the controller has the drive selected (CM is HIGH). Unless this condition is met, the drive status is stacked in an unselected drive and sent when the drive is selected (see figure 1-16).

The eight DM lines coming from the maximum of eight 206 spindles are gated by the unit designation level on one of two drive interface cards. The term DMDATAIN is sent to the DM control logic and the deskew flip-flop network.

The deskew flip-flop produces terms called DMBUF and DMBUF/ that are at a 5 megahertz rate. These two terms will be used to gate the first seven bits of DM data and to gate the 24-bit serial-to-parallel register.

The first seven bits of the DM are stored in seven 74S109 JK flip-flops that are clocked by the term DM CLK.

The remaining 24 bits of the DM are obtained from three 74164 serial-to-parallel registers.

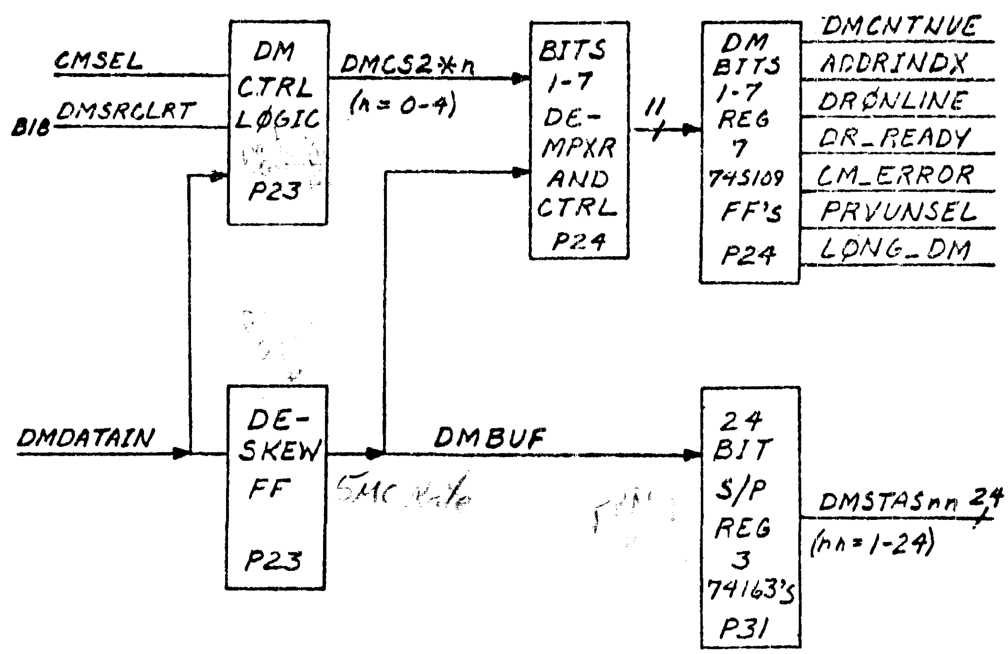

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Figure 1-16. DM Logic

DRIVE INTERFACE

Two interface cards are used to accommodate the eight spindles that can be used with the 206 DPEC. The S card is the drive-to-DPEC interface for spindles 0 through 3 and the R card, the interface between spindles 4 through 7 and the DPEC (see figure 1-17).

Four 75107 receiver integrated circuits are used on each card to receive the positive and negative data and clock information from the respective spindles. The data outputs from the receivers are used as inputs to a 74S51 multiplexer to produce RAWDTAIN. The clock outputs from the receivers are used as inputs to 74S151 multiplexers to produce the CK10DRV output, which is the 10 megahertz clock from the drive.

The GUNIT terms (2*0 through 2*2) are used to gate both the clock and data multiplexers.

DM data from the eight possible spindles is sent to four 8T24 receiver integrated circuits on the two interface cards. The outputs are the DRnDM terms, where n represents the drive number, from 0 through 7. All the DRnDM terms are used as inputs to a 74S251 multiplexer that uses the GUNIT terms to select the desired input. The output from the multiplexer is DMDATAIN.

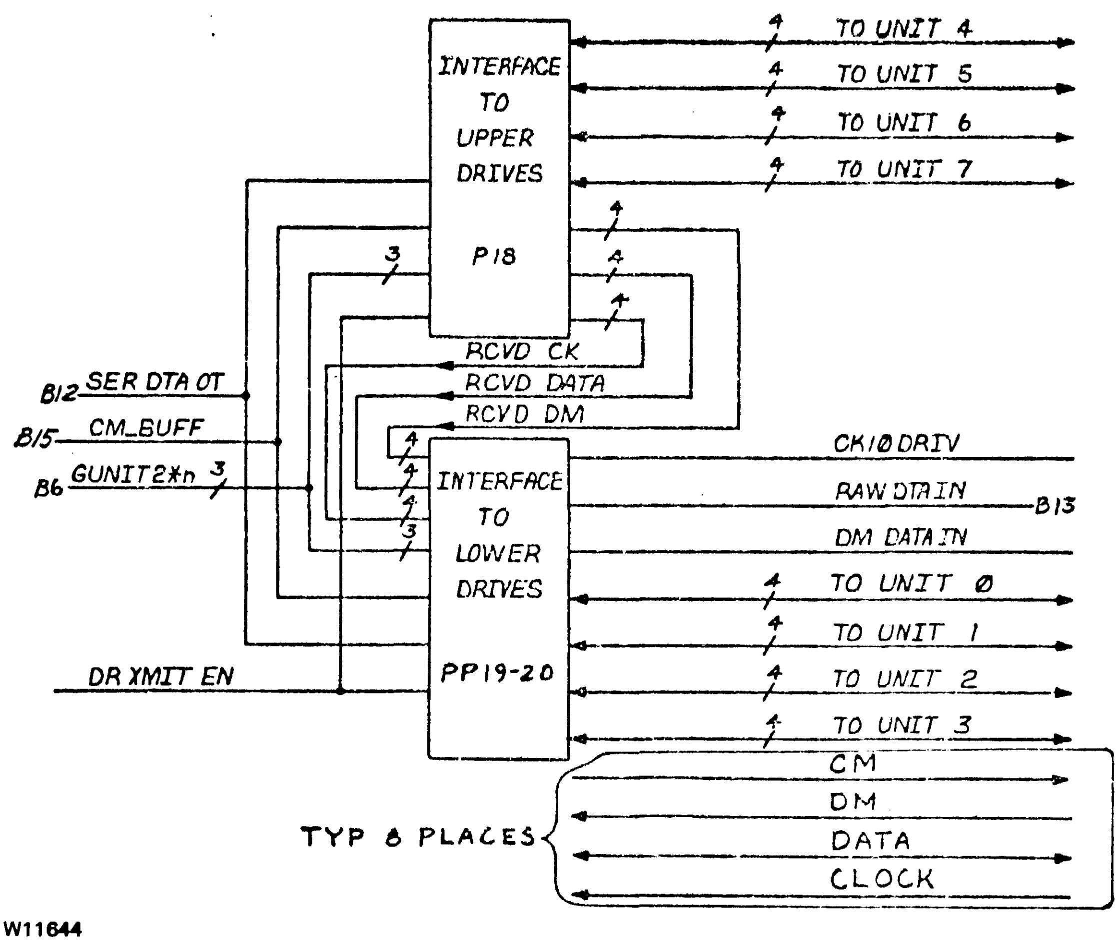

Figure 1-17. Drive Interface

RD AND ERD LOGIC

Three 8095 tri-state buffer integrated circuits are used to accept the 12 result descriptor (RD) status lines. The term RESDESEN/ (result descriptor enable) is used to enable the buffers. The outputs from these buffers are used as inputs to the internal DPEC data bus lines (see figure 1-18).

Seventeen 74173 D-type registers are used to store the 64 bits of ERD (extended result descriptor) information. The terms ERDFFB/ and ERDFFC/ are used for output controls of the register, and ERD XFEREN/ and STOBAD/ are used as the data and enable inputs.

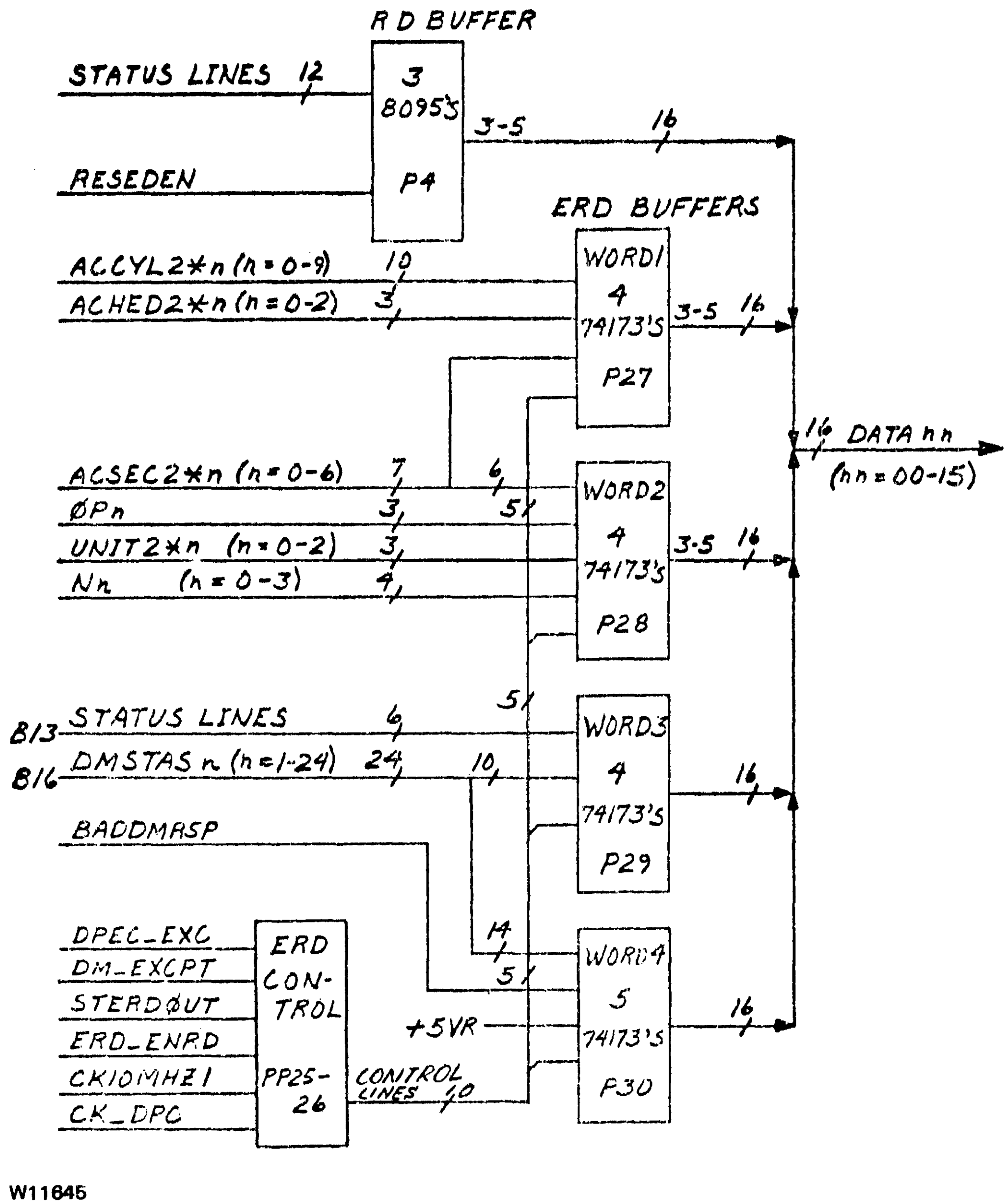

Figure 1-18. RD and ERD Logic

MAIN MODE LOGIC

The function of the "go to mode logic" is to generate a series of terms that will have a GOTOMDEn (where n is any mode from 1 to 15) format (see figure 1-19). Refer to figure 3-2 in the DPEC Function and Operation manual, form number 1084365, for additional information.

The priority encoder block includes two 74148 integrated circuits that form a 16-bit to 6-bit decoder.

The mode decoders consist of a pair of 74S138 3-to-8 decoders and several 74S04 inverters. The output from the mode decoders will be the actual mode lines MDE0 through MD15.

Mode decoders will be found on the L, K, and J cards.

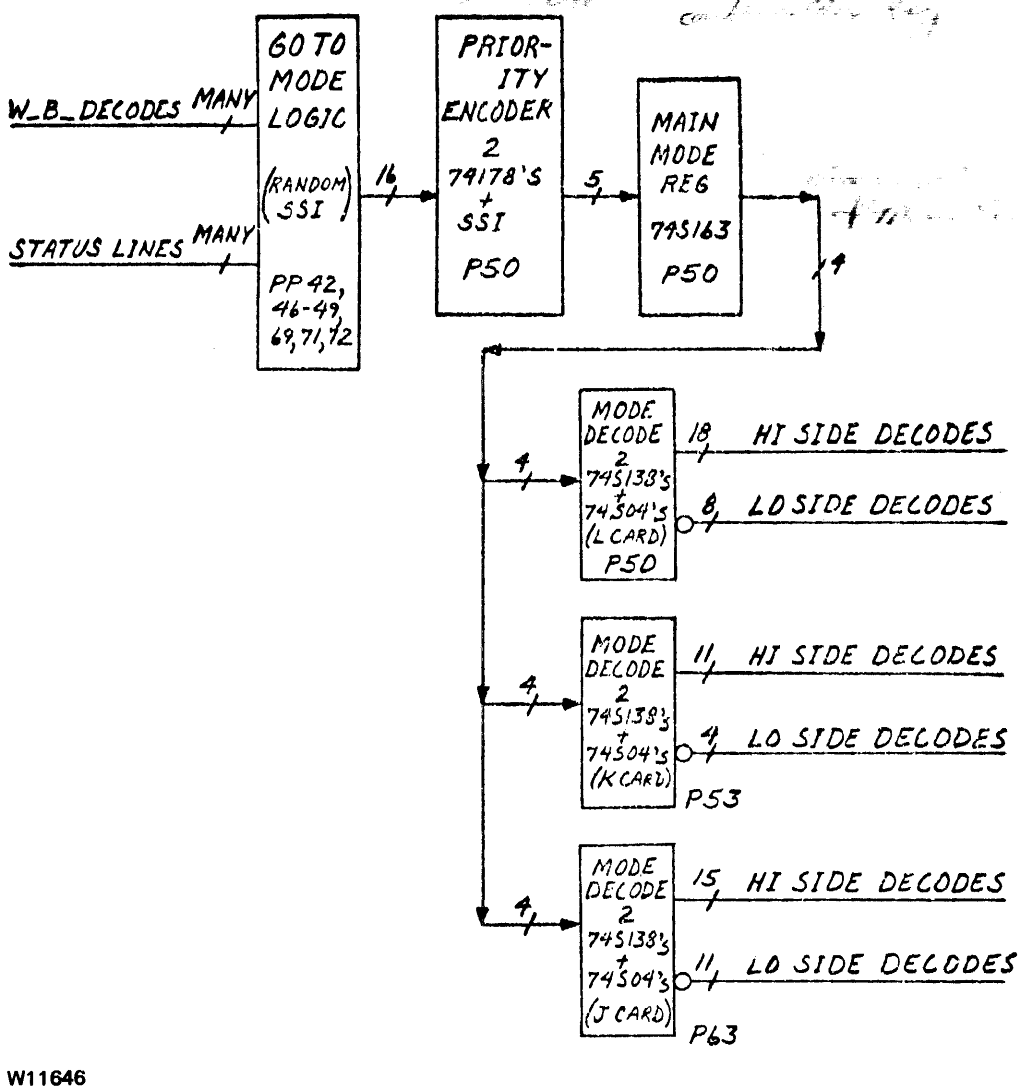

Figure 1-19. Main Mode Logic

SECTOR LOCATION COUNTER AND DECODER

The sector location counter is composed of three 74S163 counters (see figure 1-20).

The terms ADSNCSTF/ and ADSNCSTF (from the sync start logic) will be used to force word 5, bit 4 and word 17, bit 0 values into the counter. The first term will be TRUE at address sync time (W5B4), and the second term will be TRUE at data sync time (W17B0).

Two of the 74S163 integrated circuits are used to generate the word terms, and the third is used to generate the bit terms.

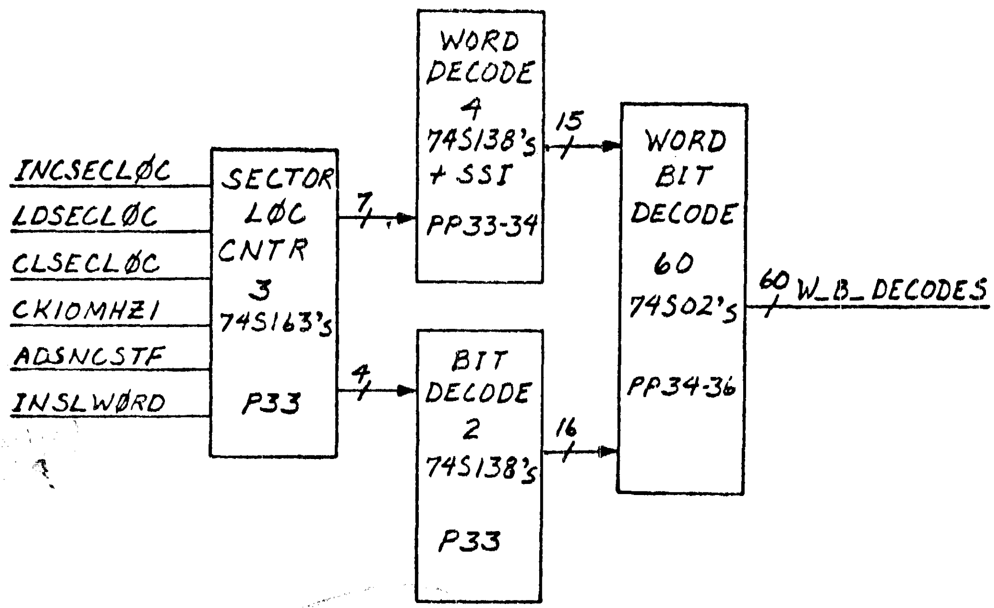

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Figure 1-20. Sector Location Counter and Decoder

SEEK STATUS LOGIC

The basic function of the seek status logic is to prevent the system from accessing a spindle that has not performed a data transfer. Once a seek operation has been initiated, the overlapping seek function allows the DPEC to satisfy other DPC service requests and not wait for the first seek operation to be completed (see figure 1-21).

When the seek status flip-flop is set for one spindle, the DPEC will not allow the DPC to address any other cylinder on that spindle until a data transfer has taken place. If the term old = new/ is LOW (TRUE), the operation is completed. If the term old = new/ is HIGH (FALSE), the operation is not performed and a positioner not settled result descriptor is reported.

The write enable logic is used to allow writing address information into the 6561 memory integrated circuits. The memory integrated circuits are used to store the old cylinder address. Eight exclusive OR circuits are used to compare the old cylinder address to the new cylinder address.

The write zero cylinder logic is used to clear, or set the memory integrated circuits to all "0's". This will be done at PWRRSYNC time, at RESTORE time, or if DRONLINE goes FALSE.

The memory clear counter (74163) is part of the write zero cylinder logic.

The 1-to-8 demultiplexer is used to furnish a clock pulse to the appropriate seek status flip-flop. At SETSKSTS time, all eight seek status flip-flops will have a TRUE at their D inputs. However, only the flip-flop that receives a clock pulse will be set.

Any time a unit is selected, the 8-to-1 multiplexer is interrogated to determine if the seek status flip-flop is set for that unit.

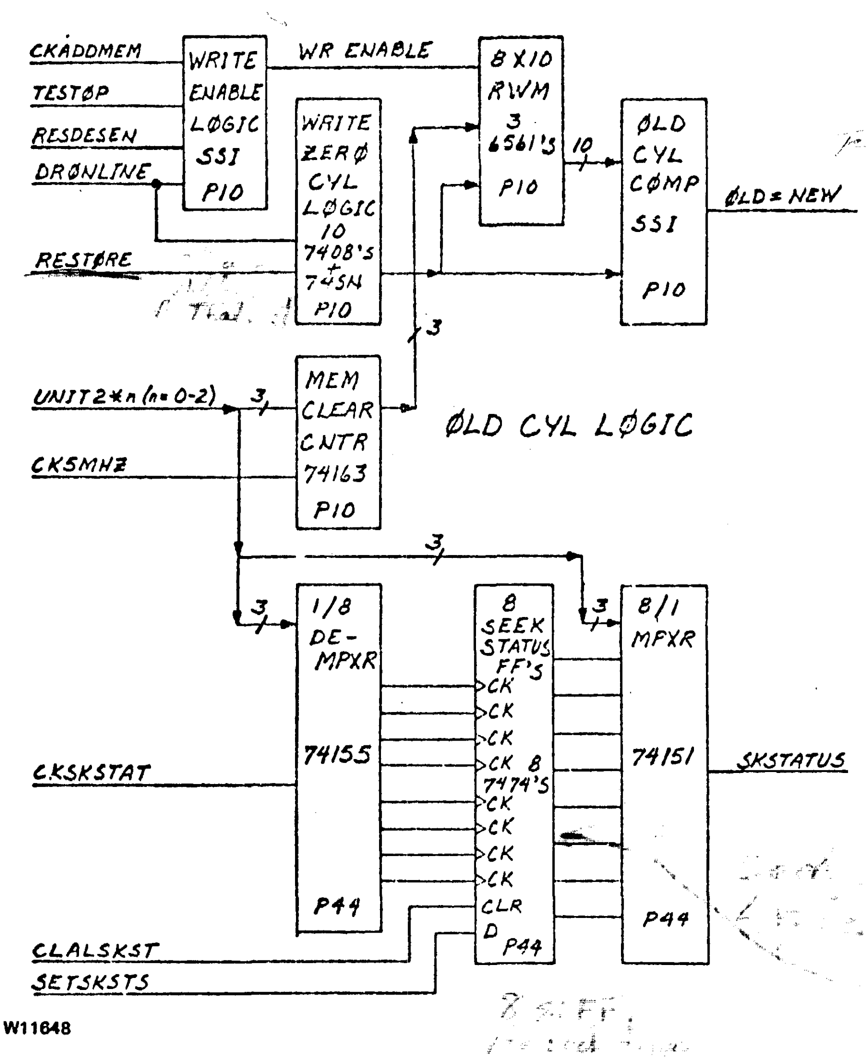

Figure 1-21. Seek Status Logic

TIMER LOGIC

The timer logic consists of three timer circuits (see figure 1-22). A 250 microsecond timer is used to detect the absence of address marks. A 25 millisecond timer is used to detect the absence of index marks. If either of these timers is allowed to time out, a fault condition exists. An 8-second timer is used during the power-on sequence, to ensure that not more than one spindle is allowed to power on at a time.

The three timer circuits consist of a basic timer or oscillator, a synchronous flip-flop, and a down edge detect flip-flop.

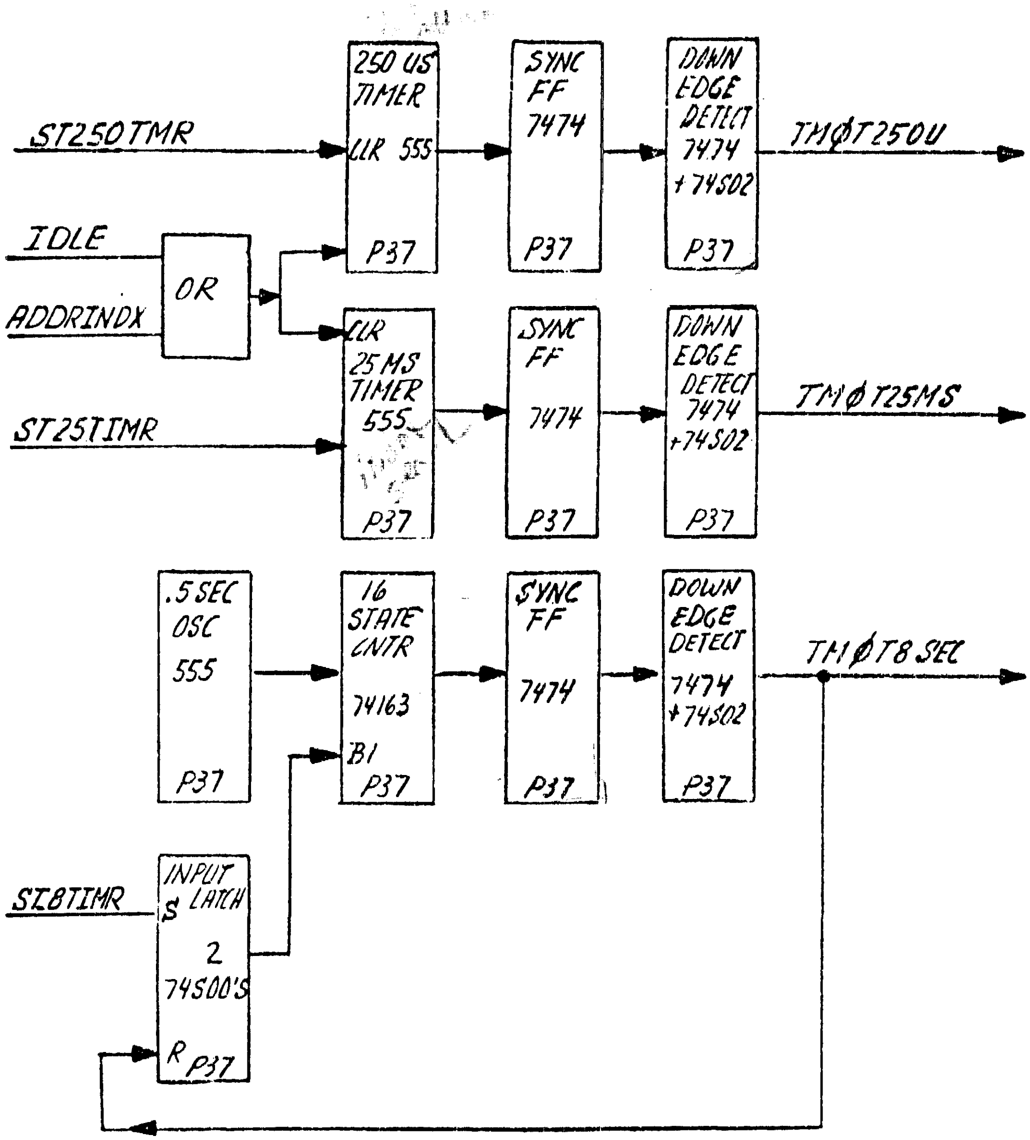

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Figure 1-22. Timer Logic

Controls All data flow in DPEC

FORMAT CONTROL LOGIC

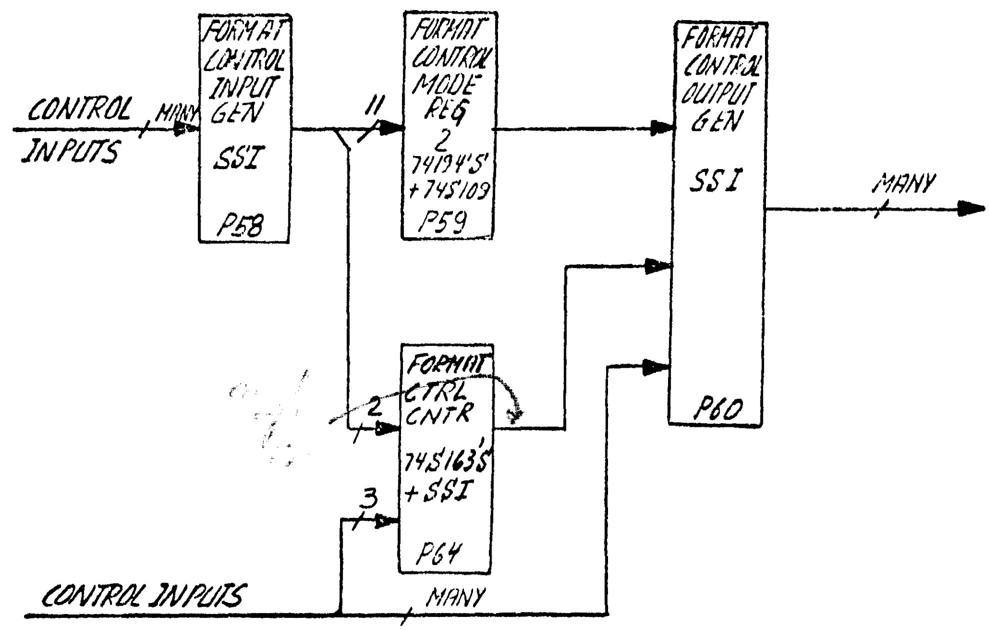
The format control input generator consists of a series of gates that convert mode and word/bit terms into format terms (see figure 1-23).

The format control mode registers are used to process the format terms that will be used by the data stream control logic.

The format control counter uses the FMWRONES/ term as a load term. The primary functions of the counter are to furnish the RAWCKDPC (raw clock to the DPC) and to load the read buffer in the parallel-serial-parallel register.

The format control output generator is used to convert mode and write terms to CM mode terms that will be used by the CM control logic.

Refer to figure 1-5 in the 206 DPEC Function and Operation manual, form number 1084365, for the illustration of the track format used with the 206 DPEC and the 206 disk pack drive.



W11650

Figure 1-23. Format Control Logic

Controlled by mode, word and bit times

CM MESSAGE

The controller message (CM) is used to allow the controller to select a drive, power on or power off the drive, position the head carriage to the proper cylinder, select a head, perform a read or write operation, make head offset and data strobe adjustments, and receive drive status. Figure 1-24 illustrates the controller messages, and table 1-1 lists the definitions of the CM bits.

The CM is either 6 bits or 24 bits long. The mark bit (bit 1) being LOW indicates the beginning of a message. The write, read, and address mark bits are HIGH active. The parity and continue bits are LOW active. The remaining bits in a 24-bit message are also LOW active.

a. 6-bit message. A read or write command has the continue bit (bit 6) set HIGH (inactive). When this bit is HIGH, no further message is to follow.

b. 24-bit message. When the continue bit is LOW (active), the CM will contain 24 bits. If bit 7 is LOW (active), the message is an address command. If bit 7 is HIGH (inactive), the message is a control command. Bit 8 is used to describe the information that will follow. Each bit has a period of two clock pulses.

Table 1-2 contains the bit configurations for the various CM messages within the DPEC.

Column 1 contains the CM number, column 2 the CM message name, and the output bit configuration is shown in column 3. The legend at the bottom of the table lists the active state of the bits used. Unless otherwise stated, the bits shown in table 1-2 are LOW active levels.

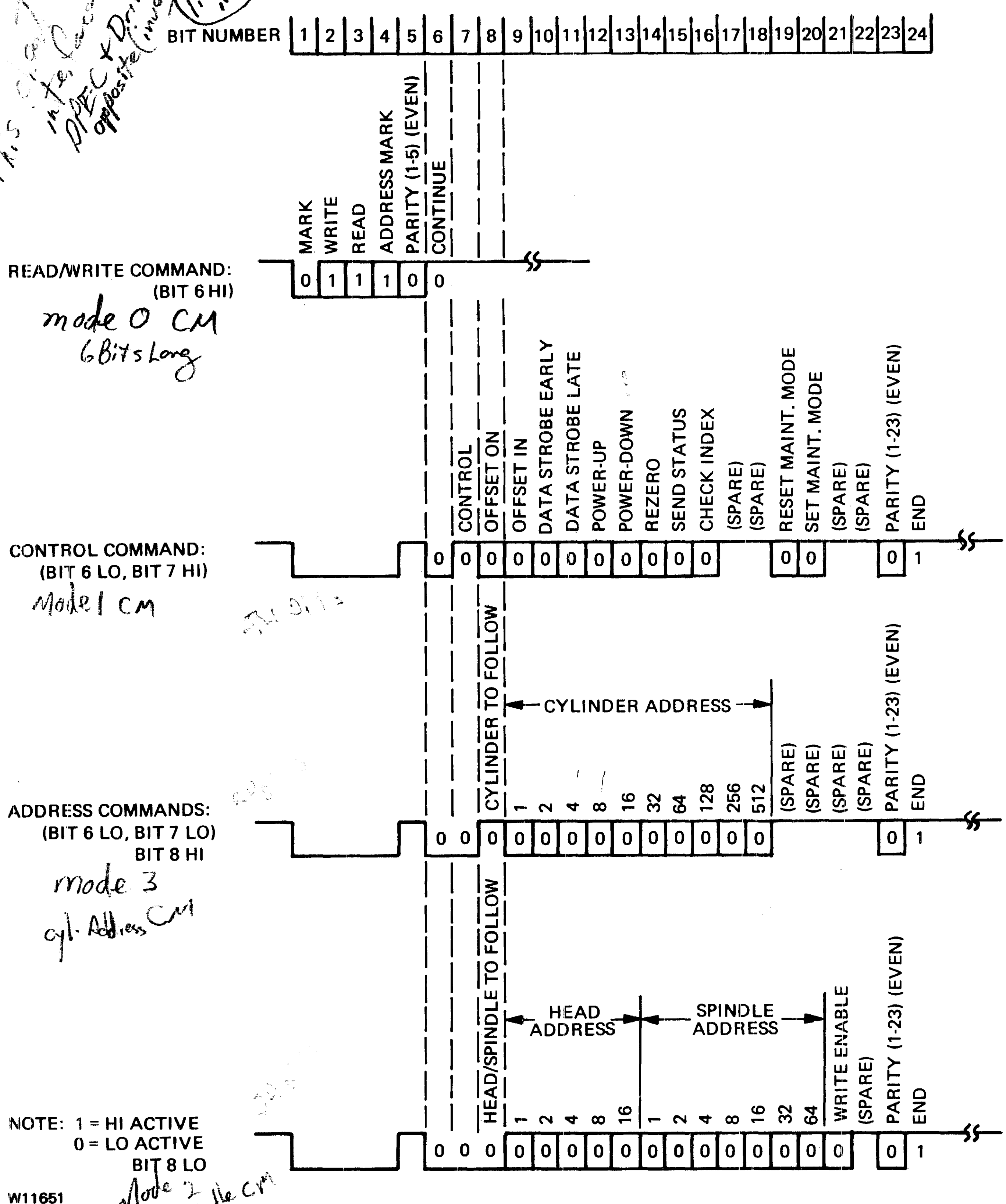


Figure 1-24. Controller Message (CM) to Drive

10 meg. bit serially

INVERTED

Table 1-1. Controller Message Bits

Bit	Name	Function
1	Mark	When LOW, indicates the beginning of a message.
2	Write	When HIGH, indicates a write mode. Write starts if no errors were detected when bit 6 is received and write enable (bit 21) is previously set. When LOW, write stops immediately.
3	Read	When HIGH, indicates a read mode. Read starts if no errors were detected when bit 6 is received.
4	Address Mark	When HIGH, indicates a search for address mark (AM) if in read mode or write AM if in the write mode. Action starts if no errors are detected when bit 6 is received. Search for AM is reset by AM detection. Write AM is reset after writing three bytes of no flux transitions.
5	Parity	Provides an even number of LOW states for bits 1 through 4. If a parity error exists, operations indicated by the previous bits are processed. An 8-bit DM with bit 6 active (parity error) is generated.
6	Continue	When LOW, indicates the message continues and the CM is 24 bits long. If LOW in a read or write mode, an error exists, causing the operation to be terminated and generates a DM error message.
7	Control	When HIGH, indicates bits 8 through 24 are control bits. When LOW, the state of bit 8 determines the definition of bits 9 through 24.

NOTE

When bit 7 is HIGH, the following definitions apply to bits 8 through 24.

Bit	Name	Function
8	Offset On	When LOW, indicates the head is to be offset during a read mode. The state of bit 9 will determine the direction of the offset.
9	Offset In	When LOW, indicates the offset is in toward the spindle. Action starts at bit 24.
10	Data Strobe Early	When LOW, indicates read data is detected using the early strobe. Used to recover data errors. Action starts at bit 24.
11	Data Strobe Late	When LOW, indicates read data is detected using the early strobe. Used to recover data errors. Action starts at bit 24.
12	Power On	When LOW, initiates a drive power on. Action starts at bit 24.
13	Power Off	When LOW, initiates a drive to power off. Action starts at bit 24.
14	Rezero	When LOW, initiates a head retraction into the outer guard band, on the pack and forward to cylinder zero. Action starts at bit 24.
15	Send Status	When LOW, sets the drive exception bit and initiates a 32-bit status drive message (DM). Action starts at bit 24.
16	Check Index	When LOW, specifies a drive message will be sent at the next index mark detection. Index is not normally reported. Any drive error will stop the index mark search. Action starts at bit 24.
17	Spare	
18	Spare	
19	Reset Maint Mode	When LOW, the maintenance mode is reset.
20	Set Maint Mode	When LOW, the maintenance mode is set.
21	Spare	
22	Spare	
23	Parity	Provides an even number of LOW states for bits 1 through 23.
24	End	End of message. It must be HIGH. If LOW, the operations specified by the previous bits will not start.

NOTE

When bit 7 is LOW, and bit 8 is HIGH, the following definitions apply to bits 8 through 24.

Bit	Name	Function
8		When HIGH, indicates that the cylinder address will follow.

Table 1-1. Controller Message Bits (Cont)

Bit	Name	Function
9-18	Cylinder Address information	
19-22	Spare	
23	Parity	Provides an even number of LOW states for bits 1 through 22.
24	End	Same as above.

NOTE

When bit 7 and bit 8 are LOW, the following definitions apply to bits 8 through 24.

Bit	Name	Function
8	Address Flag	When LOW, indicates head or spindle address will follow.
9-13	Address	Head address, LSB to MSB.
14-20	Address	Spindle address, LSB to MSB.
21	Write Status	When LOW, sets write enable.

before interface in DPEC   oposite from other chart

Table 1-2. 206 DPEC Control Messages

idle state

CM No.	Name	Output Bits							Inputs				
		0	1234	5678	9112	3456	7892	1234	M	RAE	DIEL	UD	RSIW
			MWRA	PE				PE					
CM #1-0	NO OFFSET/PLO	L	HHHH	LHLL	LLLL	LLLL	LLLL	LLHL	1	XHH	LLLL	LL	LLLL
CM #1-1	OFFSET/PLO	L	HHHH	LHL*	***L	LLLL	LLLL	LL*L	1	XHH	****	LL	LLLL
CM #1-2	POWER UP	L	HHHH	LHLL	LLLH	LLLL	LLLL	LLLL	1	XHH	LLLL	HL	LLLL
CM #1-3	POWER DOWN	L	HHHH	LHLL	LLLL	HLLL	LLLL	LLLL	1	XHH	LLLL	LH	LLLL
CM #1-4	RESTORE-SEND STTS	L	HHHH	LHLL	LLLL	LHHL	LLLL	LLLL	1	XHH	LLLL	LL	HHLL
CM #1-5	SEND STATUS	L	HHHH	LHLL	LLLL	LLHL	LLLL	LLLL	1	XHH	LLLL	LL	LHLL
CM #1-6	FIND INDEX MARK	L	HHHH	LHLL	LLLL	LLLH	LLLL	LLLL	1	XHH	LLLL	LL	LLHL
CM #2-0	WR EN HEAD SPNDL	L	HHHH	LHHH				HL*L	2	XHH	LLLL	LL	LLLH
CM #2-1	HEAD SPINDLE ONLY	L	HHHH	LHHH				LL*L	2	XHH	LLLL	LL	LLLL
CM #3	CYLINDER	L	HHHH	LHHL			LL	LL*L	3	XHH	LLLL	LL	LLLL
CM #4	READ DATA	L	HHLH	HL					0	HHH	LLLL	LL	LLLL
CM #5	WRITE DATA	L	HLHH	HL					0	LHH	LLLL	LL	LLLL
CM #6	READ ADDR MARK	L	HHLL	LL					0	HLH	LLLL	LL	LLLL
CM #7	WRITE ADDR MARK	L	HLHL	LL					0	LLH	LLLL	LL	LLLL
CM #8	GO IDLE	L	HHHH	LL					0	XHL	LLLL	LL	LLLL
CM #9	SELECT DRIVE	HHHH	HLLL	LL						CM SEL =		HI	
CM #10	DE-SELECT DRIVE	L	HHHH	HH						CM SEL =		L0	

LEGEND

INPUTS:	M	=	MODE	0 = SHORT CM. 1 = CONTROL CM	CMODE2*0
				2 = HEAD CM. 3 = CYLINDER CM	CMODE2*1
	R	=	READ	(READ=H, WRITE=L)	CM_R/W/
	A	=	ADDRESS MARK	– LO ACTIVE	CM_ADD M/
	E	=	GO IDLE CM	– LO ACTIVE	CMGO IDLE/
	O	=	OFFSET ON	– HI ACTIVE	OFFSETON
	I	=	OFFSET IN	– HI ACTIVE	OFFSETIN
	E	=	PLO EARLY	– HI ACTIVE	PLOEARLY
	L	=	PLO LATE	– HI ACTIVE	PLO_LATE
	U	=	POWER UP	– HI ACTIVE	POWER_UP
	D	=	POWER DOWN	– HI ACTIVE	POWER_DN
	R	=	RESTORE	– HI ACTIVE	RESTORE
	S	=	SEND STATUS	– HI ACTIVE	SEND STS
	I	=	FIND INDEX MARK	– HI ACTIVE	INDXSRCH
	W	=	REQUEST WRITE ENABLE	HI ACTIVE	ENABL_WR

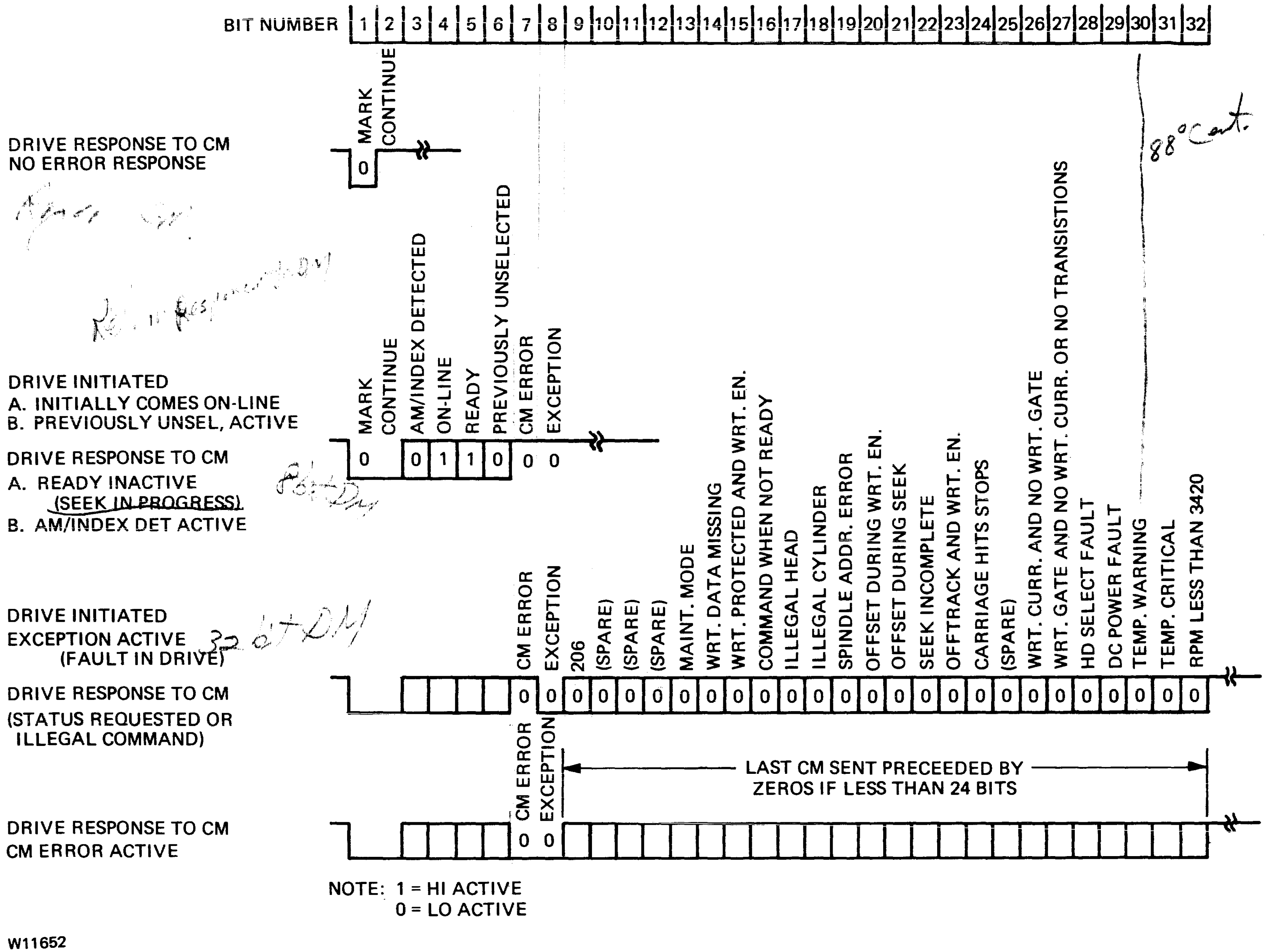


Figure 1-25. Drive Message (DM) from Drive

DM MESSAGE

The drive communicates with the DPEC by sending a serial drive message (DM). The DM can be sent only while the DPEC has the drive selected (CM is HIGH). The drive status is stacked with an unselected drive and sent with a selected drive. The DM message can be 1 bit, 8 bits, or 32 bits in length. Each bit has a period of two clock pulses. Figure 1-25 illustrates the drive messages. (Refer to table 1-3 for bit functions.)

a. 1-bit DM. The 1-bit DM consists of only a mark bit. For each CM sent by the DPEC, the drive should respond with the 1-bit DM, if no errors exist.

b. 8-bit DM. If the drive is not selected, an 8-bit DM is stacked in the drive when the drive initially is placed on-line. When selected, the drive sends an 8-bit DM indicating on-line, ready, and previously unselected. If the CM is held LOW, the drive is deselected and the drive status is stacked. When again selected, the drive sends an 8-bit DM indicating on-line, ready, and previously unselected.

An 8-bit DM is also sent in response to a CM. When a CM commands a seek to a new cylinder, the drive responds immediately with an 8-bit DM, with ready inactive, and starts the seek. When the seek has been successfully completed, the drive responds with a 1-bit DM.

Table 1-3. Drive Message Bits

Bit	Name	Function
1	Mark	When LOW, indicates beginning of the message. A no error response to a CM consists of bit 1 LOW and bit 2 HIGH.
2	Continue	When HIGH, indicates that the last controller message was received correctly, the drive is READY, and there is no EXCEPTION.
		When LOW, indicates continuation of the message.
3	AM/Index	When LOW, indicates an Address Mark (AM) has been detected in response to an AM search or that an Index Mark has been detected in response to an Index Mark search. A DM is generated when bit 3 goes LOW.
4	OnLine	When HIGH, indicates the spindle is up to speed and ready for operation.
5	Ready	When HIGH, indicates the spindle in ONLINE and the heads are not seeking to a new cylinder. When a seek is completed, READY goes HIGH and a DM is generated.
6	Previously Unselected	When LOW, indicates bits 1 through 5 of the last CM were all LOW (bad parity). This could be the result of deselecting a drive (CM goes LOW). When a drive is reselected (CM goes HIGH), a DM is generated with bit 6 LOW.
7	CM Error	When LOW, indicates an input error (parity error or control bit conflicts) other than the one specified by bit 6. Presence of this bit will initiate the generation of a drive message. When this bit is LOW, bits 9-32 of the DM will contain the last CM sent to the drive (preceded by zeros if less than 24-bit message).
8	Exception	When LOW, indicates that a drive exception condition exists or that a read status command was sent to the drive in the last CM. Presence of this bit will initiate generation of a drive message. When this bit is LOW and bit 7 is HIGH, bits 9-32 of the DM will contain status register information from the drive.
9-32	Status	These bits will contain status information if bit 8 is LOW and bit 7 is HIGH, or the previous controller message if bit 7 is LOW.
9	Unit ID	When LOW, indicates type 206 spindle.
10-12	Spares	
13	Maintenance Mode	When LOW, indicates maintenance mode.
14	Write Data Missing	When LOW, indicates no transitions during a write mode. At the end of the write mode, a DM is generated with status bit 14 LOW.

Table 1-3. Drive Message Bits (Cont)

Bit	Name	Function
15	Write Protect and Write Enable	When LOW, indicates WRITE ENABLE bit (CM bit 21) was received while WRITE ENABLE switch was off. Bit 15 also goes LOW if WRITE command (CM bit 2) is received while WRITE ENABLE switch is off or WRITE ENABLE bit is inactive.
16	Command When Not READY	When LOW, indicates cylinder address CM was sent while drive was not READY.
17	Illegal Head	When LOW, indicates head address is greater than 4.
18	Illegal Cylinder	When LOW, indicates cylinder address is greater than 814.
19	Spindle Address Error	When LOW, indicates drive spindle address does not agree with CM spindle address.
20	Offset During Write Enable	When LOW, indicates an offset command while in the WRITE ENABLE state.
21	Offset During Seek	When LOW, indicates OFFSET active when a cylinder address CM is received.
22	Seek Incomplete	When LOW, indicates the heads were not settled within 700 milliseconds after seek started.
23	Offtrack and Write Enable	When LOW, indicates the servo is offtrack while the WRITE ENABLE state is active.
24	Carriage Hit Forward or Rear Stop	When LOW, indicates heads have hit forward or rear endstop and caused an emergency head retract and power off. To reset and power on, the drive RUN/STOP switch must be turned off and then back on.
25	Spare	
26	Write Current and No Write Gate	When LOW, indicates write current sensed without a write command.
27	Write Gate and No Write Current	When LOW, indicates write command and no write current sensed or write command and no data transitions sensed to the write driver.
28	Head Select Fault	When LOW, indicates no heads or more than one head selected while reading or writing.
29	DC Power Fault	When LOW, indicates servo voltage or -12 Vdc low or missing.
30	Temperature Warning	When LOW, indicates temperature has exceeded normal levels.
31	Temperature Critical	When LOW, indicates temperature has exceeded safe operating limits.
32	RPM Less Than 3420	When LOW, indicates the spindle speed is less than 3420 rpm.

DPEC-DPC CONTROL AND STATUS INTERFACE LINES

The following are terms generated by the disk pack control (DPC) and sent to the DPEC, along with the terms generated by the DPEC in response to those terms.

Term	Description
SELECT (#H) (DPC to DPEC)	A TRUE level enables the initiate phase for the DPEC. The INFOnn lines must be stable at the time the SELECT level goes TRUE. A SELECT FALSE before word 91 indicates termination by the disk pack control at completion of the coincident sector. A SELECT FALSE after word 92 indicates to continue the operation for one more sector and then terminate the operation. If the DPEC terminates the operation, the DPC will drop (SELECT FALSE) the select line within 1±0.5 microsecond.
READY (#R) (DPEC to DPC)	A TRUE level indicates that the DPEC is ready to receive the second initiate word. READY goes TRUE 200±100 nanoseconds after the leading edge of the first initiate clock sent to the DPC. Refer to SELECT, READY, and BUSY status in table 1-4.
BUSY ($R) (DPEC to DPC)	A TRUE level indicates that the DPEC has received the second initiate word and is conditioned for normal operation. BUSY goes TRUE 200±100 nanoseconds after the leading edge of the second initiate clock. Refer to SELECT, READY, and BUSY status in table 1-4.
EXECUTE ($H) (DPC to DPEC)	A TRUE indicates that the DPC is ready to send data or receive data. FALSE indicates that the DPC is not ready to send or receive data. For slip mode, the EXECUTE line goes FALSE before word 91 of the data field to indicate to the DPEC that it is to go into a slip holding mode during a multisector operation.
CLOCK ($U)	The width of the TRUE level is 300 nanoseconds at the transfer rate. The minimum period at transfer rate is 1.6 microseconds. The clock level informs the DPC that, in a write mode of operation, the INFOnn lines information was accepted by the DPEC. In the read mode, the CLOCK levels indicate that the INFOnn lines are stable for at least 150 nanoseconds and remain stable for the CLOCK period.
PARITY ($K) (Bi-Directional)	Parity is TRUE when the modulo 2 sum of the INFOnn lines is equal to 0; otherwise, parity is FALSE (odd parity).
READY STATUS (#N) (DPEC to DPC)	When TRUE, indicates that the DPEC is powered on, in remote, and ready to be selected. When FALSE, indicates that the power is off, or the DPEC is in a local mode of operation.
INFO 00 ($W)	Least significant bit (LSB).
INFO 01 ($N)	
INFO 02 ($T)	
INFO 03 (#T)	
INFO 04 ($Q)	
INFO 05 (#Q)	Sixteen-bit bidirectional information lines between the DPC and the DPEC. These lines are HIGH for a "1" bit and LOW for a "0" bit and are used to transfer initiate descriptors, information, and result descriptors.
INFO 06 ($M)	
INFO 07 (#M)	
INFO 08 ($J)	
INFO 09 (#J)	
INFO 10 ($G)	
INFO 11 (#G)	
INFO 12 ($E)	
INFO 13 (#E)	
INFO 14 ($D)	
INFO 15 (#D)	Most significant bit (MSB).
EX SEL (#K)	Not used.
EX BUSY (#U)	Not used.

DPEC-DPC INTERFACE OPERATION

The initiate operation begins with the interface in an idle state defined by the lines READY/*BUSY/*SELECT/ (refer to table 1-4). The DPC brings up the SEND line to begin the operation, simultaneously putting the first initiate word on the INFO (0-15) lines.

Within 166 to 500 nanoseconds after setting the SEND line, the DPC brings up the SELECT line. The interface lines are now SELECT*BUSY/*READY/. This state indicates to the DPEC that the first initiate word is on the INFO lines. When the DPEC has accepted the first initiate word, it puts out a clock pulse (300 nanoseconds minimum width). The leading edge of this pulse indicates to the DPC that the first word has been accepted by the DPEC and also causes the DPC to set the READY line.

Table 1-4. SELECT, READY, and BUSY Status

Level Status	State/Phase	Remarks
SELECT/*BUSY/*READY/	Idle	
SELECT * BUSY/*EXECUTE	Initiate phase	READY/ = DPEC receiving the first initiate word READY = DPEC receiving second initiate word
SELECT*BUSY*READY* EXECUTE	Data transfer phase	EXECUTE/ = Slip Mode (see note section of this table)
SELECT/*BUSY*READY/	Result status phase	
SELECT/*BUSY*READY	Wait for result status phase	Operation terminated by Disk Pack Control (DPC)
SELECT/*BUSY/*READY	Sequence error	DPEC failure
SELECT*BUSY*READY/	Go to result status phase	Operation terminated by the DPEC

NOTE

SELECT will stay up for the initiate and verify operations. SELECT/ will terminate the initiate and verify operation. For timing, see figure 1-26.

The DPC will drop the EXECUTE line if, during the data phase with more data to come, the DPC has full buffers during a read operation or empty buffers during a write operation. This will put the DPEC in the slip mode. When data or buffers become available, the DPC will raise the EXECUTE line and the operation will continue.

Within 500 nanoseconds after the trailing edge of the clock, assuming READY is on, the second initiate word is put on the INFO lines. The second initiate word contains the remainder of the file address which was started with the last five bits of the first initiate word. Again, the DPEC sends a clock pulse to the DPC whose leading edge indicates its receipt of the second initiate word. This causes the BUSY line to come up, and conditions are now in the data mode as defined by the lines SELECT*BUSY*READY.

If the operation is a read, the DPC will drop the SEND line and wait for the first two bytes of data. If the operation is a write, the DPC will transfer the first two bytes of data on the lines. If the operation (read or write) cannot be performed (a seek is required, the unit is still seeking, etc.), the DPEC will drop the READY line, and the DPC will drop the SELECT line within the following 1 millisecond (and drop SEND if it is still on) and wait for the result word. The interface lines are now in the result state of SELECT/*READY/ *BUSY. The following DPEC clock indicates that the result word is on the INFO lines, which are stable for the entire clock period. Some time after the leading edge of the clock, BUSY drops to return the interface lines to the idle state.

If the operation can be performed after the initiate phase, the READY line will stay on. Each clock indicates that data is on the INFO lines for a read operation or accepted for a write operation. On a write operation, the data can change any time after the leading edge of the clock. During a read operation, the data must be stable for the entire clock width.

If the DPEC must terminate for any reason (end of initialize, relocate or read maintenance, or any error condition), it drops the READY line. The DPC then drops SELECT and waits for the result. If the DPC must terminate the operation, it drops SELECT on or before the 90th data transfer (last of the sector's data field) for any sector. The DPEC finishes transferring for that sector, drops READY and sends the result. If SELECT is still on after the 90th transfer, the DPEC will continue reading or writing into the next sector. There will be only one result phase for each operation. The DPEC sends a result for each sector on a read, occurring in the data transfer mode.

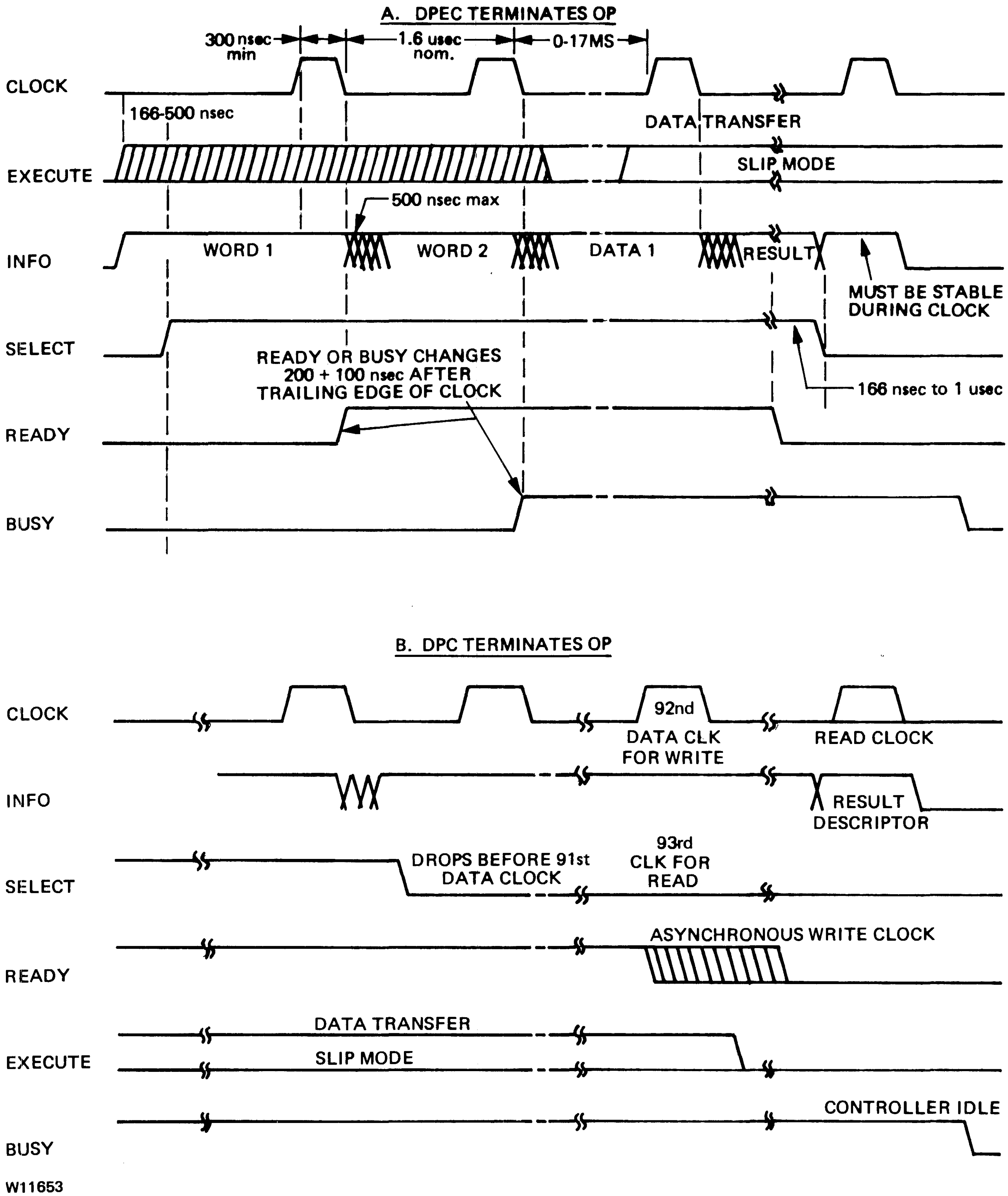


Figure 1-26. Interface Timing

2. POWER SUPPLY THEORY

INTRODUCTION

This section contains a description of the power supply used in the 206 disk pack electronic controller (DPEC).

POWER SUPPLY

The DPEC power supply contains the following subassemblies.

a. An OEM power supply subassembly (see figure 2-1) that furnishes the following:

1. An adjustable +5.0 volts output at 20 amperes.

2. A fixed -5.2 volts output at 0.7 ampere.

3. Taps on the input of the supply to compensate for various ac input voltages.

b. A 12 volt supply that furnishes front panel lamp voltage and voltage to pick power supply relay K1 (see figure 2-2). (K1 will be energized when the front panel POWER switch is pressed. When energized, K1 will provide 208 volts ac to the fans and the power supply subassembly.)

c. Terminal board TB4 that provides a convenient location to rewire the DPEC power supply for phase-to-neutral operation that is required for international installations and certain domestic installations where single phase operation is required. (Refer to 206 DPEC Function and Operation manual, form number 1084365, section 2.)

d. AC output power receptacles J2 through J5 that provide power for the disk pack drives and rotate the phases to provide a more balanced load on the input power source.

Overvoltage protection is provided on the +5.0 volts supply. The protection circuit is calibrated to prevent the output from exceeding approximately 6.0 volts. If an overvoltage condition occurs, the output will drop to less than 1.0 volt in 50 microseconds or less. (There will be no damage to the overvoltage protection device if left in this condition for up to 24 hours.)

An overload protection circuit is provided in the OEM subassembly power supply. It is calibrated to prevent the current output from the +5.0 volts supply from exceeding approximately 20 amperes. See figure 2-3.

Thermal protection is provided in the OEM subassembly. If the heat sink temperature exceeds 194 degrees F (90 degrees C) ±6 percent, the power supply will be turned off.

194°F

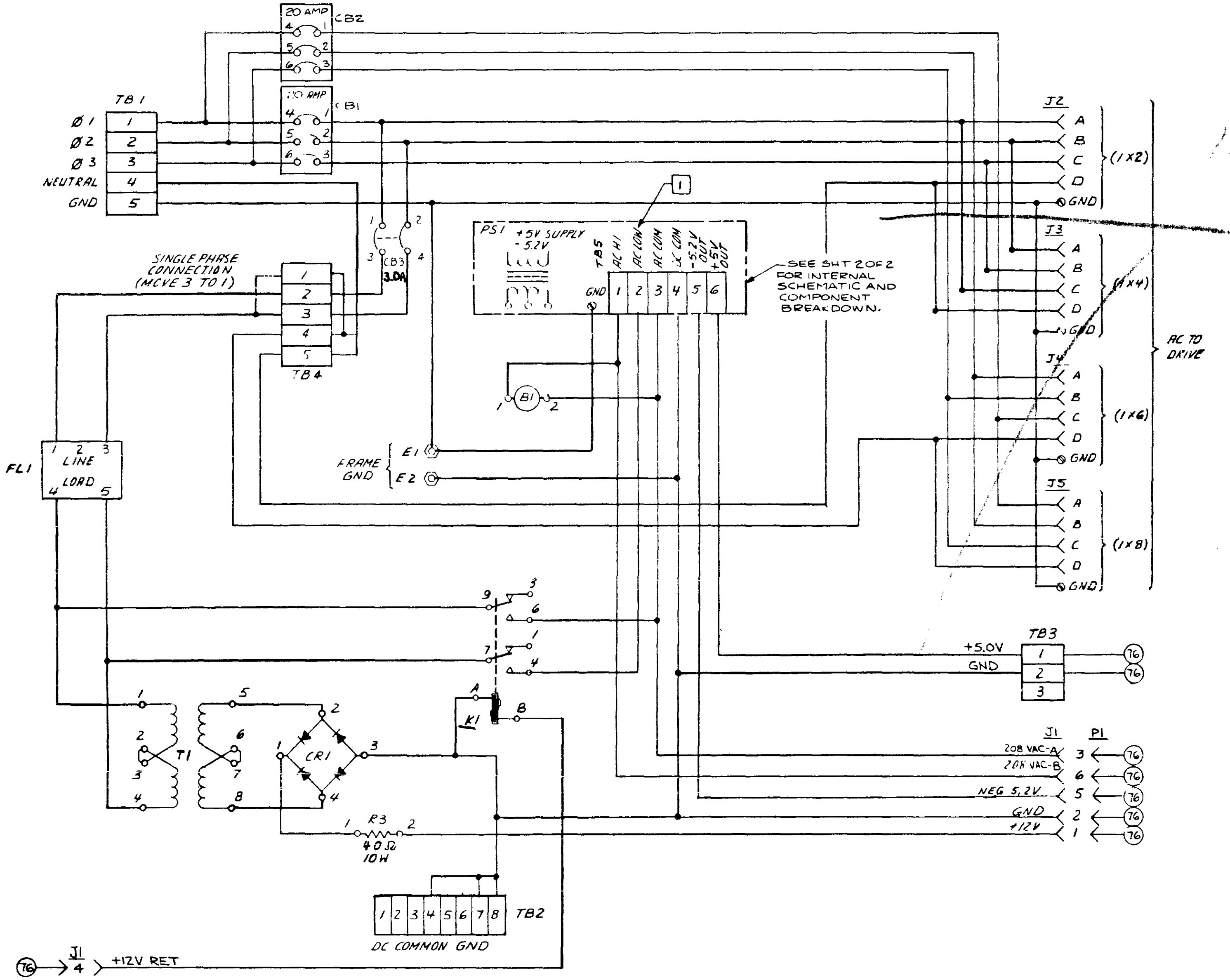


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Figure 2-1. Power Supply Schematic

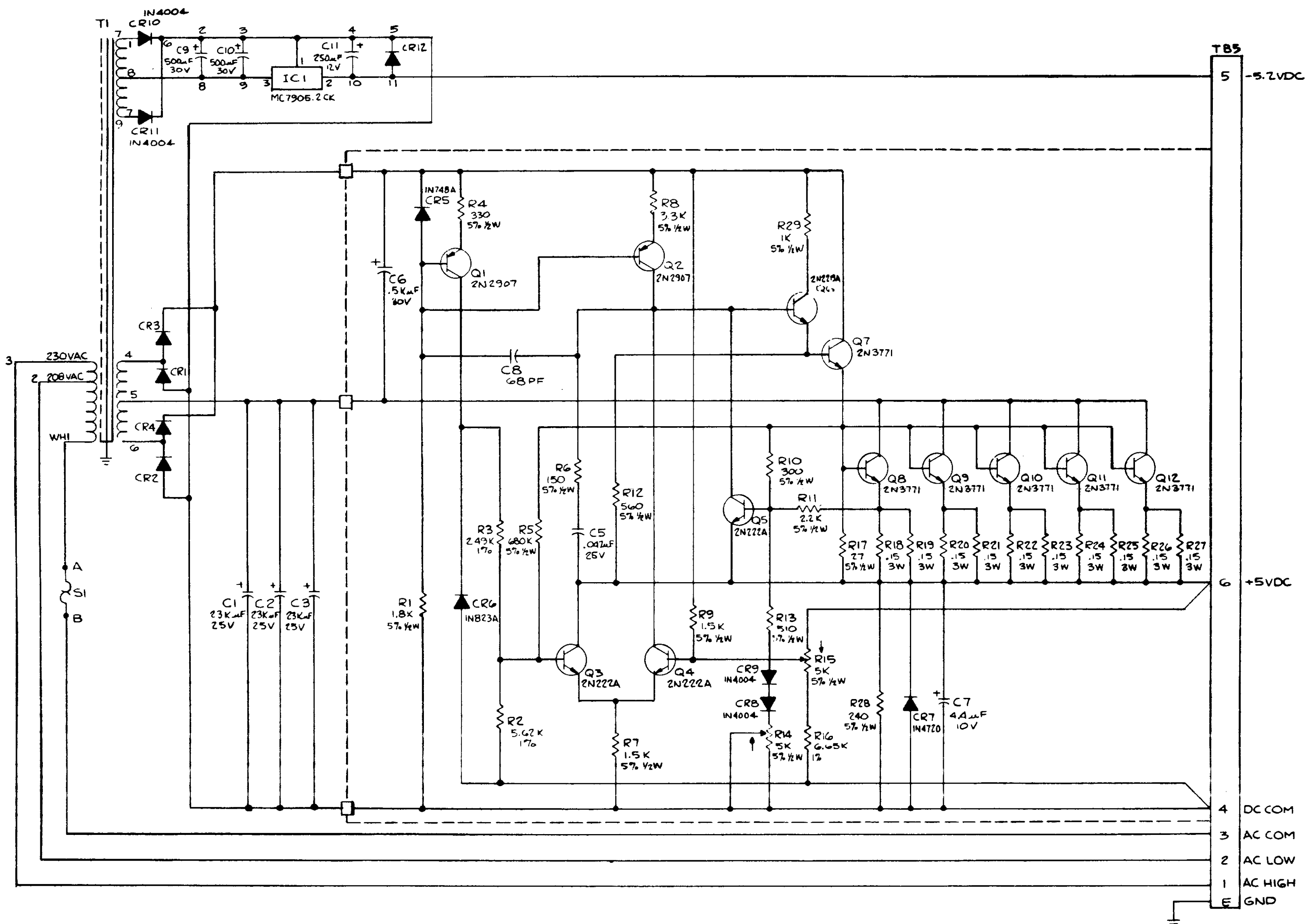

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Figure 2-2. Internal Power Supply Schematic

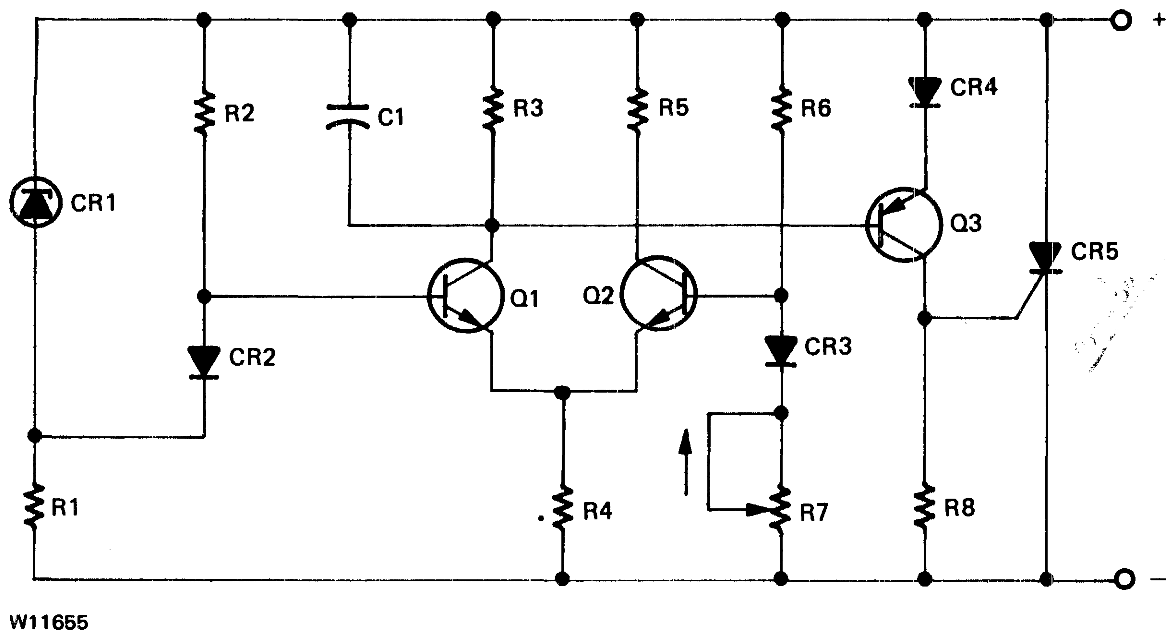

Figure 2-3. Overvoltage Protection Schematic

Burroughs FIELD ENGINEERING	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B1700	NO. R4365-001
		STYLE/MODEL B9499-3	PAGE 1 OF 1
ORIGINATOR: TIO Westlake		TOP UNIT NO. 2160 6561	
STD. INSTALL. TIME N/A	UNITS AFFECTED *	UNIT DESCRIPTION Disk Pack Electronic Controller	
TITLE Updated Test and Field Documentation			DATE 4/28/77
TYPE OF CHANGE ☐ FUNCTIONAL	☒ IMPROVED MAINTAINABILITY	☐ IMPROVED RELIABILITY	

*Below serial number 103056966

PREREQUISITE: None

CONDITION: Incomplete T & F documentation shipped with B9499-3 DPEC.

CAUSE: N/A

CORRECTION: Order complete, updated T & F package

PARTS REQUIRED:

Media Package Number 1088739

Contains complete T & F package, 304 pages.

☐ THIS CHANGE IS A RESULT OF FIELD REPORTING

F.E. Dist. Code DB

FOR LIBRARY BINDER 349

FOR F.E. TECHNICAL MANUAL FORM 1084365

Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B1700	NO. L4365-001
		STYLE/MODEL B9499-3	PAGE 1 OF 1
ORIGINATOR: TIO Westlake		TOP UNIT NO. 2160 6561	
STD. INSTALL. TIME 0.5 hr or less	UNITS AFFECTED Below B103057048	UNIT DESCRIPTION 206 Disk Pack Electronic Controller	
TITLE Improper Read Maintenance Operation (ECN 62918)			DATE 2/28/77

INSTALLATION IS MANDATORY

PREREQUISITE: None

CONDITION: The read maintenance operation code does not perform correctly.

CAUSE: Missing wire on the K card.

CORRECTION: Add logic to the K card to correct this condition.

PARTS REQUIRED:

Part Number	Description	Qty	Unit List Price
1356 9520	30 Awg wire	Less than 1 foot	$0.08/ft

INSTRUCTIONS:

1. Remove power from the DPEC.
2. Remove the K card from the DPEC. (The card assembly part number should be 2162 6189).
3. Add a wire from card backplane pin 1B06 to pin 1C06.
4. Add this wire to the K1B06 (MD12A/) logic in the K card circuit list.
5. Change the card assembly part number from 2162 6189 to 2162 9423.

F.E. Dist Code DC

☐ THIS CHANGE IS A RESULT OF FIELD REPORTING

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FOR F.E. TECHNICAL MANUAL FORM 1084365

Printed in U.S. America

Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B1700	NO. L4365-002
ORIGINATOR: TIO Westlake		STYLE/MODEL B9499-3	PAGE 1 OF 1
		TOP UNIT NO. 2160 6561	
STD. INSTALL. TIME 0.5 hour	UNITS AFFECTED Below 103057550	UNIT DESCRIPTION Disk Pack Electronic Controller	
TITLE Intermittent Data Transmission Errors (ECN 63175)			DATE 4/27/77

INSTALLATION IS MANDATORY

PREREQUISITE: None

CONDITION: Erroneous data transmission errors

CAUSE: Floating clock input on RAWCKDPC flip flop

CORRECTION: Add a ground to the clock input of the chip.

PARTS REQUIRED:

Part Number	Description	Qty	Unit List Price
1356 9520	30 AWG wire	less than a foot	$0.08/ft

INSTRUCTIONS:

1. Remove power from the DPEC
2. Remove the H card, part number 2160 9284.
3. Add a wire from 1N04 to 1N08 on the backplane side of the card.
4. Modify the T & F documents to reflect this change.
5. Change the card part number to 2163 2401.

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Burroughs FIELD ENGINEERING	**RELIABILITY IMPROVEMENT NOTICE**	SYSTEM SERIES B1700	NO. R4365-002
ORIGINATOR: TIO Westlake		STYLE/MODEL B9499-3	PAGE 1 OF 1
		TOP UNIT NO. 2160 6561	
STD. INSTALL. TIME 0.5 hr	UNITS AFFECTED Below 103080016	UNIT DESCRIPTION 206 Disk Pack Electronic Controller	
TITLE Intermittent Eight Second Timer Operation (ECN 63284)			DATE 9/26/77

TYPE OF CHANGE

☐ FUNCTIONAL ☒ IMPROVED MAINTAINABILITY ☐ IMPROVED RELIABILITY

PREREQUISITE: None

CONDITION: The operation of the eight second timer (TMOT8SEC) is intermittent under certain conditions.

CAUSE: The load input on the integrated circuit at location TU2 on the "M" card is floating.

CORRECTION: Connect the load input to the +5VR source

PARTS REQUIRED:

Part Number	Description	Qty	Unit List Price
1356 9520	30 Awg wire	1 foot or less	$0.08/foot

INSTRUCTIONS:

1. Remove DPEC power.
2. Remove the "M" card. It should be part number 2163 4811.
3. Add a wire from 2U08 (TU2 load input) to 1G00 (+5VR) on the "M" card.
4. Change the card assembly number from 2163 4811 to 2163 4910.
5. Modify schematic page 37 and the T & F documentation to reflect this change.

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Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B1700	NO. L4365-003
ORIGINATOR: TIO Westlake		STYLE/MODEL B9499-3	PAGE 1 OF 2
		TOP UNIT NO. 2160 6561	
STD. INSTALL. TIME 1.0 hour	UNITS AFFECTED All	UNIT DESCRIPTION 206 Disk Pack Electronic Controller	
TITLE Intermittent DPEC Errors			DATE 7/21/77

INSTALLATION IS MANDATORY

PREREQUISITE: None

CONDITION: Intermittent DPEC errors

CAUSE: Floating inputs on several chips in the DPEC cause susceptibility to noise.

CORRECTION: Perform the modifications listed below.

PARTS REQUIRED:

Part Number	Description	Qty	Unit List Price
1356 9520	30 Awg wire	2 feet or less	$ 0.08/foot

INSTRUCTIONS:

1. Remove power from the DPEC.
2. Remove the F card. It should be card assembly number 2162 9266.
   A. Add a jumper wire from 1B05 to 1A08 on the backplane of the card. (Chip AB-1 clock input to ground).
   B. Mark the card to indicate LIN 003 has been installed. The card assembly part number will be changed at a later date.
   C. Modify schematic page 45 to reflect this change. (Chip AB-1, REMOTE logic).
3. Remove the G card. It should be card assembly number 2162 5447.
   A. Add a jumper wire from 1R04 to 1R08 on the backplane of the card. (RS-1 clock input to ground).
   B. Mark the card to indicate LIN 003 has been installed. The card assembly number will be changed at a later date.
   C. Modify schematic page number 71 to reflect this change. (Chip RS-1, CMSELHD4 logic).
4. Remove the R card. It should be card assembly number 2160 8641.
   A. Add the following jumpers to the card backplane:
      (1). From 1N04 to 1N08 (Chip NP1 clock input to ground)
      (2). From 1P05 to 1R08 (Chip NP1 clock input to ground)
      (3). From 2K08 to 2K01 (Chip JK2 load input to +5 VR)
   B. Mark the card to indicate LIN 003 has been installed. The card assembly number will be changed at a later date.
   C. Modify schematic pages 15 and 17 to reflect these changes.

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5. Remove the M card. It should be card assembly number 2162 9241.

   A. Add the following jumpers to the card backplane:

      (1). From 4W08 to 4W01. (Chip VW4 load input to +5 VR)
      (2). From 2U08 to 2U01. (Chip TU2 load input to +5 VR)

   B. Mark the card to indicate LIN 003 has been installed. The card assembly number will be changed at a later date.

   C. Modify schematic pages 37 and 38 to reflect these changes.

Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B1700	NO. L4365-004
		STYLE/MODEL B9499-3	PAGE 1 OF 1
ORIGINATOR: TIO Westlake		TOP UNIT NO. 2160 6561	
STD. INSTALL. TIME Less than 1.0 hrs	UNITS AFFECTED Below 10307860x	UNIT DESCRIPTION 206 Disk Pack Electronic Controller	
TITLE Intermittent Data Shift Errors (ECN 63272)			DATE 8/1/77

INSTALLATION IS MANDATORY

PREREQUISITE: None

CONDITION: Under certain conditions, unwanted bits of information can be added to the data field before the actual data information is received.

CAUSE: There is a wiring error on the "H" card (Control Logic Four Card).

CORRECTION: Perform the wiring changes listed below.

PARTS REQUIRED:

Part Number	Description	Qty	Unit List Price
1356 9520	30 Awg wire	less than one foot	$0.08 per foot

INSTRUCTIONS:

1. Be sure DPEC power is off.
2. Remove the "H" card. It should be part number 2163 2401.
3. Perform the following wiring changes to the backplane of the card.
   A. Delete 0K07 to 1K04 (level 2)
   B. Delete 3L04 to 1K04 (level 1) (H3L04)
   C. Add 0K07 to 3L04 (level 2)
   D. Add 3L07 to 1K04 (level 1) (H3L07)
4. Change the card part number to 2163 4753 (ECN 63272).
5. Modify page 203 of the circuit list for the "H" card as follows:
   A. Draw a line through:
      "H3L04 1K04 3L04 1 294"
   B. Add the following line:
      "H3L07 1K04 3L07 1 294"
      (The schematic on page 65 is drawn correctly).

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Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B1700	NO. L4365-004
		STYLE/MODEL B9499-3	PAGE 1 OF 1
ORIGINATOR: TIO Westlake		TOP UNIT NO. 2160 6561	
STD. INSTALL. TIME Less than 1.0 hrs	UNITS AFFECTED Below 10307860x	UNIT DESCRIPTION 206 Disk Pack Electronic Controller	
TITLE Intermittent Data Shift Errors (ECN 63272)			DATE 8/1/77
INSTALLATION IS MANDATORY			

PREREQUISITE: None

CONDITION: Under certain conditions, unwanted bits of information can be added to the data field before the actual data information is received.

CAUSE: There is a wiring error on the "H" card (Control Logic Four Card).

CORRECTION: Perform the wiring changes listed below.

PARTS REQUIRED:

Part Number	Description	Qty	Unit List Price
1356 9520	30 Awg wire	less than one foot	$0.08 per foot

INSTRUCTIONS:

1. Be sure DPEC power is off.
2. Remove the "H" card. It should be part number 2163 2401.
3. Perform the following wiring changes to the backplane of the card.
   A. Delete 0K07 to 1K04 (level 2)
   B. Delete 3L04 to 1K04 (level 1) (H3L04)
   C. Add 0K07 to 3L04 (level 2)
   D. Add 3L07 to 1K04 (level 1) (H3L07)
4. Change the card part number to 2163 4753 (ECN 63272).
5. Modify page 203 of the circuit list for the "H" card as follows:
   A. Draw a line through:
   "H3L04 1K04 3L04 1 294"
   B. Add the following line:
   "H3L07 1K04 3L07 1 294"
   (The schematic on page 65 is drawn correctly).

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Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B1700	NO. L4365-005
		STYLE/MODEL B9499-3	PAGE 1 OF 1
ORIGINATOR: TIO Westlake		TOP UNIT NO. 2160 6561	
STD. INSTALL. TIME 1.0 hour	UNITS AFFECTED 103078689	UNIT DESCRIPTION 206 Disk Pack Controller	
TITLE False Address Mark Errors (ECN 63275)			DATE 9/20/77

INSTALLATION IS MANDATORY

PREREQUISITE: None

CONDITION: The 250 microsecond timer on the "M" card may be timing out too soon.

CAUSE: Excessive tolerance of components.

CORRECTION: Replace timing components on the timer at VWO of the "M" card.

PARTS REQUIRED:

Part Number	Description	Qty	Unit List Price
1265 5874	43KΩ, 1/4W, ±5% Resistor	1	$0.32
2155 4688	.0068 mfd, ± 10% 100 WVDC Capacitor	1	1.62

INSTRUCTIONS:

1. Remove DPEC power.
2. Remove the "M" card. It should be part number 2162 9241.
3. Remove the 3.9KΩ resistor from location 0U09 to 0W09.
4. Install part number 1265 5874, 43KΩ resistor, at this location (from 0U09 to 0W09).
5. Remove the .068 mfd capacitor from location 0W03 to 0V03.
6. Install part number 2155 4688, .0068 mfd capacitor at this location (from 0W03 to 0V03).
7. Change the card assembly number from 2162 9241 to 2163 4811.
8. Modify schematic page 37 to reflect this change.

NOTE:

After the installation of this LIN, the assembly part numbers for the cards will be as follows:

Q	2160 8690	
P	2162 4440	
R	2163 4894	ECN 63283 LIN L4365-003
S	2160 8591	
N	2160 8849	
M	2163 4811	ECN 63275 LIN L4365-005
F	2163 4852	ECN 63276 LIN L4365-003
L	2162 6353	
K	2162 9423	ECN 62918 LIN L4365-001
J	2162 2881	
H	2163 4803	ATI 56205
G	2163 4878	ECN 63278 LIN L4365-003

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Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B1700	NO. L4365-006
		STYLE/MODEL B9499-3	PAGE 1 OF 1
ORIGINATOR: TIO Westlake		TOP UNIT NO. 2160 6561	
STD. INSTALL. TIME 0.5 hour	UNITS AFFECTED Below B103080016	UNIT DESCRIPTION 206 Disk Pack Electronic Controller	
TITLE Sixteen Bit Data Shift Problem Primarily on B1714 Systems (ECN 63294)			DATE 9/26/77

INSTALLATION IS MANDATORY

PREREQUISITE: None

CONDITION: Most B1714 systems using 206 Disk Packs have a intermittent 16 bit data shift problem.

CAUSE: A timing problem exists in the generation of the first data transfer "CK DPC" pulse.

CORRECTION: Replace critical integrated circuits with Schottky type devices.

PARTS REQUIRED:

Part Number	Description	Qty	Unit List Price
2600 1487	74S00 integrated circuit	1	$9.13
2600 1495	74S04 integrated circuit	1	3.40
2600 1503	74S10 integrated circuit	1	2.37
2604 6805	74S08 integrated circuit	1	5.06

INSTRUCTIONS:

1. Power off the DPEC.
2. Remove the "H" card. It should be part number 2163 4803.
3. Remove the following integrated circuits:

	Location	Type	Part Number
A.	JK3	7404	1447 3532
B.	JK4	7408	1447 3524
C.	LM2	7400	1447 3516
D.	NP3	7410	1447 3540

(Save for local spares).

4. Install the Schottky devices as listed below:

	Location	Type
A.	JK3	74S04
B.	JK4	74S08
C.	LM2	74S00
D.	NP3	74S10

5. Change the card assembly number to 2163 5420
6. Modify the appropriate pages in the test and field documentation.

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