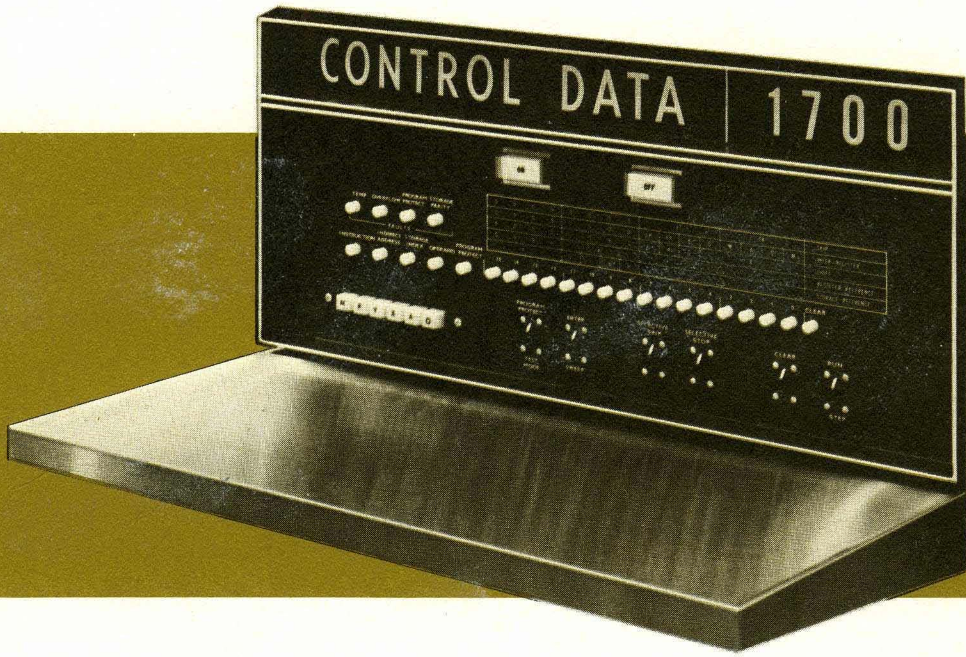
1700 COMPUTER MAINTENANCE

Volume III

SECOND EDITION



CONTROL DATA INSTITUTE

1700 COMPUTER MAINTENANCE TRAINING MANUAL

VOLUME III

<u>For Training Purposes Only</u>

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Address comments concerning this manual to:
CONTROL DATA EDUCATION INSTITUTES
4530 West 77th Street
Minneapolis, Minnesota 55435

ATTN: Advanced Technology
Development Division,
Hardware Development, PGT310

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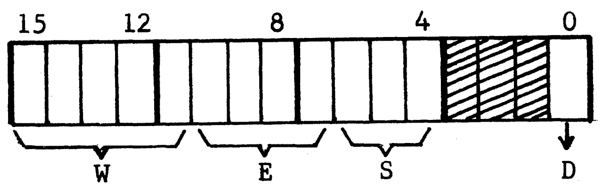
INTRODUCTION

The Basic 1700 system incorporates provisions for four Input/Output devices which operate in a non-buffered fashion. Each device has its own controller logic. The four controllers, in turn, communicate with the computer via an interface called the Common Synchronizer.

It is necessary to place into the 1704 Q Register, codes which identify completely the communications link desired. For low speed operations, the contents of Q has the following format:



Where W must be all zeros, E (the equipment code) must be 0001, S (the station code) must match the station number of the desired controller and D (the director bit) identifies the operation as being data transfer (D = "0") or non-data transfer (D = "1").

Station codes to be used in low-speed operations are given in table A. It should be noted that station code 0 is restricted to non-data transfers and applies to equipment rather than station operations. Its use will be explained during discussion of the Common Synchronizer.

Station 0 - - -	Common Synchronizer
Station 1 - - -	Teletypewriter
Station 2 - - -	Paper Tape Reader
Station 4 - - -	Paper Tape Punch
Station 6 - - -	Card Reader

Table A
Low Speed Station Codes

During low-speed input operations, the 1704 A Register is the destination of all transfers; whereas during output operations, the A Register is the source of all transfers.

The following chapters discuss the logic operation of the Common Synchronizer and each controller. Reference throughout these chapters will be to the low speed logic diagrams #60164200.

CHAPTER I

COMMON SYNCHRONIZER

CHAPTER I

COMMON SYNCHRONIZER

INTRODUCTION

The 1700 Low Speed Common Synchronizer provides the interface logic between the 1704 A and Q Registers and the four possible low-speed controllers. It is designated Equipment #1 on all 1700 systems. The synchronizer contains 12 logic modules which are located on the computer main frame. These modules are considered to be a part of the 1704 and will, therefore, be included in each 1700 computer.

One function of the Common Synchronizer is to translate the codes received from the Q Register. This determines whether the intended operation is to be performed within the low speed system or is to be performed by equipment and stations outside the low speed system. It is for this reason that equipment code #1 has been reserved for the Common Synchronizer and must not be used by equipments which interface directly with the A and Q Registers (via the 1705 AQ Data Channel).

CODE TRANSLATION

W = 0

Since the computer contains a W = 0 translator (page 75), no similar translator in needed within the Common Synchronizer. Instead, a W = 0 line is sent to 3-B17-8 of the Synchronizer. If W does equal zero, this line is a logical "1".

(W = 0) (E = 1)

If the W = 0 line is a "1" and the Equipment Code (bits 7-10 of Q) equals 0001, the AND gate feeding TP /3\ (B17, page 3) is satisfied and forces a logical "1" out of logic gate (A). Within the module, this enables the Read (Input Instruction) signal at 3-B17-2 or the Write (Output instruction) signal at 3-B17-28 to be recognized.

LOW SPEED OPERATIONS

Four basic operations may be performed with the low speed system:

(1) Non-data input transfer (status)

(2) Data input transfer (Read Data).

(3) Non-data output transfer (Function).

(4) Data output transfer (Write Data).

Translations for each of these operations is performed within the Common Synchronizer in the following manner.

Status Translation

If the computer is executing an Input instruction, the W code equals zero, the E code equals one and the D bit is "1", AND gate (D) (ZOO module, page 3) is satisfied which, in turn, satisfies the AND gate at TP /2\. This causes a logical one to leave the module at pin 1, informing the Common Synchronizer that a Status operation is being requested.

Read Data Translation

If the computer is executing an Input instruction, the W code equals zero, the E code equals one and the D bit is "0", AND gate (D) (ZOO module, page 3) is satisfied which, in turn, satisfies the AND gate at TP /1\. This causes logical ones to leave the module at pins 3, 5, 7, and 9, informing the synchronizer that a Read Data operation is being requested.

Function Translation

If the computer is executing an Output instruction, W = 0, E = 1 and the D bit is "1", AND gate (E) (Z00 module, page 3) is satisfied which, in turn, satisfies the AND gate at TP 6. This causes logical ones to leave the module at pins 16, 17, 19, 21, and 25, informing the synchronizer that a Function operation is being requested.

Write Data Translation

If the computer is executing an Output instruction, W = 0, E = 1 and the D bit is "0", AND gate (E) (Z00 module, page 3) is satisfied which, in turn, satisfies the AND gate at TP 5. This causes logical ones to leave the module at pins 23 and 27, informing the synchronizer that a Write Data Operation is being requested.

STATION CODE TRANSLATION

Bits 4, 5, and 6, of the Q Register determine the station with which communications is to be established. These bits enter the Z03 module, page 5. Translation logic within this module will determine the station number provided that W = 0 and E = 1.

Once the Common Synchronizer has completely translated the contents of Q and a Read or a Write signal is generated by the computer, the synchronizer then makes the appropriate transfers to allow the operation to be performed. For any input operation, it is a matter of connecting the source to the data lines feeding the computer A Register. For any output operation, it is a matter of connecting the A Register output lines to the proper destination.

INPUT OPERATIONS

STATUS STATION 1

When a status operation is requested, the Common Synchronizer must connect the designated station status code to the A Register input data lines. For the following example, assume that station 1 (teletypewriter) has been designated.

With a request for status, the output of 3-B17-1 is a logical one. If station 1 is designated, the outputs of 5-B14-25 and 5-B14-27 are logical ones while the outputs of 5-B14-8 and 5-B14-10 are logical zeros. The "0" output of 5-B14-8 will transfer the Ready, Busy, Interrupt and Data status bits being received from station 1 to the TG module at location B10 (page 7).

The logical "0" from 5-B14-10 will transfer the Protected, Alarm, Lost Data and End of Operation Status bits being received from station 1 to the TG module (page 7) at location B09.

The logical "1" from 5-B14-27 provides a signal to the teletypewriter (TTY) controller for its use during data transfers or function operations. The logical "1" from 5-B14-25 goes to the Z04 module, page 7, where it:

(1) enables the TTY Read Mode status to bit A09.

(2) enables the Reply/Reject logic (Z01 module, page 3).

(3) enables the Manual Interrupt status to bit A11 (Z10 module, page 9).

The status signal at 3-B17-1 goes to the Z04 module (page 7) where it:

(1) transfers Ready, Busy, Interrupt and Data status bits to A00, A01, A02, and A03, respectively (TG module at location B10).

(2) transfers End of Operation, Alarm, Lost Data and Protected status bits to A04, A05, A06, and A07, respectively (TG module at location B09).

(3) transfers Read Mode status to bit A09 (Z04 module).

(4) transfers Manual Interrupt status to bit A11 (Z10 module, page 9).

The logical "0" at 3-B17-6 will give an unconditional Reply to the computer for any low speed status request. Receipt of the Reply signal by the computer will cause the timing chain (which stops at time 200 for any I/O instruction) to continue. This, in turn, will cause:

(1) the Input to A FF (page 31) to set and transfer the status into the A Register.

(2) the Read signal to drop (Input FF, page 75 clears).

The computer then continues with its program at P + 1. When the Read signal to the common synchronizer (3-B17-2) drops, this will cause status to drop which drops the Reply to the computer. The Common Synchronizer is now in a position to accept another command from the computer.

Status operations from the other controllers would be similar to that just explained for the TTY. A status request from station 0 is also acceptable. Its meaning is an equipment status rather than a controller status. Equipment status for the low speed system means the inclusive OR of all status bits common to a data line.

STATUS STATION 0

If a low-speed status request is made with the station code equal to zero, the following conditions will exist in the Common Synchronizer:

(1) 5-B14-15, 17 outputs are ones

(2) 5-B14-8, 10 outputs are zeros

(3) 5-B14-12, 16 outputs are zeros

(4) 5-B14-7 output is zero

(5) 5-B14-6 output is one

(6) 5-B14-9, 11 outputs are zeros

(7) 3-B17-1 output is one

(8) 3-B17-6 output is zero

The outputs of 5-B14-8, 12, 7, and 9, being zeros simultaneously will inclusively OR the Ready, Busy, Interrupt and Data status outputs from all four controllers into the four outputs of the TG module (page 5). These four outputs transfer to the TG module at location B10 (page 7) as the four lowest bits of the status. The outputs of 5-B14-10, 16, and 11, being zeros simultaneously with 5-B14-6 being a logical "1", will inclusively OR the Protected, Alarm, Lost Data, and End of Operation status outputs from those controllers which provide these status indications. The four status outputs of the Z02 module transfer to the TG module at location B09 (page 7) as bits 04 through 07 of the status. These eight bits form the entire equipment status which is transferred via the TG modules at locations B09 and B10 (page 7) to the computer A Register fan-in.

The logical "0" at 3-B17-6 will generate a Reply to the computer. The computer then transfers this status into the lower 8 bits of the A Register (zeros transfer into the upper 8 bits) and continues with the program.

One important use of the equipment status is in checking interrupts. It should be remembered that the low speed interrupt is ORed with external interrupt line #1. If a level 1 interrupt occurs, the programmer can determine if it originated from the low speed system by executing an equipment status, then checking the interrupt bit. If the bit is a "1", the interrupt was due to a low speed device; if the bit is a "0", the interrupt was due to the equipment connected to external interrupt line #1.

READ DATA, STATION 2

When a Read Data operation is requested, the Common Synchronizer must connect the data output lines of the designated station to the A Register data input lines. The following example assumes station 2 (Paper Tape Reader) has been designated.

With a Read Data request, the outputs of 3-B17-3, 5, 7, and 9 are logical ones while the outputs of 3-B17-20, 12, 14, and 18 are logical zeros. The outputs of 3-B17-18, 12, 14, 3, 5, and 7 are used within the controllers to indicate the operation being requested. The logical "1" output of 3-B17-9 goes to the Z04 module, page 7, where it:

(1) enables AND gates feeding TP △3, TP △6 and TP △5

(2) generates an output at 7-B13-21 which enables the generation of a Character Input signal to the computer if station 1 or 2 is selected.

Since we are considering a read from station 2, the outputs of 5-B14-13 and 23 are logical ones while the outputs of 5-B14-12 and 16 are logical zeros.

The logical zero from 5-B14-12 connects data line bits 00 through 03 of station 2 controller through the TG module (page 5) to the TG module at location B10, page 7. The logical zero from 5-B14-16 connects data line bits 04 through 07 of station 2 controller through the Z02 module (page 5) to the TG module at location B09, page 7. The Z02 module also generates a Character Input signal to the computer which prevents I/O transfer into the upper 8 bits of the A Register.

The logical one from 5-B14-13 goes to the Z04 module, page 7, where it causes logical zeros to leave the module at pins 22 and 27. The logical "0" from 7-B13-27 connects bits 00 through 03 of the P. T. Reader data lines to bits 00 through 03 of the data line inputs to the A Register. The logical "0" from 7-B13-22 connects bits 04 through 07 of the P. T. Reader data lines to bits 04 through 07 of the data line inputs to the A Register. An 8-bit data transfer path from station 2 controller to the A Register fan-in gates has now been established.

The logical "1" output of 7-B13-12 goes to the Z01 module, page 3, where it enables the Reply and Reject logic. If station 2 responds to the Read Data Command, it will place data on the lines and send a Reply signal to the Common Synchronizer. The Reply signal enters 11-B06-7 where it passes on to 3-B16-18. This will satisfy an AND gate which generates a Reply signal to the computer. Receipt of the Reply signal by the computer causes:

(1) the computer timing chain to start up (from time 200).

(2) the Input to A FF (page 31) to set, gating the character into A00-A07.

(3) the clearing of the Input FF (page 75) which drops the Read signal to 3-B17-2 in the Common Synchronizer.

When the Read signal drops, it causes the Read Data signal to drop. Loss of the Read Data signal to the P. T. Reader controller will cause its Reply signal to drop. The computer continues with its program at P + 1.

If station 2 cannot respond to the Read Data request, it will not place data on the lines and will send a Reject signal to the Common Synchronizer. The Reject signal enters 11-B06-1 where it passes on to 3-B16-15. This will satisfy an AND gate which generates a Reject signal to the computer. Receipt of the Reject signal by the computer causes:

(1) the computer timing chain (page 7) to start up (from time 200).

(2) the set input of the Input to A FF (page 31) to become disabled, thereby preventing any transfer into the A Register.

(3) the clearing of the Input FF (page 75), which drops the Read signal to 3-B17-2 in the Common Synchronizer.

(4) the formation of P + Δ with the result going to P.

When the Read signal drops, it causes the Read Data signal to drop. Loss of a Read Data signal to station 2 controller will cause its Reject signal to drop. The computer continues with its program at P + 1 (which is, in reality, the original contents of P + Δ + 1).

READ DATA, STATION 0

What would happen if a Read Data request was made from station 0? There would be an automatic Reject directly from the Common Synchronizer. Any attempt to Read Data from station 0 would satisfy the AND gate off input pin 13 of the Z01 module, page 3. The B term on the AND gate translates as (Read + Write) $\overline{\text{(Reply)}}$. Any time low speed Read or a Write signal is generated by the computer and a Reply is not generated, logic gate [B] outputs a logical "1". If the station code is 0, the AND gate becomes satisfied and generates a Reject signal to the computer.

At first glance this may seem to contradict our capability of performing a status from station 0, but this is not the case. It should be recalled that any status operation gives an immediate logical "0" out of logic gate [A] on the Z01 module. This will prevent logic gate [B] from outputting a "1".

It should be noted that there are only five ways of getting a Reject signal to the computer, the one just discussed or a reject signal from the four controllers.

This means that any Input or Output operation involving station codes which are non-existent (3,5, and 7) will have neither a Reply nor a Reject response. If the computer receives no response within 7 usec after it has generated a Read or a Write signal, the computer will reject itself (called an Internal Reject). Under conditions of an Internal Reject, the computer:

(1) starts the computer timing chain (page 7) from time 200.

(2) clears the Input or Output FF's (page 75), thereby dropping the Read or the Write signals.

(3) prevents any transfer into the A Register.

(4) continues the program at $P + \Delta$ (not $P + \Delta + 1$, as is true for an External Reject).

OUTPUT OPERATIONS

FUNCTION, STATION 4

When a Function operation is requested, the Common Synchronizer has the task of connecting the A Register output data lines to the designated station. The codes on these lines will then be interpreted by the controller to perform the function(s). The following example assumes a Function for the Paper Tape Punch (station 4).

With a Function request on Station 4, the following initial conditions exist in the Common Synchronizer:

(1) 3-B17-17, 19, 21, 25, and 16 all output logical ones.

(2) 3-B17-26 outputs a logical "0".

(3) 5-B14-22, 24, and 6 all output logical ones.

(4) 5-B14-7 outputs a logical "0".

The function signal outputs of 3-B17-17, 19, 21, and 25 are sent out to the various controllers to inform the controller that the information being sent is a Function Code, not a data word. The logical "1" output of 3-B17-16 is used within the Common Synchronizer for an Equipment Function, which will be discussed later.

The logical "1" output of 5-B14-24 is sent to station 4, informing the controller that it is to perform the Function specified by the incoming code. The logical "1" outputs of 5-B14-22 and 6 and the logical "0" output of 5-B14-7 are used within the Common Synchronizer for Input operations from station 4 and have no significance during output operations.

Data lines from the A Register fan-out pass directly through the Common Synchronizer and go to the four controllers without requiring any gating. The data line from A00 enters 3-B16-3 where it fans out to become five signals, one for each controller and one to be used within the synchronizer. The data lines from A01, A02, A03, A04, A06, and A07 pass through the TH module and go out to the appropriate controllers. The data line from A05 passes through the Z02 module, page 5, and goes out to the four controllers. The fan-out of A06 is insufficient in the TH module, page 9. The remainder of this fan-out is through the Z01 module, page 3.

Upon receipt of the function command from the Common Synchronizer, the designated controller will either Reply or Reject. If it sends a Reply, it means at least one function was performed. The Reply will be treated in the same manner as previously discussed under the topic Read Data. Upon receipt of the Reply, the computer will:

(1) start the computer timing chain (page 7) at time 200.

(2) clear the Output FF (page 75), causing the Write signal to drop.

(3) continue with its program at P + 1.

If the controller responds to the Function command by Rejecting, it means no functions were performed. The Reject is treated in the same manner as the Reply with the exception that the program continues at $P + \Delta + 1$.

FUNCTION, STATION 0

If a low-speed Function request is made with the station code equal to 0, it means an Equipment Function. The only permissable Equipment Function is the Equipment Clear (A00 = "1"). A low-speed equipment clear is identical to a Master Clear of the low-speed system with the exception that a Reply signal is produced for the equipment clear command.

The Equipment Clear Function will satisfy the AND gate fed by input pins 4, 6, and 8 of the Z10 module, page 9. It generates a Master Clear signal to the four controllers and sends a logical "0" to 3-B16-19. This logical "0" generates a Reply to the computer and disables the output of the [B] logic (bottom of the Z01 module, page 3), thereby preventing a Reject.

NOTE: If an Equipment Function is attempted which does not have a Function Code of A00 = "1", a Reject is sent to the computer.

What happens if a Function is issued to a non-existent low-speed station? Since the station does not exist, there can be no response, either Reply or Reject. The computer will generate an Internal Reject 7 usec after it sends the Write signal. The Internal Reject operations are the same as was given for the reply except that the computer program continues at $P + \Delta$.

WRITE DATA, STATION 4

When a Write Data operation is requested, the Common Synchronizer must connect the A Register output data lines to the designated station. The data on these lines will transfer to the output device where a write operation is performed. The following example assumes a Write Data to the paper tape punch.

With a Write Data request on station 4, the following initial conditions exist in the Common Synchronizer:

(1) 3-B17-23 and -27 output logical ones.

(2) 3-B17-26 outputs a logical "0".

(3) 5-B14-22,24, and 6 all output logical ones.

(4) 5-B14-7 outputs a logical "0".

The Write Data signal outputs of 3-B17-23 and 3-B17-27 are sent to the two controllers capable of write operations, (teletypewriter and punch). The station 4 translation (page 5) along with the Write Data signal informs the punch controller that a write operation is being requested. If the punch can accept the data, it will do so and send a Reply to the Common Synchronizer. If the punch cannot accept the data, no data transfer will occur and a Reject will be sent to the Common Synchronizer. The effect of Reply or Reject upon computer operations is the same as for the function operation.

Once data has transferred to an output device, the device goes into a Busy condition while the data is processed. During this Busy state further data transfers are prohibited. Once the data word has been processed, a Not Busy condition will exist allowing another data transfer from the computer.

CHAPTER II

TELETYPEWRITER CONTROLLER

CHAPTER II

TELETYPEWRITER CONTROLLER

INTRODUCTION

Two models of teletypewriters are available in the 1700 low-speed system. One model has been modified to provide a total of three options, these are the Keyboard Send Receive (KSR), Automatic Send Receive (ASR) and modified Automatic Send Receive. The 1711 option provides a KSR teletypewriter and appropriate controller logic. The 1712 provides an ASR teletypewriter and appropriate controller logic. The 1713 provides a modified ASR teletypewriter and appropriate controller logic.

The 1711 teletypewriter contains a keyboard and page printer. The unit can send and receive page-printed information via ordinary telegraph lines. It is connected to another set and both print whatever is typed from either keyboard. The KSR features an automatic keyboard lock which senses an open-circuit condition (a NULL-NULL code) and locks the keyboard at the sending unit. This prevents further transmission and loss of characters. The lock may also be activated manually by pressing the BREAK button. The keyboard is unlocked by pressing the BREAK REL (Break Release) button on the keyboard. Another important feature of the KSR is that even vertical parity is generated for error detection.

The 1712 teletypewriter consists of a send-receive page printer, a paper tape punch and a paper tape reader. The ASR has all the capabilities of the KSR with additional capabilities provided by the paper tape units. The teletypewriter contains a 5-position Mode Switching Control to the left of the keyboard. An operator can manually select any of the five following modes:

(1) Keyboard Mode-K

When the mode Control switch is placed in the K position, the keyboard and printer act as a send-receive page printer. In this mode the teletypewriter acts as a KSR. The paper tape units serve no function in this mode.

(2) Keyboard/Tape Mode-KT

When the Mode Control switch is placed in the KT position, the keyboard and paper tape reader are connected in parallel as information sources while the page printer and paper tape punch are connected in parallel as information destinations. In this mode, read operations will transfer data to the computer from either the keyboard or the paper tape reader while the page printer and paper tape punch make copies of the source information. If the paper tape reader is active and a key on the keyboard is pressed, the results will be garbled information. In the KT mode, write operations will transfer information from the computer to the page printer and paper tape punch.

NOTE: If the LINE/LOCAL/OFF switch is placed in LOCAL position, the teletypewriter is disconnected from the computer. While in LOCAL operation, the KT mode can be used to prepare punched tapes from keyboard entry or duplicate tapes from paper tape reader entry with the printer making readable copies of either entry.

(3) Tape Mode - T

When the Mode Control switch is placed in the T position, only the page printer and paper tape reader are connected on-line to the computer. At the same time, the keyboard is connected off-line to the paper tape punch. In the T mode, write operations will transfer information from the computer to the page printer while read operations will transfer information from the paper tape reader to the computer and the page printer. Simultaneously, a new tape can be prepared from keyboard entry.

NOTE: If the LINE/LOCAL/OFF switch is placed in LOCAL position with T mode selected, the reader and printer are connected on one circuit while the keyboard and punch are connected on another circuit. The keyboard-punch combination can be used to prepare a new tape while the reader-printer combination can be simultaneously used to verify a previously punched tape.

(4) Tape-to-Tape Send Mode - TTs

When the Mode Control switch is placed in the TTs position, the paper tape reader is the only unit connected to the computer. The page printer is completely disconnected while the keyboard and punch are connected together off-line. In this mode, only read operations are allowed; however, since the page printer is inactive, tapes of 5, 6, 7, or 8 levels can be read into the computer. The off-line function of the keyboard and punch is the same as for T mode.

(5) Tape-to-Tape Receive Mode - TTr

When the Mode Control switch is placed in the TTr position, the paper tape punch is the only unit connected to the computer. The page printer, keyboard and reader are inactive in this mode. In the TTr mode, only write operations are allowed; however, since the page printer is inactive, 1-inch tapes of 5, 6, 7, or 8 levels can be punched with information from the computer.

The 1713 teletypewriter is an ASR which has been modified to allow mode selection from the computer (via Function Codes) or manually at the teletypewriter. In this option, the rotary Mode Selection switch has been replaced by push-button indicator switches and necessary internal hardware to accommodate the added capability.

Whenever the page printer is activated, information must correspond to the 8-bit American Standard Communications Information Interchange (ASCII) code given in table 2-1.

AMERICAN STANDARDS CODE FOR INFORMATION INTERCHANGE

VERSION OF JUNE 1962

b7 b6 b5 →					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b_4 ↓	b_3 ↓	b_2 ↓	b_1 ↓	Column → / Row ↓	0	1	2	3	4	5	6	7
0	0	0	0	0	NULL	DCO	SP	0	@	P		
0	0	0	1	1	SOM	X-ON	!	1	A	Q	ALT MODE	
0	0	1	0	2	EOA	TAPE Aux On	"	2	B	R	ACK	
0	0	1	1	3	EOM	X-OFF	#	3	C	S		
0	1	0	0	4	EOT	TAPE Aux off	$	4	D	T		
0	1	0	1	5	WRU	ERROR	%	5	E	U		
0	1	1	0	6	RU	SYNC	&	6	F	V		
0	1	1	1	7	BELL	LEM	'	7	G	W		
1	0	0	0	8	FE_0	S_0	(	8	H	X		
1	0	0	1	9	H. TAB	S_1	)	9	I	Y		
1	0	1	0	10	LINE FEED	S_2	*	:	J	Z		
1	0	1	1	11	V. TAB	S_3	+	;	K	[		
1	1	0	0	12	FORM	S_4	,	<	L	\		
1	1	0	1	13	RETURN	S_5	-	=	M	]		
1	1	1	0	14	SO	S_6	.	>	N	↑		
1	1	1	1	15	SI	S_7	/	?	O	←		RUB OUT

Table 2-1
Teletypewriter ASCII Code

All 1700 low-speed teletypewriters are capable of responding to four computer commands:

(1) status

(2) Read Data

(3) Function

(4) Write Data

The first two commands require that the computer execute an Input instruction; the last two, an Output instruction. The contents of Q must be properly set to establish communications with station 1 for all four commands.

STATUS

Status of the 1700 low speed teletypewriter is indicated by a Status Word sent to the computer A Register whenever an input non-data transfer (Q00 = "1") is requested from low speed station.1. Bits within the Status Word each have particular significance regarding the operational state of station 1 at the time a status is requested. The status words for all three options are identical and the meaning of individual bits within the word is given in table 2-2.

A00	Ready
A01	Busy
A02	Interrupt
A03	Data
A04	End of Operation
A05	Alarm
A06	Lost Data
A07	(unused)
A08	(unused)
A09	Read Mode
A10	Unused
A11	Manual Interrupt
A12-A14	Unused

Table 2-2

Teletypewriter Status Code

The status logic operations explained in the following paragraphs makes use of the 1712 controller diagrams #60164200, pages 13 through 25.

READY

A teletypewriter Ready status is indicated by bit 00 of the Status Word from station 1 being a logical "1". The Ready status bit is sent to the Common Synchronizer from 23-C11-15. For this bit to be a logical "1", the requirement is that the LINE/LOCAL/OFF switch (to right of teletypewriter keyboard) be placed in the LINE position. When this happens, a relay within the teletypewriter energizes, placing ground at 13-C11-9. This causes the controller Ready FF to set, giving a Ready status.

BUSY

A teletypewriter Busy status is indicated by bit 01 of the Status Word from station 1 being a logical "1". The Busy status bit is sent to the Common Synchronizer from 23-C06-14. There are four ways in which this bit can become a logical "1".

(1) Set the Mech. Busy FF (Z36 module, page 23).

(2) Set the Data Read FF (Z12 module, page 17).

(3) Set the Break FF (Z12 module, page 17).

(4) Set the TTY mode Busy FF (Z36 module, page 23).

INTERRUPT

A teletypewriter Interrupt status is indicated by bit 02 of the station 1 Status Word being a logical "1". The Interrupt status bit is sent to the Common Synchronizer from 17-C13-17. For this bit to be a logical "1", one or more of the following conditions exist:

(1) a Data Interrupt had been previously selected (via Function, to be discussed) and:

  (a) data from the computer is required by the controller in write mode, or

  (b) data is available to the computer from the controller in read mode.

(2) an End of Operation Interrupt had been previously selected (via Function, to be discussed) and the internal mechanical cycle of the teletypewriter and the electrical cycle of the controller have completed.

(3) an Alarm Interrupt had been previously selected and

  (a) a $\overline{\text{Ready}}$ condition exists, or

  (b) a Lost Data condition exists.

(4) The MANUAL INTERRUPT switch on the teletypewriter has been pressed.

DATA

A teletypewriter Data status is indicated by bit 03 of the station 1 Status Word being a logical "1". The Data status bit is sent to the Common Synchronizer from 17-C14-8. For this bit to be a logical "1", either of the following conditions exist:

(1) the TTY is in Read Mode and the Data Read FF (Z12 module, page 17) is set. This means a character is available for the computer.

(2) the TTY is in Write Mode and the Data Write FF (Z12 module, page 17) is set. This means the controller is in a position to accept a character transfer from the computer.

END OF OPERATION

A teletypewriter End of Operation status is indicated by bit 04 of the station 1 Status Word being a logical "1". The End of Operation status bit is sent to the Common Synchronizer from 23-C06-21. For this bit to be a logical "1", cycling of the controller Timing Chain (page 21) must be complete. This means that another data transfer between computer and controller can occur.

ALARM

A teletypewriter Alarm status is indicated by bit 05 of the station 1 Status Word being a logical "1". The Alarm status bit is sent to the Common Synchronizer from 17-C13-9. For this bit to be a logical "1", either of the following conditions exists:

(1) the controller Ready FF (page 23) is clear, indicating that the LINE/LOCAL/OFF switch is not in the LINE position.

(2) the Lost Data FF (Z12 module, page 17) is set. A lost Data condition occurs in Read Mode when a second key is pressed before data generated by the previous key has been transferred to the computer. Information from the second key is lost and the TTY goes into a Break condition.

LOST DATA

A teletypewriter Lost Data status is indicated by bit 06 of the station 1 Status Word being a logical "1". The Lost Data status bit is sent to the Common Synchronizer from 17-C14-20. For this bit to be a logical "1", the Lost Data FF (Z12 module, page 17) is set.

PROTECTED

The teletypewriter is a non-protected device and, hence, status bit 07 will always be a logical "0".

READ MODE

The teletypewriter Read Mode status is indicated by bit 09 of the station 1 Status Word being a logical "1". The Read Mode status bit is sent to the Common Synchronizer from 13-C16-10. For this bit to be a logical "1", the Write Mode FF (Z13 module, page 13) must be clear. This is accomplished by:

(1) a Master Clear, Equipment Clear or Station 1 Clear Controller, or

(2) a Read Mode function command.

In the Read Mode, data transfers from the teletypewriter to the computer. If the Read Mode status bit is a logical "0", it indicates the Write Mode FF is set. This is accomplished by a Write Mode Function command. In the Write Mode, data transfers from the computer to the teletypewriter.

MANUAL INTERRUPT

The teletypewriter Manual Interrupt status is indicated by bit 11 of the station 1 Status Word being a logical "1". The Manual Interrupt status bit is sent to the Common Synchronizer from 17-C13-23. For this bit to be a logical "1", the Manual Interrupt FF is set which indicates closure of the MANUAL INTERRUPT switch on the teletypewriter. This FF remains set until cleared by:

(1) Master Clear, Equipment Clear or station 1 Clear Controller, or

(2) a station 1 Clear Interrupt function command.

FUNCTION

Functions of the 1700 low speed teletypewriter are controlled by a Function Code sent to the teletypewriter controller from the computer. This code is placed in the computer A Register Prior to execution of an output non-data transfer (Q00 = "1") to low speed station 1. Bits within the Function Code each have particular significance regarding functional operations being requested.

The Function Code bit significance for the 1711 and 1712 options is given in table 2-3; that for the 1713 option is given in table 2-4.

A00	Clear Controller
A01	Clear Interrupt
A02	Select Data Interrupt
A03	Select End of Operation Interrupt
A04	Select Alarm Interrupt
A05 - A07	Unused
A08	Select Write Mode
A09	Select Read Mode
A10 - A14	Unused

Table 2-3

1711/1712 Function Code Bit Significance

A00	Clear Controller
A01	Clear Interrupt
A02	Select Data Interrupt
A03	Select End of Operation Interrupt
A04	Select Alarm Interrupt
A05	Start Tape
A06	Stop Tape
A07	Unused
A08	Select Write Mode
A09	Select Read Mode
A10	Select K Mode
A11	Select KT Mode
A12	Select T Mode
A13	Select TTs Mode
A14	Select TTr Mode
A15	Unused

Table 2-4

1713 Function Code Bit Significance

The function logic operations explained in the following paragraphs is for the 1711/1712 options, using diagram #60164200, pages 13 through 25.

CLEAR CONTROLLER

A teletypewriter Clear Controller function is indicated by bit 00 of the Function Code from the computer being a logical "1". This bit enters the TTY controller at 15-C12-2 along with a Function command at 13-B19-28, and the Equipment 1, Station 1 signal at 13-B19-6. If a Clear Controller function is sent to the teletypewriter controller it will perform the function, provided neither the Mech. Busy FF (page 23) nor the Break FF (page 17) are set. These conditions will satisfy the AND gate at TP △2 (Z22 module, page 15), generating Clear Controller signals which will master clear the controller logic. The logical "0" at 15-C12-12 will generate a Reply to the Common Synchronizer which is sent on to the computer.

If the Clear Controller function is attempted with the TTY controller either in a mechanical busy or a break condition, the function will not be performed and a Reject is returned to the Common Synchronizer. The TTY Reply/Reject logic is contained in the Z15 module on page 13. Every station 1 Function will cause a logical "1" to be generated at 13-B19-11 which starts a 2 usec time delay before the Reject FF can set. If the function is performed, a logical "0" will appear at the appropriate input pin to the Z18 module (page 13). A logical "1" will leave 13-C04-15 and start a 1 usec time delay. If the Reply time delay times out before the Reject time delay, a Reply signal is returned to the Common Synchronizer indicating the function was performed. If the Reject time delay is the first to time out, a Reject is returned to the Common Synchronizer indicating the Function was not performed.

Note that the Clear Controller command also clears the Data Holding Register (logical ones at 15-C12-26 and -24) and clears the Data Read FF (Logical "1" at 15-C12-13). This means that any data previously held in the Holding Register has been lost. Note also that this function clears the Write Mode FF (page 13), automatically placing the TTY in Read Mode.

CLEAR INTERRUPT

A teletypewriter Clear Interrupt function is indicated by bit 01 of the Function Code from the computer being a logical "1". This bit enters the TTY controller at 17-C13-28. If a Function command (13-B19-28) and the Equipment 1 Station 1 signal (13-B19-6) also enter the TTY controller, the AND gate fed by TP △5 (Z14 module, page 17) will be satisfied causing a logical "0" to appear at 17-C13-14 and the [I] logic to output a logical "1". The [I] logic will clear all the FFs in the Z14 module while the logical "0" output of 17-C13-14 will generate a Reply to the Common Synchronizer.

NOTE: With the exception of the Manual Interrupt FF, the Clear signal into the interrupt enable FFs is momentary. This is to give priority to interrupt selection. Issuance of a Clear Controller or a Clear Interrupt function will only clear those interrupt enable FFs which are not being selected via bits 02, 03, or 04.

SELECT DATA INTERRUPT

A teletypewriter Select Data Interrupt function is indicated by bit 02 of the Function Code being a logical "1". This bit enters the TTY controller at 17-C13 -1. If a Function Command (13-B19-28) and the Equipment 1, Station 1 signal (13-B19-6) are also present, AND gate (F) (Z14 module, page 17) will be satisfied causing the Data Interrupt Enable FF to set. This will be used to interrupt the computer due to the presence of data (Read Mode) or the need for data (Write Mode).

SELECT END OF OPERATION INTERRUPT

A teletypewriter Select End of Operation Interrupt function is indicated by bit 03 of the Function Code being a logical "1". This bit enters the TTY controller at 17-C13-6. If a Function command (13-B19-28) and the Equipment 1, Station 1 signal (13-B19-6) are also present, AND gate (G) (Z14 module, page 17) will be satisfied. This causes the End of Operation Interrupt Enable FF to set. This will interrupt the computer at effectively the time the controller goes into a Not Busy status.

SELECT ALARM INTERRUPT

A teletypewriter Select Alarm Interrupt function is indicated by bit 04 of the function code being a logical "1". This bit enters the TTY controller at 17-C13-22. If a Function command (13-B19-28) and the Equipment 1, Station 1 signal (13-B19-6) are also present, AND gate (H) (Z14 module, page 17) will be satisfied. This will cause the Alarm Interrupt Enable FF to set. With this FF set, any condition which generates an Alarm status ($\overline{\text{Ready}}$ + Lost Data) will cause an interrupt to be sent to the computer.

SELECT WRITE MODE

Due to its close relationship with Data Write operations, the Select Write Mode discussion is postponed until the Data Write topic. This will provide you with a better understanding of the TTY controller status just prior to data transfer in the Write Mode.

SELECT READ MODE

Due to its necessity in preparing for Data Read operations, the Select Read Mode discussion is postponed until the Data Read topic.

READ DATA

Before data can transfer from the low speed teletypewriter controller to the computer, the TTY station must be placed into the Read Mode and data must be available in the Holding Register. Placing the TTY controller in Read Mode can be accomplished by:

(1) any operation which causes the TTY station to clear, such as Master Clear, Equipment Clear or Clear TTY Controller.

(2) a Select Read Mode function command.

SELECT READ MODE

A teletypewriter Select Read Mode function requires that bit 09 of the Function Code be a logical "1". This bit enters the TTY controller at 13-C16-11 where it will satisfy AND gate (B) provided:

(1) the controller is not busy, and

(2) a TTY Function is being requested.

Whenever AND gate (B) becomes satisfied, the Write Mode FF clears and the AND gate at TP △4 is broken. The following signals emerge from the Z13 module:

(1) logical ones at 13-C16-5, 10, and 8.

(2) logical zero at 13-C16-14.

The logical zero at 13-C16-14 will set the Reply FF, sending a Reply to the Common Synchronizer.

The signal leaving 13-C16-10 provides a Read Mode status bit. The signal leaving 13-C16-8 creates a 100 nsec pulse which clears:

(1) the Data Read FF (Z12, page 17).

(2) the Data Holding Register (page 25).

The signal which leaves 13-C16-5 provides an enable for keyboard entry. When a key on the keyboard is depressed, code bars within the TTY engages and rotates a cam containing ten lobes. As the cam rotates, each lobe is positioned with its respective code bar in such a manner that only one code bar can be monitored at a time.

If a lobe makes contact with a code bar, indicating a mark condition, a logical "1" is sent to the controller via the keyboard line (23-C11-4). If the lobe fails to make contact with a code bar (indicating a space condition), a logical "0" is sent to the controller. Circuits in the controller convert the non-logic level signals to logic level.

The first code bar monitored during cam rotation represents a Start signal to synchronize the controller logic with cam rotation speed. The code bar for the Start signal will always cause a logical "0" to appear at TP 2 of the Z19 module (page 23). This signal is shaped into a 100 nsec pulse by the Start Detector (Page 23) which is used to:

(1) Set the Mechanical Busy FF (23-C06-2).

(2) Set the Clock Control FF (19-C04-19).

(3) Enable setting the Lost Data FF (17-C14-25). If the Data Read FF is set, the Lost Data FF will set at this time.

(4) Clear Tape Motion FF (25.1-C17-20).

Setting of the Clock Control FF causes the Clock FF (Z18, page 19) to set. Setting of the Clock FF causes a 100 nsec Clock 1 pulse to be generated at 19-C05-9. The Clock 1 pulse is applied to the Timing Chain (page 21), causing the first FF (TP 4) to set. (All Timing Chain FFs had been previously cleared.) This produces a logical "0" from 21-C08-7 which prevents the contents of the Data Holding register from being printed prematurely.

After a 4.5 msec time delay, the set output of the Clock FF (page 19) causes the Strobe FF to set. This has no effect upon the Data Holding Register at this time since the Receive Enable Strobe circuit (page 19) is disabled by the logical "0" (space) from the keyboard line (logic [A] , Z19 module, page 23).

After a delay of 4.5 msec, the set output of the Strobe FF (page 19) clears the Clock FF. This causes a 100 nsec Clock 2 pulse (19-C05-20) to be applied to the Timing Chain (page 21). This sets the second FF in addition to the first, giving time 2 (t2) of the Timing Chain. At t2, the Start Detector logic (page 23) is disabled by the logical "0" from 21-C08-15. Also at t2, transfer of bit 00 from the keyboard line into the lowest bit of the Data Holding Register is enabled ("0" from 21-C08-4) as soon as the next Receive Enable Strobe signal is generated. The receive Enable Strobe signal will be produced when the Strobe FF clears (page 19) if the next code bar monitored sends a "1" into the controller via the keyboard line (23-C11-4). If the code bar sends a "0" into the controller, no transfer is needed since the FF is already cleared.

The clock control circuits (page 19) continue advancing the Timing Chain and generating transfer pulses into the Data Holding Register until the 7-bit character code and the parity bit (even) have been transferred. The Timing Chain advances by setting each FF left to right, then clearing each FF left to right. Each time a FF changes state, a new time is generated. Considering the first change to be t1, the second change t2, etc., the following table summarizes the events which occur with each time generated from t1 until the timing chain is returned to an all-cleared status (t12).

Keyboard Line Information	Timing Chain	Operation
Start Pulse	t1	Generate Start Pulse
Data Bits	t2	Generate Disable Start Detector & transfer bit 00 into Holding Reg. & printer
	t3	Transfer bit 01 into Holding Reg. & printer
	t4	Transfer bit 02 into Holding Reg. & printer
	t5	Transfer bit 03 into Holding Reg. & printer
	t6	Transfer bit 04 into Holding Reg. & printer
	t7	Transfer bit 05 into Holding Reg. & printer
	t8	Transfer bit 06 into Holding Reg. & printer
	t9	Transfer bit 07 into Holding Reg. & printer
Stop Pulse	t10	Stop pulse to printer
	t11	Timing Chain Cleared Sig., Set Data Read, Clear Clock control & stop pulse to printer
	t12 (t00)	Clear Disable Start Detector Signal.

Table 2-5

TTY Timing Chain Events for Read

Setting of the Data Read FF (Z12, page 17) holds the Busy Status (Z36, page 23), enables generating a Data Interrupt (Z14, page 17), and enables the computer to read the contents of the Holding Register (Z13, page 13).

A $\overline{\text{Busy}}$ 23-C06-(A) is used to generate End of Operation signals at 23-C06-21 and 23-C06-23. The signal from 23-C06-21 produces an End of Operation Status

23-C06-21 produces an End of Operation Status (Bit 04) while the signal from 23-C06-23 enables generation of an End of Operation Interrupt (17-C13-17).

The last (10th) code bar monitored generates a Stop command which is twice as long as any other keyboard line entry. This Stop command is sent to the printer which releases the TTY clutch, causing cam rotation to stop. One cam rotation requires 100 msec with 9 msec allowed for monitoring each of the first 9 code bars and 18 msec for the 10th code bar.

When the Clock Control FF clears (t11), a variable time delay is initiated (19-Z20-4) after which time a 100 nsec pulse is generated which clears the Mech. Busy FF (page 23). The delay time on this variable delay is adjusted so that the set duration of the Mech Busy FF is 100 msec. From this time on, the computer can initiate a character transfer from the TTY Holding Register to the 1704 A Register. If this transfer does not occur before the next start pulse arrives on the keyboard line, a Lost Data Condition will result.

READ DATA OPERATION

When the computer executes an Input instruction and the TTY is selected, a Read signal appears at 13-B19-26. If the Data Read FF (page 17) is set and the Write Mode FF (page 13) is clear, a Read Enable signal is generated which:

(1) transfers the contents of the Holding Register to the 1704 A Register.

(2) sends a Reply to the 1704 after a 1 usec delay.

(3) generates a 100 nsec clearing pulse (page 15) for the Holding Register (page 21) and the Data Read FF (page 17).

Clearing of the Data Read FF disables the TTY Busy status. This places the TTY in the proper condition for another keyboard entry or for a change of mode. If another TTY key is pressed (or a character read on the P. T. Reader), the preceding operations will be repeated.

Should a Read signal be applied to the TTY under conditions which prevent generating a Read Enable signal (i.e., Data Read FF clear or Write Mode FF set), a Reject is sent to the computer.

LOST DATA

If the contents of the Data Holding Register have not been transferred to the computer before another keyboard line transfer occurs, the Lost Data FF (page 17) will be set by the Start signal entering the controller from the keyboard line. When the Lost Data FF sets:

(1) a lost data Status is produced (17-C14-20).

(2) the Break FF (page 17) sets.

(3) a 180 msec time delay is started.

Setting of the Break FF prevents the keyboard entry from transferring into the Holding Register (page 23). The Break FF also holds a Busy status throughout the 180 msec delay. These two operations insure that previously held data will not be destroyed and that this data cannot be read during the 180 msec time delay in progress.

During the 180 msec delay period, the keyboard becomes locked so that other keys cannot be depressed, the paper tape reader (if running) is stopped and a BREAK light on the TTY console is illuminated. The period of 180 msec without transmission is equivalent to a NULL-NULL Code which will cause remote stations to disconnect. To unlock the keyboard, it is necessary to press the BREAK REL (Break Release) button on the keyboard. This also turns off the BREAK light. Even with the keyboard unlocked, read operations cannot continue until the Lost

Data FF (page 17) is cleared.

Clearing of the Lost Data FF (page 17) can be done either of two ways:

(1) By any operation which clears the TTY station (M.C., Equipment Clear or Clear Controller).

(2) By a Select Write Mode function.

If the programmer elects the first method, he will lose the character presently held in the Holding Register. The second method will not disturb the Holding Register contents provided data transfer does not take place in the Write Mode.

To continue Read operations from the point where data was actually lost, the following procedure is recommended:

Keyboard Entry

(1) Release the keyboard by pressing Break Release.

(2) Press Backspace Key two times on keyboard.

(3) Execute clear controller function.

(4) Continue with Read Data operations.

Paper Tape Reader Entry

(1) Release the keyboard by pressing Break Release.

(2) Press Backspace Key three times on keyboard.

(3) Execute Clear Controller Function.

(4) Continue with Read Data operations.

NOTE: During the 180 msec Break condition, the paper tape reader passes two frames before stopping.

Even with the keyboard locked up, write data operations can be performed after selection of the Write Mode.

WRITE DATA

Before data can transfer to the low speed teletypewriter Controller from the computer, the TTY station must be placed into the Write Mode. Placing the TTY Controller in Write Mode can be accomplished by a Select Write Mode Function.

SELECT WRITE MODE

A teletypewriter Select Write Mode function is indicated by bit 08 or the function code being a logical "1". This bit enters the TTY controller at 13-C16-12. If a Function Command (13-B19-28) and the Equipment 1, Station 1 signal (13-B19-6) are also present, AND gate Ⓐ (Z13 module, page 13) will be satisfied if the controller has a $\overline{\text{Busy}}$ status (13-C16-9). Satisfaction of AND gate Ⓐ will cause the Write Mode FF to set (placing the controller in Write Mode) and generate a logical "0" at 13-C16-14 which will cause a Reply to be sent to the Common Synchronizer.

With the setting of the Write Mode FF,the AND gate feeding TP $\triangle$2 becomes enabled and Write Mode signals leave the module at pins 1, 6, and 4. The logical "1" outputs of pins 1 and 6 enable the contents of the Holding Register (page 25) to be sampled by the receiving unit (page printer and/or paper tape punch). The logical "1" output of pin 4 enables the Data status bit at 17-C14-8. In Write Mode, this status bit becomes a "1" whenever the Data Write FF sets. The conditions for setting this FF a ($\overline{\text{Busy}}$) ($\overline{\text{Read}}$ + $\overline{\text{Write}}$). The $\overline{\text{Busy}}$ condition already exists (a prerequisite to setting Write Mode FF). The $\overline{\text{Read}}$ + $\overline{\text{Write}}$ condition is not met, however, until the computer receives a Reply or Reject signal.

Assuming normal operations, the Reply to the computer drops the Write signal which, in turn, sets the Data Write FF (page 17) and clears the Reply FF (page 13). With the Data Write FF set, a Data status bit (17-C14-8) is sent to the Common Synchronizer, an interrupt on data is enabled (AND gate (A), Z14 module, page 17) and a Data Write signal is applied to 13-C16-22. At this point, Data Write operations can commence whenever the computer performs an output data transfer to the station 1 Holding Register.

WRITE DATA OPERATION

When the 1704 executes an Output instruction to the TTY, a Write signal appears at 13-B19-24. This generates Write Enable signals from module Z13 if the Write Mode and Write Data FFs are set. The Write Enable signals cause:

(1) a Reply to the 1704 after a 1 usec delay.

(2) transfer of data bits from the 1704 A Register to the Holding Register (page 21).

(3) setting of the mech Busy FF and the Start Motor FF (page 23).

(4) setting of the Clock Control FF (page 19).

If the Write Enable signal cannot be generated (Write Mode FF or Data Write FF clear), a Reject is sent to the 1704. Receipt of either a Reply or Reject by the 1704 will cause the Write signal to drop while the computer continues at the appropriate program step. When the Write signal drops, the Write Data FF (page 17) clears.

Setting of the Clock Control FF (page 19) will cause the Clock FF to set. This generates a 100 nsec Clock 1 pulse which advances the Timing Chain (page 21) to time 1 (t1). The Clock FF also starts a 4.5 msec time delay. At time 1, a Start Pulse (21-C08-7) is generated which sends a Start signal ("0") to the Printer

Line (Z19, page 23), causing synchronization of the TTY with the controller logic.

The Strobe FF (page 19) sets 4.5 msec after setting of the Clock FF. After another 4.5 msec delay, the Clock FF clears. This generates a 100 nsec Clock 2 pulse which advances the Timing Chain to t2. During t2, bit 00 of the Holding Register is transferred to the Printer Line (Z19, page 23).

The clock circuitry cycles once every 9 msec. With each cycle of the clock circuitry, the Timing Chain advances one time. The following table shows the events which occur with each time generated by the Timing Chain.

t1	Start Pulse
t2	Holding Reg. bit 00 to Printer Line
t3	Holding Reg. bit 01 to Printer Line
t4	Holding Reg. bit 02 to Printer Line
t5	Holding Reg. bit 03 to Printer Line.
t6	Holding Reg. bit 04 to Printer Line
t7	Holding Reg. bit 05 to Printer Line
t8	Holding Reg. bit 06 to Printer Line
t9	Holding Reg. bit 07 to Printer Line
t10	Nothing
t11	Timing Chain Cleared signal & Clear Clock Control FF.
t12	Nothing

Table 2-6

Timing Chain Events for Write

After a 12 msec delay, the Timing Chain Cleared signal (page 21) generates an End of Operation status (page 23) and enables an End of Operation Interrupt to the computer. Clearing of the Clock Control FF (page 19) initiates a variable delay after which time a 100 nsec pulse is generated which clears the Mech Busy FF (Z16, page 23).

Clearing of the Mech Busy FF causes a $\overline{\text{Busy}}$ Status to occur which, in turn, sets the Write Data FF (page 17). Setting of the Write Data FF causes a Data status and enables a Data Interrupt to the computer. At this time, the TTY is in a position to accept another character from the computer.

CHAPTER III

PAPER TAPE READER CONTROLLER

CHAPTER III

PAPER TAPE READER CONTROLLER

INTRODUCTION

The 1700 Paper Tape Reader comes in six models. The 1721A consists of a controller and a 350 Reader which operates from 50cps power. The 1721B consists of a controller and a 370 Reader which operates from 60cps power. The 1721C consists of a controller and a 350 Reader which operates from 60cps power. The 1721D consists of a controller and a 370 Reader which operates from 60cps power. The 1722 is a 1721 with the Reader containing a Remex Tape Spooler (available in 60cps power only).

Table 3-1 shows the Function Codes and table 3-2 shows the status codes for the Paper Tape Reader.

A00 - -	Clear Controller
A01 - -	Clear Interrupt
A02 - -	Select Data Int.
A04 - -	Select Alarm Int.
A05 - -	Start Motion
A06 - -	Stop Motion

Table 3-1

P. T. Reader Function Codes

A00 - -	Ready
A01 - -	Busy
A02 - -	Interrupt
A03 - -	Data
A05 - -	Alarm
A06 - -	Lost Data
A07 - -	Protected
A08 - -	Controller present
A09 - -	Paper Mot. Fail.
A10 - -	Power On

Table 3-2

P. T. Reader Status Codes

The paper tape reader must be loaded with tape before operation can begin. Power is applied by pressing the READER POWER switch. The controller is made ready for operation by pressing the READY/MASTER CLEAR switch on the reader. The reader is now ready for operation. In this state Ready and Power On status signals are available to the computer.

START PAPER TAPE MOTION

To start paper tape motion, the computer sends to the Paper Tape Reader a function code having bit 05 a "1". This enters the controller logic at 31-A16-20, causing the Start FF to set. With the setting of the Start FF, a busy status is produced (31-A15-22), and the Clutch FF set input is enabled. The Clutch FF will set if the condition ($\overline{\text{Lost Data}}$) ($\overline{\text{Data Ready}}$) is met. These conditions are met following a clear controller since the Lost Data FF and the Data Ready FF are cleared (page 29).

When the Clutch FF (page 31) sets, the clutch in the reader becomes engaged, causing tape to begin moving (27-C20-20).

A reply to any Paper Tape Reader function code is returned automatically to the computer. The Reply signal causes the computer to continue with its program at instruction step P + 1.

With the setting of the Clutch FF, a 40 msec time delay is initiated (29-A12-2). If this time delay times out before a feedhole is sensed, it indicates that paper is not moving through the reader. Consequently, the Paper Motion Failure FF (page 29) will be set. This gives a Not Ready status, enables the Alarm Interrupt and gives a Paper Motion Failure (Alarm) status.

In normal operation, a Feedhole is sensed before the 40 msec time lapse. The Feedhole signal enters the controller at 27-C20-16 and generates logic ones at 27-C20-13 and 27-C20-15. The output of 27-C20-13 will cause the Feed 1 FF (page 31) to set if the following conditions are met: ($\overline{\text{Paper Motion Failure}}$) (Clutch) ($\overline{\text{Feed 2}}$). The output of 27-C20-15 is ANDed with the Clutch signal (Z09 module, page 29) and starts a second 40 msec time delay (29-A12-3). If this delay times out, it also will mean that paper is not moving through the reader. The Paper Motion Failure FF will set.

When the Feed 1 FF (page 31) sets, it will:

(1) Enable setting of the Data Ready FF (page 29).

(2) Enable setting of the Lost Data FF (page 29).

(3) Generate a 100 nsec pulse which clears the Holding Register (page 27).

(4) Initiates a 400 usec delay (page 29).

(5) Transfers data from the read station photo diodes to the Holding Register.

The 400 usec time delay insures that data transfer into the Holding Register occurs during that time when the punched data holes are positioned directly over the read station photo diodes. After the 400 usec time delay, a Delayed Feedhole signal sets the Feed 2 FF (page 31).

When the Feed 2 FF sets, a logical "0" appears 29-A14-13 which:

(1) disables the first 40 msec time delay (29-A12-2)

(2) sets the Data Ready FF if the following conditions are met: (Reader Ready) (Feed 1) ($\overline{\text{Lost Data}}$).

Setting of the Data Ready FF (page 29) will:

(1) provide a Data status bit (31-A16-23) if the Start FF is still set and one of the following conditions are met: ($\overline{\text{Read}}$) + ($\overline{\text{Protect Fault}}$).

(2) Enables a Data interrupt to the computer if the Data Interrupt FF (page 31) is set.

(3) set Lost Data FF (page 29) if the Feed 1 FF is still set.

(4) Disable the set input to the Clutch FF (page 31).

(5) Clear the Clutch FF upon the trailing edge of the feedhole signal if a Data Interrupt has not been selected. This will cause paper motion to stop.

(6) Enable the clear input to the Feed 1 FF (page 31)

(7) Clear the Feed 1 FF (page 31) if the feed 2 FF is set.

When the feedhole passes the read station, the Feedhole signal drops, enabling several operations to occur:

(1) Stop tape motion if a Data Interrupt has not been selected. This allows reading one frame and stopping until the information is

transferred to the computer. After the transfer, the reader starts motion automatically, reading the next frame and stopping, etc.

(2) Stop tape motion if a Lost Data condition exists.

(3) Stop tape motion if the Start FF has been cleared.

(4) disables the second 40 msec time delay (29-A12-3).

(5) Clears the Feed 2 FF (page 31) as soon as the information signal drops. (Information signal drops when the data holes in the tape leave the read station.)

When the Feed 2 FF clears, the first 40 msec time delay (29-A12-2) is restarted if tape is still in motion. Information in the Holding Register is now available to the computer. If tape is still in motion, the information will have to be transferred from the Holding Register before the next Feedhole signal appears or a Lost Data condition will result.

READ DATA OPERATION

When the computer executes an Input instruction to the Paper Tape Reader, a Read Data signal appears at 31-A17-11. If the protect requirements are met and data is available, a Reply signal is generated at 31-A16-16. This Reply is sent to the computer allowing it to transfer data from the Holding Registers to the 1704 A Register, then to continue with program execution at P + 1. If the conditions for a Reply are not met, a Reject is sent to the computer preventing data transfer to the A Register and causing the program to continue at $P + \Delta + 1$.

Assuming normal operation, the Read signal will generate a Reply and clear the Data Ready FF (page 29). The Reply signal to the computer will cause the Read signal (31-A17-11) to drop. Clearing of the Data Ready FF will set the Clutch

FF (page 31) if it had been cleared and if the Start FF is still set.

Tape motion continues until one of the following events occurs:

(1) A Stop Function code is sent to the Paper Tape Reader (clearing the Start FF, page 31).

(2) A paper Motion Failure occurs (logical "0" at 31-A15-21) and Data Interrupt has not been selected.

(3) Loss of the feedhole signal (31-A15-23) and Data Interrupt has not been selected.

(4) Loss of the feedhole signal with the Lost Data FF set (31-A15-6).

It should be noted that under conditions of Lost Data, the previous frame of information is lost and the second frame is retained in the Holding Register. To restart the tape reader, both the Data Ready and the Lost Data FFs must be cleared. The Data Ready FF clears by a Read signal from the computer or a Master Clear whereas the Lost Data FF clears due to a Master Clear or a Clear Interrupt Function. If a Master Clear is used, two frames of information will be lost, since the Holding Register is also cleared.

CHAPTER IV

PAPER TAPE PUNCH CONTROLLER

CHAPTER IV

PAPER TAPE PUNCH CONTROLLER

INTRODUCTION

The NCR Model EM-B1 Paper Tape Punch is used in the 1700 Low speed System. The EM-B1 is capable of punching 120 characters/sec., using 5, 7, or 8, level tape. The 1723 consists of a controller and an EM-B1 Paper Tape Punch. The 1724 consists of a controller, an EM-B1 Paper Tape Punch and an EM-B2 handler.

Table 4-1 shows the Function Codes and table 4-2 shows the Status Codes for the Paper Tape Punch.

A00	-- Clear Controller
A01	-- Clear Interrupt
A02	-- Select Data Int.
A04	-- Select Alarm Int.
A05	-- Start Motion
A06	-- Stop Motion

Table 4-1

P. T. Punch Function Codes

A00	-- Ready
A01	-- Busy
A02	-- Interrupt
A03	-- Data
A05	-- Alarm
A07	-- Protected
A08	-- Existance Code
A09	-- Tape Break
A10	-- Power On
A11	-- Tape Supply Low

Table 4-2

P. T. Punch Status Codes

Paper tape must be loaded into the head of the paper tape punch before operation can begin. To make the Paper Tape system ready requires that the Power and the READY/MASTER CLEAR switches on the punch be pressed. The READY/MASTER CLEAR switch clears the controller for operation. A Power On status and a Ready status will be available to the computer at this time.

START PAPER TAPE MOTION

To start tape motion in the paper tape punch, the computer sends a Function Code having bit 05 a "1". This causes the Start FF (page 35) to set. With the setting of the Start FF, the following events occur:

(1) A Reply is sent to the computer (35-A10-16) provided the Ready & Protect requirements are met.

(2) A Busy Status is generated by the Paper Tape Controller (Z07, page 35).

(3) The Punch 1 FF set input is enabled (page 35).

The Reply signal to the computer causes the Function signal to drop and allows the computer to continue at program step P + 1. If a Reply could not have been generated ($\overline{\text{Ready}}$ or a Protect violation), a Reject would have been sent to the computer. This would also drop the Function signal to the Paper Tape Controller but the program would have continued at $P + \Delta + 1$.

When a Busy status is generated, the following events occur:

(1) A logical "1" at 35-A09-5 produces a Busy status bit (33-C19-17) and enables a Clear Pulse to clear the Feed and Punch 2 FFs (page 35).

(2) A logical "1" at 35-A09-13 starts an 800 msec time delay. This allows time for the punch motor to reach operating speed before pulses from the punch are acceptable to the controller.

(3) A logical "0" at 35-A09-10 disables the effect of the READY/MASTER CLEAR switch on the punch.

(4) A logical "0" at 35-A09-8 causes the punch motor to turn on.

After a delay time of 800 msec, the output of 29-A12-28 becomes a logical "1". This enables timing pulses (from a timing disc connected to the punch motor) to be recognized by the controller. The controller logic now awaits a Write Data signal from the computer.

WRITE DATA OPERATION

When the computer executes an Output instruction to the Paper Tape Punch, a Write Data signal appears at 35-A11-11. This causes the following events:

(1) A logical "1" at 35-A11-8, which will set the Punch 1 FF (page 35) if the following conditions are met: (Ready) (Protect OK) (Start) ($\overline{\text{Punch 2}}$).

(2) A logical "0" at 35-A11-9, which will:

(a) Enable setting the Ready & Protect OK FF (center of module Z06, page 35) if Data status is present and Ready and Protect requirements are met.

(b) Transfer data from computer A Register to the Holding Register (page 33).

Setting of the Punch 1 FF (page 35) will generate a Reply to the computer (35-A10-16). This will cause the write signal and data transfer to end, allowing the computer to continue with its program. Setting of the Punch 1 FF also removes the Data status bit at 35-A09-12. If the computer performs any more write operations with the punch before the Data status re-appears, a reject will be returned to the computer.

At some point in the revolution of the Punch timing disc, a Set Punch timing pulse is generated and appears at 33-C19-4. This pulse will cause the Punch 2 FF (page 35) to set if the 800 msec time delay has passed and the Punch 1 FF is set. Setting of the Punch 2 FF will cause the contents of the Holding Register and a Feedhole to be punched simultaneously on tape (page 33).

After a delay of 1.5 msec from the leading edge of the Set Punch timing pulse, a Set Feed timing pulse appears at 33-C19-2. This causes the Feed FF (page 35) to set if the Punch 2 FF is set. Setting of the Feed FF will clear the Punch 1 FF and generate a signal at 33-A07-19, which will begin the advancement of tape.

After a delay of 5 msec from the leading edge of the Set Punch timing pulse, a Clear Punch timing pulse appears at 33-C19-13. This causes the Punch 2 FF (page 35) to clear. With both Punch 1 and Punch 2 FFs clear, a Data status is generated and the Data Interrupt is enabled. The Holding Register is also cleared at this time.

At this point, the computer can send another character to be punched.

After a delay of 5 msec from the leading edge of the Set Feed timing signal, a Clear Feed timing signal appears at 33-C19-8. This clears the Feed FF (page 35), preventing further tape motion.

CHAPTER V

CARD READER CONTROLLER

CHAPTER V

CARD READER CONTROLLER

INTRODUCTION

The NCR Model EM-D2 (PE) Card Reader is used in the 1700 Low Speed System. This card reader is capable of reading approximately 100 cards/min. Card columns are read by photocells in the read station area of the card reader. The data is amplified by preamplifiers before being transferred to the card reader controller. The 1729 includes the controller logic and one card reader.

Table 5-1 shows the Function codes and table 5-2 shows the Status Codes for the card Reader.

A00--Clear Controller
A01--Clear Interrupt
A02--Select Data Int.
A03--Select E.O.R. Int.
A04--Select Alarm Int.
A05--Start Motion
A06--Stop Motion

Table 5-1

Card Reader Function Codes

A00--Ready
A01--Busy
A02--Interrupt
A03--Data
A04--End of Record
A05--Alarm
A06-- Lost Data
A07--Protected
A08--Controller Present
A09--Read Station Empty

Table 5-2

Card Read Status Codes

The Card Reader hopper (which can hold approximately 500 cards) is loaded with cards face down having row 9 to the rear of the stack. Pressing the REG (Register) switch on the card reader will move one card from the hopper to the read station. Two signals are then generated to the controller:

(1) One signal indicates that the read station is not empty ($\overline{\text{RSE}}$). This signal remains until the card leaves the read station.

(2) The other signal is a Field pulse (3.5 msec duration). The Field pulse and the $\overline{\text{RSE}}$ signal together set the Field 1 and the Stop FFs.

The Field 1 FF (Z28 module, page 39) sets on the leading edge of the Field pulse since the Field 2 FF is cleared. Setting of the Field 1 FF, enables the Field 2 FF to set and enables setting of the Stop FF (page 43). The Stop FF sets if the following conditions are met: ($\overline{\text{Field 2}}$) ($\overline{\text{Motion}}$) ($\overline{\text{RSE}}$). Setting of the Stop FF will produce a Not Busy status and enables a Start Motion Function.

after a 100 usec delay.

The trailing edge of the Field pulse will cause the Field 2 FF (Z28, page 39) to set. With Field 1 and Field 2 FFs both set, the Permit Read FF (Z27, page 37) sets. This FF sets the Ready FF (page 39) giving a Ready Status, Enables the Timing Chain (Z28, page 39), disables the set input to the End of Record FF (page 41) and enables clearing the Holding Register during time 2 of a timing chain cycle (43-C03-25).

Before the stop command to the Card Reader (43-B04-7) can take effect, column 1 appears over the read station photocells and a clock pulse (3.5 msec) enters the controller at 43-C03-6. This pulse enables the AND gate at TP ⚠5 (Z33, page 43). The purpose for this is to control the escapement between cards, and has no effect at this time. A clock pulse at 43-C03-7 will cause the timing chain to start.

The controller timing chain consists of two FFs located on the Z28 module, page 39. Normally these two FFs are cleared, indicating time 0 (t0). Cycling of the timing chain occurs in this fashion:

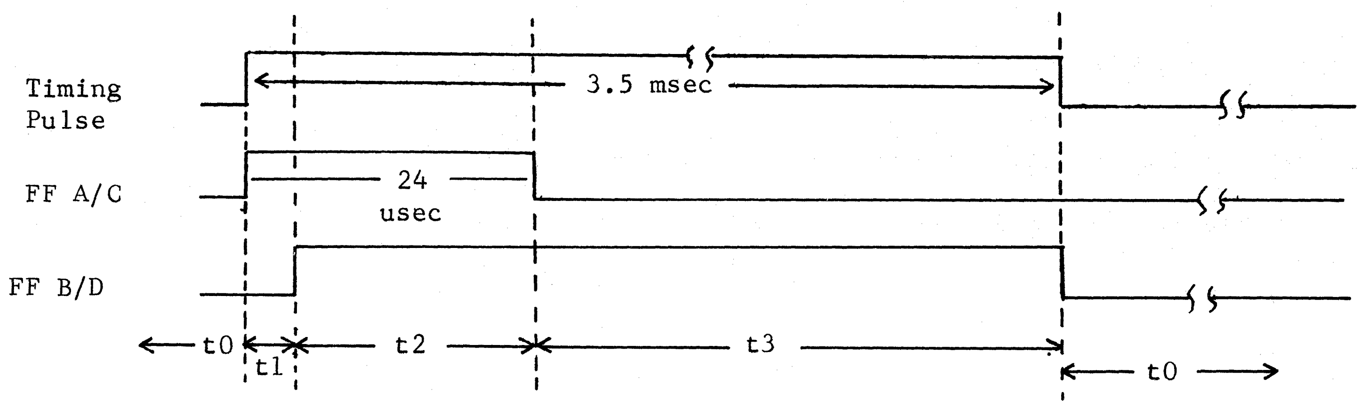
t0--both FFs cleared ([C] and [D] both equal ones)

t1--the top FF is set (logic [A] = "1"), the bottom FF is clear (logic [D] = "1")

t2--both FFs set ([A] and [B] both equal ones)

t3--top FF cleared ([C] = "1")

Figure 5-1 shows the FF relationship within the timing chain. Time t1 begins with the leading edge of the Clock pulse from the reader.



t0 = time between trailing edge of one clock pulse & leading edge of another clock pulse (approx. 3.5 msec)

t1 = 4 usec

t2 = 20 usec

t3 = time between end of t2 and trailing edge of clock pulse (approx. 3.25 msec)

Figure 5-1

Card Reader Timing Chain

Table 5-3 gives events accomplished during a timing chain cycle.

Time	Operation
t1	Clear Data Register (page 45)
t2	transfer data from read station to Data Register
t3	(only first 100 nsec used) set Data FF (page 41)
t0	Enable recycling timing chain

Table 5-3

Card Reader Timing Chain Cycle

At this point in time, column 1 of the card is over the read station, the information from that column has transferred to the Data Register, Card motion has stopped, a Ready, Data, and Not Busy status is being generated and the controller is in a position to transfer data to the computer.

The computer can transfer the column 1 data only after a Start Motion function command. If it inputs this data before starting motion, a Reject will be sent to the Common Synchronizer. If the card motion is started, a data transfer must occur before another frame enters the read station or data will be lost.

START CARD MOTION

When a Start Motion Function is executed by the computer to the Card Reader, a logical "0" appears at 41-B02-26 and a logical "1" appears at 41-B02-27. This sets the Reply FF, sending a Reply to the computer, and sets the Motion FF. Setting of the Motion FF will:

(1) Enable generating a Data Interrupt when Data becomes available if a data interrupt has been selected (page 37).

(2) Set the Alarm FF (page 41) if the read station has been empty for 30 msec or more or if the card reader is not ready.

(3) Disable the set input and clear the Stop FF (page 43).

(4) Enables setting of the Ready FF (page 39).

When column 2 of the card appears over the read station photocells, another 3.5 msec clock pulse appears at 43-C03-6, causing the timing chain to cycle and the information to transfer to the Data Register. This procedure repeats with each frame passing the read station.

READ DATA OPERATION

When the computer executes an Input instruction to the Card Reader, a Read Data signal appears at 41-B02-8. This causes the Reply FF to set if the Data and the Motion FFs are set. Setting of the Reply FF sends a Reply to the Computer and clears the Data FF.

With the card in motion, as soon as each column enters the read station, another clock pulse appears at 43-C03-6. The clock pulse starts the Timing chain and the read operation repeats. This procedure continues until column 79 enters the read station.

When column 79 enters the read station, a second Field pulse appears at 39-A03 -23. The leading edge of this pulse clears the Field 1 FF (page 39). (The Field 2 FF remains set.) The Clock 79 pulse starts the controller Timing Chain, as before, and the information is transferred from column 79 to the Data Register. The trailing edge of the Field pulse clears the Field 2 FF (page 39).

Card motion continues until column 80 appears under the photocells in the read station. Clock pulse 80 starts the Timing Chain, as before, and the information is transferred from the card to the Data Register. At time 3 of the timing chain, however, the Permit Read FF (page 37) is cleared since Field 1 and Field 2 FFs are both cleared. This time, when the information is transferred to the computer and the Data FF is cleared (page 41), the End of Record FF (page 41) becomes set. This sends an End of Record status to the Common Synchronizer indicating the end of the card. The end of Record FF self-clears after 1 msec. A status check must be performed during the 1 msec time interval or it will be missed.

When the card leaves the read station, a Read Station Empty signal appears at 43-C03-8, forcing logical ones at 43-C03-11 and -9 and logical zeros at 43-C03-12 and -10. The logical "1" at 43-C03-11 causes:

(1) a FF to clear in the Z33 module, page 43, which enables AND gate (E)

(2) the [L] logic in the Z33 module to output a logical "0" which disables the set input to the Stop FF.

The logical "1" from 43-C03-9 starts a 30 msec time delay on Page 47. If this delay times out, it means the hopper is empty and no more cards are to be read. The logical zeros from 43-C03-12 and -10 prevent the controller from reacting to any more clock pulses.

If the card leaving the read station is not the last card to be read, another one will enter the read station before 30 msec have elapsed since the Read Station Empty signal was generated. As the old card leaves the read station, pressure rollers are raised. In the raised position, these rollers cause a ground to appear at 43-B04-10. With the arrival of clock pulses (clock pulses are generated until column 82), the AND gate at TP △5 (Z33 module, page 43) is satisfied. This generates a 3.5 msec stop pulse to the excapement control circuit in the card reader -- a requirement to insure that the incoming card is positioned squarely into the read station. Since these Stop pulses are only momentary, they do not, in fact, stop the card reader operations.

As soon as a new card enters the read station, the Read Station Empty signal (43-C03-8) drops, causing card movement to continue through the read station. The first Field pulse will appear, followed by the Clock pulse for column 1. This will cause Field 1 and Field 2 FFs to set (page 41), the timing chain to cycle, information to transfer from column 1 to the Data Register, the Stop FF to set and the Motion FF (page 41) to clear, allowing the card to stop on column 1. When the card stops, a Ready Status is generated and the controller awaits a Start Motion Function to continue. The previously explained operations repeat for the reading of this card.

If the card leaving the read station is the last card, the 30 msec delay (47-B05 -2) will time out sending a RSE + 30 msec signal to 43-B04-18. This will generate a Read Station Empty Status (43-B04-17), satisfy AND gate (E) (which sends a Stop signal to the reader, causing mechanical movement to stop) and sets the Alarm FF (page 41).

LOST DATA

If the computer does not accept data from the Data Register before the next column enters the read station and the Clock pulse is generated, data in the Data Register will be lost. At time 1 of the Timing Chain, the Lost Data FF would set causing:

(1) The Alarm FF (page 41) to set, giving an Alarm status and enabling an Interrupt on Alarm.

(2) The Data FF (page 41) to clear, removing data status.

(3) The Motion FF (page 41) to clear so that the next card to enter the read station stops on column 1.

When Lost Data occurs, the card continues to move through the card reader but signals from the reader have no effect upon the controller logic. When the next card enters the read station, the $\overline{\text{RSE}}$ signal clears the Lost Data FF and removes Lost Data Status. The Alarm status remains until cleared by the proper Function code (or Master Clear). A normal read can now be performed on the card presently in the read station.

START MOTION DURING CARD READ

If a Start Motion function is requested while a card is moving through the read station, logic gate [D], Z30 module, page 41, outputs a logical 1. This will set the FF whose cleared output is [C], near the top of the module. When this FF sets, the set input to the Data FF becomes disabled preventing Data Status.

When the next clock pulse enters the controller and starts the timing chain, at t3 the FF at TP (4) sets but cannot clear, since the Data FF cannot set. The cleared output of the t3 FF (logic gate [I]) disables the Read Data Reply path so that attempts to read throughout the remainder of this punched card will result in Rejects to the computer. After this card leaves the read station and a new card enters, read operations may be resumed (the leading edge pulse of the $\overline{\text{RSE}}$ signal clears the FF at 41-B02-19).

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III