CYBER 18-20 MAINTENANCE AND TROUBLESHOOTING

SUPPLEMENTARY REFERENCE MANUAL

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Block 1

System Troubleshooting

Processor Register Access (Text)

As a computer technician, you will be expected to diagnose system hardware failures. This activity describes use of the following maintenance aids available to help you in analyzing and solving hardware failures.

- Function control register use
- Control commands
- Macromemory access
- Breakpoint
- Auto display

Many aids in analyzing a hardware failure are available to the computer technician. There are manuals which explain the operation of equipment and those which give you valuable information on maintaining that equipment. There are software diagnostic tests which provide a valuable tool which you can use to define specific hardware problems. For example, the operational diagnostic system used by the CYBER 18 can usually define a system failure to a replaceable module or a specific adjustment. But what can you do to isolate a failing component in a functional area of logic? To do this, you must know how to access the functional logic suspected of failing and must be able to examine its operation. For example, suppose that each time an ADD operation using the A and X registers was performed, the answer came out wrong. A possible reason for this might be that the data contained in one of these two registers at the time the ADD operation was performed was incorrect. To check these registers for correct operation, you could enter a hexidecimal number into the A or X registers and then read the content from that register out to be displayed on the console as shown:

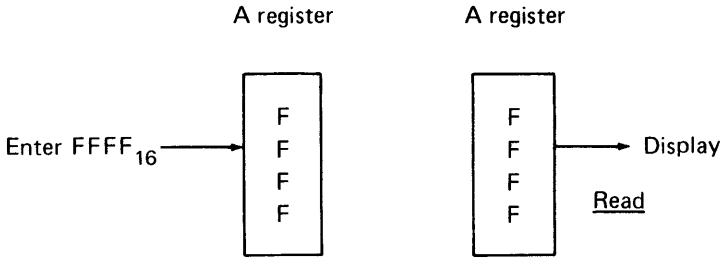


Figure 1. Register Entry and Display

If what is read from the register is the same as that entered, it verifies for the most part that the register is working properly. Suppose that the suspected failure was memory.

It may be that when attempting to enter data into memory, it is not written correctly; in other words, the data entered doesn't equal the data stored. It would be very useful for you to verify this problem by first entering a number into suspected memory locations, and then reading the contents of those locations. If the number read does not equal the number entered, as shown in the example, a definite problem exists.

Figure 2. Memory Errors

You should be able to analyze the information read and determine the failing component causing the memory problem.

Function Control Register

This activity will familiarize you with the methods which can be used to access the processor's registers and memory. To do this the CYBER 18's function control register (FCR) must be understood, since it is the basic means of communication between the microprocessor and the operator. Through the function control register, many functions of the microprocessor can be accessed.

The function control register or FCR is a 32-bit register. Refer to table 1. The 32 bits are divided into 8 hexadecimal digits which can be grouped as follows.

Machine status digits: Digits 6 and 7 of the FCR are set by the microprocessor and indicate the machine status, such as overflow on/off, macromemory parity error, protect fault, etc. Any attempt to change these bits will cause an error, and the FCR will be displayed.

TABLE 1
Function Control Register (FCR)

Bits Decimal	Bits Hex	Digits	Bit Definitions
(LSB)31	1F	7	Overflow
30	1E		Not Protected Instruction*
29	1D		Protect Fault*
28	1C		Parity Error*
27	1B	6	Interrupt System Active*
26	1A		Auto-Restart Enabled
25	19		Micro Running
24	18		Macro Running*
23	17	5	Not used
22	16		Not used
21	15		Enable Auto Display
20	14		Enable Console Echo
19	13	4	Enable Micro Memory Write
18	12		Multilevel Indirect Addressing Mode*
17	11		Not used
16	10		Suppress Console Transmit
15	0F	3	0 0 Breakpoint Off 0 1 Instruction Reference Breakpoint 1 0 Storage Operand Breakpoint 1 1 All References Breakpoint
14	0E		
13	0D		Breakpoint Interrupt (BP Stop if Clear)
12	0C		Micro Breakpoint, Step, Go, Stop (Macro if Clear)
11	0B	2	Step
10	0A		Selective Stop*
09	09		Selective Skip*
08	08		Protect Switch*
07	07	1	Display 1
06	06		
05	05		
04	04		
03	03	0	Display 0
02	02		
01	01		
(MSB)00	00		

Status Only

*These FCR bits may be assigned as desired, depending on the microprocessor application. The definitions shown are standard for enhanced 1700 emulation.

Machine code digits: Digits 2 to 5 of the FCR are used to set such conditions as selective stop, on, off, step-run mode, etc.

Bits 14_{16} and 15_{16} of the FCR (enable console echo and enable auto display) are mutually exclusive; that is, the operator may select one or the other, but not both simultaneously.

Digit 3 of the FCR (bits $0C_{16}$ to $0F_{16}$), breakpoint, is applicable only if the user has the optional maintenance panel and panel interface card.

Digit 2 of the FCR (bits 08_{16} to $0B_{16}$) allows setting or clearing of the selective stop, selective skip, and protect bit switches.

Display digits: The display digits, 0 and 1, determine which individual registers or groups of registers (identified in table 2) can be displayed or modified.

Unassigned display codes (table 2) should be assumed to be undefined.

Selecting BP or P/MA (table 2) will result in both BP and P/MA being displayed. BP is the leftmost 16 bits and P/MA is the rightmost 16 bits. BP can be modified only if BP is selected; P/MA cannot be modified in either case.

Selecting N or K (table 2) results in both N and K being displayed. N is the left 8 bits and K is the right 8 bits. However, when K is selected, only the K register can be modified.

TABLE 2
Display Code Definitions

Codes		Display 1	Display 0
0	0 0 0 0	FCR	F2 (Addressed by N)
1	0 0 0 1	P*	N (MSBs)**
2	0 0 1 0	I	K (LSBs)**
3	0 0 1 1		X
4	0 1 0 0	A	Q
5	0 1 0 1	MIR	F
6	0 1 1 0	BP-P/MA (Display only)	F1 Addressed by K Enabled by SM111
7	0 1 1 1	P/MA (Display only)	MEM
8	1 0 0 0	SM1	
9	1 0 0 1	M1	$\overline{\text{RTJ}}$
A	1 0 1 0	SM2	
B	1 0 1 1	M2	
C	1 1 0 0		MM
D	1 1 0 1	A*	
E	1 1 1 0	X*	
F	1 1 1 1	Q*	

*Used to address macromemory. Automatically incremented after each memory reference.

**The combined contents of the K and N registers are used to address micromemory. The K register is automatically incremented after each memory reference. The N register does not automatically increment.

Control Commands

The control commands used in the panel interface mode include H, I, J, K, L, :, G, and ?. Control commands H through L are used to set or clear specific bits in the FCR or to display the contents of specific registers. The colon (:) or G performs an entry termination function. The question mark (?) generates a master clear to the microprocessor.

A normal entry consists of one of the control characters H through L, and two, four or eight hexadecimal digits (0 through F). The entry is then terminated by an entry of a colon (:) or a G. Two examples are given below. Note that the ESC key must also be depressed prior to entering the desired control information. The escape key (ESC) permits the operator to go into the panel mode and thus have access to the microprocessor registers.

1. Depress ESC key
2. Enter J04:
3. Enter LG

The contents of the Q register will be displayed on the CRT screen.

1. Depress ESC key
2. Enter J14G
3. Enter KG

The contents of the A register will be displayed on the CRT screen.

The control codes are used as follows.

H Key

The H key can be used as a macrostop if bit 12 of the FCR is clear and a microstop if bit 12 is set.

H : or HG (halt)

The CRT will display the contents of the function control register as a response to this entry.

The H control key may also be used to clear a specific bit in the FCR.

H14G clear enable console echo (FCR bit 14_{16})

The new contents of the FCR would be displayed on the CRT. Other examples of operation are shown below.

H08:	Clears the protect switch bit	(bit 08_{16})
H0C:	Clears micro BP	(bit $0C_{16}$)
H14:	Clears enable console echo	(bit 14_{16})

I Key

The I key can be used as a macrogo if bit 12 of the FCR is clear and can be used as a microgo if bit 12 of the FCR is set.

I: or IG (initiate)

The CRT will display the contents of the FCR as a response to this entry.

The I control function may also be used to set a bit in the FCR. Examples of these operations are given below:

I09G	Set the selective skip switch bit	(bit 09_{16})
I15G	Set enable auto display bit	(bit 15_{16})

J Key

The J control function is used to replace the contents of the function control register in a digit mode. It can be used to change the value of any FCR digit including digits 0 and 1. The value of display 0 and display 1 specifies which MP parameter will be displayed on display requests or enter requests. The J function always consists of J followed by two hexadecimal digits and a terminator (: or G). The first hexadecimal digit specifies the FCR digit 0 through 5 and the second hexadecimal digit specifies the value the digit is to be changed to; that is, 0 through F.

For example, the code J14: would set FCR digit 1 to a 4 (select A register); the CRT would display the updated contents of the function control register. Other examples are shown below:

J77G	Display the FCR	
J26:	Set the skip and stop switches	(bits $0A_{16}$ and 09_{16})
J20G	Clear the skip, stop, step, and protect switches	(bits 08_{16}, 09_{16}, $0A_{16}$, and $0B_{16}$)
J15:	Select the MIR	(set bits 05_{16} and 07_{16})
J04G	Select the Q register	(set bit 01_{16})

K Key

The K control function is used to display or enter data into the register specified by display 1 (refer to table 1 and table 2). The K function uses two formats.

The first format is a request to display the parameter specified by display 1. A function of KG will display the information requested. An example is given below.

1. Depress ESC key
2. Enter J14G ⟶ Display; J04000800
3. Enter KG ⟶ Display; KXXXX

The CRT should now display the contents of the A register. The J14G input changed the FCR digit 1 to a 4 which specified a request for the A register to be accessed. A KG function allowed the contents of A to be displayed.

The second format is an enter data request. The data is entered again by first selecting the register to be accessed in either digit 0 or 1 of the FCR. A K function followed by four hexadecimal digits is then entered, following by a terminator (: or G).

1. Depress ESC key
2. Enter J11G ⟶ Display; J01000800
3. Enter K1000G

The P register will now contain the address 1000.

L Key

The L key functions in the same way as the K key except that it is associated with display 0. An example is given below.

1. Depress ESC key
2. Enter J04G ⟶ Display; J40000800
3. Enter LFFFFG

The operation above would access the Q register and then enter the hexadecimal quantity FFFF into that register. LFFFF would be displayed on the keyboard.

Access of Macromemory

When macromemory is to be displayed or when the contents of memory is to be changed, the display 1 selection must be either the P or A register. The displayed register is incremented by 1 after each display or entry. For example:

1. STOP, MASTER CLEAR Computer
2. Depress ESC key
3. Enter: K71000800G (set FCR bits 01_{16}, 02_{16}, 03_{16}, 07_{16}, and 14_{16})
4. Enter: K0000G (set P register to 0000)
5. Enter: LG (display contents of memory location 0000)

Step 3 of the example will allow access to memory at the address specified by P. Step 4 enters address 0000 to be displayed. Step 5 entry displays contents of address 0000 of memory.

Breakpoint (BP)

There are two types of breakpoint used on the CYBER 18-20: micro and macro. In breakpoint condition, a micro- or macromemory address equals the contents of the breakpoint register. If bit 12 of the FCR is set, microbreakpoint is selected. If bit 12 is clear, macrobreakpoint is selected. Bits 14 and 15 of the FCR are used to select three types of macrobreakpoint (BP):

Bit 14	Bit 15	
0	0	BP not selected
0	1	Instruction reference BP
1	0	Store operand BP
1	1	All references BP

A macrobreakpoint occurs if the breakpoint register is equal to the macromemory address and the select conditions are met. For example:

J16G	Set display 1 to breakpoint register
K0050G	Set breakpoint register to 0050
J31G	Set macromode and breakpoint on instruction reference.

A stop will occur after the instruction at macrolocation 50_{16} is executed.

For microbreakpoint, P/MA is compared to the lower 12 bits of the breakpoint register. In addition, the upper/lower selection (32-bit select) is compared to bit 13 of the breakpoint register. If all bits are equal and the combination of FCR bits 14 and 15 is not zero, then a microstop occurs. If FCR bit 14 is set, then a comparison of FCR bit 13 and the upper/lower selector is not required.

To check the contents of a macroaddress, first enter the address to be checked, then enter an LG function. The contents of the specified address will be displayed. The address will automatically increment with subsequent terminations being entered. An example is given below pertaining to the program entered on the preceding page.

1.	Enter: K0000G	Address to be displayed
2.	Enter: LG	Contents of address 0000 are displayed
3.	Enter: G	Contents of address 0001 are displayed

Each additional termination will display the contents of the next address of macro-memory. Also, a KG function being executed while monitoring memory contents will allow the address being monitored to be displayed.

Program Execution

To execute a program the beginning address of the program must be specified and an initiate function executed as below.

1.	Enter: K0000G	Place (beginning address of the program) 0000 in A register
2.	Enter: IG	Initiate program (Go)

When the program has stopped a display of the FCR will be present on the CRT.

Summary

This activity described the purpose of the FCR and the significance of each bit position. It also described the purpose of each control command and gave examples of entering and executing programs.

Processor Register Access (Lab)

This laboratory exercise will familiarize you with the function control register, register display techniques, and memory access methods. You must use the CYBER 18 with conversational display terminal. It will require about one hour to complete this lab assignment. Follow the exercise procedures indicated, and answer any questions that are asked. When you have completed this assignment, compare your results with the answer key.

The CYBER 18 switch settings affecting system operation should be checked prior to use. Refer to Appendix B for the correct switch settings.

Function Control Register Access

1. On the computer console press: STOP, MASTER CLEAR

2. On CDT keyboard press: CLEAR and ESC, KG

3. What is displayed on the CDT display screen? _____

4. What condition is specified by the above function control register displayed contents? _____

5. Enter: K71200800G

6. What is displayed on the CDT display screen as a result of this entry?
   _____

7. Which register of display 0 has been accessed in step 5?
   _____

8. Which register of display 1 has been accessed in step 5?
   _____

9. What condition of digit 2 of the FCR has been enabled in step 5?
   _____

10. Enter: K1000G
    Enter: LG

11. The entries made in step 10 caused the display of _____.

12. What two keyboard entries will display the contents of memory address 1FFF?
    a. _____ b. _____

13. Enter: K0000G
    Enter: LFFFFG

14. What is the result of the two entries made in step 13?
    _____

15. Enter: HG

16. The CDT screen should display the FCR contents 712008XX.

17. Enter: J14G
    Enter: KG

18. Which register contents is displayed when the entry in step 17 is made?
    _____

19. What keyboard entries are necessary to display the Q register?
    a. _____ b. _____

20. What keyboard entry is necessary to enter the quantity C0FE into the Q register?
    _____

21. It is sometimes necessary to change the mode of operation of the microprocessor. This is done by changing the bits in the function control register.

    If the contents of the FCR were changed to perform the following microprocessor functions:

    - Enable console echo
    - Selective stop
    - Selective skip
    - Display mask register 1

    What would the contents of the FCR be?_____

22. What keyboard entries must be made to change the contents of the FCR to the previous value? (There may be more than one way of performing this operation.)
    _____

23. What is the contents of mask register 1?_____

24. The first card of the LODCHK diagnostic program controls the address at which the LODCHK program is deadstarted into main memory of the microprocessor. The format of this card is:

    K71000800K1FFFG

    Into which address of memory will the LODCHK program begin to load?

    _____

ANSWERS

3. K00000020
4. Status bit 1A set, indicating auto restart
6. K71200820
7. Memory
8. P register
9. Selective stop
11. The contents of memory address 1000
12. a. K1FFFG b. LG
14. Memory location 0000 contains FFFF
18. A register
19. a. J04G b. LG
20. LCOFEG
21. 09600800
22. a. ESC,? b. ESC,K09600800G
23. This 4-digit value will vary
24. 1FFF

Problem Solving Using the Function Control Register

Register Failure

It is often possible to isolate a problem in a failing register to a bit or bits in that register which are failing. For example, suppose that the most significant bit of the P register could not be set to a 1. Since this register is used to address main memory, it would mean that alternate addresses of main memory which require that bit for addressing could not be accessed, as demonstrated in Figure 3.

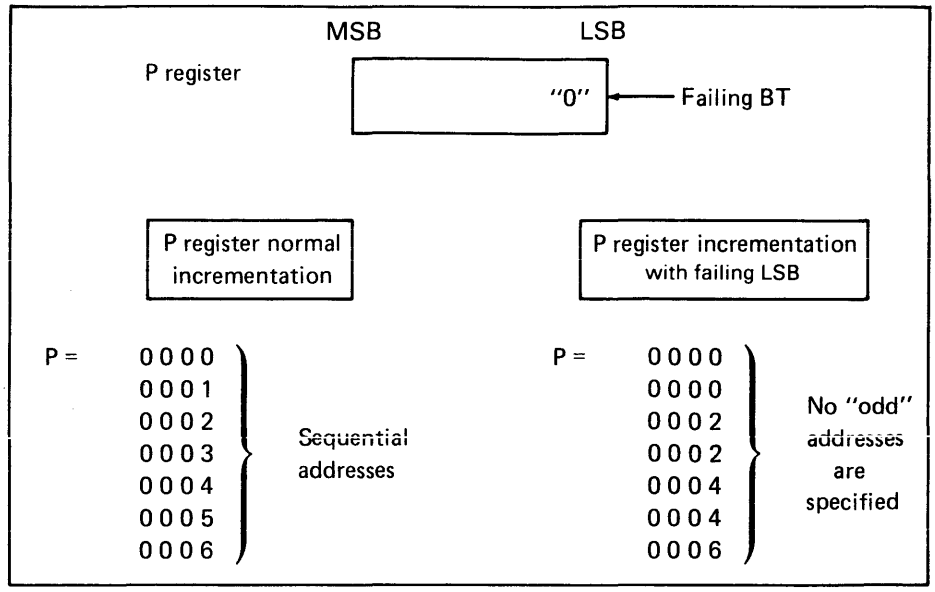


Figure 3. P Register Failure

1. What keyboard entries are made to display the P register contents through the FCR?
   a. _____
   b. _____
   c. _____

2. Enter the quantity FFFF into the P register. List the entries necessary to do this.
   _____

3. The value of P register just entered can be displayed with what keyboard entry?
   _____

4. Does the value that was entered into the P register in step 2 match the value displayed in step 3?
   _____

ANSWERS

1. a. ESC, KG (display FCR) b. K01000800G (P register in display 1) c. KG (display P register) 2. ENTER KFFFFG 3. KG 4. Yes. If not, procedure was incorrect.

Memory Access Method

Often it is necessary to check instructions or data contained in memory. For example, if a program is entered into main memory which fails to run as expected, it may be necessary for you to observe the addresses of memory in which the program is contained. In this way you can determine if the instructions were correctly written into memory. Other reasons for accessing memory locations may be to observe memory locations which contain special program parameters or which are suspected of failure. Now enter the following short program which demonstrates accessing of memory. Follow the steps outlined and answer the questions.

1. STOP, MASTER CLEAR computer
2. Enter: ESC
   Enter: KG (display should be K00000020)
   Enter: K71200800G (display upon entry should be K71200820)

3. What is the meaning of each digit of the FCR displayed in previous steps? (Refer to table 1.)
   a. digit 0 _____
   b. digit 1 _____
   c. digit 2 _____
   d. digit 5 _____
   e. digit 6 _____

4. The program to be entered will begin at address 0000 of memory. The keyboard entry to access 0000 is _____ .

5. The program to be entered is as follows:

0AC0	ENA	sign extended
60FF	STA	△
0000	SLS	

6. The keyboard entries to be made to enter the above program are:
   a. _____
   b. _____
   c. _____

7. Execute the program entered in the previous step. Keyboard entries are:
   a. _____
   b. _____

8. After execution, the A register contents can be found at which memory address?
   _____

9. The contents of the above address are _____ .

10. The A register contents are _____ .

11. If the CYBER 18 contains 48K of macromemory, which is the largest hexadecimal address which can be specified? _____

ANSWERS

3. a. Memory is accessed and can be displayed with an LG entry.
   b. P register is accessed and can be displayed with a KG entry.
   c. Selective stop option is selected.
   d. Enable console echo
   e. Auto restart enabled
4. K0000G
6. a. LOACOG
   b. 60FFG
   c. 0000G
7. a. K0000G
   b. IG
8. 00FF
9. FFC0
10. FFC0
11. BFFF

Summary

This activity has demonstrated the operation of the function control register. If correctly accessed, this register can be used to observe register contents, memory locations, processor operating parameters, and status conditions.

Diagnostic Loading and Execution (Text)

In earlier learning activities you were introduced to the diagnostic software used on the CYBER 18-20 processor. This diagnostic package is called the operational diagnostic system (ODS). You have seen the types of diagnostics in the ODS software and how they may be controlled and executed. In this activity you take a closer look at parts of the ODS software and you will operate these tests on the system. The purpose of this activity is to:

- Become familiar with the purpose of each test
- Become familiar with the loading procedure and execution of the ODS level 1 tests
- Check out the operation of the CPU and memory

Before continuing with this activity, let's briefly review some important facts about the ODS tests. The ODS software is stored on floppy disk. It is divided into three sections: Loadcheck, Level I tests and Level II monitor, and tests. Loadcheck is always run first and other tests will not load unless loadcheck runs correctly. Level I tests check the internal working of the CPU and Level II tests check external operations. The operator may control test operation by modifying the test run parameters. The loading and execution of each test is also controlled by special function keys located on the CDT.

General Procedure

During this activity you will be working with five diagnostic programs. The first program is LODCHK, followed by four level-one tests:

- MPINS
- MPMOS
- MPRTC
- LIAT1

Loadcheck (LODCHK)

The loadcheck routine is a stand-alone deadstart program that performs the following functions:

- Checks the microinstructions of the CYBER 18 processor by executing a selected set of macrolevel instructions.
- Checks all available memory (up to 32K)
- Checks the load path to ensure that further diagnostic tests can be loaded into the CPU
- Checks the operation of the conversational display terminal (CDT)
- Loads level I programs and/or level II monitor

The loadcheck program is always the first ODS program loaded. Other tests will not load until this test has been executed successfully.

Loadcheck is divided into the following six sections or subprograms.

Section 1: Command Test, Part 1

The command test part 1 is the first routine executed. It tests the basic processor and emulator paths and the instructions to be used by the check sum test. When section 1 is completed, a 1 is displayed on the CDT.

Section 2: Check Sum Test

The check sum test verifies that LODCHK is loaded properly. A check sum of zero indicates that LODCHK is properly loaded. When section 2 is successfully completed, a 2 is displayed on the CDT.

Section 3: Command Test, Part 2

The command test part 2 tests the instructions that will be used by the remaining sections of LODCHK. After the instructions are tested, the parity errors in memory locations 0000 through 0FFF are cleared. When the instructions test good and the parity errors are cleared, a 3 is displayed on the CDT.

Section 4: Memory Test

This section tests the lower 4K memory locations, addresses 0000 through 0FFF. The test consists of loading the locations with specific patterns, and reading to make sure those locations were loaded correctly. Only the lower 4K of memory is checked since that is where the level 1 tests are loaded. There is a level 1 test which will check all the remaining memory locations. When the memory tests satisfactory, a 4 is displayed on the CDT.

Section 5: Load Device Test

The load device test exercises the ODS loading path. A test pattern is read from the load device and compared with a pattern in memory. When the load device operates correctly, a 5 will be displayed on the CDT.

Section 6: Mover

The mover program moves the loader program and the test parameters to higher memory locations to provide space in lower memory for use by other ODS tests. The loader program is used to load other ODS tests and test parameters. After the loader program and the test parameters are moved, control is transferred to the loader program and the next level I test or the level II monitor is loaded. If no error occurs, a 6 is displayed on the CDT.

The successful completion of each LODCHK section is noted by displaying the section number on the CDT. A 123456 appearing on the CDT indicates all six sections of LODCHK have run correctly. When a malfunction occurs, the section number where the error occurred is not displayed and the CPU halts with an error code in the P register.

The parameters for LODCHK are loaded into memory along with the LODCHK programs. The only parameter that may be changed is the equipment code for the load device.

After the successful completion of LODCHK either level I tests or the level II monitor may be loaded. This activity is concerned with the level I tests. The level I test may be executed in any order; however, the preferred order of MPINS, MPMOS, MPRTC, LIAT2 will be used in this activity.

The run parameters used to control test execution consist of a number of words, each serving a special purpose. The parameter list is similar for each level I test; however, some changes are evident from test to test. By making changes in the run list, each test can be modified to meet special system requirements.

Instruction Test MPINS

The first level I test to be executed is MPINS, the microprocessor instruction test. This test insures that the macroinstructions, both basic and enhanced, are operating correctly. The instruction test is divided into nine independent sections or programs. These sections may be executed in any order but for greatest effectiveness should be run in order from one to nine.

Section 1

This section tests the basic register reference and interregister instructions.

Section 2

In section two, the memory reference instructions and addressing modes are tested. The addressing modes tested are absolute and relative addressing, and indexing with I, Q, both or no registers.

Section 3

This section tests the shift instructions including left and right shifts of the A, Q, and A/Q registers. The shift counts are varied from zero to thirty-one using twelve different patterns.

Section 4

This section tests the decrement and repeat, enhanced interregister, and enhanced skip instructions.

Section 5

In this section the load and store register group instructions are tested. Each instruction is tested in conjunction with a set and clear overflow value.

Section 6

This section is used to test the enhanced memory reference instructions with absolute, relative, and indexing address modes.

Section 7

In this section the enhanced field reference instructions are tested along with the relative and absolute addressing modes.

Section 8

In section 8 the operation of the parity generation instructions are tested. Each instruction is tested with 64 possible patterns.

Section 9

This section consists of two parts. Part 1 tests the execute micro sequence instruction and part 2 tests the A scale instruction.

The parameter run list for MPINS is shown in Table 3. Word A is a parameter used only by the MPINS test. When word A is zero, the multilevel indirect switch is off. Any non-zero value in word A indicates the switch is on. Word A is used in conjunction with sections 2 and 7 which deal with the addressing modes.

TABLE 3
MPINS Run Parameter List

Words	Initial Value (Hex)	Definitions
TESTID	0001	Test ID
PASCNT	0000	Pass Count
ERRCNT	0000	Error Count
1	2080	Control Word
2	0001	Repeat Count
3	1234	Sections Selected
4	5678	Sections Selected
5	9000	Sections Selected
6	0000	Sections Selected
7	0000	Equipment Address
8	0000	Interrupt Lines (Micro/Macro)
9	0000	Logical Unit
A	FFFF	If not zero, assume multilevel indirect switch to be on. Otherwise assume it is off.

MOS Memory and Addressing Test MPMOS

The test MPMOS verifies that every memory location in both memory banks is addressable and capable of storing various word patterns. MPMOS loads memory with special patterns, then reads from memory and verifies that the patterns read are the same as those previously stored. The special patterns are determined by the special sections with the MPMOS test.

MPMOS consist of six sections:

Section 1

The addressing test verifies that each location is capable of being addressed. Each location is addressed and the address written to that location. After all locations have been written into, each location is read from. The data read should be the address of the location.

Section 2

The shift diagonal test verifies that each memory chip in a diagonal line can store all ones while other locations in the chip are zeros.

Section 3

The marching ones and zeros test verifies that writing into one memory cell does not affect the contents of another cell. It will also verify decoder problems. The test writes zeros into all locations and reads to verify, then writes all ones and reads to verify. This test is performed on all 4K blocks separately.

Section 4

The checkerboard test verifies that all memory cells can hold an alternate one-zero (checkerboard) pattern. This test is performed on individual 4K blocks.

Section 5

The constant row/column test verifies that areas within each memory chip can be addressed. The locations are addressed by first holding the column address to zero and incrementing the row address; then by holding the row address at 3F and incrementing the column address. This insures that each memory cell can be addressed.

Section 6

The complement row/column test verifies the operation of the address drivers on the A and CI board and the memory array boards. The addressing operation tests 4K locations at a time. The memory locations are tested by writing into each cell in

the 4K block, using row and column addresses that are complements of each other– for example, each cell whose row address is 0000 and column address is FFFF. The row address is then changed and the column address is made the complement of the row address.

The run parameter list for MPMOS is shown in Table 4. Words A through F and 10 through 13 are used only by this test. Words A through E specify the size of the memory, and the start and stop addresses for the memory areas to be tested. Since indirect addressing is required for addresses above 65K, words B, C, D and E specify an 18-bit indirect address.

Word F specifies:

- If the error correction code ECC option is available in the processor.
- If a full write cycle or a split write cycle is to be performed.
- If the program is to determine the memory size available and compare it with word A.

Words 10 and 12 specify the type of patterns used for writing and reading. Words 11 and 13 specify the value of the protect bit to be used.

TABLE 4
MPMOS Run Parameter List

Words	Initial Values (Hex)	Definitions
TESTID	0024	TESTID
PASCNT	0000	PASS COUNT
ERRCNT	0000	ERROR COUNT
1	2088	Control Word
2	0001	Repeat Count
3	1345	Sections Selected
4	6000	Sections Selected

TABLE 4 (cont'd.)

Words	Initial Values (Hex)	Definitions
5	0000	Sections Selected
6	0000	Sections Selected
7	0000	Equipment Address (not used)
8	0000	Interrupt Lines (not used)
9	0000	Logical Unit (not used)
A	0001	Bits 0-3 No. of 16K blocks in local bank (Min = 1, Max = 8) 8-11 No. of 16K blocks in remote bank (Min = 0, Max = 8)
B	0000	Most significant 2 bits of start address*
C	0000	Least significant 16 bits of start address*
D	0000	Most significant 2 bits of stop address*
E	3FFF	Least significant 16 bits of stop address*
F	0002	Bits 0 ECC present in local CPU (yes = 1, no = 0) 1 Memory in split cycle or full write mode (split write = 1, full write = 0)* 2 Do not size memory (do not size = 1, size = 0)

TABLE 4 (cont'd.)

Words	Initial Values (Hex)	Definitions
10	CDCD	Special Pattern 1
11	0001	Protect bit for special pattern 1 (Set = 1, Clear = 0)
12	4545	Special Pattern 2
13	0000	Protect bit for special pattern 2

*Physical (absolute) address reference. Eighteen bits are required to specify locations above 65K. Words B and C are used to specify the start address and words D and E for the stop address. All locations from the start to (and including) the stop address are tested.

MPRTC Test

The next level I test to be executed is MPRTC. This diagnostic verifies the operation of the protect system, the interrupt system and the real-time clock. The MPRTC is divided into five test sections.

Section 1

This section insures that when the protect bit is set or cleared, the other bits in the memory location do not change.

Section 2

This section verifies that a protect fault occurs if a privileged instruction is executed from an unprotected location. Examples of privileged instructions are: EIN, IIN, SPB, CPB, EXI. The execution of these instructions from unprotected locations should also cause an internal interrupt to occur to test the protect and interrupt systems.

Section 3

This test section verifies that a protect fault and interrupt occurs if an attempt is made to execute a protected instruction immediately after the execution of an unprotected instruction.

Section 4

This test section insures that an attempt to store data in a protected memory location with an unprotected instruction causes a protect fault and prevents the contents of the protected location from being altered. All instructions capable of altering memory contents are tested.

Section 5

This section test the properties of the protect system:

- An instruction which causes a protect fault is treated as a selective stop instruction.
- When an unprotected instruction is executed and an interrupt causes a protected instruction to be executed next, no protect fault occurs.

The run parameters for MPRTC are shown in Table 5. Word A specifies the last memory location to be tested. If zero, the last address is calculated by the program. The first or starting address is the first location after the MPRTC diagnostic program.

TABLE 5
MPRTC Run Parameter List

Words	Initial Values (Hex)	Definitions
TESTID	0006	TEST ID
PASCNT	0000	Pass Count
ERRCNT	0000	Error Count
1	2080	Control Word
2	0001	Repeat Count
3	1234	Sections Selected
4	5000	Sections Selected
5	0000	Sections Selected
6	0000	Sections Selected
7	00F3	Equipment Address of Clock
8	0088	Interrupt Lines of Clock (Micro/Macro)
9	0000	Logical Unit
A	0000	Stop Address*

*The start address is set to the address of the last cell occupied by the test +1. The stop address is automatically calculated by the test when the default value (0000) is used; otherwise the address given is used as the stop address.

LIAT1 Test

This test verifies the operation of the I/O controller and the CDT. The LIAT1 test consists of nine sections.

Section 1

The controller command/status test verifies that the controller recognizes director function codes and performs the functions. The functions are sent to the controller and the controller status is checked to insure the functions have been performed.

Section 2

The terminal display command test executes the following commands and requires the operator to verify that each command was executed.

- Bell—The bell rings 3 times. Operator should judge loudness and tone of the bell.
- Skip and backspace—cursor should perform a carriage return, skip 80 spaces, then backspace 80 spaces. The space-backspace is repeated twice.
- Line clear—performs the following actions:
  1. Reset cursor (Positions cursor in the first position of the top line) and clear the line.
  2. Write 20 characters, reset, line clear.
  3. Write 40 characters, reset, line clear.
  4. Write 60 characters, reset, line clear.
  5. Write 80 characters, reset, line clear.
- Screen clear—The S character is displayed in every position; then the screen clear function is performed, blanking all screen positions.

Section 3

The display data transmission test ensures that characters can be sent from the processor to the CDT 3 ways: A/Q channel, ADT word mode, and ADT character mode. The data patterns used are: 1) all 96 characters, 2) display H's in all positions, 3) display *U*U pattern in all positions, and 4) display a line of blanks, a line of W's, and a line of hyphens (-).

Section 4

The cursor positioning test verifies the movement of the cursor. The screen is first cleared; then the cursor traces consecutive V patterns on the screen. Next the screen display is compared with an expected display.

Section 5

The lamp check test verifies the operation of the keyboard lock, clear to send, character and carrier indicator lamps. These lamps should light for 30 seconds. The KEYBOARD LOCK, ALERT, and FORMAT MODE indicators should be OFF.

Section 6

The keyboard test verifies the function of the keyboard. The operator enters the characters 1234567890 and the program verifies the character pattern.

Section 7

The computer echo test checks the data path between the CDT and the computer. The operator inputs a set of characters from the keyboard which are sent to the computer and back to the CDT screen. The operator compares the data entered against the displayed value.

Section 8

The keyboard enable/disable test exercises the keyboard lock and unlock features. The operator is asked to enter characters in both modes.

Section 9

The parity error check verifies both even and odd parity features of the CDT. The operator inputs a character in both parity modes and the program checks if parity is correct.

The run parameter list for LIAT1 is shown in table 6. Words 7 through 9 are for data transmission between the CPU and CDT. Word A indicates the number of lines to be tested on the CDT display and word B indicates a delay time to be used as an output delay.

TABLE 6
LIAT1 Run Parameter List

Words	Initial Values (Hex)	Definitions
TESTID	0007	Test ID
PASCNT	0000	Pass Count
ERRCNT	0000	Error Count
1	2082	Control Word
2	0001	Repeat Count
3	1234	Sections Selected
4	5678	Sections Selected
5	9000	Sections Selected
6	0000	Sections Selected
7	0091	Equipment Address
8	0011	Interrupt Lines (Micro) (Macro)
9	0004	Logical Unit
A	0018	Total Number of Lines on Screen
B	0001	Number of Seconds to Wait for Output

Summary

In this text you have read about five diagnostic tests. LODCHK is the first diagnostic program run. It consists of 6 sections which test the diagnostic loading path, basic macroinstructions, and the lower 4K of memory.

MPINS contains nine sections which test the operation of all macroinstructions. MPMOS verifies the operation of the memory used in the processor; it contains six sections. MPRTC checks the operation of the protect and interrupt systems and the realtime clock. LIAT1 tests the I/O path and the CDT terminal. Each test may be controlled by manipulating the parameter run list.

Diagnostic Loading and Execution (Lab)

In this laboratory activity you will run the operational diagnostic system (ODS) tests on the CYBER 18-20 computer system. In addition to this lab guide, you will need the following materials:

1. The floppy disk containing the ODS software.

2. The CYBER 18-20 Hardware Maintenance Manual containing the diagnostic decision logic tables (DDLTs) Pub. No. 96768682.

3. Writing materials for taking notes.

The procedures for setting up the CPU and floppy disk to run the diagnostics are located in the first few pages of the DDLT manual. These lab worksheets will guide you in the use of the manual.

If during this lab, the CDT displays any information not indicated in the worksheets, you should notify your course administrators.

The first diagnostic you run will be LODCHK. Turn to the DDLT reference sheets specified in each step.

Step 1: Reference Sheet 1 of 11

Assumptions	Action and Description
1. System is plugged into power outlet.	1. Verify CPU is plugged into power outlet.
2. CDT is plugged into power outlet.	2. Verify CDT is plugged into power outlet.
3. Power is turned on at each device.	3. Apply power to CPU and CDT.

This processor is a CYBER 18-20 system and the DDLT directs you to sheet 2 of the LODCHK DDLT.

If the system was a CYBER 18-30 timeshare system, where would the DDLT tell you to go?_____

ANSWER: To sheet 3

Step 2: Reference Sheet 2

Assumptions	Action and Description
1. Entry is made from sheet 1	
2. This is a CYBER 18-20.	
3. MASTER CLEAR on operator's panel is pressed.	3. Press MASTER CLEAR on the operator's console.
4. CLEAR key on keyboard is pressed.	4. Press CLEAR key on keyboard. If keyboard lock indicator is lit, press BREAK key, then CLEAR key. Display should clear.
5. Enter the following at keyboard ESC key: J58G.	5. Press the ESC key, enter J58G. (This enables console echo capabilities.)

After performing action 4, the display should have cleared. When action 5 was performed, the CDT should display J000008X0 or J000008X8, as described by the conditions on sheet 2 of the LODCHK DDLTs. If these conditions do not exist, repeat actions 3, 4, and 5 again or notify your course administrator. If these conditions are as described, you can proceed with the lab.

The next step is on sheet 4 of the LODCHK DDLT. The conditions on sheet 4 specify that if the ODS tests are loaded into the processor from the floppy disk, turn to sheet 5.

If the ODS diagnostics were loaded by the Card Reader, to which sheet would you turn?_____

ANSWER: Sheet 7

Step 3: Reference Sheet 5

Assumptions	Action and Description
1. Insert ODS level I diskette into flexible disk drive.	Note position of notch on diskette. Insert diskette with notch facing to the rear. Do not force the diskette.
2. Close door to flexible disk drive.	

Once the diskette is properly loaded, proceed to the conditions described below and on sheet 5 of the LODCHK DDLT. These conditions ensure proper diskette loading.

Step 4: Reference Sheet 5

Conditions	Action and Description
1. Is UNIT REV indicator on?	1. If no, go to condition 2. If yes, depress UNIT REV switch; if UNIT REV indicator goes out, go to condition 2. If the indicator stays on, notify your course administrator.
2. Is WRITE ENAB indicator on?	2. If no, go to condition 3. If yes, depress WRITE ENAB switch. If the indicator goes off, go to condition 3; if not, notify your course administrator.
3. Press STOP, MASTER CLEAR, and DEADSTART switches. Does DEADSTART indicator go on?	3. If yes, the diskette has been properly loaded. If no, repeat steps 3 and 4 of this lab. If the answer is still no, notify the course administrator.

In condition 1 what would be the second item you would check? _____

ANSWER: Cabling to operator panel

In condition 3 what is the next step if the DEADSTART indicator goes on?_____

ANSWER: Proceed to sheet 8

Since you are reading this paragraph, it means that the above conditions worked. When you depressed the DEADSTART switch in condition 3 above, the LODCHK program was loaded into memory and began executing. The LODCHK diagnostic consists of six sections. After each section runs successfully the number of that section is displayed on the CDT. When LODCHK is completed and no errors are found the CDT will display as 123456. Any display other than this indicates a problem and the procedure to follow looks like this:

Step 5: Reference Sheet 8

Conditions	Action and Description
1. Does the CDT display 123456?	1. This display indicates LODCHK ran without errors; go to condition 2. Any other display indicates discrepancies have been found; notify the course administrator.
2. Have all deadstart devices been tested?	2. If no other load devices are to be tested, as in this case, go to condition 3.
3. Is the card reader being tested?	3. In this case, the card reader is not being tested. This indicates that LODCHK is now complete and the next diagnostic may be run.

In condition 1 above if any display other than 123456 was found, you were to notify the course administrator. This action is for the lab situation only. If you were the technician then you would have followed the actions listed on sheet 8 of the LODCHK DDLTs. For example, let's say that the CDT displays a 123 instead of 123456. Using sheet 8 of the LODCHK DDLT, what would be your first action? _____

ANSWER: Use another diskette to load LODCHK and restart the diagnostic

Suppose the CDT displayed a 12345. You perform actions 1 and 2 and the problem still exists. What would you do next? _____

ANSWER: Replace the card in slot X

Now that LODCHK has run successfully, the level I tests may be run. The first level I diagnostic to run will be MPINS. The CDT should display:

123456
MPINS?

This indicates that LODCHK is completed and asks if you want to run the MPINS diagnostic.

The remainder of the lab is conducted without reference to the DDLTs.

Conditions	Action and Description
1. CDT displays: 123456 MPINS?*	1. Type GO, press CARRIAGE RETURN. This causes MPINS to execute.
2. CDT displays: MPINS EXECUTING	2. If this is not displayed, call course administrator.

*This display may include information regarding the revision level of the ODS tests being used.

Conditions	Action and Description
3. CDT displays: MPINS SUSPENDED BOT	3. Type GO Press CARRIAGE RETURN
4. CDT displays: SET MULTILEVEL INDIRECT SWITCH OFF (ESC J40 @ GO CR) MPINS SUSPENDED SELF	4. Press ESC Type J40 @ GO Press CARRIAGE RETURN
5. CDT displays: MPINS SECTION 0001 MPINS SECTION 0002 MULTILEVEL INDIRECT SWITCH IS EXPECTED TO BE OFF. MPINS SECTION 0003 MPINS SECTION 0004 MPINS SECTION 0005 MPINS SECTION 0006 MPINS SECTION 0007 MPINS SECTION 0008 MPINS SECTION 0009 MPINS SECTION 000A MPINS SECTION 000B MPINS COMPLETED 0001 PASSES SET MULTILEVEL INDIRECT SWITCH ON (ESC J42 @ GO CR) MPINS SUSPENDED SELF	5. Press ESC Type J42 @ GO Press CARRIAGE RETURN
6. CDT displays: MPINS TERMINATED 0000 ERRORS	

MPINS is now executing. After approximately 10 seconds the CDT should display MPINS TERMINATED. This indicates that MPINS ran without errors and you may continue testing. Any other display indicates a problem; notify your course administrator.

Conditions	Action and Description
1. CDT displays: MPMOS?	1. Type GO, press CARRIAGE RETURN. This causes MPMOS to execute.
2. CDT displays: MPMOS EXECUTING MPMOS SUSPENDED BOT	2. MPMOS is waiting for you to enter required run parameters.* Enter A,004 CARRIAGE RETURN D, 0, FFFF CARRIAGE RETURN GO CARRIAGE RETURN By entering these values you have specified: A, 004 – The number of 16K sections to be tested (64K) D, 0, FFFF – A single processor, the stop address.
3. CDT displays: A, 004 D, 0, FFFF GO SET MULTILEVEL INDIRECT SWITCH OFF (ESC J40 @ GO CR) MPMOS SUSPENDED SELF	3. Press ESC Enter J40 @ GO Press CARRIAGE RETURN This will clear the multilevel indirect switch.

*Refer to ODS manual for systems with other than 64K memory.

Conditions	Action and Description
4. After several minutes, CDT displays: MPMOS SECTION 0001 MPMOS SECTION 0003 MPMOS SECTION 0004 MPMOS SECTION 0005 MPMOS SECTION 0006 MPMOS COMPLETED 0001 PASSES SET MULTILEVEL INDIRECT SWITCH ON (ESC J42 @ GO CR) MPMOS SUSPENDED SELF	4. Press ESC Type J42 @ GO Press CARRIAGE RETURN This turns on the multilevel indirect switch.
5. CDT displays: MPMOS TERMINATED 0000 ERRORS	5. MPMOS ran with no errors.

The next test to be run is MPRTC.

Conditions	Action and Description
CDT displays: MOSMA?	Type MPRTC Press CARRIAGE RETURN This will cause MPRTC to be executed instead of MOSMA.
The CDT displays: MPRTC EXECUTING	
1. CLEAR PROTECT AND STOP SWITCHES (ESC J20 @ GO CR) MPRTC SUSPEND SELF	1. Press ESC key Type in J20 @ GO Press CARRIAGE RETURN
2. SET PROTECT, AND CLEAR stop switches (ESC J28 @ GO CR) MPRTC SUSPEND SELF	2. Press ESC key Type in J28 @ GO Press CARRIAGE RETURN

Conditions	Action and Description
3. MPRTC SECTION 0001 MPRTC SECTION 0002 MPRTC SECTION 0003 MPRTC SECTION 0004 MPRTC SECTION 0005	
4. SET PROTECT AND STOP SWITCHES (ESC J2A @ GO CR) MPRTC SUSPEND SELF	4. Press ESC key Type in J2A @ GO Press CARRIAGE RETURN
5. VERIFY CPU IS HALTED AT XXXX (ESC J11G KG) and restart CPU (I@)	5. Press ESC key Type in J11G KG Observe the value Knnnn, where nnnn portion equals XXXX value in message. If not equal, notify lab manager. If equal, type in I@ at the keyboard.*
6. SET PROTECT, AND CLEAR STOP SWITCHES (ESC J28 @ GO CR) MPRTC SUSPEND SELF	6. Press ESC key Type in J28 @ GO Press CARRIAGE RETURN
7. MPRTC COMPLETED 0001 passes.	
8. CLEAR PROTECT, AND SET STOP SWITCHES (ESC J22 @ GO CR) MPRTC SUSPEND SELF	8. Press ESC key Type in J22 @ GO Press CARRIAGE RETURN
9. MPRTC TERMINATED 0000 errors.	9. MPRTC ran without errors.

*XXXX = ODA9 OR OD91

The next test to run is LIAT1.

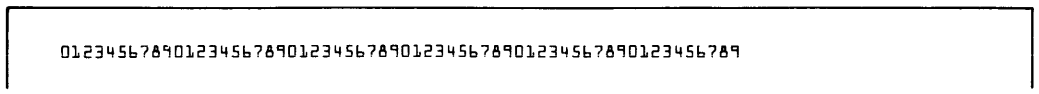
Conditions	Action and Description
1. CDT displays: MIMEM?	1. Type LIAT1 Press CARRIAGE RETURN This will initiate LIAT1
2. CDT displays: LIAT1 EXECUTING	
3. CDT displays: LIAT1 SUSPENDED ENDS	3. Type GO Press CARRIAGE RETURN Observe the following action on the screen: a. Alarm sounds 3 times. b. Screen clears. c. Cursor moves from left to right and back, twice. d. Screen displays patterns shown below. e. Screen clears

```
0123456789012345678?
```

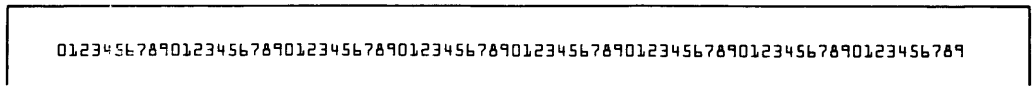
Test Pattern 1

```
012345678901234567890123456789012345678?
```

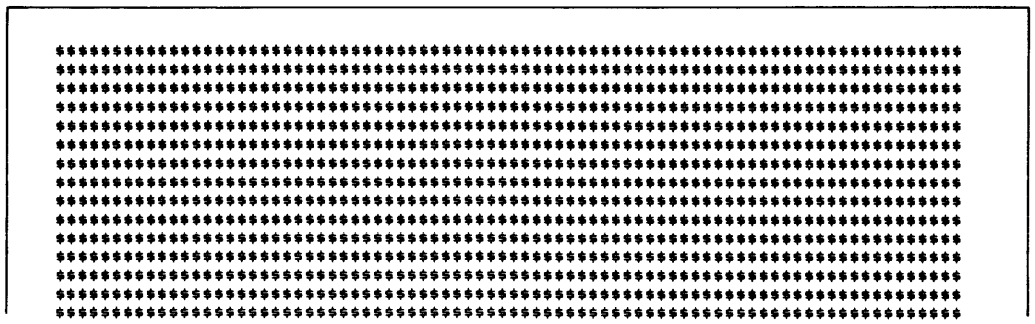
Test Pattern 2



Test Pattern 3

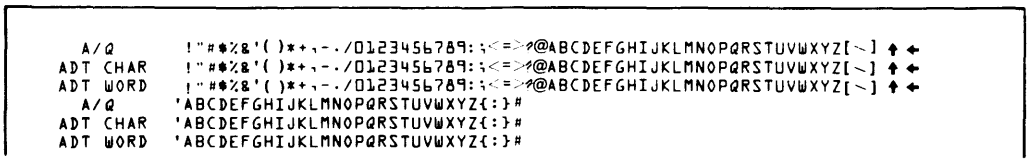


Test Pattern 4

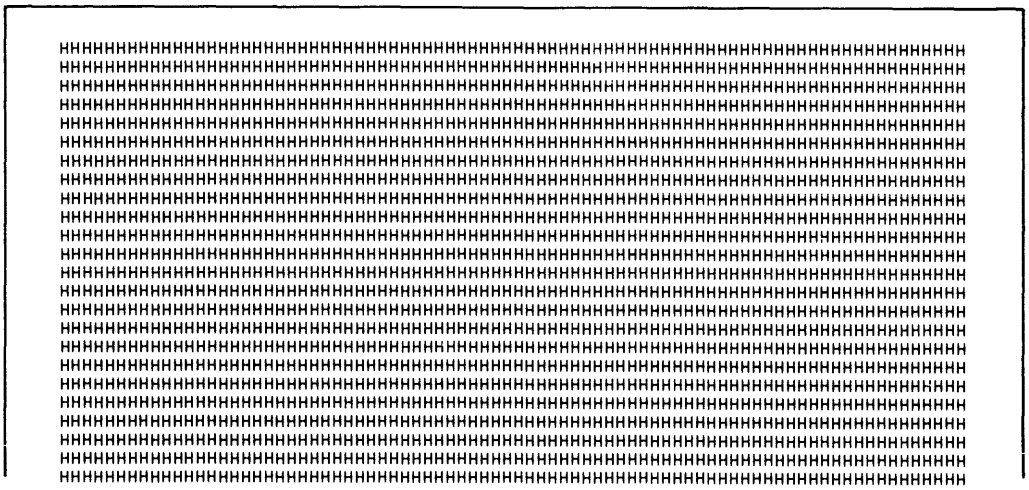


Test Pattern 5

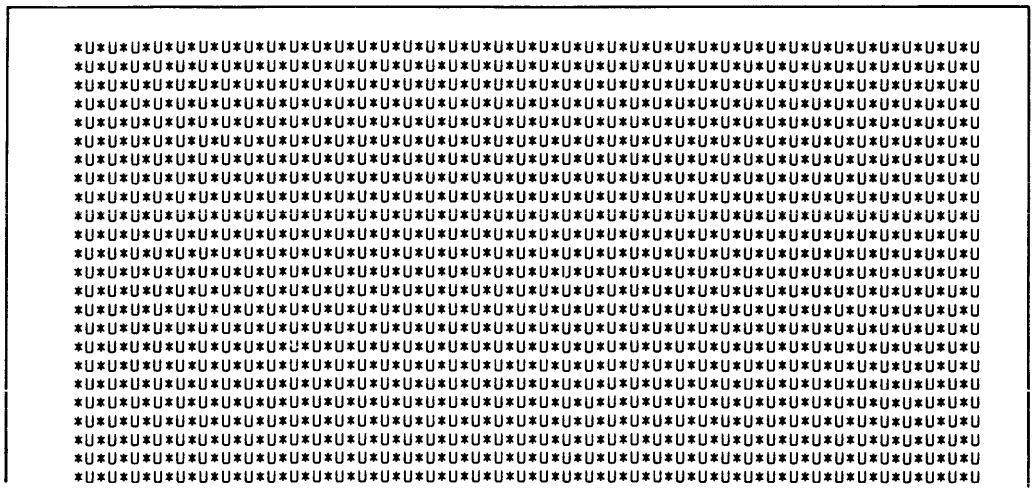
Conditions	Action and Description
4. CDT displays: LIAT1 SUSPEND ENDS	4. Type GO Press CARRIAGE RETURN Screen will display patterns below:



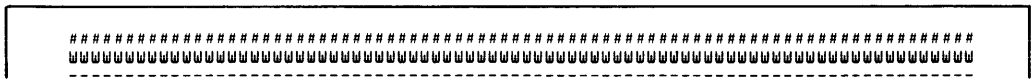
Test Pattern 6



Test Pattern 7

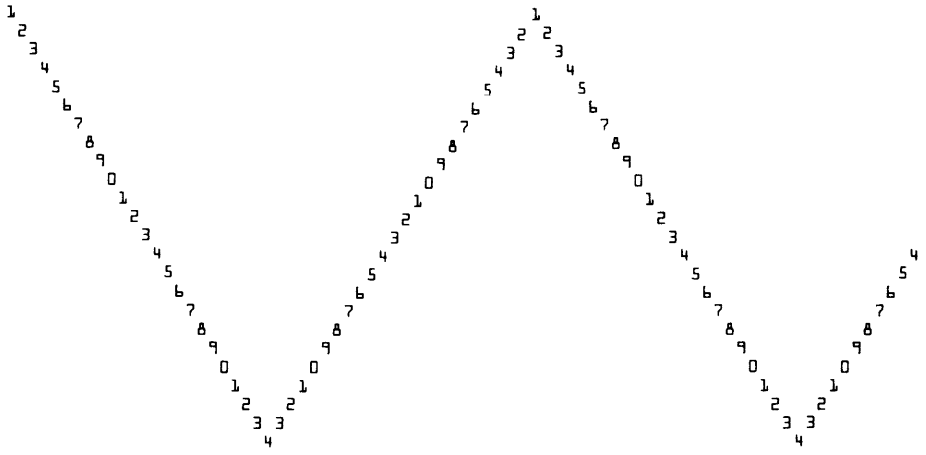


Test Pattern 8



Test Pattern 9

Conditions	Action and Description
5. CDT displays: LIAT1 SUSPEND ENDS	5. Type GO Press CARRIAGE RETURN
6. CDT displays:	



Test Pattern 10

Conditions	Action and Description
7. CDT displays: LIAT1 SUSPEND ENDS	7. Type GO Press CARRIAGE RETURN All indicator lamps except: KEYBOARD LOCK, ALERT, and FORMAT MODE are illuminated.

Conditions	Action and Description
8. Enter 1–0 from keyboard	8. When requested enter: 1234567890 Press CARRIAGE RETURN
9. CDT displays: LIAT1 SUSPEND ENDS	9. Type GO Press CARRIAGE RETURN When requested enter up to 80 characters of A through Z, 1 through 0 Press CARRIAGE RETURN
10. CDT displays your last entry	
11. CDT displays: LIAT1 SUSPEND ENDS	11. Type GO Press CARRIAGE RETURN Make entries and switch changes as requested by CDT.
12. CDT displays: WITHIN 30 SECONDS DO THIS SWITCH TO ODD PARITY INPUT ONE ALPHANUMERIC CHARACTER SWITCH TO EVEN PARITY INPUT ONE ALPHANUMERIC CHARACTER	12. Perform the steps when requested
13. CDT displays: LIAT1 SUSPEND ENDS	13. Type GO Press CARRIAGE RETURN
14. CDT displays: WITHIN 30 SECONDS ENTER 4 CHARACTERS	14. When requested enter 4 characters
15. CDT displays: LIAT1 SUSPEND ENDS	15. Type GO Press CARRIAGE RETURN
16. CDT displays: LIAT1 COMPLETED 0001 PASSES LIAT1 TERMINATED 0000 ERRORS	

Summary

You have just had a brief look at the diagnostic system for the CYBER 18-20 processor. The diagnostics consists of LODCHK and Level I and Level II tests. The diagnostics along with the DDLTs are used to verify the operation of the CPU and the associated peripherals. In this lab you studied LODCHK and Level I diagnostics: MPINS, MPMOS, MPRTC and LIAT1, and observed how the DDLTs are used to run LODCHK.

Repair of Problems

Now that you have completed the learning activities in CYBER 18-20 Maintenance and Troubleshooting, you are ready to perform the following lab exercise. Correct your answers, using the answer key that follows this lab. Consult with your learning center administrator to determine which, if any, learning activities you should review before proceeding to the posttest.

Directions

In previous learning activities you studied various methods for analyzing and repairing specific CYBER 18-20 central processor hardware failures. This laboratory activity tests your ability to locate, isolate, and repair hardware problems.

Ask the course administrator to introduce a failure into the computer. Run the ODS tests, and using the diagnostic decision logic tables, isolate the failure and identify possible repairs that would fix the problem. After you have isolated a problem, notify the course administrator and verify your analysis by answering the questions pertaining to each problem. In order to satisfactorily complete this laboratory, you should answer 60 percent correctly (or two of the three problems).

Problem 1

1. Which, if any, of the ODS tests failed to run to completion?

   _____

2. What are the visual symptoms of this failure? _____

   _____

3. In the DDLTs the failing CONDITION can be located on sheet_____of table_____.

4. What is the failing CONDITION you found in the DDLTs? _____

   _____

5. List, in sequential order, the first five ACTIONS you would do to correct this hardware failure.

   a.

   b.

   c.

   d.

   e.

Problem 2

1. Which, if any, of the ODS tests failed to run to completion?

   _____

2. What are the visual symptoms of this failure? _____

   _____

3. In the DDLTs, the failing CONDITION can be located on sheet _____ of table _____.

4. What is the failing CONDITION you found in the DDLTs? _____

   _____

5. List, in sequential order, the first five ACTIONS you would do to correct this hardware failure.

   a.

   b.

   c.

   d.

   e.

Problem 3

1. Which, if any, of the ODS tests failed to run to completion?

   _____

2. What are the visual symptoms of this failure?_____

   _____

3. In the DDLT's, the failing CONDITION can be located on sheet_____of table_____.

4. What is the failing CONDITION you found in the DDLTs? _____

   _____

5. List, in sequential order, the first five ACTIONS you would do to correct this hardware failure.

   a.

   b.

   c.

   d.

   e.

ANSWERS

PROBLEM 1

1. MPINS 2. After a GO initiates test, it halts and displays an error code of 0111 3. 3, 6-4 4. Condition #3, a condition code of 0111 is present 5. Replace transform (CARD SLOT R) (Action 4); Replace ALU (CARD SLOT M) (Action 5); Replace SMI (CARD SLOT L) (Action 8); Replace CONTROL 2 (CARD SLOT N) (Action 7); Replace CONTROL 1 (CARD SLOT P) (Action 6)

PROBLEM 2

1. LODCHK 2. Test stops after the numbers 123 are displayed 3. 8, 6-3 4. Condition #1, a display of the numbers 123 5. Use another load device if available (Action 4); Set up and deadstart system using another load device (Action 2); Replace memory (CARD SLOT X) (Action 5); Replace memory interface (CARD SLOT V) (Action 6); Replace memory interface (CARD SLOT W) (Action 7)

PROBLEM 3

1. MPRTC 2. Test would not respond in assumption 3 to any entry of J28@GO cr 3. 1, 6-7 4. Condition #3, is microprocessor halted at address displayed in display message directive 4? The answer is NO. 5. Replace transform (CARD SLOT R) (Action 3); Replace memory interface (CARD SLOT V) (Action 1); Replace memory interface (CARD SLOT W) (Action 2); Replace SMI (CARD SLOT L) (Action 4); Replace memory (CARD SLOT X) (Action 5)

PROGRESS CHECK

QUESTIONS

1. Which control command generates a MASTER CLEAR to the microprocessor?

   a. H
   b. I
   c. K
   d. ?

2. What function in the FCR must be enabled if the operator wishes to display an entry made at the CDT keyboard on the CDT screen?

   a. Step (bit 11)
   b. Console echo (bit 20)
   c. Auto display (bit 21)
   d. Suppress console transmit (bit 16)

3. Which Level 1 ODS diagnostic program tests all macroinstructions used by the microprocessor?

   a. MPINS
   b. MPMOS
   c. MPRTC
   d. LIAT1

4. Which display indicates that the LODCHK program ran successfully, without errors?

   a. 123456
      MPINS?
   b. 12345
   c. LODCHK OK
   d. MPINS!

5. Which control command sets all bits in digit 5 of the Function Control Register?

   a. J05G
   b. J25G
   c. J45G
   d. J5FG

6. Which ODS diagnostic program verifies the operation of the CDT?

   a. LODCHK
   b. MPMOS
   c. MPRTC
   d. LIAT1

7. Which control command will place the computer in the run mode (macrogo)?

   a. HG
   b. IG
   c. KG
   d. LG

8. What is the correct sequence of codes required to enter 1234 into macromemory location 0FF4?

   a. J17:, H01:, K1234:, L0FF4:
   b. I1234:, H0FF4:, K11:, L00:
   c. J1234:, K0FF4:, L11:, M07:
   d. J11:, J07:, k0FF4:, L1234:

9. Test section 4 of the loadcheck routine is a _____ test.

   a. command
   b. memory
   c. check ram
   d. load device

10. What set of commands causes the contents of "Q" to be displayed?

    a. J04G; KG
    b. J04G; LG
    c. J14G; KG
    d. J14G; LG

11. What ODS program verifies the operation of the I/O controller?

    a. MPINS
    b. MPMOS
    c. MPRTC
    d. LIAT1

12. What ODS program verifies the operation of the protect and interrupt systems?

    a. LIAT1
    b. MPINS
    c. MPMOS
    d. MPRTC

13. Which control command performs an entry termination function?

    a. ?
    b. G
    c. J
    d. L

14. Which FCR display indicates that a main memory parity error exists?

    a. 05442882
    b. 446814C7
    c. 71000849
    d. 1A830021

15. Which FCR display is required to change the contents of the P register?

    a. 00000040
    b. 440000C8
    c. 71000840
    d. C2400800

16. What section of the loadcheck routine verifies that the routine has been properly loaded?

    a. Command test 1
    b. Command test 2
    c. Check sum test
    d. Memory test

ANSWERS

1. Correct Answer: d
   Resource: Text: CYBER 18-20 Maintenance and Troubleshooting SRM, page 6.

2. Correct Answer: b
   Resource: Text: CYBER 18-20 Maintenance and Troubleshooting SRM, page 10.

3. Correct Answer: a
   Resource: Text: CYBER 18-20 Maintenance and Troubleshooting SRM, page 20.

4. Correct Answer: a
   Resource: Text: CYBER 18-20 Maintenance and Troubleshooting SRM, page 37.

5. Correct Answer: d
   Resource: Text: CYBER 18-20 Maintenance and Troubleshooting SRM, page 7.

6. Correct Answer: d
   Resource: Text: CYBER 18-20 Maintenance and Troubleshooting SRM, pages 29 through 31.

7. Correct Answer: b
   Resource: Text: CYBER 18-20 Maintenance and Troubleshooting SRM, page 7.

8. Correct Answer: d
   Resource: Text: CYBER 18-20 Maintenance and Troubleshooting SRM, page 8.

9. Correct Answer: b
   Resource: Text: CYBER 18-20 Maintenance and Troubleshooting SRM, page 19.

10. Correct Answer: b
    Resource: Text: CYBER 18-20 Maintenance and Troubleshooting SRM, page 8.

11. Correct Answer: d
    Resource: Text: CYBER 18-20 Maintenance and Troubleshooting SRM, page 29.

12. Correct Answer: d
    Resource: Text: CYBER 18-20 Maintenance and Troubleshooting SRM, page 27.

13. Correct Answer: b
    Resource: Text: CYBER 18-20 Maintenance and Troubleshooting SRM, page 6.

14. Correct Answer: c
    Resource: Text: CYBER 18-20 Maintenance and Troubleshooting SRM, page 3.

15. Correct Answer: a
    Resource: Text: CYBER 18-20 Maintenance and Troubleshooting SRM, page 5.

16. Correct Answer: c
    Resource: Text: CYBER 18-20 Maintenance and Troubleshooting SRM, page 19.

Appendix A

Test Item Diagram

SHEET 1 of 3					
ASSUMPTIONS: 1. For the remaining testing in tables 6-4 through 6-103, all tests must be loaded from the same load device that loadcheck is loaded from. This requires a full set of diagnostics on either diskette or cassette. 2. After xxxxx? is displayed, the following is entered at the keyboard (if xxxxx is not displayed, go to table 6-100): MPINS is typed in. CARRIAGE RETURN is pressed. NOTE: xxxxx = test name 3. Observe the CDT display for the following conditions.					
CONDITIONS: 1. Does the CDT display: MPINS EXECUTING MPINS SUSPENDED BOT 2. Is RUN indicator illuminated? 3. Is the equipment one of the following? a. AA132-A or AA133-A with ST010428-1 installed or b. AA132-B or AA133-B	1	2	3	4	
	Y		N		
			N	Y	
	Y	N			
ACTIONS: 1. Go to sheet 2.	X				
2. Enter the following at the keyboard 5,9000 (CR) B,0 (CR) GO (CR)		1			
3. Go to sheet 3.		2			
4. Go to table 6-101.			2	X	
5. Replace operator's panel.			1		

Diagram 7.1

Appendix B
Switch Settings

For normal system operation, the CYBER 18 switches should be set as follows:

Breakpoint Panel

Remote/local switch in remote position

CDT

Keyboard lock switch	off	
64/96 character switch	64 position	(up)
Format switch	off	(down)
On line/local switch	on line	(up)
Char/line/block switch	char	(up)
Parity switch	even	(down)
Duplex switch	full	(up)
High/low rate switch	high	(up)

CYBER 18-20 MAINTENANCE AND TROUBLESHOOTING

LEARNING GUIDE

CONTROL DATA

Pub. No. 76770504

1/85

CONTENTS

INTRODUCTION

In this unit, you enter microprocessor operational parameter changes from the CDT keyboard, load and execute ODS tests, and isolate hardware problems in the CYBER 18-20 computer system.

Text Resources

- CYBER 18-20 Timeshare Computer System Reference Manual, volumes I, II, and III, Control Data Corporation, pub. nos. 96768681, 96768682, and 96768682.

- Systems Hardware Maintenance Manual (Reprint), Control Data Corporation, pub. no. 76361304.

Other Resources

- CDC® 110 terminal with disk drive.

- PLATO course disk ct-cpu2, Control Data Corporation, pub. no. 76773086.

__1-A PROCESSOR REGISTER ACCESS (TEXT)

In this activity, you learn how to enter changes into the processor registers and memory locations.

Objective

- Enter microprocessor operational parameter changes, and change processor register contents from the CDT keyboard.

Resource

Text/ Reading	CYBER 18-20 Maintenance and Troubleshooting Supplementary Reference Manual, "Processor Register Access (Text)," pages 1 through 11.

__1-B PROCESSOR REGISTER ACCESS (LAB)

In this activity, you enter changes into the processor registers and memory locations.

Objective

- Enter microprocessor operational parameter changes, and change processor register contents from the CDT keyboard.

Resource

Text/ Lab	CYBER 18-20 Maintenance and Troubleshooting Supplementary Reference Manual, "Processor Register Access (Lab)," pages 12 through 17.

__1-C DIAGNOSTIC LOADING AND EXECUTION (TEXT)

In this activity, you take a closer look at parts of the ODS software and operate these tests on a system.

Objective

- Load and execute ODS diagnostic tests.

Resource

Text/ Reading	CYBER 18-20 Maintenance and Troubleshooting Supplementary Reference Manual, "Diagnostic Loading and Execution (Text)," pages 18 through 32.

_1-D DIAGNOSTIC LOADING AND EXECUTION (LAB)

This activity explains how to run the ODS tests on the CYBER 18-20 system.

Objective

- Load and execute ODS diagnostic tests.

Resource

Text/ Lab	CYBER 18-20 Maintenance and Troubleshooting Supplementary Reference Manual, "Diagnostic Loading and Execution (Lab)," pages 33 through 48.
Text/ Reference	CYBER 18-20 Timeshare Computer System Reference Manual, vols. I, II, and III, or
Text/ Reference	Systems Hardware Maintenance Manual (Reprint).

_1-E SYSTEM TROUBLESHOOTING

In this activity, you practice diagnosing and isolating CYBER 18-20 system hardware problems.

Objective

- Isolate the hardware problems on the CYBER 18-20 system.

Resource

CBE	"System Troubleshooting" (PLATO course disk ct-cpu2)

_1-F REPAIR OF PROBLEMS

In this activity, you locate and isolate hardware problems in the CYBER 18-20 processor.

Objective

- Isolate the hardware problems on the CYBER 18-20 system.

Resource

Text/ Lab	CYBER 18-20 Maintenance and Troubleshooting Supplementary Reference Manual, "Repair of Problems," pages 49 through 52.

_1-G PROGRESS CHECK

At this point you should check your understanding of the material in this block by answering the progress check questions.

Resource

Text/ Exercise	CYBER 18-20 Maintenance and Troubleshooting Supplementary Reference Manual, "Progress Check," pages 53 through 55; answers, pages 56 and 57.